Military MOS Microprocessors and Peripherals

1988 Data Book

Advanced Micro Devices

Advanced General Purpose Peripherals

iAPX 86 Family

Single-Chip Microcontrollers

Z8000 Family

Advanced Micro Devices

MOS Microprocessors and Peripherals Military Data Book

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The Advanced Micro Devices MOS Microprocessors and Peripherals Military Data Book presents military versions of AMD's broad line of MOS fixed-instruction set microprocessors, peripherals, and microcontrollers. AMD has continually provided the military systems designer a complete system solution.

This document used together with AMD's MOS Microprocessors and Peripherals Data Book is your source for innovative military designs.

Today more than ever your satisfaction is essential. At Advanced Micro Devices, we bring you the quality, reliability and innovation you need from a leader in semiconductor VLSI definition, design and manufacturing. Our worldwide hardware and software support teams of field applications engineers are ready to help you utilize our advanced microprogrammable products to complete your designs in a timely and cost-effective manner.

If you have questions about any of the products described in this data book or if you'd like to know more about our product line, call your local AMD Sales office, licensed representative or franchised distributor.

George Rigg
Vice President
Processor Products Division
Advanced Micro Devices

Introduction

Advanced Micro Devices offers a broad range of military MOS and CMOS fixed-instruction-set microprocessors, peripherals and microcontrollers. These products enable the designer to build sophisticated military systems that meet the latest military quality and reliability standards.

AMD's advanced 32-bit processor, the Am29000, operating at a sustained 17 MIPS level, provides higher levels of performance and flexibility than ever before. This development will open the door to faster and more sophisticated military-system applications.

AMD is the number-one alternate source for the iAPX microprocessor family from the 8088/8086 and 80186/80188 to the high-performance 80286. Its military products are fully compatible with the latest revisions of these iAPX processors and are available in a variety of hermetic packages including DIP, PGA and LCC.

AMD offers military versions — both NMOS and CMOS — of the peripherals that support the iAPX microprocessor family. The 82C54-12/BJA is a high-performance 12-MHz CMOS part replacing the industry-standard 8254 counter/timer. High-performance proprietary advanced peripherals are available including the Am9517A-/BQA DMA Controller, the Am9513A/BQA System-Timing Controller, the Am9516A-4/BXC Advanced DMA Controller, and the industry-standard Z8530 Serial-Communication Controller.

Another family of military products offered by AMD is the popular 8051 microcontroller family. For prototyping or small-volume usage, AMD supplies military options of the 8751 — an EPROM version of the 8051. For applications where more on-chip program memory is required, the 8753 has 8 Kbytes of on-chip EPROM. For high-volume military applications, AMD offers the 80C31/BQA and 80C51/BQA — the CMOS versions of the 8031/8051. These CMOS devices are ideally suited for power-sensitive military applications because they feature idle and power-down modes for additional power conservation.

Advanced Micro Devices' goal is to qualify each of its products at the Defense Electronic Supply Center so that qualified military parts can be purchased without the burden of source-control drawings. AMD's military products are tested to the most stringent military specifications; military flows and testing are based on MIL-M-38510 and MIL-STD-883. If needed, additional testing and screening are available by special order.

For more information on these products or other AMD products, contact your nearest AMD sales office, representative or distributor.

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*DESC approved
**Pending DESC approval

NUMERICAL DEVICE LISTING

CHAPTER 1

Military Manufacturing Flows

Description of Requirements and Screens	MIL-M-38510, MIL-STD-883 Requirements Methods and Test Conditions	Requirement	Processing Level DESC	883C Class B (APL)
1. General MIL-M-38510 A. Pre-Certification B. Qualification Test Plan C. Product Assurance Program Plan	The manufacturer shall establish and implement a product-assurance program plan and qualification test plan and submit to qualifying activity.		N/A	N/A
2. Certification	DESC survey Manufacturer's Q.A. survey		N/A X	N/A X
3. Traceability	Traceability to wafer production lots		X	X
4. Country of Origin	Devices must be manufactured, assembled, and tested within U.S. or its territories.		N/A	N/A
MIL-STD-833, Method 5004 Screening				
5. Internal Visual	Method 2010 condition B	100%	X	X
6. Stabilization Bake	Method 1008 condition C	100%	X	X
7. Temperature Cycle	Method 1010 condition C (10 cycles, - 65° C to + 150° C)	100%	X	X
8. Constant Acceleration	Method 2001 condition D or E; Y1 (30 kg in Y_1 axis)	100%	X	X
9. Visual Inspection	Method 2009 4th Optical Criteria	100%	X	X
10. Hermeticity A. Fine Leak B. Gross Leak	 Method 1014 condition A or B Method 1014 condition C	 100%	 X	 X
11. Interium Electricals (initial class test)	Per manufacturers documented data sheet	100%	X	X
12. Burn-In	Method 1015, condition as specified Minimum 160 hours at 125° C	100%	X	X
13. Post Burn-In/ Final Electrical Test	25° C with 5% PDA and in-line Group A per method 5005	100%	X	X
	Data Sheet Limits at cold temperature extreme, with in-line Group A, per method 5005	100%	X	X
14. Lead Finish	A. Hot solder dip B. Gold	100%	X	X
15. Mark	Fungus inhibiting ink includes ESD and Part Nomenclature.	100%	X 5962-8552301QX + Vendor P/N	X JEDEC 101 "/BQA"

Military Manufacturing Flows (continued)

Description of Requirements and Screens	MIL-M-38510, MIL-STD-883 Requirements Methods and Test Conditions	Requirement	Processing Level DESC	883C Class B (APL)
MIL-STD-833, Method 5004 Screening (continued)				
16. Quality Conformance Inspection	Method 5005 in-line Group B	Sub-groups B1, B2, B3 B4, B5	X	X
17. Post Mark/Final Electrical Test	Data Sheet Limits at hot temperature extreme. Balance of Method 5005, in-line Group A	100%	X	X
18. Lead Scan/Straighten		AMD 07-549.1 100%	X	X
19. Hermetic Fine and Gross Leak Sample	Method 1014	AMD 06-099 Sample	X	X
20. Visual/Mechanical/ Paperwork	Method 2009	AMD 16-049 100%	X	X
21. Pack/Ship	Per MIL-M-38510, Includes C of C	AMD 16-050 100%	X	X
Quality Conformance Inspection per Method 5005 of MIL-STD-833 (attributes data only)				
22. Group A	Electrical per slash sheet or manufacturer's data sheets: sub-groups 1-11 as specified.	Each lot/ sublot	In-line	In-line
23. Group B	Package functional and constructional related test.	Each package type on each lot	In-line	In-line
24. Group C	Die related test (1,000 hour operating life).	Each micro-circuit group	Generic every 52 weeks	Generic every 52 weeks
25. Group D	Package related test.	Each package type	Generic every 52 weeks	Generic every 52 weeks

Military Ordering/Marking Information

I. MIL-STD-883C devices listed on AMD's Approved Products List are fully compliant to all provisions of paragraph 1.2.

A. Part Number: The complete part number shall be as shown in the following example:

80186	/	B	U	C
Device Type	Slash	Device Class	Case Outline	Lead Finish
(1)	(2)	(3)	(4)	(5)

1) Device type is standard generic type including considerations for revision level of die, speed requirements, or limited temperature per M38510.

2) A Slash (/) separates the device type and device class.

3) The device class is the M38510 product assurance designator, i.e., B=Class B.

4) The case outline is in accordance with Appendix C of MIL-M-38510 and listed in AMD's 09-000. See Case Outline Table.

5) The lead finish designator shall be as defined in MIL-M-38510 and documented in AMD's 16-018.1.
A = Hot Solder Dip
B = Tin Reflow
C = Gold

II. Devices listed utilizing AMD's existing nomenclature are existing products not on the APL/CPL list processed to MIL-STD-883B, Method 5004 and QCI per Method 5005.

A. The part number shall be as shown in the following example:

Am9511A	D	M	B
Device Type	Pkg	Military Temperature Range	Military Burn-in
(1)	(2)	(3)	(4)

1) Standard Generic Part

2) Package Configuration
D = Dual-in Line
L = Leadless Chip Carrier

3) Military Temperature Range Testing

4) Military Burn-in

Case Outline Table
Military Package Designators

Letter	Description
J	24-lead DIP (1/2" x 1-1/4")
Q	40-lead DIP (9/16" x 2-1/16")
U	44-terminal SQ. CCP (.650" x .650")
U	68-terminal SQ. CCP (.950" x .850")

If the case outline or case outline letter is not included in the above table, use letter:

U — For all chip carrier packages.

X — For dual-in-line packages (i.e., Cerdips and sidebraze).

Z — For all other configurations (PGAs, etc.).

CHAPTER 2

* DESC approved

Am29000

Streamlined Instruction Processor

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Full 32-bit, three-bus architecture
- 17 million instructions per second (MIPS) sustained
- 25-MHz operating frequency
- Efficient execution of high-level language programs
- CMOS technology
- 4-gigabyte virtual address space with demand paging
- Concurrent instruction and data accesses
- Burst-mode access support
- 192 general-purpose registers
- 512-byte Branch Target Cache
- 64-entry Memory-Management Unit
- De-multiplexed, pipelined address, instruction, and data buses
- Three-address instruction architecture

GENERAL DESCRIPTION

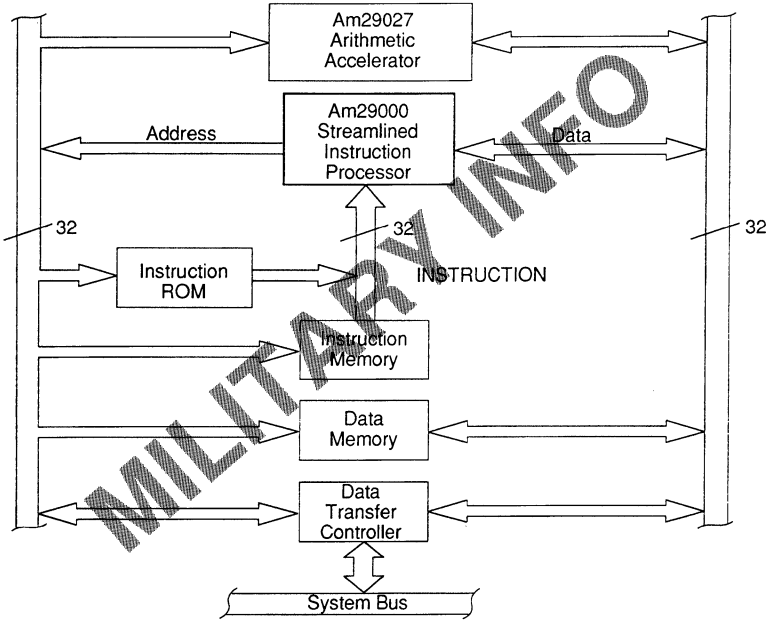
The Am29000 Streamlined Instruction Processor is a high-performance, general-purpose, 32-bit microprocessor implemented in CMOS technology. It supports a variety of applications, by virtue of a flexible architecture and rapid execution of simple instructions which are common to a wide range of tasks.

The Am29000 efficiently performs operations common to all systems, while deferring most decisions on system policies to the system architect. It is well suited for application in high-performance workstations, general-purpose super-minicomputers, high-performance real-time controllers, laser printer controllers, network protocol converters, and many other applications where high-performance, flexibility, and the ability to program using standard software tools is important.

The Am29000 instruction set has been influenced by the results of high-level-language, optimizing-compiler research. It is appropriate for a variety of languages, because it efficiently executes operations which are common to all languages. Consequently, the Am29000 is an ideal target for high-level languages such as C, Fortran, Pascal, and ADA.

The processor is packaged in a 169-terminal pin-grid-array (PGA) package, using 141 signal pins, 27 power and ground pins, and 1 alignment pin. A representative system diagram is shown below.

SIMPLIFIED SYSTEM DIAGRAM



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Publication # 09075 | Rev. A | Amendment /0
Issue Date: February 1987

Am9511A

Arithmetic Processor

MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

- 2 and 3 MHz operation; fixed point 16-bit and 32-bit operations
- Floating point 32-bit operations; binary data formats
- Add, Subtract, Multiply and Divide; trigonometric and inverse trigonometric functions
- Square roots, logarithms, exponentiation; float-to-fixed fixed-to-float conversions
- Stack-oriented operand storage; DMA or programmed I/O data transfers
- End signal simplifies concurrent processing; Synchronous/Asynchronous operations
- General purpose 8-bit data bus interface; standard 24-pin package

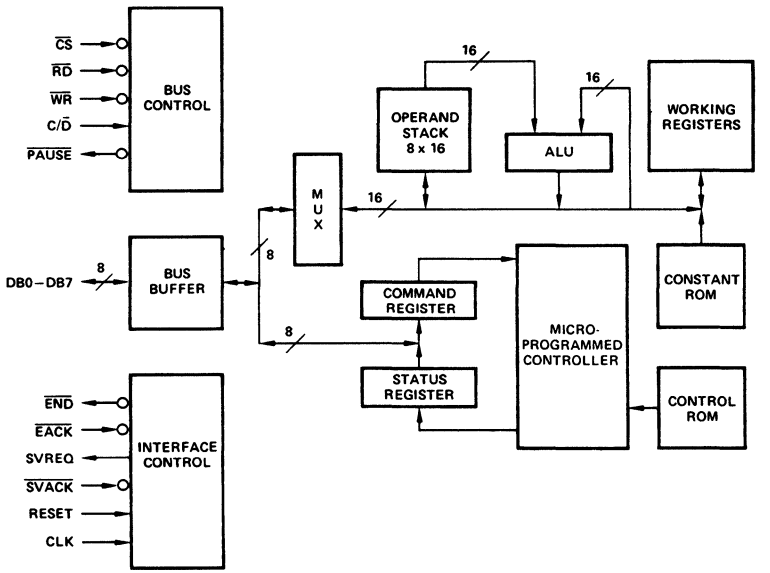
GENERAL DESCRIPTION

The Am9511A Arithmetic Processing Unit (APU) is a monolithic MOS/LSI device that provides high-performance fixed and floating point arithmetic and a variety of floating point trigonometric and mathematical operations. It may be used to enhance the computational capability of a wide variety of processor-oriented systems.

All transfers, including operand, result, status, and command information, take place over an 8-bit bidirectional data bus. Operands are pushed onto an internal stack, and a command is issued to perform operations on the data in the stack. Results are then available to be retrieved from the stack, or additional commands may be entered.

Transfers to and from the APU may be handled by the associated processor using conventional programmed I/O, or may be handled by a direct memory access controller for improved performance. Upon completion of each command, the APU issues an end-of-execution signal that may be used as an interrupt by the CPU to help coordinate program execution.

BLOCK DIAGRAM



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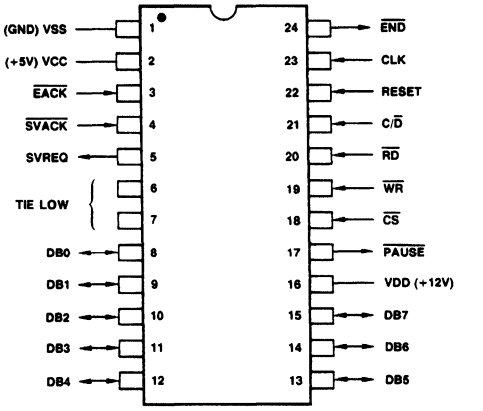
Publication # 09224 Rev. A Amendment /0
Issue Date: December 1987

CONNECTION DIAGRAM
Top View



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Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

NPL Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM9511A — –1 — D — M — B

e. OPTIONAL PROCESSING
B = Burn-in

d. TEMPERATURE RANGE
M = Military* (–55 to +125°C)

c. PACKAGE TYPE
D = 24-Pin Ceramic DIP (CD 024)

b. SPEED OPTION
Blank = 2 MHz
–1 = 3 MHz

a. DEVICE NUMBER/DESCRIPTION
Am9511A
Arithmetic Processor

Valid Combinations	
AM9511A	DMB
AM9511A-1	

*Military or Limited Military temperature range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
V_{DD} with Respect to V_{SS} ..... −0.5 V to +15.0 V
V_{CC} with Respect to V_{SS} ..... −0.5 V to +7.0 V
All Signal Voltages
with Respect to V_{SS} ..... −5.0 V to +7.0 V
Power Dissipation (Package Limitation) ..... 2.0 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... 5 V ±10%
(V_{DD}) ..... 12 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range

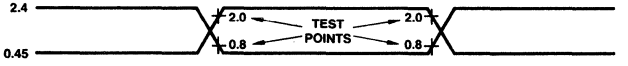
Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -200\ \mu A$	3.7		V
V_{OL}	Output LOW Voltage	$I_{OL} = 3.2$ mA		0.4	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC}*	V
V_{IL}	Input LOW Voltage		−0.5*	0.8	V
I_{IX}	Input Load Current	$V_{SS} \leq V_I \leq V_{CC}$		±10	μA
I_{OZ}	Data Bus Leakage	$V_O = 0.4$ V	10		μA
		$V_O = V_{CC}$		10	
I_{CC}	V_{CC} Supply Current			100	mA

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_O	Output Capacitance	$f_C = 1.0$ MHz, Inputs = 0 V		10*	pF
C_I	Input Capacitance			8*	pF
C_{IO}	I/O Capacitance			12*	pF

*Not tested; guaranteed by design.

SWITCHING TEST INPUT WAVEFORM



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See Section 6 of the MOS Microprocessors and Peripherals Data Book (Order #09067A) for Thermal Characteristics Information.

SWITCHING CHARACTERISTICS over operating range

Parameter Symbol	Parameter Description		Am9511A Min.	Am9511A Max.	Am9511A-1 Min.	Am9511A-1 Max.	Unit
TAPW	$\overline{EACK}$ LOW Pulse Width		100		75		ns
TCDR	C/$\overline{D}$ to $\overline{RD}$ LOW Setup Time		0		0		ns
TCDW	C/$\overline{D}$ to $\overline{WR}$ LOW Setup Time		0		0		ns
TCPH	Clock Pulse HIGH Width		200		140		ns
TCPL	Clock Pulse LOW Width		240		160		ns
TCSR	$\overline{CS}$ LOW to $\overline{RD}$ LOW Setup Time		0		0		ns
TCSW	$\overline{CS}$ LOW to $\overline{WR}$ LOW Setup Time		0		0		ns
TCY	Clock Period		480	5000	320	3300	ns
TDW	Data Bus Stable to $\overline{WR}$ HIGH Setup Time		150		150		ns
TEAE	$\overline{EACK}$ LOW to $\overline{END}$ HIGH Delay			200		175	ns
TEPW	$\overline{END}$ LOW Pulse Width (Note 4)		400		270		ns
TOP	Data Bus Output Valid to $\overline{PAUSE}$ HIGH Delay		0		0		ns
TPPWR	$\overline{PAUSE}$ LOW Pulse Width Read (Note 5)	Data	3.5TCY + 50	5.5TCY + 300	3.5TCY + 50	5.5TCY + 200	ns
		Status	1.5TCY + 50	3.5TCY + 300	1.5TCY + 50	3.5TCY + 200	
TPPWW	$\overline{PAUSE}$ LOW Pulse Width Write (Note 8)			50		50	ns
TPR	$\overline{PAUSE}$ HIGH to $\overline{RD}$ HIGH Hold Time		0		0		ns
TPW	$\overline{PAUSE}$ HIGH to $\overline{WR}$ HIGH Hold Time		0		0		ns
TRCD	$\overline{RD}$ HIGH to C/$\overline{D}$ Hold Time		0		0		ns
TRCS	$\overline{RD}$ HIGH to $\overline{CS}$ HIGH Hold Time		0		0		ns
TRO	$\overline{RD}$ LOW to Data Bus ON Delay		50		50		ns
TRP	$\overline{RD}$ LOW to $\overline{PAUSE}$ LOW Delay (Note 6)			150		150	ns
TRZ	$\overline{RD}$ HIGH to Data Bus OFF Delay		50	200	50	150	ns
TSAPW	$\overline{SVACK}$ LOW Pulse Width		100		75		ns
TSAR	$\overline{SVACK}$ LOW to SVREQ LOW Delay			300		200	ns
TWCD	$\overline{WR}$ HIGH to C/$\overline{D}$ Hold Time		60		30		ns
TWCS	$\overline{WR}$ HIGH to $\overline{CS}$ HIGH Hold Time		60		30		ns
TWD	$\overline{WR}$ HIGH to Data Bus Hold Time		20		20		ns
TWI	Write Inactive Time	Command	4TCY		4TCY		ns
		Data	5TCY		5TCY		
TWP	$\overline{WR}$ LOW to $\overline{PAUSE}$ LOW Delay (Note 6)			150		150	ns

Notes:
1. Typical values are for T_A = 25°C, nominal supply voltages and nominal processing parameters.
2. Switching parameters are listed in alphabetical order.
3. Test conditions assume transition times of 20 ns or less, output loading of one TTL gate plus 100 pF ±20 pF and timing reference levels of 0.8 V and 2.0 V.
4. $\overline{END}$ low pulse width is specified for $\overline{EACK}$ tied to V_{SS}. Otherwise TEAE applies.
5. Minimum values shown assume no previously entered command is being executed for the data access. If a previously entered command is being executed, $\overline{PAUSE}$ LOW Pulse Width is the time to complete execution plus the time shown. Status may be read at any time without exceeding the time shown.
6. $\overline{PAUSE}$ is pulled low for both command and data operations.
7. TEX is the execution time of the current command (see the Command Execution Times table).
8. $\overline{PAUSE}$ low pulse width is less than 50 ns when writing into the data port or the control port as long as the duty requirement (TWI) is observed and no previous command is being executed. TWI may be safely violated up to 500 ns as long as the extended TPPWW that results is observed. If a previously entered command is being executed, $\overline{PAUSE}$ LOW Pulse Width is the time to complete execution plus the time shown.

Am9513A

System Timing Controller

MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

- SMD/DESC qualified
- Five independent 16-bit counters
- High speed counting rates
- Up/down and binary/BCD counting
- Internal oscillator frequency source
- Tapped frequency scaler
- Programmable frequency output
- 8-bit or 16-bit bus interface
- Time-of-day option
- Alarm comparators on counters 1 and 2
- One-shot or continuous outputs
- Programmable count/gate source selection
- Programmable input and output polarities
- Programmable gating functions
- Retriggering capability
- Standard 40-pin DIP package; 44-Pin LCC

GENERAL DESCRIPTION

The Am9513A System Timing Controller is an LSI circuit designed to service many types of counting, sequencing and timing applications. It provides the capability for programmable frequency synthesis, high resolution programmable duty cycle waveforms, retriggerable digital one-shots, time-of-day clocking, coincidence alarms, complex pulse generation, high resolution baud rate generation, frequency shift keying, stop-watching timing, event count accumulation, waveform analysis, etc. A variety of programmable operating modes and control features allow the Am9513A to be personalized for particular applications as well as dynamically reconfigured under program control.

The STC includes five general-purpose 16-bit counters. A variety of internal frequency sources and external pins may be selected as inputs for individual counters with software selectable active-high or active-low input polarity. Both hardware and software gating of each counter is available. Three-state outputs for each counter provide pulses or levels and can be active-high or active-low. The counters can be programmed to count up or down in either binary or BCD. The host processor may read an accumulated count at any time without disturbing the counting process. Any of the counters may be internally concatenated to form any effective counter length up to 80 bits.

BLOCK DIAGRAM

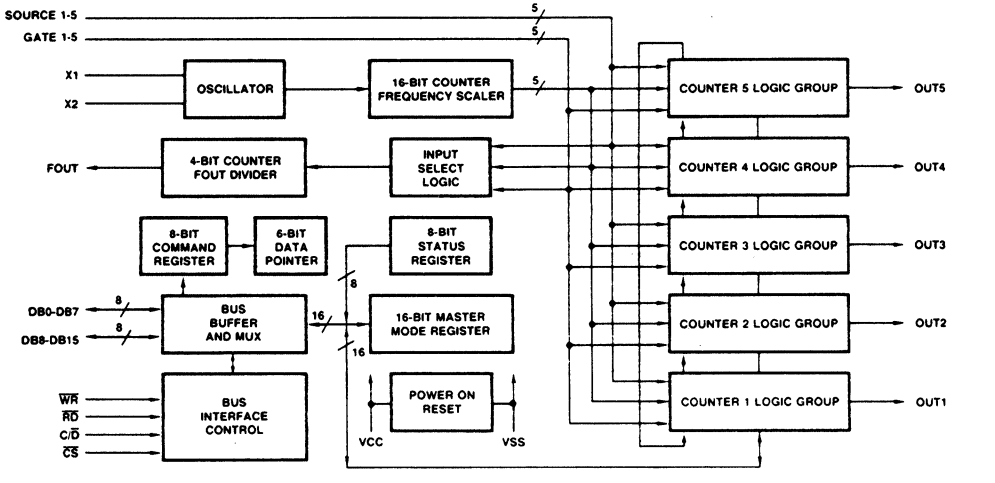

Figure 1-1.

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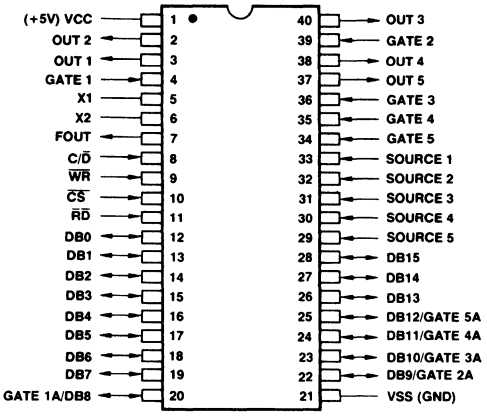
Issue Date: November 1987

CONNECTION DIAGRAMS
Top View

AAB6B

DIPs



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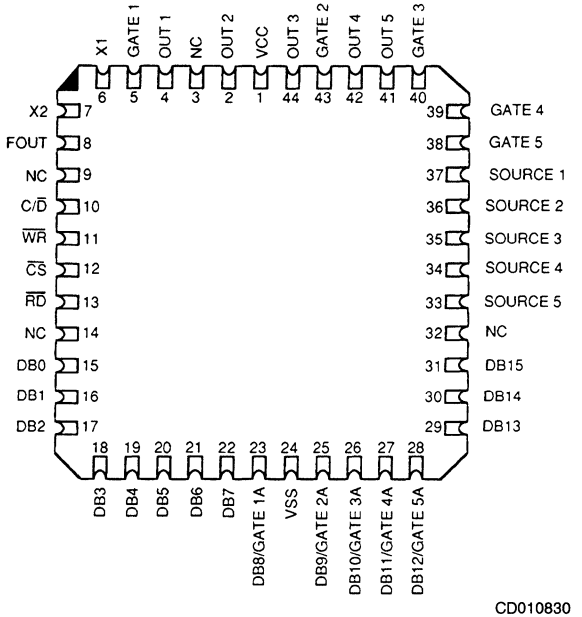
Note: Pin 1 is marked for orientation.

LCC



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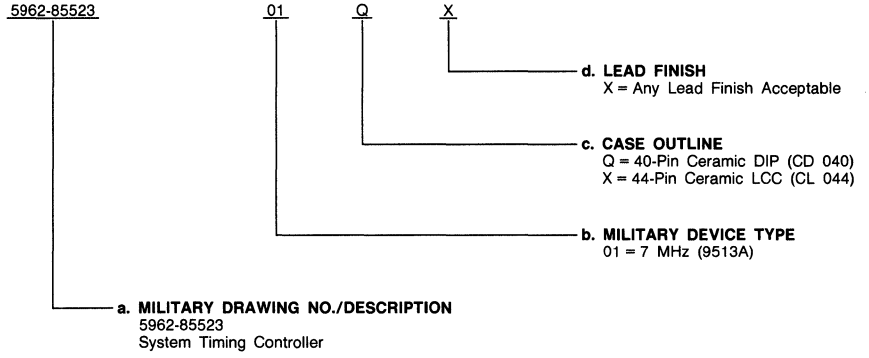
MILITARY ORDERING INFORMATION

Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of: **a. Military Drawing Part Number**
b. Device Type
c. Case Outline
d. Lead Finish



Valid Combinations	
5962-8552301	QX, XX

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

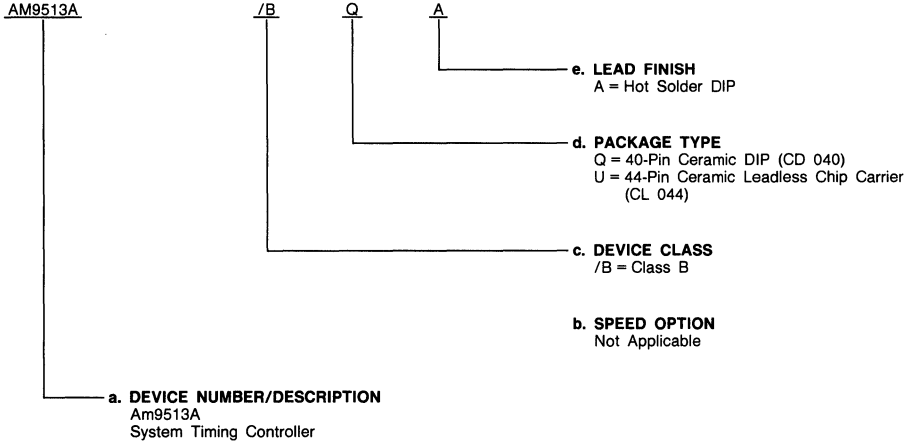
Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

MILITARY ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM9513A	/BQA, /BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of
Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
VCC with Respect to VSS ..... −0.5 V to +7.0 V
All Signal Voltages
with Respect to VSS ..... −0.5 V to +7.0 V
Power Dissipitation (Package Limitation) ..... 1.5 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... 5 V ±5%

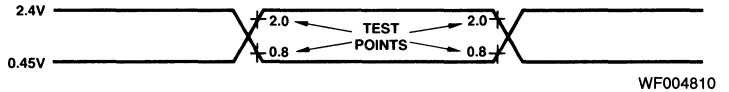
Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

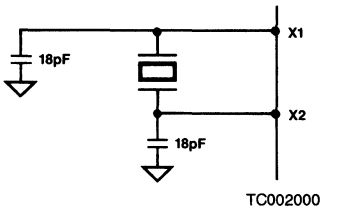
Parameter Symbol	Parameter Description		Test Conditions	Min.	Max.	Unit
VIL	Input Low Voltage	All Inputs Except X2		VSS − 0.5*	0.8	V
		X2 Input		VSS − 0.5*	0.8	
VIH	Input High Voltage	All Input Except X2		2.2 V	VCC*	V
		X2 Input		3.8	VCC*	
VITH	Input Hysteresis (SRC and GATE Inputs Only)			0.2		V
VOL	Output Low Voltage		IOL = 3.2 mA		0.4	V
VOH	Output High Voltage		IOH = −200 µA	2.4		V
IIX	Input Load Current (Except X2)		VSS ≤ VIN ≤ VCC		±10	µA
IIX	Input Load Current X2		VSS ≤ VIN ≤ VCC		±100	µA
IOZ	Output Leakage Current (Except X1)		VSS + 0.4 ≤ VOUT ≤ VCC High-Impedance State		±25	µA
ICC	VCC Supply Current (Steady State)				275	mA
CIN †	Input Capacitance		f = 1 MHz, T_C = +25°C. All pins not under test at 0 V.		20*	pF
COUT †	Output Capacitance				20*	
CIO †	IN/OUT Capacitance				20*	

* Guaranteed by design; not tested.
† Not included in Group A tests.

SWITCHING TEST INPUT/OUTPUT WAVEFORMS



WF004810



TC002000

Crystal is fundamental mode parallel resonant 32 pF load capacitance less than 100 Ω ESR C_o less than 100 pF.

SWITCHING CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description		Am9513A Min.	Am9513A Max.	Unit
TAVRL	C/$\overline{D}$ Valid to Read Low		25		ns
TAVWH	C/$\overline{D}$ Valid to Write High		170		ns
TCHCH	X2 High to X2 High (X2 Period) (Note 13)		145		ns
TCHCL	X2 High to X2 Low (X2 High Pulse Width) (Note 13)		70		ns
TCLCH	X2 Low to X2 High (X2 Low Pulse Width) (Note 13)		70		ns
TDVWH	Data In Valid to Write High		80		ns
TEHEH	Count Source High to Count Source High (Source Cycle Time) (Note 7)		145		ns
TEHEL TELEH	Count Source Pulse Duration (Note 7)		70		ns
TEHFV	Count Source High to FOUT Valid (Note 7)			500	ns
TEHGV	Count Source High to Gate Valid (Level Gating Hold Time) (Notes 7, 9, 10)		10		ns
TEHRL	Count Source High to Read Low (Set-up Time) (Notes 2, 7)		190		ns
TEHWH	Count Source High to Write High (Set-up Time) (Notes 3, 7)		-100		ns
TEHYV	Count Source High to Out Valid (Note 7)	TC Output		300	ns
		Immediate or Delayed Toggle Output		300	
		Comparator Output		350	
TFN	FN High to FN + 1 Valid (Note 11)			75	ns
TGVEH	Gate Valid to Count Source High (Level Gating Set-up Time) (Notes 7, 9, 10)		100		ns
TGVGV	Gate Valid to Gate Valid (Gate Pulse Duration) (Notes 8, 10)		145		ns
TGVWH	Gate Valid to Write High (Notes 3, 10)		-100		ns
TRHAX	Read High to C/$\overline{D}$ Don't Care		0		ns
TRHEH	Read High to Count Source High (Notes 4, 7)		0		ns
TRHQX	Read High to Data Out Invalid		10		ns
TRHQZ	Read High to Data Out at High-Impedance (Data Bus Release Time)			85	ns
TRHRL	Read High to Read Low (Read Recovery Time)		1000		ns
TRHSH	Read High to $\overline{CS}$ High (Note 12)		0		ns
TRHWL	Read High to Write Low (Read Recovery Time)		1000		ns
TRLQV	Read Low to Data Out Valid			110	ns
TRLQX	Read Low to Data Bus Driven (Data Bus Drive Time)		20		ns
TRLRH	Read Low to Read High (Read Pulse Duration) (Note 12)		160		ns
TSLRL	$\overline{CS}$ Low to Read Low (Note 12)		20		ns
TSLWH	$\overline{CS}$ Low to Write High (Note 12)		170		ns
TWHAX	Write High to C/$\overline{D}$ Don't Care		20		ns
TWHDX	Write High to Data In Don't Care		20		ns
TWHEH	Write High to Count Source High (Notes 5, 7, 14, 15)		550		ns
TWHGV	Write High to Gate Valid (Notes 5, 10, 14)		475		ns
TWHRL	Write High to Read Low (Write Recovery Time) (Note 16)		1500		ns
TWHSH	Write High to $\overline{CS}$ High (Note 12)		20		ns
TWHWL	Write High to Write Low (Write Recovery Time) (Note 16)		1500		ns
TWHYV	Write High to Out Valid (Notes 6, 14)			650	ns
TWLWH	Write Low to Write High (Write Pulse Duration) (Note 12)		150		ns
TGVEH2	Gate Valid to Count Source High (Special Gate) (Notes 10, 13, 17)		200		ns
TEHGV2	Count Source High to Gate Valid (Special Gate) (Notes 10, 13, 18)		80		ns

Notes:

1. Abbreviations used for the switching parameter symbols are given as the letter T followed by four or five characters. The first and third characters represent the signal names on which the measurements start and end. Signal abbreviations used are:

   A (Address) = C/$\overline{D}$
   C (Clock) = X2
   D (Data In) = DB0-DB15
   E (Enabled counter source input) = SRC1-SRC5, GATE1-GATE5, F1-F5,TCN-1
   F = FOUT
   G (Counter gate input) = GATE1-GATE5, TCN-1
   Q (Data Out) = DB0-DB15
   R (Read) = $\overline{RD}$
   S (Chip Select) = $\overline{CS}$
   W (Write) = $\overline{WR}$
   Y (Output) = OUT1-OUT5

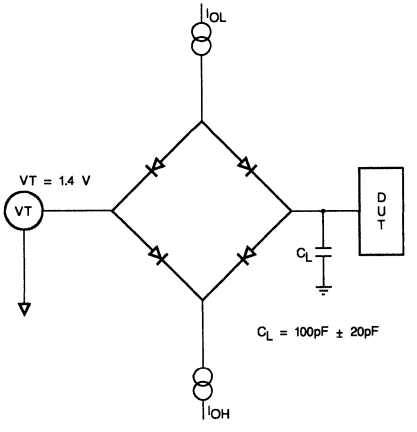
— Continued on next page —

The second and fourth letters designate the reference states of the signals named in the first and third letters respectively, using the following abbreviations.

H = HIGH
L = LOW
V = VALID
X = Unknown or Don't care
Z = High-Impedance

2. Any input transition that occurs before this minimum setup requirement will be reflected in the contents read from the status register.
3. Any input transition that occurs before this minimum setup requirement will act on the counter before the execution of the operation initiated by the write and the counter may be off by one count.
4. Any input transition that occurs after this minimum hold time is guaranteed to not influence the contents read from the status register on the current read operation.
5. Any input transition that occurs after this minimum hold time is guaranteed to be seen by the counter as occurring after the action initiated by the write operation and the counter may be off by one count.
6. This parameter applies to cases where the write operation causes a change in the output bit.
7. The enabled count source is one of F1-F5, TCN-1 SRC1-SRC5 or GATE1-GATE 5, as selected in the applicable Counter Mode register. The timing diagram assumes the counter counts on rising source edges. The timing specifications are the same for falling-edge counting.
8. This parameter applies to edge gating (CM15-CM13 = 110 or 111) and gating when both CM7 = 1 and CM15-CM13 ≠ 000. This parameter represents the minimum GATE pulse width needed to ensure that the pulse initiates counting or counter reloading.
9. This parameter applies to both edge and level gating (CM15-CM13 = 001 through 111 and CM7 = 0). This parameter represents the minimum setup or hold times to ensure that the Gate input is seen at the intended level on the active source edge and the counter may be off by one count.
10. This parameter assumes that the GATENA input is unused (16-bit bus mode) or is tied high. In cases where the GATENA input is used, this timing specification must be met by both the GATE and GATENA inputs.
11. Signals F1-F5 cannot be directly monitored by the user. The phase difference between these signals will manifest itself by causing counters using two different F signals to count at different times on nominally simultaneous transitions in the F signals. F1 = X2.
12. This timing specification assumes that $\overline{CS}$ is active whenever $\overline{RD}$ or $\overline{WR}$ are active. $\overline{CS}$ may be held active indefinitely.
13. This parameter assumes X2 is driven from an external gate with a square wave.
14. This parameter assumes that the write operation is to the command register.
15. This timing specification applies to single-action commands only (e.g., LOAD, ARM, SAVE, etc.). For double-action commands such as LOAD AND ARM and DISARM AND SAVE, TWHEH minimum = 700 ns.
16. In short data write mode, TWHRL and TWHWL minimum = 1000 ns.
17. This parameter applies to the hardware retrigger/save modes N, O, Q, R, and X (CM7 = 1 and CM15-CM13 < > 000). This parameter ensures that the gating pulse initiates a hardware retrigger/save operation.
18. This parameter applies to hardware load source select modes S and V (CM7 = 1 and CM15-CM13 = 000). This parameter represents the minimum hold time to ensure that the GATE input selects the correct load source on the active source edge.

SWITCHING TEST CIRCUIT



TC003853

This test circuit is the dynamic load of a Teradyne J941.

Am9516A

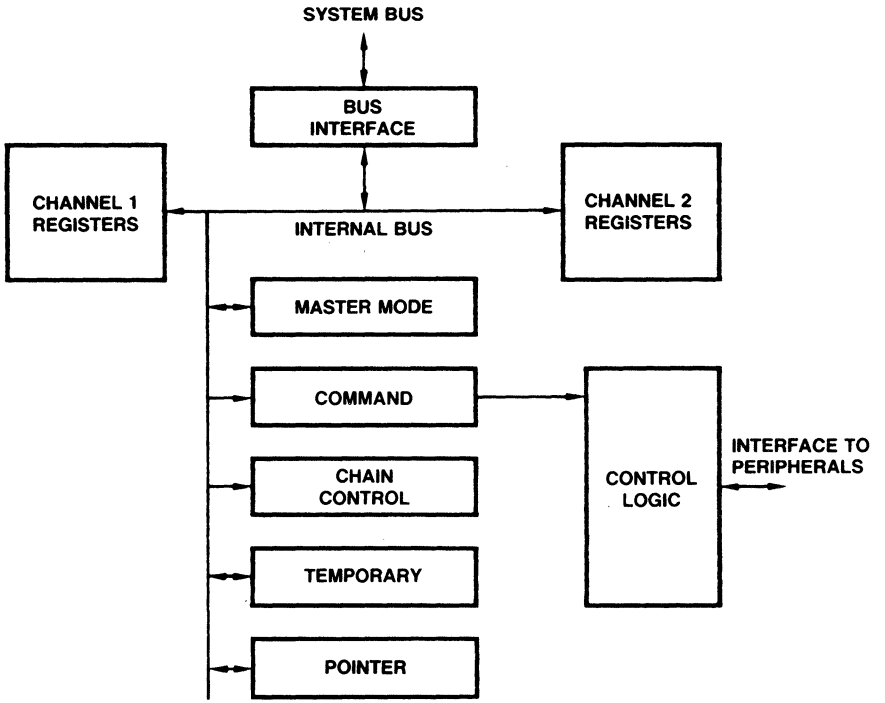
Universal DMA Controller (UDC)

MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

- Transfer Modes: single, demand dedicated with bus hold, demand dedicated with bus release, demand interleave
- 16 Megabyte physical addressing range
- Automatic loading/reloading of control parameters by each channel
- Optional automatic chaining of operations
- Channel interleave operations
- Interleave operations with system bus
- Masked data pattern matching for search operations
- Vectored interrupts on selected transfer conditions
- Software DMA request
- Software or hardware wait-state insertion
- Transfer up to 6.66 Mbytes/second at 10 MHz clock

BLOCK DIAGRAM



BD003830

Publication # 09226 | Rev. A | Amendment /0
Issue Date: November 1987

GENERAL DESCRIPTION

The Am9516A Universal DMA Controller (UDC) is a high-performance peripheral interface circuit for 8086 and 68000 CPUs. In addition to providing data block transfer capability between memory and peripherals, each of the UDC's two channels can perform peripheral-to-peripheral, as well as memory-to-memory transfer. A special Search Mode of Operation compares data read from a memory or peripheral source to the content of a pattern register.

For all DMA operations (search, transfer, and transfer-and-search), the UDC can operate with either byte or word data sizes. In some system configurations it may be necessary to transfer between word-organized memory and a byte-oriented peripheral. The UDC provides a byte packing/unpacking capability through its byte-word funneling transfer or transfer-and-search option. Some DMA applications may continuously transfer data between the same two memory areas. These applications may not require the flexibility inherent in reloading registers from memory tables. To service these repetitive DMA operations, base registers are provided on each channel which re-initialize the current source and destination Address and Operation Count registers. To change the data transfer direction under CPU control, provision is made for reassigning the source address as a destination and the destination as a source, eliminating the need for actual reloading of these address registers.

Frequently, DMA devices must interface to slow peripherals or slow memory. In addition to providing a hardware $\overline{WAIT}$ input, the Am9516A UDC allows the user to select independently for both source and destination addresses and automatic insertion of 0, 1, 2 or 4 wait states. The user may even disable the $\overline{WAIT}$ input pin function altogether and use these software-programmed wait states exclusively.

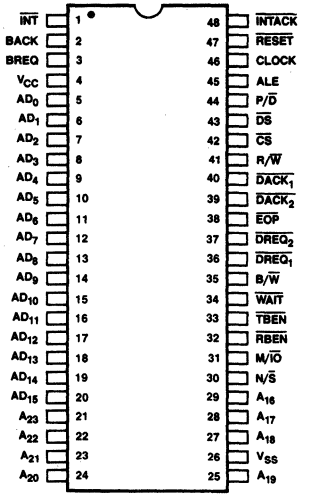
High throughput and powerful transfer options are of limited usefulness if a DMA requires frequent reloading by the host CPU. The Am9516A UDC minimizes CPU interactions by allowing each channel to load its control parameters from memory into the channel's control registers. The only action required of the CPU is to load the address of the control parameter table into the channel's Chain Address register and then issue a "Start Chain" Command to start the register loading operation.

The Am9516A UDC is packaged in a 48-pin DIP and uses a single +5 V power supply.

CONNECTION DIAGRAM

Top View

DIP



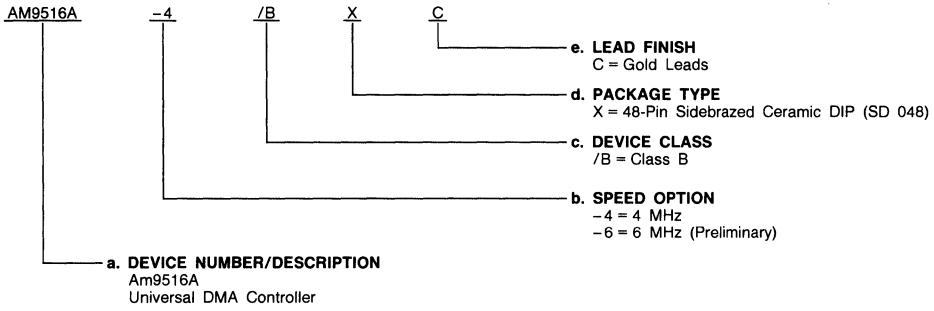
CD005592

Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM9516A-4	/BXC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
V_{CC} with Respect to V_{SS} ..... −0.5 to +7.0 V
All Signal Voltages with Respect to V_{SS} .. −0.5 to +7.0 V

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to 125°C
Supply Voltage (V_{CC}) ..... 5 V ± 10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

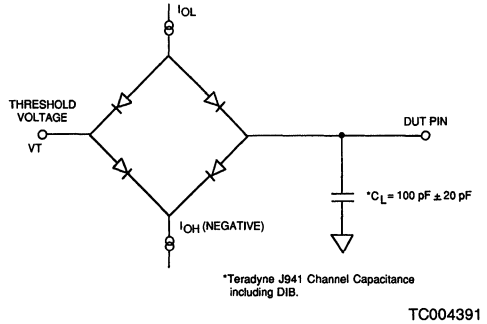
Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{CH} †	Clock Input HIGH Voltage	Driven by External Clock Generator	3.8	V_{CC} +0.3*	V
V_{CL} †	Clock Input LOW Voltage	Driven by External Clock Generator	−0.5*	0.45	V
V_{IH1} †	Input HIGH Voltage	All Pins Except 2, 36, 37, 38, 47, 48	2.0	V_{CC} +0.3*	V
V_{IH2} †	Input HIGH Voltage	Pins 2, 36, 37, 38, 47, 48	2.2	V_{CC} +0.3*	V
V_{IL} †	Input LOW Voltage		−0.5*	0.8	V
V_{OH1}	Output HIGH Voltage	I_{OH} = −250μA Except Pins 1, 32, 33, 38	2.4		V
V_{OH2}	Output HIGH Voltage	I_{OH} = −200 μA, Pins 1, 32, 33, 38	2.0		V
V_{OL}	Output LOW Voltage	I_{OL} = 3.2 mA		0.45	V
I_{IL}	Input Leakage	$V_{SS} \leq V_{IN} \leq V_{CC}$		±10	μA
I_{OL}	Output Leakage	$V_{SS} \leq V_{OUT} \leq V_{CC}$		±10	μA
I_{CC}	V_{CC} Supply Current	T_C = −55°C		350	mA
		T_C = +125°C		200	mA
C_{CLK} ††	Input Capacitance (Clock)	Unmeasured pins returned to ground. f = 1 MHz over specified temperature range.		25*	pF
C_{IN} ††	Input Capacitance (Except Pin 46)	Unmeasured pins returned to ground. f = 1MHz over specified temperature range.		10*	pF
C_{OUT} ††	Output Capacitance			15*	pF
$C_{I/O}$ ††	Bidirectional Capacitance			20*	pF

* Guaranteed by design; not tested.
† Group A, Subgroups 9, 10, and 11 only are tested.
†† Not included in Group A tests.

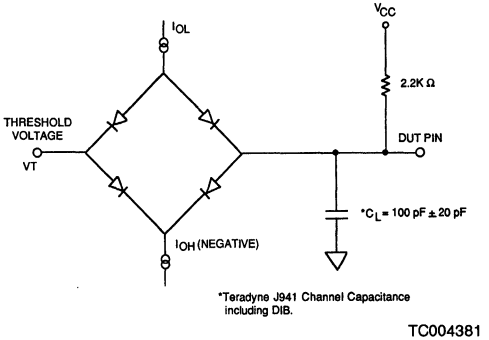
Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

+4.75 ≤ V_{CC} ≤ +5.25 V
GND = 0 V
−55 ≤ T_C ≤ +125°C

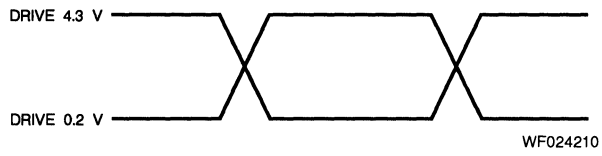


A. Standard Dynamic Load

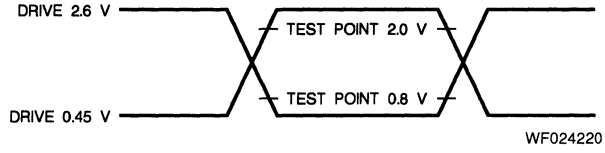


B. Open-Drain Dynamic Load

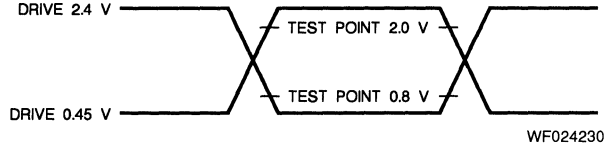
SWITCHING TEST WAVEFORMS



A. External CLOCK Generator



B. BACK, $\overline{\text{DREQ1}}$, $\overline{\text{DREQ2}}$, $\overline{\text{RESET}}$, $\overline{\text{INTACK}}$, and $\overline{\text{EOP}}$ only



C. ALL pins except BACK, $\overline{\text{DREQ1}}$, $\overline{\text{DREQ2}}$, $\overline{\text{RESET}}$, $\overline{\text{INTACK}}$, and $\overline{\text{EOP}}$.

SWITCHING CHARACTERISTICS over operating range (for APL Products, Subgroups 9, 10, 11 are tested unless otherwise noted)

TIMING FOR UDC AS BUS MASTER

No.	Parameter Symbol	Parameter Description	4 MHz		Preliminary 6 MHz		Unit
			Min.	Max.	Min.	Max.	
1	TcC	Clock Cycle Time	250	2000	165	2000	ns
2	TwCh	Clock Width (HIGH)	105	1000	70	1000	ns
3	TwCl	Clock Width (LOW)	105		70		ns
4	TfC	Clock Fall Time		20		10	ns
5	TrC	Clock Rise Time		20		15	ns
6	TdC(AUv)	Clock RE to Upper Address (A_{16}-A_{23}) Valid Delay		90		80	ns
7	ThC(AUv)	Clock RE to Upper Address Valid Hold Time	5		5		ns
8	TdC(ST)	Clock RE to R/$\overline{W}$ and B/$\overline{W}$ Valid Delay		110		90	ns
9	TdC(A)	Clock RE to Lower Address (A_0-A_{15}) Valid Delay		90		90	ns
10	TdC(Az)	Clock RE to Lower Address (A_0-A_{15}) Float Delay		60		60	ns
11	TdC(ALr)	Clock RE to ALE RE Delay		70		60	ns
12	TdC(AL)	Clock FE to ALE FE Delay		70		60	ns
13	TdC(DS)	Clock RE to $\overline{DS}$ (Read) FE Delay		60		60	ns
14	TdC(DSf)	Clock FE to $\overline{DS}$ (Write) FE Delay		60		60	ns
15	TdC(DSr)	Clock FE to $\overline{DS}$ RE Delay		60		60	ns
16	TdC(DO)	Clock RE to Data Out Valid Delay		90		90	ns
17	TsDI(C)	Data in to Clock FE Setup Time	20		15		ns
18	TdA(AL)	Address Valid to ALE FE Delay	50		35		ns
19	ThAL(A)	ALE FE to Lower Address Valid Hold Time	60		40		ns
20	TwAL	ALE Width (HIGH)	80		60		ns
21	TdAz(DS)	Lower Address Float to $\overline{DS}$ LOW Delay	0		0		ns
22	TdAL(DS)	ALE FE to $\overline{DS}$ (Read) FE Delay	75		35		ns
23	TdAL(DI)	ALE FE to Data in Required Valid Delay		300		215	ns
24	TdA(DI)	Address Valid to Data in Required Valid Delay		410		305	ns
25	TdDS(A)	$\overline{DS}$ RE to Address Active Delay	80		45		ns
26	TdDS(AI)	$\overline{DS}$ RE to ALE RE Delay	75		40		ns
27	TdA(DS)	Address Valid to $\overline{DS}$ (Read) FE Delay	160		110		ns
28	TdDO(DSr)	Data Out Valid to $\overline{DS}$ RE Delay	230		150		ns
29	TdDO(DSf)	Data Out Valid to $\overline{DS}$ FE Delay	55		35		ns
30	ThDS(DO)	$\overline{DS}$ RE to Data Out Valid Hold Time	85		45		ns
31	TdDS(DI)	$\overline{DS}$ (Read) FE to Data in Required Valid Delay		205		155	ns
33	ThDI(DS)	$\overline{DS}$ RE to Data in Hold Time	0		0		ns
34	TwDSmw	$\overline{DS}$ (Write) Width (LOW)	185		110		ns
35	TwDSmr	$\overline{DS}$ (Read) Width (LOW)	275		220		ns
36	TdC(RBr)	Clock FE to $\overline{RBEN}$ RE Delay*		70		65	ns
37	ThDS(ST)	$\overline{DS}$ RE to B/$\overline{W}$, N/$\overline{S}$, R/$\overline{W}$ and M/$\overline{IO}$ Valid Hold Time	70		45		ns
38	TdC(TRf)	Clock RE to $\overline{TBEN}$ or $\overline{RBEN}$ FE Delay		60		60	ns
39	TdC(TRr)	Clock RE to $\overline{TBEN}$ RE Delay		60		60	ns
40	TdC(ST)	Clock RE to M/$\overline{IO}$ and N/$\overline{S}$ Valid Delay		90		75	ns
41	TdS(AL)	R/$\overline{W}$, M/$\overline{IO}$, B/$\overline{W}$ and N/$\overline{S}$ Valid to ALE FE Delay	60		35		ns
42	TsWT(C)	$\overline{WAIT}$ to Clock FF Setup Time	20		20		ns
43	ThWT(C)	$\overline{WAIT}$ to Clock FE Hold Time	20		20		ns
44	TwDRQ	$\overline{DREQ}$ Pulse Width (Single Transfer Mode)	20		20		ns
45	TsDRQ(C)	$\overline{DREQ}$ Valid to Clock RE Setup Time	60		50		ns
46	ThDRQ(C)	Clock RE to $\overline{DREQ}$ Valid Hold Time	20		20		ns
47	TdC(INTf)	Clock FE to $\overline{INT}$ FE Delay		150		150	ns

*These must not occur simultaneously.
Note: RE = rising edge
FE = falling edge

Am9516A CLOCK-CYCLE-TIME-DEPENDENT CHARACTERISTICS

The parameters listed below are also shown in the Switching specification. However, they are dependent on the actual values of the clock periods. The equations below define that dependence so that the exact limit for these parameters may be determined for any given system in relation to its specific clock characteristics.

Number	Parameters	Derivation
18	TdA (AL)	0.5TcC – #9 + (#12 – tr)
19	ThAL (A)	0.5TcC – #12 (ALE FE @ 0.8V) + #10
21	TdAz (DS)	#13 – #10
22	TdAL (DS)	0.5TcC – #12 + #13
23	TdAL (DI)	2TcC – #12 – #17
24	TdA (DI)	2.5TcC – #9 – #17
25	TdDS (A)	0.5TcC – #15 + #9
26	TsDS (AL)	0.5TcC – #15 + #11 (ALE RE)
27	TdA (DS)	TcC – #9 + #13
28	TdDO (DSr)	1.5TcC – #16 + #15
29	TdDO (DSf)	0.5TcC – #16 + #14
30	ThDS (DO)	0.5TcC – #15 + #32
31	TdDS (DI)	1.5TcC – #13 – #17
34	TwDSmw	TcC – #14 + #15
35	TwDSmr	1.5TcC – #13 + #15
37	ThDS (ST)	0.5TcC – #15 + (#40 – tr)
41	TdS (AL)	0.5TcC – #40 + (#12 – tr)

Note: tr (nominal) = 10 ns
#32 CLCK RE to Data Out Not Valid Delay = 20 ns (4 and 6 MHz)

SWITCHING CHARACTERISTICS (Cont'd.)
UDC AS BUS SLAVE BUS EXCHANGE

			Preliminary				
			4 MHz		6 MHz		
No.	Parameter Symbol	Parameter Description	Min.	Max.	Min.	Max.	Unit
61	TdIN(DO)	$\overline{INTACK}$ FE to Data Output Valid Delay		135		135	ns
62	TdIN(DOz)	$\overline{INTACK}$ RE to Data Output Float Delay		80		80	ns
63	TdDS(DO)	$\overline{DS}$ FE (IOR) to Data Output Driven Delay		135*		135	ns
64	TdDS(DOz)	$\overline{DS}$ RE (IOR) to Data Output Float Delay		80		80	ns
65	TsDI(DS)	Data Valid to $\overline{DS}$ RE (IOW) Setup Time	40		40		ns
66	ThDS(DI)	$\overline{DS}$ RE (IOW) to Data Valid Hold Time	40		30		ns
67	TwDS	$\overline{DS}$ LOW Width	150*		150*		ns
68	TwIN	$\overline{INTACK}$ LOW Width	150		150		ns
69	ThDS(CS)	$\overline{DS}$ RE to $\overline{CS}$ Valid Hold Time	20		20		ns
70	ThDS(PD)	$\overline{DS}$ RE to P/$\overline{D}$ Valid Hold Time	20		20		ns
71	TsPD(DS)	P/$\overline{D}$ Valid to $\overline{DS}$ FE Setup Time (IOR)	10		10		ns
		P/$\overline{D}$ Valid to $\overline{DS}$ FE Setup Time (IOW)	50		50		
72	TsCS(DS)	$\overline{CS}$ Valid to $\overline{DS}$ FE Setup Time	30		30		ns
73	TrDS	$\overline{DS}$ RE to $\overline{DS}$ FE Recovery Time (for Commands Only)	4TcC		4TcC		ns
74	TwRST	$\overline{RESET}$ LOW Width	3TcC		3TcC		ns
75	TdC(BRQf)	Clock RE to BREQ RE Delay		165		150	ns
76	TdC(BRQr)	Clock FE to BREQ FE Delay		150		150	ns
77	TdBRQ(CTRz)	BREQ FE to Control Bus Float Delay		140		140	ns
78	TdBRQ(ADz)	BREQ FE to AD Bus Float Delay		140		140	ns
79	TdBRQ(BAK)	BREQ RE to BACK RE Required Delay	0		0		ns
80	TsBAK(C)	BACK Valid to Clock RE Setup Time	50		45		ns
81	TdRES(ADz)	RESET FE to A and AD Buses Float Delay		135**		135	ns
82	TdRES(CTRz)	RESET FE to Control Bus Float Delay		100**		100	ns
83	TdRES(DSz)	RESET FE to $\overline{DS}$ Float Delay		90**		90	ns
84	TsRW(DS)	R/$\overline{W}$ Valid to $\overline{DS}$ FE Setup Time (IOW)	2		2		ns
85	ThDS(RW)	$\overline{DS}$ RE to R/$\overline{W}$ Valid Hold Time (IOW)	−10		−10		ns
86	TsRW(DS)	R/$\overline{W}$ Valid to $\overline{DS}$ FE Setup Time (IOR)	20		20		ns
87	ThDS(RW)	$\overline{DS}$ RE to R/$\overline{W}$ Valid Hold Time (IOR)	20		20		ns

*2000 ns for slow readable registers (worst case)
**Guaranted but not tested.
Note: RE = rising edge
FE = falling edge

UDC-PERIPHERAL INTERFACE

			Preliminary				
			4 MHz		6 MHz		
No.	Parameter Symbol	Parameter Description	Min.	Max.	Min.	Max.	Unit
90	TCHDL	Clock RE to Pulsed $\overline{DACK}$ FE Delay (Flyby Transactions Only)		100		85	ns
91	TCHDH	Clock RE to Pulsed $\overline{DACK}$ RE Delay (To Flyby Transactions Only)		100		85	ns
92	TDSK	$\overline{DS}$ RE to Pulsed $\overline{DACK}$ RE Delay (FROM Flyby Transactions Only)	10		10		ns
93	TDAD	Clock RE to Level $\overline{DACK}$ Valid Delay		100		85	ns
94	TDAH	Clock FE to Level $\overline{DACK}$ Valid Hold Time		100		85	ns
95	TEIDL	Clock FE to Internal $\overline{EOP}$ LOW Delay		110		90	ns
96	TEIDH	Clock FE to Internal $\overline{EOP}$ RE Delay		110		90	ns
97	TES	External $\overline{EOP}$ Valid to Clock RE Setup Time During Operation	10		10		ns
98	TEW	External $\overline{EOP}$ Pulse Width Required During Operation	20		20		ns
99	TES(BH)	External $\overline{EOP}$ Valid to Clock RE Setup Time During Bus Hold	10		10		ns
100	TEW(BH)	External $\overline{EOP}$ Pulse Width Required During Bus Hold	20		20		ns

Note: RE = rising edge
FE = falling edge

Am9517A

Multimode DMA Controller

MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

- SMD/DESC qualified
- Four independent DMA channels, each with separate registers for Mode Control, Current Address, Base Address, Current Word Count and Base Word Count
- Transfer modes: Block, Demand, Single Word, Cascade
- Independent Autoinitialization of all channels
- Memory-to-memory transfers
- Memory block initialization
- Address increment or decrement
- Master system disable
- Enable/disable control of individual DMA requests
- Directly expandable to any number of channels
- End of Process input for terminating transfers
- Software DMA requests
- Independent polarity control for DREQ and DACK signals
- Compressed timing option speeds transfers – up to 2.5M bytes/second
- 40-pin Hermetic DIP package

GENERAL DESCRIPTION

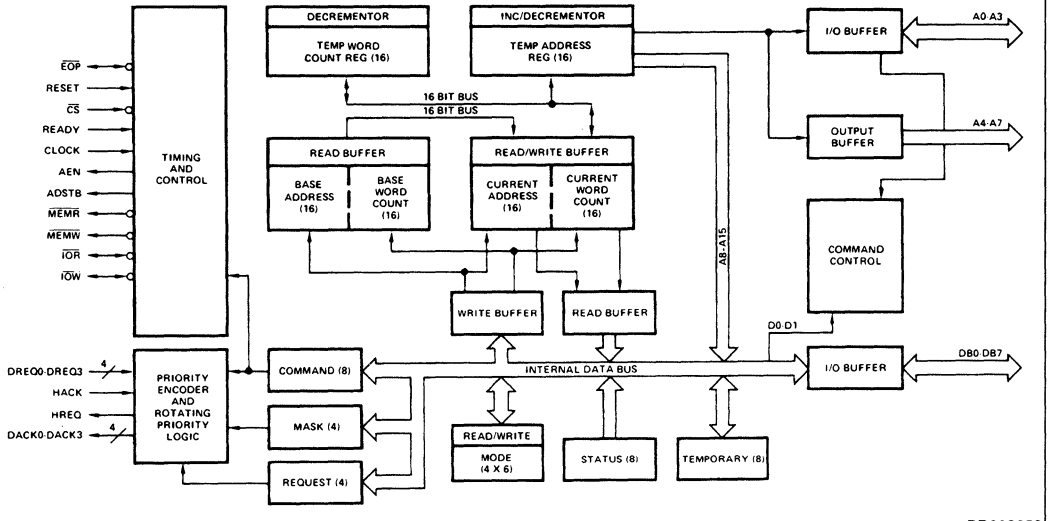
The Am9517A Multimode Direct Memory Access (DMA) Controller is a peripheral interface circuit for microprocessor systems. It is designed to improve system performance by allowing external devices to directly transfer information to or from the system memory. Memory-to-memory transfer capability is also provided. The Am9517A offers a wide variety of programmable control features to enhance data throughput and system optimization and to allow dynamic reconfiguration under program control.

The Am9517A is designed to be used in conjunction with an external 8-bit address register such as the Am74LS373. It contains four independent channels and may be expanded to any number of channels by cascading additional controller chips.

The three basic transfer modes allow programmability of the types of DMA service by the user. Each channel can be individually programmed to Autoinitialize to its original condition following an End of Process ($\overline{EOP}$).

Each channel has a full 64K address and word count capability. An external $\overline{EOP}$ signal can terminate a DMA or memory-to-memory transfer. This is useful for block search or compare operations using external comparators or for intelligent peripherals to abort erroneous services.

BLOCK DIAGRAM



BD003250

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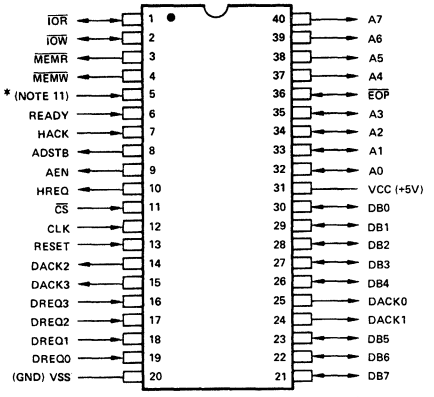
CONNECTION DIAGRAM
Top View

DIPs



CD005072

Note: Pin 1 is marked for orientation.
*See Note 9 under DC Characteristics table.

MILITARY ORDERING INFORMATION

Standard Military Drawing (SMD)/DESC Products

AMD standard products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of: **a. Military Drawing Part Number**
b. Device Type
c. Case Outline
d. Lead Finish

5962-87575 — 01 — Q — X

e. LEAD FINISH
X = Any Lead Finish Acceptable

c. CASE OUTLINE
Q = 40 pin Ceramic DIP (CD 040)

b. MILITARY DEVICE TYPE
01 = 3 MHz (9517A)
02 = 4 MHz (9517A-4)

a. MILITARY DRAWING NO./DESCRIPTION
5962-87575
Multimode DMA Controller

Valid Combinations	
5962-8757501	QX
5962-8757502	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

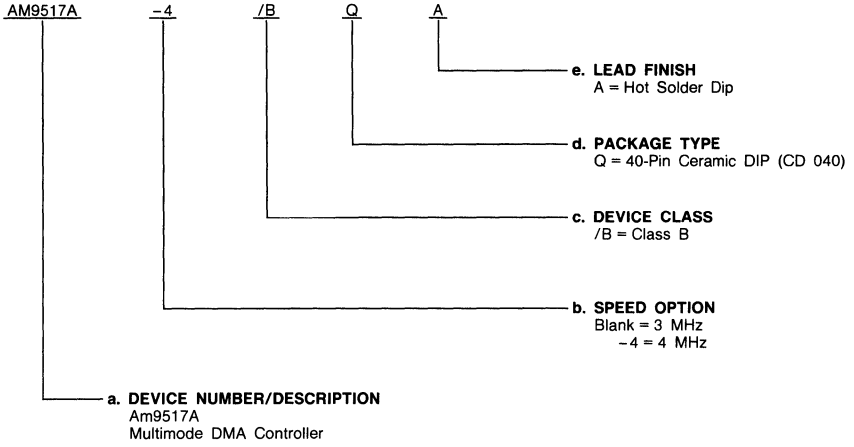
Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

MILITARY ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM9517A	/BQA
AM9517A-4	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage temperature ..... −65 to +150°C
V_{CC} with Respect to V_{SS} ..... −0.5 to +7.0 V
All Signal Voltages with Respect to V_{SS} .. −0.5 to +7.0 V
Power Dissipation (Package Limitation) ..... 1.5 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... 5 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −200 µA, V_{CC} = 4.5 V	2.4		V
		I_{OH} = −100 µA, (HREQ Only)	3.3		
V_{OL}	Output LOW Voltage	I_{OL} = 3.2 mA, V_{CC} = 5.5 V		0.45 V	V
V_{IH}	Input HIGH Voltage	V_{CC} = 4.5 V, 5.5 V	2.2	V_{CC} + 0.5*	V
V_{IHCLK}	Input HIGH Voltage	V_{CC} = 4.5 V, 5.5 V (CLK Only)	2.35	V_{CC} + 0.5*	V
V_{IL}	Input LOW Voltage	V_{CC} = 4.5 V, 5.5 V	−0.5*	0.7	V
I_{IX}	Input Load Current	$V_{SS} \leq V_I \leq V_{CC}$, V_{CC} = 5.5 V	−10	+10	µA
I_{OZ}	Output Leakage Current	$V_{CC} \leq V_O \leq V_{SS}$ + 0.40, V_{CC} = 5.5 V	−10	+10	µA
I_{CC}	V_{CC} Supply Current	(Note 1)		150	mA
C_O †	Output Capacitance (Note 12)	fc = 1.0 MHz, Inputs = 0 V		20*	pF
C_I †	Input Capacitance			15*	pF
C_{IO} †	I/O Capacitance		18*	pF	

* Guaranteed by design.
† Not included in Group A tests.
Notes:
1. I_{CC} is measured in a dynamic condition with outputs in a worst-case state having no loads applied.
2. Input timing parameters assume transition times of 20 ns or less. Waveform measurement points for both input and output signals are 2.0 V for HIGH and 0.8 V for LOW, unless otherwise noted.
3. The new $\overline{IOW}$ or $\overline{MEMW}$ pulse width for normal write will be TCY-100 ns and for extended write will be 2TCY-100 ns. The net $\overline{IOR}$ or $\overline{MEMR}$ pulse width for normal read will be 2TCY-50 ns and for compressed read will be TCY-50 ns.
4. TDQ is specified for two different output HIGH levels. TDQ1 is measured at 2.0 V. TDQ2 is measured at 3.3 V. The value for TDQ2 assumes an external 3.3 kΩ pull-up resistor connected from HREQ to V_{CC}.
5. DREQ should be held active until DACK is returned.
6. DREQ and DACK signals may be active HIGH or active LOW. Timing diagrams assume the active-HIGH mode.
7. Successive read and/or write operations by the external processor to program or examine the controller must be timed to allow at least 600 ns for the Am9517A, at least 450 ns for the Am9517A-4 as recovery time between active read or write pulses.
8. Parameters are listed in alphabetical order.
9. Pin 5 is an input that should always be at a logic-HIGH level. An internal pull-up resistor will establish a logic HIGH when the pin is left floating. Alternatively, pin 5 may be tied to V_{CC}.
10. Signals $\overline{READ}$ and $\overline{WRITE}$ refer to $\overline{IOR}$ and $\overline{MEMW}$ respectively for peripheral-to-memory DMA operations and to $\overline{MEMR}$ and $\overline{IOW}$ respectively for memory-to-peripheral DMA operations.
11. If N wait states are added during the write-to-memory half of a memory-to-memory transfer, this parameter will increase by N (TCY).
12. All output pins except HREQ.
13. Because $\overline{EOP}$ HIGH from clock HIGH is load-dependent, users wishing to test these parameters should use a 2k pull-up resistor and a tester with 50 pF or less load capacitance. Time constant R_C = 120 ns is added to the specified number in the data sheet for testing.

See Section 6 of the MOS Microprocessors and Peripherals Data Book
(Order #09067A) for Thermal Characteristics Information.

SWITCHING CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

ACTIVE CYCLE (Notes 2, 8, 9, and 10)

Parameter Symbol	Parameter Description	Am9517A		Am9517A-4		Unit
		Min.	Max.	Min.	Max.	
TAEL	AEN HIGH from CLK LOW (S1) Delay Time		300		225	ns
TAET	AEN LOW from CLK HIGH (S1) Delay Time		200		150	ns
TAFAB	ADR Active to Float Delay from CLK HIGH		150		120	ns
TAFC	$\overline{READ}$ or $\overline{WRITE}$ Float from CLK HIGH		150		120	ns
TAFDB	DB Active to Float Delay from CLK HIGH		250		190	ns
TAHR	ADR from $\overline{READ}$ HIGH Hold Time	TCY-100		TCY-100		ns
TAHS	DB from ADSTB LOW Hold Time	30		30		ns
TAHW	ADR from WRITE HIGH Hold Time	TCY-50		TCY-50		ns
TAK	DACK Valid from CLK LOW Delay Time		280		220	ns
	$\overline{EOP}$ HIGH from CLK HIGH Delay Time		250		190	ns
	$\overline{EOP}$ LOW to CLK HIGH Delay Time		250		190	ns
TASM	ADR Stable from CLK HIGH		250		190	ns
TASS	DB to ADSTB LOW Setup Time	100		100		ns
TCH	Clock High Time (Transitions $\leqslant$ 10ns)	120		100		ns
TCL	Clock Low Time (Transitions $\leqslant$ 10ns)	150		110		ns
TCY	CLK Cycle Time	320		250		ns
TDCL	CLK HIGH to $\overline{READ}$ or $\overline{WRITE}$ LOW Delay (Note 3)		270		200	ns
TDCTR	$\overline{Read}$ HIGH from CLK HIGH (S4) Delay Time (Note 3)		270		210	ns
TDCTW	$\overline{WRITE}$ HIGH from CLK HIGH (S4) Delay Time (Note 3)		200		150	ns
TDQ1	HREQ Valid from CLK HIGH Delay Time (Note 4)		160		120	ns
TDQ2			2TCY + 250		2TCY + 190	ns
TEPS	$\overline{EOP}$ LOW from CLK LOW Setup Time	60		45		ns
TEPW	$\overline{EOP}$ Pulse Width	300		225		ns
TFAAB	ADR Float to Active Delay from CLK HIGH		250		190	ns
TFAC	$\overline{READ}$ or $\overline{WRITE}$ Active from CLK HIGH		200		150	ns
TFADB	DB Float to Active Delay from CLK HIGH		300		225	ns
THS	HACK Valid to CLK HIGH Setup Time	100		75		ns
TIDH	Input Data from $\overline{MEMR}$ HIGH Hold Time	0		0		ns
TIDS	Input Data to $\overline{MEMR}$ HIGH Setup Time	250		190		ns
TODH	Output Data from $\overline{MEMW}$ HIGH Hold Time	20		20		ns
TODV	Output Data Valid to $\overline{MEMW}$ HIGH (Note 11)	200		125		ns
TQS	DREQ to CLK LOW (S1, S4) Setup Time	0		0		ns
TRH	CLK to READY LOW Hold Time	20		20		ns
TRS	READY to CLK LOW Setup Time	100		60		ns
TSTL	ADSTB HIGH from CLK HIGH Delay Time		200		150	ns
TSTT	ADSTB LOW from CLK HIGH Delay Time		140		110	ns
TQH	DREQ from DACK Valid Hold Time	0		0		ns
TRQHA	HREQ to HACK Delay Time	1		1		clk

AC Device Test Conditions: V_{CC} = 4.5 V, 5.5 V
V_{IL} = 0.45 V, V_{IH} = 2.4 V
V_{OL} = 0.8 V, V_{OH} = 2.0 V
I_{OL} = 3.2 mA, I_{OH} = 200 μA
CL = 100 pF ±20 pF

Notes: See notes following DC Characteristics.

SWITCHING CHARACTERISTICS (Cont'd.)

PROGRAM CONDITION (Idle Cycle) (Notes 2, 3, 10, and 11)

Parameter Symbol	Parameter Description	Am9517A		Am9517A-4		Unit
		Min.	Max.	Min.	Max.	
TAR	ADR Valid or $\overline{CS}$ LOW to $\overline{READ}$ LOW	50		50		ns
TAW	ADR Valid to $\overline{WRITE}$ HIGH Setup Time	200		150		ns
TCW	CS LOW to $\overline{WRITE}$ HIGH Setup Time	200		150		ns
TDW	Data Valid to $\overline{WRITE}$ HIGH Setup Time	200		150		ns
TRA	ADR or CS Hold from $\overline{READ}$ HIGH	0		0		ns
TRDE	Data Access from $\overline{READ}$ LOW (Note 8)		300		200	ns
TRDF	DB Float Delay from $\overline{READ}$ HIGH	20	150	20	100	ns
TRSTD	Power Supply HIGH to RESET LOW Setup Time	500		500		μs
TRSTS	RESET to First $\overline{IOWR}$	2TCY		2TCY		ns
TRSTW	RESET Pulse Width	300		300		ns
TRW	$\overline{READ}$ Width	300		250		ns
TWA	ADR from $\overline{WRITE}$ HIGH Hold Time	20		20		ns
TWC	CS HIGH from $\overline{WRITE}$ HIGH Hold Time	20		20		ns
TWD	Data from $\overline{WRITE}$ HIGH Hold Time	30		30		ns
TWWS	Write Width	200		200		ns
TAD	Data Access from ADR Valid $\overline{CS}$ LOW (TAD = TAR + TRDE)		300		300	ns

Notes: See notes following DC Characteristics.

Am9519A

Universal Interrupt Controller

MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

- SMD/DESC qualified
- Eight individually maskable interrupt inputs reduce CPU overhead
- Unlimited interrupt channel expansion with no extra hardware
- Programmable 1-byte to 4-byte response provides vector address and message protocol for 8-bit CPUs
- Rotating and fixed priority resolution logic
- Software interrupt request capability
- Common vector and polled mode options
- Automatic hardware clear of in-service interrupts reduces software overhead
- Polarity control of interrupt inputs and outputs
- Reset minimizes software initialization by automatically generating CALL to location zero

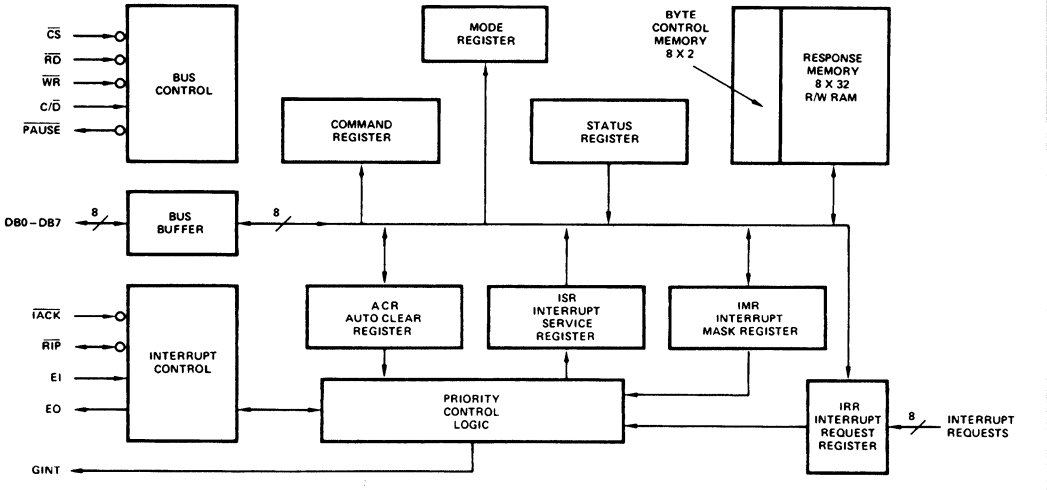
GENERAL DESCRIPTION

The Am9519A Universal Interrupt Controller is a processor support circuit that provides a powerful interrupt structure to increase the efficiency and versatility of microcomputer-based systems. A single Am9519A manages up to eight maskable interrupt request inputs, resolves priorities, and supplies up to four bytes of fully programmable response for each interrupt. It uses a simple expansion structure that allows many units to be cascaded for control of large numbers of interrupts. Several programmable control features are provided to enhance system flexibility and optimization.

The Universal Interrupt Controller is designed with a general-purpose interface to facilitate its use with a wide range of digital systems, including most popular 8-bit microprocessors. Since the response bytes are fully programmable, any instruction or vectoring protocol appropriate for the host processor may be used.

When the Am9519A controller receives an unmasked interrupt request, it issues a Group Interrupt output to the CPU. When the interrupt is acknowledged, the controller outputs the one-to-four byte response associated with the highest priority unmasked interrupt request. The ability of the CPU to set interrupt requests under software control permits hardware prioritization of software tasks, and aids system diagnostic and maintenance procedures.

BLOCK DIAGRAM

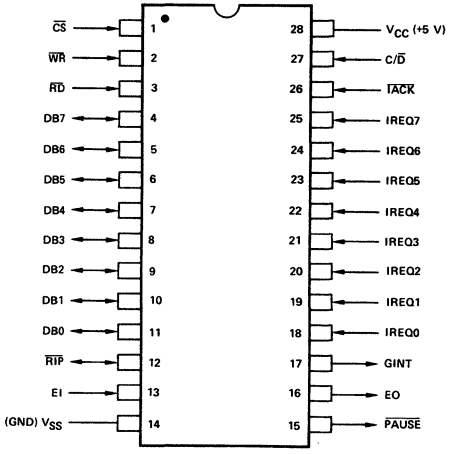


BD003280

Publication # 09228 | Rev. A | Amendment /0
Issue Date: November 1987

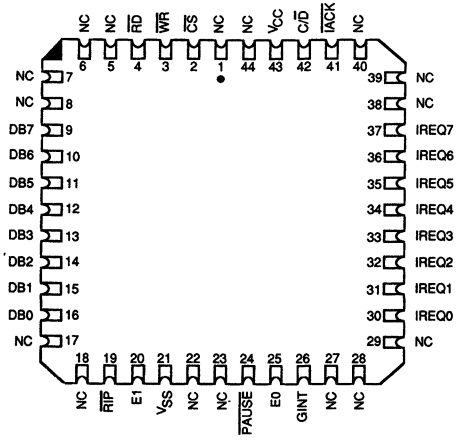
CONNECTION DIAGRAMS
Top View

DIPs



CD005102

LCC



CD010880

Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of: **a. Military Drawing Fart Number**
b. Device Type
c. Case Outline
d. Lead Finish

5962-87597 — 01 — X — X

d. LEAD FINISH
X = Any Lead Finish Acceptable

c. CASE OUTLINE
X = 28-Pin Ceramic DIP (CD 028)
Y = 44-Pin Ceramic Leadless Chip Carrier (CL 044)

b. MILITARY DEVICE TYPE
01 = 2 MHz (9519A)

a. MILITARY DRAWING NO./DESCRIPTION
5962-87597
Universal Interrupt Controller

Valid Combinations	
5962-8759701	XX, XY

Valid Combinations

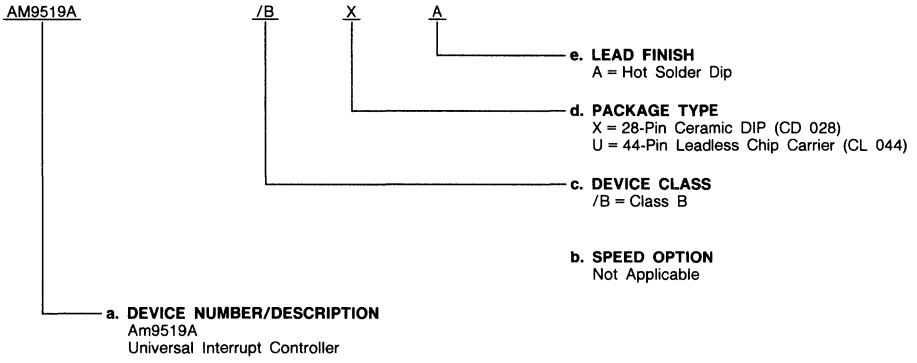
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests
Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

MILITARY ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM9519A	/BXA, /BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
VCC with Respect to V_{SS} ..... −0.5 V to +7.0 V
All Signal Voltages
with Respect to V_{SS} ..... −0.5 V to +7.0 V
Power Dissipitation (Package Limitation)..... 1.5 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C)..... −55 to 125°C
Supply Voltage (V_{CC}) ..... 5 V ± 10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

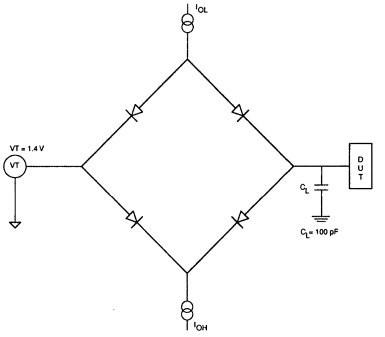
DC CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise specified)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage (Note 8)	I_{OH} = −200 µA		2.4		V
		I_{OH} = −100 µA (EO only)		2.4		
V_{OL}	Output LOW Voltage	I_{OL} = 3.2 mA			0.4	V
		I_{OL} = 1.0 mA (EO only)			0.4	
V_{IH}	Input HIGH Voltage			2.0	V_{CC}*	V
V_{IL}	Input LOW Voltage			−0.5*	0.8	V
I_{IX}	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{CC}$	EI Input	−60	10	µA
			Other Inputs	−10	10	
I_{OZ}	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{CC}$, Output Off		−150	150	µA
I_{CC}	V_{CC} Supply Current	V_{CC} = 5.5 V (Note 1)			200	mA
C_O †	Output Capacitance	f_c = 1.0 MHz			15*	pF
C_I †	Input Capacitance	T_C = 25°C			10*	
C_{IO} †	I/O Capacitance	All pins at 0 V			20*	

*Guaranteed by design; not tested.
†Not included in Group A tests.

Note 1. I_{CC} is measured in a static condition with outputs in the worst condition with all outputs unloaded.

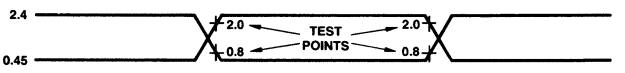
SWITCHING TEST CIRCUIT



TC004200

This test circuit is the dynamic load of a Teradyne J941.

SWITCHING TEST INPUT/OUTPUT WAVEFORM



WF007820

SWITCHING CHARACTERISTICS over operating ranges (for SMD/DESC and APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted). (Notes 1, 2)

No.	Parameter Symbol	Parameter Description	Am9519A Min.	Am9519A Max.	Unit
1	TAVRL	C/$\overline{D}$ Valid and $\overline{CS}$ LOW to Read LOW	0		ns
2	TAVWL	C/$\overline{D}$ Valid and $\overline{CS}$ LOW to Write LOW	0		ns
3	TCLPH	$\overline{RIP}$ LOW to $\overline{PAUSE}$ HIGH (Note 3)	75	375	ns
4	TCLQV	$\overline{RIP}$ LOW to Data Out Valid (Note 4)		50	ns
5	TDVWH	Data in Valid to Write HIGH	250		ns
6	TEHCL	Enable in HIGH to $\overline{RIP}$ LOW (Note 5)	30	300	ns
7	TIVGV	Interrupt Request Valid to Group Interrupt Valid	100	800	ns
8	TIVIX	Interrupt Request Valid to Interrupt Request Don't Care (IREQ Pulse Duration)	250		ns
9	TKHCH	$\overline{IACK}$ HIGH to $\overline{RIP}$ HIGH (Note 5)		450	ns
10	TKHKL	$\overline{IACK}$ HIGH to $\overline{IACK}$ LOW ($\overline{IACK}$ Recovery)	140		ns
11	TKHNH	$\overline{IACK}$ HIGH to EO HIGH (Notes 6, 7)		975	ns
12	TKHQX	$\overline{IACK}$ HIGH to Data Out Invalid	20	200	ns
13	TKLCL	$\overline{IACK}$ LOW to $\overline{RIP}$ LOW (Notes 5, 9)	75	650	ns
14	TKLKH	$\overline{IACK}$ LOW to $\overline{IACK}$ HIGH (1st $\overline{IACK}$) (Note 9)	975		ns
15	TKLNL	$\overline{IACK}$ LOW to EO LOW (Notes 6, 7, 9)		125	ns
16	TKLPL	$\overline{IACK}$ LOW to $\overline{PAUSE}$ LOW (Note 9)	25	175	ns
17	TKLQV	$\overline{IACK}$ LOW to Data Out Valid (Notes 4, 9)	25	300	ns
18	TKLQV1	1st $\overline{IACK}$ LOW to Data Out Valid (Note 9)	75	650	ns
19	TPHKH	$\overline{PAUSE}$ HIGH to $\overline{IACK}$ HIGH	0		ns
20	TRHAX	Read HIGH to C/$\overline{D}$ and $\overline{CS}$ Don't Care	0		ns
21	TRHQX	Read HIGH to Data Out Invalid	20	200	ns
22	TRLQV	Read LOW to Data Out Valid		300	ns
23	TRLQX	Read LOW to Data Out Unknown	35		ns
24	TRLRH	Read LOW to Read HIGH ($\overline{RD}$ Pulse Duration)	300		ns
25	TWHAX	Write HIGH to C/$\overline{D}$ and $\overline{CS}$ Don't Care	25		ns
26	TWHDX	Write HIGH to Data in Don't Care	25		ns
27	TWHRW	Write HIGH to Read or Write LOW (Write Recovery)	600		ns
28	TWLWH	Write LOW to Write HIGH ($\overline{WR}$ Pulse Duration)	300		ns
29	TKHIH	$\overline{IACK}$ HIGH to GINT Inactive		1000	ns

Notes:
1. Transition abbreviations used for the switching parameter symbols include: H = HIGH, L = LOW, V = Valid, X = unknown or don't care, Z = high-impedance.
2. Signal abbreviations used for the switching parameter symbols include: R = Read, W = Write, Q = Data Out, D = Data In, A = Address ($\overline{CS}$ and C/$\overline{D}$), K = Interrupt Acknowledge, N = Enable Out, E = Enable In, P = Pause, C = $\overline{RIP}$.
3. During the first $\overline{IACK}$ pulse, $\overline{PAUSE}$ will be LOW long enough to allow for priority resolution and will not go HIGH until after RIP goes LOW (TCLPH).
4. TKLQV applies only to second, third and fourth $\overline{IACK}$ pulses while $\overline{RIP}$ is LOW. During the first $\overline{IACK}$ pulse, Data Out will be valid following the falling edge of $\overline{RIP}$ (TCLQV).
5. $\overline{RIP}$ is pulled LOW to indicate that an interrupt request has been selected. $\overline{RIP}$ cannot be pulled LOW until EI is HIGH following an internal delay. TKLCL will govern the falling edge of $\overline{RIP}$ when EI is always HIGH or is HIGH early in the acknowledge cycle. The TEHCL will govern when EI goes HIGH later in the cycle. The rising edge of EI will be determined by the length of the preceding priority resolution chain.
   $\overline{RIP}$ remains LOW until after the rising edge of the $\overline{IACK}$ pulse that transfers the last response byte for the selected IREQ.
6. Test conditions for the EO line assume an output loading of IOL = 1.0 mA and IOH = −100 μA. Since EO normally only drives EI of another Am9519A, higher speed operations can be specified with this more realistic test condition.
7. The arrival of $\overline{IACK}$ will cause EO to go LOW, disabling additional circuits that may be connected to EO. If no valid interrupt is pending, EO will return HIGH when EI is HIGH. If a pending request is selected, EO will stay LOW until after the last $\overline{IACK}$ pulse for that interrupt is complete and $\overline{RIP}$ goes HIGH.
8. V_{OH} specifications do not apply to $\overline{RIP}$, $\overline{PAUSE}$, or to $\overline{GINT}$ when active-LOW. These outputs are open drain, and V_{OH} levels will be determined by external circuitry.
9. $\overline{CS}$ must be HIGH for at least 100 ns prior to $\overline{IACK}$ going LOW.

CHAPTER 3

*DESC approved
**Pending DESC approval

80186

High-Integration 16-Bit Microprocessor
iAPX86 Family
MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

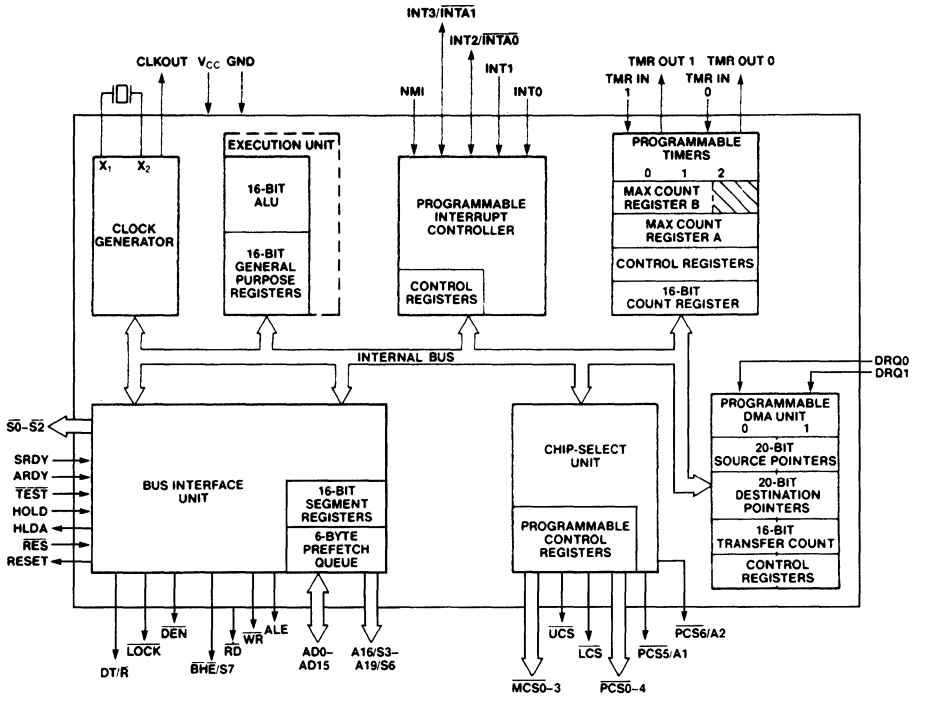
- Integrated feature set
  - Enhanced 8-MHz 8086-2 CPU
  - Clock generator
  - Two independent, high-speed DMA channels
  - Programmable interrupt controller
  - Three programmable 16-bit timers
  - Programmable memory and peripheral chip-select logic
  - Programmable wait-state generator
  - Local bus controller
- Available in 8 MHz (80186) and 6 MHz (80186-6)
- High-performance processor
  - Two times the performance of the standard 8086
  - 4 Mbyte/sec bus bandwidth interface
- Direct addressing capability to 1 Mbyte of memory
- Completely object-code-compatible with all existing iAPX 86, 88 software
  - Ten new instruction types
  - Compatible with 29843/45 and 8284 bus support components
- Optional numeric processor extension
- Available in 68-pin Ceramic Leadless Chip Carrier (LCC) and Pin Grid Array (PGA) packages

GENERAL DESCRIPTION

The 80186 is a highly integrated 16-bit microprocessor. It effectively combines 15-20 of the most common iAPX 86 system components onto one. The 80186 provides two times greater throughput than the standard 5-MHz 8086. The 80186 is upward-compatible with 8086 and 8088 software, and adds ten new instruction types to the existing set.

The 80186 comes in a 68-pin package and requires a single ±5V power supply.

BLOCK DIAGRAM

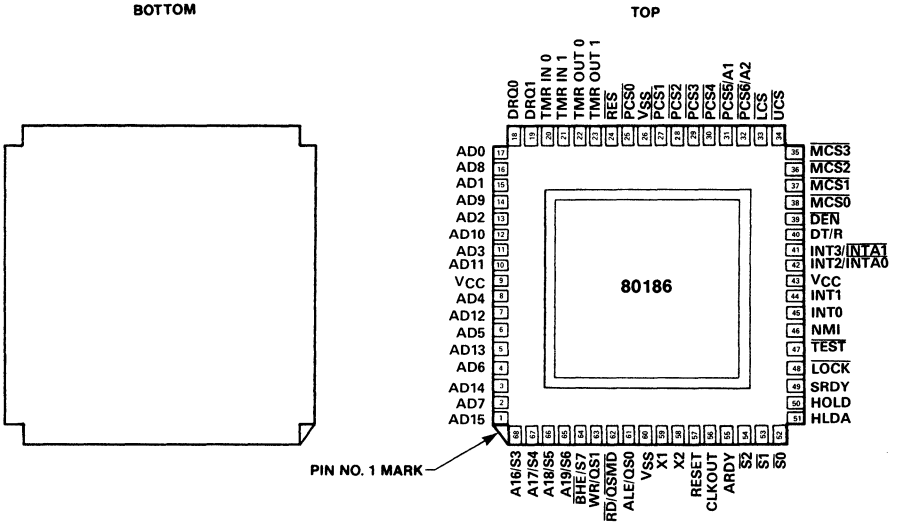


BD003560

Publication # 07039 | Rev. B | Amendment /0
Issue Date: December 1987

CONNECTION DIAGRAMS

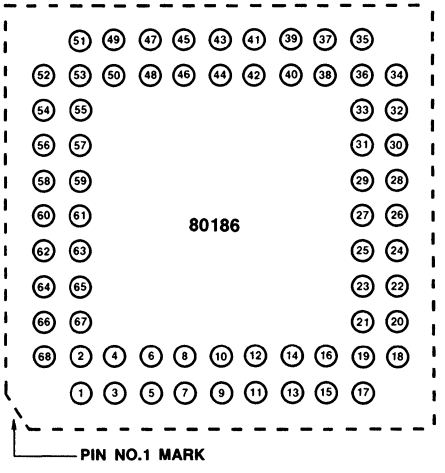
68-Pin Ceramic LCC Package



CD005393

68-Pin Grid Array
Cavity Down Package

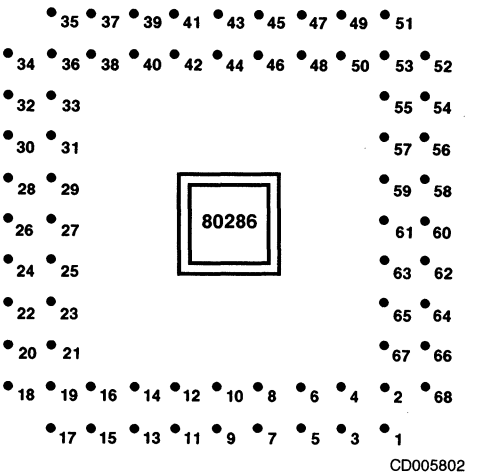
Top
(Pins pointing away from viewer)
0



CD005792

Pins are not visible from the top of this package.

Bottom
(Pins pointing toward viewer)
3835



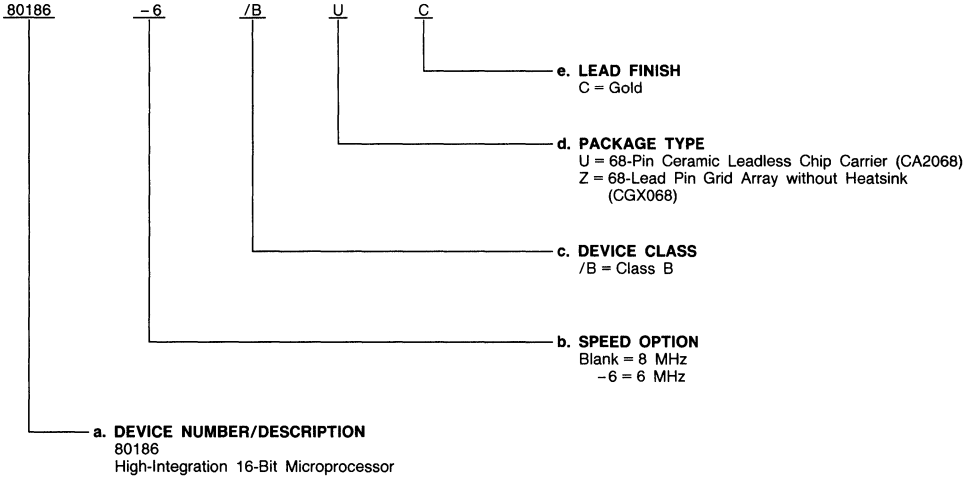
CD005802

Pins are visible from the bottom of this package.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
80186	/BUC, /BZC
80186-6	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage on Any Pin with
Respect to Ground..... −1.0 V to +7 V
Power Dissipation ..... 3 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C)..... −55 to +125°C
Supply Voltage (V_{CC}) ..... 5 V ±5%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for APL products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL} †	Input LOW Voltage		−0.5	+0.8	V
V_{IH} †	Input HIGH Voltage (All Except X_1 and $\overline{RES}$)		2.0	V_{CC} + 0.5	V
V_{IH1} †	Input HIGH Voltage ($\overline{RES}$)		3.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.5 mA for $\overline{S_0}$–$\overline{S_2}$ I_{OL} = 2.0 mA for All Other Outputs		0.45	V
V_{OH}	Output HIGH Voltage	I_{OH} = −400 μA	2.4		V
I_{CC}	Power Supply Current	T_C = −55°C, V_{CC} = V_{CC} Max.		600	mA
I_{LI}	Input Leakage Current	0 V < V_{IN} < V_{CC} Max.		±10	μA
I_{LO}	Output Leakage Current	0.45 V < V_{OUT} < V_{CC} Max.		±10	μA
V_{CLO}	Clock Output LOW	I_{OL} = 4.0 mA		0.6	V
V_{CHO}	Clock Output HIGH	I_{OH} = −200 μA	4.0		V
V_{CLI} †	Clock Input LOW Voltage		−0.5	0.6	V
V_{CHI} †	Clock Input HIGH Voltage		3.9	V_{CC} + 1.0	V
C_{IN} ††	Input Capacitance			10*	pF
C_{IO} ††	I/O Capacitance			20*	pF

* Not tested; guaranteed by design.
† Group A, Subgroups 7 and 8 only are tested.
†† Not included in Group A tests.

See Section 6 of the MOS Microprocessors and Peripherals Data Book (Order #09067A) for Thermal Characteristics Information.

SWITCHING CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

PIN TIMING

80186 Timing Requirements (all timings measured at 1.5 V unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	80186 (8 MHz) & 80186-6 (6 MHz)		Unit
			Min.	Max.	
TDVCL	Data in Setup (A/D)		20		ns
TCLDX	Data in Hold (A/D)		10		ns
TARYHCH	Asynchronous Ready (AREADY) Active Setup Time*		20		ns
TARYLCL	AREADY Inactive Setup Time		38		ns
TCHARYX	AREADY Hold Time		15		ns
TSRYCL	Synchronous Ready (SREADY) Transition Setup Time		35		ns
TCLSRY	SREADY Transition Hold Time		15		ns
THVCL	HOLD Setup*		25		ns
TINVCH	INTR, NMI, $\overline{TEST}$, TIMERIN, Setup*		25		ns
TINVCL	DRQ_0, DRQ_1, Setup*		25		ns

*To guarantee recognition at next clock.

Note: Case temperatures are instant-on.

80186 Master Interface Timing Responses

Parameter Symbol	Description	Test Conditions	80186 (8 MHz)		80186-6 (6 MHz)		Unit
			Min.	Max.	Min.	Max.	
TCLAV	Address Valid Delay	C_L = 100 pF all outputs	5	59	5	63	ns
TCLAX	Address Hold		5		5		ns
TCLAZ	A ddress Float Delay		TCLAX	35	TCLAX	44	ns
TCHCZ	Command Lines Float Delay			45		56	ns
TCHCV	Command Lines Valid Delay (After Float)			55		76	ns
TLHLL	ALE Width		TCLCL-35		TCLCL-35		ns
TCHLH	ALE Active Delay			35		44	ns
TCHLL	ALE Inactive Delay			35		44	ns
TLLAX	Address Hold to ALE Inactive		TCHCL-25		TCHCL-30		ns
TCLDV	Data Valid Delay		5	44	5	55	ns
TCLDOX	Data Hold Time		5		5		ns
TWHDX	Data Hold after WR		TCLCL-40		TCLCL-50		ns
TCVCTV	Control Active Delay1		10	50	10	87	ns
TCHCTV	Control Active Delay2		5	73	5	76	ns
TCVCTX	Control Inactive Delay		5	55	5	76	ns
TCVDEX	$\overline{DEN}$ Inactive Delay (Non-Write Cycle)			70		87	ns
TAZRL	Address Float to $\overline{RD}$ Active		0		0		ns
TCLRL	$\overline{RD}$ Active Delay		10	70	10	87	ns
TCLRH	$\overline{RD}$ Inactive Delay		10	55	10	76	ns
TRHAV	$\overline{RD}$ Inactive to Address Active		TCLCL-40		TCLCL-50		ns
TCLHAV	HLDA Valid Delay		5	67	5	67	ns
TRLRH	$\overline{RD}$ Width		2TCLCL-50		2TCLCL-50		ns
TWLWH	$\overline{WR}$ Width		2TCLCL-40		2TCLCL-40		ns
TAVAL	Address Valid to ALE LOW		TCLCH-25		TCLCH-45		ns
TCHSV	Status Active Delay		10	55	10	76	ns
TCLSH	Status Inactive Delay		10	65	10	76	ns
TCLTMV	Timer Output Delay	100 pF Max.		60		75	ns
TCLRO	Reset Delay			60		75	ns
TCHQSV	Queue Status Delay			35		44	ns
TCHDX	Status Hold Time		10		10		ns
TAVCH	Address Valid to Clock HIGH		10		10		ns

SWITCHING CHARACTERISTICS (Cont'd.)

80186 Chip-Select Timing Responses

Parameter Symbol	Parameter Description	Test Conditions	80186 (8 MHz)		80186-6 (6 MHz)		Unit
			Min.	Max.	Min.	Max.	
TCLCSV	Chip-Select Active Delay		5	66	5	80	ns
TCXCSX	Chip-Select Hold from Command Inactive		35		35		ns
TCHCSX	Chip-Select Inactive Delay		5	47	5	47	ns

80186 CLKIN Requirements

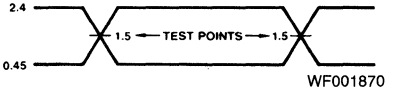
Parameter Symbol	Parameter Description	Test Conditions	80186 (8 MHz)		80186-6 (6 MHz)		Unit
			Min.	Max.	Min.	Max.	
TCKIN	CLKIN Period		62.5	250	83.2	250	ns
TCKHL	CLKIN Fall Time	3.5 to 1.0 volts		10		10	ns
TCKLH	CLKIN Rise Time	1.0 to 3.5 volts		10		10	ns
TCLCK	CLKIN Low Time	1.5 volts	25		33		ns
TCHCK	CLKIN High Time	1.5 volts	25		33		ns

80186 CLKOUT Timing (200-pF load)

Parameter Symbol	Parameter Description	Test Conditions	80186 (8 MHz)		80186-6 (6 MHz)		Unit
			Min.	Max.	Min.	Max.	
TCICO	CLKIN to CLKOUT Skew			50		62.5	ns
TCLCL	CLKOUT Period		125	500	166	500	ns
TCLCH	CLKOUT Low Time	1.5 volts	½TCLCL-7.5		½TCLCL-7.5		ns
TCHCL	CLKOUT High Time	1.5 volts	½TCLCL-7.5		½TCLCL-7.5		ns
TCH1CH2	CLKOUT Rise Time	1.0 to 3.5 volts		15		15	ns
TCL2CL1	CLKOUT Fall Time	3.5 to 1 volts		15		15	ns

All timings measured at 1.5 volts unless otherwise noted.

SWITCHING TEST INPUT/OUTPUT WAVEFORM



WF001870

AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." The clock is driven at 4.3 V and 0.25 V. Timing measurements are made at 1.5 V for both a logic "1" and "0."

80286

High-Performance Microprocessor with
Memory Management and Protection
PRELIMINARY MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

- High performance processor (up to six times iAPX 86 when using the 8 MHz 80286)
- Large address space
  - 16 megabytes physical
  - 1 gigabyte virtual memory per task
- Integrated memory management, four-level memory protection and support for virtual memory and operating systems
- Military temperature range (T_C = −55 to 125°C)
- Two iAPX 86 upward compatible operating modes
  - iAPX 86 real address mode
  - Protected virtual address mode
- High bandwidth bus interface (16 megabyte/sec)
- Range of clock rates
  - 8 MHz 80286-8

GENERAL DESCRIPTION

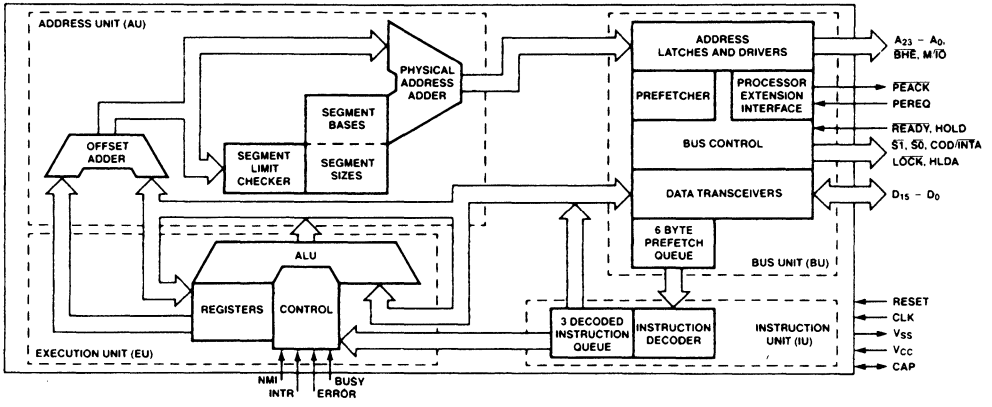
The 80286 is an advanced, high performance microprocessor with specially optimized capabilities for multiple user and multi-tasking systems. The 80286 has built-in memory protection that supports operating system and task isolation as well as program and data privacy within tasks. A 12 MHz 80286 provides up to ten times greater throughput than the standard 5 MHz 8086. The 80286 includes memory management capabilities that map up to 2^{30} bytes (one gigabyte) of virtual address space per task into 2^{24} bytes (16 megabytes) of physical memory.

The 80286 is upward compatible with iAPX 86 and 88 software. Using iAPX 86 real address mode, the 80286 is object code compatible with existing iAPX 86, 88 software.

In protected virtual address mode, the 80286 is source code compatible with iAPX 86, 88 software and may require upgrading to use virtual addresses supported by the 80286's integrated memory management and protection mechanism. Both modes operate at full 80286 performance and execute a superset of the iAPX 86 and 88 instructions.

The 80286 provides special operations to support the efficient implementation and execution of operating systems. For example, one instruction can end execution of one task, save its state, switch to a new task, load its state, and start execution of the new task. The 80286 also supports virtual memory systems by providing a segment-not-present exception and restartable instructions.

BLOCK DIAGRAM



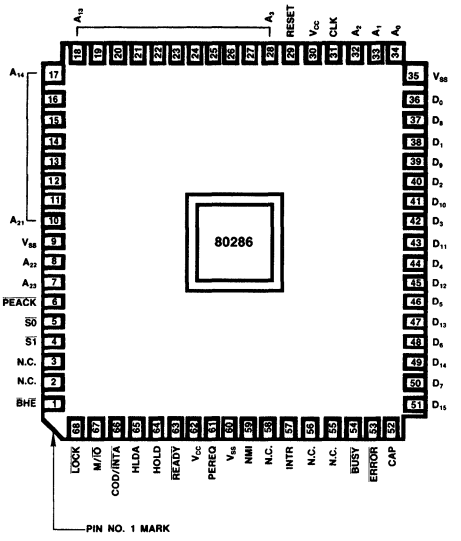
BD003960

Publication # 09398 | Rev. A | Amendment /0
Issue Date: October 1987

CONNECTION DIAGRAMS

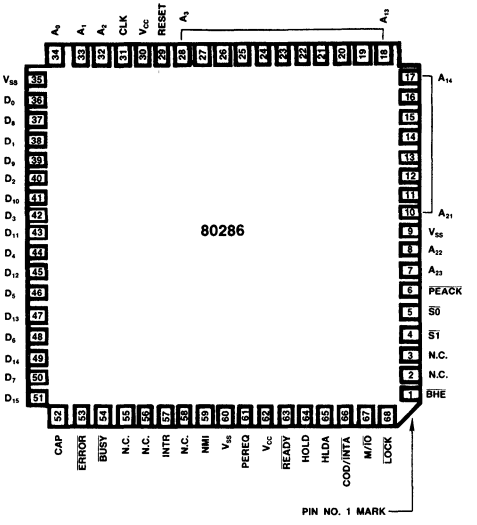
LCC

Component Pad Views –
as viewed from underside of component on the P.C. board.



CD005613

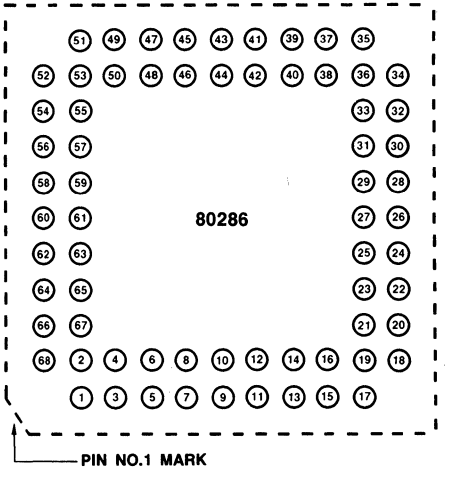
P.C. Board Views –
as viewed from the component side of the P.C. board.



CD005902

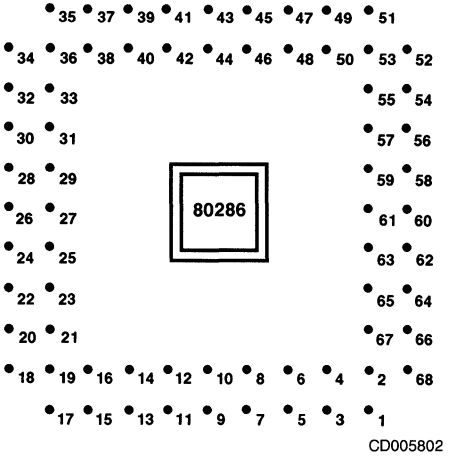
There are no electrical connections on the bottom of this package.

PGA



CD005794

Pins pointing away from viewer

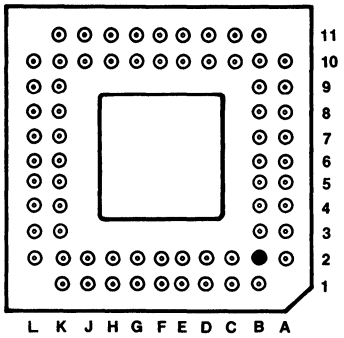


CD005802

Pins pointing toward viewer

PGA (continued)

Bottom View



CD005911

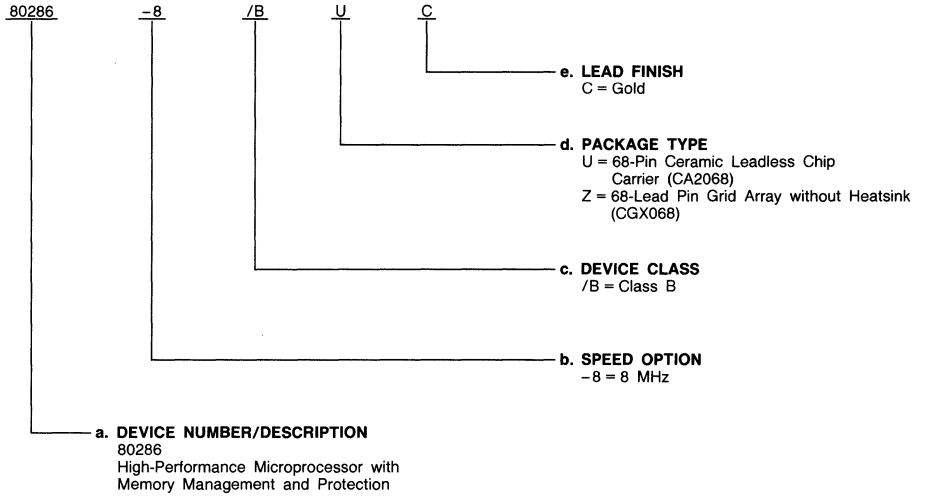
NAME	PAD	PIN
$\overline{BHE}$	1	B1
NC	2	B2
NC	3	C1
$\overline{S1}$	4	C2
$\overline{S0}$	5	D1
$\overline{PEACK}$	6	D2
A_{23}	7	E1
A_{22}	8	E2
V_{SS}	9	F1
A_{21}	10	F2
A_{20}	11	G1
A_{19}	12	G2
A_{18}	13	H1
A_{17}	14	H2
A_{16}	15	J1
A_{15}	16	J2
A_{14}	17	K1
A_{13}	18	L2
A_{12}	19	K2
A_{11}	20	L3
A_{10}	21	K3
A_9	22	L4
A_8	23	K4
A_7	24	L5
A_6	25	K5
A_5	26	L6
A_4	27	K6
A_3	28	L7
RESET	29	K7
V_{CC}	30	L8
CLK	31	K8
A_2	32	L9
A_1	33	K9
A_0	34	L10

NAME	PAD	PIN
V_{SS}	35	K11
D_0	36	K10
D_8	37	J11
D_1	38	J10
D_9	39	H11
D_2	40	H10
D_{10}	41	G11
D_3	42	G10
D_{11}	43	F11
D_4	44	F10
D_{12}	45	E11
D_5	46	E10
D_{13}	47	D11
D_6	48	D10
D_{14}	49	C11
D_7	50	C10
D_{15}	51	B11
CAP	52	A10
$\overline{ERROR}$	53	B10
$\overline{BUSY}$	54	A9
NC	55	B9
NC	56	A8
INTR	57	B8
NC	58	A7
NMI	59	B7
V_{SS}	60	A6
PEREQ	61	B6
V_{CC}	62	A5
$\overline{READY}$	63	B5
HOLD	64	A4
HLDA	65	B4
COD/$\overline{INTA}$	66	A3
M/$\overline{IO}$	67	B3
$\overline{LOCK}$	68	A2

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
80286-8	/BUC, /BZC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage on Any Pin with
Respect to Ground..... −1.0 to +7.0 V
Power Dissipation ..... 3.3 Watts

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C)..... −55 to +125°C
Supply Voltage (V_{CC}) ..... 5 V ± 10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage		−.5	.8	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + .5	V
V_{ILC}	CLK Input LOW Voltage		−.5	.6	V
V_{IHC}	CLK Input HIGH Voltage		3.8	V_{CC} + .5	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.0 mA		.45	V
V_{OH}	Output HIGH Voltage	I_{OH} = −400 µA	2.4		V
I_{LI}	Input Leakage Current	$0 V \leq V_{IN} \leq V_{CC}$		±10	µA
I_{LO}	Output Leakage Current	$.45 V \leq V_{OUT} \leq V_{CC}$		±10	µA
I_{CC}	Supply Current (turn on, 0°C)	Note 1		600	mA
I_{LO}	Output Leakage Current	$0 V \leq V_{out} \leq .045 V$		±1	mA
I_{IL}	Input Sustaining Current on $\overline{BUSY}$ and $\overline{ERROR}$ pins	V_{in} = 0 V	30	500	µA

Notes: 1. Low temperature is worst case.

CAPACITANCE*

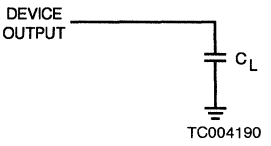
Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_{CLK} †	CLK Input Capacitance	f_C = 1 MHz		20*	pF
C_{IN} †	Other Input Capacitance	f_C = 1 MHz		10*	pF
C_O †	Input/Output Capacitance	f_C = 1 MHz		20*	pF

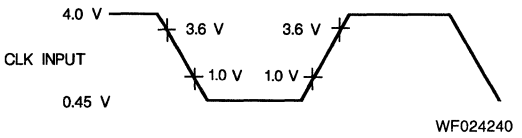
* Not tested; guaranteed by design.
† Not included in Group A tests.

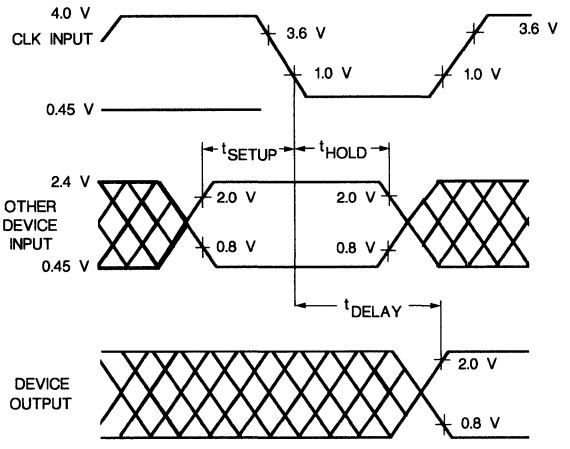
SWITCHING CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (V_{CC} = 5 V ± 10%, T_C = −55 to +125°C); AC timings are referenced to 0.8 V and 2.0 V points of signals as illustrated in datasheet waveforms, unless otherwise noted.

No.	Parameter Description	Test Conditions	Min.	Max.	Unit
1	System Clock (CLK) Period		62	250	ns
2	System Clock (CLK) LOW Time	at 1.0 V	15	225	ns
3	System Clock (CLK) HIGH Time	at 3.6 V	25	235	ns
17	System Clock (CLK) Rise Time	1.0 V to 3.6 V		10	ns
18	System Clock (CLK) Fall Time	3.6 V to 1.0 V		10	ns
4	Asynch. Inputs Set-up Time	Note 1	20		ns
5	Asynch. Inputs Hold Time	Note 1	20		ns
6	RESET Set-up Time		28		ns
7	RESET Hold Time		5		ns
8	Read Data Set-up Time		10		ns
9	Read Data Hold Time		8		ns
10	$\overline{\text{READY}}$ Set-up Time		38		ns
11	$\overline{\text{READY}}$ Hold Time		25		ns
12	Status/$\overline{\text{PEACK}}$ Valid Delay	Note 2, Note 3	1	40	ns
12a	Status/$\overline{\text{PEACK}}$ Active Delay	Note 2, Note 3	-	-	ns
12b	Status/$\overline{\text{PEACK}}$ Inactive Delay	Note 2, Note 3	-	-	ns
13	Address Valid Delay	Note 2, Note 3	1	60	ns
14	Write Data Valid Delay	Note 2, Note 3	0	50	ns
15	Address/Status/Data Float Delay	Note 2, Note 4	0	50	ns
16	HLDA Valid Delay	Note 2, Note 3	0	50	ns
19	Address Valid To Status Valid Setup Time	Note 3, Note 5, Note 6	38		ns

Notes:
1. Asynchronous inputs are INTR, NMI, HOLD PEREQ, $\overline{\text{ERROR}}$, and $\overline{\text{BUSY}}$. This specification is given only for testing purposes to assure recognition at a specific CLK edge.
2. Delay from 0.8 V on the CLK to 0.8 V or 2.0 V or float on the output as appropriate for valid or floating condition.
3. Output load: C_L = 100 pF.
4. Float condition occurs when output current is less than I_{LO} in magnitude.
5. Delay measured from address either reaching 0.8 V or 2.0 V (valid) to status going active reaching 2.0 V or status going inactive reaching 0.8 V.
6. For load capacitance of 10 pF on STATUS/$\overline{\text{PEACK}}$ lines, subtract typically 7 ns for 8 MHz spec.







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82284 Timing Requirements

No.	Parameter Description	Test Conditions	82284-8 Min.	82284-8 Max.	Unit
11	$\overline{SRDY}$/$\overline{SRDYEN}$ Set-up Time		17		ns
12	$\overline{SRDY}$/$\overline{SRDYEN}$ Hold Time		0		ns
13	$\overline{ARDY}$/$\overline{ARDYEN}$ Set-up Time	Note 1	0		ns
14	$\overline{ARDY}$/$\overline{ARDYEN}$ Hold Time	Note 1	30		ns
19	PCLK Delay	C_L = 75 pF I_{OL} = 5 mA I_{OH} = −1 mA	0	45	ns

Note 1. These times are given for testing purposes to assure a predetermined action.

82C288 Timing Requirements

No.	Parameter Description		Test Conditions	82C288-8 Min.	82C288-8 Max.	Unit
12	CMDLY Set-up Time			20		ns
13	CMDLT Hold Time			1		ns
30	Command Delay from CLK	Command Inactive	C_L = 300 pF Max. I_{OL} = 32 mA Max. I_{OH} = 5 mA Max.	5	25	ns
29		Command Active		3	25	
16	ALE Active Delay		C_L = 150 pF I_{OL} = 16 mA Max. I_{OH} = −1 mA Max.	3	20	ns
17	ALE Inactive Delay				25	ns
19	DT/$\overline{R}$ Read Active Delay				25	ns
22	DT/$\overline{R}$ Read Inactive Delay			5	35	ns
20	DEN Read Active Delay			5	35	ns
21	DEN Read Inactive Delay			3	35	ns
23	DEN Write Active Delay				30	ns
24	DEN Write Inactive Delay			3	30	ns

8085A

8-Bit Microprocessor

MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

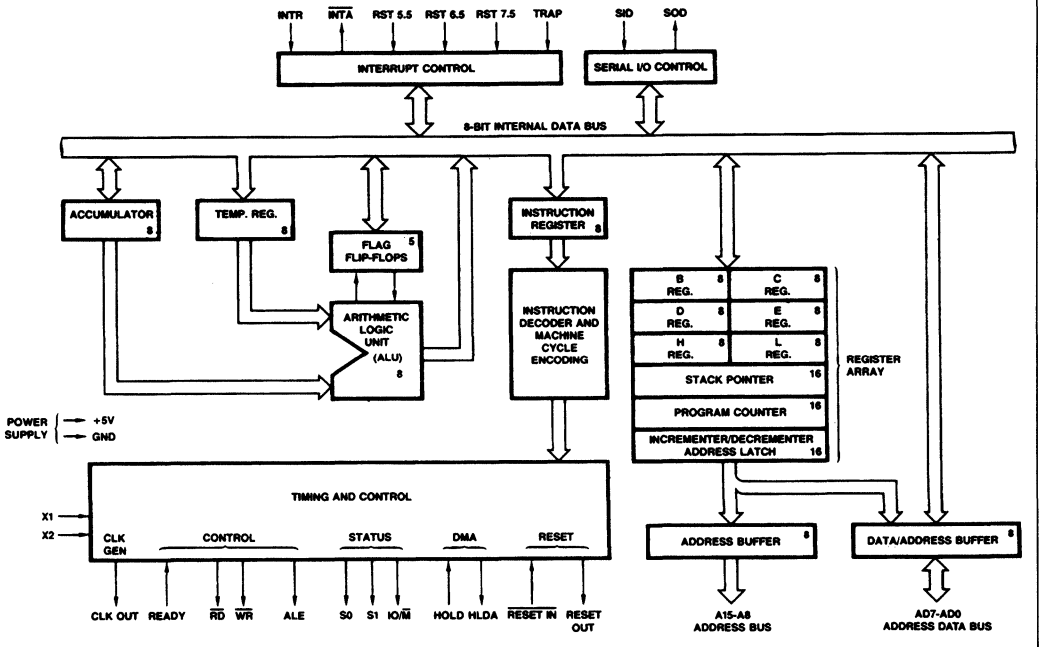
- SMD/DESC qualified
- 3- and 5-MHz selections available
- On-chip system controller; advanced cycle status information available for large system control
- Four vectored interrupts (one is non-maskable)
- On-chip clock generator (with external crystal, LC or R/C network)
- Serial-in/serial-out port
- Decimal, binary, and double-precision arithmetic
- Direct addressing capability to 64K bytes of memory
- 1.3 μs instruction cycle (8085A)
- 0.8 μs instruction cycle (8085A-2)
- 100% software-compatible with 8080A
- Single +5 V power supply

GENERAL DESCRIPTION

The 8085A is a new generation, complete 8-bit parallel central processing unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor. Specifically, the 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A. The 8085A-2 is a faster version of the 8085A. The 8085A is a 3-MHz CPU with 10% supply tolerances and lower power consumption.

The 8085A uses a multiplexed data bus. The address is split between the 8-bit address bus and the 8-bit data bus. The on-chip address latches of 8155H/56H memory products allow a direct interface with 8085A. The 8085A components, including various timing-compatible support chips, allow system speed optimization.

BLOCK DIAGRAM



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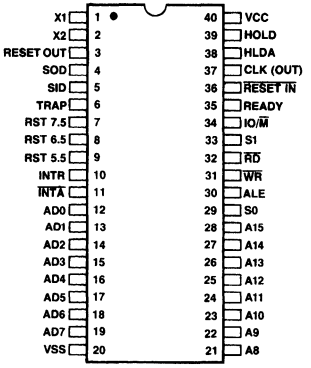
Publication # 09231 Rev. A Amendment /0
Issue Date: November 1987

CONNECTION DIAGRAM
Top View
DIPs



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Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of: **a. Military Drawing Part Number**
b. Device Type
c. Case Outline
d. Lead Finish

79010 01 Q X

d. LEAD FINISH
X = Any Lead Finish Acceptable

c. CASE OUTLINE
Q = 40-Pin Ceramic DIP (CD 040)

b. MILITARY DEVICE TYPE
01 = 3 MHz (8085A)

a. MILITARY DRAWING PART NUMBER
79010
8-Bit Microprocessor

Valid Combinations	
7901001	QX

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check on newly released valid combinations.

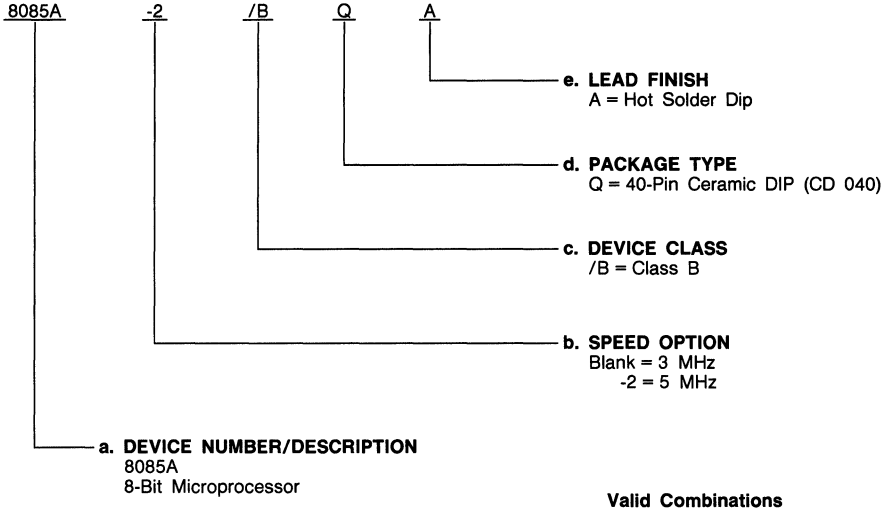
Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

MILITARY ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
8085A	/BQA
8085A-2	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage on Any Pin
With Respect to Ground..... −0.5 to +7 V
Power Dissipation ..... 1.5 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C)..... −55 to +125°C
Supply Voltage (V_{CC}) ..... 5 V ±10%
Supply Current (I_{CC})..... 200 mA

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage	V_{CC} = 5 V ±10%	−0.5*	+0.8	V
V_{IH}	Input HIGH Voltage	V_{CC} = 5 V ±10%	2.2	V_{CC} +0.5*	V
V_{OL}	Output LOW Voltage	I_{OL} = 2 mA, V_{CC} = 5 V ±10%		0.45	V
V_{OH}	Output HIGH Voltage	I_{OH} = −400 μA, V_{CC} = 5 V ±10%	2.4		V
I_{CC}	Power Supply Current	V_{CC} = 5.5 V (Note 1)		200	mA
I_{IL1}	Input Leakage, Except Pin 1	V_{CC} = 5.5 V, V_{IN} = V_{CC} to 0 V		±10	μA
I_{IL2}	Input Leakage, Pin 1	V_{CC} = 5.5 V, V_{IN} = V_{CC} to 0 V		±70	μA
I_{LO}	Output Leakage	V_{CC} = 5.5 V, V_{OUT} = V_{CC} to .45 V		±10	μA
V_{ILR}	Input LOW Level, RESET	V_{CC} = 5 V ±10%	−0.5*	+0.8	V
V_{IHR}	Input HIGH Level, RESET	V_{CC} = 5 V ±10%	2.4	V_{CC} +0.5*	V
V_{HY}	Hysteresis, RESET	V_{CC} = 5 V ±10%	0.25		V

*Guaranteed by design; not tested.

Notes: 1. I_{CC} is measured while running a functional pattern with no loads applied.

See Section 6 of the MOS Microprocessors and Peripherals Data Book (Order #09067A) for Thermal Characteristics Information.

SWITCHING CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	8085A (Note 2)		8085A-2 (Note 2)		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	CLK Cycle Period	320	2000	200	2000	ns
t_1	CLK LOW Time (Standard CLK Loading)	80		40		ns
t_2	CLK HIGH Time (Standard CLK Loading)	120		70		ns
t_r, t_f	CLK Rise and Fall Time		30		30	ns
t_{XKR}	X_1 Rising to CLK Rising	20	120	20	100	ns
t_{XKF}	X_1 Rising to CLK Falling	20	150	20	110	ns
t_{AC}	A_{8-15} Valid to Leading Edge of Control (Note 1)	270		115		ns
t_{ACL}	A_{0-7} Valid to Leading Edge of Control	240		115		ns
t_{AD}	A_{0-15} Valid to Valid Data In		575		350	ns
t_{AFR}	Address Float After Leading Edge of $\overline{READ}$ ($\overline{INTA}$)		0		0	ns
t_{AL}	A_{8-15} Valid Before Trailing Edge of ALE (Note 1)	90		50		ns
t_{ALL}	A_{0-7} Valid Before Trailing Edge of ALE	70		50		ns
t_{ARY}	READY Valid from Address Valid		220		100	ns
t_{CA}	Address (A_{8-15}) Valid After Control	120		60		ns
t_{CC}	Width of Control LOW ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$) Edge of ALE	400		230		ns
t_{CL}	Trailing Edge of Control to Leading Edge of ALE	50		25		ns
t_{DW}	Data Valid to Trailing Edge of $\overline{WRITE}$	420		230		ns
t_{HABE}	HLDA to Bus Enable		210		150	ns
t_{HABF}	Bus Float After HLDA		210		150	ns
t_{HACK}	HLDA Valid to Trailing Edge of CLK	110		40		ns
t_{HDH}	HOLD Hold Time	0		0		ns
t_{HDS}	HOLD Setup Time to Trailing Edge of CLK	170		120		ns
t_{INH}	INTR Hold Time	0		0		ns
t_{INS}	INTR, RST, and TRAP Setup Time to Falling Edge of CLK	160		150		ns
t_{LA}	Address Hold Time After ALE	100		50		ns
t_{LC}	Trailing Edge of ALE to Leading Edge of Control	130		60		ns
t_{LCK}	ALE LOW During CLK HIGH	100		50		ns
t_{LDR}	ALE to Valid Data During Read		460		270	ns
t_{LDW}	ALE to Valid Data During Write		200		120	ns
t_{LL}	ALE Width	140		80		ns
t_{LRY}	ALE to READY Stable		110		30	ns
t_{RAE}	Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	150		90		ns
t_{RD}	$\overline{READ}$ (or $\overline{INTA}$) to Valid Data		300		150	ns
t_{RV}	Control Trailing Edge to Leading Edge of Next Control	400		220		ns
t_{RDH}	Data Hold Time After $\overline{READ}$ $\overline{INTA}$ (Note 6)	0		0		ns
t_{RYH}	READY Hold Time	0		0		ns
t_{RYS}	READY Setup Time to Leading Edge of CLK	110		100		ns
t_{WD}	Data Valid After Trailing Edge of $\overline{WRITE}$	100		60		ns
t_{WDL}	LEADING Edge of WRITE to Data Valid		40		20	ns

Notes:
1. $A_8 - A_{15}$ address Specs apply to IO/$\overline{M}$, S_0, and S_1, except $A_8 - A_{15}$ are undefined during $T_4 - T_6$ of OF cycle; whereas, IO/$\overline{M}$, S_0, and S_1 are stable.
2. Test conditions: t_{CYC} = 320 ns (8085A)/200 ns (8085A-2); C_L = 100 pF, V_{CC} = 5 V ±10%, V_{IL} = .45 V, V_{IH} = 2.4 V; V_{OL} = .8 V, V_{OH} = 2.0 V.
3. For all output timing where C_L = 150 pF use the following correction factors:
   25 pF ≤ C_L < 150 pF: −0.10 ns/pF
   150 pF < C_L ≤ 300 pF: +0.30 ns/pF
4. Output timings are measured with purely capacitive load.
5. To calculate timing specifications at other values of t_{CYC} use Table 3 on page 3-191 of the MOS Microprocessors and Peripherals Data Book (Order #09067A)
6. Data hold time is guaranteed under all loading conditions.

8086

16-Bit Microprocessor
iAPX86 Family
MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

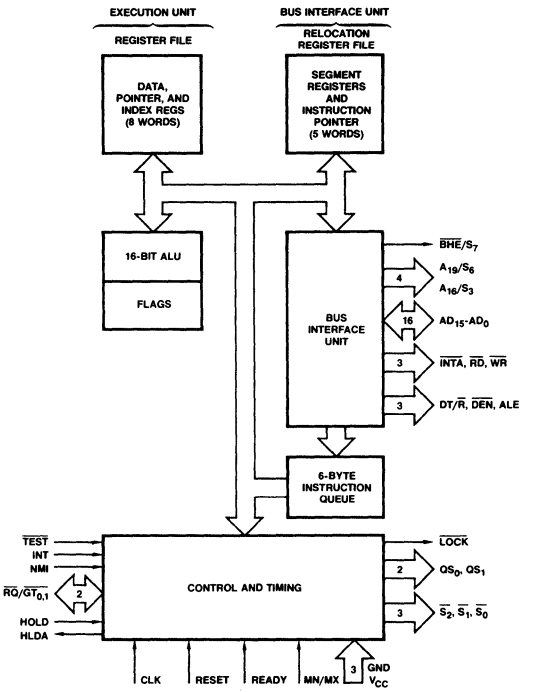
- Directly addresses up to 1 Mbyte of memory
- 24 operand addressing modes
- Efficient implementation of high-level languages
- Instruction set compatible with 8080 software
- Bit, byte, word, and block operations
- 8- and 16-bit signed and unsigned arithmetic in binary or decimal
- MULTIBUS* system interface
- Two speed options:
  - 5 MHz for 8086
  - 8 MHz for 8086-2

GENERAL DESCRIPTION

The 8086 is a general purpose 16-bit microprocessor CPU. Its architecture is built around thirteen 16-bit registers and nine 1-bit flags. The CPU operates on 16-bit address spaces, and can directly address up to 1 megabyte using offset addresses within four distinct memory segments, designated as code, data, stack, and extra code. The 8086 implements a powerful instruction set with 24 operand addressing modes. This instruction set is compatible with that of the 8080 and 8085. In addition, the 8086 is particularly effective in executing high-level languages.

The 8086 can operate in minimum and maximum modes. Maximum mode offloads certain bus control functions to a peripheral device and allows the CPU to operate efficiently in a multi-processor system. The CPU and its high performance peripherals are MULTIBUS compatible. The 8086 is implemented in N-channel, depletion load, silicon gate technology, and is contained in a 40-pin ceramic DIP package.

BLOCK DIAGRAM



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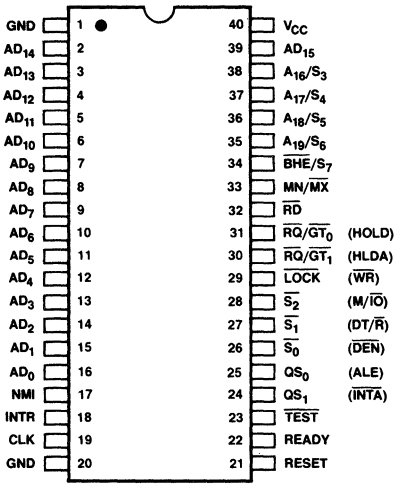
MULTIBUS is a registered trademark of Intel Corp.

Publication # 09232 Rev. A Amendment /0
Issue Date: December 1987

CONNECTION DIAGRAM
Top View



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Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

8086 -2 /B Q A

e. LEAD FINISH
A = Hot Solder Dip

d. PACKAGE TYPE
Q = 40-Pin Ceramic DIP (CD 040)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Blank = 5 MHz
-2 = 8 MHz

a. DEVICE NUMBER/DESCRIPTION
8086
16-Bit Microprocessor
iAPX Family

Valid Combinations	
8086	/BQA
8086-2	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature Under Bias ..... 0 to 70°C
Voltage on any Pin
with Respect to Ground ..... −1 to +7.0 V
Power Dissipation ..... 2.5 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... 5 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

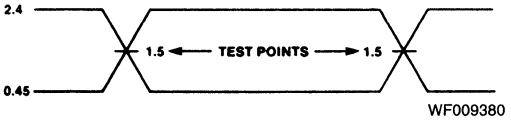
DC CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL} †	Input LOW Voltage	V_{CC} = Min. & Max.	−0.5*	+0.8	V
V_{IH} †	Input HIGH Voltage	V_{CC} = Min. & Max.	2.0	V_{CC} + 0.5*	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.0 mA, V_{CC} = Min.		0.45	V
V_{OH}	Output HIGH Voltage	I_{OH} = −400 µA, V_{CC} = Min.	2.4		V
I_{CC}	Power Supply Current (Note 1)	T_C = 25°C, V_{CC} = Max.		340	mA
I_{LI}	Input Leakage Current	V_{CC} = Max., V_{IN} = 5.5 V & 0 V	−10	10	µA
I_{LO} ††	Output Leakage Current	V_{CC} = Max., V_{OUT} = 5.5 V & 0.45 V	−10	10	µA
V_{CL} †	Clock Input LOW Voltage	V_{CC} = Min. & Max.	−0.5*	+0.6	V
V_{CH} †	Clock Input HIGH Voltage	V_{CC} = Min. & Max.	3.9	V_{CC} + 1.0*	V
C_{IN} †††	Capacitance of Input Buffer (All Input Except AD_0-AD_{15}, $\overline{RQ}/\overline{GT}$)	fc = 1 MHz		20*	pF
C_{IO} †††	Capacitance of I/O Buffer (AD_0-AD_{15}, $\overline{RQ}/\overline{GT}$)	fc = 1 MHz		20*	pF

* Guaranteed by design; not tested.
† Group A, Subgroups 7 and 8 only are tested.
†† Group A, Subgroups 1 and 2 only are tested.
††† Not included in Group A tests.

Notes: 1. I_{CC} is measured while running a functional pattern with spec value I_{OL}/I_{OH} loads applied.

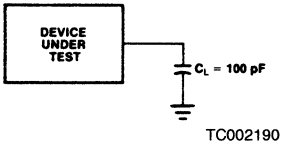
SWITCHING TEST INPUT/OUTPUT WAVEFORM



WF009380

AC TESTING INPUTS ARE DRIVEN AT 2.4 V FOR A LOGIC "1" AND 0.45 V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 1.5 V FOR BOTH A LOGIC "1" AND "0."

SWITCHING TEST LOAD CIRCUIT



TC002190

C_L INCLUDES JIG CAPACITANCE

SWITCHING CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

MINIMUM COMPLEXITY SYSTEM TIMING REQUIREMENTS

Parameter Symbol	Parameter Description	Test Conditions (Note 6)	8086		8086-2		Unit
			Min.	Max.	Min.	Max.	
TCLCL	CLK Cycle Period (Note 11)		200	500	125	500	ns
TCLCH	CLK LOW Time		118		68		ns
TCHCL	CLK HIGH Time		69		44		ns
TCH1CH2	CLK Rise Time (Note 5)	From 1.0 to 3.5 V		10		10	ns
TCL2CL1	CLK Fall Time (Note 5)	From 3.5 to 1.0 V		10		10	ns
TDVCL	Data in Setup Time		30		20		ns
TCLDX	Data in Hold Time		10		10		ns
TR1VCL	RDY Setup Time into 8284A (Notes 1 & 2)		35		35		ns
TCLR1X	RDY Hold Time into 8284A (Notes 1 & 2)		0		0		ns
TRYHCH	READY Setup Time into 8086		118		68		ns
TCHRYX	READY Hold Time into 8086		30		20		ns
TRYLCL	READY Inactive to CLK (Note 4)		-8		-8		ns
THVCH	HOLD Setup Time		35		20		ns
TINVCH	INTR, NMI, $\overline{\text{TEST}}$ Setup Time (Note 2)		30		15		ns
TILIH	Input Rise Time (Except CLK) (Note 5)	From 0.8 to 2.0 V		2 0		20	ns
TIHIL	Input Fall Time (Except CLK) (Note 5)	From 2.0 to 0.8 V		12		12	ns

Notes:
1. Signal at 8284A and 8288 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T3 and wait states.
4. Applies only to T2 state (8 ns into T3).
5. Not tested; these specs are controlled by the Teradyne J941 tester.
6. V_{CC} = 4.5 V, 5.5 V V_{IH} = 2.4 V
   V_{IL} = .45 V V_{IHC} = 4.3 V
   V_{ILC} = .25 V V_{OH} = 1.6 V
   V_{OL} = 1.4 V
7. Minimum spec tested at V_{CC} Max. (5.5 V) only.
8. Maximum spec tested at V_{CC} Min. (4.5 V) only.
9. Tested at V_{CC} Max. (5.5 V) only.
10. Tested at V_{CC} Min. (4.5 V) only.
11. Test conditions for TCLCL Max. are:
    V_{CC} = 4.5 V V_{OL} = 1 V
    V_{IL} = 0 V V_{IH} = 4 V
    V_{ILC} = 0 V V_{IHC} = 5 V

SWITCHING CHARACTERISTICS (Cont'd.)

TIMING RESPONSES

Parameter Symbol	Parameter Description	Test Conditions (Note 6)	8086		8086-2		Unit
			Min.	Max.	Min.	Max.	
TCLAV	Address Valid Delay	C_L = 100 pF for all 8086 Outputs (in addition to 8086 internal loads)	10	110	10	60	ns
TCLAX	Address Hold Time (Notes 7 & 8)		10		10		ns
TCLAZ	Address Float Delay (Note 8)		10	80	10	50	ns
TLHLL	ALE Width (Note 10)		58		58		ns
TCLLH	ALE Active Delay (Note 8)			80		50	ns
TCHLL	ALE Inactive Delay (Note 8)			85		55	ns
TLLAX	Address Hold Time to ALE Inactive (Note 7)		59		34		ns
TCLDV	Data Valid Delay (Note 8)		10	110	10	60	ns
TCHDX	Data Hold Time (Note 10)		10		10		ns
TWHDX	Data Hold Time After WR (Note 9)		88		38		ns
TCVCTV	Control Active Delay 1 (Note 8)		10	110	10	70	ns
TCHCTV	Control Active Delay 2 (Note 8)		10	110	10	60	ns
TCVCTX	Control Inactive Delay (Note 8)		10	110	10	70	ns
TAZRL	Address Float to READ Active (Note 8)		0		0		ns
TCLRL	$\overline{RD}$ Active Delay (Note 8)		10	165	10	100	ns
TCLRH	$\overline{RD}$ Inactive Delay (Note 8)		10	150	10	80	ns
TRHAV	$\overline{RD}$ Inactive to Next Address Active (Note 10)		155		85		ns
TCLHAV	HLDA Valid Delay (Note 8)		10	160	10	100	ns
TRLRH	$\overline{RD}$ Width (Note 10)		325		200		ns
TWLWH	$\overline{WR}$ Width (Note 10)		340		210		ns
TAVAL	Address Valid to ALE LOW (Note 9)		58		28		ns
TOLOH	Output Rise Time (Note 9)	From 0.8 to 2.0 V		20		20	ns
TOHOL	Output Fall Time (Note 9)	From 2.0 to 0.8 V		12		12	ns

Notes:
1. Signal at 8284A and 8288 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T3 and wait states.
4. Applies only to T2 state (8 ns into T3).
5. Not tested; these specs are controlled by the Teradyne J941 tester.
6. V_{CC} = 4.5 V, 5.5 V; V_{IH} = 2.4 V; V_{IL} = .45 V; V_{IHC} = 4.3 V; V_{ILC} = .25 V; V_{OH} = 1.6 V; V_{OL} = 1.4 V
7. Minimum spec tested at V_{CC} Max. (5.5 V) only.
8. Maximum spec tested at V_{CC} Min. (4.5 V) only.
9. Tested at V_{CC} Max. (5.5 V) only.
10. Tested at V_{CC} Min. (4.5 V) only.
11. Test conditions for TCLCL Max. are: V_{CC} = 4.5 V; V_{OL} = 1 V; V_{IL} = 0 V; V_{IH} = 4 V; V_{ILC} = 0 V; V_{IHC} = 5 V

SWITCHING CHARACTERISTICS (Cont'd.)

MAX MODE SYSTEM (USING 8288 BUS CONTROLLER) TIMING REQUIREMENTS

Parameter Symbol	Parameter Description	Test Conditions (Note 6)	8086		8086-2		Unit
			Min.	Max.	Min.	Max.	
TCLCL	CLK Cycle Period (Note 11)		200	500	125	500	ns
TCLCH	CLK LOW Time		118		68		ns
TCHCL	CLK HIGH Time		69		44		ns
TCH1CH2	CLK Rise Time (Note 5)	From 1.0 to 3.5 V		10		10	ns
TCL2CL1	CLK Fall Time (Note 5)	From 3.5 to 1.0 V		10		10	ns
TDVCL	Data in Setup Time		30		20		ns
TCLDX	Data in Hold Time		10		10		ns
TR1VCL	RDY Setup Time into 8284A (Notes 1 & 2)		35		35		ns
TCLR1X	RDY Hold Time into 8284A (Notes 1 & 2)		0		0		ns
TRYHCH	READY Setup Time into 8086		118		68		ns
TCHRYX	READY Hold Time into 8086		30		20		ns
TRYLCL	READY Inactive to CLK (Note 4)		−8		−8		ns
TINVCH	Setup Time for Recognition (INTR, NMI, $\overline{TEST}$) (Note 2)		30		15		ns
TGVCH	$\overline{RQ}/\overline{GT}$ Setup Time		30		15		ns
TCHGX	$\overline{RQ}$ Hold Time into 8086		40		30		ns
TILIH	Input Rise Time (Except CLK) (Note 5)	From 0.8 to 2.0 V		20		20	ns
TIHIL	Input Fall Time (Except CLK) (Note 5)	From 2.0 to 0.8 V		12		12	ns

Notes:
1. Signal at 8284A and 8288 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T3 and wait states.
4. Applies only to T2 state (8 ns into T3).
5. Not tested; these specs are controlled by the Teradyne J941 tester.
6. V_{CC} = 4.5 V, 5.5 V V_{IH} = 2.4 V
   V_{IL} = .45 V V_{IHC} = 4.3 V
   V_{ILC} = .25 V V_{OH} = 1.6 V
   V_{OL} = 1.4 V
7. Minimum spec tested at V_{CC} Max. (5.5 V) only.
8. Maximum spec tested at V_{CC} Min. (4.5 V) only.
9. Tested at V_{CC} Max. (5.5 V) only.
10. Tested at V_{CC} Min. (4.5 V) only.
11. Test conditions for TCLCL Max. are:
    V_{CC} = 4.5 V V_{OL} = 1 V
    V_{IL} = 0 V V_{IH} = 4 V
    V_{ILC} = 0 V V_{IHC} = 5 V

SWITCHING CHARACTERISTICS (Cont'd.)

TIMING RESPONSES

Parameter Symbol	Parameter Description	Test Conditions (Note 6)	8086		8086-2		Unit
			Min.	Max.	Min.	Max.	
TCLML	Command Active Delay (Note 1)	C_L = 100 pF for all 8086 Outputs (In addition to 8086 internal loads)	10	35	10	35	ns
TCLMH	Command Inactive Delay (Note 1)		10	35	10	35	ns
TRYHSH	READY Active to Status Passive (Note 3)			110		65	ns
TCHSV	Status Active Delay (Notes 7 & 8)		10	110	10	60	ns
TCLSH	Status Inactive Delay		10	130	10	70	ns
TCLAV	Address Valid Delay		10	110	10	60	ns
TCLAX	Address Hold Time		10		10		ns
TCLAZ	Address Float Delay		10	80	10	50	ns
TSVLH	Status Valid to ALE HIGH (Note 1)			15		15	ns
TSVMCH	Status Valid to MCE HIGH (Note 1)			15		15	ns
TCLLH	CLK LOW to ALE Valid (Note 1)			15		15	ns
TCLMCH	CLK LOW to MCE HIGH (Note 1)			15		15	ns
TCHLL	ALE Inactive Delay (Note 1)			15		15	ns
TCLMCL	MCE Inactive Delay (Note 1)			15		15	ns
TCLDV	Data Valid Delay		10	110	10	60	ns
TCHDX	Data Hold Time		10		10		ns
TCVNV	Control Active Delay (Note 1)		5	45	5	45	ns
TCVNX	Control Inactive Delay (Note 1)		10	45	10	45	ns
TAZRL	Address Float to Read Active		0		0		ns
TCLRL	$\overline{RD}$ Active Delay		10	165	10	100	ns
TCLRH	$\overline{RD}$ Inactive Delay		10	150	10	80	ns
TRHAV	$\overline{RD}$ Inactive to Next Address Active		155		85		ns
TCHDTL	Direction Control Active Delay (Note 1)			50		50	ns
TCHDTH	Direction Control Inactive Delay (Note 1)			30		30	ns
TCLGL	GT Active Delay (Note 8)		0	85	0	50	ns
TCLGH	GT Inactive Delay (Note 8)		0	85	0	50	ns
TRLRH	$\overline{RD}$ Width		325		200		ns
TOLOH	Output Rise Time	From 0.8 to 2.0 V		20		20	ns
TOHOL	Output Fall Time	From 2.0 to 0.8 V		12		12	ns

Notes:
1. Signal at 8284A and 8288 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T3 and wait states.
4. Applies only to T2 state (8 ns into T3).
5. Not tested; these specs are controlled by the Teradyne J941 tester.
6. V_{CC} = 4.5 V, 5.5 V; V_{IH} = 2.4 V; V_{IL} = .45 V; V_{IHC} = 4.3 V; V_{ILC} = .25 V; V_{OH} = 1.6 V; V_{OL} = 1.4 V
7. Minimum spec tested at V_{CC} Max. (5.5 V) only.
8. Maximum spec tested at V_{CC} Min. (4.5 V) only.
9. Tested at V_{CC} Max. (5.5 V) only.
10. Tested at V_{CC} Min. (4.5 V) only.
11. Test conditions for TCLCL Max. are: V_{CC} = 4.5 V; V_{OL} = 1 V; V_{IL} = 0 V; V_{IH} = 4 V; V_{ILC} = 0 V; V_{IHC} = 5 V

8088

8-Bit Microprocessor CPU
iAPX86 Family
MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

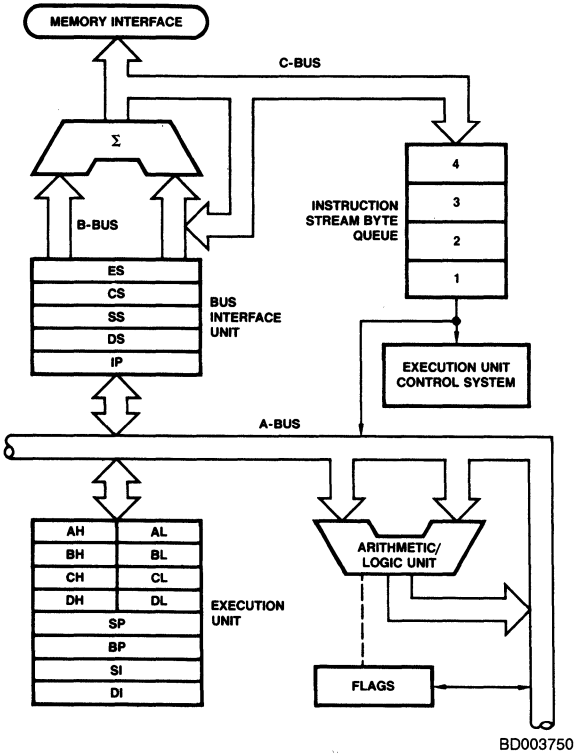
- 8-bit data bus, 16-bit internal architecture
- Directly addresses 1 Mbyte of memory
- Software compatible with 8086 CPU
- Byte, word, and block operations
- 24 operand addressing modes
- Powerful instruction set
- Efficient high level language implementation
- Three block options: 5 MHz 8088
  8 MHz 8088-2

GENERAL DESCRIPTION

The 8088 CPU is an 8-bit processor designed around the 8086 internal structure. Most functions of the 8088 are identical to the equivalent 8086 functions. The pinout is slightly different. The 8088 handles the external bus the same way the 8086 does, but it handles only 8 bits at a time. Sixteen-bit words are fetched or written in two consecutive bus cycles. Both processors will appear identical to the software engineer, with the exception of execution time.

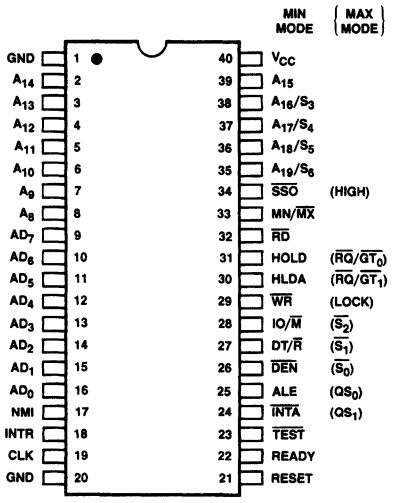
The 8088 is fabricated with N-channel silicon gate technology and is packaged in a 40-pin Ceramic DIP. For complete information, refer to the 8088 Product Specification in the "MOS Microprocessors and Peripherals" Data Book, Order #09067A.

BLOCK DIAGRAM



Publication # 07936 | Rev. B | Amendment /0
Issue Date: December 1987

CONNECTION DIAGRAM
Top View



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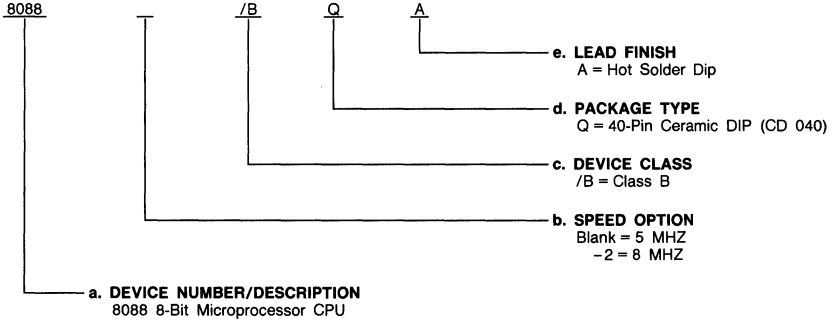
Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
8088	/BQA
8088-2	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature Under Bias ..... 0 to 70°C
Voltage on any Pin
with Respect to Ground ..... −1 to +7.0 V
Power Dissipation ..... 2.5 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... 5 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

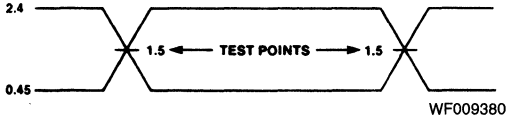
DC CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL} †	Input LOW Voltage	V_{CC} = Min. & Max.	−0.5*	+0.8	V
V_{IH} †	Input HIGH Voltage	V_{CC} = Min. & Max.	2.0	V_{CC} + 0.5*	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.0 mA, V_{CC} = Min.		0.45	V
V_{OH}	Output HIGH Voltage	I_{OH} = −400 μA, V_{CC} = Min.	2.4		V
I_{CC}	Power Supply Current (Note 1)	T_C = 25°C, V_{CC} = Max.		340	mA
I_{LI}	Input Leakage Current	V_{CC} = Max., V_{IN} = 5.5 V & 0 V	−10	10	μA
I_{LO} ††	Output Leakage Current	V_{CC} = Max., V_{OUT} = 5.5 V & 0.45 V	−10	10	μA
V_{CL} †	Clock Input LOW Voltage	V_{CC} = Min. & Max.	−0.5*	+0.6	V
V_{CH} †	Clock Input HIGH Voltage	V_{CC} = Min. & Max.	3.9	V_{CC} + 1.0*	V
C_{IN} †††	Capacitance of Input Buffer (All Input Except AD_0-AD_7, $\overline{RQ}/GT$)	fc = 1 MHz		20*	pF
C_{IO} †††	Capacitance of I/O Buffer (AD_0-AD_7, $\overline{RQ}/GT$)	fc = 1 MHz		20*	pF

* Guaranteed by design; not tested.
† Group A, Subgroups 7 and 8 only are tested.
†† Group A, Subgroups 1 and 2 only are tested.
††† Not included in Group A tests.

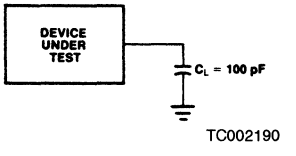
Notes: 1. I_{CC} is measured while running a functional pattern with spec value I_{OL}/I_{OH} loads applied.

SWITCHING TEST INPUT/OUTPUT WAVEFORM



AC TESTING INPUTS ARE DRIVEN AT 2.4 V FOR A LOGIC "1" AND 0.45 V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT 1.5 V FOR BOTH A LOGIC "1" AND "0."

SWITCHING TEST LOAD CIRCUIT



C_L INCLUDES JIG CAPACITANCE

See Section 6 of the MOS Microprocessors and Peripherals Data Book (Order #09067A) for Thermal Characteristics Information.

SWITCHING CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

MINIMUM COMPLEXITY SYSTEM TIMING REQUIREMENTS

Parameter Symbol	Parameter Description	Test Conditions (Note 6)	8088		8088-2		Unit
			Min.	Max.	Min.	Max.	
TCLCL	CLK Cycle Period (Note 11)		200	500	125	500	ns
TCLCH	CLK LOW Time		118		68		ns
TCHCL	CLK HIGH Time		69		44		ns
TCH1CH2	CLK Rise Time (Note 5)	From 1.0 to 3.5 V		10		10	ns
TCL2CL1	CLK Fall Time (Note 5)	From 3.5 to 1.0 V		10		10	ns
TDVCL	Data in Setup Time		30		20		ns
TCLDX	Data in Hold Time		10		10		ns
TR1VCL	RDY Setup Time into 8284A (Notes 1 & 2)		35		35		ns
TCLR1X	RDY Hold Time into 8284A (Notes 1 & 2)		0		0		ns
TRYHCH	READY Setup Time into 8088		118		68		ns
TCHRYX	READY Hold Time into 8088		30		20		ns
TRYLCL	READY Inactive to CLK (Note 4)		−8		−8		ns
THVCH	HOLD Setup Time		35		20		ns
TINVCH	INTR, NMI, TEST Setup Time (Note 2)		30		15		ns
TILIH	Input Rise Time (Except CLK) (Note 5)	From 0.8 to 2.0 V		20		20	ns
TIHIL	Input Fall Time (Except CLK) (Note 5)	From 2.0 to 0.8 V		12		12	ns

Notes:
1. Signal at 8284A and 8288 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T3 and wait states.
4. Applies only to T2 state (8 ns into T3).
5. Not tested; these specs are controlled by the Teradyne J941 tester.
6. V_{CC} = 4.5 V, 5.5 V; V_{IH} = 2.4 V; V_{IL} = .45 V; V_{IHC} = 4.3 V; V_{ILC} = .25 V; V_{OH} = 1.6 V; V_{OL} = 1.4 V
7. Minimum spec tested at V_{CC} Max. (5.5 V) only.
8. Maximum spec tested at V_{CC} Min. (4.5 V) only.
9. Tested at V_{CC} Max. (5.5 V) only.
10. Tested at V_{CC} Min. (4.5 V) only.
11. Test conditions for TCLCL Max. are: V_{CC} = 4.5 V; V_{OL} = 1 V; V_{IL} = 0 V; V_{IH} = 4 V; V_{ILC} = 0 V; V_{IHC} = 5 V

SWITCHING CHARACTERISTICS (Cont'd.)

TIMING RESPONSES

Parameter Symbol	Parameter Description	Test Conditions (Note 6)	8088		8088-2		Unit
			Min.	Max.	Min.	Max.	
TCLAV	Address Valid Delay	C_L = 100 pF for all 8088 Outputs (in addition to internal loads).	10	110	10	60	ns
TCLAX	Address Hold Time (Notes 7 & 8)		10		10		ns
TCLAZ	Address Float Delay (Note 8)		10	80	10	50	ns
TLHLL	ALE Width (Note 10)		98		58		ns
TCLLH	ALE Active Delay (Note 8)			80		50	ns
TCHLL	ALE Inactive Delay (Note 8)			85		55	ns
TLLAX	Address Hold Time to ALE Inactive (Note 7)		59		34		ns
TCLDV	Data Valid Delay (Note 8)		10	110	10	60	ns
TCHDX	Data Hold Time (Note 10)		10		10		ns
TWHDX	Data Hold Time After WR (Note 9)		88		38		ns
TCVCTV	Control Active Delay 1 (Note 8)		10	110	10	70	ns
TCHCTV	Control Active Delay 2 (Note 8)		10	110	10	60	ns
TCVCTX	Control Inactive Delay (Note 8)		10	110	10	70	ns
TAZRL	Address Float to READ Active (Note 9)		0		0		ns
TCLRL	$\overline{RD}$ Active Delay (Note 8)		10	165	10	100	ns
TCLRH	$\overline{RD}$ Inactive Delay (Note 8)		10	150	10	80	ns
TRHAV	$\overline{RD}$ Inactive to Next Address Active (Note 10)		155		85		ns
TCLHAV	HLDA Valid Delay (Note 8)		10	160	10	100	ns
TRLRH	$\overline{RD}$ Width (Note 10)		325		200		ns
TWLWH	$\overline{WR}$ Width (Note 10)		340		210		ns
TAVAL	Address Valid to ALE Low (Note 9)		58		28		ns
TOLOH	Output Rise Time (Note 9)	From 0.8 to 2.0 V		20		20	ns
TOHOL	Output Fall Time (Note 9)	From 2.0 to 0.8 V		12		12	ns

Notes:
1. Signal at 8284A and 8288 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T3 and wait states.
4. Applies only to T2 state (8 ns into T3).
5. Not tested; these specs are controlled by the Teradyne J941 tester.
6. V_{CC} = 4.5 V, 5.5 V; V_{IH} = 2.4 V; V_{IL} = .45 V; V_{IHC} = 4.3 V; V_{ILC} = .25 V; V_{OH} = 1.6 V; V_{OL} = 1.4 V
7. Minimum spec tested at V_{CC} Max. (5.5 V) only.
8. Maximum spec tested at V_{CC} Min. (4.5 V) only.
9. Tested at V_{CC} Max. (5.5 V) only.
10. Tested at V_{CC} Min. (4.5 V) only.
11. Test conditions for TCLCL Max. are: V_{CC} = 4.5 V; V_{OL} = 1 V; V_{IL} = 0 V; V_{IH} = 4 V; V_{ILC} = 0 V; V_{IHC} = 5 V

SWITCHING CHARACTERISTICS (Cont'd.)

MAX MODE SYSTEM (USING 8288 BUS CONTROLLER) TIMING REQUIREMENTS

Parameter Symbol	Parameter Description	Test Conditions (Note 6)	8088		8088-2		Unit
			Min.	Max.	Min.	Max.	
TCLCL	CLK Cycle Period (Note 11)		200	500	125	500	ns
TCLCH	CLK LOW Time		118		68		ns
TCHCL	CLK HIGH Time		68		44		ns
TCH1CH2	CLK Rise Time (Note 5)	From 1.0 to 3.5 V		10		10	ns
TCL2CL1	CLK Fall Time (Note 5)	From 3.5 to 1.0 V		10		10	ns
TDVCL	Data in Setup Time		30		20		ns
TCLDX	Data in Hold Time		10		10		ns
TR1VCL	RDY Setup Time into 8284A (Notes 1 & 2)		35		35		ns
TCLR1X	RDY Hold Time into 8284A (Notes 1 & 2)		0		0		ns
TRYHCH	READY Setup Time into 8088		118		68		ns
TCHRYX	READY Hold Time into 8088		30		20		ns
TRYLCL	READY Inactive to CLK (Note 4)		-8		-8		ns
TINVCH	Setup Time for Recognition (INTR, NMI, $\overline{TEST}$ (Note 2)		30		15		ns
TGVCH	$\overline{RQ}/\overline{GT}$ Setup Time		30		15		ns
TCHGX	$\overline{RQ}$ Hold Time into 8086		40		30		ns
TILIH	Input Rise Time (Except CLK) (Note 5)	From 0.8 to 2.0 V		20		20	ns
TIHIL	Input Fall Time (Except CLK) (Note 5)	From 2.0 to 0.8 V		12		12	ns

Notes:
1. Signal at 8284A and 8288 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognitio
3. Applies only to T3 and wait states.
3. Applies only to T3 and wait states.
4. Applies only to T2 state (8 ns into T3).
5. Not tested; these specs are controlled by the Teradyne J941 tester.
6. V_{CC} = 4.5 V, 5.5 V V_{IH} = 2.4 V
   V_{IL} = .45 V V_{IHC} = 4.3 V
   V_{ILC} = .25 V V_{OH} = 1.6 V
   V_{OL} = 1.4 V
7. Minimum spec tested at V_{CC} Max. (5.5 V) only.
8. Maximum spec tested at V_{CC} Min. (4.5 V) only.
9. Tested at V_{CC} Max. (5.5 V) only.
10. Tested at V_{CC} Min. (4.5 V) only.
11. Test conditions for TCLCL Max. are:
    V_{CC} = 4.5 V V_{OL} = 1 V
    V_{IL} = 0 V V_{IH} = 4 V
    V_{ILC} = 0 V V_{IHC} = 5 V

SWITCHING CHARACTERISTICS (Cont'd.)

TIMING RESPONSES

Parameter Symbol	Parameter Description	Test Conditions (Note 6)	8088		8088-2		Unit
			Min.	Max.	Min.	Max.	
TCLML	Command Active Delay (Note 1)	C_L = 100 pF for all 8088 Outputs (In addition to internal loads)	10	35	10	35	ns
TCLMH	Command Inactive Delay (Note 1)		10	35	10	35	ns
TRYHSH	READY Active to Status Passive (Note 3)			110		65	ns
TCHSV	Status Active Delay (Notes 7 & 8)		10	110	10	60	ns
TCLSH	Status Inactive Delay		10	130	10	70	ns
TCLAV	Address Valid Delay		10	110	10	60	ns
TCLAX	Address Hold Time		10		10		ns
TCLAZ	Address Float Delay		10	80	10	50	ns
TSVLH	Status Valid to ALE HIGH (Note 1)			15		15	ns
TSVMCH	Status Valid to MCE HIGH (Note 1)			15		15	ns
TCLLH	CLK LOW to ALE Valid (Note 1)			15		15	ns
TCLMCH	CLK LOW to MCE HIGH (Note 1)			15		15	ns
TCHLL	ALE Inactive Delay (Note 1)			15		15	ns
TCLMCL	MCE Inactive Delay (Note 1)			15		15	ns
TCLDV	Data Valid Delay		10	110	10	60	ns
TCHDX	Data Hold Time		10		10		ns
TCVNV	Control Active Delay (Note 1)		5	45	5	45	ns
TCVNX	Control Inactive Delay (Note 1)		10	45	10	45	ns
TAZRL	Address Float to Read Active		0		0		ns
TCLRL	$\overline{RD}$ Active Delay		10	165	10	100	ns
TCLRH	$\overline{RD}$ Inactive Delay		10	150	10	80	ns
TRHAV	$\overline{RD}$ Inactive to Next Address Active		155		85		ns
TCHDTL	Direction Control Active Delay (Note 1)			50		50	ns
TCHDTH	Direction Control Inactive Delay (Note 1)			30		30	ns
TCLGL	GT Active Delay (Note 8)			110		50	ns
TCLGH	GT Inactive Delay (Note 8)			85		50	ns
TRLRH	$\overline{RD}$ Width		325		200		ns
TOLOH	Output Rise Time	From 0.8 to 2.0 V		20		20	ns
TOHOL	Output Fall Time	From 2.0 to 0.8 V		12		12	ns

Notes:
1. Signal at 8284A and 8288 shown for reference only.
2. Setup requirement for asynchronous signal only to guarantee recognition at next CLK.
3. Applies only to T3 and wait states.
4. Applies only to T2 state (8 ns into T3).
5. Not tested; these specs are controlled by the Teradyne J941 tester.
6. V_{CC} = 4.5 V, 5.5 V; V_{IH} = 2.4 V; V_{IL} = .45 V; V_{IHC} = 4.3 V; V_{ILC} = .25 V; V_{OH} = 1.6 V; V_{OL} = 1.4 V
7. Minimum spec tested at V_{CC} Max. (5.5 V) only.
8. Maximum spec tested at V_{CC} Min. (4.5 V) only.
9. Tested at V_{CC} Max. (5.5 V) only.
10. Tested at V_{CC} Min. (4.5 V) only.
11. Test conditions for TCLCL Max. are: V_{CC} = 4.5 V; V_{OL} = 1 V; V_{IL} = 0 V; V_{IH} = 4 V; V_{ILC} = 0 V; V_{IHC} = 5 V

8251/Am9551

Programmable Communication Interface
iAPX86 Family
MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

- Separate control and transmit register input buffers
- Synchronous or asynchronous serial data transfer
- Parity, overrun, and framing errors detected
- Half- or full-duplex signaling
- Character length of 5, 6, 7, or 8 bits
- Internal or external synchronization
- Odd parity, even parity, or no parity bit
- Modem interface controlled by processor
  - Programmable Sync pattern
  - Fully TTL-compatible logic levels

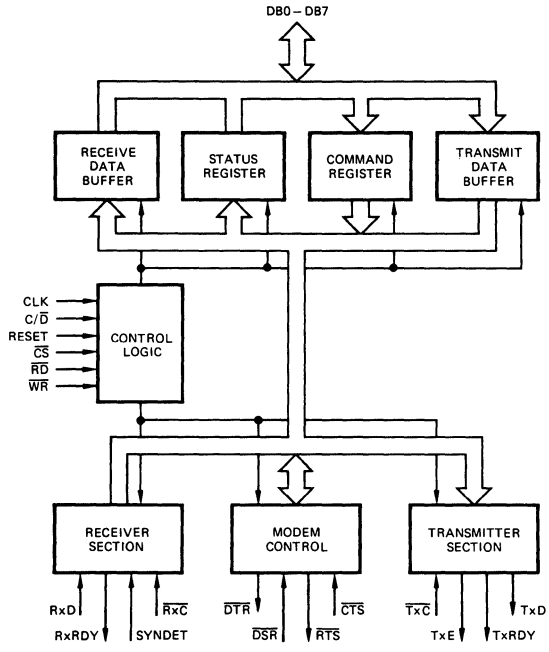
GENERAL DESCRIPTION

The 8251/Am9551 is a programmable serial data communication interface that provides a Universal Synchronous/Asynchronous Receiver/Transmitter (USART) function. It is normally used as a peripheral device for an associated processor and may be programmed by the processor to operate in a variety of standard serial communication formats.

The device accepts parallel data from the CPU, formats and serializes the information based on its current operating mode, and then transmits the data as a serial bit stream. Simultaneously, serial data can be received, converted into parallel form, deformatted, and then presented to the CPU. The USART can operate in an independent full-duplex mode.

Data, control, operation, and format options are all selected by commands from an associated processor. This provides an unusual degree of flexibility and allows the 8251/Am9551 to service a wide range of communication disciplines and applications.

BLOCK DIAGRAM



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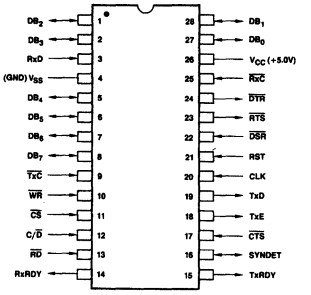
Publication # 09233 | Rev. A | Amendment /0
Issue Date: November 1987

CONNECTION DIAGRAM
Top View

DIPs



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Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

8251 /B X A

e. LEAD FINISH
A = Hot Solder Dip

d. PACKAGE TYPE
X = 28-Pin Ceramic DIP (CD 028)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
8251/Am9551
Programmable Communication Interface
iAPX Family

Valid Combinations	
8251	/BXA
AM9551	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
V_{CC} with Respect to V_{SS} ..... −0.5 to +7.0 V
All Signal Voltages
with Respect to V_{SS} ..... −0.5 V to +7.0 V
Power Dissipation ..... 1.0 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... 5 V ± 10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

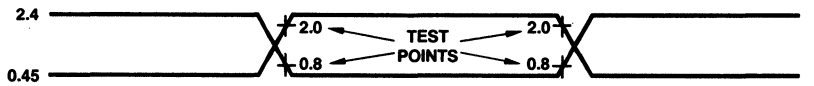
Parameter Symbol	Parameter Description	Test Conditions	8251		Am9551		Unit
			Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = −200 μA, V_{CC} = 4.5 V			2.4		V
		I_{OH} = −100 μA	2.4				
V_{OL}	Output LOW Voltage	I_{OL} = 1.6 mA, V_{CC} = 4.5 V		0.45		0.45	V
V_{IH}	Input HIGH Voltage	V_{CC} = 5 V ± 10%	2.2	V_{CC}*	2.2	V_{CC}*	V
V_{IL}	Input LOW Voltage	V_{CC} = 5 V ± 10%	−0.5*	0.8	−0.5*	0.8	V
I_{LI}	Input Load Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V 0 V		±10		±10	μA
I_{DL}	Data Bus Leakage	V_{OUT} = 0.45 V, V_{CC} = 5.5 V		−50		−50	μA
		V_{OUT} = 5.5 V, V_{CC} = 5.5 V		10		10	
I_{CC}	V_{CC} Supply Current			120		120	mA
C_O †	Output Capacitance	fc = 1.0 MHz, Inputs = 0 V		15*		15*	pF
C_I †	Input Capacitance			10*		10*	pF
$C_{I/O}$ †	I/O Capacitance			20*		20*	pF

* Guaranteed by design; not tested.
† Not included in Group A tests.

Notes: 1. I_{CC} is measured in a static condition with outputs in the worst-case condition with all outputs unloaded.

See Section 6 of the MOS Microprocessors and Peripherals Data Book (Order #09067A) for Thermal Characteristics Information.

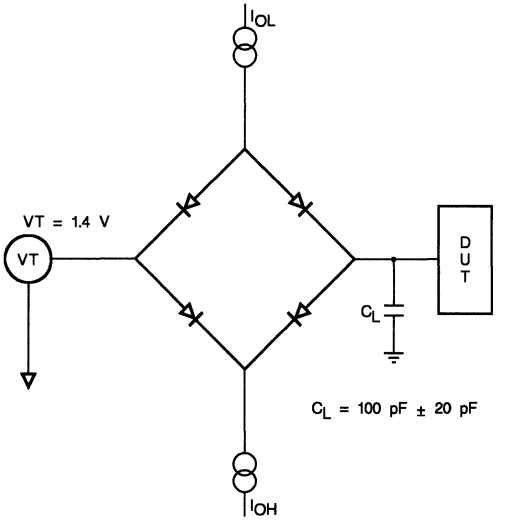
SWITCHING TEST INPUT/OUTPUT WAVEFORM



WF006490

AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0."

SWITCHING TEST CIRCUIT



TC003851

This test circuit is the dynamic load of a Teradyne J941.

SWITCHING CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 4)

Parameter Symbol	Parameter Description		8251 Min.	8251 Max.	Am9551 Min.	Am9551 Max.	Unit
t_{AR}	$\overline{CS}$, C/$\overline{D}$ Stable to $\overline{READ}$ LOW Setup Time		50		50		ns
t_{AW}	$\overline{CS}$, C/$\overline{D}$ Stable to $\overline{WRITE}$ LOW Setup Time		20		20		ns
t_{CR}	$\overline{DSR}$, $\overline{CTS}$ to $\overline{READ}$ LOW Setup Time			16		16	t_{CY}
t_{CY}	Clock Period		0.420	1.35	0.380	1.35	μs
t_{DF}	$\overline{READ}$ HIGH to Data Bus Off Delay		25	200	25	200	ns
t_{DTx}	TxC LOW to TxD Delay			1.0		1.0	μs
t_{DW}	Data to $\overline{WRITE}$ HIGH Setup Time		200		150		ns
t_{ES}	External SYNDET to RxC LOW Setup Time		16		16		t_{CY}
t_{HRx}	Sampling Pulse to Rx Data Hold Time (Note 5)		2.0		2.0		μs
t_{IS}	Data Bit (Center) to Internal SYNDET Delay			30		30	t_{CY}
$t\phi W$	Clock Pulse Width		220	$0.6t_{CY}$	175	$0.6t_{CY}$	ns
t_{RA}	$\overline{READ}$ HIGH to $\overline{CS}$, C/$\overline{D}$ Hold Time		5.0		5.0		ns
t_{RD}	$\overline{READ}$ LOW to Data Bus On Delay			350		250	ns
t_{RPD}	Receiver Clock HIGH Time	1x Baud Rate	15		15		t_{CY}
		16x & 64x Baud Rate	3		3		
t_{RPW}	Receiver Clock LOW Time	1x Baud Rate	12		12		t_{CY}
		16x & 64x Baud Rate	1		1		
t_{RR}	$\overline{READ}$ Pulse Width		430		380		ns
t_{RV}	Time Between $\overline{WRITE}$ Pulses During Initialization (Note 1)		6.0		6.0		t_{CY}
t_{Rx}	Data Bit (Center) to RxRDY Delay			20		20	t_{CY}
t_{SRx}	Rx Data to Sampling Pulse Setup Time (Note 5)		2.0		2.0		μS
t_{TPD}	Transmitter Clock HIGH Time	1x Baud Rate	15		15		t_{CY}
		16x & 64x Baud Rate	3		3		
t_{TPW}	Transmitter Clock LOW Time	1x Baud Rate	12		12		t_{CY}
		16x & 64x Baud Rate	1		1		
t_{TX}	Data Bit (Center) to TxRDY Delay			16		16	t_{CY}
t_{TxE}	Data Bit (Center) to Tx EMPTY Delay			16		16	t_{CY}
t_{WA}	$\overline{WRITE}$ HIGH to $\overline{CS}$, C/$\overline{D}$ Hold Time		20		20		ns
t_{WC}	$\overline{WRITE}$ HIGH to TxE, $\overline{DTR}$, $\overline{RTS}$ Delay			16		16	t_{CY}
t_{WD}	$\overline{WRITE}$ HIGH to Data Hold Time		40		40		ns
t_{WW}	$\overline{WRITE}$ Pulse Width		430		380		ns
f_{Rx}	Receiver Clock Frequency	1x Baud Rate	DC	56	DC	56	kHz
		16x & 64x Baud Rate	DC	520	DC	520	
f_{Tx}	Transmitter Clock Frequency	1x Baud Rate	DC	56	DC	56	kHz
		16x & 64x Baud Rate	DC	520	DC	520	

Notes:
1. This time period between write pulses is specified for initialization purposes only when MODE, SYNC 1, SYNC 2, COMMAND, and first DATA BYTE are written into the Am9551. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1. t_{RV} after internal Reset = 8 * t_{CY}.
2. Reset Pulse Width = $6t_{CY}$ Min.
3. Switching Characteristics parameters are listed in alphabetical order.
4. Clock Rise and Fall times are controlled by the Teradyne J941 tester. Measurement of typical signals generated by the J941 showed $t_R = t_F = 5$ ns.
5. Sampling pulse is internal and not tested; guaranteed by design.

8251A

Programmable Communication Interface
iAPX86 Family
MILITARY INFORMATION

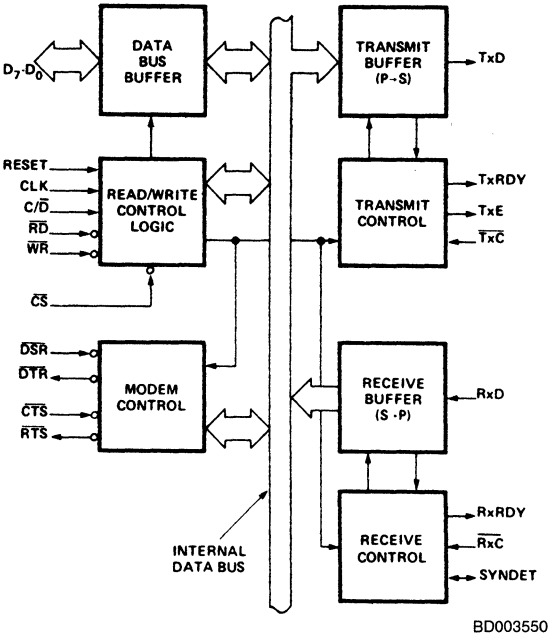
DISTINCTIVE CHARACTERISTICS

- SMD/DESC qualified
- Synchronous and asynchronous operation
- Synchronous 5 – 8-bit characters; internal or external character synchronization; automatic sync insertion
- Asynchronous 5 – 8-bit characters; clock rate – 1, 16, or 64 times baud rate; break character generation: 1, 1 1/2, or 2 stop bits; false start bit detection; automatic break detect and handling
- Synchronous baud rate – DC to 64K baud
- Asynchronous baud rate – DC to 19.2K baud
- Full-duplex, double-buffered transmitter and receiver
- Error detection – parity, overrun, and framing
- Compatible with an extended range of microprocessors
- 28-pin DIP package
- All inputs and outputs are TTL compatible

GENERAL DESCRIPTION

The 8251A is the enhanced version of the industry standard 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for data communications with microprocessor families, such as the iAPX86, 88. The 8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time including data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is fabricated using N-channel silicon gate technology.

BLOCK DIAGRAM



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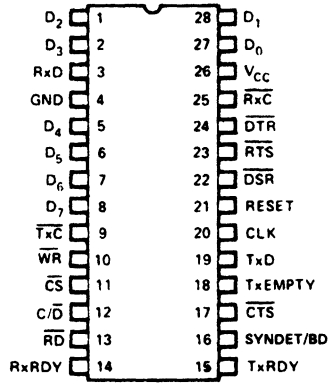
Publication # 07910 | Rev. B | Amendment /0
Issue Date: November 1987

CONNECTION DIAGRAM
Top View



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MILITARY ORDERING INFORMATION

Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of: **a. Military Drawing Part Number**
b. Device Type
c. Case Outline
d. Lead Finish

5962-87548 01 X X

d. LEAD FINISH
X = Any Lead Finish Acceptable

c. CASE OUTLINE
X = 28-Pin Ceramic DIP (CD 028)

b. MILITARY DEVICE TYPE
01 = 2.4 MHz (8251A)

a. MILITARY DRAWING NO./DESCRIPTION
5962-87548
Programmable Communication Interface

Valid Combinations	
5962-8754801	XX

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

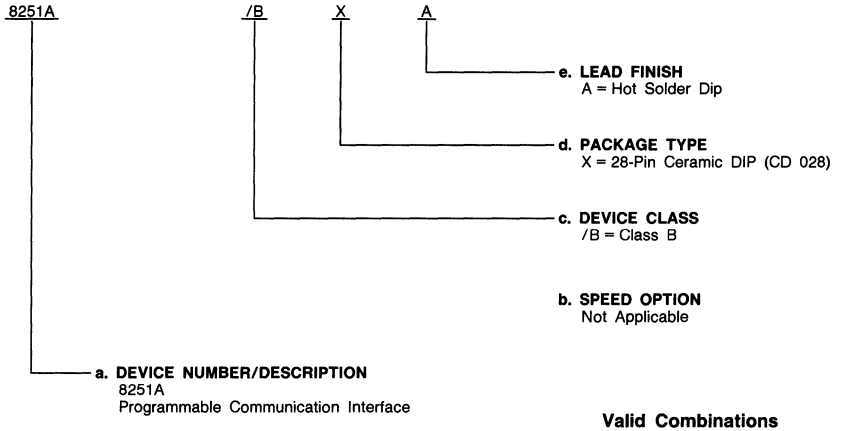
Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

MILITARY ORDERING INFORMATION (Cont'd)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
8251A	/BXA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage on Any Pin
with Respect to Ground ..... −0.5 to +7 V
Power Dissipation ..... 1 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... 5 V ± 10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

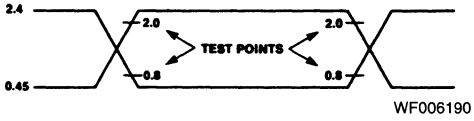
Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage	V_{CC} = 5 V ±10%	−0.5*	0.8	V
V_{IH}	Input HIGH Voltage	V_{CC} = 5 V ±10%	2.2	V_{CC}*	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.2 mA, V_{CC} = 4.5 V		0.45	V
V_{OH}	Output HIGH Voltage	I_{OH} = −400 μA, V_{CC} = 4.5 V	2.4		V
I_{OFL}	Output Float Leakage	V_{OUT} = 5.5 V to 0.45 V, V_{CC} = 5.5 V		±10	μA
I_{IL}	Input Leakage	V_{IN} = 5.5 V to 0.45 V, V_{CC} = 5.5 V		±10	μA
I_{CC}	Power Supply Current	Outputs Unloaded Static (Note 1) V_{CC} = 5.5 V		120	mA

CAPACITANCE (T_C = 25°C, V_{CC} = GND = 0 V)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_{IN}†	Input Capacitance	fc = 1 MHz		10*	pF
$C_{I/O}$†	I/O Capacitance	Unmeasured Pins Returned to GND		20*	pF

* Guaranteed by design.
† Not included in Group A tests.

SWITCHING TEST WAVEFORM



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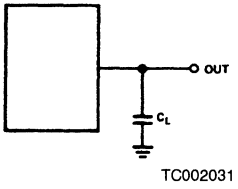
SWITCHING TEST CIRCUIT



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Input/Output

A.C. testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0."

C_L = 100 pF ± 20 pF

SWITCHING CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

BUS PARAMETERS (Notes 2 and 3)

No.	Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
READ CYCLE						
1	t_{AR}	Address Stable Before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)		0		ns
2	t_{RA}	Address Hold Time for $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)		0		ns
3	t_{RR}	$\overline{READ}$ Pulse Width		250		ns
4	t_{RD}	Data Delay from $\overline{READ}$	(Note 4)		200	ns
5	t_{DF}	$\overline{READ}$ to Data Floating		10	250	ns
WRITE CYCLE						
6	t_{AW}	Address Stable Before $\overline{WRITE}$		0		ns
7	t_{WA}	Address Hold Time for $\overline{WRITE}$		20		ns
8	t_{WW}	$\overline{WRITE}$ Pulse Width		250		ns
9	t_{DW}	Data Setup Time for $\overline{WRITE}$		150		ns
10	t_{WD}	Data Hold Time for $\overline{WRITE}$		20		ns
11	t_{RV}	Recovery Time Between WRITES	(Note 5)	6		t_{CY}
OTHER TIMINGS						
12	t_{CY}	Clock Period	(Note 6)	320	1350	ns
13	t_0	Clock HIGH Pulse Width		140	t_{CY}–90	ns
14	$t_{\overline{0}}$	Clock LOW Pulse Width		90		ns
15	t_{DTX}	TxD Delay from Falling Edge of TxC			1	μs
16	f_{TX}	Transmitter Input Clock Frequency 1x Baud Rate		DC	64	kHz
		16x Baud Rate		DC	310	kHz
		64x Baud Rate		DC	615	kHz
17	t_{TPN}	Transmitter Input Clock Pulse Width 1x Baud Rate		12		t_{CY}
		16x and 64x Baud Rate		1		t_{CY}
18	t_{TPD}	Transmitter Input Clock Pulse Delay 1x Baud Rate		15		t_{CY}
		16x and 64x Baud Rate		3		t_{CY}
19	f_{RX}	Receiver Input Clock Frequency 1x Baud Rate		DC	64	kHz
		16x Baud Rate		DC	310	kHz
		64x Baud Rate		DC	615	kHz
20	t_{RPW}	Receiver Input Clock Pulse Width 1x Baud Rate		12		t_{CY}
		16x and 64x Baud Rate		1		t_{CY}
21	t_{RPD}	Receiver Input Clock Pulse Delay 1x Baud Rate		15		t_{CY}
		16x and 64x Baud Rate		3		t_{CY}
22	t_{TxRDY}	TxRDY Pin Delay from Center of Last Bit			12	t_{CY}
23	$t_{TxRDY\ CLEAR}$	TxRDY ↓ from Leading Edge of $\overline{WR}$			400	ns
24	t_{RxRDY}	RxRDY Pin Delay from Center of Last Bit			26	t_{CY}
25	$t_{RxRDY\ CLEAR}$	RxRDY ↓ from Leading Edge of $\overline{RD}$			400	t_{CY}
26	t_{IS}	Internal SYNDET Delay from Rising Edge of $\overline{RxC}$			26	t_{CY}

SWITCHING CHARACTERISTICS (Cont'd.)

No.	Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
27	t_{ES}	External SYNDET Setup Time After Rising Edge of $\overline{RXC}$		16 t_{CY}	$t_{RPD} - t_{CY}$	ns
28	$t_{TxEMPTY}$	TxEMPTY Delay from Center of Last Bit			20	t_{CY}
29	t_{WC}	Control Delay from Rising Edge of WRITE ($\overline{TxEn}$, $\overline{DTR}$, $\overline{RTS}$)			8	t_{CY}
30	t_{CR}	Control to READ Setup Time ($\overline{DSR}$, $\overline{CTS}$)		20		t_{CY}

Notes: 1. I_{CC} is measured in a static condition with outputs in the worst-case condition with all outputs unloaded.
2. Test Conditions: $V_{CC} = 5\ V \pm 10\%$; $V_{IL} = 0.45\ V$, $V_{IH} = 2.4\ V$
$V_{OL} = 0.8\ V$, $V_{OH} = 2.0\ V$ $I_{OL} = 2.2\ mA$, $I_{OH} = -400\ \mu A$
3. Clock Rise and Fall times are controlled by the Teradyne J-941 tester. Measurement of typical signals generated by the J-941 showed $t_R = t_F = 5$ ns.
4. Test condition: $C_L = 100\ pF \pm 20\ pF$, guaranteed by Teradyne J941 DIB.
5. This recovery time is for Mode Initialization only. Write Data is allowed only when TxRDY = 1. Recovery time between Writes for Asynchronous Mode is $8t_{CY}$ and for Synchronous Mode is $16t_{CY}$.
6. Reset Pulse Width = $6t_{CY}$ minimum. System Clock must be running during Reset.

8253

Programmable Interval Timer
iAPX86 Family
MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

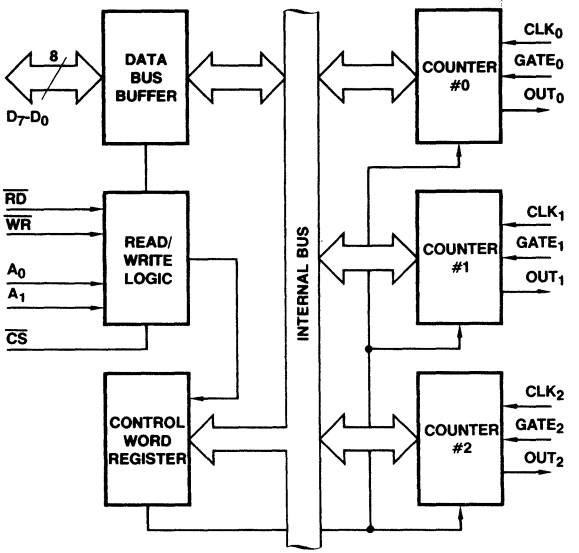
- SMD/DESC qualified
- Both Binary and BCD counting
- Single +5-V supply
- Three independent 16-bit counters
- DC to 5 MHz
- Programmable counter modes
- Bus-oriented I/O

GENERAL DESCRIPTION

The 8253 is a programmable counter/timer chip designed for use with 8080A/8085A microprocessors. It uses NMOS technology with a single +5-V supply and is a direct replacement for Intel's 8253/8253-5.

Each device is organized as three independent 16-bit counters, each counter having a rate of up to 5 MHz. All modes of operation are software-programmable. For improved performance devices, see the Am9513A System Timing Controller.

BLOCK DIAGRAM



BD003760

Power Supplies { +5 V, GND

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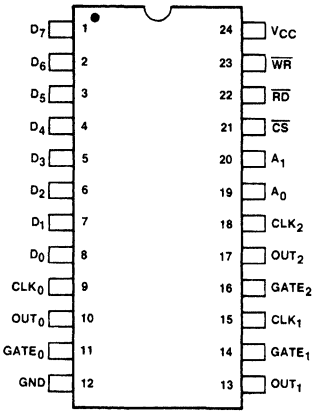
Issue Date: November 1987

CONNECTION DIAGRAM
Top View



CD005671

Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of: **a. Military Drawing Part Number**
b. Device Type
c. Case Outline
d. Lead Finish

5962-87520 | 01 | J | X

d. LEAD FINISH
X = Any Lead Finish Acceptable

c. CASE OUTLINE
J = 24-Pin Ceramic DIP (CD 024)

b. MILITARY DEVICE TYPE
01 = 2.6 MHz; t_{RD} = 300 ns (8253)
03 = 2.6 MHz; t_{RD} = 200 ns (8253-5)

a. MILITARY DRAWING NO./DESCRIPTION
5962-87520
Programmable Interval Timer

Valid Combinations	
5962-8752001	JX
5962-8752003	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

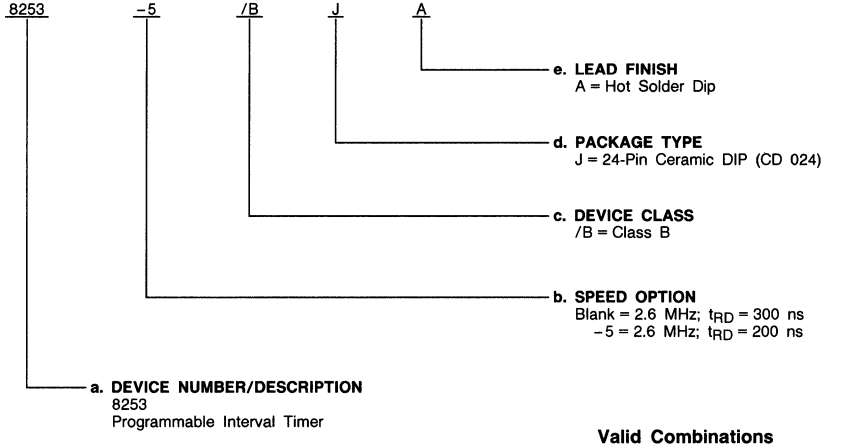
Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

MILITARY ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
8253	/BJA
8253-5	

Group A Tests
Group A Tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage On Any Pin
with Respect to Ground ..... −0.5 to +7.0 V
Power Dissipation ..... 1 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to 125°C
Supply Voltage (V_{CC}) ..... 5 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

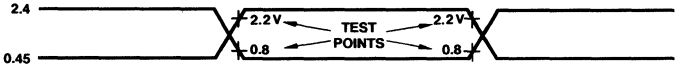
Parameter Symbol	Parameter Description	Test Conditions	8253-5		8253		Unit
			Min.	Max.	Min.	Max.	
V_{IL}	Input LOW Voltage	V_{CC} = 5 V ±10%	−.5*	.7	−.5*	.7	V
V_{IH}	Input HIGH Voltage	V_{CC} = 5 V ±10%	2.2	V_{CC} + .5 V*	2.2	V_{CC} + .5 V*	V
V_{OL}	Output LOW Voltage	I_{OL} = 1.6 mA, V_{CC} = 5 V ±10%		0.45		0.45	V
V_{OH}	Output HIGH Voltage	I_{OH} = −150 μA, V_{CC} = 5 V ±10%	2.4		2.4		V
I_{IL}	Input Load Current	V_{IN} = V_{CC} to 0 V, V_{CC} = Max.		±20		±20	μA
I_{OFL}	Output Float Leakage	V_{OUT} = V_{CC} to 0 V, V_{CC} = Max.		±20		±20	μA
I_{CC}	V_{CC} Supply Current	V_{CC} = Max., Outputs Unloaded Static (Note 1)		140		140	mA

CAPACITANCE T_C = 25°C; V_{CC} = GND = 0 V

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN} †	Input Capacitance	f_c = 1 MHz			10*	pF
$C_{I/O}$ †	I/O Capacitance	Unmeasured pins returned to V_{SS}			20*	pF

*Guaranteed by design; not tested.
†Not included in Group A tests.

SWITCHING TEST WAVEFORM



WF006951

Input

SWITCHING CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 2)

No.	Parameter Symbol	Parameter Description	8253 Min.	8253 Max.	8253-5 Min.	8253-5 Max.	Unit
READ CYCLE							
1	t_{AR}	Address Stable Before $\overline{READ}$	50		30		ns
2	t_{RA}	Address Hold Time for $\overline{READ}$	5		5		ns
3	t_{RR}	$\overline{READ}$ Pulse Width	400		300		ns
4	t_{RD} (Note 3)	Data Delay from $\overline{READ}$		300		200	ns
5	t_{DF}	$\overline{READ}$ to Data Floating	25	125	25	100	ns
6	t_{RV}	Recovery Time Between $\overline{READ}$ and Any Other Control Signal	1		1		μs
WRITE CYCLE							
7	t_{AW}	Address Stable Before $\overline{WRITE}$	50		30		ns
8	t_{WA}	Address Hold Time for $\overline{WRITE}$	30		30		ns
9	t_{WW}	$\overline{WRITE}$ Pulse Width	400		300		ns
10	t_{DW}	Data Setup Time for $\overline{WRITE}$	300		250		ns
11	t_{WD}	Data Hold Time for $\overline{WRITE}$	40		30		ns
12	t_{RV}	Recovery Time Between $\overline{WRITE}$ and Any Other Control Signal	1		1		μs
CLOCK AND GATE TIMING (Note 2)							
13	t_{CLK}	Clock Period	380	DC	380	DC	ns
14	t_{PWH}	HIGH Pulse Width	230		230		ns
15	t_{PWL}	LOW Pulse Width	150		150		ns
16	t_{GW}	Gate Width HIGH	150		150		ns
17	t_{GL}	Gate Width LOW	100		100		ns
18	t_{GS}	Gate Setup Time to CLK↑	100		100		ns
19	t_{GH}	Gate Hold Time After CLK↑	55		55		ns
20	t_{OD} (Note 3)	Output Delay from CLK↓		400		400	ns
21	t_{ODG} (Note 3)	Output Delay from Gate↓		300		300	ns

Notes: 1. I_{CC} is measured in a static condition with no output loads applied.
2. Test Conditions: $V_{CC} = 5\ V \pm 10\%$
$V_{IL} = 0.45\ V$, $V_{IH} = 2.4\ V$
$V_{OL} = 0.8\ V$, $V_{OH} = 2.2\ V$
$I_{OL} = 1.6\ mA$, $I_{OH} = 150\ \mu A$
3. Test Condition: $C_L = 100\ pF \pm 20\ pF$.

82C54

CMOS Programmable Interval Timer

MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

- Compatible with all Intel and most other microprocessors
- High-speed, zero-wait-state operation with 10-MHz 8086/88 and 80186/188
- Three independent 16-bit counters
- Handles inputs from DC to 8 MHz
  - 10 MHz for 82C54-2
  - 12.5 MHz for 82C54-12
- Low-power CMOS
  - I_{CC} = 50 μA military standby current I_{CC}
- Completely TTL compatible
- Six programmable counter modes
- Binary or BCD counting
- Status read-back command
- Available in 24-pin DIP

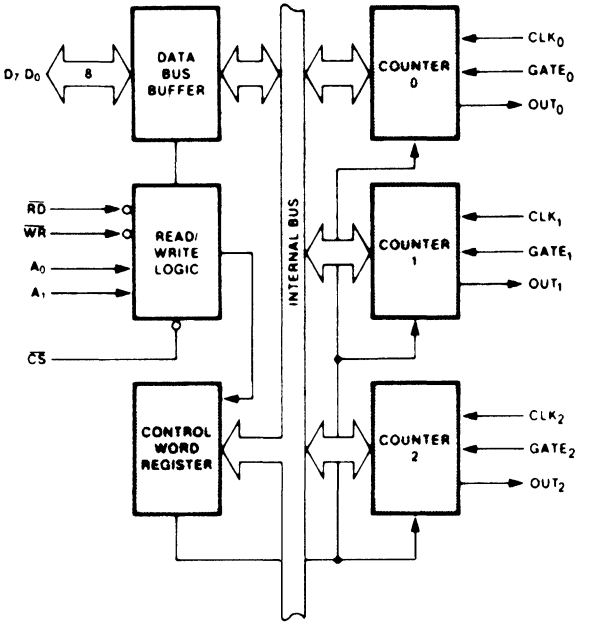
GENERAL DESCRIPTION

The AMD 82C54 is a high-performance, CMOS version of the industry-standard 8254 counter/timer which is designed to solve the timing-control problems common in microcomputer system design. It provides three independent 16-bit Counters — each capable of handling clock inputs up to 12.5 MHz. All modes are software-programmable. The 82C54 is pin-compatible with the NMOS 8254 and is a superset of the 8253.

Six programmable-timer modes allow the 82C54 to be used as an event counter, elapsed time indicator, programmable one-shot, and in many other applications as well.

The 82C54 is fabricated with AMD's CMOS technology providing low-power consumption with performance equal to or greater than the equivalent NMOS product. The 82C54 is available in 24-pin DIP package.

BLOCK DIAGRAM



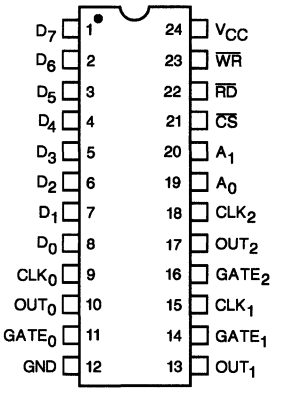
BD006111

Publication #	Rev.	Amendment
09235	A	/0

Issue Date: November 1987

CONNECTION DIAGRAM
Top View

DIP



CD009390

Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

82C54 −12 /B J A

e. LEAD FINISH
A = Hot Solder Dip

d. PACKAGE TYPE
J = 24-Pin Ceramic DIP (CD 024)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Blank = 8 MHz
−2 = 10 MHz
−12 = 12.5 MHz

a. DEVICE NUMBER/DESCRIPTION
82C54
CMOS Programmable Interval Timer

Valid Combinations	
82C54	/BJA
82C54-2	
82C54-12	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage on Any Pin
with Respect to GND ..... −0.5 to +7.0 V
Power Dissipation ..... 1 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... 5 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min.	Max.	Unit
V_{IL}	Input LOW Voltage			−0.5*	0.8	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}+0.5 V*	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.0 mA			.45	V
V_{OH}	Output HIGH Voltage	I_{OH} = −400 µA		2.4		V
I_{IL}	Input Load Current	V_{IN} = V_{CC} to 0 V			±10	µA
I_{OFL}	Output Float Leakage Current	V_{OUT} = V_{CC} to 0 V			±10	µA
I_{CC}	Operating Power-Supply Current (Note 1)	CLK Freq =	8 MHz		20	mA
			10 MHz		20	
			12.5 MHz		20	
I_{CCSB}	Standby Power-Supply Current (Note 2)	CLK Freq = DC, $\overline{CS}$ = HIGH, All Inputs/Data Bus HIGH, All Outputs Floating			±50	µA

CAPACITANCE (T_C = 25°C, V_{CC} = GND = 0 V)

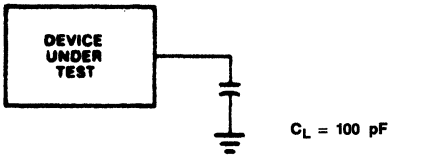
Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
C_{IN} †	Input Capacitance	fc = 1 MHZ Unmeasured pins returned to GND		10*	pF
$C_{I/O}$ †	I/O Capacitance			20*	pF
C_{OUT} †	Output Capacitance			20*	pF

* Guaranteed by design; not tested.
† Not included in Group A tests.

Notes: 1. I_{CC} is measured in a dynamic condition with no output loads applied and inputs at rail levels.
2. Standby I_{CC} is measured in a static condition (CLK = DC) with no output loads applied, and $\overline{CS}$ and all inputs/databus at the V_{CC} rail level.

See Section 6 of the MOS Microprocessors and Peripherals Data Book (Order #09067A) for Thermal Characteristics Information.

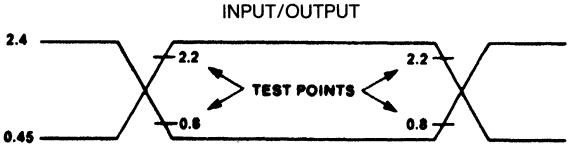
SWITCHING TEST CIRCUIT



TC003431

C_L = 100 pF
C_L includes jig capacitance

SWITCHING TEST WAVEFORM



WF021041

A.C. Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." Timing measurements are made at 2.2 V for a logic "1" and 0.8 V for a logic "0."

SWITCHING CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 1).

No.	Parameter Symbol	Parameter Description	8 MHz		10 MHz		12.5 MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE									
1	t_{AR}	Address Stable Before $\overline{RD}$ ↓	45		30		25		ns
2	t_{SR}	$\overline{CS}$ Stable Before $\overline{RD}$ ↓	0		0		0		ns
3	t_{RA}	Address Hold Time After $\overline{RD}$ ↑	0		0		0		ns
4	t_{RR}	$\overline{RD}$ Pulse Width	150		95		90		ns
5	t_{RD}	Data Delay from $\overline{RD}$ ↓		120		85		80	ns
6	t_{AD}	Data Delay from Address		220		185		150	ns
7	t_{DF}	$\overline{RD}$ ↑ to Data Floating	5	90	5	65	5	55	ns
8	t_{RV}	Command Recovery Time	200		165		135		ns
WRITE CYCLE									
9	t_{AW}	Address Stable Before $\overline{WR}$ ↓	0		0		0		ns
10	t_{SW}	$\overline{CS}$ Stable Before $\overline{WR}$ ↓	0		0		0		ns
11	t_{WA}	Address Hold Time After $\overline{WR}$ ↑	0		0		0		ns
12	t_{WW}	$\overline{WR}$ Pulse Width	150		95		80		ns
13	t_{DW}	Data Setup Time Before $\overline{WR}$ ↑	120		95		80		ns
14	t_{WD}	Data Hold Time After $\overline{WR}$ ↑	0		0		0		ns
15	t_{RV}	Command Recovery Time	200		165		135		ns
CLOCK AND GATE CYCLE									
16	t_{CLK}	Clock Period	125	DC	100	DC	80	DC	ns
17	t_{PWH}	HIGH Pulse Width (Note 3)	60		30		30		ns
18	t_{PWL}	LOW Pulse Width (Note 3)	60		50		40		ns
19	t_R	Clock Rise Time (Note 4)		25		25		25	ns
20	t_F	Clock Fall Time (Note 4)		25		25		25	ns
21	t_{GW}	Gate Width HIGH	50		50		40		ns
22	t_{GL}	Gate Width LOW	50		50		40		ns
23	t_{GS}	Gate Setup Time to CLK ↑	50		40		30		ns
24	t_{GH}	Gate Hold Time After CLK ↑ (Note 2)	50		50		40		ns
25	t_{OD}	Output Delay from CLK ↓		150		100		80	ns
26	t_{ODG}	Output Delay from Gate ↓		120		100		80	ns
27	t_{WC}	CLK Delay for Loading	0	55	0	55	0	45	ns
28	t_{WG}	Gate Delay for Sampling	−5	50	−5	40	−5	35	ns
29	t_{WO}	Out Delay from Mode Write		260		240		200	ns
30	t_{CL}	CLK Set Up for Count Latch	−4	45	−4	40	−4	35	ns

Notes: 1. Timings measured at V_{OH} = 2.2 V, V_{OL} = 0.8 V. C_L = 100 pF ±20 pF.
2. In Modes 1 and 5, triggers are sampled on each rising clock edge. A second trigger within 120 ns (70 ns for the 82C54-2) of the rising clock edge may not be detected.
3. LOW-going glitches that violate t_{PWH}, t_{PWL} may cause errors requiring Counter re-programming.
4. Clock rise and fall times are tested at 5 ns, guaranteed by Teradyne J941 test equipment.

8255A

Programmable Peripheral Interface
iAPX86 Family
MILITARY INFORMATION

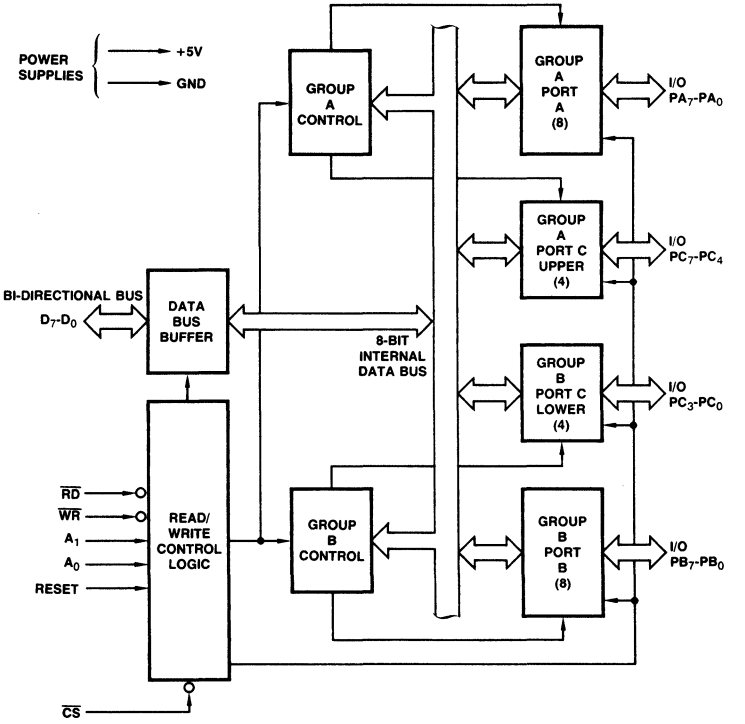
DISTINCTIVE CHARACTERISTICS

- SMD/DESC qualified
- Direct bit set/reset capability easing control application interface
- Reduces system package count
- Improved DC driving capability
- 24 programmable I/O pins
- Completely TTL-compatible
- Fully compatible with the iAPX86 microprocessor family
- Improved timing characteristics

GENERAL DESCRIPTION

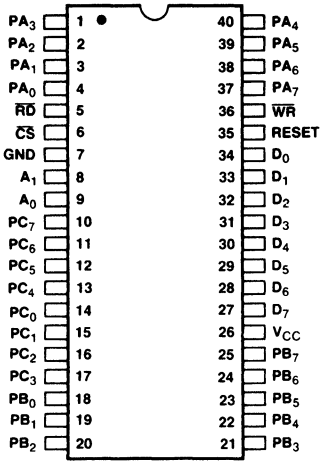
The 8255A is a general-purpose, programmable I/O device designed for use with iAPX Family microprocessors. It has 24 I/O pins which may be individually programmed in two groups of twelve, and used in three major modes of operation. In the first mode, each group of twelve I/O pins may be programmed in sets of four and eight to be input or output. In Mode 1, the second mode, each group may be programmed to have eight lines of input or output. Of the remaining four pins, three are used for handshaking and interrupt control signals. The third mode of operation (Mode 2) is a bidirectional bus mode which uses eight lines for a bidirectional bus, and five lines, borrowing one from the other group, for handshaking.

BLOCK DIAGRAM



Publication # 07912 | Rev. B | Amendment /0
Issue Date: November 1987

CONNECTION DIAGRAM
Top View



CD005401

Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of: **a. Military Drawing Part Number**
b. Device Type
c. Case Outline
d. Lead Finish

5962-87570 01 Q X

d. LEAD FINISH
X = Any Lead Finish Acceptable

c. CASE OUTLINE
Q = 40-Pin Ceramic DIP (CD 040)

b. MILITARY DEVICE TYPE
01 = 2.5 MHz (8255A)
02 = 3.3 MHz (8255A-5)

a. MILITARY DRAWING NO./DESCRIPTION
5962-87570
Programmable Peripheral Interface

Valid Combinations	
5962-8757001	QX
5962-8757002	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

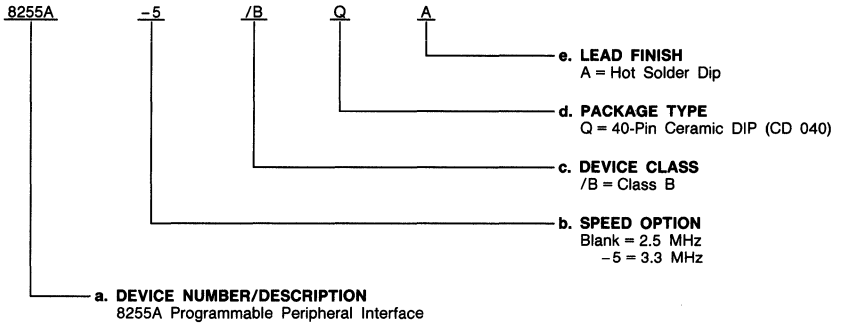
Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

MILITARY ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
8255A	/BQA
8255A-5	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
V_{CC} with Respect to V_{SS} ..... −0.5 to 7.0 V
All Signal Voltages
with Respect to V_{SS} ..... −0.5 to +7.0 V
Power Dissipation ..... 1.0 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (TC) ..... −55 to 125°C
Supply Voltage (V_{CC}) ..... 5 V ± 10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

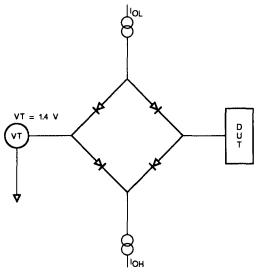
Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}†	Input Low Voltage	V_{CC} = 4.5 V	−0.5 *	0.8	V
V_{IH}†	Input High Voltage	V_{CC} = 5.5 V	2.2	5.5*	V
V_{OL}(DB)	Output Low Voltage (Data Bus)	I_{OL} = 2.5 mA, V_{CC} = 5.5 V		0.45	V
V_{OL}(PER)	Output Low Voltage (Peripheral Port)	I_{OL} = 1.7 mA, V_{CC} = 5.5 V		0.45	V
V_{OH}(DB)	Output High Voltage (Data Bus)	I_{OH} = −400 μA, V_{CC} = 4.5 V	2.4		V
V_{OH}(PER)	Output High Voltage (Peripheral Port)	I_{OH} = −200 μA, V_{CC} = 4.5 V	2.4		V
I_{DAR}	Darlington Drive Current (Note 1)	R_{EXT} = 750 Ω, V_{EXT} = 1.5 V	−1.0	−4.0	mA
I_{CC}	Power Supply Current (Note 2)	V_{CC} = 5.5 V		120	mA
I_{IL}	Input Load Current	V_{IN} = V_{CC} to 0 V, V_{CC} = 5.5 V		±10	μA
I_{OFL}	Output Float Leakage	V_{OUT} = V_{CC} to 0 V, V_{CC} = 5.5 V		±10	μA

CAPACITANCE T_C = 25°C; V_{CC} = GND = 0 V

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}††	Input Capacitance	fc = 1 MHz			15*	pF
$C_{I/O}$††	I/O Capacitance	Unmeasured pins returned to GND			25*	pF

*Guaranteed by design; not tested.
†Group A, Subgroups 9, 10, 11 only are tested.
††Not included in Group A tests.
Notes: 1. Available on any 8 pins from Port B and C.
2. I_{CC} test conditions: the supply current is measured with loaded outputs while running AC patterns.

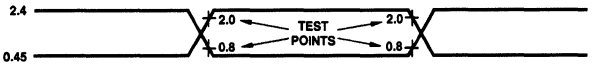
SWITCHING TEST CIRCUIT



TC003850

This test circuit is the dynamic load of a Teradyne J941.

SWITCHING TEST WAVEFORM



WF006351

AC testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0."
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0."

See Section 6 of the MOS Microprocessors and Peripherals Data Book (Order #09067A) for Thermal Characteristics Information.

SWITCHING CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (Note 1)

BUS PARAMETERS

No.	Parameter Symbol	Parameter Description	8255A		8255A-5		Unit
			Min.	Max.	Min.	Max.	
READ							
1	t_{AR}	Address Stable Before READ	0		0		ns
2	t_{RA}	Address Stable After READ	0		0		ns
3	t_{RR}	READ Pulse Width	300		300		ns
4	t_{RD}	Data Valid From READ (Note 1)		250		200	ns
5	t_{DF}	Data Float After READ (Note 3)	10	150	10	100	ns
6	t_{RV}	Time Between READs and/or WRITEs	850		850		ns
WRITE							
7	t_{AW}	Address Stable Before WRITE	0		0		ns
8	t_{WA}	Address Stable After WRITE	20		20		ns
9	t_{WW}	WRITE Pulse Width	400		300		ns
10	t_{DW}	Data Valid to WRITE (T.E.)	100		100		ns
11	t_{WD}	Data Valid After WRITE	30		30		ns
OTHER TIMINGS							
12	t_{WB}	WR = 1 to Output (Note 1)		350		350	ns
13	t_{IR}	Peripheral Data Before RD	0		0		ns
14	t_{HR}	Peripheral Data After RD	0		0		ns
15	t_{AK}	ACK Pulse Width	300		300		ns
16	t_{ST}	STB Pulse Width	500		500		ns
17	t_{PS}	Per. Data Before T.E. of STB	0		0		ns
18	t_{PH}	Per. Data After T.E. of STB	180		180		ns
19	t_{AD}	ACK = 0 to Output (Note 1)		300		300	ns
20	t_{KD}	ACK = 1 to Output Float (Note 3)	20	250	20	250	ns
21	t_{WOB}	WR = 1 to OBF = 0 (Note 1)		650		650	ns
22	t_{AOB}	ACK = 0 to OBF = 1 (Note 1)		350		350	ns
23	t_{SIB}	STB = 0 to IBF = 1 (Note 1)		300		300	ns
24	t_{RIB}	RD = 1 to IBF = 0 (Note 1)		300		300	ns
25	t_{RIT}	RD = 0 to INTR = 0 (Note 1)		400		400	ns
26	t_{SIT}	STB = 1 to INTR = 1 (Note 1)		300		300	ns
27	t_{AIT}	ACK = 1 to INTR = 1 (Note 1)		350		350	ns
28	t_{WIT}	WR = 1 to INTR = 0 (Note 1)		450		450	ns

Notes: 1. Test Conditions: V_{CC} = 5.5 V and 4.5 V, V_{IH} = 2.4 V, V_{IL} = .45 V, V_{OH} = 2.0 V, V_{OL} = .8 V, C_L = 100 pF ± 20 pF.

2. Period of Reset pulse must be at least 50 μs during or after power on. Subsequent Reset pulse can be 500 ns min.

3. AC float timing parameters t_{DF} and t_{KD} are tested Logic 0 to float only.

8259A

Programmable Interrupt Controller
iAPX86 Family
MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

- SMD/DESC qualified
- Eight-level priority controller
- Expandable to 64 levels
- Programmable interrupt modes
- Individual request mask capability
- Single +5-V supply (no clocks)
- 28-pin dual-in-line package

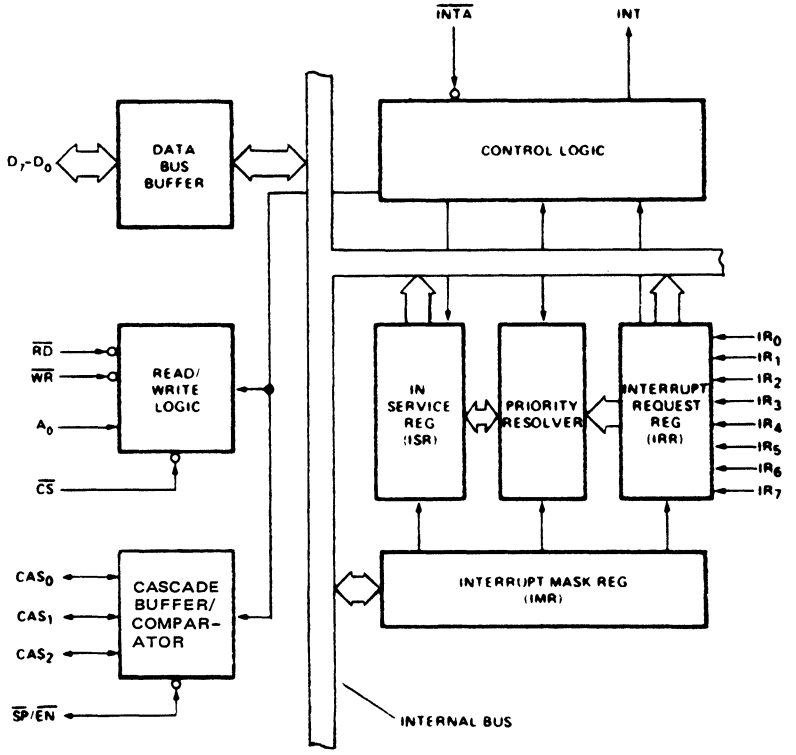
GENERAL DESCRIPTION

The 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology, and requires a single +5-V supply. Circuitry is static, requiring no clock input.

The 8259A is designed to minimize the software and real-time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

The 8259A is fully upward-compatible with the 8259. Software originally written for the 8259 will operate the 8259A in all 8259-equivalent modes.

BLOCK DIAGRAM



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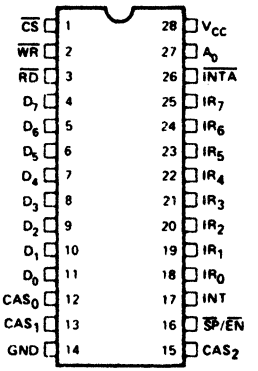
CONNECTION DIAGRAM
Top View



CD005642

Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

Standard Military Drawing (SMD)/DESC Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. Standard Military Drawing (SMD)/DESC products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for SMD/DESC products is formed by a combination of: **a. Military Drawing Part Number**
b. Device Type
c. Case Outline
d. Lead Finish

5962-87518 — 01 — X — X

d. LEAD FINISH
X = Any Lead Finish Acceptable

c. CASE OUTLINE
X = 28-Pin Ceramic DIP (CD 028)

b. MILITARY DEVICE TYPE
01 = 5 MHz (8259A)

a. MILITARY DRAWING NO./DESCRIPTION
5962-87518
Programmable Interrupt Controller

Valid Combinations	
5962-8751801	XX

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

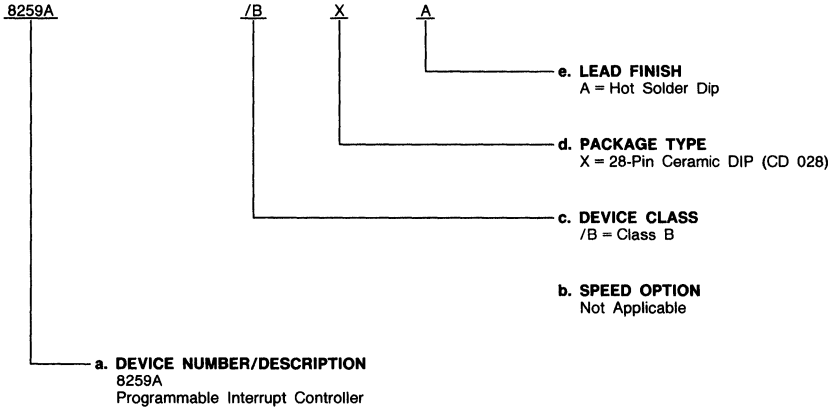
Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

MILITARY ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
8259A	/BXA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of subgroups 1, 2, 3, 7, 8, 9 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage on Any Pin
with Respect to Ground ..... −0.5 V to +7 V
Power Dissipation ..... 1 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to 125°C
Supply Voltage (V_{CC}) ..... 5 V ± 10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage	V_{CC} = 4.5 V to 5.5 V	−0.5*	0.8	V
V_{IH}	Input HIGH Voltage	V_{CC} = 4.5 V to 5.5 V	2.3	V_{CC} + 0.5 V*	V
V_{OL}	Output LOW Voltage	I_{OL} = 2.2 mA, V_{CC} = 4.5 V		0.45	V
V_{OH}	Output HIGH Voltage	I_{OH} = −400 μA, V_{CC} = 4.5 V	2.4		V
$V_{OH(INT)}$	Interrupt Output HIGH Voltage	I_{OH} = −100 μA, V_{CC} = 4.5 V	3.5		V
		I_{OH} = −400 μA, V_{CC} = 4.5 V	2.4		V
I_{LI}	Input Load Current	V_{CC} = 5.5 V, V_{IN} = 5.5 V and 0 V	−10	+10	μA
I_{LOL}, I_{LOH}	Output Leakage Current	V_{CC} = 5.5 V, V_{OUT} = 5.5 V and 0.45 V	−10	+10	μA
I_{CC}	V_{CC} Supply Current	V_{CC} = 5.5 V (Note 1)		125	mA

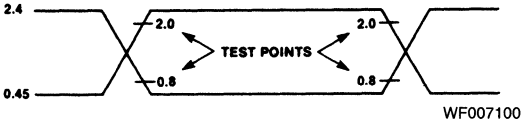
Notes: 1. I_{CC} measured in a static condition with outputs in a worst-case state, having standard I_{OL}/I_{OH} loads applied.

CAPACITANCE (T_C = 25°C, V_{CC} = GND = 0 V)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_{IN}†	Input Capacitance	fc = 1 MHz		10*	pF
$C_{I/O}$†	I/O Capacitance	Unmeasured pins returned to V_{SS}		20*	pF

*Guaranteed by design; not tested.
†Not included in Group A tests.

SWITCHING TEST WAVEFORM



WF007100

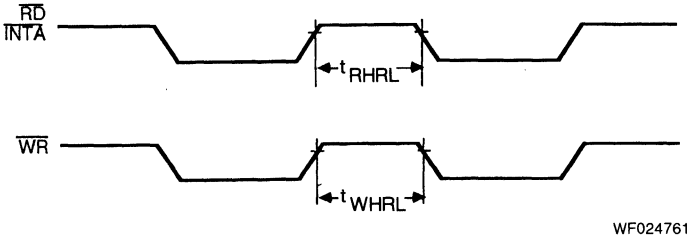
Input/Output

Note: AC testing inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0." Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0."

SWITCHING CHARACTERISTICS over operating range (for SMD/DESC and APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted).

No.	Parameter Symbol	Parameter Description	Test Conditions	8259A Min.	8259A Max.	Unit
TIMING REQUIREMENTS						
1	t_{AHRL}	$A_0/\overline{CS}$ Setup to $\overline{RD}/\overline{INTA}\downarrow$	(Note 1)	0		ns
2	t_{RHAX}	$A_0/\overline{CS}$ Hold after $\overline{RD}/\overline{INTA}\uparrow$		0		ns
3	t_{RLRH}	$\overline{RD}$ Pulse Width		235		ns
4	t_{AHWL}	$A_0/\overline{CS}$ Setup to $\overline{WR}\downarrow$		0		ns
5	t_{WHAX}	$A_0/\overline{CS}$ Hold after $\overline{WR}\uparrow$		0		ns
6	t_{WLWH}	$\overline{WR}$ Pulse Width		290		ns
7	t_{DVWH}	Data Setup to $\overline{WR}\uparrow$		240		ns
8	t_{WHDX}	Data Hold after $\overline{WR}\uparrow$		0		ns
9	t_{JLJH}	Interrupt Request Width (LOW)		100		ns
10	t_{CVIAL}	Cascade Setup Second or Third $\overline{INTA}\downarrow$ (Slave Only)		55		ns
11	t_{RHRL}	End of $\overline{RD}$ to next Command		300		ns
12	t_{WHRL}	End of $\overline{WR}$ to next Command		370		ns
TIMING RESPONSES						
13	t_{RLDV}	Data Valid from $\overline{RD}/\overline{INTA}\downarrow$	(Notes 1 and 2)		200	ns
14	t_{RHDZ}	Data Float after $\overline{RD}/\overline{INTA}\uparrow$		10	100	ns
15	t_{JHIH}	Interrupt Output Delay			350	ns
16	t_{IALCV}	Cascade Valid from First $\overline{INTA}\downarrow$ (Master Only)			565	ns
17	t_{RLEL}	Enable Active from $\overline{RD}\downarrow$ or $\overline{INTA}\downarrow$			125	ns
18	t_{RHEH}	Enable Inactive from $\overline{RD}\uparrow$ or $\overline{INTA}\uparrow$			150	ns
19	t_{AHDV}	Data Valid from Stable Address			200	ns
20	t_{CVDV}	Cascade Valid to Valid Data			300	ns

Notes: 1. Test Conditions: V_{CC} = 4.5 V to 5.5 V
V_{IL} = 0.45 V, V_{IH} = 2.4 V; V_{OL} = 0.8 V, V_{OH} = = 2.0 V
I_{OL} = 2.2 mA, I_{OH} = −400 μA
2. Test Condition: C_L = 100 pF ±20 pF.



WF024761

Other Timing (Military)

CHAPTER 4

* DESC approved
** Pending DESC approval

8031AH

Single-Chip 8-Bit Microcontroller

MILITARY INFORMATION

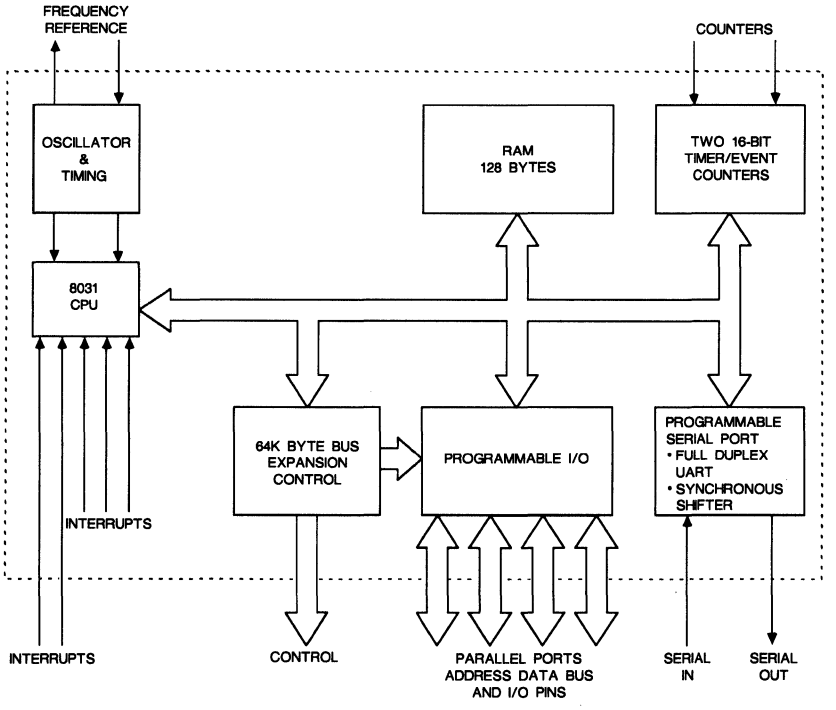
DISTINCTIVE CHARACTERISTICS

- 128 x 8 RAM
- Four 8-bit ports, 32 I/O lines
- Two 16-bit timer/event counters
- 64K addressable Program Memory
- All versions are pin-compatible
- Boolean processor
- Programmable Serial Port
- Five interrupt sources/two priority levels
- On-chip Oscillator/Clock Circuit
- 64K addressable Data Memory

GENERAL DESCRIPTION

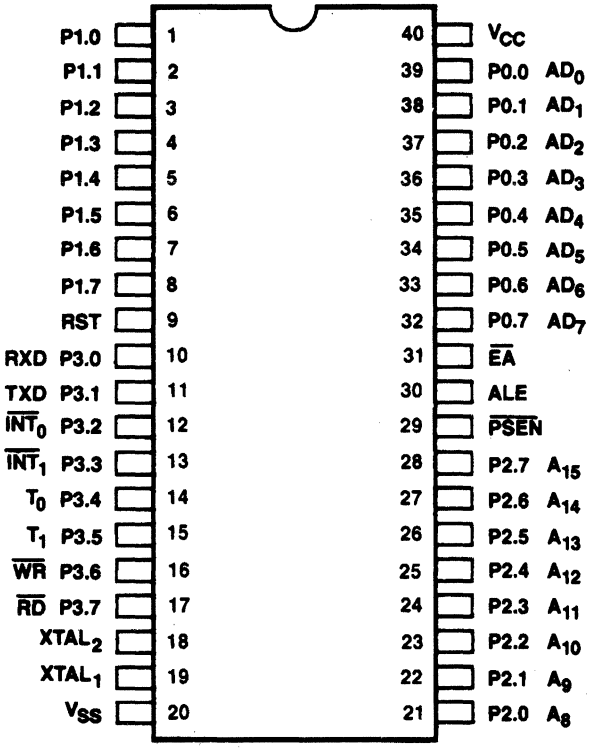
The 8031AH is optimized for control applications. Byte processing and numerical operations on small data structures are facilitated by a variety of fast addressing modes for accessing the internal RAM. The instruction set provides a convenient menu of 8-bit arithmetic instructions, including multiply and divide instructions. Extensive on-chip support is provided for 1-bit variables as a separate data type. This allows direct bit manipulation and testing in control and logic systems that require Boolean processing. Efficient use of program memory results from an instruction set consisting of 44% 1-byte, 41% 2-byte, and 15% 3-byte instructions. With a 12 MHz crystal, 58% of the instructions execute in 1 μs, 40% in 2 μs, and multiply and divide require only 4 μs.

BLOCK DIAGRAM



Publication # 09399 | Rev. A | Amendment /0
Issue Date: December 1987

CONNECTION DIAGRAM
Top View

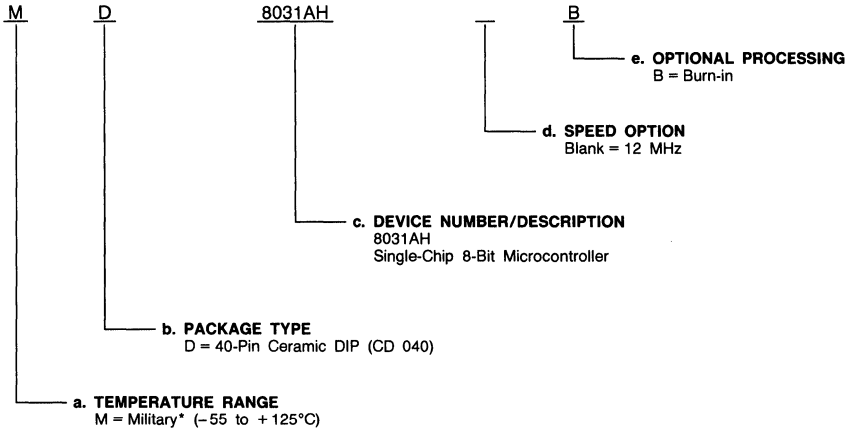


CD005551

Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Temperature Range**
b. Package Type
c. Device Number
d. Speed Option
e. Optional Processing



Valid Combinations	
MD	8031AHB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

*Military temperature range products are NPL (Non-Compliant Products List) or Non-MIL-STD-883C Compliant Products only.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage on Any Pin
with Respect to Ground ..... −0.5 to +7.0 V
Power Dissipation ..... 1 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V
Ground (V_{SS}) ..... 0 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage		−0.5	0.7	V
V_{IH}	Input HIGH Voltage (Except RST/V_{PD} and $XTAL_2$)		2.2	V_{CC} +0.5	V
V_{IH1}	Input HIGH Voltage to RST/V_{PD}, $XTAL_2$	$XTAL_1 = V_{SS}$	2.8	V_{CC} +0.5	V
V_{PD}	Power-Down Voltage to RST/V_{PD}	V_{CC} = 0 V	4.5	5.5	V
V_{OL}	Output LOW Voltage, Ports 1, 2, 3 (Note 1)	I_{OL} = 1.2 mA		0.45	V
V_{OL1}	Output LOW Voltage, Port 0, ALE, $\overline{PSEN}$ (Note 1)	I_{OL} = 2.4 mA		0.45	V
V_{OH}	Output HIGH Voltage, Ports 1, 2, 3	I_{OH} = −60 μA	2.4		V
V_{OH1}	Output HIGH Voltage, Port 0, ALE, $\overline{PSEN}$	I_{OH} = −400 μA	2.4		V
I_{IL}	Logical 0 Input Current, Ports 1, 2, 3	V_{IL} = 0.45 V		−800	μA
I_{IL2}	Logical 0 Input Current for $XTAL_2$	$XTAL_1 = V_{SS}$ V_{IN} = 0.45 V		−3.2	mA
I_{IH1}	Input HIGH Current to RST/V_{PD} for Reset	$V_{IN} < (V_{CC} - 1.5\ V)$		600	μA
I_{LI}	Input Leakage Current to Port 0, $\overline{EA}$	$0.45 < V_{IN} < V_{CC}$		±10	μA
I_{CC}	Power-Supply Current	$\overline{EA} = V_{CC}$		140	mA
I_{PD}	Power-Down Current	V_{CC} = 0 V; V_{PO} = 5.0 V		15	mA
C_{IO}	Capacitance of I/O Buffer	fc = 1 MHz		10	pF

Notes: 1. Capacitive load on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.

See Section 6 of the MOS Microprocessors and Peripherals Data Book (Order #09067A) for Thermal Characteristics Information.

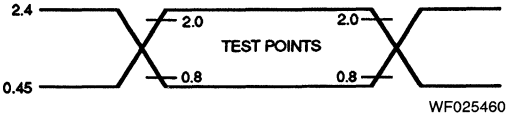
SWITCHING CHARACTERISTICS over operating range (Load Capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF; Load Capacitance for all other outputs = 80 pF)

Parameter Symbol	Parameter Description	12-MHz Clock		Variable Clock		Unit
		Min.	Max.	Min.	Max.	
TCY 1/TCLCL	Oscillator Frequency			3.5TCLCL	12TCLCL	MHz
TLHLL	ALE Pulse Width	112		2TCLCL–55		ns
TAVLL	Address Setup to ALE	28		TCLCL–55		ns
TLLAX	Address Hold After ALE	33		TCLCL–50		ns
TLLIV	ALE to Valid Instruction In		218		4TCLCL–115	ns
TLLPL	ALE to $\overline{PSEN}$	43		TCLCL–40		ns
TPLPH	$\overline{PSEN}$ Pulse Width	190		3TCLCL–60		ns
TPLIV	$\overline{PSEN}$ to Valid Instruction In		150		3TCLCL–140	ns
TPXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
TPXIZ	Input Instruction Float After $\overline{PSEN}$		48		TCLCL–35	ns
TPXAV	Address Valid After $\overline{PSEN}$	58		TCLCL–25		ns
TAVIV	Address to Valid Instruction In		287		5TCLCL–130	ns
TPLAZ	Address Float After $\overline{PSEN}$		20		20	ns
TRLRH	$\overline{RD}$ Pulse Width	400		6TCLCL–100		ns
TWLWH	$\overline{WR}$ Pulse Width	400		6TCLCL–100		ns
TRLDV	$\overline{RD}$ to Valid Data In		232		5TCLCL–185	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		ns
TRHDZ	Data Float After $\overline{RD}$		82		2TCLCL–85	ns
TLLDV	ALE to Valid Data In		497		8TCLCL–170	ns
TAVDV	Address to Valid Data In		565		9TCLCL–185	ns
TLLWL	ALE to $\overline{WR}$ or $\overline{RD}$	185	315	3TCLCL–65	3TCLCL+65	ns
TAVWL	Address to $\overline{WR}$ or $\overline{RD}$	188		4TCLCL–145		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	8		TCLCL–75		ns
TQVWH	Data Setup Before $\overline{WR}$	508		7TCLCL–75		ns
TWHQX	Data Hold After $\overline{WR}$	18		TCLCL–65		ns
TRLAZ	Address Float After $\overline{RD}$		20		20	ns
TWHLH	$\overline{WR}$ or $\overline{RD}$ HIGH to ALE HIGH	18	148	TCLCL–65	TCLCL+65	ns

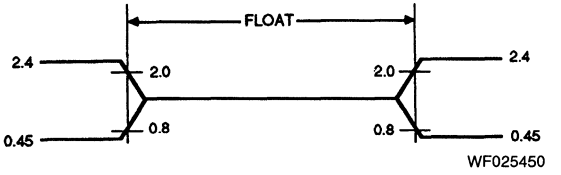
EXTERNAL CLOCK DRIVE

Parameter Symbol	Parameter Description	Min.	Max.	Units
1/TCLCL	Oscillator Frequency	3.5	12	MHz
TCHCX	HIGH Time	20		ns
TCLCX	LOW Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

AC TESTING



Input/Output Waveform



Float Waveform

AC inputs during testing are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for a logic "0". For timing purposes, the float state is defined as the point at which a P0 pin sinks 2.4 mA or sources 400 μA at the voltage test levels.

80C51BH/80C31BH

CMOS Single-Chip Microcontroller

PRELIMINARY MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

- CMOS versions of 8051 and 8031
- 80C51 = 80C31 + 4K bytes ROM
- 128 bytes of RAM
- 32 programmable I/O lines
- CMOS and TTL compatible
- Two 16-bit timer/counters
- Low-power consumption:
  - Normal operation: 16 mA @ 5 V, 12 MHz
  - Idle mode: 3.7 mA @ 5 V, 12 MHz
  - Power-Down mode: 50 μA @ 2 V to 6 V
- 64K bytes Program Memory space
- 64 K bytes Data Memory space
- Boolean processor

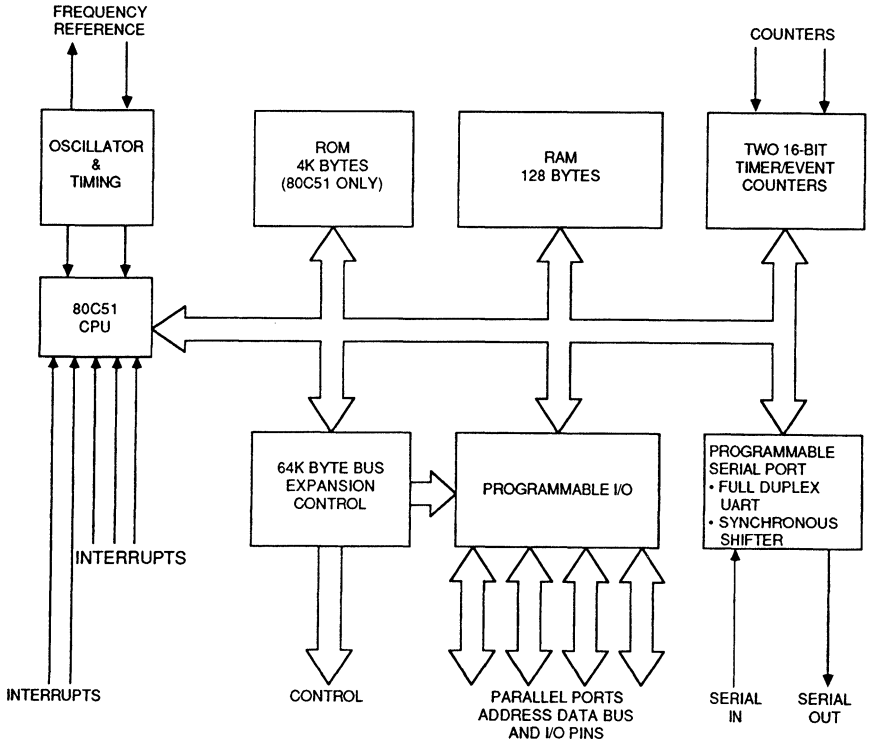
GENERAL DESCRIPTION

The AMD 80C51 and 80C31 are CMOS versions of the 8051 and 8031 8-bit microcontrollers. They combine the power savings of CMOS with the powerful 8051/31 microcontroller.

These CMOS versions retain all the features of their NMOS counterparts: 4K bytes on-chip ROM (80C51 only); 128 bytes RAM; 32 I/O lines; two 16-bit timers; a five-source, two-level interrupt structure; a full-duplex serial port; and on-chip oscillator and clock circuits.

In addition, the 80C51/31 has two software-selectable modes of reduced activity for further power conservation — Idle and Power-Down. In the Idle mode, the CPU is frozen while the RAM, timers, serial port, and the interrupt system continue to function. In the Power-Down mode, the RAM is saved and all other functions are inoperative.

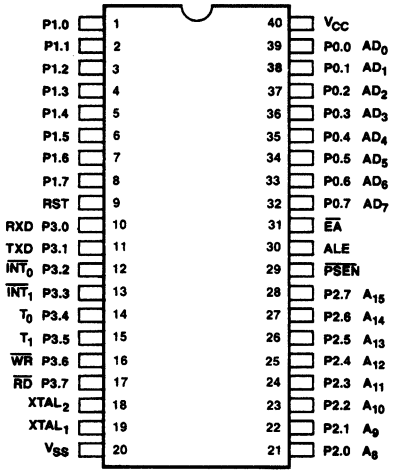
BLOCK DIAGRAM



Publication # 09236 | Rev. A | Amendment /0
Issue Date: October 1987

CONNECTION DIAGRAM
Top View

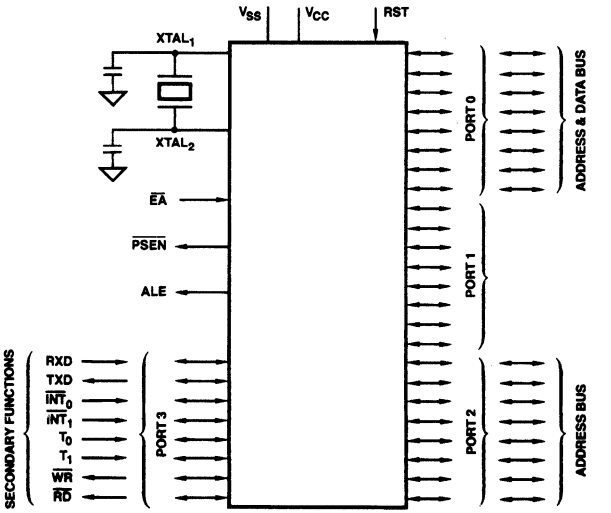
DIP



CD005551

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

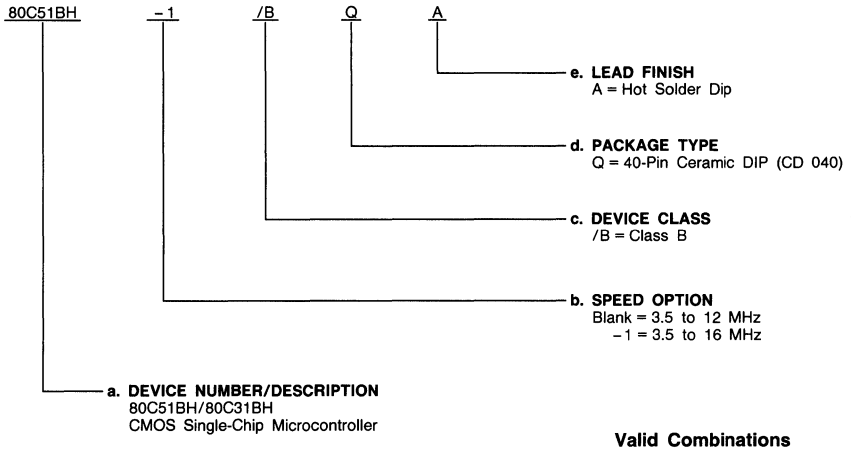


LS001323

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant withMIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
80C51BH	/BQA
80C51BH-1	
80C31BH	
80C31BH-1	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 4, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage on Any
Pin to V_{SS} ..... −0.5 V to V_{CC} +0.5 V
Voltage on V_{CC} to V_{SS} ..... −0.5 V to 6.5 V
Power Dissipation .....200 mW

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4 V to +6 V
Ground (V_{SS}) .....0 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges (for APL Products, Group A, Subgroups 1, 2, 3, are tested)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input LOW Voltage (Except $\overline{EA}$)		−0.5	.2 V_{CC} − 0.25	V
V_{IL1}	Input LOW Voltage ($\overline{EA}$)		−0.5	.2 V_{CC} − 0.45	V
V_{IH}	Input HIGH Voltage (Except $XTAL_1$, RST)		.2 V_{CC} + 1.1	V_{CC} + 0.5	V
V_{IH1}	Input HIGH Voltage ($XTAL_1$ RST)		.7 V_{CC} + .2	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage (Ports 1, 2, 3)	I_{OL} = 1.6 mA (Note 1)		0.45	V
V_{OL1}	Output LOW Voltage (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA (Note 1)		0.45	V
V_{OH}	Output HIGH Voltage (Ports 1, 2, 3)	I_{OH} = −60 μA, V_{CC} = 5 V ±10%	2.4		V
		I_{OH} = −25 μA	.75 V_{CC}		V
		I_{OH} = −10 μA	.9 V_{CC}		V
V_{OH1}	Output HIGH Voltage (Port 0 in External Bus Mode, ALE, $\overline{PSEN}$)	I_{OH} = −400 μA, V_{CC} = 5 V ±10%	2.4		V
		I_{OH} = −150 μA	.75 V_{CC}		V
		I_{OH} = −40 μA (Note 2)	.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.45 V		−75	μA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, 3)	V_{IN} = 2 V		−750	μA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	μA
RRST	Reset Pulldown Resistor		50	150	kΩ
CIO	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{PD}	Power Down Current	V_{CC} = 2 to 6 V (Note 3)		75	μA

MAXIMUM I_{CC} (mA)

	Operating (Note 4)			Idle (Note 5)		
Freq. V_{CC}	4 V	5 V	6 V	4 V	5 V	6 V
3.5 MHz	4.3	5.7	7.5	1.1	1.6	2.2
8.0 MHz	8.3	11	14	1.8	2.7	3.7
12 MHz	12	16	20	2.5	3.7	5
16 MHz	16	20.5	25	3.5	5	6.5

Notes:
1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OLS} of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt-Trigger STROBE input.
2. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall before the .9 V_{CC} specification when the address bits are stabilizing.
3. Power-Down I_{CC} is measured with all outputs pins disconnected: $\overline{EA}$ = Port 0 = V_{CC}; $XTAL_2$ N.C.; RST = V_{SS}.
4. I_{CC} is measured with all output pins disconnected; $XTAL_1$ driven with TCLCH, TCHCL = 5 ns, V_{IL} = V_{SS} + .5 V, V_{IH} = V_{CC} − .5 V; $XTAL_2$ N.C.; $\overline{EA}$ = RST = Port 0 = V_{CC}.
   I_{CC} would be slightly higher if a crystal oscillator is used.
5. Idle I_{CC} is measured with all output pins disconnected; $XTAL_1$ driven with TCLCH, TCHCL = 5 ns, V_{IL} = V_{SS} + .5 V, V_{IH} = V_{CC} − .5 V; $XTAL_2$ N.C.; Port 0 = V_{CC}; $\overline{EA}$ = RST = V_{SS}.

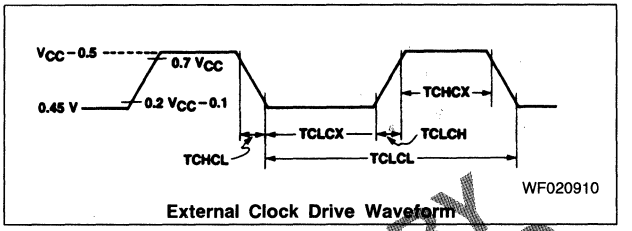
See Section 6 of the MOS Microprocessors and Peripherals Data Book (Order # 09067A) for Thermal Characteristics Information.

SWITCHING CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted) (C_L for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; C_L for All Other Outputs = 80 pF)

Parameter Symbol	Parameter Description	16 MHz Osc.		12 MHz Osc.		Variable Oscillator		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
External Program and Data Memory Characteristics								
1/TCLCL	Oscillator Frequency					3.5	16	MHz
TLHLL	ALE Pulse Width	85		112		2TCLCL – 55		ns
TAVLL	Address Valid to ALE LOW	7		13		TCLCL – 70		ns
TLLAX	Address Hold After ALE LOW	27		38		TCLCL – 50		ns
TLLIV	ALE LOW to Valid Instr. In		150		218		4TCLCL – 115	ns
TLLPL	ALE LOW to $\overline{PSEN}$ LOW	22		28		TCLCL – 55		ns
TPLPH	$\overline{PSEN}$ Pulse Width	142		19		3TCLCL – 60		ns
TPLIV	$\overline{PSEN}$ LOW to Valid Instr. In		83		130		3TCLCL – 120	ns
TPXIX	Input Instr. Hold After $\overline{PSEN}$	0		0		0		ns
TPXIZ	Input Instr. Float After $\overline{PSEN}$		38		43		TCLCL – 40	ns
TAVIV	Address to Valid Instr. In		208		297		5TCLCL – 120	ns
TPLAZ	$\overline{PSEN}$ LOW to Address Float		10		25		25	ns
TRLRH	$\overline{RD}$ Pulse Width	275		400		6TCLCL – 100		ns
TWLWH	$\overline{WR}$ Pulse Width	275		400		6TCLCL – 100		ns
TRLDV	$\overline{RD}$ LOW to Valid Data In		148		232		5TCLCL – 185	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		0		ns
TRHDZ	Data Float After $\overline{RD}$		55		82		2TCLCL – 85	ns
TLLDV	ALE LOW to Valid Data In		350		49		8TCLCL – 170	ns
TAVDV	Address to Valid Data In		398		565		9TCLCL – 185	ns
TLLWL	ALE LOW to $\overline{RD}$ or $\overline{WR}$ LOW	137	238	185	315	3TCLCL – 65	3TCLCL + 65	ns
TAVWL	Address Valid to Read or Write LOW	120		188		4TCLCL-145		ns
TQVWX	Data Valid to $\overline{WR}$ Transiiton	2		8		TCLCL – 75		ns
TWHQX	Data Hold After $\overline{WR}$	12		18		TCLCL – 65		ns
TRLAZ	$\overline{RD}$ LOW to Address Float		0		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	22	103	18	148	TCLCL – 65	TCLCL + 65	ns

EXTERNAL CLOCK DRIVE

Parameter Symbol	Parameter Description	Min.	Max.	Unit
1/TCLCL	Oscillator Frequency	3.5	16	MHz
TCHCX	HIGH Time	20		ns
TCLCX	LOW Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns

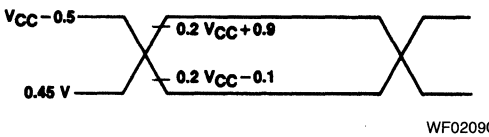


External Clock Drive Waveform

SERIAL PORT TIMING — SHIFT REGISTER MODE

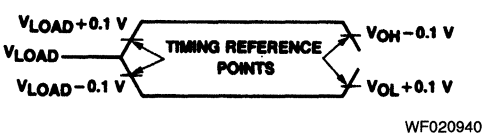
(Test Conditions: T_C = −55 to +125°C; V_{CC} = 5 V ±20%; V_{SS} = 0 V; Load Capacitance = 80 pF)

Parameter Symbol	Parameter Description	16 MHz Osc.		Variable Oscillator		Unit
		Min.	Max.	Min.	Max.	
TXLXL	Serial Port Clock Cycle Time	750		12TCLCL		ns
TQVXH	Output Data Setup to Clock Rising Edge	492		10TCLCL – 133		ns
TXHQX	Output Data Hold After Clock Rising Edge	8		2TCLCL – 117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		492		10TCLCL – 133	ns



AC INPUTS DURING TESTING ARE DRIVEN AT V_{CC} – 0.5 FOR A LOGIC "1" AND 0.45 V FOR A LOGIC "0." TIMING MEASUREMENTS ARE MADE AT V_{IH} MIN. FOR A LOGIC "1" AND V_{IL} MAX. FOR A LOGIC "0."

AC Testing Input/Output Waveforms



FOR TIMING PURPOSES A PORT PIN IS NO LONGER FLOATING WHEN A 100 mV CHANGE FROM LOAD VOLTAGE OCCURS, AND BEGINS TO FLOAT WHEN A 100 mV CHANGE FROM THE LOADED V_{OH}/V_{OL} LEVEL OCCURS. $I_{OL}/I_{OH} \geq \pm 20$ mA.

Float Waveform

8751H/8753H

Single-Chip 8-Bit Microcontroller

MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

- Military Temperature Range
  - −55 to +125°C (T_C)
- 4K x 8 EPROM (8751); 8K x 8 EPROM (8753)
- 128 x 8 RAM
- 64K bytes Program Memory space
- 64K bytes Data Memory space
- Pin-compatible with entire 8051 Family
- Full-duplex programmable serial ports
- 32 I/O lines (four 8-bit ports)
- Supports Adaptive EPROM Programming
- EPROM Security Feature
- Two 16-bit Timer/Event counters

GENERAL DESCRIPTION

The 8751H and 8753H are members of a family of advanced single-chip microcontrollers. Both the 8751H, which has 4K bytes of EPROM, and the 8753H, which has 8K bytes of EPROM, are pin-compatible EPROM versions of the 8051AH and 8053AH, respectively. Thus, the 8751H/8753H are full-speed prototyping tools which provide effective single-chip solutions for controller applications that require code modification flexibility. Refer to the block diagram of the 8051 family.

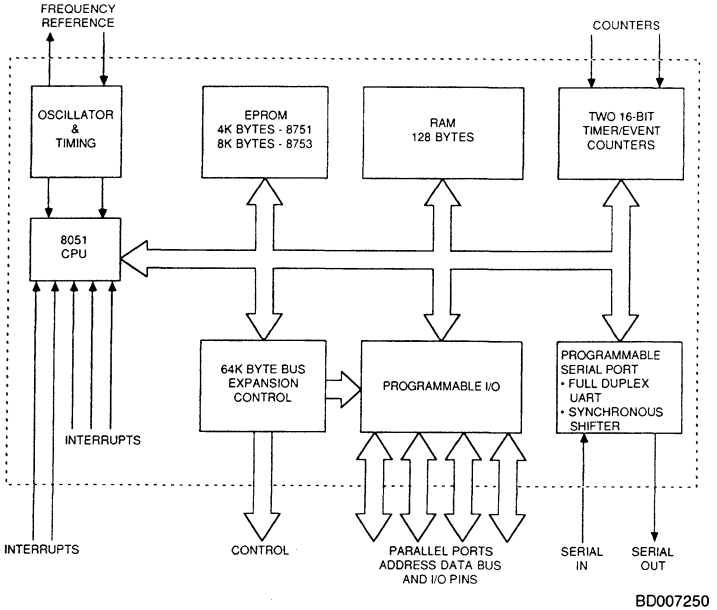
The 8751H/8753H devices feature: thirty-two I/O lines; two 16-bit timer/event counters; a Boolean processor, a 5-source, bi-level interrupt structure; a full-duplex serial channel; and on-chip oscillator and clock circuitry.

Program and Data Memory are located in independent addresses. The AMD family of microcontrollers can access up to 64K bytes of external Program Memory and up to 64K bytes of external Data Memory. The 8751H and the 8753H contain the lower 4K and 8K bytes of Program Memory, respectively, on-chip. Both parts have 128 bytes of on-chip read/write data memory.

The AMD 8051 Microcontroller Family is specifically suited for control applications. A variety of fast addressing modes, which access the internal RAM, facilitates byte processing and numerical operations on small data structures. Included in the instruction set is a menu of 8-bit arithmetic instructions, including 4-cycle multiply and divide instructions.

Extensive on-chip support enables direct bit manipulation and testing of 1-bit variables as separate data types. Thus, the device is also suited for control and logic systems that require Boolean processing.

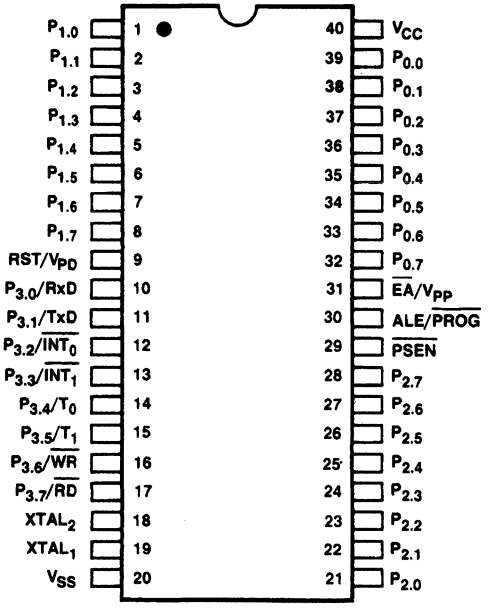
BLOCK DIAGRAM



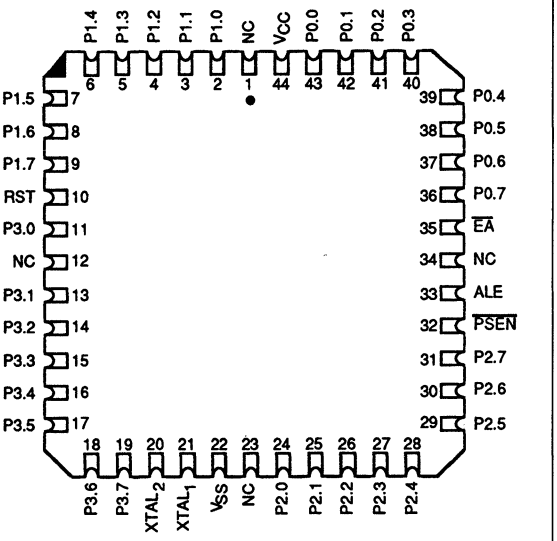
BD007250

Publication # 09285 Rev. A Amendment /0
Issue Date: November 1987

CONNECTION DIAGRAMS
Top View



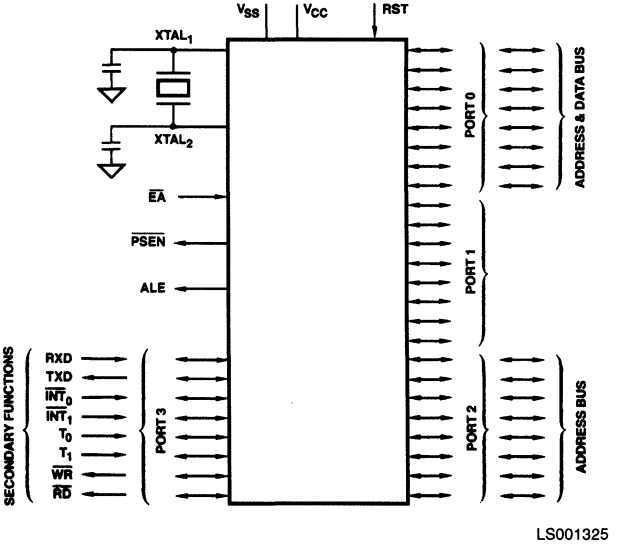
CD005651



CD010870

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

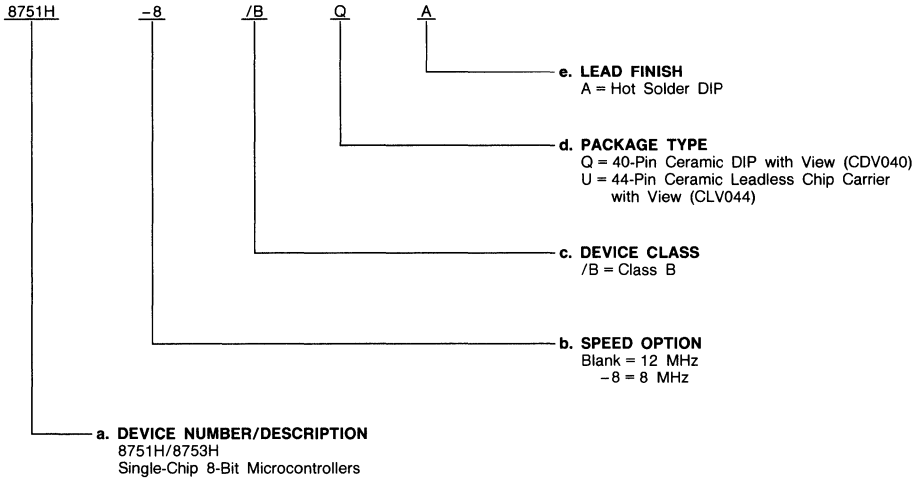


LS001325

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
8751H	/BQA, /BUA
8751H-8	
8753H	
8753H-8	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage on Any Other Pin to V_{SS}
(Except V_{PP}) ..... −0.5 to +7.0 V
Voltage from V_{PP} to V_{SS} ..... −0.5 to +21.5 V
Power Dissipation ..... 2 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V
Ground (V_{SS}) ..... 0 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL} †	Input LOW Voltage		−0.5	0.7	V
V_{IL1} †	Input LOW Voltage to $\overline{EA}$		0	0.7	V
V_{IH} †	Input HIGH Voltage (Except $XTAL_2$, RST)		2.2	V_{CC} + 0.5	V
V_{IH1} †	Input HIGH Voltage to $XTAL_2$, RST	$XTAL_1 = V_{SS}$	2.5	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage (Ports 1, 2, 3) (Note 1)	I_{OL} = 1.2 mA		0.45	V
V_{OL1}	Output LOW Voltage (Port 0, ALE, $\overline{PSEN}$) (Note 1)	I_{OL} = 2.8 mA		0.60	V
		I_{OL}=2.4 mA		0.45	
V_{OH}	Output HIGH Voltage (Ports 1, 2, 3)	I_{OH} = −60 μA	2.4		V
V_{OH1}	Output HIGH Voltage (Port 0 in External Bus Mode, ALE, $\overline{PSEN}$)	I_{OH} = −300 μA	2.4		V
I_{IL}	Logical 0 Input Current P1, P2, P3	V_{IN} = 0.45 V		−500	μA
I_{IL1}	Logical 0 Input Current to $\overline{EA}/V_{PP}$	V_{IN} = 0.45 V		−15	mA
I_{IL2}	Logical 0 Input Current to $XTAL_2$	$XTAL_1 = V_{SS}$, V_{IN} = 0.45 V		−4.5	mA
I_{LI}	Input Leakage Current to Port 0	0.45 < V_{IN} < V_{CC}		±100	μA
I_{IH}	Logical Input Current to $\overline{EA}/V_{PP}$	V_{IN} = 2.4 V		500	μA
I_{IH1}	Input Current to RST/V_{PP} to Activate Reset	V_{IN} < (V_{CC} − 1.5 V)		500	μA
I_{CC}	Power Supply Current (Note 3)	All Outputs Disconnected, $\overline{EA} = V_{CC}$		275	mA
C_{IO} ††	Capacitance of I/O Buffers	f_C = 1 MHz, T_A = 25°C		30*	pF
I_{PD}	Power-Down Current (Note 2)	T_A = 25°C, V_{PD} = 5.0 V, V_{CC} = 0 V		10	mA

Notes: 1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
2. Power-Down I_{CC} is measured with all output pins disconnected; $\overline{EA} = V_{CC} = 0$; $XTAL_2$ = N.C.; RST = V_{PD} = 5.0 V.
3. I_{CC} is measured with all output pins disconnected; $XTAL_1$ driven with t_{CLCH}, t_{CHCL} = 5 ns, $V_{IL} = V_{SS}$ + 5 V, $V_{IH} = V_{CC}$ − 5 V; $XTAL_2$ = N.C.; $\overline{EA}$ = RST = V_{CC}.

† Group A, Subgroups 7 and 8 only are tested.
†† Not included in Group A tests.
* Not tested; guaranteed by design.

SWITCHING CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)
(Load Capacitance for Port 0, ALE, and $\overline{PSEN}$ = 100 pF, Load Capacitance for All Other Outputs = 80 pF)

External Program Memory Characteristics

Parameter Symbol	Parameter Description	12-MHz Osc.		8-MHz Osc.		Variable Oscillator		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$1/t_{CLCL}$	Oscillator Frequency	3.5	12	3.5	8	3.5	12	MHz
t_{LHLL}	ALE Pulse Width	112		195		$2t_{CLCL}-55$		ns
t_{AVLL}	Address Setup to ALE	28		70		$t_{CLCL}-55$		ns
t_{LLAX}	Address Hold After ALE	33		75		$t_{CLCL}-50$		ns
t_{LLIV}	ALE to Valid Instr In		168		335		$4t_{CLCL}-165$	ns
t_{LLPL}	ALE to $\overline{PSEN}$	43		85		$t_{CLCL}-40$		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	175		300		$3t_{CLCL}-75$		ns
t_{PLIV}	$\overline{PSEN}$ to Valid Instr In		85		210		$3t_{CLCL}-165$	ns
t_{PXIX}	Input Instr Hold After $\overline{PSEN}$	0		0		0		ns
t_{PXIZ}	Input Instr Float After $\overline{PSEN}$		48		90		$t_{CLCL}-35$	ns
t_{PXAV}	Address Valid After $\overline{PSEN}$	58		100		$t_{CLCL}-25$		ns
t_{AVIV}	Address to Valid Instr In		252		460		$5t_{CLCL}-165$	ns
t_{PLAZ}	Addr Float After $\overline{PSEN}$		20		20		20	ns

External Data Memory Characteristics

Parameter Symbol	Parameter Description	12-MHz Osc.		8-MHz Osc.		Variable Oscillator		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RLRH}	$\overline{RD}$ Pulse Width	400		650		$6t_{CLCL}-100$		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		650		$6t_{CLCL}-100$		ns
t_{LLAX}	Address Hold After ALE	33		75		$t_{CLCL}-50$		ns
t_{RLDV}	$\overline{RD}$ to Valid Data In		232		440		$5t_{CLCL}-185$	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		82		165		$2t_{CLCL}-85$	ns
t_{LLDV}	ALE to Valid Data In		496		830		$8t_{CLCL}-170$	ns
t_{AVDV}	Address to Valid Data In		565		940		$9t_{CLCL}-185$	ns
t_{LLWL}	ALE to $\overline{RD}$ or $\overline{WR}$	185	315	310	440	$3t_{CLCL}-65$	$3t_{CLCL}+65$	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$	188		355		$4t_{CLCL}-145$		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	0		40		$t_{CLCL}-85$		ns
t_{QVWH}	Data Setup Before $\overline{WR}$	508		800		$7t_{CLCL}-75$		ns
t_{WHQX}	Data Hold After $\overline{WR}$	18		60		$t_{CLCL}-65$		ns
t_{RLAZ}	Address Float After $\overline{RD}$		20		20		20	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ HIGH to ALE HIGH	18	148	60	190	$t_{CLCL}-65$	$t_{CLCL}+65$	ns

External Clock Drive*

Parameter Symbol	Parameter Description	Min.	Max.	Unit
$1/t_{CLCL}$	Oscillator Frequency	1.2	12	MHz
t_{CHCX}	HIGH Time	20		ns
t_{CLCX}	LOW Time	20		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

*Not tested; these specs are controlled by the Teradyne J941, J983 tester.

SWITCHING CHARACTERISTICS (Cont'd.)
Serial Port Timing — Shift Register Mode (C_L = 8 pF)

Parameter Symbol	Parameter Description	12-MHz Osc.		8-MHz Osc.		Variable Oscillator		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		1.0		$12t_{CLCL}$		μs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		1117		$10t_{CLCL}-133$		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	49		133		$2t_{CLCL}-117$		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		1117		$10t_{CLCL}-133$	ns

EPROM Programming and Verification Characteristics*
(T_A = +21 to +27°C, V_{CC} = +5 V ±10%, V_{SS} = 0 V)

Parameter Symbol	Parameter Description	Min.	Max.	Unit
V_{PP}	Programming Supply Voltage	20.5	21.5	V
I_{PP}	Programming Supply Current		30	mA
$1/t_{CLCL}$	Oscillator Frequency	4	6	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	$P_{2.7}$ ($\overline{ENABLE}$) HIGH to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$	10		μs
t_{GHSL}	V_{PP} Hold after $\overline{PROG}$	10		μs
t_{GLGH}	$\overline{PROG}$ Width	45	55	ms
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	

*Not tested; guaranteed by design.

CHAPTER 5

* DESC approved
** Pending DESC approval

Z8002*

16-Bit Microprocessor

MILITARY INFORMATION

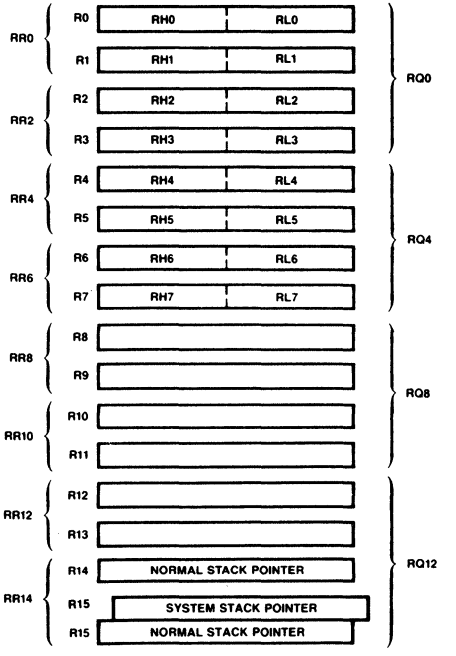
DISTINCTIVE CHARACTERISTICS

- **4- and 6-MHz CPU Clock**
  High throughput with low system clock rate for easier system design
- **Powerful General Register Architecture**
  16 general registers provide high throughput in all types of applications
- **Wide Variety of Data Types**
  Instructions operate on bits, bytes, 16- and 32-bit words for efficient programming of a wide variety of functions
- **Partitioned for Operating System Protection**
  Hardware bit protects privileged instructions from execution except by operating system
- **Supports 3 Types of Interrupts**
  Separate pins provided for vectored, non-vectored and non-maskable interrupts
- **Two Compatible CPUs**
  Compact 40-pin Z8002 supports 64KB memory

GENERAL DESCRIPTION

The Z8002 is a general-purpose 16-bit CPU belonging to the Z8000 family of microprocessors. Its architecture is centered around sixteen 16-bit general registers. The CPU deals with 23-bit address space which consists of two components: 7-bit segment number and 16-bit offset. Facilities are provided to maintain three distinct address spaces — code, data and stack. The Z8002 implements a powerful instruction set with flexible addressing modes. These instructions operate on several data types — bit, byte, word (16-bit), long word (32-bit), byte string and word string. The CPU can execute instructions in one of two modes — System and Normal. Sometimes these modes are also known as Privileged and Non-Privileged, respectively. The CPU also contains an on-chip memory refresh facility. The Z8002 is fabricated using silicon-gate N-MOS technology and is packaged in a 40-pin DIP. The Z8002 requires a single +5-V power supply and a single phase clock for its operation.

GENERAL REGISTERS



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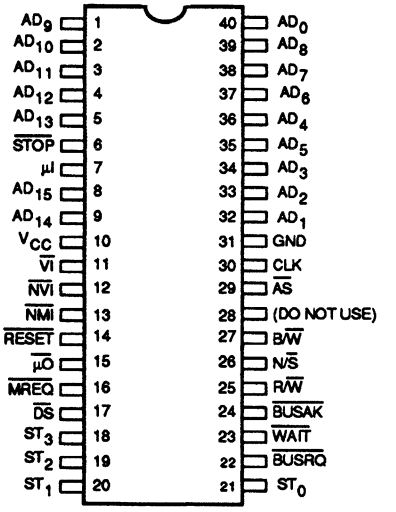
*Z8000 and Z8002 are trademarks of Zilog, Inc.

Publication # 09237 Rev. A Amendment /0
Issue Date: December 1987

CONNECTION DIAGRAMS
Top View

DIPs



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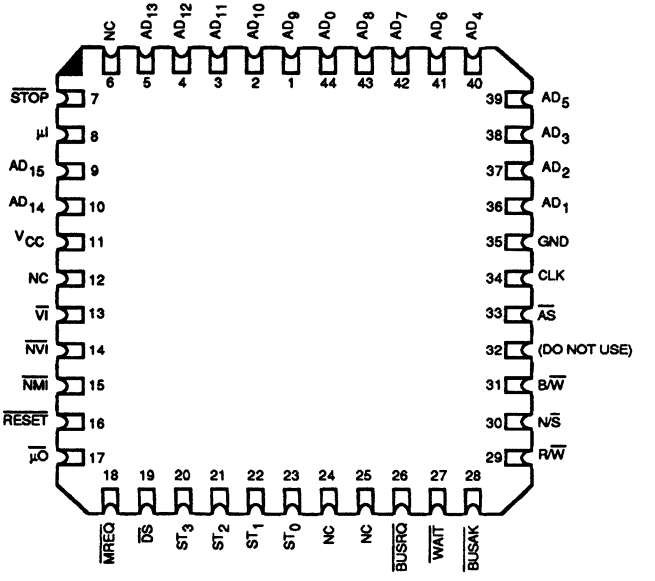
LCC



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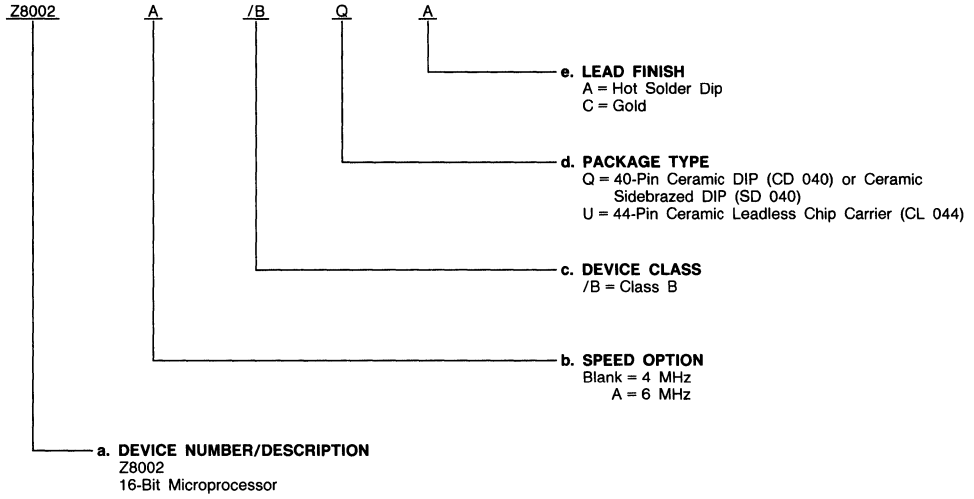
MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
Z8002	/BQA, /BQC, /BUA
Z8002A	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage at any Pin
Relative to V_{SS} ..... −0.3 to +7.0V
Power Dissipation 2.5W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... 5 V ± 5%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{CH} †	Clock Input HIGH Voltage	Driven by External Clock Generator	V_{CC}−0.4	V_{CC}+0.3*	V
V_{CL} †	Clock Input LOW Voltage	Driven by External Clock Generator	−0.3*	0.45	V
V_{IH} †	Input HIGH Voltage		2.0	V_{CC}+0.3*	V
V_{IH} $\overline{NMI}$, † Reset	Input HIGH Voltage		2.4	V_{CC}+0.3*	V
V_{IL} †	Input LOW Voltage		−0.3*	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = −250μA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = +2.0mA		0.4	V
I_{IL}	Input Leakage Except $\overline{SEGT}$ Pin	$0.4 \leqslant V_{IN} \leqslant +2.4V$		±10	μA
I_{IL} on $\overline{SEGT}$	Input Leakage on $\overline{SEGT}$ Pin		−100	100	μA
I_{OL}	Output Leakage	$0.4 \leqslant V_{OUT} \leqslant +2.4V$		±10	μA
ICC	V_{CC} Supply Current (Note 1)			400	mA

* Not tested; guaranteed by design.
† Group A, Subgroups 7 and 8 only are tested.

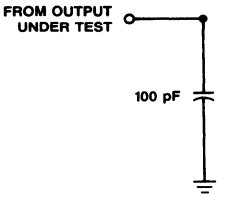
Notes: 1. I_{CC} is measured while running a functional pattern with the loads turned on.

See Section 6 of the MOS Microprocessors and Peripherals Data Book (Order #09067A) for Thermal Characteristics Information.

Standard Test Conditions

The characteristics below apply for the following test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

SWITCHING TEST CIRCUIT



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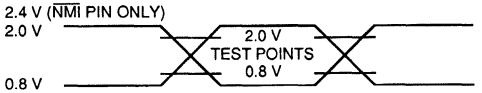
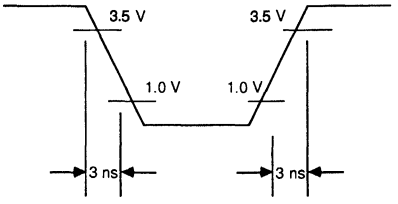
SWITCHING TEST WAVEFORMS
Input/Output



LS003011

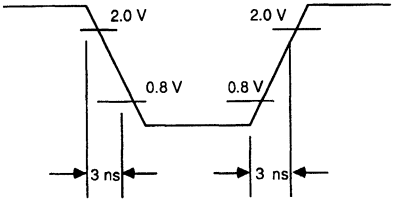
AC testing outputs are driven at 2.0 V for a logical 1 and 0.5 V for a logical 0. The clock is driven at V_{CC} −0.4 V and 0.45 V. Timing measurements are made at 2.0 V for a logical 1 and 0.5 V for a logical 0.

AC Clock Input



WF024271

AC Input (Except Clock)



WF024281

SWITCHING CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol	Parameter Description	4-MHz Devices		6-MHz Devices		Unit
			Min.	Max.	Min.	Max.	
1	TcC	Clock Cycle Time	250	500	160	500	ns
2	TwCh	Clock Width (HIGH)	105	250	70	250	ns
3	TwCl	Clock Width (LOW)	105	250	70	250	ns
4	TfC	Clock Fall Time (Note 1)		20		10	ns
5	TrC	Clock Rise Time (Note 1)		20		15	ns
8	TdC(Bz)	Clock ↑ to Bus Float (Note 2)		65		55	ns
9	TdC(A)	Clock ↑ to Address Valid		100		75	ns
10	TdC(Az)	Clock ↑ to Address Float (Note 2)		65		55	ns
11	TdA(DR)	Address Valid to Read Data Required Valid (Note 2)		475		305	ns
12	TsDI(C)	Data In to Clock ↓ Setup Time	50		20		ns
13	TdDS(A)	$\overline{DS}$ ↑ to Address Active (Note 2)	80		45		ns
14	TdC(DW)	Clock ↑ to Write Data Valid		100		75	ns
15	ThDI(DS)	Data In to $\overline{DS}$ ↑ Hold Time	0		0		ns
16	TdDO(DS)	Data Out Valid to $\overline{DS}$ ↑ Delay (Note 2)	295		195		ns
17	TdA(MR)	Address Valid to $\overline{MREQ}$ ↓ Delay (Note 2)	55		35		ns
18	TdC(MR)	Clock ↓ to $\overline{MREQ}$ ↓ Delay		80		60	ns
19	TwMRh	$\overline{MREQ}$ Width (HIGH) (Note 2)	210		135		ns
20	TdMR(A)	$\overline{MREQ}$ ↓ to Address Not Active (Note 2)	70		35		ns
21	TdDO(DSW)	Data Out Valid to $\overline{DS}$ ↓ (Write) Delay (Note 2)	55		35		ns
22	TdMR(DR)	$\overline{MREQ}$ ↓ to Read Data Required Valid (Note 2)		370		230	ns
23	TdC(MR)	Clock ↓ to $\overline{MREQ}$ ↑ Delay		80		60	ns
24	TdC(ASf)	Clock ↑ to $\overline{AS}$ ↓ Delay		80		60	ns
25	TdA(AS)	Address Valid to $\overline{AS}$ ↑ Delay (Note 2)	55		35		ns
26	TdC(ASr)	Clock ↓ to $\overline{AS}$ ↑ Delay		90		80	ns
27	TdAS(DR)	$\overline{AS}$ ↑ to Read Data Required Valid (Note 2)		360		220	ns
28	TdDS(AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay (Note 2)	70		35		ns
29	TwAS	$\overline{AS}$ Width (LOW) (Note 2)	85		55		ns
30	TdAS(A)	$\overline{AS}$ ↑ to Address Not Active Delay (Note 2)	70		45		ns
31	TdAz(DSR)	Address Float to $\overline{DS}$ (Read) ↓ Delay (Note 2)	0		0		ns
32	TdAS(DSR)	$\overline{AS}$ ↑ to $\overline{DS}$ (Read) ↓ Delay (Note 2)	80		55		ns
33	TdDSR(DR)	$\overline{DS}$ (Read) ↓ to Read Data Required Valid (Note 2)		205		130	ns
34	TdC(DSr)	Clock ↓ to $\overline{DS}$ ↑ Delay		70		65	ns
35	TdDS(DW)	$\overline{DS}$ ↑ to Write Data and STATUS Not Valid (Note 2)	75		45		ns
36	TdA(DSR)	Address Valid to $\overline{DS}$ (Read) ↓ Delay (Note 2)	180		110		ns
37	TdC(DSR)	Clock ↑ to $\overline{DS}$ (Read) ↓ Delay		120		85	ns
38	TwDSR	$\overline{DS}$ (Read) Width (LOW) (Note 2)	275		185		ns

Notes: See next page for notes.

SWITCHING CHARACTERISTICS (Cont'd.)

No.	Parameter Symbol	Parameter Description	4-MHz Devices		6-MHz Devices		Unit
			Min.	Max.	Min.	Max.	
39	TdC(DSW)	Clock ↓ to $\overline{DS}$ (Write) ↓ Delay		95		80	ns
40	TwDSW	$\overline{DS}$ (Write) Width (LOW) (Note 2)	185		110		ns
41	TdDSI(DR)	$\overline{DS}$ (Input) ↓ to Read Data Required Valid (Note 2)		330		210	ns
42	TdC(DSF)	Clock ↓ to $\overline{DS}$ (I/O) ↓ Delay		120		100	ns
43	TwDS	$\overline{DS}$ (I/O) Width (LOW) (Note 2)	410		255		ns
44	TdAS(DSA)	$\overline{AS}$ ↑ to $\overline{DS}$ (Acknowledge) ↓ Delay (Note 2)	1065		690		ns
45	TdC(DSA)	Clock ↑ to $\overline{DS}$ (Acknowledge) ↓ Delay		120		85	ns
46	TdDSA(DR)	$\overline{DS}$ (Acknowledge) ↓ to Read Data Required Delay (Note 2)		455		295	ns
47	TdC(S)	Clock ↑ to Status Valid Delay		110		85	ns
48	TdS(AS)	Status Valid to $\overline{AS}$ ↑ Delay (Note 2)	50		30		ns
49	TsR(C)	$\overline{RESET}$ to Clock ↑ Setup Time	180		70		ns
50	ThR(C)	$\overline{RESET}$ to Clock ↑ Hold Time	0		0		ns
51	TwNMI	$\overline{NMI}$ Width (LOW)	100		70		ns
52	TsNMI(C)	$\overline{NMI}$ to Clock ↑ Setup Time	140		70		ns
53	TsVI(C)	$\overline{VI}$, $\overline{NVI}$ to Clock ↑ Setup Time	110		50		ns
54	ThVI(C)	$\overline{VI}$, $\overline{NVI}$ to Clock ↑ Hold Time	20		20		ns
57	TsMI(C)	$\overline{MI}$ to Clock ↑ Setup Time	180		110		ns
58	ThMI(C)	$\overline{MI}$ to Clock ↑ Hold Time	0		0		ns
59	TdC(MO)	Clock ↑ to MO Delay		120		85	ns
60	TsSTP(C)	$\overline{STOP}$ to Clock ↓ Setup Time	140		80		ns
61	ThSTP(C)	$\overline{STOP}$ to Clock ↓ Hold Time	0		0		ns
62	TsWT(C)	$\overline{WAIT}$ to Clock ↓ Setup Time	50		30		ns
63	ThWT(C)	$\overline{WAIT}$ to Clock ↓ Hold Time	10		10		ns
64	TsBRQ(C)	$\overline{BUSRQ}$ to Clock ↑ Setup Time	90		80		ns
65	ThBRQ(C)	$\overline{BUSRQ}$ to Clock ↑ Hold Time	10		10		ns
66	TdC(BAKr)	Clock ↑ to $\overline{BUSAK}$ ↑ Delay		100		75	ns
67	TdC(BAKf)	Clock ↑ to $\overline{BUSAK}$ ↓ Delay		100		75	ns
68	TwA	Address Valid Width (Note 2)	150		95		ns
69	TdDS(S)	$\overline{DS}$ ↑ to STATUS Not Valid (Note 2)	80		55		ns

Notes: 1. Clock rise and fall times are intended for design information only; not tested.
2. Not tested.

Z8530*

Serial Communications Controller

MILITARY INFORMATION

DISTINCTIVE CHARACTERISTICS

- **Two 0 to 2 Mbps full-duplex serial channels**
  Each channel has independent oscillator, baud-rate generator, and PLL for clock recovery, dramatically reducing external components.
- **Programmable protocols**
  NRZ, NRZI, and FM data encoding supported under program control.
- **Programmable Asynchronous Modes**
  5- to 8-bit characters with programmable stop bits, clock, break detect, and error conditions.
- **Programmable Synchronous Modes**
  SDLC and HDLC and SDLC loop supported with frame control, zero insertion and deletion, abort, and residue handling. CRC-16 and CCITT generators and checkers.
- **Compatible with non-multiplexed bus**
  The Z8530 interfaces easily to most other CPUs.

GENERAL DESCRIPTION

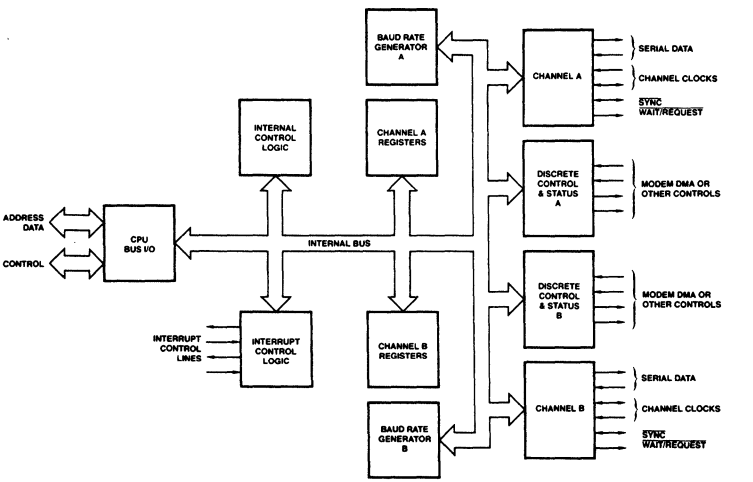
The SCC Serial Communications Controller is a dual-channel, multi-protocol data communications peripheral designed for use with 8- and 16-bit microprocessors. The SCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The SCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions, including on-chip baud rate generators, digital phase-locked loops, and crystal oscillators, which dramatically reduce the need for external logic.

The SCC handles asynchronous formats, synchronous byte-oriented protocols, such as IBM Bisync, and synchronous bit-oriented protocols, such as HDLC and IBM SDLC. This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drivers, etc.).

The device can generate and check CRC codes in any synchronous mode and can be programmed to check data integrity in various modes. The SCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The Z8530 is designed for non-multiplexed buses and is easily interfaced with most other CPUs, such as Z80, 6800, 68000, and MULTIBUS.†

BLOCK DIAGRAM



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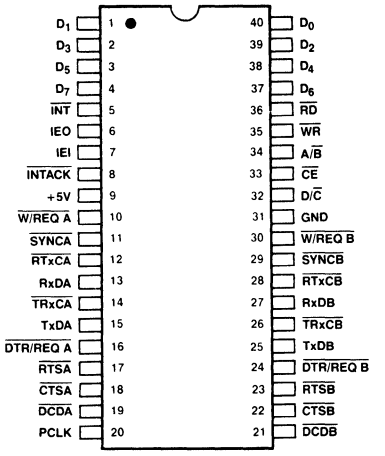
* Z8530 is a trademark of Zilog, Inc.
†MULTIBUS is a trademark of Intel, Corp.

Publication # 09238 | Rev. A | Amendment /0
Issue Date: October 1987

CONNECTION DIAGRAM
Top View



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Note: Pin 1 is marked for orientation.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant withMIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish

Z8530 – /B Q A

e. LEAD FINISH
A = Hot Solder Dip

d. PACKAGE TYPE
Q = 40-Pin Ceramic DIP (CD 040)

c. DEVICE CLASS
/B = Class B

b. SPEED OPTION
Blank = –4 MHz

a. DEVICE NUMBER/DESCRIPTION
Z8530
Serial Communications Controller

Valid Combinations	
Z8530	/BQA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests
Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Voltage at any Pin
Relative to V_{SS} ..... −0.5 to +7.0 V
Power Dissipation ..... 1.8 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (M) Devices
Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... 5 V ±10%

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Voltage		2.2		V_{CC}+0.3*	V
V_{IL}	Input LOW Voltage		−0.3*		0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = −250 µA	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = +2.0 mA			0.4	V
I_{IL}	Input Leakage	0.4 V ≤ V_{IN} ≤ 2.4 V			±10.0	µA
I_{OL}	Output Leakage	0.4 V ≤ V_{OUT} ≤ 2.4 V			±10.0	µA
I_{CC}	V_{CC} Supply Current				250	mA

CAPACITANCE*

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}†	Input Capacitance	Unmeasured pins returned to ground. f = 1 MHz at T_C = 25°C			10*	pF
C_{OUT}†	Output Capacitance				15*	pF
$C_{I/O}$†	Bidirectional Capacitance				20*	pF

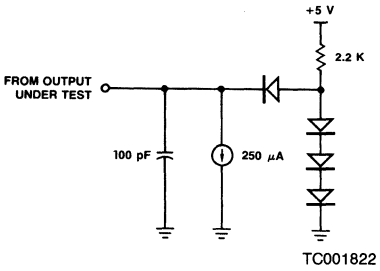
* Not tested; guaranteed by design.
† Not included in Group A tests.

Standard Test Conditions

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to GND. Positive current flows into the referenced pin. Standard conditions are as follows:

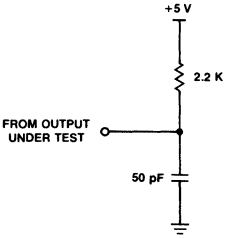
+4.5 V ≤ V_{CC} ≤ 5.5 V
GND = 0 V
−55°C ≤ T_C ≤ 125°C

SWITCHING TEST CIRCUITS



TC001822

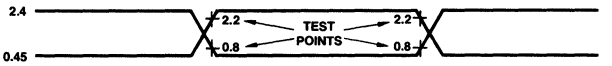
A. Standard Test Load



TC001831

B. Open-Drain Test Load

SWITCHING TEST INPUT/OUTPUT WAVEFORM



WF006353

AC testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and 0.8 V for logic "0".

*See Section 6 of the MOS Microprocessors and Peripherals Data Book (Order #09067A) for Thermal Characteristics Information.

SWITCHING CHARACTERISTICS over operating range (for APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted)

GENERAL TIMING

No.	Parameter Symbol	Parameter Description	Min.	Max.	Unit
1	TdPC(REQ)	PCLK ↓ to W/REQ Valid Delay		250	ns
2	TdPC(W)	PCLK ↓ to Wait Inactive Delay		350	ns
3	TsRXC(PC)	RxC↑ to PCLK ↑ Set-up Time (Note 1, 4)	80	T_{WPCL}	ns
4	TsRXD(RXCr)	RxD to RxC ↑ Set-up Time (XI Mode) (Note 1)	0		ns
5	ThRXD(RXCr)	RxD to RxC ↑ Hold Time (XI Mode) (Note 1)	150		ns
6	TsRXD(RXCf)	RxD to RxC ↓ Set-up Time (XI Mode) (Notes 1, 5)	0		ns
7	ThRXD(RXCf)	RxD to RxC ↓ Hold Time (XI Mode) (Notes 1, 5)	150		ns
8	TsSY(RXC)	SYNC to RxC ↑ Set-up Time (Note 1)	−200		ns
9	ThSY(RXC)	SYNC to RxC ↑ Hold Time (Note 1)	3TcPC + 400		ns
10	TsTXC(PC)	TxC ↓ to PCLK ↑ Set-up Time (Notes 2, 4)	0		ns
11	TdTXCf(TXD)	TxC ↓ to TxD Delay (XI Mode) (Note 2)		300	ns
12	TdTXCr(TXD)	TxC ↑ to TxD Delay (XI Mode) (Notes 2, 5)		300	ns
13	TdTXD(TRX)	TxD to TRxC Delay (Send Clock Echo)		200	ns
14	TwRTXh	RTxC High Width (Note 6)	180		ns
15	TwRTXl	RTxC Low Width (Note 6)	180		ns
16	TcRTX	RTxC Cycle Time (Notes 6, 7)	1000		ns
17	TcRTXX	Crystal Oscillator Period (Note 8)	250	1000	ns
18	TwTRXh	TRxC High Width (Note 6)	180		ns
19	TwTRXl	TRxC Low Width (Note 6)	180		ns
20	TcTRX	TRxC Cycle Time (Notes 6, 7)	1000		ns
21	TwEXT	DCD or CTS Pulse Width	200		ns
22	TwSY	SYNC Pulse Width	200		ns

Notes: 1. RxC is RTxC or TRxC, whichever is supplying the receive clock.
2. TxC is TRxC or RTxC, whichever is supplying the transmit clock.
3. Both RTxC and SYNC have 30 pF capacitors to ground connected to them.
4. Parameter applies only if the data rate is one-fourth the PCLK rate. In all other cases, no phase relationship between RxC and PCLK or TxC and PCLK is required.
5. Parameter applies only to FM encoding/decoding.
6. Parameter applies only for transmitter and receiver; DPLL and baud rate generator timing requirements are identical to chip PCLK requirements.
7. The maximum receive or transmit data is 1/4 PCLK.
8. Not tested; guaranteed by design.

SWITCHING CHARACTERISTICS (Cont'd.)

SYSTEM TIMING

No.	Parameter Symbol	Parameter Description	Min.	Max.	Unit
1	TdRXC(REQ)	$\overline{RxC}$ ↑ $\overline{W/REQ}$ Valid Delay (Note 2)	8	12	TcPC
2	TdRXC(W)	$\overline{RxC}$ ↑ to Wait Inactive Delay (Notes 1, 2)	8	14	TcPC
3	TdRXC(SY)	$\overline{RxC}$ ↑ to $\overline{SYNC}$ Valid Delay (Note 2)	4	7	TcPC
4	TdRXC(INT)	$\overline{RxC}$ ↑ to $\overline{INT}$ Valid Delay (Notes 1, 2)	10	16	TcPC
5	TdTXC(REQ)	$\overline{TxC}$ ↓ to $\overline{W/REQ}$ Valid Delay (Note 3)	5	8	TcPC
6	TdTXC(W)	$\overline{TxC}$ ↓ to Wait Inactive Delay (Notes 1, 3)	5	11	TcPC
7	TdTXC(DRQ)	$\overline{TxC}$ ↓ to $\overline{DTR/REQ}$ Valid Delay (Note 3)	4	7	TcPC
8	TdTXC(INT)	$\overline{TxC}$ ↓ to $\overline{INT}$ Valid Delay (Notes 1, 3)	6	10	TcPC
9	TdSY(INT)	$\overline{SYNC}$ Transition to $\overline{INT}$ Valid Delay (Note 1)	2	6	TcPC
10	TdEXT(INT)	$\overline{DCD}$ or $\overline{CTS}$ Transition to $\overline{INT}$ Valid Delay (Note 1)	2	6	TcPC

Notes: 1. Open-drain output, measured with open-drain test load.
2. $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
3. $\overline{TxC}$ is $\overline{TRxC}$ or $\overline{RTxC}$, whichever is supplying the transmit clock.

READ AND WRITE TIMING

No.	Parameter Symbol	Parameter Description	Min.	Max.	Unit
1	TwPCl	PCLK Low Width	105	1000	ns
2	TwPCh	PCLK High Width	105	1000	ns
3	TfPC	PCLK Fall Time		20	ns
4	TrPC	PCLK Rise Time		20	ns
5	TcPC	PCLK Cycle Time	250	2000	ns
6	TsA(WR)	Address to $\overline{WR}$ ↓ Set-up Time	80		ns
7	ThA(WR)	Address to $\overline{WR}$ ↑ Hold Time	0		ns
8	TsA(RD)	Address to $\overline{RD}$ ↓ Set-up Time	80		ns
9	ThA(RD)	Address to $\overline{RD}$ ↑ Hold Time	0		ns
10	TslA(PC)	$\overline{INTACK}$ to PCLK ↑ Set-up Time	10		ns
11	TslAi(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↓ Set-up Time (Note 1)	200		ns
12	ThlA(WR)	$\overline{INTACK}$ to $\overline{WR}$ ↑ Hold Time	0		ns
13	TslAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ Set-up Time (Note 1)	200		ns
14	ThlA(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↑ Hold Time	0		ns
15	ThlA(PC)	$\overline{INTACK}$ to PCLK ↑ Hold Time	100		ns
16	TsCEl(WR)	$\overline{CE}$ Low to $\overline{WR}$ ↓ Set-up Time	0		ns
17	ThCE(WR)	$\overline{CE}$ to $\overline{WR}$ ↑ Hold Time	0		ns
18	TsCEh(WR)	$\overline{CE}$ High to $\overline{WR}$ ↓ Set-up Time	100		ns
19	TsCEl(RD)	$\overline{CE}$ Low to $\overline{RD}$ ↓ Set-up Time (Note 1)	0		ns
20	ThCE(RD)	$\overline{CE}$ to $\overline{RD}$ ↑ Hold Time (Note 1)	0		ns
21	TsCEh(RD)	$\overline{CE}$ High to $\overline{RD}$ ↓ Set-up Time (Note 1)	100		ns
22	TwRDl	$\overline{RD}$ Low Width (Note 1)	240		ns
23	TdRD(DRA)	$\overline{RD}$ ↓ to Read Data Active Delay	0		ns
24	TdRDr(DR)	$\overline{RD}$ ↑ to Read Data Not Valid Delay	0		ns
25	TdRDf(DR)	$\overline{RD}$ ↓ to Read Data Valid Delay		220	ns
26	TdRD(DRz)	$\overline{RD}$ ↑ to Read Data Float Delay (Note 2)		70	ns

Notes: 1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Float delay is defined as the time required for the data bus to be released with a maximum DC load and minimum AC load.

SWITCHING CHARACTERISTICS (Cont'd.)

INTERRUPT ACKNOWLEDGE TIMING, RESET TIMING, CYCLE TIMING

No.	Parameter Symbol	Parameter Description	Min.	Max.	Unit
27	TdA(DR)	Adress Required Valid to Read Data Valid Delay		400	ns
28	TwWRI	$\overline{WR}$ Low Width	240		ns
29	TsDW(WR)	Write Data to $\overline{WR}$ ↓ Set-up Time	10		ns
30	ThDW(WR)	Write Data to $\overline{WR}$ ↑ Hold Time	0		ns
31	TdWR(W)	$\overline{WR}$ ↓ to Wait Valid Delay (Note 4)		240	ns
32	TdRD(W)	$\overline{RD}$ ↓ to Wait Valid Delay (Note 4)		240	ns
33	TdWRf(REQ)	$\overline{WR}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		240	ns
34	TdRDf(REQ)	$\overline{RD}$ ↓ to $\overline{W/REQ}$ Not Valid Delay		240	ns
35	TdWRr(REQ)	$\overline{WR}$ ↑ to $\overline{DTR/REQ}$ Not Valid Delay		4TcPC	ns
36	TdRDr(REQ)	$\overline{RD}$ ↑ to $\overline{DTR/REQ}$ Not Valid Delay		4TcPC	ns
37	TdPC(INT)	PCLK ↓ to $\overline{INT}$ Valid Delay (Note 4)		500	ns
38	TdIAi(RD)	$\overline{INTACK}$ to $\overline{RD}$ ↓ (Acknowledge) Delay (Note 5)	250		ns
39	TwRDA	$\overline{RD}$ (Acknowledge) Width	250		ns
40	TdRDA(DR)	$\overline{RD}$ ↓ (Acknowledge) to Read Data Valid Delay		250	ns
41	TsIEI(RDA)	IEI to $\overline{RD}$ ↓ (Acknowledge) Set-up Time	120		ns
42	ThIEI(RDA)	IEI to $\overline{RD}$ ↑ (Acknowledge) Hold Time	0		ns
43	TdIEI(IEO)	IEI to IEO Delay Time		120	ns
44	TdPC(IEO)	PCLK ↑ to IEO Delay		250	ns
45	TdRDA(INT)	$\overline{RD}$ ↓ to $\overline{INT}$ Inactive Delay (Note 4)		500	ns
46	TdRD(WRQ)	$\overline{RD}$ ↑ to $\overline{WR}$ ↓ Delay for No Reset	30		ns
47	TdWRQ(RD)	$\overline{WR}$ ↑ to $\overline{RD}$ ↓ Delay for No Reset	30		ns
48	TwRES	$\overline{WR}$ and $\overline{RD}$ Coincident Low for Reset	250		ns
49	Trc	Valid Access Recovery Time (Note 3)	6TcPC + 200		ns

Notes: 3. Parameter applies only between transactions involving the SCC.
4. Open-drain output, measured with open-drain test load.
5. Parameter is system dependent. For any SCC in the daisy chain, TdIAI(RD) must be greater than the sum of TdPC(IEO) for the highest priority device in the daisy chain, TsIEI(RDA) for the SCC, and TdIEIf(IEO) for each device separating them in the daisy chain.

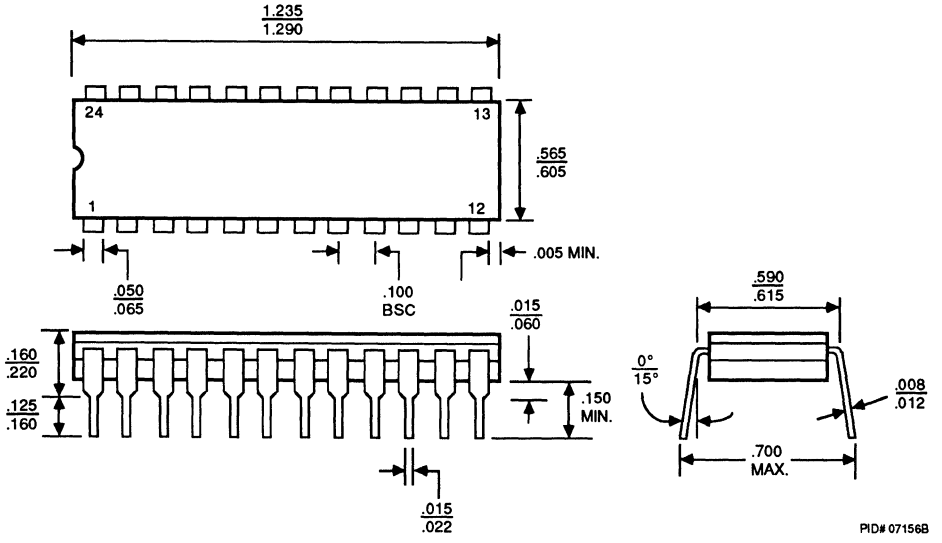
CHAPTER 6

General Information

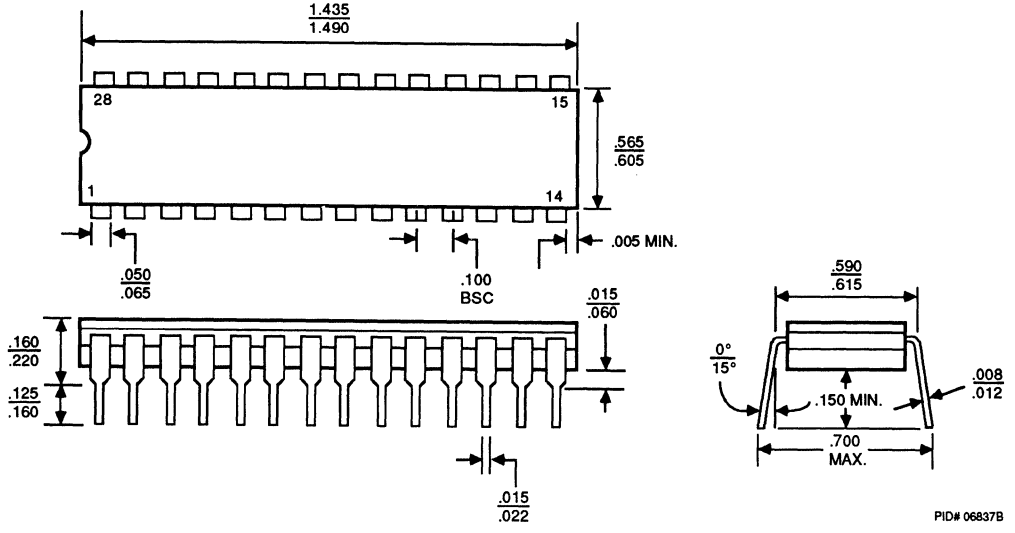
PACKAGE OUTLINES*

Ceramic DIPs (CD)

CD 024



CD 028



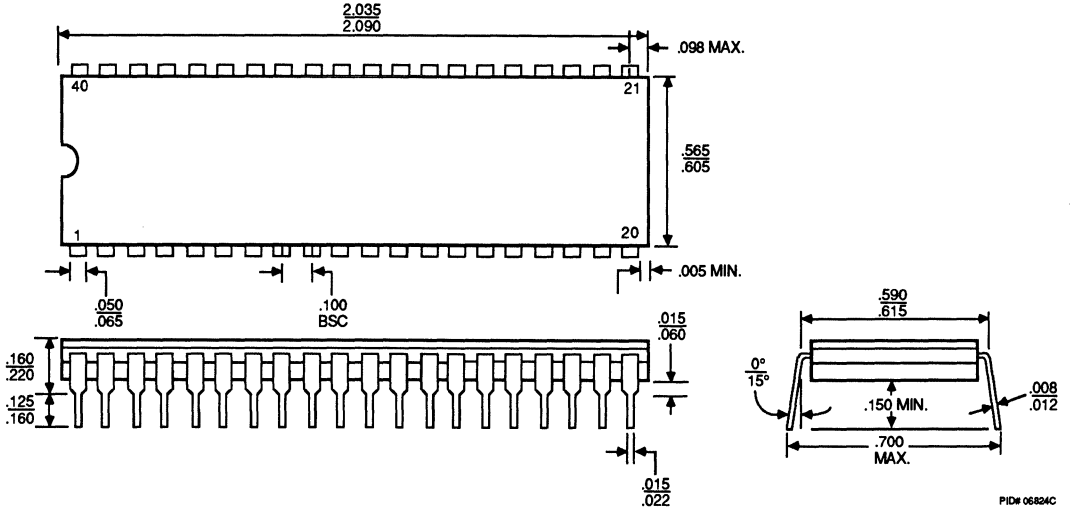
* For reference only.

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

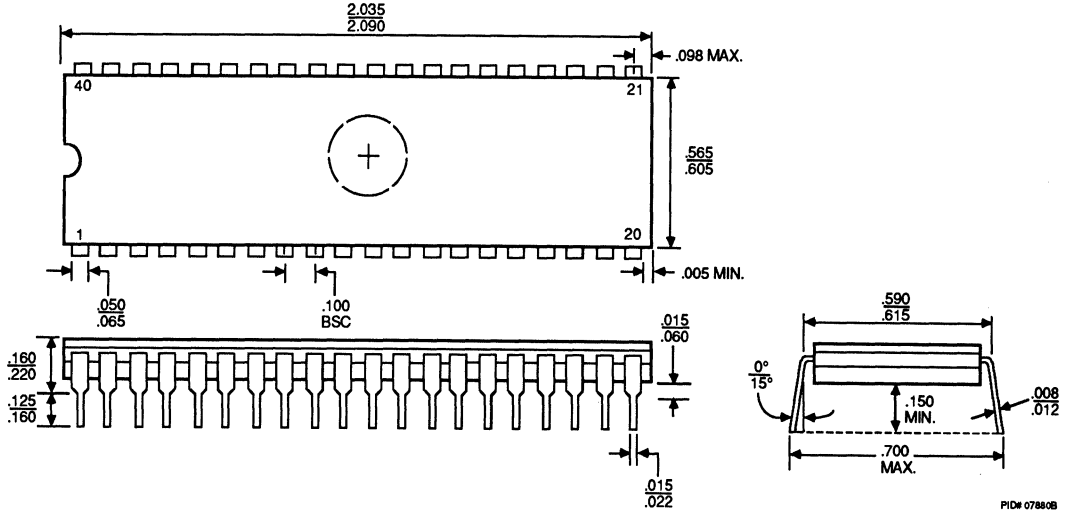
PACKAGE OUTLINES (Continued)

Ceramic DIPs (CD) (Continued)

CD 040



CDV040

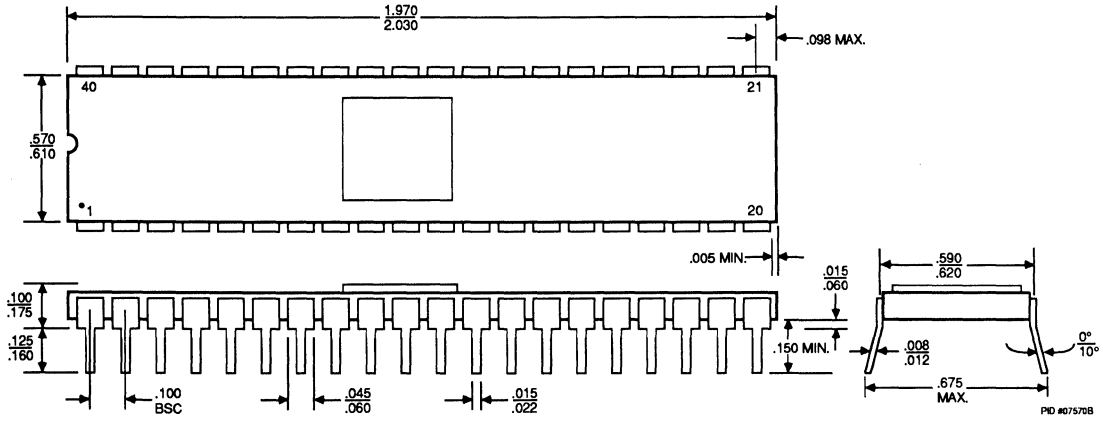


NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

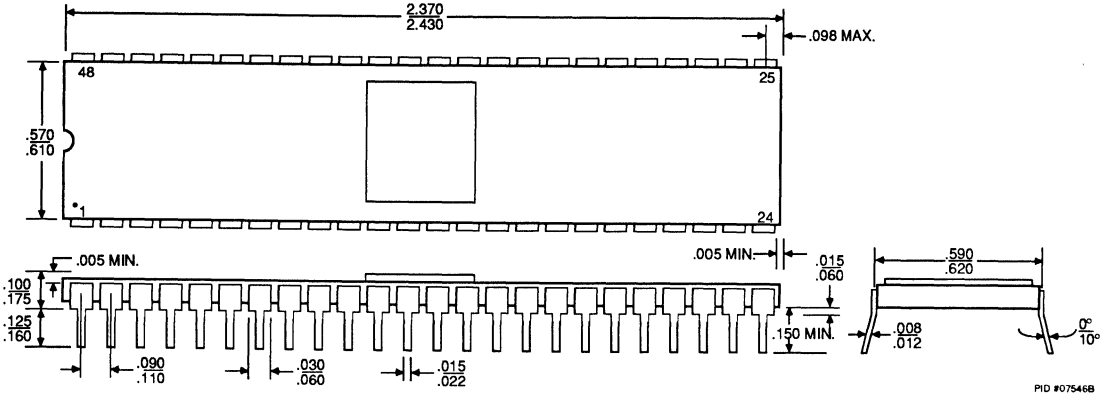
PACKAGE OUTLINES (Continued)

Ceramic Sidebrazed DIPs (SD)

SD 040



SD 048

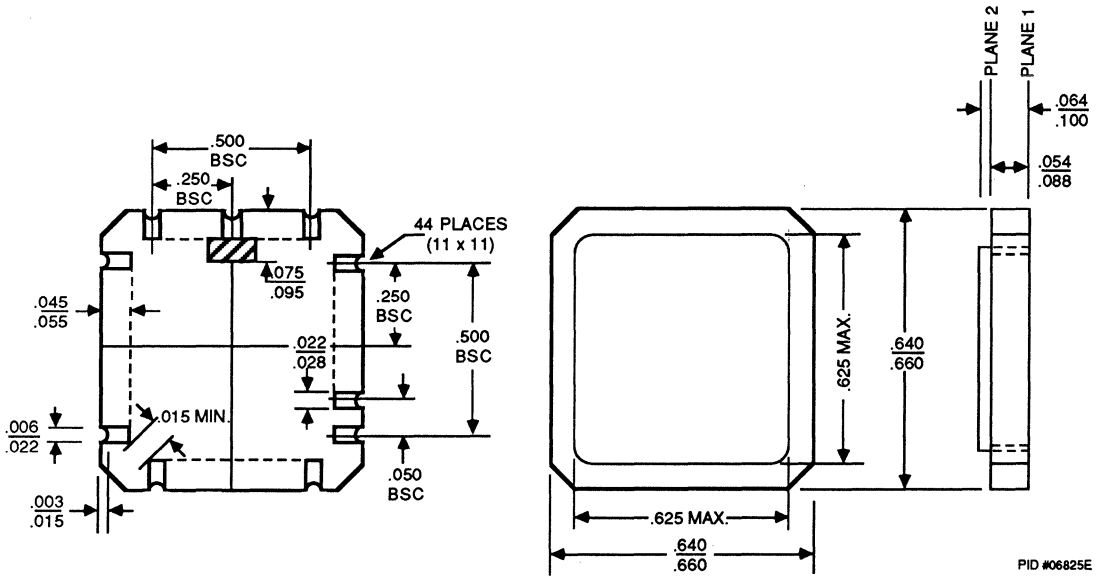


NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

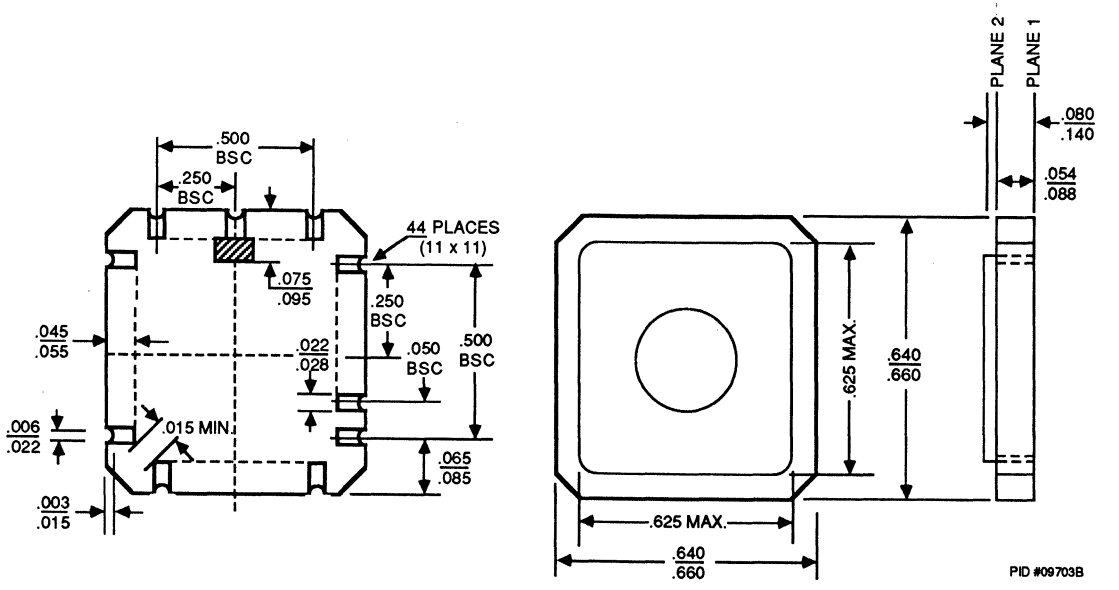
PACKAGE OUTLINES (Continued)

Ceramic Leadless Chip Carriers (CL/CLV)

CL 044



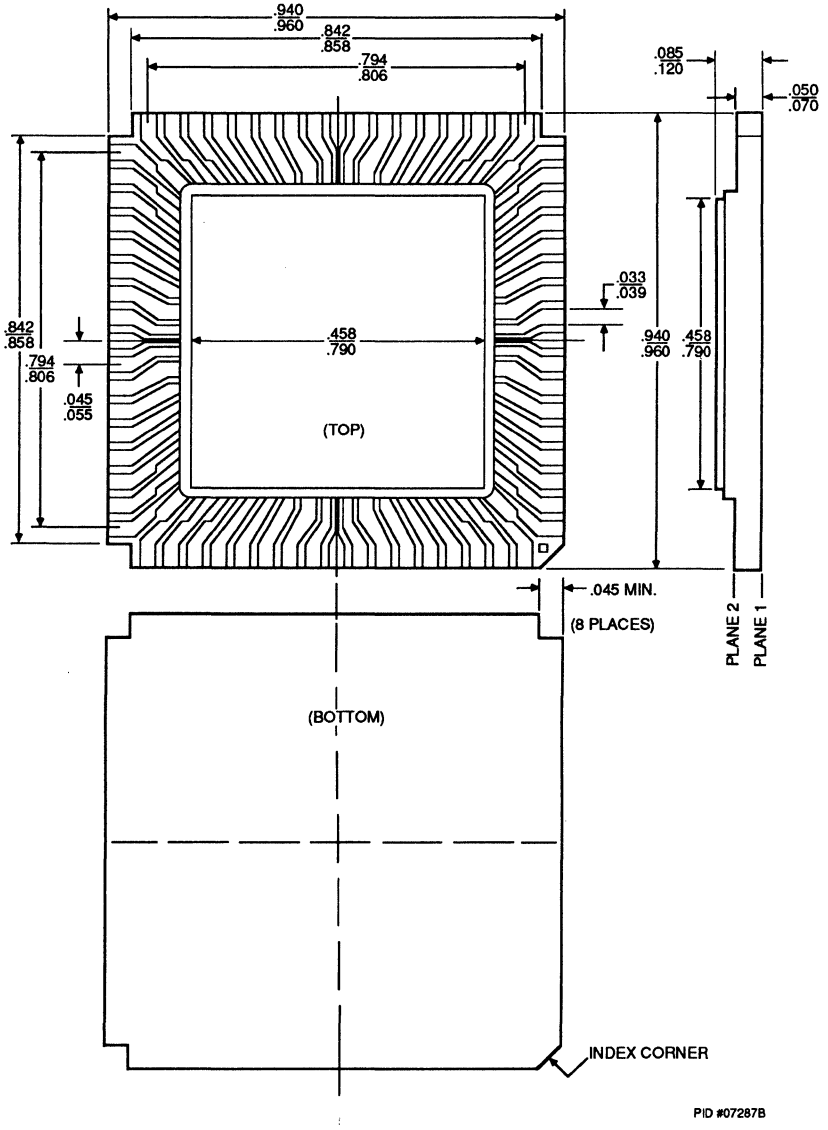
CLV044



NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

PACKAGE OUTLINES (Continued)

68-Pin Square Leadless Chip Carrier (CA2)
CA2068



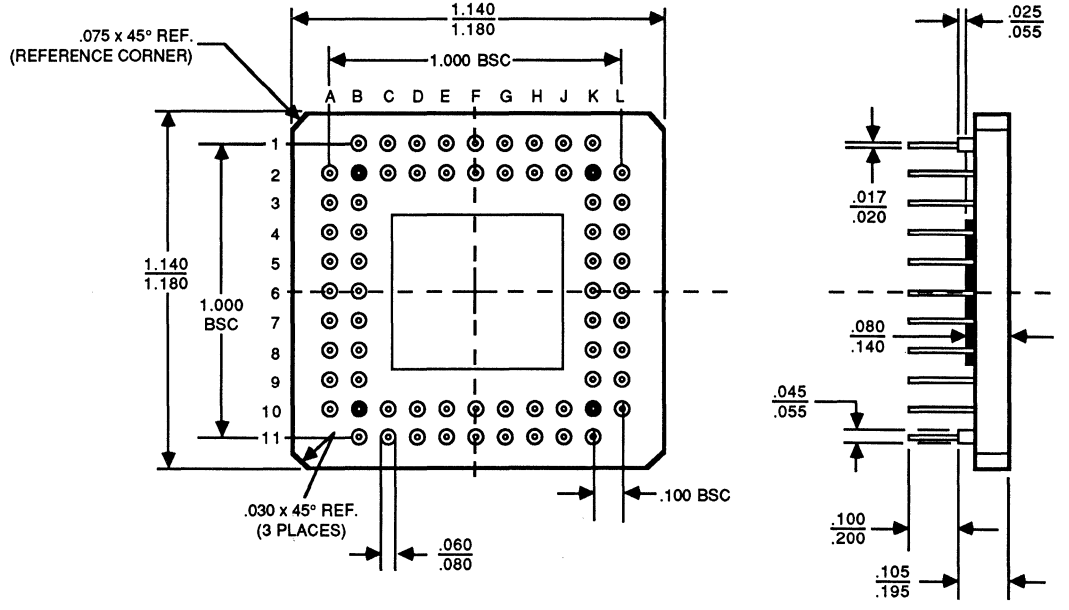
NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

PACKAGE OUTLINES (Continued)

Ceramic Pin-Grid-Array Package (CG/CGX)

CGX068

BOTTOM VIEW



PID # 07547B

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

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NOTES

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