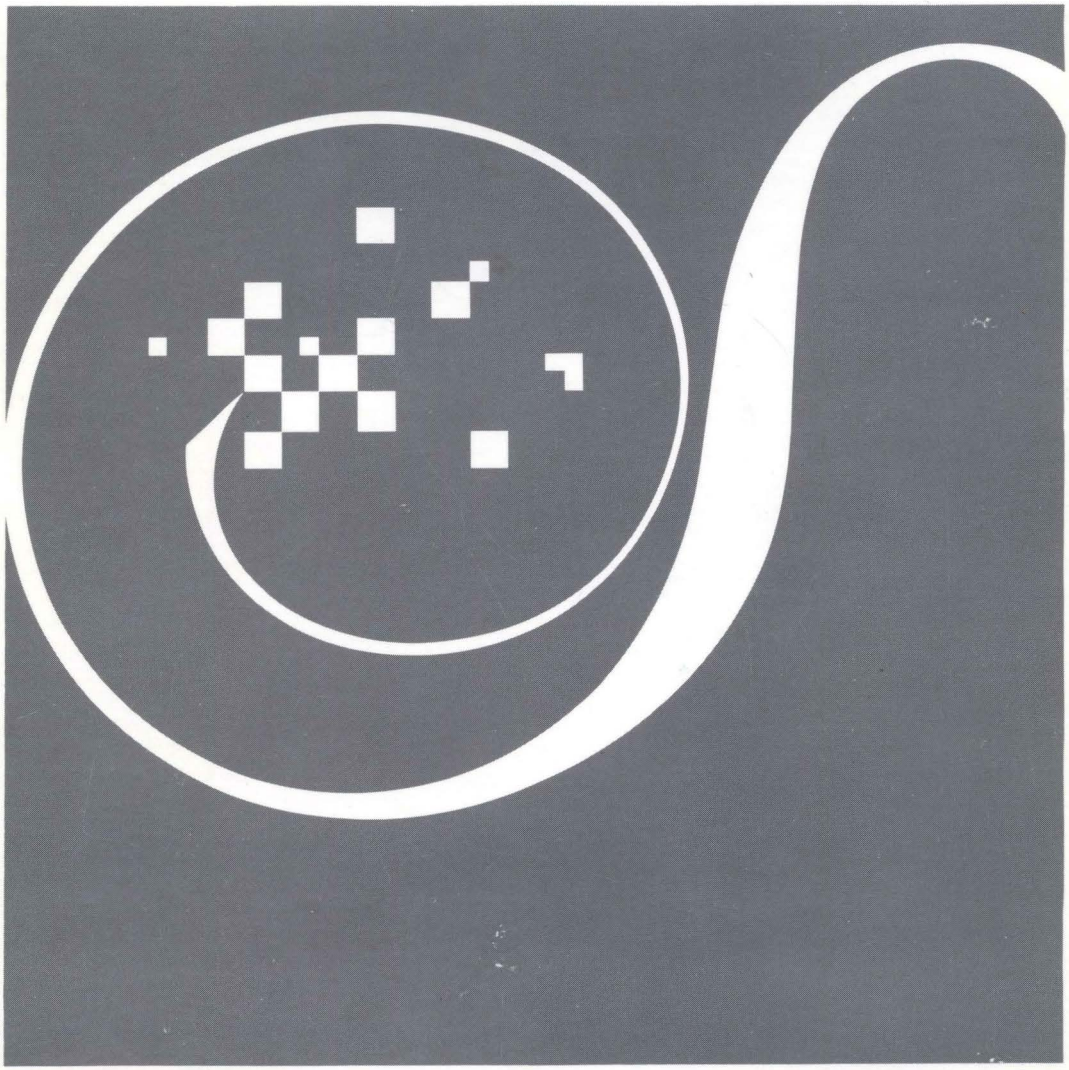
Specialty Memory Products
1988 Data Book

Advanced
Micro
Devices



Monolithic Memories MMI
A Wholly Owned Subsidiary of Advanced Micro Devices

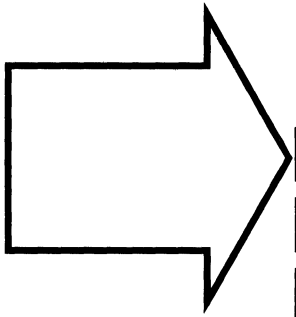
1988 Data Book

Specialty Memory Products

AMD AND MMI

Advanced
Micro
Devices

Specialty Memory Products Data Book/Handbook



Since the original printing if this material, Monolithic Memories has merged with Advanced Micro Devices. References in this handbook to either company now pertain to the new combined entity, which markets all products under the AMD name.

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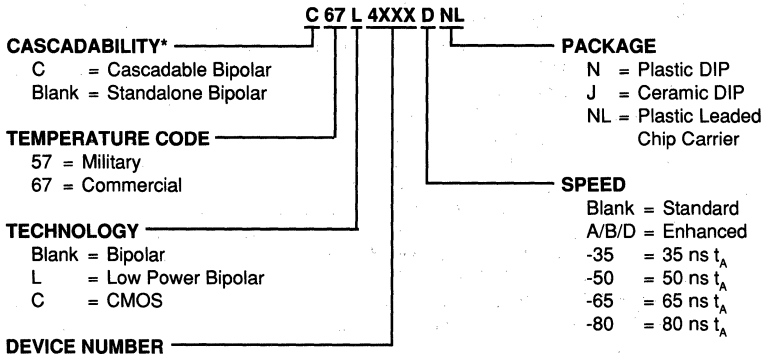
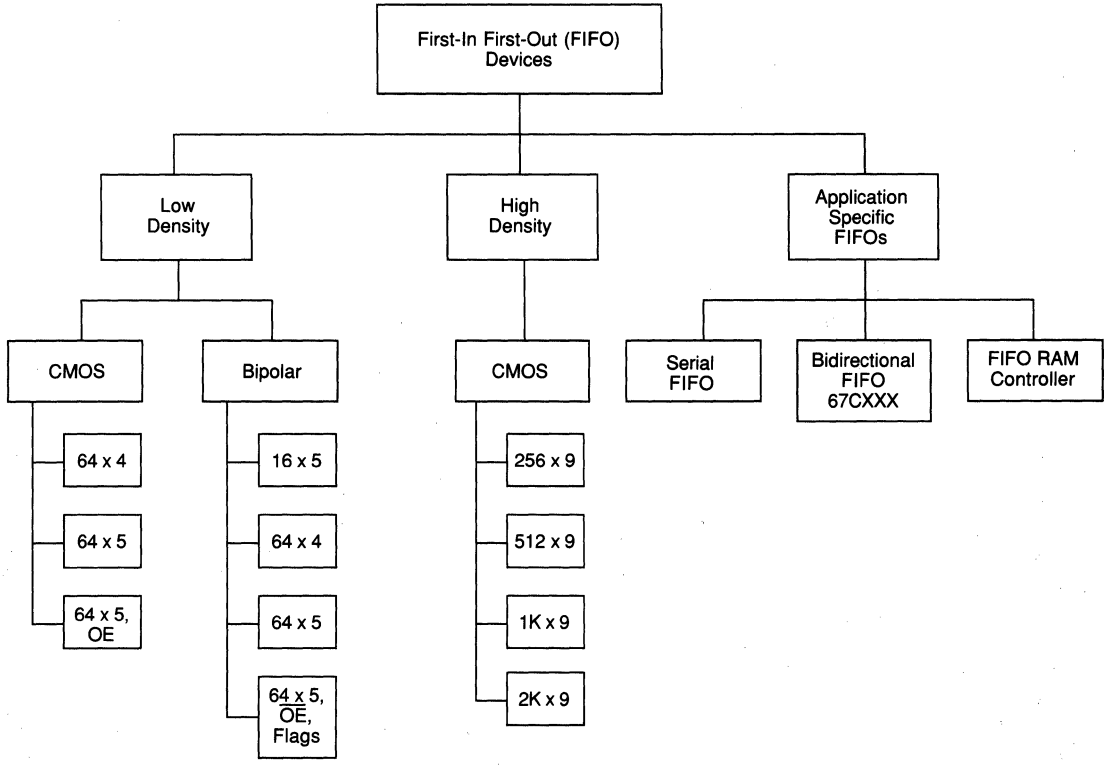
FIFO



* All CMOS devices are cascadable

First-In First-Out (FIFO) Devices



Features and Benefits

Low Density CMOS FIFOs (64x4/5)

- Zero standby power consumption
- RAM-based technology with fast access times
- Three-state output and status flags
- Expandable in width and depth

High Density CMOS FIFOs (1/4K, 1/2K, 1Kx9, 2Kx9)

- Low power consumption – 60 mA max
- Status flags – Half-full, Empty, Full
- Asynchronous and simultaneous read/write
- Expandable in width and depth

Competitive Cross Reference Guide

CYPRESS	AMD/MMI
CY7C401-5 PC	67C401-10 N
CY7C401-5 DC	67C401-10 J
CY7C401-10 PC	67C401-10 N
CY7C401-10 DC	67C401-10 J
CY7C401-15 PC	67C401-15 N
CY7C401-15 DC	67C401-15 J
CY7C402-5 PC	67C402-10 N
CY7C402-5 DC	67C402-10 J
CY7C402-10 PC	67C402-10 N
CY7C402-10 DC	67C402-10 J
CY7C402-15 PC	67C402-15 N
CY7C402-15 DC	67C402-15 J
CY7C403-5 PC	67C4013-10 N
CY7C403-5 DC	67C4013-10 J
CY7C403-10 PC	67C4013-10 N
CY7C403-10 DC	67C4013-10 J
CY7C403-15 PC	67C4013-15 N
CY7C403-15 DC	67C4013-15 J
CY7C404-5 PC	67C4023-10 N
CY7C404-5 DC	67C4023-10 J
CY7C404-10 PC	67C4023-10 N
CY7C404-10 DC	67C4023-10 J
CY7C404-15 PC	67C4023-15 N
CY7C404-15 DC	67C4023-15 J
CY7C412-40 PC	67C4501-35 N
CY7C412-40 DC	67C4501-35 J
CY7C412-40 JC	67C4501-35 NL
CY7C412-65 PC	67C4501-65 N
CY7C412-65 DC	67C4501-65 J
CY7C412-65 JC	67C4501-65 NL
CY7C424-40 PC	67C4502-35 N
CY7C424-40 DC	67C4502-35 J
CY7C424-40 JC	67C4502-35 NL
CY7C424-65 PC	67C4502-65 N
CY7C424-65 DC	67C4502-65 J
CY7C424-65 JC	67C4502-65 NL

DALLAS SEMICONDUCTOR	AMD/MMI
DS 2009	67C4501
DS 2010	67C4502

IDT	AMD/MMI
IDT 7200 S/L-35 P	67C4500-35N
IDT 7200 S/L-35 D	67C4500-35J
IDT 7200 S/L-35 J	67C4500-35NL
IDT 7200 S/L-50 P	67C4500-50N
IDT 7200 S/L-50 D	67C4500-50J
IDT 7200 S/L-50 J	67C4500-50NL
IDT 7200 S/L-65 P	67C4500-65P
IDT 7200 S/L-65 D	67C4500-65J
IDT 7200 S/L-65 J	67C4500-65NL
IDT 7200 S/L-80 P	67C4500-80 N
IDT 7200 S/L-80 D	67C4500-80 J
IDT 7200 S/L-80 J	67C4500-80 NL
IDT 7201 SA/LA-120 P	67C4501-80 N
IDT 7201 SA/LA-120 D	67C4501-80 J
IDT 7201 SA/LA-120 J	67C4501-80 NL
IDT 7201 SA/LA-80 P	67C4501-80 N
IDT 7201 SA/LA-80 D	67C4501-80 J
IDT 7201 SA/LA-80 J	67C4501-80 NL
IDT 7201 SA/LA-65 P	67C4501-65 N
IDT 7201 SA/LA-65 D	67C4501-65 J
IDT 7201 SA/LA-65 J	67C4501-65 NL
IDT 7201 SA/LA-50 P	67C4501-50 N
IDT 7201 SA/LA-50 D	67C4501-50 J
IDT 7201 SA/LA-50 J	67C4501-50 NL
IDT 7201 SA/LA-35 P	67C4501-35 N
IDT 7201 SA/LA-35 D	67C4501-35 J
IDT 7201 SA/LA-35 J	67C4501-35 NL
IDT 7201 S/L-120 P	67C4501-80 N
IDT 7201 S/L-120 D	67C4501-80 J
IDT 7201 S/L-120 J	67C4501-80 NL
IDT 7201 S/L-80 P	67C4501-80 N
IDT 7201 S/L-80 D	67C4501-80 J
IDT 7201 S/L-80 J	67C4501-80 NL
IDT 7201 S/L-65 P	67C4501-65 N
IDT 7201 S/L-65 D	67C4501-65 J
IDT 7201 S/L-65 J	67C4501-65 NL
IDT 7201 S/L-50 P	67C4501-50 N
IDT 7201 S/L-50 D	67C4501-50 J
IDT 7201 S/L-50 J	67C4501-50 NL
IDT 7202 SA/LA-120 P	67C4502-80 N
IDT 7202 SA/LA-120 D	67C4502-80 J
IDT 7202 SA/LA-120 J	67C4502-80 NL
IDT 7202 SA/LA-80 P	67C4502-80 N
IDT 7202 SA/LA-80 D	67C4502-80 J
IDT 7202 SA/LA-80 J	67C4502-80 NL
IDT 7202 SA/LA-65 P	67C4502-65 N
IDT 7202 SA/LA-65 D	67C4502-65 J
IDT 7202 SA/LA-65 J	67C4502-65 NL
IDT 7202 SA/LA-50 P	67C4502-50 N
IDT 7202 SA/LA-50 D	67C4502-50 J
IDT 7202 SA/LA-50 J	67C4502-50 NL
IDT 7202 SA/LA-35 P	67C4502-35 N
IDT 7202 SA/LA-35 D	67C4502-35 J
IDT 7202 SA/LA-35 J	67C4502-35 NL
IDT 7202 S/L-120 P	67C4502-80 N
IDT 7202 S/L-120 D	67C4502-80 J
IDT 7202 S/L-120 J	67C4502-80 NL
IDT 7202 S/L-80 P	67C4502-80 N
IDT 7202 S/L-80 D	67C4502-80 J
IDT 7202 S/L-80 J	67C4502-80 NL
IDT 7202 S/L-65 P	67C4502-65 N
IDT 7202 S/L-65 D	67C4502-65 J
IDT 7202 S/L-65 J	67C4502-65 NL
IDT 7202 S/L-50 P	67C4502-50 N
IDT 7202 S/L-50 D	67C4502-50 J
IDT 7202 S/L-50 J	67C4502-50 NL
IDT 72401 L-10 P	67C401-10 N
IDT 72401 L-10 D	67C401-10 J
IDT 72401 L-10 J	67C401-10 NL
IDT 72401 L-15 P	67C401-15 N
IDT 72401 L-15 D	67C401-15 J
IDT 72401 L-15 J	67C401-15 NL
IDT 72402 L-10 P	67C402-10 N
IDT 72402 L-10 D	67C402-10 J
IDT 72402 L-10 J	67C402-10 NL
IDT 72402 L-15 P	67C402-15 N
IDT 72402 L-15 D	67C402-15 J
IDT 72402 L-15 J	67C402-15 NL
IDT 72403 L-10 P	67C4013-10 N
IDT 72403 L-10 D	67C4013-10 J
IDT 72403 L-10 J	67C4013-10 NL
IDT 72403 L-15 P	67C4013-15 N
IDT 72403 L-15 D	67C4013-15 J
IDT 72403 L-15 J	67C4013-15 NL
IDT 72404 L-10 P	67C4023-10 N
IDT 72404 L-10 D	67C4023-10 J
IDT 72404 L-10 J	67C4023-10 NL
IDT 72404 L-15 P	67C4023-15 N
IDT 72404 L-15 D	67C4023-15 J
IDT 72404 L-15 J	67C4023-15 NL

MOSTEK	AMD/MMI
MK 4501-65 N	67C4501-65 N
MK 4501-80 N	67C4501-80 N
MK 4501-100 N	67C4501-80 N
MK 4501-120 N	67C4501-80 N

T.I.	AMD/MMI
SN74S225 N	74S225 N
SN74S225 J	74S225 J
SN74ALS236J	67411AJ
SN74 ALS235J	67413AJ
SN74ACT7202 N	67C4502N

FIFO IC Selector Guide (COM)

Low Density FIFOs

Tech-nology	Part Number	Organ-ization	Type	Max Data Rate, MHz	Max I_{CC}, mA	Package Type	Pin Count	Features
B	74S225	16x5	C	10	120	N, J	20	TSO
B	74S225A	16x5	C	20	120	N, J	20	TSO
B	C67401	64x4	C	10	160	N, J, NL	16, 20 (NL)	TPO
B	67401	64x4	S	10	160	N, J, NL	16, 20 (NL)	TPO
B	C67401A	64x4	C	15	170	N, J, NL	16, 20 (NL)	TPO
B	67401A	64x4	S	15	170	N, J, NL	16, 20 (NL)	TPO
B	C67401B	64x4	C	16.7	180	J	16	TPO
B	67401B	64x4	S	16.7	180	J	16	TPO
B	C67L401D	64x4	C	15	100	N, J	16	TPO Low Power I_{OL} = 24 mA
B	C67L4013D	64x4	C	15	100	N, J	16	TSO Low Power I_{OL} = 24 mA
B	C67402	64x5	C	10	180	N, J, NL	18, 20 (NL)	TPO
B	67402	64x5	S	10	180	N, J, NL	18, 20 (NL)	TPO
B	C67402A	64x5	C	15	190	J	18	TPO
B	67402A	64x5	S	15	190	J	18	TPO
B	C67402B	64x5	C	16.7	200	J	18	TPO
B	67402B	64x5	S	16.7	200	J	18	TPO
B	C67L402D	64x5	C	15	100	N, J	18	TPO Low Power I_{OL} = 24 mA
B	C67L4033D	64x5	C	15	115	N, J	20	TSO Low Power I_{OL} = 24 mA, Status Flags
C	67C401-10	64x4	C	10	35	N, J, NL	16	TPO Low Power, RAM Based
C	67C401-15	64x4	C	15	45	N, J, NL	16	TPO Low Power, RAM Based
C	67C4013-10	64x4	C	10	35	N, J, NL	16	TSO Low Power, RAM Based
C	67C4013-15	64x4	C	15	45	N, J, NL	16	TSO Low Power, RAM Based
C	67C402-10	64x5	C	10	35	N, J, NL	18	TPO Low Power, RAM Based
C	67C402-15	64x5	C	15	45	N, J, NL	18	TPO Low Power, RAM Based
C	67C4023-10	64x5	C	10	35	N, J, NL	18	TSO Low Power, RAM Based
C	67C4023-15	64x5	C	15	45	N, J, NL	18	TSO Low Power, RAM Based
C	67C4033-10	64x5	C	10	35	N, J, NL	20	TSO Low Power, RAM Based, Status Flags
C	67C4033-15	64x5	C	15	45	N, J, NL	20	TSO Low Power, RAM Based, Status Flags
B	67411	64x4	S	25	240	J	16	TPO
B	67411A	64x4	S	35	240	J	16	TPO
B	67412	64x4	S	25	240	J	18	TPO
B	67412A	64x4	S	35	240	J	18	TPO
B	67413	64x4	S	25	240	J	20	TSO, Status Flags
B	67413A	64x4	S	35	240	J	20	TSO, Status Flags

Notes:

Technology:
B – Bipolar
C – CMOS

C – Cascadable
S – Standalone

PackageType:
N – Plastic
J – Ceramic
NL – PLCC

Features:
TSO – Three State Output
TPO – Totem Pole Output

High Density FIFOs

Tech-nology	Part Number	Organ-ization	Type	Max Data Rate, MHz	Max I_{CC}, mA	Package Type	Pin Count	Features
C	67C4500-80	256x9	C	10	60	N, J, NL	28, 32 (NL)	TSO Access Time=80 ns, Status Flags
C	67C4500-65	256x9	C	12	60	N, J, NL	28, 32 (NL)	TSO Access Time=65 ns, Status Flags
C	67C4500-50	256x9	C	15	60	N, J, NL	28, 32 (NL)	TSO Access Time=50 ns, Status Flags
C	67C4500-35	256x9	C	22	60	N, J, NL	28, 32 (NL)	TSO Access Time=35 ns, Status Flags
C	67C4501-80	512x9	C	10	60	N, J, NL	28, 32 (NL)	TSO Access Time=80 ns, Status Flags
C	67C4501-65	512x9	C	12	60	N, J, NL	28, 32 (NL)	TSO Access Time=65 ns, Status Flags
C	67C4501-50	512x9	C	15	60	N, J, NL	28, 32 (NL)	TSO Access Time=50 ns, Status Flags
C	67C4501-35	512x9	C	22	60	N, J, NL	28, 32 (NL)	TSO Access Time=35 ns, Status Flags
C	67C4502-80	1Kx9	C	10	60	N, J, NL	28, 32 (NL)	TSO Access Time=80 ns, Status Flags
C	67C4502-65	1Kx9	C	12	60	N, J, NL	28, 32 (NL)	TSO Access Time=65 ns, Status Flags
C	67C4502-50	1Kx9	C	15	60	N, J, NL	28, 32 (NL)	TSO Access Time=50 ns, Status Flags
C	67C4502-35	1Kx9	C	22	60	N, J, NL	28, 32 (NL)	TSO Access Time=35 ns, Status Flags
C	67C4503-80	2Kx9	C	10	60	N, J, NL	28, 32 (NL)	TSO Access Time=80 ns, Status Flags
C	67C4503-65	2Kx9	C	12	60	N, J, NL	28, 32 (NL)	TSO Access Time=65 ns, Status Flags
C	67C4503-50	2Kx9	C	15	60	N, J, NL	28, 32 (NL)	TSO Access Time=50 ns, Status Flags
C	67C4503-35	2Kx9	C	22	60	N, J, NL	28, 32 (NL)	TSO Access Time=35 ns, Status Flags

Application Specific FIFOs

Tech-nology	Part Number	Organ-ization	Type	Max Data Rate, MHz	Max I_{CC}, mA	Package Type	Pin Count	Features
B	67417	64xm/9/1	S	10 Par. 28 Ser.	350	J	24	TSO Parallel/Serial, Status Flags
B	674219	512-64K	S	10	350	J	40	TSO FIFO RAM Controller, 16-Bit SRAM Address, Status Flags

Bidirectional FIFO

Tech-nology	Part Number	Organ-ization	Type	Max Data Rate, MHz	Max I_{CC}, mA	Package Type	Pin Count	Features
C	67C4701	Dual 512x9	S	16	100	N	28	TSO, Programmable Status Flags, Mailbox

Notes:

Technology:
B – Bipolar
C – CMOS

C – Cascadable
S – Standalone

PackageType:
N – Plastic
J – Ceramic
NL – PLCC

Features:
TSO – Three-State Output
TPO – Totem-Pole Output

FIFO IC Selector Guide (MIL)

Low Density FIFOs

Technology	Part Number	Organization	Type	Max Data Rate, MHz	Max I_{CC}, mA	Package Type	Pin Count	Features
B	C57401	64x4	C	7	160	J, L	16, 20 (LCC)	TPO
B	57401	64x4	S	7	160	J, L	16, 20 (LCC)	TPO
B	C57401A	64x4	C	10	180	J, L	16, 20 (LCC)	TPO
B	57401A	64x4	S	10	180	J, L	16, 20 (LCC)	TPO
B	57L401D	64x4	S	12	120	J	16	TPO Low Power I_{OL} = 12 MA
B	57L4013D	64x4	S	12	120	J	16	TSO Low Power I_{OL} = 12 MA
B	C57402	64x5	C	7	180	J, L	18, 20 (LCC)	TPO
B	57402	64x5	S	7	180	J, L	18, 20 (LCC)	TPO
B	C57402A	64x5	C	10	200	J	18	TPO
B	57402A	64x5	S	10	200	J	18	TPO
B	57L402D	64x5	S	12	120	J	18	TPO Low Power I_{OL} = 12 MA
C	57C401-12	64x4	C	12	40	J	16	TPO Low Power, RAM Based
C	57C4013-12	64x4	C	12	40	J	16	TSO Low Power, RAM Based
C	57C402-12	64x5	C	12	40	J	18	TPO Low Power, RAM Based
C	57C4023-12	64x5	C	12	40	J	18	TSO Low Power, RAM Based
C	57C4033-12	64x5	C	12	40	J	20	TSO Low Power, RAM Based, Status Flags
B	57413A	64x5	S	25	240	J	20	TSO, Status Flags

High Density FIFOs

Technology	Part Number	Organization	Type	Max Data Rate, MHz	Max I_{CC}, mA	Package Type	Pin Count	Features
C	57C4500-80	256x9	C	10	80	J	28	TSO Access Time = 80 ns, Status Flags
C	57C4500-65	265x9	C	12	80	J	28	TSO Access Time = 65 ns, Status Flags
C	57C4500-50	265x9	C	15	80	J	28	TSO Access Time = 50 ns, Status Flags
C	57C4500-40	265x9	C	20	80	J	28	TSO Access Time = 40 ns, Status Flags
C	57C4501-80	512x9	C	10	80	J	28	TSO Access Time = 80 ns, Status Flags
C	57C4501-65	512x9	C	12	80	J	28	TSO Access Time = 65 ns, Status Flags
C	57C4501-50	512x9	C	15	80	J	28	TSO Access Time = 50 ns, Status Flags
C	57C4501-40	512x9	C	20	80	J	28	TSO Access Time = 40 ns, Status Flags
C	57C4502-80	1Kx9	C	10	80	J	28	TSO Access Time = 80 ns, Status Flags
C	57C4502-65	1Kx9	C	12	80	J	28	TSO Access Time = 65 ns, Status Flags
C	57C4502-50	1Kx9	C	15	80	J	28	TSO Access Time = 50 ns, Status Flags
C	57C4502-40	1Kx9	C	20	80	J	28	TSO Access Time = 40 ns, Status Flags

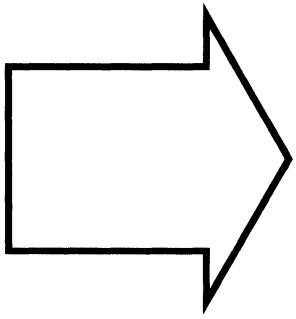
Notes:

Technology:
B – Bipolar
C – CMOS

C – Cascadable
S – Standalone

PackageType:
N – Plastic
J – Ceramic
NL – PLCC
L – Leadless Chip Carrier

Features:
TSO – Three State Output
TPO – Totem Pole Output



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Commercial Datasheets

First-In First-Out (FIFO) 64x4 64x5
Standalone Memory

67401 67401A 67401B
67402 67402A 67402B

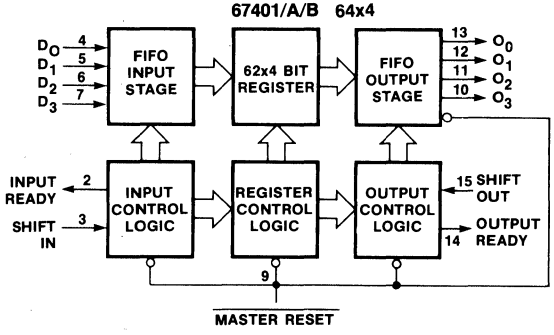
Features/Benefits
- Choice of 16.7, 15 and 10 MHz shift-out/shift-in rates
- Choice of 4-bit or 5-bit data width
- TTL inputs and outputs
- Readily expandable in the word dimension only
- Structured pin outs. Output pins directly opposite corresponding input pins
- Asynchronous operation

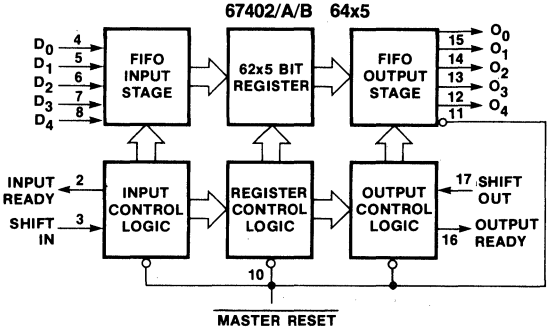
Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
67401	J,N,NL(20)	Com	10 MHz 64x4 FIFO
67402	J,N,NL(20)	Com	10 MHz 64x5 FIFO
67401A	J,N,NL(20)	Com	15 MHz 64x4 FIFO
67402A	J,N,NL(20)	Com	15 MHz 64x5 FIFO
67401B	J	Com	16.7 MHz 64x4 FIFO
67402B	J	Com	16.7 MHz 64x5 FIFO

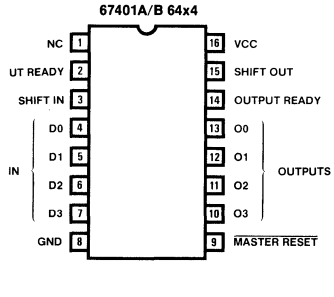
Description
The 67401B/2B/1A/2A/1/2 are "fall-through" high speed First-In First-Out (FIFO) memory organized 64 words by 4-bits and 64 words by 5-bits respectively. A 16.7 MHz data rate allows usage in digtal video systems; a 15 MHz data rate allows usage in high speed tape or disc controllers and communication buffer applications. Word length is expandable; FIFO depth is not expandable.

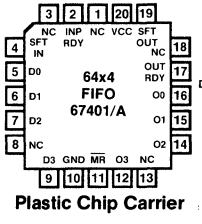
Block Diagrams



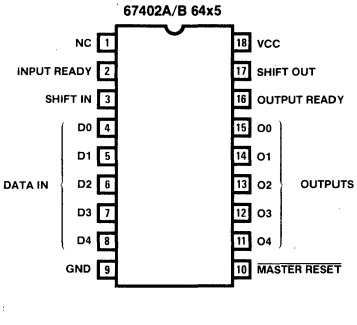


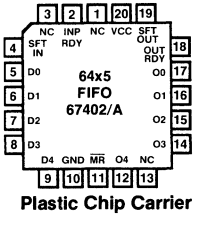
Pin Configurations





Plastic Chip Carrier





Plastic Chip Carrier

Publication # 10676 | Rev. A | Amendment /0
Issue Date: May 1988

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -1.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	67401B/2B MIN	TYP	MAX	67401A/2A MIN	TYP	MAX	67401/2 MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
T_A	Operating free-air temperatue		0		75	0		75	0		75	°C
t_{SIH}†	Shift in HIGH time	1	18			23		28†	35			ns
t_{SIL}	Shift in LOW time	1	18			25			35			ns
t_{IDS}	Input data setup	1	5			5			5			ns
t_{IDH}	Input data hold time	1	40			40			45			ns
t_{SOH}†	Shift Out HIGH time	5	18			23			35			ns
t_{SOL}	Shift Out LOW time	5	18			25			35			ns
t_{MRW}	Master Reset pulse	10	35			35			35			ns
t_{MRS}	Master Reset to SI	10	35			35			35			ns

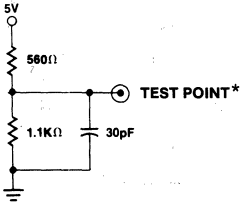
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	C67401B/2B MIN	TYP	MAX	C67401A/2A MIN	TYP	MAX	C67401/2 MIN	TYP	MAX	UNIT
f_{IN}	Shift in rate	1	16.7			15			10			MHz
t_{IRL}†	Shift In to Input Ready LOW	1			35			40			45	ns
t_{IRH}†	Shift In to Input Ready HIGH	1			37			40			45	ns
f_{OUT}†	Shift Out rate	5	16.7			15			10			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			38			45			55	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			48			50			60	ns
t_{ODH}	Output Data Hold (previous word)	5	5			10			10			ns
t_{ODS}	Output Data Shift (next word)	5			44			45			55	ns
t_{PT}	Data throughput or "fall through"	4, 8			1.45			1.6			3	μs
t_{MRORL}	Master Reset to OR LOW	10			55			60			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			55			60			60	ns
t_{IPH}*	Input Ready pulse HIGH	4	15			20			20			ns
t_{OPH}*	Output Ready pulse HIGH	8	15			20			20			ns

†See AC test and high speed application note.

Test Load

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



Input Pulse 0 to 3 V
Input Rise and Fall Time (10% - 90%)
5 ns minimum
Measurements made at 1.5 V

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150°C

Operating Conditions 67401A/2A

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	23		28†	ns
t_{SIL}	Shift in LOW time	1	25			ns
t_{IDS}	Input data setup	1	5			ns
t_{IDH}	Input data hold time	1	40			ns
t_{SOH}†	Shift Out HIGH time	5	23			ns
t_{SOL}	Shift Out LOW time	5	25			ns
t_{MRW}	Master Reset pulse	10	35			ns
t_{MRS}	Master Reset to SI	10	35			ns

2

Switching Characteristics 67401A/2A Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	15			MHz
t_{IRL}†	Shift In to Input Ready LOW	1			40	ns
t_{IRH}†	Shift In to Input Ready HIGH	1			40	ns
f_{OUT}	Shift Out rate	5	15			MHz
t_{ORL}†	Shift Out to Output'Ready LOW	5			45	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			50	ns
t_{ODH}	Output Data Hold (previous word)	5	10			ns
t_{ODS}	Output Data Shift (next word)	5			45	ns
t_{PT}	Data throughput or "fall through"	4, 8			1.6	μs
t_{MRORL}	Master Reset to OR LOW	10			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			60	ns
t_{IPH}	Input Ready pulse HIGH	4	20			ns
t_{OPH}	Output Ready pulse HIGH	8	20			ns

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150°C

Operating Conditions 67401/2

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	35			ns
t_{SIL}	Shift in LOW time	1	35			ns
t_{IDS}	Input data setup	1	5			ns
t_{IDH}	Input data hold time	1	45			ns
t_{SOH}†	Shift Out HIGH time	5	35			ns
t_{SOL}	Shift Out LOW time	5	35			ns
t_{MRW}	Master Reset pulse†	10	35			ns
t_{MRS}	Master Reset to SI	10	35			ns

Switching Characteristics 67401/2 Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	10			MHz
t_{IRL}†	Shift In to Input Ready LOW	1			45	ns
t_{IRH}†	Shift In to Input Ready HIGH	1			45	ns
f_{OUT}	Shift Out rate	5	10			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			55	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			60	ns
t_{ODH}	Output Data Hold (previous word)	5	10			ns
t_{ODS}	Output Data Shift (next word)	5			55	ns
t_{PT}	Data throughput or "fall through"	4, 8			3	μs
t_{MRORL}	Master Reset to OR LOW	10			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			60	ns
t_{IPH}	Input Ready pulse HIGH	4	20			ns
t_{OPH}	Output Ready pulse HIGH	8	20			ns

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8†	V
V_{IH}	High-level input voltage				2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL1}	Low-level input current	D_0-D_n, $\overline{MR}$	V_{CC} = MAX	V_I = 0.45V			−0.8	mA
I_{IL2}		SI, SO					−1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		VCC = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = −0.9mA	2.4			V
I_{OS}	Output short-circuit current *		V_{CC} = MAX	V_0 = 0V	−20		−90	mA
I_{CC}	Supply current		V_{CC} = MAX, All inputs low, All outputs open.	67401			160	
				67402			180	
				67401A			170	
				67402A			190	
				67401B			180	
				67402B			200	

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
†There are absolute voltages with respect to degree GND (PIN 8 or 9) and includes all overshoots due to test equipment.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitance and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift In-Input Ready combination, as well as the Shift Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency or FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going High. This same type of problem is also related to t_{IRH}, t_{ORL} and t_{ORH} as related to Shift-Out.

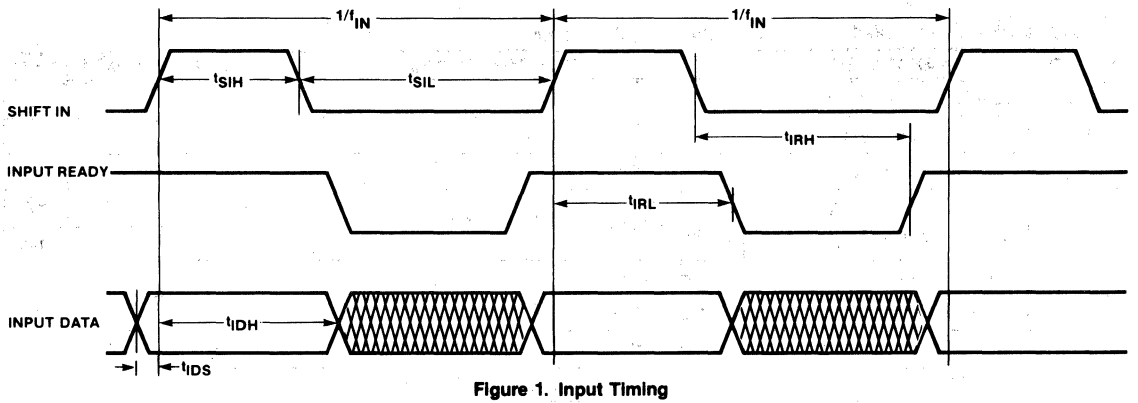


Figure 1. Input Timing

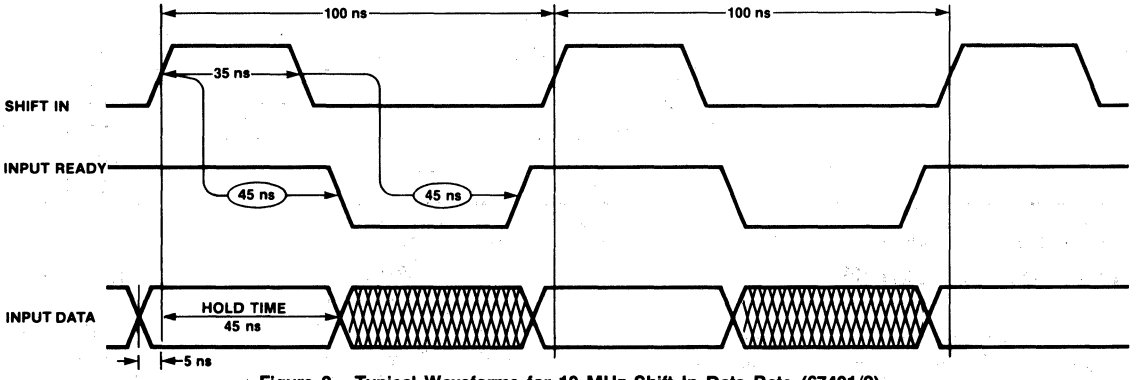


Figure 2. Typical Waveforms for 10 MHz Shift In Data Rate (67401/2)

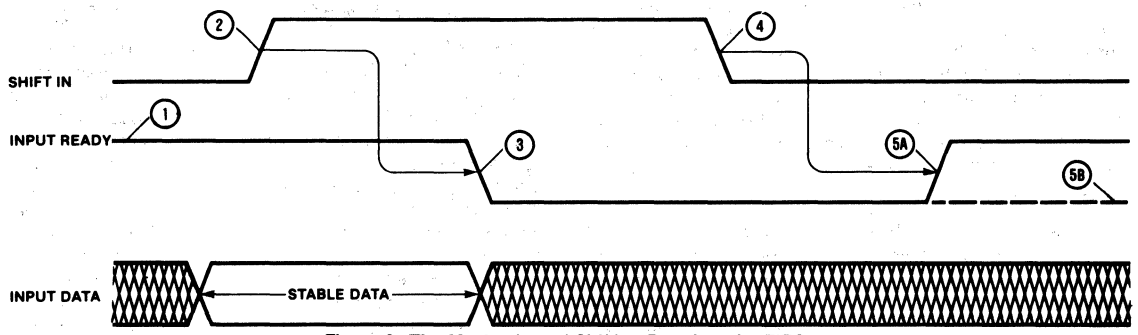


Figure 3. The Mechanism of Shifting Data into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied.

(2) Input Data is loaded into the first word.

(3) Input Ready goes LOW indicating the first word is full.

(4) The Data from the first word is released for "fall-through" to second word.

(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored. (See Figure 4.)

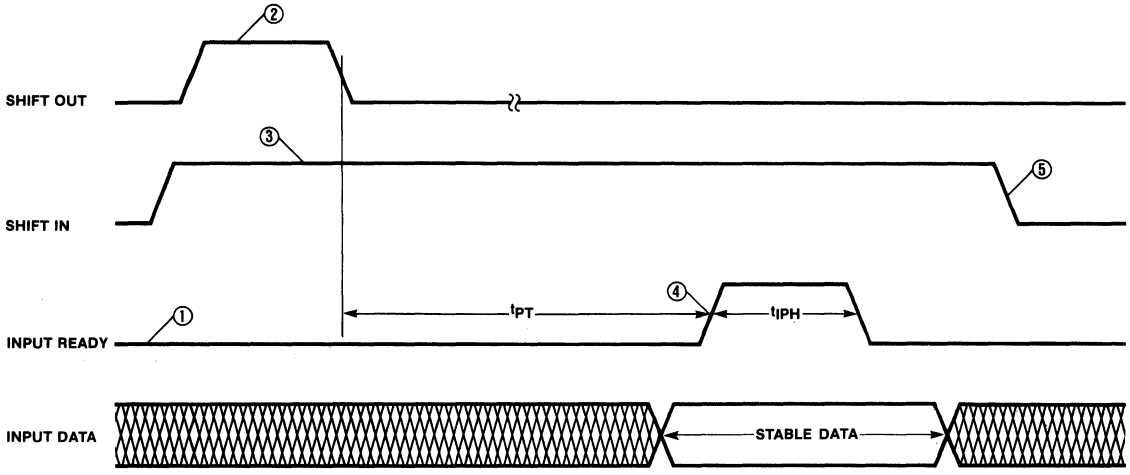


Figure 4. Data is Shifted In Whenever Shift In and Input Ready are Both HIGH

(1) FIFO is initially full.

(2) Shift Out pulse is applied. An empty location starts "bubbling" to the front.

(3) Shift In is held HIGH.

(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

(5) The Data from the first word is released for "fall through" to second word.

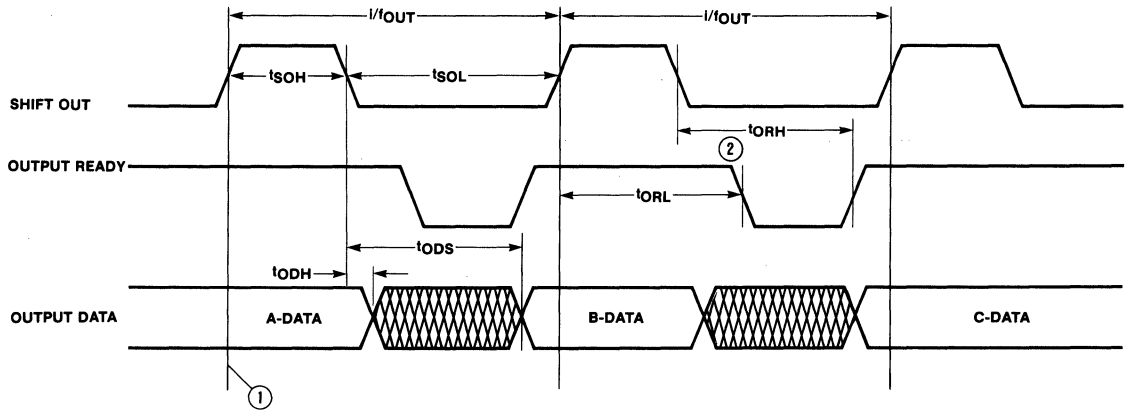


Figure 5. Output Timing

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data is shifted out when Shift Out makes a HIGH to LOW transition.

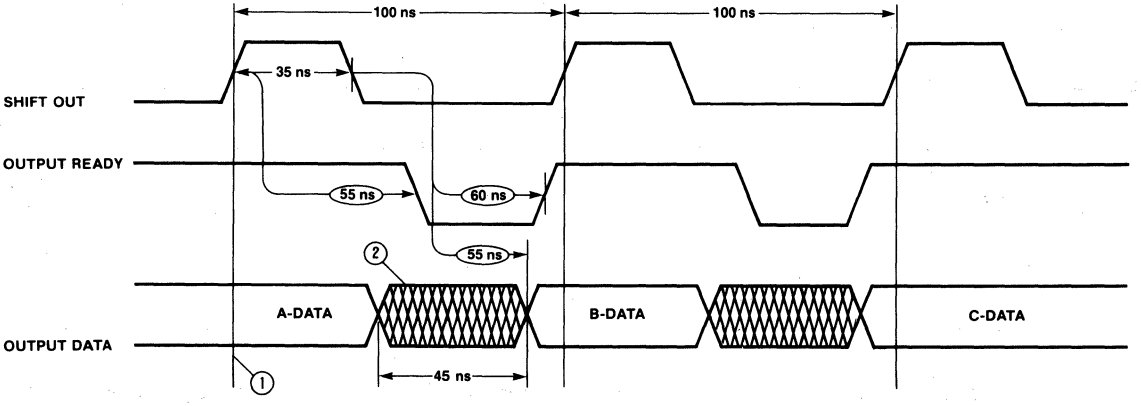


Figure 6. Typical Waveforms for 10 MHz Shift Out Data Rate (67401/2)

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data in the crosshatched region may be A or B Data.

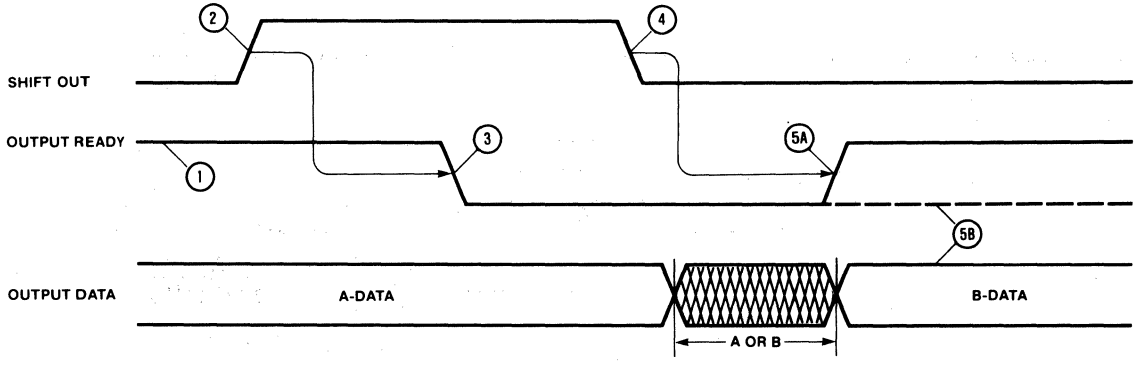


Figure 7. The Mechanism of Shifting Data Out of the FIFO.

(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

(2) Shift Out goes HIGH causing the next step.

(3) Output Ready goes LOW.

(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

NOTE: Shift Out pulses applied when Output Ready is LOW will be ignored.

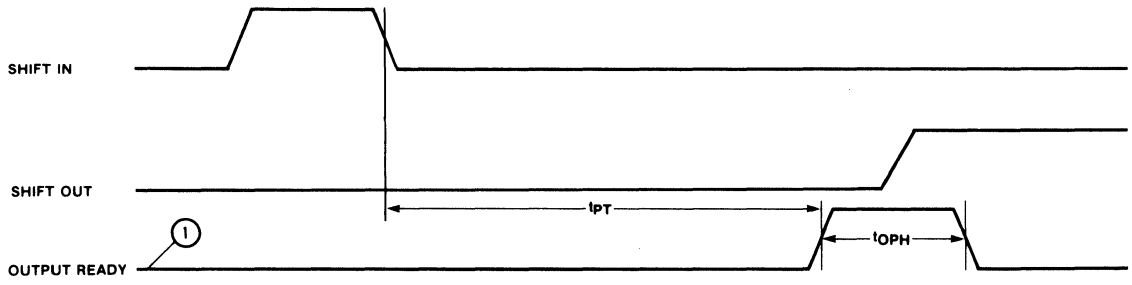


Figure 8. t_{PT} and t_{OPH} Specification

(1) FIFO initially empty.

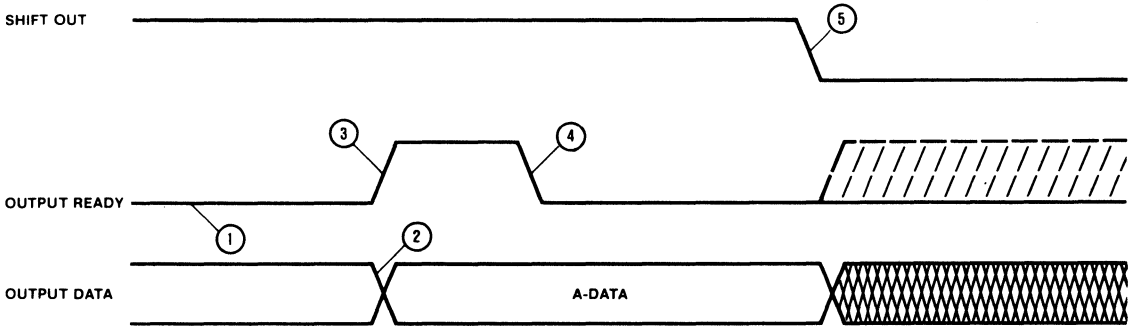


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

(1) Word 63 is empty.

(2) New data (A) arrives at the outputs (word 63).

(3) Output Ready goes HIGH indicating the arrival of the new data.

(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.

(5) As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.

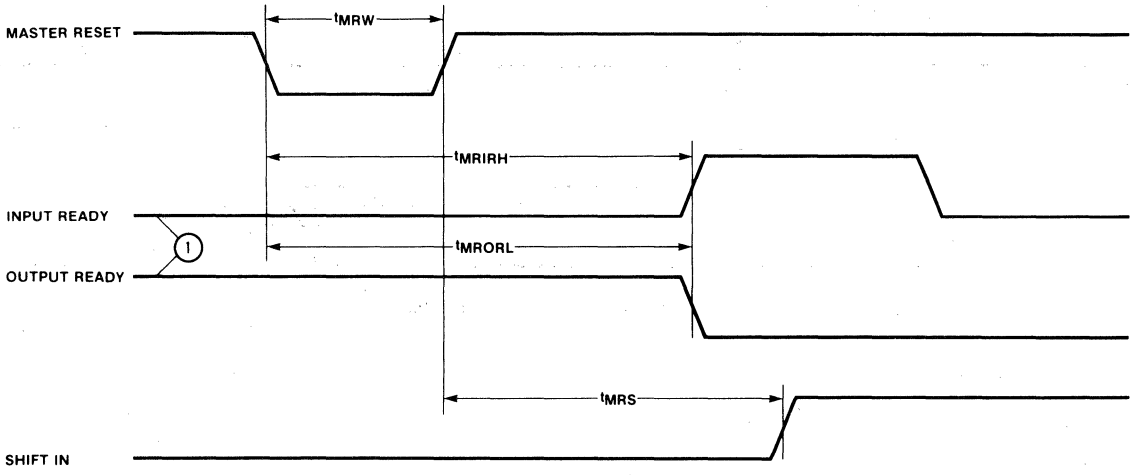


Figure 10. Master Reset Timing

(1) FIFO initially full.

First-In First-Out (FIFO) 64x4 64x5 Cascadable Memory

C67401 C67401A C67401B C67402 C67402A C67402B

Features/Benefits

- **Choice of 16.7, 15 and 10 MHz shift-out/shift-in rates**
- **Choice of 4-bit or 5-bit data width**
- **TTL inputs and outputs**
- **Readily expandable in the word and bit dimensions**
- **Structured pinouts. Output pins directly opposite corresponding input pins**
- **Asynchronous operation**

Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
C67401	J,N,NL(20)	Com	10 MHz 64x4 FIFO
C67402	J,N,NL(20)	Com	10 MHz 64x5 FIFO
C67401A	J,N,NL(20)	Com	15 MHz 64x4 FIFO
C67402A	J,N,NL(20)	Com	15 MHz 64x5 FIFO
C67401B	J	Com	16.7 MHz 64x4 FIFO
C67402B	J	Com	16.7 MHz 64x5 FIFO

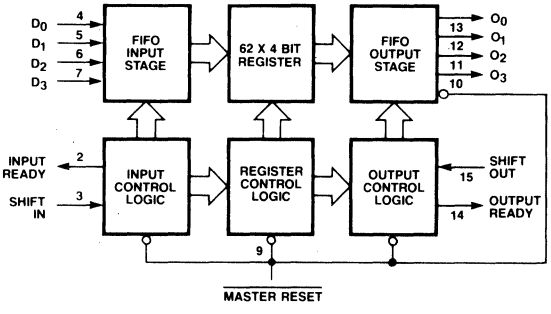
Description

The C5/C67401B/2B/1A/2A/1/2 are "fall-through" high speed First-In First-Out (FIFO) memory organized 64 words by 4 bits and 64 words by 5 bits respectively. A 16.7 MHz data rate allows usage in digital video systems; a 15 MHz data rate allows usage in high speed tape or disc controllers and communications buffer applications. Both word length and FIFO depth are expandable.

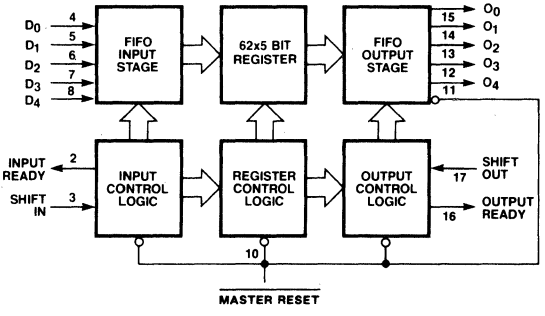
2

Block Diagrams

C67401A/B 64x4

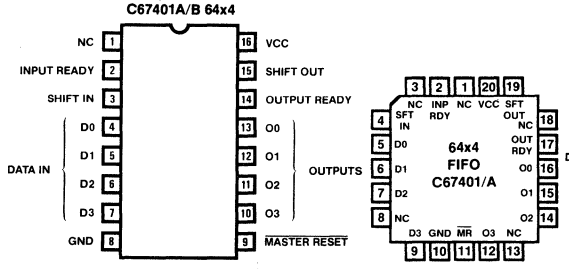


C67402A/B 64x5

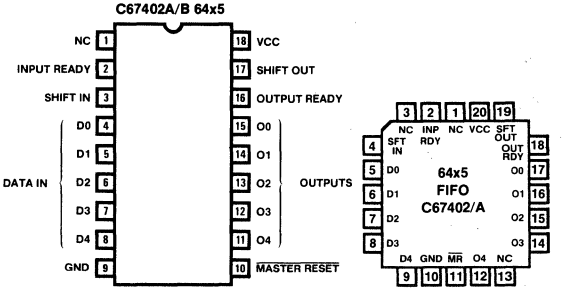


Pin Configurations

C67401A/B 64x4



C67402A/B 64x5



Publication #	Rev.	Amendment
10675	A	/0

Issue Date: May 1988

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	C67401B/2B MIN	C67401B/2B TYP	C67401B/2B MAX	C67401A/2A MIN	C67401A/2A TYP	C67401A/2A MAX	C67401/2 MIN	C67401/2 TYP	C67401/2 MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	0		75	0		75	°C
t_{SIH}†	Shift in HIGH time	1	18			23			23			ns
t_{SIL}	Shift in LOW time	1	18			25			35			ns
t_{IDS}	Input data setup	1	0			0			0			ns
t_{IDH}	Input data hold time	1	40			40			45			ns
t_{SOH}†	Shift Out HIGH time	5	18			23			23			ns
t_{SOL}	Shift Out LOW time	5	18			25			35			ns
t_{MRW}	Master Reset pulse	10	35			35			35			ns
t_{MRS}	Master Reset to SI	10	35			35			35			ns

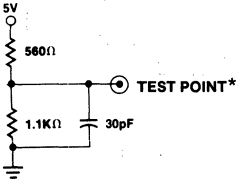
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	67401B/2B MIN	67401B/2B TYP	67401B/2B MAX	67401A/2A MIN	67401A/2A TYP	67401A/2A MAX	67401/2 MIN	67401/2 TYP	67401/2 MAX	UNIT
f_{IN}	Shift in rate	1	16.7			15			10			MHz
t_{IRL}	Shift In to Input Ready LOW	1			35			40			45	ns
t_{IRH}	Shift In to Input Ready HIGH	1			37			40			45	ns
f_{OUT}	Shift Out rate	5	16.7			15			10			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			38			45			55	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			48			50			60	ns
t_{ODH}	Output Data Hold (previous word)	5	5			10			10			ns
t_{ODS}	Output Data Shift (next word)	5			44			45			55	ns
t_{PT}	Data throughput or "fall through"	4, 8			1.45			1.6			3	μs
t_{MRORL}	Master Reset to OR LOW	10			55			60			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			55			60			60	ns
t_{IPH}	Input Ready pulse HIGH	4	15			20			20			ns
t_{OPH}*	Output Ready pulse HIGH	8	15			20			20			ns

†See AC test and High Speed application note.
*This parameter applies to FIFOs communicating with each other in a cascaded mode.

Test Load

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



Input Pulse 0 to 3 V
Input Rise and Fall Time (10% - 90%)
5 ns minimum
Measurements made at 1.5 V

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150°C

Operating Conditions C67401A/2A

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	23			ns
t_{SIL}	Shift in LOW time	1	25			ns
t_{IDS}	Input data setup	1	0			ns
t_{IDH}	Input data hold time	1	40			ns
t_{SOH}†	Shift Out HIGH time	5	23			ns
t_{SOL}	Shift Out LOW time	5	25			ns
t_{MRW}	Master Reset pulse	10	35			ns
t_{MRS}	Master Reset to SI	10	35			ns

Switching Characteristics C67401A/2A Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	15			MHz
t_{IRL}†	Shift In to Input Ready LOW	1			40	ns
t_{IRH}†	Shift In to Input Ready HIGH	1			40	ns
f_{OUT}†	Shift Out rate	5	15			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			45	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			50	ns
t_{ODH}	Output Data Hold (previous word)	5	10			ns
t_{ODS}	Output Data Shift (next word)	5			45	ns
t_{PT}	Data throughput or "fall through"	4, 8			1.6	μs
t_{MRORL}	Master Reset to OR LOW	10			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			60	ns
t_{IPH}*	Input Ready pulse HIGH	4	23			ns
t_{OPH}*	Output Ready pulse HIGH	8	23			ns

† See AC test and High Speed application note.
* This parameter applies to FIFOs communicating with each other in a cascaded mode.

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150°C

Operating Conditions C67401/2

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	23			ns
t_{SIL}	Shift in LOW time	1	35			ns
t_{IDS}	Input data setup	1	0			ns
t_{IDH}	Input data hold time	1	45			ns
t_{SOH}†	Shift Out HIGH time	5	23			ns
t_{SOL}	Shift Out LOW time	5	35			ns
t_{MRW}	Master Reset pulse	10	35			ns
t_{MRS}	Master Reset to SI	10	35			ns

Switching Characteristics C67401/2 Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	10			MHz
t_{IRL}†	Shift In to Input Ready LOW	1			45	ns
t_{IRH}†	Shift In to Input Ready HIGH	1			45	ns
f_{OUT}	Shift Out rate	5	10			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			55	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			60	ns
t_{ODH}	Output Data Hold (previous word)	5	10			ns
t_{ODS}	Output Data Shift (next word)	5			55	ns
t_{PT}	Data throughput or "fall through"	4, 8			3	μs
t_{MRORL}	Master Reset to OR LOW	10			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			60	ns
t_{IPH}*	Input Ready pulse HIGH	4	23			ns
t_{OPH}*	Output Ready pulse HIGH	8	23			ns

† See AC test and High Speed application note.
* This parameter applies to FIFOs communicating with each other in a cascaded mode.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8†	V
V_{IH}	High-level input voltage				2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL1}	Low-level input current	D_0-D_n, $\overline{MR}$	V_{CC} = MAX	V_I = 0.45V			−0.8	mA
I_{IL2}		SI, SO					−1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		VCC = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = −0.9mA	2.4			V
I_{OS}	Output short-circuit current *		V_{CC} = MAX	V_0 = 0V	−20		−90	mA
I_{CC}	Supply current		V_{CC} = MAX, All inputs low, All outputs open.	C67401			160	mA
				C67402			180	
				C67401A			170	
				C67702A			190	
				C67401B			180	
				C67402B			200	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
†There are absolute voltage with respect to device GND (Pin 8 or 9) and includes all overshoots due to test equipment

2

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty). Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitance and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift In-Input Ready combination, as well as the Shift Out-Output Ready combination, timing measurements may be misleading, i.e. rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency or FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going High. This same type of problem is also related to t_{IRH}, t_{ORL} and t_{ORH} as related to Shift-Out.

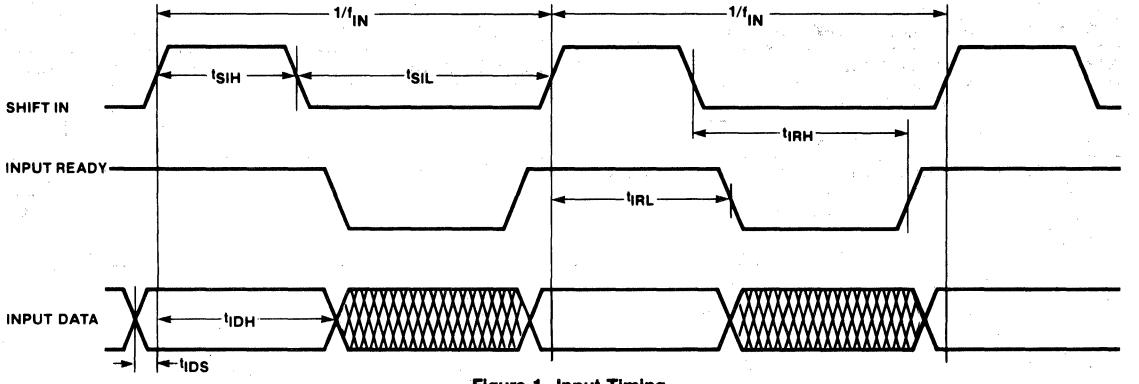


Figure 1. Input Timing

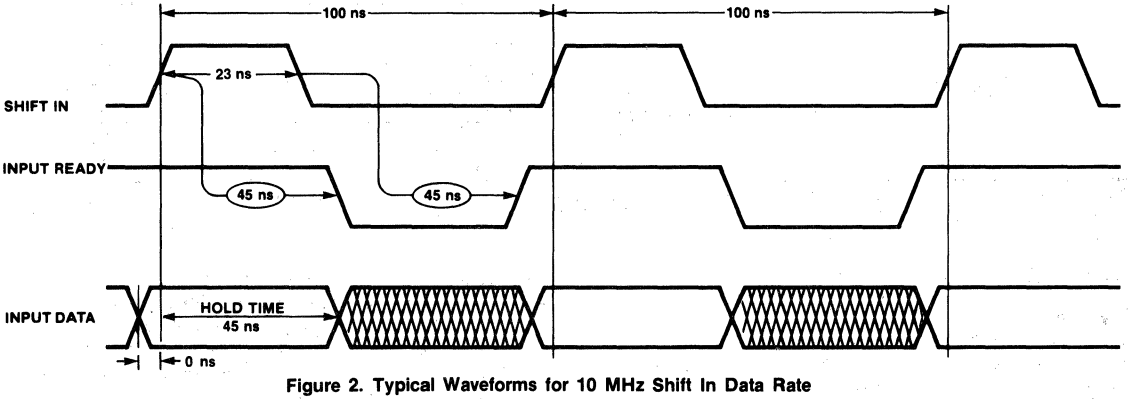


Figure 2. Typical Waveforms for 10 MHz Shift In Data Rate

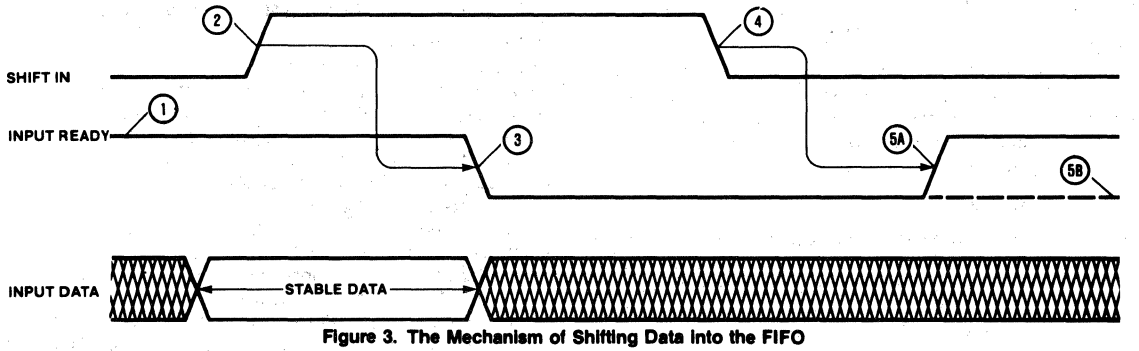


Figure 3. The Mechanism of Shifting Data into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied.

(2) Input Data is loaded into the first word.

(3) Input Ready goes LOW indicating the first word is full.

(4) The Data from the first word is released for "fall-through" to second word.

(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 4).

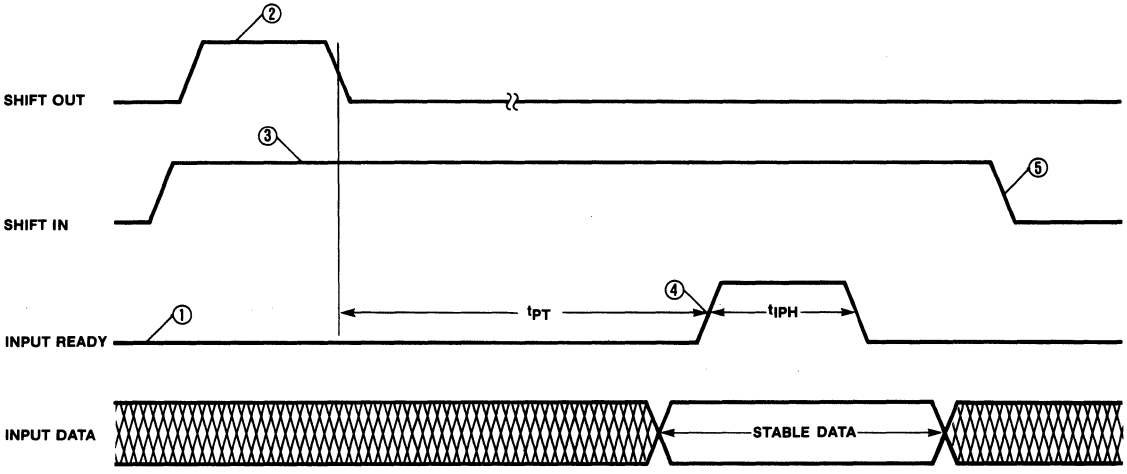
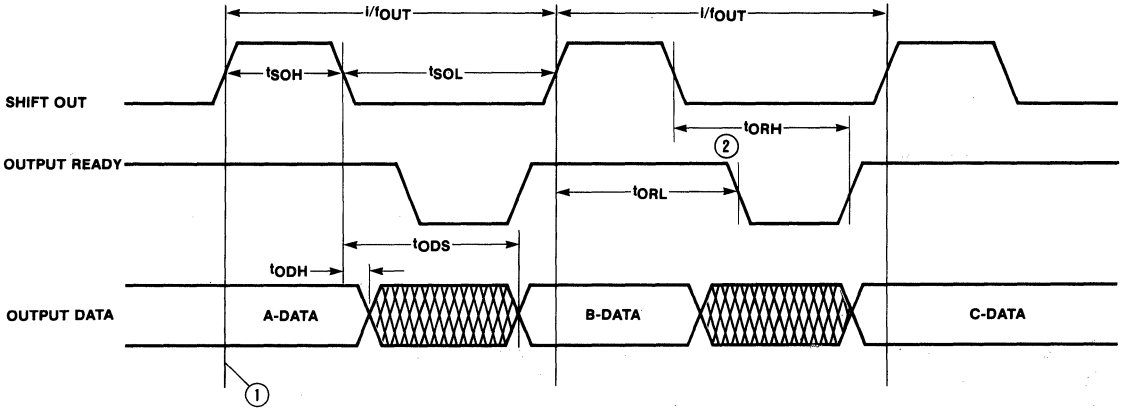


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

(1) FIFO is initially full.
(2) Shift Out pulse is applied. An empty location starts "bubbling" to the front.
(3) Shift In is held HIGH.
(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
(5) The Data from the first word is released for "fall through" to second word.



(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.
(2) Data is shifted out when Shift Out makes a HIGH to LOW transition.

Figure 5. Output Timing

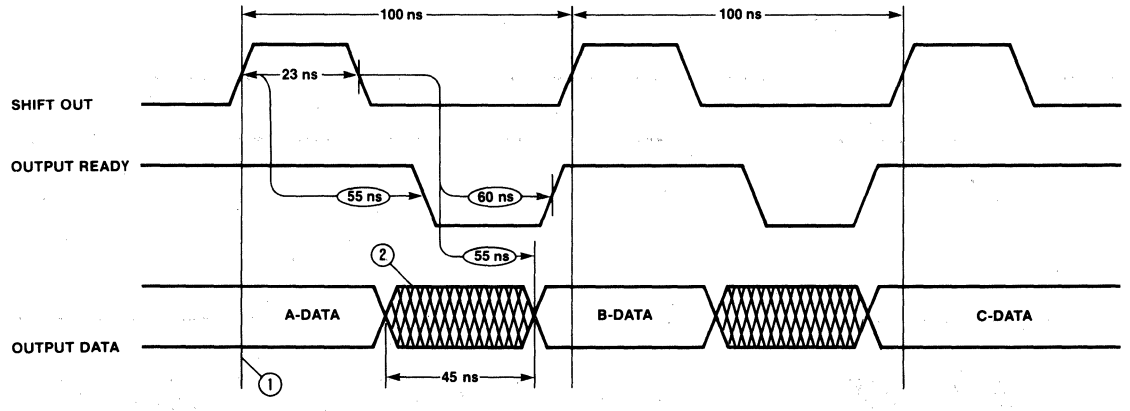


Figure 6. Typical Waveforms for 10 MHz Shift Out Data Rate

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data in the crosshatched region may be A or B Data.

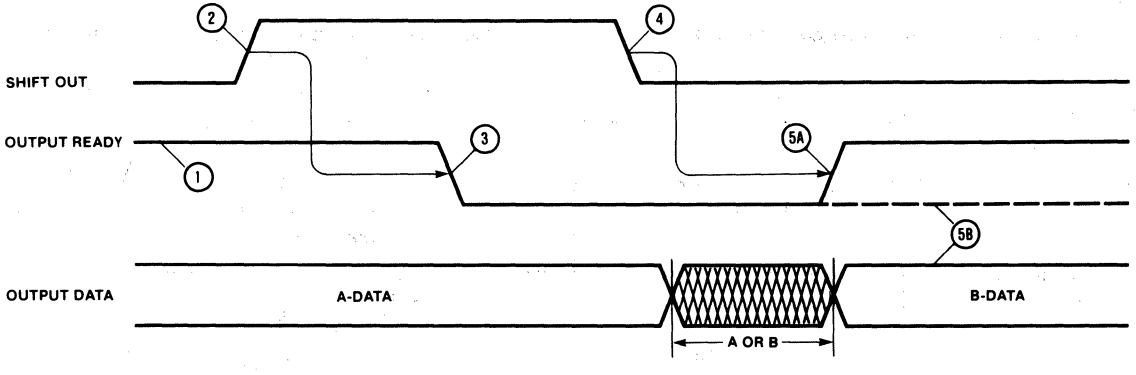


Figure 7. The Mechanism of Shifting Data Out of the FIFO.

(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

(2) Shift Out goes HIGH causing the next step.

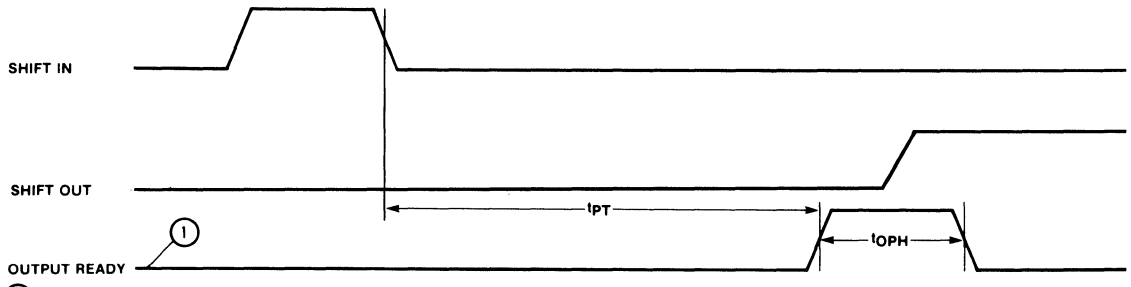
(3) Output Ready goes LOW.

(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

NOTE: Shift Out pulses applied when Output Ready is LOW will be ignored.



(1) FIFO initially empty.

Figure 8. t_{PT} and t_{OPH} Specification

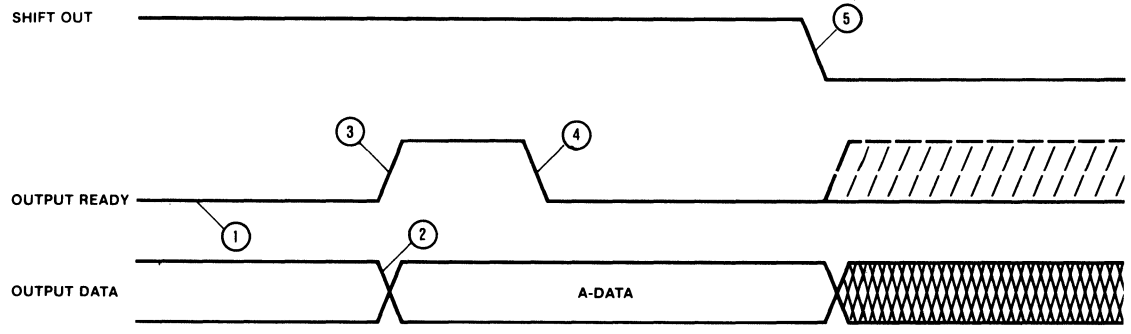


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

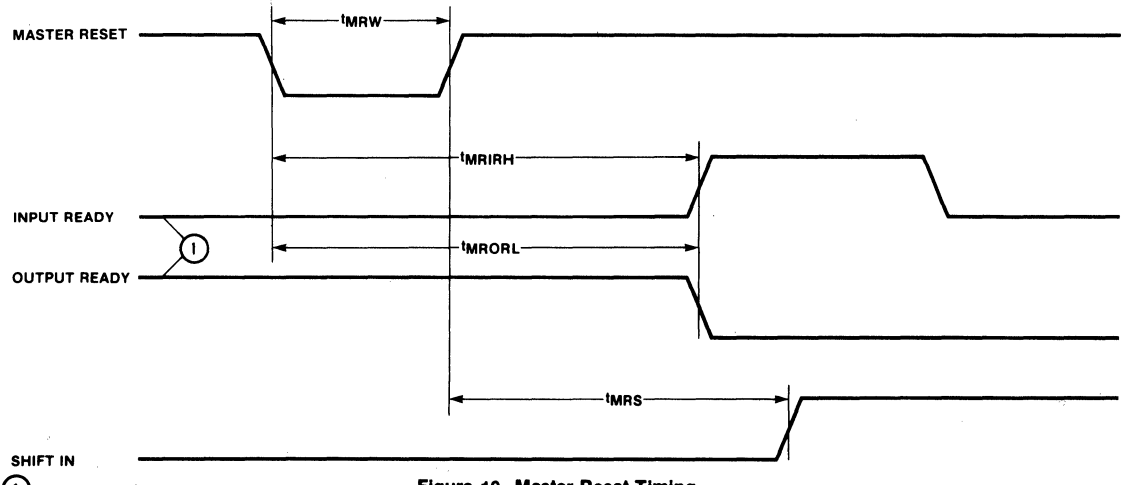
(1) Word 63 is empty.

(2) New data (A) arrives at the outputs (word 63).

(3) Output Ready goes HIGH indicating the arrival of the new data.

(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.

(5) As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.



(1) FIFO initially full.

Figure 10. Master Reset Timing

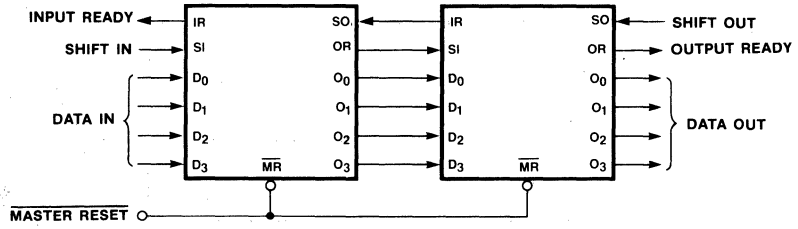


Figure 11. Cascading FIFOs to Form 128x4 FIFO with C5/C67401A/1

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the FIFOs themselves.

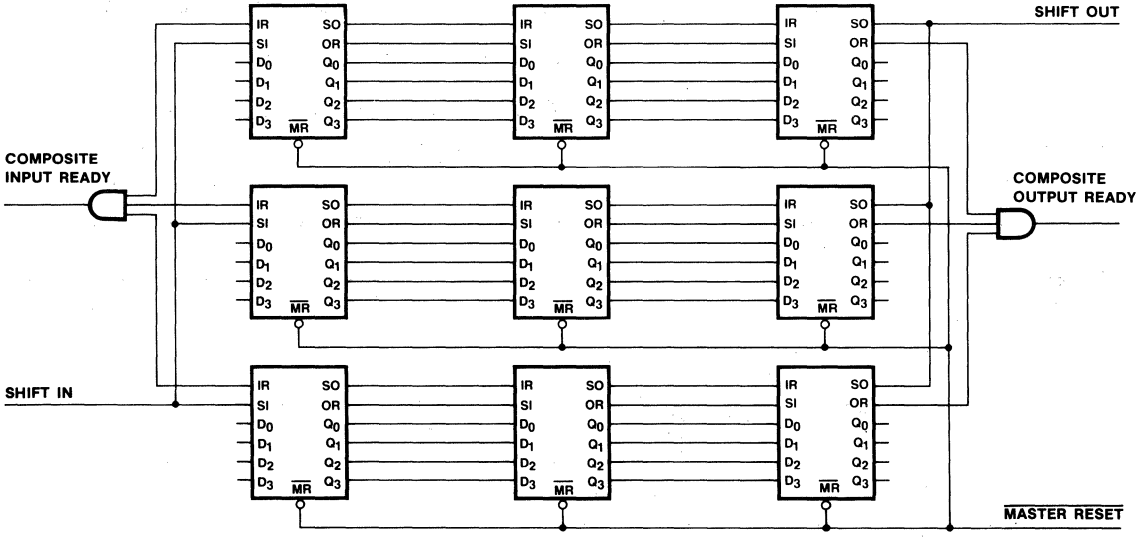
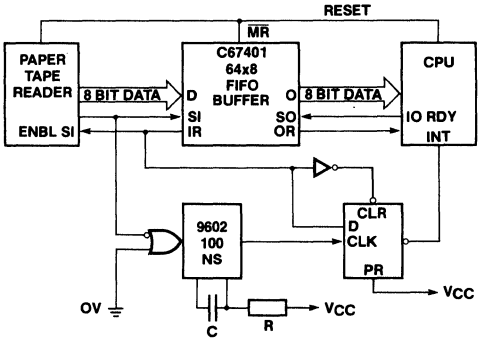


Figure 12. 192x12 FIFO with C5/C67401/1A/1B

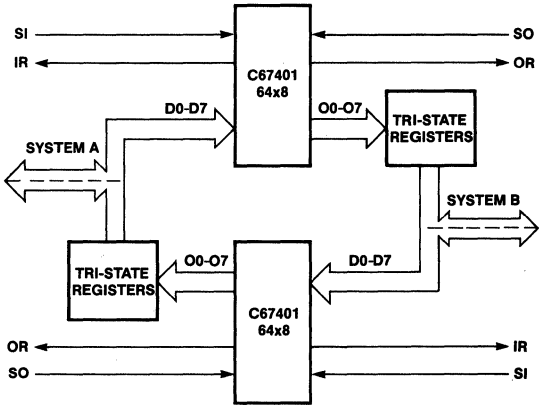
FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall-through times of the FIFOs.

Applications



NOTE: The output of monostable holds off the "Buffer full" interrupt for 100ns. If 100ns after shift in, there has not been an input Ready to reset the "D Flip-flop" an interrupt is issued, as the FIFO is full. The CPU then empties the FIFO before the next character is output from the tape drive.

Figure 13. Slow Steady Rate to Fast "Blocked" Rate



NOTE: Both depth and width expansion can be used in this mode. The IR and OR signals are the anded versions of the individual IR and OR signals.

Figure 14. Bidirectional FIFO Application

Low Power First-In First-Out (FIFO) 64x4 Memory
67L401

Features/Benefits

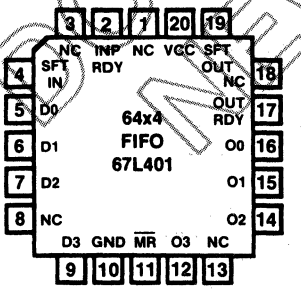
- **Guaranteed 5 MHz shift-out/shift-in rates**
- **Low Power Consumption**
- **TTL inputs and outputs**
- **Readily expandable in the bit dimensions**
- **Structured pinouts. Output pins directly opposite corresponding input pins**
- **Asynchronous operation**
- **Pin compatible with Fairchild's F3341 MOS FIFO and much faster**

Description

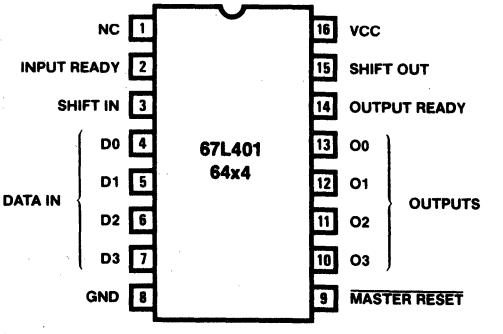
The 67L401 is a low-power First-In First-Out (FIFO) memory device with TTL speed. This device is organized in a 64x4-bit structure and easily expandable to any width. A 5 MHz data rate with fast "fall through" time allows usage in tape and disc controllers, printers and communications buffer applications. This data rate is much faster than a comparable MOS device. The FIFO is a register-based device. Data entered at the inputs "falls through" to the empty space closest to the output. Data is shifted out in the same sequence it is shifted in. Also, the width can be increased by putting the Input Ready signals through an AND gate to give a composite Input Ready. Similarly, the Output Ready signals should be gated to form a composite Output Ready.

Generally, FIFOs are used in digital systems performing data transfers when source and receiver are not operating at the same data rate. FIFOs are also used as data buffers where the source and receiver are not operating at the same time. The 67L401 is particularly useful where low-power consumption is critical.

Pin Configurations



Plastic Chip Carrier

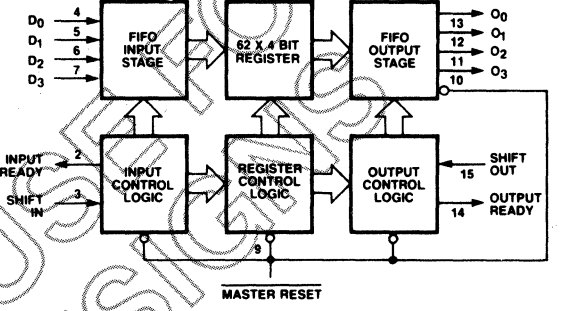


Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
67L401	N, NL	COM	5 MHz 64x4 FIFO
67L401	J, NL	COM	5 MHz 64x4 FIFO

Block Diagram

67L401 64x4



Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	55			ns
t_{SIL}	Shift in LOW time	1	55			ns
t_{IDS}	Input data setup	1	10			ns
t_{IDH}	Input data hold time	1	80			ns
t_{SOH}†	Shift Out HIGH time	5	55			ns
t_{SOL}	Shift Out LOW time	5	55			ns
t_{MRW}	Master Reset pulse	10	40			ns
t_{MRS}	Master Reset to SI	10	35			ns

Switching Characteristics Over Operating Conditions

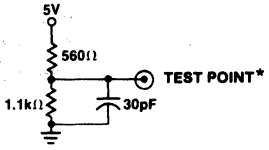
SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	5			MHz
t_{IRL}†	Shift in to Input Ready LOW	1			75	ns
t_{IRH}†	Shift in to Input Ready HIGH	1			75	ns
f_{OUT}	Shift Out rate	5	5			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			75	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			80	ns
t_{ODH}	Output Data Hold (previous word)	5	8			ns
t_{ODS}	Output Data Shift (next word)	5			70	ns
t_{PT}	Data throughput or "fall-through"	4, 8			4	μs
t_{MRORL}	Master Reset to OR LOW	10			85	ns
t_{MRIRH}	Master Reset to IR HIGH	10			85	ns
t_{IPH}*	Input Ready pulse HIGH	4	20			ns
t_{OPH}*	Output Ready pulse HIGH	8	20			ns

† See AC test and application note.

* This parameter applies to FIFOs communicating with each other in a cascade mode.

Test Load

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



Input Pulse 0 to 3 V
Input Rise and Fall Time (10% - 90%)
5 ns minimum
Measurements made at 1.5 V

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18mA			-1.5	V
I_{IL1}	Low-level	D_0-D_3 MR	V_{CC} = MAX	V_I = 0.45V			-0.8	mA
I_{IL2}	input current	SI, SO					-1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = -0.9mA	2.4			V
I_{OS}	Output short-circuit current*		V_{CC} = MAX	V_O = 0V	-20		-90	mA
I_{CC}	Supply Current		V_{CC} = MAX	Inputs Low, Outputs Open		95	110	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† This is an absolute voltage with respect to device GND (Pin 8 or 9) and includes all overshoots due to test equipment.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 11) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_x inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_x outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_x remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and Application Note

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing. Though the external data rate is 5 MHz internally the device is several times as fast. Device grounding and decoupling is crucial to correct operation, as the FIFO will respond to very small glitches caused by long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in timing set up and measurement of parameters. For example, since an AND gate function is associated with both the Shift In-Input Ready Combination, as well as the Shift Out-Output Ready Combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency, or the FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going High.

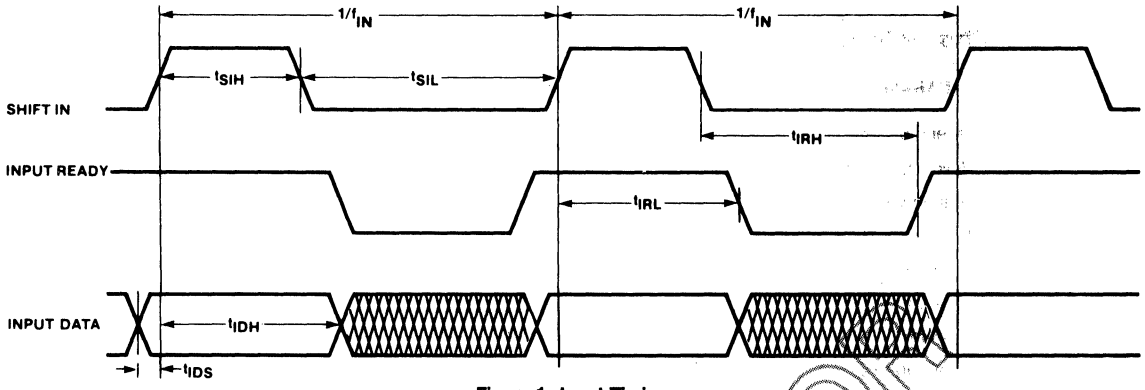


Figure 1. Input Timing

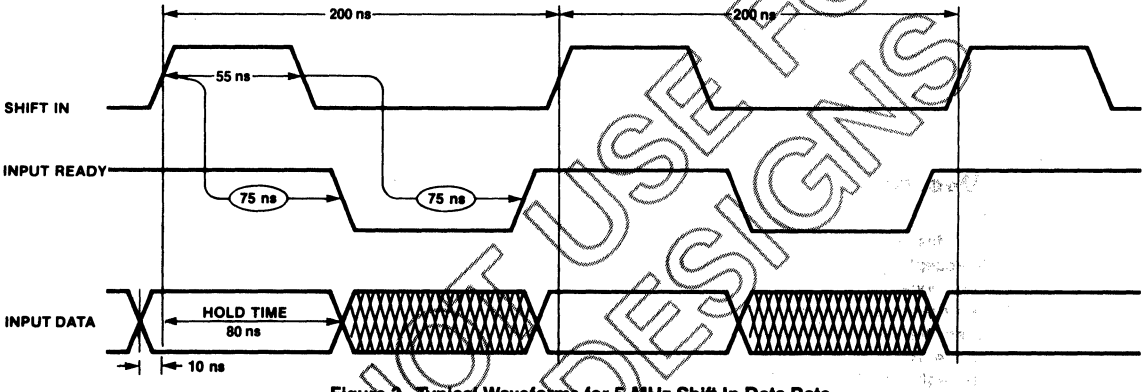


Figure 2. Typical Waveforms for 5-MHz Shift In Data Rate

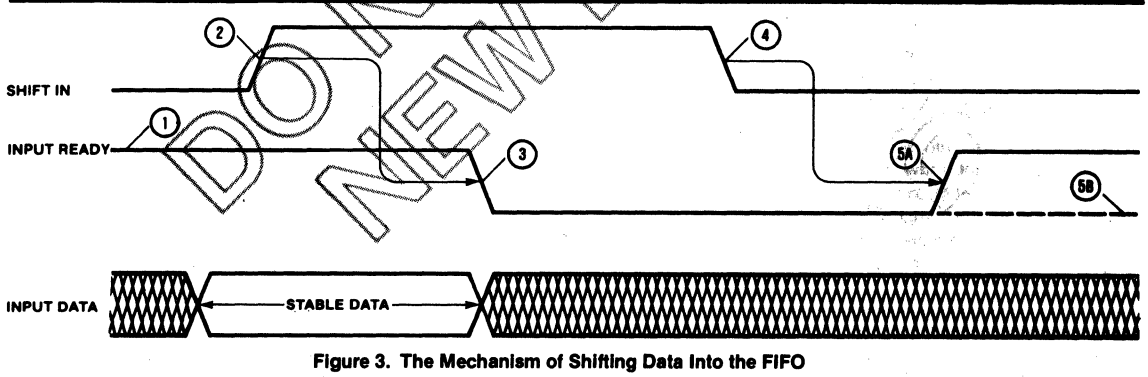


Figure 3. The Mechanism of Shifting Data Into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied.

(2) Input Data is loaded into the first word.

(3) Input Ready goes LOW indicating the first word is full.

(4) The Data from the first word is released for "fall-through" to second word.

(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

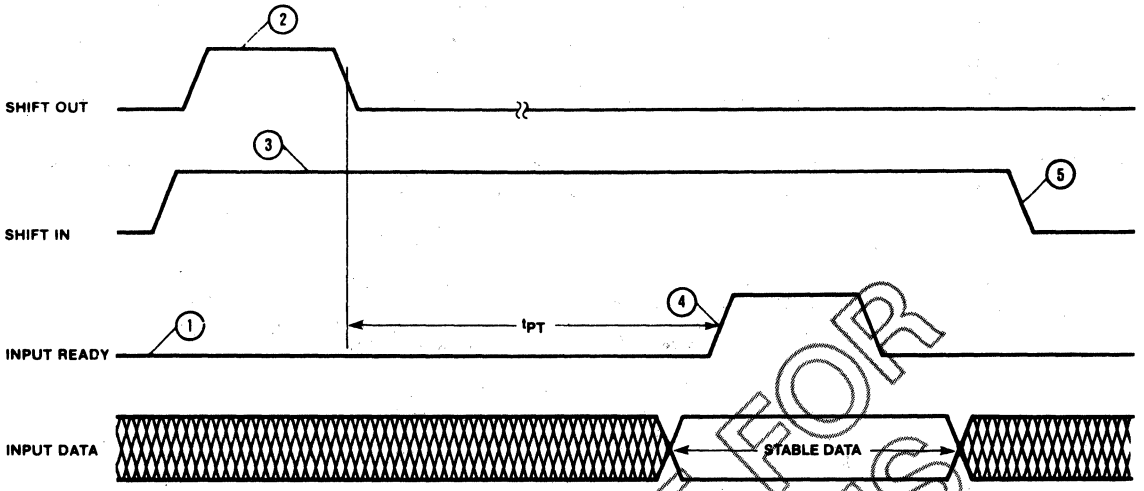
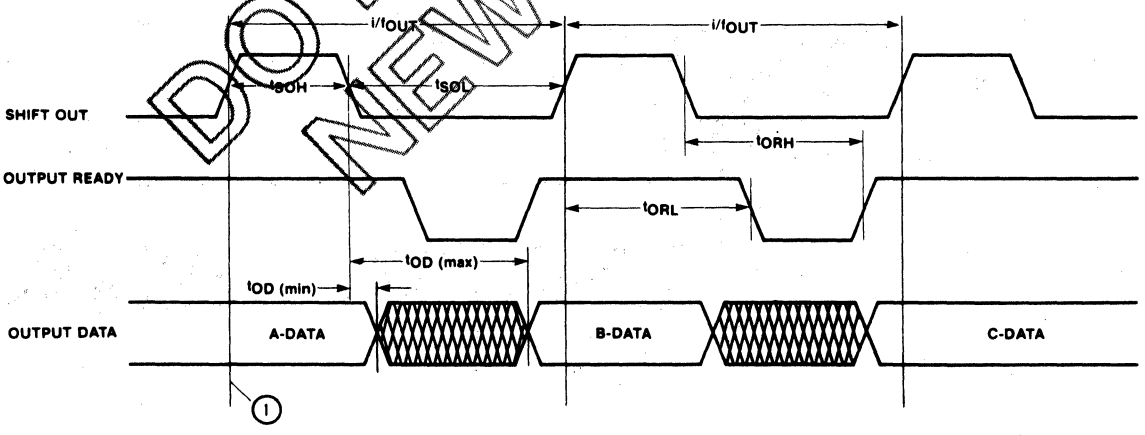


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

(1) FIFO is initially full.
(2) Shift Out pulse is applied. An empty location start "bubbling" to the front.
(3) Shift In is held HIGH.
(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
(5) The Data from the first word is released for "fall through" to second word.



(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively

Figure 5. Output Timing

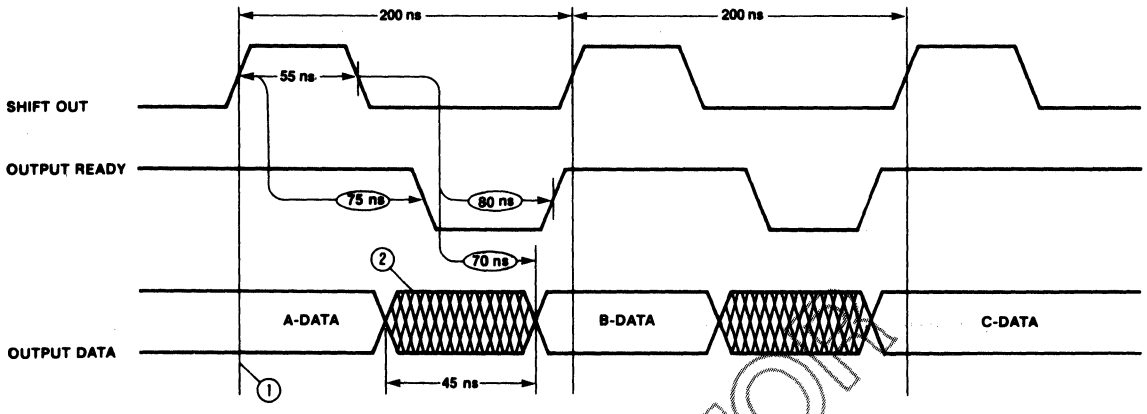


Figure 6. Typical Waveform for 5 MHz Shift Out Data Rate

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data in the crosshatched region may be A or B Data.

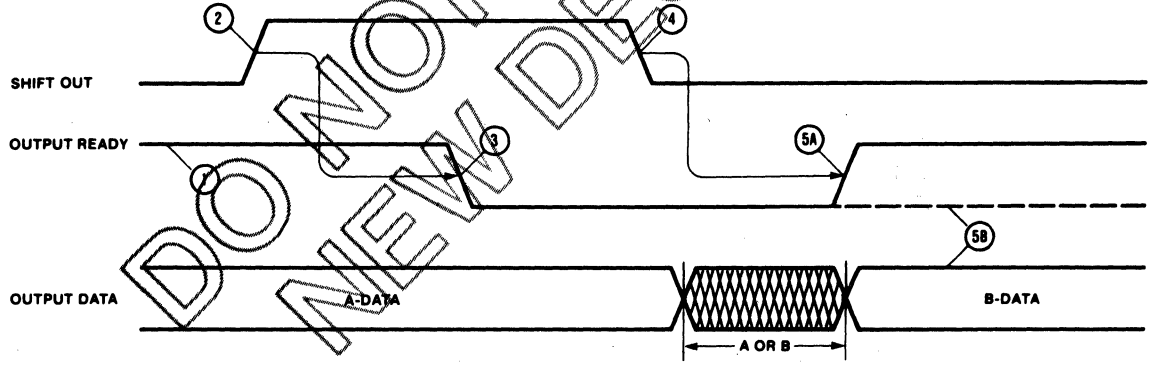


Figure 7. The Mechanism of Shifting Data Out of the FIFO

(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

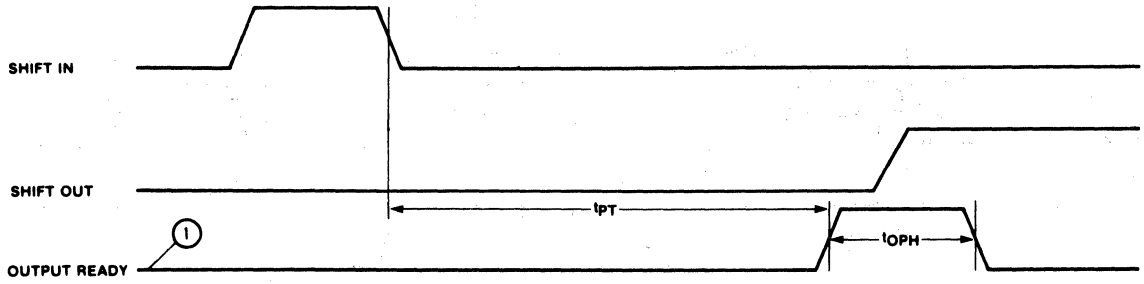
(2) Shift Out goes HIGH causing the next step.

(3) Output Ready goes LOW.

(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.



1. FIFO initially empty.

Figure 8. t_{PT} and t_{OPH} Specification

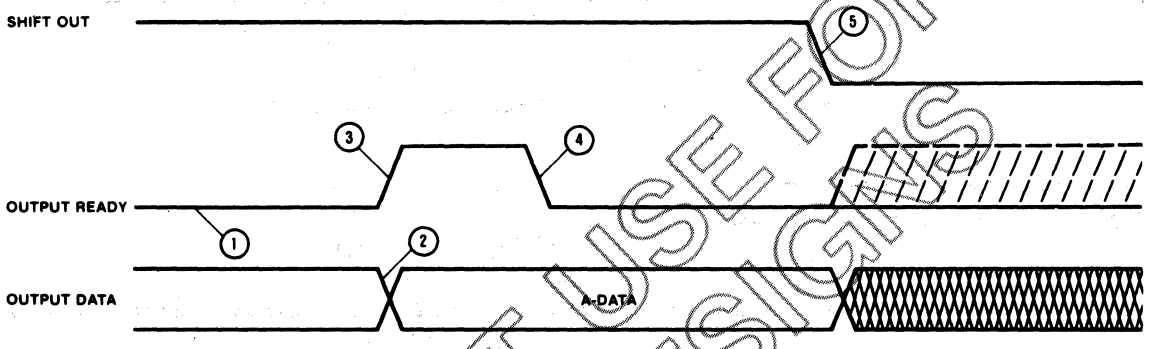
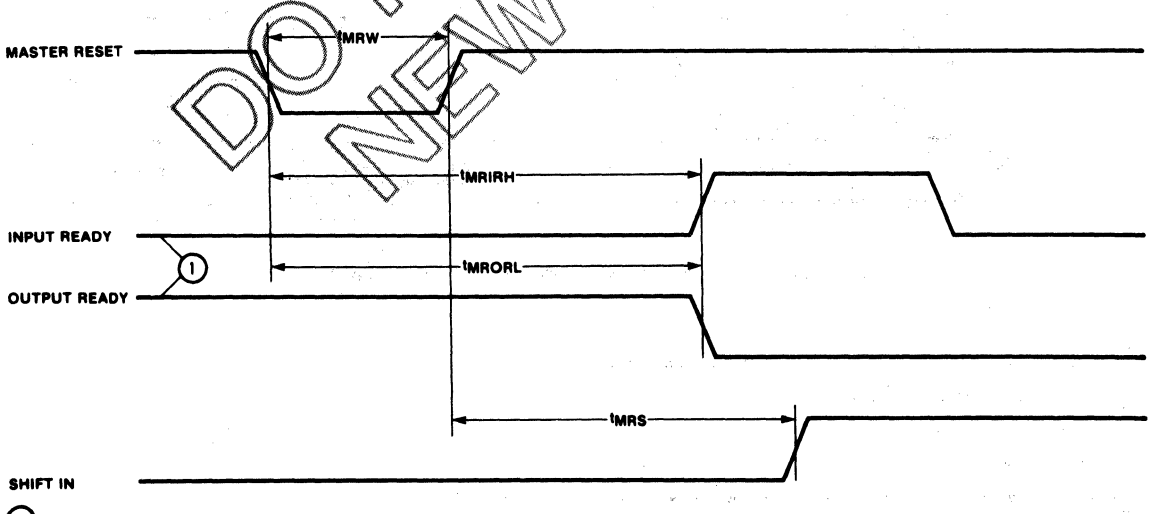


Figure 9. Data is ,Shifted Out Whenever Shift Out and Output Ready are Both HIGH

1. Word 63 is empty.
2. New data (A) arrives at the outputs (word 63).
3. Output Ready goes HIGH indicating the arrival of the new data.
4. Since Shift Out is held HIGH, Output Ready goes immediately LOW.
5. As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.



1. FIFO initially full.

Figure 10. Master Reset Timing

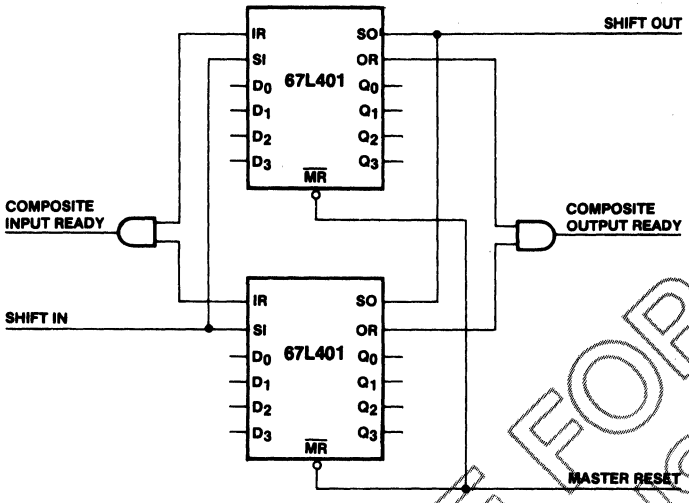


Figure 12. 64x8 FIFO With Two 67L401's

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall through times of the FIFOs.

Applications

FIFOs are typically used as temporary data buffers between mismatching data rates. Such an application is shown in Figure 13.

The 67L401 can also be used in a bidirectional operation as shown in Figure 14.

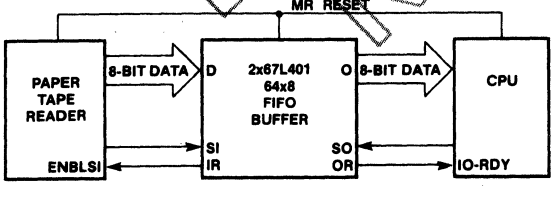
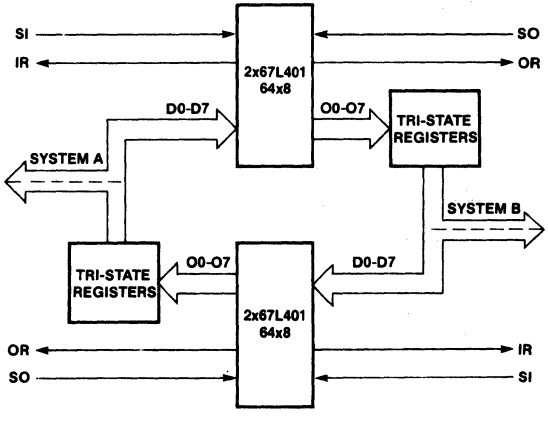


Figure 13. FIFO As Data Buffer Between Slow Steady Rate and Fast 'Burst' Rate



NOTE: Both depth and width expansion can be used in this mode.

Figure 14. Bidirectional FIFO Application

First-In First-Out (FIFO) 64x4 64x5 Memory 15 MHz (Cascadable)

C67L401D C67L402D

Features/Benefits

- High-speed 15-MHz shift-in/shift-out rates
- Low power consumption
- Choice of 4-bit or 5-bit data width
- TTL inputs and outputs
- Readily expandable in word width and depth
- Structured pinouts. Output pins directly opposite corresponding input pins
- High-drive capability
- Asynchronous operation

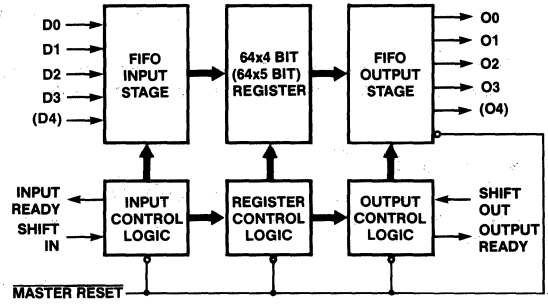
Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
C67L401D	N, J	Com	15 MHz 64x4 FIFO
C67L402D	N, J	Com	15 MHz 64x5 FIFO

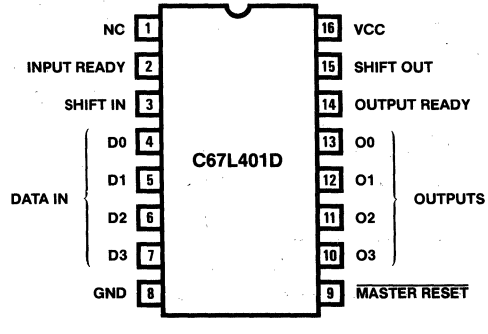
Description

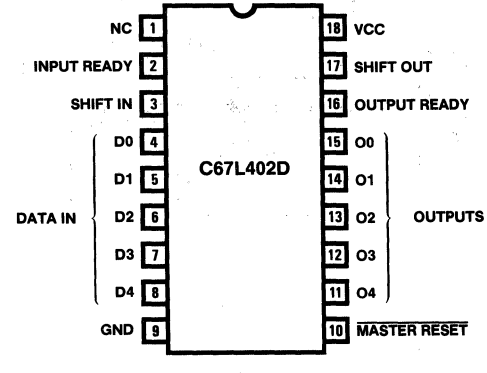
The C67L401D/2D are "fall-through" high-speed First-In First-Out (FIFO) memories organized 64 words by 4 bits and 64 words by 5 bits respectively. The FIFO is expandable in word width and depth. The FIFO is attractive for many applications such as disk controllers, communication buffers, rate buffers, etc. They feature high-drive (I_{OL} = 24 mA) outputs.

C67L401D
(C67L402D)



Pin Configurations





Publication #	Rev.	Amendment
10677	A	/0

Issue Date: May 1988

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		70	°C
f_{IN}	Shift in rate	1			15	MHz
t_{SIH}	Shift in High time	1	24			ns
t_{SIL}	Shift in Low time		15			
t_{IDS}	Input data setup to SI (Shift In)	1	0			ns
t_{IDH}	Input data hold from SI (Shift In)	1	26			ns
t_{RIDS}	Input data setup to IR (Input Ready)	4	0			ns
t_{RIDH}	Input data hold from IR (Input Ready)	4	26			ns
f_{OUT}	Shift out rate	5			15	MHz
t_{SOH}	Shift out High time	5	17			ns
t_{SOL}	Shift out Low time		15			
t_{MRW}	Master Reset pulse**	10	35			ns
t_{MRS}	Master Reset to SI*	10	35			ns

* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.

** See AC test and high-speed application note.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITION		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage						0.8**	V
V_{IH}	High-level input voltage				2**			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18 mA			-1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.45 V			-250	μA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4 V			50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level Output voltage	Output, O	V_{CC} = MIN	I_{OL} = 24 mA			0.5	V
		IR, OR	V_{CC} = MIN	I_{OL} = 8 mA				
V_{OH}	High-level Output voltage	Output, O	V_{CC} = MIN	I_{OH} = -3.0 mA	2.4			V
		IR, OR	V_{CC} = MIN	I_{OH} = -0.9 mA				
I_{OS}	Output short-circuit current*		V_{CC} = MAX	V_O = 0V	-20		-90	mA
I_{CC}	Supply current		V_{CC} = MAX All inputs low. All outputs open.	L401D/2D			100	mA

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
** These are absolute voltages with respect to GND (Pin 8 or 9) and include all overshoots due to test equipment

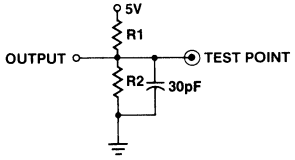
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
t_{IRL}†	Shift In ↑ to Input Ready LOW	1			40	ns
t_{IRH}†	Shift In ↓ to Input Ready HIGH				26	ns
t_{ORL}†	Shift Out ↑ to Output Ready LOW	5			45	ns
t_{ORH}†	Shift Out ↓ to Output Ready HIGH				50	ns
t_{ODH}†	Output Data Hold (previous word)		12			ns
t_{ODS}	Output Data Shift (next word)				40	ns
t_{PT}	Data throughput	4,8			1600	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	10			60	ns
t_{MRIRH}*	Master Reset ↑ to Input Ready HIGH				30	ns
t_{MRIRL}*	Master Reset ↓ to Input Ready LOW				50	ns
t_{MRO}	Master Reset ↓ to Outputs LOW				60	ns
t_{IPH}	Input ready pulse HIGH	4	17			ns
t_{OPH}	Output ready pulse HIGH	8	24			ns
t_{ORD}	Output ready ↑ to Data Valid	5			-3	ns

* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.

† See AC test and high-speed application note.

Standard Test Load



I_{OL}	R1	R2
24 mA	200 Ω	300 Ω
8 mA	600 Ω	1200 Ω

Input Pulse Amplitude = 3 V
Input Rise and Fall Time (10%–90%) = 2.5 ns
Measurements made at 1.5 V

2

Functional Description

Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW. The FIFO should always be cleared by using master reset.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided the upstream stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between VCC and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input-Ready combination, as well as the Shift-Out-Output-Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to shift-in going HIGH. This same type of situation occurs with T_{ORL} and T_{ORH} as related to Shift-Out. For high-speed applications, proper grounding technique is essential.

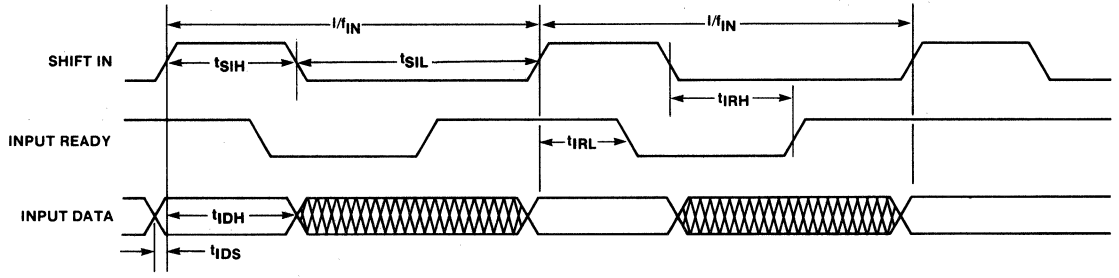


Figure 1. Input Timing

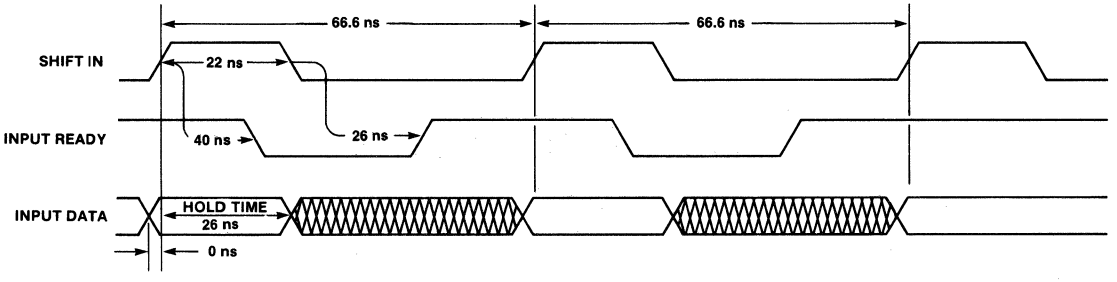


Figure 2. Typical Waveforms for 15-MHz Shift-In Rate

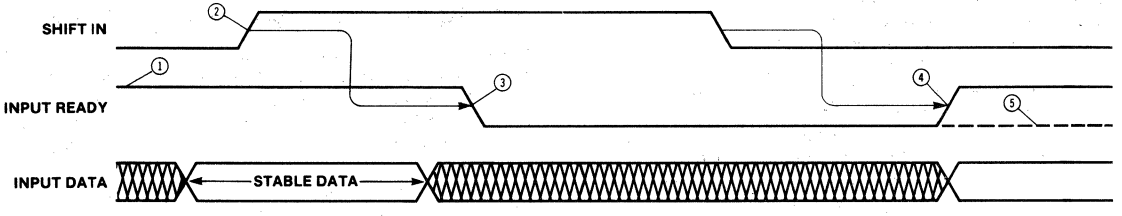


Figure 3. The Mechanism of Shifting Data into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
(2) Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.
(3) Input Ready goes LOW indicating the first word is full.
(4) Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.
(5) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.
NOTE: Shift-In pulses applied while Input Ready is LOW will be ignored

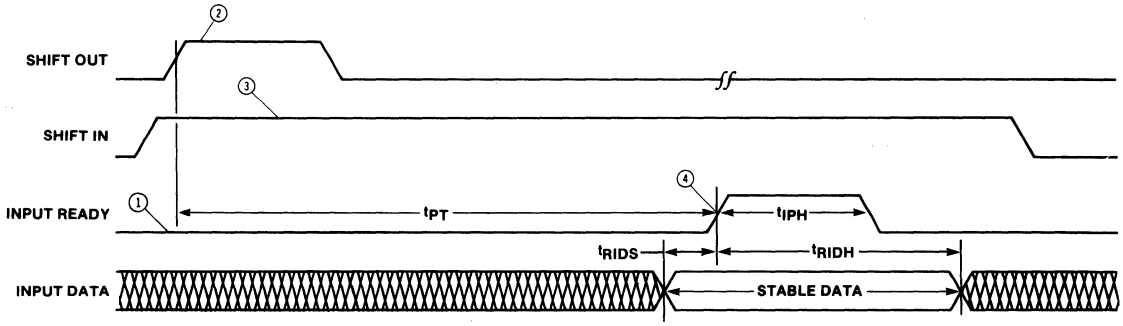


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

① FIFO is initially full.

② Shift Out pulse is applied. An empty location starts "bubbling" to the front.

③ Shift In is held HIGH

④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

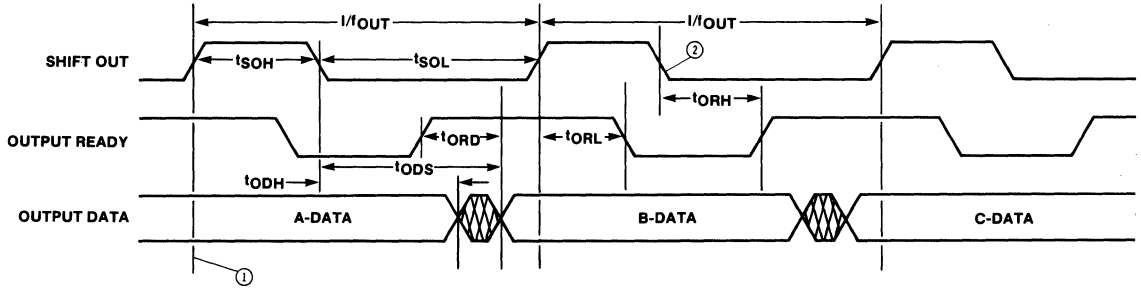


Figure 5. Output Timing

① The diagram assumes that at this time, words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.

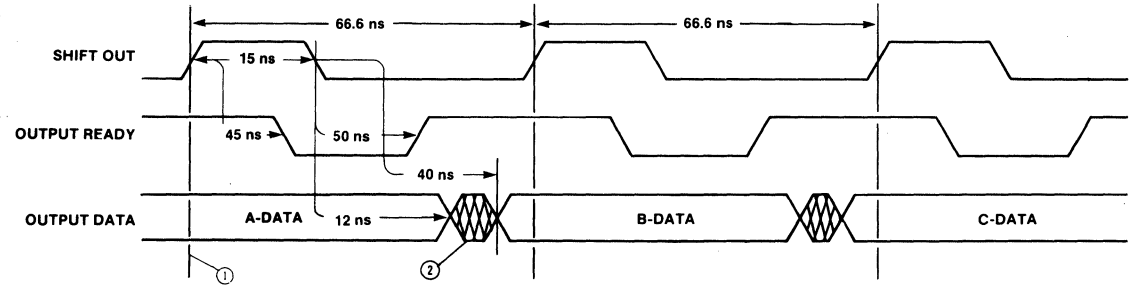


Figure 6. Waveforms for 15 MHz Shift-Out Data Rate

① The diagram assumes that at this time words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Data in the first crosshatched region may be A or B Data.

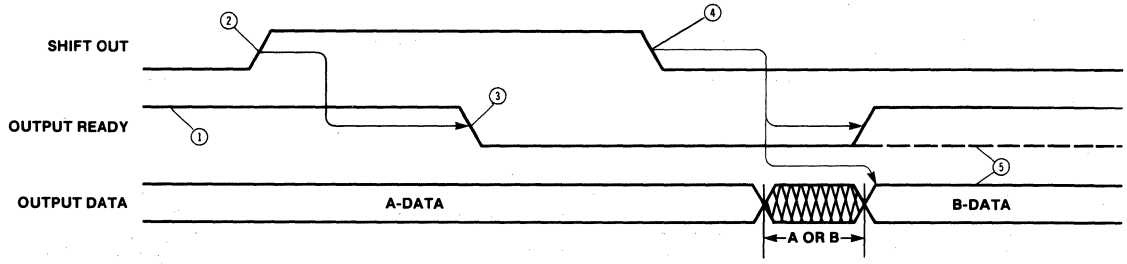


Figure 7. The Mechanism of Shifting Data Out of the FIFO

(1) Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.

(2) Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.

(3) Output Ready goes LOW.

(4) Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.

(5) If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

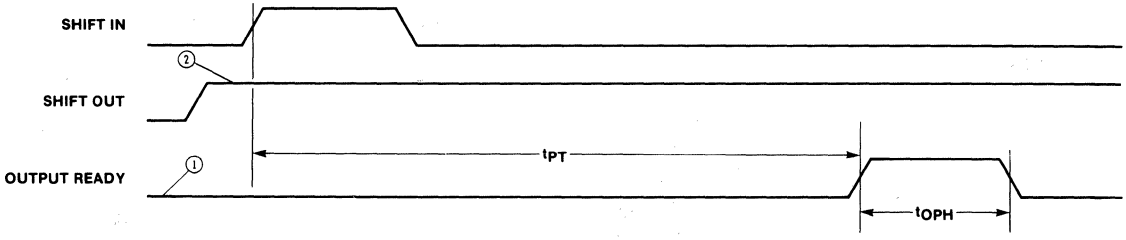


Figure 8. t_{PT} and t_{OPH} Specification

(1) FIFO initially empty.

(2) Shift Out held HIGH

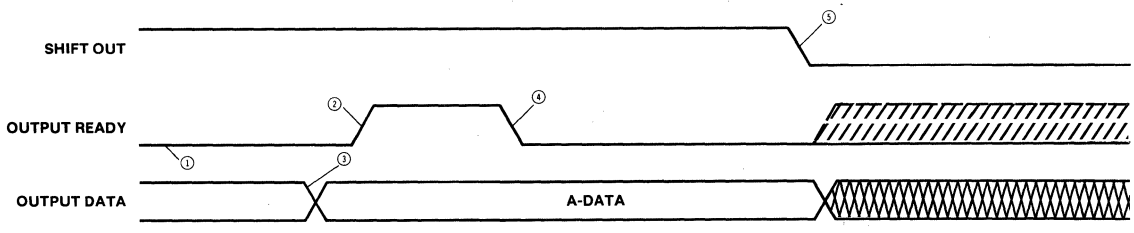


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

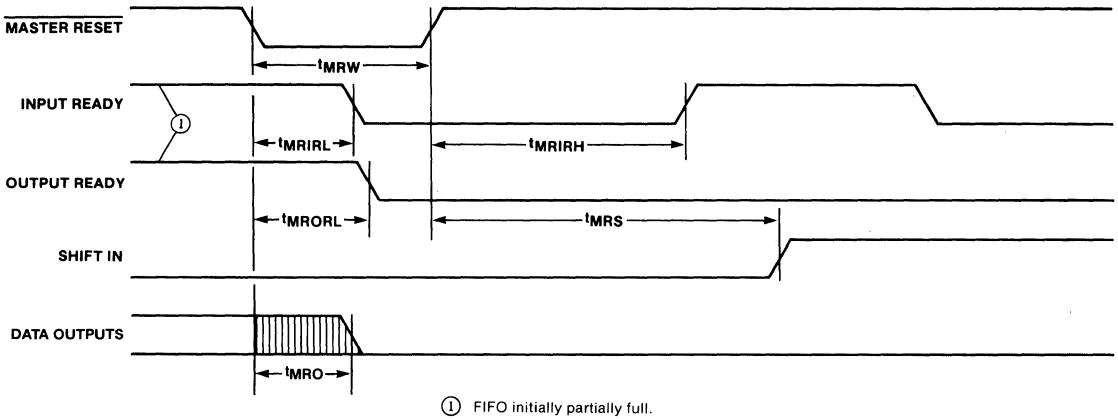
(1) Word 63 is empty.

(2) Output Ready goes HIGH indicating arrival of the new data.

(3) New data (A) arrives at the outputs (word 63).

(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.

(5) As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.



① FIFO initially partially full.

Figure 10. Master Reset Timing

First-In First-Out (FIFO) 64x4 Memory 15 MHz (Cascadable) With Three-State Outputs

C67L4013D

Features/Benefits

- **High-speed 15-MHz shift-in/shift-out rates**
- **Low power consumption**
- **TTL inputs and outputs**
- **Readily expandable in word width and depth**
- **Structured pinouts. Output pins directly opposite corresponding input pins**
- **High-drive capability**
- **Asynchronous operation**
- **Output Enable feature**

Ordering Information

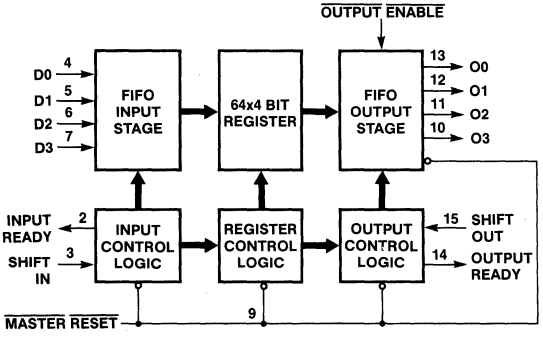
PART NUMBER	PKG	TEMP	O/P	DESCRIPTION
C67L4013D	N, J	Com	3-state	15 MHz FIFO

Description

The C67L4013D is a "fall-through" high-speed First-In First-Out (FIFO) memory organized 64 words by 4 bits. The FIFO is expandable in word width and depth. The FIFO is attractive for many applications such as disk controllers, communication buffers, rate buffers, etc. The C67L4013D has three-state, high-drive (I_{OL} = 24 mA) outputs.

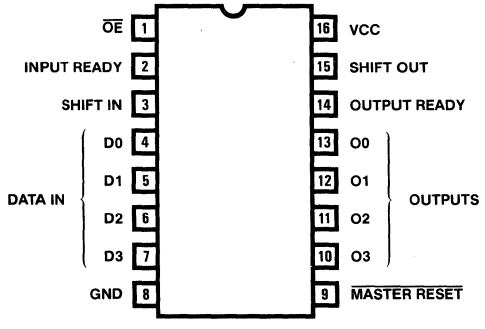
Block Diagram

C67L4013D



Pin Configuration

C67L4013D



Publication #	Rev.	Amendment
10682	A	/0

Issue Date: May 1988

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		70	°C
f_{IN}	Shift in rate	1			15	MHz
t_{SIH}	Shift in High time	1	24			ns
t_{SIL}	Shift in Low time	1	15			ns
t_{IDS}	Input data setup to SI (Shift In)	1	0			ns
t_{IDH}	Input data hold time to SI (Shift In)	1	26			ns
t_{RIDS}	Input data setup to IR (Input Ready)	4	0			ns
t_{RIDH}	Input data hold time to IR (Input Ready)	4	26			ns
f_{OUT}	Shift out rate	5			15	MHz
t_{SOH}	Shift out High time	5	17			ns
t_{SOL}	Shift out Low time	5	15			ns
t_{MRW}	Master Reset pulse**	10	35			ns
t_{MRS}	Master Reset to SI*	10	35			ns

* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.
** See AC test and high-speed application note.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITION		COMMERCIAL MIN	COMMERCIAL MAX	UNIT
V_{IL}	Low-level input voltage					0.8**	V
V_{IH}	High-level input voltage				2**		V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18 mA		-1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.45 V		-250	μA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4 V		50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5 V		1	mA
V_{OL}	Low-level Output voltage	Output, O	V_{CC} = MIN	I_{OL} = 24 mA		0.5	V
		IR, OR		I_{OL} = 8 mA			
V_{OH}	High-level Output voltage	Output, O	V_{CC} = MIN	I_{OH} = -3.0 mA	2.4		V
		IR, OR		I_{OH} = -0.9 mA			
I_{OS}	Output short-circuit current*		V_{CC} = MAX	V_O = 0V	-20	-90	mA
I_{OZL}	Off-state output current		V_{CC} = MAX	V_O = 0.4 V		-50	μA
I_{OZH}				V_O = 2.4 V		+50	
I_{CC}	Supply current		V_{CC} = MAX All inputs low. All outputs open.			110	mA

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
** These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL MAX	UNIT
t_{IRL}†	Shift In ↑ to Input Ready LOW	1		40	ns
t_{IRH}†	Shift In ↓ to Input Ready HIGH			26	ns
t_{ORL}†	Shift Out ↑ to Output Ready LOW	5		45	ns
t_{ORH}†	Shift Out ↓ to Output Ready HIGH			50	ns
t_{ODH}†	Output Data Hold (previous word)		12		ns
t_{ODS}	Output Data Shift (next word)			40	ns
t_{PT}	Data throughput	4,8		1600	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	10		60	ns
t_{MRIRH}	Master Reset ↑ to Input Ready HIGH*			30	ns
t_{MRIRL}	Master Reset ↓ to Input Ready LOW*			50	ns
t_{MRO}	Master Reset ↓ to Outputs LOW			60	ns
t_{IPH}	Input ready pulse HIGH	4	17		ns
t_{OPH}	Output ready pulse HIGH	8	24		ns
t_{ORD}	Output ready ↑ to Data Valid	5		-3	ns
t_{PHZ}	Output Disable Delay, C67L4013D	A		30	ns
t_{PLZ}				30	
t_{PZL}	Output Enable Delay, C67L4013D			30	ns
t_{PZH}				40	

Note: Typicals at 5V V_{CC} and 25° C T_A.

* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.

† See AC test and high-speed application note.

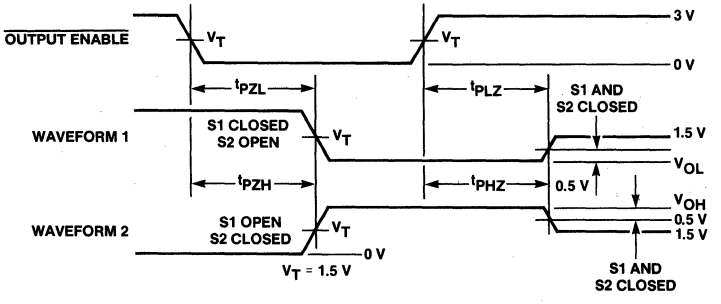
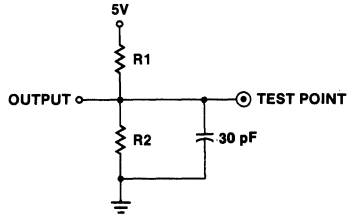


Figure A. Enable and Disable

Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

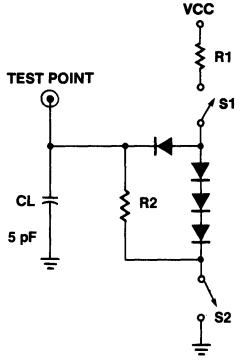
Standard Test Load



I_{OL}	R1	R2
24 mA	200 Ω	300 Ω
8 mA	600 Ω	1200 Ω

Input Pulse Amplitude = 3 V
Input Rise and Fall Time (10%-90%) = 2.5 ns
Measurements made at 1.5 V
All Diodes are 1N916 or 1N3064

Three-State Test Load



2

Functional Description

Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. An SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW. The FIFO should always be cleared by using master reset.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided the upstream stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between VCC and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input-Ready combination, as well as the Shift-Out-Output-Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to shift-in going HIGH. This same type of situation occurs with T_{ORL} and T_{ORH} as related to Shift-Out. For high-speed applications, proper grounding technique is essential.

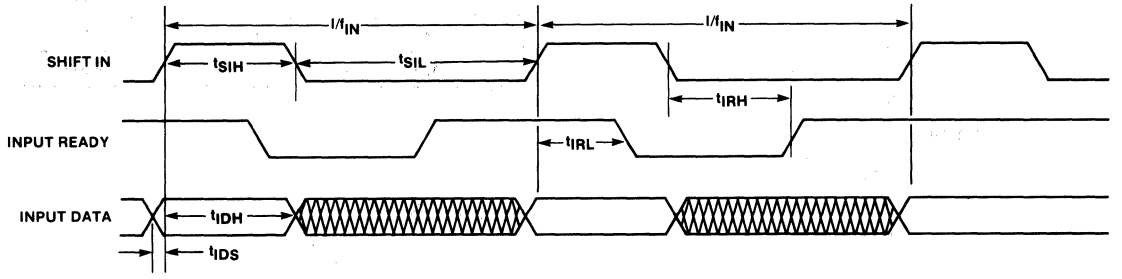


Figure 1. Input Timing

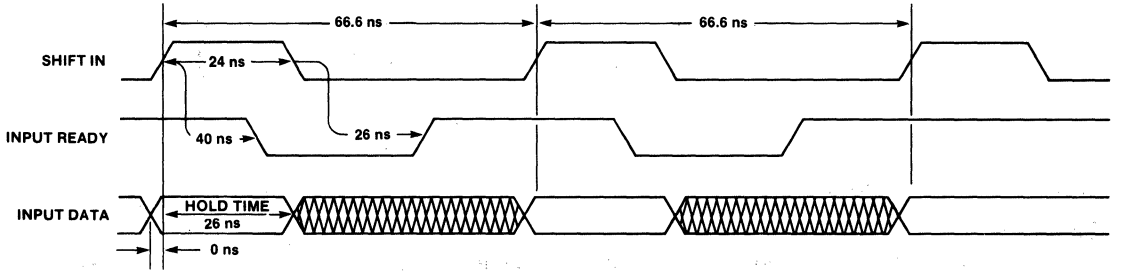


Figure 2. Typical Waveforms for 15 MHz Shift-In Rate

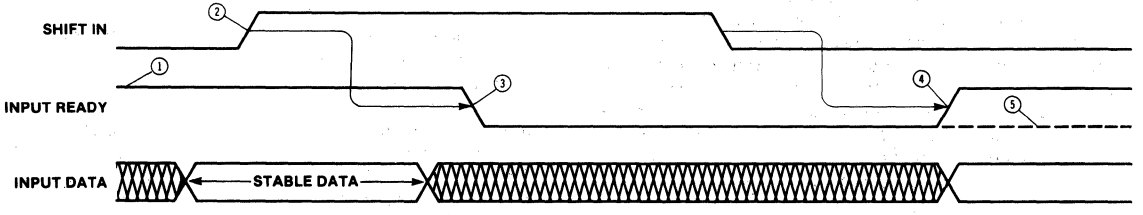


Figure 3. The Mechanism of Shifting Data into the FIFO

① Input Ready HIGH indicates space is avialable and a Shift-In pulse may be applied.

② Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.

③ Input Ready goes LOW indicating the first word is full.

④ Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.

⑤ If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

Note: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

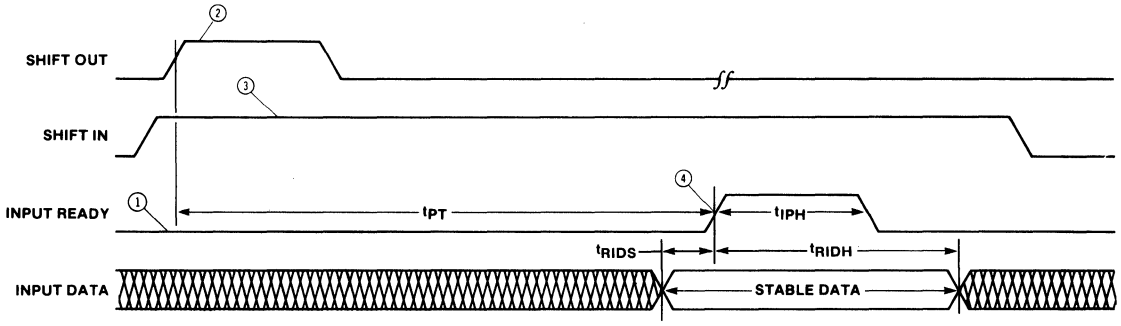


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

① FIFO is initially full.

② Shift Out pulsed is applied. An empty location starts "bubbling" to the front.

③ Shift In is held HIGH.

④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

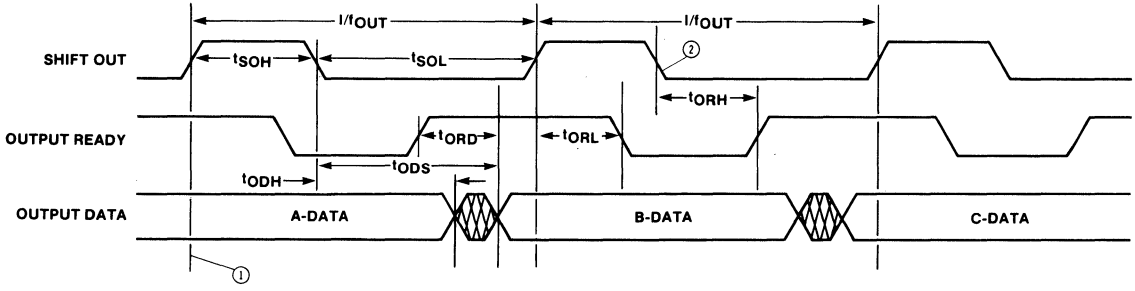


Figure 5. Output Timing

① The diagram assumes that at this time, words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.

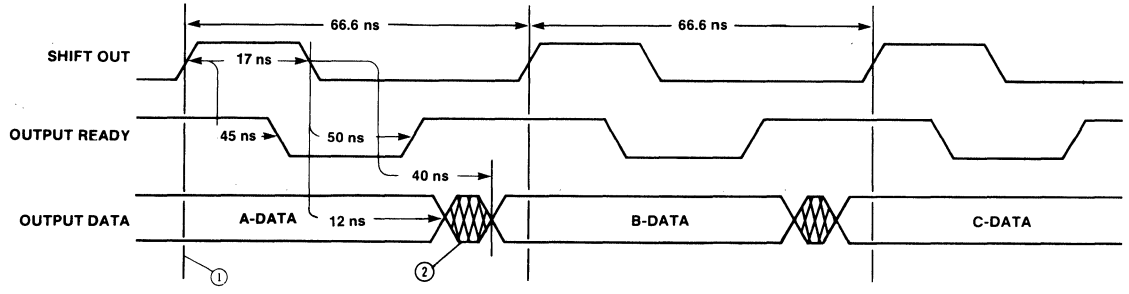


Figure 6. Waveforms for 15 MHz Shift-Out Data Rate

① The diagram assumes that at this time words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Data in the first crosshatched region may be A or B Data.

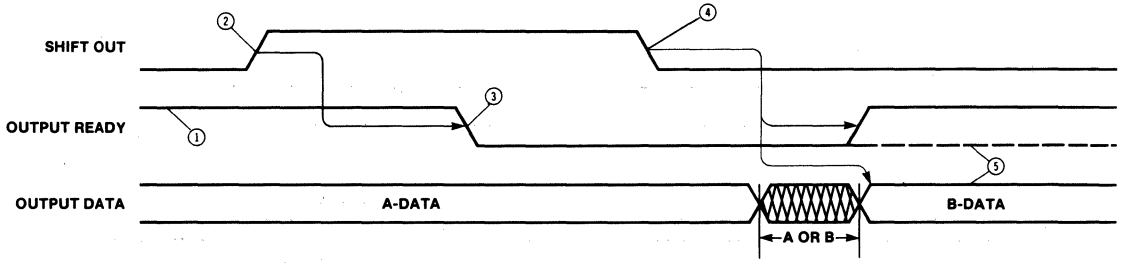


Figure 7. The Mechanism of Shifting Data Out of the FIFO

① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.

② Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.

③ Output Ready goes LOW.

④ Shift-Out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.

⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

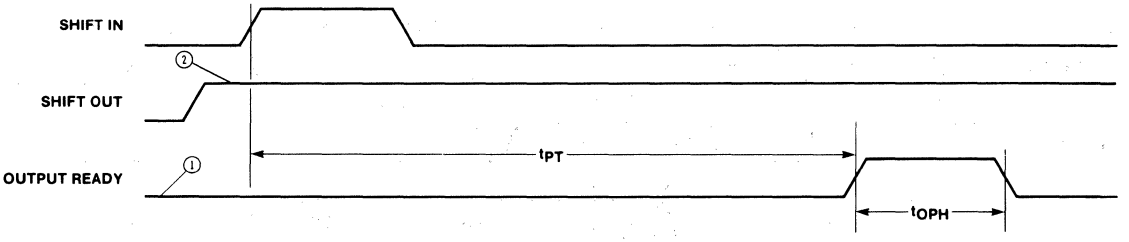


Figure 8. t_{PT} and t_{OPH} Specification

① FIFO initially empty.

② Shift Out held HIGH.

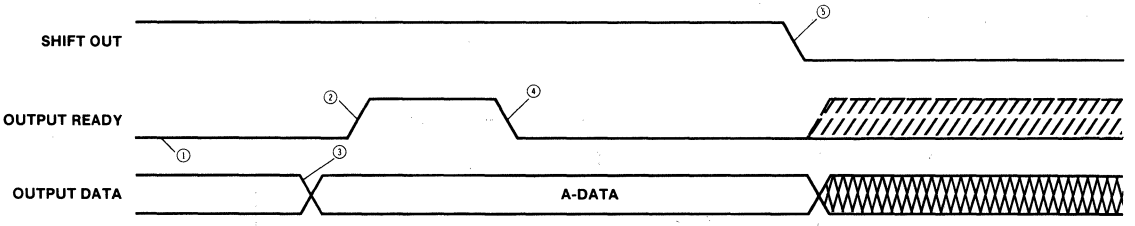


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

① Word 63 is empty.

② Output Ready goes HIGH indicating arrival of the new data.

③ New data (A) arrives at the outputs (word 63).

④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.

⑤ As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.

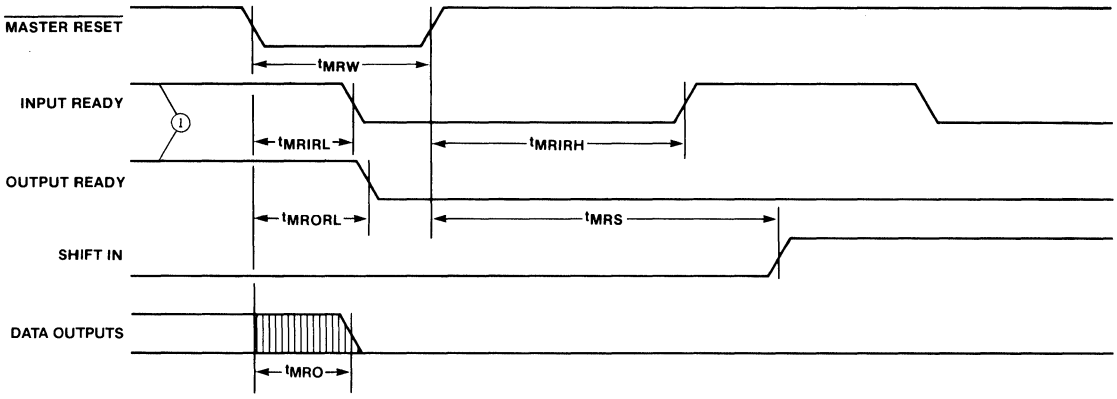


Figure 10. Master Reset Timing

① FIFO initially partially full.

Asynchronous First-In First-Out Memory (FIFO) 16x5 74S225/A

Features/Benefits

- **DC to 20-MHz shift-in/shift-out rates**
- **Fully expandable by word width and depth**
- **Three-state outputs**
- **TTL-compatible inputs and outputs**
- **Functionally compatible with T.I. SN74S225**
- **Designed for extended testability**

Description

The 74S225/A is a Schottky-clamped transistor-transistor logic (STTL) 16x5 First-In-First-Out memory (FIFO) which operates from DC to 10/20 MHz. The data is loaded and emptied on a first-in-first-out basis through asynchronous input and output ports. These devices are used in digital systems performing data transfers when source and receiver are not operating at the same data rate. FIFOs are also used as data buffers where the source and receiver are not operating at the same time. Both word length and FIFO depth are expandable. Unload clock output (Pin 3) is designed for testability of V_{OL}.

Ordering Information

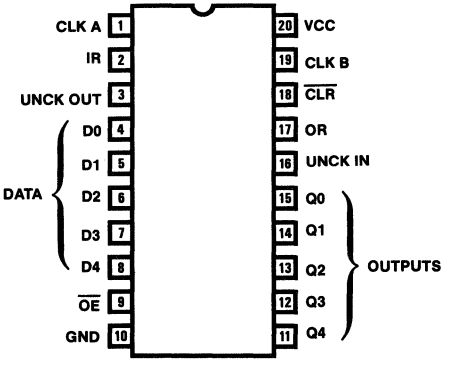
PART NUMBER	PACKAGE	TEMPERATURE
74S225	J, N	10 MHz Com
74S225A	J, N	20 MHz Com

Pin Names

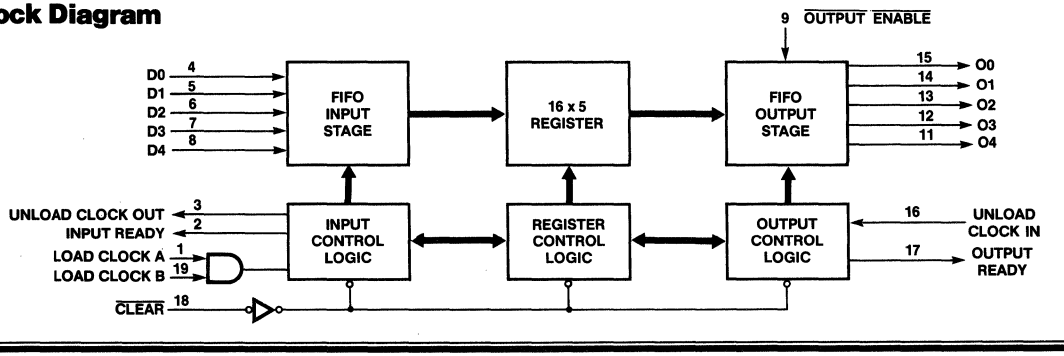
PIN #	PIN NAME	DESCRIPTION
1	CLK A	Load clock A
2	IR	Input ready
3	UNCK OUT	Unload clock output
4-8	D0-D4	Data inputs
9	$\overline{OE}$	Output enable
10	GND	Ground pin
11-15	Q4-Q0	Data outputs
16	UNCLK IN	Unload clock input
17	OR	Output ready
18	$\overline{CLR}$	Clear
19	CLK B	Load clock B
20	V_{CC}	Supply voltage

Pin Configuration

74S225/A . . J or N Package
(Top View)



Block Diagram



Publication #	Rev.	Amendment
10674	A	/0

Issue Date: May 1988

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65 to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	74S225A MIN	74S225A TYP	74S225A MAX	74S225 MIN	74S225 TYP	74S225 MAX	UNIT
V_{CC}	Supply voltage		4.75		5.25	4.75		5.25	V
t_A	Operating free-air temperature		0		75	0		75	°C
t_{LCKH}	LOAD CLOCK pulse width, A or B, t_w (HIGH)	2	22		36	25			ns
t_{IDS}	Setup time, data to load clock	2	-20↑*			-20↑*			ns
t_{IDH}	Hold time, data from load clock	2	50↑			70↑			ns
t_{UCKL}	UNLOAD CLOCK INPUT pulse width, t_w (LOW)	4	7		36	7			ns
t_{CLW}	CLEAR pulse width, t_w (low)	2	20			40			ns
t_{CLCK}	Setup time, clear release to load clock, t_{su}	2	10			25↑			ns

* Data must be setup within 20 ns after valid Load Clock (A or B) pulse (positive transition).

↑ = Arrow indicates that it is referenced to the LOW-to-HIGH transition.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		FIGURE	74S225A MIN	74S225A TYP	74S225A MAX	74S225 MIN	74S225 TYP	74S225 MAX	UNIT
f_{IN}	Load clock A or clock B	Cascade Mode**	2	20	22		10	20		MHz
		Standalone Mode								
t_{LCIRL}	CLK A or CLK B to IR↓ **		2		43	55		55	75	ns
t_{LCCOL}	CLK A or CLK B to UNCK OUT↓		2		31	40		25	50	ns
f_{OUT}	Unload clock input	Cascade Mode***	4	20	22		10	20		MHz
		Standalone Mode								
t_{UCKORL}	UNCK IN ↑ to OR LOW		4		26	35		30	45	ns
t_{UCKORH}	UNCK IN ↑ to OR HIGH		4		32	45		40	60	ns
t_{ODH}	Output data hold, UNCK IN to output data		4	20	30		20	50		ns
t_{ODS}	Output data setup, UNCK IN to output data		4		41	55		50	75	ns
t_{RIP}	CLK A or CLK B to OR ↑		7		167	220		190	300	ns
t_{CLOL}	CLR to OR ↓		6		31	40		35	60	ns
t_{CLIH}	CLR to IR ↑		6		15	20		16	35	ns
t_{UCKOW}	Pulse width, UNCK OUT, t_w		2	7	11		7	14		ns
t_{ORD}	OR ↑ to output data		4		9	15		10	20	ns
t_{BUBI}	UNCK IN to IR ↑ (bubble-back time)		8		214	290		255	400	ns
t_{BUBC}	UNCK IN to UNCK OUT ↓ (bubble-back time)		8		226	290		270	400	ns

↓ Arrow indicates that it is referenced to the HIGH-to-LOW transition.

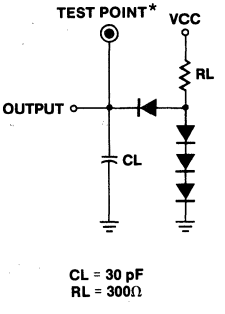
** 16th word only.

*** Devices connected to provide FIFO of greater than 16 word depth.

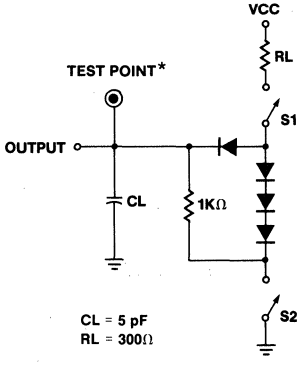
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	74S225A MIN	74S225A TYP	74S225A MAX	74S225 MIN	74S225 TYP	74S225 MAX	UNIT
t_{PHZ}	Output disable delay, $\overline{OE}$ to Q_i, C_L = 5 pF	1		8	25		10	25	ns
t_{PLZ}				18	25				
t_{PZL}	Output enable delay, $\overline{OE}$ to Q_i, C_L = 5 pF	1		19	40		25	40	ns
t_{PZH}				23	40				

Test Load for Bi-State Output



Test Load for Three-State Output



* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

Input Pulse Amplitude = 3.0 V
Input Rise and Fall Time (15%–90%) = 2.5 ns
Measurements made at 1.5 V

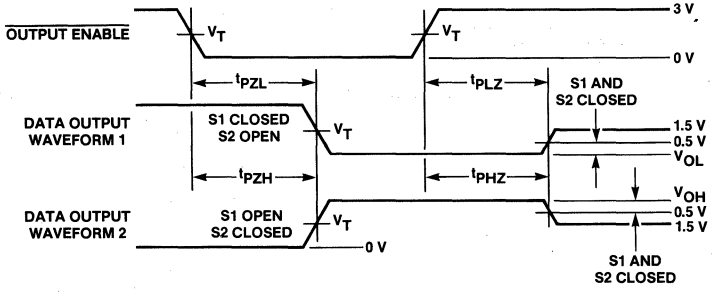


Figure 1. Enable and Disable

Waveform 1 is for an output with internal conditions such that the output is low except when disabled.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage							0.8	V
V_{IH}	High-level input voltage					2.0			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18 mA				−1.5	V
I_{IL1}	Low-level input current	D_0–D_4	V_{CC} = MAX	V_I = 0.5 V				−1	mA
I_{IL2}		All others						−.25	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.7 V	Data inputs			40	μA
					Others			25	
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5 V				1	mA
V_{OL}	Low-level output voltage*		V_{CC} = MIN	I_{OL} = 16 mA (Data outputs)				0.5	V
				I_{OL} = 8 mA (All others)					
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = −6.5 mA (Data outputs)		2.4			V
				I_{OH} = −3.2 mA (All others)					
I_{OS}	Output short-circuit current**		V_{CC} = MAX	V_O = 0 V		−30		−100	mA
I_{HZ}	Off-state output current		V_{CC} = MAX	V_O = 2.4 V				50	μA
I_{LZ}			V_{CC} = MAX	V_O = 0.5 V				−50	μA
I_{CC}	Supply current		V_{CC} = MAX	Inputs low, All outputs open	74S225		80	120	mA
					74S225A		80	125	

* To measure V_{OL} on Pin 3, force 10 V on Pin 9 (Extended Testability).

** Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Functional Description

Data Input

After power up the CLEAR is pulsed low (Figure 5) to prepare the FIFO to accept data in the first location. Clear must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH, the first location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when both Load Clocks (CLK A and CLK B) are brought HIGH. The CLK A HIGH and CLK B HIGH signal causes the IR and UNCK OUT to pulse LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{RIP} defines the time required for the first data to travel from input to the output of a previously empty device. When the sixteenth word is clocked into the device, the memory is full (sixteen words) and IR remains low. The Unload Clock Output is provided chiefly for use in cascading devices to extend FIFO depth (Figure 9). When Input Ready is Low, do not attempt to shift-in new data.

Data Output

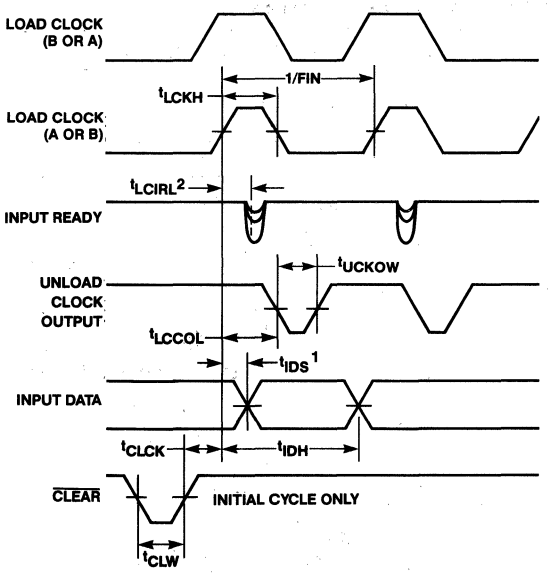
Data is read from the Q_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Unload Clock Input (UNCK IN) LOW. A LOW signal at UNCK IN causes the OR to go LOW. Valid data is maintained while the UNCK IN is LOW. When UNCK IN is brought HIGH the upstream data, provided that stage has valid data, is shifted to the output stage.

When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data remains valid for the last word.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{BUBI}) or completely empty (Output Ready stays LOW for at least t_{RIP}).

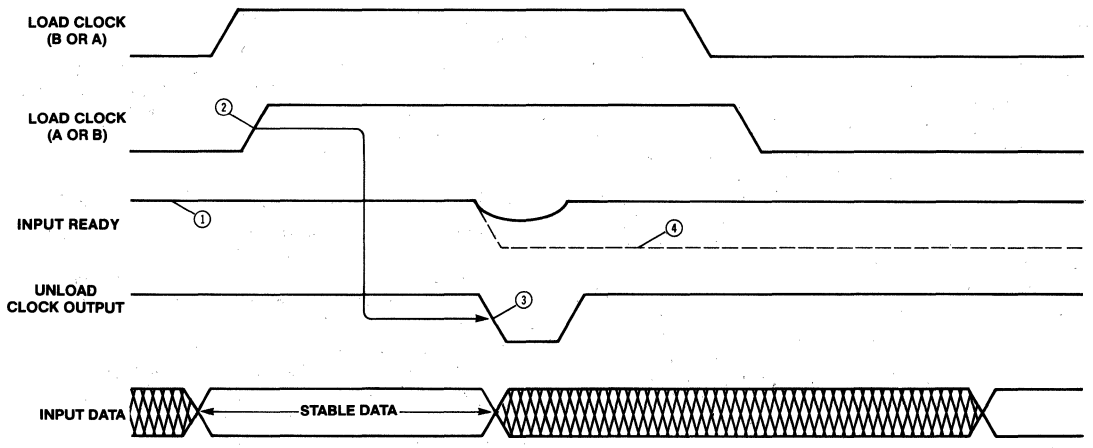
AC Test and High-Speed App. Notes

Since the FIFO is a high-speed device, care must be exercised in the design of the hardware and the timing utilized within the PC board design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Load Clocks (A, B) — Unload Clock Output-Input Ready combination, as well as the Unload Clock Input-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Load Clock pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or affected by ($\overline{CLR}$), the LOAD-CK activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (t_{IDH}) and the next activity of Input Ready (t_{LCIRL}) to be extended relative to Load Clock (A or B) going HIGH.



NOTES: 1. Permissible negative setup time for input data
2. Measure t_{LCIRL} for 16th input word only

Figure 2. Input Timing



NOTES: 1. Input Ready HIGH indicates space is available and a Load Clock (A and B) pulse may be applied.
2. Input Data is loaded into the first word.
3. Unload Clock Output pulses indicating the first word is full and the Data from the first word is released for "fall-through" to second word.
4. If the second word is already full, then the data remains at the first word. Since the FIFO is now full, Input Ready remains LOW.

Figure 3. The Mechanism of Clocking Data into the FIFO

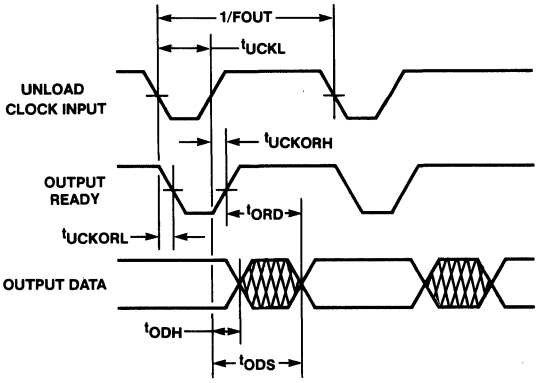
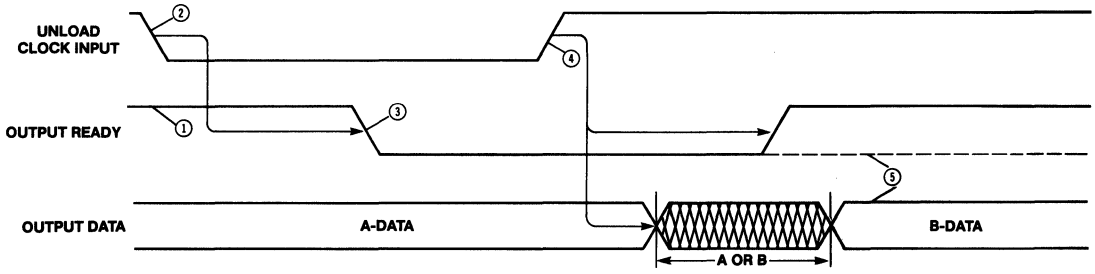


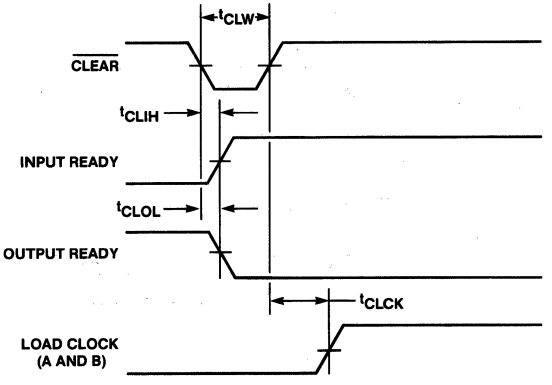
Figure 4. Output Timing



NOTES: 1. Output Ready HIGH indicates that data is available and an Unload Clock Input pulse may be applied.
2. Unload Clock Input goes LOW creating an empty position at word 16 for word 15 to "fall-through" to.
3. Output Ready goes LOW.
4. Unload Clock Input goes HIGH, causing Output Ready to go HIGH, indicating that new data (B) is now available at the FIFO outputs.
5. If the FIFO has only one word loaded (A-DATA), then Output Ready stays LOW and the A-DATA remains on the outputs.

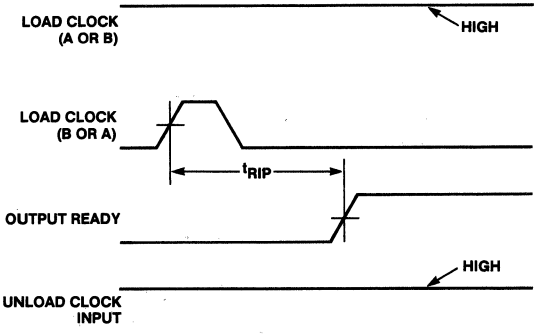
NOTE: Assume FIFO initially contains at least two words.

Figure 5. The Mechanism of Shifting Data Out of the FIFO



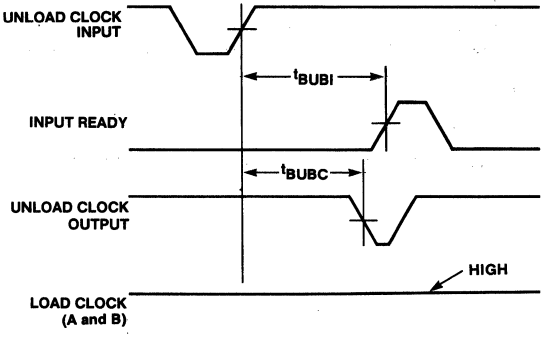
NOTE: Assume FIFO is full before $\overline{\text{CLEAR}}$ goes active.

Figure 6. Clear Timing



NOTES: 1. FIFO is initially empty.
2. Unload Clock Input and one Load Clock held HIGH throughout.

Figure 7. t_{RIP} Specifications



NOTES: 1. FIFO is initially full.
2. Load Clock (A and B) held HIGH throughout.

Figure 8. t_{BUBI}, t_{BUBC} Specifications

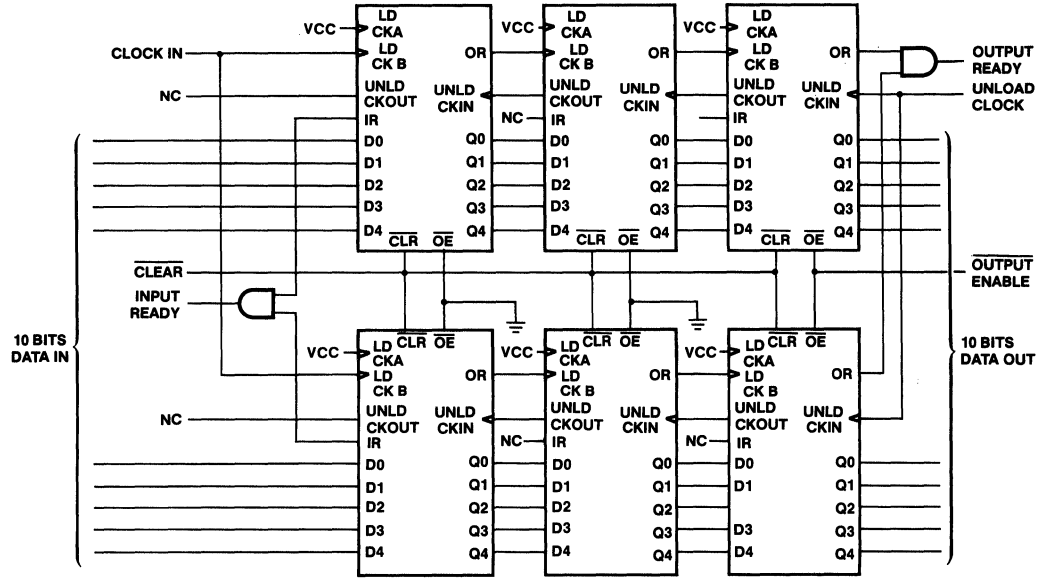


Figure 9. 48x10 FIFO with 74S225/A

Low Power First-In First-Out (FIFO) 64x5 Memory
67L402

Features/Benefits

- **Guaranteed 5 MHz shift-out/shift-in rates**
- **Low power consumption**
- **TTL inputs and outputs**
- **Readily expandable in the bit dimensions**
- **Structured pinouts. Output pins directly opposite corresponding input pins**
- **Asynchronous operation**

Ordering Information

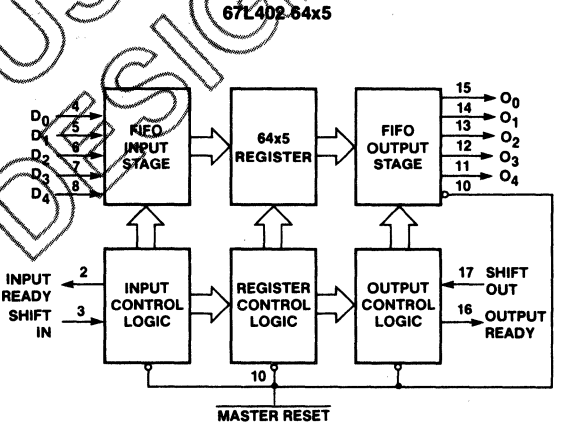
PART PACKAGE	PKG	TEMP	DESCRIPTION
67L402	N, NL	Com	5 MHz 64x5 FIFO
67L402	J, NL	Com	5 MHz 64x5 FIFO

Description

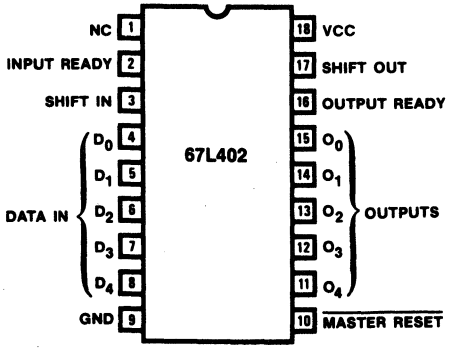
The 67L402 is a low-power First-In First-Out (FIFO) memory device with TTL speed. This device is organized in a 64x5-bit structure and easily expandable to any width. A 5 MHz data rate with fast "fall through" time allows usage in tape and disc controllers, printers and communications buffer applications. This data rate is much faster than a comparable MOS device. The FIFO is a register-based device. Data entered at the inputs "falls through" to the empty space closest to the output. Data is shifted out in the same sequence it is shifted in. Also, the width can be increased by putting the Input Ready signals through an AND gate to give a composite Input Ready. Similarly, the Output Ready signals should be gated to form a composite Output Ready.

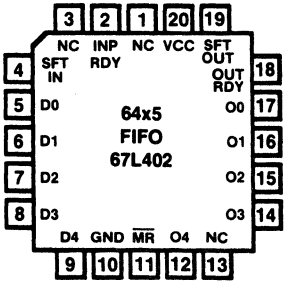
Generally, FIFOs are used in digital systems performing data transfers when source and receiver are not operating at the same data rate. FIFOs are also used as data buffers where the source and receiver are not operating at the same time. The 67L402 is particularly useful where low-power consumption is critical.

Block Diagram



Pin Configurations





Plastic Chip Carrier

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150° C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	55			ns
t_{SIL}	Shift in LOW time	1	55			ns
t_{IDS}	Input data setup	1	10			ns
t_{IDH}	Input data hold time	1	80			ns
t_{SOH}†	Shift Out HIGH time	5	55			ns
t_{SOL}	Shift Out LOW time	5	55			ns
t_{MRW}	Master Reset pulse	10	40			ns
t_{MRS}	Master Reset to SI	10	35			ns

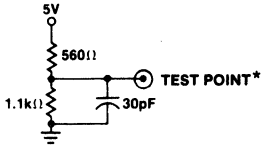
Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	5			MHz
t_{IRL}†	Shift in to Input Ready LOW	1			75	ns
t_{IRH}†	Shift in to Input Ready HIGH	1			75	ns
f_{OUT}	Shift Out rate	5	5			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			75	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			80	ns
t_{ODH}	Output Data Hold (previous word)	5	8			ns
t_{ODS}	Output Data Shift (next word)	5			70	ns
t_{PT}	Data throughput or "fall through"	4, 8			4	μs
t_{MRORL}	Master Reset to OR LOW	10			85	ns
t_{MRIRH}	Master Reset to IR HIGH	10			85	ns
t_{IPH}	Input Ready pulse HIGH	4	20			ns
t_{OPH}	Output Ready pulse HIGH	8	20			ns

† See AC test and application note

Test Load

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



Input Pulse 0 to 3 V
Input Rise and Fall Time (10% - 90%)
5 ns minimum
Measurements made at 1.5 V

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18mA			-1.5	V
I_{IL1}	Low-level	D_0-D_3 MR	V_{CC} = MAX	V_I = 0.45V			-0.8	mA
I_{IL2}	input current	SI, SO					-1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = -0.9mA	2.4			V
I_{OS}	Output short-circuit current*		V_{CC} = MAX	V_O = 0V	-20		-90	mA
I_{CC}	Supply Current		V_{CC} = MAX	Inputs Low, Outputs Open		113	130	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† This is an absolute voltage with respect to device GND (Pin 8 or 9) and includes all overshoots due to test equipment.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 11) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and Application Note

Since the FIFO is a high-speed device, care must be exercised in design of the hardware and the timing. Though the external data rate is 5 MHz, internally the device is several times as fast. Device grounding and decoupling is crucial to correct operation, as the FIFO is sensitive to very small glitches caused by long reflective lines, high capacitances, and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with a very short lead length. In addition, care must be exercised in timing setup and measurement of parameters. For example, since an AND gate function is associated with both the Shift In-Input Ready Combination as well as the Shift Out-Output Ready Combination, timing measurements may be misleading. i.e., rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency, or the FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going High.

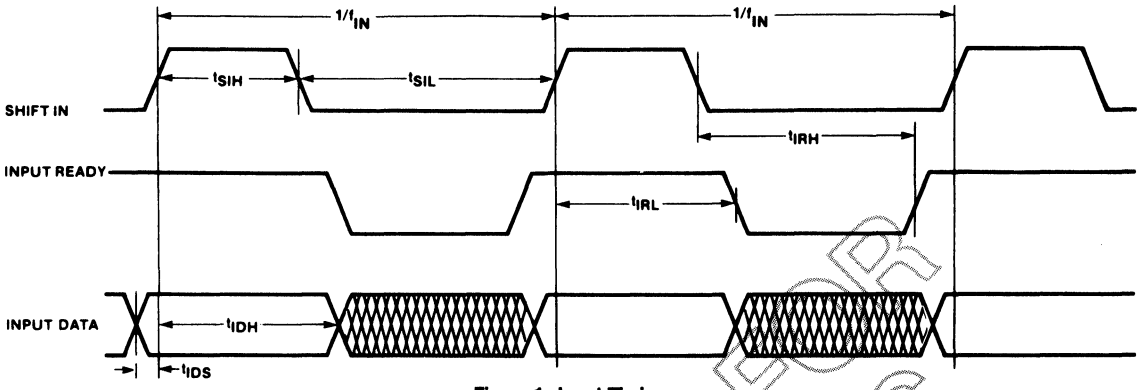


Figure 1. Input Timing

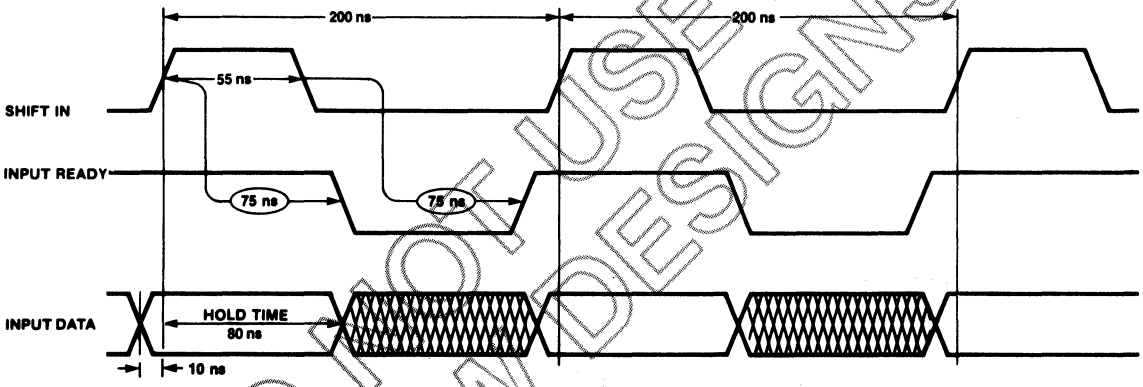


Figure 2. Typical Waveforms for 5 MHz Shift In Data Rate

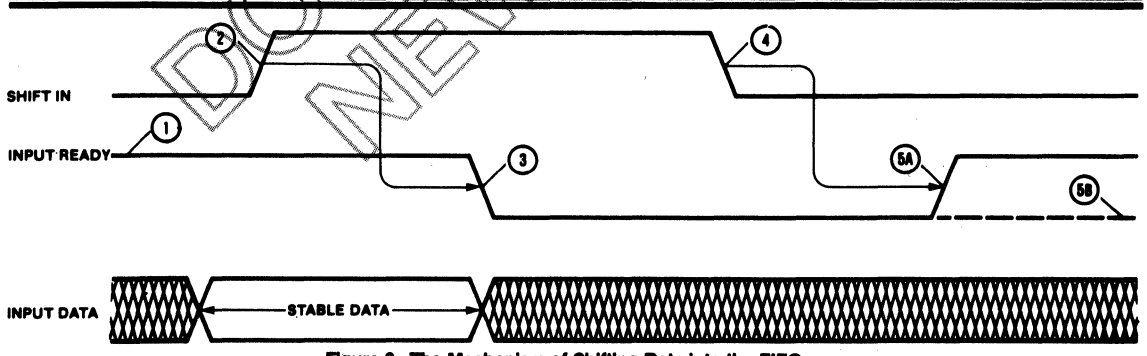


Figure 3. The Mechanism of Shifting Data into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied.

(2) Input Data is loaded into the first word.

(3) Input Ready goes LOW indicating the first word is full.

(4) The Data from the first word is released for "fall-through" to second word.

(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

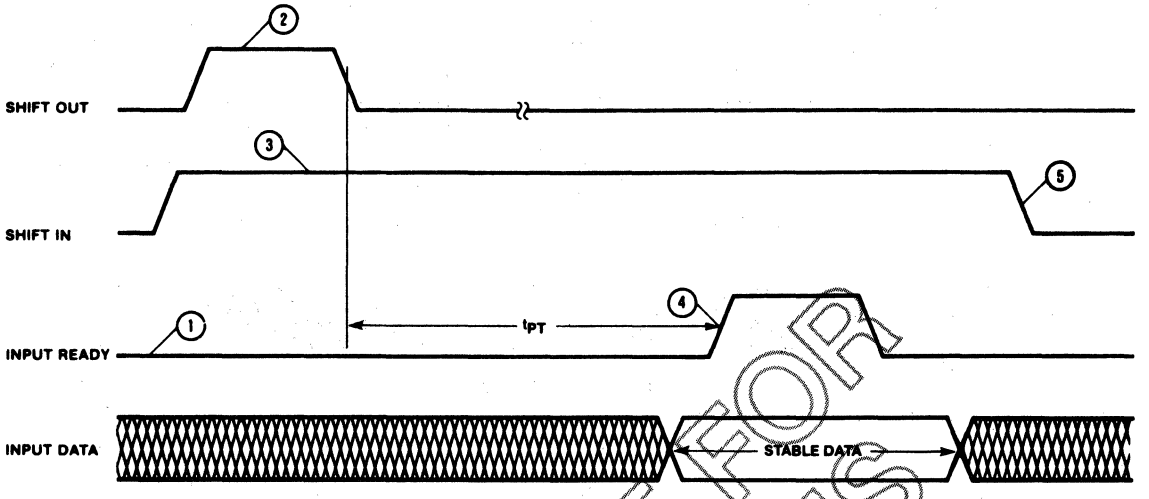
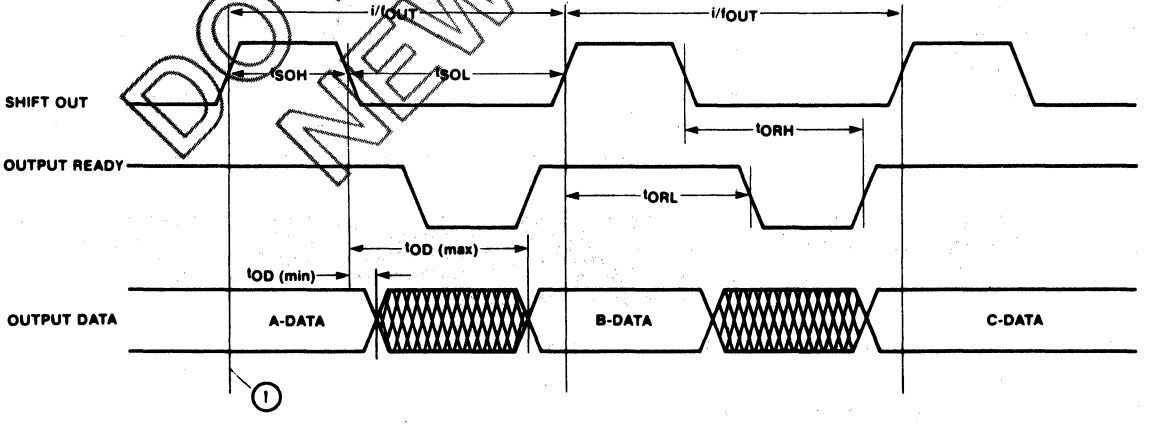


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

(1) FIFO is initially full.
(2) Shift Out pulse is applied. An empty location start "bubbling" to the front.
(3) Shift In is held HIGH.
(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
(5) The Data from the first word is released for "fall through" to second word.



(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively

Figure 5. Output Timing

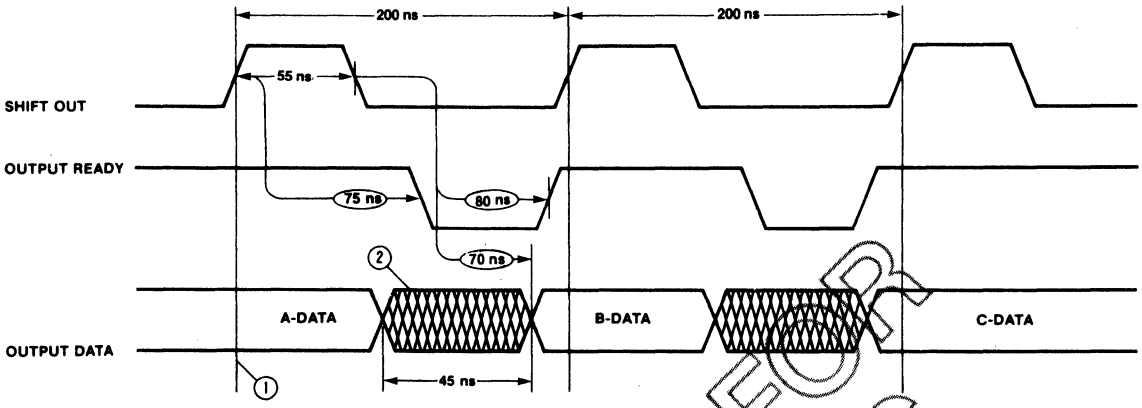


Figure 6. Typical Waveform for 5 MHz Shift Out Data Rate

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data in the crosshatched region may be A or B Data.

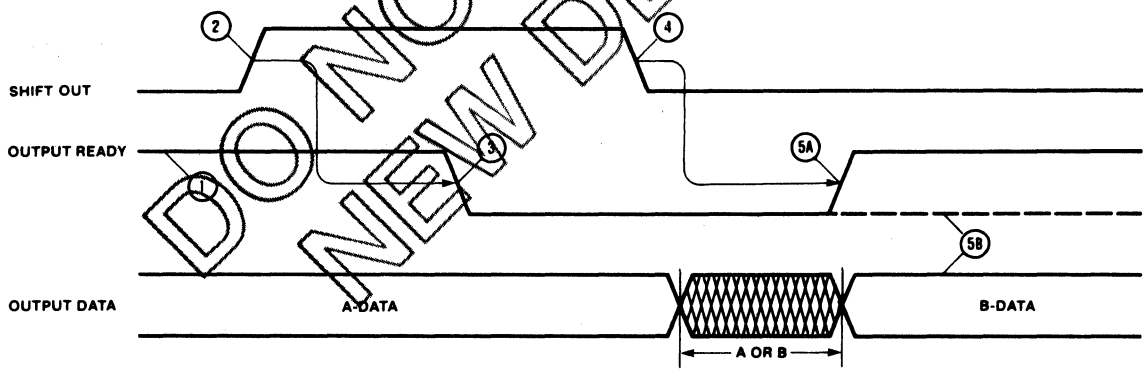


Figure 7. The Mechanism of Shifting Data Out of the FIFO

(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

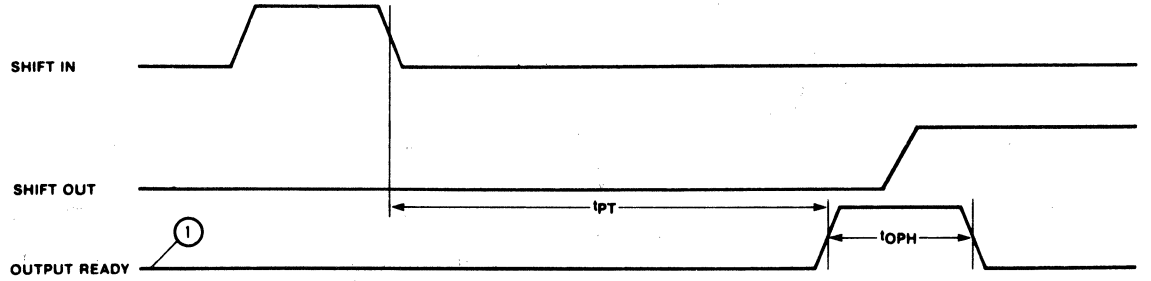
(2) Shift Out goes HIGH causing the next step.

(3) Output Ready goes LOW.

(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.



1 FIFO initially empty.

Figure 8. t_{PT} and t_{OPH} Specification

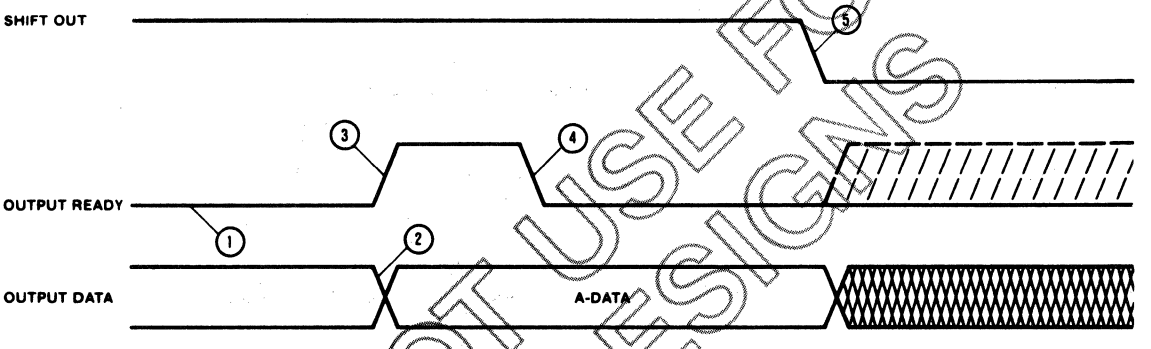
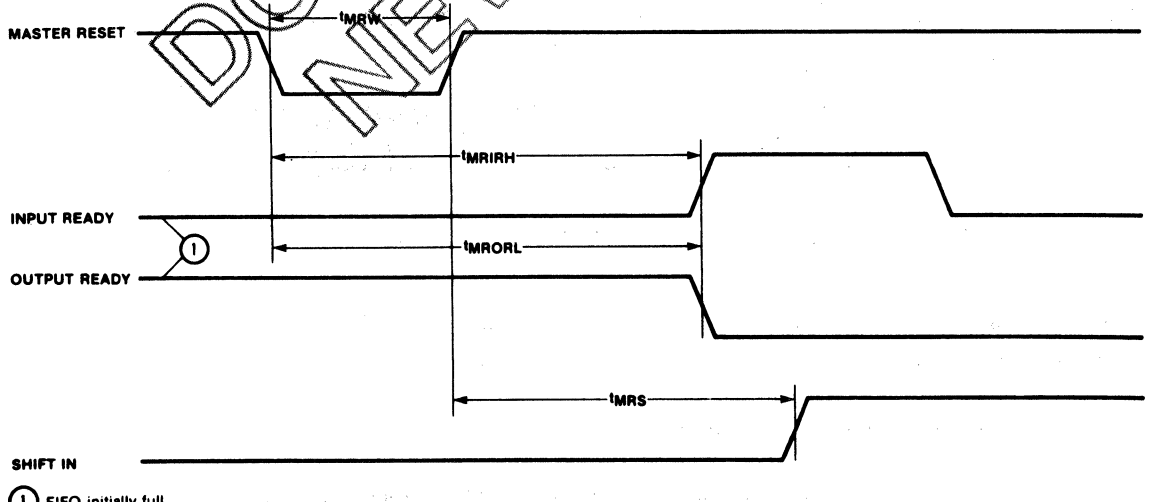


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH

1. Word 63 is empty.
2. New data (A) arrives at the outputs (word 63).
3. Output Ready goes HIGH indicating the arrival of the new data.
4. Since Shift Out is held HIGH, Output Ready goes immediately LOW.
5. As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.



1 FIFO initially full.

Figure 10. Master Reset Timing

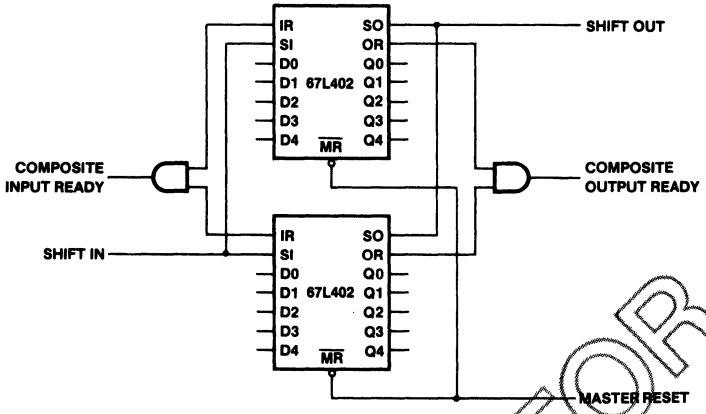


Figure 11. 64x8 FIFO With 67L402's

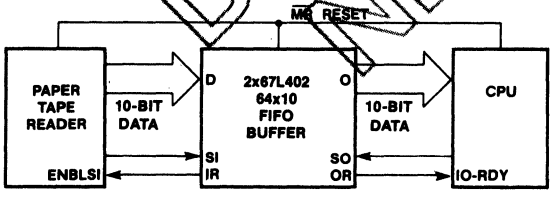
FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall through times of the FIFOs.

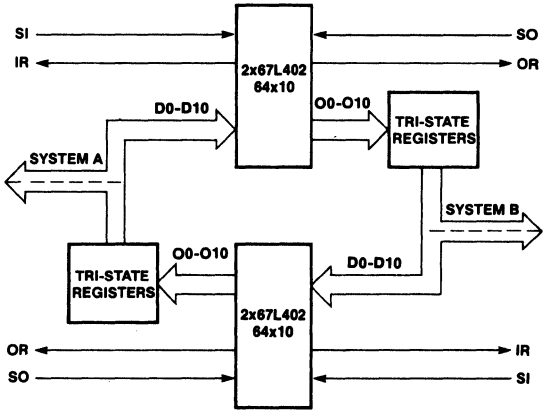
2

Applications

FIFOs are typically used as temporary data buffers between mismatching data rates. Such an application is shown in Figure 12.

The 67LS402 can also be used in a bidirectional operation as shown in Figure 13.





NOTE: Both depth and width expansion can be used in this mode.

Figure 12. FIFO As Data Buffer Between Slow Steady Rate and Fast 'Burst' Rate

Figure 13. Bidirectional FIFO Application

First-In First-Out (FIFO) 64x5 Memory 15 MHz (Cascadable)

C67L4033D

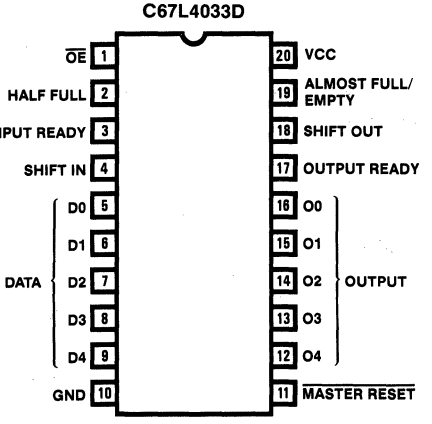
Features/Benefits

- **High-speed 15 MHz shift-in/shift-out rates**
- **High drive capability**
- **Low-power consumption**
- **Three-state outputs**
- **Fully expandable by word width and depth**
- **Half-Full and Almost-Full/Empty status flags**
- **Structured pinouts. Output pins directly opposite corresponding input pins.**
- **Asynchronous operation**
- **TTL-compatible inputs and outputs**

Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
C67L4033D	N,J	Com	15 MHz in/out

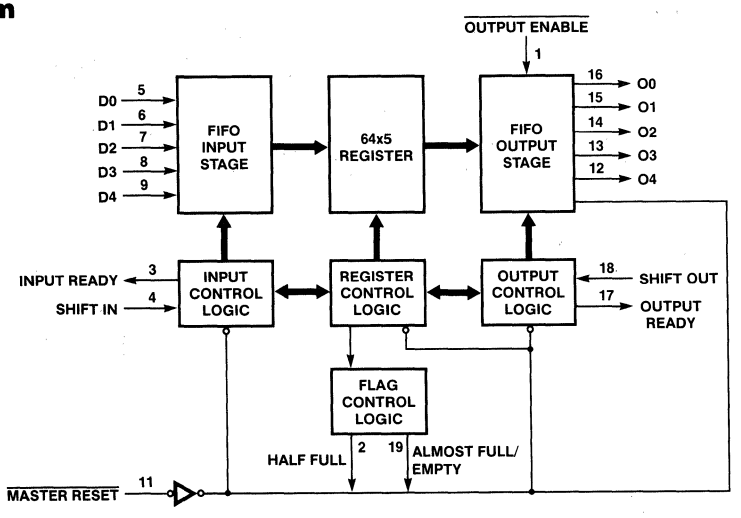
Pin Configuration



Description

The C67L4033D is a high-speed, 64x5 First-In-First-Out (FIFO) memory which operates at 15 MHz input/output rates. The data is loaded and emptied on a first-in-first-out basis. It is a three-state device with high-drive (I_{OL} = 24 mA) data outputs. These devices can be expanded to any word width and depth. It has a Half-Full flag (thirty-two or more words full) and an almost full/empty flag (fifty-six or more words or eight or less words). The main application of C67L4033D is as a rate buffer; sourcing and absorbing data at different rates. Other applications are high-speed tape and disk controllers, data communications systems and plotter control systems.

Block Diagram



Publication #	Rev.	Amendment
10681	A	/0

Issue Date: May 1988

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		70	°C
f_{IN}	Shift In rate	1			15	MHz
t_{SIH}*	Shift in HIGH time	1	24			ns
t_{SIL}*	Shift in LOW time	1	15			ns
t_{IDS}	Input data setup to SI (Shift In)	1	0			ns
t_{IDH}	Input data hold time from SI (Shift In)	1	26			ns
t_{RIDS}	Input data setup to IR (Input Ready)	4	0			ns
t_{RIDH}	Input data hold time from IR (Input Ready)	4	26			ns
f_{OUT}	Shift Out rate	5			15	MHz
t_{SOH}**	Shift Out HIGH time	5	17			ns
t_{SOL}	Shift Out LOW time	5	15			ns
t_{MRW}*	Master Reset pulse	10	35			ns
t_{MRS}**	Master Reset to SI	10	35			ns

* See AC test and high-speed application note.
** If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITION		COMMERCIAL MIN	COMMERCIAL MAX	UNIT
V_{IL}*	Low-level input voltage					0.8	V
V_{IH}*	High-level input voltage				2		V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18 mA		-1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.45 V		-250	μA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4 V		50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5 V		1	mA
V_{OL}	Low-level output voltage	Output, O	V_{CC} = MIN	I_{OL} = 24 mA		0.5	V
		IR,OR,HF,AF/E		I_{OL} = 8 mA		0.5	
V_{OH}	High-level output voltage	Output, O	V_{CC} = MIN	I_{OH} = - 3 mA	2.4		V
		IR,OR,HF,AF/E		I_{OH} = -0.9 mA			
I_{OS}**	Output short-circuit current		V_{CC} = MAX	V_O = 0 V	-20	-90	mA
I_{OZL}	Off-state output current		V_{CC} = MAX	V_O = 0.4 V		-50	μA
I_{OZH}				V_O = 2.4 V		50	
I_{CC}	Supply current		V_{CC} = MAX	All inputs low. All outputs open.		120	mA

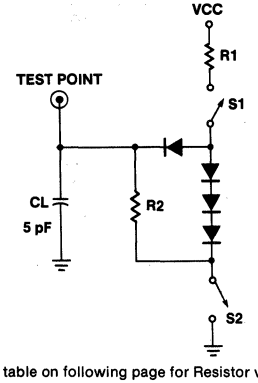
* These are absolute voltages with respect to GND (Pin 10) and include all overshoots due to system and/or tester noise.
** Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL MAX	UNIT
t_{IRL}	Shift In ↑ to Input Ready LOW	1		40	ns
t_{IRH}	Shift In ↓ to Input Ready HIGH	1		26	ns
t_{ORL}	Shift Out ↑ to Output Ready LOW	5		45	ns
t_{ORH}	Shift Out ↓ to Output Ready HIGH	5		50	ns
t_{ODH}	Output Data Hold (previous word)	5	12		ns
t_{ODS}	Output Data Shift (next word)	5		40	ns
t_{PT}	Data throughput	4,8		1600	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	10		60	ns
t_{MRIRH}*	Master Reset ↑ to Input Ready HIGH	10		30	ns
t_{MRIRL}*	Master Reset ↓ to Input Ready LOW	10		50	ns
t_{MRO}	Master Reset ↓ to Outputs LOW	10		60	ns
t_{IPH}	Input ready pulse HIGH	4	17		ns
t_{OPH}	Output ready pulse HIGH	8	24		ns
t_{ORD}	Output ready ↑ to Data Valid	5		-3	ns
t_{AEH}*	Shift Out ↑ to AF/E HIGH	11		320	ns
t_{AEL}*	Shift In ↑ to AF/E LOW	11		1400	ns
t_{AFL}*	Shift Out ↑ to AF/E LOW	12		1400	ns
t_{AFH}*	Shift In ↑ to AF/E HIGH	12		320	ns
t_{HFH}*	Shift In ↑ to HF HIGH	13		800	ns
t_{HFL}*	Shift Out ↑ to HF LOW	13		800	ns
t_{PHZ}*	Output Disable Delay	A		30	ns
t_{PLZ}*				30	
t_{PZL}*	Output Enable Delay			30	ns
t_{PZH}*				40	

* See timing diagram for explanation of parameters.

Three-State Test Load



See table on following page for Resistor values

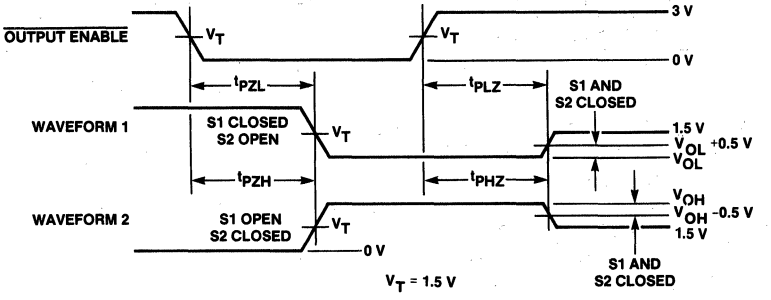
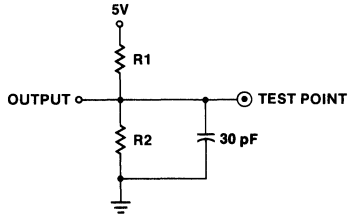


Figure A. Enable and Disable

Waveform 1 is for a data output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for a data output with internal conditions such that the output is high except when disabled by the output control.

Standard Test Load



I_{OL}	R1	R2
24 mA (Data)	200 Ω	300 Ω
8 mA (IR, OR, Flags)	600 Ω	1200 Ω

Input Pulse Amplitude = 3 V
Input Rise and Fall Time (10%-90%) = 2.5 ns
Measurements made at 1.5 V
All Diodes are 1N916 or 1N3064

Functional Description

Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master Reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the D_X inputs. Data then present at the the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data in any full cell to the adjacent (downstream) empty cell is automatically activated by an on-chip control. Thus data will stack up at the end of the device (while empty locations will "bubble" to the front when data is shifted out). t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW. The FIFO should always be cleared by using Master Reset before starting the operation.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that there is valid upstream data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to Shift-in going HIGH. This same type of problem is also related to T_{IRH}, T_{ORL} and T_{ORH} as related to Shift-Out. For high-speed applications, proper grounding technique is essential.

Timing Waveforms

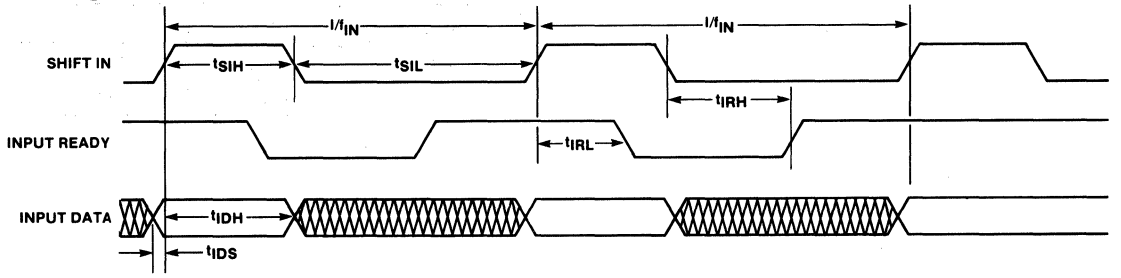


Figure 1. Input Timing

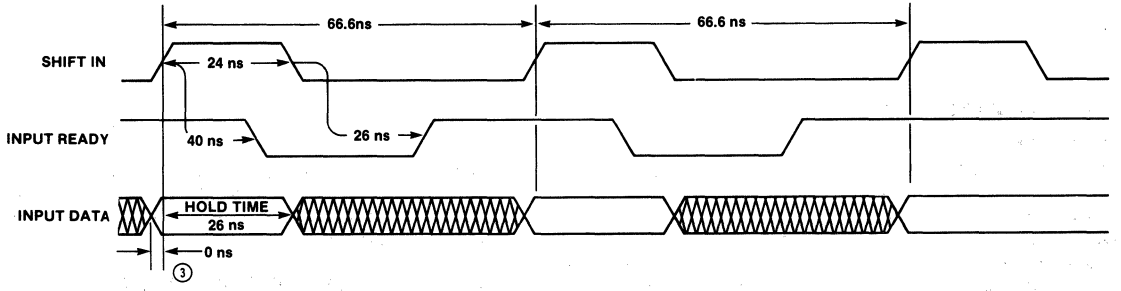


Figure 2. Typical Waveforms for 15 MHz Shift-In Data Rate

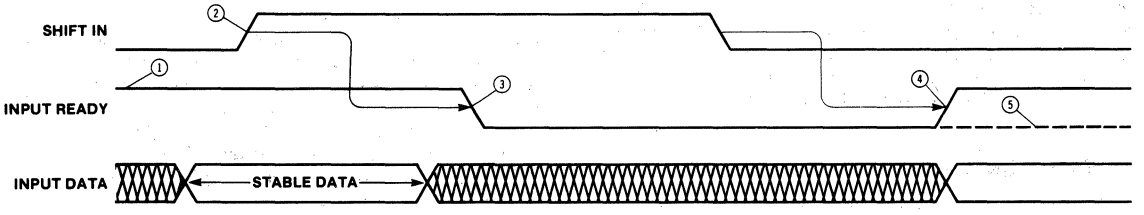


Figure 3. The Mechanism of Shifting Data into the FIFO

① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.

② Input Data is loaded into the first word. The data from the first word is released for "fall-through" to second word.

③ Input Ready goes LOW indicating the first word is full.

④ Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.

⑤ If the second word is already full then data remains at the first word. Since the FIFO is now full Input Ready remains low.

Note: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

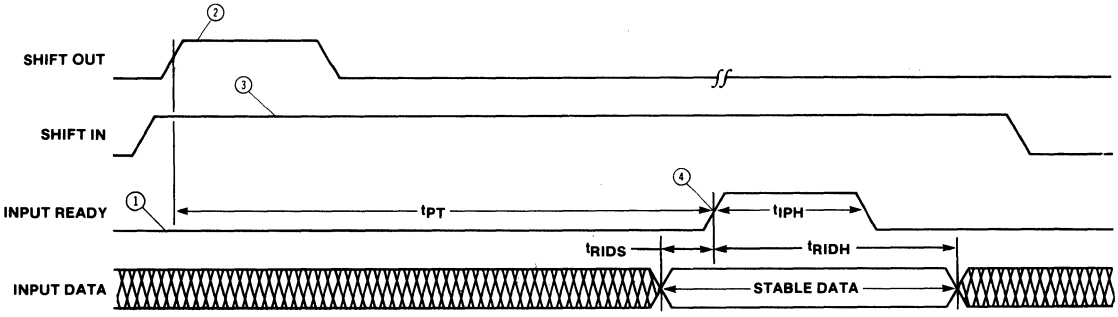


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

① FIFO is initially full.

② Shift Out pulse is applied. An empty location starts "bubbling" to the front.

③ Shift In is held HIGH.

④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

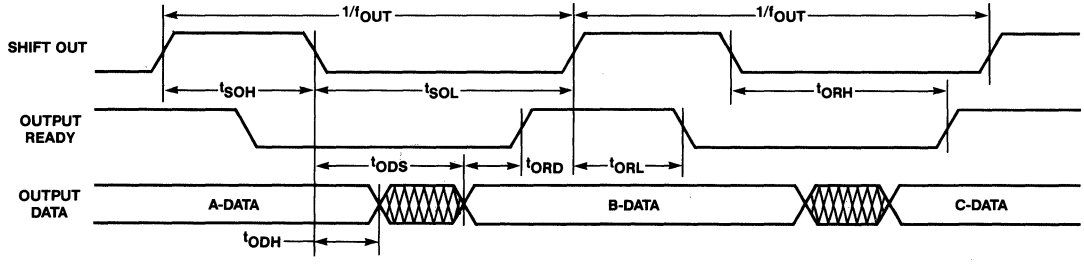


Figure 5. Output Timing

① The diagram assumes that at this time, words 64, 63 and 62 are loaded with A, B and C Data, respectively.

② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO are both high together.

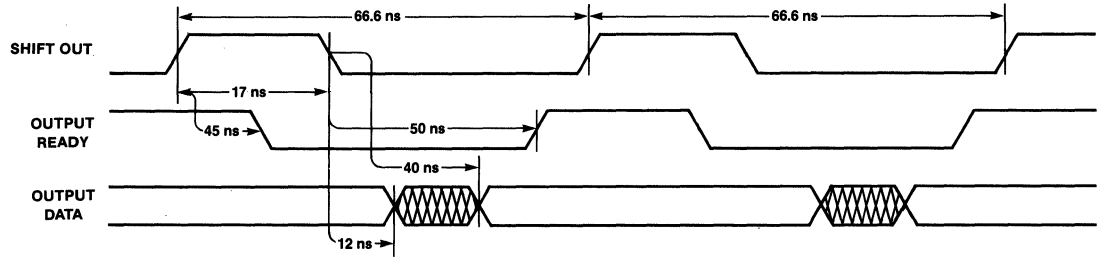


Figure 6. Typical Waveforms for 15 MHz Shift-Out Data Rate

① The diagram assumes that at this time words 64, 63 and 62 are loaded with A, B and C Data, respectively.

② Data in the first crosshatched region may be A or B Data.

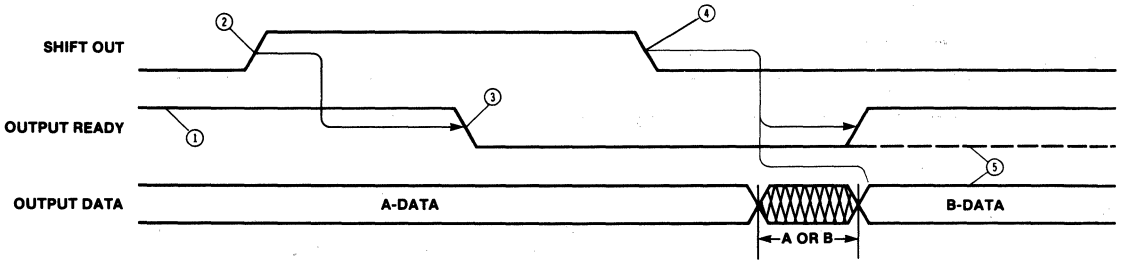


Figure 7. The Mechanism of Shifting Data Out of the FIFO

① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
② Shift-Out goes HIGH causing the contents of word 63 (B-Data) to be released for fall-through to word 64. Output data remains as valid A-Data while Shift-Out is HIGH.
③ Output Ready goes LOW.
④ Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

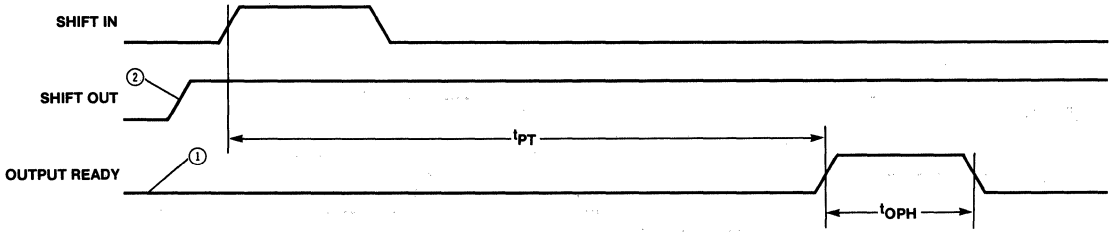


Figure 8. t_{PT} and t_{OPH} Specification

① FIFO initially empty.
② Shift-Out is held HIGH.

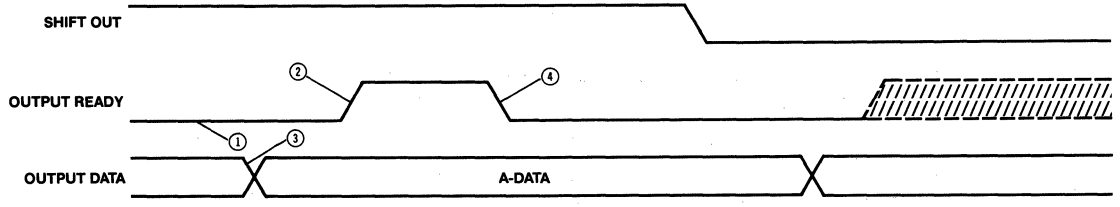


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH

① Word 64 is empty.
② Output Ready goes HIGH indicating arrival of the new data.
③ New data (A) arrives at the outputs (word 64).
④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.
⑤ As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.

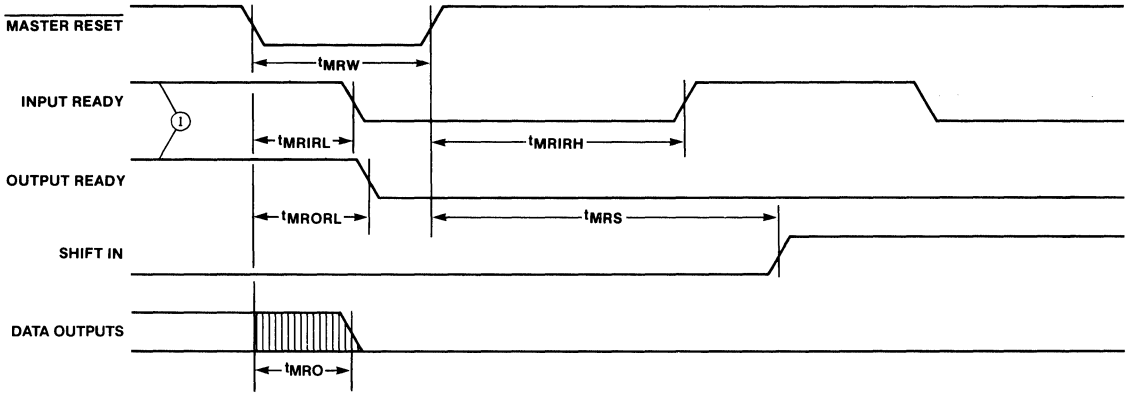


Figure 10. Master Reset Timing

① FIFO is partially full.

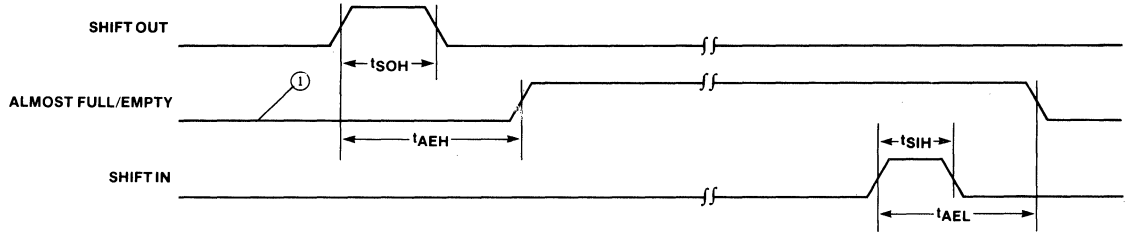


Figure 11. t_{AEH}, t_{AEL} Specifications

① FIFO contains 9 words (one more than almost empty).

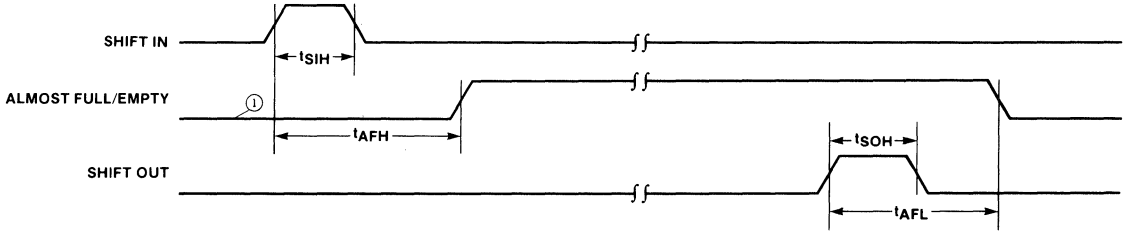


Figure 12. t_{AFH}, t_{AFL} Specifications

① FIFO contains 55 words (one short of almost full).

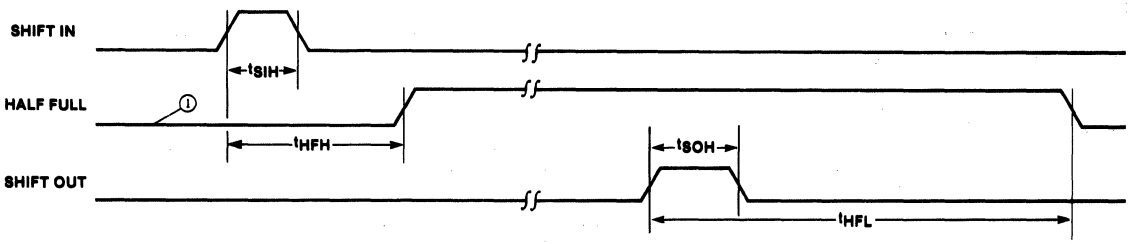
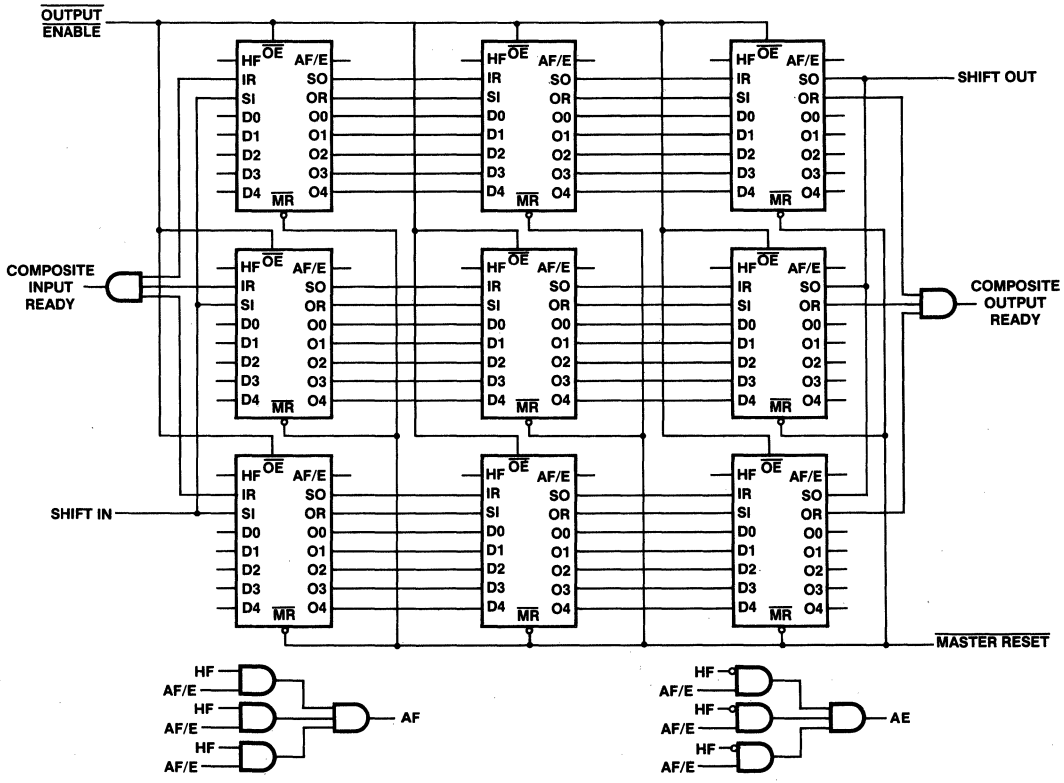


Figure 13. t_{HFL}, t_{HFH} Specifications

① FIFO contains 31 words (one short of half full).



The First Column of FIFOs

The Last Column of FIFOs

Almost Full (AF) is eight words or less to FIFO full.
Almost Empty (AE) is eight words or less to FIFO empty

Figure 14. 192x15 FIFO with C67L4033D

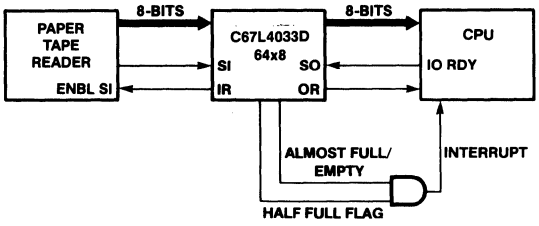


Figure 15. Application for C67L4033D "Slow and Steady Rate to Fast 'Blocked Rate' "

Note: Cascading the FIFO's in word width is done by ANDing the IR and OR as shown in Figure 14.

First-In First-Out (FIFO) 64x4 64x5 Memory

67411A 67412A

35 MHz (Standalone)

Features/Benefits

- High-speed 35-MHz shift-in/shift-out rates
- Choice of 4-bit or 5-bit data width
- TTL inputs and outputs
- Readily expandable in word width
- Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation

Ordering Information

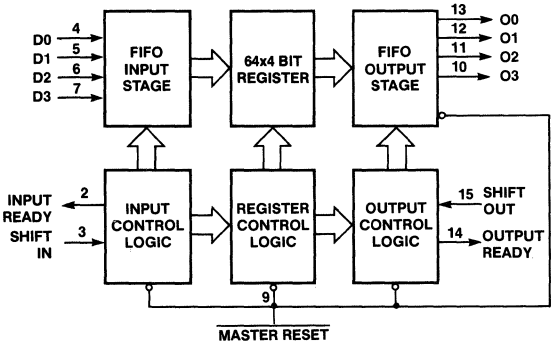
PART NUMBER	PKG	TEMP	DESCRIPTION
67411A	J	Com	35 MHz 64x4 FIFO
67412A	J	Com	35 MHz 64x5 FIFO

Description

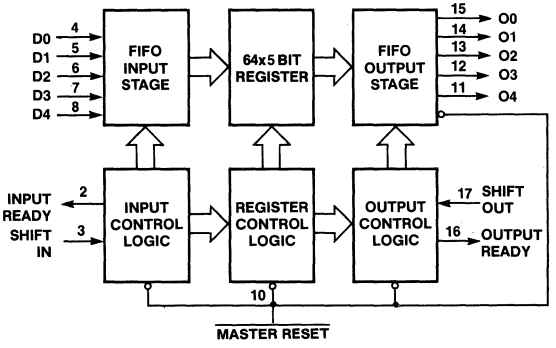
The 67411/2A are "fall-through" high-speed First-In First-Out (FIFO) memory organized 64 words by 4 bits and 64 words by 5 bits respectively. The FIFO is expandable in word width only. It is the fastest FIFO available on the market. The FIFO is attractive for many applications such as disk controllers, communication buffers, rate buffers, etc.

Block Diagrams

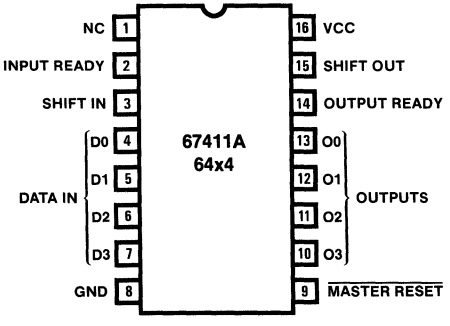
67411A

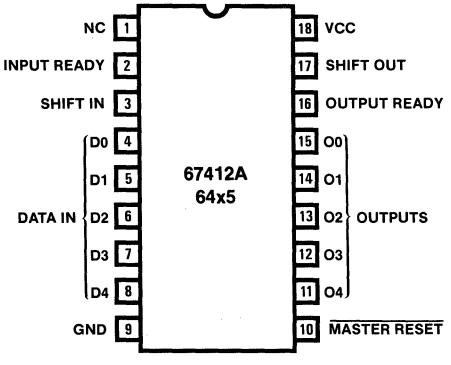


67412A



Pin Configurations





Publication #	Rev.	Amendment
10679	A	/0

Issue Date: May 1988

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -.5 V to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	9			ns
t_{IDS}	Input data set up	1	2			ns
t_{IDH}	Input data hold time	1	14			ns
t_{SOH}†	Shift Out HIGH time	5	11			ns
t_{MRW}	Master Reset pulse †	10	30			ns
t_{MRS}	Master Reset to SI*	10	35			ns

2

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
f_{IN}	Shift In rate	1	DC		††30	MHz
			DC		†††35	
t_{IRL}†	Shift In ↑ to Input Ready LOW	1		12	18	ns
t_{IRH}†	Shift In ↓ to Input Ready HIGH	1		14	20	ns
f_{OUT}	Shift Out rate	5	DC		††30	MHz
			DC		†††35	
t_{ORL}†	Shift Out ↑ to Output Ready LOW	5		12	18	ns
t_{ORH}†	Shift Out ↓ to Output Ready HIGH	5		14	20	ns
t_{ODH}†	Output Data Hold (previous word)	5	9			ns
t_{ODS}	Output Data Shift (next word)	5			31	ns
t_{PT}	Data throughput or "fall through"	4,8		510	650	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	10		18	28	ns
t_{MRIRH}	Master Reset ↑ to Input Ready HIGH*	10		21	35	ns
t_{MRIRL}	Master Reset ↓ Input Ready LOW*	10		18	28	ns
t_{MRO}	Master Reset ↓ to Outputs LOW	10		32	45	ns

Note: Typical at 5 V V_{CC} and 25°C T_{AA}.
* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low returning high when $\overline{MR}$ goes high.
† See AC test and high-speed application note.
†† Tested.
††† Guaranteed by design (see test load).

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION				MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage							0.8 †	V
V_{IH}	High-level input voltage					2 †			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA					-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45 V					-50	μA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V					50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V					1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} (Data Outputs)	67411/2A = 24 mA				0.5	V
			I_{OL} (IR, OR)	67411/2A = 8 mA ††					
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} (Data Out)	67411/2A	-3.0 mA	2.4			V
			I_{OH} (IR,OR)		-0.9 mA				
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0 V			-20		-90	mA
I_{CC}	Supply current	V_{CC} = MAX. Inputs low, outputs open (67411/2A)						**240	mA

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

** See curve for I_{CC} vs. temp.

† These are absolute voltages with respect to GND (Pin 8 or 9) and includes all overshoots due to test equipment.

†† Care should be taken to minimize as much as possible the DC and capacitive load on IR and OR when operating at frequencies above 25 MHz.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. Master reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided the upstream stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

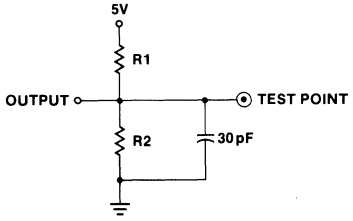
AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 60 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input-Ready combination, as well as the Shift-Out-Output-Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to shift-in going HIGH. This same type of situation occurs with T_{ORL} and T_{ORH} as related to Shift-Out. Data outputs driving a bus should be limited to 10 MHz frequency. For high-speed applications, proper grounding technique is essential.

Switching Characteristics Over Operating Conditions (continued)

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
t_{IPH}	Input ready pulse HIGH	4	5	12		ns
t_{OPH}	Output ready pulse HIGH	8	5	12		ns
t_{ORD}	Ouput ready ↑ to Data Valid	5			18	ns

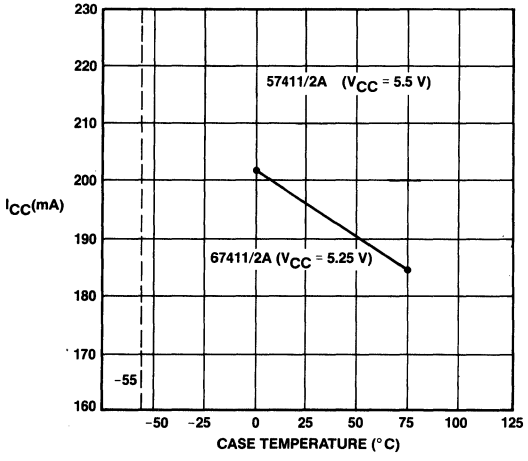
Standard Test Load



Input Pulse Amplitude = 3 V
Input Rise and Fall Time (10%-90%) = 2.5 ns
Measurements made at 1.5 V

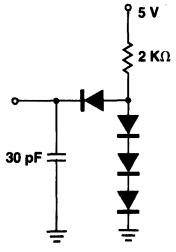
I_{OL}	R1	R2
24 mA	200 Ω	300 Ω
8 mA	600 Ω	1200 Ω

Typical I_{CC} vs Temperature (V_{CC} + MAX)



Test Load

Design Test Load (35 MHz)



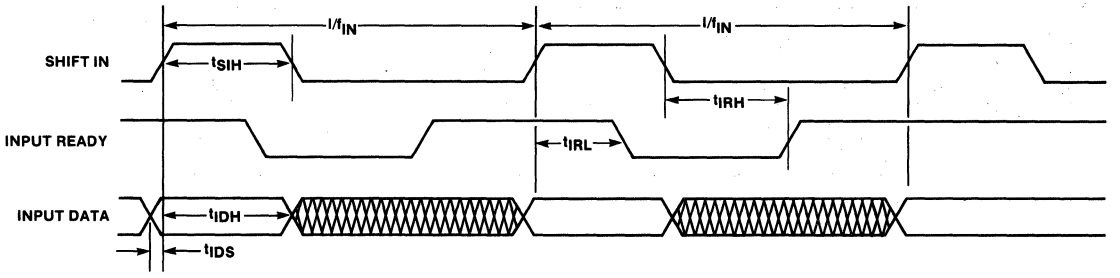


Figure 1. Input Timing

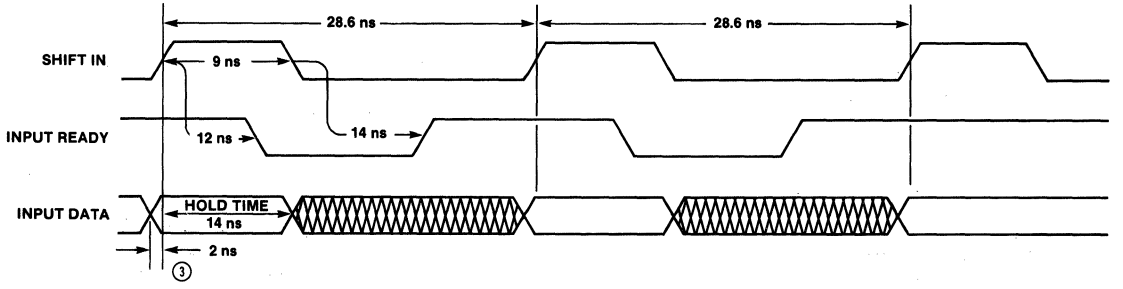


Figure 2. Typical Waveforms for 35 MHz Shift-In Data Rate

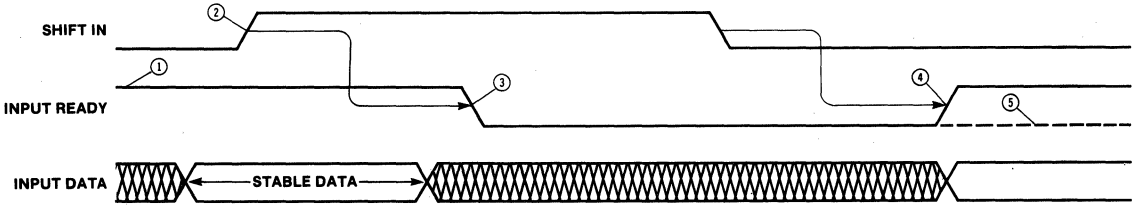


Figure 3. The Mechanism of Shifting Data into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
(2) Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.
(3) Input Ready goes LOW indicating the first word is full.
(4) Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.
(5) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.
NOTE: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

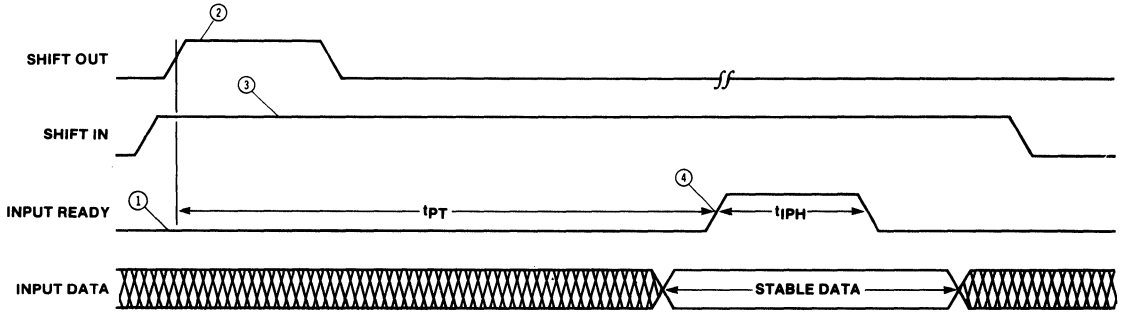


Figure 4. Data is Shifted In Whenever Shift In and Input Ready are Both HIGH

① FIFO is initially full.

② Shift Out pulse is applied. An empty location starts "bubbling" to the front.

③ Shift In is held HIGH

④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

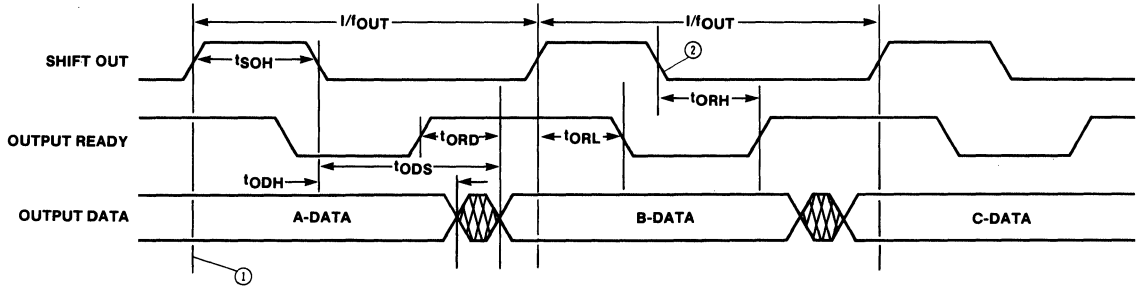


Figure 5. Output Timing

① The diagram assumes that at this time, words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.

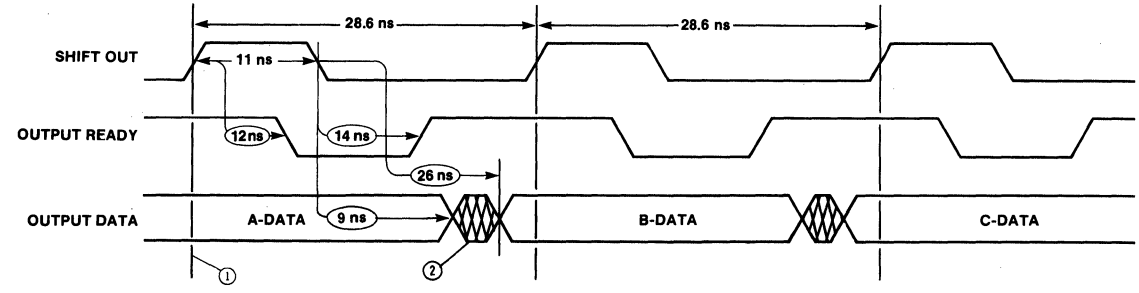


Figure 6. Typical Waveforms for 35 MHz Shift-Out Data Rate

① The diagram assumes that at this time words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Data in the first crosshatched region may be A or B Data.

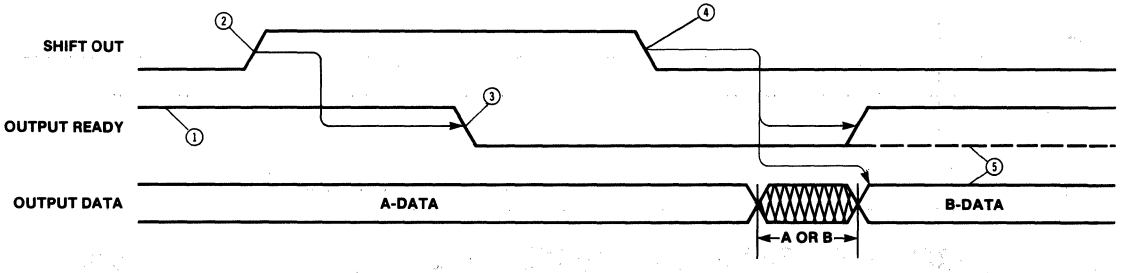


Figure 7. The Mechanism of Shifting Data Out of the FIFO

① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.

② Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.

③ Output Ready goes LOW.

④ Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.

⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

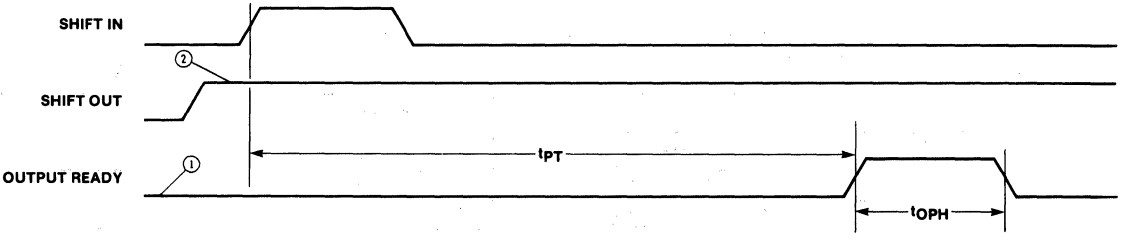


Figure 8. t_{PT} and t_{OPH} Specification

① FIFO initially empty.

② Shift Out held HIGH

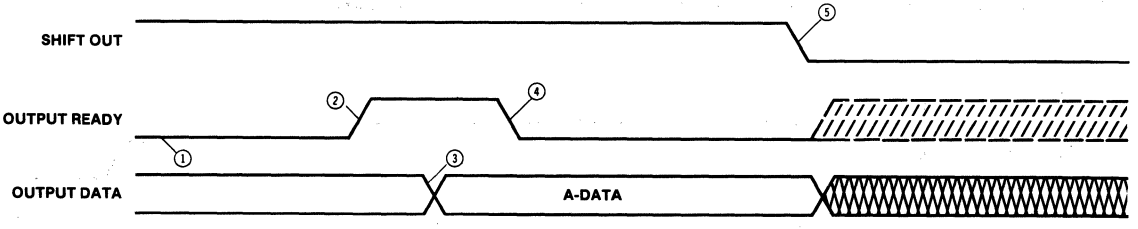


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

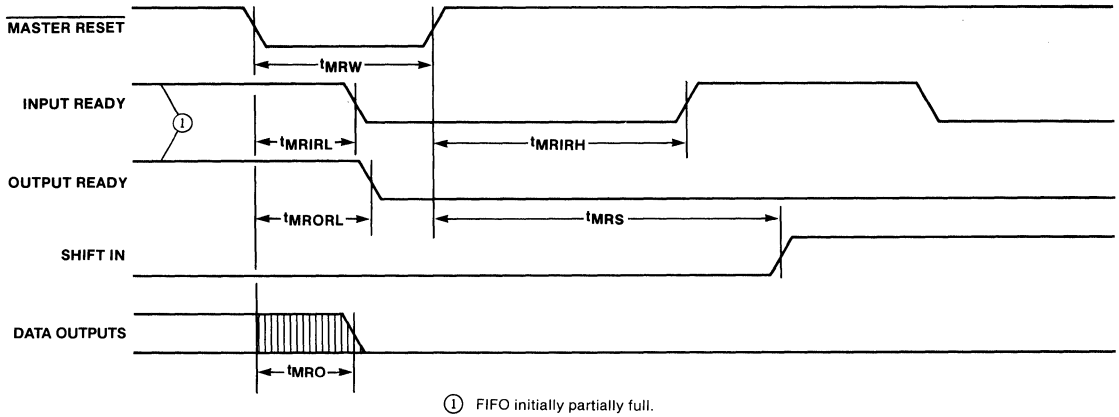
① Word 63 is empty.

② Output Ready goes HIGH indicating arrival of the new data.

③ New data (A) arrives at the outputs (word 63).

④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.

⑤ As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.



① FIFO initially partially full.

Figure 10. Master Reset Timing

First-In First-Out (FIFO) 64x5 Memory 35 MHz (Standalone)

67413A 67413

Features/Benefits

- **High-speed 35 MHz shift-in/shift-out rates**
- **High-drive capability**
- **Three-state outputs**
- **Half-full and Almost-full/Empty status flags**
- **Structured pinouts. Output pins directly opposite corresponding input pins.**
- **Asynchronous operation**
- **TTL-compatible inputs and outputs**

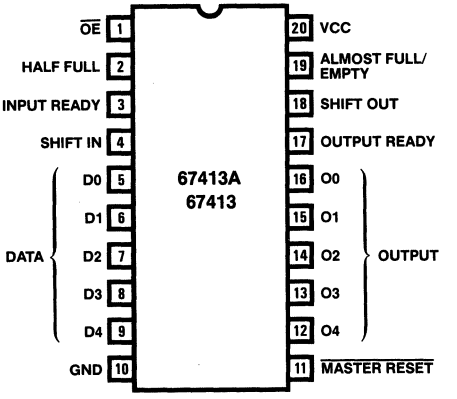
Description

The 67413A is a high-speed, 64x5 First-In-First-Out (FIFO) memory which operates at 35-MHz input/output rates (67413 operates at 25-MHz in-out). The data is loaded and emptied on a first-in-first-out basis. It is a three-state device with high-drive (I_{OL} = 24 mA) data outputs. These devices can be connected in parallel to give FIFOs of any word length. It has a Half-full flag (thirty-two or more words full) and an almost full/empty flag (fifty-six or more words or eight or less words). The main applications of 67413A, 67413 are rate buffers; sourcing and absorbing data at different rates. Other applications are high-speed tape and disk controllers, data communications systems and plotter control systems.

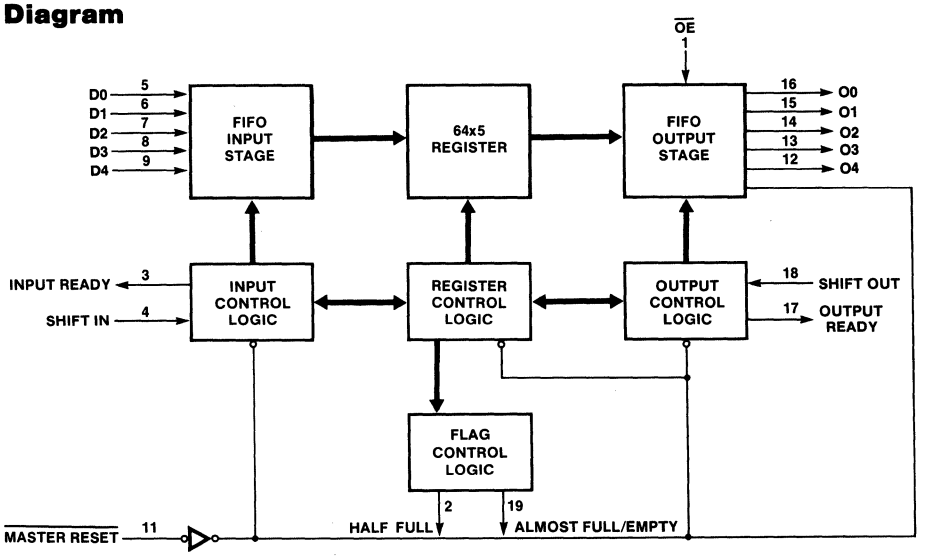
Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
67413A	J	Com	35 MHz-in/out
67413	J	Com	25 MHz-in/out

Pin Configuration



Block Diagram



Publication #	Rev.	Amendment
10678	A	/0

Issue Date: May 1988

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 to 7 V
Input voltage ..... -1.5 to 7 V
Off-state output voltage ..... -0.5 to 5.5 V
Storage temperature ..... -65°C to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	67413A MIN	67413A TYP	67413A MAX	67413 MIN	67413 TYP	67413 MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	4.75	5	5.25	V
T_A	Operating free-air temperatue		0		75	0		75	°C
t_{SIH}†	Shift in HIGH time	1	9			16			ns
t_{SIL}†	Shift in LOW time	1	17			20			ns
t_{IDS}	Input data setup	1	2			3			ns
t_{IDH}	Input data hold time	1	15			25			ns
t_{SOH}†	Shift Out HIGH time	5	9			16			ns
t_{SOL}	Shift Out LOW time	5	17			20			ns
t_{MRW}†	Master Reset pulse	10	30			35			ns
t_{MRS}	Master Reset to SI	10	35			35			ns

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	67413A MIN	67413A TYP	67413A MAX	67413 MIN	67413 TYP	67413 MAX	UNIT
f_{IN}	Shift in rate	1	DC DC		††30 †††35	DC		25	MHz
t_{IRL}†	Shift In ↑ to Input Ready LOW	1		12	18		12	28	ns
t_{IRH}†	Shift In ↓ to Input Ready HIGH	1		14	20		14	25	ns
f_{OUT}	Shift Out rate	5	DC DC		††30 †††35	DC		25	MHz
t_{ORL}†	Shift Out ↑ to Output Ready LOW	5		12	18		12	28	ns
t_{ORH}†	Shift Out † to Output Ready HIGH	5		14	20		14	25	ns
t_{ODH}†	Output Data Hold (previous word)	5	12				10		ns
t_{ODS}	Output Data Shift (next word)	5			34			40	ns
t_{PT}	Data throughput or "fall through"	4, 8		510	650		510	750	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	10		18	28		18	30	ns
t_{MRIRH}	Master Reset ↑ to Input Ready HIGH	10		21	28		21	30	ns
t_{MRIRL}	Master Reset ↓ Input Ready LOW*	10		18	28		18	30	ns
t_{MRO}*	Master Reset ↓ to Outputs LOW	10		32	45		32	55	ns

Note: Typicals at 5 V V_{CC} and 25°C T_A.

* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.

† See AC test and high-speed application note.

†† Tested

††† Guaranteed by design (see test load).

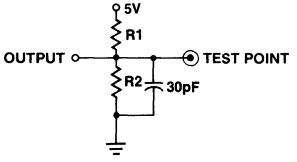
Switching Characteristics Over Operating Conditions (continued)

SYMBOL	PARAMETER	FIGURE	67413A MIN	67413A TYP	67413A MAX	67413 MIN	67413 TYP	67413 MAX	UNIT
t_{IPH}	Input ready pulse HIGH	4	5	12		5	12		ns
t_{OPH}	Output ready pulse HIGH	8	5	12		5	12		ns
t_{ORD}	Output ready ↑ HIGH to Data Valid	5			18			20	ns
t_{AEH}*	Shift Out ↑ to AF/E HIGH	11		100	135		100	145	ns
t_{AEL}*	Shift In ↑ to AF/E LOW	11		450	600		450	650	ns
t_{AFL}*	Shift Out ↑ to AF/E LOW	12		450	600		450	650	ns
t_{AFH}*	Shift In ↑ AF/E HIGH	12		100	135		100	145	ns
t_{HFH}*	Shift In ↑ to HF HIGH	13		280	360		280	380	ns
t_{HFL}*	Shift Out ↑ to HF LOW	13		280	360		280	380	ns
t_{PHZ}	Output Disable Delay	A		14	25		14	30	ns
t_{PLZ}		A		14	25		14	30	
t_{PZL}	Output Enable Delay	A		14	25		14	30	ns
t_{PZH}		A		24	38		24	50	

Note: Input rise and fall time (10%-90%) = 2.5 ns. * See timing diagram for explanation of parameters.

67413A/67413

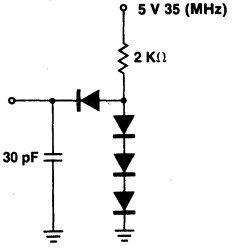
Standard Test Load



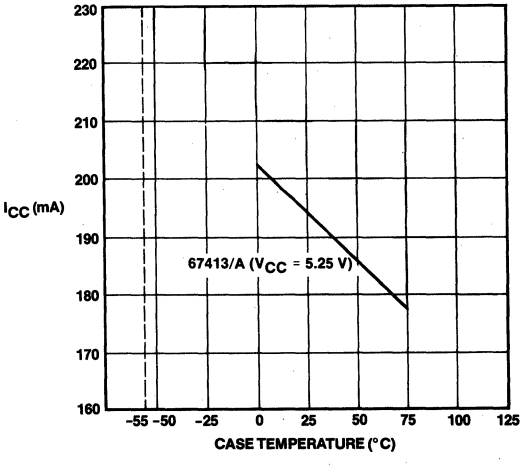
I_{OL}	R1	R2
24 mA	200 Ω	300 Ω
8 mA	600 Ω	1200 Ω

Input Pulse Amplitude = 3V
Input Rise and Fall Time (10%–90%) = 2.5 ns
Measurements made at 1.5 V

Design Test Load



Typical I_{CC} vs Temperature (V_{CC} = MAX)



67413 Switching Characteristics Over Operating Conditions (continued)

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{IPH}	Input ready pulse HIGH	4	5	12		ns
t_{OPH}	Output ready pulse HIGH	8	5	12		ns
t_{ORD}	Output ready ↑ HIGH to Data Valid	5			20	ns
t_{AEH}*	Shift Out ↑ to AF/E HIGH	11		100	145	ns
t_{AEL}*	Shift In ↑ to AF/E LOW	11		450	650	ns
t_{AFL}*	Shift Out ↑ to AF/E LOW	12		450	650	ns
t_{AFH}*	Shift In ↑ to AF/E HIGH	12		100	145	ns
t_{HFH}*	Shift In ↑ to HF HIGH	13		280	380	ns
t_{HFL}*	Shift Out ↑ to HF LOW	13		280	380	ns
t_{PHZ}	Output Disable Delay	A		14	30	ns
t_{PLZ}		A		14	30	ns
t_{PZL}	Output Enable Delay	A		14	30	ns
t_{PZH}		A		24	50	ns

Note: Input rise and fall time (10%-90%) = 2.5 ns.

* See timing diagram for explanation of parameters.

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150°C

67413 Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	16			ns
t_{SIL}†	Shift in LOW time	1	20			ns
t_{IDS}	Input data set up	1	3			ns
t_{IDH}	Input data hold time	1	25			ns
t_{SOH}†	Shift Out HIGH time	5	16			ns
t_{SOL}	Shift Out LOW time	5	20			ns
t_{MRW}	Master Reset pulse †	10	35			ns
t_{MRS}	Master Reset to SI	10	35			ns

67413 Switching Characteristics Over Temperature Range

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
f_{IN}	Shift in rate	1	DC		25	MHz
t_{IRL}†	Shift In ↑ to Input Ready LOW	1		12	28	ns
t_{IRH}†	Shift In ↓ to Input Ready HIGH	1		14	25	ns
f_{OUT}	Shift Out rate	5	DC		25	MHz
t_{ORL}†	Shift Out ↑ to Output Ready LOW	5		12	28	ns
t_{ORH}†	Shift Out ↓ to Output Ready HIGH	5		14	25	ns
t_{ODH}†	Output Data Hold (previous word)	5	10			ns
t_{ODS}	Output Data Shift (next word)	5			40	ns
t_{PT}	Data throughput or "fall through"	4,8		510	750	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	10		18	30	ns
t_{MRIRH}	Master Reset ↑ to Input Ready HIGH	10		21	30	ns
t_{MRIRL}	Master Reset ↓ Input Ready LOW*	10		18	30	ns
t_{MRO}	Master Reset ↓ to Outputs LOW	10		32	55	ns

Note: Typicals at 5 V V_{CC} and 25°C T_A.

* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.

† See AC test and high-speed application note.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION				MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage							0.8†	V
V_{IH}	High-level input voltage					2†			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA					−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45 V					−250	μA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V					50	μA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V					1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} (Data outputs)	67413A 67413	24 mA			0.5	V
			I_{OL} (IR, OR)	67413A 67413	8 mA††				
			I_{OL} (Flag outputs)	67413A 67413	8 mA				
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} (Data outputs)	67413A 67413	−3.0 mA	2.4			V
			I_{OH} (IR,OR)		−0.9 mA				
			I_{OH} (Flag outputs)		−0.9 mA				
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0 V			−20		−90	mA
I_{HZ}	Off-state output current	V_{CC} = MAX	V_O = 2.4 V					+20	μA
I_{LZ}		V_{CC} = MAX	V_O = 0.4 V					−20	μA
I_{CC}	Supply current	V_{CC} = MAX. All inputs low. All outputs open. (67413A/67413)						**240	mA

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

** See curve for I_{CC} vs. temp.

† There are absolute voltages with respect to GND (PIN 8 or 9) and includes all overshoots due to test equipment.

†† Care should be taken to minimize as much as possible the DC and capacitive load on IR and OR when operating at frequencies above 25 MHz.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Figure 10) to prepare the FIFO to accept data in the first location. Master Reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data in any full cell to the adjacent (downstream) empty cell is automatically activated by an on-chip control. Thus data will stack up at the end of the device (while empty locations will "bubble" to the front when data is shifted out). t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that there is valid upstream data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 60 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition,

care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a funcitonal standpoint, and will also cause the "effective" timing of Input Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to Shift-ingoing HIGH. This same type of problem is also related to T_{IRH}, T_{ORL} and T_{ORH} as related to Shift-Out. Data outputs driving a bus should be limited to 10 MHz frequency. For high-speed applications, proper grounding technique is essential.

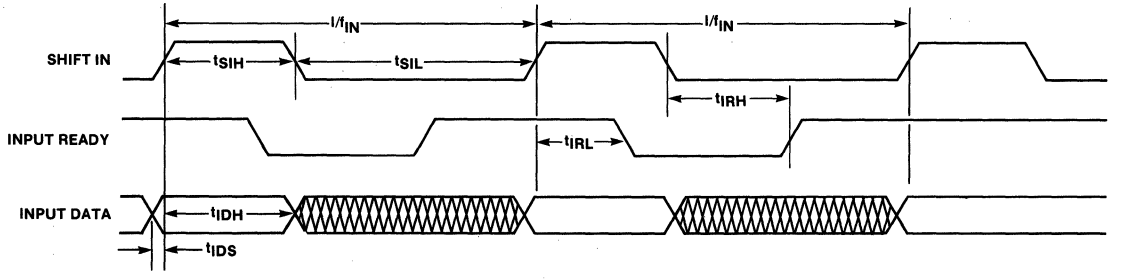


Figure 1. Input Timing

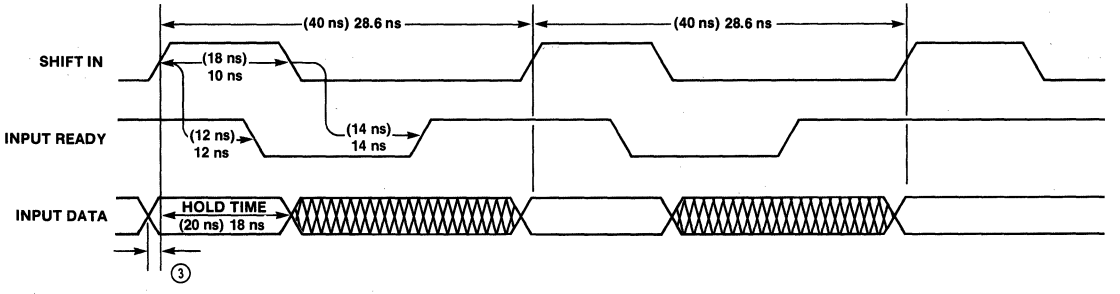


Figure 2. Typical Waveforms for 35 MHz Shift-In Data Rate (67413A)

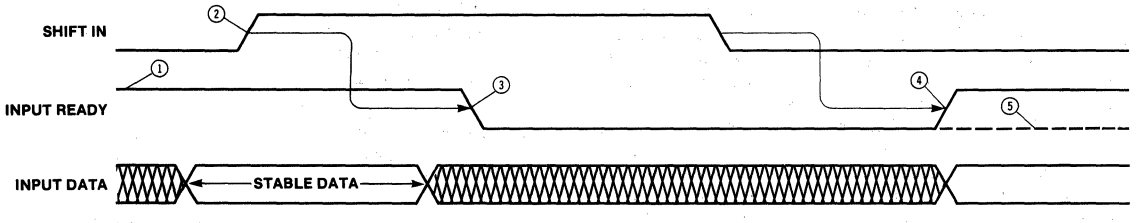


Figure 3. The Mechanism of Shifting Data into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
(2) Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.
(3) Input Ready goes LOW indicating the first word is full.
(4) Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.
5. If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.
Note: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

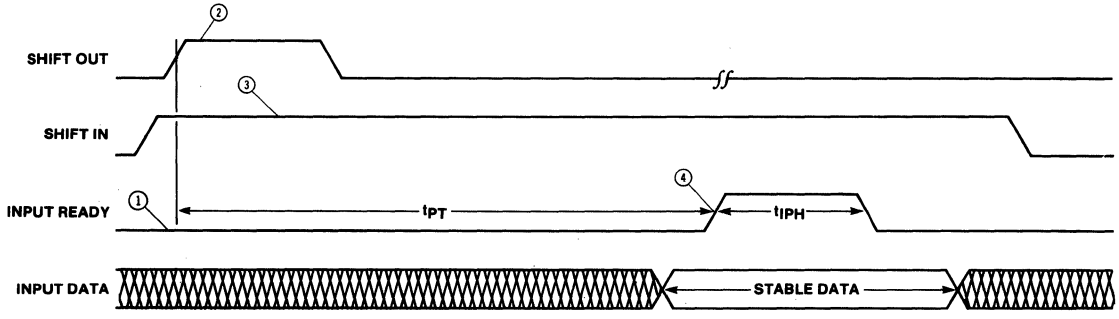


Figure 4. Data Is Shifted In Whenever Shift In and Input Ready are Both HIGH

① FIFO is initially full.

② Shift Out pulse is applied. An empty location starts "bubbling" to the front.

③ Shift In is held HIGH

④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

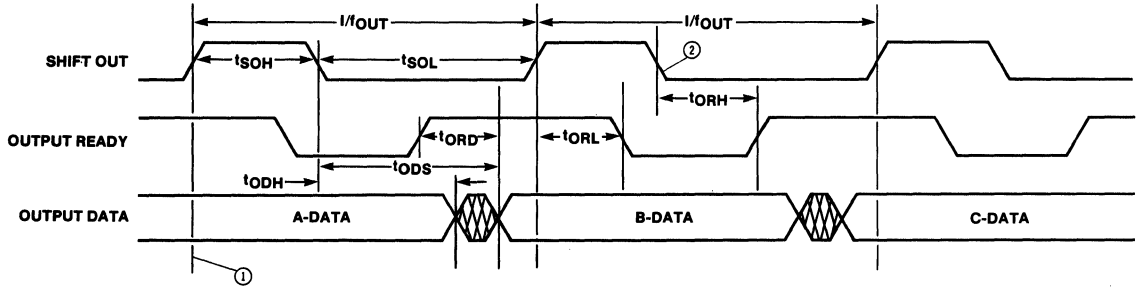


Figure 5. Output Timing

① The diagram assumes that at this time, words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e. OR and SO are both high together.

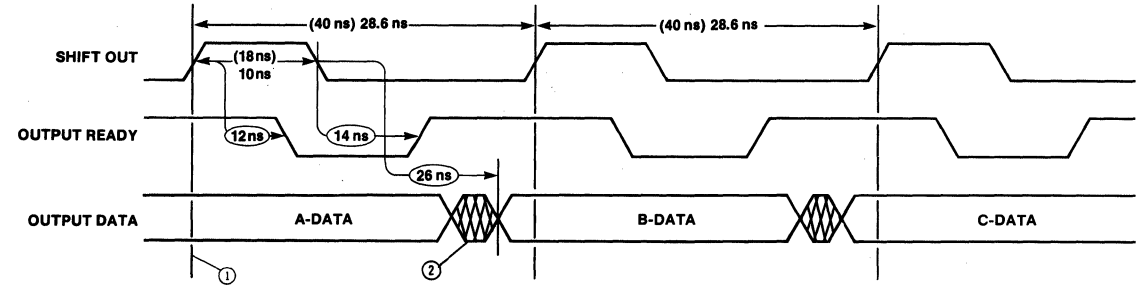


Figure 6. Typical Waveforms for 35 MHz Shift-Out Data Rate (67413A)

① The diagram assumes that at this time words 63, 62 and 61 are loaded with A, B and C Data, respectively.

② Data in the first crosshatched region may be A or B Data.

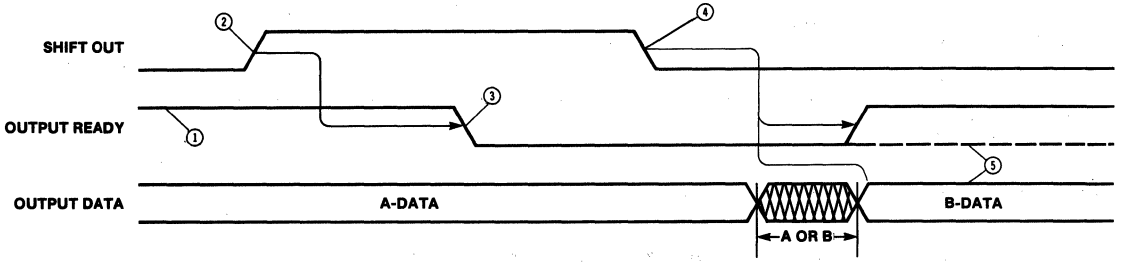


Figure 7. The Mechanism of Shifting Data Out of the FIFO

① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.

② Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.

③ Output Ready goes LOW.

④ Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.

⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

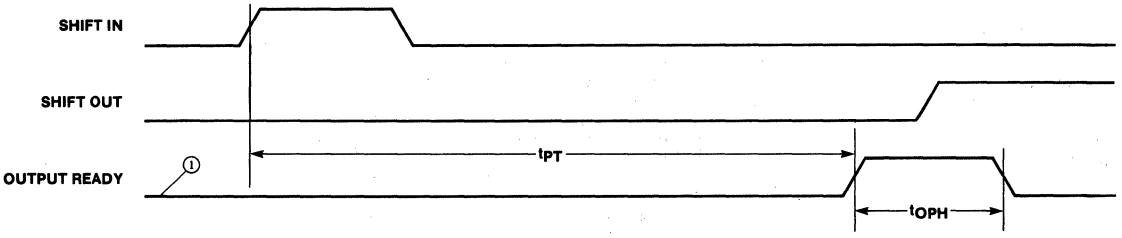


Figure 8. t_{PT} and t_{OPH} Specification

① FIFO initially empty.

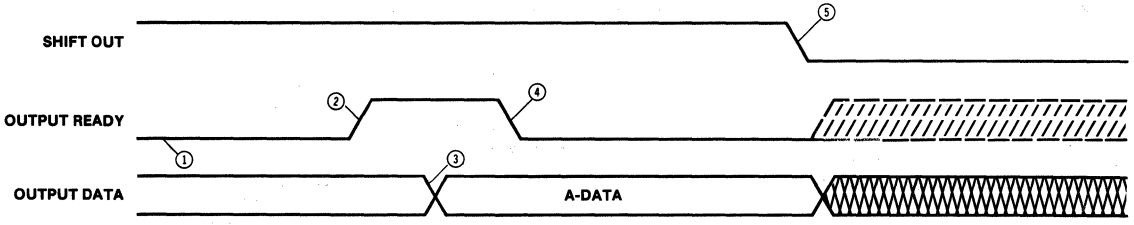


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH

① Word 63 is empty.

② Output Ready goes HIGH indicating arrival of the new data.

③ New data (A) arrives at the outputs (word 63).

④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.

⑤ As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.

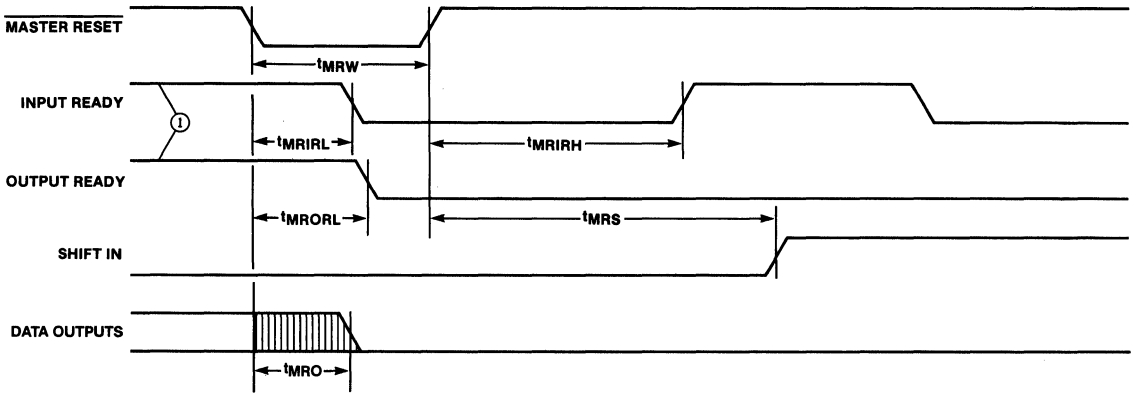


Figure 10. Master Reset Timing

① FIFO is partially full.

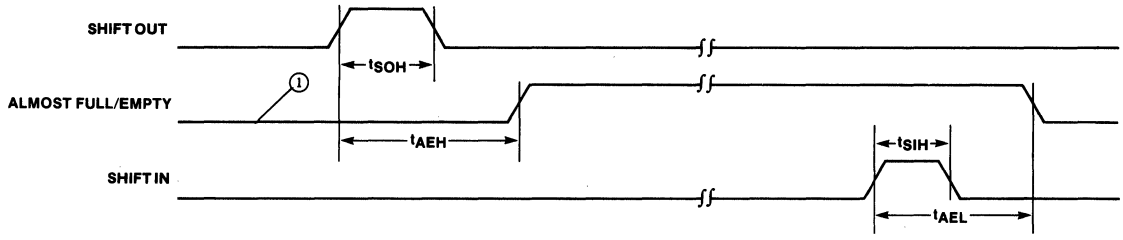


Figure 11. t_{AEH}, t_{AEL} Specifications

① FIFO contains 9 words (one more than almost empty).

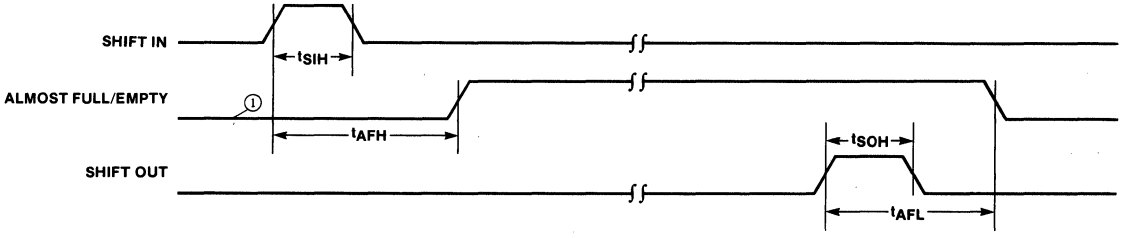


Figure 12. t_{AFH}, t_{AFL} Specifications

① FIFO contains 55 words (one short of almost full)

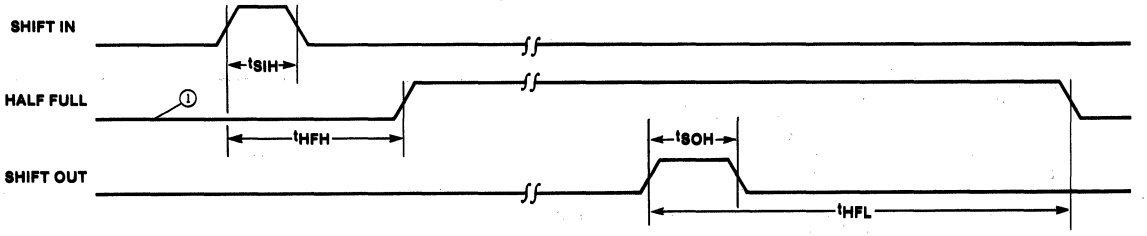


Figure 13. t_{HFL}, t_{HFH} Specifications

① FIFO contains 31 words (one short of half full).

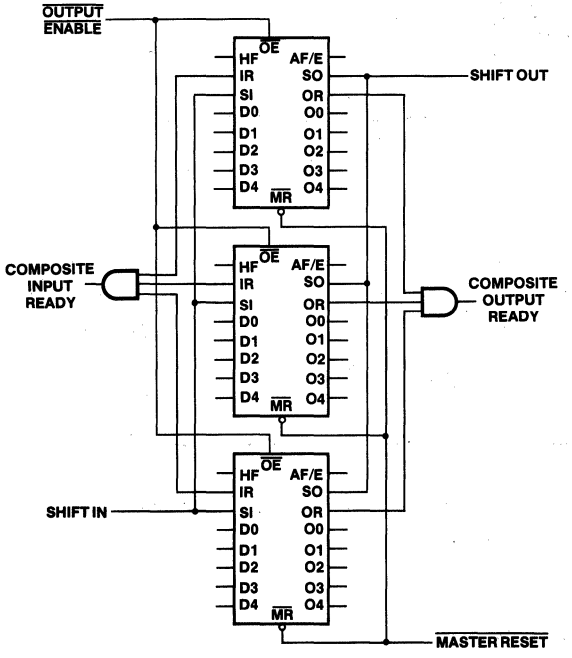


Figure 14. 64x15 FIFO with 67413A/67413

FIFOs are expandable in width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This requirement is due to the different fall through times of the FIFOs.

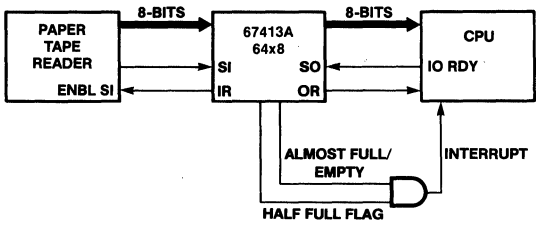
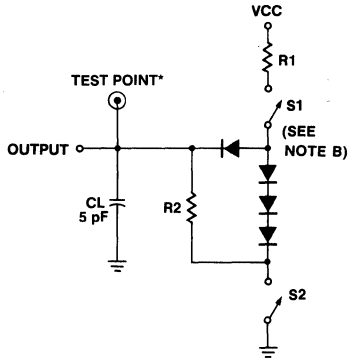


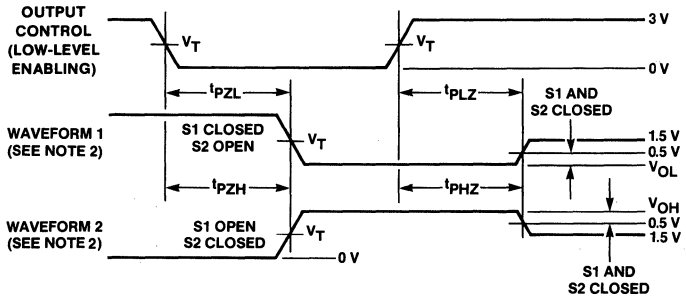
Figure 15. Application for 67413A "Slow and Steady Rate to Fast 'Blocked Rate' "

Note: Cascading the FIFO's in word width is done by ANDing the IR and OR as shown in Figure 14.

Three-State Test Load



Design Test Load



Enable and Disable

Notes: A. All diodes are 1N916 or 1N3064.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

D. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

First-In First-Out (FIFO) 64x4, 64x5 Memory 10/15 MHz (Cascadable) CMOS

67C401/13 67C402/23

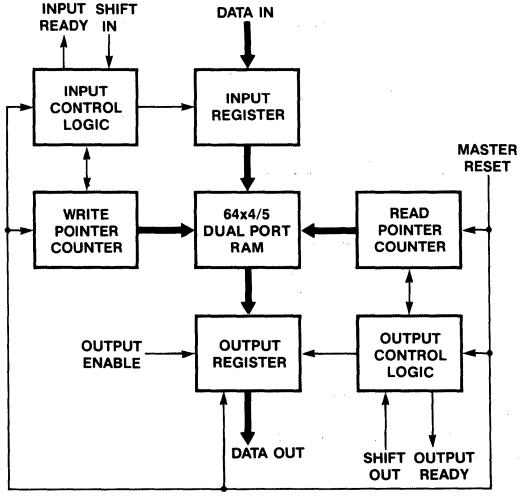
Features

- Zero standby power
- High-speed 15-MHz shift-in/shift-out rates
- Very low active power consumption
- TTL-compatible inputs and outputs
- Readily expandable in word width and depth
- RAM-based architecture for short fall-through delay
- Full CMOS 8-transistor cell for maximum noise immunity
- Asynchronous operation
- Output Enable feature (67C4013/23)

General Description

The 67C40X/XX series devices are high-performance CMOS RAM-based First-In First-Out (FIFO) buffer memory products organized as 64 words by 4 or by 5 bits wide. These devices use Monolithic Memories' latest CMOS process technology and meet the demands for high-speed, low-power operation. By utilizing an on-chip, dual-port RAM, a very short fall-through time is realized, thus improving overall system performance. By using both Read and Write pointers for addressing each memory location, the data can propagate to the outputs in much less time than in traditional register-based FIFOs. These FIFOs are easily integrated into many applications and perform particularly well for high-speed disc controllers, graphics, and communication network systems. The 550-μwatt standby power specification makes these devices ideal for ultra-low-power and battery-powered systems.

Block Diagram

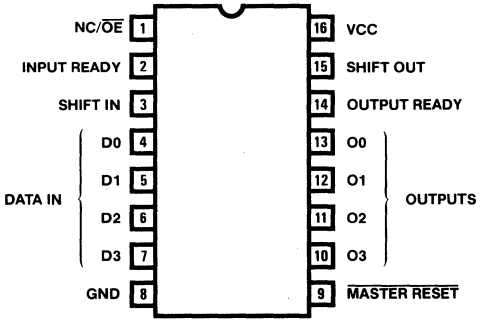


Ordering Information

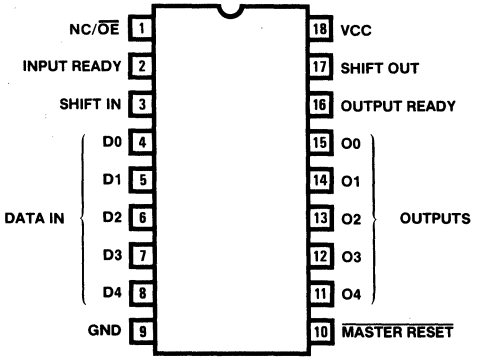
PART NUMBER	PKG	TEMP	OUTPUT	DESCRIPTION
67C401-10	N,J,NL	Com	Totem Pole	10 MHz 64x4
67C401-15	N,J,NL	Com	Totem Pole	15 MHz 64x4
67C4013-10	N,J,NL	Com	3-State	10 MHz 64x4
67C4013-15	N,J,NL	Com	3-State	15 MHz 64x4
67C402-10	N,J,NL	Com	Totem Pole	10 MHz 64x5
67C402-15	N,J,NL	Com	Totem Pole	15 MHz 64x5
67C4023-10	N,J,NL	Com	3-State	10 MHz 64x5
67C4023-15	N,J,NL	Com	3-State	15 MHz 64x5

Pin Configurations

67C401/13



67C402/23



Publication #	Rev.	Amendment
10683	A	/0

Issue Date: May 1988

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to V_{CC} +0.5 V
Storage temperature ..... -65°C to +150°C
Power dissipation ..... 1.0 W
Latch-up trigger current (all outputs) ..... 140 mA

Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	67C40X/XX-10 MIN	67C40X/XX-10 MAX	67C40X/XX-15 MIN	67C40X/XX-15 MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
T_A	Operating free-air temperature		0	70	0	70	°C
f_{IN}	Shift in rate	1		10		15	MHz
t_{SIH}	Shift in HIGH time	1,B	14		14		ns
t_{SIL}	Shift in LOW time	1	25		25		ns
t_{IDS}	Input data setup to SI (Shift In)	1	0		0		ns
t_{IDH}	Input data hold time from SI (Shift In)	1	40		40		ns
t_{RIDS}	Input data setup to IR (Input Ready)	3	0		0		ns
t_{RIDH}	Input data hold time from IR (Input Ready)	3	30		30		ns
f_{OUT}	Shift out rate	4		10		15	MHz
t_{SOH}	Shift out HIGH time	4,B	24		21		ns
t_{SOL}	Shift out LOW time	4	25		25		ns
t_{MRW}*	Master Reset pulse	8	35		35		ns
t_{MRS}	Master Reset to SI	8	65		65		ns

* See AC test and high-speed application note.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		67C40X/XX-10 MIN	67C40X/XX-10 MAX	67C40X/XX-15 MIN	67C40X/XX-15 MAX	UNIT
V_{IL}*	Low-level input voltage				0.8		0.8	V
V_{IH}*	High-level input voltage			2		2		V
I_{IN}	Input current	V_{CC} = MAX	GND<V_{IN}<V_{CC}	-1	1	-1	1	μA
I_{OZ}	Off-state output current	V_{CC} = MAX	GND<V_{OUT}<V_{CC}	-5	5	-5	5	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 20 μA		0.1		0.1	V
			I_{OL} = 8 mA		0.4		0.4	
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = -20 μA	V_{CC} -0.1		V_{CC} -0.1		V
			I_{OH} = -4 mA	2.4		2.4		
I_{OS}**	Output short-circuit current	V_{CC} = MAX	V_O = 0 V	-90	-20	-90	-20	mA
I_{CC}	Standby supply current	V_{CC} = MAX	V_{IH} = V_{CC} V_{IL} = GND		100		100	μA
	Operating supply current	I_{OUT} = 0	V_{IH} = MIN, V_{IL} = MAX f_{IN} = f_{OUT} = MAX		35		45	mA

* These are absolute voltages with respect to GND (Pin 9) and include all overshoots due to system and/or tester noise.

** Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	67C40X/XX-10 MIN	67C40X/XX-10 MAX	67C40X/XX-15 MIN	67C40X/XX-15 MAX	UNIT
t_{IRL}*	Shift In ↑ to Input Ready LOW	1		60		55	ns
t_{IRH}*	Shift In ↓ to Input Ready HIGH			50		50	ns
t_{ORL}*	Shift Out ↑ to Output Ready LOW	4		55		45	ns
t_{ORH}*	Shift Out ↓ to Output Ready HIGH			50		41	ns
t_{ODH}	Output Data Hold (previous word)		5		5		ns
t_{ODS}	Output Data Shift (next word)			35		30	ns
t_{PT}	Data throughput	3,6		100		90	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	8		100		100	ns
t_{MRIRH}	Master Reset ↓ to Input Ready HIGH			100		100	ns
t_{MRO}	Master Reset ↓ to Outputs LOW			35		35	ns
t_{IPH}	Input ready pulse HIGH	3,B	19		16		ns
t_{OPH}	Output ready pulse HIGH	6,B	14		14		ns
t_{ORD}	Output ready ↑ to Data Valid	4		-3		-3	ns
t_{PHZ}	Output Disable Delay	A		25		25	ns
t_{PLZ}				25		25	
t_{PZL}	Output Enable Delay			30		30	ns
t_{PZH}				30		30	

* See AC test and high-speed application note.

Capacitances*

SYMBOL	PARAMETER	TEST CONDITION	67C40X/XX-10 MIN	67C40X/XX-10 MAX	67C40X/XX-15 MIN	67C40X/XX-15 MAX	UNIT
C_{IN}	Input capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 4.5 V		10		10	pF
C_{OUT}	Output capacitance			7		7	pF

* Not tested in production.

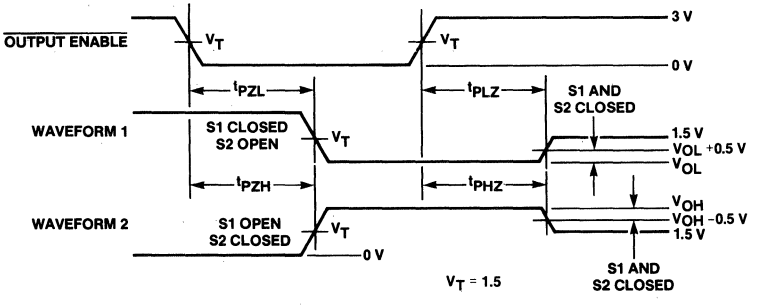
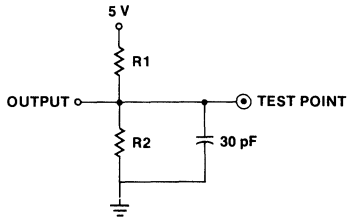


Figure A. Enable and Disable

Waveform 1 is for a data output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for a data output with internal conditions such that the output is high except when disabled by the output control.

Standard AC Test Load

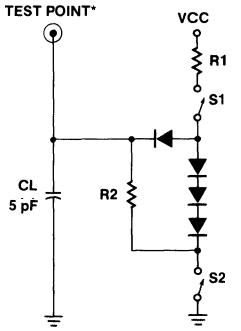


Input Pulse Amplitude = 3 V
Input Rise and Fall Time (10%-90%) = 2.5 ns
Measurements made at 1.5 V
All Diodes are 1N916 or 1N3064

Resistor Values

I_{OL}	R1	R2
8 mA	600 Ω	1200 Ω

Three-State Test Load



Functional Description

Data Input

The FIFO consists of a dual-port RAM and two ring counters for read and write. After power-up, the Master Reset should be pulsed LOW, which internally resets both the read and write counters. When the Input Ready (IR) is HIGH, the FIFO is ready to accept DATA from the D_X inputs. Data then present at the inputs is written into the first location of the RAM when Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. When the SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. The write pointer now points to the next location in the RAM. If the memory is full, then the IR will remain LOW.

Data Output

Data is read from the O_X outputs. Just after the first shift-in, the first data word is available at the outputs, which is indicated by the Output Ready (OR) going HIGH. When the OR is HIGH, data may be shifted out by bringing the Shift-Out (SO) HIGH. A HIGH signal at SO causes the read pointer to point to the next location in the RAM, and also the OR to go LOW. Valid data is maintained while the SO is HIGH. When the SO is brought LOW, the OR goes HIGH, indicating the presence of new valid data. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e., data does not change if the FIFO is empty). A dual-port RAM inside the chip provides the capability of simultaneous and asynchronous writes (Shift-Ins) and reads (Shift-Outs).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading; i.e., rising edge of the Shift-In pulse is not recognized until Input ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to Shift-In going HIGH. This same type of problem is also related to T_{IRH}, T_{ORL}, and T_{ORH} as related to Shift-In and Shift-Out. For high-speed applications, proper grounding technique is essential.

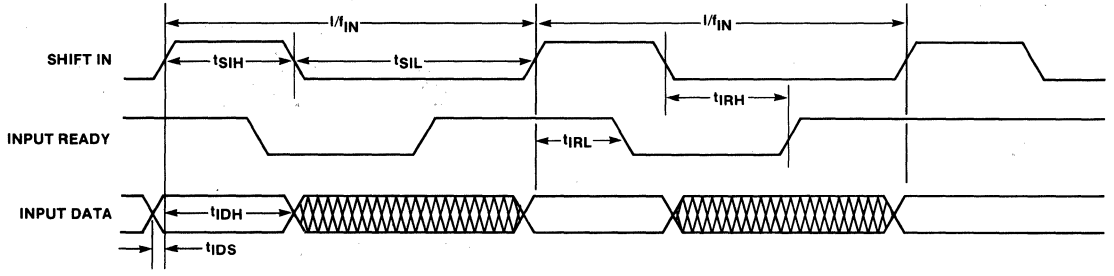


Figure 1. Input Timing

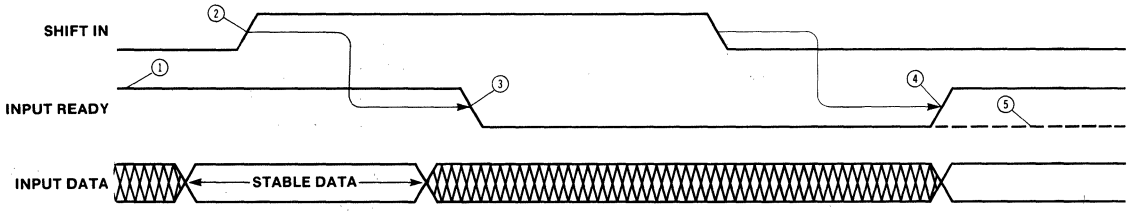


Figure 2. The Mechanism of Shifting Data into the FIFO

① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
② Input Data is loaded into the first available memory location.
③ Input Ready goes LOW indicating this memory location is full.
④ Shift-In going LOW allows Input Ready to sense the status of the next memory location. The next memory location is empty as indicated by Input Ready HIGH.
⑤ If the FIFO is already full then the Input Ready remains low.
Note: Shift-In pulses applied while Input Ready is LOW will be ignored.

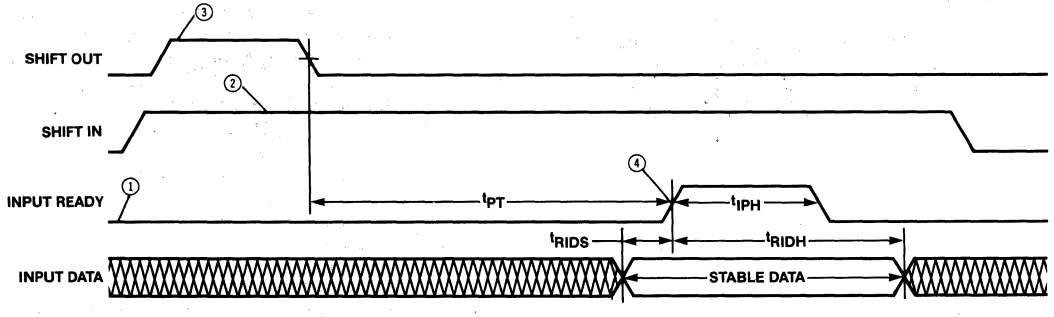


Figure 3. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

① FIFO is initially full.
② Shift In is held HIGH.
③ Shift Out pulse is applied. An empty location is detected by the internal pointers on the falling edge of SO.
④ As soon as Input Ready becomes HIGH the Input Data is loaded into this location.

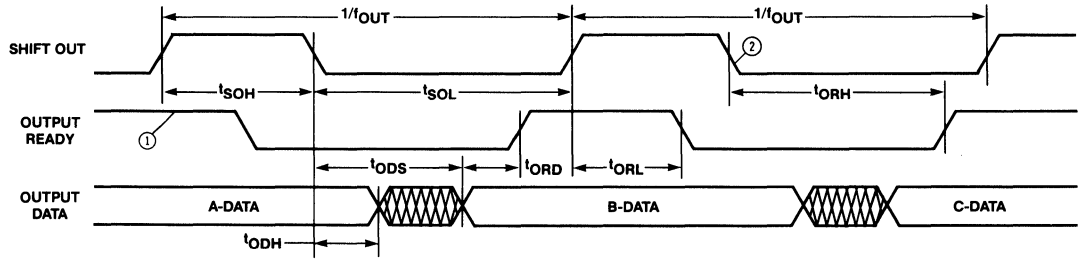


Figure 4. Output Timing

① The diagram assumes that the FIFO contains at least three words: A-Data (first input word), B-Data (second input word), and C-Data (third input word).
② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO are both high together.

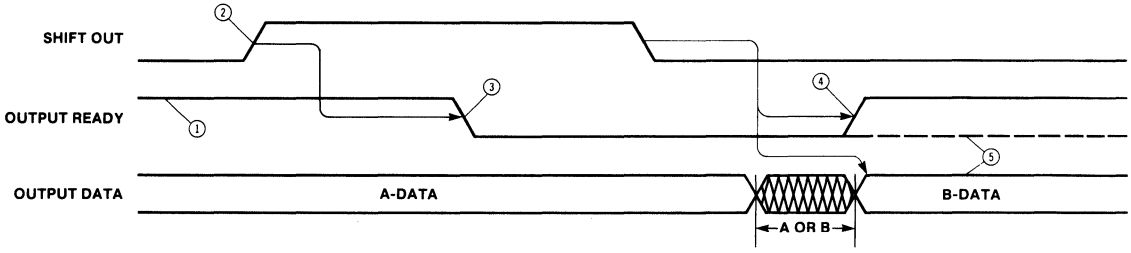


Figure 5. The Mechanism of Shifting Data Out of the FIFO

① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
② Shift-Out goes HIGH causing B-Data (second input word) to advance to the output register. Output data remains as valid A-Data while Shift-Out is HIGH.
③ Output Ready goes LOW.
④ Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data remains the same (A-Data).

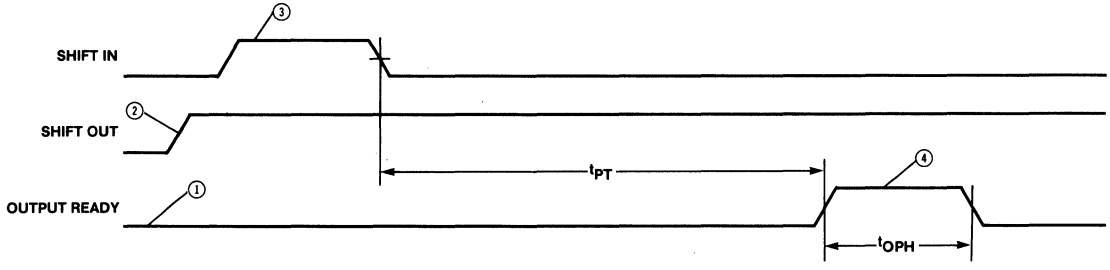


Figure 6. t_{PT} and t_{OPH} Specification

① FIFO initially empty.
② Shift-Out held HIGH.
③ Shift-In pulse applied. A full location is detected by the internal pointers on the falling edge of Shift-In.
④ As soon as Output Ready becomes HIGH, the word is shifted out.

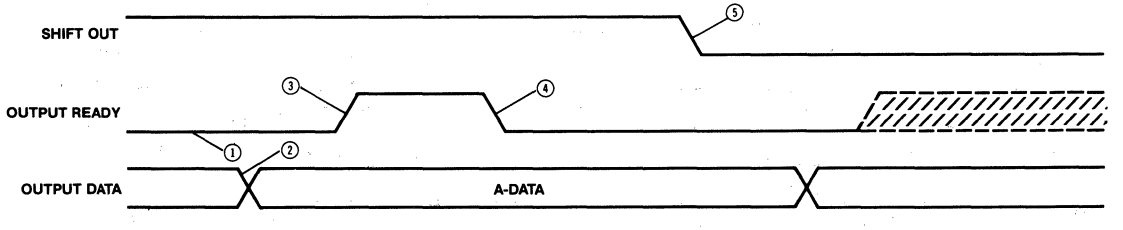


Figure 7. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH

① The internal logic does not detect the presence of any words in the FIFO.
② New data (A) arrives at the outputs.
③ Output Ready goes HIGH indicating arrival of the new data.
④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.
⑤ As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or remain LOW depending on whether there are any additional words in the FIFO.

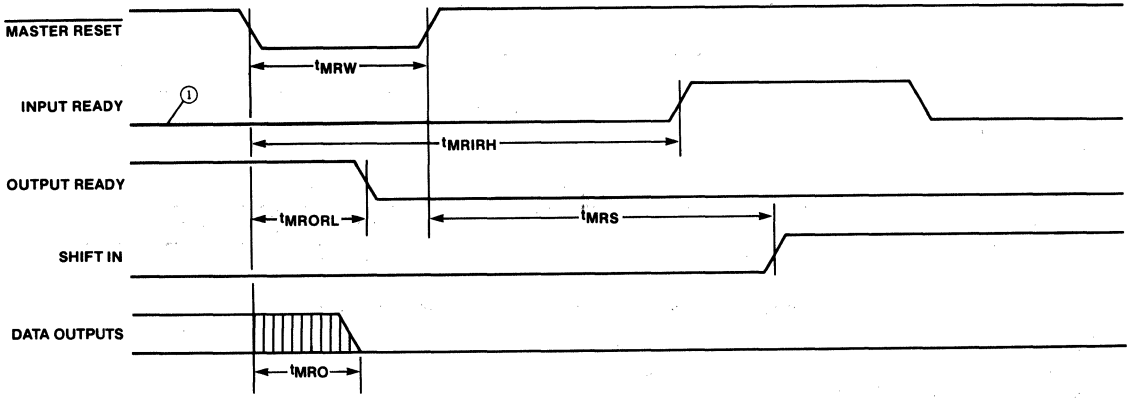
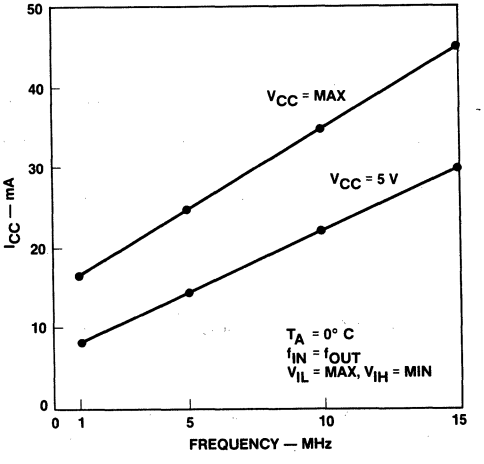


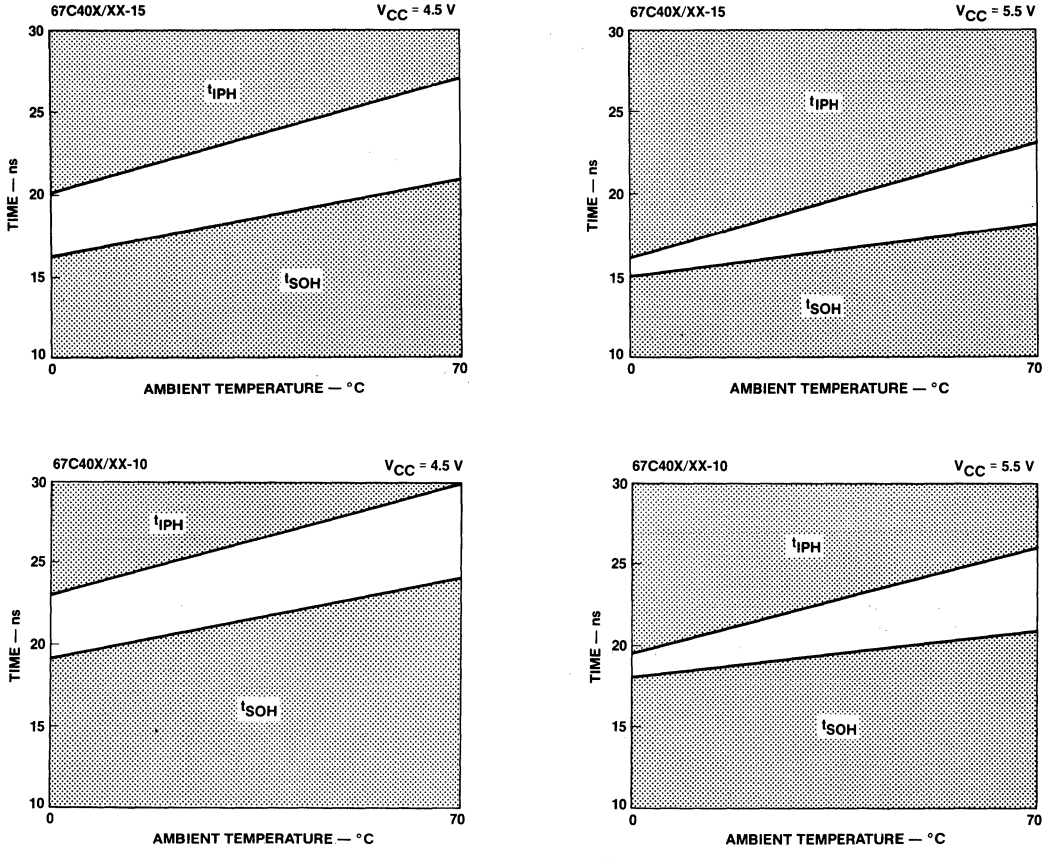
Figure 8. Master Reset Timing

① FIFO is initially full.

I_{CC} vs. Frequency



Guaranteed Distribution of t_{IPH}, t_{SOH} vs. Temperature (For Cascadability Only)



Guaranteed Distribution of t_{OPH}, t_{SIH} vs. Temperature (For Cascadability Only)

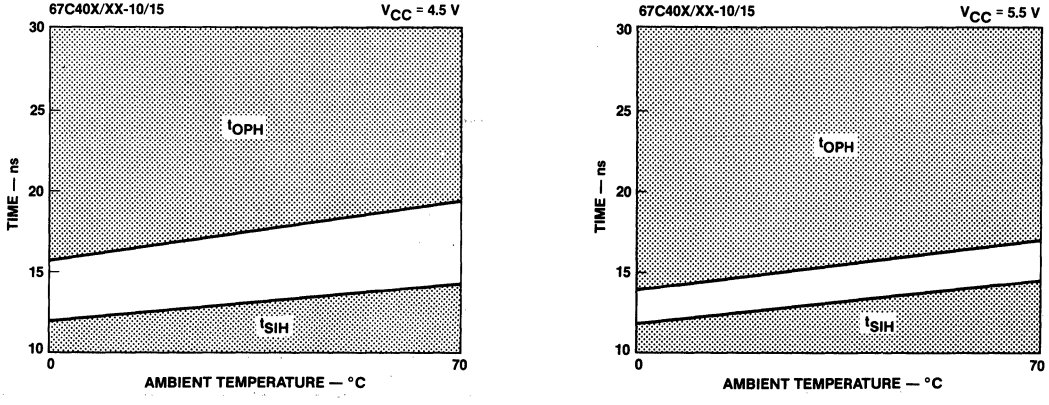


Figure B. Cascadability

First-In First-Out (FIFO) 64x5 Memory 10/15 MHz (Cascadable) CMOS

67C4033

Features

- Zero standby power
- High-speed 15-MHz shift-in/shift-out rates
- Very low active power consumption
- TTL-compatible inputs and outputs
- Readily expandable in word width and depth
- Half-Full and Almost-Full/Empty status flags
- RAM-based architecture for short fall-through delay
- Full CMOS 8-transistor cell for maximum noise immunity
- Asynchronous operation
- Output enable

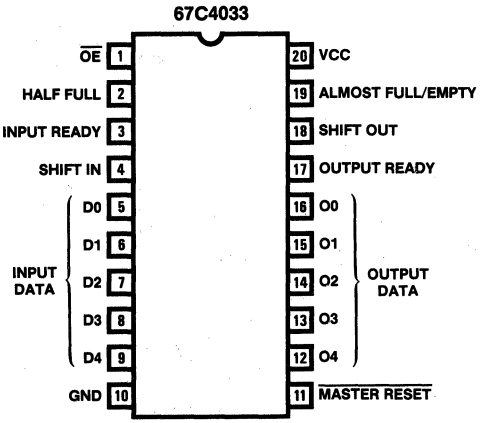
General Description

The 67C4033 device is a high-performance CMOS RAM-based First-In First-Out (FIFO) buffer product organized as 64 words by 5 bits wide. This device uses Monolithic Memories' latest CMOS process technology and meets the demands for high-speed, low-power operation. By utilizing an on-chip, dual-port RAM, a very short fall-through time is realized, thus improving overall system performance. By using Read and Write pointers for addressing each memory location, the data can propagate to the outputs in much less time than in traditional register-based FIFOs. These FIFOs are easily integrated into many applications and perform particularly well for high-speed disk controllers, graphics, and communication network systems. The 550 μwatt standby power specification of this device makes it ideal for ultra-low-power and battery-powered systems.

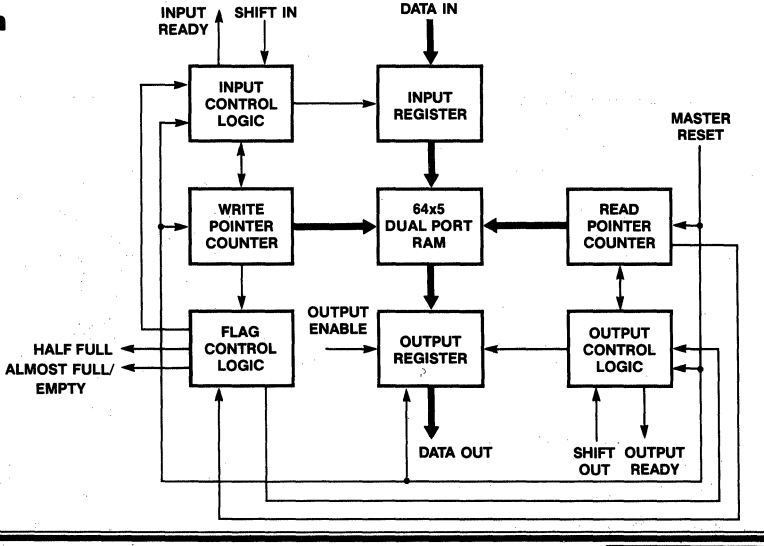
Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
67C4033-10	N,J,NL	Com	10 MHz in/out
67C4033-15	N,J,NL	Com	15 MHz in/out

Pin Configuration



Block Diagram



Publication #	Rev.	Amendment
10684	A	/0

Issue Date: May 1988

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to V_{CC} +0.5 V
Storage temperature ..... -65°C to +150°C
Power dissipation ..... 1.0 W
Latch-up trigger current, all outputs ..... 140 mA

Operating Conditions Over Temperature Range

SYMBOL	PARAMETER	FIGURE	67C4033-10 MIN	67C4033-10 MAX	67C4033-15 MIN	67C4033-15 MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	4.5	5.5	V
T_A	Operating free-air temperature		0	70	0	70	°C
f_{IN}	Shift In rate	1		10		15	MHz
t_{SIH}	Shift in HIGH time	1,B	14		14		ns
t_{SIL}	Shift in LOW time	1	25		25		ns
t_{IDS}	Input data setup to SI (Shift In)	1	0		0		ns
t_{IDH}	Input data hold time from SI (Shift In)	1	40		40		ns
t_{RIDS}	Input data setup to IR (Input Ready)	3	0		0		ns
t_{RIDH}	Input data hold time from IR (Input Ready)	3	30		30		ns
f_{OUT}	Shift Out rate	4		10		15	MHz
t_{SOH}	Shift Out HIGH time	4,B	24		21		ns
t_{SOL}	Shift Out LOW time	4	25		25		ns
t_{MRW}*	Master Reset pulse	8	35		35		ns
t_{MRS}	Master Reset to SI	8	65		65		ns

* See AC test and high-speed application note.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		67C4033-10 MIN	67C4033-10 MAX	67C4033-15 MIN	67C4033-15 MAX	UNIT
V_{IL}*	Low-level input voltage				0.8		0.8	V
V_{IH}*	High-level input voltage			2		2		V
I_{IN}	Input current	V_{CC} = MAX	GND<V_{IN} <V_{CC}	-1	1	-1	1	μA
I_{OZ}	Off-state output current	V_{CC} = MAX	GND<V_{OUT} <V_{CC}	-5	5	-5	5	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 20 μA		0.1		0.1	V
			I_{OL} = 8 mA		0.4		0.4	
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = -20 μA	V_{CC} -0.1		V_{CC} -0.1		V
			I_{OH} = -4 mA	2.4		2.4		
I_{OS}**	Output short-circuit current	V_{CC} = MAX	V_O = 0 V	-90	-20	-90	-20	mA
I_{CC}	Standby supply current	V_{CC} = MAX, I_{OUT} = 0	V_{IH} = V_{CC}, V_{IL} = GND		100		100	μA
	Operating supply current		V_{IH} = MIN, V_{IL} = MAX, f_{IN} = f_{OUT} = MAX		35		45	mA

* These are absolute voltages with respect to GND (Pin 10) and include all overshoots due to system and/or tester noise.

** Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	67C4033-10 MIN	67C4033-10 MAX	67C4033-15 MIN	67C4033-15 MAX	UNIT
t_{IRL}*	Shift In ↑ to Input Ready LOW	1		60		55	ns
t_{IRH}*	Shift In ↓ to Input Ready HIGH			50		50	ns
t_{ORL}*	Shift Out ↑ to Output Ready LOW	4		55		45	ns
t_{ORH}*	Shift Out ↓ to Output Ready HIGH			50		41	ns
t_{ODH}	Output Data Hold (previous word)		5		5		ns
t_{ODS}	Output Data Shift (next word)			35		30	ns
t_{PT}	Data throughput	3,6		100		90	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	8		100		100	ns
t_{MRIRH}	Master Reset ↓ to Input Ready HIGH			100		100	ns
t_{MRO}	Master Reset ↓ to Ouputs LOW			35		35	ns
t_{MRHFL}	Master Reset ↓ to Half-Full Flag LOW	9		100		100	ns
t_{MRAEH}	Master Reset ↓ to Almost Empty Flag HIGH			100		100	ns
t_{IPH}	Input ready pulse HIGH	3,B	19		16		ns
t_{OPH}	Output ready pulse HIGH	6,B	14		14		ns
t_{ORD}	Output ready ↑ to Data Valid	4		-3		-3	ns
t_{AEH}	Shift Out ↑ to AF/E HIGH	10		110		110	ns
t_{AEL}	Shift In ↑ to AF/E LOW			110		110	ns
t_{AFL}	Shift Out ↑ to AF/E LOW	11		110		110	ns
t_{AFH}	Shift In ↑ to AF/E HIGH			110		110	ns
t_{HFH}	Shift In ↑ to HF HIGH	12		110		110	ns
t_{HFL}	Shift Out ↑ to HF LOW			110		110	ns
t_{PHZ}	Output Disable Delay	A		25		25	ns
t_{PLZ}				25		25	
t_{PZL}	Output Enable Delay			30		30	ns
t_{PZH}				30		30	

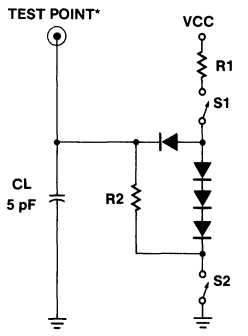
* See timing diagram for explanation of parameters.

Capacitances*

SYMBOL	PARAMETER	TEST CONDITION	67C4033-XX MIN	67C4033-XX MAX	UNIT
C_{IN}	Input capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 4.5 V		10	pF
C_{OUT}	Output capacitance			7	pF

* Values not tested in production.

Three-State Test Load



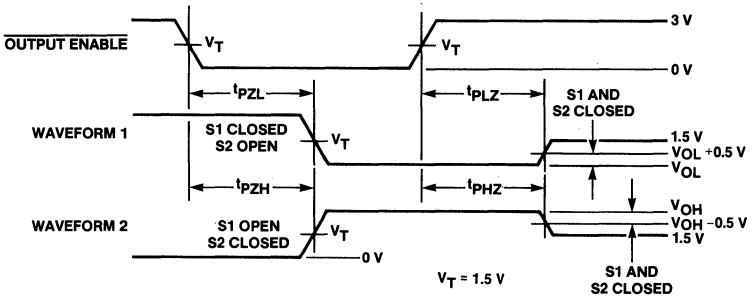
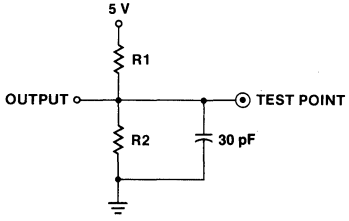


Figure A. Enable and Disable

Standard A.C. Test Load



Input Pulse Amplitude = 3 V
Input Rise and Fall Time (10%-90%) = 2.5 ns
Measurements made at 1.5 V
All Diodes are 1N916 or 1N3064

Waveform 1 is for a data output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for a data output with internal conditions such that the output is high except when disabled by the output control.

Resistor Values

I_{OL}	R1	R2
8 mA	600 Ω	1200 Ω

Functional Description

Data Input

The FIFO consists of a dual-port RAM and two ring counters for read and write. After power-up, the Master Reset should be pulsed LOW, which internally resets both the read and write counters. When the Input Ready (IR) is HIGH, the FIFO is ready to accept DATA from the D_X inputs. Data then present at the inputs is written into the first location of the RAM when Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. When the SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. The write pointer now points to the next location in the RAM. If the memory is full, then the IR will remain LOW.

Data Output

Data is read from the O_X outputs. Just after the first shift-in, the first data word is available at the outputs, which is indicated by the Output Ready (OR) going HIGH. When the OR is HIGH, data may be shifted out by bringing the Shift-Out (SO) HIGH. A HIGH signal at SO causes the read pointer to point to the next location in the RAM, and also the OR to go LOW. Valid data is maintained while the SO is HIGH. When the SO is brought LOW, the OR goes HIGH, indicating the presence of new valid data. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e., data does not change if the FIFO is empty). A dual-port RAM inside the chip provides the capability of simultaneous and asynchronous writes (Shift-Ins) and reads (Shift-Outs).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Monolithic Memories recommends a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading; i.e., rising edge of the Shift-In pulse is not recognized until Input ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to Shift-In going HIGH. This same type of problem is also related to T_{IRH}, T_{ORL}, T_{ORH}, and the Status Flag timing as related to Shift-In and Shift-Out. For high-speed applications, proper grounding technique is essential.

HF and AFE Status Flags

The Half-Full (HF) will be high only when the net balance of words shifted into the FIFO exceeds the number of words shifted out by thirty-two or more (i.e., when the FIFO contains thirty-two or more words). The Almost-Full/Empty (AFE) flag will be HIGH when the FIFO contains fifty-six or more words or when the FIFO contains eight or fewer words (see Figures 9, 10, and 11).

Care should be exercised in using the status flags because they are capable of producing arbitrarily short pulses. For example, if the FIFO contains thirty-one words, and SI and SO pulses are applied simultaneously, the HF flag may produce an arbitrarily short pulse, depending on the precise phase of SI and SO.

The flags will always settle to the correct state after the appropriate delay (e.g., T_{HFL}, T_{HFH} in this example). This property of the status flags will clearly be a function of the dynamic relation between SI and SO. Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

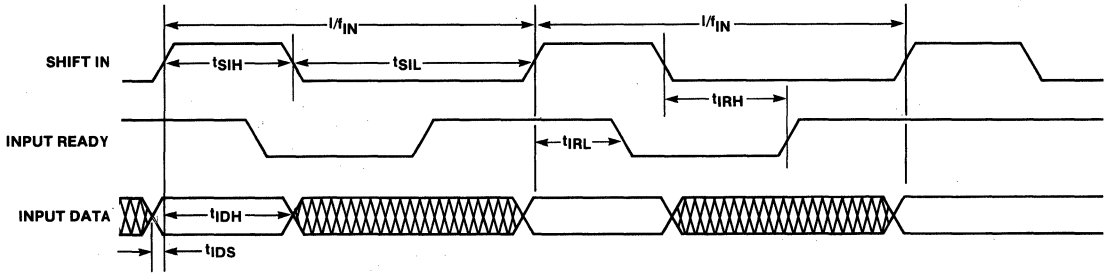


Figure 1. Input Timing

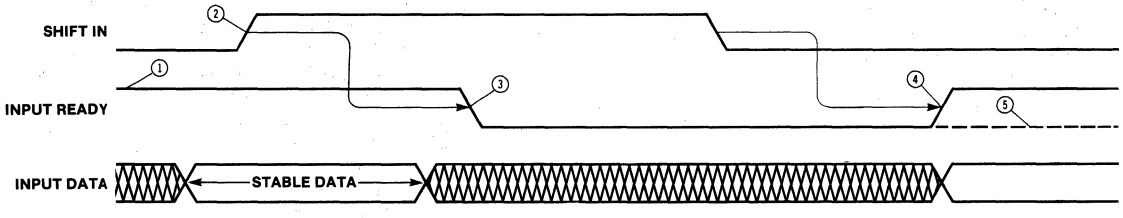


Figure 2. The Mechanism of Shifting Data into the FIFO

① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
② Input Data is loaded into the first available memory location.
③ Input Ready goes LOW indicating this memory location is full.
④ Shift-In going LOW allows Input Ready to sense the status of the next memory location. The next memory location is empty as indicated by Input Ready HIGH.
⑤ If the FIFO is already full then the Input Ready remains low.
Note: Shift-In pulses applied while Input Ready is LOW will be ignored.

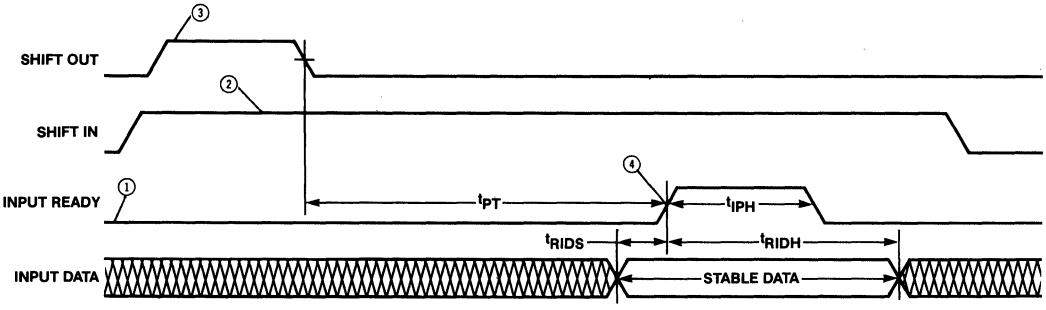


Figure 3. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

① FIFO is initially full.
② Shift In is held HIGH.
③ Shift Out pulse is applied. An empty location is detected by the internal pointers on the falling edge of SO.
④ As soon as Input Ready becomes HIGH the Input Data is loaded into this location.

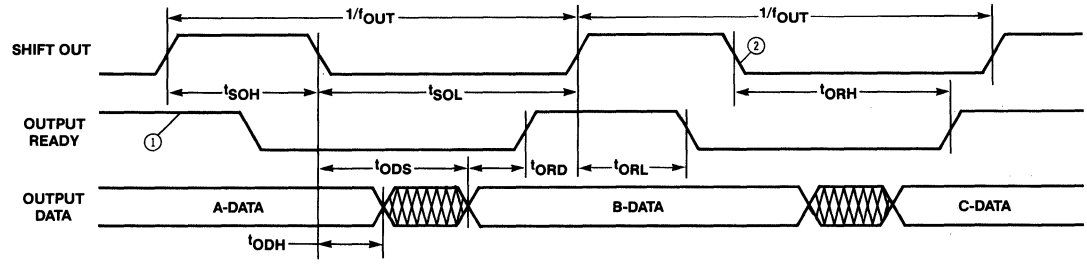


Figure 4. Output Timing

① The diagram assumes that the FIFO contains at least three words: A-Data (first input word), B-Data (second input word), and C-Data (third input word).
② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO are both high together.

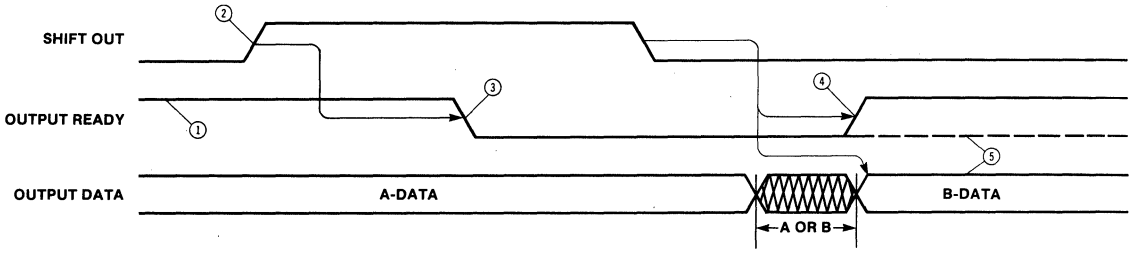


Figure 5. The Mechanism of Shifting Data Out of the FIFO

① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
② Shift-Out goes HIGH causing B-Data (second input word) to advance to the output register. Output data remains as valid A-Data while Shift-Out is HIGH.
③ Output Ready goes LOW.
④ Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data remains the same (A-Data).

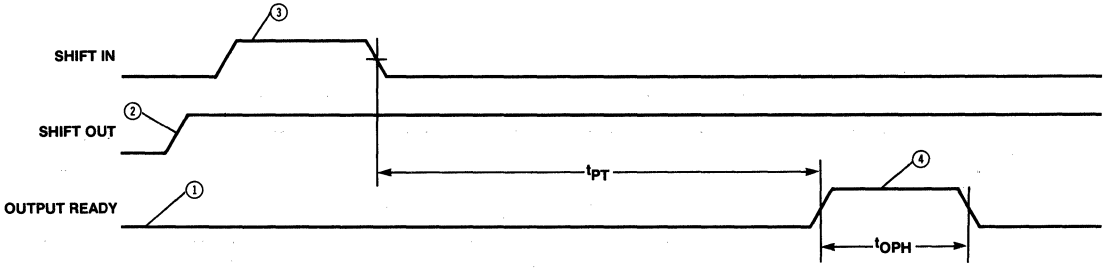


Figure 6. t_{PT} and t_{OPH} Specification

① FIFO is initially empty.
② Shift-Out is held HIGH.
③ Shift-In pulse applied. A full location is detected by the internal pointers on the falling edge of Shift-In
④ As soon as Output Ready becomes HIGH, the word is shifted out.

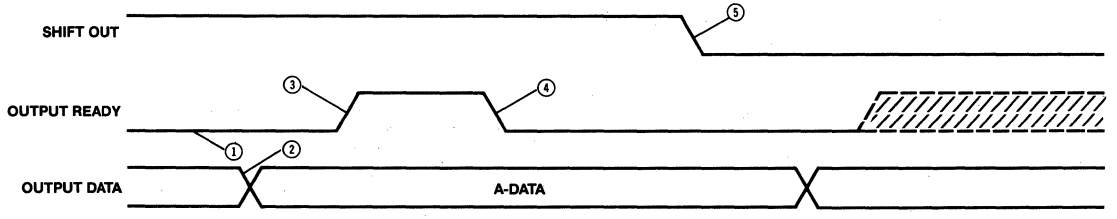


Figure 7. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH

① The internal logic does not detect the presence of any data in the FIFO.
② New data (A) arrives at the outputs.
③ Output Ready goes HIGH indicating arrival of the new data.
④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.
⑤ As soon as Shift Out goes LOW the Output Data is subject to change.
Output Ready will go HIGH or remain LOW depending on whether there are any additional upstream words in the FIFO.

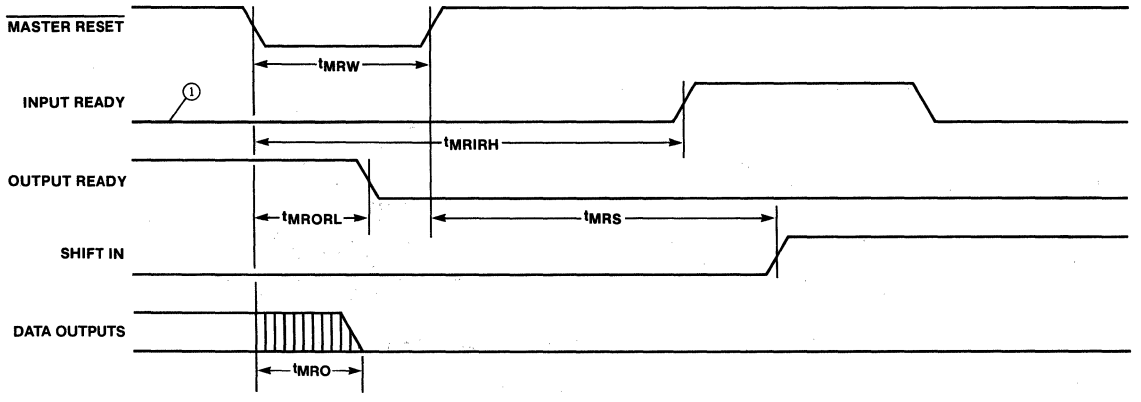


Figure 8. Master Reset Timing

① FIFO is initially full.

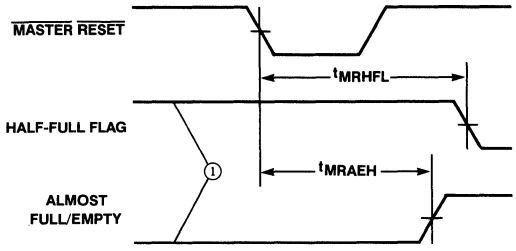


Figure 9. t_{MRHFL}, t_{MRAEH} Specifications

① FIFO intially has between 32 and 56 words.

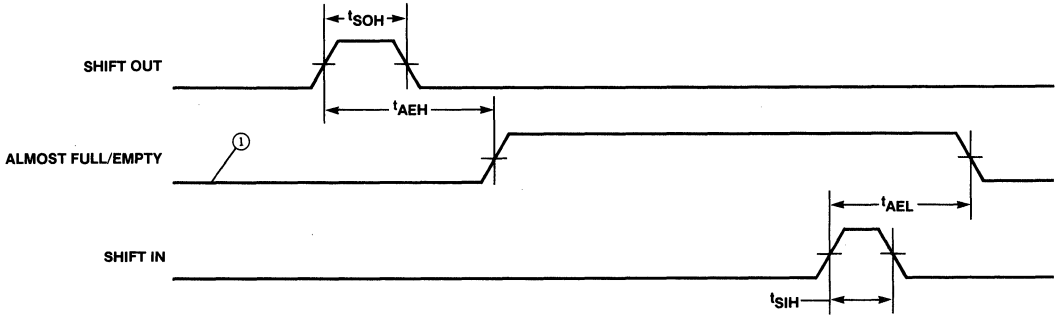


Figure 10. t_{AEH}, t_{AEL} Specifications

① FIFO contains 9 words (one more than almost empty).

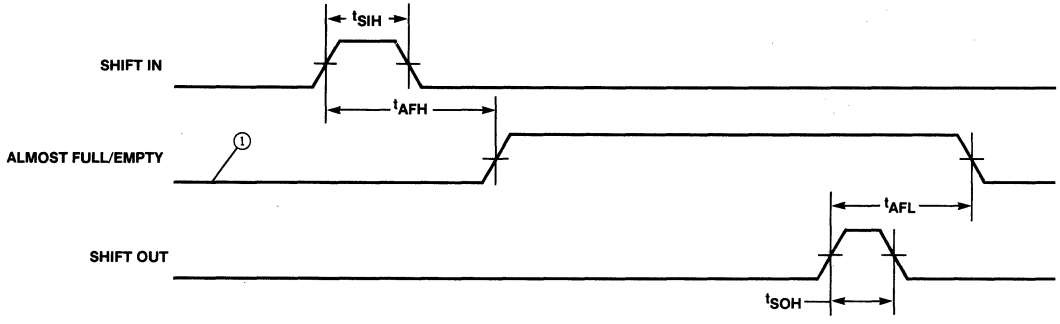


Figure 11. t_{AFH}, t_{AFL} Specifications

① FIFO contains 55 words (one short of almost full).

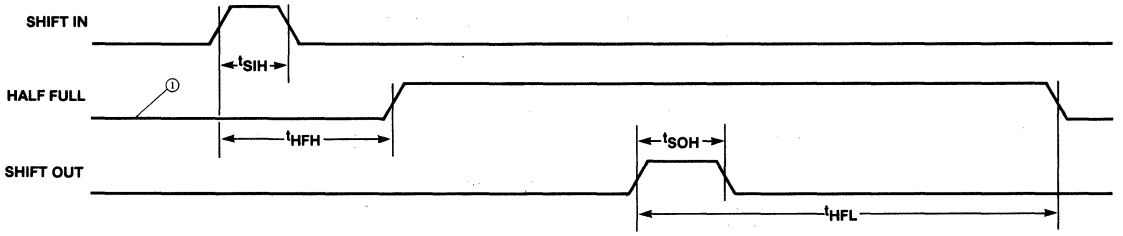
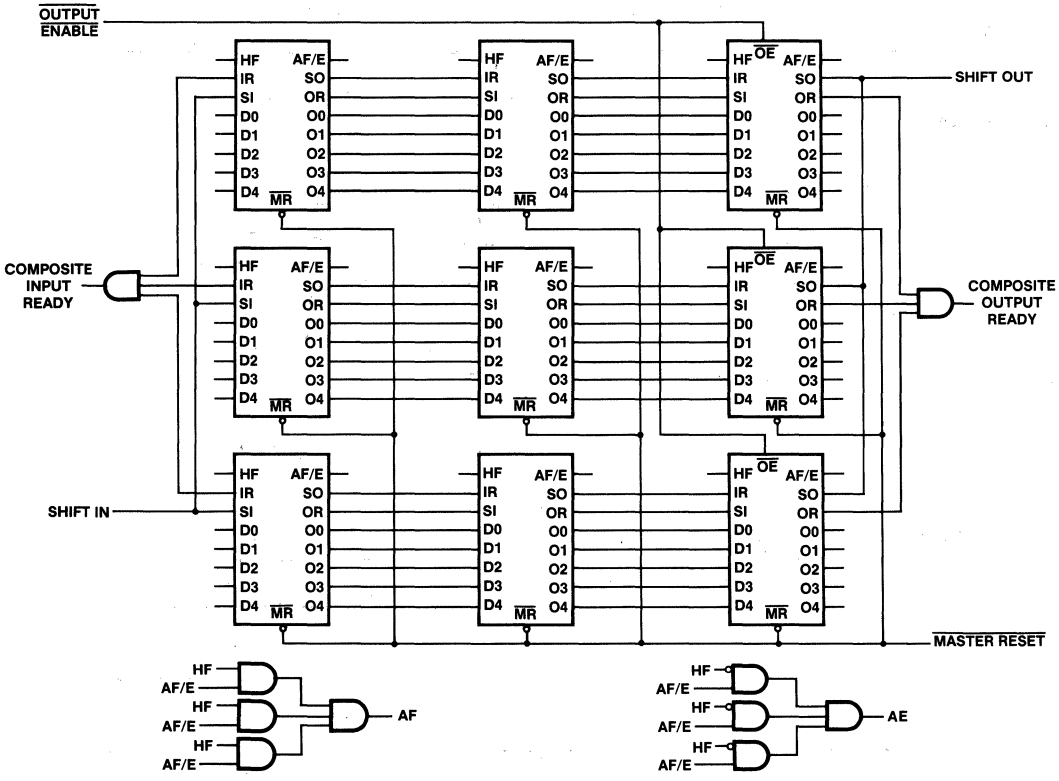


Figure 12. t_{HFL}, t_{HFH} Specifications

① FIFO contains 31 words (one short of half full).



Almost Full (AF) is eight words or less to FIFO full.
Almost Empty (AE) is eight words or less to FIFO empty

Figure 13. 192x15 FIFO

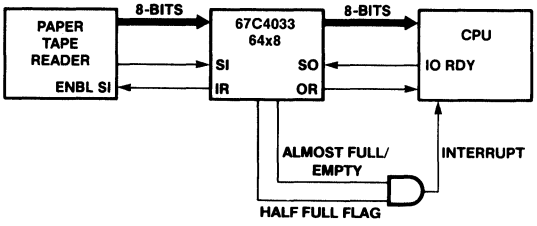
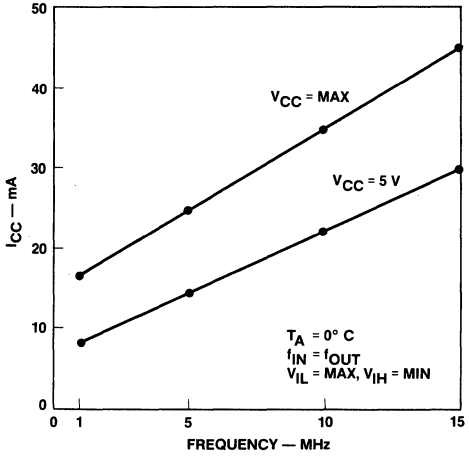


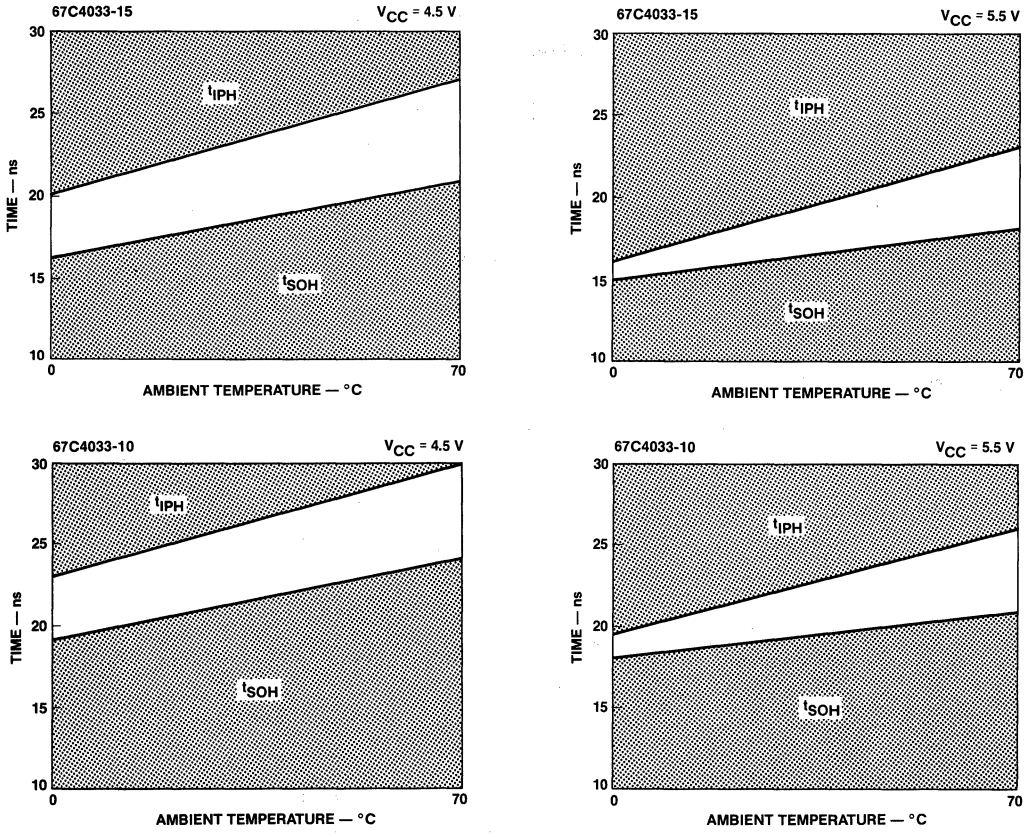
Figure 14. Application for 67C4033 "Slow and Steady Rate to Fast 'Blocked Rate' "

Note: Expanding the FIFOs in word width is done by ANDing the IR and OR as shown in Figure 13.

I_{CC} vs. Frequency



Guaranteed Distribution of t_{IPH}, t_{SOH} vs. Temperature (For Cascadability Only)



Guaranteed Distribution of t_{OPH}, t_{SIH} vs. Temperature (For Cascadability Only)

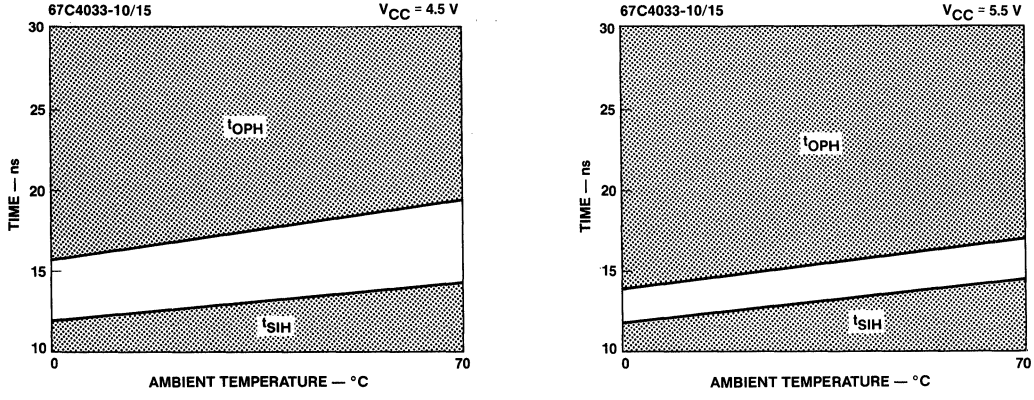


Figure B. Cascadability

67C4500-35/50/65/80

Deep First-in First-out (FIFO)
256x9 CMOS Memory

DISTINCTIVE CHARACTERISTICS

- **RAM based FIFO**
- **256x9 organization**
- **Cycle times of 45/65/80/100 nanoseconds**
- **Asynchronous and simultaneous writes and reads**
- **Low power consumption — 60 mA maximum**
- **Status flags - full, half-full, empty**
- **Retransmit capability**
- **Expandable in both width and depth**
- **Increased noise immunity for $\overline{XI}$ - CMOS threshold**
- **Functional and pin compatible with industry standard devices**

GENERAL DESCRIPTION

The 67C4500 is a RAM-based CMOS FIFO that is 256 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 22 MHz. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

Deep FIFOs such as the 67C4500 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the 67C4500 useful in communication, image processing, mass storage, DSP, and printing systems.

BLOCK DIAGRAM

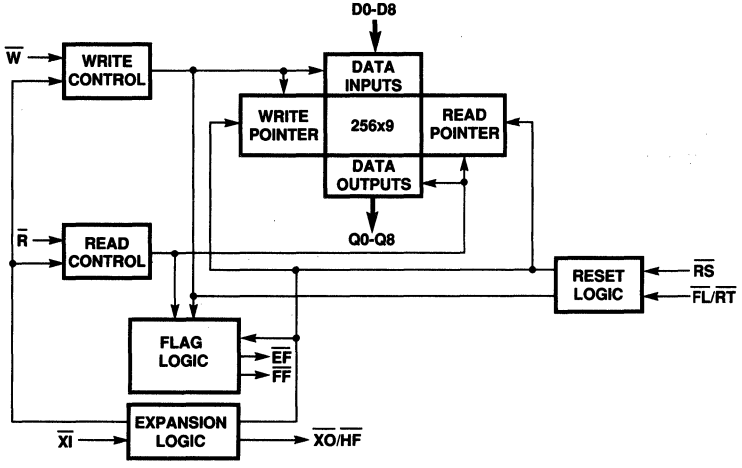


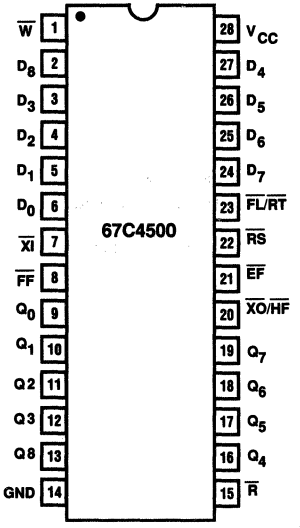
Figure 1.

Publication #	Rev.	Amendment
10804A	B	/0

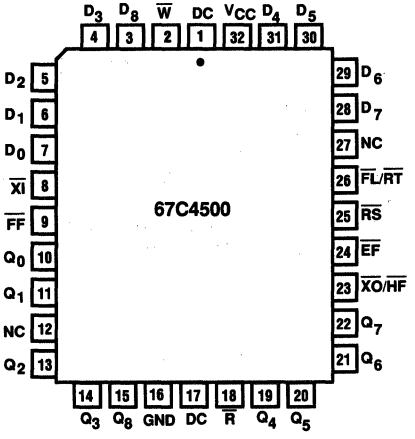
Issue Date: July 1988

CONNECTION DIAGRAMS

DIP



PLCC



Note: Pin 1 is marked for orientation.

Pin Designations: $\overline{W}$ = Write
$\overline{R}$ = Read
$\overline{RS}$ = Reset
$\overline{FL}/\overline{RT}$ = First Load/Retransmit
D_x = Data In
Q_x = Data Out
$\overline{XI}$ = Expansion In
$\overline{XO}/\overline{HF}$ = Expansion Out/Half-Full Flag
$\overline{FF}$ = Full Flag
$\overline{EF}$ = Empty Flag
V_{cc} = Supply Voltage
GND = Ground

ORDERING INFORMATION

Standard Products

AMD/MMI standard products are available in several packages. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Operating Conditions
d. Package Type

67 C 4500 - 35 N

c. OPERATING CONDITIONS
67 = Commercial (0°C to 70°C)

CMOS TECHNOLOGY

a. PART NUMBER

b. PERFORMANCE
35 ns = 35 ns t_A
50 ns = 50 ns t_A
65 ns = 65 ns t_A
80 ns = 80 ns t_A

d. PACKAGE TYPE
N = Plastic DIP
J = Ceramic DIP
NL = Plastic Leaded Chip Carrier

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC} ..... -0.5 V to + 7.0 V
Input voltage ..... -0.5 V to V_{CC} + 0.5 V
Operating temperature ..... 0°C to + 70°C
Storage temperature ..... -55°C to + 150°C
Power dissipation ..... 1.0 W
DC output current ..... 50 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC CHARACTERISTICS Commercial: V_{CC} = 5 V ± 10%, T_A = 0°C to + 70°C

Parameter Symbol	Parameter Description	67C4500-35 T_A = 35 ns Min.	67C4500-35 T_A = 35 ns Max.	67C4500-50 T_A = 50 ns Min.	67C4500-50 T_A = 50 ns Max.	67C4500-65 T_A = 65 ns Min.	67C4500-65 T_A = 65 ns Max.	67C4500-80 T_A = 80 ns Min.	67C4500-80 T_A = 80 ns Max.	Unit
I_{IL}	Input Leakage Current (any input) (Note 1)	-1	1	-1	1	-1	1	-1	1	µA
I_{IO}	Output Leakage Current (data outputs) (Note 2)	-10	10	-10	10	-10	10	-10	10	µA
V_{IH}	Input High Voltage (all inputs except $\overline{XI}$) (Note 3)	2.0	–	2.0	–	2.0	–	2.0	–	V
V_{IL}	Input Low Voltage (all inputs except $\overline{XI}$) (Note 3)	–	0.8	–	0.8	–	0.8	–	0.8	V
V_{IHXI}	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	–	3.5	–	3.5	–	3.5	–	V
V_{ILXI}	Input Low Voltage, $\overline{XI}$ (Note 3)	–	1.5	–	1.5	–	1.5	–	1.5	V
V_{OH}	Output Logic "1" Voltage I_{OH} = -2 mA	2.4	–	2.4	–	2.4	–	2.4	–	V
V_{OL}	Output Logic "0" voltage I_{OL} = 8 mA	–	0.4	–	0.4	–	0.4	–	0.4	V
I_{CC1}	Average V_{CC} Power Supply Current (Note 4)	–	60	–	60	–	60	–	60	mA
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH}) (Note 4)	–	20	–	20	–	20	–	20	mA
I_{CC3}	Power Down Current (all inputs = V_{CC} -0.2 V) (Note 4)	–	5	–	5	–	5	–	5	mA

Notes:
1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. These are absolute voltage levels with respect to the ground pins on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

AC CHARACTERISTICS V_{CC} = 5 V ± 10%, TA = 0°C to + 70°C

Parameter Symbol	Parameter Description	Figures	67C4500-35 Min.	67C4500-35 Max.	67C4500-50 Min.	67C4500-50 Max.	67C4500-65 Min.	67C4500-65 Max.	67C4500-80 Min.	67C4500-80 Max.	Unit
Write and Flag Timing											
t_{WC}	Write Cycle Time	3	45		65		80		100		ns
t_{WPW}	Write Pulse Width	3	35		50		65		80		ns
t_{WR}	Write Recovery Time	3	10		15		15		20		ns
t_{DS}	Data Setup Time	3,9	25		30		30		40		ns
t_{DH}	Data Hold Time	3,9	0		5		10		10		ns
t_{WFF}	Write LOW to Full Flag LOW	6,9		30		45		60		60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	5		45		65		80		100	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	4,8		30		45		60		60	ns
t_{WLZ}	Write pulse HIGH to data bus at LOW Z (Note 1)	8	10		15		15		20		ns
Read and Flag Timing											
t_{RC}	Read Cycle Time	3	45		65		80		100		ns
t_A	Access Time	3,4,8,9		35		50		65		80	ns
t_{RR}	Read Recovery Time	3	10		15		15		20		ns
t_{RPW}	Read Pulse Width	3	35		50		65		80		ns
t_{RLZ}	Read pulse LOW to data bus at LOW Z (Note 1)	3	5		10		10		10		ns
t_{DV}	Data Valid from read pulse HIGH	3	5		5		5		5		ns
t_{RHZ}	Read pulse HIGH to data bus at HIGH Z (Note 1)	3		20		30		30		30	ns
t_{RFF}	Read HIGH to Full Flag HIGH	6,9		30		45		60		60	ns
t_{RHF}	Read HIGH to Half Full-Flag HIGH	5		45		65		80		100	ns
t_{REF}	Read LOW to Empty Flag LOW	4,8		30		45		60		60	ns
Reset Timing											
t_{RSC}	Reset Cycle Time	2	45		65		80		100		ns
t_{RS}	Reset Pulse Width	2	35		50		65		80		ns
t_{RSS}	Reset Setup Time	2	35		50		65		80		ns
t_{RSR}	Reset Recovery Time	2	10		15		15		20		ns
t_{EFL}	Reset to Empty Flag LOW	2		45		65		80		100	ns
t_{HFH}	Reset to Half-Full Flag High	2		45		65		80		100	ns
t_{FFH}	Reset to Full Flag HIGH	2		45		65		80		100	ns
Retransmit Timing											
t_{RTC}	Retransmit Cycle Time	7	45		65		80		100		ns
t_{RT}	Retransmit Pulse Width	7	35		50		65		80		ns
t_{RTR}	Retransmit Recovery Time	7	10		15		15		20		ns

Note: 1. Characterized parameters.

FUNCTIONAL DESCRIPTION

The 67C4500 CMOS FIFO is designed around a 256x9 dual-port static RAM array. (See Figure 1.) RAM-based FIFOs store the data written into them in a sequential pattern.

The dual-port RAM array has dedicated write and read address pointers. The flag logic prevents illogical writes and reads from occurring. The Empty Flag prevents reading while empty, which is a data underflow condition, while the Full Flag prevents writing while full, which is a data overflow condition. Once data that has been stored at a given address is read, it can be overwritten.

Address pointers automatically overflow to address zero after reaching address 255. Thus the flag status of the FIFO is a function of the difference between the pointers, not their absolute value.

Resetting the FIFO simply initializes both address pointers to address zero. Pulsing Retransmit initializes the read address pointer to zero without affecting the write address pointer.

Expansion Logic is used when implementing a FIFO of a depth greater than that of the 67C4500. The write, read, data-in and data-out lines of the 67C4500 are connected in parallel, and the Expansion-Out ($\overline{XO}$) and the Expansion-In ($\overline{XI}$) lines are daisy-chained together. The write and read control circuits of the individual FIFOs are automatically enabled and disabled through the handshake between $\overline{XO}$ and $\overline{XI}$.

OPERATIONAL DESCRIPTION

Resetting The FIFO

Upon power up, the FIFO must be initialized with a Reset cycle. (See Figure 2.) The states of $\overline{XI}$ and $\overline{FL}$ are used during the reset cycle to determine the FIFO's mode of operation, as shown in Tables 1 and 2. For a valid reset cycle to occur, both the Read ($\overline{R}$) and Write ($\overline{W}$) signals must be HIGH t_{RSS} prior to and t_{RSR} after the rising edge of Reset ($\overline{RS}$). The reset cycle initializes the FIFO to an empty condition, signified by the Empty Flag ($\overline{EF}$) being LOW, active, and both the Half-Full ($\overline{HF}$) and Full Flag ($\overline{FF}$) being HIGH, inactive.

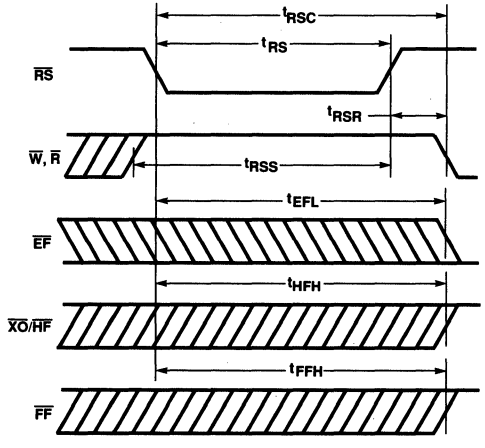


Figure 2. Reset Timing

Writing Data To The FIFO

The HIGH state of the Full Flag ($\overline{FF}$) indicates that the FIFO is capable of accepting data. The falling edge of Write ($\overline{W}$) initiates a write cycle. (See Figure 3.) Data appearing at inputs D0-D8 t_{DS} prior to and t_{DH} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The LOW- to-HIGH transition of the Empty Flag ($\overline{EF}$) occurs t_{WEF} after the rising edge of $\overline{W}$ during the first write cycle on an empty FIFO. (See Figure 4.) The Half-Full Flag /HF) will go LOW t_{WHF} after the falling edge of $\overline{W}$ during the write operation which creates the half-full condition. (See Figure 5.) $\overline{HF}$ will remain LOW, while the number of writes to the FIFO exceeds the number of reads by 128 or more. The Half-Full Flag is not available in Depth-Expansion Mode. The Full Flag ($\overline{FF}$) goes LOW t_{WFF} after the falling edge of $\overline{W}$ during the write cycle which creates a full condition. (See Figure 6.) A full condition exists when there have been 256 more write cycles than read cycles. The Full Flag being active prohibits any further write operations, thus preventing data overflow situations.

Reading Data From The FIFO

The HIGH state of the Empty Flag ($\overline{EF}$) indicates that the FIFO is ready to output data. The falling edge of Read ($\overline{R}$) initiates a read cycle. (See Figure 3.) Valid data appears on the outputs Q0-Q8 t_A after the falling edge of $\overline{R}$, and remains until t_{DV} after the rising edge of $\overline{R}$. Q0-Q8 return to a high-impedance state when a valid read is not in progress.

The Full Flag ($\overline{FF}$) will go HIGH t_{RFF} after the rising edge of $\overline{R}$ during the first read cycle following a full condition. (See Figure 6.) The Half-Full Flag ($\overline{HF}$) will go HIGH t_{RHF} after the rising edge of $\overline{R}$ during the read operation, which eliminates the half-full condition. (See Figure 5). $\overline{HF}$ will remain HIGH, while the number of writes to the FIFO exceeds the number of reads by 127 or less. The Half-Full Flag is not available in Depth-Expansion Mode. The HIGH-to-LOW transition of $\overline{EF}$ occurs t_{REF} after the falling edge of $\overline{R}$ during the read cycle, which creates an empty condition. (See Figure 4.) An empty condition exists when there has been an equal number of write cycles and read cycles. The Empty Flag being active prohibits any further read operations, thus preventing a data underflow situation.

Half-Full Flag

The Half-Full ($\overline{HF}$) Flag will be active LOW only when the net balance of the words written into the FIFO exceeds the number of words read out by 128 or more. (See Figure 5.)

Care should be exercised in using the Half-Full Flag, because it is capable of producing arbitrarily short pulses. For example, if the FIFO contains 128 words, and Read and Write pulses are applied simultaneously, the $\overline{HF}$ flag may produce an arbitrarily short pulse, depending on the precise phase of Read and Write.

$\overline{HF}$ will always settle to the correct state after the appropriate delay, t_{WHF} or t_{RHF}. This property of the Half-Full Flag is clearly a function of the dynamic relation between $\overline{W}$ and $\overline{R}$. Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

RESET AND RETRANSMIT TRUTH TABLE Single-Device Configuration/Width-Expansion Mode

Mode	Input			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X (Note 1)	X (Note 1)	X (Note 1)
Read/Write	1	1	0	Increment (Note 2)	Increment (Note 2)	X	X	X

Notes: 1. Flags will change to show correct state according to write pointer.
2. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 1.

RESET AND FIRST LOAD TRUTH TABLE Depth-Expansion/Compound-Expansion Mode

Mode	Input			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset–first device	0	0	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Reset all other devices	0	1	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Read/Write	1	X (Note 2)	$\overline{XO}$ (Note 1)	Increment (Note 3)	Increment (Note 3)	X	X

Notes: 1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12.
2. Same as during Reset Cycle.
3. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 2.

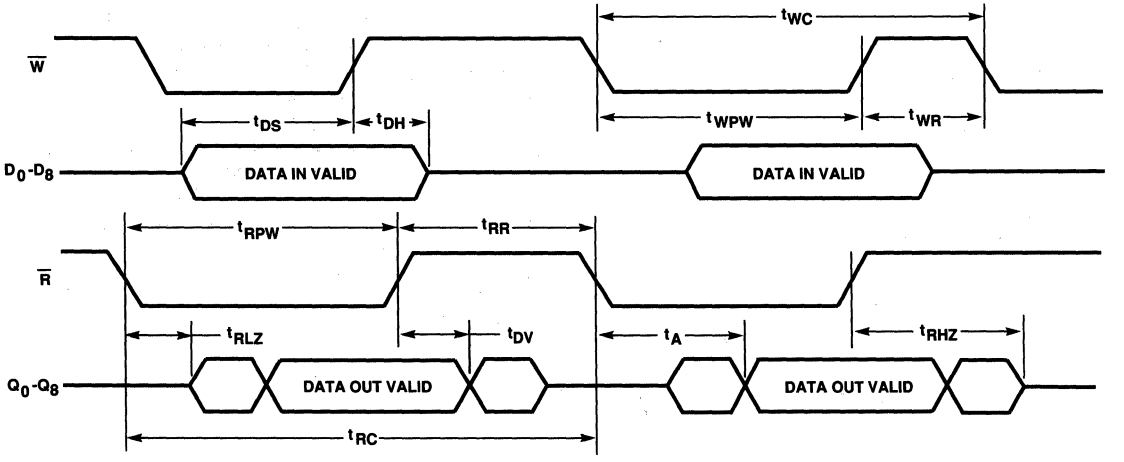


Figure 3. Asynchronous Write and Read Timing

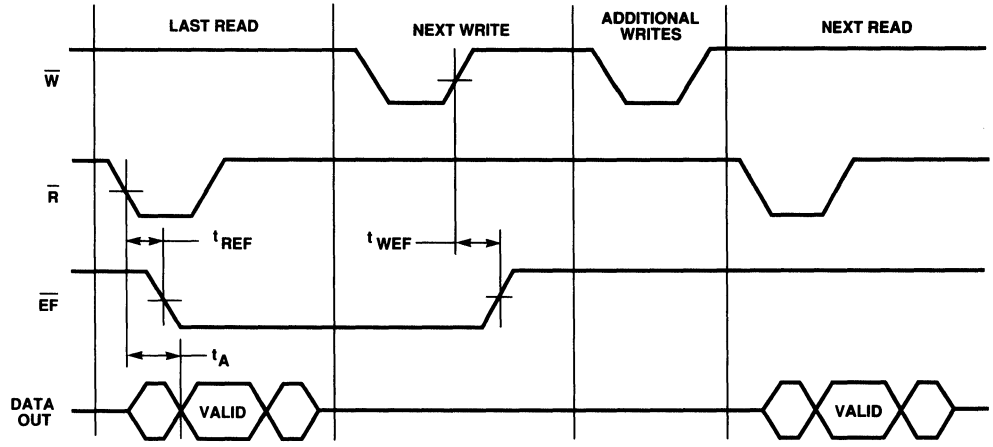
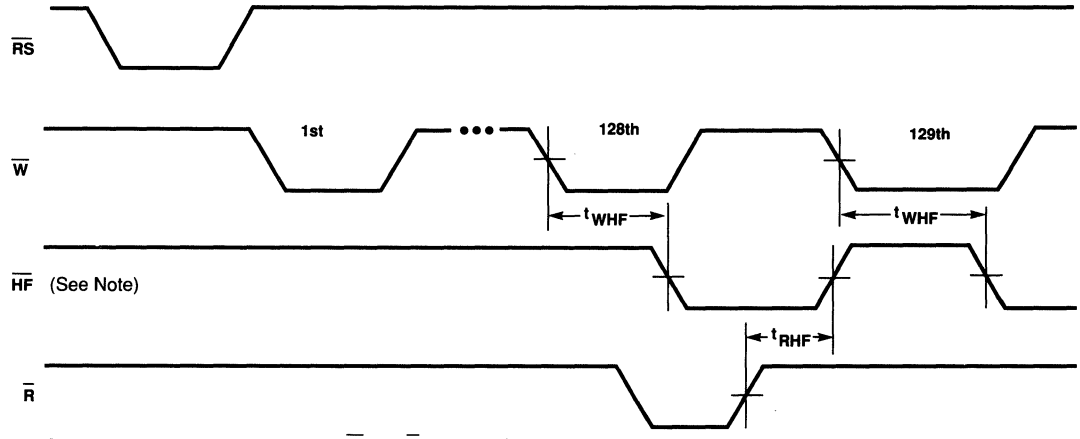


Figure 4. Empty Flag Timing



Note: Depending on the precise phase of $\overline{W}$ and $\overline{R}$, the Half-Full Flag may appear as a pulse of arbitrarily short duration of either polarity when $\overline{W}$ and $\overline{R}$ are operating asynchronously near half full.

Figure 5. Half-Full Flag Timing

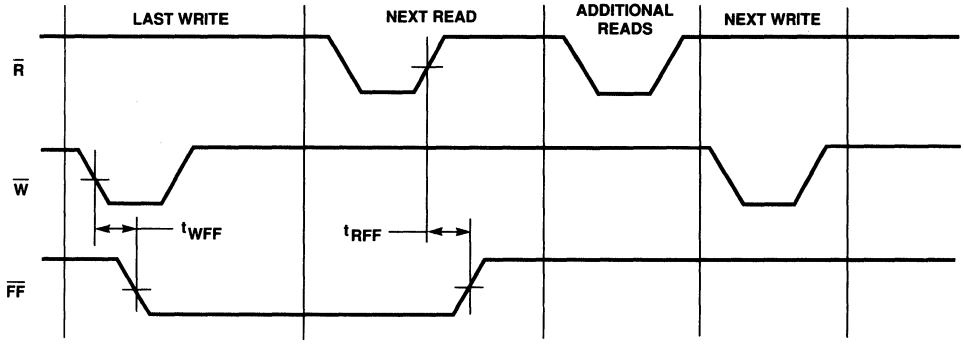


Figure 6. Full Flag Timing

Retransmit

The retransmit function resets the read address pointer allowing the data that was previously read to be read again. This capability is useful when the block of data being transferred through the FIFO doesn't exceed the FIFO's depth and is intended for use when there are 256 or less writes between reset cycles.

The $\overline{FL}/\overline{RT}$ is used as the Retransmit ($\overline{RT}$) input in Single-Device Mode. $\overline{RT}$, an active LOW-going pulse of at least t_{RT} in duration, returns the internal read pointer to address zero and leaves the write pointer unaffected. $\overline{W}$ and $\overline{R}$ must both be HIGH during the retransmit cycle. The first write or read cycle should not start until t_{RTR} after the rising edge of $\overline{RT}$. The flags may change state during this cycle, but they will accurately reflect the new state of the FIFO t_{RTC} after the falling edge of $\overline{RT}$. (See Figure 7 and Table 1).

Single-Device/Width-Expansion Modes

Single-Device and Width-Expansion Modes are configured by grounding the Expansion-In ($\overline{XI}$) input. (See Figures 10 and 11, and Table 1.) During these modes of operation, the Half-Full Flag and Retransmit features are available. The 67C4500 can be expanded in width to create FIFOs of word widths greater than nine bits. In Width-Expansion Mode all of the control line inputs are common to all devices. (See Figure 11.) Creating composite status flags can pose two hazards. 1.) OR-ing the flag outputs is fine for the HIGH-to-LOW transition, because the skew between devices is masked out. However, when the flags make a LOW-to-HIGH transition, a false composite flag is generated. 2.) The converse is true when the flags are AND-ed: the LOW-to-HIGH transition is fine, and the HIGH-to-LOW generates a false flag. These two hazards can be avoided if one device's flags are used as the flags for the expanded FIFO, and the write control circuitry and read control circuitry is designed to hold off sampling the flags until the worst case settling time (t_{WEF}, t_{WHF}, t_{WFF}, t_{REF}, t_{RHF}, and t_{WFF}) for each flag has elapsed.

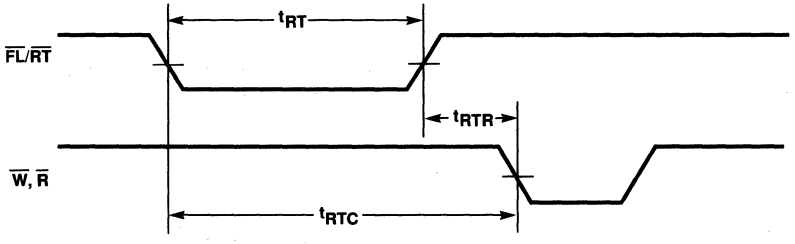
Depth-Expansion Mode

Depth-Expansion Mode is configured during the Reset cycle. (See Figure 12 and Table 2.) Expansion Out ($\overline{XO}$) of one device must be connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device being connected to $\overline{XI}$ of the first device. The device that is to receive data first has its First Load ($\overline{FL}$) input tied LOW, while all other devices must have this input HIGH. Write and read control is passed between devices using $\overline{XO}$ and XI. A LOW-going pulse on $\overline{XO}$ occurs when the last physical location of an active device, address 255, is written to, and another LOW-going pulse occurs when the last physical location of an active device is read. Only one device is enabled for writes, and only one device is enabled for reads at any given time.

When expanding in depth, a composite Full Flag must be created by OR-ing all the $\overline{FF}$ outputs together. Likewise, a composite Empty Flag is created by OR-ing all the $\overline{EF}$ outputs together. The Half-Full Flag and Retransmit functions are not available in Depth-Expansion Mode.

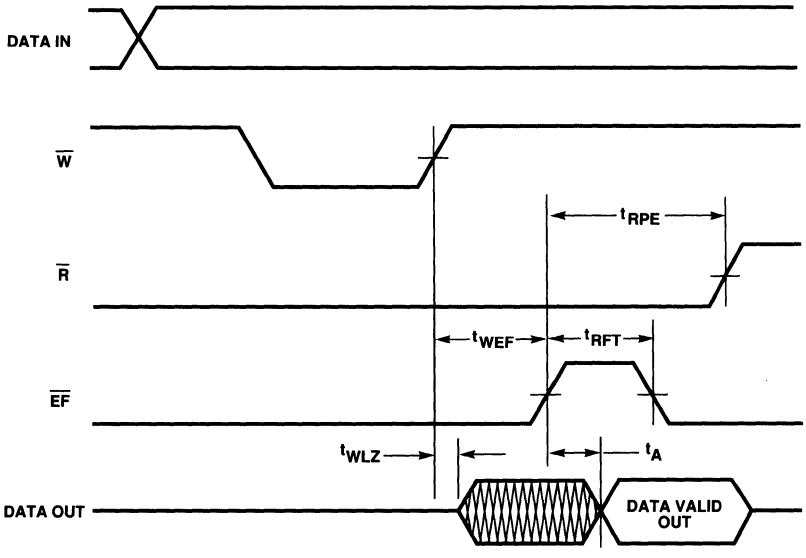
Compound Expansion

FIFOs of greater width and depth than the 67C4500 can be created by using both Width-Expansion Mode and Depth-Expansion Mode simultaneously. (See Figure 13.)



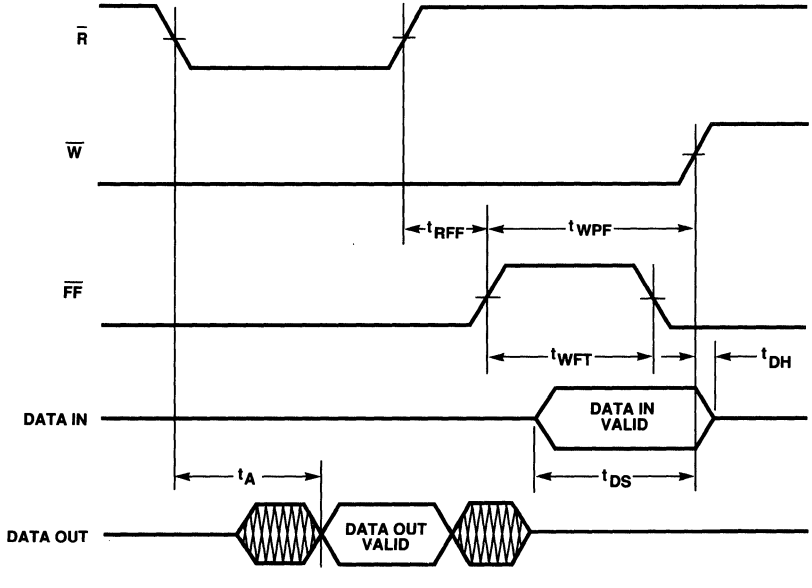
Note: $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during Retransmit as a result of the offset of the read and write pointers, but the flags will be valid at t_{RTC}.

Figure 7. Retransmit Timing



Note: ($t_{RPE} = t_{RPW}$, $t_{RFT} = t_{REF}$)

Figure 8. Read Data Flow Through Mode



Note: ($t_{WPF} = t_{WPW}$, $t_{WFT} = t_{WFF}$)

Figure 9. Write Data Flow Through Mode

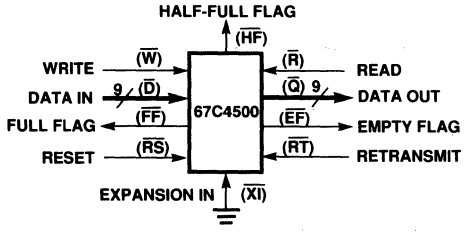


Figure 10. Single FIFO Configuration

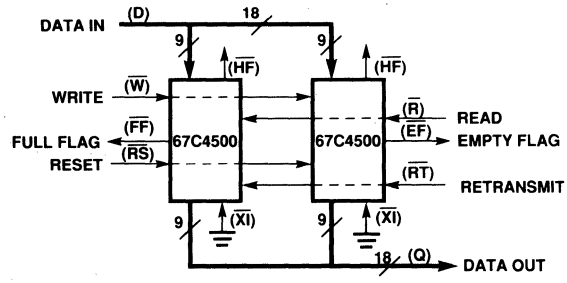


Figure 11. Width-Expansion to Form a 256x18 FIFO

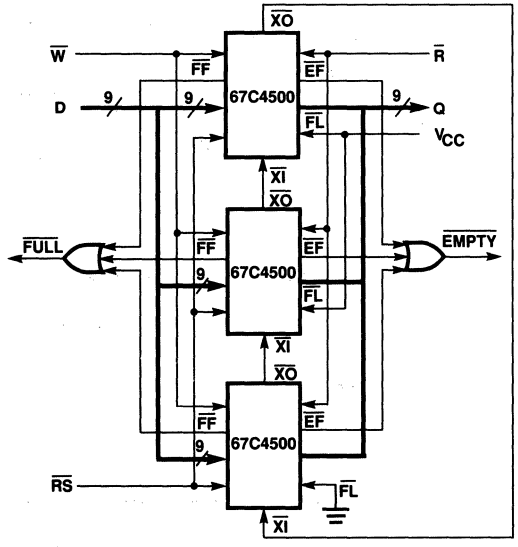


Figure 12. Depth-Expansion to Form a 768x9 FIFO

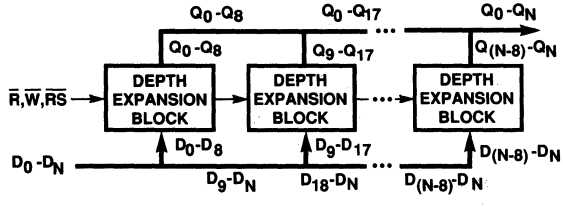


Figure 13. FIFO Array Using Both Width-Expansion and Depth-Expansion Techniques

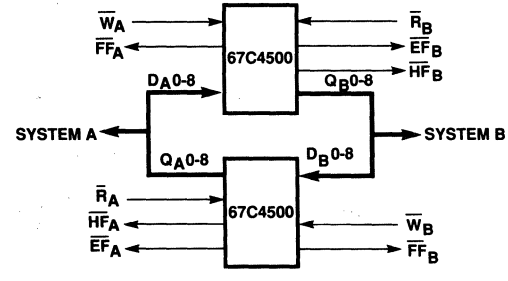
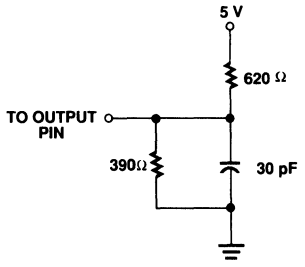


Figure 14. Bidirectional FIFO Mode

AC TEST CONDITIONS

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V
Output load	See Figure 15



* Includes jig and scope capacitances.

Figure 15. A.C. Test Load

CAPACITANCE (T_A = + 25°C, f = 1.0 MHz)

Symbol	Parameter (Note 1)	Conditions	Typ.	Unit
C_{IN}	Input capacitance	V_{IN}= 0 V	5	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V	7	pF

Note: 1. For reference only.

2

Deep First-In First-Out (FIFO) 512x9 CMOS Memory 67C4501-35/50/65/80

Features

- **Ram-based FIFO**
- **512x9 organization**
- **Cycle times of 45/65/80/100 nanoseconds**
- **Asynchronous and simultaneous writes and reads**
- **Low power consumption — 60 mA max**
- **Status flags - Full, Half-Full, Empty**
- **Retransmit capability**
- **Expandable in both width and depth**
- **Increased noise immunity for $\overline{XI}$ - CMOS threshold**
- **Functional and pin-compatible with industry standard devices**

General Description

The 67C4501 is a RAM-based CMOS FIFO that is 512 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 22 MHz. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

Deep FIFOs such as the 67C4501 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the 67C4501 useful in communication, image processing, mass storage, DSP, and printing systems.

Pin Names

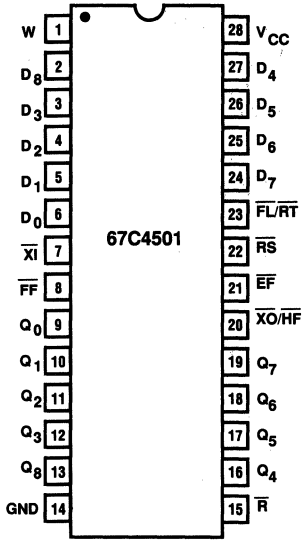
PIN NAME	DESIGNATION
$\overline{W}$	Write
$\overline{R}$	Read
$\overline{RS}$	Reset
$\overline{FL}/\overline{RT}$	First Load/Retransmit
D_X	Data In
Q_X	Data Out
$\overline{XI}$	Expansion In
$\overline{XO}/\overline{HF}$	Expansion Out/Half-Full Flag
$\overline{FF}$	Full Flag
$\overline{EF}$	Empty Flag
VCC	Supply Voltage
GND	Ground

Ordering Information

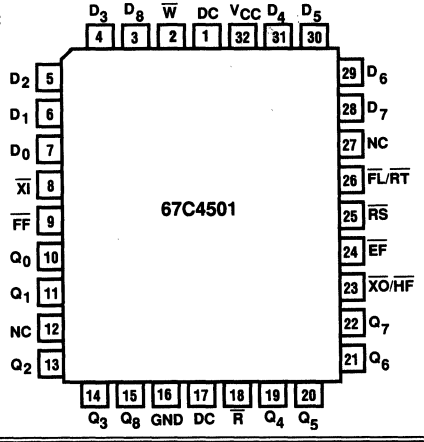
PART NUMBER	DESCRIPTION	PACK	TEMP
67C4501-35	512-word by 9-bit FIFO	N,J,NL	Com
67C4501-50	512-word by 9-bit FIFO	N,J,NL	Com
67C4501-65	512-word by 9-bit FIFO	N,J,NL	Com
67C4501-80	512-word by 9-bit FIFO	N,J,NL	Com

Pin Configurations

DIP



PLCC



Publication #	Rev.	Amendment
10175	B	/0

Issue Date: July 1988

Absolute Maximum Ratings*

Supply voltage, V_{CC} ..... -0.5 V to +7.0 V
Input voltage ..... -0.5 V to V_{CC} +0.5 V
Operating temperature ..... 0°C to +70°C
Storage temperature ..... -55°C to +150°C
Power dissipation ..... 1.0 W
D.C. output current ..... 50 mA

*Note:
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC Electrical Characteristics Commercial: V_{CC} = 5 V ±10%, T_A = 0°C to + 70°C

SYMBOL	PARAMETER	67C4501-35 T_A = 35 ns MIN	MAX	67C4501-50 T_A = 50 ns MIN	MAX	67C4501-65 T_A = 65 ns MIN	MAX	67C4501-80 T_A = 80 ns MIN	MAX	UNITS
I_{LI}[1]	Input leakage current (any input)	-1	1	-1	1	-1	1	-1	1	µA
I_{LO}[2]	Output leakage current	-10	10	-10	10	-10	10	-10	10	µA
V_{IH}[3]	Input high voltage (all inputs except $\overline{XI}$)	2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}[3]	Input low voltage (all inputs except $\overline{XI}$)	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHXI}[3]	Input high voltage, $\overline{XI}$	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{ILXI}[3]	Input low voltage, $\overline{XI}$	—	1.5	—	1.5	—	1.5	—	1.5	V
V_{OH}	Output logic "1" voltage I_{OH} = -2 mA	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output logic "0" voltage I_{OL} = 8 mA	—	0.4	—	0.4	—	0.4	—	0.4	V
I_{CC1}[4]	Average V_{CC} power supply current	—	60	—	60	—	60	—	60	mA
I_{CC2}[4]	Average standby current (R = W = RS = FL/RT = V_{IH})	—	20	—	20	—	20	—	20	mA
I_{CC3}[4]	Power down current (all inputs = V_{CC} -0.2 V)	—	5	—	5	—	5	—	5	mA

Notes:
1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. These are absolute voltage levels with respect to the ground pins on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

AC Electrical Characteristics V_{CC} = 5 V ±10%, T_A = 0°C to +70°C

SYMBOL	DESCRIPTION	FIGURES	67C4501-35 MIN MAX	67C4501-50 MIN MAX	67C4501-65 MIN MAX	67C4501-80 MIN MAX	UNITS
Write and Flag Timing							
t_{WC}	Write cycle time	3	45	65	80	100	ns
t_{WPW}	Write pulse width	3	35	50	65	80	ns
t_{WR}	Write recovery time	3	10	15	15	20	ns
t_{DS}	Data set-up time	3, 9	25	30	30	40	ns
t_{DH}	Data hold time	3, 9	0	5	10	10	ns
t_{WFF}	Write LOW to full flag LOW	6, 9	30	45	60	60	ns
t_{WHF}	Write LOW to half-full flag LOW	5	45	65	80	100	ns
t_{WEF}	Write HIGH to empty flag HIGH	4, 8	30	45	60	60	ns
t_{WLZ}[1]	Write pulse HIGH to data bus at LOW Z	8	10	15	15	20	ns
Read and Flag Timing							
t_{RC}	Read cycle time	3	45	65	80	100	ns
t_A	Access time	3, 4, 8, 9	35	50	65	80	ns
t_{RR}	Read recovery time	3	10	15	15	20	ns
t_{RPW}	Read pulse width	3	35	50	65	80	ns
t_{RLZ}[1]	Read pulse LOW to data bus at LOW Z	3	5	10	10	10	ns
t_{DV}	Data valid from read pulse HIGH	3	5	5	5	5	ns
t_{RHZ}[1]	Read pulse HIGH to data bus at HIGH Z	3	20	30	30	30	ns
t_{RFF}	Read HIGH to full flag HIGH	6, 9	30	45	60	60	ns
t_{RHF}	Read HIGH to half-full flag HIGH	5	45	65	80	100	ns
t_{REF}	Read LOW to empty flag LOW	4, 8	30	45	60	60	ns
Reset Timing							
t_{RSC}	Reset cycle time	2	45	65	80	100	ns
t_{RS}	Reset pulse width	2	35	50	65	80	ns
t_{RSS}	Reset set-up time	2	35	50	65	80	ns
t_{RSR}	Reset recovery time	2	10	15	15	20	ns
t_{EFL}	Reset to empty flag LOW	2	45	65	80	100	ns
t_{HFH}	Reset to half-full flag HIGH	2	45	65	80	100	ns
t_{FFH}	Reset to full flag HIGH	2	45	65	80	100	ns
Retransmit Timing							
t_{RTC}	Retransmit cycle time	7	45	65	80	100	ns
t_{RT}	Retransmit pulse width	7	35	50	65	80	ns
t_{RTR}	Retransmit recovery time	7	10	15	15	20	ns

Note:

1. Characterized parameters.

Block Diagram

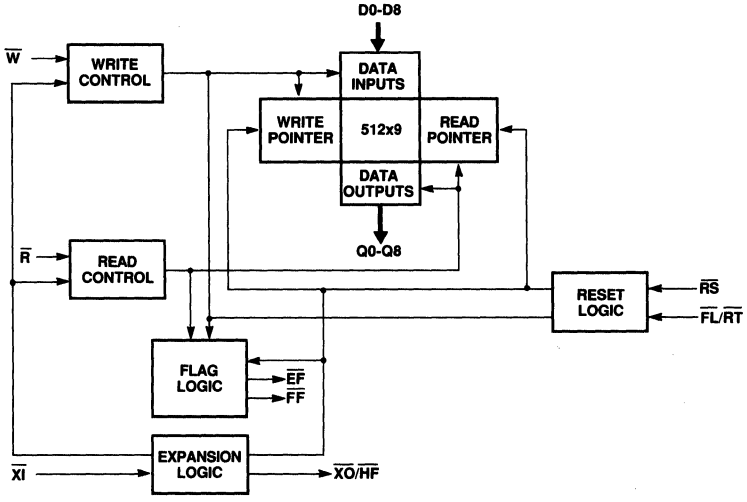


Figure 1.

2

Functional Description

The 67C4501 CMOS FIFO is designed around a 512x9 dual-port static RAM array. (See Figure 1.) RAM-based FIFOs store the data written into them in a sequential pattern.

The dual-port RAM array has dedicated write and read address pointers. The flag logic prevents illogical writes and reads from occurring. The Empty Flag prevents reading while empty, a data underflow condition. While the Full Flag prevents writing while full, a data overflow condition. Once data that has been stored at a given address is read, it can be overwritten.

Address pointers automatically overflow to address zero after reaching address 511. Thus the flag status of the FIFO is a function of the difference between the pointers, not their absolute value.

Resetting the FIFO simply initializes both address pointers to address zero. Pulsing Retransmit initializes the read address pointer to zero without affecting the write address pointer.

Expansion Logic is used when implementing a FIFO of a depth greater than that of the 67C4501. The write, read, data-in and data-out lines of the 67C4501 are connected in parallel, and the Expansion-Out ($\overline{XO}$) and the Expansion-In ($\overline{XI}$) lines are daisy-chained together. The write and read control circuits of the individual FIFOs are automatically enabled and disabled through the handshake between $\overline{XO}$ and $\overline{XI}$.

Operational Description

Resetting the FIFO

Upon power up, the FIFO must be initialized with a Reset cycle. (See Figure 2.) The states of $\overline{XI}$ and $\overline{FL}$ are used during the reset cycle to determine the FIFO's mode of operation, as shown in Tables 1 and 2. For a valid reset cycle to occur, both the Read ($\overline{R}$) and Write ($\overline{W}$) signals must be HIGH tRSS prior to, and tRSR after, the rising edge of Reset ($\overline{RS}$). The reset cycle initializes the FIFO to an empty condition, signified by the Empty Flag ($\overline{EF}$) being LOW (active), and both the Half-Full ($\overline{HF}$) and Full Flag ($\overline{FF}$) being HIGH (inactive).

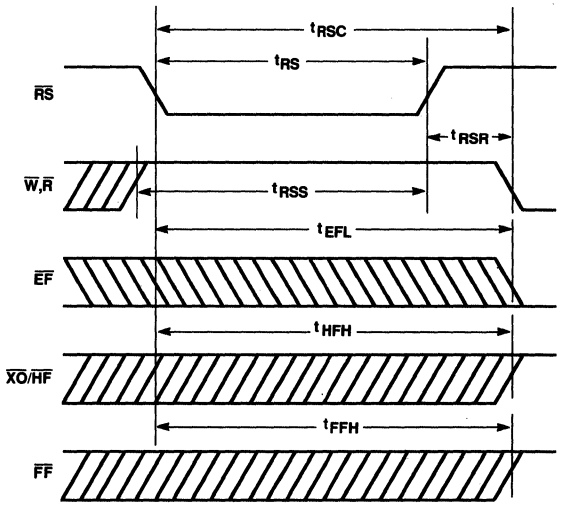


Figure 2. Reset Timing

Reset and Retransmit Truth Table — Single-Device Configuration/Width-Expansion Mode

MODE	INPUT			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	READ POINTER	WRITE POINTER	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X[1]	X[1]	X[1]
Read/Write	1	1	0	Increment[2]	Increment[2]	X	X	X

1. Flags will change to show correct state according to write pointer.
2. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 1.

Reset and First Load Truth Table — Depth-Expansion/Compound-Expansion Mode

MODE	INPUT			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	READ POINTER	WRITE POINTER	$\overline{EF}$	$\overline{FF}$
Reset — first device	0	0	$\overline{XO}$[1]	Location zero	Location zero	0	1
Reset all other devices	0	1	$\overline{XO}$[1]	Location zero	Location zero	0	1
Read/Write	1	X[2]	$\overline{XO}$[1]	Increment[3]	Increment[3]	X	X

1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12.
2. Same as during Reset Cycle.
3. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 2.

Writing Data to the FIFO

The HIGH state of the Full Flag ($\overline{FF}$) indicates that the FIFO is capable of accepting data. The falling edge of Write ($\overline{W}$) initiates a write cycle. (See Figure 3.) Data appearing at inputs D0-D8 tDS prior to, and tDH after, the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The LOW-to-HIGH transition of the Empty Flag ($\overline{EF}$) occurs tWEF after the rising edge of $\overline{W}$ during the first write cycle on an empty FIFO. (See Figure 4.) The Half-Full Flag ($\overline{HF}$) will go LOW tWHF after the falling edge of $\overline{W}$ during the write operation which creates the half-full condition. (See Figure 5.) $\overline{HF}$ will remain LOW, while the number of writes to the FIFO exceed the number of reads by 256 or more. The Half-Full Flag is not available in Depth-Expansion Mode. The Full Flag ($\overline{FF}$) goes LOW tWFF after the falling edge of $\overline{W}$ during the write cycle which creates a full condition. (See Figure 6.) A full condition exists when there have been 512 more write cycles than read cycles. The Full Flag being active prohibits any further write operations, thus preventing data overflow situations.

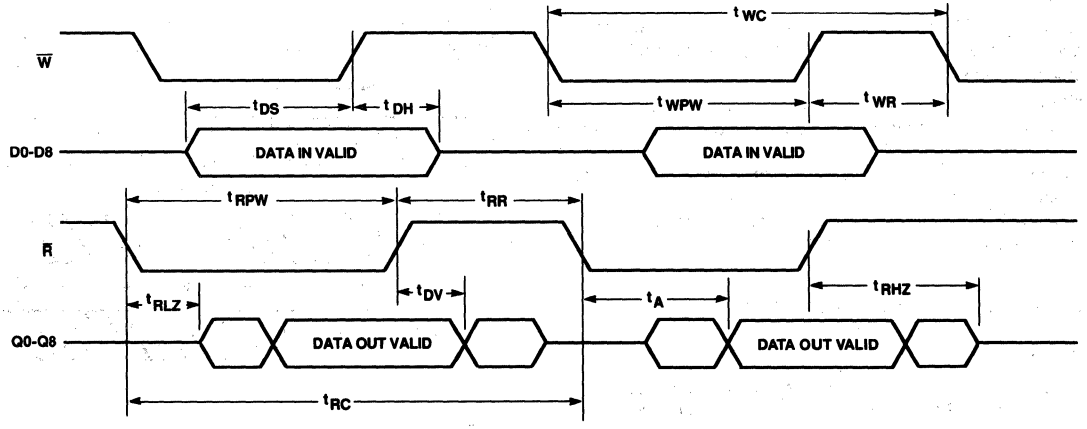


Figure 3. Asynchronous Write and Read Timing

Reading Data from the FIFO

The HIGH state of the Empty Flag ($\overline{EF}$) indicates that the FIFO is ready to output data. The falling edge of Read ($\overline{R}$) initiates a read cycle. (See Figure 3.) Valid data appears on the outputs Q0-Q8 tA after the falling edge of $\overline{R}$, and remains until tDV after the rising edge of $\overline{R}$. Q0-Q8 return to a high impedance state when $\overline{R}$ is inactive, when the FIFO is empty, or when the FIFO is in Depth Expansion Mode but is not active.

The Full Flag ($\overline{FF}$) will go HIGH tRFF after the rising edge of $\overline{R}$ during the first read cycle following a full condition. (See Figure 6.) The Half-Full Flag ($\overline{HF}$) will go HIGH tRHF after the rising edge of $\overline{R}$ during the read operation, which eliminates the half-full condition. (See Figure 5.) $\overline{HF}$ will remain HIGH, while the number of writes to the FIFO exceed the number of reads by 255 or less. The Half-Full Flag is not available in Depth-Expansion Mode. The HIGH-to-LOW transition of $\overline{EF}$ occurs tREF after the falling edge of $\overline{R}$ during the read cycle, which creates an empty condition. An empty condition exists when there have been an equal number of write cycles and read cycles. The Empty Flag being active prohibits any further read operations, thus preventing a data underflow situation.

Half-Full Flag

The Half-Full ($\overline{HF}$) Flag will be active LOW only when the net balance of the words written into the FIFO exceeds the number of words read out by 256 or more. (See Figure 5.)

Care should be exercised in using the Half-Full Flag, because it is capable of producing arbitrarily short pulses. For example, if the FIFO contains 256 words, and Read and Write pulses are applied simultaneously, the $\overline{HF}$ flag may produce an arbitrarily short pulse, depending on the precise phase of Read and Write.

$\overline{HF}$ will always settle to the correct state after the appropriate delay, tWHF or tRHF. This property of the Half-Full Flag is clearly a function of the dynamic relation between $\overline{W}$ and $\overline{R}$. Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

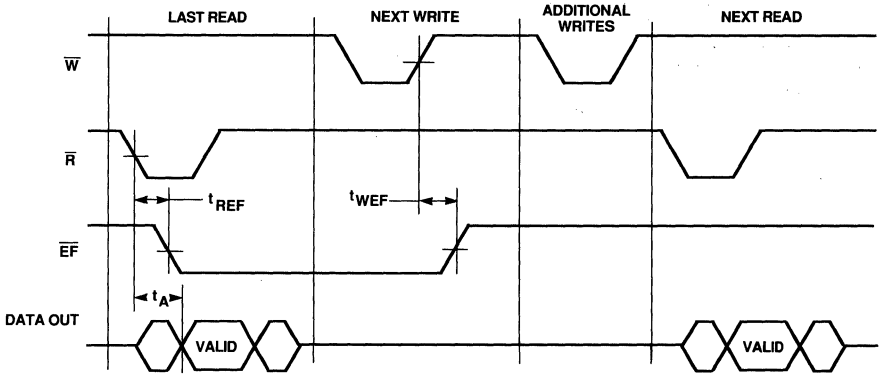
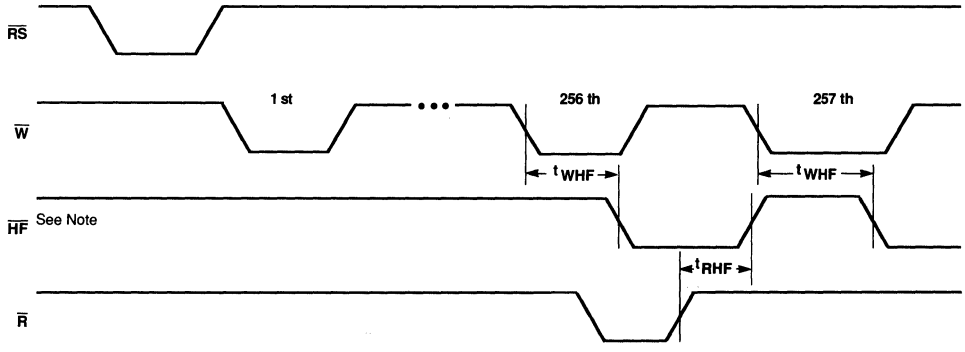


Figure 4. Empty Flag Timing



Note: Depending on the precise phase of $\overline{W}$ and $\overline{R}$, the Half-Full Flag may appear as a pulse of arbitrarily short duration of either polarity when $\overline{W}$ and $\overline{R}$ are operating asynchronously near half-full.

Figure 5. Half-Full Flag Timing

Retransmit

The $\overline{FL}/\overline{RT}$ is used as the Retransmit ($\overline{RT}$) input in Single Device Mode. The retransmit capability is intended for use when there are 512 or less writes between reset cycles. $\overline{RT}$, an active LOW going pulse of at least tRT in duration, initializes the internal read pointer to address zero and leaves the write pointer unaffected. $\overline{W}$ and $\overline{R}$ must both be HIGH during the retransmit cycle. The first write or read cycle should not start until tRTR after the rising edge of $\overline{RT}$. The flags may change state during this cycle, but they will accurately reflect the new state of the FIFO tRTC after the falling edge of $\overline{RT}$. (See Figure 7 and Table 1.)

Single-Device/Width-Expansion Modes

Single-Device and Width-Expansion Modes are configured by grounding the Expansion-In ($\overline{XI}$) input. (See Figures 10 & 11 and Table 1.) During these modes of operation, the Half-Full Flag and Retransmit features are available. The 67C4501 can be expanded in width to create FIFOs of word widths greater than 9 bits . In Width-Expansion Mode all of the control line inputs are common to all devices. (See Figure 11.) Creating composite status flags can pose two hazards. 1) OR-ing the flag outputs is fine for the HIGH-to-LOW transition, because the skew between devices is masked out. However, when the flags make a LOW-to-HIGH transition, a false composite flag is generated due to the skew between devices. 2) The converse is true when the flags are AND-ed: the LOW-to-HIGH transition is fine, and the HIGH-to-LOW generates a false flag. These two hazards can be avoided if one devices' flags are used as the flags for the expanded FIFO, and the write and read control circuitry is designed to hold off sampling the flags until the worst case settling time (tWEF, tWHF, tWFF, tREF, tRHF, and tWFF) for each flag has elapsed.

Depth-Expansion Mode

Depth-Expansion Mode is configured during the Reset cycle. (See Figure 12 and Table 2.) Expansion Out ($\overline{XO}$) of one device must be connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device being connected to $\overline{XI}$ of the first device. The device that is to receive data first has its First Load ($\overline{FL}$) input tied LOW, while all other devices must have this input HIGH. Write and read control is passed between devices using $\overline{XO}$ and $\overline{XI}$. A LOW-going pulse on $\overline{XO}$ occurs when the last physical location, address 511, of an active device is written to, and another LOW-going pulse occurs when the last physical location of an active device is read. Only one device is enabled for writes, and only one device is enabled for reads at any given time.

When expanding in depth, a composite Full Flag must be created by OR-ing all the $\overline{FF}$ outputs together. Likewise, a composite Empty Flag is created by OR-ing all the $\overline{EF}$ outputs together. The Half-Full Flag and Retransmit functions are not available in Depth-Expansion Mode.

Compound Expansion

FIFOs of greater width and depth than the 67C4501 can be created by using both Width-Expansion Mode and Depth-Expansion Mode simultaneously. (See Figure 13.)

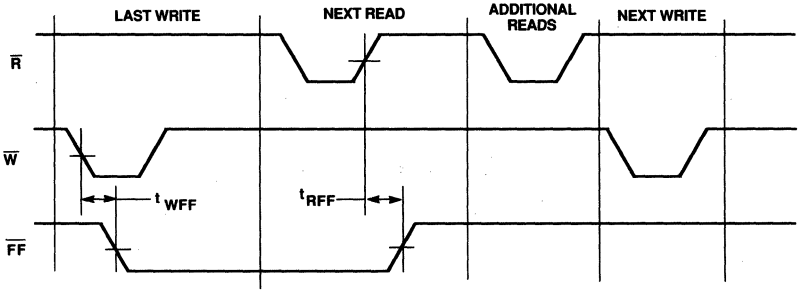
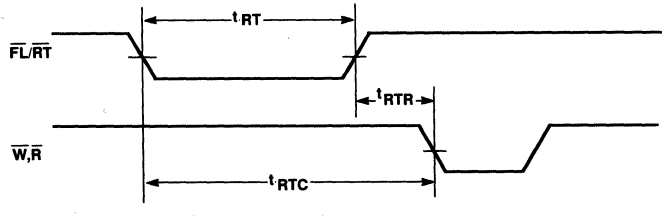
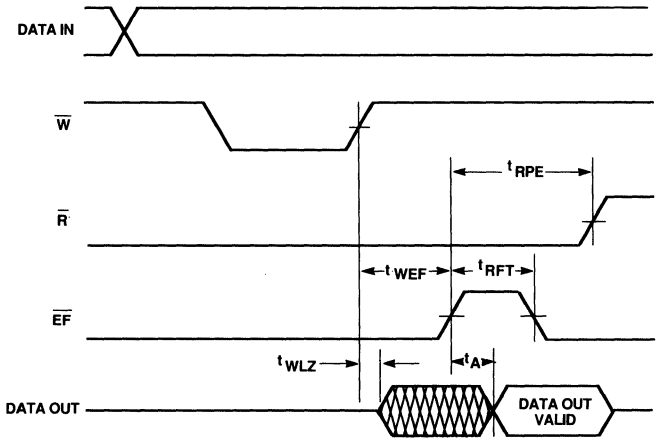


Figure 6. Full Flag Timing



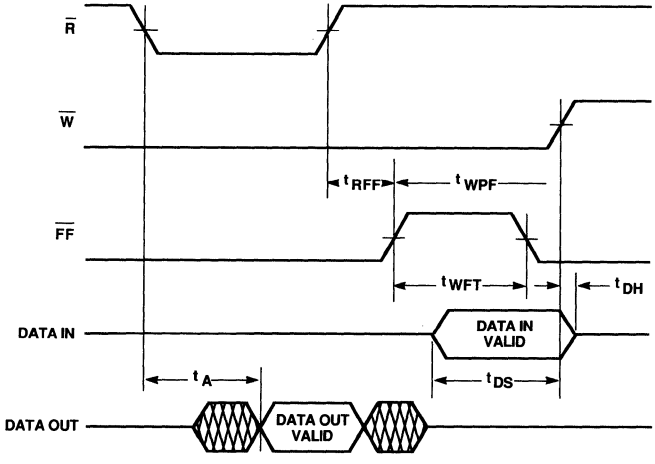
Note: $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during Retransmit as a result of the offset of the read and write pointers, but the flags will be valid at tRTC.

Figure 7. Retransmit Timing



Note: ($t_{RPE} = t_{RPW}$, $t_{RFT} = t_{REF}$)

Figure 8. Read Data Flow Through Mode



Note : ($t_{WPF} = t_{WPW}$, $t_{WFT} = t_{WFF}$)

Figure 9. Write Data Flow Through Mode

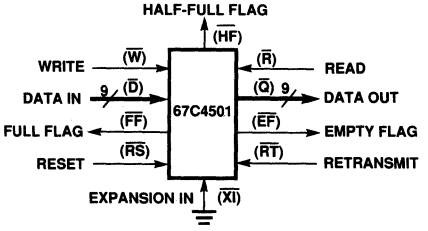


Figure 10. Single FIFO Configuration

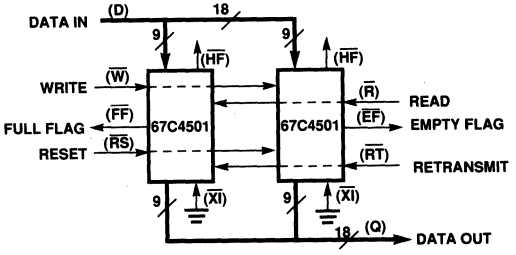


Figure 11. Width-Expansion to Form a 512x18 FIFO

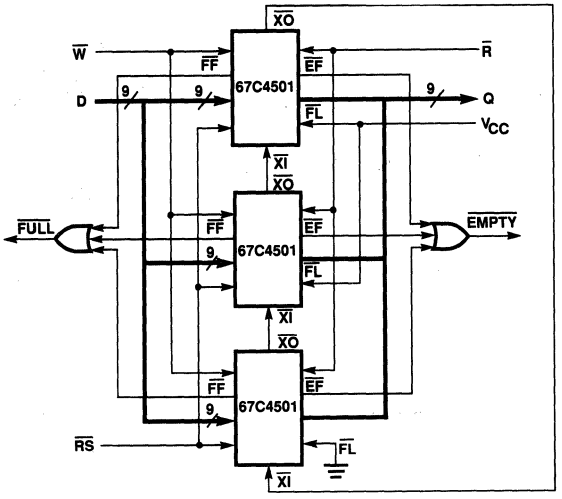


Figure 12. Depth-Expansion to Form a 1536x9 FIFO

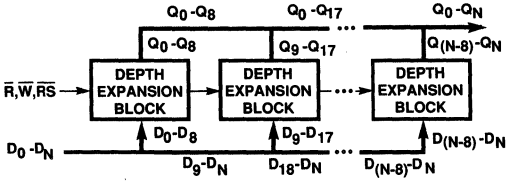


Figure 13. FIFO Array Using Both Width-Expansion and Depth-Expansion Techniques

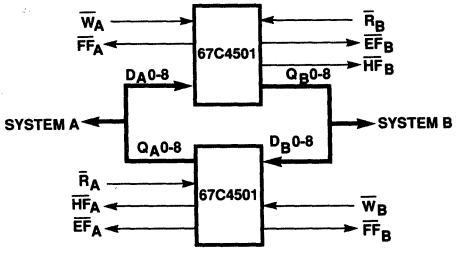
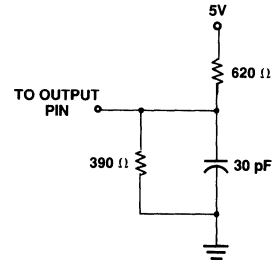


Figure 14. Bidirectional FIFO Mode

AC Test Conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V
Output load	See Figure 15



*Includes jig and scope capacitances.

Figure 15. A.C. Test Load

Capacitance (T_A = +25°C, f = 1.0 MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP	UNITS
C_{in}	Input capacitance	V_{in} = 0 V	5	pF
C_{out}	Output capacitance	V_{out} = 0 V	7	pF

Note:
1. For reference only.

2

67C4502-35/50/65/80

Deep First-in First-out (FIFO)
1024x9 CMOS Memory

DISTINCTIVE CHARACTERISTICS

- **RAM based FIFO**
- **1024x9 organization**
- **Cycle times of 45/65/80/100 nanoseconds**
- **Asynchronous and simultaneous writes and reads**
- **Low power consumption — 60 mA maximum**
- **Status flags - full, half-full, empty**
- **Retransmit capability**
- **Expandable in both width and depth**
- **Increased noise immunity for $\overline{XI}$ - CMOS threshold**
- **Functional and pin compatible with industry standard devices**

GENERAL DESCRIPTION

The 67C4502 is a RAM-based CMOS FIFO that is 1024 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 22 MHz. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

Deep FIFOs such as the 67C4502 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the 67C4502 useful in communication, image processing, mass storage, DSP, and printing systems.

BLOCK DIAGRAM

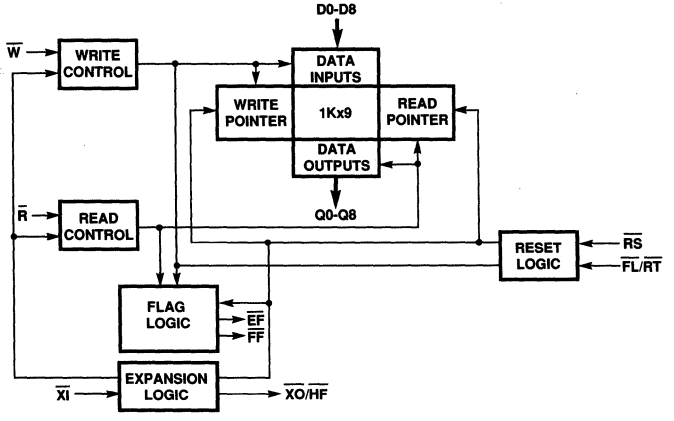


Figure 1.

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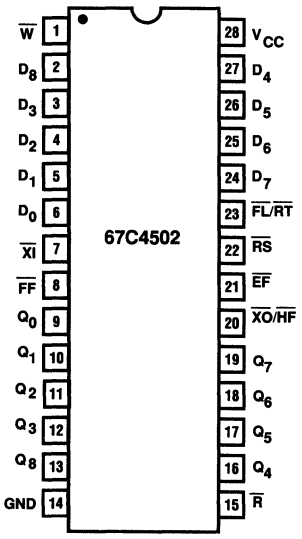
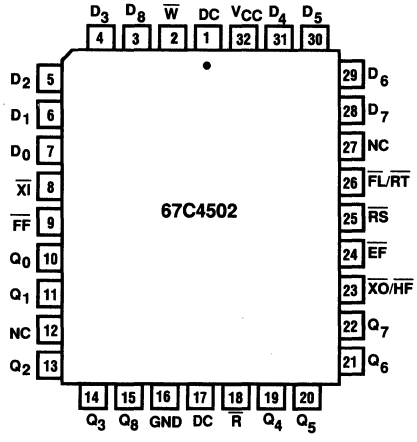
CONNECTION DIAGRAMS

DIP



PLCC



Note: Pin 1 is marked for orientation.

Pin Designations: $\overline{W}$ = Write
$\overline{R}$ = Read
$\overline{RS}$ = Reset
$\overline{FL}/\overline{RT}$ = First Load/Retransmit
D_x = Data In
Q_x = Data Out
$\overline{XI}$ = Expansion In
$\overline{XO}/\overline{HF}$ = Expansion Out/Half-Full Flag
$\overline{FF}$ = Full Flag
$\overline{EF}$ = Empty Flag
V_{CC} = Supply Voltage
GND = Ground

ORDERING INFORMATION

Standard Products

AMD/MMI standard products are available in several packages. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Operating Conditions
d. Package Type

67 C 4502 - 50 N

c. OPERATING CONDITIONS
67 = Commercial (0°C to 70°C)

CMOS TECHNOLOGY

a. PART NUMBER

b. PERFORMANCE
35 = 35 ns t_A
50 = 50 ns t_A
65 = 65 ns t_A
80 = 80 ns t_A

d. PACKAGE TYPE
N = Plastic DIP
J = Ceramic DIP
NL = Plastic Leaded Chip Carrier

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC} ..... -0.5 V to +7.0 V
Input voltage ..... -0.5 V to V_{CC} +0.5 V
Operating temperature ..... 0°C to +70°C
Storage temperature ..... -55°C to +150°C
Power dissipation ..... 1.0 W
DC output current ..... 50 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC CHARACTERISTICS Commercial: V_{CC} = 5 V ±10%, T_A = 0°C to +70°C

Parameter Symbol	Parameter Description	67C4502-35 T_A = 35 ns		67C4502-50 T_A = 50 ns		67C4502-65 T_A = 65 ns		67C4502-80 T_A = 80 ns		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I_{IL}	Input Leakage Current (any input) (Note 1)	-1	1	-1	1	-1	1	-1	1	µA
I_{IO}	Output Leakage Current (data outputs) (Note 2)	-10	10	-10	10	-10	10	-10	10	µA
V_{IH}	Input High Voltage (all inputs except $\overline{XI}$) (Note 3)	2.0	–	2.0	–	2.0	–	2.0	–	V
V_{IL}	Input Low Voltage (all inputs except $\overline{XI}$) (Note 3)	–	0.8	–	0.8	–	0.8	–	0.8	V
V_{IHXI}	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	–	3.5	–	3.5	–	3.5	–	V
V_{ILXI}	Input Low Voltage, $\overline{XI}$ (Note 3)	–	1.5	–	1.5	–	1.5	–	1.5	V
V_{OH}	Output Logic "1" Voltage I_{OH} = -2 mA	2.4	–	2.4	–	2.4	–	2.4	–	V
V_{OL}	Output Logic "0" voltage I_{OL} = 8 mA	–	0.4	–	0.4	–	0.4	–	0.4	V
I_{CC1}	Average V_{CC} Power Supply Current (Note 4)	–	60	–	60	–	60	–	60	mA
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}) (Note 4)	–	20	–	20	–	20	–	20	mA
I_{CC3}	Power Down Current (all inputs = V_{CC} -0.2 V) (Note 4)	–	5	–	5	–	5	–	5	mA

Notes:
1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. These are absolute voltage levels with respect to the ground pins on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

AC CHARACTERISTICS V_{CC} = 5 V ±10%, T_A = 0°C to +70°C

Parameter Symbol	Parameter Description	Figures	67C4502-35 Min.	67C4502-35 Max.	67C4502-50 Min.	67C4502-50 Max.	67C4502-65 Min.	67C4502-65 Max.	67C4502-80 Min.	67C4502-80 Max.	Unit
Write and Flag Timing											
t_{WC}	Write Cycle Time	3	45		65		80		100		ns
t_{WPW}	Write Pulse Width	3	35		50		65		80		ns
t_{WR}	Write Recovery Time	3	10		15		15		20		ns
t_{DS}	Data Setup Time	3,9	25		30		30		40		ns
t_{DH}	Data Hold Time	3,9	0		5		10		10		ns
t_{WFF}	Write LOW to Full Flag LOW	6,9		30		45		60		60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	5		45		65		80		100	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	4,8		30		45		60		60	ns
t_{WLZ}	Write pulse HIGH to data bus at LOW Z (Note 1)	8	10		15		15		20		ns
Read and Flag Timing											
t_{RC}	Read Cycle Time	3	45		65		80		100		ns
t_A	Access Time	3,4,8,9		35		50		65		80	ns
t_{RR}	Read Recovery Time	3	10		15		15		20		ns
t_{RPW}	Read Pulse Width	3	35		50		65		80		ns
t_{RLZ}	Read pulse LOW to data bus at LOW Z (Note 1)	3	5		10		10		10		ns
t_{DV}	Data Valid from read pulse HIGH	3	5		5		5		5		ns
t_{RHZ}	Read pulse HIGH to data bus at HIGH Z (Note 1)	3		20		30		30		30	ns
t_{RFF}	Read HIGH to Full Flag HIGH	6,9		30		45		60		60	ns
t_{RHF}	Read HIGH to Half Full-Flag HIGH	5		45		65		80		100	ns
t_{REF}	Read LOW to Empty Flag LOW	4,8		30		45		60		60	ns
Reset Timing											
t_{RSC}	Reset Cycle Time	2	45		65		80		100		ns
t_{RS}	Reset Pulse Width	2	35		50		65		80		ns
t_{RSS}	Reset Setup Time	2	35		50		65		80		ns
t_{RSR}	Reset Recovery Time	2	10		15		15		20		ns
t_{EFL}	Reset to Empty Flag LOW	2		45		65		80		100	ns
t_{HFH}	Reset to Half-Full Flag High	2		45		65		80		100	ns
t_{FFH}	Reset to Full Flag HIGH	2		45		65		80		100	ns
Retransmit Timing											
t_{RTC}	Retransmit Cycle Time	7	45		65		80		100		ns
t_{RT}	Retransmit Pulse Width	7	35		50		65		80		ns
t_{RTR}	Retransmit Recovery Time	7	10		15		15		20		ns

Note: 1. Characterized parameters.

FUNCTIONAL DESCRIPTION

The 67C4502 CMOS FIFO is designed around a 1024x9 dual-port static RAM array. (See Figure 1.) RAM-based FIFOs store the data written into them in a sequential pattern.

The dual-port RAM array has dedicated write and read address pointers. The flag logic prevents illogical writes and reads from occurring. The Empty Flag prevents reading while empty, which is a data underflow condition, while the Full Flag prevents writing while full, which is a data overflow condition. Once data that has been stored at a given address is read, it can be overwritten.

Address pointers automatically overflow to address zero after reaching address 1023. Thus the flag status of the FIFO is a function of the difference between the pointers, not their absolute value.

Resetting the FIFO simply initializes both address pointers to address zero. Pulsing Retransmit initializes the read address pointer to zero without affecting the write address pointer.

Expansion Logic is used when implementing a FIFO of a depth greater than that of the 67C4502. The write, read, data-in and data-out lines of the 67C4502 are connected in parallel, and the Expansion-Out ($\overline{XO}$) and the Expansion-In ($\overline{XI}$) lines are daisy-chained together. The write and read control circuits of the individual FIFOs are automatically enabled and disabled through the handshake between $\overline{XO}$ and $\overline{XI}$.

OPERATIONAL DESCRIPTION

Resetting The FIFO

Upon power up, the FIFO must be initialized with a Reset cycle. (See Figure 2.) The states of $\overline{XI}$ and $\overline{FL}$ are used during the reset cycle to determine the FIFO's mode of operation, as shown in Tables 1 and 2. For a valid reset cycle to occur, both the Read ($\overline{R}$) and Write ($\overline{W}$) signals must be HIGH t_{RSS} prior to and t_{RSR} after the rising edge of Reset ($\overline{RS}$). The reset cycle initializes the FIFO to an empty condition, signified by the Empty Flag ($\overline{EF}$) being LOW, active, and both the Half-Full ($\overline{HF}$) and Full Flag ($\overline{FF}$) being HIGH, inactive.

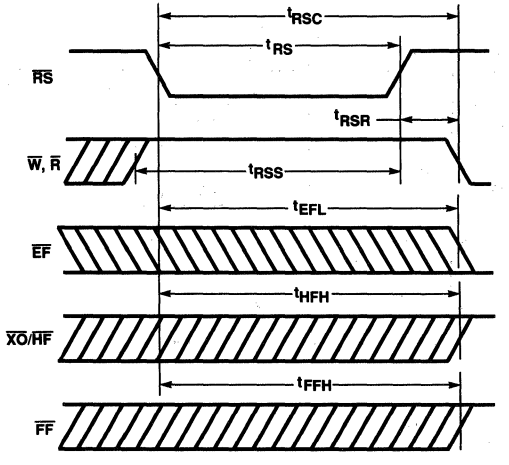


Figure 2. Reset Timing

Writing Data To The FIFO

The HIGH state of the Full Flag ($\overline{FF}$) indicates that the FIFO is capable of accepting data. The falling edge of Write ($\overline{W}$) initiates a write cycle. (See Figure 3.) Data appearing at inputs D0-D8 t_{DS} prior to and t_{DH} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The LOW- to-HIGH transition of the Empty Flag ($\overline{EF}$) occurs t_{WEF} after the rising edge of $\overline{W}$ during the first write cycle on an empty FIFO. (See Figure 4.) The Half-Full Flag ($\overline{HF}$) will go LOW t_{WHF} after the falling edge of $\overline{W}$ during the write operation which creates the half-full condition. (See Figure 5.) $\overline{HF}$ will remain LOW, while the number of writes to the FIFO exceeds the number of reads by 512 or more. The Half-Full Flag is not available in Depth-Expansion Mode. The Full Flag ($\overline{FF}$) goes LOW t_{WFF} after the falling edge of $\overline{W}$ during the write cycle which creates a full condition. (See Figure 6.) A full condition exists when there have been 1024 more write cycles than read cycles. The Full Flag being active prohibits any further write operations, thus preventing data overflow situations.

Reading Data From The FIFO

The HIGH state of the Empty Flag ($\overline{EF}$) indicates that the FIFO is ready to output data. The falling edge of Read ($\overline{R}$) initiates a read cycle. (See Figure 3.) Valid data appears on the outputs Q0-Q8 t_A after the falling edge of $\overline{R}$, and remains until t_{DV} after the rising edge of $\overline{R}$. Q0-Q8 return to a high-impedance state when a valid read is not in progress.

The Full Flag ($\overline{FF}$) will go HIGH t_{RFF} after the rising edge of $\overline{R}$ during the first read cycle following a full condition. (See Figure 6.) The Half-Full Flag ($\overline{HF}$) will go HIGH t_{RHF} after the rising edge of $\overline{R}$ during the read operation, which eliminates the half-full condition. (See Figure 5). $\overline{HF}$ will remain HIGH, while the number of writes to the FIFO exceeds the number of reads by 511 or less. The Half-Full Flag is not available in Depth-Expansion Mode. The HIGH-to-LOW transition of $\overline{EF}$ occurs t_{REF} after the falling edge of $\overline{R}$ during the read cycle, which creates an empty condition. (See Figure 4.) An empty condition exists when there has been an equal number of write cycles and read cycles. The Empty Flag being active prohibits any further read operations, thus preventing a data underflow situation.

Half-Full Flag

The Half-Full ($\overline{HF}$) Flag will be active LOW only when the net balance of the words written into the FIFO exceeds the number of words read out by 512 or more. (See Figure 5.)

Care should be exercised in using the Half-Full Flag, because it is capable of producing arbitrarily short pulses. For example, if the FIFO contains 512 words, and Read and Write pulses are applied simultaneously, the $\overline{HF}$ flag may produce an arbitrarily short pulse, depending on the precise phase of Read and Write.

$\overline{HF}$ will always settle to the correct state after the appropriate delay, t_{WHF} or t_{RHF}. This property of the Half-Full Flag is clearly a function of the dynamic relation between $\overline{W}$ and $\overline{R}$. Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

RESET AND RETRANSMIT TRUTH TABLE Single-Device Configuration/Width-Expansion Mode

Mode	Input			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X (Note 1)	X (Note 1)	X (Note 1)
Read/Write	1	1	0	Increment (Note 2)	Increment (Note 2)	X	X	X

Notes: 1. Flags will change to show correct state according to write pointer.
2. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 1.

RESET AND FIRST LOAD TRUTH TABLE Depth-Expansion/Compound-Expansion Mode

Mode	Input			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset–first device	0	0	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Reset all other devices	0	1	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Read/Write	1	X (Note 2)	$\overline{XO}$ (Note 1)	Increment (Note 3)	Increment (Note 3)	X	X

Notes: 1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12.
2. Same as during Reset Cycle.
3. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 2.

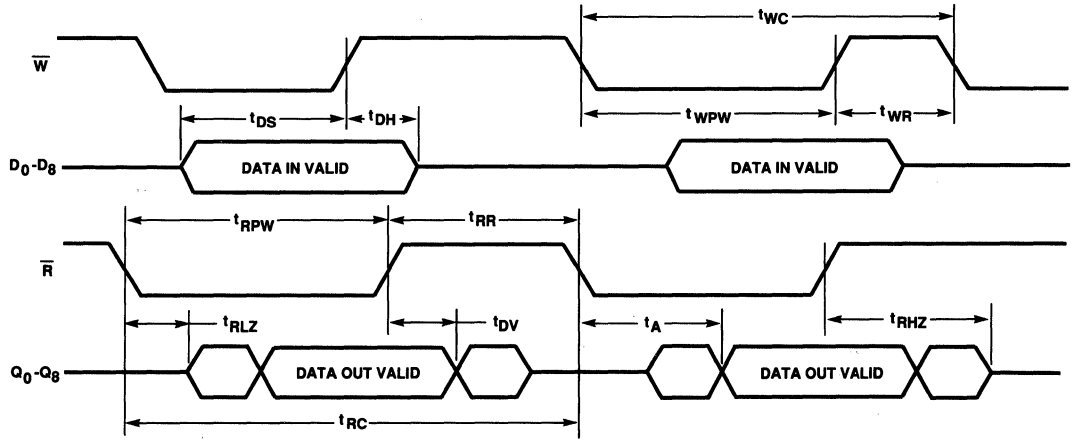


Figure 3. Asynchronous Write and Read Timing

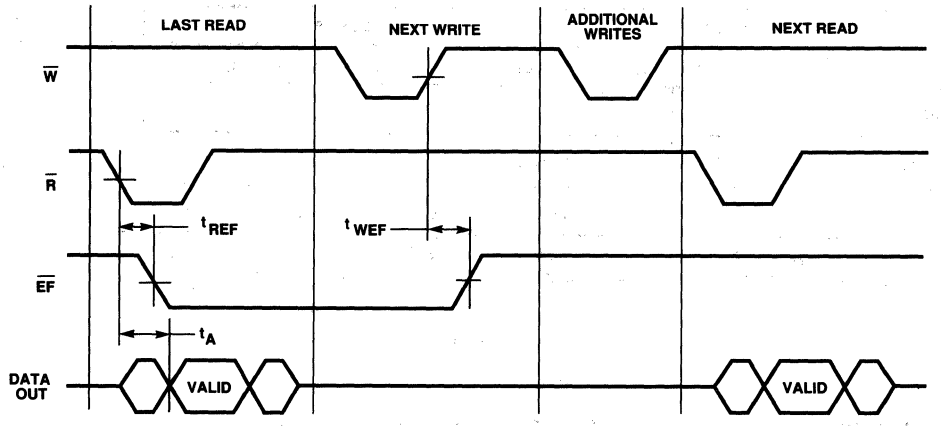
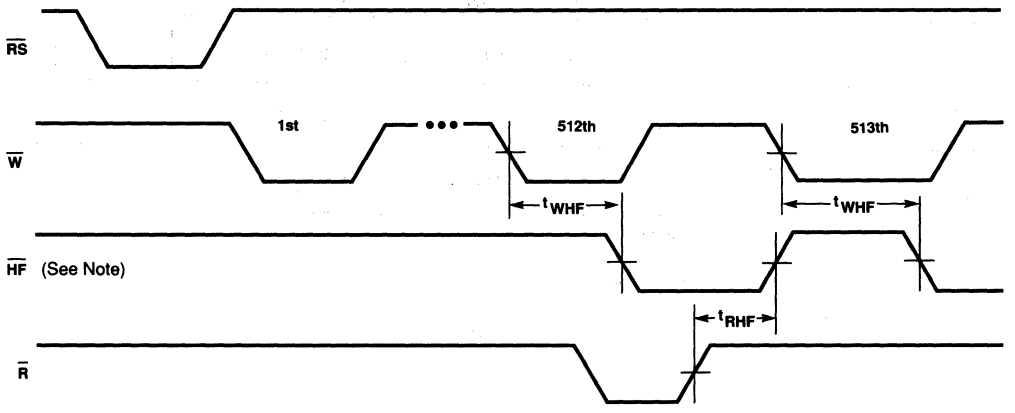


Figure 4. Empty Flag Timing



Note: Depending on the precise phase of $\overline{W}$ and $\overline{R}$, the Half-Full Flag may appear as a pulse of arbitrarily short duration of either polarity when $\overline{W}$ and $\overline{R}$ are operating asynchronously near half full.

Figure 5. Half-Full Flag Timing

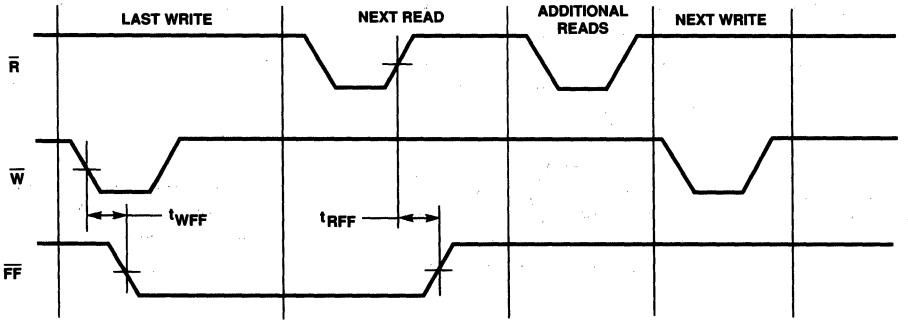


Figure 6. Full Flag Timing

Retransmit

The retransmit function resets the read address pointer allowing the data that was previously read to be read again. This capability is useful when the block of data being transferred through the FIFO doesn't exceed the FIFO's depth and is intended for use when there are 1024 or less writes between reset cycles.

The $\overline{FL}/\overline{RT}$ is used as the Retransmit ($\overline{RT}$) input in Single-Device Mode. $\overline{RT}$, an active LOW-going pulse of at least t_{RT} in duration, returns the internal read pointer to address zero and leaves the write pointer unaffected. $\overline{W}$ and $\overline{R}$ must both be HIGH during the retransmit cycle. The first write or read cycle should not start until t_{RTR} after the rising edge of $\overline{RT}$. The flags may change state during this cycle, but they will accurately reflect the new state of the FIFO t_{RTC} after the falling edge of $\overline{RT}$. (See Figure 7 and Table 1).

Single-Device/Width-Expansion Modes

Single-Device and Width-Expansion Modes are configured by grounding the Expansion-In ($\overline{XI}$) input. (See Figures 10 and 11, and Table 1.) During these modes of operation, the Half-Full Flag and Retransmit features are available. The 67C4502 can be expanded in width to create FIFOs of word widths greater than nine bits. In Width-Expansion Mode all of the control line inputs are common to all devices. (See Figure 11.) Creating composite status flags can pose two hazards. 1.) OR-ing the flag outputs is fine for the HIGH-to-LOW transition, because the skew between devices is masked out. However, when the flags make a LOW-to-HIGH transition, a false composite flag is generated. 2.) The converse is true when the flags are AND-ed: the LOW-to-HIGH transition is fine, and the HIGH-to-LOW generates a false flag. These two hazards can be avoided if one device's flags are used as the flags for the expanded FIFO, and the write control circuitry and read control circuitry is designed to hold off sampling the flags until the worst case settling time (t_{WEF}, t_{WHF}, t_{WFF}, t_{REF}, t_{RHF}, and t_{WFF}) for each flag has elapsed.

Depth-Expansion Mode

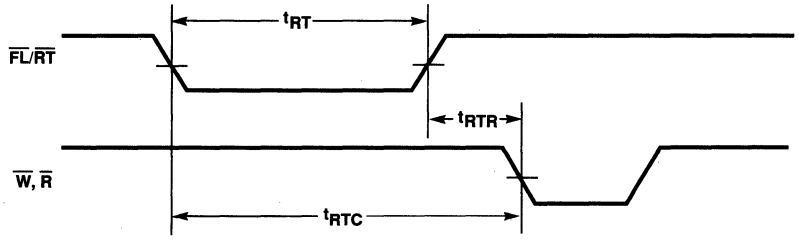
Depth-Expansion Mode is configured during the Reset cycle. (See Figure 12 and Table 2.) Expansion Out ($\overline{XO}$) of one device must be connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device being connected to $\overline{XI}$ of the first device. The device that is to receive data first has its First Load ($\overline{FL}$) input tied LOW, while all other devices must have this input HIGH. Write and read control is passed between devices using $\overline{XO}$ and $\overline{XI}$. A LOW-going pulse on $\overline{XO}$ occurs when the last physical location of an active device, address 1023, is written to, and another LOW-going pulse occurs when the last physical location of an active device is read. Only one device is enabled for writes, and only one device is enabled for reads at any given time.

When expanding in depth, a composite Full Flag must be created by OR-ing all the $\overline{FF}$ outputs together. Likewise, a composite Empty Flag is created by OR-ing all the $\overline{EF}$ outputs together. The Half-Full Flag and Retransmit functions are not available in Depth-Expansion Mode.

Compound Expansion

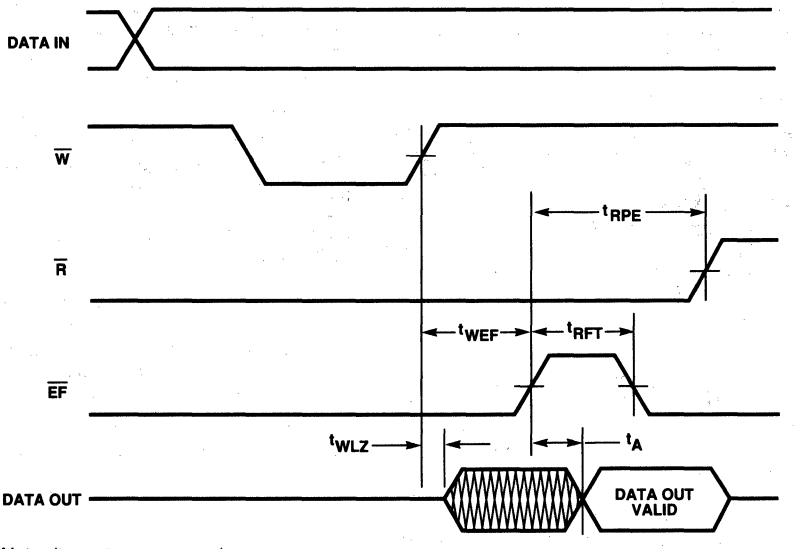
FIFOs of greater width and depth than the 67C4502 can be created by using both Width-Expansion Mode and Depth-Expansion Mode simultaneously. (See Figure 13.)

2



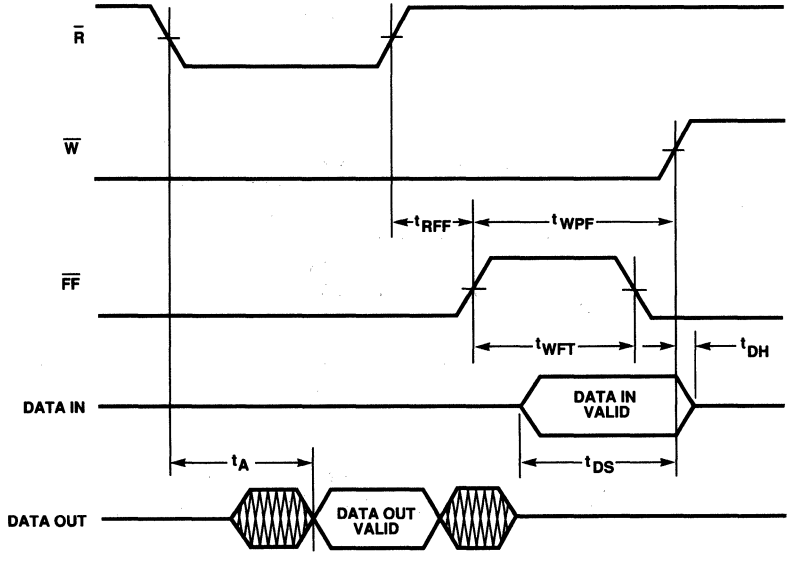
Note: $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during Retransmit as a result of the offset of the read and write pointers, but the flags will be valid at t_{RTC}.

Figure 7. Retransmit Timing



Note: ($t_{RPE} = t_{RPW}$, $t_{RFT} = t_{REF}$)

Figure 8. Read Data Flow Through Mode



Note: ($t_{WPF} = t_{WPW}$, $t_{WFT} = t_{WFF}$)

Figure 9. Write Data Flow Through Mode

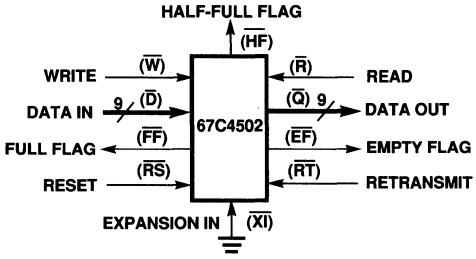


Figure 10. Single FIFO Configuration

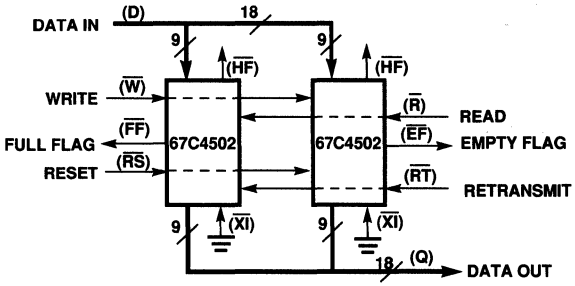


Figure 11. Width-Expansion to Form a 1024x18 FIFO

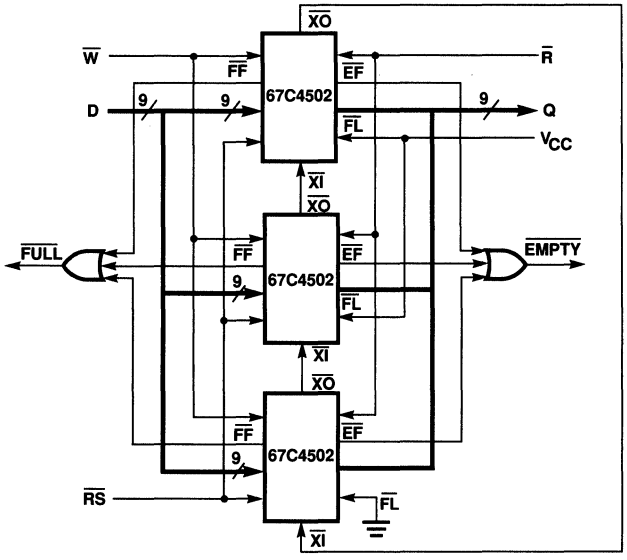


Figure 12. Depth-Expansion to Form a 3072x9 FIFO

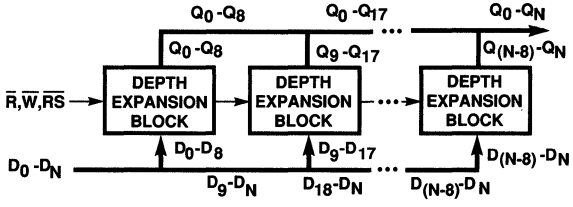


Figure 13. FIFO Array Using Both Width-Expansion and Depth-Expansion Techniques

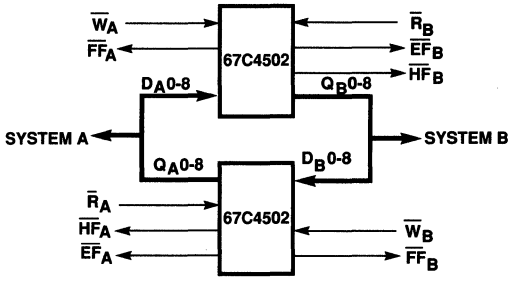
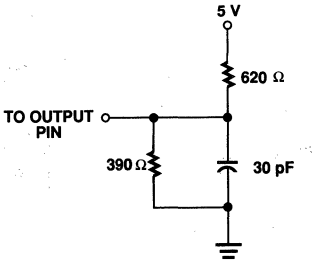


Figure 14. Bidirectional FIFO Mode

AC TEST CONDITIONS

Input pulse levels	GND to 3.0 V
Input rise and fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V
Output load	See Figure 15



* Includes jig and scope capacitances.

Figure 15. A.C. Test Load

CAPACITANCE (T_A = + 25°C, f = 1.0 MHz)

Symbol	Parameter (Note 1)	Conditions	Typ.	Unit
C_{IN}	Input capacitance	V_{IN}= 0 V	5	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V	7	pF

Note: 1. For reference only.

Serializing First-In-First-Out (FIFO) 64x8/9 Memory

67417

Features/Benefits

- **High-speed 28-MHz serial shift-in/shift-out rate**
- **10-MHz parallel shift-in/shift-out rate**
- **Three-state outputs with Hi-current drive**
- **Cascadable at parallel port only**
- **Half-full flag (32 or more)**
- **Selectable 64x8 or 64x9 FIFO configuration thus providing "frame mark bit"**

Typical Applications

- **LAN equipment**
- **Data communication**
- **Office automation**
- **Microcomputers**
- **Minicomputers**
- **Disk/tape controllers**

Description

The 67417 is a serializing/deserializing FIFO. This FIFO, the first one of its type in the industry, is organized 64 words x 8/9 bits wide. Like traditional Monolithic Memories' FIFOs it is cascadable, but only at the parallel port.

Ordering Information

PART NUMBER	PACKAGE	TEMPERATURE	DESCRIPTION
67417	J	Com	64x8/9

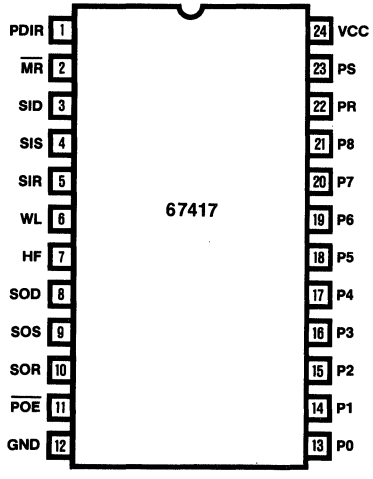
In addition, the device has the ability to connect directly to a system bus. These features make it a complete "sub-system on a chip."

The FIFO basically has three modes of operation;

1. Serial in to parallel out
2. Parallel in to serial out
3. Serial in to serial out (requires non-standard logic level on PDIR).

In the first mode, serial data can be accepted at up to 28 MHz and the FIFO outputs parallel data at up to 10 MHz. Similarly, in the alternate mode parallel data can be transformed into serial data. Please refer to appendix for detailed description.

Pin Configuration



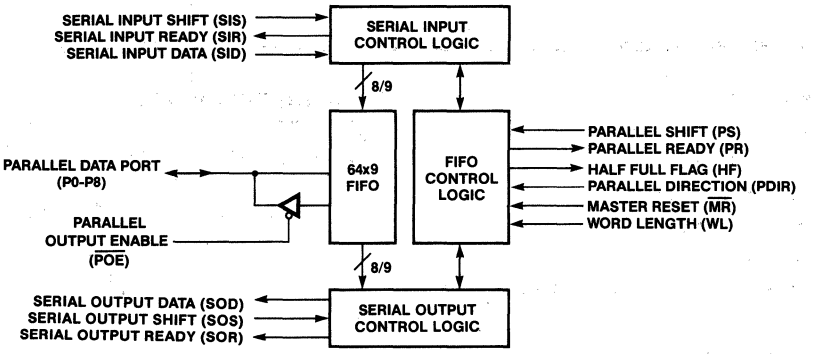
Pin Names

P0-P8	Parallel Data
PS	Parallel Shift In/Out
PR	Parallel Input/Output Ready
$\overline{POE}$	Parallel Output Enable
SID	Serial Input Data
SIS	Serial Input Shift
SIR	Serial Input Ready
SOD	Serial Output Data
SOS	Serial Output Shift
SOR	Serial Output Ready
PDIR	Parallel Port Direction
WL	Word Length
$\overline{MR}$	Master Reset
HF	Half Full Flag
VCC	VCC
GND	Ground

Publication #	Rev.	Amendment
10680	A	/0

Issue Date: **May 1988**

Block Diagram



Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150° C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
	SERIAL INPUT PARAMETERS					
f_{SIN}	Max. Serial Shift-In Rate	1			28	MHz
t_{SISH}	Serial Shift-In HIGH time	1	23			ns
t_{SISL}	Serial Shift-In LOW time	1	12			ns
t_{SIDS}	Serial Input Data Setup time	1	14			ns
t_{SIDH}	Serial Input Data Hold time	1	0			ns
t_{SIRHS}	Recovery Time Serial Input Ready ↑ to Serial Input Shift ↑	1	0			ns
	SERIAL OUTPUT PARAMETERS					
f_{SOUT}	Max. Serial Shift-Out Rate	1			28	MHz
t_{SOSH}	Serial Shift-Out HIGH time	3	15			ns
t_{SOSL}	Serial Shift-Out LOW time	3	15			ns
t_{ORHS}	Recovery time Serial Output Ready ↑ to Serial Output Shift ↑	3	5			ns
	WORD LENGTH PARAMETERS					
t_{SWL}	Setup SIS, SOS	1,3	18			ns
t_{HWL}	Hold SIS, SOS	1,3	3			ns
	PARALLEL PORT PARAMETERS					
f_P	Parallel shift-in/shift-out rate	8			10	MHz
t_{PSH}	Parallel Shift-In/Out HIGH time	5/8	30			ns
t_{PSL}	Parallel Shift-In/Out LOW time	5/8	30			ns
t_{PIDS}	Parallel Input Data Setup time	5	-5			ns
t_{PIDH}	Parallel Input Data hold time	5	35			ns
t_{PDIRSL}	Shift LOW to parallel direction transition	14	50			ns
t_{PDIRSH}	Parallel direction transition to Shift HIGH	14	50			ns
t_{PRHS}	Parallel Ready ↑ to Parallel Shift Low	10/11	30			ns
	MASTER RESET PARAMETER					
t_{MRW}	Master Reset LOW time	12/13	40			ns

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
	SERIAL INPUT PARAMETERS					
t_{SIRL}	Serial Input Shift ↑ to Serial Input Ready LOW	2			23	ns
t_{SIHFH}	Serial Input Shift ↑ to Half-Full Flag HIGH	7			1.3	µs
	SERIAL OUTPUT PARAMETERS					
t_{SORL}	Serial Output Shift ↑ to Serial Output Ready LOW	4			23	ns
t_{SOD}	Serial Output Shift ↑ to Serial Output data	3			23	ns
t_{ODRH}	Serial Output Data valid to Serial Output Ready HIGH	3	0	25		ns
t_{SOHFL}	Serial Output Shift ↑ to Half-Full LOW	7			1.3	µs
	PARALLEL INPUT/OUTPUT PARAMETERS					
t_{PSPRL}	Parallel Shift ↑ to Parallel Ready LOW	5/8			65	ns
t_{PSPRH}	Parallel Shift ↓ to Parallel Ready HIGH	5/8/10			80	ns
t_{PSHFH}	Parallel Shift-In ↓ to Half-Full HIGH	6			1.3	µs
t_{PSHFL}	Parallel Shift-Out ↓ to Half-Full LOW	9			1.3	µs
	PARALLEL OUTPUT PARAMETERS					
t_{PODH}	Minimum Parallel Shift ↓ to Ouput data	8	20			ns
t_{POD}	Maximum Parallel Shift ↓ to Output data	8			60	ns
t_{PODV}	Minimum Output data valid to parallel ready HIGH	8	0	15		ns
	OTHER PARAMETERS					
t_{PT}	Fall-through time	10/11/16/17			2.6	µs
t_{IPH}	Parallel Input Ready pulse HIGH	11	30			ns
t_{OPH}	Parallel Output Ready pulse HIGH	10	30			ns
t_{MRO}	$\overline{\text{Master Reset}}$ ↓ to Data Out LOW	12			65	ns
t_{MRSIRL}	$\overline{\text{Master Reset}}$ ↓ to Serial Input Ready LOW	12			40	ns
t_{MRSIRH}	$\overline{\text{Master Reset}}$ ↑ to Serial Input Ready HIGH	12			40	ns
t_{MRPRL}	$\overline{\text{Master Reset}}$ ↓ to Parallel Ready LOW	12/13			40	ns
t_{MRPRH}	$\overline{\text{Master Reset}}$ ↑ to Parallel Ready HIGH	13			30	ns
t_{MRSORL}	$\overline{\text{Master Reset}}$ ↓ to Serial Output Ready LOW	13			40	ns
t_{MRHFL}	Master Reset ↓ to Half-Full LOW	12/13			60	ns
t_{PDIROR}	Parallel Direction change to new Output Ready	14			60	ns
t_{PDIROD}	Parallel Direction change to Output data valid	14			60	ns
t_{PDIRPZ}	Parallel Direction change to Parallel Output data Hi-Z	14			35	ns
t_{PDIRSZ}	Parallel Direction changes to Serial Output-data Hi-Z	14			80	ns
t_{PZX}	Output enable time $\overline{\text{POE}}$ to P0-8	15			30	ns
t_{PXZ}	Output disable time $\overline{\text{POE}}$ to P0-8	15			35	ns

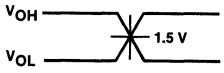
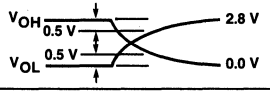
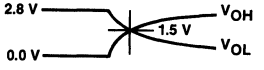
Electrical Characteristics Over Operating Conditions

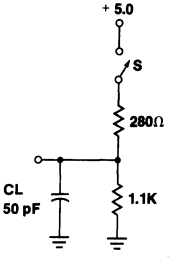
SYMBOL	PARAMETER	TEST CONDITIONS				COM MIN	COM TYP	COM MAX	UNIT
V_{IL}	Low-level input voltage							0.8†	V
V_{IH}	High-level input voltage					2†			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA					−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V					−0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V					0.1	mA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V					0.4	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Data Outputs P0-P8, SOD	I_{OL} = 24 mA	0°C-75°C			0.58	V
					25°C			0.55	
				I_{OL} = 16 mA	0°C-75°C			0.5	
			All other outputs	I_{OL} = 8 mA				0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3 mA			2.4			V
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0 V			−20		−90	mA
I_{LZ}	Off-state output current* SOD	V_{CC} = MAX	V_O = 0.4 V					−100	μA
I_{HZ}	Off-state output current* P0 to P8		V_O = 2.4 V					100	mA
I_{CC}	Supply current	V_{CC} = MAX						350	mA
O_V	PDIR non-standard over voltage	Serial-In, Serial-Out				10		16	V

* Not more than one output should be shorted at a time and duration of the short circuit not exceed one second.

† This is an absolute voltage with respect to device GND (pin 12) and includes all overshoots due to test equipment.

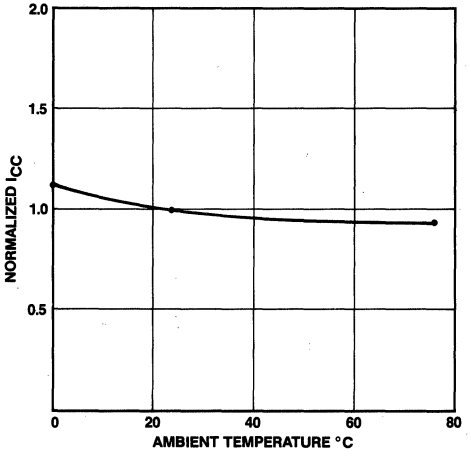
Test Waveforms

TEST	S = OPEN	S = CLOSED	OUTPUT WAVEFORM-MEAS-LEVEL
All t_{PD}		All t_{PD}	
t_{PXZ}	t_{PHZ}	t_{PLZ}	
t_{PZX}	t_{PZH}	t_{PZL}	

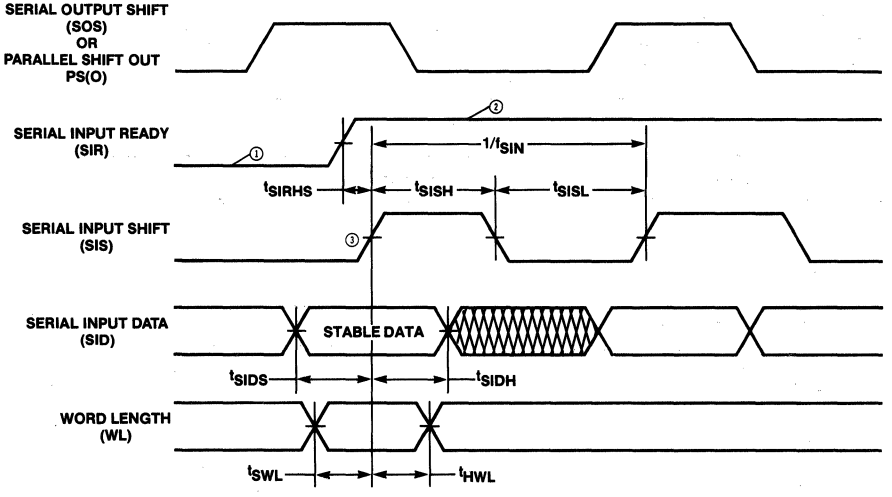


2

I_{CC} VS Temperature

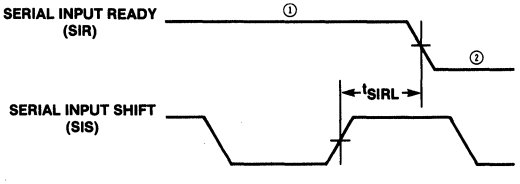


Definition of Waveforms



① FIFO is full.
② Shift-out (serial or parallel) is asserted, SIR goes High.
③ SIS can be asserted t_{SIRHS} after serial input ready changes from low-to-high.

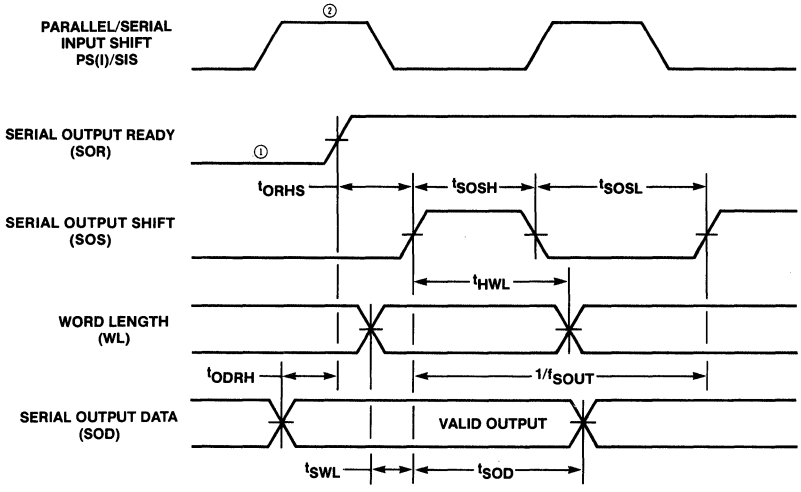
Figure 1. Serial Input Timing



① FIFO is not full.
② FIFO is full.

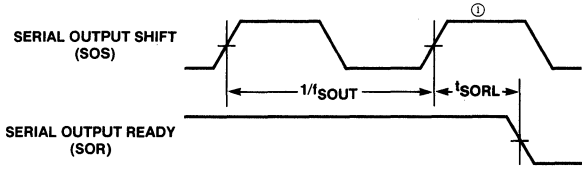
Figure 2. FIFO Full Specification (t_{SIRL})

Definition of Waveforms (cont'd)



① FIFO is empty, output ready remains Low and shift-out cannot be applied.
② After a word is shifted in, output ready goes High and shift-out can be applied.
③ The first serial bit is P0.

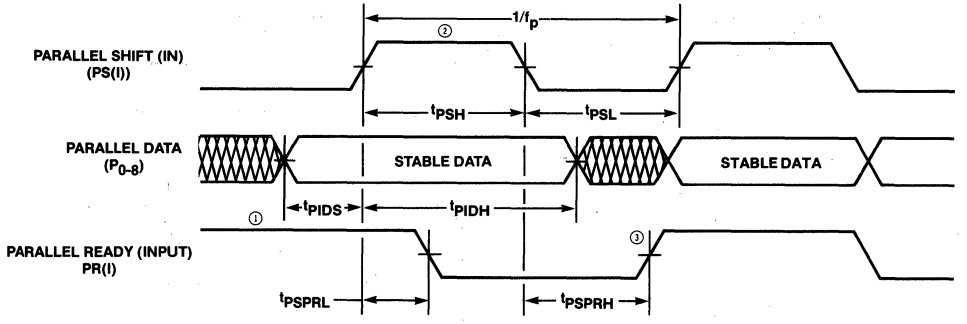
Figure 3. Serial Output Timing



① After the last shift-out, output ready goes Low indicating FIFO is empty.

Figure 4. FIFO Empty Specifications (t_{SORL})

Definition of Waveforms (cont'd)



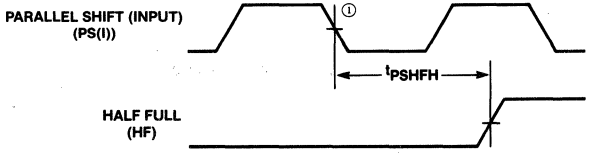
NOTE: P_{DIR} = High for the mode parallel-in to serial-out. Parallel ready is an output flag from the FIFO indicating that a word can be loaded into the FIFO.

① FIFO is not full and ready for input.

② PS (In) is asserted, shifting in parallel data P0-8.
PR (In) goes Low indicating parallel port is in use and no longer ready.
PR (In) will remain Low as long as PS (In) remains High.

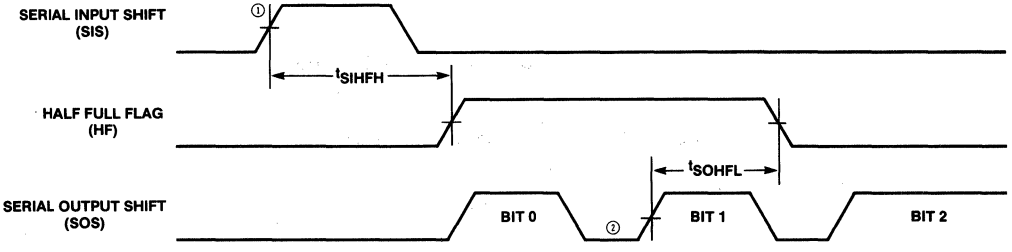
③ PS (In) has gone Low, allowing recent word to propagate through FIFO, PR (In) returns High when ready for more input.

Figure 5. Parallel Input Shift Timing



① for P_{DIR} = High, the direction is parallel-in to serial-out. After the 32nd shift-in, the half-full flag is set to High, and remains High, indicating the presence of 32 or more words.

Figure 6. Half-full Flag Specifications on Parallel (t_{PSHFH})

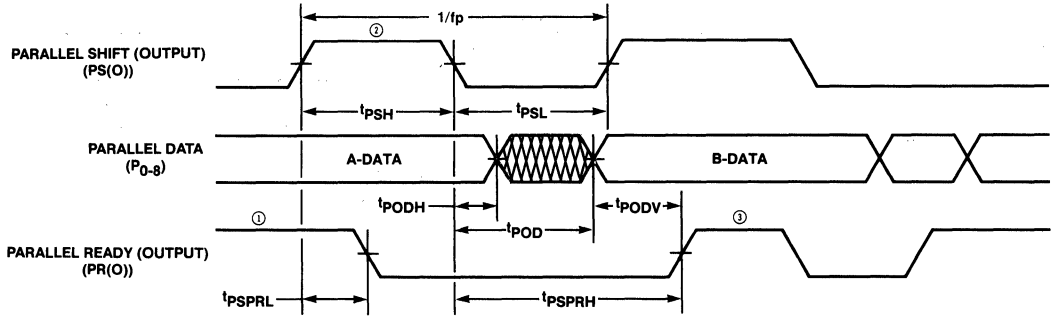


① When there are 31 words in the FIFO, the next shift-in on the 32nd word sets the half-full flag (HF) High indicating that there are 32 or more words.

② As soon as one word is partially shifted out, HF goes Low indicating there are less than 32 words.

Figure 7. Half-full Flag Specification on Serial Operation (t_{SIHFH}, t_{SOHFL})

Definition of Waveforms (cont'd)



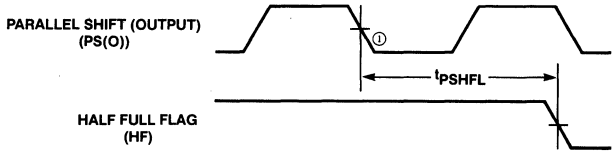
NOTE: For above conditions P_{DIR} = Low indicating that the direction is from serial-in to parallel-out. Thus parallel ready indicates the output status.

① FIFO is not empty and at least one word is valid and ready at P0-8 outputs.

② PS (Out) is asserted, shifting out parallel data. Data remains valid, but:
PR (Out) goes Low to indicate parallel port is in use and no longer ready.
PR (Out) will remain Low as long as PS (Out) remains High.

③ PS (Out) has gone Low, allowing data word to be shifted out. Next data word appears at output and PR (Out) is asserted to indicate valid data ready.

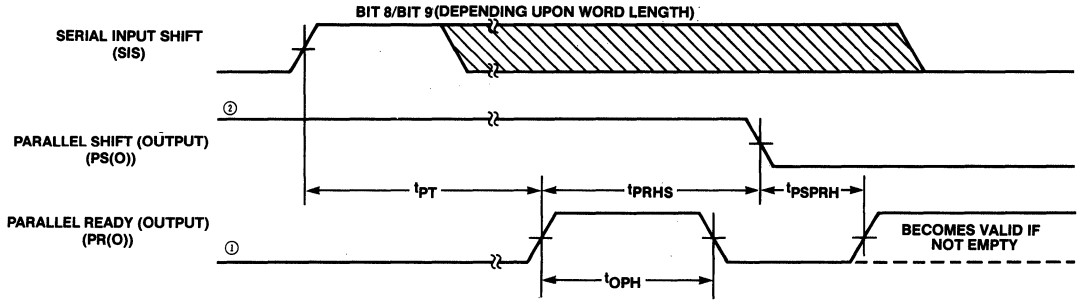
Figure 8. Serial-in to Parallel-out Specifications (t_{POD}, t_{PODH}, t_{ODV})



NOTE: For P_{DIR} = Low the direction is serial-in to parallel-out.

① When a word is shifted out and the half-full flag goes Low, 31 words or less are in the FIFO.

Figure 9. Half-full Flag Specification on Parallel Shift-out (t_{PSHFL})



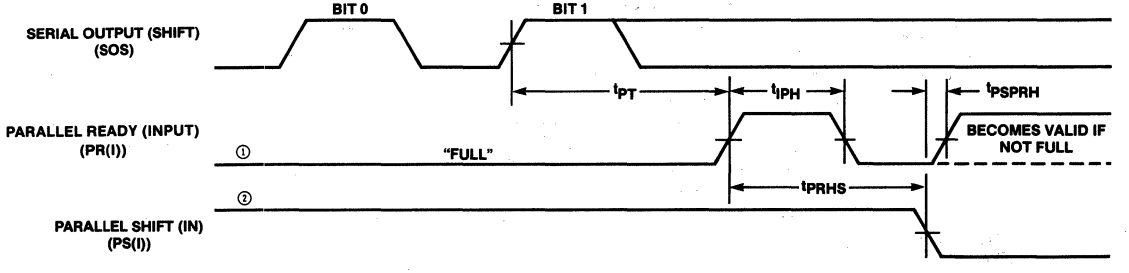
NOTE: P_{DIR} = Low indicating serial-in to parallel-out.

① FIFO initially empty.

② PS (Out) held High.

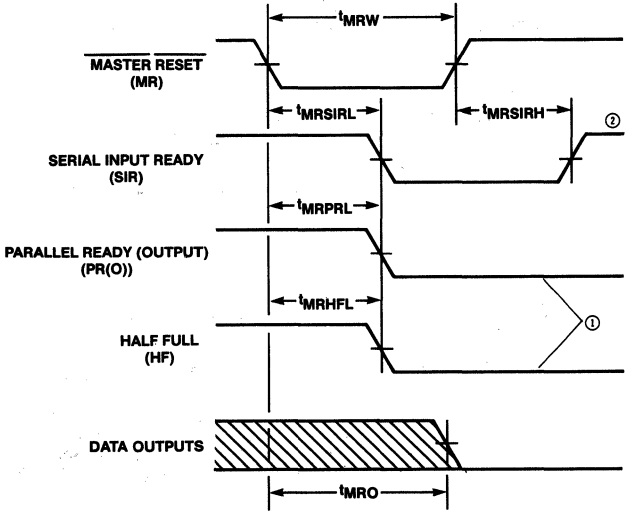
Figure 10. t_{PSPRH}, t_{PT}, t_{POH} Specifications (Serial Input Mode)

Definition of Waveforms (cont'd)



NOTE: P_{DIR} = High (parallel-in to serial-out).
① FIFO is full.
② PS (I) held High.

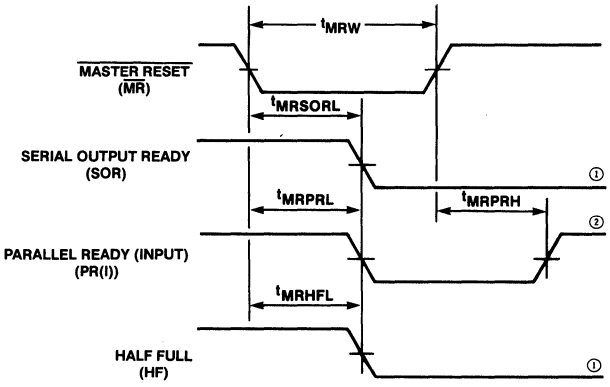
Figure 11. Fall-through Specifications



NOTE: P_{DIR} = Low.
① PR (O) and HF go Low.
② After $\overline{MR}$ goes High, SIR goes High.

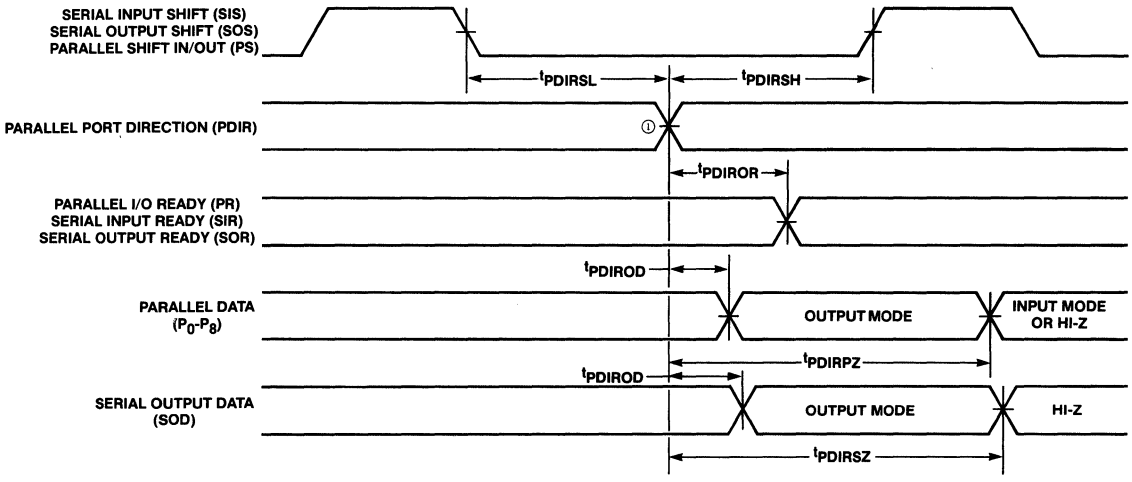
Figure 12. Master Reset Timing Serial-in to Parallel-out

Definition of Waveforms (cont'd)



NOTE: P_{DIR} = High.
① SOR and HF go Low.
② Affter $\overline{MR}$ goes High, PR(I) goes High.

Figure 13. Master Reset Timing (Parallel-in to Serial-out)



NOTE: When the FIFO is used as a stack, change the port direction before the FIFO is full; otherwise, data may be lost.

Figure 14. P_{DIR} Transition Parameters

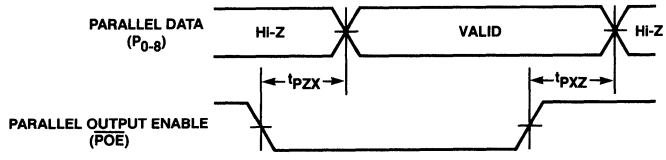


Figure 15. Parallel Port Enable and Disable Timing

Definition of Waveforms (cont'd)

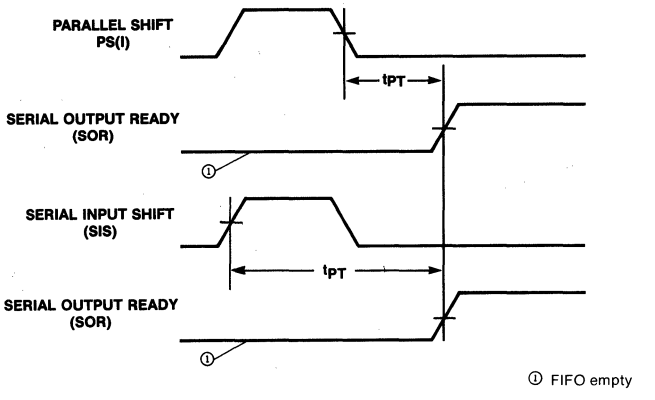


Figure 16. t_{PT} Specification (Shift-in to Serial Output Ready)

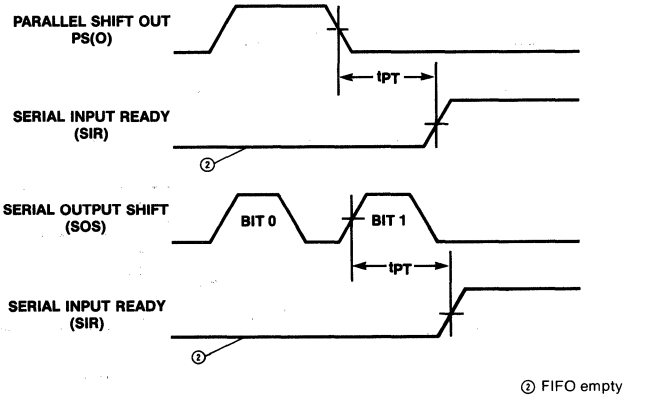


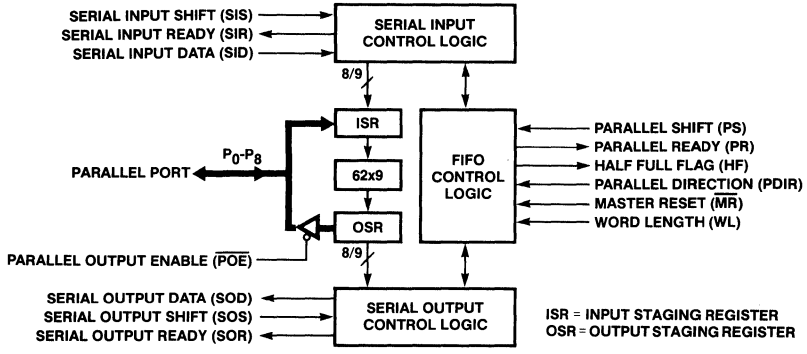
Figure 17. t_{PT} Specification (Shift-in to Serial Input Ready)

Appendix
Detailed Functional/Description for 67417

The 67417 is a serializing FIFO intended as a one-chip solution for data buffering and serializing/deserializing. It can be successfully used for interfacing parallel-format computing equipment to serial-format data communications and mass-memory equipment. The 67417 is a word-oriented device. It is meant to function with complete 8- or 9-bit words of data.

Parallel Port

This is a fully bidirectional port, and it operates at a more conservative data rate of 10 MHz. The input-staging register (ISR) internally controls the parallel input data port bus signals. Likewise the OSR internally controls the parallel output data port. The ISR data outputs drive the parallel data inputs to the cell array, and the OSR inputs are likewise driven by the final parallel data stage of the cell array



Basically the major internal subsystems of the 67417 are:

(i) The serial input port
(ii) The serial output port
(iii) The parallel port
(iv) The FIFO control logic and
(v) The cell array

Serial Port

The two serial ports (input and output) are entirely separate which allows a high-speed data rate of 28 MHz. These serial ports do not share data pins, control pins, or internal circuits. However, since the serial output data is a three-state output, the serial data ports could be connected together in the normal serial-parallel operation mode with separate SOR and SIR status signals.

The serial input port interface consists of the Serial Input Ready (SIR) output, Serial Input Data (SID) input, and the Serial Input Shift (SIS) clock input. Unlike the analogous SI and IR signals on the 67401/2, SIS and SIR do not accomplish a "handshake" with the rest of the logic of the system which incorporates the 67417; rather SIR is asserted whenever the 67417 is still capable of receiving at least one more bit. SIS is a positive edge-triggered input which sequences the serial input control logic. This logic in turn controls SIR and the 8/9-bit Input Staging Register (ISR).

The serial output port interface is the dual of the above, with a Serial Output Data (SOD) output, a Serial Output Shift (SOS) clock input, and a Serial Output Ready (SOR) status output. SOR is asserted whenever at least one more bit is available at the output. SOS is a positive edge-triggered input which sequences the 8/9-bit Output Staging Register (OSR). Serial Output Data is automatically three-stated whenever the serial output port is disabled (during Master Reset) and PDIR = Low. The parallel port is controlled by Parallel Shift (PS) input and Parallel Direction Input (PDIR). Parallel Ready (PR) is the handshake/status output. At the Parallel Port PS and PR *do* accomplish a handshake with the outside world as SI, IR, SO and OR on the 67401/2.

Modes of Operation

There are three modes in which the 67417 can operate

(i) Parallel-in to serial-out
(ii) Serial-in to parallel-out and
(iii) Serial-in to serial-out.

In the parallel-in to serial-out mode, PDIR = HIGH. Thus Parallel Shift (PS) acts as a Shift In (SI) and similarly, Parallel Ready (PR) as Input Ready (IR). The first bit shifted out of the serial port will be bit 0 of the parallel word input.

Similarly for serial-in to parallel-out mode, PDIR = LOW, and Parallel Shift (PS) acts as a Shift Out(SO) and Parallel Ready (PR) as Output Ready (OR). The first bit shifted into the serial port will be bit 0 of the parallel word output.

If the direction mode for a particular application of the 67417 is not intended to change during system operation, the PDIR input should be strapped to a logic LOW or HGH.

In the serial-in to serial-out mode, PDIR = 10 V minimum.

The parallel port does not function during this mode and is three-stated. The direction operating mode should not be changed if the FIFO is FULL otherwise stored data will be lost.

Cell Array

The 67417 cell array can function *either* as a 64x8 FIFO (with the 9th bit padded to a zero) or as a 64x9 FIFO, according to the setting of the word length (WL) control input. Like the PDIR

control input, WL can be switched at electronic speeds during system operations; but if the word length of a particular 67417 is *never* to change during system operation, WL for that part can be strapped to ground or V_{CC}.

It is a permissible 67417 mode of operation to almost fill the FIFO (there should be at least two empty locations) with WL set to 8-bit operation, then switch WL to 9-bit operation (WL = HIGH) to load one more word plus a frame marker in the last bit, and then switch PDIR and unload the 67417 in a 9-bit mode. This sequence of operations has the effect of providing a "frame marker bit" in the ninth bit of the last word loaded. The corresponding 9th bits will have been zeroed by the 67417 internal logic for all the other words in the frame since they were loaded while the 67417 was operating as an 8-bit device.

It is, however, the system designer's responsibility to avoid changing PDIR inputs when only part of an 8- or 9-bit word has been received or transmitted. In general, if such a change occurs, the part in general will try to add zero bits to pad out the impacted word to assume full length.

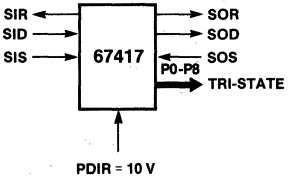
Half-Full Flag

This status output indicates when the 67417 statically contains 32 words or more. This provides an indication to send in more data if the device is operated in a mostly-empty mode or send out more data if the 67417 is operated in a mostly-full mode.

Cascading

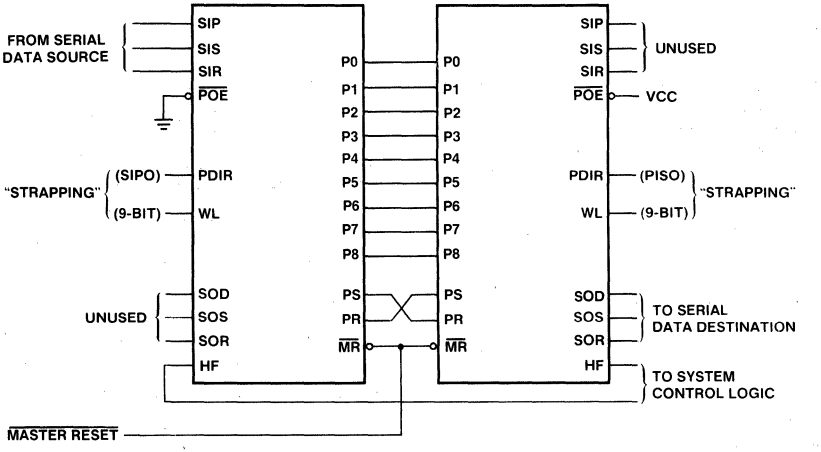
The 67417 is designed to be cascaded at the parallel port only, due to very high data transfer rates at the serial ports. Cascading two 67417's is accomplished by connecting Parallel Input/Output Ready (PR) of each part to control the Parallel Shift In/Out (PS) of the other part, with one FIFO in serial-in to parallel-out mode, and the other FIFO in parallel-in to serial-out mode. The combined effect of this is a reversible 128x8 or 128x9 serial-in serial-out FIFO. The 67417 can not be cascaded at the serial ports because SIR and SOR are not acknowledged signals but rather status signals only.

Applications



NOTE: It can shift in data serially in the multiples of 8- or 9-bit according to WL.

Figure 18. 512/576x1 Serial-in to Serial-out Mode



* SIPO = Serial-in to Parallel-out.
** PISO = Parallel-in to Serial-out.

Figure 19. Cascading of Two 'S417s for Serial-in to Serial-out Operation as a 128x9 (1152x1) FIFO

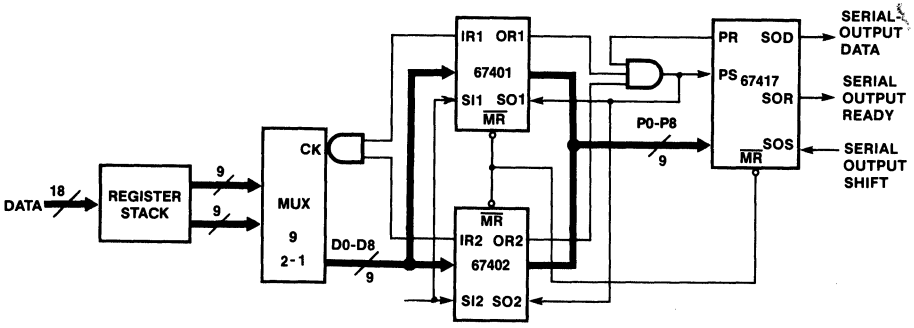


Figure 20. An Example of an Expansion Scheme for a 64x18 Parallel-to-Serial FIFO

An 18-bit data word is multiplexed into the two 67401/2 FIFOs. Since the 67417 FIFO is cascadable at the parallel port only, two 67401/2 FIFOs were used along with the 67417 to obtain the appropriate organization.

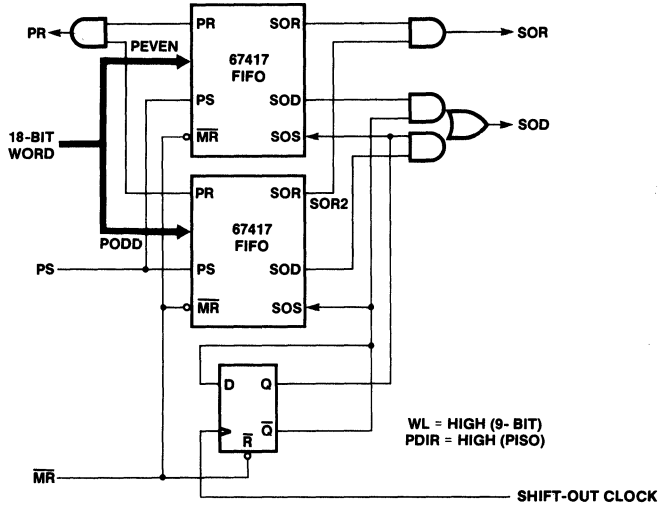


Figure 21. Another Example of an Expansion Scheme for a 64x18 Parallel-in to Serial-out FIFO Two 67417 FIFOs Are Used to Implement a 64x18 Parallel-in to Serial-out FIFO

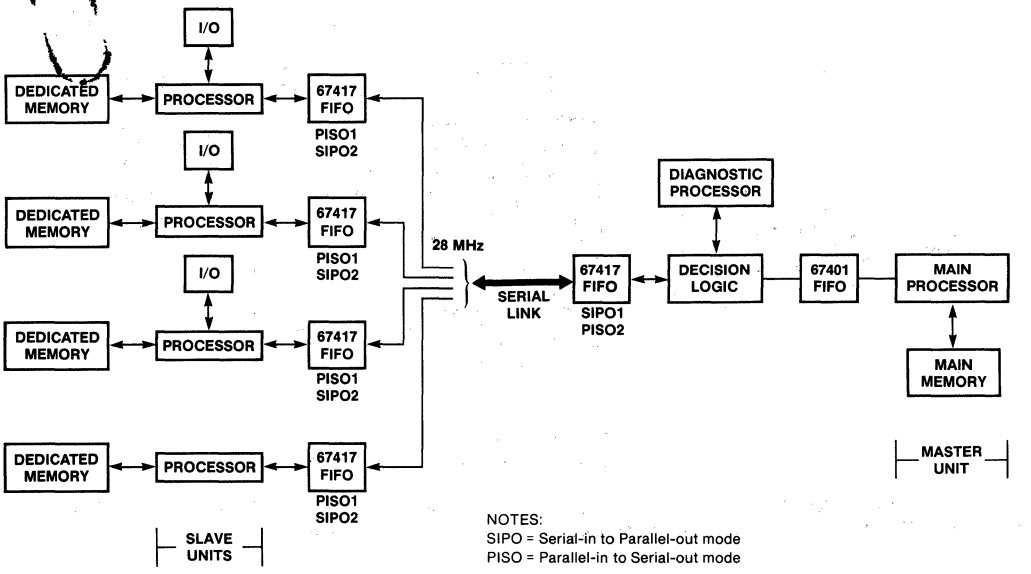


Figure 22. A Multiprocessing System

Each processor unit on the left has its own communication interface which consists of a serializing FIFO. The serial data link can operate in either direction 1 or direction 2 which is decided by the Decision logic. In direction 1 either of the slave units send the data to the master over the serial link, with its respective 67417 operating in parallel-in to serial-out mode (PISO1). While the 67417 for the master unit operates in serial-in to parallel-out mode (SIPO1). The direction 2 has the FIFOs (67417) operating in the reverse direction from the above case. Decision logic determines the priority of the slave processors to use the serial link.

FIFO RAM Controller

674219

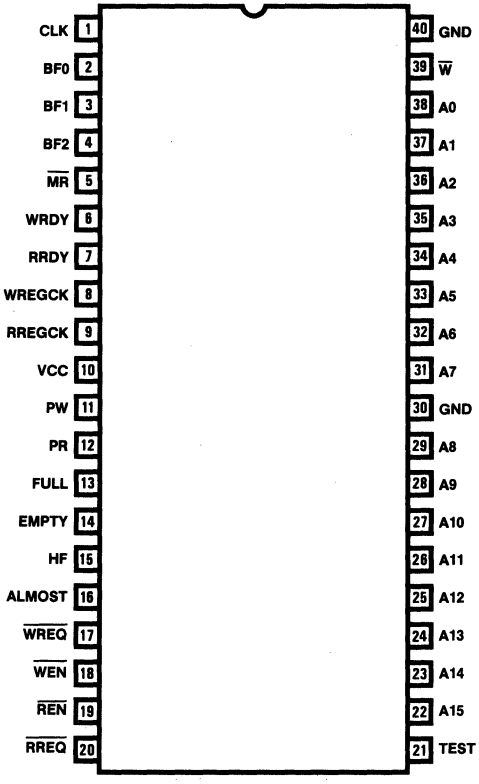
Features/Benefits

- High-speed, no fall-through time
- Deep FIFOs—16-bit SRAM address
- Arbitration read/write
- Control signals for data latching
- Full, Half-Full, Empty, Almost flags for buffer sizes from 512 to 64 K
- Three-state outputs

Applications

- LAN equipment
- Data communication
- Disk/tape controllers
- Host-to-dedicated-processor interface

Pin Configuration



Ordering Information

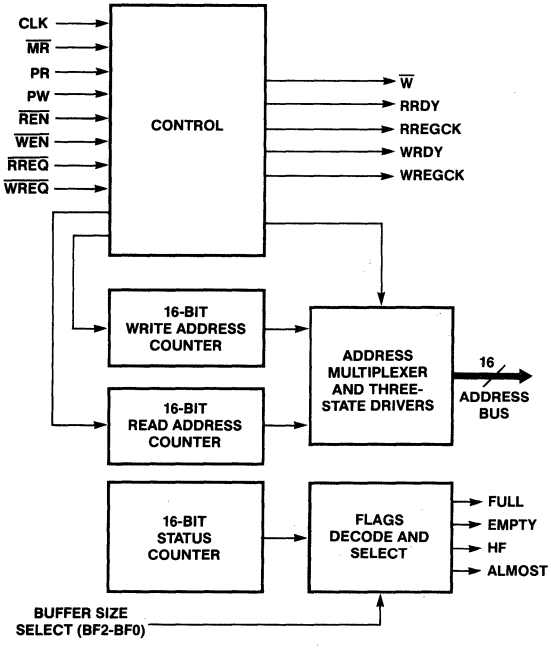
PART NUMBER	PACKAGE		TEMPERATURE
	PINS	TYPE	
674219	40	J	Com

Description

The 674219 FIFO RAM Controller provides addressing control, status, and arbitration for a static RAM array used as a First-In-First-Out (FIFO) buffer. The sixteen address lines can address a FIFO buffer area ranging from 512 to 65,536 static RAM words. Control signals including W (the write enable signal for the static RAMs), handshaking signals for the read and write ports, and strobes for external data latching.

The 674219 allows single-port static RAMs to resolve read and write request conflicts according to priority rules selected via the Priority-on-Read (PR) and Priority-on-Write (PW) inputs. If priority is given to either port, or if only one port is used, the maximum data rate through that port is 10 MHz.

Block Diagram



Publication #	Rev.	Amendment
10685	A	/0

Issue Date: May 1988

Definition of Terms

LATCHED A request has been received by the 674219 on one of its ports. The request has been internally latched, but not sampled.

SAMPLED The state of a latched request when it has been internally synchronized.

PROCESSED A decision to perform a sampled request.

PERFORMED When the processed request is executed as a memory cycle.

PENDING REQUEST A sampled request that has been held until the FIFO completes its current operation(s).

WRITE DATA PORT The register(s) where the system places the data that is to be written into the FIFO.

READ DATA PORT The register(s) where the system reads the FIFO data.

WRITE DATA REGISTER The register(s) which serves as the data input to the FIFO.

READ DATA REGISTER The register(s) where the FIFO leaves the read data for the system to take.

Architecture

The 674219 FIFO RAM Controller, together with an array of static RAMs and two registers, comprises a First-In-First-Out (FIFO) memory. (See Figure 1.)

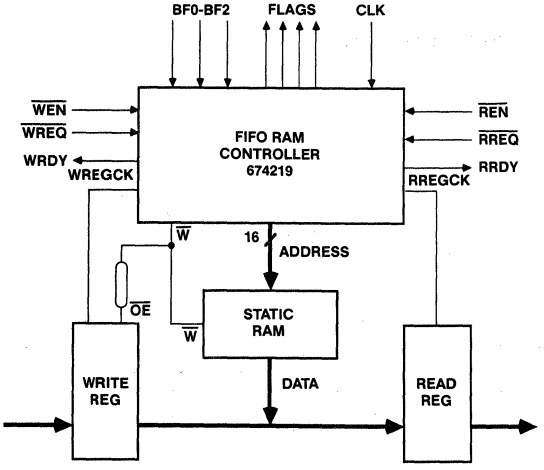


Figure 1. 57/674219 In and Implementation of a FIFO Buffer

The 674219 provides addresses and control signals to the static RAMs, and interfaces with the system via a write port, a read port, and status flags. The 674219 includes three 16-bit counters: a write-address counter, a read-address counter, and a status counter. The status flags are generated as a function of the state of the status counter and the buffer length selected. The write port has a Write REQuest ($\overline{WREQ}$) input, a Write ENable ($\overline{WEN}$) input, and a Write ReaDY (WRDY) output. The read port has a Read REQuest ($\overline{RREQ}$) input, a Read ENable ($\overline{REN}$) input, and a Read ReaDY (RRDY) output. Two priority-control inputs, Priority-on-Write (PW) and Priority-on-Read (PR), determine the priority rules by which the 674219 arbitrates between simultaneous read and write requests. The 674219 provides two clock signals (RREGCK, WREGCK) to the Read Data Register and the Write Data Register, as well as a Write signal ($\overline{W}$) to be connected to the Write Enable ($\overline{WE}$) inputs of the static RAMs. Sixteen address outputs provide the read and write addresses to the static RAMs. When both $\overline{REN}$ and $\overline{WEN}$ are HIGH, the address outputs go into high-impedance (Hi-Z) state, so that the static RAMs can be accessed externally.

A Master Reset ($\overline{MR}$) input allows initializing the part by clearing the three counters and presetting the flags. (See Table 1.)

FLAG	CONDITION
Empty	High
Full	Low
Almost	High
Half	Low

Table 1. Condition of Flags After Master Reset

Pin Definitions

V_{CC} 5.0 V ± 10%

GND Ground

CLK CLOCK—Controls synchronous operation of the device. All requests are sampled internally on every other LOW-to-HIGH transition of the clock. These transitions are called sampling clock edges. The first sampling clock edge is the first LOW-to-HIGH transition of the clock after master reset.

BF2-BF0 BUFFER SIZE CONTROLS—Determine the desired buffer size. (See Table 3.) Setting the buffer size is essential for correct operation of the status flags.

$\overline{MR}$ MASTER RESET—Clears all counters when LOW. The first LOW-to-HIGH transition of the clock, following a LOW-going Master Reset pulse, is the first sampling clock edge; the first request to be serviced is a write request. (See Figure 7.)

A15-A0 ADDRESS OUTPUTS—Three-state outputs which provide a read address when $\overline{W}$ is HIGH, or a write address when $\overline{W}$ is LOW. A15-A0 are in the Hi-Z state only when both $\overline{REN}$ and $\overline{WEN}$ are HIGH.

TEST An input used during manufacturing final test. For normal operation, TEST should be tied to GND.

$\overline{W}$ WRITE CONTROL—Used to control the SRAM arrays Write Enable pin and to output enable the write data register.

$\overline{WREQ}$ WRITE REQUEST—A LOW-going pulse on this pin requests a write to the FIFO. A write request can only be latched if the write port is enabled ($\overline{WEN}$ is LOW), and the previous write request has been processed (WRDY is HIGH).

$\overline{RREQ}$ READ REQUEST—A LOW-going pulse on this pin requests a read from the FIFO. A read request can only be latched if the read port is enabled ($\overline{REN}$ is LOW), and the previous read request has been processed (RRDY is HIGH).

$\overline{WEN}$ WRITE ENABLE—When this input is HIGH, all write requests are ignored. When $\overline{WEN}$ is LOW and WRDY is HIGH, a write request ($\overline{WREQ}$ = LOW-going pulse) will be latched by the 674219. If both $\overline{WEN}$ and $\overline{REN}$ are HIGH, the address outputs A15-A0 go into the Hi-Z state, permitting external access to the SRAM array.

$\overline{REN}$ READ ENABLE—When this input is HIGH, all read requests are ignored. When $\overline{REN}$ is LOW and RRDY is HIGH, a read request ($\overline{RREQ}$ = LOW-going pulse) will be latched by the 674219. If both $\overline{WEN}$ and $\overline{REN}$ are HIGH, the address outputs A15-A0 go into the Hi-Z state, permitting external access to the SRAM array.

PW, PR WRITE PRIORITY and READ PRIORITY—These two inputs determine the rules governing the arbitration between write and read requests. (See Table 2.) *These inputs must not both be HIGH simultaneously.*

WRDY WRITE READY—When this output is HIGH, and $\overline{WEN}$ is LOW, a write request may be sent to the $\overline{WREQ}$ pin.

WRDY goes LOW on the sampling clock edge which samples the write request. WRDY will go HIGH on the non-sampling clock edge which starts the write cycle. WRDY will stay LOW if the FIFO is full.

Write requests should be made only when WRDY is HIGH.

RRDY READ READY—When this output is HIGH, and $\overline{REN}$ is LOW, a read request may be sent to the $\overline{RREQ}$ pin.

RRDY goes LOW on the sampling clock edge which samples the read request. RRDY will go HIGH on the non-sampling clock edge which starts the read cycle. RRDY will stay LOW if the FIFO is empty.

Read requests should be made only when RRDY is HIGH.

WREGCK WRITE REGISTER CLOCK—This output is used to clock the write data register.

RREGCK READ REGISTER CLOCK—This output is used to clock the read data register.

EMPTY EMPTY FLAG—When HIGH, indicates that the FIFO is empty. Read requests are not permitted when the FIFO is EMPTY.

FULL FULL FLAG—When HIGH, indicates that the FIFO is full. Write requests are not permitted when the FIFO is FULL.

HF HALF-FULL FLAG—When HIGH, indicates that the FIFO has half, or more, of its locations occupied.

ALMOST ALMOST FLAG—When HIGH, indicates that one of the following conditions exists:

1. The FIFO is almost empty (less than sixteen words in the FIFO), if ALMOST is HIGH and HF is LOW.
2. The FIFO is almost full (sixteen or less locations are available) if ALMOST is HIGH and HF is HIGH.

Requests, Arbitration and Data Capture

A clock, supplied via the CLK input of the 57/674219, generates the internal sequence of events which constitutes a single FIFO operation. The read and write ports recognize and latch read and write requests asynchronously, provided that the respective enable ($\overline{REN}$ or $\overline{WEN}$) is LOW, and the request window setup time is observed.

The FIFO *write* operation is as follows (see Figure 2):

Stage 1 A write request is sent to the 674219 by a LOW-going pulse on the $\overline{WREQ}$ pin.

Stage 2 The write request is latched internally, asynchronous to the clock.

Stage 3 WRDY goes LOW on the sampling clock edge that latched the request to indicate to the system that the request has been latched and synchronized internally. WRDY also indicates to the system that the write port is no longer accepting write requests. In order to guarantee that a request is properly synchronized, the request must not occur during the window stated by the tWRQC specifications.

Stage 4a Regardless of whether the write cycle is started or not, WREGCK will go HIGH for one clock cycle on the non-sampling clock edge that follows WRDY going LOW. The transition from LOW-to-HIGH on the WREGCK pin clocks data into the write data port, reading the data for writing to the SRAM.

Stage 4b A decision to wait, or to perform the write cycle is made based on the following:

Case 1 If read priority is set, the 674219 will process all pending read requests first. The write cycle will be delayed until all of the read cycles have been performed. Then, and only then, will the pending write cycle be performed.

Case 2 If write priority is set, regardless if there is a pending read request or not, the write cycle will start on the next non-sampling clock edge that follows WRDY going LOW. If there was a pending read request, the read cycle will not be started until the write cycle has been completed.

Case 3 If no priority is set, and there is no pending read request, the FRC will start the write cycle on the next non-sampling clock edge that follows WRDY going LOW.

Case 4 If no priority is set, and there are simultaneous requests (i.e., a read request and a write request have both been latched before the same sampling clock edge), the FIFO will decide which is to be processed first according to the following:

If the last case of simultaneous requests (with no priority) performed a read cycle first, the write request will be processed first, followed by the read request.

If the last case of simultaneous requests (with no priority) performed a write cycle first, the read request will be processed first, followed by the write request.

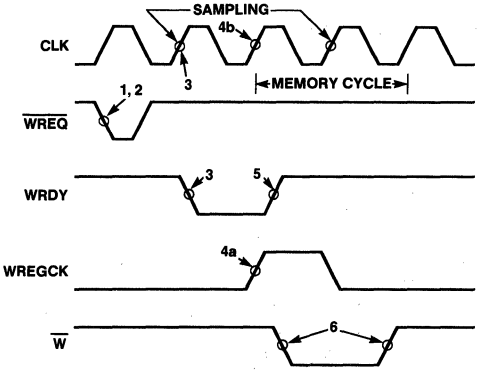


Figure 2. The Stages of a FIFO Write Operation

Stage 5 WRDY will go HIGH on the non-sampling edge that starts the write cycle.

Stage 6 Once a request has been granted, the memory cycle takes place over two clock cycles, starting with the non-sampling clock edge on which the request is granted (WRDY going from LOW-to-HIGH). The Write line ($\overline{W}$) goes LOW at tCWL after the clock edge starting the memory cycle and stays low until tCWH after the clock edge terminating the memory cycle.

The FIFO *read* operation is as follows (see Figure 3):

Stage 1 A read request is sent to the 674219 by a LOW-going pulse on the $\overline{RREQ}$ pin.

Stage 2 The read request is latched internally, asynchronous to the clock.

Stage 3 RRDY goes LOW on the sampling clock edge that latched the request to indicate to the system that the request has been latched and synchronized internally. RRDY also indicates to the system that the read port is no longer accepting read requests. In order to guarantee that a request is properly synchronized, the request must not occur during the window stated by the tRRQC specifications.

Stage 4 A decision to wait, or to perform the read cycle is made based on the following:

Case 1 If write priority is set, the 674219 will process all pending write requests first. The read cycle will be delayed until all of the write cycles have been performed. Then, and only then, will the pending read cycle be performed.

Case 2 If read priority is set, regardless if there is a pending write request or not, the read cycle will start on the next non-sampling clock edge that follows RRDY going LOW. If there was a pending write request, the write cycle will not be started until the read cycle has been completed.

Case 3 If no priority is set, and there is no pending write request, the FRC will start the read cycle on the next non-sampling clock edge that follows RRDY going LOW.

Case 4 If no priority is set, and there are simultaneous requests (i.e., a read request and a write request have both been latched before the same sampling clock edge), the FIFO will decide which is to be processed first according to the following:

1. If the last case of simultaneous requests (with no priority) performed a read cycle first, the write request will be processed first, followed by the read request.
2. If the last case of simultaneous requests (with no priority) performed a write cycle first, the read request will be processed first, followed by the write request.

Stage 5 RRDY will go HIGH on the non-sampling edge that starts the write cycle.

Stage 6 Once a request has been granted, the memory cycle takes place over two clock cycles, starting with the non-sampling clock edge on which the request is granted (RRDY going from LOW-to-HIGH). Read REGister Clock (RREGCK) goes LOW for one clock cycle, starting with the sampling edge that occurred within the read memory cycle. RREGCK clocks data from the SRAM array to the read data port on the LOW-to-HIGH transition, which terminates the read cycle.

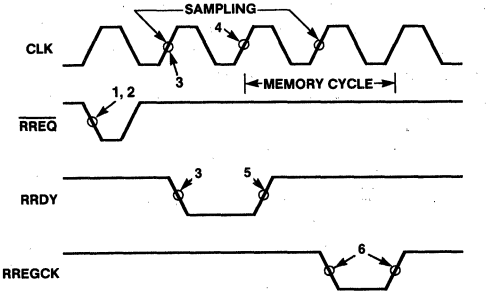


Figure 3. The Stages of a FIFO Read Operation

Priority

Two input signals, Priority-on Read (PR) and Priority -on-Write (PW), determine the arbitration rule which sequences the read and write cycles, for various cases as follows: (see Table 2):

PW	PR	PRIORITY
0	0	No priority
0	1	Priority on READ
1	0	Priority on WRITE
1	1	(Not allowed)

Table 2. Priority Encoding

No-Priority Case

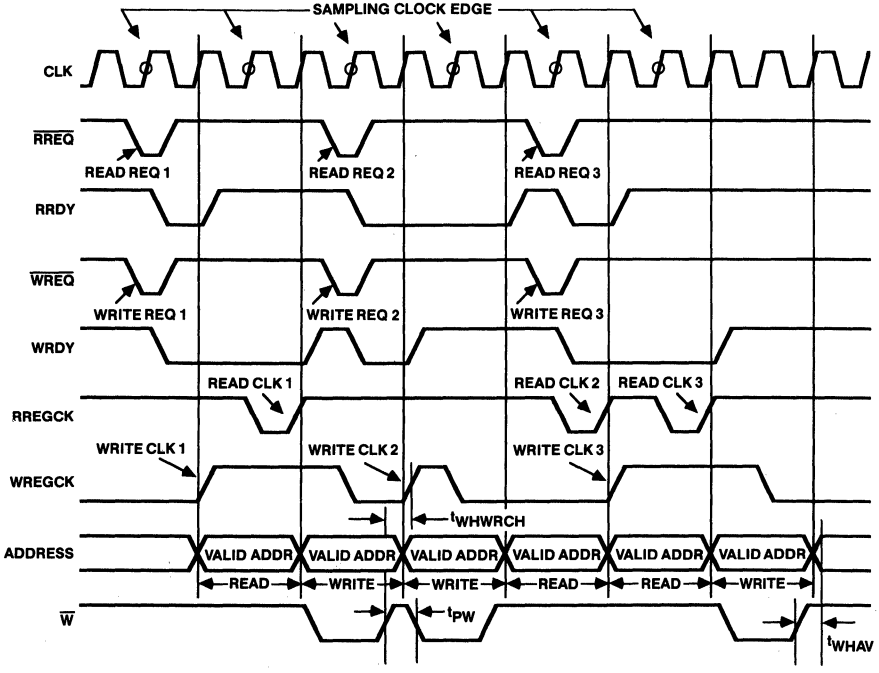
If no priority is selected (PR = PW = LOW), each request is processed in the order it came into the FRC.

If no priority is set and both a read and write request are latched before the same sampling clock edge, the 674219 will perform read and write cycles alternately. (See Figure 4.)

Write Priority Case

If write priority is selected (PR = LOW, PW = HIGH) write requests are always processed before read requests (assuming that the requests meet the setup time).

If write priority is set and both a read and write request are latched before the same sampling clock edge, (i.e., a simultaneous request), the write cycle will take place first. If, before the next sampling clock edge, another write request is latched, another write cycle will take place, and the pending read request will not be processed. Only when the sampling clock edge encounters no further write requests will the pending read request be processed. At this time the read cycle will start and the RRDY output will go HIGH. (See Figure 5.)



Notes: 1. Assumes not at FULL and not at EMPTY.
2. Assumes last case of simultaneous requests processed a write first.

Figure 4. Operation With No Priority

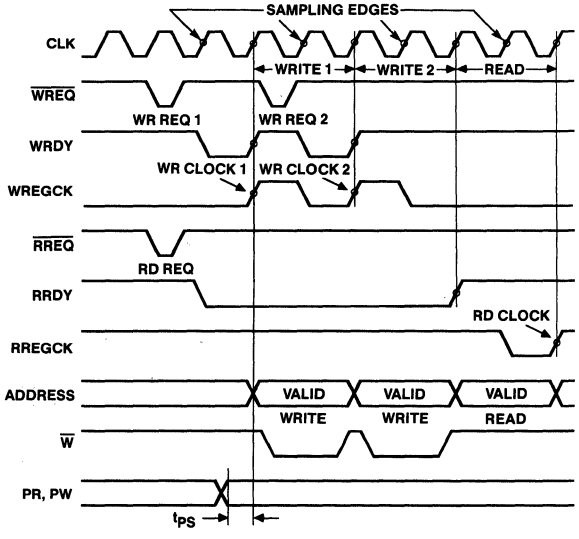


Figure 5. Operation With Write Priority

Read Priority Case

If read priority is selected (PR = HIGH, PW = LOW) read requests are always processed before write requests assuming that the requests meet the setup time).

If read priority is set and both a read and write request are latched before the same sampling clock edge, (i.e., a simultaneous request), the read cycle will take place first. If, before the next sampling clock edge, another read request is latched, another read cycle will take place and the pending write request will not be processed. Only when the sampling clock edge encounters no further read requests will the pending write requests be processed. At this time, the write cycle will start and the WRDY output will go HIGH. (See Figure 6.)

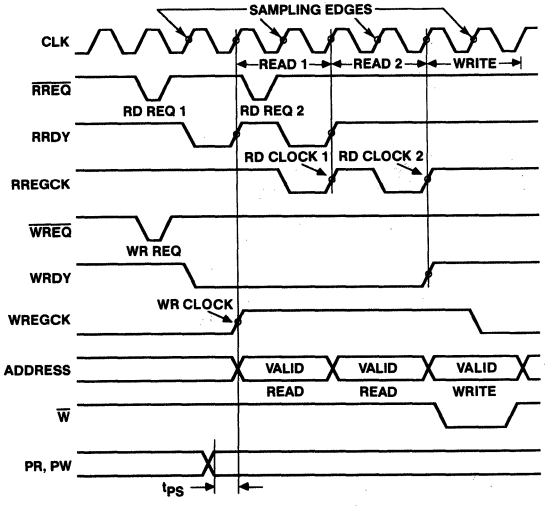


Figure 6. Operation With Read Priority

Buffer Length

A three-bit input control field, BF2-0, selects the buffer length ("depth") of the FIFO. Any power of 2 from 512 to 65,536 may be chosen as the buffer length. (See Table 3.)

BF2	BF1	BF2	BUFFER SIZE
0	0	0	512
0	0	1	1024
0	1	0	2048
0	1	1	4096
1	0	0	8192
1	0	1	16384
1	1	0	32768
1	1	1	65536

Table 3. Buffer Length

Status Flags

The flags are generated as a function of the buffer length, selected via inputs BF2-BF0, and the state of the status counter. The status flags are:

EMPTY When HIGH, the EMPTY flag indicates that the FIFO is empty. The EMPTY flag goes HIGH on the first sampling clock edge during the memory cycle which empties out the FIFO.

FULL When HIGH, the FULL flag indicates that the FIFO is full, and no more data can be written into it until a read cycle takes place. The FULL flag goes HIGH on the first sampling clock edge during the memory write cycle which fills up the FIFO.

HF When HIGH, the Half-Full flag indicates that the FIFO is filled to half its depth, or more.

ALMOST When HIGH, the ALMOST flag indicates that one of the following conditions exists:

1. The FIFO is almost empty (less than sixteen words in the FIFO), if ALMOST is HIGH and HF is LOW.
2. The FIFO is almost full (sixteen or less locations are available) if ALMOST is HIGH and HF is HIGH.

The flags Master Reset to the states shown in Table 1.

First Write Cycle (After a Master Reset or When FIFO is Empty)

The first LOW-to-HIGH clock edge, following Master Reset ($\overline{MR}$) going LOW-to-HIGH, is the first sampling clock edge. The sampling clock edge occurs every other positive-going transition of the clock. The LOW pulse on $\overline{MR}$ clears the three internal 16-bit counters (status, read and write). The FIFO is set to the EMPTY state, and no read requests are allowed (RRDY = LOW).

After an interval of at least tMRS after $\overline{MR}$ goes HIGH, a LOW-going pulse on the $\overline{WREQ}$ pin tells the 674219 that a write to the FIFO is requested. The write request is latched by the write port, provided that $\overline{WEN}$ is LOW. (See Figure 7.) The following sampling clock edge samples the request, and causes WRDY to go LOW. WRDY goes HIGH again on the next (non-sampling) positive clock edge, regardless of priority. The write cycle takes place over two clock periods, starting on the positive non-sampling clock edge following the sampling clock edge which brought WRDY HIGH. The data is clocked into the external Write Data Register on the same non-sampling clock edge, and into the external Read Data Register on the second sampling clock edge, to allow minimal fall-through time. (See again Figure 7.) EMPTY will go LOW to indicate that there is valid data in the FIFO. RRDY goes HIGH indicating that there is data to be read from the FIFO. The same sequence of events occurs for the first write request that is initiated when the FIFO is empty.

Methodology for Reading

In order to maintain a consistent system level architecture, the 674219 has been constructed such that the system should read the data port *before* a read request is sent. (See Figure 8.)

This ability allows the FIFO a zero fall-through time on all cycles. The system is able to get the data from the FIFO right away, without having to wait for the FRC to perform a read cycle of the SRAMs.

On the read port, a positive-going edge of RREGCK signals to the system that the read data register is being updated. The system should read the data first and then send a request to obtain the next word from memory to the read data register.

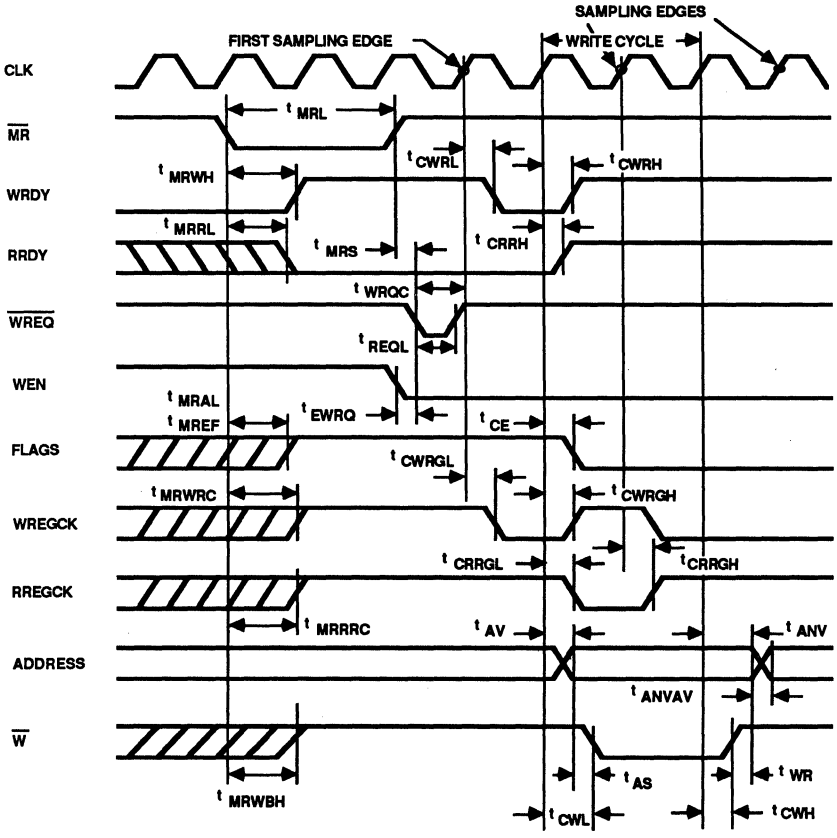


Figure 7. First Write After Master Reset or When FIFO Is Empty

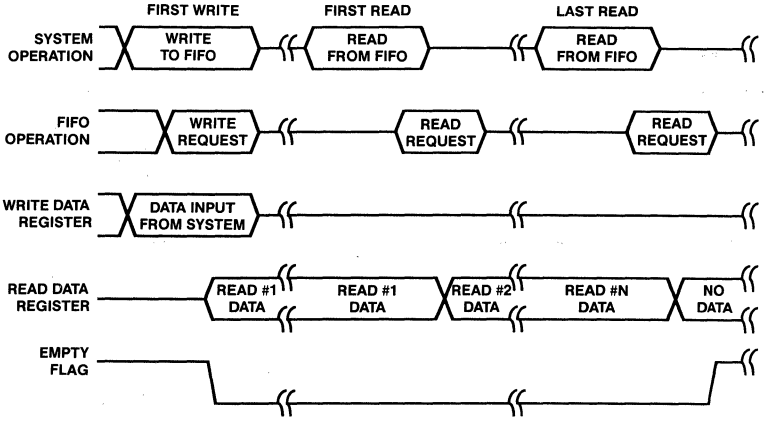


Figure 8. Methodology for Reading From the FIFO

Write Cycle (Figure 9)

A write request, indicated by a LOW-going pulse on the $\overline{WREQ}$ pin, is latched by the 674219, provided that $\overline{WEN}$ is LOW and WRDY is HIGH. The request is sampled internally on the sampling clock edge. WRDY goes LOW on the same sampling clock edge, to indicate to the system that a write request has been latched and synchronized internally. In addition, WREGCK will go HIGH for one clock cycle on the non-sampling clock edge that follows WRDY going LOW, regardless of whether the write request is processed. The write request will be processed only if one of the following sets of conditions is true:

1. Write Priority has been selected.

   If write priority has been selected, the FRC will process all write requests before any pending read requests.

2. No read request has been latched.

   If no read request has been latched, regardless of priority, the FRC will process the write request immediately and will start the write memory cycle on the non-sampling clock edge that follows WRDY going LOW.

3. No priority has been selected, both a read and a write request occur before the same sampling clock edge (simultaneous request), and in the last case of a simultaneous request, the FRC processed the read request first.

   In this case, the 674219 will process the write request first, and then process the read request.

4. No priority has been selected, both a read and a write request occur before the same sampling clock edge (simultaneous request), and in the last case of a simultaneous request, the FRC processed the write request first.

   In this case the 674219 will process the read request first, and then process the write request.

Once the write request has been processed, a write cycle takes place over two clock cycles starting with the non-sampling clock edge on which WRDY goes HIGH. $\overline{W}$ will go LOW, tCWL after the start of the write cycle. $\overline{W}$ is used to Write Enable the SRAM array and to Output Enable the write data register. Two clocks later (tCWH) $\overline{W}$ will go HIGH again, terminating the write cycle.

In order to avoid the bus contention inherent in shared-I/O memory systems, a delay line and an OR gate may be required (see Memory Interface Design Guidelines).

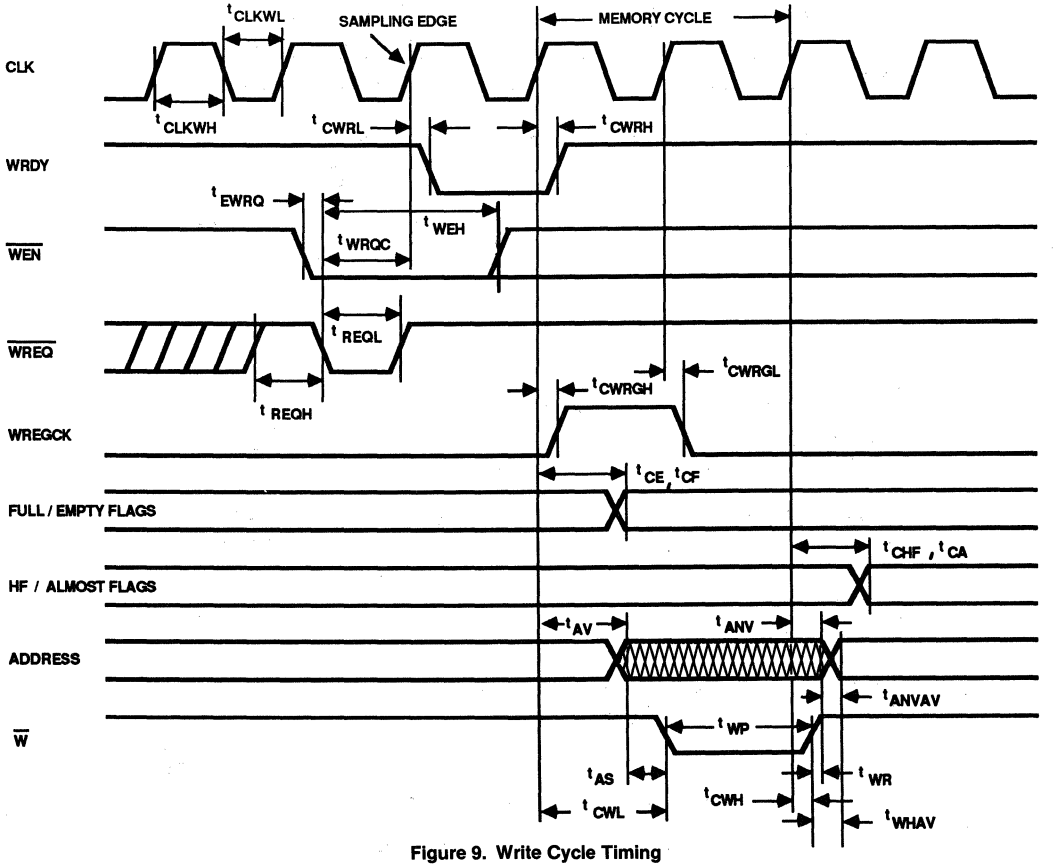


Figure 9. Write Cycle Timing

Read Cycle (Figure 10)

A read request, indicated by a LOW-going pulse on the $\overline{RREQ}$ pin, is latched by the 674219, provided that $\overline{REN}$ is LOW and RRDY is HIGH. The request is sampled internally on the sampling clock edge. RRDY goes LOW on the same sampling clock edge to indicate to the system that a read request has been latched and synchronized internally. The read request is processed only if one of the following sets of conditions is true:

1. Read Priority has been selected.

   If read priority has been selected, the FRC will process all read requests before any pending write request.

2. No write request has been latched.

   If no write request has been latched, regardless of priority, the FRC will process the read request immediately and will start the read memory cycle on the non-sampling clock edge that follows RRDY going LOW.

3. No priority has been selected, both a read and a write request occur before the same sampling clock edge (simultaneous request), and in the last case of a simultaneous request, the FRC processed the write request first.

   In this case, the 674219 will process the read request first.

4. No priority has been selected, both a read and a write request occur before the same sampling clock edge (simultaneous request), and in the last case of a simultaneous request, the FRC processed the read request first.

   In this case, the 674219 will process the write request first, and then process the read request.

Once the read request has been processed, a read cycle takes place over two clock cycles starting with the non-sampling clock edge on which the RRDY goes HIGH. RREGCK goes LOW on the next sampling clock edge, stays LOW for one clock cycle, and goes HIGH on the following non-sampling clock edge, thus clocking the data which appears at the SRAM array's data outputs into the Read Data Register. RREGCK going HIGH terminates the read cycle.

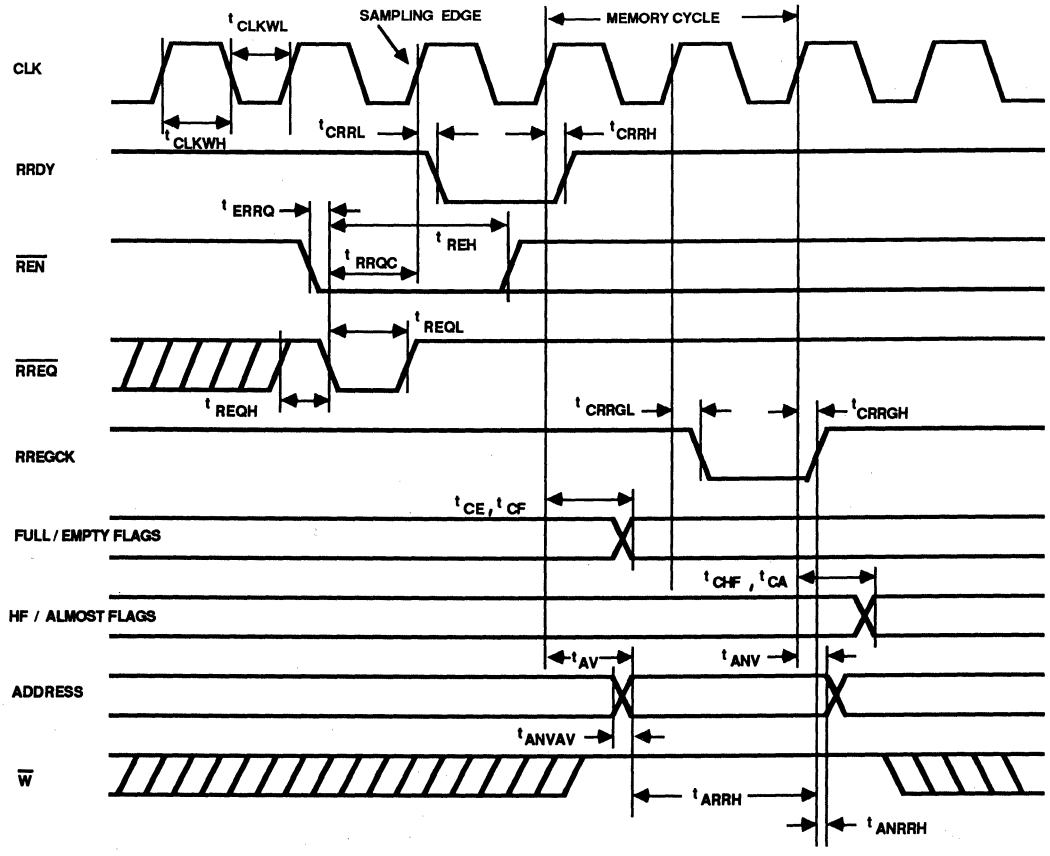


Figure 10. Read Cycle Timing

Memory Interface Design Guidelines

Introduction

The purpose of the memory interface design guideline is to aid the engineer in interfacing the 674219 FIFO RAM Controller (FRC) to an array of static RAMs. This guideline will be broken down into three separate sections. The first section is a timing analysis of the read cycle. The second section is a timing analysis of the write cycle. The final section will guide the designer through a real design.

Figure 11 shows a typical SRAM interface schematic.

Section One: Read Cycle Timing Analysis

Figure 12 shows the basic timings which are critical to the read cycle. Some of these parameters apply to the FRC, some to the SRAM array, and others to external logic. For convenience, these parameters are broken up below:

FRC Parameters:

t_{AV}	Clock to Address Valid Time
t_{ANV}	Clock to Address Not Valid Time

SRAM Parameters

t_{RC}	Read Cycle Time
t_{ACS}	Chip Select Access Time
t_{AA}	Address Access Time
t_{OH}	Output Data Hold Time from Address Change
t_{HZ}	Chip Deselect to Output in High-Z

External Logic:

Chip Select Decoder Parameters:

t_{DECODE}	t_{PD} through Decoder

Read Data Register Parameters:

t_S	Data Setup Time
t_H	Data Hold Time

Other Parameters (See Text):

t_{RDREGH}	Clock to RDCLK High [RDCLK is the clock input of the Read Data Register]

(This parameter is normally t_{CRRGH} of the FRC)

There are six separate equations which must each be met in order to determine what speed of SRAM the designer will need. It is assumed that the user has already specified a speed of operation and the external components needed. The equations listed can be used at any frequency, up to a maximum of a 20-MHz clock rate.

Since every read cycle consists of two physical clock cycles, all equations are with respect to 2T (2 x Cycle Time).

The first equation which should be satisfied is the read cycle time (tRC). This identifies what speed SRAM is required. The equation is based on the total time that the address is valid minus the decoder time. Since the decoder has some minimum skew on the negating edge, this time is ADDED to the equation. The equation thus becomes:

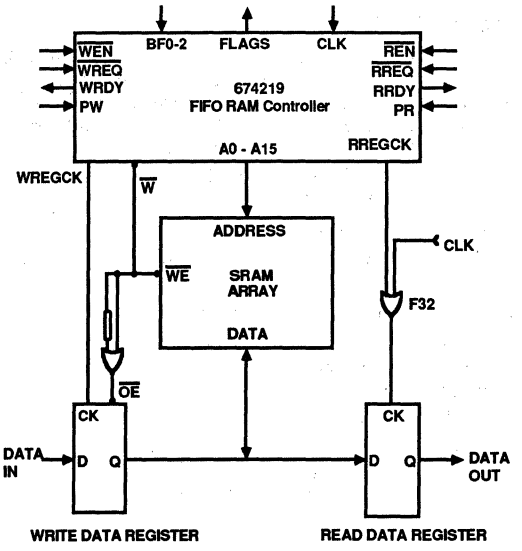


Figure 11. A Typical SRAM Interface

Equation 1-1

$$t_{RC} \leq 2T - t_{DECODE(max)} + t_{DECODE(min)} - t_{ANVAV(max)}$$

The access time must be looked at next. There are actually two separate equations that help determine the access time.

Equation 1-2 determines the address access time (tAA). tAA is based on the time that the address is valid before the read register gets clocked. The equation takes into account the setup time of the read data register (tS) as well. The equation is:

Equation 1-2

$$t_{AA} \leq 2T - MAX(t_{AV} - t_{RDREGH}) - t_{S(min)}$$

Where $MAX(t_{AV} - t_{RDREGH})$ is the maximum difference between t_{AV} and t_{RDREGH}

Equation 1-3 determines the chip select access time (tACS). This time is based on the time the address is valid before the read register gets clocked MINUS the maximum skew through the chip select decoder. This is done to ensure that the decoder delay is taken into consideration. Again, the read register setup time is considered. The modified equation thus becomes:

Equation 1-3

$$t_{ACS} \leq 2T - t_{DECODE(max)} - MAX(t_{AV} - t_{RDREGH}) - t_{S(min)}$$

Where $MAX(t_{AV} - t_{RDREGH})$ is the maximum difference between t_{AV} and t_{RDREGH}

The next two equations take into consideration the read data hold time with respect to the address (tOH), and the chip deselect to data outputs in High-Z time (tHZ). We will consider the more critical tOH. tOH can easily be determined by comparing the data hold time PLUS the clock to address not valid (tANV) time with the sum of the clock to RDCLK HIGH time (tRDREGH) and the data register hold time (tH). The equation for this becomes:

Equation 1-4

$t_{OH(min)} + t_{ANV(min)} \geq t_{RDREGH(max)} + t_{H(min)}$

If the SRAM has an extraordinarily long read data hold time (tOH), the above equation must be modified to include the now more critical chip deselect to data outputs in High-Z time (tHZ). This is done by simply substituting tHZ for tOH. The modified equation is:

Equation 1-5

$t_{HZ(min)} + t_{ANV(min)} \geq t_{RDREGH(max)} + t_{H(min)}$

In addition to the above equations, one more is necessary in certain cases. In Figure 12, the read cycle is shown. At the very end of a read cycle, the read data register is clocked. The normal clocking signal for the FRC is RREGCK. Since the read data register's clock is normally connected to RREGCK, if RREGCK goes HIGH after the data from the SRAMs goes away, the data will be lost. This is only true if the SRAMs have a low tOH(min). Normally, in all of the above equations, the clock to RREGCK HIGH (tCRRGH) is substituted in place of tRDREGH. In the cases where a low tOH does not guarantee the data will be properly clocked, the user has another alternative.

By adding an external OR gate between the clock and RREGCK, the user can effectively shorten tCRRGH(max). The gate "ANDs" the active LOW RREGCK with the clock when it is LOW. This produces an active LOW output signal called RDCLK (see Figure 12). This will bring the edge of read register clock into specification for any tOH, even one of zero. Figure 11 shows a typical example of a SRAM interface, including this gate, should it be necessary.

Because the OR gate inherently has some delay, an equation is necessary to calculate the new tCRRGH. (This "new" parameter is called tRDREGH). It should be noted that if the designer finds it necessary to implement this logic, due to a low tOH, he/she must replace the tRDREGH in Equation 1-1 through 1-5 with the result from the following equation, rather than the normal tCRRGH. The equation for the gate is:

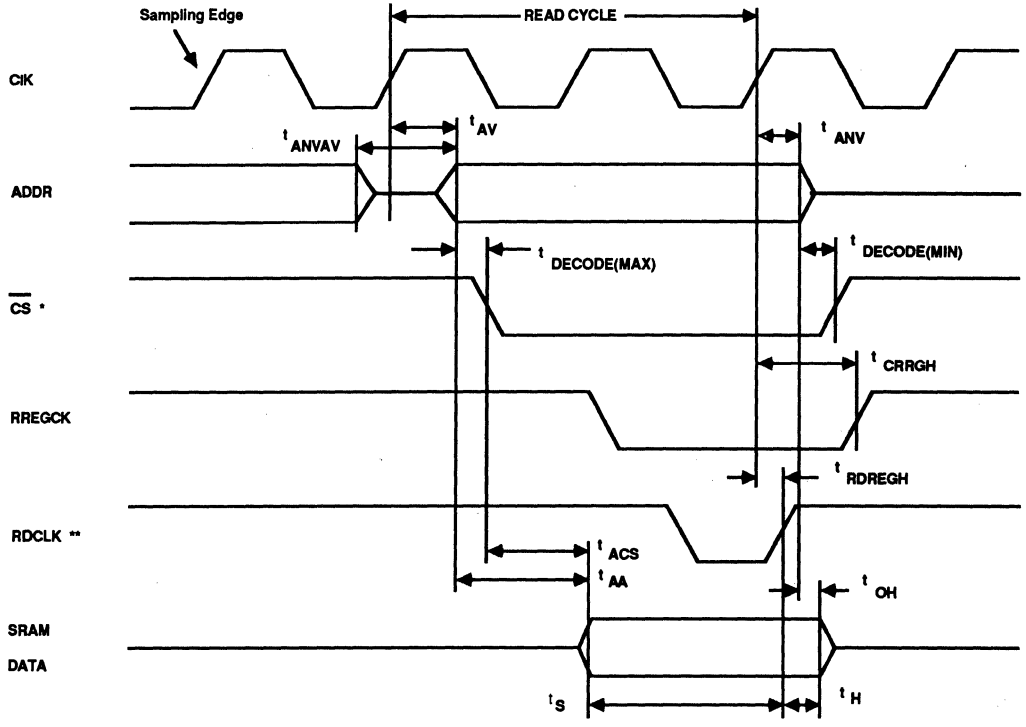
Equation 1-6

$t_{RDREGH\ (max)} = t_{PDOR\ (max)}$

Where $t_{PDOR(max)}$ is the maximum t_{PD} through the OR gate.

Since the clock will bring RDCLK low some tPDOR(max) later, the setup time of the read data register is automatically achieved.

The above equations complete the timing analysis for a read cycle. Once the user has gone through both the read and write cycle timings, an appropriate Static RAM may be chosen.



* CS to the Static RAM bank
** Actual clock input to the Read Data Register. This may be the same as RREGCK or may be the output of the OR-gate shown in Figure 1

Figure 12. Read Cycle Timing

Section Two: Write Cycle Timing Analysis

Figure 13 shows the basic timings which are critical to the write cycle. Some of these parameters apply to the FRC, some to the Static RAM array, and others to external logic. The parameters that are unique to the write cycle will be summarized below:

FRC Parameters:

t_{PW}	Write Pulse Width HIGH
t_{WHAV}	$\overline{W}$ HIGH to Address Valid
t_{ANVAV}	Address Not Valid to Address Valid
t_{WHWRCH}	$\overline{W}$ HIGH to WREGCK HIGH

SRAM Parameters

t_{WC}	Write Cycle Time
t_{AW}	Address Valid to End of Write
t_{CW}	$\overline{CS}$ to End of Write
t_{WP}	$\overline{WE}$ Pulse Width LOW
t_{DW}	Data Valid to End of Write
t_{WZ}	$\overline{WE}$ LOW to Outputs in High-Z

External Logic:

Write Data Register Parameters:

t_{PZ}	$\overline{OE}$ to Outputs in Low-Z
t_{CP}	Clock to Outputs Valid

Other Parameters (See Text):

t_{WOE} $t_{DLY(max)} + t_{ORSKEW(max)}$

There are six equations which must determine the write cycle specifications for the Static RAM. It is assumed that the user has already selected the frequency of operation and the external components needed for his/her system.

Since every write cycle consists of two physical clock cycles, all equations are with respect to 2T (2 x Cycle Time).

The first equation which should be looked at is the write cycle time (tWC). This equation will determine what speed of SRAM is required for proper operation. This parameter is the same as the total time that the address is valid. This is calculated with the following equation:

Equation 2-1

$t_{WC} \leq 2T - t_{ANVAV(max)}$

There are three basic areas to be looked at once the write cycle time has been determined. The first is the access time of the SRAM. There are two separate equations in this area.

The first parameter to be analyzed is the time from address valid to the end of write (tAW). This parameter can be calculated by taking the total write cycle time (2T) and subtracting from it, the time from $\overline{W}$ going HIGH to the next address becoming valid. The equation is:

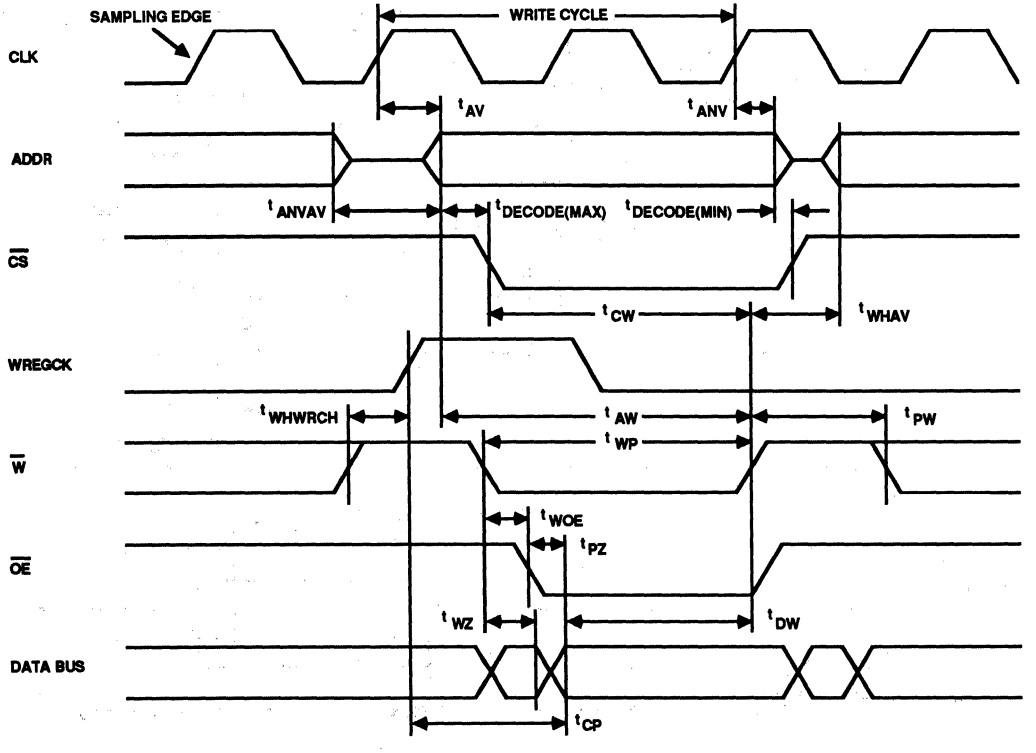


Figure 13. Write Cycle Timing

Equation 2-2

$t_{AW} \leq 2T - t_{WHAV(max)}$

The designer must also check the chip select to end of write time (tCW). This is often more critical than tAW in determining which SRAM to use in the system. The tCW parameter can be obtained in the same way as tAW except that the decode time is also included in the equation. The modified equation is:

Equation 2-3

$t_{CW} \leq 2T - t_{WHAV(max)} - t_{DECODE(max)}$

In addition to the various access times of the write cycle, the user must next look at the pulse width of the write signal (tWP). This is basically the difference between 2T and the FRC's write time HIGH (tPW). The equation is:

Equation 2-4

$t_{WP} \leq 2T - t_{PW(max)}$

The last area that needs to be analyzed is the data setup time of the SRAM. The data setup time is specified as the time data is valid before write goes HIGH (tDW).

There are three separate equations which determine the required tDW of the SRAM.

The write register has a certain propagation delay from its clock input pulse before the data becomes valid. Data must be valid at least tDW before $\overline{WE}$ goes HIGH or it will be lost. The equation takes into account the clock to output time (tCP) of the write register. The equation is:

Equation 2-5

$t_{DW} \leq 2T - t_{CP(max)} - t_{WHWRCH(max)}$

The write data register is enabled by the $\overline{W}$ signal of the FRC. The register takes some minimum time before it enables its outputs from the High-Z state (tPZ).

The SRAMs have some maximum time in which they disable their outputs when the $\overline{WE}$ signal goes LOW. This parameter is the time from $\overline{WE}$ LOW to the data outputs in High-Z (tWZ).

If tWZ(max) is greater than tPZ(min), bus contention will result. To counter this problem a delay must be introduced between the W signal of the FRC and the $\overline{OE}$ input of the write data register. In addition, an OR gate is used to bring $\overline{OE}$ HIGH shortly after $\overline{W}$ goes HIGH. This is illustrated in Figure 11. tWOE(max) is the total delay between $\overline{W}$ going LOW and $\overline{OE}$ going LOW. It is calculated by the following equation:

Equation 2-6

$t_{WOE(max)} = t_{DLY(max)} + t_{PDOR(max)}$

Where $t_{DLY(max)}$ is the maximum delay through the delay line.

$t_{PDOR(max)}$ is the maximum propagation delay through the OR gate.

Equation 2-5 dictated the tDW based on the clock to output time of the register. In most cases though, this time is automatically guaranteed. Since the data will not be valid (Low-Z) until some tPZ after $\overline{OE}$ goes LOW, even though it has been clocked properly, a new equation is necessary to determine the tDW of the SRAM. This equation must take into account the delay that was added in to prevent bus contention. It must also take into account the tPZ time of the register. The equation is very similar to Equation 2-5 with those exceptions. The equation thus becomes:

Equation 2-7

$t_{DW} \leq 2T - t_{PW(max)} - t_{PZ(max)} - t_{WOE(max)}$

One additional equation is required to determine the delay line required to prevent bus contention. The equation for the delay line takes into account the maximum tPD through the OR gate. The equation is based on the tWZ of the SRAM and the tPZ of the write data register. The equation is:

Equation 2-8

$t_{DLY(min)} = t_{WZ(max)} - t_{PZ(min)} - t_{OR(min)}$

The above equations complete the timing analysis of the write cycle. Once the user has gone through both the read and write cycle timings, an appropriate Static RAM may be chosen.

An Example Interface

In order to determine any Static RAM parameters, the user must know several things. He/she must identify the frequency of operation, the read and write data registers, the chip select decoder, and any other logic which may be necessary.

As an example, assume that a 5-MHz data throughput is desired. This will allow a 10-MHz all read or all write data rate. This data rate dictates a 20-MHz clock speed for the FRC.

For worst case design, assume that the selected SRAM has a tOH of zero. Since tOH = 0 ns, there must be an external OR-gate to clock the read register. In addition, assume that the selected SRAM has a $t_{WZ(max)} \leq 20$ ns.

In order to resolve any bus contention a delay line and another OR gate will be added.

74F series parts are used to keep the design clean. It should be noted that the user can use any kind of logic. Because of the particular worst case SRAM parameters that were chosen, this design contains the maximum number of parts that are required for any design.

Given the above considerations, this 20-MHz design requires the following parts:

Parts List:

QTY	PART	DESCRIPTION
1	674219	FIFO RAM Controller
1	74F138	Address Decoder
2	74F374	8-bit Register
1	74F32	OR-Gate
1	20 ns ±10%	Delay Line

The following is a step-by-step analysis of the read and write equations to determine the required SRAM parameters. The equations will also show the delay line needed to avoid bus contention.

Read Equations:

Equation 1-1

$t_{RC} \leq 2T - t_{DECODE(max)} + t_{DECODE(min)} - t_{ANVAV(max)}$

100 -	9.0	+	3.0	-	12
[FRC]	[F138]		[F138]		[FRC]

$t_{RC} \leq 82.0$ ns

Equation 1-6

$t_{RDREGH(max)} = t_{ANV(min)} - t_{ORSKEW(max)}$

	15	-	6.6
	[FRC]		[F32]

$t_{RDREGH(max)} = 6.6$ ns

Equation 1-2

$t_{AA} \leq 2T - MAX(t_{AV} - t_{RDREGH}) - t_{S(min)}$

100 -	(40	-	8.4)	-	2.0
[FRC]	[FRC]		[F32]		[F374]

$t_{AA} \leq 66.4$ ns

Equation 1-3

$t_{ACS} \leq 2T - t_{DECODE(max)} - MAX(t_{AV} - t_{RDREGH}) - t_{S(min)}$

100 -	9.0	-	(40	-	8.4)	-	2.0
[FRC]	[F138]		[FRC]		[F32]		[F374]

$t_{ACS} \leq 57.4$ ns

Equation 1-4

$t_{OH(min)} + t_{ANV(min)} \geq t_{RDREGH(max)} + t_{H(min)}$

0	+	15	≥	8.4	+	2.0
[SRAM]		[FRC]		[F32]		[F374]

15 ns ≥ 10.4 ns

Equation 1-5

$t_{HZ(min)} + t_{ANV(min)} \geq t_{RDREGH(max)} + t_{H(min)}$

0	+	15	≥	8.4	+	2.0
[SRAM]		[FRC]		[F32]		[F374]

15 ns ≥ 10.4 ns

Write Equations:

Equation 2-1

$t_{WC} \leq 2T - t_{ANVAV(max)}$

100 -	12
[FRC]	[FRC]

$t_{WC} \leq 88.0$ ns

Equation 2-2

$t_{AW} \leq 2T - t_{WHAV(max)}$

100 -	25
[FRC]	[FRC]

$t_{AW} \leq 75.0$ ns

Equation 2-3

$t_{CW} \leq 2T - t_{WHAV(max)} - t_{DECODE(max)}$

100 -	25	-	9.0
[FRC]	[FRC]		[F138]

$t_{CW} \leq 66.0$ ns

Equation 2-4

$t_{WP} \leq 2T - t_{PW(max)}$

100 -	25
[FRC]	[FRC]

$t_{WP} \leq 75.0$ ns

Equation 2-5

$t_{DW} \leq 2T - t_{CP(max)} - t_{WHWRCH(max)}$

100 -	12.5	-	18
[FRC]	[F374]		[FRC]

$t_{DW} \leq 69.5$ ns

Equation 2-8

$t_{DLY(min)} = t_{WZ(max)} - t_{PZ(min)} - t_{OR(min)}$

	20	-	2.0	-	3.0
	[SRAM]		[F374]		[F32]

$t_{DLY(min)} = 15$ ns (USE 20 ns ' 10%

Equation 2-6

$t_{WOE(max)} = t_{DLY(max)} + t_{OR(max)}$

	22	+	6.6
	[DELAY]		[F32]

$t_{WOE(max)} = 28.6$ ns

Equation 2-7

$t_{DW} \leq 2T - t_{PW(max)} - t_{PZ(max)} - t_{WOE(max)}$

100 -	25	-	12.5	-	28.6
[FRC]	[FRC]		[F374]		[delay]

$t_{DW} \leq 33.9$ ns

RESULTS

READ PARAMETERS:

Minimum t_{RC} = 82.0 ns
Minimum t_{AA} = 66.4 ns
Minimum t_{ACS} = 57.4 ns
Minimum t_{OH} = 0 ns (Assumed)
Minimum t_{HZ} = 0 ns (Assumed)

WRITE PARAMETERS:

Minimum t_{WC} = 88.0 ns
Minimum t_{AW} = 75.0 ns
Minimum t_{CW} = 66.0 ns
Minimum t_{WP} = 75.0 ns
Minimum t_{DW} = 33.9 ns (Equation 2-7 used for $t_{DW(min)}$)
Minimum t_{WR} = 0 ns (Because FRC's t_{WR} = 0 ns)

DELAY LINE:

20 ns Delay Line ('10%)

Based on those results, the Hitachi HM6168H-45 was selected. This is a 4096 x 4-bit Static RAM with a 45-ns access time. Its specifications are:

READ PARAMETERS:

Minimum t_{RC} = 45.0 ns
Minimum t_{AA} = 45.0 ns
Minimum t_{ACS} = 45.0 ns
Minimum t_{OH} = 5.0 ns
Minimum t_{HZ} = 0 ns

WRITE PARAMETERS:

Minimum t_{WC} = 45.0 ns
Minimum t_{AW} = 40.0 ns
Minimum t_{CW} = 40.0 ns
Minimum t_{WP} = 35.0 ns
Minimum t_{DW} = 20.0 ns
Minimum t_{WR} = 0 ns

Sixteen 4K x 4-bit SRAMs are required to complete a 32K x 8-bit FIFO buffer. The complete design is shown in Figure 14. This illustrates the two OR-gates, the delay line, the decoder, the two registers, the Static RAM array and the 674219 FIFO RAM Controller in a 20-MHz design.

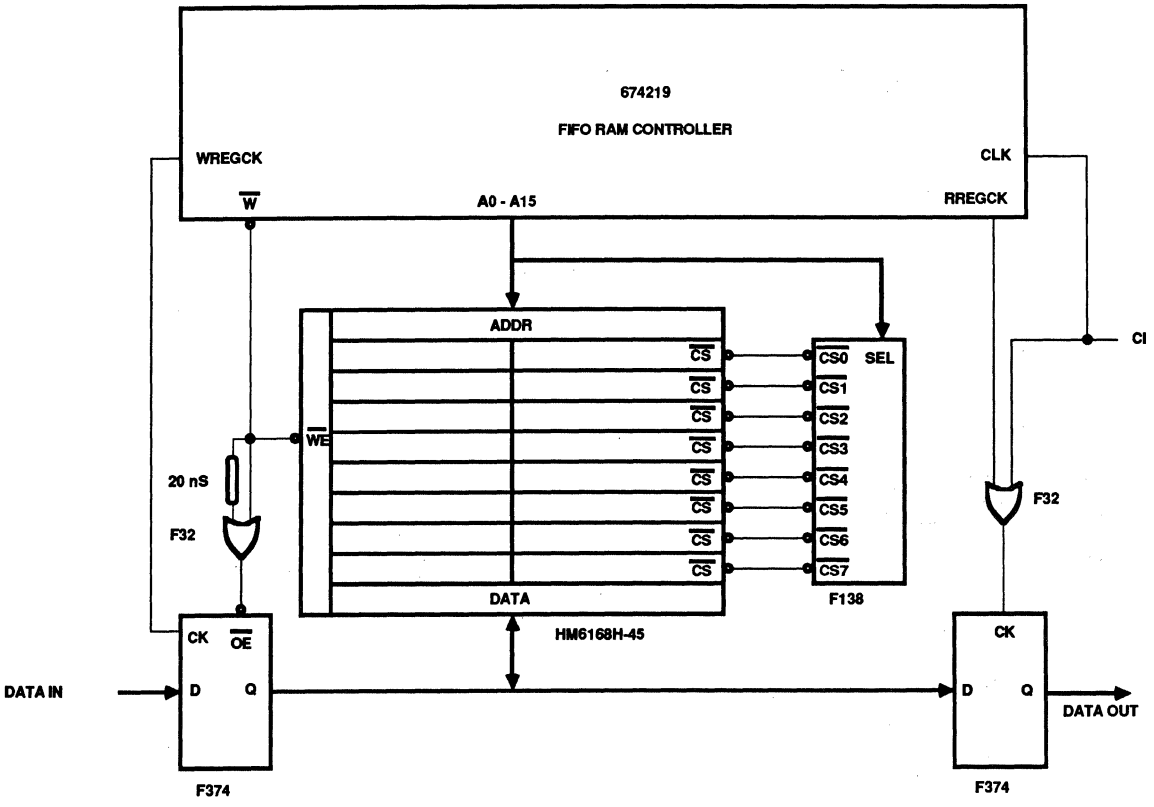


Figure 14. Worst Case Design for 20 MHz

Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7.0 V
DC input voltage V_I ..... -0.5 V to 5.5 V
DC output voltage, V_O ..... -0.5 V to 5.5 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage termperature ..... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIG.	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	N/A	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	N/A	-55		125	0		75	°C
t_{CLKWH}	Clock width HIGH	9,10	45			31			ns
t_{CLKWL}	Clock width LOW	9,10	34			18			ns
f_{CLK}	Clock frequency	N/A			12.5			20	MHz
t_{REQL}	Request LOW time	7,9,10	12			12			ns
t_{REQH}	Request HIGH time	9,10	25			25			ns
t_{MRL}	Master Reset width LOW	7	60			50			ns
t_{MRS}	Master Reset HIGH to WREQ LOW	7	25			25			ns
t_{PS}	Priority to non-sampling clock setup time	5,6	30			25			ns
t_{EWRQ}	WEN to WREQ setup time	7,9	0			0			ns
t_{ERRQ}	REN to RREQ setup time	10	0			0			ns
t_{WEH}	WREQ to WEN hold time	9	15			15			ns
t_{REH}	RREQ to REN hold time	10	15			15			ns
t_{WRQC}	WREQ LOW to sampling clock setup time	7,9	5*		30*	10*		25*	ns
t_{RRQC}	RREQ low to sampling clock setup time	10	5*		30*	10*		25*	ns

* The request window must be observed to guarantee proper operation, between min and max values are not allowed.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITION		COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IL}	Low-Level input voltage					0.8	V
V_A	High-level input voltage			2			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18 mA			-1.5	V
I_{IL}*	Low-level input current	V_{CC} = MIN	V_I = 0.45 V			-250	μA
I_{IH}*	High-level input current	V_{CC} = MIN	V_I = 2.4 V			50	μA
I_I	Maximum input current	V_{CC} = MIN	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{CC} = MIN V_{CC} = MIN	I_{OL} (Address) = 16 mA I_{OL} (Control) = 8 mA I_{OL} (Flag) = 8 mA			0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN V_{CC} = MIN V_{CC} = MIN	I_{OH} (Address) = -3 mA I_{OH} (Control) = -3 mA I_{OH} (Flag) = -3 mA	2.4			V
I_{OS}**	Output short-circuit current	V_{CC} = MAX	V_{OH} = 0 V	-20		-90	mA
I_{OZH} I_{OZL}	Off-state output currents	V_{CC} = MAX V_{CC} = MAX	V_O = 2.4 V V_O = 0.4 V			+40 -350†	μA
I_{CC}	Supply current	V_{CC} = MAX				350	mA

*Except TEST pin, which should always be grounded.

**No more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

†I_{OZL} is Output leakage current plus I_{IL}.

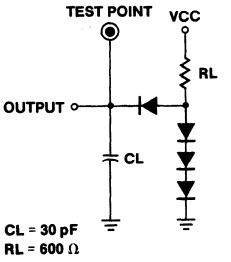
Switching Characteristics

SYMBOL	PARAMETER	FIG.	MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
t_{MRWH}	Master Reset LOW to WRDY HIGH	7			50			50	ns
t_{MRRL}	Master Reset LOW to RRDY LOW	7			50			50	ns
t_{MREF}	Master Reset LOW to EMPTY flag HIGH	7			50			50	ns
t_{MRAL}	Master Reset LOW to Almost HIGH	7			60			55	ns
t_{MRWRC}	Master Reset LOW to WREGCK HIGH	7			40			35	ns
t_{MRRRC}	Master Reset LOW to RREGCK HIGH	7			40			35	ns
t_{MRWBH}	Master Reset LOW to W HIGH	7			50			50	ns
t_{AV}	Clock to address valid	7,9,10,12,13			50			40	ns
t_{ANV}	Clock to address not valid	7,9,10,12,13	15			15			ns
t_{ANVAV}	Address not valid to address valid	7,9,10,12,13			20			12	ns
t_{CWRL}	Clock to WRDY LOW	7,9			35			35	ns
t_{CWRH}	Clock to WRDY HIGH	7,9			40			35	ns
t_{CWRGL}	Clock to WREGCK LOW	7,9			35			30	ns
t_{CWRGH}	Clock to WREGCK HIGH	7,9			35			30	ns
t_{CWL}	Clock to W LOW	7,9			50			45	ns
t_{CWH}	Clock to W HIGH	7,9			25			25	ns
t_{AS}	Address valid to W LOW	7,9	0		12	0		12	ns
t_{WR}	Address not valid to W HIGH	7,9			0			0	ns
t_{WP}	W pulse width LOW at f_{CLK}(max)	9,13	100*			50**			ns
t_{PW}	W pulse width HIGH	4,13	12		30	12		25	ns
t_{WHAV}	W HIGH to address valid	4,9,13			35			25	ns
t_{WHWRCH}	W HIGH to WREGCK HIGH	4,13			25			18	ns
t_{CRRL}	Clock to RRDY LOW	10			35			30	ns
t_{CRRH}	Clock to RRDY HIGH	7,10			40			35	ns
t_{CRRGL}	Clock to RREGCK LOW	7,10			35			30	ns
t_{CRRGH}	Clock to RREGCK HIGH	7,10,12			35			30	ns
t_{ARRH}	Address valid to RREGCK HIGH at f_{CLK}(max)	10	110*			60**			ns
t_{ANRRH}	Address not valid to RREGCK HIGH	10			10			8	ns
t_{CE}	Clock to EMPTY flag	7,9,10			40			35	ns
t_{CF}	Clock to FULL flag	9,10			40			35	ns
t_{CHF}	Clock to Half-Full flag	9,10			50			45	ns
t_{CA}	Clock to Almost flag	9,10			60			55	ns
t_{LZ}	Address bit LOW to Hi-Z	15			30			30	ns
t_{HZ}	Address bit HIGH to Hi-Z	15			30			30	ns
t_{ZL}	Address bit Hi-Z to LOW	15			30			30	ns
t_{ZH}	Address bit Hi-Z to HIGH	15			30			30	ns

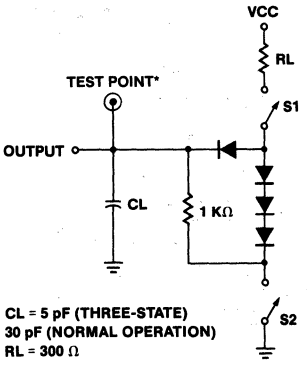
* f_{CLK}(max) = 12.5 MHz (Military).

** f_{CLK}(max) = 20 MHz (Commercial).

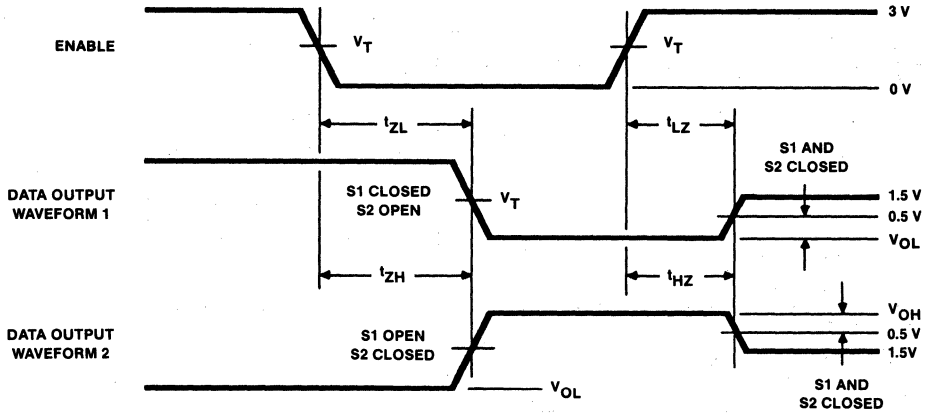
Standard Test Load



Load Circuit
for Bi-State Outputs
(Control and Flag Outputs)



Load Ciruit
for Three-State Outputs
(Address Outputs)



Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled.
Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled.

Figure 15. Enable and Disable Timing

Notes: A. C_L includes probe and jig capacitance.
B. All diodes are 1N916 or 1N306A.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
E. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz. Z_{out} = 50 Ω and t_R ≤ 2.5 ns t_F ≤ 2.5 ns.
F. When measuring propagation delay times of three-state outputs, switches S1 and S2 are closed.

67C4701

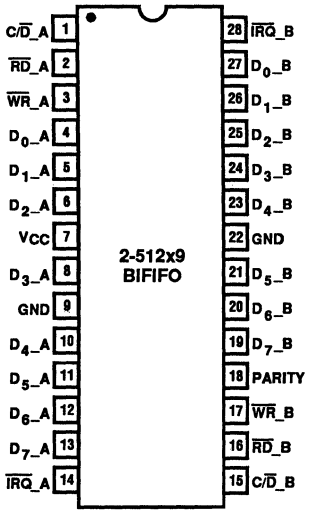
Bidirectional 512x9
FIFO (BIFIFO)

Advance Information

DISTINCTIVE CHARACTERISTICS

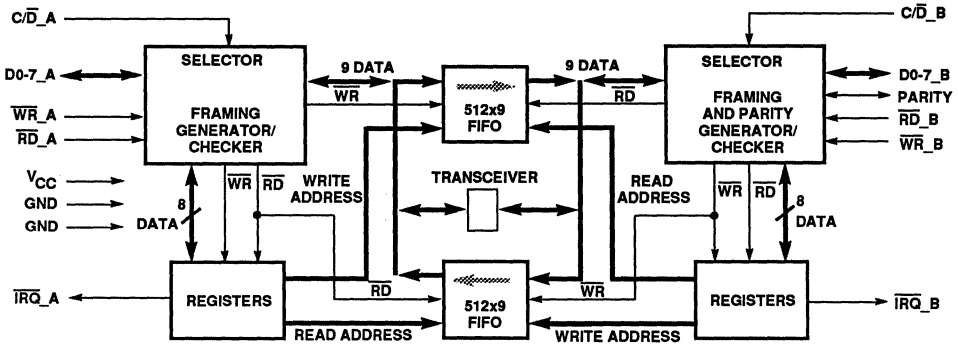
- 2-512x9 FIFO buffer, provides asynchronous bidirectional communication
- Programmable Almost-Full and Almost-Empty flags
- Byte detect mode
- No handshaking necessary
- Built in parity checker/generator
- Generates and detects framing bit
- Programmable Interrupt request
- Bypass mode – changes the BIFIFO to a transceiver
- Two mailboxes

PIN CONFIGURATION



28 PDIP
(600 mil)

BLOCK DIAGRAM



Publication # 10925A/D | Rev. A | Amendment /0
Issue Date: June 1988

Am2130/Am2140

1024 x 8 Dual-Port Static Random-Access Memories

DISTINCTIVE CHARACTERISTICS

- True dual port operation
- Access time as fast as 55 ns
- Master device (Am2130) has on-chip arbitration
- Expandable data bus width in multiples of 8 bits using one master (Am2130) and required number of slave devices (Am2140)
- Automatic power-down feature
- All inputs and outputs are TTL-compatible
- 48-pin DIP or 52-pin LCC/PLCC
- Single +5-volt power supply
- Advanced N-MOS technology

GENERAL DESCRIPTION

The Am2130 and the Am2140 are members of the 1K x 8 dual-port static RAM family. The Am2130 is designated as the master and the Am2140 as the slave device. The master provides the necessary control signal to the slave devices to facilitate implementing a wider data bus in a system. The master/slave concept allows expansion with minimal external logic.

Both devices have two independent ports called Left and Right port. Each port consists of an 8-bit bidirectional data bus and a 10-bit address input bus and necessary control signals.

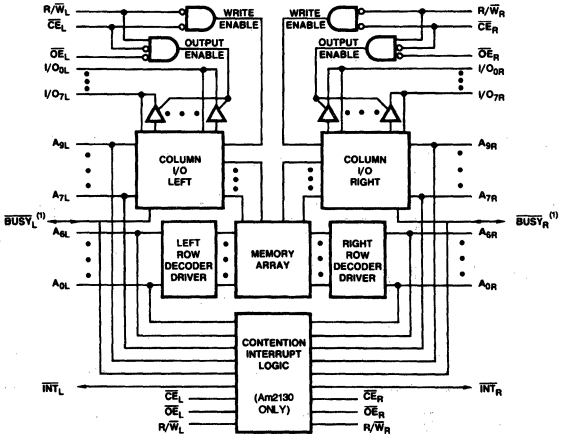
The Am2130 has an on-board arbiter to resolve contention between the left and right ports. When contention between ports occurs, one port is given priority while the other port receives a busy indication.

The Am2130 also contains on-chip facilities for supporting semaphores. Addresses $(3FE)_H$ and $(3FF)_H$ serve as interrupt generators. If any data is written at the address $(3FF)_H$ from the left port, an interrupt signal becomes active for the right port. The interrupt signal is deactivated by reading from the right port at the same address. The address $(3FE)_H$ is used in a similar fashion by the right port to activate the interrupt signal for the left port.

The Am2130/Am2140 also have two chip enable signals corresponding to the left and right ports. Before any transaction on a port takes place, the corresponding chip enable input must be activated. If a chip enable signal is not active, the circuitry corresponding to its side automatically powers down and enters standby mode.

The Am2130/Am2140 are packaged in 48-pin DIPs or 52-pin chip carriers. All inputs and outputs are TTL-compatible and the devices operate from a single +5-volt power supply.

BLOCK DIAGRAM



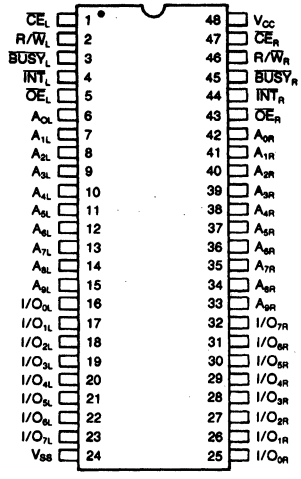
BD005085

Notes: 1. Am2130 (Master): BUSY is open-drain output and requires pull-up resistor.
Am2140 (Slave): BUSY is an input.

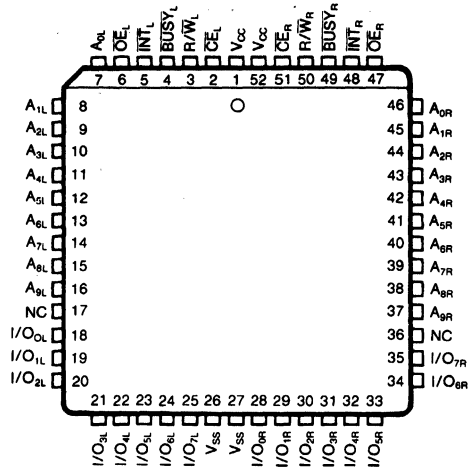
Publication # 05157 Rev. E Amendment /0
Issue Date: July 1988

CONNECTION DIAGRAMS
Top View

PLCC*



CD005813

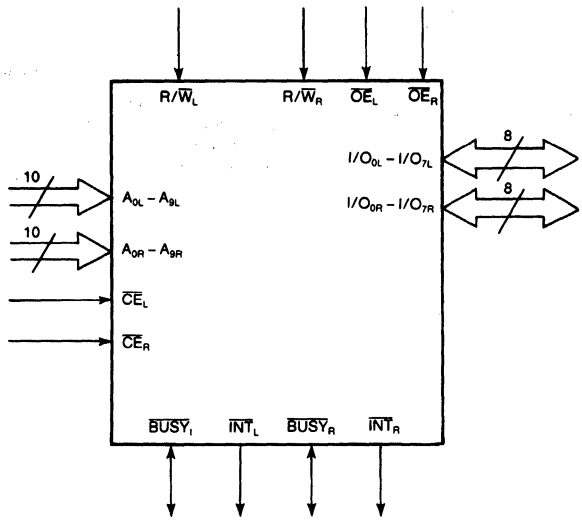


CD009600

* Same Pinouts apply for LCC.

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



LS002232

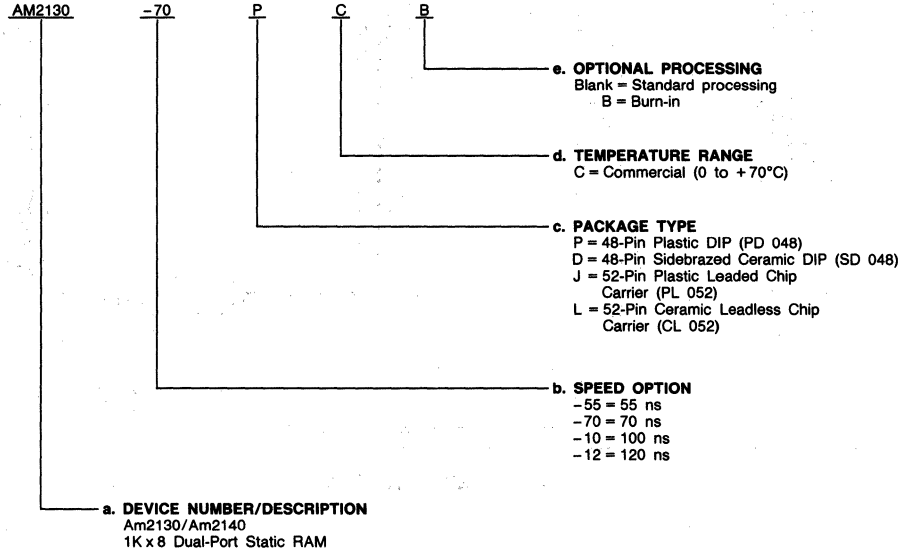
V_{CC} = +5-V Power Supply
V_{SS} = Ground

2

ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM2130-55	PC, PCB, DC, DCB, JC, JCB, LC, LCB
AM2130-70	
AM2130-10	
AM2130-12	
AM2140-55	
AM2140-70	
AM2140-10	
AM2140-12	

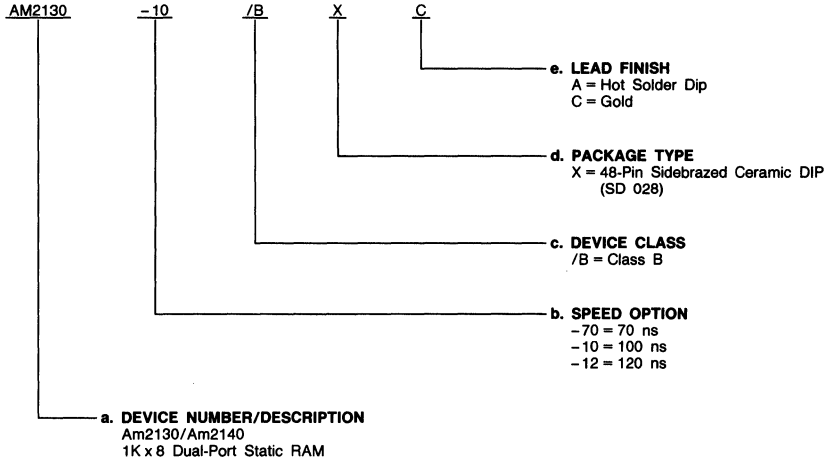
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM2130-70	/BXC
AM2130-10	
AM2130-12	
AM2140-70	
AM2140-10	
AM2140-12	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A Tests consist of subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am2130

$A_{0L} - A_{9L}$ Left Port Address (Inputs)
These 10 inputs constitute the memory address for the left port. A_0 is the least significant bit position and A_9 is the most significant position. A HIGH level on any of these inputs represents a logic 1 at that position and LOW represents a logic 0. The sequence of events and related timing for the address inputs during read and write operations will be discussed in later sections of this data sheet.

If a write operation is performed using $(3FF)_H$, an interrupt signal is activated for the right port (see $\overline{INT}_R$ pin description).

If a read operation is performed using $(3FE)_H$, the $\overline{INT}_L$ signal will be deactivated (see $\overline{INT}_L$ description).

$A_{0R} - A_{9R}$ Right Port Address (Inputs)
These 10 inputs constitute the memory address for the right port. A_0 is the least significant bit position and A_9 is the most significant position. A HIGH level on any of these inputs represents a logic 1 at that position and LOW represents a logic 0. The sequence of events and related timing for the address inputs during read and write operations will be discussed in later sections of this data sheet.

If a write operation is performed using $(3FE)_H$, an interrupt signal is activated for the left port (see $\overline{INT}_L$ pin description).

If a read operation is performed using $(3FF)_H$, the $\overline{INT}_R$ signal will be deactivated (see $\overline{INT}_R$ description).

$\overline{BUSY}_L$ Left Port Busy Flag (Output; Open Drain)
This open-drain output requires a pull-up resistor for proper operation. A LOW on this output indicates that the on-chip arbitration logic detected a contention between the left and right ports and the right port is given priority. All left port signals must be held stable until a HIGH on this output is indicated.

The $\overline{BUSY}_L$ signal generation is a logical function of the left and right port address inputs and the $\overline{CE}_L$ and $\overline{CE}_R$ inputs. The transient behavior of the $\overline{BUSY}_L$ output is not assured while the inputs are changing.

$\overline{BUSY}_R$ Right Port Busy Flag (Output; Open Drain)
This open-drain output requires a pull-up resistor for proper operation. A LOW on this output indicates that the on-chip arbitration logic detected a contention between the left and right ports and the left port is given priority. All right port signals must be held stable until a HIGH on this output is indicated.

The $\overline{BUSY}_R$ signal generation is a logical function of the left and right port address inputs and the $\overline{CE}_L$ and $\overline{CE}_R$ inputs. The transient behavior of the $\overline{BUSY}_R$ output is not assured while the inputs are changing.

$\overline{CE}_L$ Left Port Chip Enable (Input)
This input must be LOW before any transaction from the left port and remain LOW for the duration of the transaction. When this input goes HIGH, left port logic circuits enter standby power mode and remain in this mode as long as this input remains HIGH. It should be noted that powering down the left port to standby mode does not affect the $\overline{INT}_L$ or $\overline{INT}_R$ outputs. This input going HIGH also initializes the internal arbitration latch. It is recommended that $\overline{CE}_L$ go HIGH after completing a transaction (see discussion on arbitration).

$\overline{CE}_R$ Right Port Chip Enable (Input)
Operation of this input is identical to $\overline{CE}_L$ except that the $\overline{CE}_R$ input controls the right port.

GND (V_{SS}) Ground

$I/O_{0L} - I/O_{7L}$ Left Port Input/Output Bus (Input/Output; Three State)
These eight lines constitute the data bus for the left port. If a read operation is performed using the left port, data from the location addressed by the left port address will be available on these lines. Similarly, to perform a write operation using the left port, data to be written into the memory must be presented on these lines. The drivers on the chip to drive these lines are enabled only when the $\overline{CE}_L$ is LOW, $\overline{OE}_L$ is LOW and $R/\overline{W}_L$ is HIGH.

$I/O_{0R} - I/O_{7R}$ Right Port Input/Output Bus (Input/Output; Three State)
These eight lines constitute the data bus for the right port. If a read operation is performed using the right port, data from the location addressed by the right port address will be available on these lines. Similarly, to perform a write operation using the right port, data to be written into the memory must be presented on these lines. The drivers on the chip to drive these lines are enabled only when the $\overline{CE}_R$ is LOW, $\overline{OE}_R$ is LOW and $R/\overline{W}_R$ is HIGH.

$\overline{INT}_L$ Left Port Interrupt Flag (Output; Open Drain)
This open-drain output requires a pull-up resistor for proper operation. If the right port performs any write operation using address $(3FE)_H$, then this output goes LOW. It will remain LOW until the left port successfully completes any read operation using the address $(3FE)_H$. It should be noted that powering down the ports has no effect on this output.

$\overline{INT}_R$ Right Port Interrupt Flag (Output; Open Drain)
This open-drain output requires a pull-up resistor for proper operation. If the left port performs any write operation using address $(3FF)_H$, then this output goes LOW. It will remain LOW until the right port successfully completes any read operation using the address $(3FF)_H$. It should be noted that powering down the ports has no effect on this output.

$\overline{OE}_L$ Output Enable Left I/O Port (Input)
When this input is HIGH, the left port I/O bus lines are in high impedance state. If this input is LOW and $\overline{CE}_L$ is LOW and $R/\overline{W}_L$ is HIGH, the left port drivers are enabled and data from the location addressed by the $A_{0L} - A_{9L}$ inputs will be available on the I/O bus lines of the left port. It may be of interest to note that the $\overline{OE}_L$ input has no effect on the $\overline{BUSY}_L$ or $\overline{BUSY}_R$ or $\overline{INT}_L$ or $\overline{INT}_R$ signals. Even though the left port I/O port drivers are disabled when the $R/\overline{W}_L$ input goes LOW (write operation), it is recommended that the $\overline{OE}_L$ signal be kept HIGH during write operations to the left port.

$\overline{OE}_R$ Output Enable Right I/O Port (Input)
When this input is HIGH, the right port I/O bus lines are in high impedance state. If this input is LOW and $\overline{CE}_R$ is LOW and R/$\overline{W}_R$ is HIGH, the right port drivers are enabled and data from the location addressed by the $A_{0R} - A_{9R}$ inputs will be available on the I/O bus lines of the right port. It may be of interest to note that the $\overline{OE}_R$ input has no effect on the $\overline{BUSY}_L$ or $\overline{BUSY}_R$ or $\overline{INT}_L$ or $\overline{INT}_R$ signals. Even though the left port I/O port drivers are disabled when the R/$\overline{W}_R$ input goes LOW (write operation), it is recommended that the $\overline{OE}_R$ signal be kept HIGH during write operations to the right port.

R/$\overline{W}_L$ Left Port Read/$\overline{Write}$ Enable (Input)
This input is used to specify the left port function to be performed. HIGH indicates a read and LOW indicates a write function.

When the $\overline{CE}_L$ is LOW and the $\overline{OE}_L$ is LOW and the R/$\overline{W}_L$ is HIGH, data from the location addressed by the $A_{0L} - A_{9L}$ will be available on the $I/O_{0L} - I/O_{7L}$ lines. As mentioned earlier, reading from the left port at the location $(3FE)_H$ disables the $\overline{INT}_L$ output.

When the $\overline{CE}_L$ is LOW and the R/$\overline{W}_L$ goes LOW, data present on the $I/O_{0L} - I/O_{7L}$ lines will be written into the location addressed by the $A_{0L} - A_{9L}$ inputs. It should be noted that the write operation is not affected by the $\overline{OE}_L$ input. However, it is recommended that the $\overline{OE}_L$ input be held HIGH during a write operation. As mentioned earlier, performing a write operation from the left port at the address $(3FF)_H$ causes the $\overline{INT}_R$ output to go LOW.

It should be noted that even though R/$\overline{W}_L$ is LOW, writing is internally inhibited if the right port is given priority by the arbiter. Discussion on arbitration can be found in a later section.

R/$\overline{W}_R$ Right Port Read/$\overline{Write}$ Enable (Input)
This input is used to specify the right port function to be performed. HIGH indicates a read and LOW indicates a write function.

When the $\overline{CE}_R$ is LOW and the $\overline{OE}_R$ is LOW and the R/$\overline{W}_R$ is HIGH, data from the location addressed by the $A_{0R} - A_{9R}$ will be available on the $I/O_{0R} - I/O_{7R}$ lines. As mentioned earlier, reading from the right port at the location $(3FF)_H$ disables the $\overline{INT}_R$ output.

When the $\overline{CE}_R$ is LOW and the R/$\overline{W}_R$ goes LOW, data present on the $I/O_{0R} - I/O_{7R}$ lines will be written into the location addressed by the $A_{0R} - A_{9R}$ inputs. It should be noted that the write operation is not affected by the $\overline{OE}_R$ input. However, it is recommended that the $\overline{OE}_R$ input be held HIGH during a write operation. As mentioned earlier, performing a write operation from the left port at the address $(3FE)_H$ causes the $\overline{INT}_L$ output to go LOW.

It should be noted that even though R/$\overline{W}_R$ is LOW, writing is internally inhibited if the left port is given priority by the arbiter. Discussion on arbitration can be found in a later section.

V_{CC} +5-Volt Power Supply

2

Am2140

The Am2140 is functionally very similar to the Am2130. The Am2140 differs from the Am2130 in two signals only — $\overline{BUSY}_L$ and $\overline{BUSY}_R$. In the case of the Am2140 they are used as inputs and play a significant role in expanding the word width.

$\overline{BUSY}_L$ Left Port Busy Flag (Input)
If this input is LOW, a write enable signal to the left side of the memory array is internally disabled. In expanded systems where an Am2130 is used as the master, this input is connected to the $\overline{BUSY}_L$ output of the Am2130.

$\overline{BUSY}_R$ Right Port Busy Flag (Output; Open Drain)
If this input is LOW, a write enable signal to the right side of the memory array is internally disabled. In expanded systems where an Am2130 is used as the master, this input is connected to the $\overline{BUSY}_R$ output of the Am2130.

FUNCTIONAL DESCRIPTION

As shown in the block diagram, the Am2130/Am2140 is a true 1K x 8 dual-port RAM. It consists of a memory array with two sets of address decoders and associated logic. This arrangement allows the accessing of every word in the memory array from two independent sources. We call these sources left side and right side for convenience. Data accessed by the left-side address inputs appears on the left-side data lines of the array and is connected to the left-side I/O pins through the associated three-state buffers. The enable control signal for these buffers is generated using the $R/\overline{W}_L$, $\overline{CE}_L$ and $\overline{OE}_L$ inputs. If the I/O buffers are disabled on the chip, the I/O pins can be used as inputs. Data to be written from the left port is presented on these inputs. Writing into the memory array from the left side is controlled by the left write enable signal generated on the chip using the $R/\overline{W}_L$ and $\overline{CE}_L$ inputs. An identical arrangement exists for the right side also. In addition, there is on-chip arbitration logic to give priority to one port over the other in case of a contention, and interrupt flag logic.

Contention Arbitration

Two independent access facilities are provided in a dual-port memory to eliminate physical interference between signals. However, there are two significant possibilities of "logical" interference which are not tolerable: when one port is reading from a location while the other port is writing into the same location at the same time. In this case, data received by the reading port may not be predictable. Similarly, consider the situation when both ports write information into the same location simultaneously. The resultant data that finally ends up in the memory location may not be valid. These two situations are commonly called contention. The Am2130 has on-chip logic to detect contention and give priority to one port over the other. In a true dual-port RAM, simultaneous reading from both ports at the same address does not corrupt the data. Hence, it can be construed that no contention occurs. However, for the sake of simplicity and compatibility with the industry standard practices, the Am2130 arbitration is based purely on addresses. Hence, in the case of a simultaneous read from both ports at the same address, the arbitration logic will sense contention and give priority to one of the ports. The other port will receive a busy indication.

Figure 1 is a conceptual logic diagram of contention arbitration logic. It consists of two equality comparators. The left comparator compares the left port address inputs to the delayed version of the right port address. Similarly, the right comparator compares the right-port address to the delayed version of the left port address. The output of the comparators is connected to a latch formed by two cross-coupled NAND gates as shown in Figure 1. The chip enable signals, $\overline{CE}_L$ and $\overline{CE}_R$, are also inputs to this latch as shown. The $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs are generated by gating the latch output with the proper chip enable signal as shown. Also note that the latch outputs are used internally for left and right write inhibit signals. For example, if the right side write inhibit signal in Figure 1 is LOW, writing into the memory does not occur even if the $R/\overline{W}_R$ input of the Am2130 is LOW.

The operation of the arbitration circuit can now be explained. Assume that the left port address had been stable and $\overline{CE}_L$ is LOW. Both Q and Q' outputs of the latch will be HIGH because the output of both comparators is LOW (addresses are different). So the $\overline{BUSY}$ output on both sides is HIGH. Now assume that the right address changes and becomes equal to the left address. The right address comparator output goes HIGH and the Q' output of the latch goes LOW. Eventually the output of the left comparator also goes HIGH, but because of the cross coupling of the Q' into the gate generating the Q output, Q output remains HIGH. As soon as the $\overline{CE}_R$ input goes LOW, $\overline{BUSY}_R$ becomes LOW. Thus, the arbitrator gave priority to the left port by indicating a busy signal to the right port. Thus in this example, the left port is the winner and the right port is the loser in the contention for the memory. Sooner or later the left port will finish its transaction at the contended location and change the address or its chip enable will go HIGH. Thus when the contention is over the Q output of the latch will become HIGH and $\overline{BUSY}_R$ will go HIGH. A similar reasoning can be used to understand the operation of the left side. It should be clear then, in cases of contention, the arbiter will decide one port as the winner and the losing port must wait for the winner to complete the use of the memory. The winning port must indicate to the arbiter that it has completed its operation either by changing the address or making its chip enable input HIGH. Without such an indication, the arbiter will not remove the busy indication to the losing port.

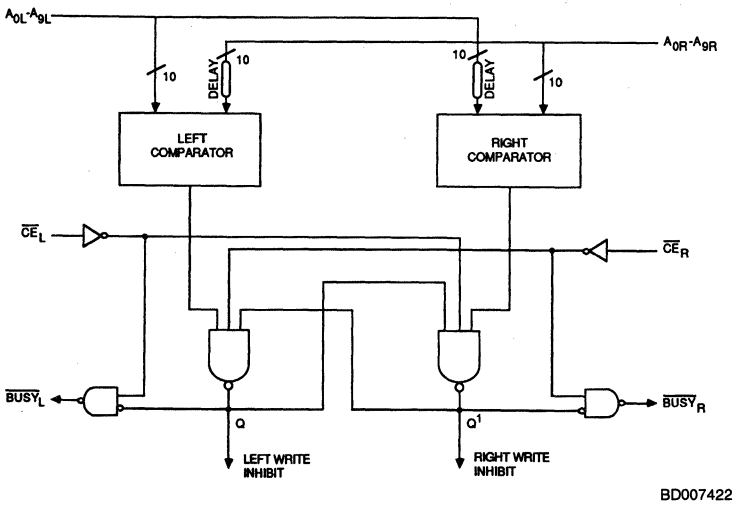


Figure 1. Conceptual Arbitration Logic

Read/Write Operations

Performing read/write operations when there is no contention is relatively straightforward. The sequence of events for a read is listed below. The timing relationships between various signals can be found in later sections of this data sheet.

1. Establish HIGH on the R/$\overline{W}$ and LOW on the $\overline{CE}$ input of the desired port.
2. Establish the desired address on the desired port address lines.
3. Make the $\overline{OE}$ input of the desired port LOW.
4. The I/O lines of the selected port will contain the data after the access time has elapsed.
5. Make the output enable and chip enable inputs HIGH to complete the read operation.

Performing write operations when there is no contention is equally straightforward. The sequence of events for a write is listed below. The timing relationships between various signals can be found in later sections of this data sheet.

1. Establish LOW on the $\overline{CE}$ input of the desired port.
2. Establish the desired address on the desired port address lines.
3. Establish the desired data on the I/O lines of the port.
4. Make the R/$\overline{W}$ input of the port LOW and bring it HIGH after the specified amount of time.
5. Make the $\overline{CE}$ input HIGH to complete the operation.

When a read or write operation is initiated by a port and contention from the other port occurs, the implications are very simple. The losing port will see its $\overline{BUSY}$ line go LOW. The port must wait until a HIGH is indicated on the $\overline{BUSY}$ line. Thus in this case of contention, the operation did not really start when the port initiated it. Instead, the operation actually started when the $\overline{BUSY}$ line went HIGH. See the timing diagram for details.

Interrupts

Each port has an associated output called interrupt. The interrupt outputs are activated and deactivated by the on-chip logic when read and write operations occur with a particular address location. For example, if a write operation is performed by the left port with address $(3FF)_H$, an on-chip latch is set. This latch drives the $\overline{INT}_R$ output LOW. The latch is cleared only when a read operation from the right port using the address $(3FF)_H$ takes place. Similarly, if a write operation from the right port using the address $(3FE)_H$ occurs, a latch is set to drive the $\overline{INT}_L$ output LOW. The $\overline{INT}_L$ will go HIGH (latch is cleared) only after a read operation from the left port using the address $(3FE)_H$ occurs. As mentioned before, powering down a port to standby mode does not affect these outputs.

Depth Expansion Using Multiple Am2130s

The Am2130 has an intrinsic storage capacity of 1K bytes. However, it is simple to expand the storage capacity by using multiple devices. Figure 2 is a conceptual diagram of a 2K byte dual port memory system using two Am2130 devices. The principle behind such expansion is obvious: all that needs to be done is to decode the most significant system address to generate the individual $\overline{CE}$ inputs for the Am2130s. For example in Figure 2, A_{10} is the most significant address bit. When this signal is LOW and $\overline{CE}$ input is LOW, the chip enable input of the upper Am2130 goes LOW. Thus, the first 1K locations are selected for transactions. On the other hand, if A_{10} is HIGH and $\overline{CE}$ is LOW, the chip enable input of the lower Am2130 goes LOW selecting the second 1K locations. As depicted in the figure, the address inputs of both Am2130 devices are bussed together. Similarly, the I/O signals are also bussed to create the overall data bus. Also note that the other control signals are connected between the two devices.

In this example, we have not used the interrupt outputs. However, it should be noted that depth expansion using multiple devices does not change the operation of the interrupt outputs. The interrupt output of each device behaves as described before. Hence, the user must decide which interrupt output from which device will be used in his system.

Width Expansion

The intrinsic width of the data word of the Am2130 is eight bits. However, it is possible to realize wider data words (multiples of 8) by using multiple devices. The instinctive solution of taking the required number of the devices and assigning the data bits to individual devices is potentially unreliable. As we know, the Am2130 has arbitration logic on the chip, and hence is called the master. When several of these masters are present, device-to-device variations and other factors may cause one device to give priority to one port, while another device gives priority to the other port. In essence both ports are busy! This is an undesirable situation and should not be allowed in operation. The most elegant way to avoid the situation is to allow only one device to arbitrate the contention. It is recommended that when expanding the width of the data words, the Am2130 be used as the master and a number of Am2140s be used as slave devices. The Am2140 does not have the arbitration capability; instead it accepts the $\overline{BUSY}$ outputs generated by the Am2130 as inputs.

Figure 3 is a conceptual diagram of a 16-bit system using one Am2130 and one Am2140. As can be seen, using master/slave devices avoids external logic for expansion. For the sake of completeness of this discussion, it may be noted that it is indeed possible to expand the width using Am2130s only. However, external logic must be provided to prevent every device of the system from arbitrating. We want only one device to be the arbitrator. As explained in Figure 1, arbitration can be defeated by suitable control of the $\overline{CE}$ input of the Am2130.

Figure 4 shows a conceptual diagram of a 16-bit system using two Am2130s. Device 1 in this figure behaves as the master. The external logic shown in the figure ensures that the $\overline{CE}$ input of Device 2 is HIGH if the corresponding $\overline{BUSY}$ output of Device 1 is LOW. Thus the arbitration logic of Device 2 is prevented from taking part in resolving contention.

Simultaneous Width and Depth Expansion

By combining the depth and width expansion schemes discussed, it is possible to build systems with greater depth (multiples of 1K) and wider words (multiples of 8). Figure 5 shows a conceptual diagram of a 2K x 16 system. The operation of this scheme is understood by suitably combining the explanation of Figure 2 and Figure 3 and hence is not repeated here.

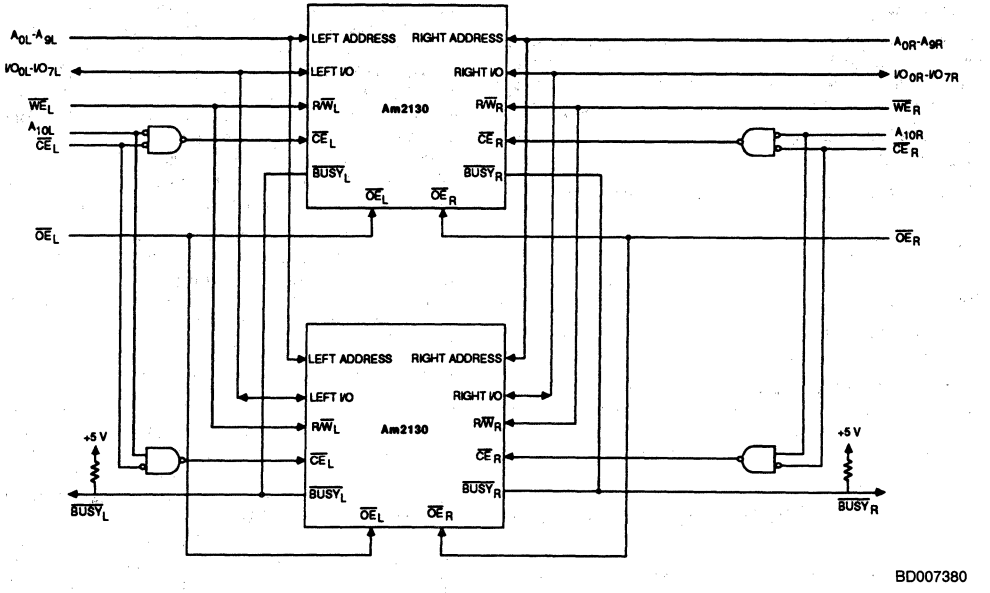


Figure 2. Conceptual Depth Expansion

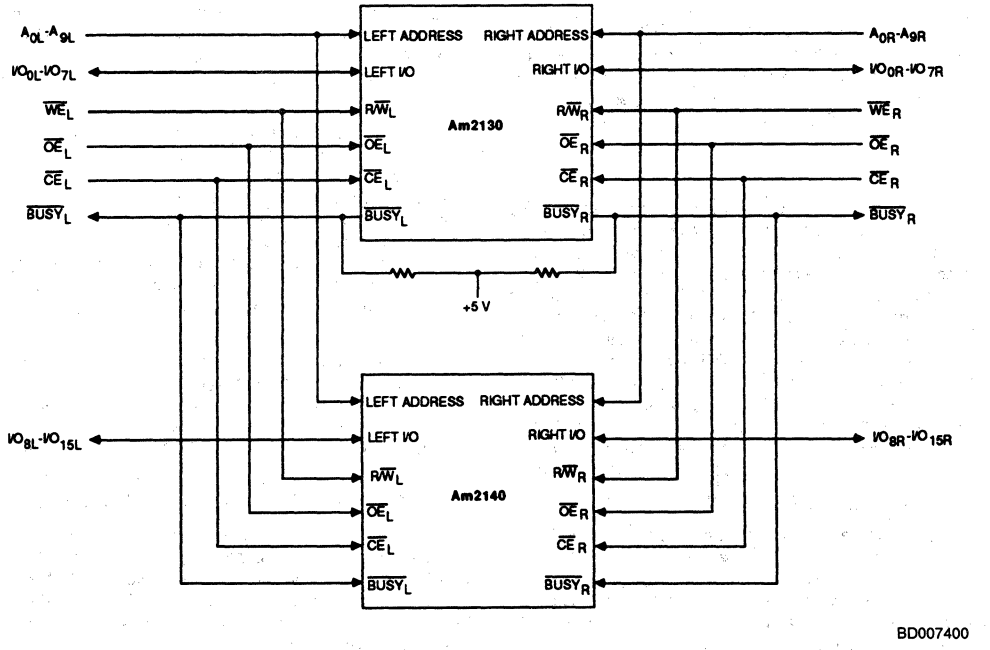


Figure 3. Width Expansion with Master/Slave

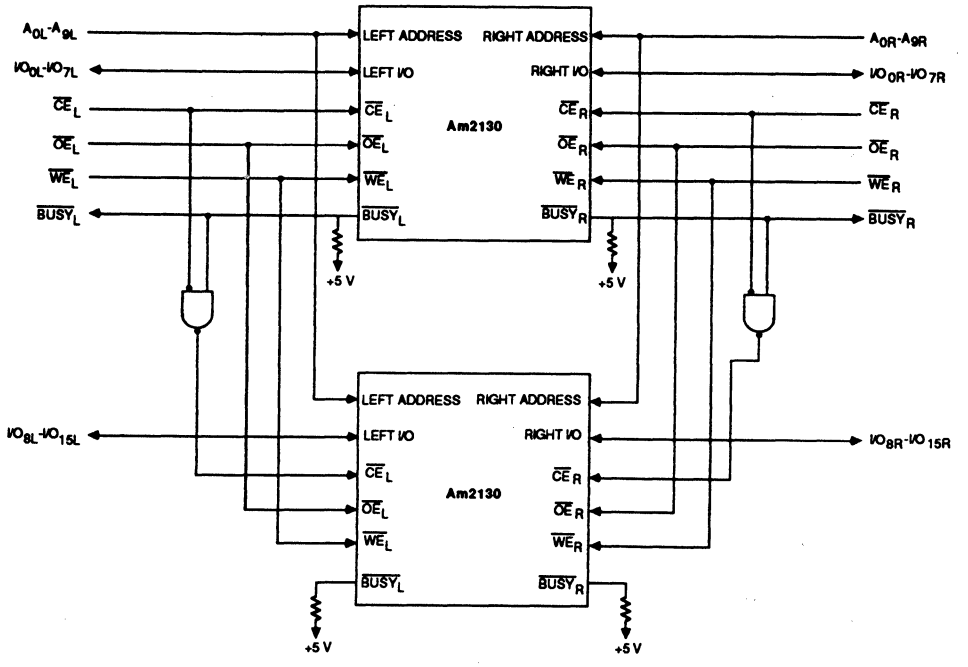


Figure 4. Width Expansion with Master

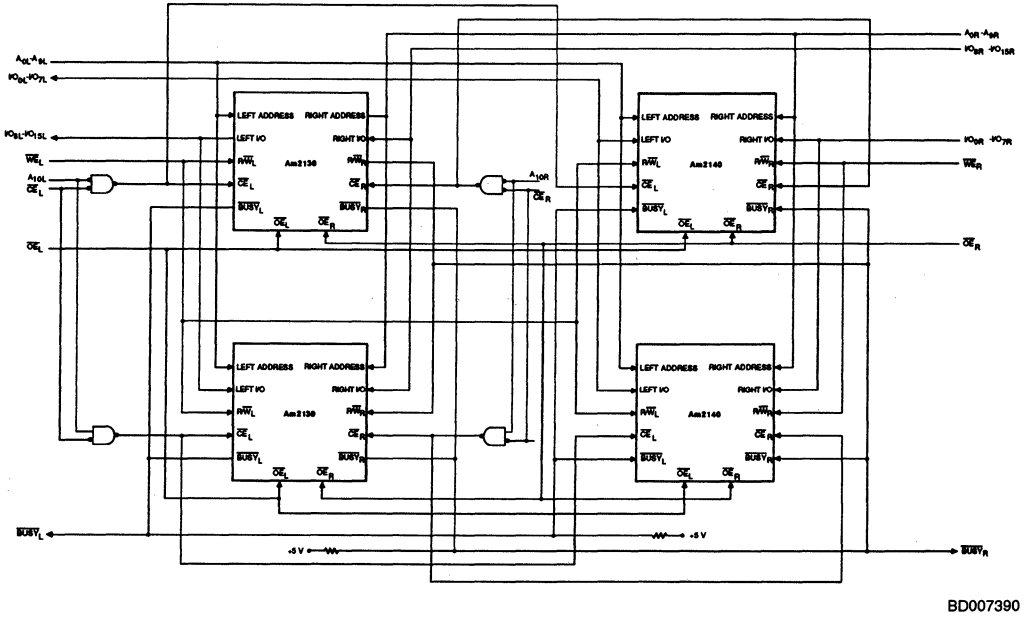


Figure 5. Conceptual Diagram of a 2K x 16 System Using Master/Slave

TABLE 1. NON-CONTENTION READ/WRITE CONTROL

	Left Port Inputs			Right Port Inputs				Left Flags		Right Flags		
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L}-A_{9L}$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0R}-A_{9R}$	$\overline{BUSY}_L$	$\overline{INT}_L$	$\overline{BUSY}_R$	$\overline{INT}_R$	Function
X	H	X	X	X	X	X	X	H	X	H	X	Left port in power-down mode
X	X	X	X	X	H	X	X	H	X	H	X	Right port in power-down mode
L	L	X	X	X	X	X	X	H	X	X	X	Data on left port written to memory location $A_{0L}-A_{9L}$
H	L	L	X	X	X	X	X	H	X	X	X	Data in memory location $A_{0L}-A_{9L}$ output on left port
X	X	X	X	L	L	X	X	X	X	H	X	Data on right port written to memory location $A_{0R}-A_{9R}$
X	X	X	X	H	L	L	X	X	X	H	X	Data in memory location $A_{0R}-A_{9R}$ output on right port
L	L	X	3FF	X	X	X	X	H	X	H	L	Left port flags right port to read memory location 3FF
X	X	X	X	L	L	X	3FE	H	L	H	X	Right port flags left port to read memory location 3FE

TABLE 2. BUSY ARBITRATION OF ADDRESS CONTENTION

Left Port				Right Port				Flags (Note 1)		
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L}-A_{9L}$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0R}-A_{9R}$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	Function
X	L (LIV)	X	Match	X	L	X	Match	L	H	Right-Port operation only is permitted. (Note 3)
X	L	X	Match (LIV)	X	L	X	Match	L	H	
X	L	X	Match	X	L (LIV)	X	Match	H	L	Left-port operation only is permitted. (Note 4)
X	L	X	Match	X	L	X	Match (LIV)	H	L	

TABLE 3. INTERRUPT FLAG

Left Port					Right Port					
$R/\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{0L}-A_{9L}$	$\overline{INT}_L$	$R/\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{0R}-A_{9R}$	$\overline{INT}_R$	Function
L	L	X	3FF	X	X	X	X	X_1	L	Set $\overline{INT}_R$
X	X	X	X_1	X	H	L	L	3FF	H	Reset $\overline{INT}_R$
X	X	X	X_1	L	L	L	X	3FE	X	Set $\overline{INT}_L$
H	L	L	3FE	H	X	X	X	X_1	X	Reset $\overline{INT}_L$

Key: H = HIGH
L = LOW
LIV = Last Input Valid; meets t_{APS} spec (Note 2)
X = Don't Care
X_1 = No Match, or
Same port deselected, or
Opposite port has priority

Notes: 1. INT Flags = X
2. If LIV violates t_{APS} spec then one of the two ports receives priority, and the remaining port's $\overline{BUSY}$ Flag goes LOW. However, there is an extremely rare metastable event which can occur when the arbitration circuitry cannot determine which port was "first" at the matching address. On this rare occurrence, both ports may momentarily receive $\overline{BUSY}$ = LOW signals until the metastable state is resolved (usually within a few nanoseconds). Thereafter, one port's $\overline{BUSY}$ remains LOW while the other completes its operation and resumes normal operation.
3. A Left-Port Read operation is also permitted if the Right-Port is also reading.
4. A Right-Port Read operation is also permitted if the Left-Port is also reading.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Ambient Temperature
with Power Applied ..... −55 to +125°C
Supply Voltage
with Respect to Ground ..... −0.5 to +7.0 V
All Signal Voltages ..... −3.5 to +7.0 V
Power Dissipation ..... 1.2 W

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices (Note 8)
Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Military (M) Devices (Note 8)*
Temperature (T_A) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Am2130/Am2140 Min.	Am2130/Am2140 Max.	Units
I_{LI}	Input Load Current (All Input Pins)	V_{CC} = Max., V_{IN} = GND to V_{CC}			10	µA
I_{LO}	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{CC} = Max., V_{OUT} = GND to V_{CC}			10	µA
I_{CC}	Power Supply Current (Both Ports Active)	V_{CC} = Max., $\overline{CE}$ = V_{IL} Outputs Open	C Devices		170	mA
			M Devices		185	
I_{SB1}	Standby Current (Both Ports Standby)	V_{CC} = Min. to Max., $\overline{CE_L}$ and $\overline{CE_R}$ = V_{IH}	C Devices		30	mA
			M Devices		40	
I_{SB2}	Standby Current (One Port Standby)	V_{CC} = Max., $\overline{CE_L}$ = V_{IL} and $\overline{CE_R}$ = V_{IH} or $\overline{CE_L}$ = V_{IH} and $\overline{CE_R}$ = V_{IL}	C Devices		110	mA
			M Devices		125	
V_{IL1}	Input LOW Voltage (I/O_n)			−0.5	0.8	V
V_{IL2}	Input LOW Voltage (All Addresses & Clocks)			−2.0	0.8	V
V_{IH}	Input HIGH Voltage			2.2	6.0	V
V_{OL1}	Output LOW Voltage (I/O_0 − I/O_7)	I_{OL} = 3.2 mA			0.4	V
V_{OL2}	Open-Drain Output LOW Voltage ($\overline{BUSY}$ (Note 14), $\overline{INT}$)	I_{OL} = 4 mA (Note 7)			0.5	V
V_{OH}	Output HIGH Voltage	I_{OH} = −1.0 mA (Note 7)		2.4		V

CAPACITANCE (Note 9)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
C_{OUT} †	Output Capacitance			10	pF
C_{IN} †	Input Capacitance			10	

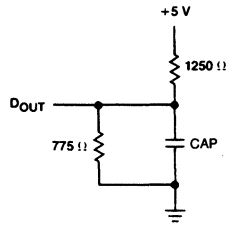
Notes: See notes following Switching Waveforms.
† Not included in Group A Tests.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 7, 8, 9, 10, 11 are tested unless otherwise noted)

No.	Parameter Symbol	Parameter Description	Test Conditions	Am2130/Am2140								Units
				-55		-70		-10		-12		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE (Note 10)												
1	t_{RC}	Read Cycle Time		55		70		100		120		ns
2	t_{AA}	Address Access Time			55		70		100		120	ns
3	t_{ACE}	Chip Enable Access Time			55		70		100		120	ns
4	t_{AOE}	Output Enable Access Time			30		35		40		60	ns
5	t_{OH}	Output Hold from Address Change		5		5		5		5		ns
6	t_{LZ} †	Output Low Z Time	(Notes 5 & 9)	5		5		5		5		ns
7	t_{HZ} †	Output High Z Time	(Notes 5 & 9)	0	25	0	30	0	40	0	40	ns
8	t_{PU} †	Chip Enable to Power Up Time	(Note 9)	0		0		0		0		ns
9	t_{PD} †	Chip Disable to Power Down Time	(Note 9)		35		35		50		60	ns
WRITE CYCLE (Note 10)												
10	t_{WC}	Write Cycle Time		55		70		100		120		ns
11	t_{EW}	Chip Enable to End of Write		55		65		90		100		ns
12	t_{AW}	Address Valid to End of Write		50		65		90		100		ns
13	t_{AS}	Address Setup Time		0		0		0		0		ns
14	t_{WP}	Write Pulse Width		45		50		60		70		ns
15	t_{WR}	Write Recovery Time		0		0		0		0		ns
16	t_{DW}	Data Valid to End of Write		30		35		40		40		ns
17	t_{DH}	Data Hold Time		0		0		0		0		ns
18	t_{WZ} †	Write Enabled to Output in High Z	(Notes 5 & 9)	0	25	0	30	0	40	0	50	ns
19	t_{OW} †	Output Active from End of Write	(Notes 5 & 9)	0		0		0		0		ns
$\overline{\text{BUSY}}$ FLAG TIMING (Notes 7 & 14)												
20	t_{RC}	Read Cycle Time		55		70		100		120		ns
21	t_{WC}	Write Cycle Time		55		70		100		120		ns
22	t_{BW}	$\overline{\text{BUSY}}$ to Write	(Note 13)	-5		-5		-5		-5		ns
23	t_{WH}	Write Hold After $\overline{\text{BUSY}}$	(Note 13)	20		20		20		20		ns
24	t_{BAA} †	$\overline{\text{BUSY}}$ Access Time to Address	(Note 9)		45		45		50		60	ns
25	t_{BDA} †	$\overline{\text{BUSY}}$ Disable Time to Address	(Note 9)		40		45		50		60	ns
26	t_{BAC} †	$\overline{\text{BUSY}}$ Access Time to Chip Enable or Chip Select	(Note 9)		40		45		50		60	ns
27	t_{BDC} †	$\overline{\text{BUSY}}$ Disable Time to Chip Enable or Chip Select	(Note 9)		40		45		50		60	ns
28	t_{APS}	Arbitration Priority Setup Time		10		10		10		10		ns
INTERRUPT TIMING (Note 7)												
29	t_{WINS}	$\overline{\text{WE}}$ to Interrupt Set Time			30		30		35		45	ns
30	t_{EINS}	$\overline{\text{CE}}$ to Interrupt Set Time			50		55		60		70	ns
31	t_{INS}	Address to Interrupt Set Time			50		55		60		70	ns
32	t_{OINR}	Output Enable to Interrupt Reset Time			30		30		35		45	ns
33	t_{INR}	Address to Interrupt Reset Time			50		55		60		70	ns
34	t_{EINR}	Chip Enable to Interrupt Reset Time			50		55		60		70	ns

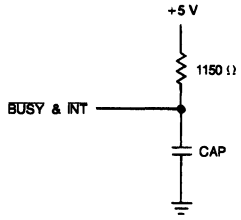
Notes: See notes following Switching Waveforms.
† Not included in Group A tests.

SWITCHING TEST CIRCUITS



TC002201

Test Loads A and B



TC002222

Test Loads C and D

TEST OUTPUT LOADS	
Test Load	**CAP**
A	5 pF (Note 1)
B	100 pF
C	50 pF
D	5 pF (Note 1)

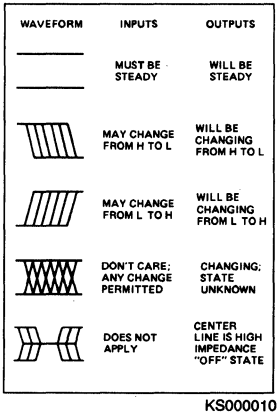
Notes: 1. Includes Scope and Jig Capacitance.

SWITCHING TEST WAVEFORM

AC Test Conditions	
Input Levels	GND to 3.0 V
Input Rise and Fall Times	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Test Output Load	See Test Output Loads Table

SWITCHING WAVEFORMS

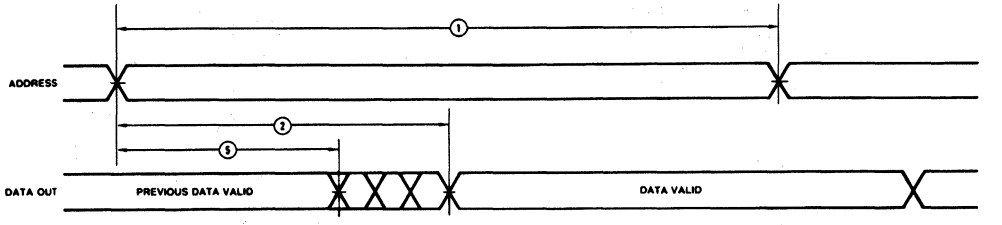
KEY TO SWITCHING WAVEFORMS



KS000010

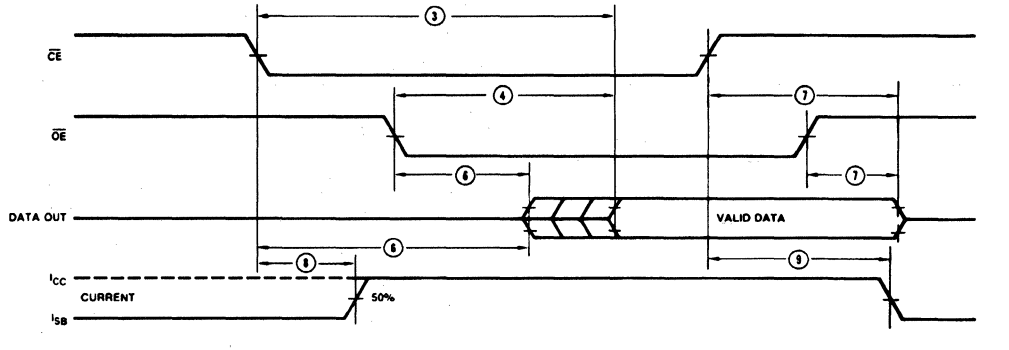
SWITCHING WAVEFORMS (Cont'd.)

READ CYCLE
(Either Side)



WF009391

Address Access
(Notes 1 & 2)

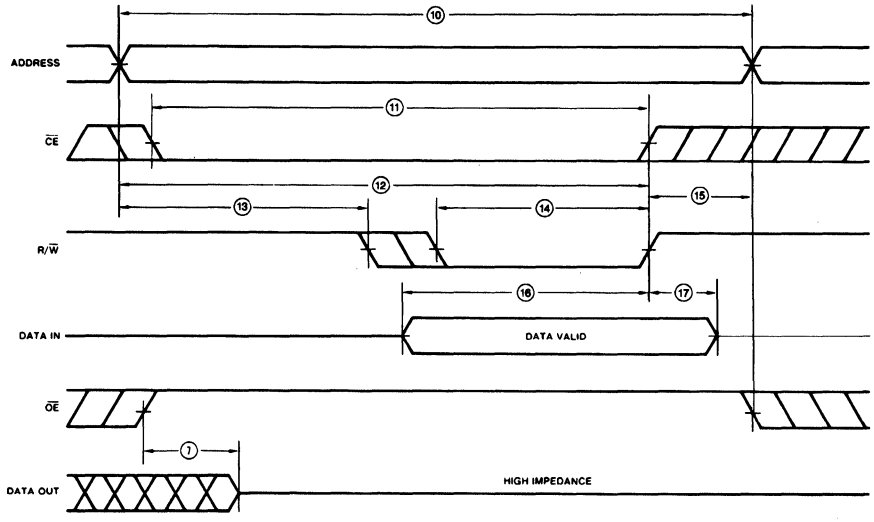


WF009401

$\overline{CE}$ and $\overline{OE}$-Controlled Access
(Notes 1 & 3)

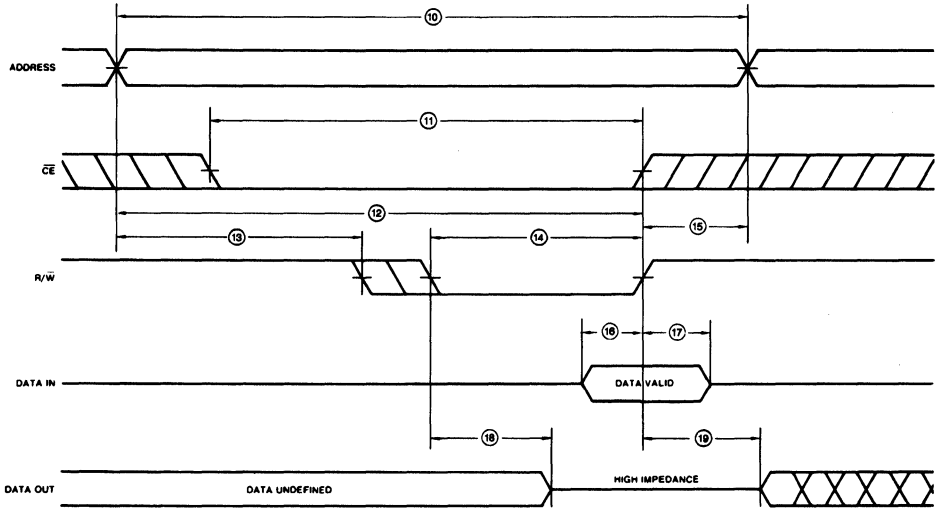
SWITCHING WAVEFORMS (Cont'd.)

WRITE CYCLE
(Either Side — Note 4)



WF009411

OE-Controlled Data Out

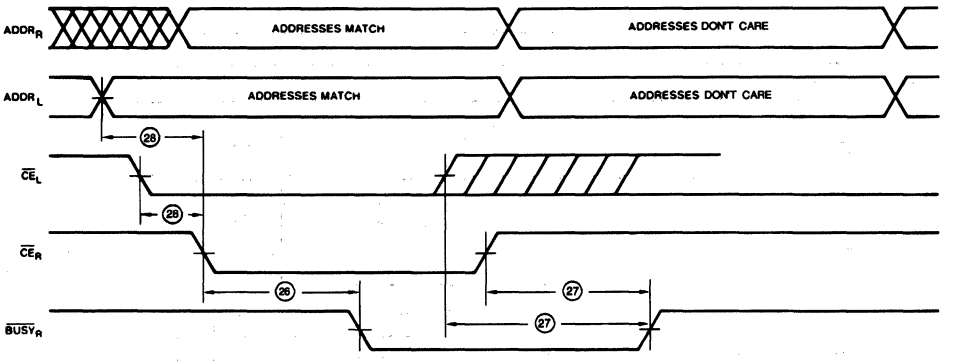


WF009421

WE-Controlled Data Out
(OE = V_{IL})

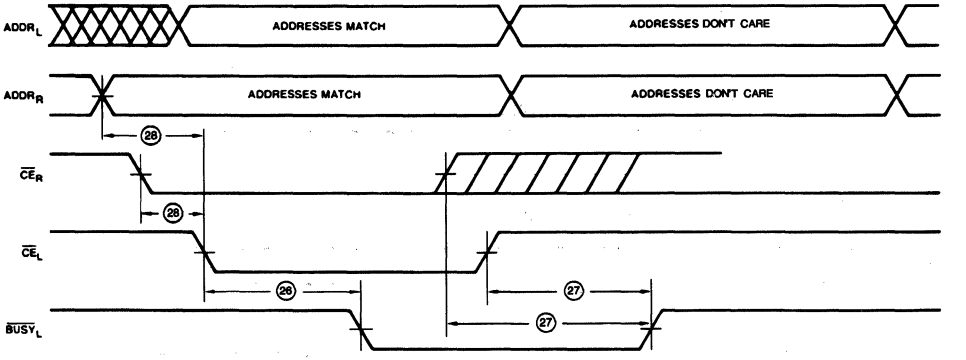
SWITCHING WAVEFORMS (Cont'd.)

$\overline{BUSY}$ FLAG TIMING (1 of 2) (Note 12)
(Chip Enable Arbitration)



WF009433

$\overline{CE}_R$ Valid Last

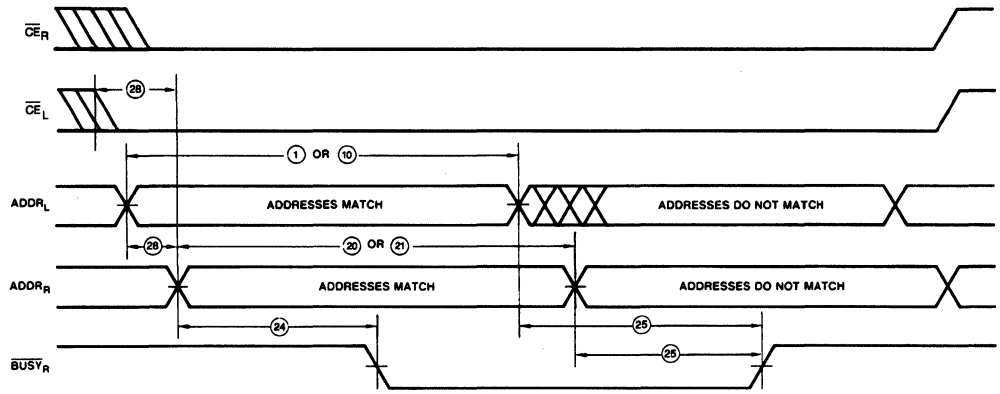


WF009434

$\overline{CE}_L$ Valid Last

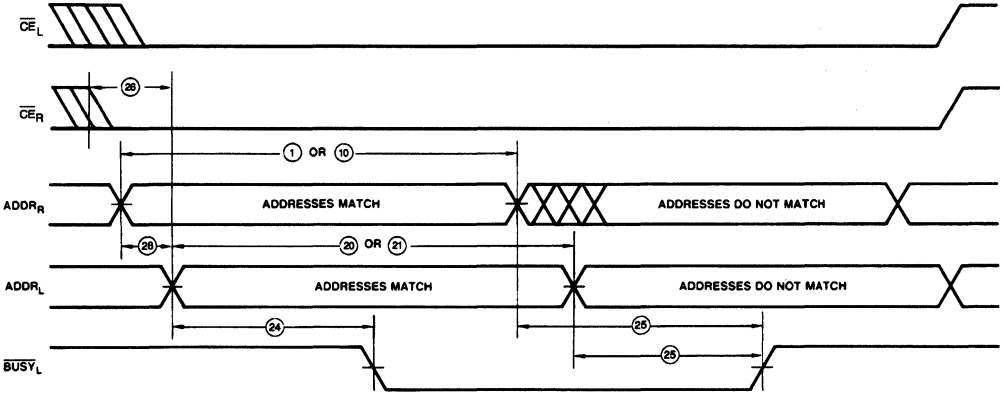
SWITCHING WAVEFORMS (Cont'd.)

$\overline{BUSY}$ FLAG TIMING (2 of 2)
(Address Arbitration)



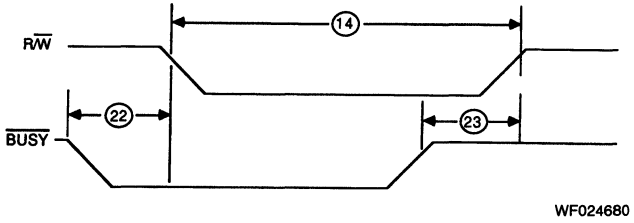
WF009443

$ADDR_R$ Valid Last



WF009444

$ADDR_L$ Valid Last

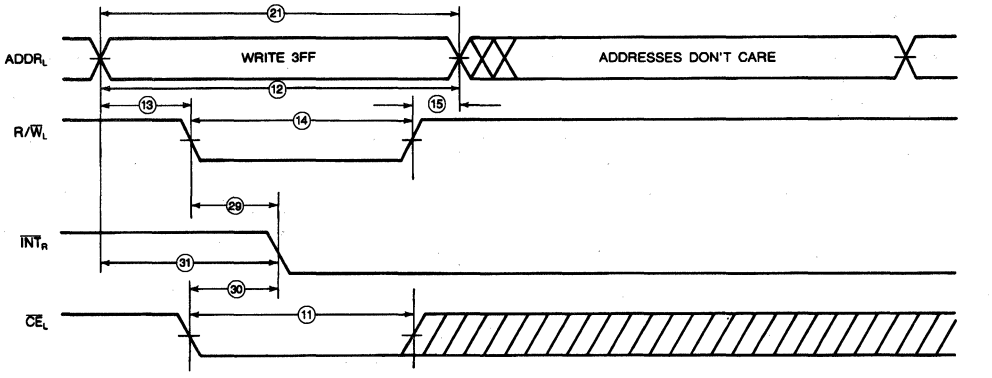


WF024680

For Am2140 Only

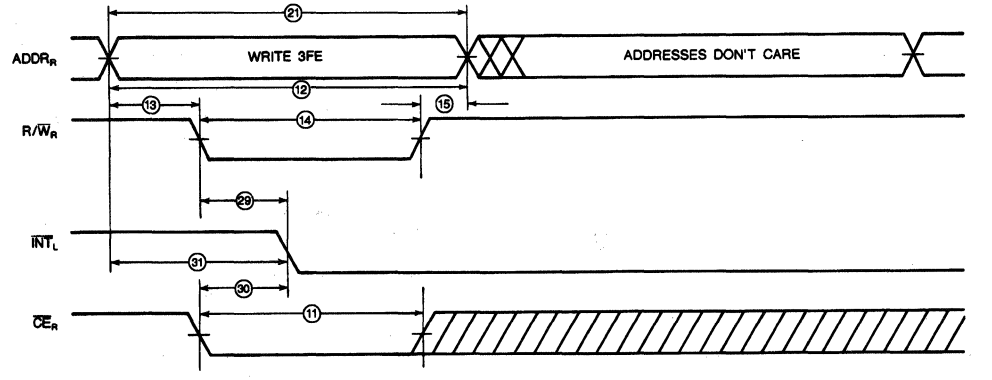
SWITCHING WAVEFORMS (Cont'd.)

INTERRUPT TIMING (1 of 2)
(Set $\overline{INT}$ Flag — Note 11)



WF009486

Left Side Flags Right Side

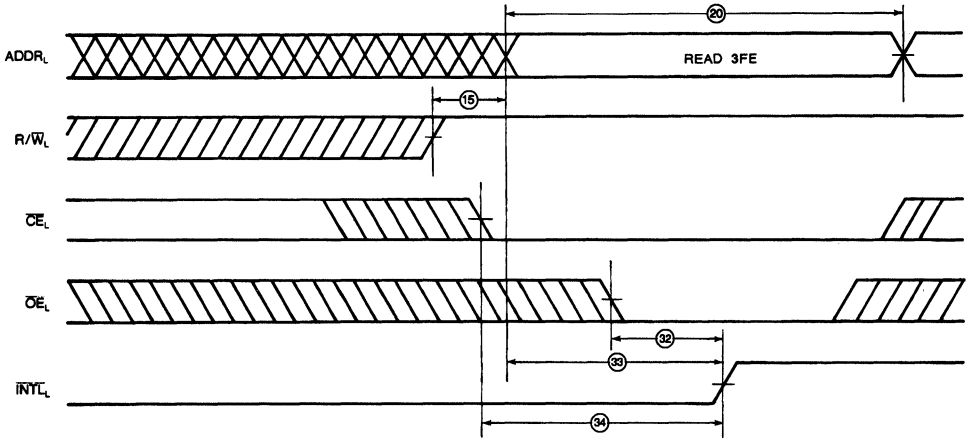


WF009487

Right Side Flags Left Side

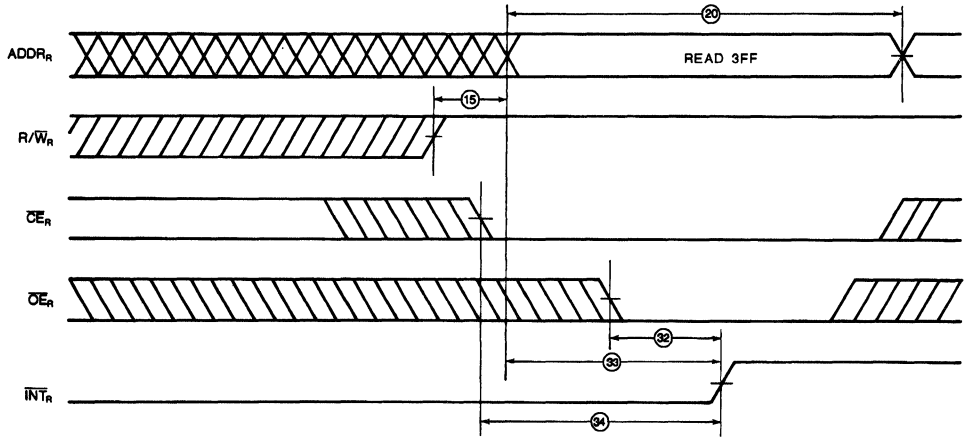
SWITCHING WAVEFORMS (Cont'd.)

INTERRUPT TIMING (2 of 2)
(Clear $\overline{INT}$ Flag)



WF009489

Left Side Clears $\overline{INT}_L$



WF009488

Right Side Clears $\overline{INT}_R$

Notes*

1. R/$\overline{W}$ is HIGH for Read Cycles.
2. Device is continuously enabled, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$.
3. Addresses valid prior to or coincident with $\overline{CE}$ transition LOW.
4. If $\overline{CE}$ and R/$\overline{W}$ go HIGH simultaneously, the outputs remain in the high-impedance state.
5. Output transition is measured at ±500 mV from the low- or high- impedance voltage levels using Load A.
6. $\overline{CE}_L = \overline{CE}_R = V_{IL}$.
7. The $\overline{BUSY}$ and $\overline{INT}$ outputs are open drain. A pull-up resistor is required for system operation. For measurement purposes, Load C is used for HIGH-to-LOW transitions; output reference level is 1.5 V. Load D is used for LOW-to-HIGH transitions; output reference level is +500 mV from the output LOW voltage level.
8. For test and correlation purposes, temperature is defined as stabilized case temperature.
9. This parameter is guaranteed by design but is not 100% tested.
10. Except where indicated, I/O pins use Load B.
11. For a given port to Set or Clear an Interrupt Flag, 1) that port must have priority if addresses match and both $\overline{CE}_L = \overline{CE}_R$ = LOW; or 2) Addresses do not match.
12. If the last input valid transition, which would ordinarily cause a match, occurs at the same time that the opposite port address or $\overline{CE}$ changes to a no-match condition, then $\overline{BUSY}$ will remain HIGH (i.e., if there is never a match, then $\overline{BUSY}$ remains HIGH).
13. For Slave Am2140 only.
14. For Master Am2130 only.

* Notes listed correspond to reference made in the following sections:
- Operating Ranges
- DC Characteristics table
- Switching Characteristics table
- Switching Waveforms

Am99C10

256 x 48 Content Addressable Memory (CAM)

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- Fast-compare time — 70 ns data to match output
- Maskable-bits and maskable-words
- Word-parallel search
- Multiple-match capabilities
- On-chip address decoder
- Time-multiplexed data input
- TTL-compatible inputs and outputs
- Low power dissipation via CMOS

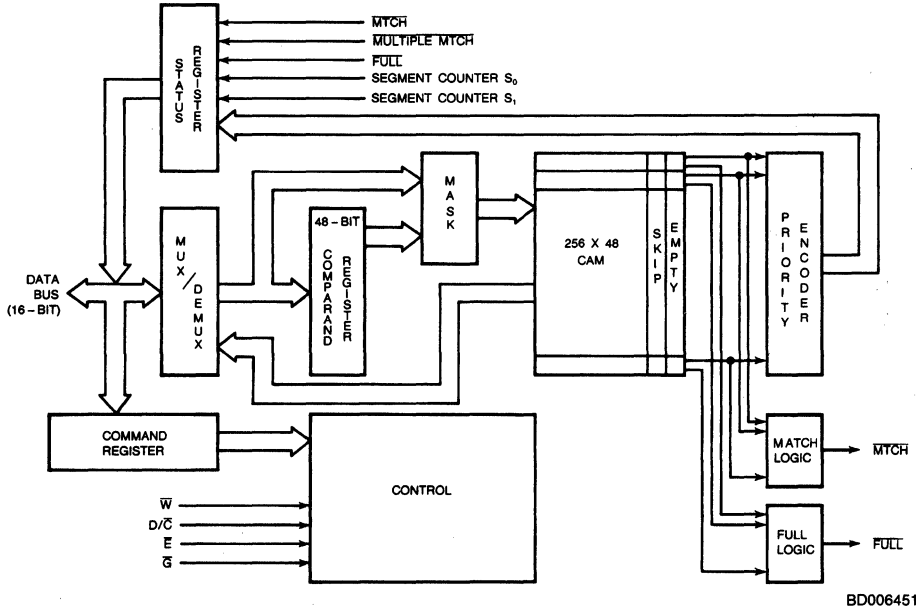
GENERAL DESCRIPTION

The Am99C10 is a high-speed Content Addressable Memory (CAM) with a capacity of 256 words of 48 bits each. The 256 x 48 organization is ideal in Ethernet network applications where it can function as an address filter and perform the network address look-up function in bridges. It can also find use in database machines, temporary storage, decoding, and scratch pad memory applications. Unlike standard memories that associate data with an address, the CAM associates an address with data. The data (comparand) is presented to the CAM which performs simultaneous compare operations on all data (256 words). When the comparand and a word in the CAM are matched, the on-chip priority encoder generates a match word address identifying the location of the data in the CAM. If multiple matches occur, the encoder generates the lowest matched address.

The Am99C10 features a 16-bit bidirectional data bus and three control signals: $\overline{W}$, $\overline{G}$ and $\overline{E}$. $\overline{W}$ controls the writing of the internal registers, latches, and the CAM. $\overline{G}$ controls the reading of the output data and status, while $\overline{E}$ controls the selection/deselection of the device.

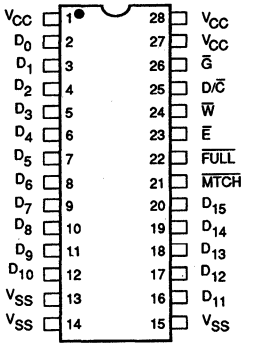
The Am99C10 CAM is manufactured with state-of-the-art CMOS processing techniques. It is assembled in a 28-pin, 400-mil wide DIP.

BLOCK DIAGRAM



Publication # 08125 Rev. B Amendment /0
Issue Date: June 1988

CONNECTION DIAGRAM
Top View



08125B-001A

CD011420

Note: Pin 1 is marked for orientation.

PIN DESCRIPTION

D/$\overline{C}$ Data/Command Mode Selection (Input, TTL, Active HIGH)
A LOW on this input selects the command mode. A HIGH on this input selects the data mode.

$\overline{W}$ Write Enable (Input, TTL, Active LOW)
This pin controls the writing of the internal registers and latches. New data may be written into a register by forcing the appropriate state of D/$\overline{C}$, $\overline{E}$ and $\overline{W}$.

$\overline{G}$ Output Enable (Input, TTL, Active LOW)
This pin controls the reading of the output data and status register. The status register can be accessed by forcing the appropriate state of D/$\overline{C}$ and pulling $\overline{G}$ LOW. $D_0 - D_{15}$ is in the high-impedance state when $\overline{G}$ is pulled HIGH.

$\overline{E}$ Chip Enable (Input, TTL, Active LOW)
A LOW on this input enables chip operations as specified by the state of D/$\overline{C}$, $\overline{W}$, $\overline{G}$ and the command word.

$D_0 - D_{15}$ Data Bus (Bidirectional, Three-State)
The 16-bit bidirectional data bus performs data transfers. The data bus is in a high-impedance state when $\overline{G}$ is HIGH and/or $\overline{E}$ is HIGH.

$\overline{FULL}$ Address Full (Output, TTL, Active LOW)
A LOW on this output indicates that all the words in the 256 address locations in CAM are used. A HIGH on this output indicates that certain locations are still available for storage or that the $\overline{FULL}$ output is disabled. The $\overline{FULL}$ output is in the logic HIGH state when $\overline{E}$ is HIGH.

$\overline{MTCH}$ Match (Output, TTL, Active LOW)
A LOW on this output indicates that the data present in the comparand register and word(s) already stored in the CAM are matched. A HIGH on this output indicates that a mismatch has taken place or the match output is disabled. The match output is in the logic HIGH state when $\overline{E}$ is HIGH.

V_{CC} Power Supply (Input) +5 V

V_{SS} Power Supply (Input) Ground

FUNCTIONAL DESCRIPTION

The following functional description briefly describes the Am99C10 Block Diagram as well as the architecture of the device.

Organized 256 x 48, the Am99C10 has an internal 16-bit bidirectional data bus, while the internal data bus is organized 48 bits wide. The demultiplexer and Comparand Register assemble 48-bit wide data from the external 16-bit data. The Segment Counter controls the multiplexer/demultiplexer operations. The Comparand Register is organized as three 16-bit registers. The source of data to the Comparand Register is selected from the CAM, Mask Register, or I/O. The Segment Counter output is used to select a 16-bit field in the 48-bit bus. The Mask Register is 48 bits wide and is loaded from the Comparand Register by issuing a "move" command. The command latch holds a 16-bit command word, providing global control of the Am99C10.

The state information memory indicates the state of the 48-bit word in the CAM and is organized 256 words by 2 bits. Each 48-bit word has a skip-bit and an empty-bit associated with it. The skip-bit enables/disables a word in the CAM in situations where there are multiple matches. The priority encoder generates the lowest match address when multiple matches occur. The skip-bit gives the user the ability to detect other matched addresses. The match address is accessed by reading the status register. The empty-bit indicates available or empty addresses in the CAM into which data can be written. If multiple empty addresses exist, the priority encoder generates the lowest empty address. The empty address is accessed by reading the status register.

Advanced
Micro
Devices

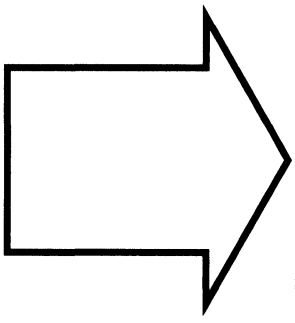


TABLE OF CONTENTS

Military Datasheets

Military Specialty Memory

Whatever your military data buffering needs, Advanced Micro Devices has the right specialty memory device to fit your application. All of our military bipolar and CMOS First-in First-out (FIFO) memories are fully screened to MIL-STD-883.

Bipolar Military FIFOs

The 57401 and 57402 standard bipolar FIFOs feature 64 words by 4-bit and 64 words by 5-bit architectures. Words can be asynchronously loaded and unloaded from these FIFOs at 7 MHz. Standard FIFOs are offered in enhanced 10 MHz versions, the 57401A and 57402A. Both standard and enhanced FIFOs are available as standalone and cascadable devices. Cascadable FIFOs are expandable in word width and depth. AMD's bipolar process has been proven to be radiation-tolerant at neutron fluences up to $1x10^{13}$ neutrons/cm^2. The process has also shown typical recovery times of 50 to 70 µs from a 1 µs pulse at a dose rate of $2x10^{10}$ RADs (Si)/s.

Low Power FIFOs

For applications requiring a shift-in speed of 12 MHz with more modest power requirements, the military low-power standalone FIFOs are an ideal solution. The 57L401D, 57L402D, and 57L4013D consume only 120 mA maximum and are available in 64x4 and 64x5 configurations. The 57L4013 also features three-state outputs, which ease board testing and are excellent for applications where the FIFO is driving a bus.

High Performance FIFO

The 57413A is AMD's fastest military FIFO. It offers a full 25 MHz shift-in/shift-out rate, for performance-critical applications. Other features include three-state outputs and status flags. Two flags, Half-Empty and Almost Empty/Full alert the system when the FIFO is half full (32 words or more), almost empty (8 words or less), or almost full (56 or more words).

CMOS FIFO Family

AMD's family of zero-power CMOS FIFOs will offer the ultimate in speed and low power. All five new devices are fully cascadable for easy expansion in word width and depth. They feature asynchronous shift-in/shift-out rates of 12 MHz with extremely low power consumption. When in standby (quiescent) mode, these devices consume only 550 µwatts of power. The active power dissipation is equally impressive. At maximum frequency (12MHz) military CMOS FIFOs require only 40 mA.

The CMOS FIFOs employ a static RAM-based memory array which allows them to operate with an extremely short fall-through time. Designers with high speed requirements will not have to wait for the ripple-through delay associated with register-based FIFOs. In addition, AMD's CMOS FIFOs offer fully-TTL compatible inputs and outputs.

The 57C401 and 57C402 are organized like the standard 64x4 and 64x5 FIFOs, but add enhanced speed and reduced power. These parts are designed for applications in systems where higher speed and zero power is a requirement.

The 57C4013 and 57C4023 resemble the 'C401 and 'C402 but also offer three-state outputs. The ability to turn off the FIFO outputs is useful in testing and in on-board bus applications.

The 57C4033 is a unique 64x5 device which offers status flags in addition to three-state outputs. The two flags, Half-Empty and Almost Empty/Full operate in the same manner as on the 57413A.

AMD will soon offer a line of high density CMOS FIFOs: the 57C4500 (256x9), 57C4501 (512x9), and 57C4502 (1Kx9) buffer memories. These devices feature static-RAM-based architectures specially tailored for applications requiring increased depth. They feature a 50 ns access time and 20 mA standby power. Our high density FIFOs are fabricated on AMD's proprietary poly-load CMOS process.

Uses of FIFOs

AMD's military FIFOs are a simple, economical way of matching the instantaneous data rates of two digital systems. Examples are dual microprocessor systems where the FIFO keeps transmitting microprocessor "free" by storing the data for the second processor in advance. The first processor is able to load the data as a block and continue with other tasks, and the second can receive the data from the FIFO as it is required. A similar situation might occur in a display system where a general-purpose microprocessor sends data to a specialized graphics processor.

In many aircraft, a central computer supervises several distributed microprocessors which, in turn, control subsystems such as weapons, targeting, radar, and displays. The use of FIFOs as serial data buffers to these subsystem microprocessors allows the central processor to prepare and send data quickly, freeing it to move on to the next task.

FIFO IC Selector Guide (MIL)

Low Density FIFOs

Technology	Part Number	Organization	Type	Max Data Rate, MHz	Max I_{CC}, mA	Package Type	Pin Count	Features
B	C57401	64x4	C	7	160	J, L	16, 20 (LCC)	TPO
B	57401	64x4	S	7	160	J, L	16, 20 (LCC)	TPO
B	C57401A	64x4	C	10	180	J, L	16, 20 (LCC)	TPO
B	57401A	64x4	S	10	180	J, L	16, 20 (LCC)	TPO
B	57L401D	64x4	S	12	120	J	16	TPO Low Power I_{OL} = 12 MA
B	57L4013D	64x4	S	12	120	J	16	TSO Low Power I_{OL} = 12 MA
B	C57402	64x5	C	7	180	J, L	18, 20 (LCC)	TPO
B	57402	64x5	S	7	180	J, L	18, 20 (LCC)	TPO
B	C57402A	64x5	C	10	200	J	18	TPO
B	57402A	64x5	S	10	200	J	18	TPO
B	57L402D	64x5	S	12	120	J	18	TPO Low Power I_{OL} = 12 MA
C	57C401-12	64x4	C	12	40	J	16	TPO Low Power, RAM Based
C	57C4013-12	64x4	C	12	40	J	16	TSO Low Power, RAM Based
C	57C402-12	64x5	C	12	40	J	18	TPO Low Power, RAM Based
C	57C4023-12	64x5	C	12	40	J	18	TSO Low Power, RAM Based
C	57C4033-12	64x5	C	12	40	J	20	TSO Low Power, RAM Based, Status Flags
B	57413A	64x5	S	25	240	J	20	TSO, Status Flags

3

High Density FIFOs

Technology	Part Number	Organization	Type	Max Data Rate, MHz	Max I_{CC}, mA	Package Type	Pin Count	Features
C	57C4500-80	256x9	C	10	80	J	28	TSO Access Time = 80 ns, Status Flags
C	57C4500-65	265x9	C	12	80	J	28	TSO Access Time = 65 ns, Status Flags
C	57C4500-50	265x9	C	15	80	J	28	TSO Access Time = 50 ns, Status Flags
C	57C4500-40	265x9	C	20	80	J	28	TSO Access Time = 40 ns, Status Flags
C	57C4501-80	512x9	C	10	80	J	28	TSO Access Time = 80 ns, Status Flags
C	57C4501-65	512x9	C	12	80	J	28	TSO Access Time = 65 ns, Status Flags
C	57C4501-50	512x9	C	15	80	J	28	TSO Access Time = 50 ns, Status Flags
C	57C4501-40	512x9	C	20	80	J	28	TSO Access Time = 40 ns, Status Flags
C	57C4502-80	1Kx9	C	10	80	J	28	TSO Access Time = 80 ns, Status Flags
C	57C4502-65	1Kx9	C	12	80	J	28	TSO Access Time = 65 ns, Status Flags
C	57C4502-50	1Kx9	C	15	80	J	28	TSO Access Time = 50 ns, Status Flags
C	57C4502-40	1Kx9	C	20	80	J	28	TSO Access Time = 40 ns, Status Flags

Notes:

Technology:
B – Bipolar
C – CMOS

C – Cascadable
S – Standalone

PackageType:
N – Plastic
J – Ceramic
NL – PLCC
L – Leadless Chip Carrier

Features:
TSO – Three State Output
TPO – Totem Pole Output

JAN 38510 and Standard Military Drawing Program

AMD is an active participant in the JAN 38510 and Standard Military Drawing (SMD) Program. The idea behind the SMD Program is to standardize MIL-STD-883, Class B microcircuits where fully qualified JAN product is not available. The advantage to the user is that SMDs are a cost effective alternative to source control drawings and are offered as off-the-shelf stocking items by IC manufacturers participating in the program.

Standard Military Drawings should always be considered to improve availability over source control drawings. It is standard practice at AMD to convert our 883, Class B processing to SMDs for all products which we are approved to supply. AMD then dual marks these devices with both the SMD number and the Generic Part Number. DESC approved products can then be procured to either part number as standard product through both OEM and Distributor channels.

The following cross reference will allow you to determine the appropriate SMD and JAN Drawing for each FIFO device. AMD will continue to work closely withe DESC, generating new drawings, which will provide a steady flow of advanced technology products to standardized specifications.

MIL-M-38510 Slash Sheet Cross Reference for AMD Generic Part Number

M38510	01	02	03	04	05	06	07	08	09	10
503	10H8	12H6	14H4			10L8	12L6	14L4		
504	16L8A	16R8A	16R6A	16R4A			16L8A-2	16R8A-2	16R8A-2	16R4A-2
505	20L8A	20R8A	20R6A	20R4A						

Standard Military Drawing Generic Part Type Cross Reference

STANDARD MILITARY PART NUMBER	GENERIC PART NUMBER	JAN REPLACEMENT NUMBER
5962-8779101EX	57401J/883B	—
5962-87791012X	57401L/883B	—
5962-8779102VX	57402J/883B	—
5962-87791022X	57402L/883B	—
5962-8779103EX	57401AJ/883B	—
5962-87791032X	57401AL/883B	—
5962-8779104VX	57402AJ/883B	—
5962-87791042X	57402AL/883B	—
5962-8779105EX	C57401J/883B	—
5962-87791052X	C57401L/883B	—
5962-8779106VX	C57402J/883B	—
5962-87791062X	C57402L/883B	—
5962-8779107EX	C57401AJ/883B	—
5962-87791072X	C57401AL/883B	—
5962-8779108VX	C57402AJ/883B	—
5962-87791082X	C57402AL/883B	—
5962-8779109EX	57L401DJ/883B	—
5962-8779110VX	57L402DJ/883B	—
5962-8779111EX	57L4013DJ/883B	—

MMI PACKAGE DESIGNATOR	PACKAGE TYPE	STANDARD LEAD FINISH	MIL-SPEC LEAD FINISH DESIGNATOR
J/JS	CERAMIC DIP	SOLDER DIP	A
W	CERAMIC FLATPACK	SOLDER DIP	A
L	CERAMIC LEADLESS CHIP CARRIER	SOLDER DIP	A

Product Introduction Procedures

All new products released by the Military Products Division must successfully pass Mil-Std-883 Class B processing prior to new product announcement. This practice allows us to do checkout of bonding diagrams, electrical test tapes and burn circuits in a manufacturing environment. Programmability is checked when applicable. Our Military Engineering Department reviews electrical data to insure performance and yields to military data sheet limits are acceptable, prior to new product release. This procedure allows MPD to keep manufacturing start-up problems to a minimum on new product orders.

Standard Processing Flows

Monolithic Memories Processing and Screening flows are organized to provide a broad selection of processing options, structured around the most commonly requested customer flows.

Standard processing flows for the Military Products Division include:

Monolithic Memories Inc. Modified Level S
JAN 38510 Class B
Military Drawing Program
Mil-Std-883 Class B
Monolithic Memories Inc. Mil-Temp Product

In addition, these flows are expanded to provide for factory programming on PAL circuits, when required by our customers.

Major benefits can be realized by ordering product to standard flows whenever possible:

- Minimize need for source control drawings.
- Cost savings on unit cost—no price adders for custom processing.
- Improved lead time—no spec review or negotiation time, plus the ability to pull product from various work-in-process stages or purchase product from finished goods inventory.

For your reference, we have included our Modified Level S flow, our Mil-Std-883 Class B flow and our Mil-Temp Product flow. For your planning purposes, we have calculated typical throughput times for each operation, as product proceeds through the processing flow.

It is the policy of Monolithic Memories, to always operate to the most current revision of Mil-M-38510 and Mil-Std-883.

Manufacturing and Screening Locations

JAN Products, Monolithic Memories Modified Level "S", and customer orders which call for U.S.A. assembly, are manufactured in our DESC certified line in Sunnyvale, California.

MIL-STD-883 Class B products, and orders to source control drawings, where stateside build is not required, are assembled at our Penang, Malaysia facility. This facility is qualified by Monolithic Memories Quality Department, as well as by many of our customers, to manufacture MIL-STD-883 Class B product. Conformance to MIL-STD-883 requirements is routinely monitored through audits at the Penang facility as well as incoming inspections in Sunnyvale. Manufacturing capabilities for each Monolithic Memories facility are highlighted on the chart below.

To identify the assembly location of each military device, the Country of origin is marked on all products prior to shipment. Products assembled in our stateside facility in Sunnyvale, California, will have "USA" marked on the topside of the device. The exception to this is JAN 38510 product, which is marked to the MIL-M-38510 requirements only.

Offshore built product, which is manufactured in Penang, Malaysia, will have "Malaysia" or "Malay" marked on the bottom side of the device.

Manufacturing Capabilities

	SUNNYVALE	PENANG
Assembly	X	X
Precap Inspection	X	X
Environmental Testing	X	X
Electrical Pre-Test	X	X
Burn-In	X	X
Post Burn-In Electricals	X	X
Group A Testing	X	X
Mark	X	X
Factory Programming	X	
Qualification and Quality Conformance Testing	X	

Standard Military Flow Chart

SCREENING	MODIFIED LEVEL S	REQUIREMENT	CLASS B	REQUIREMENT
	MIL-STD-883 METHOD 5004		MIL-STD-883 METHOD 5004	
S.E.M.	2018	Sample		
Assembly	USAAssembly		Typically offshore assembly	
Non-destruct bond pull	2023(Sample)	LTPD = 5 REJ = 0 SS = 2 all wires		
Die shear/ Destruct bond pull	2019 (sample)	SS = 2 REJ = 0		
Internal visual	2010 cond. A (modified)	100%	2010 cond. B	100%
Stabilization bake	1008	100%	1008	100%
Temperature cycling	1010	100%	1010	100%
Constant acceleration	2001 test cond. D or E Y1 orientation only	100%	2001 test cond. D or E Y1 orientation only	100%
Seal A) Fine B) Gross			1014 cond. A or B cond. C	100%
Particle impact noise detection (PIND)	2020 cond. A only	100%		
Interim electrical parameters	Per application device specification TA = 25°C only	100%		
Serialization		100%		
X-Ray	2010 two views X and Y axis only	100%		
Interim electrical (1) parameter	Per applicable device specification TA = 25°C only	100%	Per applicable device (1) specification TA = 25°C only	100%
Post electrical parameters	Per applicable device specification TA = 25°C only (delta's when required)	100%	Per applicable device specification TA = 25°C only	100%
Delta calculations (when applicable)	Per applicable device specification			
Percent defect allowable	DC Parameters PDA = 5% or 1 device whichever is greater Functional Parameters PDA = 3% or 1 device whichever is greater		DC Parameters PDA = 5% or 1 device whichever is greater	

(1) Programming and verification are performed at 25°C only.
(2) Unprogrammable PAL Devices–AC parameters are tested on programmed sample.

Standard Military Flow Chart (Cont'd.)

SCREENING	MODIFIED LEVEL S	REQUIREMENT	CLASS B	REQUIREMENT
	MIL-STD-883 METHOD 5004		MIL-STD-883 METHOD 5004	
Final electrical parameters (hot and cold extremes)	Per applicable device specification	100%	Per applicable device specification	100%
Sal A) Fine B) Gross	1014 cond, A or B cond C	100%		
Group A lot	5005 Level S. (2)	Per applicable device specification	5005 Class B (2)	Sample every lot
Group B inspection lot Group C Group D Exrternal visual	5005 level S not applicable 5005 level S 2009	As required As required 100%	5005 Class B 5005 Class B 5005 Class B 2009 Generic data available in lieu of lot quality conformance inspection	Every 6 weeks Every 13 weeks Every 26 weeks 100%

(1) Programming and verification are performed at 25°C only.
(2) Unprogrammable PAL Devices–AC parameters are tested on programmed sample.

Quality Programs

The Military Product Division quality system conforms to the following Mil-Standards:

Mil-M-38510, Appendix A, "Product Assurance Program"
Mil-Q-9858, "Quality Program Requirements"
Mil-I-45208, "Inspection System Requirements"

Monolithic Memories facilities in Sunnyvale are certified by the Defense Electronics Supply Center (DESC), to manufacture and qualify Schottky Bipolar PROMs and PAL circuits in accordance with Mil-M-38510 Class B. This certification was a result of a successful audit of our production and quality systems to the stringent requirements of Mil-M-38510. Monolithic Memories has also demonstrated compliance to the strict requirements of both controlled and captive lines connected with special Military programs.

Quality Assurance

Following 100% screening, the Military Products Division samples all products processed in conformance to Mil-Std-883 Class B, to the following LTPD levels:

Test	LTPD
DC 25°C	2
DC+125°C	3
DC-55°	5
Functional at 25°C	2
Functional at Temperature Extremes	5
AC 25°C	2
AC +125°C	3
AC –55°	5

The Military Products Division ensures outgoing product quality and integrity by performing inspection Lot Group A's and B's per Mil-Std-883 Method 5005, conducting self audits in all areas involved in screening tests per Method 5004 of MIL-STD-883, gating all shipments to our customers, and maintaining a calibration control system in accordance with Mil-Std-45662.

For products requiring programming prior to AC tests, testing is performed utilizing MIL-M-38510 slash sheet sample plans.

Product Qualification/Quality Conformance Inspection (QCI)

The Military Products Division has a quality conformance testing program in accordance with MIL-STD-883, Method 5005. Quality Conformance Testing provides necessary feedback and monitors several areas:

- Reliability of Product/Processes
- Vendor Qualification for Raw Materials
- Customer Quality Requirements
- Maintain Product Qualification
- Engineering Monitor on Products/Processes

Standard procedures for new product release specify that Monolithic Memories' Reliability Department, as a minimum, conduct qualification testing per Mil-Std-883, Method 5005. Once qualified, each package type (from each assembly line) and device (by technology group as delineated in Mil-M-38510) are incorporated into Monolithic Memories Quality Conformance Inspection program which utilizes the requirements of MIL-M-38510.

When military programs do not require that QCI data be run on the specific lot shipped Monolithic Memories Quality Conformance program allows customers to obtain generic data on all product families manufactured by the Military Products Division. Generic Qualification Data enables customers to eliminate costly qualification and destruct unit charges, and also improves delivery time by a factor of eight to ten weeks. The following product data is available:

Group B - Package Related Tests

- QCI is performed every 6 weeks of manufacture on each package type.
- Any device type in the same package type may be used regardless of the specific part number.
- Purpose: To monitor assembly and device package integrity.

Group C - Product/Process Related Tests

- QCI is performed every 13 weeks of manufacture, on representative devices from the same microcircuit group.
- Life test data may be used to qualify similar technologies.
- Purpose: To monitor the reliability of the process and the parametric performance for each product technology.

Group D - In-Depth Package Related Tests

- QCI is conducted every 26 weeks using devices which represent the same package construction and lead finish.
- Any device type in the same package type may be used regardless of the specific part number.
- Purpose: To monitor the reliability and integrity of various package materials and assembly processes.

Generic Data

Monolithic Memories' Generic Data Program is based on MIL-M-38510, which allows for shipments based on 26 weeks of coverage for Group C Testing and 36 weeks of coverage for Group D Testing.

Should circumstances arise where generic coverage to MIL-M-38510 is not possible, MMI reserves the right to ship product based on 52 weeks of generic Group C and/or D coverage per MIL-Std-883.

Process Audits

Process Audits are performed in accordance with Mil-M-38510, Appendix A, (self audits) by the Quality Assurance Department.

Customer Material Returns

In order to better service our military customers who must return product to the factory, the Military Products Division has established its own customer material returns department. Our goals and policies are outlined below so you may know what to expect when returning product to M.P.D.

Goals

10 day turn-around to respond to a return.

- Notification to the customer of any discrepancy relating to the return.
- For returns which cannot be validated, a written notice of M.P.D.'s intent to return product will be sent to our customer.
- Product returned to our customer will be accompanied by an explanation and/or parametric test data and serialized devices.

Standard Policies

- Product which is returned specifically as electrical failures and is not accompanied by test data, will be tested at all three temperatures (–55°C, 25°C, +125°C)
- If no failures found, the product will be returned to the customer.
- A device count is done upon arrival of a return at Monolithic Memories. Credit will be given only for the number of devices received by the factory.
- Product returned by the Franchised Distributor for rescreen or stock rotation will be accepted only if proper traceability paperwork accompanies each lot of product
- All returns must be sent to 3625 Peterson Way, Santa Clara, CA 95051. ATTN: "MPD CMR DEPARTMENT"

Information Checklist

The following accompanying a material return will assist us in responding to your return in the shortest possible time.

1. Double check accuracy of device counts.
2. Identify rejects from good devices, when returned together.
3. Supply as much detail as you can about the description of the electrical failure mode (i.e.: AC Fail, DC Fail, FCT Fail, or description of any test numbers used).
4. Whenever possible, identify dissimilar failures or keep separate devices which fail different parameters by serializing failures.
5. Enclose a copy of any data which you may have taken on the failed devices (i.e.: Forcing conditions, temperature tested, parameter and value, an address that failed). List what was expected vs. what was received.
6. For programmability failures, please send programming masters or a truth table. Also please indicate whether single or multiple pulse programming was used and the equipment device was programmed on.
7. What environmental testing was performed.
8. Failure rates.

Although our intent is that our customers will never have to use these guidelines, if a problem should arise, the Military Products Division will strive to disposition and respond to your material return as thoroughly and promptly as possible.

Electrostatic Discharge Control Procedures

The Military Products Division of Monolithic Memories fully employs static control procedures throughout its facilities in Penang, Malaysia and Sunnyvale, California.

All manufacturing areas where product is processed or handled, including our Reliability Labs, Engineering Labs, etc., have full static control such as wrist straps, antistatic smocks, grounded stainless steel tables, conductive mats and ion generators wherever necessary.

All product is moved throughout our facilities and shipped to customers in static shielded containers.

In addition, MPD distributors must demonstrate that they meet the same stringent standards regarding ESD handling and control procedures as the factory. Individual distributor locations are audited and approved annually by MPD's Quality Assurance Department.

An ESD identifier is marked on all products in front of the date code, and all shipping containers are labeled with an ESD Caution Message. ESD procedures are continually reviewed, to ensure that our customers receive only the highest quality product from the Military Products Division.

Radiation Hardness Program

1. Radiation Effects

It has been stated that some level of radiation tolerance will be required in up to 50% of all military applications by 1990. Due to this increased concern over radiation effects on integrated circuits, the Military Products Division has embarked on a program to determine what radiation dose rates our circuits will withstand.

2. Neutron Irradiation

We have successfully completed neutron radiation testing on our Bipolar processes in accordance with Mil-Std-883, Method 1017.2. Eleven different device types, which currently represent all our Bipolar processes, were parametrically and functionally tested at 25°C before and after exposure to fluence levels of $2x10^{12}$ N/cm², $1x10^{13}$ N/cm², $4x10^{13}$ N/cm² and $1x10^{14}$ N/cm². Input low current (IIL) is the primary measurement of permanent circuit degradation. The parametric failures (IIL > 250mA) seen occurred at relatively high fluence levels. Also, no major changes in ICC were noted for any circuit.

The following is a list of the device types tested:

53S1681	(2048x8 PROM)
53RA1681A	(2048x8 Registered PROM)
53S3281	(4096x8 PROM)
57401A	(64x4 FIFO)
PAL16R4A	(High Speed Programmable Array Logic)
PAL16R4B	(Very High Speed Programmable Array Logic)
PAL16R4D	(Oxide Isolated Ultra High Speed Programmable Array Logic)
PAL20R4A	(High Speed Programmable Array Logic)
PAL20RA10	(Asynchronous Programmable Array Logic)

All devices passed test limits at $1x10^{13}$ N/cm² level, with the 53RA1681A, 53S3281, and 57401A also passing the $4x10^{13}$ N/cm² fluence level. In addition, the 57401A passed test limits at $1x10^{14}$ N/cm² level.

3. Dose Rate Effects

Dose rate data has been obtained on our junction isolated Bipolar processes. All recovered in 50 to 70 microseconds from a 1 microsecond pulse of $2x10^{10}$ rads (Si) per second.

The products tested were:

PAL14L8	PAL10L8
PAL16L6	PAL12L6
PAL20L10	PAL16L8
PAL20X10	PAL16R8
PAL20X8	PAL16R6
PAL12H6	PAL16R4
PAL14H4	

4. Future Radiation Testing

Our future test plans include:

- Total Dose
- Single Event Upset
- Latch-up and Burn-out

Monolithic Memories' new Bipolar and CMOS processes will be radiation tested after production release.

Detailed neutron and dose rate radiation data is available from the Military Products Division.

JAN 38510 and STANDARD MILITARY DRAWING PROGRAM

STANDARD MILITARY DRAWING NUMBERING SYSTEM

81035 01 L A

DRAWING NUMBER FOR PRODUCT FAMILY
- 81035 = Small 20 Pin PAL Devices
- 81036 = Med. 20 Pin A, A-2 PAL Devices
- 84129 = 24 Pin A, XA, A-2 PAL Devices
- 85065 = Medium 20 Pin A-4 PAL Devices
- 5962-85155 = Medium 20 Pin, B, B-2 and D PAL Devices
- *** 5962-86803 = 24 RA Pin PAL Devices
- *** 5962-86804 = Small 24 Pin PAL Devices
- *** 5962-87671 = 24 Pin B PAL Devices

DEVICE TYPES

LEAD FINISH
- A = Hot Solder Dip
- X = Any Lead Finish

PACKAGE TYPES
- K = 24 Lead 3/8" x 5/8" Cerpack
- L = 24 Lead 1/4" x 1 1/4" SKINNYDIP
- R = 20 Lead 1/4" x 1 1/16" DIP
- S = 20 Lead 1/4" x 1/2" Cerpack
- 2 = 20 Terminal .350 x .350 LCC
- 3 = 28 Terminal .450 x .450 LCC

*** SMDs Being Generated

JAN PART NUMBERING SYSTEM

JM 38510 / 503 01 B R A

JAN DESIGNATOR
Part cannot be marked with a "J" unless qualified and approved for listing on QPL.

GENERAL PROCUREMENT

REFERS TO DETAILED SPEC
- 503 = Programmable Array Logic
- 504 = Programmable Array Logic
- 505 = Programmable Array Logic

DEFINES DEVICE TYPES

LEAD FINISH
- A = Hot Solder Dip
- X = Any Lead Finish

PACKAGE TYPES
- R = 20-Lead 1/4" x 1 1/16" DIP
- L = 24-Lead 1/4" x 1 1/4" SKINNYDIP
- 2 = 20-Terminal 0.35 x 0.35 LCC
- 3 = 28-Terminal 0.450 x 0.450 LCC

PROCESSING LEVEL
Class B

PART NUMBER INTERPRETATION:
When ordering to JAN 38510 and Military Drawing numbers, the lead finish designator (last letter in part number) is commonly called out as "X". This is a way of stating that the customer will accept the standard manufacturer's lead finish for the package orders. "X" is not a lead finish designator in itself, therefore, when product is shipped, the actual lead finish designator will be marked on the devices.

Military Standard FIFOs 64x4 64x5 Cascadable & Standalone Memory

C57401 C57401A C57402 C57402A
57401 57401A 57402 57402A

Features/Benefits

- **Choice of 7 or 10 MHz shift-out/shift-in rates**
- **Choice of standalone or cascadable devices**
- **Choice of 4-bit or 5-bit data width**
- **TTL inputs and outputs**
- **Cascadable devices readily expandable in the word and bit dimensions.**
- **Standalone devices expandable in the word dimension only**
- **Structured pinouts. Output pins directly opposite corresponding inputs pins**
- **Asynchronous operation**
- **Dose rate (transient upset) junction-isolated bipolar process $2x10^{10}$ RADs (Si)/s recovery time of 50 to 70 μs from a 1 μs pulse**
- **Neutron fluence (permanent damage): $1x10^{13}$ N/cm²**

Description

The C/57401/1A and C57402/2A are "fall through" high-speed First-In First-Out (FIFO) memories organized 64 words by 4 bits and 64 words by 5 bits respectively. FIFO word width and depth are expandable on cascadable devices. Standalone devices are expandable in word width only.

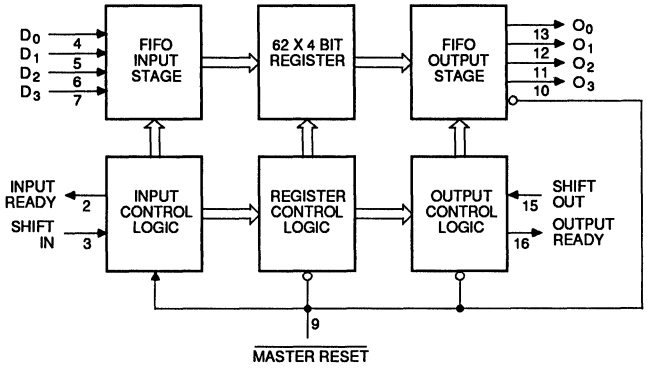
Ordering Information

PART NUMBER	PINS	PACKAGE	PACKAGE TYPE	MIL-M-38510 CASE OUTLINE	CASCADABLE/ STANDALONE	DESCRIPTION
57401	16	J	Ceramic Dip	D-2	Standalone	7 MHz 64X4 FIFO
		L (20)	Leadless Chip Carrier	C-2	Standalone	
57401A	16	J	Ceramic Dip	D-2	Standalone	10 MHz 64X4 FIFO
		L (20)	Leadless Chip Carrier	C-2	Standalone	
57402	18	J	Ceramic Dip	D-2	Standalone	7 MHz 64X5 FIFO
		L (20)	Leadless Chip Carrier	C-2	Standalone	
57402A	18	J	Ceramic Dip	D-2	Standalone	10 MHz 64X5 FIFO
		L (20)	Leadless Chip Carrier	C-2	Standalone	
C57401	16	J	Ceramic Dip	D-2	Cascadable	7 MHz 64X4 FIFO
		L (20)	Leadless Chip Carrier	C-2	Cascadable	
C57401A	16	J	Ceramic Dip	D-2	Cascadable	10 MHz 64X4 FIFO
		L (20)	Leadless Chip Carrier	C-2	Cascadable	
C57402	18	J	Ceramic Dip	D-2	Cascadable	7 MHz 64X5 FIFO
		L (20)	Leadless Chip Carrier	C-2	Cascadable	
C57402A	18	J	Ceramic Dip	D-2	Cascadable	10 MHz 64X5 FIFO
		L (20)	Leadless Chip Carrier	C-2	Cascadable	

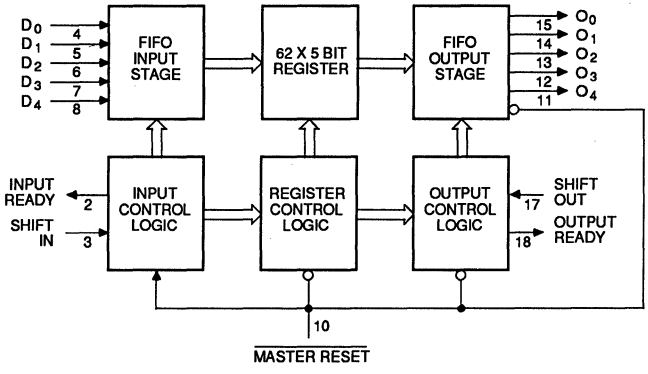
505012

Block Diagrams

57401
57401A
C57401
C57401A



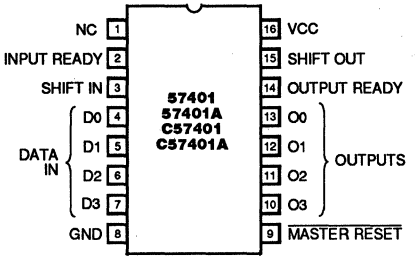
57402
57402A
C57402
C57402A

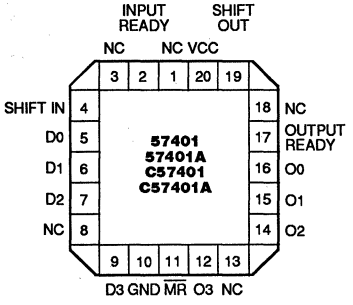


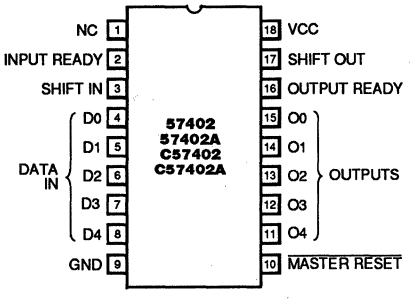
505 127

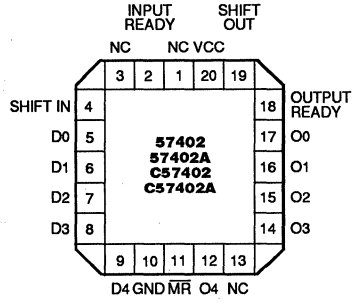
3

Pin Configuration









505 129

Absolute Maximum Ratings*

Supply voltage, V_{CC} ..... –0.5 V to 7 V
Input voltage ..... –1.5 V to 7 V
Off-state output voltage ..... –0.5 V to 5.5 V
Storage temperature ..... –65°C to +150°C

*Note:
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Operating Conditions 57401/2

SYMBOL	PARAMETER	FIGURE	MILITARY MIN		MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
T_A	Operating free-air temperature		–55		*125	°C
t_{SIH}†	Shift in HIGH time	1	45			ns
t_{SIL}	Shift in LOW time	1	45			ns
t_{IDS}	Input data setup	1	10			ns
t_{IDH}	Input data hold time	1	55			ns
t_{SOH}†	Shift Out HIGH time	4	45			ns
t_{SOL}	Shift Out LOW time	4	45			ns
t_{MRW}	Master Reset pulse†	8	30			ns
t_{MRS}**	Master Reset to SI	8	45			ns

* Instant-On Case Temperature.
** t_{MRS} is measured on initial characterization lots only and is not directly tested in production.

505013

Switching Characteristics 57401/2 Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MAX	UNIT
f_{IN}	Shift in rate	1	7		MHz
t_{IRL}†	Shift In to Input Ready LOW	1		60	ns
t_{IRH}†	Shift In to Input Ready HIGH	1		60	ns
f_{OUT}	Shift Out rate	4	7		MHz
t_{ORL}†	Shift Out to Output Ready LOW	4		65	ns
t_{ORH}†	Shift Out to Output Ready HIGH	4		70	ns
t_{ODH}	Output Data Hold (previous word)	4	10		ns
t_{ODS}	Output Data Shift (next word)	4		65	ns
t_{PT}	Data throughput or "fall through"	3, 6		4	µs
t_{MRORL}	Master Reset to OR LOW	8		65	ns
t_{MRIRH}	Master Reset to IR HIGH	8		65	ns
t_{IPH}	Input Ready pulse HIGH	3	20		ns
t_{OPH}	Output Ready pulse HIGH	6	20		ns

† See AC test and high speed application note.

505014

Absolute Maximum Ratings*

Supply voltage, V_{CC} ..... –0.5 V to 7 V
Input voltage ..... –1.5 V to 7 V
Off-state output voltage ..... –0.5 V to 5.5 V
Storage temperature ..... –65°C to +150°C

*Note:
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Operating Conditions 57401A/2A

SYMBOL	PARAMETER	FIGURE	MILITARY MIN		MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
T_A	Operating free-air temperature		–55		*125	°C
t_{SIH}†	Shift in HIGH time	1	35			ns
t_{SIL}	Shift in LOW time	1	35			ns
t_{IDS}	Input data setup	1	5			ns
t_{IDH}	Input data hold time	1	45			ns
t_{SOH}†	Shift Out HIGH time	4	35			ns
t_{SOL}	Shift Out LOW time	4	35			ns
t_{MRW}	Master Reset pulse	8	40			ns
t_{MRS}**	Master Reset to SI	8	45			ns

* Instant-On Case Temperature.
** t_{MRS} is measured on initial characterization lots only and is not directly tested in production.

505015

Switching Characteristics 57401A/2A Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MAX	UNIT
f_{IN}	Shift in rate	1	10		MHz
t_{IRL}†	Shift In to Input Ready LOW	1		50	ns
t_{IRH}†	Shift In to Input Ready HIGH	1		50	ns
f_{OUT}	Shift Out rate	4	10		MHz
t_{ORL}†	Shift Out to Output Ready LOW	4		65	ns
t_{ORH}†	Shift Out to Output Ready HIGH	4		65	ns
t_{ODH}	Output Data Hold (previous word)	4	10		ns
t_{ODS}	Output Data Shift (next word)	4		60	ns
t_{PT}	Data throughput or "fall through"	3, 6		2.2	µs
t_{MRORL}	Master Reset to OR LOW	8		65	ns
t_{MRIRH}	Master Reset to IR HIGH	8		65	ns
t_{IPH}	Input Ready pulse HIGH	3	20		ns
t_{OPH}	Output Ready pulse HIGH	6	20		ns

† See AC Test and high speed application note.

505016

Absolute Maximum Ratings*

Supply voltage, V_{CC} ..... –0.5 V to 7 V
Input voltage ..... –1.5 V to 7 V
Off-state output voltage ..... –0.5 V to 5.5 V
Storage temperature ..... –65°C to +150°C

*Note:
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Operating Conditions C57401/2

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
T_A	Operating free-air temperature		–55	*125	°C
t_{SIH}†	Shift in HIGH time	1	45		ns
t_{SIL}	Shift in LOW time	1	45		ns
t_{IDS}	Input data setup	1	0		ns
t_{IDH}	Input data hold time	1	55		ns
t_{SOH}†	Shift Out HIGH time	4	45		ns
t_{SOL}	Shift Out LOW time	4	45		ns
t_{MRW}	Master Reset pulse	8	30		ns
t_{MRS}**	Master Reset to SI	8	45		ns

* Instant-On Case Temperature.
** t_{MRS} is measured on initial characterization lots only and is not directly tested in production.

505017

Switching Characteristics C57401/2 Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY MAX	UNIT
f_{IN}	Shift in rate	1	7		MHz
t_{IRL}†	Shift In to Input Ready LOW	1		60	ns
t_{IRH}†	Shift In to Input Ready HIGH	1		60	ns
f_{OUT}	Shift Out rate	4	7		MHz
t_{ORL}†	Shift Out to Output Ready LOW	4		65	ns
t_{ORH}†	Shift Out to Output Ready HIGH	4		70	ns
t_{ODH}	Output Data Hold (previous word)	4	10		ns
t_{ODS}	Output Data Shift (next word)	4		65	ns
t_{PT}	Data throughput or "fall through"	3, 6		4	µs
t_{MRORL}	Master Reset to OR LOW	8		65	ns
t_{MRIRH}	Master Reset to IR HIGH	8		65	ns
t_{IPH}*	Input Ready pulse HIGH	3	30		ns
t_{OPH}*	Output Ready pulse HIGH	6	30		ns

† See AC test and high speed application note.
* This parameter applies to FIFOs communicating with each other in a cascaded mode.

505018

Absolute Maximum Ratings

Supply voltage, V_{CC} ..... –0.5 V to 7 V
Input voltage ..... –1.5 V to 7 V
Off-state output voltage ..... –0.5 V to 5.5 V
Storage Temperature ..... –65°C to +150°C

*Note:
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Operating Conditions C57401A/2A

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
T_A	Operating free-air temperature		–55	*125	°C
t_{SIH}†	Shift in HIGH time	1	35		ns
t_{SIL}	Shift in LOW time	1	35		ns
t_{IDS}	Input data setup	1	0		ns
t_{IDH}	Input data hold time	1	45		ns
t_{SOH}†	Shift Out HIGH time	4	35		ns
t_{SOL}	Shift Out LOW time	4	35		ns
t_{MRW}	Master Reset pulse	8	40		ns
t_{MRS}**	Master Reset to SI	8	45		ns

* Instant-On Case Temperature.
** t_{MRS} is measured on initial characterization lots only and is not directly tested in production.

505019

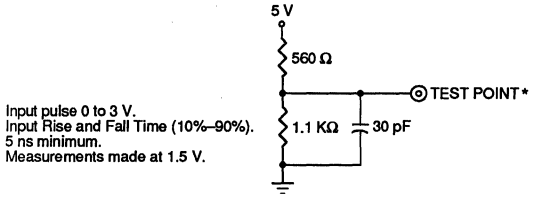
Switching Characteristics C57401A/2A Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	MILITARY MIN	MILITARY MAX	UNIT
f_{IN}	Shift in rate	1	10		MHz
t_{IRL}†	Shift in to Input Ready LOW	1		50	ns
t_{IRH}†	Shift in to Input Ready HIGH	1		50	ns
f_{OUT}	Shift Out rate	4	10		MHz
t_{ORL}†	Shift Out to Output Ready LOW	4		65	ns
t_{ORH}†	Shift Out to Output Ready HIGH	4		65	ns
t_{ODH}	Output Data Hold (previous word)	4	10		ns
t_{ODS}	Output Data Shift (next word)	4		60	ns
t_{PT}	Data throughput or "fall through"	3, 6		2.2	µs
t_{MRORL}	Master Reset to OR LOW	8		65	ns
t_{MRIRH}	Master Reset to IR HIGH	8		65	ns
t_{IPH}*	Input Ready pulse HIGH	3	30		ns
t_{OPH}*	Output Ready pulse HIGH	6	30		ns

† See AC test and high speed application note.
* This parameter applies to FIFOs communicating with each other in a cascaded mode.

505020

Test Load for All Devices



*The "TEST POINT" is driven by the output under test, and observed by instrumentation.

505 133

Electrical Characteristics Over Operating Conditions For all Devices

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8†	V
V_{IH}	High-level input voltage				2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = –18 mA			–1.5	V
I_{IL1}	Low-level input current	D_0–D_n, $\overline{MR}$	V_{CC} = MAX	V_I = 0.45 V			–0.8	mA
I_{IL2}		SI, SO					–1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4 V			50	µA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8 mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = –0.9 mA	2.4			V
I_{OS}	Output short-circuit current*		V_{CC} = MAX	V_O = 0 V	–20		–90	mA
I_{CC}	Supply current		V_{CC} = MAX	57401			160	mA
				57401A			180	
				57402			180	
				57402A			200	
			Inputs low, outputs open.	C57401			160	
				C57401A			180	
				C57402			180	
				C57402A			200	

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† These are absolute voltages with respect to device GND (Pin 8 or 9) and includes all overshoots due to test equipment. Do not attempt to test these values without suitable equipment.

505021

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig 8) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_x inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought low. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a Shift-Out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_x outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_x remains as before (i.e. data does not change if FIFO is empty). Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

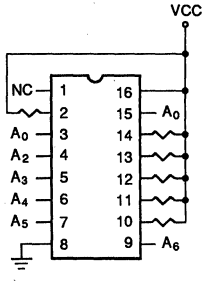
AC Test and High Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitance and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 µF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading, i.e. rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency or FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (t_{IDH}) and the next activity of the Input Ready (t_{IRL}) to be extended relative to Shift-In going High. This same type of problem is also related to t_{IRH}, t_{ORL} and t_{ORH} as related to Shift-Out.

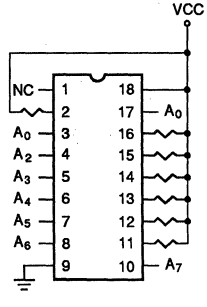
Life Test/Burn-In Circuits

Complies with Mil-Std-883 Method 1005/1015, Condition D.

57401
57401A
C57401
C57401A

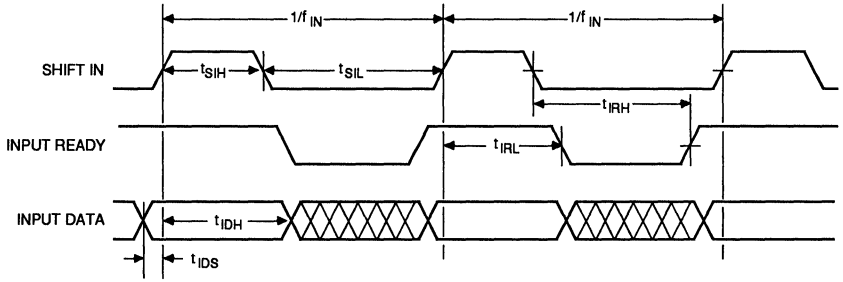


57402
57402A
C57402
C57402A



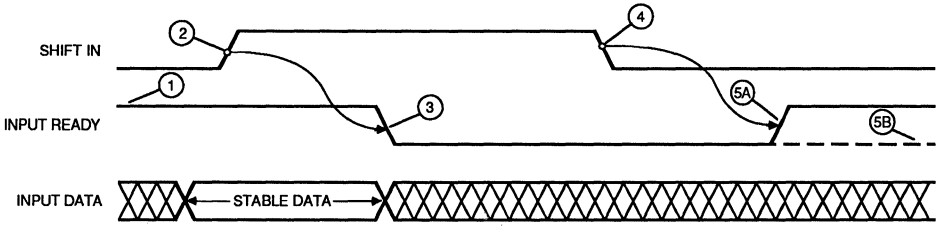
505 134

$T_{ambient}$ = 125° C
V_{CC} = 5.25 ± 0.25 V
Square wave pulses on A0 to A8 are:
1. 50% ± 15% duty cycle
2. Logic "0" = –1 V to 0.7 V
3. Logic "1" = 2.4 V to V_{CC}
4. Frequency of each address is to be one-half of each preceding input, with A0 beginning at 100 kHZ.
   e.g., A0 = 100 kHz
   A1 = 50 kHz ± 10%
   A2 = 25 kHz ± 10%
   An = 1/2 An–1 ± 10%, etc.



505 136

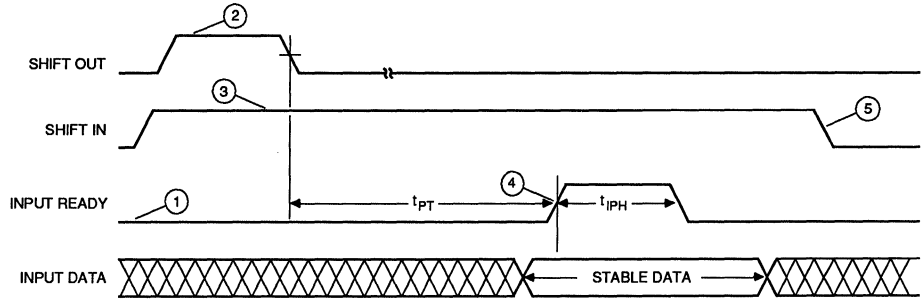
Figure 1. Input Timing



(1) Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
(2) Input Data is loaded into the first word.
(3) Input Ready goes LOW indicating the first word is full.
(4) The Data from the first word is released for "fall-through" to second word.
(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.
(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.
NOTE: Shift in pulses applied while Input Ready is LOW will be ignored (See Figure 3).

505 137

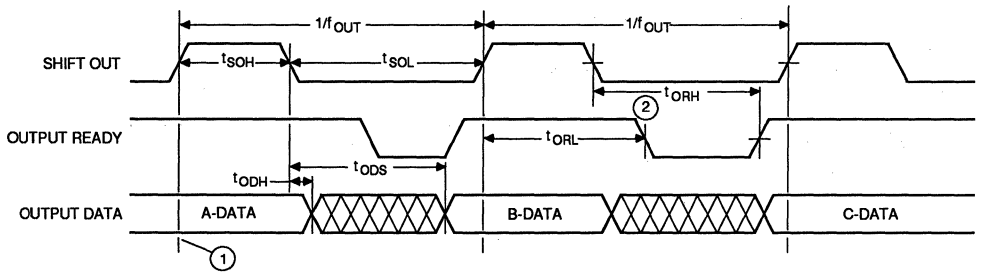
Figure 2. The Mechanism of Shifting Data Into the FIFO



(1) FIFO is initially full.
(2) Shift Out pulse is applied. An empty location starts "bubbling" to the front.
(3) Shift in is held HIGH.
(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
(5) The Data from the first word is released for "fall through" to second word.

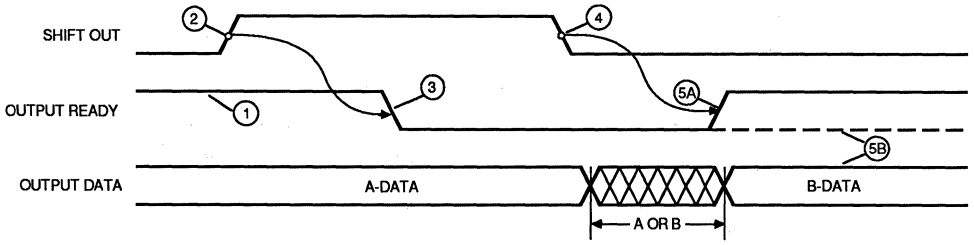
505 138

Figure 3. Data Is Shifted In Whenever Shift In and Input Ready Are Both HIGH



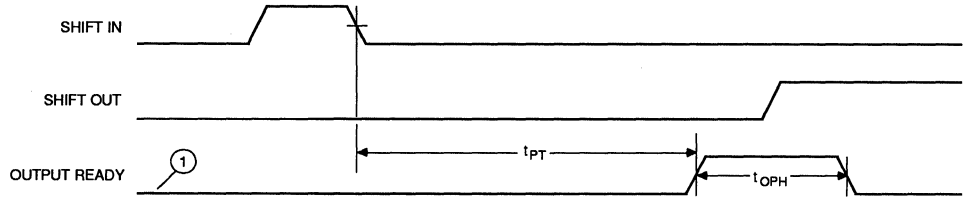
(1) The diagram assumes that at this time words 63, 62, 61 are loaded with A, B, C Data respectively.
505 139 (2) Data is shifted out when Shift Out makes a HIGH to LOW transition.

Figure 4. Output Timing



(1) Ouput Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
(2) Shift Out goes HIGH causing the next step.
(3) Output Ready goes LOW.
(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.
(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.
(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.
505 140 NOTE: Shift Out pulses applied when Output Ready is LOW will be ignored (Figure 7).

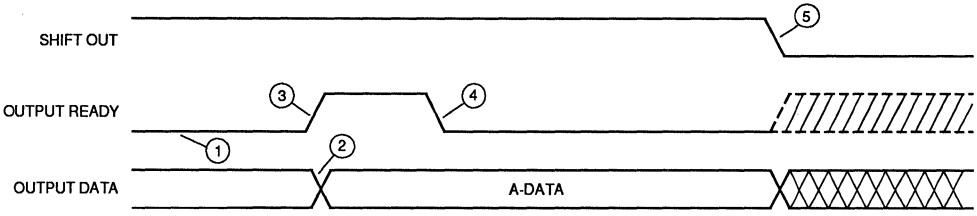
Figure 5. The Mechanism of Shifting Data Out of the FIFO



505 141

① FIFO initially empty.

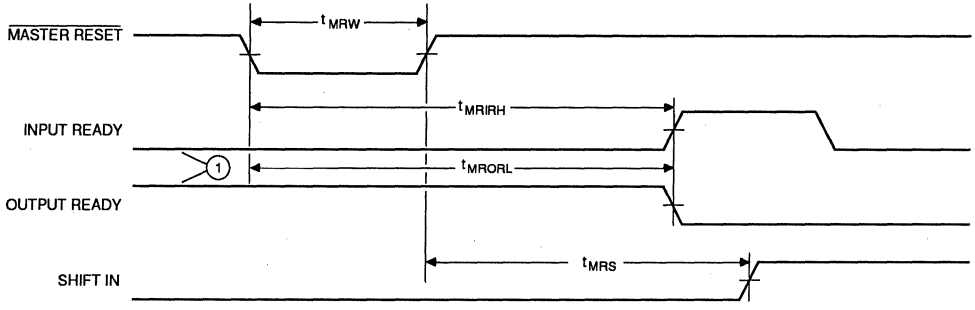
Figure 6. t_{PT} and t_{OPH} Specification



① Word 63 is empty.
② New data (A) arrives at the output (word 63).
③ Output Ready goes HIGH indicating the arrival of the new data.
④ Since Shift Out is held HIGH, Output Ready goes immediately LOW.
⑤ As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.

505 142

Figure 7. Data Is Shifted Out Whenever Shift Out and Output Ready Are Both HIGH



① FIFO initially full.

505 143

Figure 8. Master Reset Timing

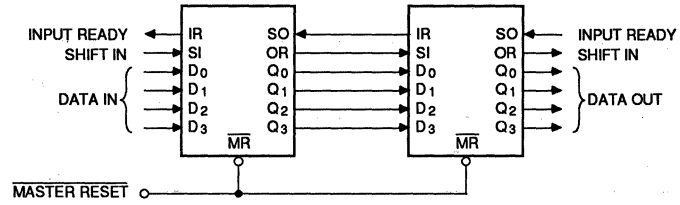


Figure 9. Cascading FIFOs to Form 128X4 FIFO with C57401/A

Cascadable FIFOs can be easily cascaded to any desired length. The handshaking and associated timing between the FIFOs are handled by the FIFOs themselves.

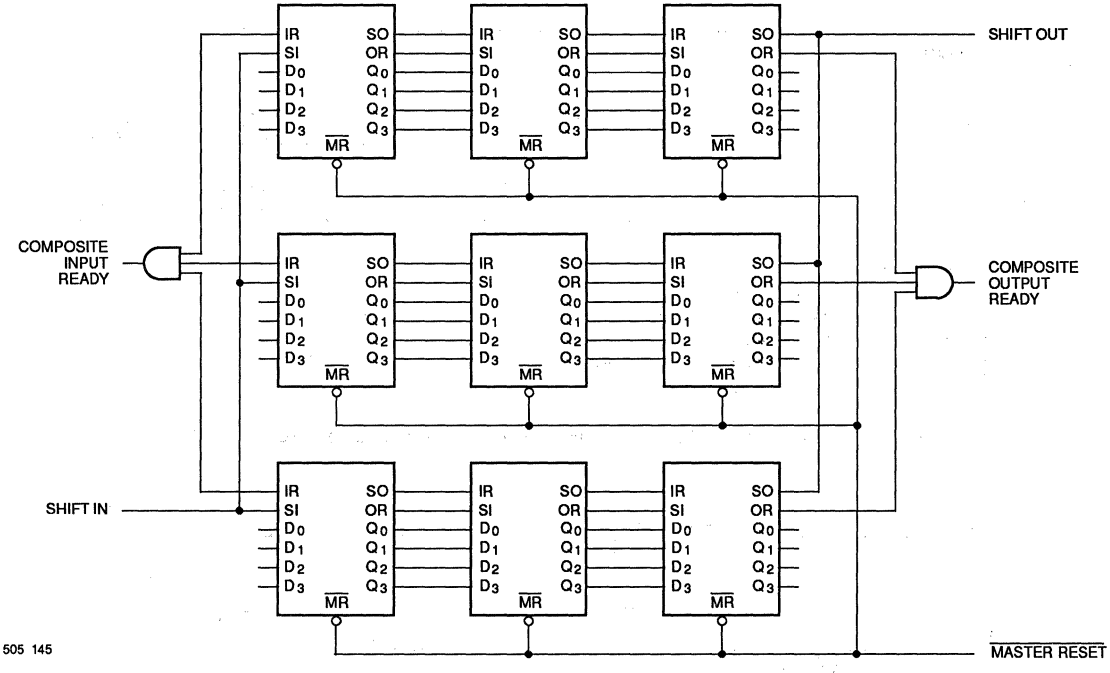


Figure 10. 192X12 FIFO with C57401/A

Cascadable FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall-through times of the FIFOs.

Military Low Power FIFOs 64x4 64x5 Memory

12 MHz (Standalone)

57L401D 57L402D 57L4013D

Conforms to Mil-Std-883, Class B

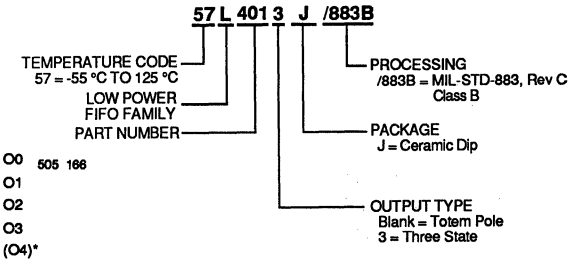
Features/Benefits

- **High-speed 12 MHz shift-in/shift-out data rates**
- **Low power consumption**
- **Choice of 4-bit or 5-bit data width**
- **TTL inputs and outputs**
- **Readily expandable in word width**
- **Structured pinouts. Outputs pins directly opposite corresponding input pins**
- **High-drive capability**
- **Asynchronous operation**
- **Dose rate (transient upset) junction-isolated bipolar process $2x10^{10}$ RADs (Si)/s recovery time of 50 to 70 µs from a 1 µs pulse**
- **Neutron fluence (permanent damage): $1x10^{13}$ N/cm²**

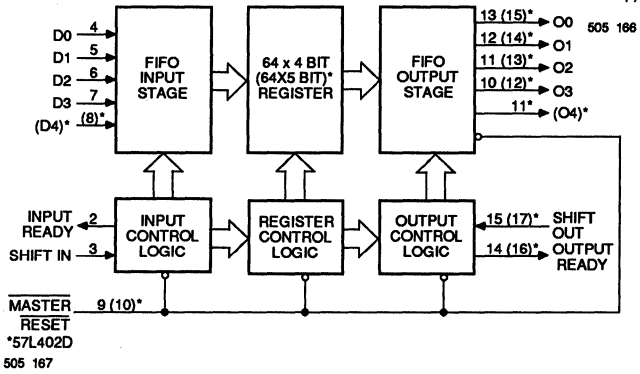
Description

The 57L401D/2D and 574013D are "fall-through" high-speed First-In First-Out (FIFO) memories organized 64 words by 4 bits and 64 words by 5 bits. These FIFOs are expandable in word width. The FIFOs are attractive for many applications such as disk controllers, communication buffers, rate buffers, etc. They feature high-drive (I_{OL} = 12 mA) outputs. The 57L4013D features three-state outputs.

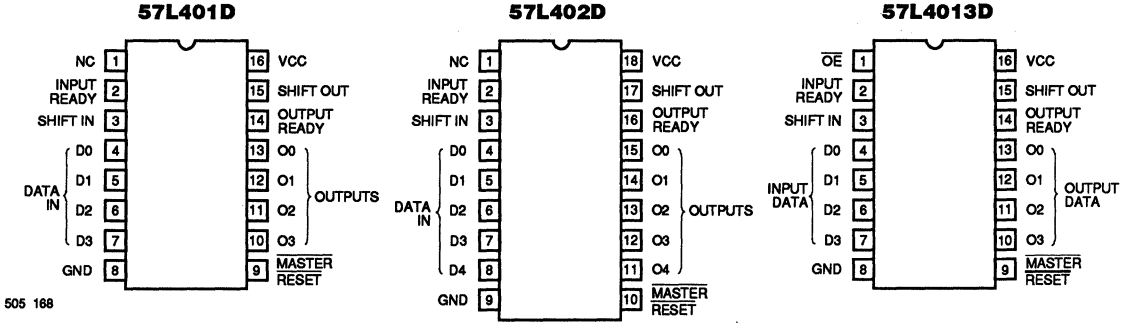
Ordering Information



Block Diagram



Device Pinouts



Absolute Maximum Ratings*

Supply voltage, V_{CC} ..... –0.5 V to 7 V
Input voltage range ..... –1.5 V to 7 V
Off-state output voltage ..... –0.5 V to to 5.5 V
Storage temperature ..... –65°C to +150°C

*Note:
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Operating Conditions

SYMBOL	PARAMETER	FIGURE	MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
t_{SIH}†	Shift in HIGH time	1	30		ns
t_{SIL}†	Shift in LOW time	1	15		ns
t_{IDS}	Input data setup to SI (Shift In)	1	0		ns
t_{IDH}	Input data hold time to SI (Shift In)	1	35		ns
t_{RIDS}	Input data setup to IR (Input Ready)	3	0		ns
t_{RIDH}	Input data hold time to IR (Input Ready)	3	35		ns
f_{IN}	Shift in rate	1		12	MHz
f_{OUT}	Shift out rate	4		12	MHz
t_{SOH}†	Shift out HIGH time	4	28		ns
t_{SOL}†	Shift out LOW time	4	18		ns
t_{MRW}**	Master Reset pulse	8	40		ns
t_{MRS}***	Master Reset to SI	8	45		ns
V_{IL}*	Low level input voltage			0.8	V
V_{IH}*	High level input voltage		2.0		V
T_A	Operating free-air temperature		–55		°C
T_C	Operating instant-on case temperature			125	°C

* These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
** If the FIFO is not full (IR HIGH) $\overline{MR}$ LOW forces IR LOW, followed by IR returning high when $\overline{MR}$ goes high.
*** t_{MRS} is measured on initial characterization lots only and is not directly tested in production.
† See AC test and high-speed application note.

505027

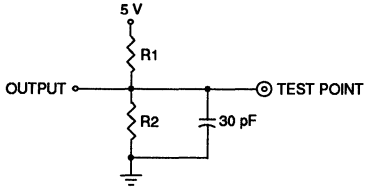
Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = –18 mA		–1.5	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = 0.45 V		–250	µA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4 V		50	µA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5 V		1	mA
V_{OL}	Low-level output voltage	Ouput, O	V_{CC} = MIN	I_{OL} = 12 mA		0.5	V
		IR, OR		I_{OL} = 8 ma			
V_{OH}	High-level output voltage	Output, O	V_{CC} = MIN	I_{OH} = –3.0 mA	2.4		V
		IR, OR		I_{OH} = –0.9 mA			
I_{OS}†	Output short-circuit current		V_{CC} = MAX	V_O = 0 V	–20	–90	mA
I_{OZL}	Off-state output current (57L4013D only)		V_{CC} = MAX	V_O = 0.4 V		–50	µA
I_{OZH}				V_O = 2.4 V		+50	
I_{CC}	Supply current		V_{CC} = MAX All inputs low. All outputs open.			120	mA

† Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

505028

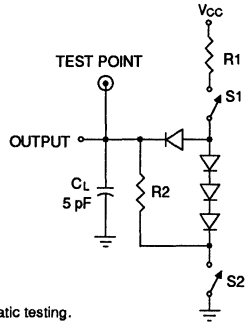
Standard Test Load*



Input Pulse Amplitude = 3 V
Input Rise and Fall Time (10% – 90%) = 2.5 ns
Measurements made at 1.5 V

505 107

Three State Test Load*



*Equivalent test loads may be used for automatic testing.

I_{OL}	R1	R2
12 mA	390 Ω	760 Ω
8 mA	600 Ω	1200 Ω

505028A

Switching Characteristics Over Operating Conditions

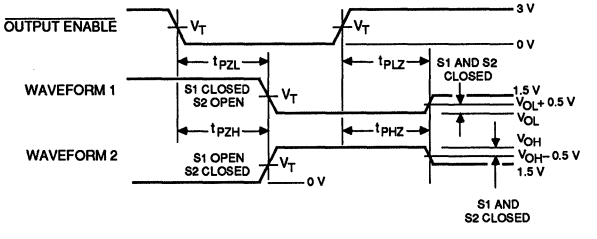
SYMBOL	PARAMETER	FIGURE	MIN	MAX	UNIT
t_{IRL}†	Shift In ↑ to Input Ready LOW	1		50	ns
t_{IRH}†	Shift In ↓ to Input Ready HIGH	1		30	ns
t_{ORL}†	Shift Out ↑ to Output Ready LOW	4		55	ns
t_{ORH}†	Shift Out ↓ Output Ready HIGH	4		55	ns
t_{ODH}†	Output Data Hold (previous word)	4	10		ns
t_{ODS}	Output Data Shift (next word)	4		50	ns
t_{PT}	Data throughput	3, 6		2.0	µs
t_{MRORL}	Master Reset ↓ to Output Ready LOW	8		65	ns
t_{MRIRH}*	Master Reset ↑ to Input Ready HIGH	8		35	ns
t_{MRIRL}*	Master Reset ↓ to Input Ready LOW	8		55	ns
t_{MRO}	Master Reset ↓ to Output LOW	8		75	ns
t_{IPH}	Input ready pulse HIGH	3	15		ns
t_{OPH}	Output ready pulse HIGH	6	20		ns
t_{ORD}	Output ready ↑ to Data Valid	4		0	ns
t_{PHZ}**	Output disable delay (57L4013D only)	A		35	ns
t_{PLZ}**				35	
t_{PZL}	Output Enable Delay (57L4013D only)	A		35	ns
t_{PZH}				45	

† See AC test and high-speed application note.

* If the FIFO is not full (IR HIGH), $\overline{MR}$ LOW forces IR LOW, followed by IR returning high when $\overline{MR}$ goes high.

** Actual test limits may be different to compensate for ATE.

505029



Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

505 171

Figure A. Enable and Disable (57L4013D Only)

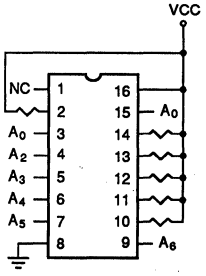
Military Case Outlines

PACKAGE OUTLINE LETTER	CONFORMS TO MIL-M-38510 APPENDIX C CASE
16J	D-2
18J	D-6

505029B

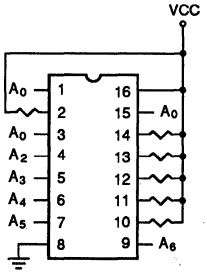
Burn-In Circuitry
Dynamic Burn-In

57L401D

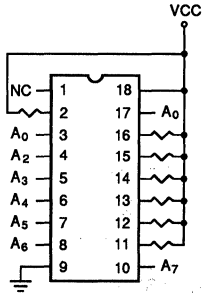


505 172

57L4013D



57L402D



$T_{ambient}$ = 125°C
V_{CC} = 5.25 ± 0.25 V
Square wave pulses on A0 to A8 are:

1. 50% ± 15% duty cycle
2. Logic "0" = –1 V to 0.7 V
3. Logic "1" = 2.4 V to V_{CC}
4. Frequency of each address is to be one-half of each preceding input, with A0 beginning at 100 kHZ.
   e.g. A0 = 100 kHz
   A1 = 50 kHz ± 10%
   A2 = 25 kHz ± 10%
   An = 1/2 An–1 ± 10%, etc.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Figure 8) to prepare the FIFO to accept data in the first location. Master reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from the D_x inputs. Data then present at the data inputs is entered into the first location when the Shift-In (SI) is brought HIGH. An SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data from any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW. The FIFO should always be cleared by using master reset.

Data Output

Data is read from the Ox outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided the upstream stage has valid data, is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor 0.1 µF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input-Ready combination, as well as the Shift-Out-Output-Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to Shift-In going HIGH. This same type of situation occurs with T_{ORL} and T_{ORH} as related to Shift-Out. For high-speed applications, proper grounding technique is essential.

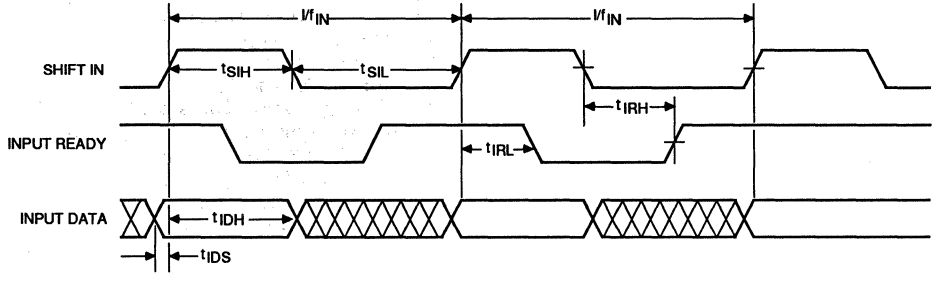
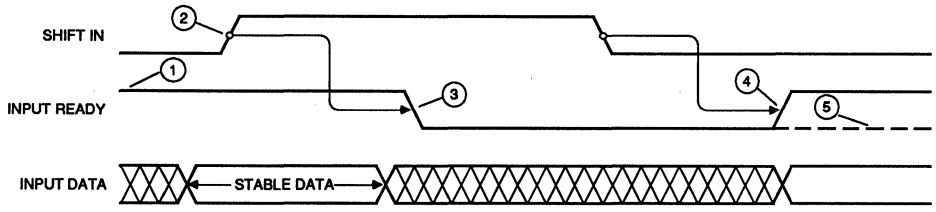


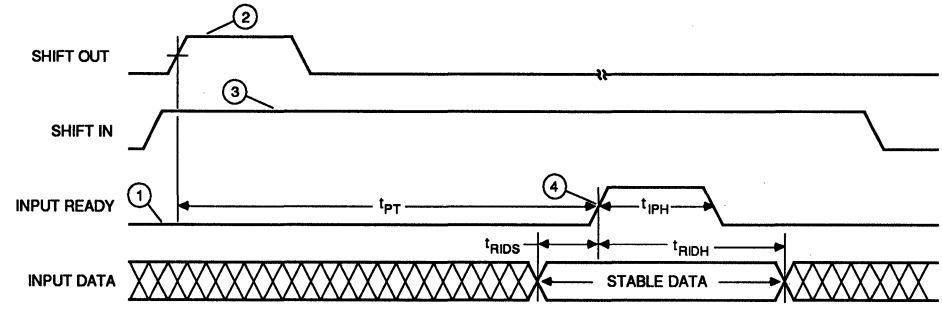
Figure 1. Input Timing



① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
② Input Data is loaded into the first word. The Data from the first word is released for "fall through" to second word.
③ Input Ready goes LOW indicating the first word is full.
④ Shift-In going LOW allows Input Ready to sense the status of the first word. The first word is now empty as indicated by Input Ready HIGH.
⑤ If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

505 154 Note: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 3).

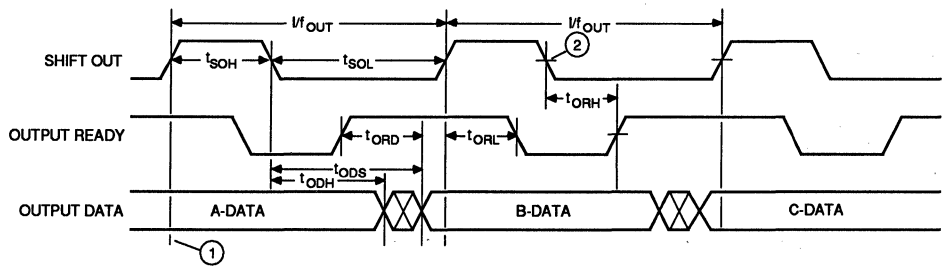
Figure 2. The Mechanism of Shifting Data Into the FIFO



① FIFO is initially full.
② Shift Out pulse is applied. An empty location starts "bubbling" to the front.
③ Shift in is held HIGH.

505 175 ④ As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

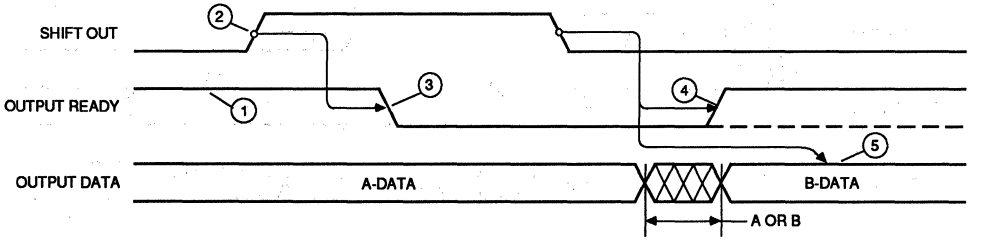
Figure 3. Data Is Shifted In Whenever Shift In and Input Ready Are Both HIGH



① The diagram assumes that at this time, words 63, 62 and 61 are loaded with A, B and C Data, respectively.

505 176 ② Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO ar both high together.

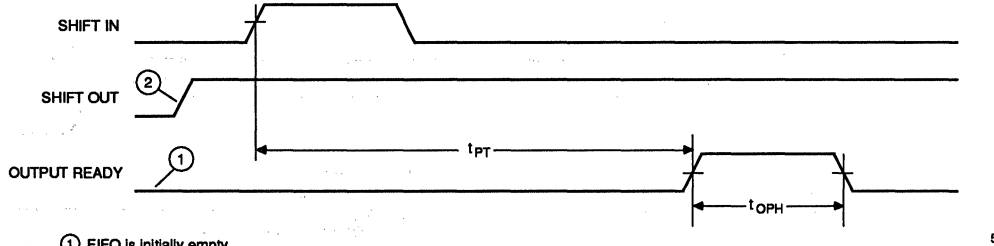
Figure 4. Output Timing



(1) Ouput Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
(2) Shift-Out goes HIGH causing the contents of word 62 (B-DATA) to be released for fall through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.
(3) Output Ready goes LOW.
(4) Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
(5) If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

505 177

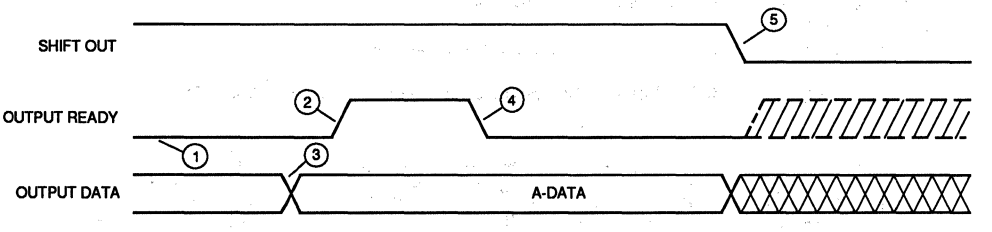
Figure 5. The Mechanism of Shifting Data Out of the FIFO



505 178

(1) FIFO is initially empty
(2) Shift Out held HIGH.

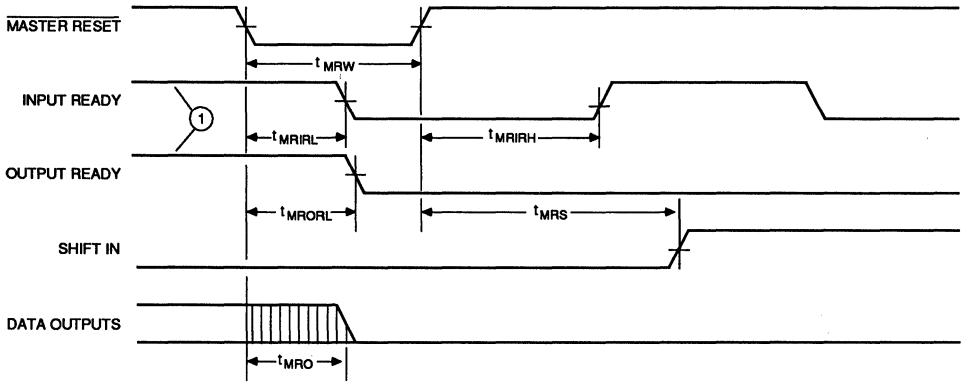
Figure 6. t_{PT} and t_{OPH} Specification



(1) Word 63 is empty.
(2) Output Ready goes HIGH indicating arrival of the new data.
(3) New data (A) arrives at the outputs (word 63).
(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.
(5) As soon as Shift Out goes LOW the Output Data is subject to change. Output Ready will go HIGH or LOW depending on whether there are any additional upstream words in the FIFO.

505 179

Figure 7. Data Is Shifted Out Whenever Shift Out and Output Ready Are Both HIGH



505 180

① FIFO is initially full.

Figure 8. Master Reset Timing

Military First-In First-Out (FIFO) 64x5 Memory

25 MHz (Standalone) 57413A

Conforms to Mil-Std-883, Class B

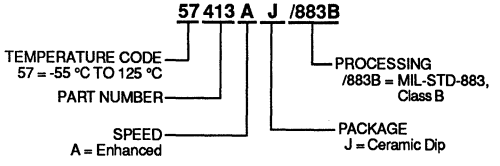
Features/Benefits

- **High-speed 25 MHz shift-in/shift-out rates**
- **High-drive capability**
- **Three-state outputs**
- **Half-Full and Almost-Full/Empty status flags**
- **Structured pinouts, Output pins directly opposite corresponding Input pins**
- **Asynchronous operation**
- **TTL-compatible Inputs and Outputs**
- **Dose rate (transient upset) junction-isolated bipolar process 2x10^{10} RADs (Si)/s recovery time of 50 to 70 µs from 1 µs pulse**
- **Neutron fluence (permanent damage): 1x10^{13} N/cm2**

Description

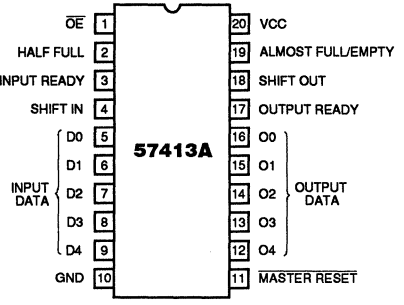
The 57413A is a high-speed, 64x5 First-In-First-Out (FIFO) memory which operates at a 25 MHz input/output rate. The data is loaded and emptied on a first-in-first-out basis. It is a three-state device with high-drive (I_{OL} = 12 mA) data outputs. This device can be connected in parallel to give FIFOs of any word length. It has a Half-Full flag (thirty-two or more words full) and an almost full/empty flag (fifty-six or more words or eight or less words). The main applications of the 57413A are rate buffers; sourcing and absorbing data at different rates. Other applications are high-speed tape and disk controllers, data communications systems and plotter control systems.

Ordering Information



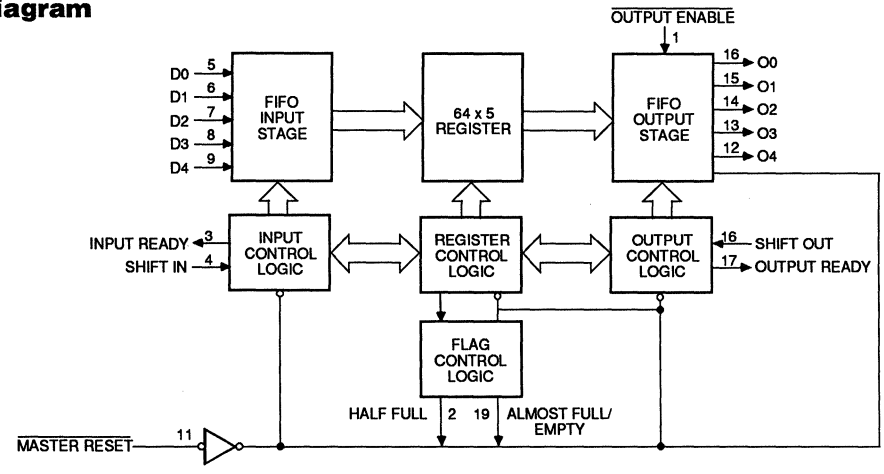
505 146

Pin Configuration



505 147

Block Diagram



505 148

Absolute Maximum Ratings*

Supply voltage, V_{CC} ..... –0.5 V to 7 V
Input Voltage range ..... –1.5 V to 7 V
Off-state output voltage ..... –0.5 V to to 5.5 V
Storage temperature ..... –65°C to +150°C

*Note:
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Operating Conditions

SYMBOL	PARAMETER	FIGURE	MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
t_{SIH}†	Shift in HIGH time	1	16		ns
t_{SIL}†	Shift in LOW time	1	20		ns
t_{IDS}	Input data setup time	1	2		ns
t_{IDH}	Input data hold time	1	25		ns
t_{SOH}†	Shift out HIGH time	4	10		ns
t_{SOL}	Shift out LOW time	4	27		ns
t_{MRW}	Master Reset pulse	8	35		ns
t_{MRS} **	Master Reset to SI	8	35		ns
V_{IL} *	Low level input voltage			0.8	V
V_{IH} *	High level input voltage		2.0		V
T_A	Operating free-air temperature		–55		°C
T_C	Operating instant-on case temperature			125	°C

* These are absolute voltages with respect to the GND (Pin 10) and includes all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
** t_{MRS} is measured on initial characterization lots only and is not directly tested in production.
†See AC test and high speed application note.

505022

Conforms to MIL-STD-883; Group A, Subgroups 1, 2, & 3.

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	MAX	UNIT
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18 mA			–1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45 V			–250	µA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V			50	µA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V			1	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} (Data outputs)	12 mA		0.5	V
			I_{OL} (IR, OR)	8 mA†			
			I_{OL} (Flag outputs)	8 mA			
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} (Data outputs)	–3.0 mA			V
			I_{OH} (IR, OR)	–0.9 mA	2.4		
			I_{OH} (Flag outputs)	–0.9 mA			
I_{OS}*	Output short-circuit current	V_{CC} = MAX	V_O = 0 V		–20	–90	mA
I_{HZ}	Off-state output current	V_{CC} = MAX	V_O = 2.4 V			20	µA
I_{LZ}		V_{CC} = MAX	V_O = 0.4 V			–20	µA
I_{CC}**	Supply current	V_{CC} = MAX, inputs low, outputs open				240	mA

* Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
** See curve for I_{CC} vs. temp.
† Care should be taken to minimize as much as possible the DC and capacitive load on IR and OR when operating at frequencies above 25 MHz.

505023

Switching Characteristics Over Operating Conditions Conforms to MIL-STD-883; Group A, Subgroups 9, 10, 11.

SYMBOL	PARAMETER	FIGURE	MIN	MAX	UNIT
f_{IN}	Shift in rate	1	DC	25	MHz
t_{IRL}†	Shift In ↑ to Input Ready LOW	1		28	ns
t_{IRH}†	Shift In ↓ to Input Ready HIGH	1		25	ns
f_{OUT}	Shift Out rate	4	DC	25	MHz
t_{ORL}†	Shift Out ↑ to Output Ready LOW	4		28	ns
t_{ORH}†	Shift Out ↓ to Output Ready HIGH	4		25	ns
t_{ODH}†	Output Data Hold (previous word)	4	10		ns
t_{ODS}	Output Data Shift (next word)	4		40	ns
t_{PT}	Data throughput or "fall through"	3, 6		750	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	8		30	ns
t_{MRIRH}	Master Reset ↑ to Input Ready HIGH	8		30	ns
t_{MRIRL}*	Master Reset ↓ Input Ready LOW	8		30	ns
t_{MRO}	Master Reset ↓ to Outputs LOW	8		55	ns

* If the FIFO is not full (IR High), $\overline{MR}$ low forces IR low, followed by IR returning high when $\overline{MR}$ goes high.
† See AC test and high-speed application note.

505024

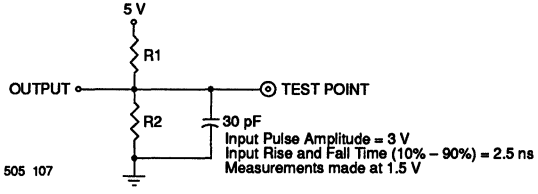
Switching Characteristics Over Operating Conditions (Cont.)

SYMBOL	PARAMETER	FIGURE	MIN	MAX	UNIT
t_{IPH}	Input ready pulse HIGH	3	5		ns
t_{OPH}	Output ready pulse HIGH	6	5		ns
t_{ORD}	Output ready ↑ HIGH to Data Valid	4		20	ns
t_{AEH}*	Shift Out ↑ AF/E HIGH	9		145	ns
t_{AEL}*	Shift In ↑ to AF/E LOW	9		650	ns
t_{AFL}*	Shift Out ↑ to AF/E LOW	10		650	ns
t_{AFH}*	Shift In ↑ to AF/E HIGH	10		145	ns
t_{HFH}*	Shift In ↑ to HF HIGH	11		380	ns
t_{HFL}*	Shift Out ↑ to HF LOW	11		380	ns
t_{PHZ}**	Ouput Disable Delay	A		30	ns
t_{PLZ}**		A		30	ns
t_{PZL}	Output Enable Delay	A		30	ns
t_{PZH}		A		50	ns

Note: Input rise and fall time (10%–90%) = 2.5 ns.
* See timing diagram for explanation of parameters.
** Actual test limits may be different to compensate for ATE.

Conforms to MIL-STD-883; Group A, Subgroups 9, 10, and 11.

Standard Test Load

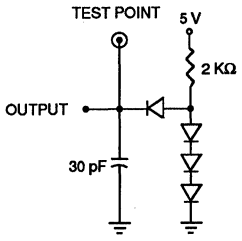


505 107

I_{OL}	R1	R2
12 mA	390 Ω	760 Ω
8 mA	600 Ω	1200 Ω

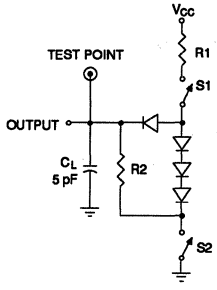
505025A

Design Test Load



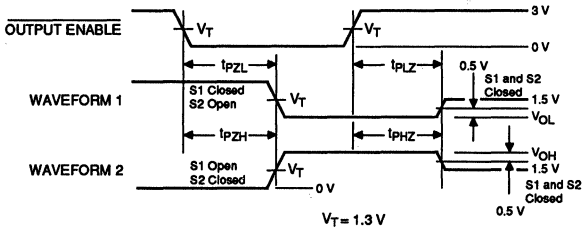
505 149

Three State Test Load*



505 107

*Equivalent test loads may be used for automatic testing



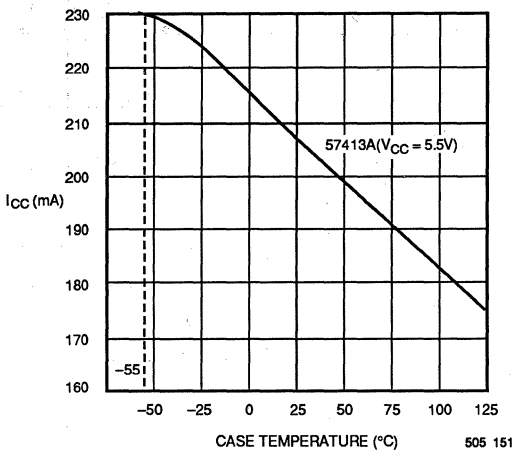
505 150

Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Figure A. Enable and Disable

Typical ICC vs Temperature (VCC = MAX)



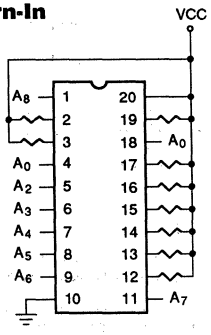
Military Case Outlines

PACKAGE OUTLINE LETTER	CONFORMS TO MIL-M-38510F APPENDIX C CASE
J	D-8

505025B

Burn-In Circuitry

Dynamic Burn-In



505 152

$T_{ambient}$ = 125°C
V_{cc} = 5.25 ± 0.25 V
Square wave pulses on A0 to A8 are:

1. 50% ± 15% duty cycle
2. Logic "0" = –1 V to 0.7 V
3. Logic "1" = 2.4 V to V_{cc}
4. Frequency of each address is to be one-half of each preceding input, with A0 beginning at 100 kHZ.
   e.g., A0 = 100 kHz
   A1 = 50 kHz ± 10%
   A2 = 25 kHz ± 10%
   An = 1/2 An–1 ± 10%

Functional Description

Data Input

After power up the Master Reset is pulsed low (Figure 8) to prepare the FIFO to accept data in the first location. Master Reset must be applied prior to use to ensure proper operation. When Input Ready (IR) is HIGH the first location is ready to accept data from D_x inputs. Data then present at the data inputs in entered into the first location when the Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Once data is entered into the first cell, the transfer of data in any full cell to the adjacent (downstream) empty cell is automatically activated by an on-chip control. Thus data will stack up at the end of the device (while empty locations will "bubble" to the front when data is shifted out), t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating more room is available. If the memory is full, IR will remain LOW.

Data Output

Data is read from the O_x outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift-Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that there is valid upstream data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW and Data output will not be valid.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 60 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 µF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not high due to (a) too high a frequency, or (b) FIFO being full or effected by the Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to Shift-In going HIGH. This same type of problem is also related to T_{IRH}, T_{DRL}, and T_{ORH} as related to Shift-Out. Data outputs driving a bus should be limited to 10 MHz frequency. For high-speed applications, proper grounding technique is essential.

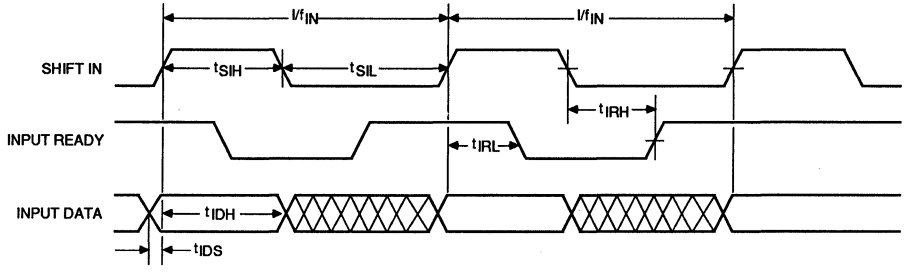
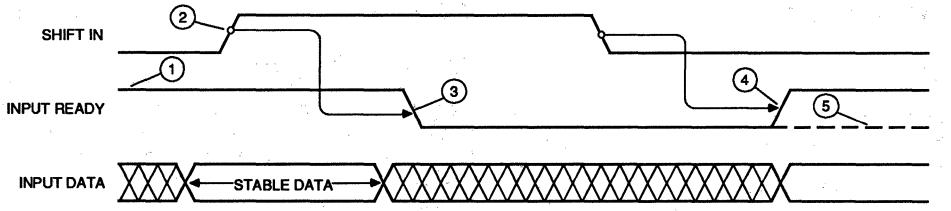


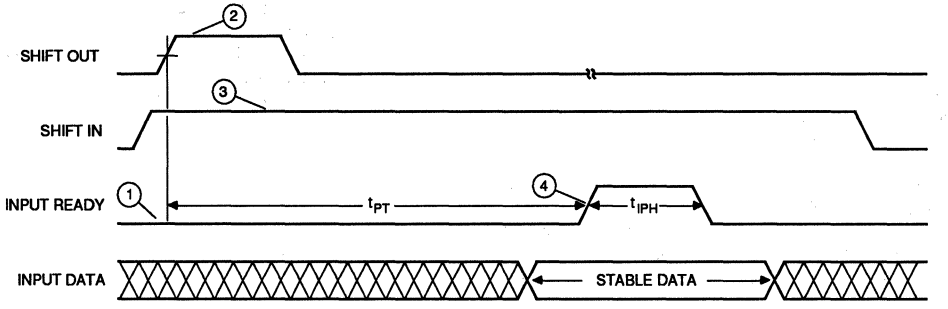
Figure 1. Input Timing



(1) Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
(2) Input Data is loaded into the first word. The Data from the first word is released for "fall through" to second word.
(3) Input Ready goes LOW indicating the first word is full.
(4) Shift-In going LOW allows Input Ready to sense the status of the first word. The first word is now empty as indicated by Input Ready HIGH.
(5) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.
Note: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 3).

505 173

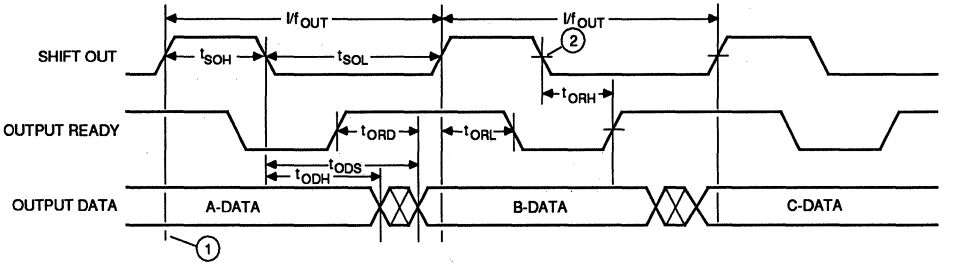
Figure 2. The Mechanism of Shifting Data Into the FIFO



(1) FIFO is initially full.
(2) Shift Out pulse is applied. An empty location starts "bubbling" to the front.
(3) Shift in is held HIGH.
(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.

505 155

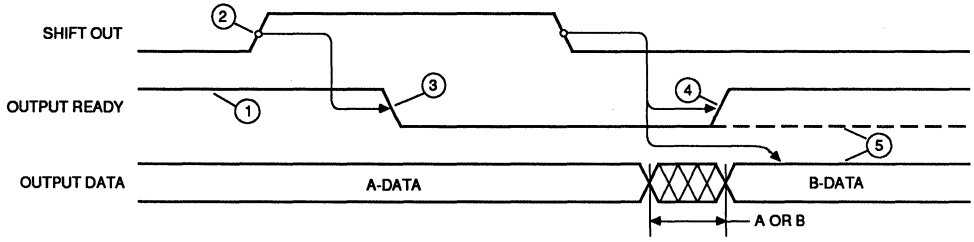
Figure 3. Data Is Shifted In Whenever Shift In and Input Ready Are Both HIGH



(1) The diagram assumes that at this time words 63, 62 and 61 are loaded with A, B and C Data, respectively.
(2) Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO are both high together.

505 156

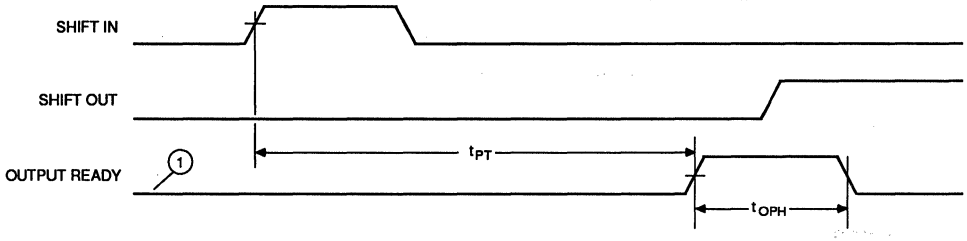
Figure 4. Output Timing



(1) Ouput Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
(2) Shift-Out goes HIGH causing the contents of word 62 (B-DATA) to be released for fall through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.
(3) Output Ready goes LOW.
(4) Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
(5) If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data become invalid.

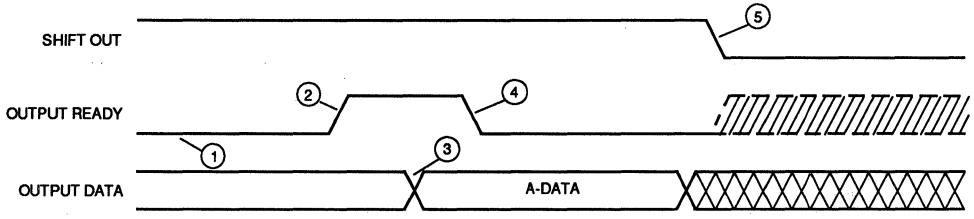
505 157 Note: Shift Out pulses applied when Output Ready is LOW will be ignored (See Figure 7).

Figure 5. The Mechanism of Shifting Data Out of the FIFO



505 158 (1) FIFO is initially empty

Figure 6. t_{PT} and t_{OPH} Specification



(1) Word 63 is empty.
(2) Output Ready goes HIGH indicating arrival of the new data
(3) New data (A) arruves at the outputs (word 63)
(4) Since Shift Out is held HIGH, Output Data is subject to change. Output Ready will go HIGH or LOW.
(5) As soon as Shift Ou goes LOW the Output Data is subject to change. Output Ready will go HIGH or Low depending on whether there are any additional upsteam words in the FIFO.

505 159 **Figure 7. Data Is Shifted Out Whenever Shift Out and Output Ready Are Both HIGH**

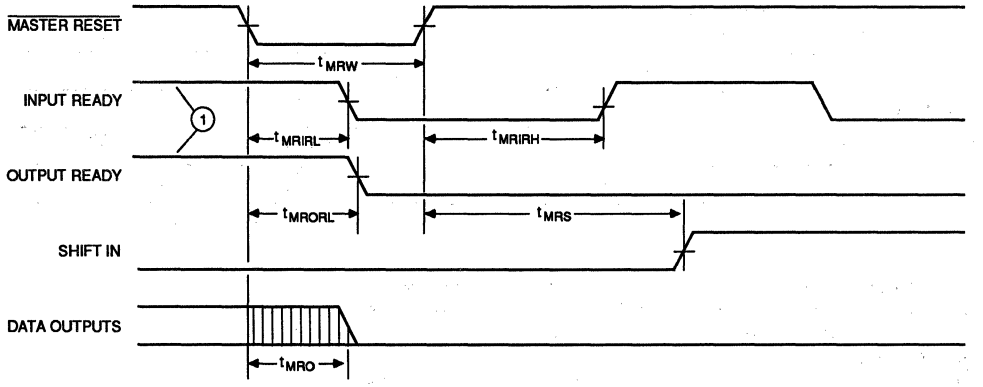
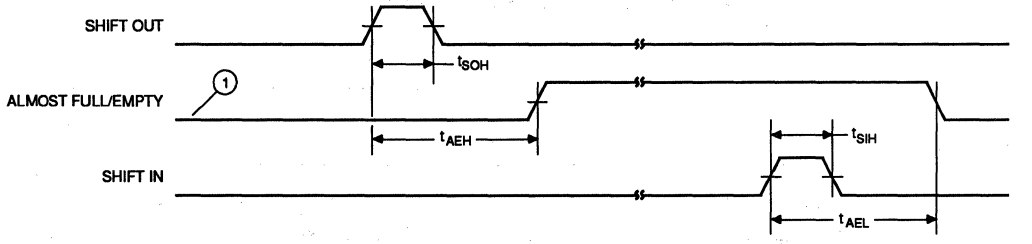


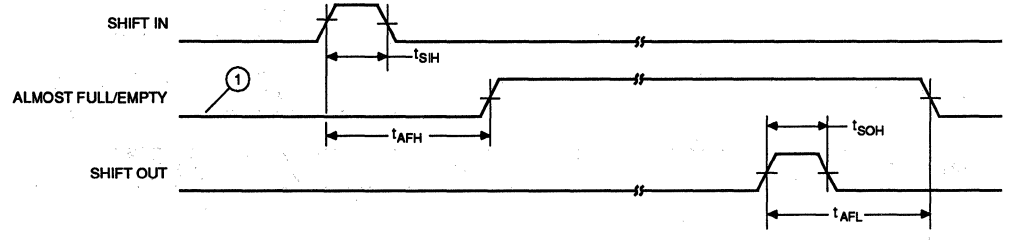
Figure 8. Master Reset Timing



① FIFO contains 9 words (one more than almost empty).

505 161

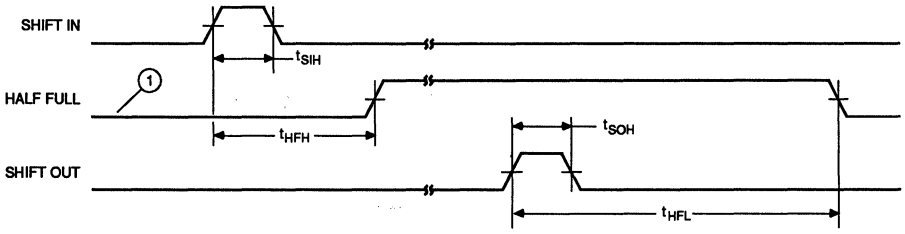
Figure 9. t_{AEH}, t_{AEL} Specifications



① FIFO contains 55 words (one short of almost full).

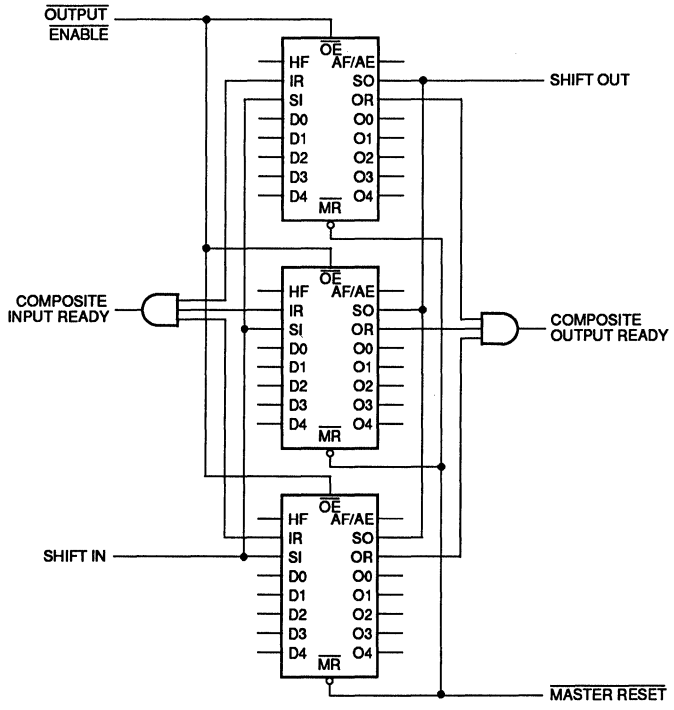
505 162

Figure 10. t_{AFH}, t_{AFL} Specifications



505 163 ① FIFO contains 31 words (one short of half full).

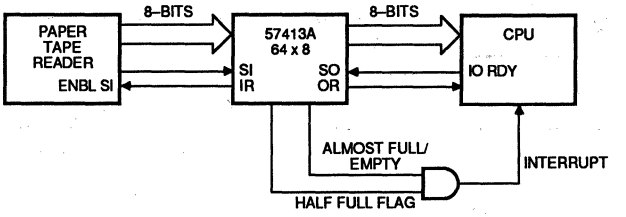
Figure 11. t_{HFL}, t_{HFH} Specifications



505 164

FIFOs are expandable in width. However, in forming wider words two external gates are required to generate composite Input and Output Ready Flags. This requirement is due to the different fall through times of the FIFOs.

Figure 12. 64 x 15 FIFO with 57413A



Note: Expanding the FIFOs in word width is done by ANDing the IR and OR as shown in Figure 12.

Figure 13. Application for the 57413A "Slow and Steady Rate to Fast 'Blocked Rate' " 505 165

Military CMOS Zero Power FIFOs

PRELIMINARY

Conforms to MIL-STD-883, Class B (Latest Revision)

57C401/13
57C402/23
57C4033
64x4 64x5 Memory
12 MHz (Cascadable)

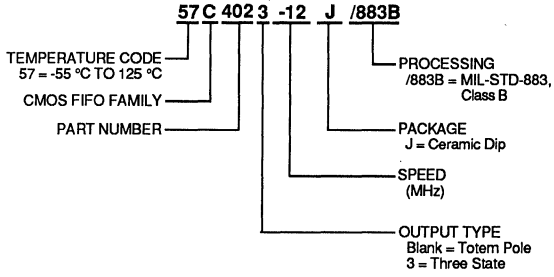
Features/Benefits

- **Zero standby power**
- **High-speed 12 MHz shift-in/shift-out data rates**
- **Very low active power consumption**
- **Choice of 4-bit or 5-bit data width**
- **TTL-compatible inputs and outputs**
- **Readily expandable in work width and depth**
- **RAM-based architecture for short fall-through delay**
- **Full CMOS 8-transistor cell for maximum noise immunity**
- **Asynchronous operation**
- **Output Enable feature (57C4013/23/33)**

Description

The 57C40X/XX series devices are high-performance CMOS RAM-based First-In First-Out buffer memory products organized as 64 words by 4 or by 5 bits wide. These devices use Monolithic Memories' CMOS process technology and meet the demands for high-reliability, high-speed, low-power operation. By utilizing an on-chip, dual-port RAM, a very short fall-through time is realized, improving overall system performance. Separate on-chip Read and Write pointers address each memory location, allowing the data to propagate to the outputs in much less time than in traditional register-based FIFOs. These FIFOs are easily integrated into many applications and perform particularly well in high-speed disk controllers, graphics, and communication systems. The 550 µwatt standby power of these devices makes them ideal for ultra-low-powered and battery powered systems.

Ordering Information

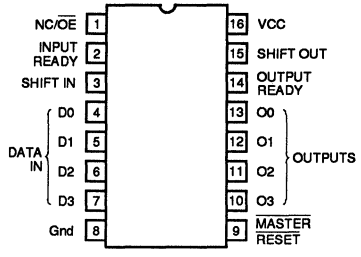


505 102

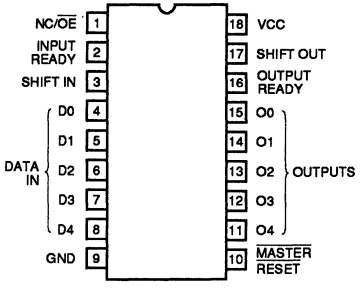
Pin Configurations

For Ceramic DIP Packages

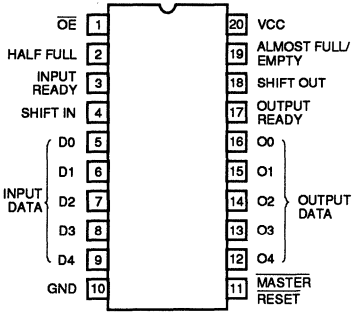
57C401/13



57C402/23



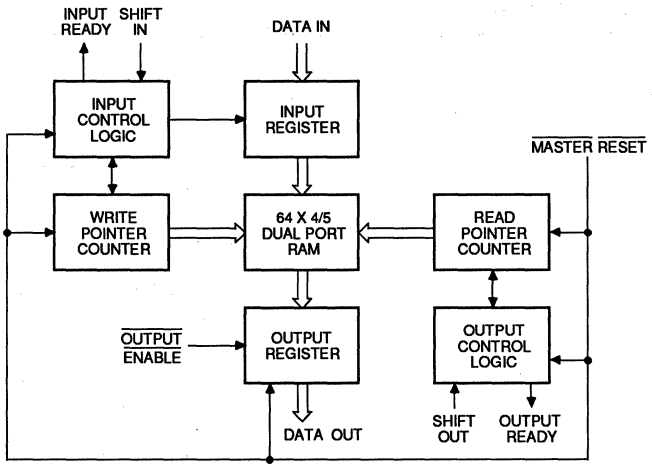
57C4033



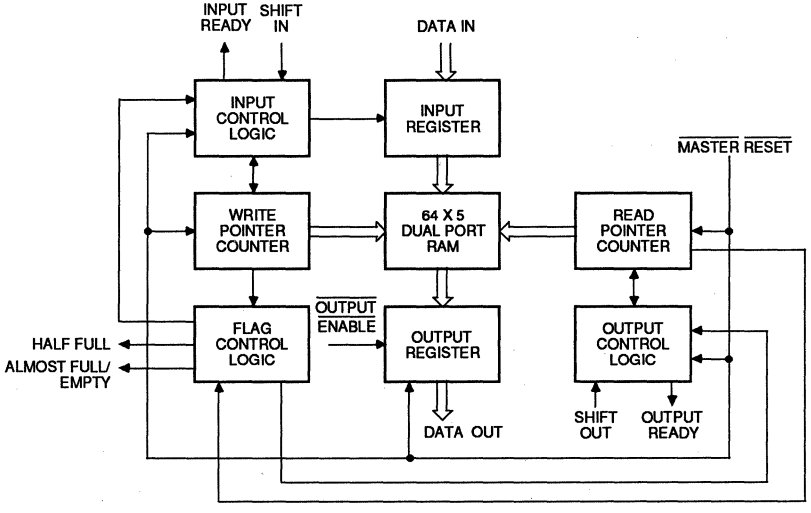
505 104

Block Diagrams

57C401/13
57C402/23



57C4033



505 101

Absolute Maximum Ratings*

Supply voltage, V_{CC} ..... –0.5 V to 7 V
Input Voltage range ..... –1.5 V to 7 V
Off state output voltage ..... –0.5 V to to 6.0 V
Storage temperature ..... –65°C to 150°C

*Note:
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

Operating Conditions

SYMBOL	PARAMETER	FIGURE	MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
t_{SIH}	Shift in HIGH time	1	16		ns
t_{SIL}	Shift in LOW time	1	25		ns
t_{IDS}	Input data setup to SI (Shift In)	1	0		ns
t_{IDH}	Input data hold time to SI (Shift In)	1	40		ns
t_{RIDS}	Input data setup to IR (Input Ready)	3	0		ns
t_{RIDH}	Input data hold time to IR (Input Ready)	3	30		ns
f_{IN}	Shift in rate	1	12		MHz
f_{OUT}	Shift out rate	4	12		MHz
t_{SOH}	Shift out HIGH time	4	27		ns
t_{SOL}	Shift out LOW time	4	25		ns
t_{MRW}**	Master Reset pulse	8	45		ns
t_{MRS}***	Master Reset to SI	8	75		ns
V_{IL}*	Low level input voltage			0.8	V
V_{IH}*	High level input voltage		2.0		V
T_A	Operating free-air temperature		–55		°C
T_C	Operating instant-on case temperature			125	°C

* These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system noise. Do not attempt to test these values without suitable equipment.
** If the FIFO is not full (IR HIGH) $\overline{MR}$ LOW forces IR LOW, followed by IR returning high when $\overline{MR}$ goes high.
*** t_{MRS} is measured on initial characterization lots only and is not directly tested in production.

505006

Conforms to MIL-STD-883; Group A, Subgroups 1, 2, and 3.

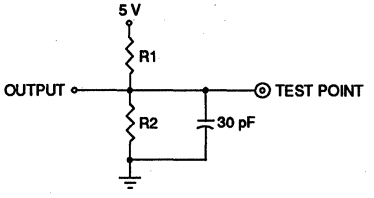
Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	MAX	UNIT
I_{IN}	Input current	V_{CC} = MAX	0 V<V_I<5.5 V	–1	1	µA
V_{OL}	Low-level output voltage	V_{CC}= MIN	I_{OL} = 2o µA		0.1	V
			I_{OL} = 8 mA		0.4	
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = –20 µA	V_{CC}–0.1		V
			I_{OH} = –4 mA	2.4		
I_{OZ}	Off-state output current ('4013, '4013, '4033 devices)	V_{CC} = MAX	0 V<V_{OUT}<5.5 V	–5	5	µA
I_{OS}*	Output short-circuit current	V_{CC} = MAX	V_O = 0 V	–20	–90	mA
I_{CC}op**	Maximum operating current	V_{CC} = MAX, All outputs open, f = 12 MHz			40	mA
I_{CC}stby	Maximum standby current ("CZ" devices only)	V_{CC} = MAX, All outputs open.			100	µA

* Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
** Tested on initial qualification lot only.

505007

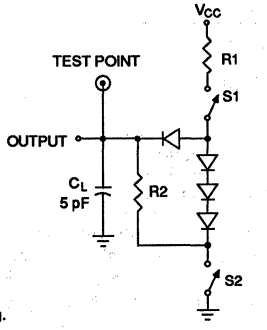
Standard Test Load*



Input Pulse Amplitude = 3 V
Input Rise and Fall Time (10% – 90%) = 2.5 ns
Measurements made at 1.5 V

505 107

Three State Test Load*



*Equivalent test load may be used for automatic testing.

Resistor Values

I_{OL}	R1	R2
8 mA	600 Ω	1200 Ω

505008

Conforms to MIL-STD-883; Group A, Subgroups 9, 10, and 11.

Switching Characteristics

SYMBOL	PARAMETER	FIGURE	MIN	MAX	UNIT
t_{IRL}†	Shift In ↑ to Input Ready LOW	1		70	ns
t_{IRH}†	Shift In ↓ to Input Ready HIGH	1		65	ns
t_{ORL}†	Shift Out ↑ to Output Ready LOW	4		65	ns
t_{ORH}†	Shift Out ↓ to Output Ready HIGH	4		60	ns
t_{ODH}†	Output Data Hold (previous word)	4	5		ns
t_{ODS}	Output Data Shift (next word)	4		40	ns
t_{PT}	Data throughput	3, 6		110	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	8		120	ns
t_{MRIRH}*	Master Reset ↓ to Input Ready HIGH	8		120	ns
t_{MRO}	Master Reset ↓ to Outputs LOW	8		45	ns
t_{MRHFL}	Master Reset ↓ to Half-Full Flag LOW ('4033 only)	9		120	ns
t_{MRAEH}	Master Reset ↓ to Almost Empty Flag HIGH ('4033 only)	9		120	ns
t_{IPH}	Input ready pulse HIGH	3	12		ns
t_{OPH}	Output ready pulse HIGH	6	10		ns
t_{ORD}	Output ready ↑ to Data Valid	4		0	ns
t_{AEH}	Shift Out ↑ to AF/E High ('4033 only)	10		125	ns
t_{AEL}	Shift In ↑ to AF/E LOW ('4033 only)	10		125	ns
t_{AFL}	Shift Out ↑ to AF/E LOW ('4033 only)	11		125	ns
t_{AFH}	Shift In ↑ to AF/E HIGH ('4033 only)	11		125	ns
t_{HFH}	Shift In ↑ to HF HIGH ('4033 only)	12		125	ns
t_{HFL}	Shift Out ↑ to HF LOW ('4033 only)	12		125	ns
t_{PHZ}**	Output disable delay ('4013, '4023, '4033 devices only)	A		30	ns
t_{PLZ}**				30	
t_{PZL}	Output enable delay ('4013, '4023, '4033 devices only)	A		35	ns
t_{PZH}				35	

* If the FIFO is not full (IR HIGH), $\overline{MR}$ LOW forces IR LOW, followed by IR returning high when $\overline{MR}$ goes high.
** Actual test limits may be different to compensate for ATE.
† See timing diagram for explanation of parameters.

505009

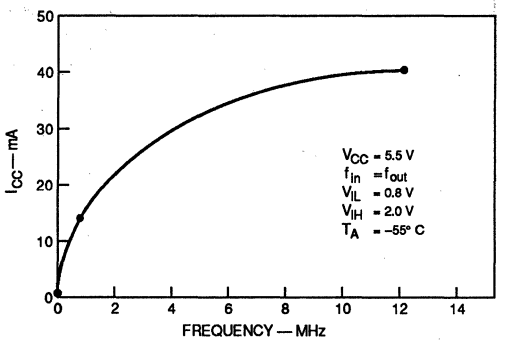
Capacitances *

SYMBOL	PARAMETER	TEST CONDITION	MIN	MAX	UNIT
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz		10	pF
C_{OUT}	Output capacitance	V_{CC} = 4.5 V		7	pF

*These parameters are not tested in production, but are evaluated at initial characterization and anytime the design is modified where capacitance may be affected.

505010

I_{CC} vs. Frequency



867 02

Military Case Outlines

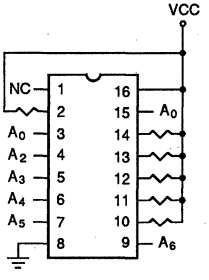
DEVICE	PACKAGE	
	J (Cerdip)	
	Package Outline	Conforms to MIL-M-38510 Appendix C Case
57C401	16J	D-2
57C4013	16J	D-2
57C402	18J	D-6
57C4023	18J	D-6
57C4033	20J	D-8

505011

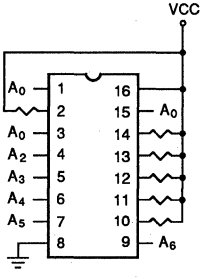
Burn-In Circuitry

Dynamic Burn-In

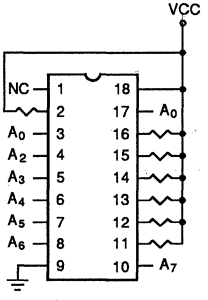
57C401



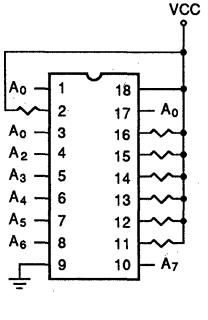
57C4013



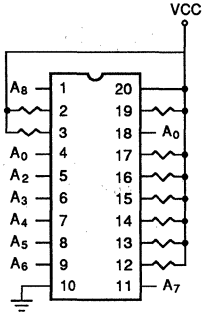
57C402



57C4023



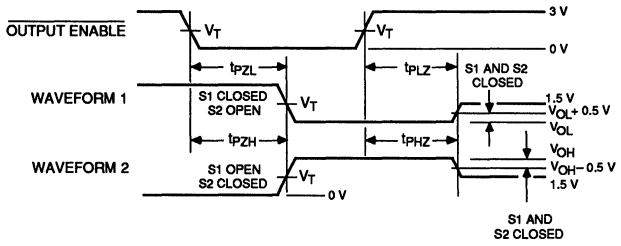
57C4033



$T_{ambient}$ = 125° C
V_{CC} = 5.25 ± 0.25 V
Square wave pulses on A0 to A8 are:

1. 50% ± 15% duty cycle
2. Logic "0" = –1 V to 0.7 V
3. Logic "1" = 2.4 V to V_{CC}
4. Frequency of each address is to be one-half of each preceding input, with A0 beginning at 100 kHZ.
   e.g., A0 = 100 kHz
   A1 = 50 kHz ± 10%
   A2 = 25 kHz ± 10%
   An = 1/2 An–1 ± 10%

505 109



Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

505 171

Figure A. Enable and Disable (57C4013/23/33 Only)

Functional Description

Data Input

The FIFO consists of a dual-port RAM and two ring counters for read and write. After power-up, the Master Reset should be pulsed LOW, which internally resets both the read and write counters. When the Input Ready (IR) is HIGH, the FIFO is ready to accept DATA from the D_x inputs. Data then present at the inputs is written into the first location of the RAM when Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. When the SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. The write pointer now points to the next location in the RAM. If the memory is full, then IR will remain LOW.

Data Output

Data is read from the O_x outputs. Just after the first shift-in, the first data word is available at the outputs, which is indicated by the Output Ready (OR) going HIGH. When the OR is HIGH, data may be shifted out by bringing the Shift-Out (SO) HIGH. A HIGH signal at SO causes the read pointer to point to the next location in the RAM, and also the OR to go LOW. Valid data is maintained while the SO is HIGH. When the SO is brought LOW, the OR goes HIGH, indicating the presence of new valid data. If the FIFO is emptied, OR stays LOW, and O_x remains as before, (i.e., data does not change if the FIFO is empty). A dual port RAM inside the chip provides the capability of simultaneous and asynchronous writes (Shift-Ins) and reads (Shift-outs).

AC Test and High-Speed App. Notes

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 µF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In-Input Ready combination, as well as the Shift-Out-Output Ready combination, timing measurements may be misleading; i.e., rising edge of the Shift-In pulse is not recognized until input ready is HIGH. If Input Ready is not high due to (a) too high a frequency, or (b) FIFO being full or effected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (T_{IDH}) and the next activity of Input Ready (T_{IRL}) to be extended relative to Shift-In going HIGH. This same type of problem is also related to T_{IRH}, T_{ORL}, T_{ORH}, and the Status Flag timing as related to Shift-In and Shift-Out. For high-speed applications, proper grounding technique is essential.

HF and AF/AE Status Flags (57C4033 Only)

The Half-Full (HF) will be high only when the net balance of words shifted into the FIFO exceeds the number of words shifted out by thirty-two or more (i.e., when the FIFO contains thirty-two or more words). The Almost-Full/Empty (AF/AE) flag will be HIGH when the FIFO contains fifty-six or more words or when the FIFO contains eight or fewer words (see Figures 10, 11 and 12).

Care should be exercised in using the status flags because they are capable of producing arbitrarily short pulses. For example, if the FIFO contains thirty-one words, and SI and SO pulses are applied simultaneously, the HF flag may produce an arbitrarily short pulse, depending on the precise phase of SI and SO.

The flags will always settle to the correct state after the appropriate delay (e.g., T_{HFL}, T_{HFH} in this example). This property of the status flags will clearly be a function of dynamic relation between SI and SO. Generally, the use of level-sensitive, rather than edge-sensitive status detection circuits will alleviate this hazard.

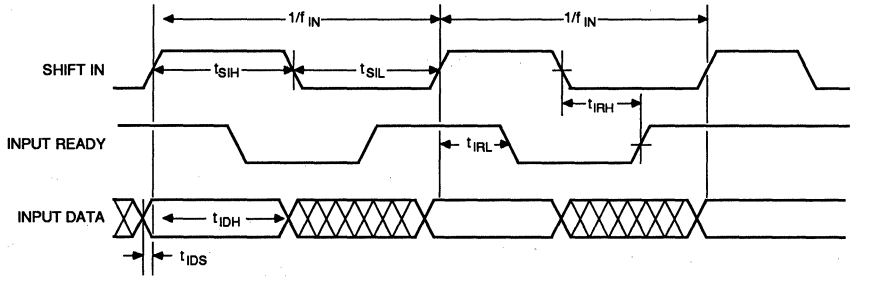
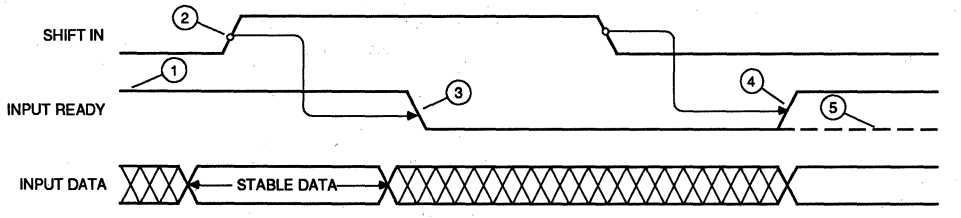


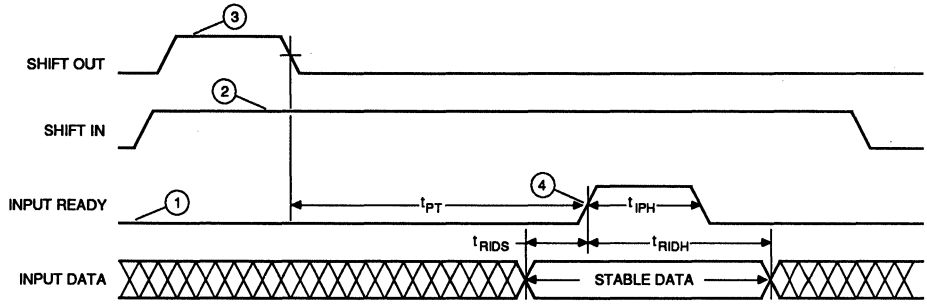
Figure 1. Input Timing



① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
② Input Data is loaded into the first available memory location.
③ Input Ready goes LOW indicating this memory location is full.
④ Shift-in going LOW allows input Ready to sense the status of the next memory location. The next memory location is empty as indicated by input Ready HIGH.
⑤ If the FIFO is already full then the input Ready remains low.
Note: Shift-in pulses applied while input Ready is LOW will be ignored.

505 116

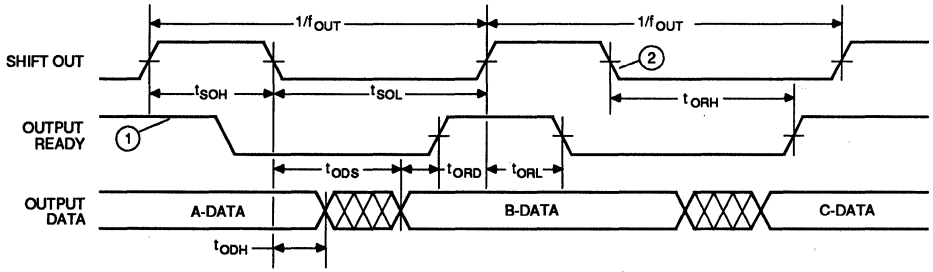
Figure 2. The Mechanism of Shifting Data Into the FIFO



① FIFO is initially full.
② Shift In is held HIGH.
③ Shift Out pulse is applied. An empty location is detected by the internal pointers on the falling edge of SO.
④ As soon as Input Ready becomes HIGH the Input Data is loaded into this location.

505 117

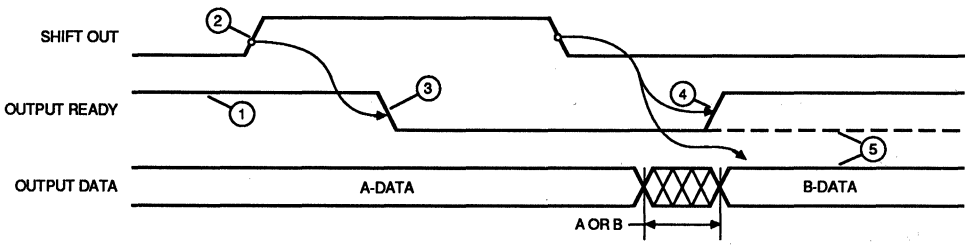
Figure 3. Data Is Shifted Whenever Shift In and Input Ready Are Both HIGH



① The diagram assumes that the FIFO contains at least three words: A-Data (first input word), B-Data (second input word), and C-Data (third input word).
② Output data changes on the falling edge of SO after a a valid Shift-Out Sequence, i.e., OR and SO ar both high together.

505 118

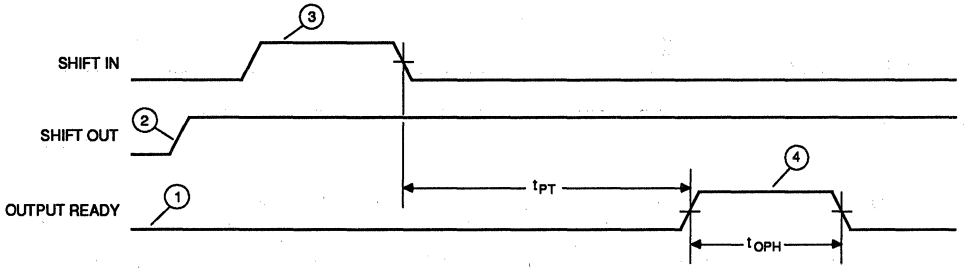
Figure 4. Output Timing



① Ouput Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
② Shift-Out goes HIGH causing B-Data (second input word) to advance to the output register. Output data remains as valid A-Data while Shift-Out is HIGH.
③ Output Ready goes LOW.
④ Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data remains the same (A-Data).

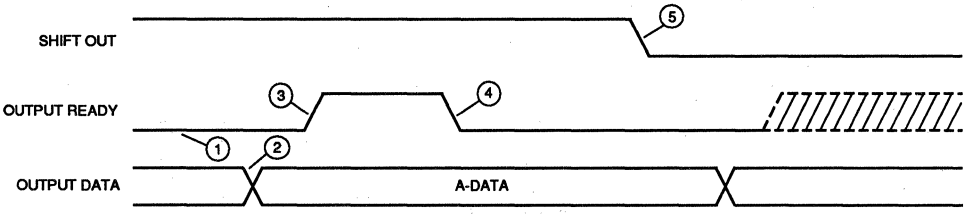
505 119

Figure 5. The Mechanism of Shifting Data Out of the FIFO



(1) FIFO is initially empty.
(2) Shift-Out is held HIGH.
(3) Shift-In pulse applied. A full location is detected by the internal pointers on the falling edge of Shift-In.
(4) As soon as Output Ready becomes HIGH, the word is shifted out.

Figure 6. t_{PT} and t_{OPH} Specification 505 120



(1) The internal logic does not detect the presence of any data n the FIFO.
(2) New data (A) arrives at the outputs.
(3) Output Ready goes HIGH indicating arrival of the new data.
(4) Since Shift Out is held HIGH, Output Ready goes immediately LOW.
(5) As soon as Shift Out goes LOW the Output Data is subject to change.
Output Ready will go HIGH or remain LOW depending on whether there are any additional upstream words in the FIFO.

Figure 7. Data Is Shifted Out Whenever Shift Out and Output Ready Are Both HIGH 505 121

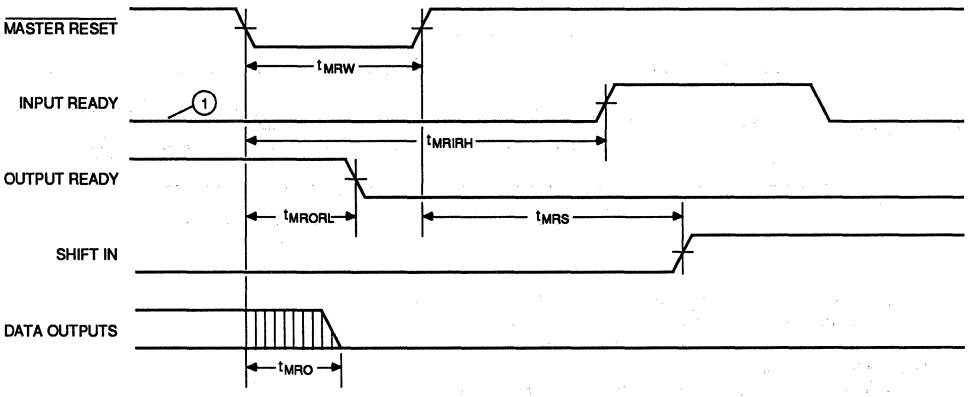
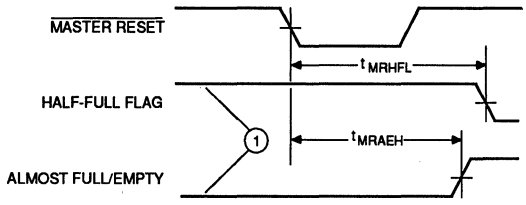
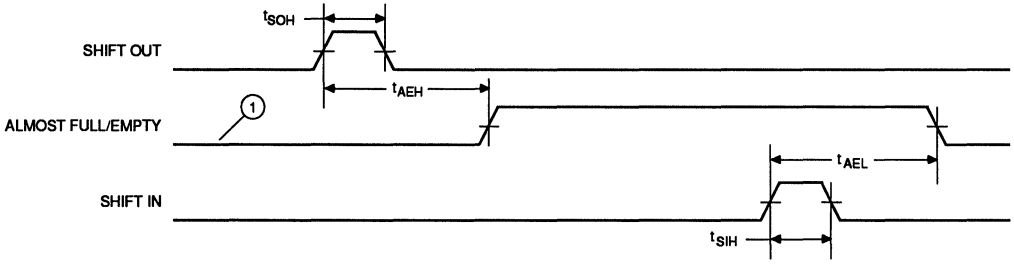


Figure 8. Master Reset Timing 505 122



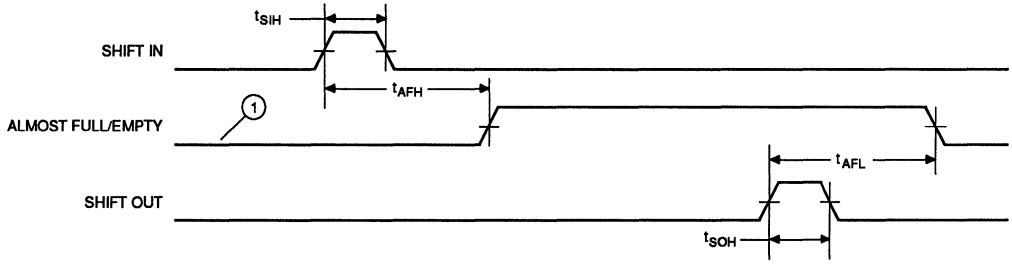
① FIFO initially has between 32 and 56 words.

505 123 **Figure 9. t_{MRHFL} and t_{MRAEH} Specifications**



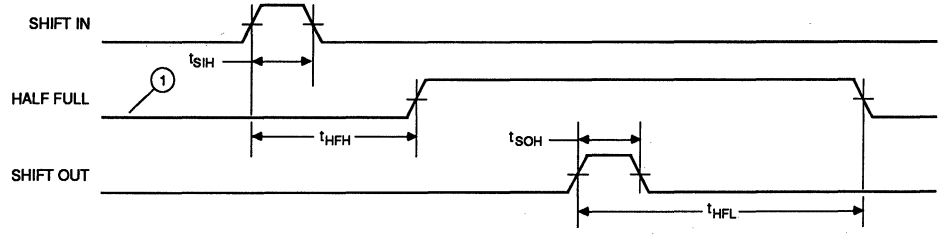
① FIFO contains 9 words (one more than almost empty).

505 124 **Figure 10. t_{AEH} and t_{AEL} Specifications**



① FIFO contains 55 words (one short of almost full).

505 125 **Figure 11. t_{AFH} and t_{AFL} Specifications**



① FIFO contains 31 words (one short of almost full).

505 126 **Figure 12. t_{HFL} and t_{HFH} Specifications**

57C4500-40/50/65/80

High Density First-in First-out (FIFO)
256x9 CMOS Memory

Advance Information

DISTINCTIVE CHARACTERISTICS

- **RAM based FIFO**
- **256x9 organization**
- **Cycle times of 50/65/80/100 nanoseconds**
- **Asynchronous and simultaneous writes and reads**
- **Low power consumption – 80 mA maximum**
- **Status flags – full, half-full, empty**
- **Retransmit capability**
- **Expandable in both width and depth**
- **Increased noise immunity for $\overline{XI}$ - CMOS threshold**
- **Functional and pin compatible with industry standard devices**

GENERAL DESCRIPTION

The 57C4500 is a RAM-based CMOS FIFO that is 256 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 20 MHz. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

High Density FIFOs such as the 57C4500 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the 57C4500 useful in communication, image processing, mass storage, DSP, and printing systems.

BLOCK DIAGRAM

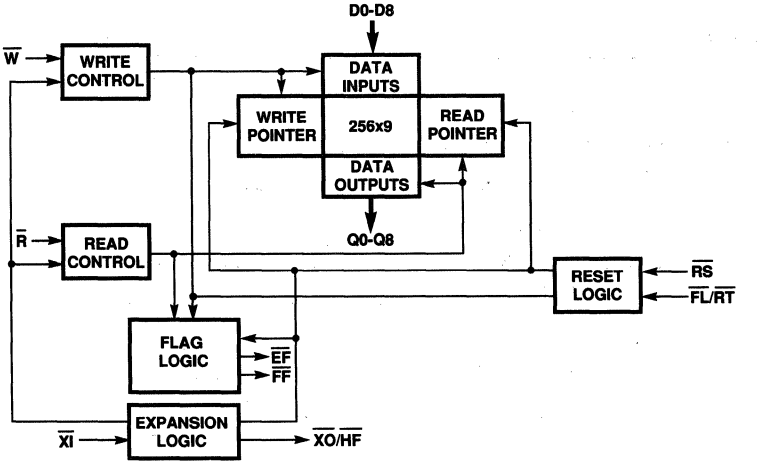
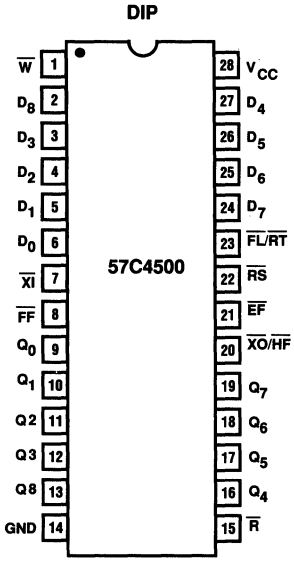


Figure 1.

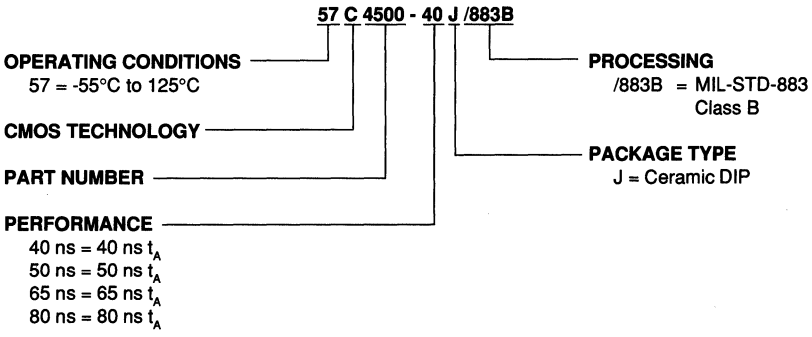
Publication # 10907 Rev. A Amendment /0
Issue Date: June 1988

CONNECTION DIAGRAMS



Pin Designations:
$\overline{W}$ = Write
$\overline{R}$ = Read
$\overline{RS}$ = Reset
$\overline{FL}/\overline{RT}$ = First Load/Retransmit
D_X = Data In
Q_X = Data Out
$\overline{XI}$ = Expansion In
$\overline{XO}/\overline{HF}$ = Expansion Out/Half-Full Flag
$\overline{FF}$ = Full Flag
$\overline{EF}$ = Empty Flag
V_{CC} = Supply Voltage
GND = Ground

ORDERING INFORMATION



ORDERING INFORMATION

Part Number	Description	Package	Temp
57C4500-40	256-word by 9-bit FIFO	J	Mil
57C4500-50			
57C4500-65			
57C4500-80			

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC} ..... -0.5 V to +7.0 V
Input voltage ..... -0.5 V to V_{CC} +0.5 V
Operating temperature ..... -55°C to +125°C
Storage temperature ..... -65°C to +150°C
Power dissipation ..... 2.0 W
DC output current ..... 50 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC CHARACTERISTICS Military: V_{CC} = 5 V ±10%, T_A = -55°C to +125°C

Parameter Symbol	Parameter Description	57C4500-40 T_A = 40 ns Min.	Max.	57C4500-50 T_A = 50 ns Min.	Max.	57C4500-65 T_A = 65 ns Min.	Max.	57C4500-80 T_A = 80 ns Min.	Max.	Unit
I_{IL}	Input Leakage Current (any input) (Note 1)	-1	1	-1	1	-1	1	-1	1	µA
I_{IO}	Output Leakage Current (data outputs) (Note 2)	-10	10	-10	10	-10	10	-10	10	µA
V_{IH}	Input High Voltage (all inputs except $\overline{XI}$) (Note 3)	2.0	–	2.0	–	2.0	–	2.0	–	V
V_{IL}	Input Low Voltage (all inputs except $\overline{XI}$) (Note 3)	–	0.8	–	0.8	–	0.8	–	0.8	V
V_{IHXI}	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	–	3.5	–	3.5	–	3.5	–	V
V_{ILXI}	Input Low Voltage, $\overline{XI}$ (Note 3)	–	1.5	–	1.5	–	1.5	–	1.5	V
V_{OH}	Output Logic "1" Voltage I_{OH} = -2 mA	2.4	–	2.4	–	2.4	–	2.4	–	V
V_{OL}	Output Logic "0" voltage I_{OL} = 8 mA	–	0.4	–	0.4	–	0.4	–	0.4	V
I_{CC1}	Average V_{CC} Power Supply Current (Note 4)	–	80	–	80	–	80	–	80	mA
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}) (Note 4)	–	25	–	25	–	25	–	25	mA
I_{CC3}	Power Down Current (all inputs = V_{CC} -0.2 V) (Note 4)	–	10	–	10	–	10	–	10	mA

Notes:
1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. These are absolute voltage levels with respect to the ground pins on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

AC CHARACTERISTICS V_{CC} = 5 V ±10%, T_A = -55°C to +125°C

Parameter Symbol	Parameter Description	57C4500-40 Min.	57C4500-40 Max.	57C4500-50 Min.	57C4500-50 Max.	57C4500-65 Min.	57C4500-65 Max.	57C4500-80 Min.	57C4500-80 Max.	Unit
Write and Flag Timing										
t_{WC}	Write Cycle Time	50		65		80		100		ns
t_{WPW}	Write Pulse Width	40		50		65		80		ns
t_{WR}	Write Recovery Time	10		15		15		20		ns
t_{DS}	Data Setup Time	25		30		30		40		ns
t_{DH}	Data Hold Time	0		5		10		10		ns
t_{WFF}	Write LOW to Full Flag LOW		35		45		60		60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW		50		65		80		100	ns
t_{WEF}	Write HIGH to Empty Flag HIGH		35		45		60		60	ns
t_{WLZ}	Write pulse HIGH to data bus at LOW Z (Note 1)	10		15		15		20		ns
Read and Flag Timing										
t_{RC}	Read Cycle Time	50		65		80		100		ns
t_A	Access Time		40		50		65		80	ns
t_{RR}	Read Recovery Time	10		15		15		20		ns
t_{RPW}	Read Pulse Width	40		50		65		80		ns
t_{RLZ}	Read pulse LOW to data bus at LOW Z (Note 1)	5		10		10		10		ns
t_{DV}	Data Valid from read pulse HIGH	5		5		5		5		ns
t_{RHZ}	Read pulse HIGH to data bus at HIGH Z (Note 1)		25		30		30		30	ns
t_{RFF}	Read HIGH to Full Flag HIGH		35		45		60		60	ns
t_{RHF}	Read HIGH to Half Full-Flag HIGH		50		65		80		100	ns
t_{REF}	Read LOW to Empty Flag LOW		35		45		60		60	ns
Reset Timing										
t_{RSC}	Reset Cycle Time	50		65		80		100		ns
t_{RS}	Reset Pulse Width	40		50		65		80		ns
t_{RSS}	Reset Setup Time	40		50		65		80		ns
t_{RSR}	Reset Recovery Time	10		15		15		20		ns
t_{EFL}	Reset to Empty Flag LOW		50		65		80		100	ns
t_{HFH}	Reset to Half-Full Flag High		50		65		80		100	ns
t_{FFH}	Reset to Full Flag HIGH		50		65		80		100	ns
Retransmit Timing										
t_{RTC}	Retransmit Cycle Time	50		65		80		100		ns
t_{RT}	Retransmit Pulse Width	40		50		65		80		ns
t_{RTR}	Retransmit Recovery Time	10		15		15		20		ns

Note: 1. Characterized parameters.

57C4501-50/65/80

High Density First-in First-out (FIFO)
512x9 CMOS Memory

Advance Information

DISTINCTIVE CHARACTERISTICS

- **RAM based FIFO**
- **512x9 organization**
- **Cycle times of 65/80/100 nanoseconds**
- **Asynchronous and simultaneous writes and reads**
- **Low power consumption – 80 mA maximum**
- **Status flags – full, half-full, empty**
- **Retransmit capability**
- **Expandable in both width and depth**
- **Increased noise immunity for $\overline{XI}$ - CMOS threshold**
- **Functional and pin compatible with industry standard devices**

GENERAL DESCRIPTION

The 57C4501 is a RAM-based CMOS FIFO that is 512 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 15 MHz. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

High Density FIFOs such as the 57C4501 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the 57C4501 useful in communication, image processing, mass storage, DSP, and printing systems.

BLOCK DIAGRAM

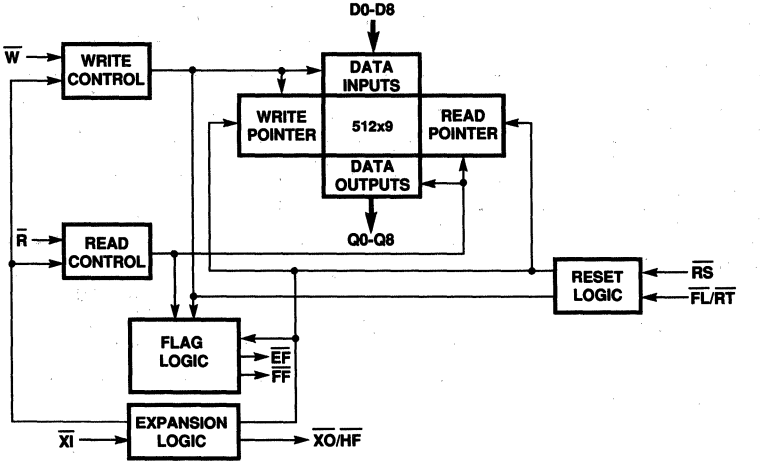
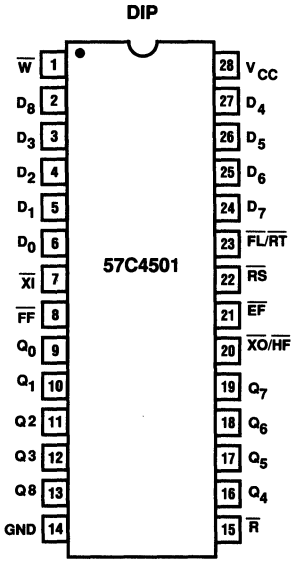


Figure 1.

Publication #	Rev.	Amendment
10908	A	/0

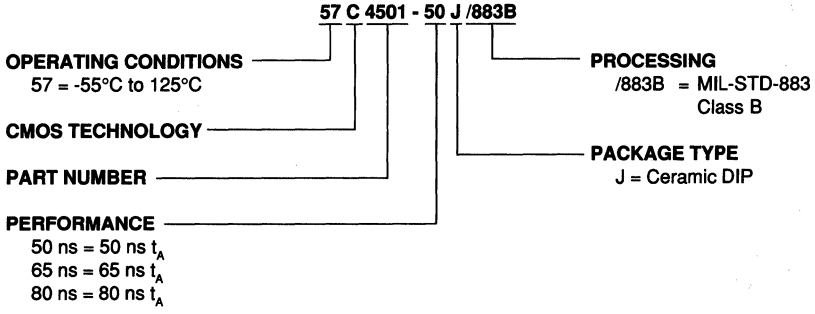
Issue Date: **June 1988**

CONNECTION DIAGRAMS



Pin Designations:
- $\overline{W}$ = Write
- $\overline{R}$ = Read
- $\overline{RS}$ = Reset
- $\overline{FL}/\overline{RT}$ = First Load/Retransmit
- D_X = Data In
- Q_X = Data Out
- $\overline{XI}$ = Expansion In
- $\overline{XO}/\overline{HF}$ = Expansion Out/Half-Full Flag
- $\overline{FF}$ = Full Flag
- $\overline{EF}$ = Empty Flag
- V_{CC} = Supply Voltage
- GND = Ground

ORDERING INFORMATION



ORDERING INFORMATION

Part Number	Description	Package	Temp
57C4501-50	512-word by 9-bit FIFO	J	Mil
57C4501-65			
57C4501-80			

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC} ..... -0.5 V to +7.0 V
Input voltage ..... -0.5 V to V_{CC} +0.5 V
Operating temperature ..... -55°C to +125°C
Storage temperature ..... -65°C to +150°C
Power dissipation ..... 2.0 W
DC output current ..... 50 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC CHARACTERISTICS Commercial: V_{CC} = 5 V ±10%, T_A = -55°C to +125°C

Symbol	Parameter	57C4501-50 T_A = 50 ns Min.	57C4501-50 T_A = 50 ns Max.	57C4501-65 T_A = 65 ns Min.	57C4501-65 T_A = 65 ns Max.	57C4501-80 T_A = 80 ns Min.	57C4501-80 T_A = 80 ns Max.	Unit
I_{IL}	Input Leakage Current (any input) (Note 1)	-1	1	-1	1	-1	1	µA
I_{IO}	Output Leakage Current (data outputs) (Note 2)	-10	10	-10	10	-10	10	µA
V_{IH}	Input High Voltage (all inputs except $\overline{XI}$) (Note 3)	2.0	–	2.0	–	2.0	–	V
V_{IL}	Input Low Voltage (all inputs except $\overline{XI}$) (Note 3)	–	0.8	–	0.8	–	0.8	V
V_{IHXI}	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	–	3.5	–	3.5	–	V
V_{ILXI}	Input Low Voltage, $\overline{XI}$ (Note 3)	–	1.5	–	1.5	–	1.5	V
V_{OH}	Output Logic "1" Voltage I_{OH} = -2 mA	2.4	–	2.4	–	2.4	–	V
V_{OL}	Output Logic "0" voltage I_{OL} = 8 mA	–	0.4	–	0.4	–	0.4	V
I_{CC1}	Average V_{CC} Power Supply Current (Note 4)	–	80	–	80	–	80	mA
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}) (Note 4)	–	25	–	25	–	25	mA
I_{CC3}	Power Down Current (all inputs = V_{CC} -0.2 V) (Note 4)	–	10	–	10	–	10	mA

Notes:
1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. These are absolute voltage levels with respect to the ground pins on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

AC CHARACTERISTICS V_{CC} = 5 V ±10%, T_A = -55°C to +125°C

Symbol	Description	57C4501-50 Min.	57C4501-50 Max.	57C4501-65 Min.	57C4501-65 Max.	57C4501-80 Min.	57C4501-80 Max.	Unit
Write and Flag Timing								
t_{WC}	Write Cycle Time	65		80		100		ns
t_{WPW}	Write Pulse Width	50		65		80		ns
t_{WR}	Write Recovery Time	15		15		20		ns
t_{DS}	Data Setup Time	30		30		40		ns
t_{DH}	Data Hold Time	5		10		10		ns
t_{WFF}	Write LOW to Full Flag LOW		45		60		60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW		65		80		100	ns
t_{WEF}	Write HIGH to Empty Flag HIGH		45		60		60	ns
t_{WLZ}	Write pulse HIGH to data bus at LOW Z (Note 1)	15		15		20		ns
Read and Flag Timing								
t_{RC}	Read Cycle Time	65		80		100		ns
t_A	Access Time		50		65		80	ns
t_{RR}	Read Recovery Time	15		15		20		ns
t_{RPW}	Read Pulse Width	50		65		80		ns
t_{RLZ}	Read pulse LOW to data bus at LOW Z (Note 1)	10		10		10		ns
t_{DV}	Data Valid from read pulse HIGH	5		5		5		ns
t_{RHZ}	Read pulse HIGH to data bus at HIGH Z (Note 1)		30		30		30	ns
t_{RFF}	Read HIGH to Full Flag HIGH		45		60		60	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH		65		80		100	ns
t_{REF}	Read LOW to Empty Flag LOW		45		60		60	ns
Reset Timing								
t_{RSC}	Reset Cycle Time	65		80		100		ns
t_{RS}	Reset Pulse Width	50		65		80		ns
t_{RSS}	Reset Setup Time	50		65		80		ns
t_{RSR}	Reset Recovery Time	15		15		20		ns
t_{EFL}	Reset to Empty Flag LOW		65		80		100	ns
t_{HFH}	Reset to Half-Full Flag High		65		80		100	ns
t_{FFH}	Reset to Full Flag HIGH		65		80		100	ns
Retransmit Timing								
t_{RTC}	Retransmit Cycle Time	65		80		100		ns
t_{RT}	Retransmit Pulse Width	50		65		80		ns
t_{RTR}	Retransmit Recovery Time	15		15		20		ns

Note: 1. Characterized parameters.

57C4502-50/65/80

High Density First-in First-out (FIFO)
1024x9 CMOS Memory

Advance Information

DISTINCTIVE CHARACTERISTICS

- **RAM based FIFO**
- **1024x9 organization**
- **Cycle times of 65/80/100 nanoseconds**
- **Asynchronous and simultaneous writes and reads**
- **Low power consumption – 80 mA maximum**
- **Status flags – full, half-full, empty**
- **Retransmit capability**
- **Expandable in both width and depth**
- **Increased noise immunity for $\overline{XI}$ - CMOS threshold**
- **Functional and pin compatible with industry standard devices**

GENERAL DESCRIPTION

The 57C4502 is a RAM-based CMOS FIFO that is 1024 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 15 MHz. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

High Density FIFOs such as the 57C4502 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the 57C4502 useful in communication, image processing, mass storage, DSP, and printing systems.

BLOCK DIAGRAM

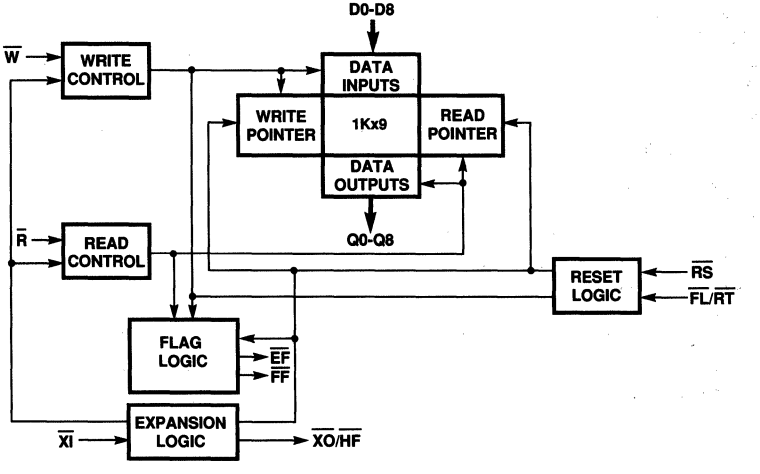
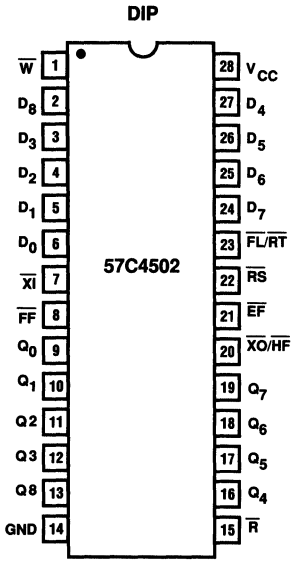


Figure 1.

Publication #	Rev.	Amendment
10909	A	/0

Issue Date: **June 1988**

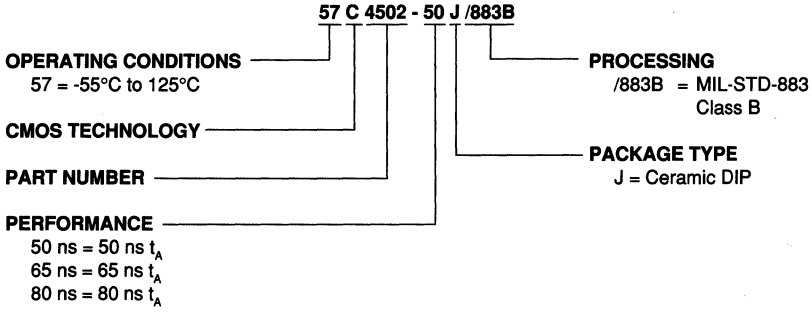
CONNECTION DIAGRAMS



Pin Designations:
- $\overline{W}$ = Write
- $\overline{R}$ = Read
- $\overline{RS}$ = Reset
- $\overline{FL}/\overline{RT}$ = First Load/Retransmit
- D_x = Data In
- Q_x = Data Out
- $\overline{XI}$ = Expansion In
- $\overline{XO}/\overline{HF}$ = Expansion Out/Half-Full Flag
- $\overline{FF}$ = Full Flag
- $\overline{EF}$ = Empty Flag
- V_{CC} = Supply Voltage
- GND = Ground

3

ORDERING INFORMATION



ORDERING INFORMATION

Part Number	Description	Package	Temp
57C4502-50	1024-word by 9-bit FIFO	J	Mil
57C4502-65			
57C4502-80			

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC} ..... -0.5 V to +7.0 V
Input voltage ..... -0.5 V to V_{CC} +0.5 V
Operating temperature ..... -55°C to +125°C
Storage temperature ..... -65°C to +150°C
Power dissipation ..... 2.0 W
DC output current ..... 50 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC CHARACTERISTICS Commercial: V_{CC} = 5 V ±10%, T_A = -55°C to +125°C

Symbol	Parameter	57C4502-50 T_A = 50 ns Min.	57C4502-50 T_A = 50 ns Max.	57C4502-65 T_A = 65 ns Min.	57C4502-65 T_A = 65 ns Max.	57C4502-80 T_A = 80 ns Min.	57C4502-80 T_A = 80 ns Max.	Unit
I_{IL}	Input Leakage Current (any input) (Note 1)	-1	1	-1	1	-1	1	µA
I_{IO}	Output Leakage Current (data outputs) (Note 2)	-10	10	-10	10	-10	10	µA
V_{IH}	Input High Voltage (all inputs except $\overline{XI}$) (Note 3)	2.0	–	2.0	–	2.0	–	V
V_{IL}	Input Low Voltage (all inputs except $\overline{XI}$) (Note 3)	–	0.8	–	0.8	–	0.8	V
V_{IHXI}	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	–	3.5	–	3.5	–	V
V_{ILXI}	Input Low Voltage, $\overline{XI}$ (Note 3)	–	1.5	–	1.5	–	1.5	V
V_{OH}	Output Logic "1" Voltage I_{OH} = -2 mA	2.4	–	2.4	–	2.4	–	V
V_{OL}	Output Logic "0" voltage I_{OL} = 8 mA	–	0.4	–	0.4	–	0.4	V
I_{CC1}	Average V_{CC} Power Supply Current (Note 4)	–	80	–	80	–	80	mA
I_{CC2}	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL/RT}$ = V_{IH}) (Note 4)	–	25	–	25	–	25	mA
I_{CC3}	Power Down Current (all inputs = V_{CC} -0.2 V) (Note 4)	–	10	–	10	–	10	mA

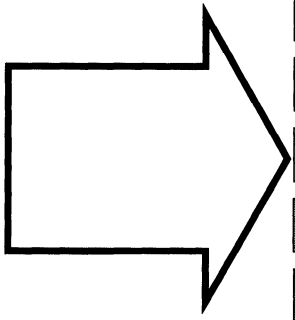
Notes: 1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. These are absolute voltage levels with respect to the ground pins on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

AC CHARACTERISTICS V_{CC} = 5 V ±10%, T_A = -55°C to +125°C

Symbol	Description	57C4502-50 Min.	57C4502-50 Max.	57C4502-65 Min.	57C4502-65 Max.	57C4502-80 Min.	57C4502-80 Max.	Unit
Write and Flag Timing								
t_{WC}	Write Cycle Time	65		80		100		ns
t_{WPW}	Write Pulse Width	50		65		80		ns
t_{WR}	Write Recovery Time	15		15		20		ns
t_{DS}	Data Setup Time	30		30		40		ns
t_{DH}	Data Hold Time	5		10		10		ns
t_{WFF}	Write LOW to Full Flag LOW		45		60		60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW		65		80		100	ns
t_{WEF}	Write HIGH to Empty Flag HIGH		45		60		60	ns
t_{WLZ}	Write pulse HIGH to data bus at LOW Z (Note 1)	15		15		20		ns
Read and Flag Timing								
t_{RC}	Read Cycle Time	65		80		100		ns
t_A	Access Time		50		65		80	ns
t_{RR}	Read Recovery Time	15		15		20		ns
t_{RPW}	Read Pulse Width	50		65		80		ns
t_{RLZ}	Read pulse LOW to data bus at LOW Z (Note 1)	10		10		10		ns
t_{DV}	Data Valid from read pulse HIGH	5		5		5		ns
t_{RHZ}	Read pulse HIGH to data bus at HIGH Z (Note 1)		30		30		30	ns
t_{RFF}	Read HIGH to Full Flag HIGH		45		60		60	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH		65		80		100	ns
t_{REF}	Read LOW to Empty Flag LOW		45		60		60	ns
Reset Timing								
t_{RSC}	Reset Cycle Time	65		80		100		ns
t_{RS}	Reset Pulse Width	50		65		80		ns
t_{RSS}	Reset Setup Time	50		65		80		ns
t_{RSR}	Reset Recovery Time	15		15		20		ns
t_{EFL}	Reset to Empty Flag LOW		65		80		100	ns
t_{HFH}	Reset to Half-Full Flag High		65		80		100	ns
t_{FFH}	Reset to Full Flag HIGH		65		80		100	ns
Retransmit Timing								
t_{RTC}	Retransmit Cycle Time	65		80		100		ns
t_{RT}	Retransmit Pulse Width	50		65		80		ns
t_{RTR}	Retransmit Recovery Time	15		15		20		ns

Note: 1. Characterized parameters.

Advanced
Micro
Devices



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AN-112

FIFOs: Rubber-Band Memories to Hold Your System Together

Chuck Hastings

Data-rate matching problems are a very basic part of the life of a builder of digital systems. Today there are components called "FIFOs" which let you keep your hardware design simple, and let each portion of your system see the data rate which it wants to see, and yet let you avoid hobbling the performance of your software by constantly interrupting or intermittently halting your microprocessor. FIFO is one of those made-up words, or acronyms, formed from the initials of a phrase — in this case, "*F*irst-*I*n, *F*irst-*O*ut." FIFOs may be thought of as "elastic storage" devices — "logical rubber bands" between the different parts of your system, which stretch and go slack so that data rates between different subsystems do not need to match up on a short-term microsecond-by-microsecond basis, but only need to average out to be the same over a much longer period of time. This tutorial paper both describes what FIFOs are in general, and introduces the 64x4 and 64x5 Monolithic Memories' FIFOs in particular.

11113A
JULY 1988

FIFOs: Rubber-Band Memories to Hold Your System Together

Chuck Hastings

Introduction

Data-rate matching problems are a very basic part of the life of a builder of digital systems. Some important electromechanical devices such as disk drives produce or absorb data at totally inflexible rates governed by media recording densities and by the speeds at which small electric motors are naturally willing to rotate. Other devices such as letter-quality printers have maximum data rates beyond which they cannot be hurried up, and which are relatively slow compared to the rates of other devices in the system.

Microprocessors and their associated main memories are generally faster and more flexible than the other system components, but they often operate with severly degraded efficiency if they must be diverted from their main tasks every few milliseconds to handle data-ready interrupts for individual dribs and drabs of data. While "one day at a time" may be a sound principle by which to live your life, "one bit at a time" or even "one byte at a time" is not a philosophy by which to make your microprocessor live if you want the best possible service from it.

Today there are components called "FIFOs" which let you keep your hardware design simple, and let each portion of your system see the data rate which it wants to see, and yet let you avoid hobbling the performance of your software by constantly interrupting your microprocessor, or even by intermittently halting it in order to let DMA (Direct Memory Access) circuits take over control of the main memory for a short time. FIFOs may be thought of as "elastic storage" devices — "logical rubber bands" between the different parts of your system, which stretch and go slack so that data rates between different subsystems do not need to match up on a short-term microsecond-by-microsecond basis, but only need to average out to be the same over a much longer period of time.

This tutorial paper both describes what FIFOs are in general, and introduces the 64x4 and 64x5 Monolithic Memories FIFOs in particular.

What is a FIFO?

FIFO is one of those made-up words, or *acronyms,* formed from the initials of a phrase — in this case, "*F*irst-*I*n, *F*irst-*O*ut." Originally, the phrase "First-In, First-Out" came from the field of operations research, where it describes a *queue discipline* which may be applied to the processing of the elements of any *queue* or waiting line. There is also a LIFO, or "Last-In, First-Out" queue discipline. The terms FIFO and LIFO have also been used for many years by accountants to describe formal procedures for allocating the costs of items withdrawn from an inventory, where these items have been bought over a period of time at varying prices.

You can probably think of some simple, everyday objects which in some manner behave according to the FIFO queue discipline. For instance, little two-seater cable-drawn boats are drawn through an amusement park tunnel of love one by one, and must emerge from the other end in the same order in which they entered the tunnel — "First-In, First-Out." The old-time coin dispensers used by the attendants at such amusement park features, or by city bus drivers, are "buffer storage" devices which handle coins in this same manner. (See Figure 1.)

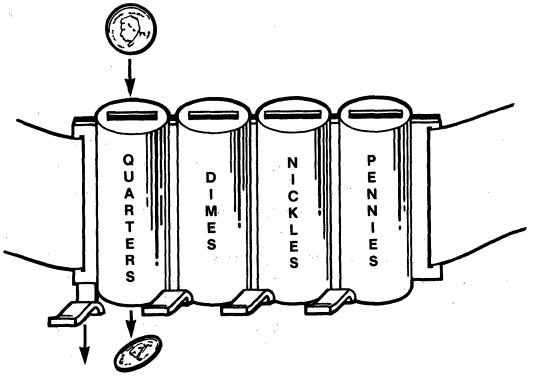


Figure 1. Primitive Mechanical FIFO Device

Notice also that the input of a coin into one of the tubes of such a coin dispenser through the slot at the top, and the output of a coin at the bottom of that tube when the lever for that tube is pushed, are completely independent events which do not have to be synchronized in any way, as long as the tube is neither totally empty nor totally full. However, if the tube fills up completely, a coin inserted into the slot will not go into the tube. Likewise, if the tube empties out completely, no coin is released from the tube at the bottom when the lever is pressed. The coin tube thus behaves as an *asynchronous* FIFO. Keep this homely example in mind.

In computer technology, both the FIFO queue discipline and the LIFO queue discipline are frequently used to control the insertion and withdrawal of information from a buffer memory, or from a dedicated buffer region of some larger memory. In input/output programming practice, a FIFO memory region is sometimes referred to as a *circular buffer,* and in programming for computer-controlled telephone systems it is called a *hopper.* A LIFO memory region is usually referred to as a *stack.*

Both FIFO and LIFO memories have frequently been implemented as special-purpose digital systems or subsystems, but as of the present time only FIFO memories are commonly implemented as individual, self-contained semiconductor devices.

Representative FIFOs

To give you the flavor of what these semiconductor devices are like, I'll describe the type 67401 64x4 FIFO and type 67402 64x5 FIFO which have been available for several years from Monolithic Memories. ("64x4" here means containing 64 words of 4 bits each.) These parts have a basic, easy-to-understand architecture and control philosophy. They also happen to be the fastest FIFOs available through normal commercial channels as of this writing, and they are in widespread use for applications ranging from microcomputers up to IBM-lookalike mainframes and large special-purpose military radar processors. A 67401 is internally organized as follows:

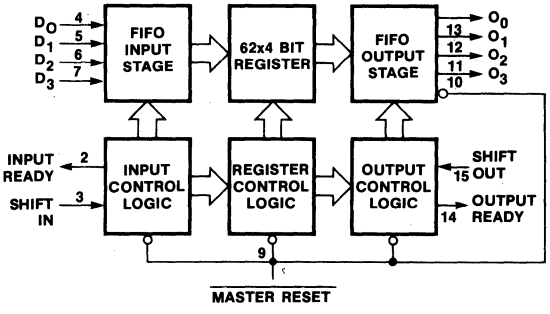
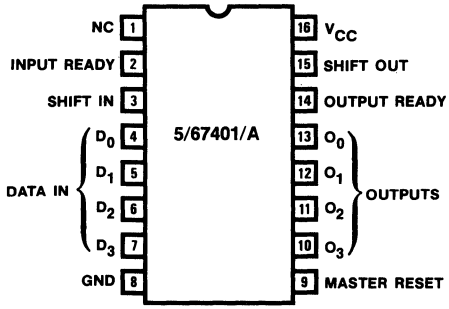


Figure 2. Architecture of the 67401 FIFO

The list of signals/pins for the 67401 is:

TYPE	HOW MANY	(CUM.)	I/O/V
Data In	4	4	I
Output	4	8	O
Control:			
Shift In	1	9	I
Shift Out	1	10	I
Master Reset	1	11	I
Status:			
Input Ready	1	12	O
Output Ready	1	13	O
Not Connected	1	14	—
Voltage:			
V_{CC} (+5V)	1	15	V
Ground	1	16	V

The corresponding list for the 67402 differs only in that there are 5 Data In lines rather than 4, and 5 Output lines rather than 4. The reason that there is an unused pin is that the 67401 was originally designed as a faster bipolar upgrade of a MOS part, the Fairchild 3341, which needs a second power-supply voltage (-12V) as well as V_{CC}. Much of the description to be given here of the 67401 also applies to the 3341, except for date rate — the 67401 can operate at 5 to 35 MHz depending on the exact version, compared with approximately 1 MHz for the 3341. Pinouts are:



(Note: "NC" pin is -12V for 3341.)

Figure 3. 67401/3341 Pinout

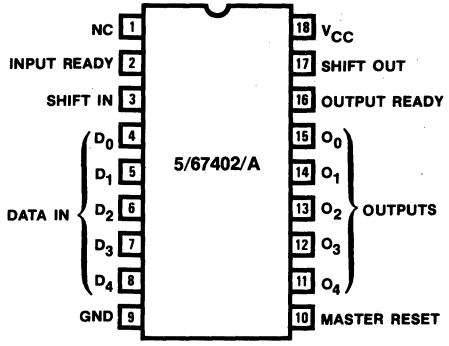
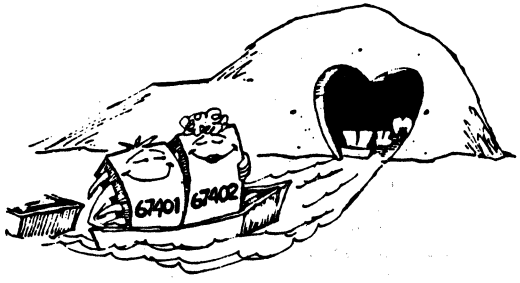


Figure 4. 67402 Pinout



"'FIRST-IN, FIRST-OUT' ... DESCRIBES A QUEUE DISCIPLINE WHICH MAY BE APPLIED TO THE PROCESSING OF THE ELEMENTS OF ANY QUEUE ..."

The reason for having a 5-bit model as well as a 4-bit model of basically the same part is that if two 4-bit FIFOs are placed side-by-side they make only an 8-bit FIFO, and many people have FIFO applications which entail using a parity bit with each byte, and/or a frame-marker bit with the last byte of a frame or block, which means that they want 9-bit or 10-bit FIFOs. A 67402 next to a 67401 makes a 9-bit FIFO, and two 67402s make a 10-bit FIFO. But I'm getting ahead of myself.

A logic HIGH signal on the Input Ready line indicates that there is at least one vacant memory location within the FIFO into which a new data word may be inserted. Likewise, a logic HIGH on the Output Ready line indicates that there is at least one data word currently stored within the FIFO and available for reading at the outputs. The operation of the FIFO is such that, once a data word has been inserted at the Data In lines (the *top* of the FIFO, as it were), this word automatically *sinks all the way to the bottom* (assuming that the FIFO was previously empty) and forthwith appears at the Output lines. (Remember the synonym *hopper?*) In keeping with the FIFO queue discipline, the first word which was inserted is the first one available at the outputs, and additional words may be withdrawn *only* in the order in which they were originally inserted.

There is no provision for *random access* in these FIFOs, since their internal implementation uses one particular variation of shift-register technology. Each FIFO word consists of 4 (for the 67401) or 5 (for the 67402) data bits, plus a control or "presence" bit which indicates whether or not the word contains significant information. There are thus 4 or 5 data "tracks" and one presence "track" if you look at a FIFO *from a magnetic-tape* perspective. What the Master Reset input does is to clear all of the bits in the presence track, and in addition to clear the very last data word (at the "bottom") which controls the Output lines. The other 63 data words are not cleared, but it doesn't really matter; their status is like unto that of operating-system files whose Directory entries have been deleted, in that they can no longer be read out and will get written over as soon as new information comes in.

We now return to what happens when a new data word gets inserted at the "top" of the FIFO. A mark (call it a "one") is made in the presence bit for word 00, the first word. Assume now that word 01 is vacant, so that there is a "zero" in its presence bit. The internal logic of the FIFO then operates so that the data from word 00 is automatically written into word 01, the presence bit for word 01 is automatically set to "one," and the presence bit for word 00 is automatically reset to "zero." If word 02 is likewise vacant, the process gets repeated, and so forth until the same piece of data has settled into the lowest *vacant* word in the FIFO — the next lower word, and all the rest, have "ones" in their presence bits, blocking further changes.

Conversely, now assume that at the moment no data word is being input, but that one has just been output. Then the bottom word in the FIFO — word 63 — has a "zero" in its presence bit, but there are a number of other words above it which have "ones" in their presence bits. The data in word 62 then moves into word 63 in the same manner described above, and the data in word 61 moves into word 62, and so forth, until there is no longer any word in the FIFO having a "one" in its presence bit which is above a word having a "zero" in its presence bit. The effect is that of empty locations bubbling up to the top of the FIFO. Or, in case you are one of those elite individuals who has been exposed to the concepts and jargon of modern semiconductor theory, you may prefer to think of the FIFO operation as one in which data ("electrons") flow from the top of the FIFO to the bottom, and vacancies ("holes") flow from the bottom of the FIFO to the top. In the general case, of course, new data words are being input at the top and old ones are being output at the bottom at random times, and there is a dynamic and continually changing situation within the FIFO as the new data words drop towards the bottom and the vacancies bubble up towards the top, and they intermix along the way.

An obvious consequence of this manner of operation in shift-register-technology FIFOs is that it takes quite a bit longer for a data word to pass all the way through the FIFO than the minimum time between successive input or output operations. There are various versions of the 67401 and 67402, rated at 5, 7, 10, 15, 167 or 35 MHz over commercial (0° C to +75° C) or military (-55° C to +125° C) temperature ranges. Thus, for instance, a 15-MHz FIFO can input data words at the top and/or output data words at the bottom at a sustained rate of a word every 66-2/3 nanoseconds. However, the "fall-through time" t_{PT} for these same FIFOs is stated in the data sheet as 1.6 microseconds, which is a long enough time for 24 words to be input or 24 words to be output! There is in principle also a "bubble-through" time for a single vacancy to travel from word 63 all the way back to word 00, which should be identical to t_{PT}, and probably is although as *measured* on a semiconductor tester it may differ by as much as 50 nanoseconds, which is probably due to artifacts of measurement. By the way, the stated operating frequencies and the t_{PT} value are "worst-case" (guaranteed) numbers; the "typical" values observed in actual parts are necessarily somewhat better, since semiconductor manufacturers are obliged to take any parts back which customers can prove do not meet the worst-case numbers, and some margin of safety is always nice (see reference 1).

Besides Monolithic Memories, other manufacturers of high-speed FIFOs include Fairchild Semiconductor, Mostek, National Semiconductor, RCA, Texas Instruments and TRW LSI Products Slow MOS FIFOs are available from Advanced Micro Devices, Fairchild Semiconductor, Texas Instruments, Western Digital and Zilog, and FIFOs in development or available at just about all of these vendors also offer new bells and whistles which I haven't discussed, such as three-state outputs, serial (one-bit-at-a-time) as well a parallel data ports, and additional status flags. TRW's new FIFO, for instance, has a "half-full" flag which tells when half of the FIFO's words contain data. Monolithic Memories now has the 67413 FIFO which supplies not only this flag, but also a second flag which indicates that the FIFO is either "almost full" (within eight words of full) or "almost empty" (within eight words of empty, reminiscent of the "yellow warning interrupt" in Digital Equipment Corporation PDP-11 computers. This "almost-full/empty flag" can be used as an interrupt to a microprocessor to indicate that *some* action must be taken, and the microprocessor can then examine the "half-full flag" to see what it actually has to do.

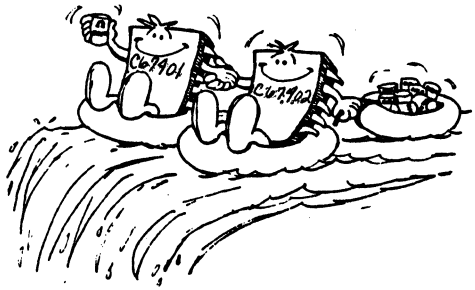
There are also other design approaches to the insides of a FIFO besides the one based on shift-register technology which has been described here. For instance, a FIFO may be organized as a random-access memory ("RAM") with two counters capable of addressing the RAM right within the chip, an "in-pointer" and an "out-pointer." The counting sequences, of course, "wrap

around" from the highest RAM address back to zero. The out-pointer chases the in-pointer, the region just traversed by the in-pointer but not yet by the out-pointer contains significant data, and the complementary region is logically "empty." This approach involves good news and bad news: the good news is that the long fall-through time goes away, but the bad news is that now reading and writing typically interfere with each other — unless the RAM is "two-port," they cannot be done simultaneously at all. Also, since this approach is more costly in "silicon area" than the shift-register approach, it would not result in as large FIFO capacities for the same size die or the same power consumption. In practice, this approach has only been used for MOS FIFOs which have turned out to be quite slow.

Another design approach is somewhat intermediate between the pure RAM approach as just described and the shift-register approach. It uses "ring counters" on the chip instead of full-blown binary counters. What this means in practice is that there are now *two* extra "tracks" along with the data tracks within the FIFO, plus also an input data bus and an output data bus. Single "one" bits move along the in-pointer track and the out-pointer track, and the out-pointer chases the in-pointer as before. The RAM is effectively two-port, and the two parallel buses both go to each and every word. Texas Instruments has announced some small (16x4) bipolar FIFOs based on this technical approach. Like the pure RAM approach, it gets rid of the fall-through time but needs proportionally more silicon area to store a given number of bits.

Designing with FIFOs

Returning now to the Monolithic Memories 67401 and 67402, if what you *really* need is a "deeper" FIFO, say 128x4 instead of just 64x4, these parts are designed to *cascade* using a simple "handshaking" procedure, without any external logic at all! If FIFO B follows FIFO A in the cascading sequence, the Shift In control input of FIFO B is connected to the Output Ready status output of FIFO A, and likewise the Shift Out control input of FIFO A is connected to the Input Ready status output of FIFO B, and the Master Reset control inputs are all tied together. (See Figure 5.) That's all there is to it. Any number of FIFOs may be cascaded in this manner.



"...THE MONOLITHIC MEMORIES 67401 AND 67402...ARE DESIGNED TO CASCADE USING A SIMPLE "HANDSHAKING" PROCEDURE..."

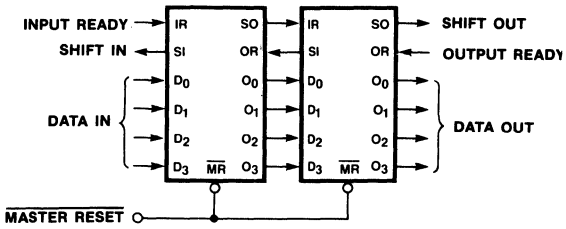


Figure 5. Cascading FIFOs to Form 128x4 FIFO

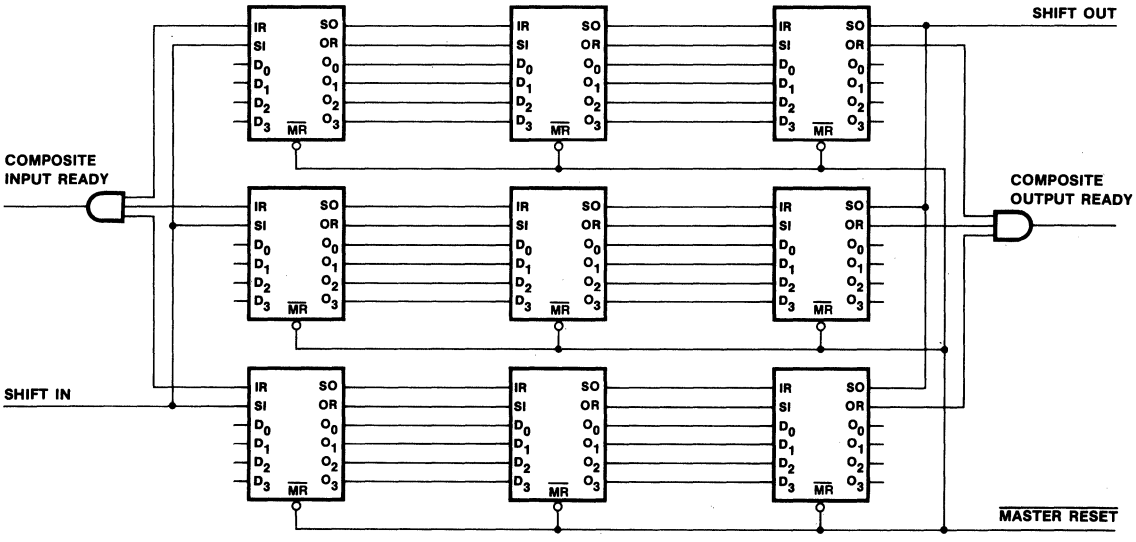
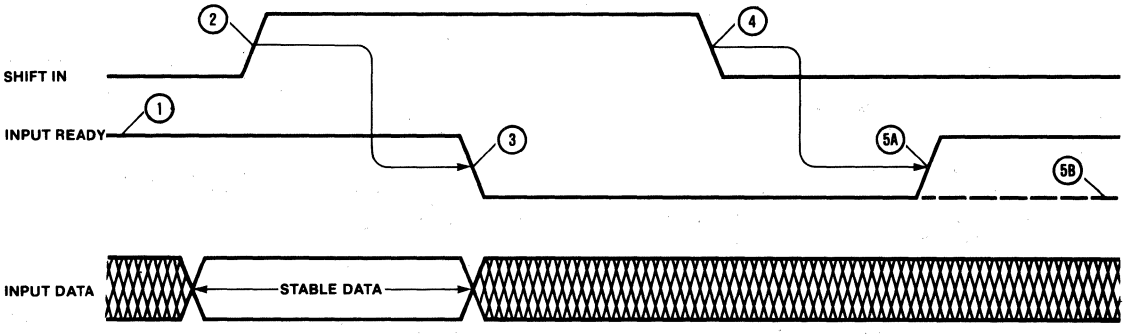


Figure 6. 192x12 FIFO

If what you *really* need is a "wider" FIFO, then you simply arrange 64x4 or 64x5 FIFOs side-by-side up to the required width. Then, you use an external AND gate such as a 74S08 or 74S11 to AND the Input Ready signals of the first rank of FIFOs if there is more than one rank, or of the only rank of FIFOs if there isn't. (See Figure 6.) Likewise, a similar AND gate is also needed to AND the Output Ready signals of the last rank of FIFOs. If you didn't provide these AND gates and just took the Input Ready signal of one FIFO as representative of when the whole array was ready, you would be taking the rather large gamble that you had correctly chosen the slowest row in this array — and if you chose wrong, 4-bit or 5-bit chunks of your input word might not get read correctly into the FIFO where they were supposed to go. Ditto on the output side. So like use the AND gates.

Although a humungous number of 67401s and 67402s are in use worldwide giving hassle-free service, it should be kept in mind that these devices are *asynchronous sequential circuits.* (One definition of "asynchronous sequential circuit" is "a fortuitous collection of race conditions," but that definition is unduly sardonic for very carefully designed parts such as these.) If your board is subject to noise, or if certain data sheet setup-time and hold-time conditions are occasionally not met, errors may occur. It is prudent system-design practice to every so often allow an array of FIFOs to empty out completely, and then issue a Master Reset. (I'm assuming, of course, to start with that you're not the kind of turkey who has to be *told* to issue a Master Reset as part of your power-up sequence.) In the event that you still get what appear to be occasional errors, very small (say from 22 to 68 picofarads) capacitors from both the Shift In control input and the Shift Out input of a FIFO to ground will often eliminate these. But by all means start with a *good* circuit board — these are high-speed-Schottky-technology circuits, and like to see a lot of ground-plane metal on the board, along with other reputable interconnection practices such as 0.1-microfarad disk capacitors between V_{CC} and ground for each chip to bypass switching noise.



(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied.

(2) Input Data is loaded into the first word.

(3) Input Ready goes LOW indicating the first word is full.

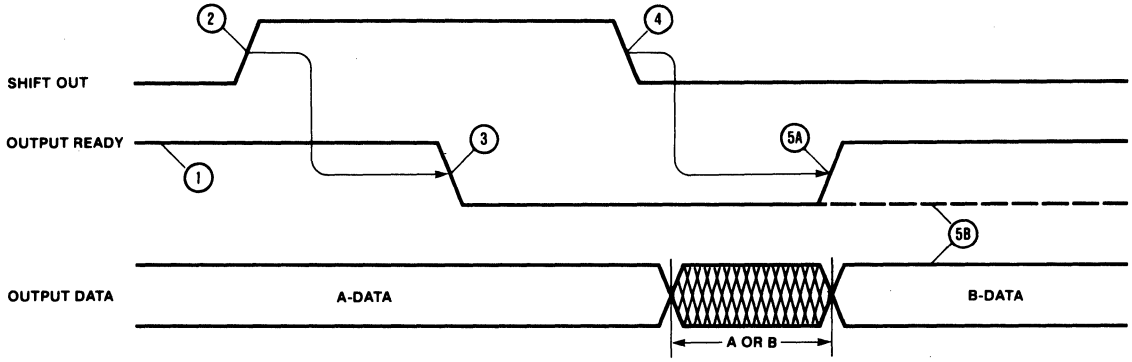
(4) The Data from the first word is released for "fall-through" to second word.

(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

Figure 7. Sequence of Events When a Data Word is Shifted into a FIFO

The sequence of events which occurs during the operation of shifting a new data word into the "top" of a FIFO is shown in Figure 7, and the corresponding sequence of events for shifting out the bottom word is shown in Figure 8. In both of these figures, it has been assumed that the external logic — whether it be the rest of your system, or just another FIFO — refrains from raising the respective Shift line to HIGH until the respective Ready line has gone HIGH, if the Shift line is raised any earlier, it simply gets ignored.



(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

(2) Shift Out goes HIGH causing the next step.

(3) Output Ready goes LOW.

(4) Contents of word 62 (B-DATA) are released for "fall through" to word 63.

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

Figure 8. Sequence of Events When a Data Word is Shifted Out of a FIFO.

When two FIFOs are cascaded as shown in Figure 5, the sequences of events shown in Figures 7 and 8 are subject to the additional ground rule that the Output Ready line of the FIFO on the left in Figure 5 (call it "FIFO A") is identically the Shift In line of the FIFO on the right (call it "FIFO B"). And likewise, the Input Ready line of FIFO B is identically the Shift Out line of FIFO A. In the terminology we have been using, FIFO A is the "upper" FIFO and FIFO B is the "lower" FIFO. Although you do not normally need to be concerned about what happens when two FIFOs are hooked together for cascaded operation in this manner, since the "handshake" occurs quite automatically without the rest of your logic having to do anything to make it happen, it is an illuminating exercise to consider Figures 7 and 8 together in this light and see why the cascading works.

In the general case, both FIFO A and FIFO B are neither completely full nor completely empty. Thus, from the description already given of FIFO internal operation, after some period of time there will be a significant piece of data in word 63 or FIFO A and a "one" in the presence bit for that word. Since the word-63 presence bit is what controls the Output Ready signal, the latter will at some point in time go HIGH, and at that same point in time the data word in FIFO A word 63 is present at the output lines. Likewise, after some period of time there will be a vacancy in word 00 of FIFO B, and a "zero" in the presence bit for that word which in turn results in the Input Ready signal going HIGH. Remembering now that each of these Ready signals is in fact the respectively-opposite Shift signal for the other FIFO, it may be seen from Figure 7 that the conditions for inputting a word into FIFO B have now been met, and from Figure 8 that the conditions for outputting a word from FIFO A and allowing the next available piece of data from somewhere further "up" in FIFO A to enter FIFO A word 63 have also been met. The time delays shown in both Figure 7 and Figure 8 from the event at 2 to the event at 3, and from the event at 4 to the event at 5A, are asynchronous internal-logic-determined times of the order of 4 or 5 gate delays, where the gates in question are high-speed-Schottky LSI *internal* gates and have significantly less propagation delay than the SSI gates you can read about in data sheets.

After a single data word has made it across the interface from FIFO A into FIFO B, each FIFO from then on behaves in accordance with the operating rules already described, with the exact sequence of events depending on the rate at which new data words are input into FIFO A and the rate at which old data words are withdrawn from FIFO B. The net effect is that the combination of FIFO A and FIFO B with this hookup behaves almost exactly like a single integrated 128x4 FIFO. In fact, the "handshake" timing/control sequence for getting a data word from FIFO A across FIFO B is almost a replica of that which occurs within each FIFO, when the internal logic associated with word n interfaces with that associated with word n+1 for the purpose of allowing a data word to advance from occupying word n to filling a vacancy in word n+1.

Returning now to applying the timing analysis shown in Figures 7 and 8 to the case of FIFO A and FIFO B operating in cascaded mode, notice that each movement (rising or falling) of the Ready signal for one FIFO is activated by the movement in the opposite sense (falling or rising, that is) for the Ready signal from the other part. The two signals, ORA/SIB (meaning "Output Ready A" which is the same signal as "Shift In B") and IRB/SOA, cannot both remain HIGH at the same time for more than a few nanoseconds, since if they are both HIGH a data word will pass between the two FIFOs as already described. So, at the point

when *both* the sequence of events shown in Figure 7 and the sequence of events shown in Figure 8 have been completed, and consequently ORA/SIB and IRB/SOA have both gone HIGH again, another similar sequence of events occurs for both FIFOs and another word is passed, and so forth. This process continues apace until either ORA/SIB sticks LOW, which can happen if FIFO A gets completely emptied out of data words and has "zeroes" everywhere in its presence track; or until IRB/SOA sticks LOW, which can likewise happen if FIFO B gets completely filled and has "ones" everywhere in its presence track. When such a deadlock situation occurs, it lasts until a new data word has been input into FIFO A and has had time to "fall all the way through" and settle into FIFO A word 63, or until the data word in word 63 of FIFO B has been read out and the resulting vacancy has had time to "bubble all the way back up" into FIFO B word 00, as the case may be.

Various Uses for FIFOs

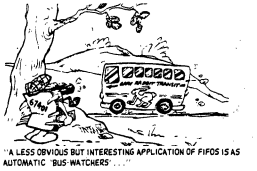
The classical FIFO application, as already mentioned at the beginning of this paper, is that of matching the instantaneous data rates of two digital systems in a simple, economical way. One of the two systems may, for reasons of design economics or even of utter necessity, want to emit or absorb data words in ultra-high-speed bursts, whereas the other one may prefer to operate at a slow-but-steady data rate or even at an erratic rate which varies between ultra-slow and slow or even between slow and fast. No matter — it's all the same to an asynchronous FIFO such as the 67401 or 67402, as long as the input rate and the output rate do match up over a long period of time so that it neither fills up nor empties out.

There are, however, some additional uses for FIFOs which arise from other, rather different circumstances. For instance, your digital system may simply need some extra buffer storage scattered around locally at different points on your block diagram, and you and your system may really just not care whether this storage is accessed on a random or on a queue basis. Under these circumstances, it is ordinarily less hassle to use a FIFO than to use a small RAM and come up with some extra logic to generate addresses and timing signals for it. Often the FIFO modus operandi is in fact the natural one for the application; as for instance when your system must accumulate a block of 64 characters and then run them by all at once in order to examine them for the presence of some control character, using some scanning logic — or perhaps even a microprocessor — which is otherwise occupied most of the time.

A less obvious but interesting application of FIFOs is as automatic "bus-watchers" for jump-history recording for hardware or even software diagnostic purposes. A FIFO whose inputs are connected to a minicomputer's program counter or microprogram counter, or to a microcomputer's main address bus, may be operated so as to record every new jump address generated by the program. This way, if at some point the hardware freaks out or the operating system crashes, a record exists of the last 64 jumps which were taken before the system was halted, assuming of course that you have provided some way for the system to sense that all is not well and halt itself. Such a record of jumps can be very valuable in tracing out what happened just before everything went haywire. FIFOs may be used in this way either as part of built-in self-monitoring features in digital systems, or as part of various kinds of external test equipment.

FIFOs may also be used as controllable delay elements for digital information which cannot be used immediately upon receipt — perhaps it must be matched against other information which is not yet available, or perhaps it must be synchronized with other streams of information which are out of phase by a varying amount. An example of the latter situation is deskewing several bit-streams off a parallel-format magnetic tape, which commonly has to be done when high recording densities are used. One FIFO *per bit-stream* is required — but the net resulting logic may still be the most reliable and economical way to get the job done, when compared with other possible digital designs. Another example is that of using FIFOs as data memories in digital correlators; the lag in an autocorrelation operation can be set simply by controlling how many words are in the FIFO at one time, and so forth. There are even some applications in which it is advantageous to operate a FIFO with all of its input and output cycles synchronized, so that absolutely all it does is to delay the data by some certain number of clock intervals.

References (2), (3), and (4) are formal applications notes available from Monolithic Memories, which discuss FIFOs from different viewpoints than this paper has taken. Each of them presents a more detailed explanation of one or more applications than there has been room for here. Reference (2) is mainly an overall applications survey, reference (3) emphasizes digital communications, and reference (4) emphasizes digital spectrum analyzers and also includes an overview of digital signal processing in general.



"A LESS OBVIOUS BUT INTERESTING APPLICATION OF FIFOS IS AS AUTOMATIC 'BUS-WATCHERS'..."

References

1. *Bipolar LSI 1982 Databook,* Monolithic Memories Inc.
2. "First In First Out Memories... Operations and Applications," applications note published March 1978 by Monolithic Memories Inc. A good survey with some thought-provoking ideas. I have to mention one error, however; one circuit diagram shows paralleled FIFO operation in the manner of that of Figure 6 in this paper, but without the use of the AND gates for the composite Ready signals. As I already warned you, that's *dangerous.*
3. "Understanding FIFO's," applications note published by Monolithic Memories Inc. The author, Alan Weisberger, has also had a modified version of this note published as a magazine article, "FIFOs Eliminate the Delay when Data Rates Differ," in *Electronic Design,* November 27, 1981. Despite the general title, the emphasis is on digital communications applications.
4. "PROMs, PALs, FIFOs and Multipliers Team Up to Implement Single-Board High-Performance Audio Spectrum Analyzer," applications note published by Monolithic Memories Inc. The author, Richard Wm. Blasco, also had this note published in *Electronic Design* in two installments, in the issues of August 20 and September 3, 1981 under the titles "PAL Shrinks Audio Spectrum Analyzer" and "PAL Improves Spectrum Analyzer Performance" respectively.

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FIFO RAM Controller Tackles Deep Data Buffering

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11111A
JULY 1988

FIFO RAM controller tackles deep data buffering

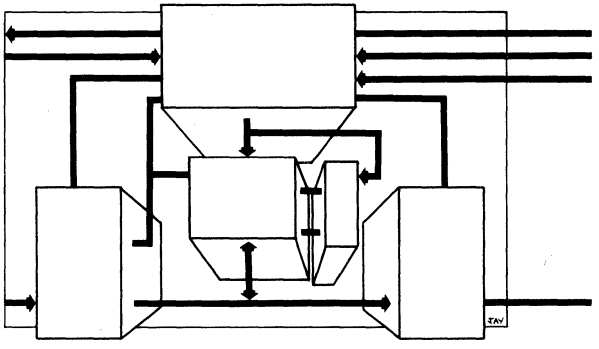
Buffering large amounts of data has long been a source of design headaches. Extra large FIFO buffers minimize system bottlenecks with an implementation as easy as it is cost-effective.

Designers are turning to innovative architectures to extend the performance of computer systems. Pipelining is one of these innovations. In pipeline architectures, data is buffered temporarily between a system's processing elements. This allows these processing elements to work more efficiently. Since data transfers can occur asynchronously, designers can minimize bottlenecks in data paths and boost overall performance.

Data buffering, however, is sometimes difficult and costly to implement. In multiprocessing and data communications applications, for example, designers encounter the problem of how to buffer large blocks of sequential data temporarily with minimum cost and trouble. Often, a few thousand to tens of thousands of words must be buffered.

In multiprocessing applications, large blocks of data and instructions are passed between the various processors. Storing information between the processors for a short time lets a sender pass data on without waiting for a receiver to finish its current task, so the sender can more quickly move on to its next task.

For data communications applications, large blocks of data must be transferred from one node to another along a data channel. Temporary buffering on and off the data channel permits each



device in the network to work more efficiently. Data can be transferred to the buffer when ready, and the device is free to move on to the next task without waiting for the data channel to be free.

Buffering large amounts of data, often called deep data buffering, can be accomplished through several methods. One technique, direct memory access (DMA), sets aside blocks of main memory as temporary data buffers. When a request for data transfer is received, the DMA controller interrupts the processor and takes control of the memory bus. The controller then moves the data into memory that has been allocated for temporary buffering.

Looking at the advantages of this buffering method, DMA controller chips are relatively inexpensive. Since they require little extra logic, the controllers are simple to implement. The DMA approach, however, has several drawbacks. First, the processor is interrupted every time a data block

Tom Pai

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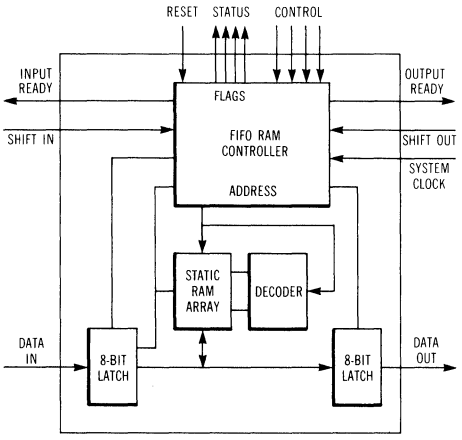


A FIFO RAM controller provides addressing, control and arbitration. In the 674219 buffer, only handshaking, status flags and buffer control lines are visible to the rest of the system.

transfer request is made. To transfer data, the processor must hand over control of the memory bus. When many data block transfers occur, system performance is severely degraded. Large blocks of data degrade performance even more.

DMA also limits rates and formats of data. Using this technique, the maximum data rate is limited to the system bus data rate. Bursts of rapid data can't be directly accommodated. Besides, DMA operation is synchronous with system operation, which means that all data transfers—both input and output—must be synchronous with the system clock. Asynchronous data can't be directly accommodated. Another drawback of DMA is that it doesn't allow for simultaneous input and output operation. This greatly limits the ability of a DMA buffer to act as a pipelining element.

The DMA approach is best suited for systems in which low cost is a top priority, and performance degradation, caused by interruptions to processors during the transfer of data, is tolerable. In effect, designers opting for DMA trade overall system performance, considerations about the rate and format of data and immediate access to information for inexpensive implementation and simple design.

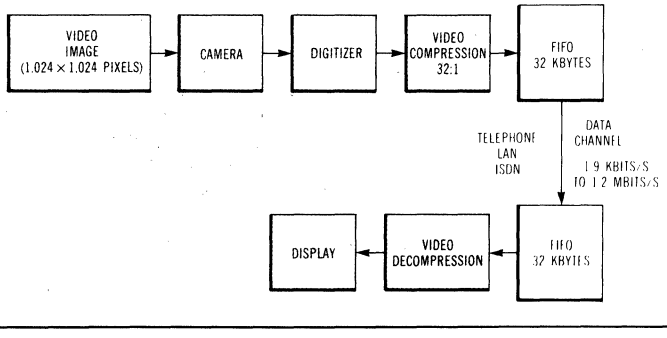
RAM approach eases bottlenecks

Another approach to deep data buffering involves dual-port RAM devices. A dual-port RAM is placed along the data transfer path and acts as temporary storage for incoming or outgoing data. These devices overcome many of the limitations of DMA. Thanks to two independent ports, data transfers can be completely asynchronous and simultaneous. Since one port can be isolated from the data bus, processors don't have to hand over control of the memory bus during data transfer.

Using dual-port RAMs for data buffering does have its disadvantages; to work as a data buffer, it requires a lot of external and control logic. Counters, comparators and control logic must be added to make the dual-port RAM read and write data sequentially and prevent buffer overflows and underflows from occurring. This external logic can add up to large amounts of valuable board real estate and limits the data rate of the buffer.

Another disadvantage is cost. Dual-port RAMs are 10 times the price of comparable conventional static RAMs; a 1-k × 8-bit device costs $25 to $30. Implementing a 4-k × 16-bit buffer will cost approximately $200 for the RAM device alone.

A third method of buffering data uses first-in, first-out buffers between elements as temporary storage sites. These FIFO devices store and output the data sequentially. Like dual-port RAMs, they



In a video teleconferencing system, a video image with a resolution of 1,024 × 1,024 pixels will generate 1 Mbyte of data per image. After a compression of 32:1, there are 32 kbytes of compressed data for each image. For optimal system performance, the data is passed to a FIFO buffer to wait for transmission along the data channel. The system is then free to begin processing the next image.

have two independent asynchronous ports. But one port is dedicated to input, the other to output.

FIFO buffers offer an extremely efficient approach for data buffering. Virtually no external control is required since control and arbitration is performed with on-chip logic. Addressing is eliminated because data is sequential. The streamlined buffering afforded by FIFOs maximizes the data rate, which makes this approach a natural for high-performance systems.

For maximum data rate and design ease, FIFO buffers offer advantages over DMA and dual-port RAM methods. But the devices are geared for data buffering of shallow-to-medium depth. Large data blocks are buffered only by using an array of FIFOs, which requires large amounts of board space, making FIFO buffers too expensive and inefficient for applications with large data amounts.

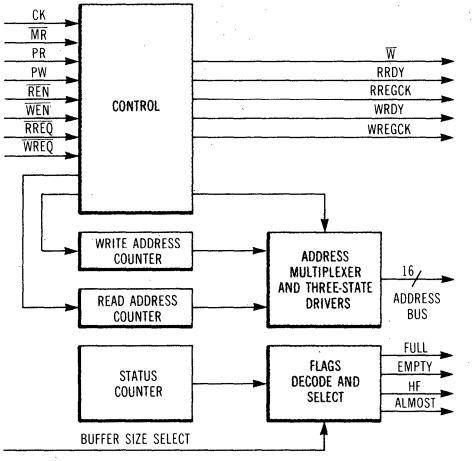
FIFO RAM controllers tackle deep data

When deep buffering is required, very large FIFO RAM buffers reduce the costs and space problems of conventional FIFO techniques. Devices such as the 674219 FIFO RAM controller from Monolithic Memories (Santa Clara, CA) can accommodate large amounts of data in high-performance systems. These devices provide the addressing, control and arbitration logic that enables an array of RAMs to function as a FIFO buffer.

One advantage of this kind of device is the large amount of data it can handle. Using inexpensive single-port static RAMs (or dynamic RAMs with additional external logic), designers can implement a fast, fully asynchronous buffer that can temporarily store from 512 to 65,536 words. In the case of the 674219 FIFO RAM controller, a performance of 12 MHz can be attained. During simultaneous input and output operation, a data rate of 6 MHz is possible.

With two registers for data latching, a few logic gates and a RAM array, these devices can replace any system function block calling for large data buffers. All of the control, arbitration and status logic is placed on a single device, greatly simplifying large FIFO buffer designs. Information about the buffer is provided by four status flags: full, empty, half-full and almost-full/almost-empty. The full and empty flags buffer overflow and underflow. When the buffer is full, attempts to write data into the buffer won't be acknowledged. Data already in the buffer, however, won't be lost. Similarly, the empty flag prevents false data from being read out.

Status flags also help increase the efficiency of buffers and optimize system performance. Together, the half-full and almost flags can indicate when the buffer is almost empty and trigger a signal to the source for more data. This ensures a steady stream of data to the receiver. In systems where a receiver, such as a peripheral, is operating at a much slower rate than the source, such as a processor, the processor can send data in high-speed bursts to the buffer and then attend to other tasks while a peripheral accepts the data in a steady, uninterrupted stream.



Two internal counters generate addresses for the RAM array to function in a first-in, first-out manner. A third counter in the FIFO RAM controller generates status information with four flags: full, empty, half-full and almost-full (16 word locations to full)/almost-empty (only 16 words remaining). This counter is programmed by buffer-size select inputs to provide the proper status information for the buffer.

Dual-pointer FIFO architecture

FIFO RAM controllers implement a RAM-based FIFO architecture, which uses two pointers. The write pointer contains the address of the next available location in the RAM array to be written and the read pointer has the address of the next location for data to be read. When either pointer is used to access the memory array, it's incremented automatically to point to the next available location. When the pointer reaches the last location, it's reset to zero and the procedure continues.

A third counter provides status information, generates flag logic and prevents overflow and underflow. The -size select inputs program this counter to give the proper status information to the buffer.

In the cycle of a typical system, the buffer is reset with the Master Reset (MR) pin. This sets the read and write pointers to zero and activates the empty flag. A write cycle is initiated by a Write Request (WREQ). The Write Ready (WRDY) line goes low, acknowledging the request. A Write Register Clock (WREGCK) pulse from the FIFO RAM controller latches the data into the write register. Data is then written to the RAM array at the address location provided by the write pointer. When the buffer has valid data, the empty flag will go low, indicating that a read can take place. The read cycle follows the same sequence as the write cycle.

Since a FIFO RAM controller uses low-cost, single-port RAMs, arbitration is needed to resolve simultaneous read and write requests. On-chip arbitration logic determines which request is serviced first. The second request is acknowledged, but will not be serviced until the first request is completed.

Conventional FIFO buffers are based on shift registers. Data is shifted from register to register to the top of the stack, and then to the output port. The time it takes for a word to move from the input port to the output port is called "fall-through," and it is dependent on the depth of the FIFO buffer.

By contrast, FIFO RAM controllers implement a RAM-based buffer. In this scheme, pointers are incremented as each read or write occurs. Since data doesn't physically move, fall-through time is eliminated. What's more, external control of the RAM array buffer is possible by disabling both the Write Enable (WEN) and the Read Enable (REN) to impose three states on the address lines from the FIFO RAM controller to the RAMs.

By reducing the cost and space requirements of FIFO buffering, FIFO RAM controllers offer systems designers an efficient and cost-effective method to buffer large amounts of data. Using these devices, designers can minimize system bottlenecks in data paths and processing elements and can boost overall system performance. **CD**

PAL Devices, PROMs, FIFOs, and Multipliers Team up to Implement Single-Board High-Performance Audio Spectrum Analyzer

This application note illustrates a high-performance audio spectrum analyzer. This circuit can analyze high fidelty audio signals with a resolution of 20 Hz and an input bandwidth of 20 kHz. It is useful in production test, performance evaluation, or adjustment of high-fidelity audio equipment. The analyzer provides a sweep generator output for rapid analysis of audio filter frequency response.

The design techniques used to implement the analyzer are quite general, and can be applied to a wide variety of DSP tasks. An understanding of the approach used will suggest solutions to a number of DSP problems. The architecture chosen for the spectrum analyzer is controlled by a microprogram stored in PROM. Many other applications can be accommodated by changing the microprogram. The high performance of this architecture provides an attractive price/performance alternative to other DSP approaches.

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AN-100

Introduction

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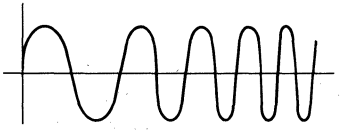
Spectrum Analyzer Functions

The spectrum analyzer requires many of the functions commonly used in DSP. Figure 1 shows the analyzer functions. An input signal is mixed with a swept audio sinewave oscillator (below).



Frequency Sweep

The frequency sweep acts as a sampler, starting from DC and increasing to its maximum frequency.

Mixing is accomplished by multiplying the input signal by the sinewave. From basic trigonometry:

$$\cos w_1 t \times \cos w_2 t = 1/2 \cos (w_1 + w_2)t + 1/2 \cos (w_1 - w_2)t \quad (1)$$

The mixing process generates two new sinewaves whose frequencies are the sum and difference of the input sinewave frequencies. When the sinewave oscillator matches the frequency of an input signal component, a DC term is generated in proportion to the amplitude of that component:

$$\cos w_1 t \times \cos w_1 t = \cos^2 w_1 t = \mathbf{1} + 2 \cos w_1 t$$

The DC term is extracted by a narrow lowpass filter. Due to the finite bandwidth of this lowpass filter, mixer output signals whose frequencies fall within the filter passband also appear at the filter output. As a result, the analyzer output will represent the energy contained in a range of frequencies, from the sinewave frequency minus the filter cutoff frequency, to the sinewave frequency plus the filter cutoff frequency. The effective bandwidth of the analyzer is twice the lowpass filter bandwidth.

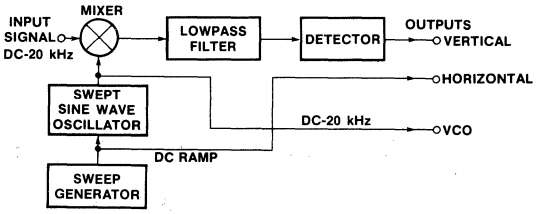


Figure 1. Spectrum Analyzer Functions

A detector converts the lowpass filter output to a DC voltage representing the total energy in the filter passband. If this DC voltage is plotted on a vertical axis with the sinewave oscillator frequency (represented by the sweep voltage) controlling the horizontal axis, a spectrum of the input signal results.

Other mixing schemes can be used to extract the spectrum. However, this "direct conversion" approach has two significant advantages. As shown in Figure 2, the swept oscillator output can be used to plot the frequency response of an audio filter. Other schemes require additional mixing to achieve the same results.

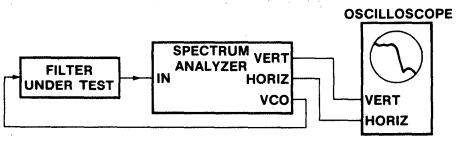


Figure 2. Filter Test Mode Setup

The direct conversion scheme confines the frequencies of all signals following the mixer to the lowpass filter bandwidth. Limiting the signal bandwidth has great benefit when the analyzer is implemented digitally. This benefit can be better understood with a brief review of DSP theory.

Digital Signal Processing Theory Review

Digital signal processing is accomplished by first converting the continuous analog input signal to a series of digital numbers. The digital numbers are then manipulated to perform the required signal processing. The processed digital numbers are then converted back to a continuous analog signal, completing the processing. The functions required for DSP are shown in Figure 3.

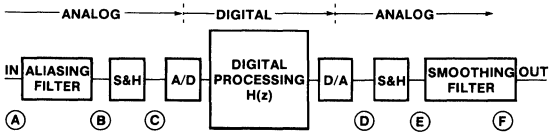


Figure 3. DSP Functions

Sampling

Representing a continuous input signal would require an infinite array of digital numbers. A finite collection of digital numbers can be obtained by considering the signal amplitude at discrete, periodic points in time. This process is called *sampling,* and is equivalent to multiplying the input signal by a periodic train of impulses of unit amplitude. The *sampling theorem* states that the input signal can be reconstructed without distortion if the input is bandlimited to contain no frequency components greater than half the sampling frequency. The sampling theorem means that the discrete samples completely represent the input signal, as long as the bandwidth constraint is met.

Aliasing

What is really happening during the sampling process? Consider the Fourier series representation of a periodic unit impulse train. It can be shown that:

$$f(t) = \sum_{k=-\infty}^{k=\infty} \cos(2\pi k f_s t),\ k = 0, 1, 2, 3, \ldots \qquad (2)$$

$$\text{where } f_s = \frac{1}{\text{sample period}}$$

The periodic impulse train is equivalent to a series of sinusoids consisting of all harmonics of the sampling frequency, including a DC term. Recalling Eq. (1) all possible sum and difference frequencies will be generated when the impluse train and the input signal are multiplied. This process is shown graphically in Figure 4. Observe that if the input contains frequencies greater than half the sampling frequency, the spectra in Figure 4 will overlap. This overlap phenomenon is known as *aliasing distortion,* and introduces noise in the signal.

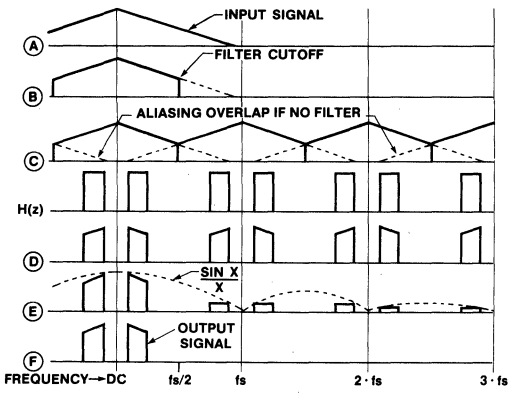


Figure 4. Aliasing Spectra of Figure 3 DSP Functions

Another consequence of the sampling process is that high-frequency signal components near a harmonic of the sampling frequency will be mixed to produce new signal components near DC. These new components have frequencies within the desired signal passband, but are really "alias" high-frequency components. The phenomenon is called *aliasing.*

To eliminate the undesirable effects of aliasing, a continuous analog lowpass filter is placed before the sampler. This *aliasing filter* removes frequency components beyond the $f_s/2$ limit.

Quantizing

The input samples are converted to a series of digital numbers by an analog-to-digital (A/D) converter. The A/D converter operates by *quantizing* the continuous sample amplitude into a finite number of amplitude ranges, and then assigning a digital number to represent the quantized amplitude value. As might be expected, this process introduces noise in the signal, known as *quantization distortion.* The quantization distortion is in the form of a "white" or broadband random noise, whose RMS amplitude is:

$$\sigma^2 = \frac{1}{12}2^{-2b} \qquad (3)$$

where b is the number of bits in the output digital word, excluding the sign bit

The effect of aliasing on quantization noise is to alias high frequency noise components to the DC to $f_s/2$ range. The resulting noise spectral density is equivalent to a white noise of amplitude σ^2, bandlimited to $f_s/2$.

Dynamic Range

The A/D output contains a finite number of bits. *Dynamic range* is defined as the ratio of the maximum-to-minimum signal amplitude that can be represented by the digital numbers. Dynamic range is determined by the number of bits in the digital numbers, and by the noise "floor."

For a digital number containing b bits plus a sign bit, the dynamic range would be:

$$\text{Dynamic range (dB)} = 10 \log_{10} 2^{-2b} \qquad (4)$$

The noise floor is the sum of all noise components that can appear at the DSP output. The primary noise factors are quantization noise and limit cycle noise (to be discussed shortly). Digital filtering will affect the noise floor by eliminating components of the noise signal. For example, the quantization noise at the DSP output is:

$$N_Q \text{ (dB)} = 10 \log_{10} \left[\sigma^2 \frac{BW}{f_s/2} \right] \qquad (5)$$

where BW is the net bandwidth of the digital filters

The noise components are uncorrelated, and are therefore combined by adding the power of each noise component. Remember that

$$\text{Power (absolute)} = \log_{10}{}^{-1} \left[\text{Power (dB)}/10 \right] \qquad (6)$$

The resulting dynamic range is:

$$\text{Dynamic range (dB)} = 10 \log_{10} \frac{0.5}{\Sigma \text{ Noise Power}} \quad (7)$$

where 0.5 = the maximum mean-squared amplitude

The overall dynamic range is the lesser of the result given by Eq. (4) or Eq. (7). In a practical system, the width of the digital numbers can vary. The dynamic range is usually calculated for all critical points in a digital system, with the overall dynamic range being the worst case value.

Digital Processing

The digital numbers from the A/D converter are manipulated to process the signal. Carrier generation, filtering, and nonlinear operations are performed by appropriate "number crunching".

Generation of sinusoidal carriers is easily accomplished using a linear ramp function (digital up/down counter) and converting the results to sinusoidal samples using ROM lookup tables. Alternately, recursive equations can produce the desired carriers.

Nonlinear operations on the digital numbers must be handled with care. Since aliasing is always present in the sampled domain, harmonics generated by nonlinear operations can alias to lower frequencies. The aliasing occurs "immediately," since it can be shown that performing a nonlinear operation in the sampled domain is equivalent to first performing the nonlinear operation on a continuous signal and then sampling the result without bandlimiting the sampler input.

The sampling rate can be changed to improve the efficiency of the digital processing. For example, discarding every other digital number would reduce the effective sampling rate by a factor of two. If the processing at the higher sample rate includes digital aliasing filters to remove components greater than half the lower sample rate, the requirements of the sampling theory are still met. The sampling rate can be increased by repeating digital sample values. This repetition is equivalent to a "sample and hold" operation, and modifies the signal spectrum by

$$F'(jw) = F(jw) \times \frac{\sin(wT/2)}{wT/2} \quad (8)$$

where $w = 2\pi \times \text{freq}$

T = input (longer) sample period

The effects of changing the sampling rate are best determined by plotting the resulting aliasing spectra.

Digital Filtering

Digital filtering is accomplished using multiplication, addition, and delay. For example, consider the biquadratic filter section in Figure 5. If z^{-1} is defined to be a unit sample period delay operator, then the input-to-output transfer function of the biquadratic section is:

$$H(z) = \frac{1 + a_1 z^{-1} + a_2 z^{-2}}{1 + b_1 z^{-1} + b_2 z^{-2}} \quad (9)$$

The biquadric sections can be cascaded to implement higher-order filters.

The Laplace transform of a unit delay is e^{-sT}, where T is the delay period. Remember that z^{-1} represents an inverse operator, so that $z \times z^{-1} = 1$. Thus,

$$z = e^{sT}, \text{ where } s = \alpha + jw \quad (10)$$

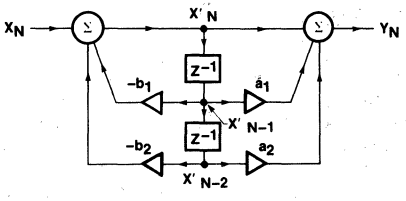


Figure 5. Digital Biquadratic Filter Section

Digital filter poles and zeroes (in the z-plane) can be mapped into the s-plane to determine the equivalent analog filter function, and vice-versa. The digital filter section of Eq. (9) corresponds to an analog biquadratic filter section with,

$$H(s) = \frac{s^2 + \alpha_o w_o s + w_o^2}{s^2 + \alpha_1 w_1 s + w_1^2} \quad (11)$$

However, the periodic nature of the e^{sT} function causes the digital filter passband to repeat periodically. The effect is the same as aliasing. The analog filter response is mixed with the sampling frequency harmonics to generate the true digital filter response.

Designing Digital Filters

How does one go about designing a digital filter? One approach is to perform a least mean squared error optimization using a computer. The desired function is specified, and the computer adjusts the a_n and b_n values until the desired response is achieved.

A second approach is to design an equivalent analog filter and then convert that design to a digital filter. This approach has great merit, since analog filter design theory is well developed. However, the digital passband will be distorted if the analog equivalent filter has significant response to frequencies greater than $f_s/2$. The aliased passbands overlap at that point.

To circumvent this problem, the analog filter function can be modified to compensate for the aliasing effects. The analog transfer response is modified using several transforms to compensate for aliasing. Unfortunately, the nature of the s-plane to z-plane mapping is such that no transform can compensate for all aliasing effects without introducing other forms of distortion.

The *standard (or impulse invariant) z-transform* represents a direct mapping to the z-plane. No frequency, amplitude, or phase distortion is introduced, but aliasing effects are not compensated. This transform should be used when the analog filter has negligible response to frequencies greater than $f_2/2$.

The *bilinear z-transform* preserves the filter amplitude response in the presence of aliasing. However, the bilinear transform introduces a distortion or *warping* of the frequency axis. As a result, only the filter cutoff frequency can be accurately transformed, using a *pre-warping* technique. Frequencies within the filter passband remain warped, introducing phase distortion in the digital filter response. The bilinear transform is used when the filter amplitude response is more critical than the phase response.

The *matched z-transform* preserves the filter phase response at the expense of amplitude response distortion. However, this amplitude distortion, unlike the aliasing distortion, can be corrected by placing additional zeroes in the transfer function. The matched transform is used when the filter phase response is critical, and either the amplitude response is not critical or the additional compensation zeroes can be accommodated.
Performing the transforms by hand is quite tedious. Fortunately, computer programs are widely available which handle the complete filter synthesis procedure, including z-transforms and pre-warping.

Limit Cycle Noise

An effect of using digital numbers with a finite number of bits is the generation of quantization noise. When implementing digital filters, the quantization noise introduces oscilaltions that are analogous to ringing in analog filters. These oscillations are called *limit cycles*. The limit cycle generates a noise which peaks at frequencies corresponding to the filter pole frequencies. The noise power is roughly proportional to pole Q. Limit cycle noise for a second order filter section of Equation (11) is given by:

$$N_L(\text{dB}) = 10 \log_{10}\left(\frac{2}{12} 2^{-2b} \frac{1+r^2}{1-r^2} \frac{1}{r^4 + 1 - 2r^2 \cos 2w}\right) \qquad (12)$$

where b = number of digital number bits (excluding sign bit)
pole freq. = w_1
pole Q = $1/\alpha_1$

$$w = 2\pi \frac{\text{pole freq.}}{f_s} \qquad r = \exp\left(\frac{-w}{2 \cdot \text{pole Q}}\right)$$

The limit cycle noise must be calculated for each complex pole pair, and adjusted to reflect the response of subsequent filter stages to the limit cycle frequency. Computer programs can calculate limit cycle noise power, including all of these considerations.

Output Signal Reconstruction

Once manipulation of the digital sample numbers is complete, the resulting digital numbers must be converted back to a continuous analog signal. Referring back to Fig. 3, a digital-to-analog (D/A) converter transforms the digital numbers to a series of analog output pulses.

A sample-and-hold (S&H) circuit eliminates transients that are introduced during the D/A conversion process. The spectrum of the S&H output is modifed as follows:

$$\text{S\&H } F'(jw) = F(jw)\frac{t}{T}\frac{\sin(wt/2)}{wt/2}$$

where t = hold time T = sample period

An output smoothing filter completes the reconstruction by removing all components with frequencies greater than $f_s/2$. The smoothing filter is often optional, depending on the importance of removing the high-frequency output components.

The spectral effects of reconstruction are shown in Figure 4.

Implementing the Spectrum Analyzer

The architecture used for the spectrum analyzer is shown in Fig. 6. Input signals are digitized and buffered with FIFOs before interface with a common 16-bit data bus. The 16-bit arithmetic unit (AU) provides multiply and accumulate operations. A 16-bit wide RAM stores intermediate results. A 16-bit temporary register facilitates z^{-1} delays and data movement. Outputs are provided using a D/A converter and S&H circuits.

The VCO output is buffered using FIFOs to provide a uniform high-speed sample rate. The VCO output is 12 bits wide, providing a signal-to-quantization noise ratio of 91 dB, using Equations (5) and (7). The calculation assumes a 500-Hz bandwidth. A smoothing filter at the VCO output is not necessary. The filter test configuration of Figure 2 allows the input aliasing filter to remove the effects of VCO high-frequency components, as long as the filter under test is a linear analog circuit.

The vertical and horizontal outputs are intended to interface an oscilloscope or X-Y plotter. The sampling of these outputs can be non-uniform, as long as the outputs track each other. The elastic storage at the input and VCO interfaces permits arbitrary non-uniform processing of the analyzer functions.

The 16-bit resolution of the internal data word provides 90-dB dynamic range according to Equation (4), or 115-dB dynamic range according to Equations (5) and (7), assuming 500-Hz bandwidth and no limit cycle noise and aliasing.

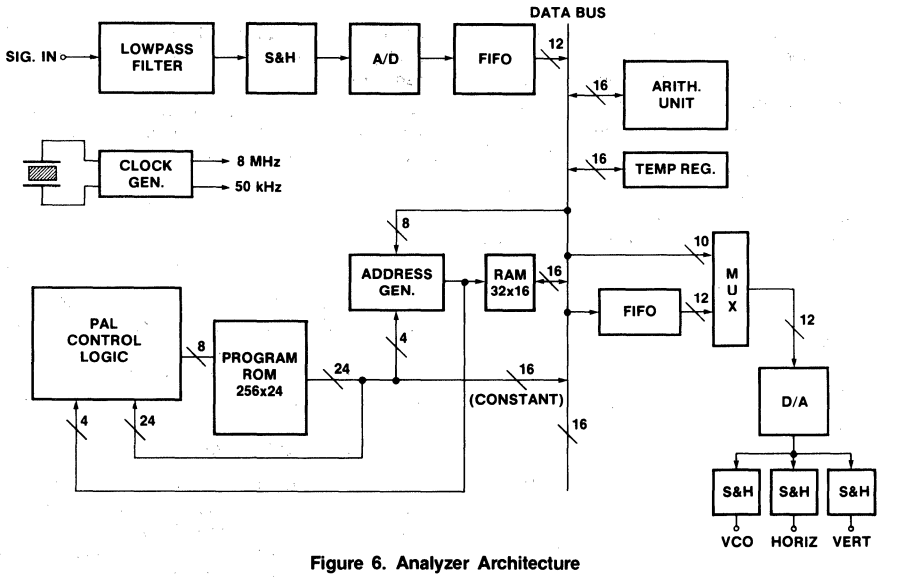


Figure 6. Analyzer Architecture

Microprogram control was selected for the analyzer. PAL devices can efficiently implement sequential state machines. It is possible to encode all control information in PAL devices, but only three packages would be saved (one PROM and two buffers). Distributing the control among several PAL devices would reduce flexibility and make corrections very difficult. The few extra packages required for microprogram control provide an extremely flexible architecture and greatly simplify the PAL device functions.

With the theoretical background and architecture in mind, the spectrum analyzer functions can be defined in detail. The objective is to realize a circuit capable of high-resolution analysis of audio signals in the DC to 20-kHz range. Selectable bandwidth and linear/logarithmic output display are highly desirable. Detailed functions are shown in Figure 7.

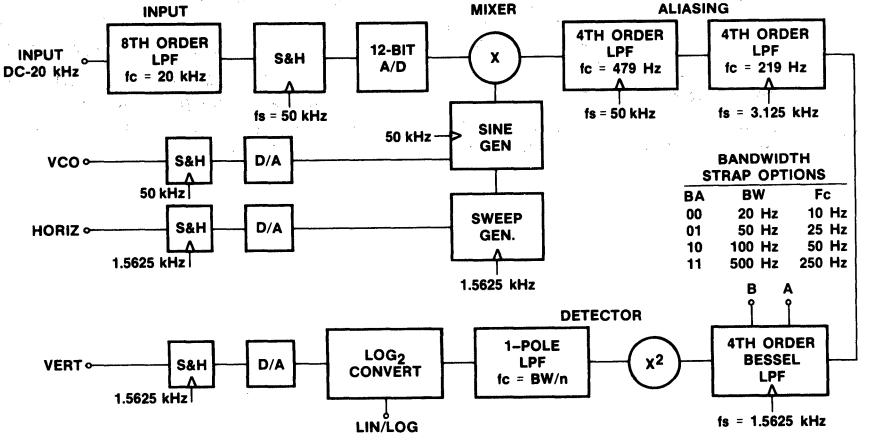


Figure 7. Detailed Functional Diagram

Input Aliasing Filter

An analog lowpass filter removes high-frequency components from the input signals. With a sample frequency of 50 kHz and a maximum input frequency of 20 kHz, the lowest aliasing frequency is (50-20) = 30 kHz.

An eighth-order Chebychev filter with 0.1-dB passband ripple will provide 44 dB of attenuation at 30 kHz, and 86 dB attenuation at 50 kHz. It is desirable to provide at least 60-dB overall dynamic range for high-performace analysis. To eliminate spurious responses above the -60-dB "floor," the input signal should have all components above 30 kHz suppressed by at least (60-44) = 16 dB. Most input signals will meet this requirement. If not, additional filtering must be provided.

S&H and A/D Converter

The input S&H maintains a constant sampled signal level while the A/D conversion is in progress. No sin X/X correction is made for this S&H since the net effect of the S&H plus A/D action is an impulse sample at the start of the "hold" period.

The A/D conversion time should be less than 16 μs. The A/D converter output digital number should "saturate" when the input signal exceeds the maximum level. The digital numbers should be in inverted two's complement form. The S&H acquisition time should be less than 4 μs.

For a full 60-dB overall dynamic range, a 12-bit A/D is required.

Mixer

The mixer multiplies the A/D output by the swept sinewave oscillator value. The multiplication produces sum and difference frequencies, according to equation (1).

Two's complement fractional arithmetic is used throughout the analyzer. Multiplication cannot overflow, since all numbers are less than 1 in magnitude.

Swept Sinusoidal Oscillator (VCO)

A precision swept sinusoid from DC to 20 kHz must be generated to mix with the input signal. A technique particularly well suited to this application is solving the two equations:

$$\sin(x+y) = \sin x \cos y + \cos x \sin y \qquad (13)$$

$$\cos(x+y) = \cos x \cos y - \sin x \sin y \qquad (14)$$

These two trigonometric identities generate a new sin and cos value with y representing the phase shift per sample period. The technique is a "CORDIC" algorithm, based on coordinate rotation. Exact results are produced, but truncation and round-off errors due to the finite digital word length can cause a slow change or "drift" of carrier amplitude. Fortunately, the swept sinusoid is periodically reset in the spectrum analyzer, arresting this amplitude drift.

The VCO frequency is swept by varying the value of y. However, since equations (13) and (14) require sin y and cos y, an identical CORDIC algorithm is used to obtain these values. To sweep the VCO, then, $\sin\Delta$ and $\cos\Delta$ are placed in RAM, selected by the bandwidth setting. These are two fixed numbers originally stored in PROM, and represent the frequency shift per sample time. Equations (13) and (14) are then applied to calculate sin y and cos y, which represent the desired phase shift per sample time. Equations (13) and (14) are executed again to generate the actual sinusoidal output.

The calculation of sin y and cos y can take place at a reduced sample rate to save processing time. Only the last execution of equations (13) and (14) must be performed at the full 50-kHz sample rate.

A linear ramp is generated to provide horizontal drive for an oscilloscope or X-Y plotter. The ramp is incremented each time the sin y and cos y values are updated, tracking the VCO sweep. When the ramp value overflows, the analyzer sweep cycle is re-initialized.

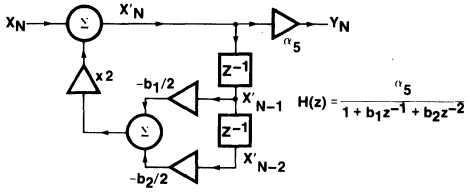


Figure 8. All-Pole Digital Filter Section

Digital Filters

Fig. 8 shows the implementation of the all-pole digital filter sections. Because of the low pole Q values in all filters, the second order sections can be simply cascaded to implement high-order filters. Fig. 8 shows a technique for handling coefficients greater than 1 with fractional number representation.

Scaling must be performed to ensure maximum dynamic range. Filter sections with high-Q poles will show peaking of signals near the pole frequencies. The input to such sections must be scaled down to prevent overflow of the arithmetic. For a second-order all-pole section, this peaking factor is exactly the Q of the poles. Thus, when a given second-order section has a pole Q of 2, the input signal to that section must be multiplied by 0.5 to prevent overflow. When the Q is less than or equal to 1, no scaling is performed.

Saturation arithmetic is not provided in this architecture. Careful scaling eliminates the need for saturation arithmetic, since the A/D will saturate at a precisely known value.

Aliasing Filters

Two 4th-order Chebyschev filters permit reduction of the sample rate following the mixer. Each filter provides 0.3 dB passband ripple and at least 68 dB attenuation of aliasing components. The slightly high passband ripple is acceptable, since subsequent filters will dominate the composite passband shape.

The first filter permits a sample rate reduction factor of 16. It is designed with a passband cutoff frequency of 479 Hz and a sample rate of 50 kHz. Eq. (12) predicts the limit cycle noise for this filter to be –58 dB.

The second filter permits a second sample rate reduction factor of two. Its cutoff frequency is 219 Hz, with a sample rate of 3.125 kHz. Equation (12) predits the limit cycle noise for this filter to be -83 dB. This filter also provides an additional 14-dB attenuation of the limit cycle noise generated in the first aliasing filter, reducing the limit cycle noise from the first filter to -72 dB.

These two filters permit an overall f_S reduction factor of 32 before processing the Bessell filter, detector, and linear-to-$\log_2$ functions. This results in a very substantial throughput improvement. Net execution time is determined by the time to execute a given function multiplied by the sample rate for that function. Thus 32 instructions at the reduced rate will increase the net execution time by an amount equivalent to only 1 instruction at the full sample rate.

Fig. 9 shows the aliasing spectra of the sample rate reduction process.

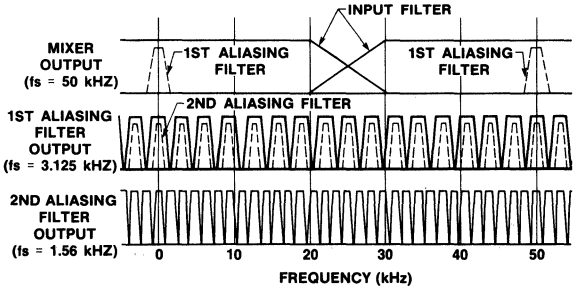


Figure 9. Aliasing Spectra for f_S Reduction

Lowpass Filter

A 4th-order Bessel lowpass filter determines the overall bandwidth of the analyzer. The overall bandwidth is twice the bandwidth of this filter. Overall bandwidths of 20, 50, 100 or 500 Hz are provided by loading the proper set of filter coefficients into RAM when the bandwidth is selected.

The Bessel filter provides an optimal transient response for the analyzer. Good transient response is important, especially at narrow bandwidths, since the spectral peaks are swept with respect to the fiter passband. The net effect is similar to pulsing the filter input. Because the phase response is critical, the matched-z transform is used to convert the analog Bessel design to the z-domain.

The second aliasing filter provides 3 dB of attenuation at 250 Hz. When cascaded with the Bessel filter, which also provides 3 dB attenuation at 250 Hz in the 500 Hz bandwidth mode, the response at this bandwidth is modified. However, since the overall bandwidth is relatively broad, good transient response is still achieved. Cascading these two filters provides a "transitional" filter with a Bessel response at low attenuation and a Chebyschev response at high attenuation. At bandwidths less than 500 Hz, the combination produces an optimal tradeoff between transient response and resolution.

Analysis of Equation (12) reveals that limit cycle noise increases exponentially as the pole frequency is reduced. Operating the lowpass filter at the lowest possible sampling frequency (1.5625 kHz) minimizes limit cycle noise, in addition to improving throughput. Limit cycle noise for the lowpass filter will be -95 dB at the 500-Hz bandwidth, increasing to -67 dB at the 20-Hz bandwidth.

Detector

A square-law detector provides a DC signal corresponding to the energy at the lowpass filter output. From trigonometry:

$$(A \cos wt)^2 = \frac{A^2}{2}(1 + \cos 2wt) \qquad (15)$$

The detector output contains the desired DC term and a single undesired term at frequency 2w. If the square law is ideal (easy in the digital domain), no additional terms are produced. The elimination of harmonics ensures the accuracy of the detector with $f_S/32$ = 1.5625 kHz. The highest component is always less than $f_S/64$ with a 250 Hz maximum lowpass filter cutoff frequency. However, 2w can be anywhere from DC to 500 Hz as the VCO sweeps past the spectral component.

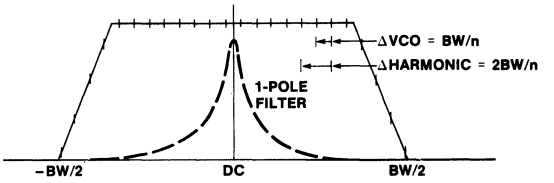


Figure 10. Detector Sweep Filtering

Fig. 10 illustrates a technique to render the effects of the 2w terms negligible. The analyzer passband is divided into n equal intervals. The VCO sweep rate is controlled so that the VCO sweeps BW/n per $f_S/32$ interval. The detector is followed by a single-pole lowpass filter with a 3 dB frequency of BW/n. As the VCO sweeps a component through the passband, the DC term is present in all n intervals, but the 2w term can affect only one interval. The worst-case DC error is 1/n for an ideal cutoff, and is multiplied by $(2^0 + 2^{-1} + 2^{-3} + 2^{-4} + 2^{-5} + 2^{-5.5} + 2^{-6} + 2^{-6.5} + 2^{-7} + 2^{-7.25} + \ldots.) = 1.85$ due to the finite 6 dB/octave rolloff of the single-pole filter. Further analysis reveals that:

$$n = \frac{1.85}{10^{e/10} - 1} \qquad (16)$$

where e represents the resulting error in dB. For e = 0.1 dB, n = 80.

In the filter test mode, the signal frequency and VCO frequency are the same, forcing w = 0. The detector has no error in this mode, but has a 3 dB gain due to the second DC term.

The detector output represents signal energy. Each bit in the detector output word thus represents only 3 dB, and 21 bits are required to reflect a 60 dB dynamic range. Double precision arithmetic is required for the detector ouput and the single-pole filter. The 67C7560 multiplier will handle double precision calculations with a time penalty. Fortunately, the calculations to be performed are simple and the operations take place at the minimum sample rate, reducing the impact on throughput.

Linear-to-Log Conversion

The architecture of Figure 6 is customized to provide an efficient algorithm for linear-to-logarithmic output conversion. The RAM address generator monitors the 8 MSBs of the data bus, and can provide a number indicating the MSB position of a positive

number. This output is used to retrieve a lookup table value. This value is used to scale the data word to quickly left-justify the MSB. A second 4-point lookup table is then used to improve the accuracy of the resulting $\log_2$ conversion. A $\log_2$ conversion is adequate, since:

$$\log_{10} x = \frac{\log_2 x}{\log_2 10} \qquad (17)$$

Equation (17) demonstrates that the output can be displayed in decibels by setting the oscilloscope or X-Y plotter Y-axis gain to the proper value.

Two lookup tables provide .027 dB accuracy for output values from 0 to –45 dB, and 3 dB accuracy from –45 to –84 dB. The logarithmic accuracy is limited by the 10-bit output word length to the D/A. This output can represent 0 to –84 dB in .082 dB increments. The accuracy of the 4-point lookup is therefore sufficient.

The logarithmic conversion procedure is as follows:

1) If the MSB of the data word is not among the 8 MSBs into the address generator, multiply the word by $2^7 = 128$, and increment the output number by 7. Repeat until the data word is greater than 2^{-7}, but no more than three times. Set a flag if this step is executed more than once.
2) Look up the appropriate scale factor, from 2^0 to 2^6. Add $\log_2$ of the scale factor to the output word. The conversion is now accurate to 3 dB.
3) If the flag was not set during step 1, multiply the data word by the scale factor to left-justify the MSB position.
4) If the flag was not set during step 1, retrieve an intercept and slope value from the 8-word lookup table (four pairs available). Perform a linear interpolation using:

$$x' = a\,x + b \qquad (18)$$

where a is the slope value
b is the intercept value

The conversion is now accurate to .027 dB.

5) Scale the result to provide 84-dB output range with a 10-bit word.
6) Subtract 2^{-1} from the output to convert it to two's complement form for the D/A.

The calculations are double precision for steps 1, 2, and 3, and single precision thereafter. The conversion sequence can be bypassed using a strap option to provide a linear amplitude output from 0 to –30 dB.

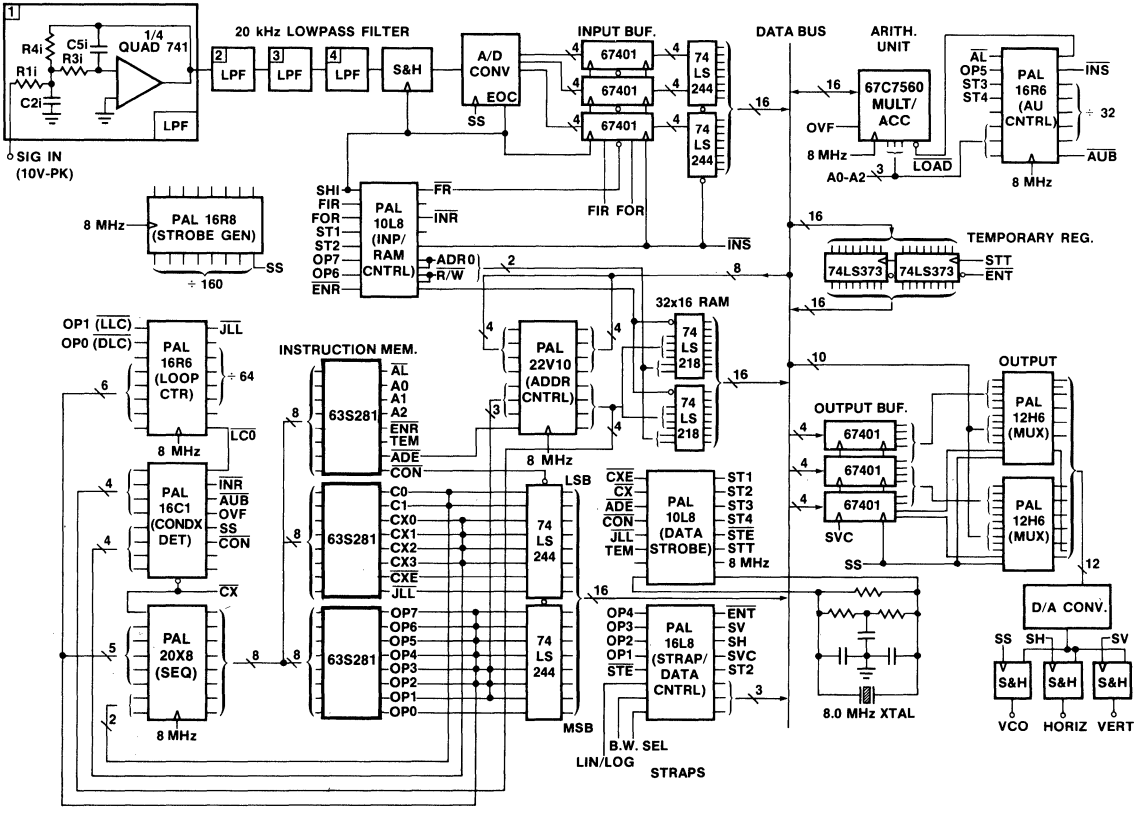


Figure 11. Simplified Schematic Hi-Fi Audio Spectrum Analyzer

Control Logic

Figure 11 shows a simplified schematic of the analyzer. All critical components are shown. Bypass capacitors and some component input connections are omitted for clarity.

The microprogram is stored in three 63S281 PROMs. The microcode word formats are shown in Figure 12. A wide, highly-parallel instruction word ensures maximum flexibility and program efficiency.

Eight PAL devices interpret the instruction word and control the analyzer. Two additional PAL devices generate a 50-kHz strobe from the 8-MHz master clock, and implement the output D/A multiplexer. The control PAL devices function as follows:

Sequencer: A PAL20X8 implements an 8-bit instruction sequencer. The sequencer performs the following operations:

C1	C0	$\overline{CX}$	Operation
0	0	X	Increment by 1 (execute next instruction)
0	1	0	Increment by 2 (skip next instruction)
1	0	0	Jump to address
1	1	0	No increment (repeat current instruction)

The $\overline{CX}$ input conditions the sequencer. Conditional branches or skip operations can be implemented. The sequencer will increment if the conditional requirement is not met.

Condition detector: A PAL16C1 monitors up to twelve status flags, and generates $\overline{CX}$. The microcode word includes a 4-bit

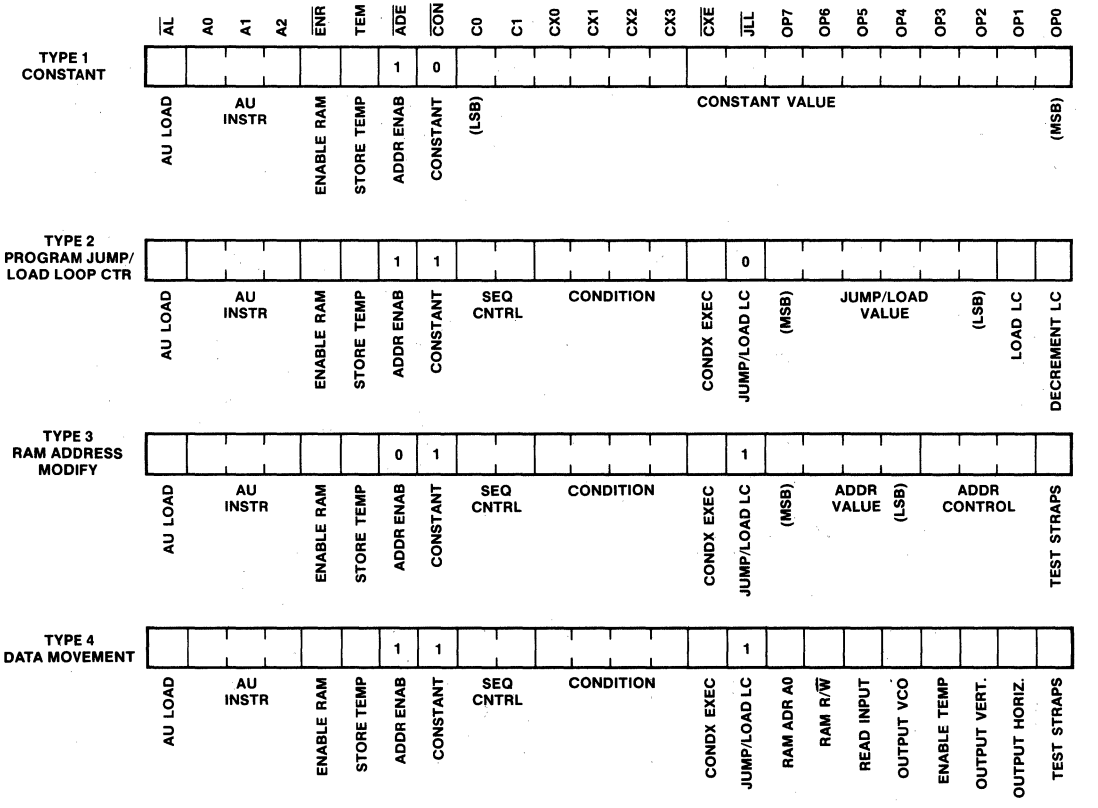


Figure 12. Microinstruction Word Formats

condition word, CX0 through CX3. $\overline{CX}$ will be zero under the following conditions:

CX3	CX2	CX1	CX0	Condition for $\overline{CX}$ = 0
0	0	0	0	Always (unconditional operation)
0	0	0	1	Sample strobe (SS) = 1
0	0	1	0	AU overflow (OVF) = 1
0	0	1	1	AU busy (AUB) = 1
0	1	0	0	Input sample ready (INR) = 0
0	1	0	1	Loop counter timeout ($\overline{LLC}$) = 0
0	1	1	0	$\overline{LLC}$ = 1
0	1	1	1	Address control (AC3-AC0) = 0
1	0	0	0	AC0 = 0
1	0	0	1	AC0 = 1
1	0	1	0	AC1 = 0
1	0	1	1	AC1 = 1
1	1	0	0	AC2 = 0
1	1	0	1	AC2 = 1
1	1	1	0	AC3 = 0
1	1	1	1	AC3 = 1

The assignment is made using the flexible PAL device coding, and is optimized for the analyzer. The user can select a different set of conditions by reprogramming the PAL device.

When the microcode represents a constant (Type 1 microinstruction — see Figure 12) the $\overline{CON}$ input forces $\overline{CX}$ = 1 to suppress conditional operations. $\overline{CX}$ is also used to suppress certain strobes in the analyzer, providing conditional arithmetic operations.

Loop counter: A PAL16R6 implements a 6-bit programmable down counter. This counter controls iteration loops and provides a timeout signal to the condition detector. The counter is preset via a Type 2 microinstruction, and can be decremented by other Type 2 microinstructions. The counter will halt when zero count is reached. Up to 64 iterations can be accommodated with minimal overhead.

Address control: A PAL22V10 provides indexed addressing for the 32x16 RAM, and analyzes the eight MSBs of the data bus for conditional operations. If D15 represents the data bus sign bit, then OP1-OP3 will provide the following functions:

OP3	OP2	OP1	AC3-AC0 Output Function
0	0	0	Clear (0000)
0	0	1	Increment
0	1	0	Decrement
0	1	1	Preset to D15-D12 (Sign + 3 MSB)
1	0	0	Preset to D14-D11 (4 MSB)
1	0	1	Preset to D11-D8 (Address load)
1	1	0	MSB position
1	1	1	No change

The $\overline{ADE}$ input enables a change in the address word. The address word will not change if $\overline{ADE}$ = 1.

The MSB position function indicates the position of the MSB for positive numbers. AC3 represents sign bit D15. This output should be zero. AC2-AC1 represent the position of the first 1 following the sign bit. Code 0000 indicates that D15-D8 are all 0.

Input/RAM control: Miscellaneous FIFO input and RAM control is provided by a PAL 10L8. The 67401 FIFO includes input ready (FIR) and output ready (FOR) signals, which are latched using the input/output shift clocks to generate two flags. The first flag ($\overline{FR}$) resets the FIFO when input ready (latched) goes low, indicating the FIFO capacity is exhausted. The latched output ready signal flag represents input sample ready ($\overline{INR}$). The INR flag is used as a sequencer condition to synchronize wait loops. Use of the FR and INR flags maintains proper fill of the FIFO.

The RAM address LSB (A0) and read-write line (R/$\overline{W}$) are decoded and latched. These signals are provided directly by Type IV microinstructions.

Notice that a clocked register function requires two PAL combinatorial outputs per bit, while a transparent latch function requires only one PAL output per bit.

Arithmetic unit control: The variety of functions listed in Table 3 indicate the utility of the arithmetic unit (AU). A PAL16R6 provides simplified control of the AU.

The PAL devices and AU load signal provide conditional arithmetic operations. Gating the load input will suppress the start of a new arithmetic operation. When $\overline{CXE}$ is high, the operation is performed unconditionally. When $\overline{CXE}$ is low, the operation is performed only if $\overline{CX}$ is low. Combining conditional jumps and conditional AU operations provides a high degree of program flexibility.

The PAL device monitors the AU instructions and generates a busy signal ($\overline{AUB}$). A counter in the PAL device keeps track of variable-length operations to provide the correct output for any instruction sequence. The $\overline{AUB}$ signal conditions the sequencer to synchronize the microprogram to the AU operation. Microprogramming is simplified as a result.

The PAL device also gates the input FIFO shift out clock ($\overline{INS}$) to eliminate transients while providing a full 125-ns pulse for proper FIFO operation.

Data strobe generator: A PAL10L8 provides a number of transient-free, gated strobes. These strobes provide control of the analyzer data flow. The PAL device interprets the microinstruction to determine the proper microinstruction type, and generates the strobes accordingly.

The PAL device also generates an 8-MHz buffered clock, as shown in Figure 11. The crystal oscillator circuit provides independent AC and DC feedback, permitting reliable operation with the PAL device.

Strap/output sample control: A PAL16L8 generates additional control strobes for the output sample-and-hold circuits.

The PAL device also provides a tristate buffer function, connecting control straps to the data bus for certain conditional jump operations. Two straps select the desired analyzer bandwidth/sweep rate, and the third strap selects linear or logarithmic output.

Signal output

The VCO output must be sampled at precise intervals to avoid phase modulation effects. Three 67401 FIFOs buffer the VCO samples, which are generated during the 50-kHz input processing. A 12-bit D/A converter provides better than 91 dB signal-to-distortion ratio. The S&H circuit provides VCO outputs at precise 50-kHz intervals, and removes spikes that are generated in the D/A converter. All necessary control signals are generated by the strap/output data control PAL device.

The horizontal and vertical outputs normally drive an X-Y plotter or oscilloscope. There is no need to buffer these signals as long as the two outputs track each other. The D/A used for the VCO output is shared by adding two PAL12H6 chips programmed as multiplexers. Use of PAL devices requires fewer packages than a TTL multiplexer. Additional S&H circuits decode the multiplexed D/A output to separate the output signals.

Microprogram

The architecture can implement a variety of DSP functions. A microprogram, stored in 63S281 PROMs, customizes the architecture to perform the spectrum analyzer tasks. The microinstruction formats were summarized in Figure 12. The algorithms to be implemented were discussed in the previous section. The step-by-step implementation of these algorithms is converted to a sequence of microinstructions to form the microprogram. The procedure is analogous to programming a microprocessor.

Operation of the microprogram is better understood by considering the allocation of the 74S218 RAM locations, shown in Figure 13. The microprogram consists of two parts. High-speed input processing provides the carrier generation, mixing, aliasing filter and lowpass filter functions. Figure 13a shows the RAM allocation during input processing. The input segment includes an efficient iteration loop, using the PAL device loop counter, to process the 50-kHz functions. The carrier frequency shift and lowpass filter functions are processed at the $f_S/32$ reduced sample rate for maximum throughput efficiency.

The values of sin Δ, cos Δ, and the Bessell filter coefficients depend on the analyzer bandwidth strap selection. These values are stored in a "table" area in Fig. 13, and can be easily changed. The fixed aliasing filter coefficients are stored as constants in the microprogram itself.

Once the input processing is complete, coefficients located in the table area can be changed. This area is re-used by the output program segment to hold the scale factors for the linear-to-log conversion routine. The detector functions are processed, and the logarithmic conversion is started with the RAM allocation of Figure 13(b). The table area is then reloaded with the interpolation coefficients (Figure 13(c)) to complete the logarithmic conversion. Shaded areas in Figure 13 provide temporary data and flag storage for the routines.

The microprogram samples the strap settings and loads the table area with the appropriate coefficients for input processing. The detector filter coefficient (b_1) is also determined and loaded. The input processing is then repeated. This sequence repeats indefinitely. The coefficient loading technique makes efficient use of RAM capacity while eliminating elaborate jump sequences. All coefficient table updates are processed at the minimum sample rate for best efficiency.

The PAL device controllers simplify the microprogram. A PAL device provides hardware iteration loops. The AU controller eliminates wasteful "NO-OP" instructions otherwise required to allow completion of AU operations. The input control PAL device simplifies handshaking with the input logic. With the benefit of the PAL device controllers, the analyzer microprogram easily fits into the 256-instruction capacity of the PROMs.

(A4-A1)

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	(A0)
–	–	SIN X	SIN Y	SIN Δ	b1	b1	–	X_{N-1}	X_{N-2}	X_{N-1}	X_{N-2}	X_{N-1}	X_{N-2}	X_{N-1}	X_{N-2}	0
–	–	COS X	COS Y	COS Δ	b2	b2	–	X_{N-1}	X_{N-2}	X_{N-1}	X_{N-2}	X	X	X	VCO RAMP	1
		CARRIER GENERATOR			LOWPASS FILTER			ALIASING FILTERS					LOWPASS FILTER			

(a) INPUT

TEMP LSB	FLAG	X	X	SCALE A	SCALE B	SCALE C	SCALE D	X	X	X	X	X	X	X	X	0
TEMP MSB	OUTPUT	X	X	LOG A	LOG B	LOG C	LOG D	X	X	X	X	X_{N-1} LSB	X_{N-1} MSB	b1	X	1
UTILITY				LIN-LOG SCALING								DETECTOR				

(b) OUTPUT-1

TEMP LSB	FLAG	X	X	a_1	a_2	a_3	a_4	X	X	X	X	X	X	X	X	0
TEMP MSB	OUTPUT	X	X	b_1	b_2	b_3	b_4	X	X	X	X	X	X	X	X	1
UTILITY				LIN-LOG INTERPOLATION												

KEY: ▨ SCRATCH — NOT USED X NOT AVAILABLE □ TABLE

(c) OUTPUT-2

Figure 13. RAM Allocation

```
TITLE           AN-100 DSP Counter
PATTERN         DSPCOUNT
REVISION        1
AUTHOR          Marc Baker
COMPANY         Monolithic Memories
DATE            August 20, 1987

CHIP DSPCOUNT PAL20X8

CLK NC OP3 OP4 OP5 OP6 OP7 C0 C1 /CX NC    GND
/OE NC A7  A6  A5  A4  A3  A2 A1 A0  /LOAD VCC

EQUATIONS

LOAD =  /C0* C1* CX                          ;FED BACK TO EQUATIONS

/A0 :=  /LOAD*/A0                            ;HOLD/INCREMENT BY 2
     +  /C0* C1* CX                          ;LOAD 0
    :+: /C0*/C1                              ;INCREMENT BY 1

/A1 :=  /LOAD*/A1                            ;HOLD
     +  /C0* C1* CX                          ;LOAD 0
    :+: /C0*/C1*     A0                      ;INCREMENT BY 1
     +   C0*/C1* CX*/A0                      ;INCREMENT BY 2

/A2 :=  /LOAD*/A2                            ;HOLD
     +  /C0* C1* CX                          ;LOAD 0
    :+: /C0*/C1*     A1* A0                  ;INCREMENT BY 1
     +   C0*/C1* CX* A1*/A0                  ;INCREMENT BY 2

/A3 :=  /LOAD*/A3                            ;HOLD
     +  /C0* C1* CX*/OP3                     ;LOAD
    :+: /C0*/C1*     A2* A1* A0              ;INCREMENT BY 1
     +   C0*/C1* CX* A2* A1*/A0              ;INCREMENT BY 2

/A4 :=  /LOAD*/A4                            ;HOLD
     +  /C0* C1* CX*/OP4                     ;LOAD
    :+: /C0*/C1*     A3* A2* A1* A0          ;INCREMENT BY 1
     +   C0*/C1* CX* A3* A2* A1*/A0          ;INCREMENT BY 2

/A5 :=  /LOAD*/A5                            ;HOLD
     +  /C0* C1* CX*/OP5                     ;LOAD
    :+: /C0*/C1*     A4* A3* A2* A1* A0      ;INCREMENT BY 1
     +   C0*/C1* CX* A4* A3* A2* A1*/A0      ;INCREMENT BY 2

/A6 :=  /LOAD*/A6                                ;HOLD
     +  /C0* C1* CX*/OP6                         ;LOAD
    :+: /C0*/C1*     A5* A4* A3* A2* A1* A0      ;INC BY 1
     +   C0*/C1* CX* A5* A4* A3* A2* A1*/A0      ;INC BY 2

/A7 :=  /LOAD*/A7                                ;HOLD
     +  /C0* C1* CX*/OP7                         ;LOAD
    :+: /C0*/C1*     A6* A5* A4* A3* A2* A1* A0  ;INC BY 1
     +   C0*/C1* CX* A6* A5* A4* A3* A2* A1*/A0  ;INC BY 2
```

```
SIMULATION

TRACE_ON CLK A7 A6 A5 A4 A3 A2 A1 A0     ;Trace CLK and outputs

SETF OE /C0 C1 CX /OP7 /OP6 /OP5 /OP4 /OP3
CLOCKF CLK                               ;Load all 0s
CHECK /A7 /A6 /A5 /A4 /A3 /A2 /A1 /A0

SETF C0 /C1
CLOCKF CLK                               ;Increment by 2
CHECK /A7 /A6 /A5 /A4 /A3 /A2  A1 /A0    ;to 2

CLOCKF CLK                               ;Increment by 2
CHECK /A7 /A6 /A5 /A4 /A3  A2 /A1 /A0    ;to 4

CLOCKF CLK                               ;Increment by 2
CHECK /A7 /A6 /A5 /A4 /A3  A2  A1 /A0    ;to 6

SETF /C0
CLOCKF CLK                               ;Increment by 1
CHECK /A7 /A6 /A5 /A4 /A3  A2  A1  A0    ;to 7

CLOCKF CLK                               ;Increment by 1
CHECK /A7 /A6 /A5 /A4  A3 /A2 /A1 /A0    ;to 8

SETF C0 C1
CLOCKF CLK                               ;Hold
CLOCKF CLK                               ;Hold
CHECK /A7 /A6 /A5 /A4  A3 /A2 /A1 /A0    ;to 8

TRACE_OFF
```

```
TITLE           AN-100 DSP Condition
PATTERN         DSPCOND
REVISION        1
AUTHOR          Marc Baker
COMPANY         Monolithic Memories
DATE            August 20, 1987

CHIP DSPCOND PAL16C1

CX3  CX2 CX1 CX0 SS  OVF     AUB INR /LLC GND
/CON AC0 AC1 AC2 /CX COMP_CX AC3 NC  NC   VCC

EQUATIONS

CX = /CX3*/CX2*/CX1*/CX0*       CON
   + /CX3*/CX2*/CX1* CX0* SS*   CON
   + /CX3*/CX2* CX1*/CX0* OVF*  CON
   + /CX3*/CX2* CX1* CX0* AUB*  CON
   + /CX3* CX2*/CX1*/CX0*/INR*  CON
   + /CX3* CX2*/CX1* CX0* LLC*  CON
   + /CX3* CX2* CX1*/CX0*/LLC*  CON
   + /CX3* CX2* CX1* CX0*/AC3*/AC2*/AC1*/AC0* CON
   +  CX3*/CX2*/CX1*/CX0*/AC0*  CON
   +  CX3*/CX2*/CX1* CX0* AC0*  CON
   +  CX3*/CX2* CX1*/CX0*/AC1*  CON
   +  CX3*/CX2* CX1* CX0* AC1*  CON
   +  CX3* CX2*/CX1*/CX0*/AC2*  CON
   +  CX3* CX2*/CX1* CX0* AC2*  CON
   +  CX3* CX2* CX1*/CX0*/AC3*  CON
   +  CX3* CX2* CX1* CX0* AC3*  CON

SIMULATION

SETF /CON                       ;SET /CX HIGH
CHECK /CX

SETF CON /CX3 /CX2 /CX1 /CX0    ;CX3-CX0=0 - SET /CX LOW
CHECK CX

SETF CX0 SS                     ;CX3-CX0=1 - SET /CX LOW
CHECK CX

SETF CX1 /CX0 OVF               ;CX3-CX0=2 - SET /CX LOW
CHECK CX

SETF CX0 AUB                    ;CX3-CX0=3 - SET /CX LOW
CHECK CX

SETF CX2 /CX1 /CX0 /INR         ;CX3-CX0=4 - SET /CX LOW
CHECK CX

SETF CX0 LLC                    ;CX3-CX0=5 - SET /CX LOW
CHECK CX
```

```
SETF CX1 /CX0 /LLC                ;CX3-CX0=6 - SET /CX LOW
CHECK CX

SETF CX0 /AC3 /AC2 /AC1 /AC0      ;CX3-CX0=7 - SET /CX LOW
CHECK CX

SETF CX3 /CX2 /CX1 /CX0           ;CX3-CX0=8 - SET /CX LOW
CHECK CX

SETF CX0 AC0                      ;CX3-CX0=9 - SET /CX LOW
CHECK CX

SETF CX1 /CX0                     ;CX3-CX0=10 - SET /CX LOW
CHECK CX

SETF CX0 AC1                      ;CX3-CX0=11 - SET /CX LOW
CHECK CX

SETF CX2 /CX1 /CX0                ;CX3-CX0=12 - SET /CX LOW
CHECK CX

SETF CX0 AC2                      ;CX3-CX0=13 - SET /CX LOW
CHECK CX

SETF CX1 /CX0                     ;CX3-CX0=14 - SET /CX LOW
CHECK CX

SETF CX0 AC3                      ;CX3-CX0=15 - SET /CX LOW
CHECK CX
```

```
TITLE           AN-100 DSP Address Control
PATTERN         ADDCONT
REVISION        1
AUTHOR          Marc Baker
COMPANY         Monolithic Memories
DATE            August 21, 1987

CHIP ADDCONT PAL22V10

CLK OP3 OP2 OP1 /ADE D15 D14 D13 D12 NC NC GND
NC  NC  D11 D10 AC0  AC1 AC2 AC3 D9  D8 NC VCC
GLOBAL

EQUATIONS

AC0 := /OP3*/OP2* OP1*/AC0* ADE                    ;INC
     + /OP3* OP2*/OP1*/AC0* ADE                    ;DEC
     + /OP3* OP2* OP1* D12* ADE                    ;D12
     +  OP3*/OP2*/OP1* D11* ADE                    ;D11
     +  OP3*/OP2* OP1* D8 * ADE                    ;D8
     +  OP3* OP2*/OP1* D14* ADE                    ;MSB EQUATIONS
     +  OP3* OP2*/OP1*/D14*/D13* D12* ADE
     +  OP3* OP2*/OP1*/D14*/D13*/D12*/D11* D10* ADE
     +  OP3* OP2*/OP1*/D14*/D13*/D12*/D11*/D10*/D9*D8* ADE
     +  OP3* OP2* OP1* AC0                         ;HOLD
     +  AC0*/ADE                                  ;HOLD

AC1 := /OP3*/OP2* OP1* AC1*/AC0* ADE               ;INC
     + /OP3*/OP2* OP1*/AC1* AC0* ADE               ;INC
     + /OP3* OP2*/OP1* AC1* AC0* ADE               ;DEC
     + /OP3* OP2*/OP1*/AC1*/AC0* ADE               ;DEC
     + /OP3* OP2* OP1* D13* ADE                    ;D13
     +  OP3*/OP2*/OP1* D12* ADE                    ;D12
     +  OP3*/OP2* OP1* D9 * ADE                    ;D9
     +  OP3* OP2*/OP1* D14* ADE                    ;MSB EQUATIONS
     +  OP3* OP2*/OP1*/D14* D13* ADE
     +  OP3* OP2*/OP1*/D14*/D13*/D12*/D11* D10* ADE
     +  OP3* OP2*/OP1*/D14*/D13*/D12*/D11*/D10* D9* ADE
     +  OP3* OP2* OP1* AC1                         ;HOLD
     +  AC1*/ADE                                  ;HOLD
```

```
AC2 := /OP3*/OP2* OP1*/AC2* AC1* AC0* ADE        ;INC
     + /OP3*/OP2* OP1* AC2*/AC1*      ADE        ;INC
     + /OP3*/OP2* OP1* AC2*     /AC0* ADE        ;INC
     + /OP3* OP2*/OP1*/AC2*/AC1*/AC0* ADE        ;DEC
     + /OP3* OP2*/OP1* AC2* AC1*      ADE        ;DEC
     + /OP3* OP2*/OP1* AC2*      AC0* ADE        ;DEC
     + /OP3* OP2* OP1* D14* ADE                   ;D14
     +  OP3*/OP2*/OP1* D13* ADE                   ;D13
     +  OP3*/OP2* OP1* D10* ADE                   ;D10
     +  OP3* OP2*/OP1* D14* ADE                   ;MSB EQUATIONS
     +  OP3* OP2*/OP1* D13* ADE
     +  OP3* OP2*/OP1* D12* ADE
     +  OP3* OP2*/OP1* D11* ADE
     +  OP3* OP2* OP1* AC2                        ;HOLD
     +  AC2*/ADE                                  ;HOLD

AC3 := /OP3*/OP2* OP1*/AC3* AC2* AC1* AC0* ADE   ;INC
     + /OP3*/OP2* OP1* AC3*/AC2*           ADE   ;INC
     + /OP3*/OP2* OP1* AC3*     /AC1*      ADE   ;INC
     + /OP3*/OP2* OP1* AC3*          /AC0* ADE   ;INC
     + /OP3* OP2*/OP1*/AC3*/AC2*/AC1*/AC0* ADE   ;DEC
     + /OP3* OP2*/OP1*/AC3* AC2*           ADE   ;DEC
     + /OP3* OP2*/OP1*/AC3*      AC1*      ADE   ;DEC
     + /OP3* OP2*/OP1*/AC3*           AC0* ADE   ;DEC
     + /OP3* OP2* OP1* D15* ADE                   ;D15
     +  OP3*/OP2*/OP1* D14* ADE                   ;D14
     +  OP3*/OP2* OP1* D11* ADE                   ;D11
     +  OP3* OP2* OP1* AC3                        ;HOLD
     +  AC3*/ADE                                  ;HOLD

SIMULATION

TRACE_ON CLK AC3 AC2 AC1 AC0

SETF ADE /OP3 /OP2 /OP1
CLOCKF CLK                          ;CLEAR TO 0
CHECK /AC3 /AC2 /AC1 /AC0

SETF OP1
CLOCKF CLK                          ;INCREMENT TO 1
CHECK /AC3 /AC2 /AC1 AC0

CLOCKF CLK                          ;INCREMENT TO 2
CHECK /AC3 /AC2 AC1 /AC0

CLOCKF CLK
CLOCKF CLK
CLOCKF CLK
CLOCKF CLK
CLOCKF CLK
CLOCKF CLK                          ;INCREMENT TO 8
CHECK AC3 /AC2 /AC1 /AC0
```

```
SETF OP2 /OP1
CLOCKF CLK                          ;DECREMENT TO 7
CHECK /AC3 AC2 AC1 AC0

CLOCKF CLK
CLOCKF CLK
CLOCKF CLK
CLOCKF CLK                          ;DECREMENT TO 3
CHECK /AC3 /AC2 AC1 AC0

SETF OP1 /D15 D14 /D13 D12 /D11
CLOCKF CLK                          ;SET TO D15-D12
CHECK /AC3 AC2 /AC1 AC0

SETF OP3 /OP2 /OP1
CLOCKF CLK                          ;SET TO D14-D11
CHECK AC3 /AC2 AC1 /AC0

SETF OP1 D10 /D9 D8
CLOCKF CLK                          ;SET TO D11-D8
CHECK /AC3 AC2 /AC1 AC0

SETF OP2 /OP1
CLOCKF CLK                          ;CHECK MSB
CHECK /AC3 AC2 AC1 AC0

SETF /D14
CLOCKF CLK                          ;CHECK MSB
CHECK /AC3 AC2 /AC1 AC0

SETF OP1
CLOCKF CLK                          ;HOLD
CHECK /AC3 AC2 /AC1 AC0

SETF /OP3 /OP2 /OP1 /ADE            ;HOLD
CLOCKF CLK
CHECK /AC3 AC2 /AC1 AC0

TRACE_OFF
```

Advanced
Micro
Devices

CP-113

Serializing FIFO and Burst Error Processor Team Up to Enhance Serial Data Reliability*

Suneel Rajpal, Nadia Sachs and Danesh Tavana

In high-speed, serial data transmission, as in state-of-the-art disk drives and data communication, there is a growing need for data reliability.

The Single Burst Error Recovery chip, SiBER, can correct 5-, 8-, or 11-bit bursts of error or detect double-burst errors in high-speed serial-data bit streams. This paper describes serial-data error detection and correction in host-independent and peripheral-independent environments. The SiBER implements the standard CCITT CRC polynomial and a computer-generated polynomial in one 24-pin bipolar LSI chip.

4

* This paper is a slightly updated version of the paper by the same name which appeared in the *Wescon/83 Professional Program Session 23* reprint, paper 23/1; 8-11 November 1983.

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JULY 1988

Serializing FIFO and Burst Error Processor Team Up to Enhance Serial Data Reliability

Suneel Rajpal, Nadia Sachs and Danesh Tavana

Introduction

With increasing densities in mass-storage systems, the probability of error in received data also increases. To remedy the problem, users incorporate error detection and correction techniques in their designs. In the area of high speed serial data transmission, as in state-of-the-art disk drives and data communication, there is a growing need for data reliability.

Monolithic Memories' Single Burst Error Recovery chip, SiBER, is ideal in applications requiring a short development time, *with no knowledge whatsoever* of the complex mathematics involved in error-correction codes. The SiBER chip can be used to correct 5-, 8-, or 11-bit bursts of erroneous data, or detect double-burst errors in high-speed serial bit streams. The SiBER implements the standard CCITT CRC polynomial and one of Neal Glover's computer-generated polynomials in one 24-pin bipolar LSI chip.

This paper describes serial-data error detection and correction in host-independent and peripheral-independent environments.

The interface of the SiBER chip between the host and the disk/peripheral is fairly straightforward. To aid in the efficient handling of data transfer between the Siber and the host, the 57/67417 provides an elegant solution. The '417 Serializing FIFO is intended as a one-chip solution for buffering and serializing/deserializing data. It is a FIFO which has one parallel port configurable as an input or an output. It also has two dedicated serial ports for input and output operations. It can typically replace four or more MSI chips. Another IC, the SN54/74S419, is a FIFO RAM Controller which converts a static RAM to a FIFO with minimal external circuitry. It is used where large blocks of data, up to 64K, need to be buffered.

The SiBER can be used with three correction options: software only, a combination of hardware and software, and entirely in hardware. These three correction options have different hardware requirements, using a Serializing FIFO or a FIFO RAM Controller as the buffer management unit. These different hardware requirements are discussed in greater detail.

Formatting the Data On the Disk

Large files and data bases can be permanently stored on the magnetic surface of a Winchester disk. Data is stored on the disk with a predefined format which varies among different manufacturers. The disk surface is subdivided into a number of circular concentric tracks, and each track is further divided into many records. Data is transferred one record at a time in a block fashion between the host and the disk. As shown in Figure 1, a record is comprised of an identification field (ID field) and a data field, with the data field typically being 256 bytes long.

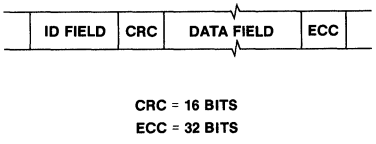


Figure 1. Data Format on a Winchester Disk

An Error Recovery Scheme

With the progress of technology, the industry's trend is towards higher memory densities. The rate of erroneous data increases as disk densities increase, and a need to recover from faulty data becomes necessary. One scheme used to detect and correct erroneous data is through an encoding/decoding algorithm that appends a series of parity checkbits to the transmitted/received data. Figure 1 represents a formatted record with a 16-bit CRC code appended to the ID field, and a 32-bit code appended to the data field. These codes or checkbits are uniquely created for the data during a write operation to the disk, and then appended to the data stream. During a read from the disk, the checkbits are regenerated as the data is being read and compared with the previously written checkbits. If the data is error-free the two sets of checkbits should match, and the system should resume normal operation; however, if the data is in error, the two sets of checkbits will not match, and an error flag will interrupt the CPU to indicate incorrect data. In hardware, the SiBER chip performs the encoding and decoding of checkbits, and provides for a hardware or software correction mode.

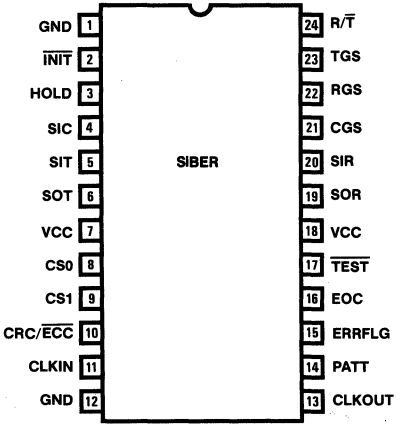


Figure 2. Pinout of the SiBER

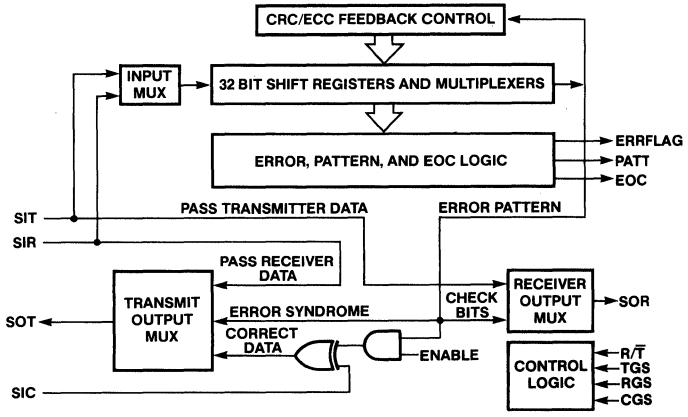


Figure 3. Block Diagram of the SiBER

The SiBER Chip

Monolithic Memories is presently designing SiBER, which will soon go into volume production. SiBER comes in a 24-pin package and operates at or above 15 megabits per second. The SiBER features a selectable standard CRC polynomial or a powerful 32-bit, computer-generated polynomial which can correct 5, 8, or 11 bits of burst error. There are various options which allow for correction in software, in hardware, or in a combination of the two. The SiBER's pinout and internal architecture are illustrated respectivley in Figures 2 and 3. The twenty-four signals can be classified into four groups: I/O ports, control signals, output flags, and power.

The two I/O ports, Transmitter and Receiver ports, easily interface to the CPU and the disk drive environment. The associated signals in the transmitter port are serial input transmitter (SIT), serial input for correction (SIC), and serial output transmitter (SOT). The I/O signals in the receiver port are serial input receiver (SIR), and serial output receiver (SOR). The control signals determine the operation which is to be performed in the chip; these control signals will not be discussed in detail. The three output flags are the *error flag* (ERRFLG) which indicates an erroneous data, the *pattern available flag* (PATT) which is raised when the error pattern is available in the 32-bit shift register, and an *end of cycle flag* (EOC) which is raised when the error pattern is shifted out of the chip. The four VCC and GND pins provide good noise immunity.

Theory of Operation

There are basically three modes of operation: Transmit, Receive, and Correction.

TRANSMIT (Write to disk):

During the transmit mode, the data is written to the disk, and the 16-bit CRC or 32-bit ECC checkbits are generated in the chip. To enter the transmit mode, the device is initialized ($\overline{INIT}$), while the receive/transmit (R/$\overline{T}$) control signal is LOW. The data to be written is input into SIT and simultaneously appears on the SOR

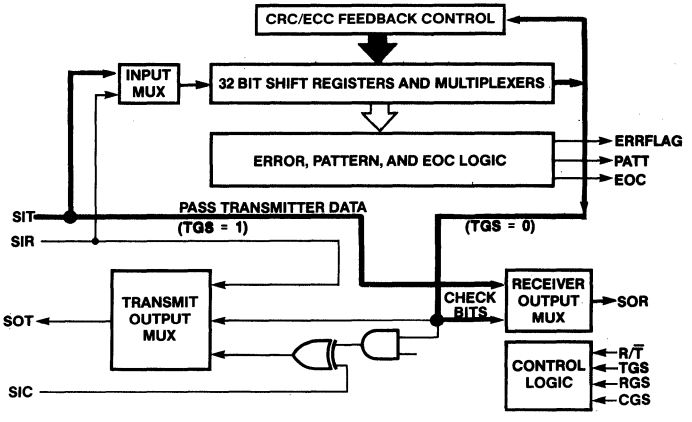


Figure 4. Data Flow in Transmit Mode

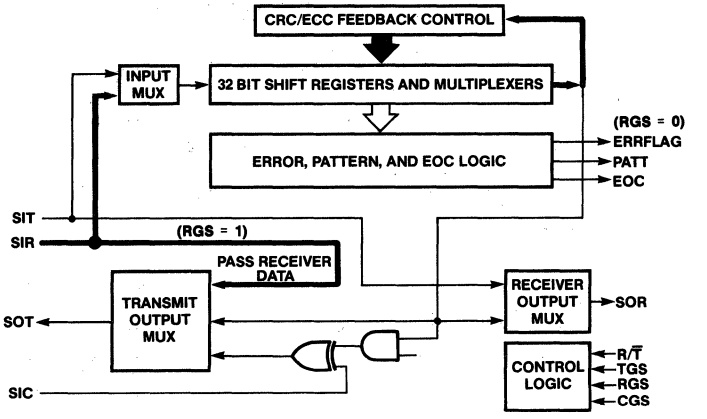


Figure 5. Data Flow in Receive Mode

output. The data on SIT also appears on SOR, while TGS (transmit generate or shift control signal) is HIGH. Once TGS is lowered, the ECC/CRC checkbits are shifted out on SOR and recorded on to the disk. The data flow during the transmit is shown by heavy lines in Figure 4.

RECEIVE (Read from disk):

In the receive mode, the data is read from the disk, and a 16-bit or 32-bit syndrome is generated internally. The syndrome contains the information necessary to perform hardware or software correction. To enter the receive mode of operation, the device is initialized ($\overline{INIT}$) while R/$\overline{T}$ is HIGH. The data being read from the disk in input into SIR and will appear on the transmitter port on SOT.

RGS (read generate or shift control signal) must be high for the duration of data and checkbits. Once RGS is lowered, the ERRFLG output will be raised, if an error condition exists. The data flow during receive is shown in Figure 5.

CORRECTION:

If the error flag (ERRFLG) was not set when RGS was lowered in the receive mode of operation, correction is not required and the data is assumed to be error-free. However, if ERRFLG was set, the data must be corrected. Note that correction is possible only with the 32-bit ECC polynomial. There are three different options for correction when using the 32-bit ECC polynomial: hardware correction, software correction, software and hardware correction. The following pages include three different applications where these modes are discussed in further detail.

The Software Solution

The SiBER can be configured to be used in systems where software correction is desired. In this mode of operation, the SiBER will transfer the necessary information to the host, so that correction can take place in software. After reading the data and the ECC bits, the user must lower the RGS (Read Generate or Shift) control pin, at which time the ERRFLG is latched, if the data is in error and the syndrome bits generated by the SiBER are available serially on the SOT output. Given the syndrome bits, the user has to perform a correction algorithm in software which would appropriately yield the location of the error and the required pattern which corrects the erroneous bits. This is not a recommended method, as the user would have to be involved in the mathematics of the error-correction codes. Therefore, this method would appeal only to certain users.

The data paths for software correction and the hardware needed to interface the SiBER to a host are shown respectively in figures 6a and 6b.

One of the elements, shown in Figure 6b and also referred to in Figure 8b, is the serializing FIFO, 57/67417. The serializing FIFO is an ideal IC for byte-oriented data buffering and serialization/deserialization capabilities. The applications of this part are in interfacing parallel-format computing euipment to serial-format data communications and mass memory equipment. The 67417 internally is a 64x9 FIFO, which can also be configured as a 64x8 FIFO using the Word Length (WL) pin. There are two serial ports, for input and output, and a 9-bit parallel port. The serializing FIFO has three modes of operation: it can be in (a) the Serial-In Parallel-Out mode, in (b) the Parallel-In Serial-Out mode, or in (c) the Serial-In Serial-Out mode. The part is cascadable in the parallel port, which runs up to 6 MHz. The serial port runs at 35 MHz. In order to build a deeper Serializing FIFO structure, the 67417 can be combined with ranks of two 67401s, which are 64x4 parallel-in parallel-out FIFOs also available from Monolithic Memories. Figure 7 shows the three modes of operation of the 67417.

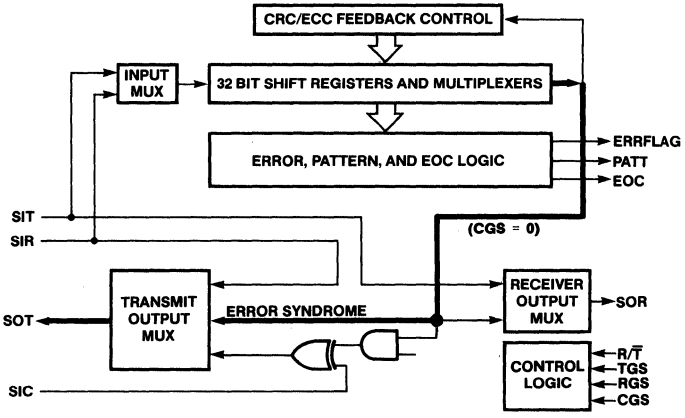


Figure 6a. Data Flow in the SiBER for Software Correction

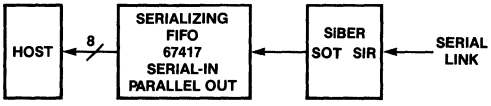


Figure 6b. The SiBER/Host Interface for Software Correction

4

The Hardware/Software Solution

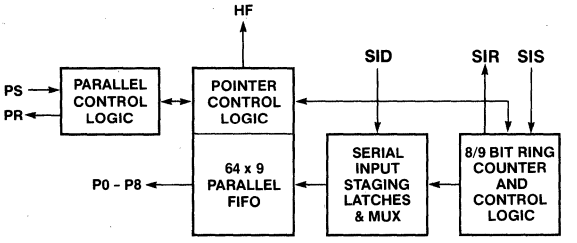
The hardware/software solution uses the SiBER more effectively. After detecting erroneous data, the SiBER can generate the (correction) pattern. Figure 8a shows the data flow within the SiBER during this mode of operation. The data and ECC fields from a serial data link are processed by the SiBER and are available on the SOT port. By maintaining CGS HIGH, the SiBER goes into a mode where it calculates the location of the error. The required pattern, which was previously computed in the host in the software solution, is now performed in the SiBER. When the SiBER completes the computation, the PATTERN flag goes HIGH. The user has to count the number of clocks between the time when the ERRFLG is raised to the time when the PATT flag is raised. This count is the position of the start of the error burst. The error pattern can be shifted out of the SiBER on the SOT port by lowering CGS. Correction is performed in software by using the count and the error pattern parameters.

The interface of the SiBER to the host requires a serializing FIFO, a serial/parallel register, an n-bit counter (dependent on data field), and a correction network which can be eight exclusive-OR gates, as shown in figure 8b. The sequence of events shown in figure 8b are as follows: Path 1 is the data field and the ECC field that are transferred to the serializing FIFO. After the data and ECC fields are read, and if the ERRFLG is raised, the SiBER is in its correction mode. The user must now keep clocking the SiBER, until the error pattern is available. The number of clocks between the assertion of the ERRFLG and the PATT flag must be saved in the counter.

Path 2 shows that the host will read the contents of the counter. The contents of the counter will be used to determine the error location in the data field. By lowering CGS, the user can clock out the error pattern on the SOT pin, as shown by path 3. The error pattern is aligned with the error bits through software, and is sent to the correction unit, as shown by path 4. The host must process the count value to determine the error location. For example, if the error location counter had a count of M, and the length of the data and ECC field is L, then the error starts at L-M bits away from the first serial output bit on the 67417. The Serial/Parallel block, shown in the diagram, would have to be connected appropriately, since the first pattern bit from SOT corresponds to the eleventh data bit in error; the second pattern bit corresponds to the tenth data bit in error, and so forth. The alignment of the pattern bit to the data/ECC bit in error can be performed by the host.

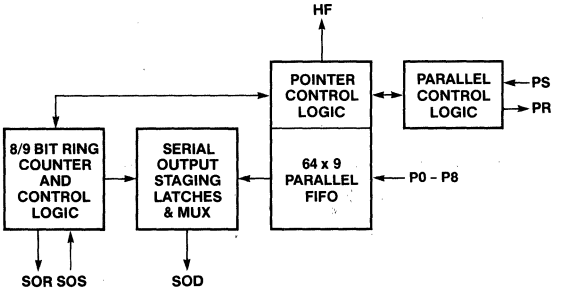
PARALLEL OUT-SERIAL IN

MODE 0 (PDIR = L)



PARALLEL IN-SERIAL OUT

MODE 1 (PDIR = H)



SERIAL IN-SERIAL OUT

MODE 2 (PDIR ≥ 8V)

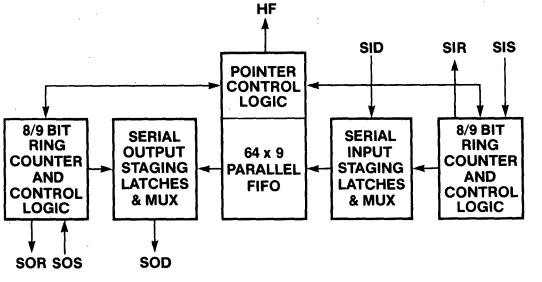


Figure 7. The Three Modes of Operation for the 57/67417 Serializing FIFO

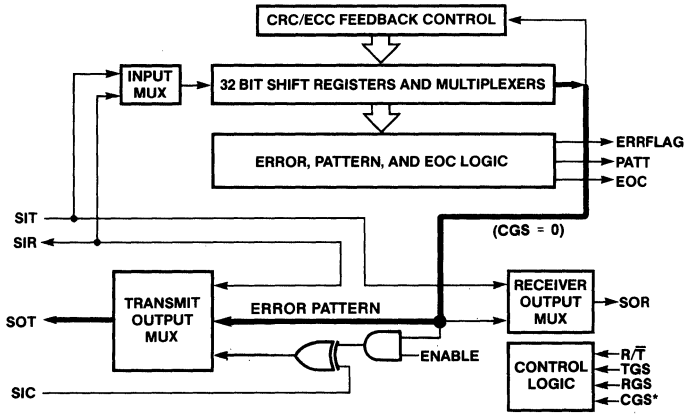


Figure 8a. Data Flow in the SiBER for Hardware/Software Correction

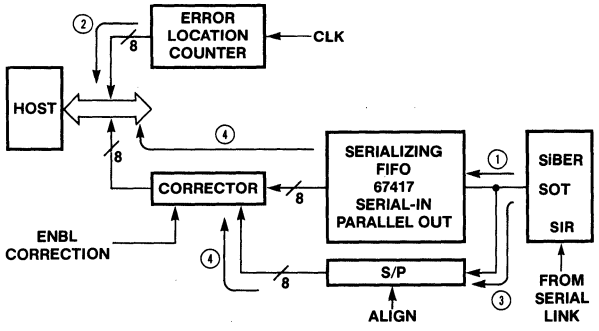


Figure 8b. The SiBER/Host Interface for Hardware/Software Correction

The Hardware Solution

The hardware solution assumes little or no host intervention for error detection and correction. The data flow inside the SiBER for this mode of operation is shown in figure 9a. The actual hardware interface is shown in figure 9b.

This example uses an 8Kx1 FIFO used to collect the serial bits. The FIFO is used to gather the data and send it to the host via a Serial/Parallel converter. In between these two steps, a correction takes place, if the error flag is raised. The actual data flow in figure 9b is as follows: The data from the serial link arrives at the SIR input of the SiBER and is stored in the static RAM via SOT. The static RAM is converted to a FIFO using the SN54/74S419 FIFO RAM Controller. At this time, the FIFO is in a write mode, and the output of the FIFO RAM Controller is sequential write addresses, as shown by 1. After the data and ECC bits are read, and an error is detected, the SiBER goes into a correction mode of operation. Since the data bits must be corrected in reverse order (Last In First Out, LIFO), a down counter addresses the static RAM. The down counter decrements, until the PATT flag goes high. When this flag is raised, the counter then addresses the static RAM, and, as shown by 2, the data from the static RAM enters the SiBER via SIC, is corrected, and written back to the static RAM via SOT. In the actual implementation, three-state buffers are recommended to isolate respectively SIC and SOT during read and write to RAM. As shown in data path 3, upon completion of the correction cycle, the entire 8Kx1 FIFO is transmitted to the host via the Serial/Parallel converter and the FIFO RAM controller. The static RAM is addressed by the FIFO RAM Controller, when the data is being read by the host.

The 74S419 FIFO RAM Controller is a Monolithic Memories' proprietary part and is currently under design. It provides address control and port arbitration for converting a static RAM to a FIFO. A 64K-deep FIFO can be created, using the sixteen address lines. In addition, a host of flags, indicative of the FIFO being full, empty, half full, almost empty, and almost full, are provided. These flags are set relative to the original buffer length selected. Port priority , such as read having precedence over write, are user defined. Handshaking signals, such as ready, are provided in response to a request input. The entire internal operation is synchronous. The SiBER is a flexible part and can be used to facilitate a read/write operation with a static RAM, by adding minimal delay and ensuring a very high throughput.

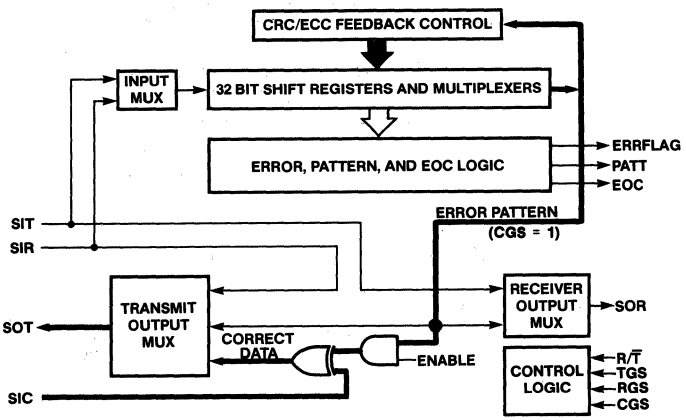


Figure 9a. Data Flow in the SiBER for Hardware Correction

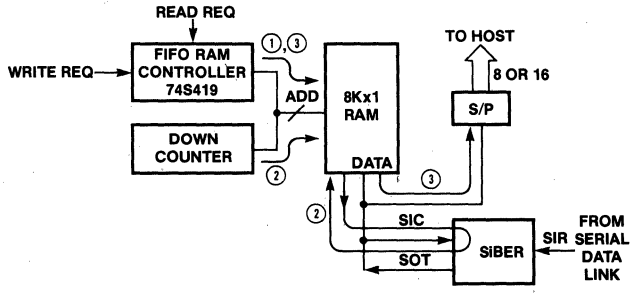


Figure 9b. The SiBER/Host Interface for Hardware Correction

Conclusion

The SiBER is a versatile chip for error detection and correction in high-speed serial data streams. It is useful in numerous applications, becuase it was designed to be host-independent and peripheral-independent. To manage blocks of data in high-speed data transfers, the 67417 Serializing FIFO and the 74S419 FIFO RAM Controller provide economic and efficient solutions. Together, these chips provide low-cost system solutions to mass-memory equipment and data communication reliability issues.

Advanced
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AN-149

First-In First-Out Memories: Operations and Applications

Zwie Amitai and Nusra Lodhi

In many digital systems, high-speed transfers of data or instructions take place between sources and destinations that have different data rates. In other cases, the source and destination cannot operate simultaneously thereby needing some kind of data buffer at either source or destination. First-In First-Out (FIFO) memories are devices used to provide both data buffering and data rate matching between source and destination in digital systems. A family of FIFO devices, available from Monolithic Memories, covers a wide range of data rates as well as different applications such as high-speed data acquisition, and serial to/from parallel format conversions.

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First-In First-Out Memories: Operations and Applications

Zwie Amitai and Nusra Lodhi

What's a FIFO?

Definition

FIFO means First-In First-Out. In this case FIFO refers to a First-In First-Out, 2-port memory device. The data stored in a FIFO memory is provided at the output port in the same sequence that the data was written via the input port. Writing and reading data can be completely independent operations except when the FIFO is full or empty. The FIFO is empty and no more words can be read whenever the total number of words read since reset is equal to the total number of words written. The FIFO is full and no more words can be written whenever the total number of words written is equal to the number of words read plus the capacity of the FIFO.

FIFO Operation

FIFO memories are used to assemble incoming data in a word serial buffer to be read out later in the order written, usually at a different rate. A simple mechanical analogy is the old fashioned coin dispenser used by the ice cream vendor or amusement park arcade vendor (Figure 1). Each coin tube has storage space for a number of coins, say sixty-four coins for example. Coins are dropped into each tube one at a time through a slot in the top of the tube. When a coin is entered, it falls to the top of the stack of coins already stored in the tube. When change is needed, the vendor pushes a lever near the bottom of the tube. This releases a single coin each time the lever is depressed and released. The coin dispenser is clearly a FIFO memory for coins because coins are released at the bottom of the tube in the same order they were entered at the top, but usually at a different rate.

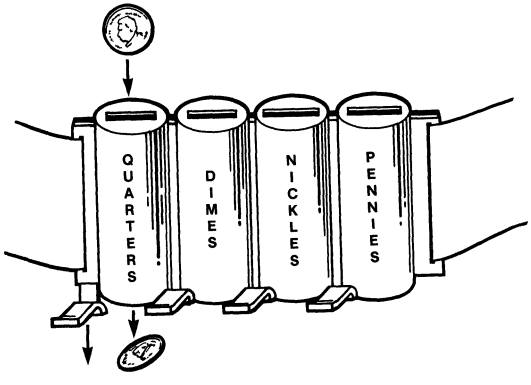

Figure 1. A FIFO Buffer for Coins

Each time a coin is removed from the bottom of the tube, the coin directly above it moves down to fill the vacant space. The same happens to each of the other coins in the stack. There is no restriction on loading and delivering coins asynchronously or simultaneously except for the empty and full conditions. If the tube is empty or if a coin has not yet fallen to the bottom of the tube, nothing will happen when the coin release lever is pressed. When the tube has sixty-four coins stored, it is not possible to stuff another coin into the tube. The operation of the 67401 FIFO is directly analogous to the coin changer except that the 67401 has four coin tubes that operate together rather than four independent tubes in the coin changer.

Using a FIFO

Do You Need a FIFO?

If you are designing or using a digital system involving high-speed transfers of data or instructions from sources to destinations, you may find a FIFO memory to be useful and economically beneficial. Many digital devices such as computers and peripherals have natural or fixed rates for transmitting and receiving data. The most efficient transfers occur when both the source device and the destination device can operate at the same high speed, and when both perform data transfers simultaneously. Unfortunately this is seldom the case, and either the source or the destination device must spend some time waiting or attending to other chores: Data rate matching, and data buffering, to provide the delay between source transmit to destination receive, are two of the principal applications for FIFO memories.

You should consider the possibility of using a FIFO whenever your system requires transferring data, commands, or instructions from any of the following sources to any of the following destinations. Table 1 shows the family of FIFOs available from Monolithic Memories.

SOURCES	DESTINATIONS
Computer CPU	Computer CPU
RAM or ROM	RAM
Disk Memory Unit	Disk Memory Unit
Magnetic Tape Unit	Magnetic Tape Unit
Paper Tape Reader	Paper Tape Punch
Keyboard	CRT Display
Analog-to-Digital Converter	Digital-to-Analog Converter
Telephone Communications Modem	Telephone Communications Modem
Radio Transmitter	Radio Receiver
Timeshare Computer System	Timeshare Computer System
Data Bus Within Computer	Printer
Address Bus Within Computer	Panel Meter Display
Electromechanical Device	Electromechanical Devices

PART NUMBER	ORGANIZATION	FEATURES
67L401	64x4	5 MHz Com
57401		7 MHz Mil
57401A		10 MHz Mil
67401		10 MHz Com
67401A		15 MHz Com
67401B		16.7 MHz Com
5/67411		Standalone 25 MHz Mil, 35 MHz Com
67L402	64x5	5 MHz Com
57402		7 MHz Mil
57402A		10 MHz Mil
67402		10 MHz Com
67402A		15 MHz Com
67402B		16.7 MHz Com
5/67412		Standalone 25 MHz-Mil, 35 MHz-Com
5/67413	64x5	Standalone 25 MHz-Mil, 35 MHz-Com
67413A		25 MHz Com
74S225	16x5	10 MHz Com
74S225A	16x5	20 MHz Com
67417A	64x8/9	Serializing FIFO 28 MHz serial rate 10 MHz parallel rate

Table 1. FIFO Family

Classes of FIFO Applications

The two principal uses for the 67401 FIFO are data rate matching and data buffering. Actually these classes overlap somewhat because data rate matching implies data buffering within the FIFO in order to achieve the objective or writing into the FIFO at one rate and reading out of the FIFO at another rate. It is also apparent that you cannot write at one rate and read at another rate continuously without eventually filling (fast write, slow read) or emptying (slow write, fast read) any fixed length FIFO memory. Once the FIFO is full, it cannot accept additional data until it begins to empty due to reading or clearing its contents.

In the other case, once the FIFO has been emptied, it makes no sense to continue reading until more data has been written. This limitation implies that the faster rate operation (whether reading or writing) must be done in bursts with gaps between bursts to allow time for empty storage space to be created within the FIFO by the slower rate operation.

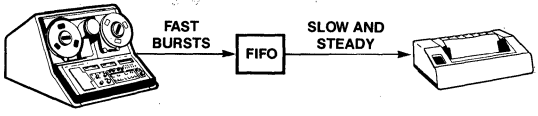

Figure 2. Data Transfer from Magnetic Tape Unit to Printer

High-Speed Burst to Lower Speed Steady Rate

Figure 2 shows a magnetic tape unit supplying data to a line printer. The printer prints characters at a regular rate that is slower than the magnetic tape unit can supply characters (Figure 3).

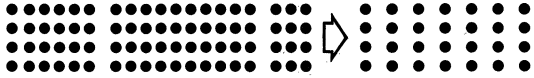

Figure 3. Fast Rate to Slow Rate

It is usually inconvenient and expensive to require the MTU to stop and start between characters to wait for the printer. The MTU operates more efficiently by writing a burst of characters at its fixed high rate into the FIFO then waiting for the printer to read the FIFO at its fixed low-speed rate. When the FIFO buffer becomes empty (or almost empty), it can notify the MTU to supply another burst of data. The FIFO's Output Ready signal can be used as an interrupt. It may be convenient to size the FIFO at the maximum line length so that the MTU can reload the FIFO whenever it sees a carriage return. Figure 4 shows a similar application where the printer is being driven from a high-speed computer. By sending bursts of data to the printer, the computer is free between bursts to perform other tasks, such as processing the data to be printed. The practice of storing high-speed bursts in the FIFO and reading at a slower steady rate is useful for many high-speed burst data sources such as disk memories, random access memories, and high-speed data communications links. The printer is typical of a number of fixed rate slow-speed devices such as a paper tape punch, analog-to-digital converter, or a telephone data link.

Direct Memory Access (DMA) is often used as a solution to this kind of rate matching problem. With DMA, the computer stores data in its RAM at the high-speed burst rate. The slow-speed device then reads the RAM directly at its leisure. This method, however, requires a considerable amount of hardware to implement the DMA operation. Because of its simple logic structure the FIFO permits a reduction in hardware.

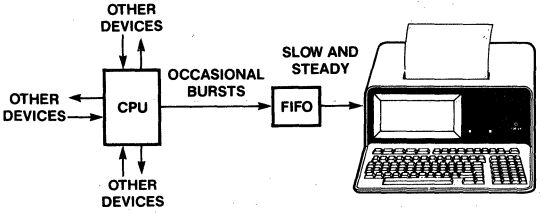

Figure 4. Data Transfer from Computer CPU to Printer

Low-Speed Steady Rate to High-Speed Burst

Another common situation in digital data transmission is shown in Figure 5. Here the source of data operates at a slow steady rate, while the data destination device is capable of higher speed burst reception. This is illustrated by a paper tape reader supplying data to a high-speed CPU in Figure 6. If the computer were required to read the paper tape reader directly in a programmed I/O operation, it would spend most of its time waiting for the reader to advance. This is a common occurance in microcomputer software development systems. If the computer can be used for other tasks while it is reading the tape, its operation becomes more efficient and its throughput is higher. Using the FIFO, the tape reader stores the incoming data at its natural rate. The computer reads the FIFO at its maximum input rate until the FIFO is empty or until the computer turns its attention to another task. This slow rate to fast burst operation is appropriate for source devices such as analog-to-digital converters and telephone modems. The destination devices could be a magnetic tape, disk, or CRT display operating at speeds up to 15 MHz.

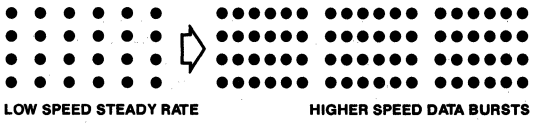

Figure 5. Slow Rate to Fast Rate

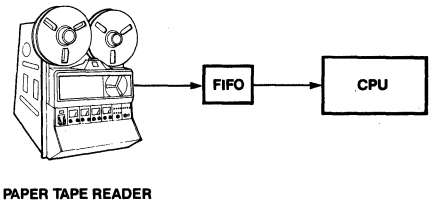

Figure 6. Data Transfer from Paper Tape Reader to CPU

Steady Rate to Erratic Rate

Figure 7 illustrates a situation where data is available from a source at a fixed rate, but is used by the destination devices at an erratic or unpredictable rate. One example of this situation is a printing terminal receiving data from a telephone modem connected to a timeshare computer (Figure 8). The computer and modem transmit the data at a steady rate, say 300 baud. The printer prints at a steady rate until it gets a carriage return character. The printer may then require several character times to execute the carriage return before it can print the characters that follow. This problem can be solved using the FIFO as a buffer so that the characters following the CR are stored in the FIFO and printed at the natural rate of the terminal. Note that the interval between printing successive characters must actually be slightly faster than 300 baud so that the printer can catch up after each carriage return. Otherwise, the FIFO would gradually fill up and overflow. This is a fundamental characteristic of FIFO buffers. In all cases the average input data rate over a long period of time cannot exceed the average output data rate. In practice the size of the FIFO is determined by the duty cycle of the higher data rate as well as the ratio of input rate to output rate.

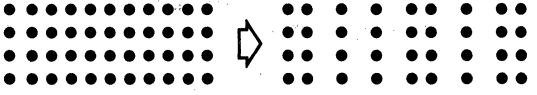

Figure 7. Steady Rate to Erratic Rate

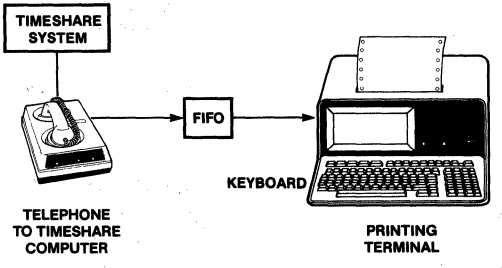

Figure 8. Timeshare Computer System to Printing Terminal

Another example of steady to erratic data rate is the interface to a machine tool such as the turret drill shown in Figure 9. The FIFO is used to store commands received from magnetic tape at a steady rate or a high-speed burst. The execution of these commands varies depending on the mechanical operation required. Changing drills may require much longer than drilling a series of holes.

In some numeric control systems the instructions for a whole shop full of machine tools may be provided by a single shared computer. In this case, FIFOs can be used in each machine tool to store a burst of instructions. Then the computer is free to control other machines, check status, or execute maintenance operations while each machine continues executing commands stored in its own FIFO memory.

The example in Figure 12 shows a digital system using a large high-speed host computer to control a multitude of slower slave computers (possibly microprocessors). The host computer transmits high-speed bursts of commands and data to microprocessors connected to its I/O bus. These are stored in FIFOs and executed by the microprocessors at their own rates. The host computer can control a large number of microprocessors and service its own peripheral devices in either timeshared or multiprocessing mode. Each individual microprocessor uses FIFOs to accumulate results and status information to be polled by the host periodically. In addition each microprocessor operates at its effective rate by buffering its I/O operations in FIFOs. The whole system is connected to a remote control radio link using a FIFO to adjust the data rate between the receiver and the host computer.

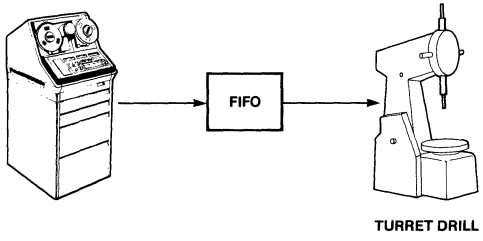

Figure 9. Magnetic Tape Unit to Turret Drill

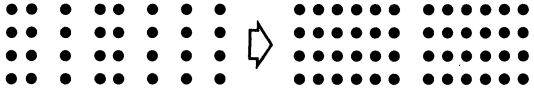

Figure 10. Erratic Rate to Steady Rate with Gaps

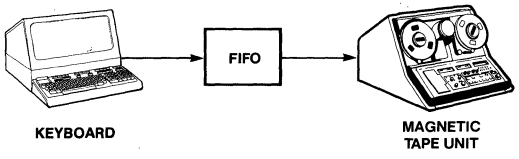

Figure 11. Keyboard to Magnetic Tape Unit

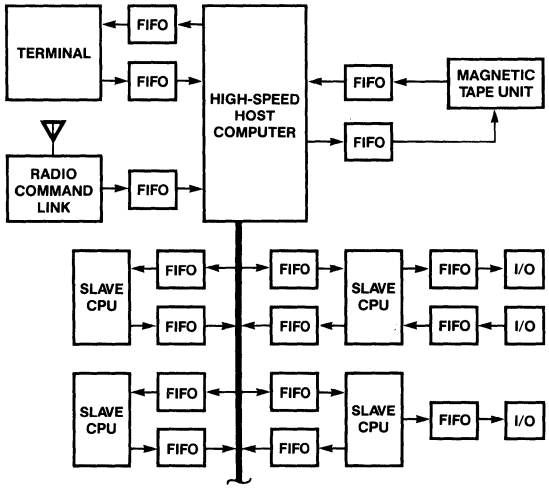

Figure 12. Multiple Processors Receive High-Speed Burst Commands, Execute at Slower Rate, Accumulate Status Information at Slow Rate and Transmit Status at Burst Rate when Polled

Erratic Rate to Steady Rate

In many cases data is transmitted at an erratic or unpredictable rate, but must be formed into steady high-speed bursts (Figure 10) to be efficiently used by the receiving device. A typical example of this situation is the keyboard to tape machine shown in Figure 11. The information is generated by the keyboard operator at a very erratic rate. The FIFO is used to avoid starting and stopping the tape at irregular intervals to record single characters. As a result, the tape unit can record data in longer records, thereby saving tape and saving the higher cost of an incremental tape recorder.

Skew Buffering

Up to this point all the examples we have considered have involved parallel words of digital data where each bit in each word was transmitted simultaneously with the other bits in that word. In high-speed magnetic tape readers and other high-speed devices, this may not be a realistic assumption. Figure 13 shows a hypothetical 4-bit magnetic tape system reading four parallel tracks from a tape. Before this data can be used in a digital system, it must be amplified, properly formatted and stored in an output register. Usually the individual bits of a given data word have been skewed with respect to each other during the record and playback operations. The actual data from the tape heads may look something like Figure 14. In some systems individual bits may be skewed as much as three words away from their companion bits. Deskewing the signals from the tape is an ideal application for the high speed of the 67401/A/B FIFO. In such systems there is usually other information about the skewed bits that can be detected and used to help deskew the data. In this application a separate FIFO must be used for each parallel bit of raw data. The remaining three bits of the FIFO may be used to buffer other data relating to the raw data. In our 4-bit example, skewed data is stored in bit zero of four parallel FIFOs and deskewed data is read at their outputs at the same average word rate for input and output.

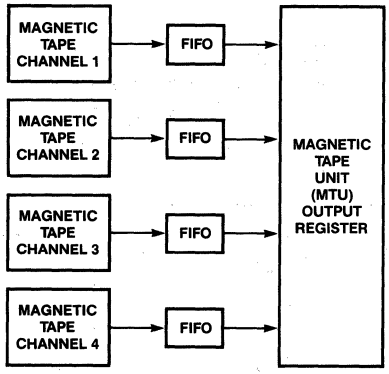

Figure 13. Magnetic Tape Lead to MTU Output

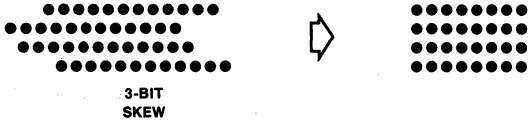

Figure 14. Magnetic Tape Deskewing

Data Buffering for Delay

In many applications the read and write rates of the FIFO are the same and may even be synchronized. This occurs when the data originating from the source must be delayed before it can be accepted by the destination device. If the destination for the data is a computer and it is occupied by controlling the source while the data is being generated, then the source data can be stored in the FIFO until the computer is freed from that task. Then it can immediately begin processing the data from the FIFO in the order that it was generated.

FIFO Detailed Description of Operation

The Monolithic Memories' 67401 (Figure 15) is a high-speed, bipolar FIFO with a capacity of sixty-four 4-bit words. Four data lines, an active high READY status signal, and a clock input are provided for both the input port and output port. Also provided is a master reset signal that logically clears the FIFO to the empty condition.

Data is entered into the first stage of the FIFO whenever the "AND" of the INPUT READY output signal and the SHIFT IN signal makes a LOW-to-HIGH transition. The device acknowledges the acceptance of data into the first stage by providing a LOW output on the INPUT READY line. The data then remains in the first stage until the SHIFT IN signal and INPUT READY signal are both LOW, and the next memory cell is empty. The device then passes the data from the input stage to the next memory cell thus freeing the input stage to accept another word. The device indicates the ability to accept the next word by providing a HIGH output on the INPUT READY pin.

Internally the data is passed from one cell to the adjacent downstream cell, as soon as the adjacent downstream cell is empty. This internal transfer operation occurs at a higher rate than data can be written into and read from the device.

The output stage is loaded with new data whenever it is empty and the next stage upstream is not empty. The loading of the output stage is indicated by the OUTPUT READY signal making a LOW-to-HIGH transition. A specified delay time after both OUTPUT READY and SHIFT OUT signals are HIGH, the OUTPUT READY signal will go LOW. The output becomes empty when the SHIFT OUT signal makes a high-to-low transition. The timing diagram for these operations is shown in Figures 16 and 17.

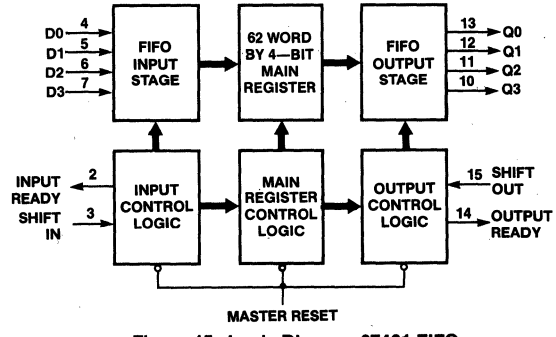

Figure 15. Logic Diagram 67401 FIFO

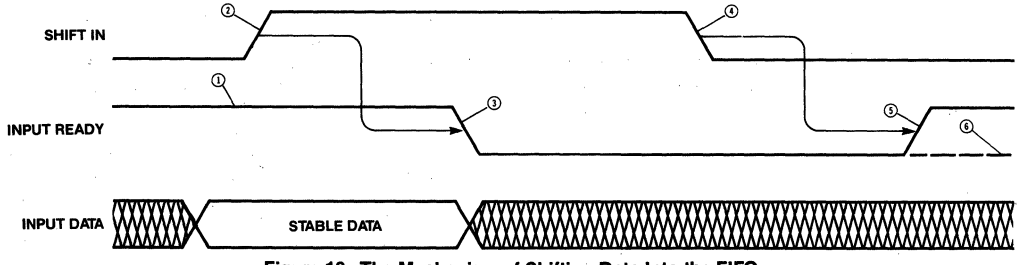

Figure 16. The Mechanism of Shifting Data Into the FIFO

① Input Ready HIGH indicates space is available and a Shift In pulse may be applied.
② Input Data is loaded into the first word.
③ Input Ready goes LOW indicating the first word is full.
④ The Data from the first word is released for "fall-through" to second word.
⑤ The Data from the first word is transferred to the second word. The first word is now empty as indicated by Input Ready HIGH.
⑥ If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.
Note: Shift In pulses applied while Input Ready is LOW will be ignored.

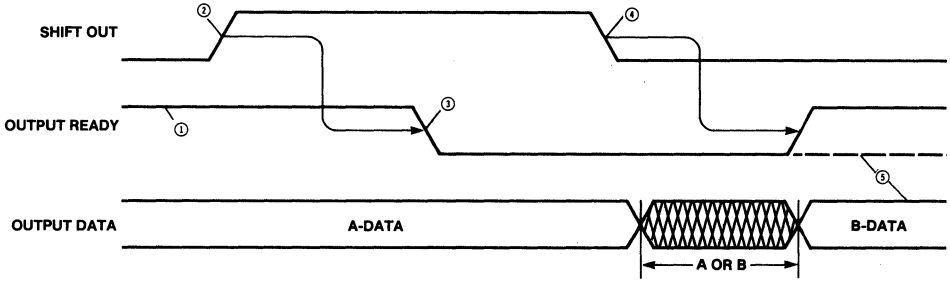

Figure 17. The Mechanism of Shifting Data Out of the FIFO

① Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.
② Shift Out goes HIGH causing the next step.
③ Output Ready goes LOW.
④ Contents of word 62 (B-DATA) is released for "fall-through" to word 63.
⑤ Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.
⑥ If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

On Cascading Issues

FIFOs sometimes have insufficient depth or width for a particular application. These FIFOs can be cascaded to increase the depth and expanded to increase the width of the data word. In order to expand the width the shift-ins of all the FIFOs should be tied together. Figure 18 shows the technique for implementing a 64x12 FIFO with 67401/A/B. IR and OR signals from all the FIFOs should be tied separately as shown. Also the shift-out clocks and the master resets of all the FIFOs should be tied together.

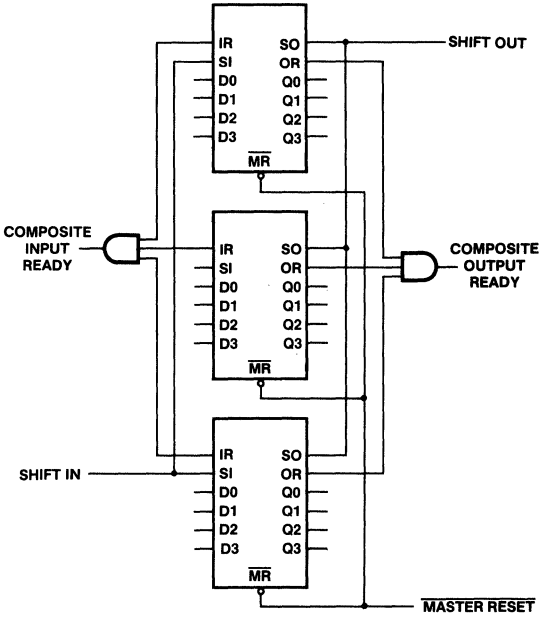

Figure 18. 64x12 FIFO with 67401/A/B

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags due to the different fall-through times of the FIFOs.

For a greater depth (increasing the number of words that can be stored in the FIFO) the technique is ahown in Figure 19. The Output Ready of the first FIFO becames the Shift-In for the second FIFO, while the Input Ready of the second FIFO becomes the Shift-Out for the first FIFO. Figure 19 shows the implementation of a 128x4 FIFO. The handshake which takes place between the two FIFOs is shown in Figure 20. After the master reset is asserted LOW the input ready of both the FIFOs goes HIGH waiting for data to be shifted in. When a word is shifted into the first FIFO it ripples to the outputs of the first FIFO, which are actually tied to the inputs of the second FIFO.

Once the data has rippled to the outputs of the first FIFO, it finds that Shift-Out was already HIGH (since it is connected to Input Ready 2, which was HIGH to indicate the second FIFO's ability to accept another piece of data). Thus, Output Ready 1 goes HIGH.

This instantly causes Shift-In 2 to go HIGH, telling the second FIFO to accept the data on its inputs. After a time tIRL, then Input-Ready 2 goes LOW. This means Shift-Out 1 also goes LOW, telling the first FIFO it can place the next data on its outputs.

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the FIFOs themeselves.

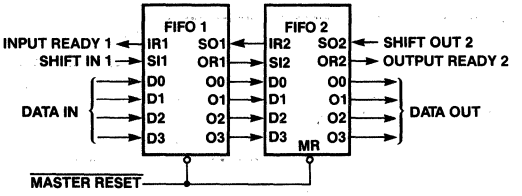

Figure 19. Cascading FIFOs to Form 128x4 FIFO with C5/C67401A/1

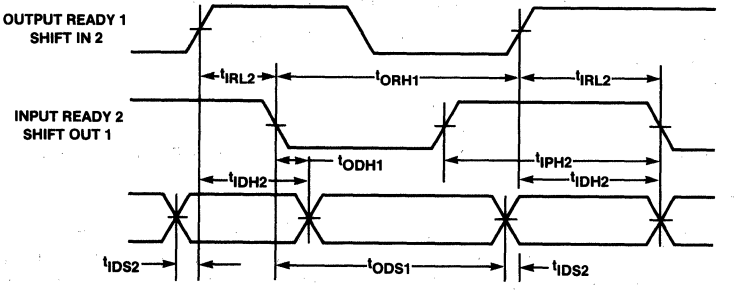

Figure 20. Handshake Timing

Some Design Considerations

A FIFO is an asynchronous device, hence great care should be exercised in designing with FIFOs. VCC should be clean, as noise on VCC can cause multiple shift cycles, internally. A recommendation is to add an 0.1-μF disk capacitor between VCC and GROUND. FIFOs should not be used to drive long lead lengths because of sensitivity to reflections. Always Master reset before starting any FIFO operation. Shift-In (SI) and Shift-Out (SO) rise and fall times are also important. It is recommended to use a Schottky device as a driver, to avoid multiple shift-ins.

Application Examples

UART to CPU Data Buffer

A UART is an MOS/LSI device designed to provide the data interface between a serial communication link and data processing equipment. When transmitting serial data the UART accepts parallel data bytes from the computer's data bus, converts to serial data, and adds start, parity, and stop bits. The receiver section of the UART accepts serial data from a transmission line, modem, or terminal, validates the data by checking proper start, parity and stop bits, and converts the data to parallel bytes to be read by the computer on its data bus. In effect, the UART is a monolithic serial I/O port for the computer. Serial data rates up to 9600 baud are permitted by the UART, but much slower rates (110 to 300 baud) are commonly used to interface terminals. 110 baud corresponds to 10 bytes per second at the data bus. FIFOs can be used between the computer's data bus and the UART in both receive and transmit mode to match the low serial transmission rates to high speed bursts that make much more efficient use of the computer's time and memory space. A logic diagram for this interface is shown in Figure 21. Four 67401 FIFOs are connected in a series/parallel arrangement for both the transmit and the receive buffers. This arrangement permits a 128-byte buffer capacity for transmit and 128 bytes for receive. The buffers can be expanded easily in both width and length to accommodate different computers or greater buffer capacity.

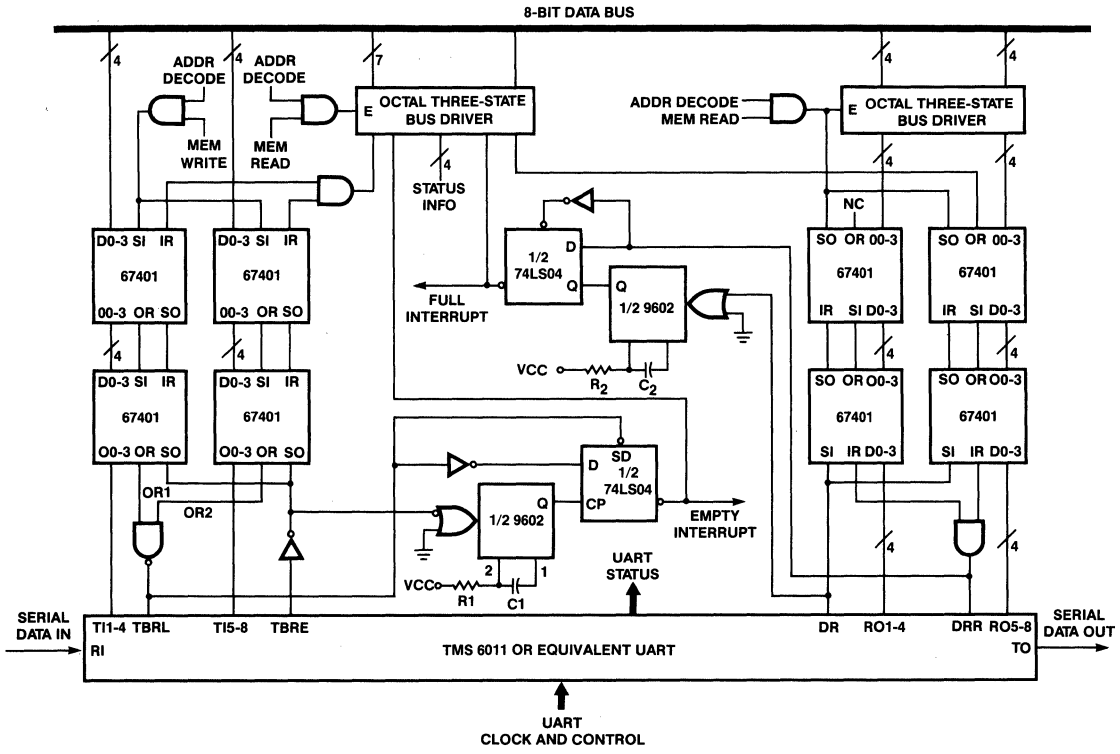

Figure 21. UART Data Buffer Logic for XMIT and RCV Using 67401 FIFOs

Transmit Buffer Operation

The interface shown in Figure 21 allows the computer to write bursts of up to 128 bytes at the maximum data rate of the computer into the 67401 FIFO array. The input ready signals are ANDed together and fed back through a status port to the computer data bus so that burst data may be written under program control as rapidly as the write program will allow. The UART reads the outputs of the FIFO array one byte at a time, adds start, stop and parity bits and serializes the data to the serial output at the desired transmission rate (assumed to be much slower than the input burst rate). Assuming that the FIFO array is initially empty, the operation proceeds in accordance with the timing diagram in Figure 22. When the first parallel byte reaches the output of the buffer, the Output Ready lines go high. When both OR1 and OR2 have gone high, the NAND gate drives the UART's Transmit Buffer Register Load (TBRL) signal low. After the tPHL delay in the UART, the Transmit Buffer Register Empty (tBRE) signal goes LOW, causing the UART to begin shifting out the serial data. tBRE is inverted and a HIGH signal is fed back to the shift out (SO) inputs causing the Output Ready lines to go LOW. When all bits have been shifted out of the transmit buffer register and tBRE is returned HIGH, SO is driven LOW. After the internal FIFO delay tORH the OR lines return HIGH if a new byte is available at the output of the FIFO and the process repeats until the buffer is emptied.

Transmit Buffer Empty Logic

In many applications of the 67401 FIFO it is necessary to determine when the transmit buffer is empty or the receive buffer is full. The logic required to provide both these signals is shown in Figure 21.

The 67403D from Monolithic Memories features two status flags: a Half-Full flag and an Almost-Full/Empty flag. These status flags can be used to signal to the system that the FIFO is approaching an empty state or a full state.

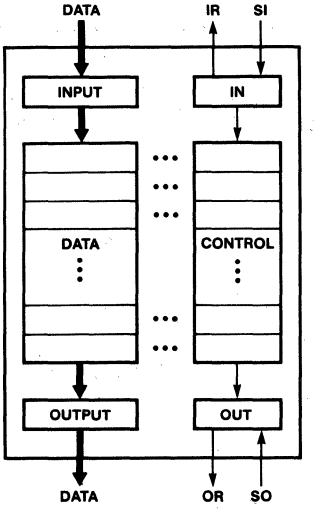

Figure 3. Fall-through, Single-stack, FIFO Architecture

A new approach to the design of FIFOs significantly enhances their maximum operating frequency by blending these two architectures. This hybrid approach, used in the design of the 57/67413A at Monolithic Memories, is a mix of mostly fall-through or "stack" architecture with a small amount of pointer operation i.e., RAM-based technique.

When a word of data is written into the "Fall-through" FIFO, it "trickles down" and stacks on top of the residing words. When a word is read out, an empty location is created at the bottom and all residing words drop down, making the empty location "bubble up."

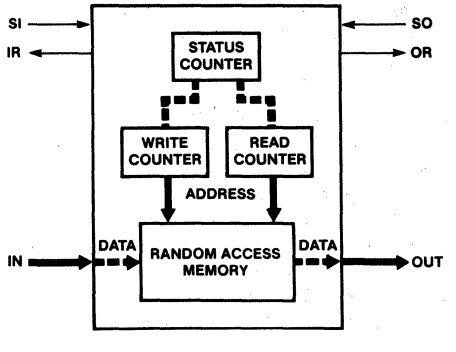

Figure 4. RAM-based FIFO Architecture

A RAM-based FIFO consists of a memory array, a write address counter, a read address counter, and a status counter/subtracter. When a word is entered into the FIFO, it is written into the location pointed by the write address counter. The counter is then incremented to point at a subsequent location. The read address counter is used to point at the location of a word which is read out of the FIFO. A subtracter can be used to keep track of the difference between these two counters and signal when the FIFO is full or empty. In order to achieve high speeds, "ring" address counters and a comparator are used instead of traditional binary counters and a subtracter.

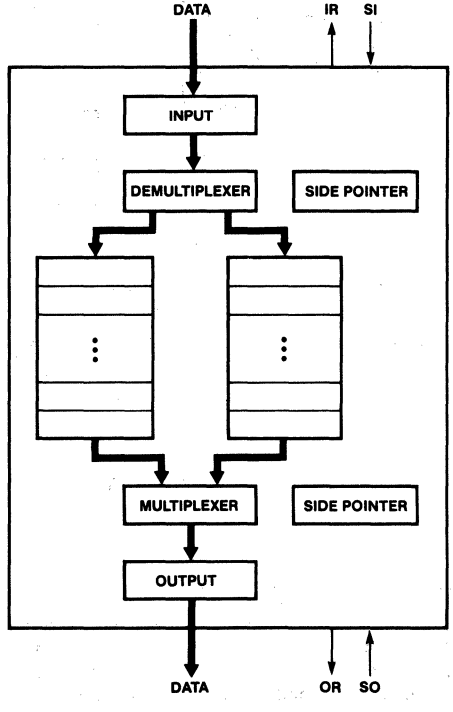

Figure 5. '413 Dual-stack, Hybrid Architecture

The internal architecture of Monolithic Memories' 57/67413 FIFO incorporates a dual stack and a pointer to double the maximum frequency and halve the fall-through time. The 57/67413 has sixty-four words, of five bits each, arranged in two separate thirty-two word "fall-through" stacks, an input port, an output port, and two side pointers. The input port and the output port each generates its own handshake signals. The input side pointer controls the demultiplexing of incoming data into the two stacks, and the output side pointer controls the multiplexing of the outgoing data from the two stacks onto the output port. The multiplexer and demultiplexer are incorporated in the input and output ports.

High-Speed Disk Memory Buffer

A common computer interface requirement is a high-speed serial data interface to a disk memory or other high-speed device. Data is often formatted into records, tracks or other blocks that can be taken together and transmitted as a burst. In the case of a high-speed, high-density disk the data transfer must be made when the desired data passes by the read head. In order for the computer to use this data it must be converted to parallel data words the size of the computer's basic data word and then resynchronized at a parallel word rate that is convenient for the computer. The reverse of this operation is required to write serial data from the computer to the disk. The logic block diagram (Figure 24) shows a method for accomplishing both serial-to-parallel read and parallel-to-serial write using 67417, 67401 and 67402 FIFOs to buffer 16-bit data words between a microcomputer and a high-speed disk. Serial data rates up to 10 MHz are possible with the components shown in the diagram.

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Second Generation FIFOs Simplify System Design and Open New Application Areas

Zwie Amitai, Barry Hoberman and Nusra Lodhi

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First-In First-Out (FIFO) memories are devices used to buffer between subsystems which have different data rates. Recent innovations in FIFO architecture resulted in a still faster FIFO semiconductor device — Monolithic Memories' 67413 — which operates in frequencies exceeding 35 MHz. New application areas induced the design and development of system-oriented FIFOs: the 54/74S417 Serializing FIFO which incorporates serial-to-parallel and parallel-to-serial conversion on the same chip, and the 4219 FIFO RAM Controller, which is used with an array of static RAMs to create very deep FIFOs (up to 64K deep) of indefinite width.

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Introduction

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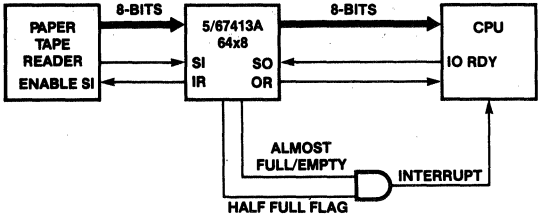
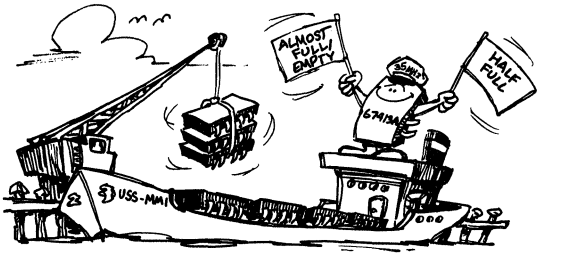


Figure 1. Slow Steady Rate to Fast 'Blocked Rate' FIFO Applications

FIFO Architectures Exhibit Performance Trade-offs

A FIFO — First-In First-Out — is a dual port memory, from which data can be read only in the same order in which it was written. A FIFO has two independent ports: an input port and an output port. Each port has a READY output and a SHIFT input, which allow the system to access the FIFO. Newer FIFOs have additional "status" flags. The 67413 has a HALF-FULL flag and an ALMOST-FULL/EMPTY flag. The ALMOST flag indicates to the system that an action has to take place to maintain the data flow. The HALF-FULL flag is used to determine which action must take place: start filling or start emptying the FIFO to maintain continuous data flow (Figure 2).



"...THE STATUS FLAGS ON THE HIGH-SPEED '413A FIFO INDICATE WHEN THE FIFO IS CLOSE TO BEING FULL OR CLOSE TO BEING EMPTY, OR MORE OR LESS THAN HALF FULL..."

There are two approaches to FIFO internal architecture. One is the "Fall-Through" architecture based on shift-register technology such as in Monolithic Memories' 57/67401/2. The other approach, the "RAM-based" approach, uses a random access memory (RAM) array and pointers (i.e. counters) that keep track of the order of the data read and written. An extreme case of the latter architecture is a FIFO constructed from an array of memory chips and an LSI FIFO RAM Controller that consists of the above mentioned counters/pointers and control logic. Each approach has its advantages and drawbacks. A successful compromise between these two architectural approaches led to the 67413's unique architecture allowing super-fast operation with a relatively low fall-through time.

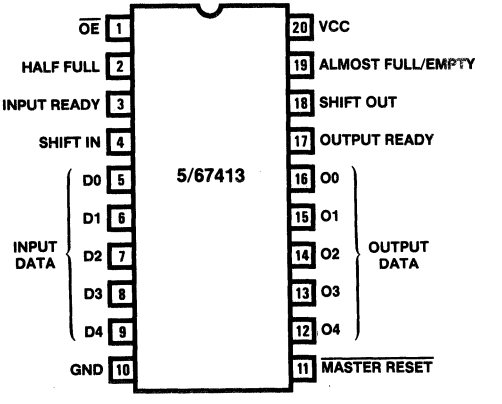


Figure 2. 67413 Pin Configuration

Receive Operation

The receive buffer logic is shown in the right hand portion of Figure 21 and the timing diagram is shown in Figure 23. The UART receives serial data with start, stop, and parity bits, evaluates parity, and converts the data to parallel bytes to be stored in the FIFO at the slow or erratic receive rate. The Data Ready (DR) signal of the UART is tied to SI on the two FIFOs and the two IR lines are ANDed together to drive the Data Ready Reset (DRR) line of the UART. When the FIFO is ready to accept a byte of data from the UART, the AND of the two IR signals holds DRR HIGH. If the UART has a new byte, it sets DR HIGH, driving SI HIGH to enter the new data into the input register of the FIFOs. After the tIRL delay, IR goes LOW driving DRR LOW. After the tPHL delay in the UART, DR goes LOW driving SI LOW. If the FIFO is not full, IR returns HIGH after tIRH indicating to the UART that the FIFO is ready for the next byte. This cycle repeats until the UART has no more data or the FIFO buffer is full.

Within the FIFOs each new data byte propagates to the top of the available storage until the computer decides to read the stored words at its higher burst rate. The FIFO outputs drive a three-state bus driver interface to the computer data bus. 67403 has a three-state capability. The OR signal is available to the computer via the status port which can be sampled periodically by the computer to determine when new data is available. The computer program initiates data transfers to the bus at its maximum rate by enabling the three-state buffer for each byte and checking the status port between each read cycle.

If the UART fills the FIFO buffer before the computer can get around to dumping it, the almost-full flag generates an interrupt.

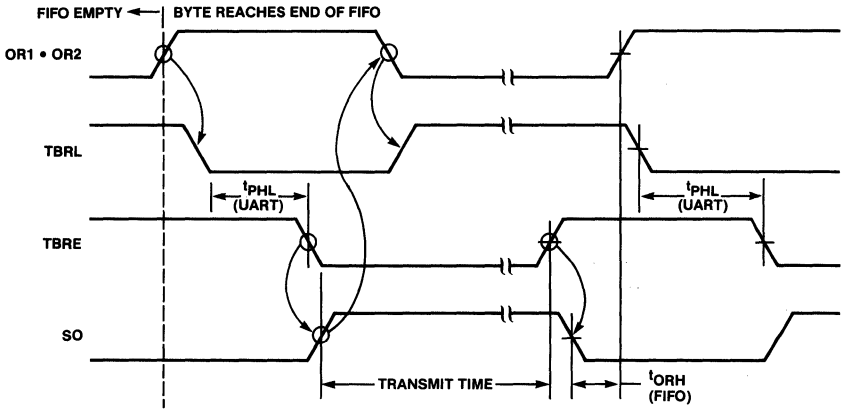


Figure 22. Timing Diagram, Transmit Buffer Operation

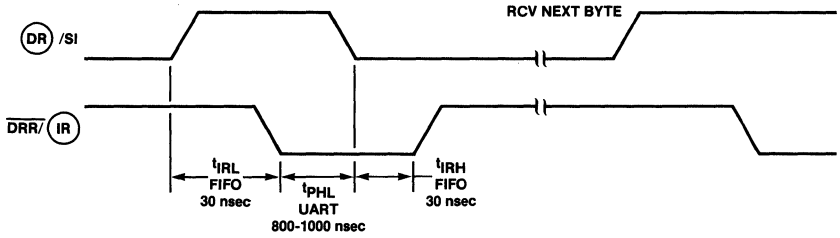


Figure 23. Timing Diagram, Receive Buffer Operation

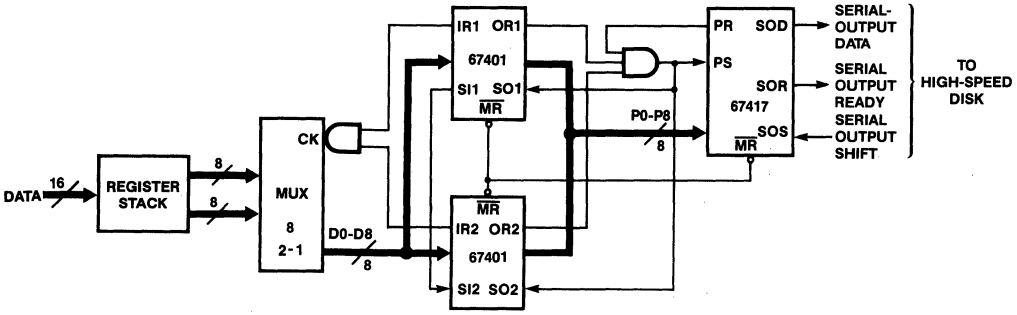
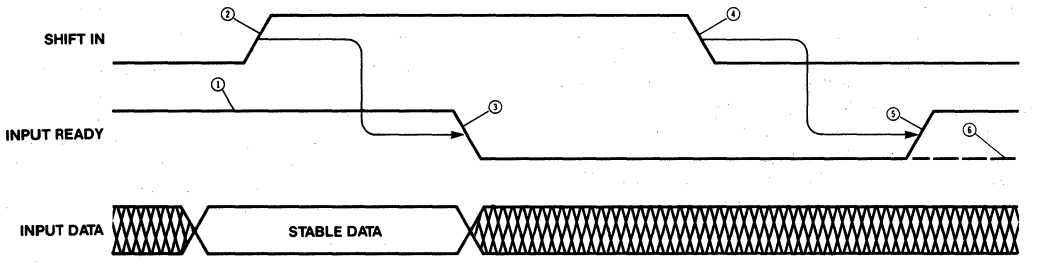
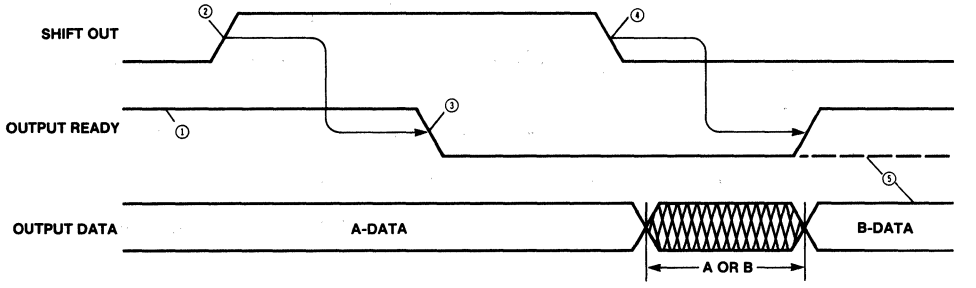


Figure 24. High-Speed Serial Interface



① Input Ready HIGH indicates space is available and a Shift-In pulse may be applied.
② Input Data is loaded into the first word. The Data from the first word is released for "fall-through" to second word.
③ Input Ready goes LOW indicating the first word is full.
④ Shift-In going LOW allows Input Ready to sense the status of first word. The first word is now empty as indicated by Input Ready HIGH.
⑤ If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.
NOTE: Shift-In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

Figure 6A. The Mechanism of Shifting Data into the FIFO



① Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
② Shift-Out goes HIGH causing the contents of word 62 (B-Data) to be released for fall-through to word 63. Output data remains as valid A-Data while Shift-Out is HIGH.
③ Output Ready goes LOW.
④ Shift-out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
⑤ If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data becomes invalid.

Figure 6B. The Mechanism of Shifting Data Out of the FIFO

The above internal scheme is transparent to the user, who is required only to conform to the FIFO's simple, asynchronous handshake protocol. Two signals: Input Ready (IR) and Shift Out (SO) control the data flow into the FIFO (see Figure 6A). Two signals: Output Ready (OR) and Shift Out (SO) control the data flow out of the FIFO (see Figure 6B). A Master Reset ($\overline{MR}$) signal is provided to clear the FIFO. The master reset must be pulsed (LOW) after power-up to prepare the FIFO to accept data in the first location.

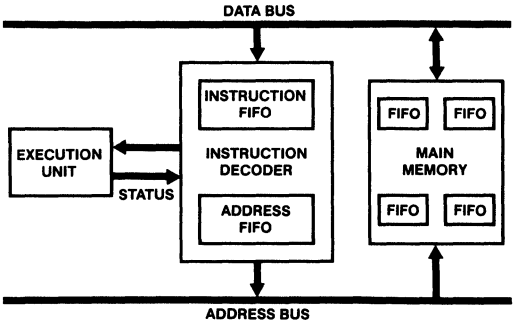


Figure 7. High-speed Processor Architecture

FIFO Interface Allows Subsystems to Operate at Independent Rates

In pipelined architectures, as shown in Figure 7, a number of events take place concurrently. Instructions are fetched from the memory into a cache, instructions undergo processing in the Instruction Decoder, and the output of this unit initiates the sequence of executable microinstructions.

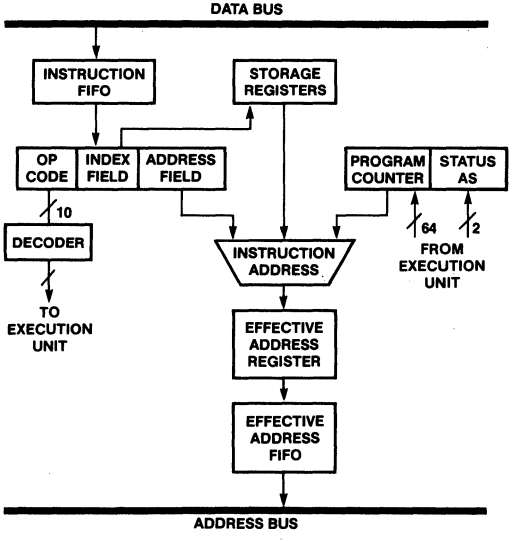


Figure 8. An Instruction FIFO and an Effective Address FIFO in a Basic Instruction Decoder

The concept of "free-running," independent subsystems that are interfaced via FIFOs can be further carried to the main memory section. Here, too, efficient choices of the data bus speed and address bus speed do not necessarily match the inherent speed of the main memory. Four FIFOs can simplify the interface of the main memory to the address and data buses, as shown in Figure 9.

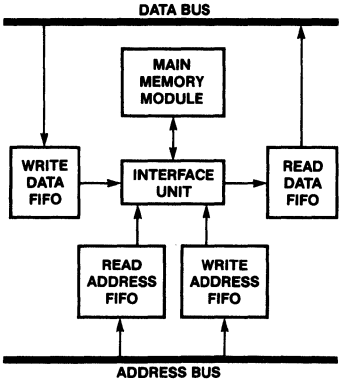


Figure 9. Four FIFOs Simplify Main Memory Interface

4

In order to achieve high throughput, the instructions are queued in an instruction FIFO, and the instruction lookahead can operate on the instructions independently of the data bus operations. A basic function of the instruction decoder is to compute and provide an effective address to the address bus (Figure 8). Once again, the rate of the address generation must fit the rate at which the addresses are needed. An effective address FIFO simplifies the design of the system sections, enabling each to operate independently, as long as their average throughputs are the same. The high speed of the 67413 (35 MHz), and its short fall-through time make it a natural candidate for this task. A three-state output stage with high drive can directly drive a bus and does away with the additional delay caused by buffers.

Fast FIFOs Capture New Application Domains

The existence of very fast FIFOs brought about new application domains such as data acquisition of fast signals. The following systems exhibit typical high-speed data acquisition techniques using high-speed memory buffers to accommodate data rate differences between the signals and the data logging system. The system shown in Figure 10 detects and stores the pulse rate and frequency of radar signals using a Bragg cell. Both amplitude

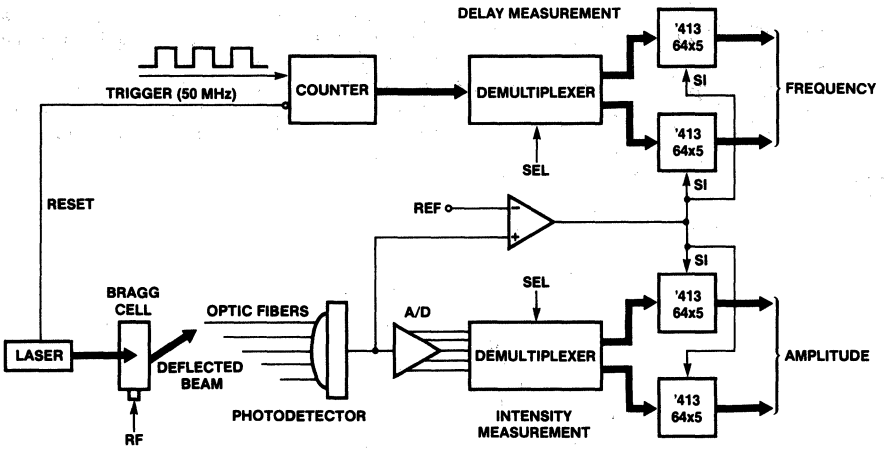


Figure 10. Radar Frequency and Amplitude Acquisition

and frequency data arrive at the rate of 50 MHz and are buffered by FIFOs. A Bragg cell translates the frequency of the radar signal into a deflection of a laser beam, and the amplitude of the radar signal into the intensity level of the laser beam. The deflected laser beam hits one or two fibers out of a collection of fibers of different lengths, that are connected to a photocell. The signal arrives at the photocell after a delay determined by the length of the fiber. Therefore, the delay relates directly to the radar frequency. A counter is used to measure the delay. The counter is reset when the laser beam is triggered, and once the beam is detected at the photodetector, its contents are written into a buffer. This technique is quite general and can be used also for pulse rate measurement. The laser beam intensity is sampled, converted to a digital format, and written into another buffer. Two FIFOs and a multiplexer are needed for each buffer to allows data rates over the FIFO's 35-MHz maximum operating frequency up to 70 MHz.

Another data acquisition application is a Particle Flight Detector. Due to the nature of the observed phenomena, the data coming out of a Particle Flight Detector is generally in short bursts. The temporal frequency of the data exceeds 30 MHz while the average rate of the data stream is much lower, and can be handled by a standard bus such as the SYSBUS (32-bit, 10-MHz international standard bus for physics instrumentation). The block diagram shown in Figure 11 utilizes an array of 35-MHz FIFOs to handle the bursts of data and two arrays of static RAMs to ensure maximum bus throughput.

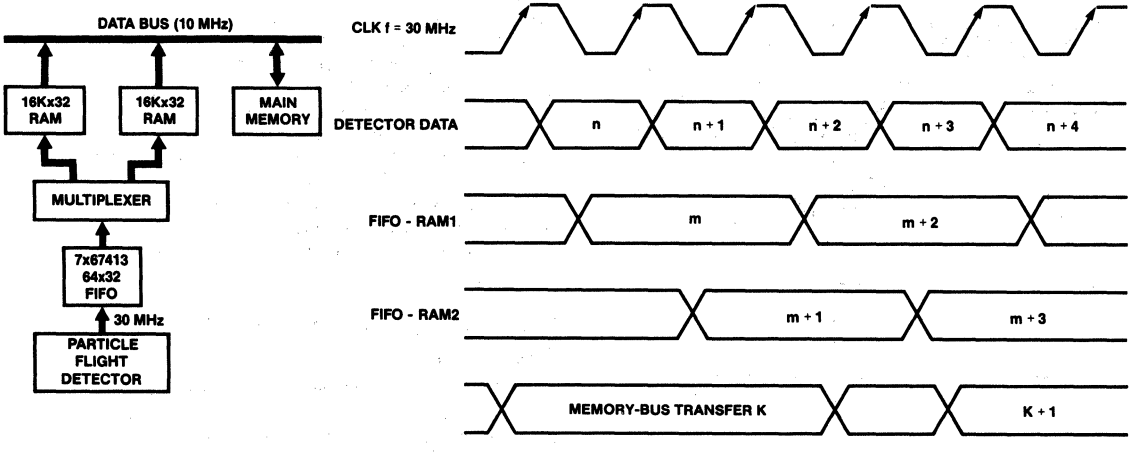


Figure 11. Particle Flight Detector Interface to a 10 MHz Bus (SYSBUS)

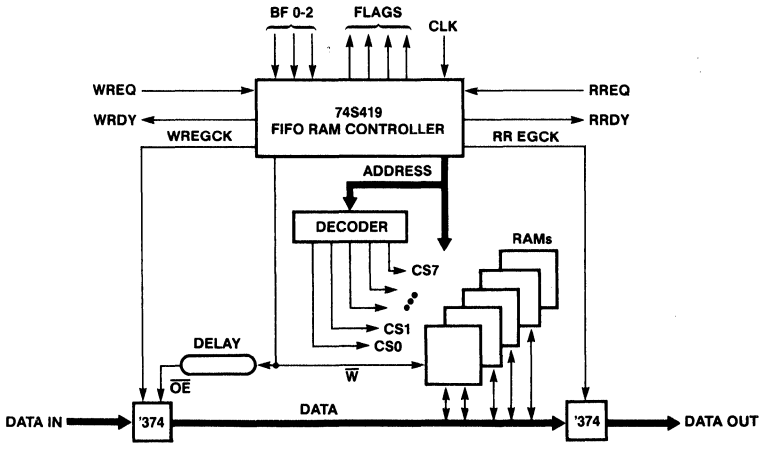
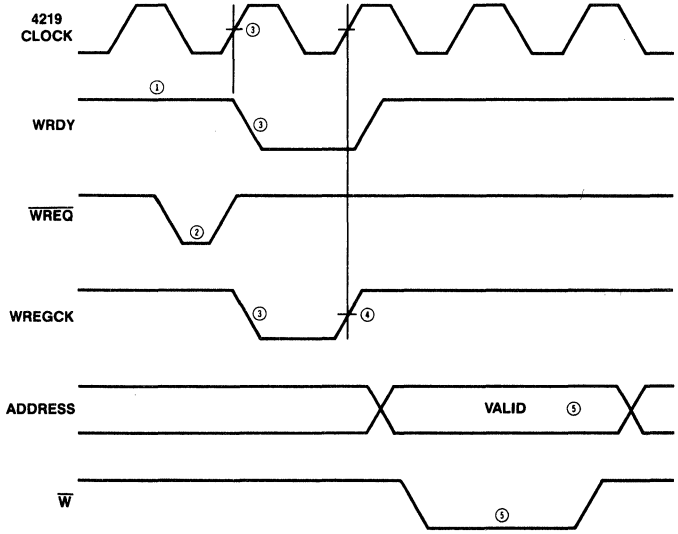


Figure 12. A FIFO RAM Controller and Static RAMs Make a Very Deep FIFO of Variable Width

Very Deep FIFOs Implemented by an LSI Controller and a Static RAM Array

The search for system-oriented LSI solutions for very deep buffers, such as those needed for communication networks, resulted in the development of the FIFO RAM Controller which can make a static RAM array look like a FIFO (see Figure 12). The 54/74S4219 FIFO RAM Controller integrates all address generation and status detection needed to control the static RAMs, giving the system designer two simple "handshake" signal sets for input (write) and output (read) operations. A read counter and a write counter provide the read and write addresses, while an up-down counter keeps track of the difference between these two counters.. The status flags include the FULL, EMPTY, ALMOST-FULL/EMPTY, and the HALF-FULL flags, and are generated according to the buffer length selected. The buffer length can vary from 512 to 64K words, and the maximum data rate at each port exceeds 15 MHz. Arbitration between read and write requests is done in the controller according to priority rules pin-selected by the user.



① WRDY is HIGH; new Write requests may be made.
② A Write request is made (WREQ pulled LOW) asynchronously of the '4219 clock.
③ The request is synchronized, WRDY goes LOW to indicate that no Write request should be made. WREGCK goes LOW.
④ WREGCK goes HIGH clocking the data into the Write Data Register.
⑤ A Write cycle takes place over two '4219 clock cycles.

Figure 13. '4219 Write FIFO Operation

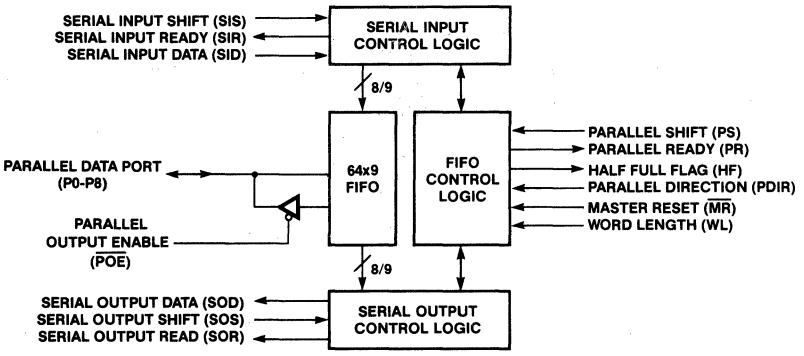


Figure 14. '67417 Serializing FIFO Architecture

The '4219 was designed to isolate the static RAM array from the rest of the system so that the handshake protocol will be similar to the protocol required by most FIFOs. The '4219 generates all the control signals for the static RAMs, and the subsystems on either side monitor two outputs of the '4219 (the Register clock and the Ready) and supply only one control signal (Request). The protocol of the write (input) FIFO transaction is shown in Figure 13. The data must be available at the write data register no later than one '4219 clock cycle after the write request has been asserted. The data may be terminated after WREGCK has gone HIGH clocking the data into the register. The read (output) FIFO transaction protocol is similar. The data is available at the read data register outputs once RREGCK is HIGH. The priority controls and the request enables give the system designer more flexibility in his system design, and allow one subsystem to take either complete control of the FIFO operation, or just priority in case of simultaneous write and read requests.

System Oriented FIFOs Incorporate Serializing/Deserializing Functions

The 67417 is a serializing FIFO intended as a one-chip solution for data buffering and serializing/deserializing operations. It can be successfully used for interfacing parallel-format computing equipment to serial-format data communications and mass memory equipment. The device's architecture (see Figure 14) includes one parallel port for both input and output of parallel-format data, and two serial ports: one for input and one for output. Data flow can be parallel-to-serial, serial-to-parallel, and serial-to-serial. Each port has its own Request-Ready signal pair and is accessed using a simple handshake protocol similar to the one used for most FIFOs.

Most applications of the 67417 conform to the block diagram shown in Figure 15. The ability to change the FIFO's direction may be used to reduce chip count in systems that always empty the FIFO contents before changing the direction of the data transfer. Other applications may use two FIFOs back-to-back to create a FIFO transceiver with serializing/deserializing capability.

The word length of the parallel format can be eight or nine bits (selected by the WL pin), and can be changed when the FIFO is partially full. This feature allows the FIFO to be loaded with 8-bit words and unloaded as a 9-bit FIFO with zeros in the 9th bit locations.

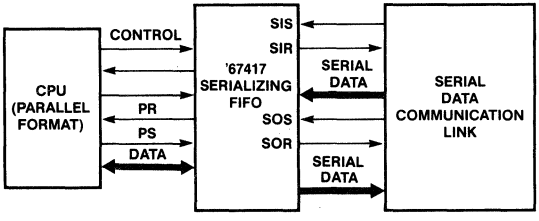


Figure 15. '67417 Serializing FIFO Interfacing a CPU and a Serial Data Communication Link

With the availability of high-speed FIFOs with "system-oriented" features, such as high drive and status flags, system designers can have a more compact and flexible system architecture. New application areas appear for the new FIFOs using their higher speeds and special features.

Advanced
Micro
Devices
AN-177

Cascadability Issues in Advanced Micro Devices' Shallow FIFOs

John McGowan

Abstract

The First-In, First-Out Memory (FIFO) allows the system designer to buffer two streams of data which are running at different rates, even asynchronously. This application note pertains to *cascadable* FIFOs, which can operate as a single-component data buffer, or can be cascaded to form deeper, multi-component, customized buffers. Ensuring that these devices can cascade over a large frequency range, and with asynchronous data streams, requires certain timing criteria to be satisfied. These criteria are the focus of this application note.

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Cascadability Issues in Advanced Micro Devices' Shallow FIFOs

John McGowan

Operation Overview

Small FIFOs are controlled by two signals, Shift In (SI) and Shift Out (SO). There are two status signals generated by the FIFO: Input Ready (IR) and Output Ready (OR). A typical small FIFO pinout is shown in Figure 1.

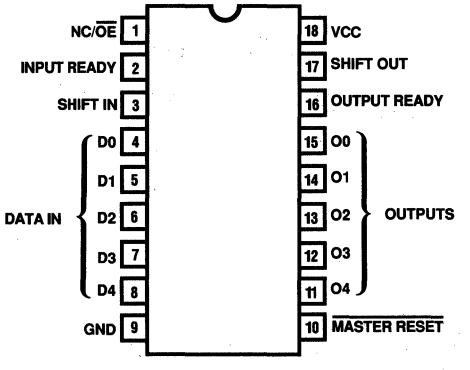


Figure 1. Typical Small-FIFO Pinout

Data is shifted into the FIFO as follows:

1. SI and IR both being HIGH initiates the shift in.
2. The FIFO internally detects a valid shift in by ANDing the SI and IR signals.
3. Data is latched by the FIFO when this valid shift is detected.
4. The FIFO acknowledges the valid shift by bringing IR LOW.
5. The SI line is brought LOW to complete the shift in operation, and to reset the valid shift detect.
6. IR returns HIGH if there is room for new data.

Data is shifted out of the FIFO as follows:

1. SO and OR both being HIGH initiates the shift out.
2. The FIFO internally detects a valid shift out by ANDing the SO and OR signals.
3. The FIFO acknowledges the valid shift out by bringing OR LOW.
4. The SO line is brought LOW to complete the shift out operation.
5. If the FIFO is not empty, OR will return HIGH following SO going LOW. Whenever OR is HIGH, a valid data word is present at the outputs.

The shift in operation is independent of the shift out operation, allowing data to be shifted in at a different rate than it is shifted out. The FIFO indicates that it is full by holding IR LOW after a shift in, and that it is empty by holding OR LOW after a shift out.

Cascading

If a deeper buffer size is required, two or more FIFOs may be cascaded, as shown in Figure 2.

The operation of this buffer is identical to that of the single FIFO buffer. The user controls the shifting of data into the most *upstream* part, and the shifting of data out of the most *downstream* part. This composite buffer has the same handshake (SI, IR, SO, and OR) and data (D0..D4, O0..O4) lines as a single FIFO.

The user has control over the data as it enters and leaves the buffer. The passage of data through the "middle" of the buffer is beyond user control. This data must be capable of being correctly transferred between any of the "middle" devices at a rate greater than or equal to the overall buffer throughput rate.

The point of data transfer between two FIFOs is called the *cascade interface*. There are numerous timing criteria which must be satisfied by the FIFOs on each side of this interface in order to ensure a flawless transfer of data. This is true even for two-FIFO buffers, in which the"middle" of the buffer consists of a single cascade interface. Such criteria must be satisfied at all frequencies within the operating range, and for asynchronous data streams. The following cases illustrate the various timing conditions that may be encountered whenever two or more FIFOs are cascaded.

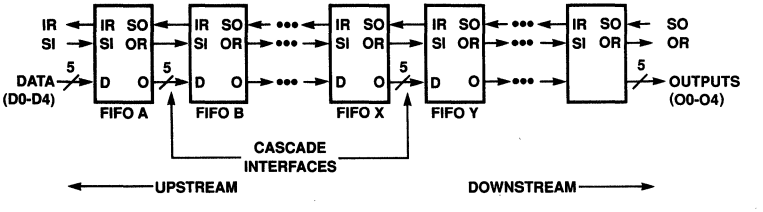


Figure 2. A Cascaded Buffer

Case 1: Low-Frequency Fallthrough

Monolithic Memories' shallow FIFOs are *fallthrough* devices, that is, the first word shifted into an empty part automatically "falls through" the buffer and it becomes visible at the outputs. Its presence is indicated by the rising edge of OR. The following sequence describes this fallthrough action as a word is shifted into FIFO A (see Figure 2):

1. IR of FIFO A is HIGH because the device is empty.
2. The user brings SI HIGH, latching the data word and commencing a shift in.
3. SI is then brought LOW to release the word for fallthrough.
4. OR of FIFO A will go HIGH within the "fallthrough time" (tPT). OR going HIGH signals a valid word at the outputs.
5. IR of FIFO B is HIGH because it, too, is empty.
6. Because OR of A is tied to SI of B, a valid shift in is begun into FIFO B on the rising edge of OR.
7. Because IR of B is tied to SO of A, a valid shift out is begun (SO*OR = 1) out of A.
8. Data is simultaneously shifted out of A, and into device B. The transfer is thus begun.
9. Because a valid shift out is detected in A, OR goes LOW to acknowledge it. This becomes a falling edge on SI for B.
10. The transfer is now complete. The word falls through B, then through FIFO C, and so on, until it reaches the outputs of the bottom FIFO.

The timing diagram for low-frequency fallthrough is shown in Figure 3.

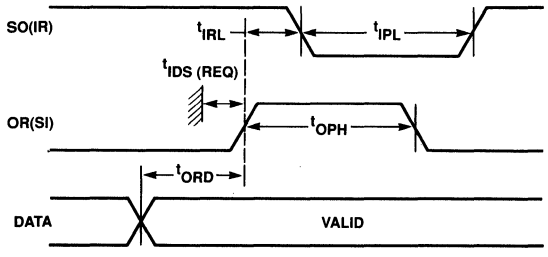


Figure 3. Low-Frequency Fallthrough

The term "low frequency" means that the time between arrival of words is long relative to the time required for a data transfer. There is a basic set of timing requirements that must be satisfied in all fallthrough cases, plus an additional one for high-frequency operation. The basic set will now be discussed.

Consider a cascade interface between FIFOs X and Y of Figure 2. The OR of X goes HIGH, then is quickly reset once a valid shift out is detected. The duration of this OR pulse, termed tOPH, must be long enough to be used by the SI of the downstream FIFO (Y). Specifically,

$$t_{OPH} > t_{SIH(required)}\ [1].$$

This requirement is shown as a function of temperature in Figure 4.

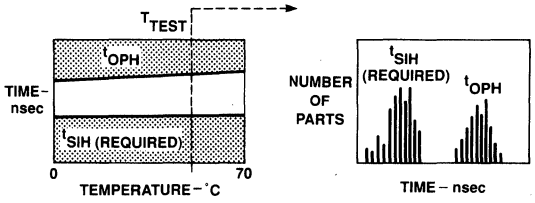


Figure 4. t_{OPH} vs. t_{SIH} at a Particular V_{CC}

The tOPH requirement is derived from histograms generated during the characterization of a broad sample of cascadable parts. The parts are tested individually at a variety of voltage and temperature conditions. Monolithic Memories specifies its cascadable FIFOs with a reliable margin between the tOPH and tSIH histograms under each condition.

A short logic 1 pulse on SI will produce a short logic 0 pulse (tIPL) on IR. tIPL must be long enough to be recognized as a legitimate SO low pulse by the upstream part X. Thus,

$$t_{IPL} > t_{SOL(req)}\ [2].$$

There is a direct relationship between tSIH and tIPL. The requirements on tIPL from [2] are used to dictate the requirements on tSIH. The parameter t_{IPL} is used only for characterization and internal testing and does not appear in Monolithic Memories data sheets.

Next, there is the need for SO and OR to be simultaneously at a logic 1 long enough for the FIFO to detect a valid shift out. This time requirement, which is not found in the datasheets is termed tSOHR(req), "time for SO to remain high after OR goes high." If IR, which drives SO, goes LOW too soon after a valid shift in is detected in Y, the tSOHR requirement in X may be violated. If so, no shift out will take place. Therefore,

$$t_{IRL} > t_{SOHR(req)}\ [3].$$

The parameter tSOHR is characterized and tested. It is normally small relative to tSOH.

The last requirement for Case 1 pertains to data set-up. When in the fallthrough mode, input data is taken as valid on the rising edge of SI. The set-up time for this data (tIDS) must be met. Note, however, that meeting this set-up time is the responsibility of the upstream part (X). When X brings its OR pin HIGH, it indicates that new data is present. The time from OR HIGH to new data valid is termed tORD. Because this rising edge commences a shift in for the downstream part, the following relationship must hold:

$$-t_{ORD} > t_{IDS(req)}\ [4].$$

In all Monolithic Memories cascadable FIFOs tIDS max is specified at zero, while tORD max is never specified greater than zero. By this convention, [4] is always satisfied. The validity of inequality [4], and others documented in this application note, are ensured via the method of separation of parametric distributions, as illustrated in Figure 4.

Case 2: Low-Frequency Bubbleback

The term "bubbleback" is a hangover from the register-based FIFOs. Bubbleback occurs when one or more devices in the composite buffer are full, and a word is clocked out of the most downstream one. A vacancy is created in this bottom FIFO, and is soon filled by the first FIFO upstream from it. The vacancy then "bubbles back" all the way to the most upstream FIFO. In the process, a data transfer is required each time the vacancy crosses a cascade interface, as was the case for fallthrough.

The following sequence describes this bubbleback action:

1. The user shifts data out of the most downstream FIFO.
2. Since this FIFO is no longer full, its IR pin goes HIGH.
3. The first FIFO upstream from it held its OR HIGH, because it was not empty.
4. The IR of the end FIFO is tied to SO of the FIFO above it. The rising edge on IR commences a shift out of the upstream FIFO.
5. Simultaneous shift cycles occur in both FIFOs. IR of the end FIFO goes LOW to acknowledge the valid shift in.
6. IR going LOW in the end FIFO resets the valid shift out of the upstream device. Since this upstream part is not empty, its OR pin returns HIGH.
7. Because this upstream part now contains a vacancy, it commences a shift out of the next higher part. This process continues until the vacancy reaches the *most upstream* device.

The timing diagram for the cascade interface is shown below.

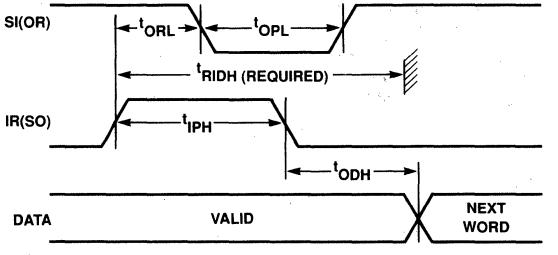


Figure 5. Low-Frequency Bubbleback

In bubbleback it is IR going HIGH which initiates the transfer of data. IR goes HIGH, then is quickly reset once a valid shift in is detected. This is analogous to the fallthrough case in which OR is pulsed HIGH. The first three bubbleback inequalities, then, are merely I/O duals of [1] through [3]:

$$t_{IPH} > t_{SOH(req)}\ [5],$$

$$t_{OPL} > t_{SIL(req)}\ [6],$$

$$t_{ORL} > t_{SIHR(req)}\ [7].$$

There is no data set-up requirement for low-frequency bubbleback since the next data word is present and waiting long before a vacancy arrives for it. This data must, however, satisfy a hold time requirement, as measured from the start of the valid shift in.

As seen in Figure 5, SO is brought LOW in the middle of the data transfer. Bringing SO LOW clears the upstream FIFO, causing its read pointer to advance. A new data word then begins its way toward the outputs. The current word being transferred eventually becomes "old" data, to be replaced by the next word. The time that the "old" data is held after SO goes LOW is called tODH.

The bubbleback hold time requirement (see Figure 5) can be expressed as:

$$t_{IPH} + t_{ODH} > t_{RIDH(req)}\ [8a].$$

The parameter tRIDH is the data hold time, relative to IR going HIGH. It is measured relative to IR because, in the bubbleback case, IR initiates the shifting-in of data.

Testing of [8a] is required to ensure cascadability in all outgoing parts. However, inequality [8a] mixes parameters from both the upstream (tODH) and the downstream (tIPH, tRIDH) parts. It is therefore necessary to rewrite [8a] so that it can be examined on individual parts:

$$[t_{IPH} - t_{RIDH(req)}] > -t_{ODH}\ [8b].$$

The quantity on the left hand side of the equation becomes a new characterization parameter, called t1. If there is a sufficient margin between the test histograms of t1 and tODH (as was the case for tOPH versus tSIH), then criterion [8a] will certainly be satisfied.

Case 3: Higher-Frequency Fallthrough

In Case 3, the frequency of operation becomes high enough such that the data transfer time is no longer negligible when compared to the time between arrivals of any two words. Still, the frequency is low enough such that the operation is clearly fallthrough, i.e., OR going HIGH initiates the transfer of data into a downstream part that is clearly waiting for new data.

The timing diagram for this case is shown in Figure 6.

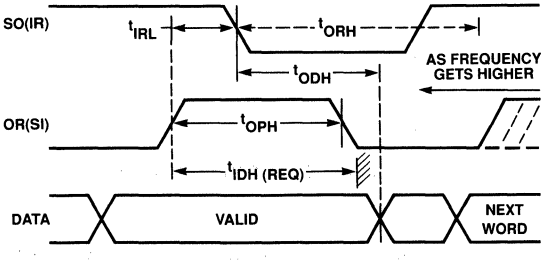


Figure 6. Higher-Frequency Fallthrough

Inequalities [1] through [4] from Case 1 still hold. One more must be added to account for the second rising edge of OR, which now occurs soon after the data transfer.

The falling edge on IR, which occurs after a valid shift in is detected, is seen by the upstream part as a falling edge on SO. This implies a read pointer advance, which could bring new data to the outputs. In the low-frequency case there was no new data to bring, so the current word remained valid for quite some time. At higher frequency, there *is* a new word to bring to the outputs, which reduces the time that the current data is

valid. There is the risk of a data hold time violation unless the following relationship is met:

$$t_{IRL} + t_{ODH} > t_{IDH(req)} \text{ [9]}.$$

The parameter t_{IDH} is the data hold time relative to SI going HIGH.

As the frequency of operation gets continually higher, the second rising edge of OR falls closer to that of IR. The limiting cycle time for true fallthrough, as depicted here, is tIRL + tORH, although this cycle time may not be obtainable due to limitations described in the section on natural frequency.

Case 4: Higher-Frequency Bubbleback

In Case 4 the time between creations of vacancies approaches the time required for data transfer. However, the frequency is assumed low enough such that the operation is clearly bubbleback, i.e., the rising edge of IR initiates a shift out of an upstream part which is clearly waiting with valid data.

The timing diagram for this case is seen below.

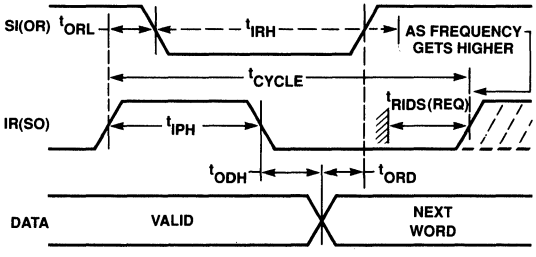


Figure 7. Higher-Frequency Bubbleback

Inequalities [5] through [8] from Case 2 are still pertinent. One more must be added to account for the rising edge of IR, which reappears soon after the data transfer.

As vacancies bubble back at ever increasing rates, there is the risk of violating the data set-up requirement as measured from the edge of IR. Specifically, the following relationship must hold:

$$t_{CYCLE} - t_{IPH} - t_{ODH} > t_{RIDS(req)} \text{ [10]}.$$

The parameter tRIDS is the set-up time relative to IR going HIGH. Inequality [10] tells us that if tCYCLE gets too short, there may be a data set-up violation. As seen in Figure 7, so long as we remain in bubbleback mode, with IR coming high after SI, we will have tIPH + tODH + |tORD| < tCYCLE, implying tCYCLE-tIPH-tODH > |tORD|. However, Monolithic Memories designs its cascadable devices such that tRIDS(req) < 0, and tORD < 0, thereby ensuring that there is no set-up violation.

As the frequency of operation gets continually higher, the second rising edge of IR falls closer to that of OR. The limiting cycle time for true bubbleback, as defined here, is tORL + tIRH, although this cycle time may not be obtainable, as discussed in the next section.

Case 5: Natural Frequency

As mentioned previously, the user has no control over the handshake operations at the cascade interfaces. If the user shifts words into a relatively empty buffer at low frequency, the cascade interfaces will operate in the fallthrough mode (Case 1). If the user shifts words out of a relatively full buffer at low frequency, then the interfaces will be forced to operate in bubbleback mode (Case 2). For continuous operation at moderately high rates, the interface timing will begin to resemble one of the next two (3 and 4) cases.

As the frequency is increased further, the interface timing may no longer be clearly bubbleback or clearly fallthrough. This is what occurs as the throughput rate approaches the *natural frequency* of the cascade interface. This natural frequency is the maximum frequency at which the handshake signals can negotiate part-to-part data transfers. Consider Figure 8.

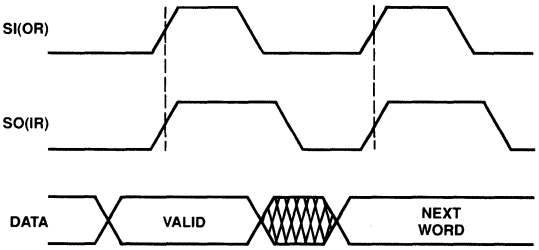


Figure 8. Zero-Phase Incidence

Figure 8 illustrates a perfectly legitimate handshake operation. There is clearly a shift in (SI*IR=1) and a shift out (SO*OR=1), implying a transfer of data. However, none of the previous cases directly apply since it is neither a fallthrough nor a bubbleback case.

In the fallthrough mode SO was clearly high before OR, while IR went high clearly before SI. Thus, SO had *positive phase* relative to OR, while SI had *negative phase*. Likewise, the bubbleback mode has negative phase for SO and positive phase for SI. The relative phases of the SI and SO signals have important implications for the cascading parameters at high frequencies. As explained later, the natural frequency of cascading must be guaranteed higher than the maximum throughput rate applied to the cascaded FIFO system. Predicting and measuring the natural frequency poses some difficulties, as explained below.

The fallthrough parameters tIRL, tOPH, tIDS, etc., are all characterized at positive SO, negative SI phase, whereas the bubbleback parameters tORL, tIPH, tRIDH, etc., are all characterized at positive SI, negative SO phase. When the relative phases approach zero from either side (Figure 8), the meaning of these parameters becomes ambiguous. Take for example the parameter "time from valid shift in (SI*IR=1) to IR going low." For positive phases this quantity approaches the tIPH asymptote, while for negative phases it approaches the tIRL asymptote. When the phase is near zero, this quantity lies somewhere in between, as shown in Figure 9.

As indicated on the graph, a new name is required for this pseudo-parameter. It will be known here as tVSIRL, or "time from valid shift in to IR low." Similar graphs can be generated for

the pseudo-parameter called tVSORL, as well as for t(R)IDS and t(R)IDH. This sort of graphical information is useful when analyzing operating characteristics at or near the natural frequency. At this point there are two approaches one can take to predicting the natural frequency:

1) Take an iterative approach to determine the minimum working values of phase (ϕ), tVSIRL(ϕ), tVSORL(ϕ), t(R)IDS(ϕ), etc., using two figures, 10 and 11.

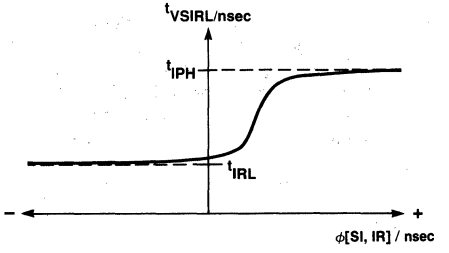


Figure 9. t_{VSIRL} as a Function of Phase

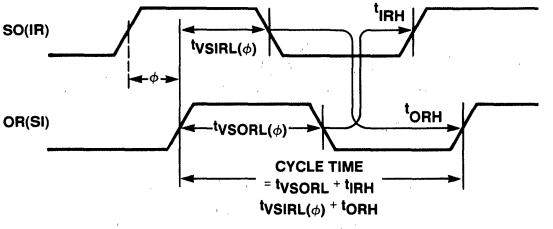


Figure 10. Positive SO/OR Phase at Natural Frequency

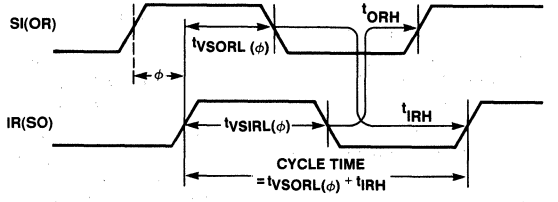


Figure 11. Positive SI/IR Phase at Natural Frequency

One needs to determine which of the two cases (Figures 10, 11) has a lower maximum frequency. In equation form:

$$1/f_{MAX} = \max\{t_{VSIRL}(O)+t_{ORH}, t_{VSORL}(O)+t_{IRH}\} \text{ [11]}.$$

2) Approach (1) provides the exact value of the natural frequency, but only after a considerable amount of iteration. There exists a simpler approach to the problem, based upon the results of Cases 3 and 4. This approach yields a conservative estimate of the natural frequency, such that if the composite buffer is operated at or below this frequency, cascadability can be guaranteed.

Figure 6 depicts fallthrough operation based on the assumption that tIRL + tORH is clearly greater than tOPH + tIRH. If this is not the case, then the second rising edge of OR could possibly occur before the second rising edge of IR. Then, the parameter tOPH is no longer valid, and should be replaced by the more applicable tORL. However, tORL pertains to cases where SO arrives substantially after OR. If the rising edges of IR and OR are close to one another, then the applicable value may lie somewhere inbetween tORL and tOPH. To be safe, merely take the greater of these two values.

The same reasoning applies for the breakdown of the fundamental assumption of Case 4. The following is a simple worst-case expression for fMAX at each operating condition:

$$1/f_{MAX(wc)} = \max\{t_{VSIRL(max)}+t_{ORH}, t_{VSORL(max)}+t_{IRH}\} \text{ [12a]},$$

where:

$$t_{VSIRL(max)} = \max\{t_{IRL}, t_{IPH}\} \text{ [12b]},$$

$$t_{VSORL(max)} = \max\{t_{ORL}, t_{OPH}\} \text{ [12c]}.$$

Note that using the results of Cases 3 and 4 produced equation [12] which bears great resemblance to the more accurate expression in [11]. One strategy for dealing with cascadability is to design a FIFO with "flat" tVSIRL, tVSORL, t(R)IDS, etc., characteristics. This eliminates the dependence on signal phase, and fMAX can be expressed exactly as:

$$1/f_{MAX} = \max\{t_{IRL}+t_{ORH}, t_{ORL}+t_{IRH}\} \text{ [13]}.$$

Such a strategy provides a more reliable cascade interface, and is well worth the price of a lower fMAX.

It should be noted that the natural frequency at each operating condition (VCC, temperature) is unique, and is the limiting frequency regardless of how it is approached, whether by fallthrough or by bubbleback. Consider the following figure.

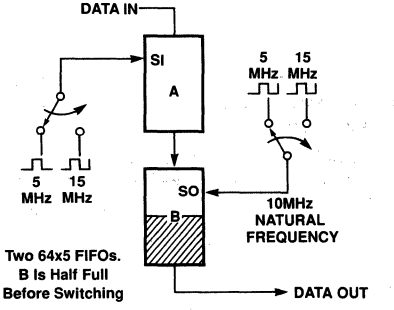


Figure 12. Approach of f_{MAX} from Fallthrough

Let us say that the natural frequency of the cascade interface between A and B is 10 MHz. Data is shifted at low frequency into A, and falls through to B, until B is one-half full. The two-device buffer is then operated for a while with the input, output, and interface working at 5 MHz.

Then, the input and output frequencies are raised to, say, 15 MHz. Immediately thereafter, the composite buffer will continue to function, since the input and output circuitry of a FIFO

can usually operate at frequencies above the natural frequency. The cascade interface, however, will be limited to a rate of 10 MHz. Eventually, the bottom part will empty, and the top part will fill. A cascade limited bottleneck occurs, limiting the overall throughput rate to 10 MHz. Data words from the 15 MHz input stream will be intermittently read at a 10 MHz rate, causing a loss of data.

At some point in time between the frequency increase and the bottlenecking, there will be five or so words in the top part, and twenty-seven or so (half of 64, minus 5) words in the bottom part. The FIFOs will no longer be in fallthrough mode, since there is more than one word in the upstream part, and more than one vacancy in the downstream part. The natural frequency mode will have been entered, and the interface will carry data as fast as possible.

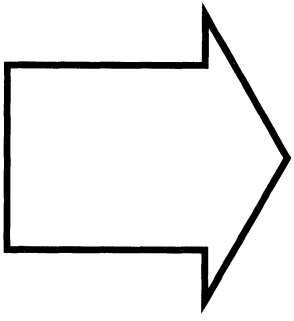
A similar example can be drawn for these FIFOs, with the composite buffer initially three-fourths filled. Eventually, the top part will fill and the bottom part will empty. At some point in between, the FIFOs will no longer be in bubbleback mode, but in the natural frequency mode, because there will exist more than one vacancy in the downstream part and more than one word in the upstream part. The overall steady state throughput rate will again be limited to 10 MHz.

In each of the above cases, the composite buffer went from either fallthrough or bubbleback mode to the natural frequency mode (where both parts were neither full nor empty), then on to an interface limited natural frequency mode, subject to throughput-related errors.

Regardless from which direction the natural frequency was approached, this frequency must be unique since it represents the case where the upstream part contains more than one word and where the downstream part contains more than one vacancy. When this happens the interface has no dependence on what is happening at the system input and output ports and shifts data across it at the maximum possible rate.

The maximum operating frequency of a cascaded FIFO must therefore be specified lower than the worst-case natural frequency in order to avoid asynchronously induced bottleneck errors.

Advanced
Micro
Devices



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Package: Thermal Characterization

MMI Package Thermal Characteristics

Introduction

Thermal resistance for a packaged integrated circuit determines the operating temperature and hence the performance and lifetime of the semiconductor device. For this reason, it is of interest to know the thermal resistance of the package configurations commonly in use and the effect of external factors such as air circulation and board-mounting conditions on the device temperature. To accomplish this end, measurement techniques and standards have been established providing certain conventions for data acquisition. Monolithic Memories has chosen to conform to these conventions in measurement and provides standard data for thermal resistance in the form of $R_{\theta JC}$ (resistance from junction to case) and $R_{\theta JA}$ (resistance from junction to ambient) as a function of air movement over the package/-board combination.

Use of Monolithic Memories Data

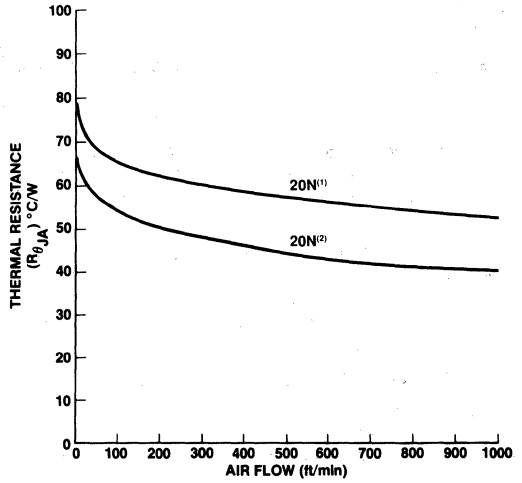
In this publication, data is presented for a variety of packages and ambient conditions. In order to simplify the data presentation, graphs of $R_{\theta JA}$ vs. airflow are provided for packages in common use. These include socket-mounted pin grid arrays, dual-in-line p-dip, cerdip and side-brazed packages, board mounted cerpacks, flatpacks, leadless-chip carriers and plastic leaded chip carriers.

Resistance from junction to ambient ($R_{\theta JA}$) is a package geometry and die size related function. The user need only look up the package type and die size for the air-flow used. Since the $R_{\theta JC}$ is largely dependent on the package type and die size, a table has been constructed for easy use.

Notes on the Tabulated Data

1. All side-brazed, cerdip-sealed, molded dual-in-line and pin grid array packages were mounted in zero insertion force sockets with 40 mils air gap and transverse to the airstream.
2. All cerpacks, flatpacks, LCC, PLCC and SOIC packages were board mounted in direct contact with a double-sided fiberglass-epoxy composite printed circuit board.
3. For measurement of $R_{\theta JC}$, all packages were immersed in a constant temperature fluorinert bath. The thermocouple was mounted directly to the bottom of the package.

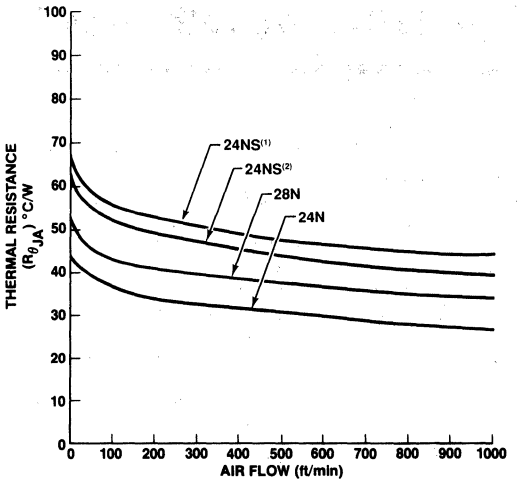
20 Lead Molded DIP (20N) Packages



PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
20N(1)	5,625	22
20N(2)	11,250	15

*These are typical values for the given die size.

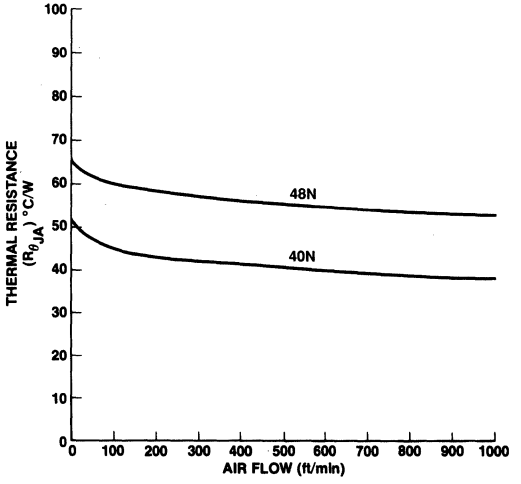
24, 28 Lead Molded DIP (24N, 28N) Packages



PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
24NS(1)	5,625	20
24NS(2)	11,250	15
24N	50,625	10
28N	22,500	13

*These are typical values for the given die size.

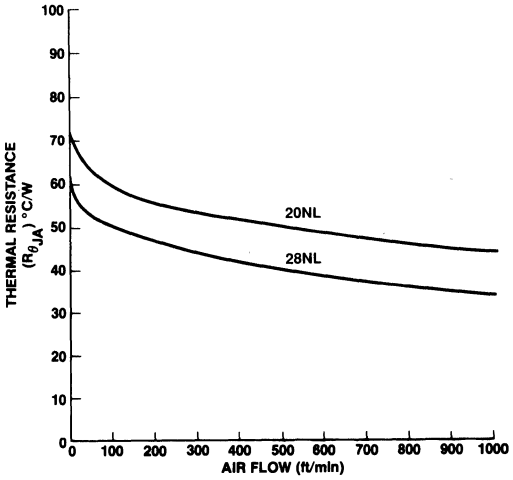
40, 48 Lead Molded DIP (40N, 48N) Packages

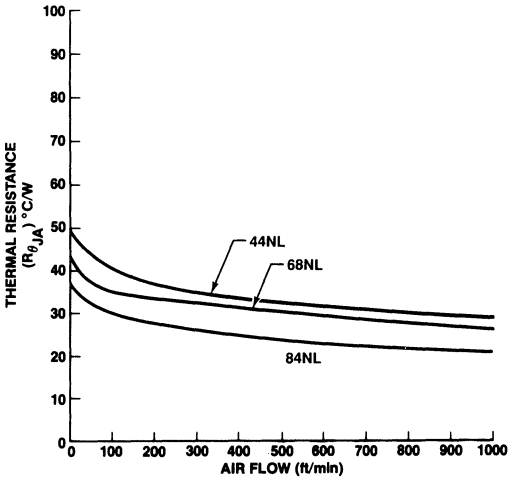


PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
40N	22,500	16
48N	5,625	23

*These are typical values for the given die size.

Plastic Leaded Chip Carrier (NL) Packages

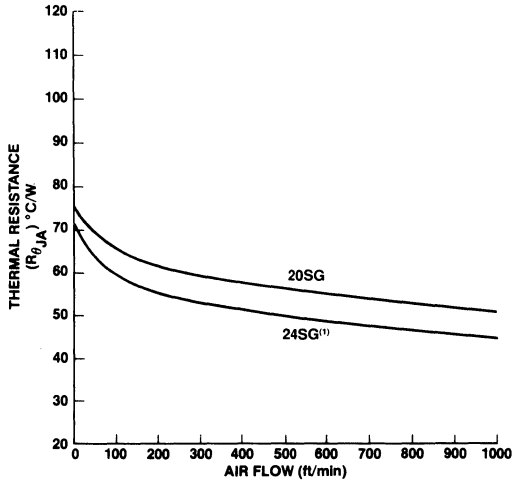




PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
20NL	11,250	14
28NL	22,500	13
44NL	22,500	11
68NL	50,625	8
84NL	50,625	6

*These are typical values for the given die size.

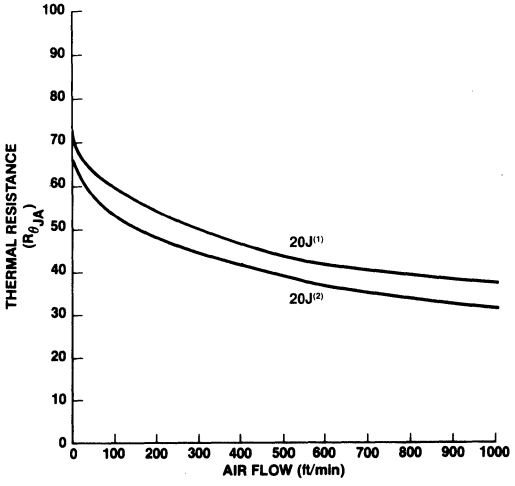
Small Outline (20SG, 24SG) Packages



PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
20SG	5,625	16
24SG(1)	11,250	13
24SG(2)	22,500	10

*These are typical values for the given die size.

20 Lead Cerdip (20J) Packages



PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
20J(1)	5,625	14
20J(2)	22,500	6

*These are typical values for the given die size.

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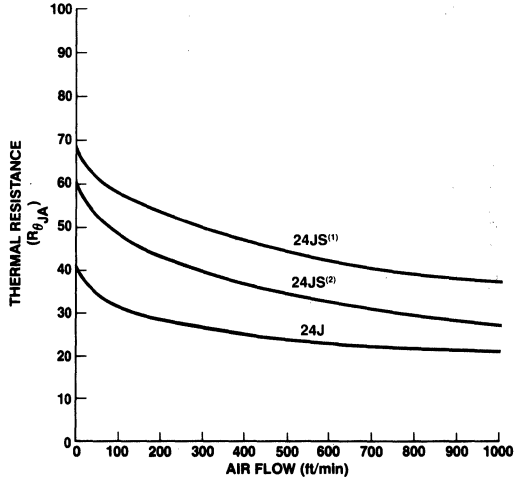
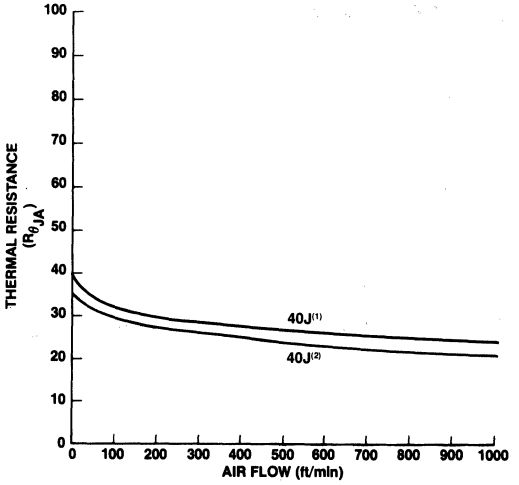
24 Lead Cerdip (24J, 24JS) Packages



PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
24JS(1)	5,625	16
24JS(2)	11,250	8
24J	50,625	3

*These are typical values for the given die size.

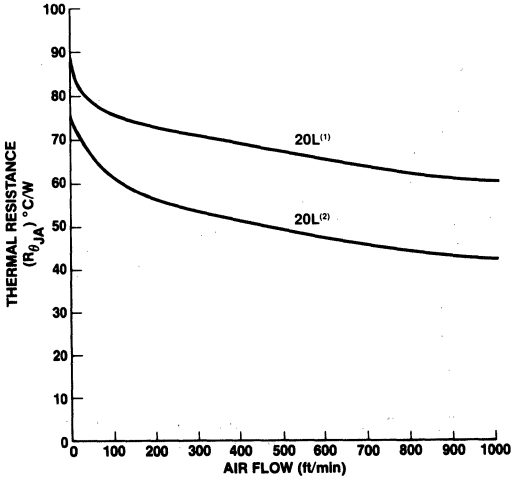
40 Lead Cerdip (40J) Packages



PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
40J(1)	22,500	4
40J(2)	50,625	2

*These are typical values for the given die size.

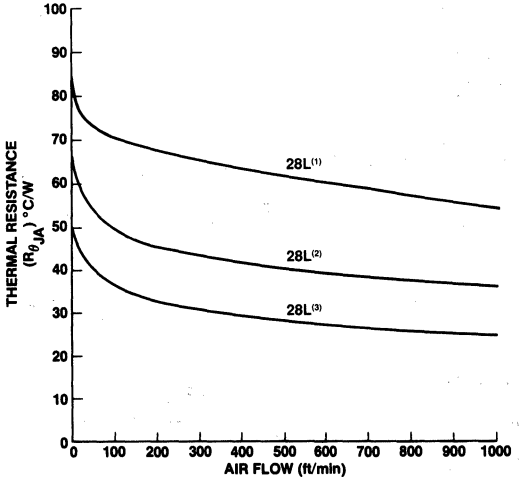
20 Leadless Chip Carrier (20L) Packages



PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
20L(1)	5,625	16
20L(2)	22,500	4

*These are typical values for the given die size.

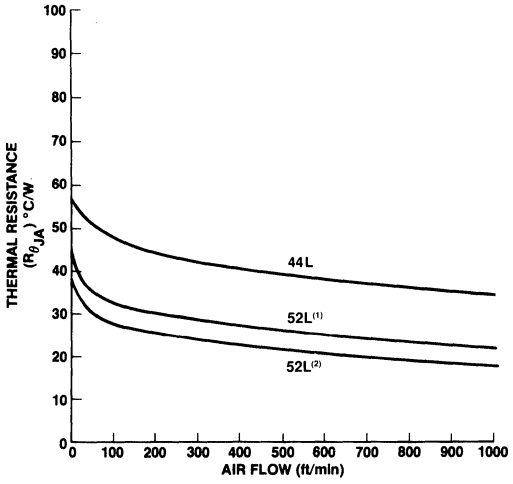
28 Leadless Chip Carrier (28L) Packages



PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
28L(1)	5,625	20
28L(2)	11,250	10
28L(3)	50,625	3

*These are typical values for the given die size.

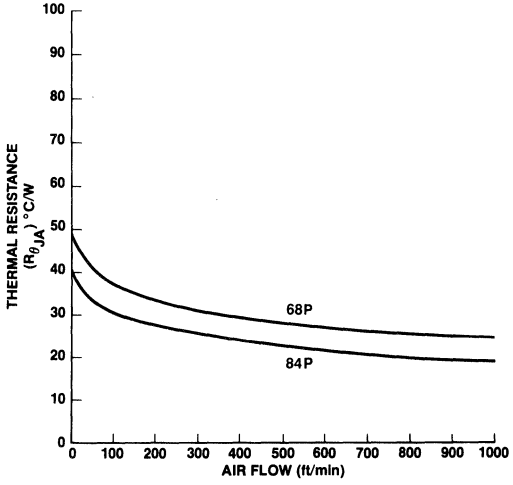
Leadless Chip Carrier (44L, 52L) Packages



PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
44L	22,500	4
52L(1)	22,500	2
52L(2)	50,625	1.5

*These are typical values for the given die size.

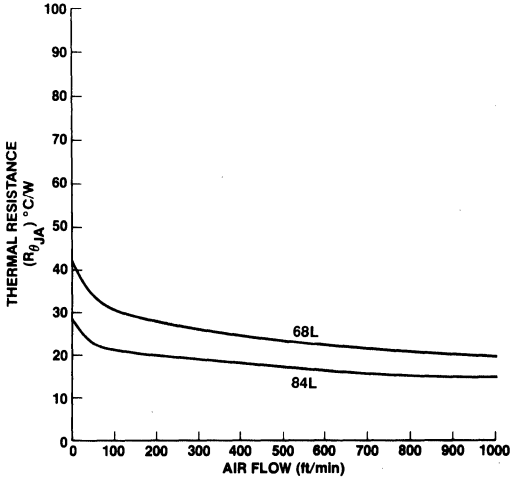
Pin Grid Array (68P, 84P) Packages



PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
68P	22,500	5
84P	90,000	2

*These are typical values for the given die size.

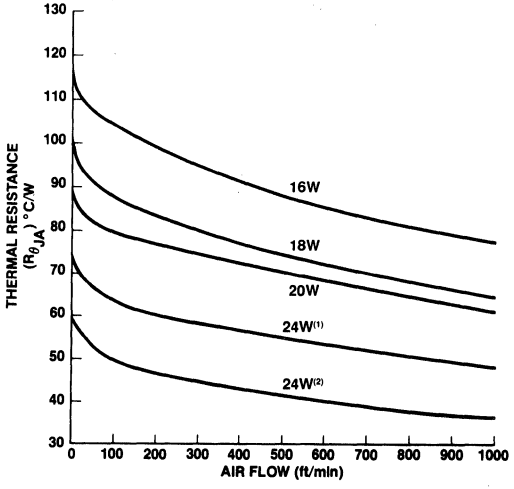
Leadless Chip Carrier (68L, 84L) Packages



PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
68L	22,500	2
84L	50,625	1

*These are typical values for the given die size.

Cerpack (W) Packages



PACKAGE	DIE SIZE (mils)^2	$R^*_{\theta JC}$ (°C/WATT)
16W	5,625	21
18W	5,625	17
20W	5,625	15
24W(1)	11,500	7
24W(2)	22,500	3

*These are typical values for the given die size.

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Thermal Resistance Measurement Procedure

Definition

Thermal resistance of a semiconductor device is a measure of the ability of its mechanical structure (package) to provide for heat removal from the semiconductor element. It is defined as the rise in the junction temperature against some reference point per unit power of dissipation or it may be described by the formula:

$$R_{\theta JR} = \frac{T_J - T_R}{P}$$

$R_{\theta JR}$ = Thermal resistance, junction to reference point, in °C/watt
T_J = Junction temperature in °C
T_R = Reference point temperature in °C
P = Power dissipation

Thermal Measurement Technique

Thermal resistance is measured using the temperature sensitive parameter (TSP) method. This method takes advantage of the linear relation between temperature and voltage drop across a p-n junction to measure the average die temperature. Thermal resistance measurement can be done either using an actual device or with thermal test chips. For the purpose of this study, thermal test chips are used.

Each test chip consists of sensing elements and a heating element. Sensing elements are two sets of diode pairs. One diode pair is located at the center of each die and one pair is near a corner. The heating element is a polysilicon resistor which covers 95 percent of the die surface area. The resistor extends underneath the bond pads but not the sensing elements.

Initially, diodes are forward biased to a low level current source (50 μA) and the voltage drop is calibrated with respect to temperature. Then, the resistor is powered and the diode voltage drop is monitored until thermal equilibrium is reached. Steady state junction temperature is calculated from the calibration data.

For the $R_{\theta JA}$ measurement the device is put in a wind tunnel. The air speed is adjustable from 0 to 1000 feet/min. The use of a wind tunnel allows us to graph the $R_{\theta JA}$ vs. air flow velocity. Average junction to case thermal resistance ($R_{\theta JC}$) is measured by immersing the package in a constant temperature fluorinert bath and sensing steady state junction temperature with case temperature being measured at the bottom of the package.

Summary

The thermal resistance measurement can be summarized as follows:

1. Calibration of the voltage drop across the sensing element with respect to temperature. This is done by measuring the voltage drop at several different temperatures with the heating power off.
2. Measurement of voltage drop across the sensing element under operating conditions, under various air flow rates (from 0 to 1000 linear ft/min.), while measuring °C ambient and power input for calculation of $R_{\theta JA}$.
3. Measurement of voltage drop across the sensing element under operating conditions, package immersed in constant temperature fluorinert bath, while measuring the case temperature at the bottom of the package and power input for calculation of $R_{\theta JC}$. The readings are recorded when the package has reached thermal equilibrium.
4. Calculation of thermal resistance

a. $R_{\theta JA} = \frac{T_J - T_A}{P}$ b. $R_{\theta JC} = \frac{T_J - T_C}{P}$

AMD Package Thermal Characteristics

TR-202

Abstract

Determination of the Thermal Resistance of Packaged Devices is of concern to the designer of new devices and to AMD customers. The Advanced Package and Material Development group has undertaken the task of characterizing current AMD products and quantifying package-related influences on Thermal Resistance. This report describes some of these effects and the technique used to measure Thermal Resistance.

Definition of Thermal Resistance

The reliability of an integrated circuit is largely dependent on the maximum temperature which the device will attain during operation. Because the stability of a semiconductor junction declines with increasing temperature, knowledge of the thermal properties of the packaged device becomes an important factor during device design. In order to increase the operating lifetime of a given device, the junction temperatures must be minimized. This demands knowledge of the thermal resistance of the completed assembly and specification of the conditions in which the device will function properly. As devices become both smaller and more complex and the requirement for high speed operation becomes more important, heat dissipation will become an ever more critical parameter.

Thermal resistance is defined as the temperature rise per unit power dissipation above some referenced condition. The unit of measure is typically °C/watt. The relationship between junction temperature and thermal resistance is given by:

$$T_J = T_X + P_D\ \theta_{JX} \qquad (1)$$

where: T_J = junction temperature
T_X = reference temperature
P_D = power dissipation
θ_{JX} = thermal resistance
X = some defined test condition

In general, one of three conditions is defined for measurement of thermal resistance:

θ_{JC}	– thermal resistance measured with reference to the temperature at some specified point on the package surface.
θ_{JA} (still air)	– thermal resistance measured with respect to the temperature of a specified volume of still air.
θ_{JA} (moving air)	– thermal resistance measured with respect to the temperature of air moving at a specified velocity.

The relationship between θ_{JC} and θ_{JA} is

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

where θ_{CA} is a measure of the heat dissipation due to natural convection (still air) or forced convection (moving air) and the effect of heat radiation and mounting techniques. θ_{JC} is dependent solely on material properties and package geometry; θ_{JA} includes the influence of the surface area of the package and environmental conditions. Each of these definitions of thermal resistance is an attempt to simulate some manner in which the package device may be used.

The thermal resistance of a packaged device, however measured, is a summation of the thermal resistances of the individual components of the assembly. These in turn are functions of the thermal conductivity of the component materials and the geometry of the heat flow paths. Like other material properties, thermal conductivity is usually temperature dependent. For alumina and silicon, two common package materials, this dependence can amount to a 30% variation in thermal conductivity over the operating temperature range of the device. The thermal resistance of a component is given by

$$\theta = \frac{L}{K(T)A} \qquad (2)$$

where: L = length of the heat flow path
A = cross sectional area of the heat flow path
K(T) = thermal conductivity as a function of temperature

and the overall thermal resistance of the assembly (discounting convective effects) will be:

$$\theta = \Sigma\theta_n = \Sigma\ \frac{L_n}{K_n A_n}$$

but since the heat flow path through a component is influenced by the materials surrounding it, determination of L and A is not always straightforward.

A second factor that affects the thermal resistance of a packaged device is the power dissipation level and, more particularly, the relationship between power level and die geometry, i.e., power distribution and power density. By rearrangement of equation 1 to

$$P_d = \frac{1}{\theta_{JX}}(T_J - T_X) = \frac{1}{\Sigma\theta_N}(T_J - T_X) \qquad (3)$$

the relationship between P_d and T_j can be more clearly seen. Thus, to dissipate a greater quantity of heat for a given geometry, T_J must increase and, since the individual θ_n will also increase with temperature, the increase in T_J will not be a linear function of increasing power levels.

A third factor of concern is the quality of the material interfaces. In terms of package construction, this relates

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specifically to the die attach bond, and for those packages having a heatsink, the heatsink attach bond. The quality of the die attach bond will most severely influence the package thermal resistance as this is the area which first impedes the transfer of heat out of the silicon die. Indeed, it seems likely that the initial thermal response of a powered device can be directly related to the quality of the die attach bond.

Experimental Method

The technique for measurement of thermal resistance involves the identification of a temperature-sensitive parameter on the device and monitoring this parameter while the device is powered. For bipolar integrated circuits the forward voltage of the substrate isolation diode provides a convenient parameter to measure and has the advantage of a linear dependence on temperature. MOS devices which do not have an accessible substrate diode present greater measurement difficulties and may require simulation through use of a specially designed thermal test die. Choice of the parameter to be measured must be made with some care to ensure that the results of the measurement are truly representative of the thermal state of the device being investigated. Thus measurement of the substrate isolation diode which is generally diffused across the area of the die yields a weighted average of the condition of the individual junctions across the die surface. Measurement of a more local source would yield a less generalized result.

For MOS devices, simulation is accomlished using the thermal test die. The basis for this test die is a 25 mil square cell containing an isolated diode and a 1 KΩ resistor. The resistors are interconnected from cell to cell on the wafer before it is cut into mulitple arrays of the basic unit cell. In use the device is powered via the resistors with voltage or current adjusted for the proper level and the voltage drop of the individual diodes is monitored as in the case of actual devices.

Prior to the thermal resistance test, the diode voltage/temperature calibration must be determined. This is done by measuring the forward voltage at 1 mA current level at two different temperatures. The diode calibration factor is then:

$$K_f = \frac{T_2 - T_1}{V_2 - V_1} = \frac{\Delta T}{\Delta V} \quad (4)$$

in units of °C/mV. For most diodes used for this test the voltage/temperature relationship is linear and these two measurement points are sufficient to determine the calibration.

The actual thermal resistance measurement has two alternating phases: measurement and power on. The device under test is pulse powered with an ON duty cycle of 99% and a repetition rate of < 100 Hz. During the brief OFF states the device is reverse-biased with a 1 mA current and the voltage drop is measured. The series of voltage readings are averaged over short periods and compared to the voltage reading obtained before the device was first powered ON. The thermal resistance is then computed as:

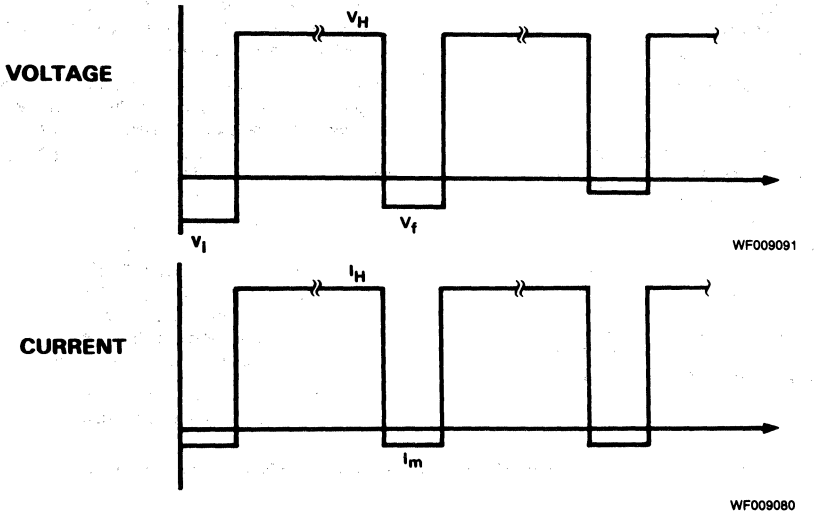
$$\theta_{jx} = \frac{K_F(V_F - V_I)}{V_H I_H} = \frac{K_f \Delta V}{P_D} \quad (5)$$

where: K_F = calibration factor
V_I = initial forward voltage value
V_F = current forward voltage value
V_H = heating voltage
I_H = heating current

The pulsing measurement is continued until the device has reached thermal equilibrium and the final value measured is the equilibrium thermal resistance of the device under test.

When the end result desired is θ_{JA} (still air), the device and the test fixture (typically a standard burn-in socket) are enclosed in a box containing approximately 1 cubic foot of air. For θ_{JC} measurements the device is attached to a large metal heatsink. This ensures that the reference point on the device surface is maintained at a constant temperature. The requirements for measurement of θ_{JA} (moving air) are rather more comple x and involve the use of a small wind tunnel with capability for monitoring air pressure, temperature and velocity in the area immediately surrounding the device tested. Standardization of this last test requires much careful attention.

WAVEFORMS FOR PULSED THERMAL RESISTANCE TEST



Experimental Results

The thermal resistance data included in the attached table was extrapolated from data collected using the procedure outlined in the preceding section. This data has resulted from an ongoing program undertaken by members of the Material Technology Development group.

Updated data will replace the data in this table as each device is measured or revised data becomes available.

Thermal Resistance of AMD Products

(Notes 1, 2 and 3)

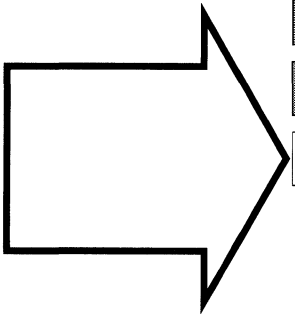
PIN COUNT	PACKAGE TYPE (Note 4)	θ_{JA}	θ_{JC}
20	Ceramic DIP	60	11
	Plastic DIP	61	30
	Ceramic Flatpack	56	CR
	Ceramic LCC	61	CR
	Plastic LCC*	CR	CR
24	Ceramic DIP	57	15
	Plastic DIP	60	CR
	Ceramic Flatpack	85	9
28	Ceramic LCC	CR	CR
	Plastic LCC*	58	CR

Notes:

1. Representative values for each package type — for information only.
2. Any given device may differ from these values. Consult local AMD sales office for specific-device information.
3. CR = Consult local AMD Representative.
4. DIP = Dual-In-Line Package
   LCC = Leadless Chip Carrier
   LCC* = Leaded Chip Carrier

Table 1.

Advanced
Micro
Devices



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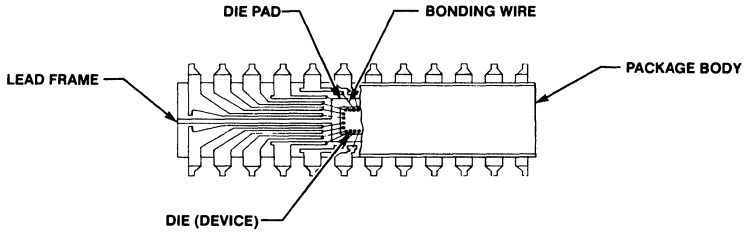
Package Drawings

MMI Package Outlines

Package Drawing

Molded DIP



LEAD FRAME

Copper Alloy 194.
Copper Alloy Tamac 5.

BONDING WIRE

1.0 Mil Gold Wire.
1.25 Mil Gold Wire.
1.30 Mil Gold Wire.

PACKAGE BODY

Thermoset Plastic.

LEAD FINISH

Solder Dip.

DIE PAD

Spot Silver Plating
(150 Micro-Inches)

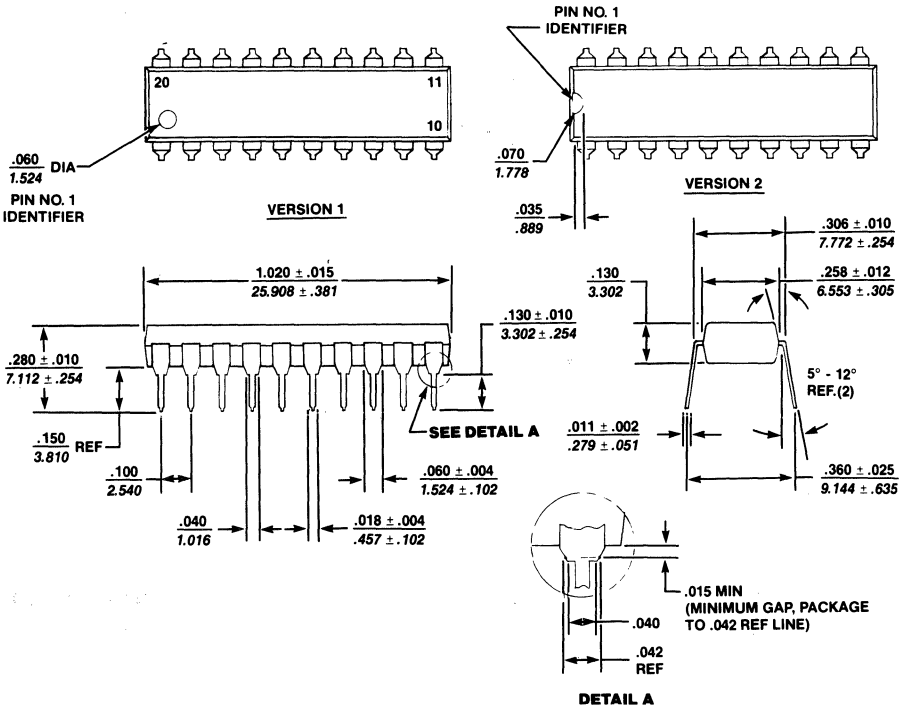
DIE BOND

Silver Filled Epoxy.

10745A

Package Drawings

20N Molded DIP
(1/4"x1")

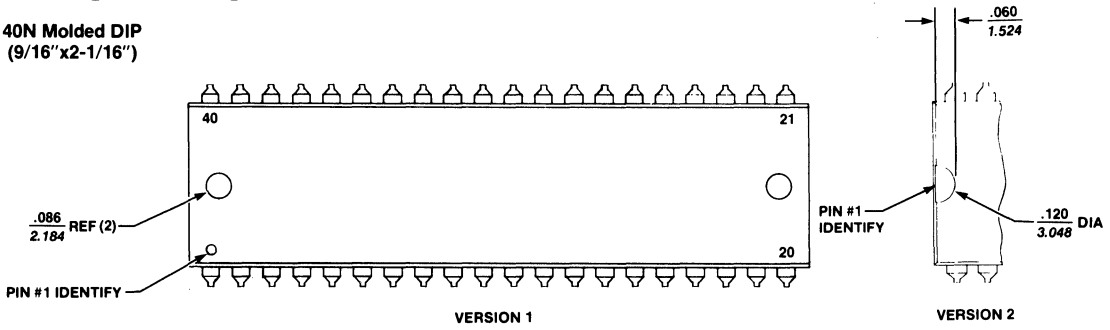


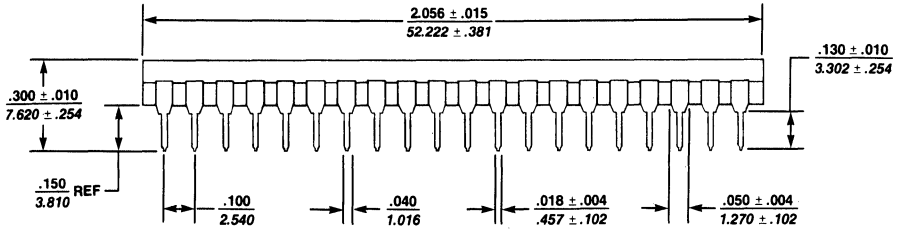
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

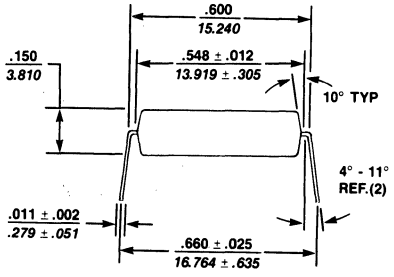
10746A

Package Drawing

40N Molded DIP
(9/16"x2-1/16")







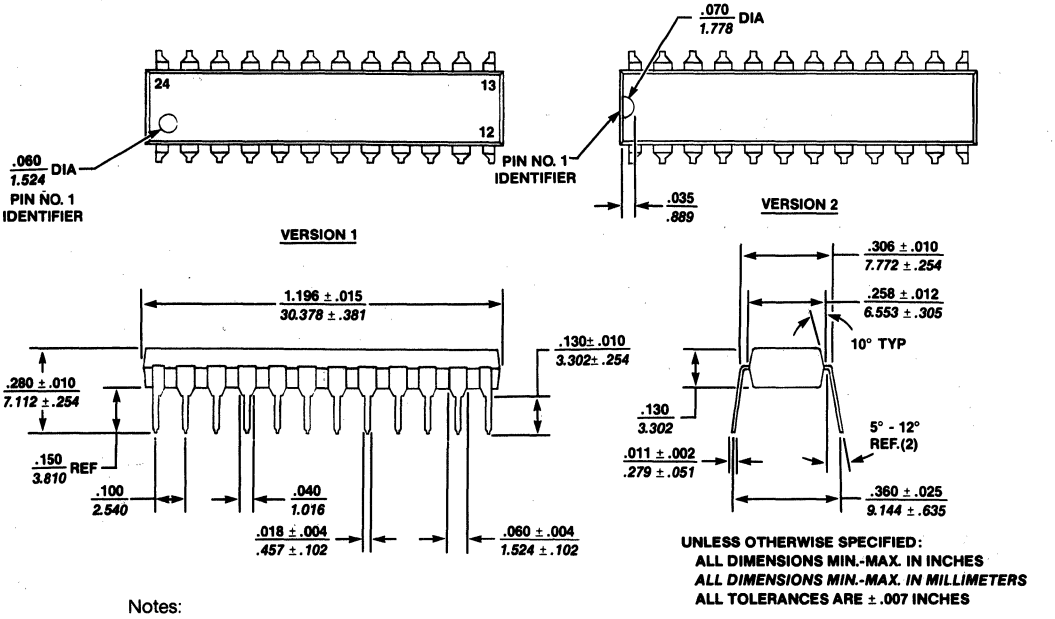
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

10748A

6

Package Drawing

24NS Molded SKINNYDIP
(1/4"x1 3/16")



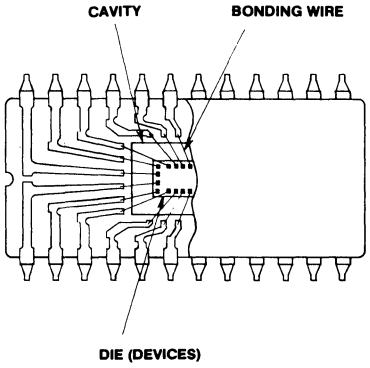
Notes:

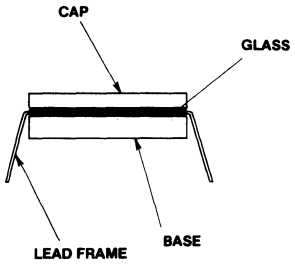
1. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.
2. Both version 1 and version 2 configurations are manufactured interchangeably.
3. Ejector pin marks on version 1 are optional.

10747A

Package Drawing

Ceramic DIP





LEAD FRAME
Alloy 42

BONDING WIRE
1.25 Mil Aluminum

CAP AND BASE
Pressed Alumina

GLASS
Vitreous
Solder Glass

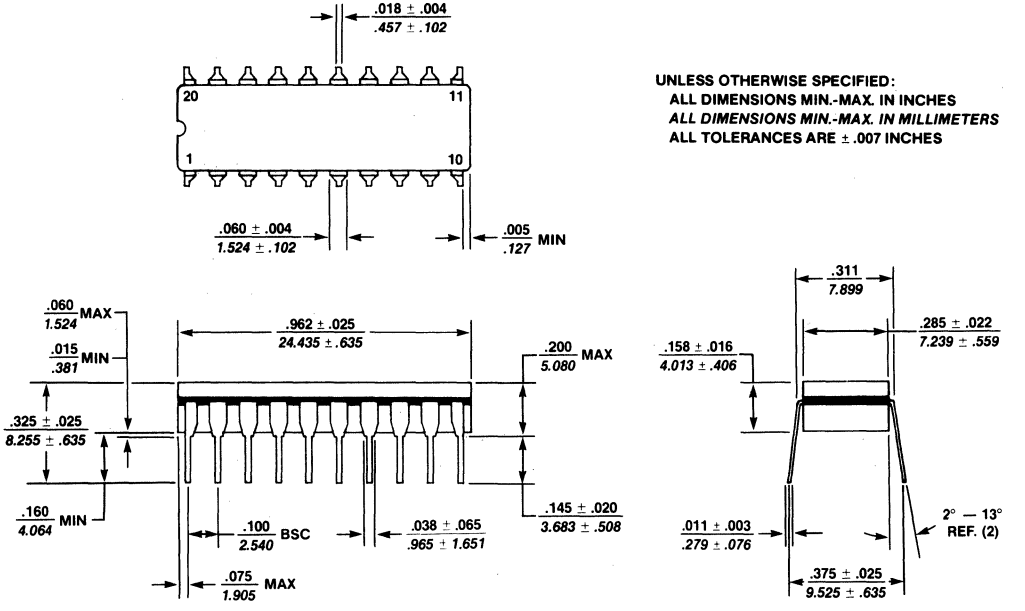
CAVITY
Gold Over Alumina
For Eutectic Die Attach

LEAD FINISHES
Solder DIP Over
Matte Tin Plate

10750A

Package Drawing

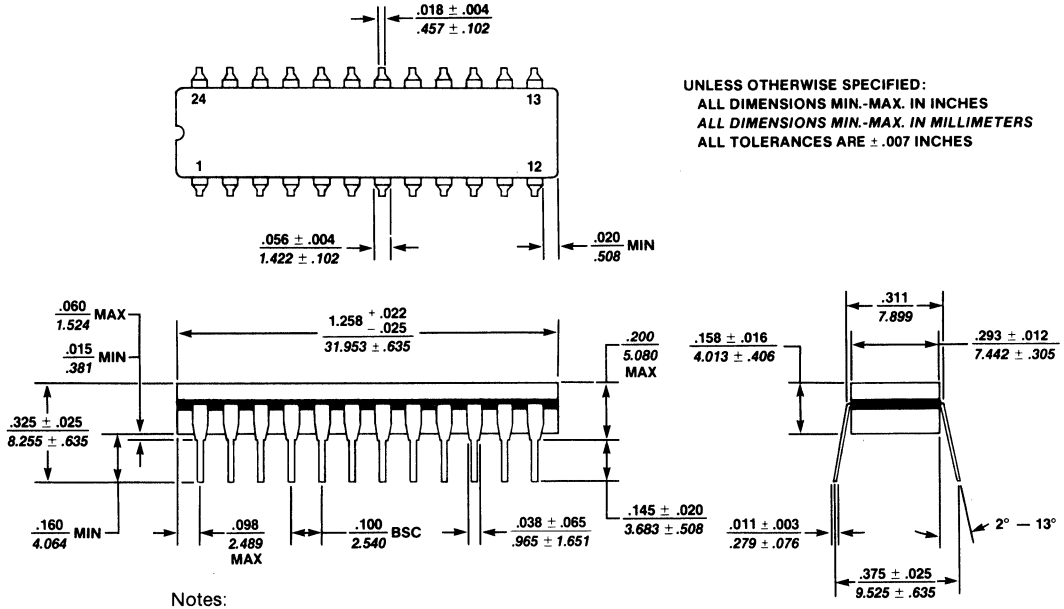
20J Ceramic DIP
Mil-M-38510,
Appendix C, D-8



10751A

Package Drawing

24JS Ceramic SKINNYDIP
Mil-M-38510,
Appendix C, D-9



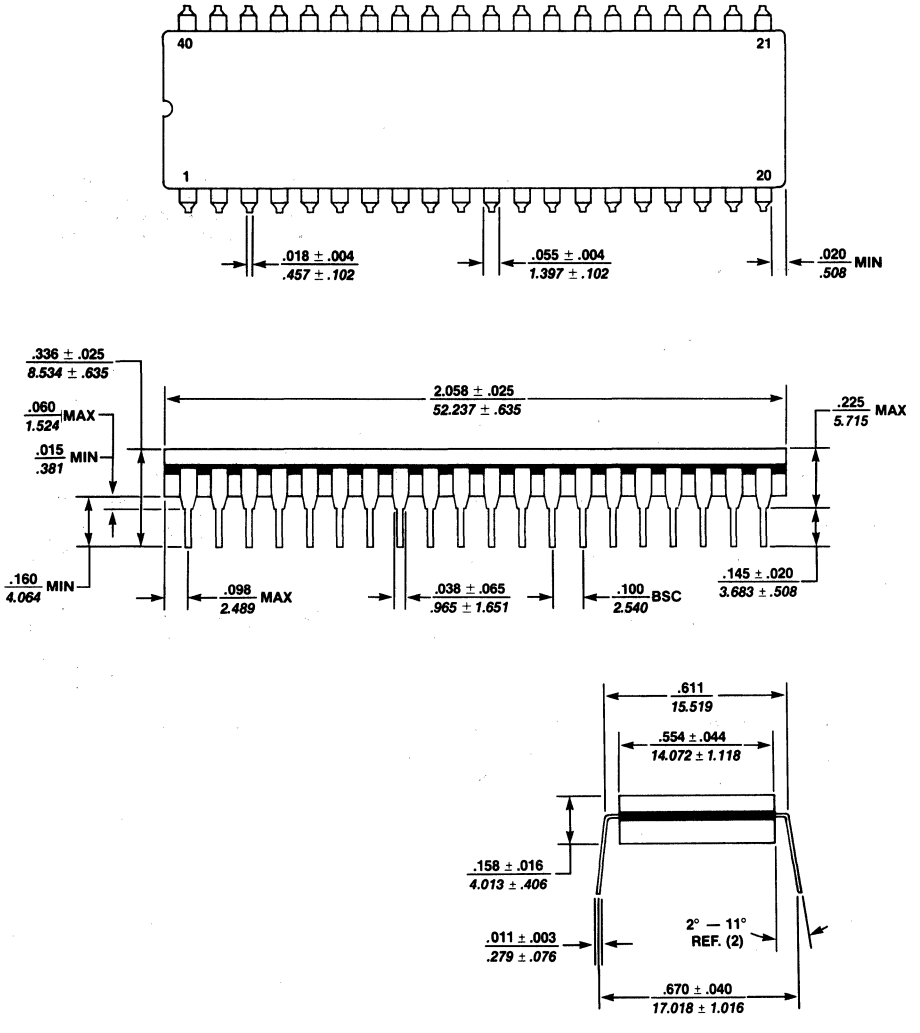
Notes:

1. Specified body dimensions allow for differences between MSI and LSI packages.
2. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.

10752A

Package Drawing

40J Ceramic DIP
Mil-M-38510,
Appendix C, D-5



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

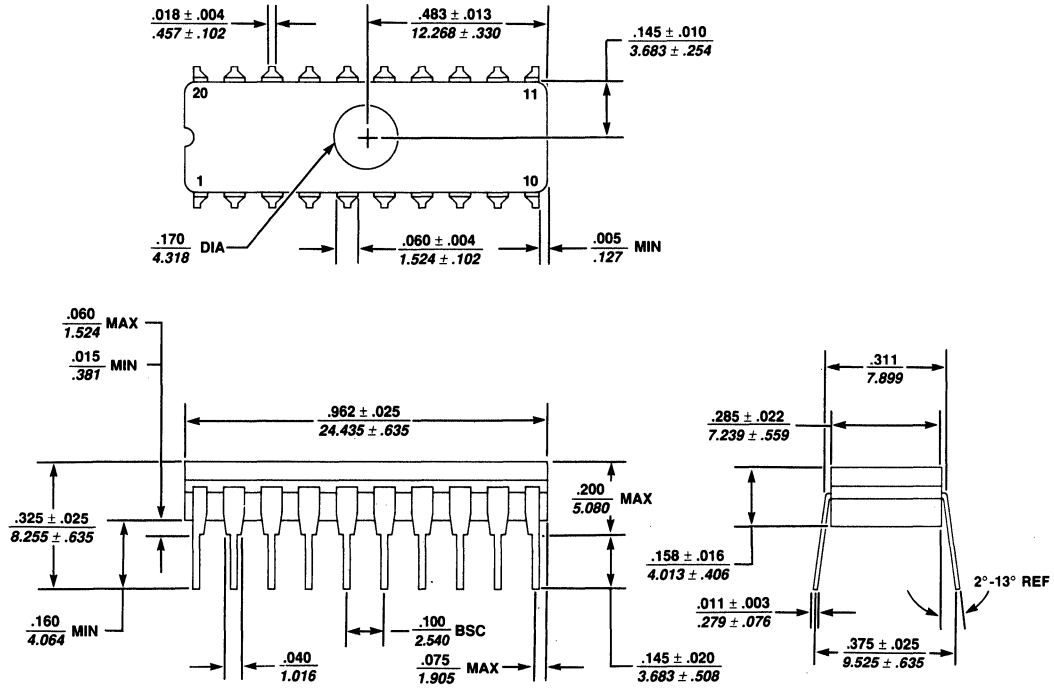
10753A

Notes:

1. Specified body dimensions allow for differences between MSI and LSI packages.
2. Lead material tolerances are for tin plate finish only. Solder dip finish adds 2-10 mils thickness to all lead tip dimensions.

Package Drawing

20Q Window CERDIP



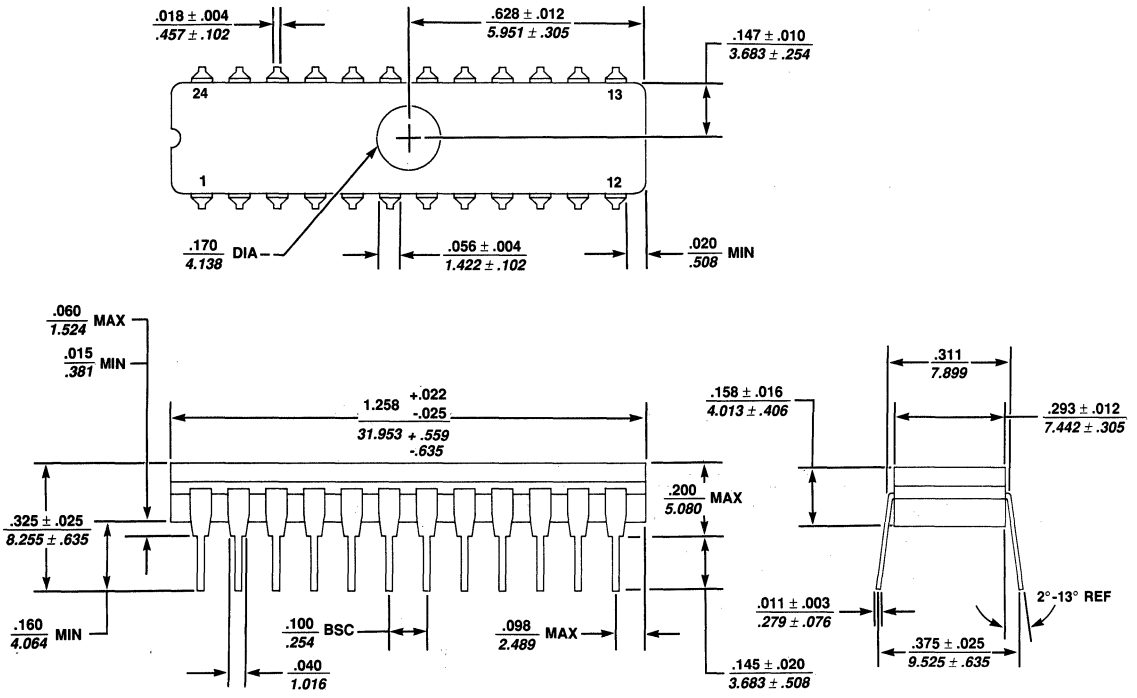
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

10754A

6

Package Drawing

24-QS Window CERDIP
(5/16″ x 1 1/4″)

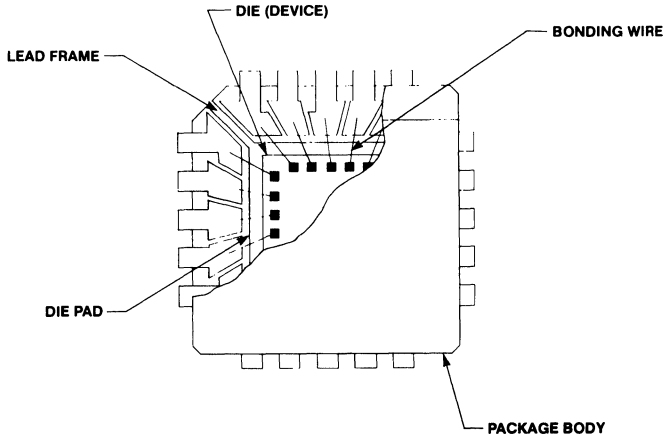


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

10755A

Package Drawing

Plastic Leaded Chip Carrier

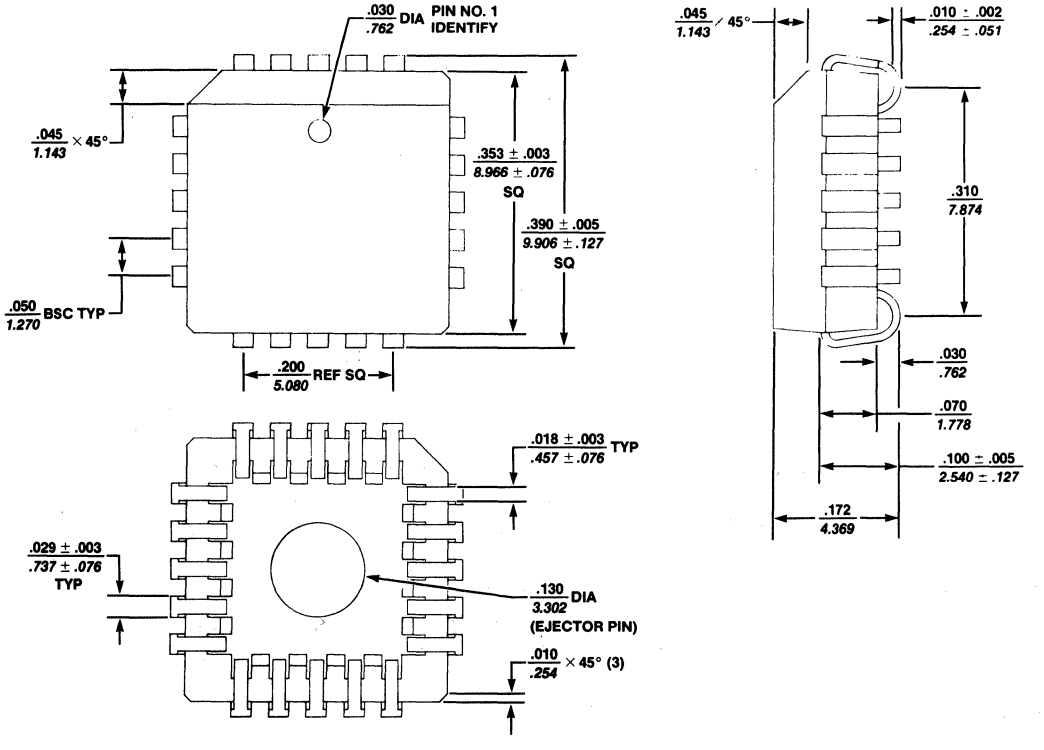


LEAD FRAME	BONDING WIRE	PACKAGE BODY
Copper Alloy 195. Copper Alloy Tamac 5.	1.25 Mil Gold Wire	Thermoset Plastic.
LEAD FINISH	**DIE PAD**	**DIE BOND**
Tin Plating. Solder Dip.	Spot Silver Plating (150 Microinches).	Silver Filled Epoxy.

10756A

Package Drawing

20NL Plastic Leaded Chip Carrier
(.351" x .351")



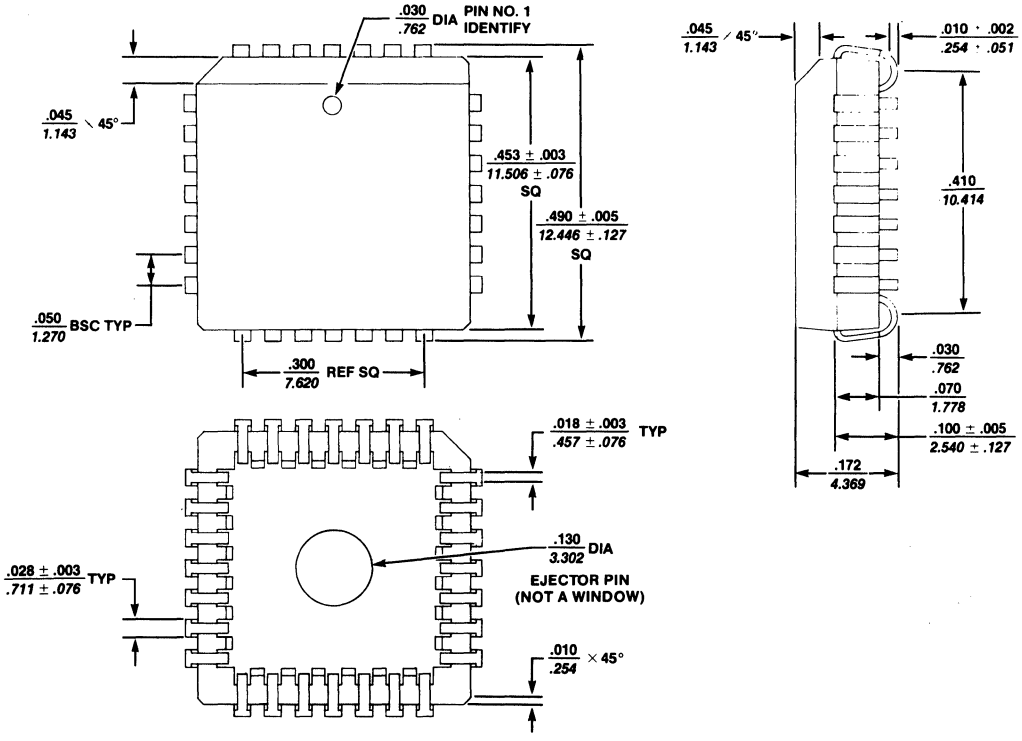
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

10757A

Package Drawing

28NL/FN Plastic Leaded Chip Carrier

(.451" x .451")



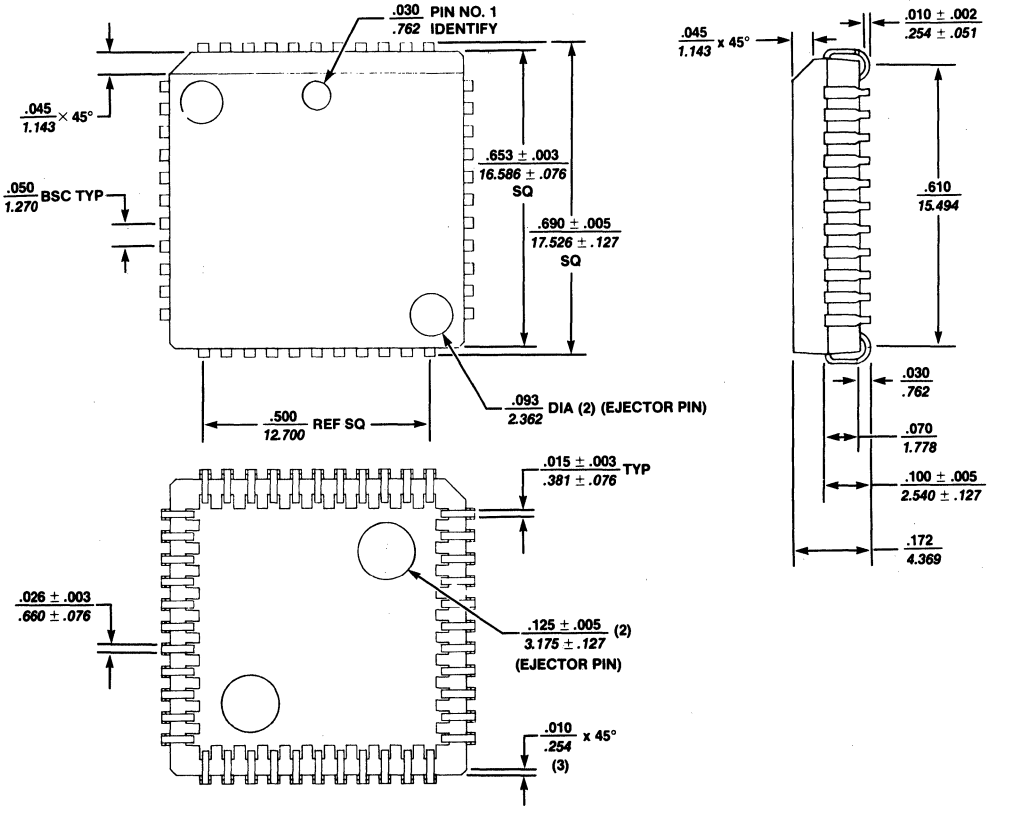
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

10758A

6

Package Drawing

44NL Plastic Leaded Chip Carrier
(.650" x .650")

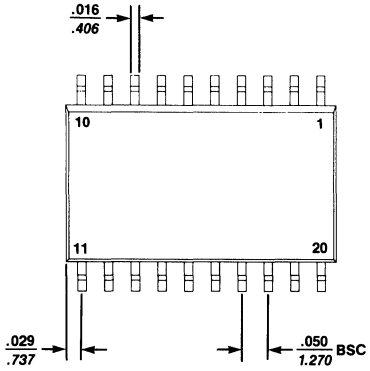


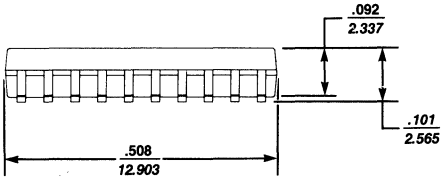
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

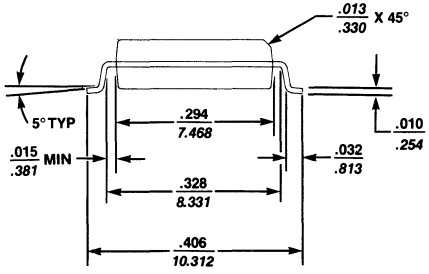
10759A

Package Drawing

20SG Small Outline Package







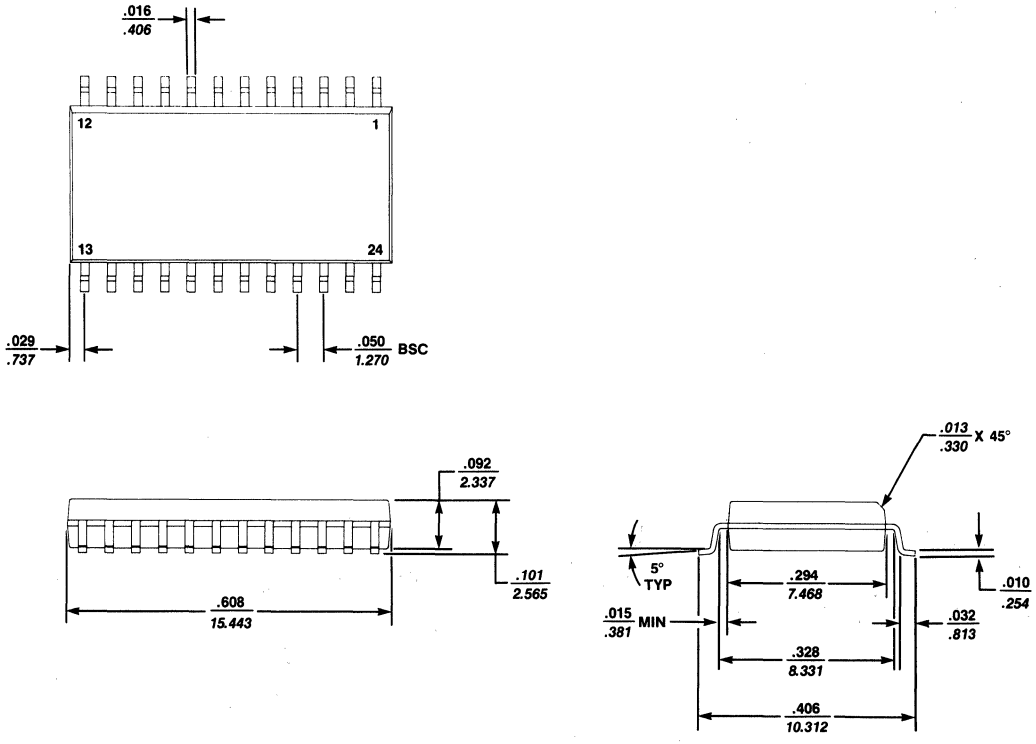
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

10762A

6

Package Drawing

24SG Small Outline Package

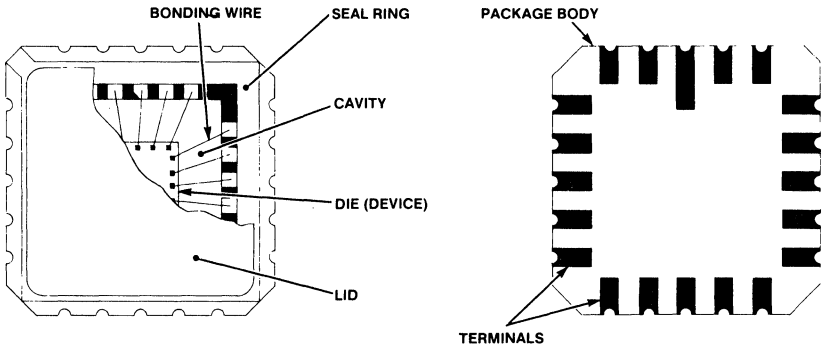


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

10763A

Package Drawing

Leadless Chip Carrier



PACKAGE BODY

Alumina
(Standard Dark)

BONDING WIRE

1.25 Mil Aluminum

LID

Gold Plated Kovar With
Nickel Underplating

CAVITY/SEAL RING

Gold Over Nickel
Over Tungsten

TERMINALS

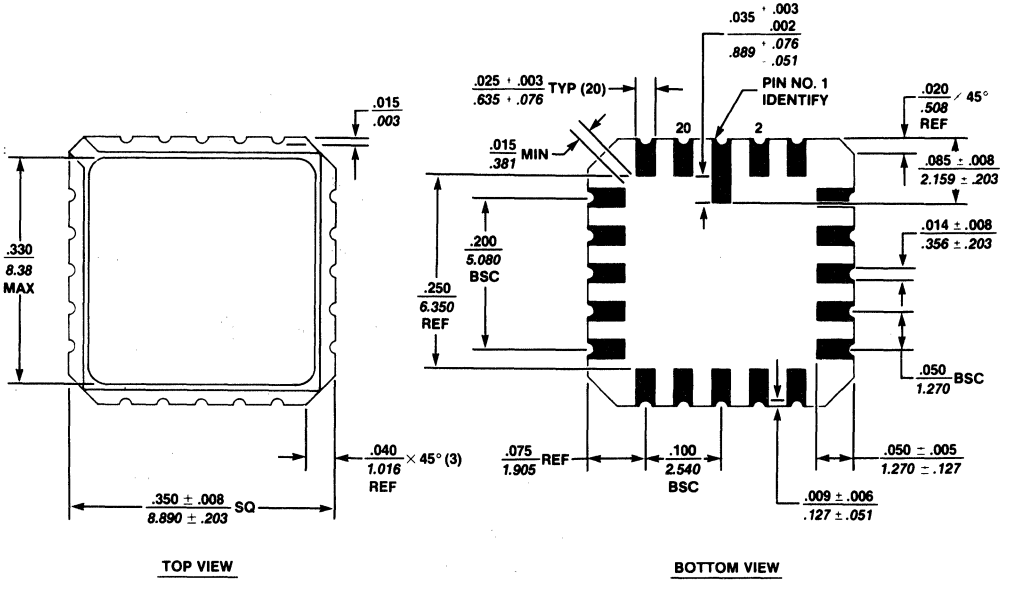
Gold Plating Over Tungsten

10767A

6

Package Drawing

20L Leadless Chip Carrier
Mil-M-38510,
Appendix C, C-2



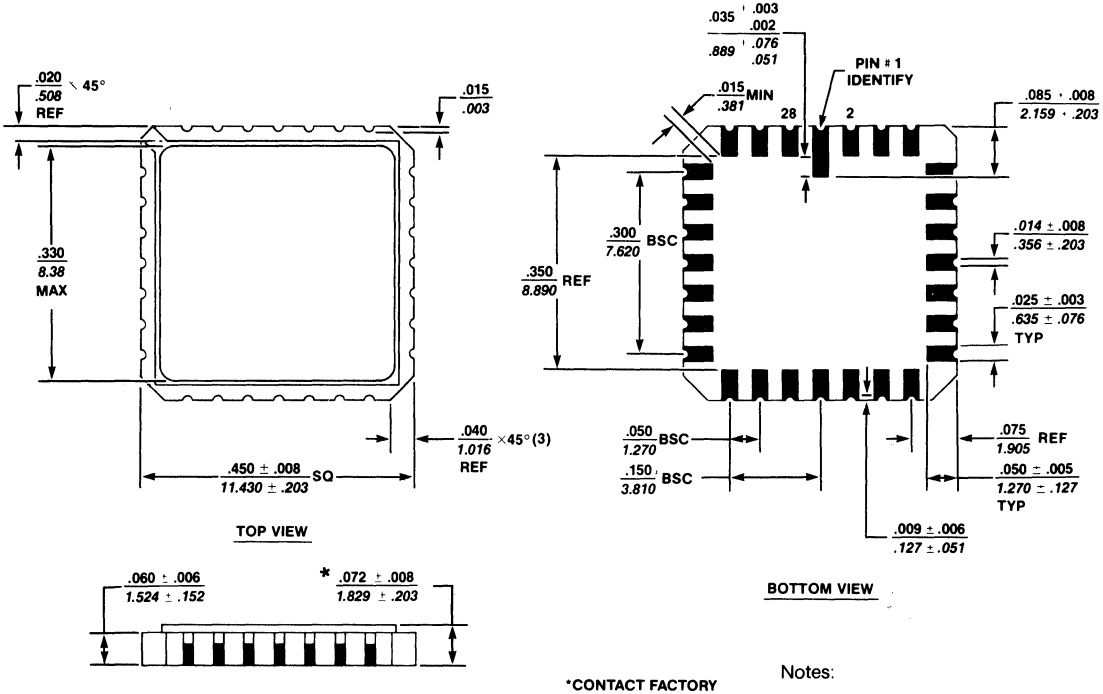
*CONTACT FACTORY FOR THIN PROFILE PKG.

UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

10768A

Package Drawing

28L Leadless Chip Carrier
Mil-M-38510,
Appendix C, C-4



Notes:

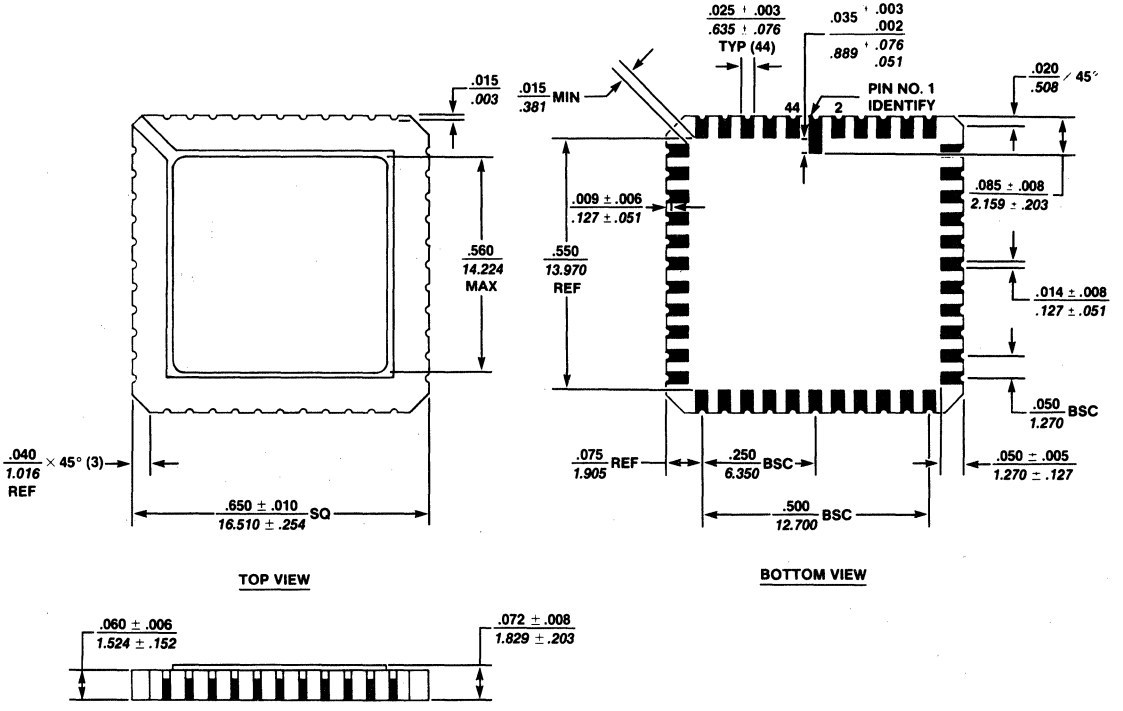
1. Solder fillets on lid edges not shown.

UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

10769A

Package Drawing

44L Leadless Chip Carrier
Mil-M-38510,
Appendix C, C-5

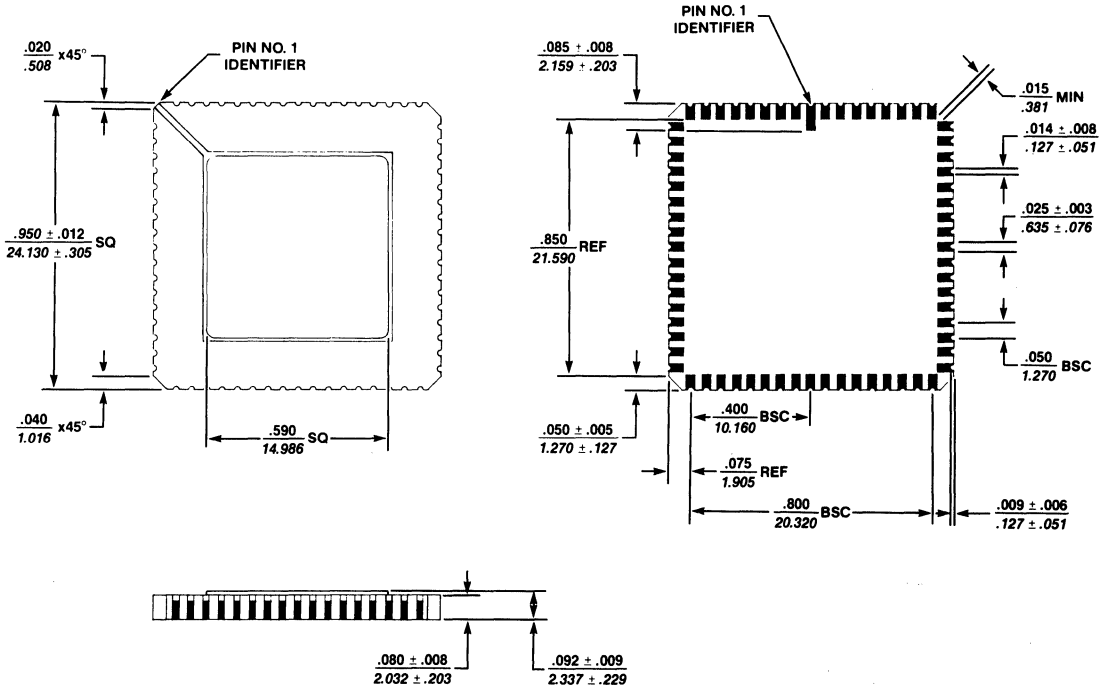


UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

10770A

Package Drawing

68L Leadless Chip Carrier
MIL-M-38510
Appendix C, C-7

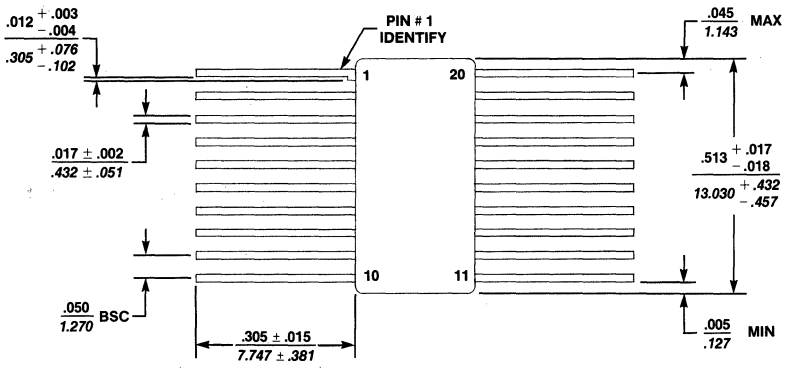


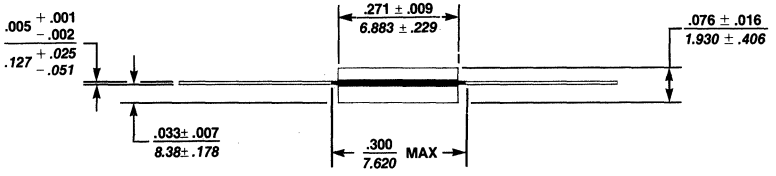
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

10771A

Package Drawings

20W Cerpack
Mil-M-38510,
Appendix C, F-9

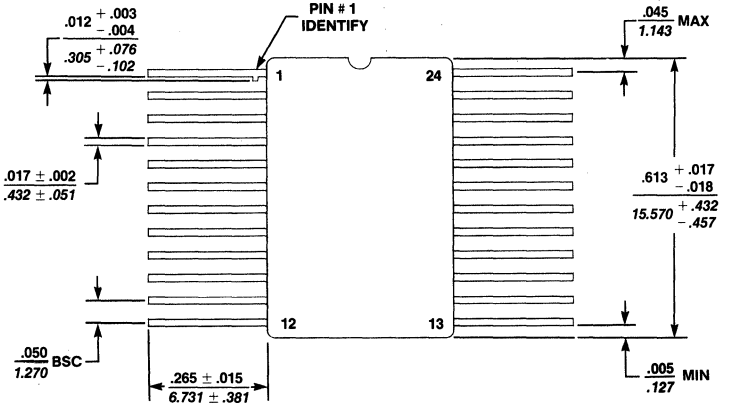


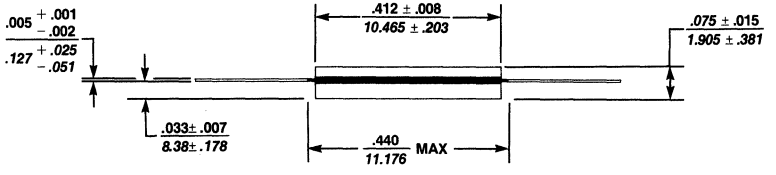


(GLASS FLOW)

10788A

24W Cerpack
Mil-M-38510,
Appendix C, F-6





(GLASS FLOW)

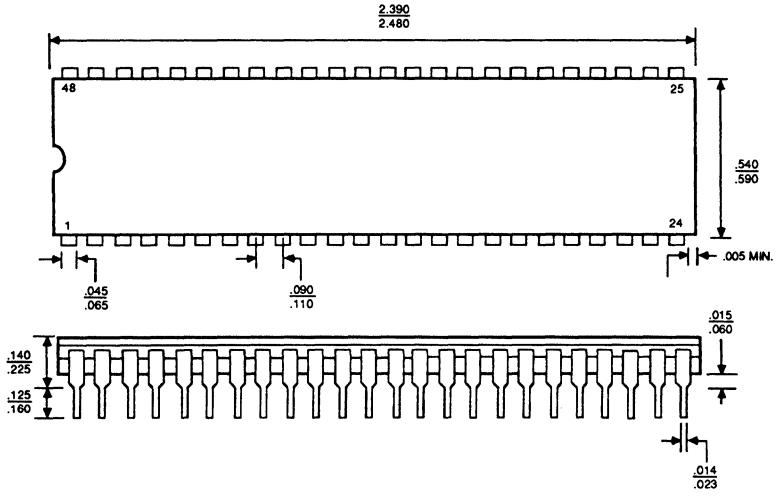
UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES
ALL DIMENSIONS MIN.-MAX. IN MILLIMETERS
ALL TOLERANCES ARE ± .007 INCHES

10789A

AMD Package Outlines

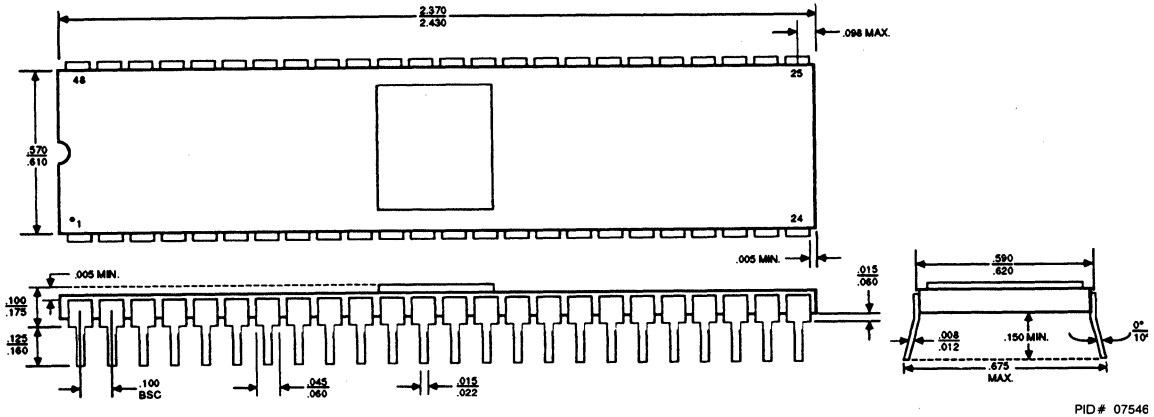
PHYSICAL DIMENSIONS*

PD 048



PID# 06566C

SD 048

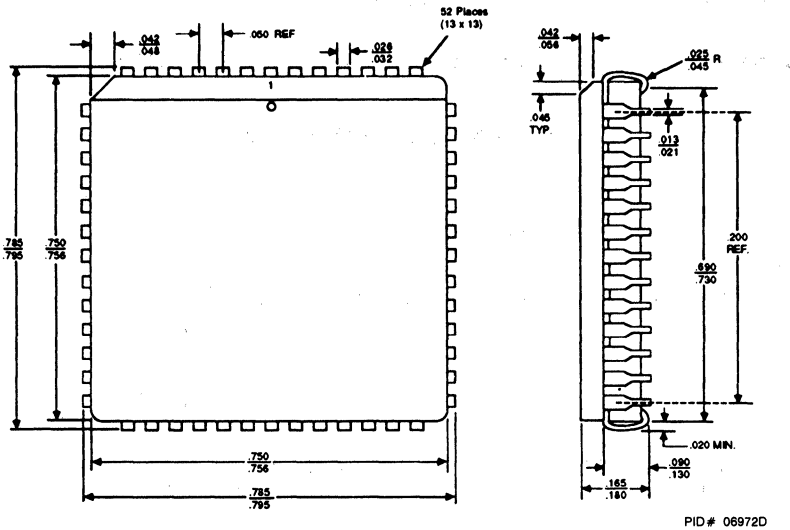


PID# 07546

*For reference only. All dimensions are measured in inches. BSC is an ANSI standard for Basic Space Centering.

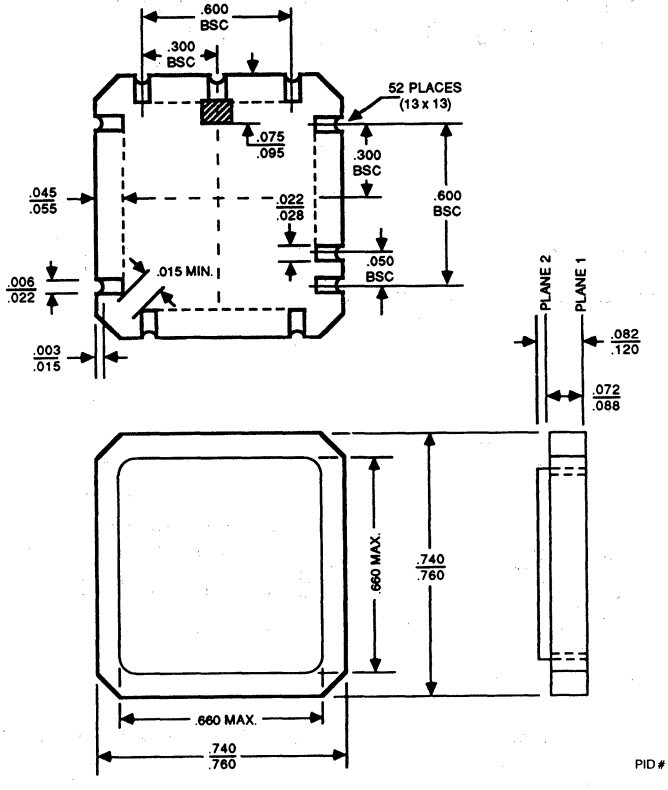
PHYSICAL DIMENSIONS (Cont'd.)

PL 052



PID # 06972D

CL 052



PID # 06705D

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