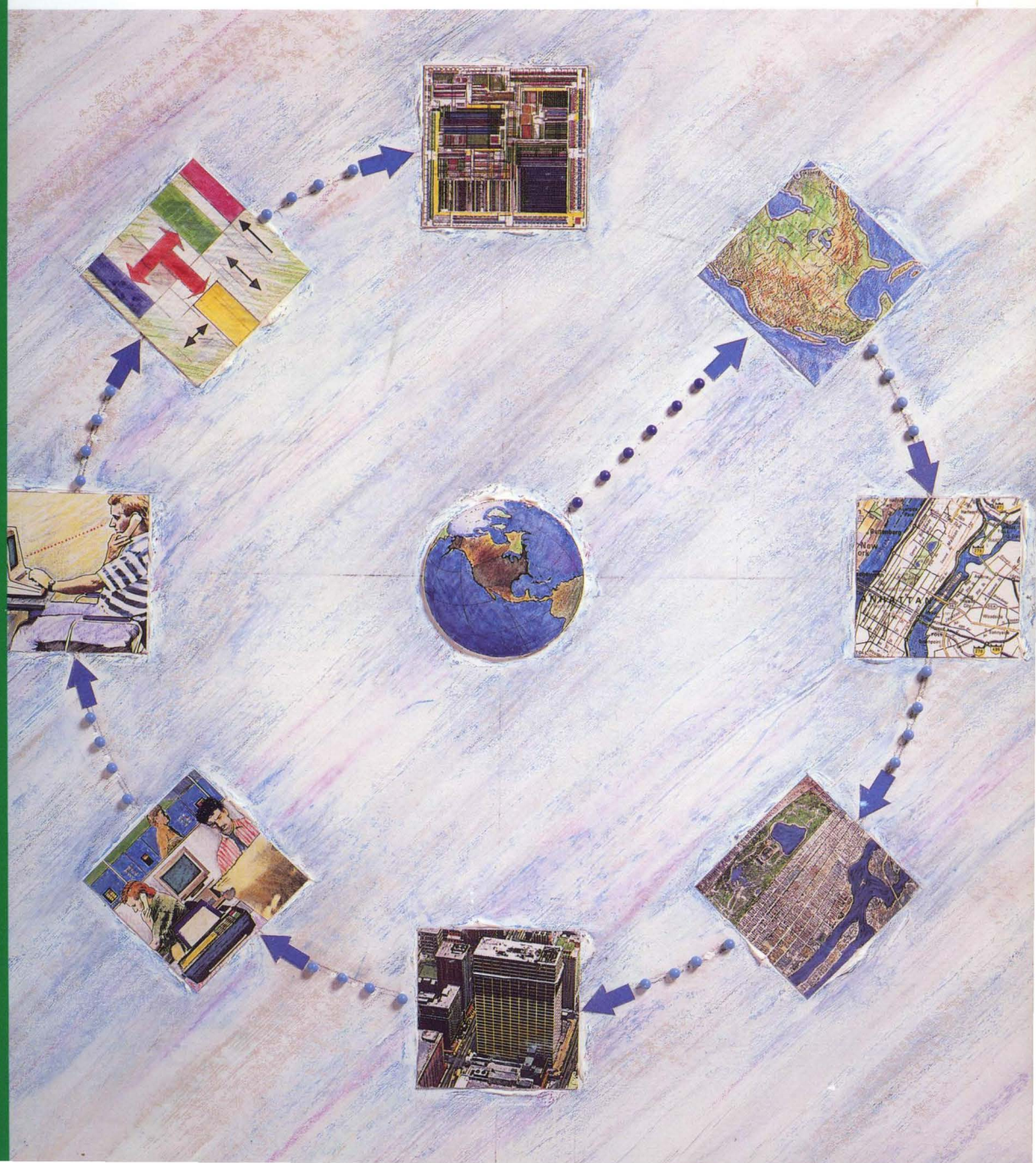
The World Network™ Catalogue

1989/1990

Advanced
Micro
Devices



The World Network™ Catalogue
1989/1990
AMD

Advanced Micro Devices

The World Network™ Catalog

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The World Network™ is an international web of voice, data and video communications facilities. With over 600 million telephones, millions of miles of cable and countless data terminals and computers, it is the largest man-made structure ever created. This World Network is a catalyst for our emerging global economy. Economies are no longer confined to small areas or even countries—they have become inextricably bound into a global economy.

This catalog is your quick reference to Advanced Micro Devices' broad range of communication products that are the tools needed to produce equipment for the World Network. These products cover a vast spectrum of communications functions from traditional voice circuits to datacom, networking, facsimile, encryption and ISDN.

AMD's system approach in defining and designing our products helps you solve your complex system design problems in a cost-effective manner. Through digital signal processing we allow you to implement high performance system functions inexpensively yet leave you the flexibility to control and/or modify device operation with software. We also understand the importance of getting your design to market quickly. Therefore, our complete solution goes well beyond just a chip. It includes evaluation tools and proven certified software modules necessary for your success.

AMD technical support stands with the best in the industry. Our trained field applications engineers, specialists in communications, are backed by system experts in the factory. So, give your local AMD sales office or the authorized representative listed in the back of this publication a call for complete device specifications. You will be glad you did because no one supplies a better solution for the World Network than Advanced Micro Devices.

Gary Ashcraft
Vice President
Communication Products Division

THE WORLD NETWORK™ CATALOG

Table of Contents

(continued)

Table of Contents (continued)

MODEM PRODUCTS

MODEM OVERVIEW

COMPLETE FSK MODEMS ON A SINGLE WORLD-CHIP®

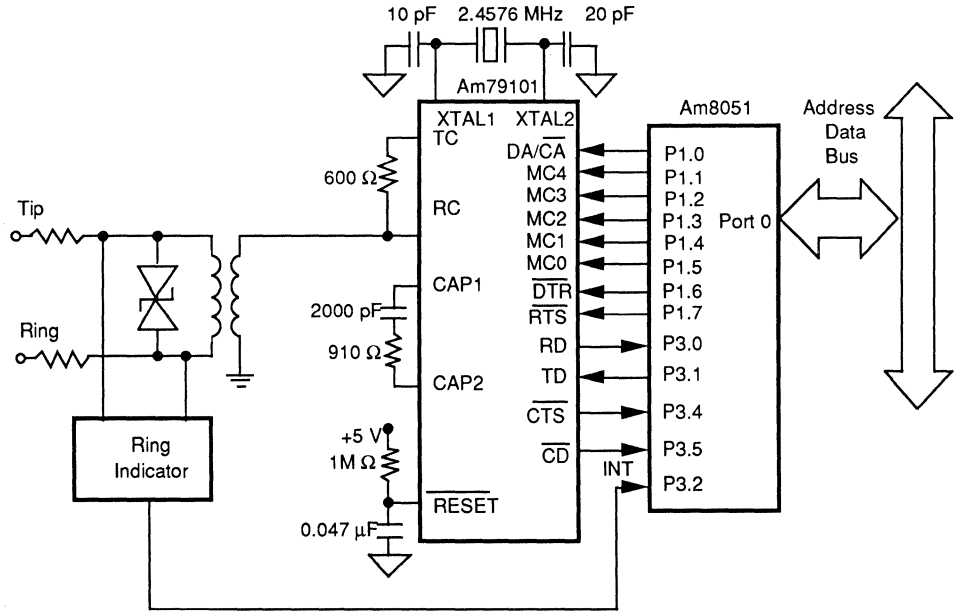
They Are the World's Most Popular

The Am79101, Am7911, and Am7910 modem family is being used in more countries, by more users on a greater variety of applications than any other FSK modem family in the world. And for very good reasons. They offer premium performance without breaking your budget. They require minimal board space with surface mount packages and few external components. Reliability is designed in with DSP technology Sand backed up with trillions of hours of rock solid operation.

They Are the World's Most Complete

All the features a modem should have are built right in. Filters are already there. So are handshake signals, auto-answer, local loopback and back channels. No extra components are required to implement these functions. In addition, the Am79101 is the only FSK modem that supports autodial with DTMF generation, Call Progress Tones Detection, and Answer Tones Detection. The 4- to 2-wire hybrid is also included on-chip. No other FSK modem chip provides so many features.

Typical Circuit Configuration



MODEM CONFIGURATIONS

STANDARD	BIT-RATE	DUPLEX	FEATURES
Bell 103	300	Full	Originate
Bell 103	300	Full	Answer
Bell 202	1200	Half	w/o Line Equalizer
Bell 202	1200	Half	w/Line Equalizer
Bell 202*	1200	Half	150 bps Back Channel
Bell 202*	1200	Half	150 bps w/ Line Equalizer
CCITT V.21	300	Full	Originate
CCITT V.21	300	Full	Answer
CCITT V.23 mode 2	1200	Half	w/o Line Equalizer
CCITT V.23 mode 2	1200	Half	w/Line Equalizer
CCITT V.23 mode 2*	1200	Half	150 bps Back Channel
CCITT V.23 mode 2*	1200	Half	150 bps w/Line Equalizer
CCITT V.23 mode 1	600	Half	

*Am7911 and Am79101 only.

Each is a WORLD-CHIP

No matter where you market your product, the Am79101, the Am7911 or the Am7910 is the perfect modem solution. Without any additional circuitry, they can be switched to any of nine Bell or CCITT standards. The flexibility of Digital Signal Processing (DSP) allows systems built with the AMD modems to be used all over the world without modification to the modem circuit.

Whether your equipment is intended for leased-line or switched-network applications, AMD has the FSK modem for you. For switched-network applications, the Am79101 is the recommended device. All of the carrier detects and handshake timings are compatible with the Bell and CCITT recommendations for switched network use. The Am79101 also provides full autodial support with on-chip DTMF generation, Call Progress Tones Detection and discrete Answerback Tones Detection. The on-chip 4- to 2-wire hybrid further simplifies the interface to the telephone line. For leased-line, telex and non-autodial switched network applications, use the Am7911. The Am7911 carrier detect and handshake timings are compatible with the requirements for leased-line and telex applications, including CCITT recommendation R.20.

Selectable to Any of Nine Different World Standards

These modems are being used in equipment all over the world. The devices operate in Bell 103 and 202, and CCITT V.21 and V.23 modem configuration at baud rates from 300 to 1200 bps (with back channel). 1200 bps full-duplex operation is also available with the Am7911 using Bell 202 and CCITT V.23 loopback modes over four-wire lines. Mode selection is controlled by five simple programming inputs. No crystals need to be changed. No extra resistors, capacitors, or interface circuits are needed— just switch a few control lines.

Final

Am79101

WORLD-CHIP® Autodial FSK Modem

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Bell 103, 113, 108 and CCITT V.21 compatible at 300 bps full-duplex
- Bell 202 and CCITT V.23 compatible at 1200 bps half-duplex with up to 150 bps back-channel (CCITT V.23 modes with optional soft carrier turn-off feature)
- Autodial support
  - –Dual-Tone Multi-Frequency (DTMF) Tone Generation
  - –Call-Progress Tone Detection
  - –Answer-Tone Detection
- Single-chip digital signal processor
- Integral 4- to 2-wire hybrid
- Public Switched Telephone Network (PSTN) response times
- Serial RS-232C/CCITT V.24-type handshake interface and protocol

GENERAL DESCRIPTION

The Am79101 WORLD-CHIP is a single-chip asynchronous Frequency Shift Keying (FSK) modem that is compatible with the applicable Bell and CCITT-recommended standards for 103/113/108, 202, V.21 and V.23-type modems. All modulation, demodulation, filtering, analog-to-digital and digital-to-analog functions are provided on-chip.

Using the features described here, an intelligent Autodial, Autoanswer FSK modem may be implemented with only an Am79101 single-chip under the control of a host microprocessor and a Data Access Arrangement (DAA) circuit.

The modem operates in a serial asynchronous mode; the serial interface supports the RS-232C/CCITT V.24-type handshake signals at TTL levels.

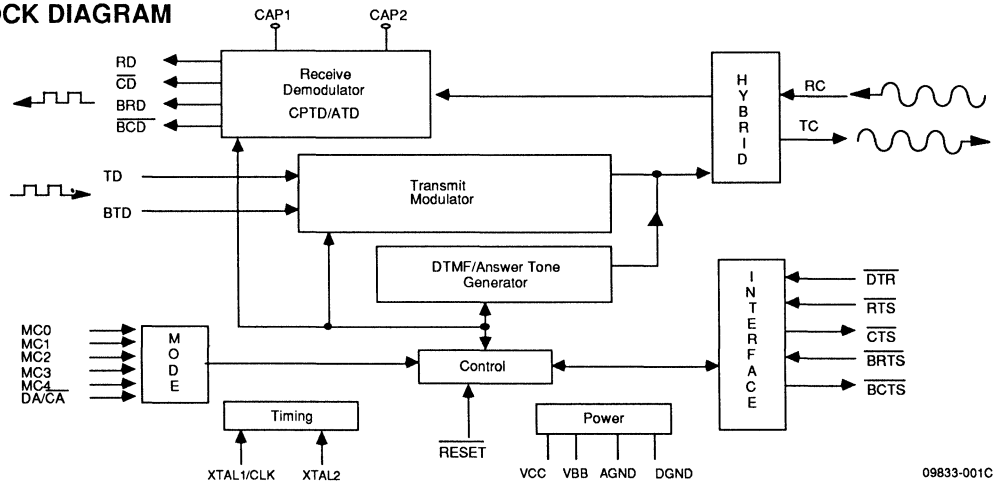
The modem analog interface provides an internal hybrid for the 4- to 2-wire conversion. Auxiliary functions performed within the Am79101 include:

- Autodial support with DTMF generation and Call Progress Tone Detection.
- Answer Tone Detection (Bell and CCITT).
- Autoanswer support.
- Analog loopback support.

The Am79101 is housed in a 28-pin plastic leaded chip carrier as well as 28-pin plastic and ceramic dual-in-line packages.

Connection to the telephone network may be via a DAA or an acoustic coupler. All digital I/O signals are TTL-compatible, except the external clock and $\overline{\text{RESET}}$ signals, and the circuit operates from ±5 V.

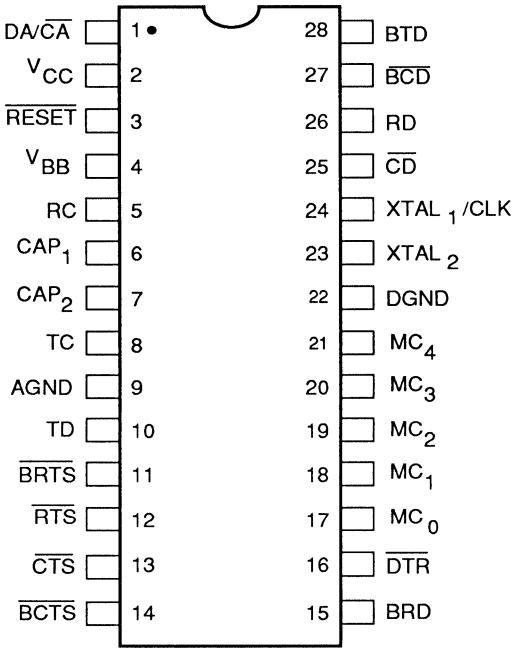
BLOCK DIAGRAM



Publication #09833 Rev. Amendment /0
Issue Date: February 1989

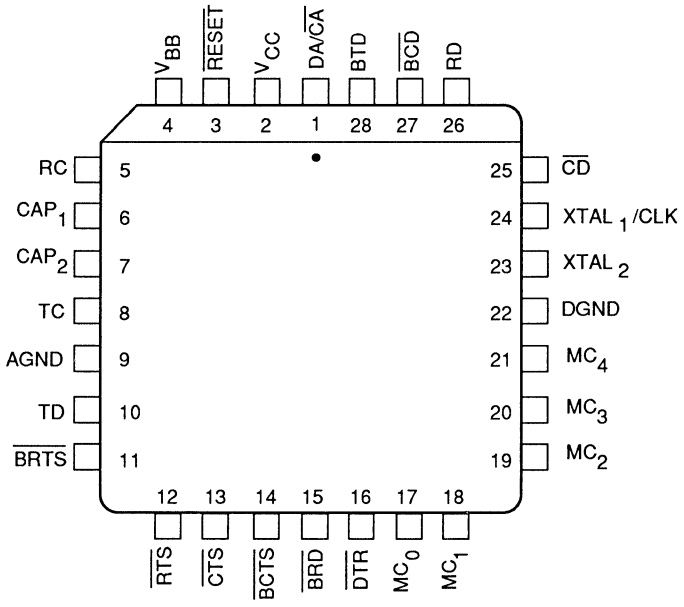
CONNECTION DIAGRAMS
Top View

28-Pin DIP



09833-2A

28-Pin PLCC



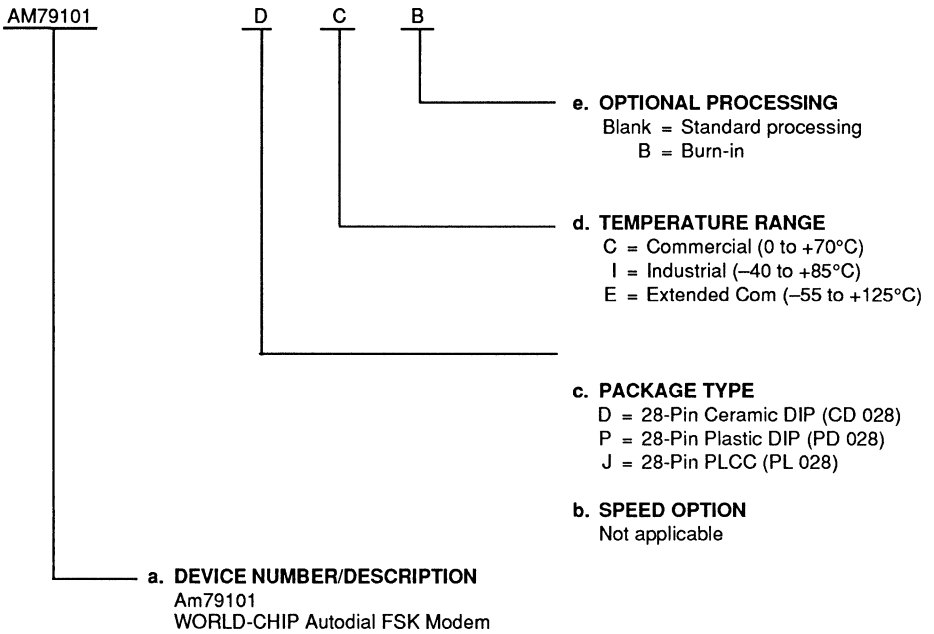
Note: Pin 1 is marked for orientation.

09833A-2

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM79101	DC, DCB, DI, DIB, PC, DE, DEB, JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

Am7910/11

WORLD-CHIP® FSK MODEM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

Common Capabilities

- Complete FSK Modem in 28-pin package
- 300 bps full-duplex operation
- 1200 bps half-duplex operation
- 1200 bps full-duplex on 4-wire
- Compatible with Bell 103/113/108, Bell 202, CCITT V.21, and V.23
- Available in CDIP, PDIP, and PLCC packages
- Commercial, Industrial and Extended temperature range
- No external filtering required
- All digital signal processing, digital filtering, and A/D-D/A conversion on-chip
- Includes essential RS-232/CCITT V.24 handshake signals on-chip
- Autoanswer capability

Unique Device Capabilities

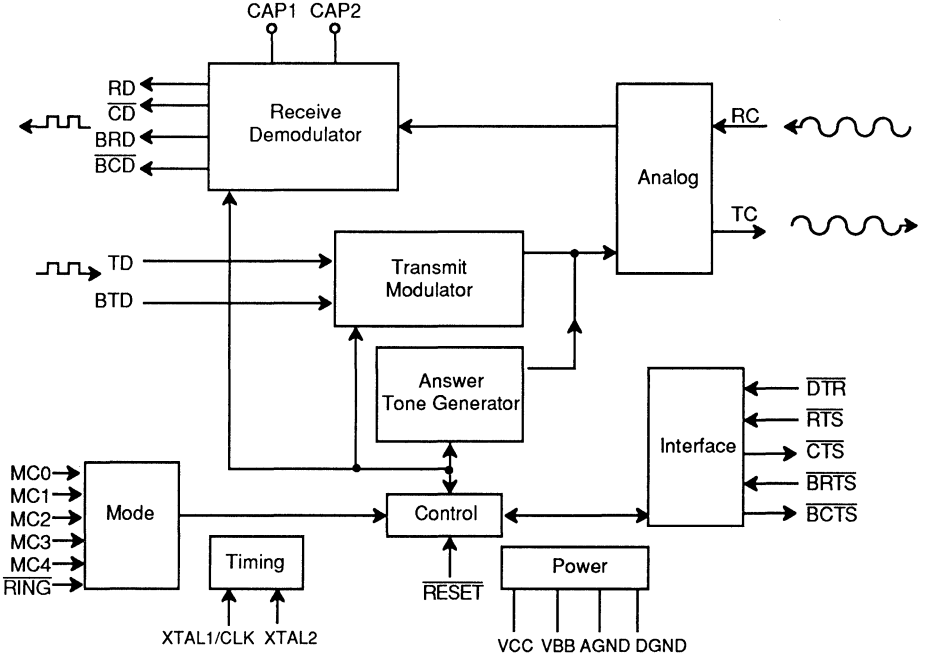
Am7910

- Dial-up network response times
- Bell 202 with 5 bps back channel
- V.23 with up to 75 bps back channel

Am7911

- Fast response time for leased-line networks
- Bell 202 with 5 bps or 150 bs back channel
- V.23 with up to 150 bps back channel

BLOCK DIAGRAM



Publication # 04262 Rev. Amendment /0
Issue Date: March 1989

GENERAL DESCRIPTION

Advanced Micro Devices offers a family of high-performance FSK modem chips that may be easily integrated in system designs to interface terminals and workstations to the Telephone Network. The product family consists of:

–Am7910 FSK Modem

–Am7911 FSK Modem

–Am79101 Autodial FSK Modem

Am7910 and Am7911

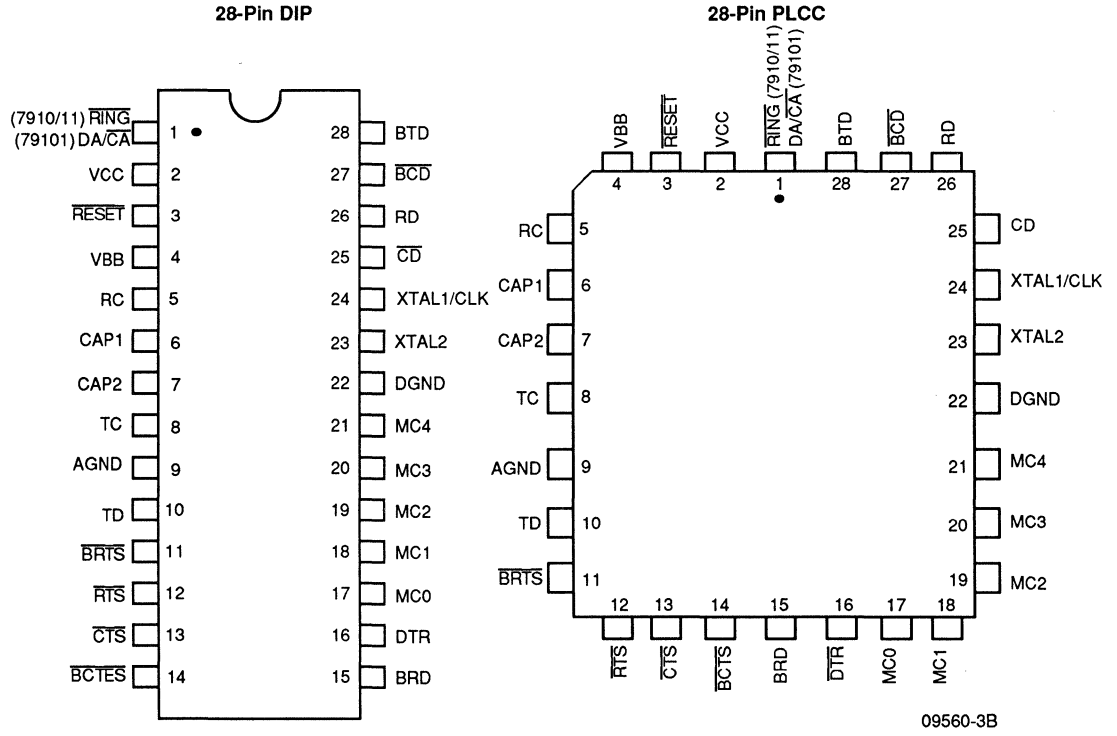
AMD currently offers three single-chip modems in the Frequency Shift Keying (FSK) series including the Am7910, the Am7911 and the Am79101. This family of modems includes most of the building blocks required for a complete communication system. Some of the on-chip features include: analog-to-digital and digital-to-analog converters, internal crystal oscillator, and the essential RS-232/CCITT V.24 terminal control signals with TTL levels. A DAA (Data Access Arrangement) or acoustic coupler must be supplied externally to provide the Phone Line Interface.

The FSK modem chips all have the same basic structure as shown in the simplified block diagram. The Am7910 and the Am7911 differ mainly in timing parameters with the Am7911 being tailored for better performance in leased-line, multidrop applications. The Am7911 also includes an extended set of modem selection modes.

The Am79101 is described in a separate data sheet (order no. 09833).

CONNECTION DIAGRAMS

Top View



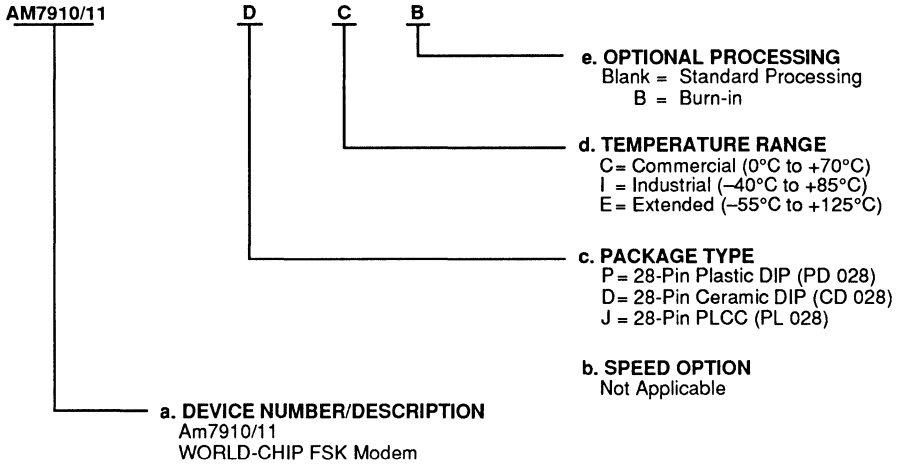
Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7910 AM7911	PC, JC, DC, DCB, DI, DIB, DE, DEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

INTEGRATED SERVICES DIGITAL NETWORK (ISDN)

INTEGRATED SERVICES DIGITAL NETWORK (ISDN)

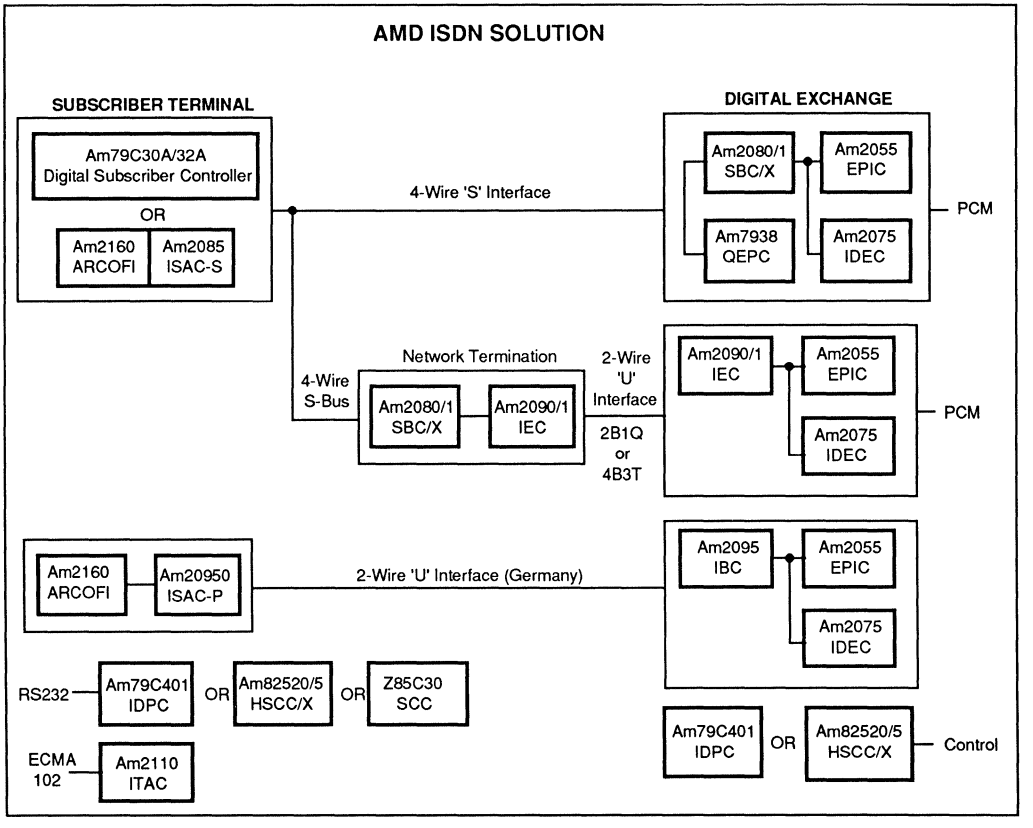
ISDN is the standard for conversion of the world telephone network to an integrated, public digital network for both voice and data. ISDN technology is being implemented and tested in many parts of the world, and its use will accelerate as the speed and cost advantages of digital communications become readily apparent. The ISDN network will provide a multitude of new services offering simultaneous transmission and reception of voice, data and video over a common network

There are important advantages to ISDN. An ISDN system lowers the operating cost of a local network because it makes better utilization of line capacity and is less expensive to install and maintain than other implementations. ISDN is faster, more effective and easier to implement than older methods. Because it is digital, ISDN produces clearer voice messages and fewer data errors.

One reason ISDN is so versatile is three separate channels for voice and data. For the ISDN Basic Interface, there are two "B" channels and one "D" channel. The two B-channels carry voice, packet-switched or circuit-switched data. They operate at 64,000 bits per second (64 Kbps)— about 50 times faster than most personal computer modems.

The D-channel operates at 16 kbps and is primarily used to control access to the ISDN network. For example, it is used to signal that a message is incoming on a B-channel. The D-channel can also be used to transmit packet-switched data while the B-channels are used for voice or other data.

Your products can take advantage of the revolution in digital communications with our ISDN solutions. We offer single-chip integrated solutions supporting voice and data using the ISDN interface.



Whether your application is terminal equipment, network terminators, line terminators, PABXs, concentrators or Central Office Line Cards, each IC is optimized for the network in which it operates. Your application uses fewer ICs, resulting in more compact designs. Your customer gets a product with more features, usually at a lower cost.

Our complete line of transceivers support the CCITT standard interface, major national interfaces, low-cost two-wire PBX interfaces and protocol processors for terminals and switches.

INTEGRATED SERVICES DIGITAL NETWORK (ISDN)

Terminal Products

Am79C30A

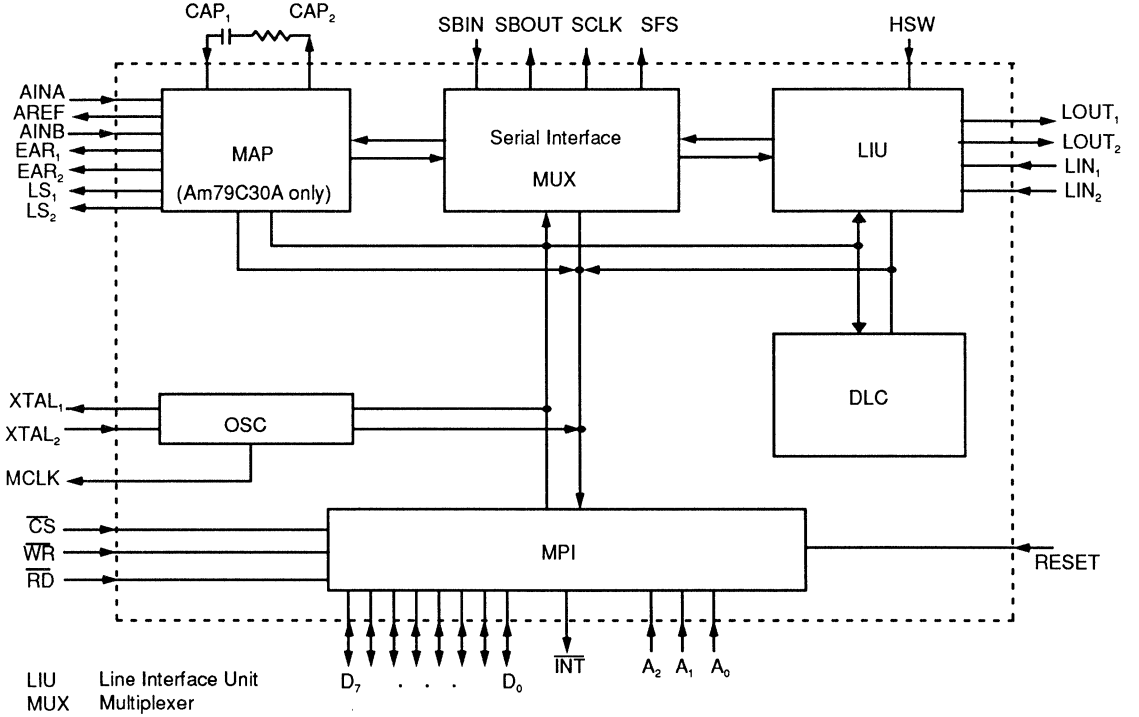
Digital Subscriber Controller (DSC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Combines CCITT I.430 S/T Interface transceiver, D-channel LAPD processor, and audio processor in a single chip
- Interrupt-driven microprocessor interface
- CMOS technology, TTL compatible
- "S" or "T" Interface Transceiver
  - Level 1 Physical Layer Controller
  - Supports point-to-point, short or extended passive bus configurations
  - Multiframe support
- D-channel Processing Capability
  - Flag generation/detection
  - CRC generation/checking
  - Zero insertion/deletion
  - Four 2-byte address detectors
  - Random number generation
  - 8-byte transmit and receive FIFOs
- Audio Processing Capability
  - Dual audio inputs
  - Earpiece and loudspeaker drivers
  - Filter/codec with A/μ selection
  - Programmable gain and equalization filters
  - Programmable sidetone level
  - Programmable DTMF, single tone, and ringer tone generation
- Pin and software compatible with the Am79C32A ISDN Data Controller (IDC)

BLOCK DIAGRAM



LIU	Line Interface Unit
MUX	Multiplexer
MAP	Main Audio Processor
DLC	Data Link Controller
MPI	Microprocessor Interface
OSC	Oscillator and Timing Circuitry

09456-1B

Publication # 09893 Rev. Amendment /0
Issue Date: March 1989

GENERAL DESCRIPTION

The Am79C30A Digital Subscriber Controller (DSC), shown in the block diagram, provides the Terminal Equipment access to the ISDN. The Am79C30A is compatible with the CCITT I-Series recommendations at the "S" reference point allowing the user of the device to design TEs which conform to the international ISDN standards.

The Am79C30A provides a 192 kbps full duplex digital path between the TE located in the subscriber's premises and the NT or PABX line card over 4-wires. The Am79C30A separates the bit stream into the B1 (64 kbps), B2 (64 kbps) and D (16 kbps) channels. The B-channels are routed to different sections of the Am79C30A under user control. The D channel is partially processed in the Am79C30A and passed to the microprocessor for further processing.

The transmission rate of 192 kbps provides a 48-bit frame every 250 µs for framing and maintenance. The frame structure provides for frame synchronization and multiple terminal contention resolution as described in the CCITT I-series recommendations. Both point-to-point and point-to-multipoint connections are supported.

The Am79C30A can be used as a voice telephone, a digital data terminal, or a voice and data terminal.

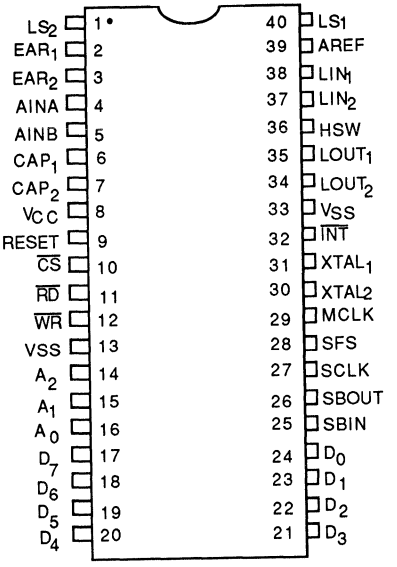
The audio processor in the Am79C30A, shown in the block diagram, uses Digital Signal Processing (DSP) to implement the codec and filter functions.The audio processor interfaces to a speaker, an earpiece, and two separate audio inputs. In the receive and transmit paths the user may program gain or alter the frequency response.

A serial port gives the user access to the B-channels of the Am79C30A multiplexer. This serial port may be used by data terminals and provides, with additional circuitry, access to the CCITT "R" reference point.

The Am79C30A is controlled via an interrupt driven microprocessor bus interface by an external microprocessor. Using this interface, the microprocessor processes the D-channel information and programs the Am79C30A accordingly. This includes programming a multiplexer within the Am79C30A to route the B-channels as specified by the D-channel control information. The microprocessor can interrogate and program the Am79C30A via its mode, status, and error registers.

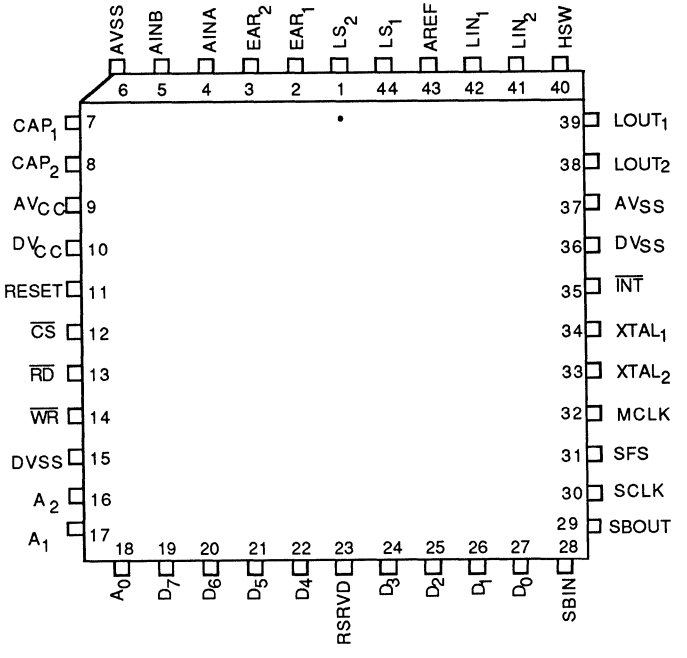
CONNECTION DIAGRAMS
Top View

40-Pin PDIP



09456-35B

44-Pin PLCC



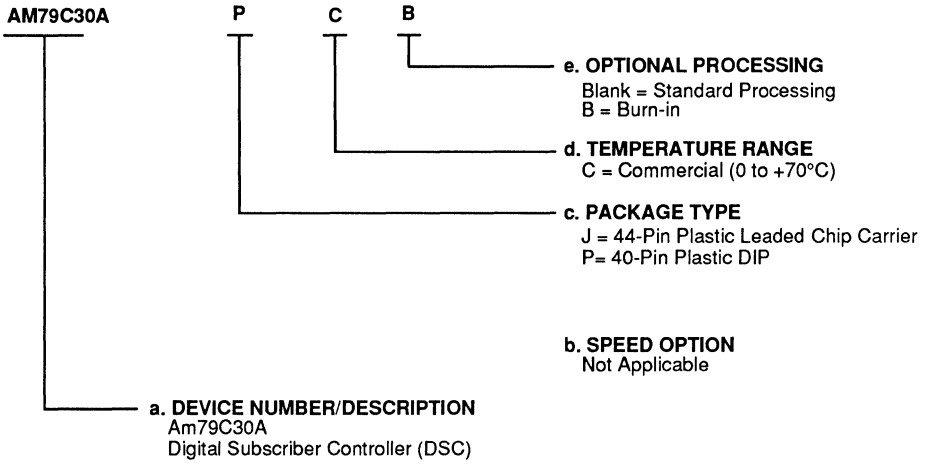
09456-36B

Note: Pin 1 is marked for orientation.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM79C30A	PC,JC,PCB,JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

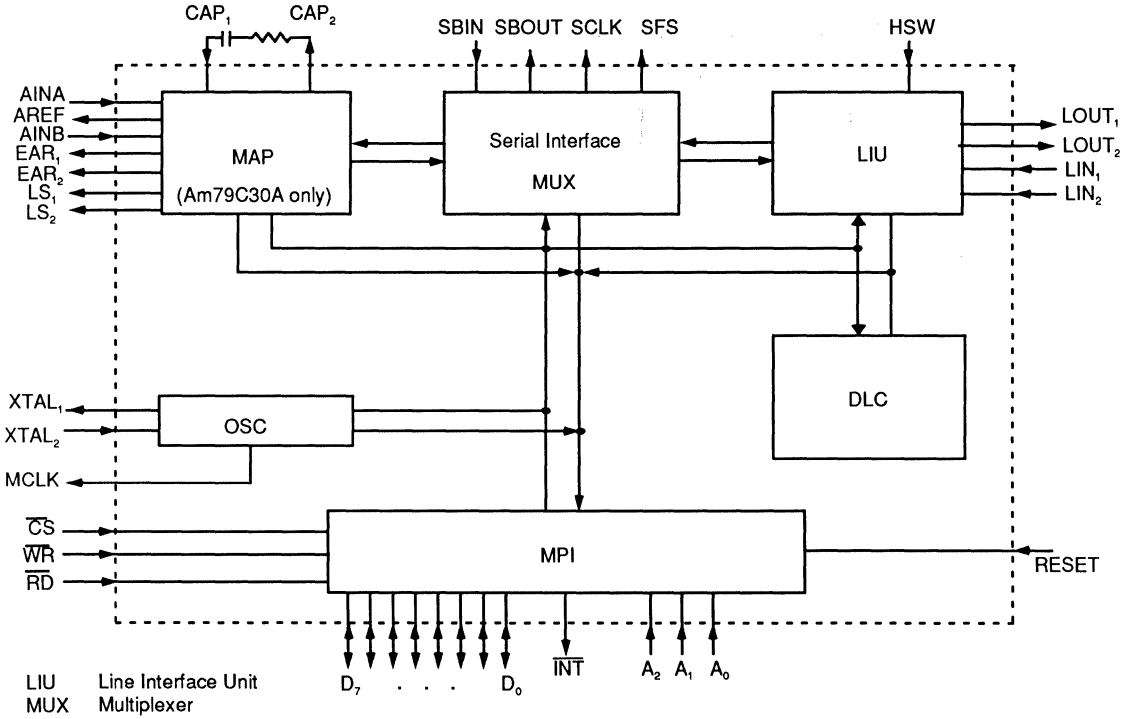
Am79C32A
ISDN Data Controller (IDC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Combines CCITT I.430 S/T Interface transceiver, D-channel LAPD processor in a single chip.
- Interrupt-driven microprocessor interface
- CMOS technology, TTL compatible
- "S" or "T" Interface Transceiver
  - Level 1 Physical Layer Controller
  - Supports point-to-point, short or extended passive bus configurations
  - Multiframe support
- D-channel Processing Capability
  - Flag generation/detection
  - CRC generation/checking
  - Zero insertion/deletion
  - Four 2-byte address detectors
  - Random number generation
  - 8-byte transmit and receive FIFOs
- Pin and software compatible with the Am79C30A Digital Subscriber Controller (DSC)

BLOCK DIAGRAM



LIU	Line Interface Unit
MUX	Multiplexer
MAP	Main Audio Processor
DLC	Data Link Controller
MPI	Microprocessor Interface
OSC	Oscillator and Timing Circuitry

09456-1B

Publication # 09893 Rev. D Amendment /0
Issue Date: March 1989

GENERAL DESCRIPTION

The Am79C32A ISDN Data Controller (IDC), shown in the block diagram, provides the Terminal Equipment access to the ISDN. The Am79C32A is compatible with the CCITT I-Series recommendations at the "S" reference point allowing the user of the device to design TEs which conform to the international ISDN standards.

The Am79C32A provides a 192 kbps full duplex digital path between the TE located in the subscriber's premises and the NT or PABX line card over 4-wires. The Am79C32A separates the bit stream into the B1- (64 kbps), B2- (64 kbps) and D- (16 kbps) channels. The B-channels are routed to different sections of the Am79C32A under user control. The D-channel is partially processed in the Am79C32A and passed to the microprocessor for further processing.

The transmission rate of 192 kbps provides a 48-bit frame every 250 µs for framing and maintenance. The frame structure provides for frame synchronization and multiple terminal contention resolution as described in the CCITT I-series recommendations. Both point-to-point and point-to-multipoint connections are supported.

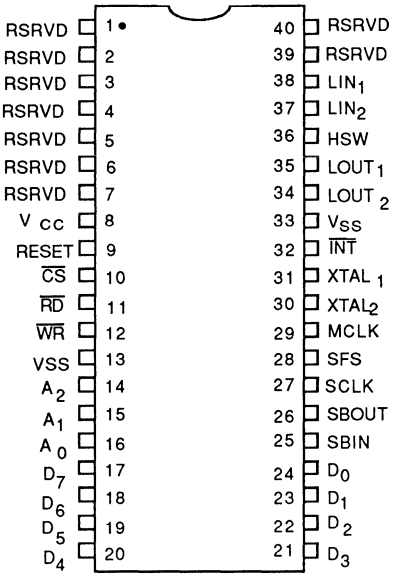
The Am79C32A can be used in digital data terminal, and terminal adaptor equipment.

A serial port gives the user access to the B-channels of the Am79C32A multiplexer. This serial port may be used by data terminals and provides, with additional circuitry, access to the CCITT "R" reference point.

The Am79C32A is controlled via an interrupt driven microprocessor bus interface by an external microprocessor. Using this interface, the microprocessor processes the D-channel information and programs the Am79C32A accordingly. This includes programming a multiplexer within the Am79C32A to route the B-channels as specified by the D-channel control information. The microprocessor can interrogate and program the Am79C32A via its mode, status, and error registers.

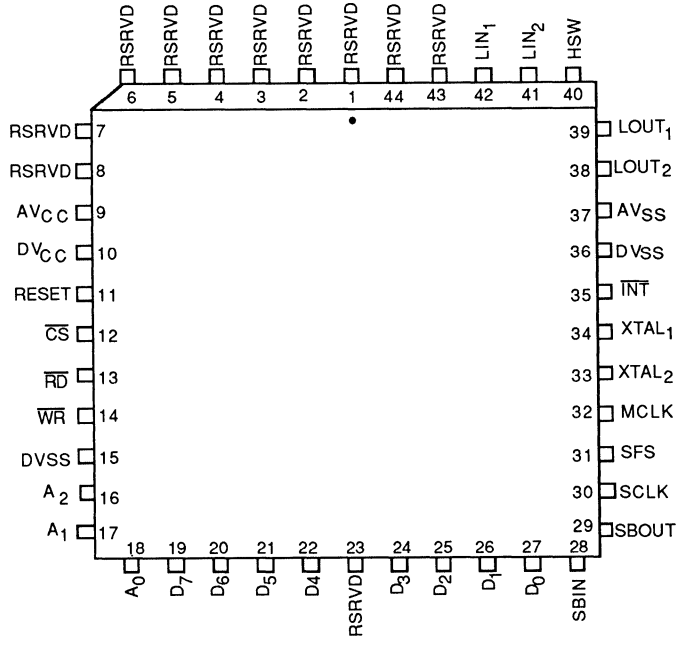
CONNECTION DIAGRAMS
Top View

40-Pin PDIP



09456-49A

44-Pin PLCC



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
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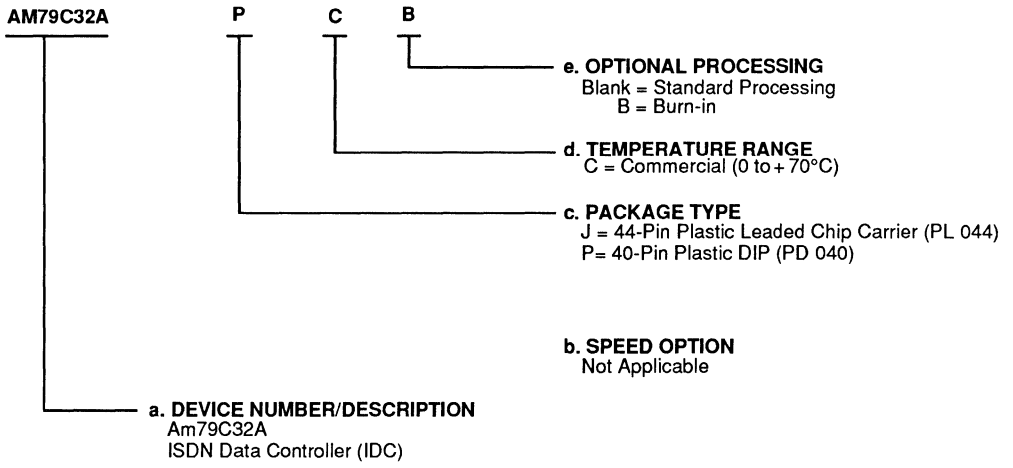
e. Optional Processing



Valid Combinations	
AM79C32A	PC,JC,PCB,JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Am79C401

Integrated Data Protocol Controller™ (IDPC™)

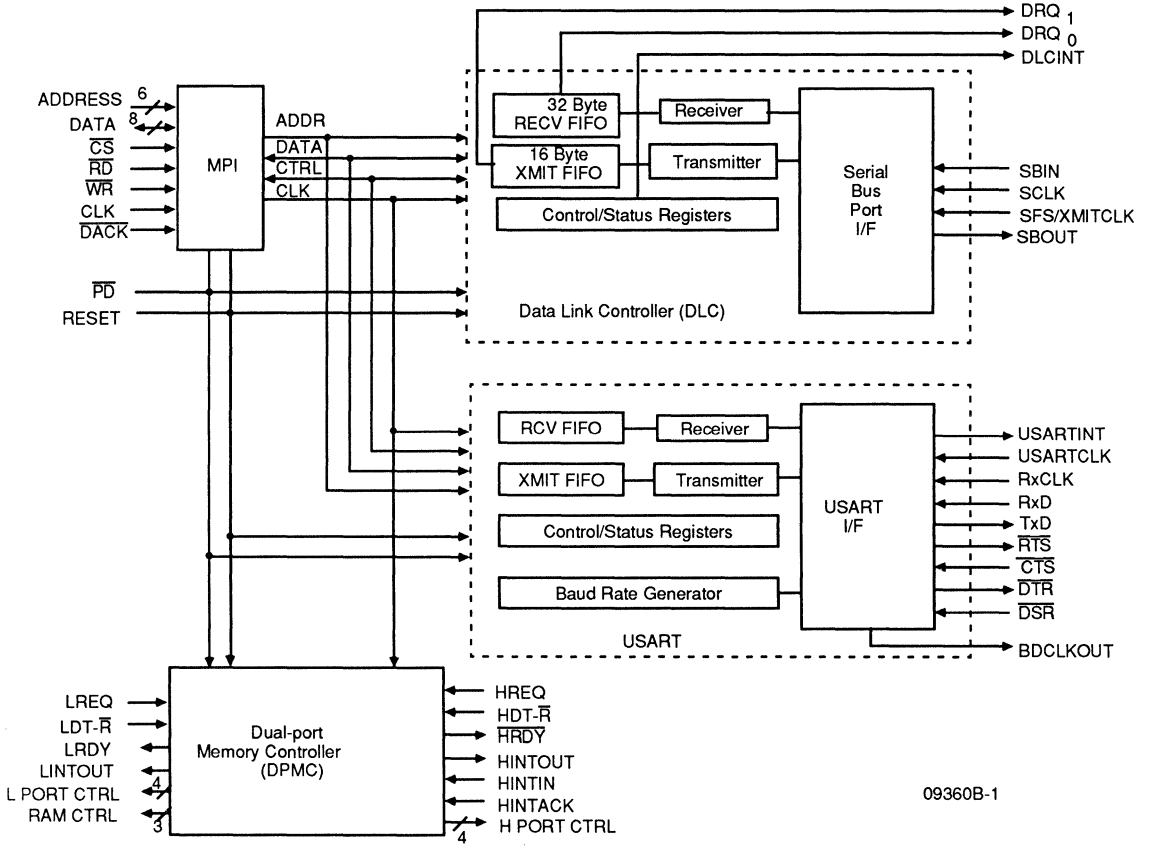
Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

Data Link Controller

- Full-featured bit-oriented communication controller supporting HDLC, SDLC, LAPB, LAPD, and DMI
- Data transfer rate: 2.048 Mbps
- 32-byte receive FIFO and 16-byte transmit FIFO with programmable thresholds and DMA handshakes
- Multiple (four plus broadcast) address recognition modes
- Multiplexed serial interface with up to thirty-one 8-bit channels or non-multiplexed serial interface
- Local and Remote Loopback Modes
- Transparent (Protocol-Free) Mode
- 56 kbps Mode

BLOCK DIAGRAM



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DISTINCTIVE CHARACTERISTICS (continued)

USART

- Superset of Industry-Standard 8250 UART features
- Four-byte transmit/receive FIFOs
- Special character recognition (up to 128 programmable)
- Synchronous mode provides a transparent serial data path
- Local Loopback mode

Dual-Port Memory Controller

- Memory bus arbitrator provides dual-port access to standard low-cost static RAM
- Programmable inter-processor interrupts support RAM-based inter-processor mailboxes

Microprocessor Interface

- 8-bit non-multiplexed data bus
- Operates with 12.5 MHz 80188 processor with zero wait states

General Features

- Compatible with Am79C30A DSC and Am79C32A IDC
- CMOS technology, single +5V supply
- Power-down mode
- 68-pin PLCC package

GENERAL DESCRIPTION

The Am79C401 Integrated Data Protocol Controller (IDPC) and companion software product, the Am79LLD401 IDPC Low-Level Driver (LLD), provide many of the essential building blocks for construction of a variety of communications systems. When combined with ROM, RAM, a microprocessor, and the appropriate physical layer transceiver, a complete ISDN, X.25, SNA, or similar system can be constructed. The IDPC is design-compatible with existing AMD communication components (Am79C30A Digital Subscriber Controller (DSC) and Am79C32A ISDN Data Controller (IDC)) and off-the-shelf microprocessors such as the 80188.

The IDPC contains hardware and software support features for use in a single-processor environment (such as a terminal adaptor to an ISDN network) or a multiprocessor application (such as a communication interface for a PC or integrated voice/data work station application). For multi-processor applications, the IDPC controls access to an external "shared" RAM which serves as a data buffer and communications area ("mailbox" concept). The IDPC arbitrates simultaneous requests for RAM access and supports an inter-processor interrupt scheme.

A companion software product, the Am79LLD401 IDPC LLD, provides isolation of the various hardware functions from the higher levels of packet protocol software. The LLD can be used with any bit-oriented protocol, including AmLINK™, which is AMD's LAPD /LAPB implementation. Additionally, AMD's AmLink3™ package offers a complete implementation of the X.25 Packet Layer (Layer 3) protocol.

For ISDN D-channel applications, a similar function is provided by the Am79C30A DSC and Am79LLD30A LLD software.

The interfaces presented by the Am79LLD30A DSC LLD and the Am79LLD401 IDPC LLD use the same primitives so that both the D-channel and the B-channel can use the same layer-2 software. Both LLDs provide a hardware-independent interface to upper-layer protocols such as AmLINK LAPD.

Functionally, the IDPC consists of four sections: Data Link Controller (DLC), Universal Synchronous/Asynchronous Receiver/Transmitter (USART), Dual-Port Memory Controller (DPMC), and Microprocessor Interface (MPI).

Data Link Controller (DLC)

The DLC shown in the Block Diagram is a high-speed, bit-oriented protocol processor that supports either multiplexed or non-multiplexed data rates up to 2.048 Mbps.

The DLC provides full-duplex (simultaneous transmit and receive) data transfer between the chip's Serial Bus Port (SBP) and internal parallel bus. Through the use of a 32-byte receive FIFO, a 16-byte transmit FIFO, and two external DMA channels, the DLC provides efficient movement of data to and from external memory and the SBP (network interface).

The DLC supports data transfers via DMA, interrupts, or polled I/O. The use of the FIFO buffers minimizes interrupt latency and frequency of interrupts.

The DLC has several programmable modes of operation which include:

- Non-multiplexed mode
- Multiplexed mode
- Local/Remote Test modes
- Transparent (Protocol-Free) Mode
- 56 kbps Mode

Non-multiplexed Mode

In non-multiplexed mode, the DLC functions as a conventional serial communications controller capable of supporting full-duplex data transfers at rates up to 2.048 Mbps. This mode is useful in non-ISDN applications such as SNA networking.

Multiplexed Mode

In multiplexed mode, the DLC's SBP interfaces cleanly with the SBP on the Am79C30A DSC or the Am79C32A IDC, and provides access to thirty-one 64 kbps time slots.

Local/Remote Loopback Test Modes

The IDPC can be placed in the local or remote loopback mode under software control. In local loopback, the transmitter output is tied back to the receiver input. In remote loopback, the receiver input from the network is transmitted back to the network for system test purposes.

Transparent Mode

In Transparent Mode, the DLC receives and transmits data without performing any HDLC protocol processing, creating a clear path between the SBP and the transmit and receive FIFOs. This mode can be used in either multiplexed or non-multiplexed modes.

56 kbps Mode

In 56 kbps Mode, the DLC transmits and receives data at a 56 kbps data rate. In this mode, the DLC sends data within an 8-bit time slot period, and always pulls the TxD pin HIGH during the transmit time period of the eighth bit. Similarly, during data reception, the DLC shifts in 7 bits during the programmed time slot, but always waits until eight bits have been accumulated before transferring the data to the receive FIFO.

Universal Synchronous/Asynchronous Receiver/ Transmitter (USART)

The IDPC contains a built-in USART for exchanging data between RS232 type terminals and the ISDN network in applications where there is no host processor. The USART provides a superset of 8250 UART features and supports both synchronous and asynchronous serial communications. The USART is capable of full-duplex operation at speeds up to 64 kbps using an internal programmable baud rate generator.

The USART supports the following functions:

- Programmable synchronous/asynchronous modes
- Software reset
- Line break recognition and generation
- Special character recognition
- Selectable stop bits (1-, 1.5-, or 2-stop bits)
- Full modem control handshake lines ($\overline{RTS}$, $\overline{CTS}$, $\overline{DSR}$, and $\overline{DTR}$)
- Local loopback and "stick parity" test features

The USART receiver can detect up to 128 user-identified special characters. As each character is received, it is tested. If it is identified as a special character, a maskable interrupt is generated.

The USART includes an internal Baud Rate Generator that receives an input from the USARTCLK pin and provides a clock for the transmitter and receiver sections (and to the external pin BDCLKOUT). The Baud Rate Generator's data rate is programmed by loading two "divisor latches" (under software control).

Dual-Port Memory Controller (DPMC)

The DPMC provides RAM access control and an interprocessor interrupt mechanism that permits two processors to share common RAM memory without the expense of dual-port RAM. These features are necessary in developing network interface applications for PCs and Integrated Voice/Data Workstations (IVDWs).

In a typical multi-processor application, a local processor (such as the 80188) exchanges data with the host processor in the PC or IVDW using shared memory. The DPMC performs RAM access arbitration between the local and host processors, allowing low-cost static RAM to appear as a dual-port memory to each processor.

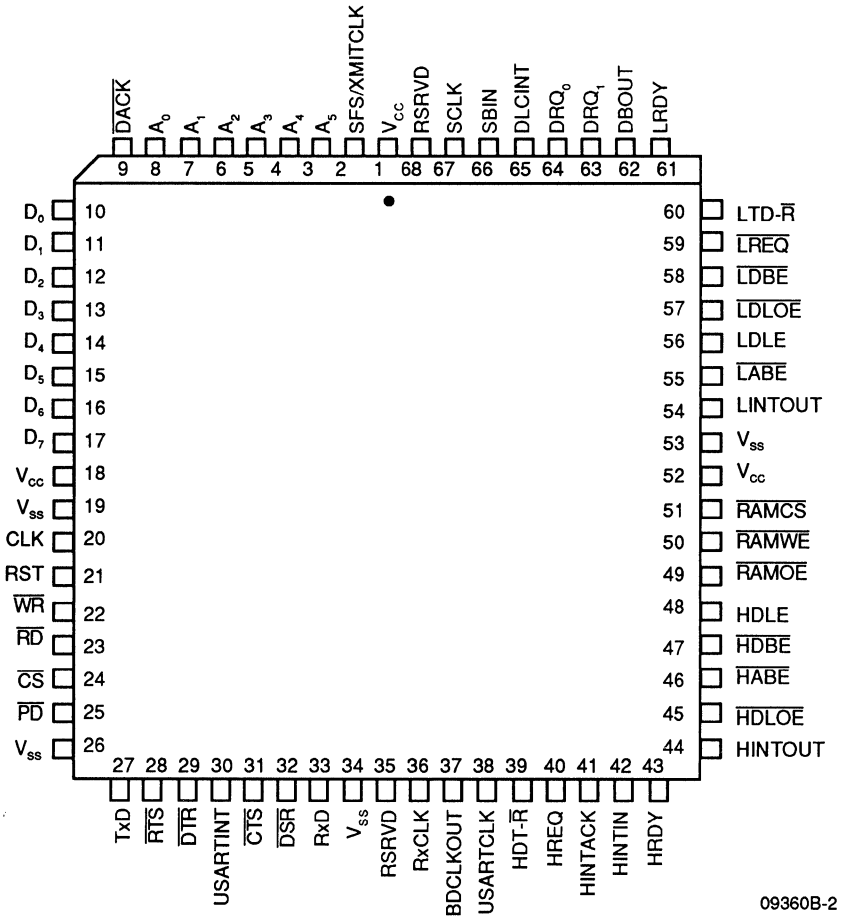
The local processor can access any device on the IDPC external bus. The host processor can only access the RAM on the IDPC external bus. Any contention between the local processor and the host processor is arbitrated by the DPMC on the IDPC. Both processors communicate via memory-resident data buffers and mailboxes. An inter-processor interrupt scheme notifies the other processor when one of the processors has written data to a buffer or a command to a mailbox.

Microprocessor Interface (MPI)

The MPI consists of an 8-bit non-multiplexed data bus that allows the IDPC to function with a 12.5 MHz 80188 processor (or other similar microprocessor) with zero wait-states.

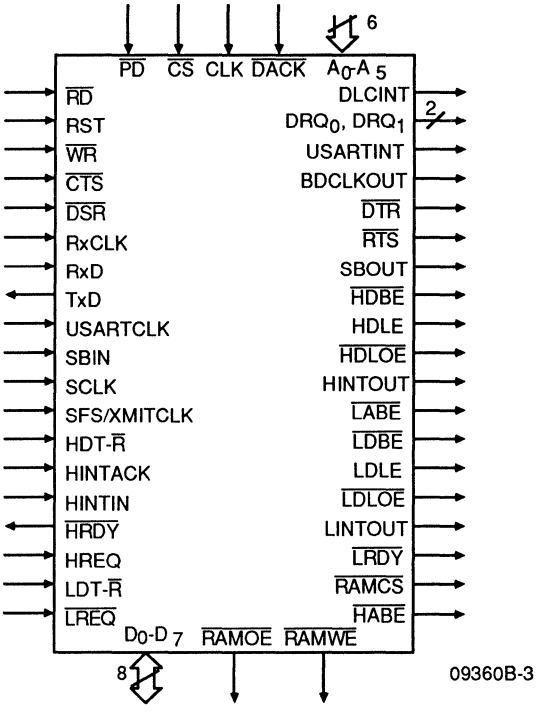
CONNECTION DIAGRAM
Top View

68-Pin PLCC



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

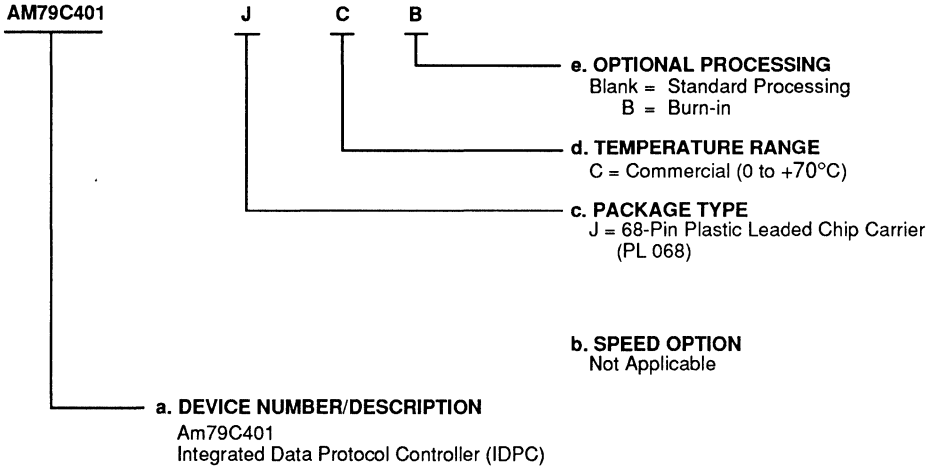


ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM79C401	JC, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Am2085

ISDN Subscriber Access Controller (ISAC-S™)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- S-Bus transceiver according to CCITT I.430
- Recovery of clock and frame
- Frame alignment for trunk line termination
- Access to Echo bit
- Implementation of activation/deactivation procedure
- Support of LAPD protocol
- FIFO buffer (2 • 64 byte) for efficient transfer of D-channel packets
- Serial interfaces for various types of B-channel sources/destinations (SLD, SSI)
- Switching functions for B-channels
- Watchdog timer
- Switching of testloops
- 8-bit microprocessor interface
- Advanced CMOS technology
- Low power consumption

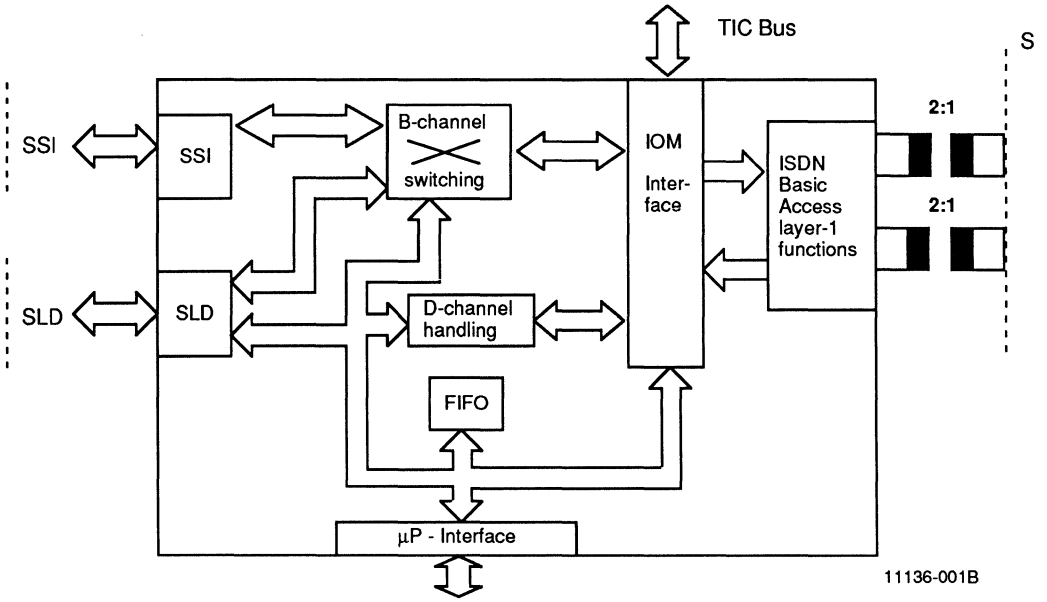
GENERAL DESCRIPTION

The Am2085 ISAC-S is a transceiver circuit able to interface voice/data communication equipment to the 4-wire CCITT S-Bus. It supports the LAPD protocol in hardware. For an efficient transfer of D-channel packets, FIFO structures are used.

The device is mounted in a 40-pin CMOS package.

The power consumption of the device in the active state is 80 mW (8 mW in Power Down State).

BLOCK DIAGRAM



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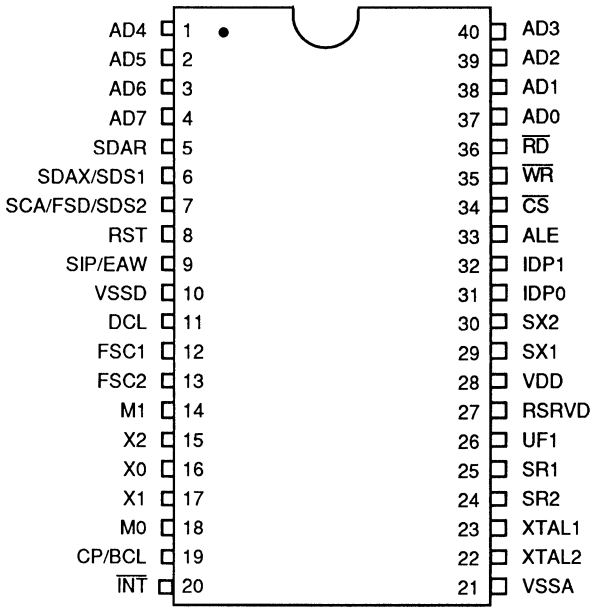
CONNECTION DIAGRAMS
Top View

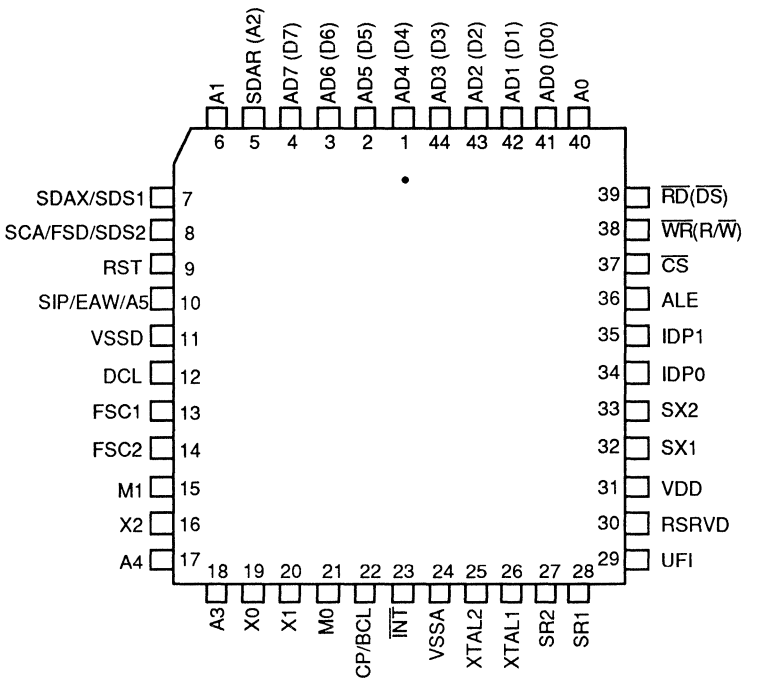
40-Pin DIP



Note: Pin 1 is marked for orientation.

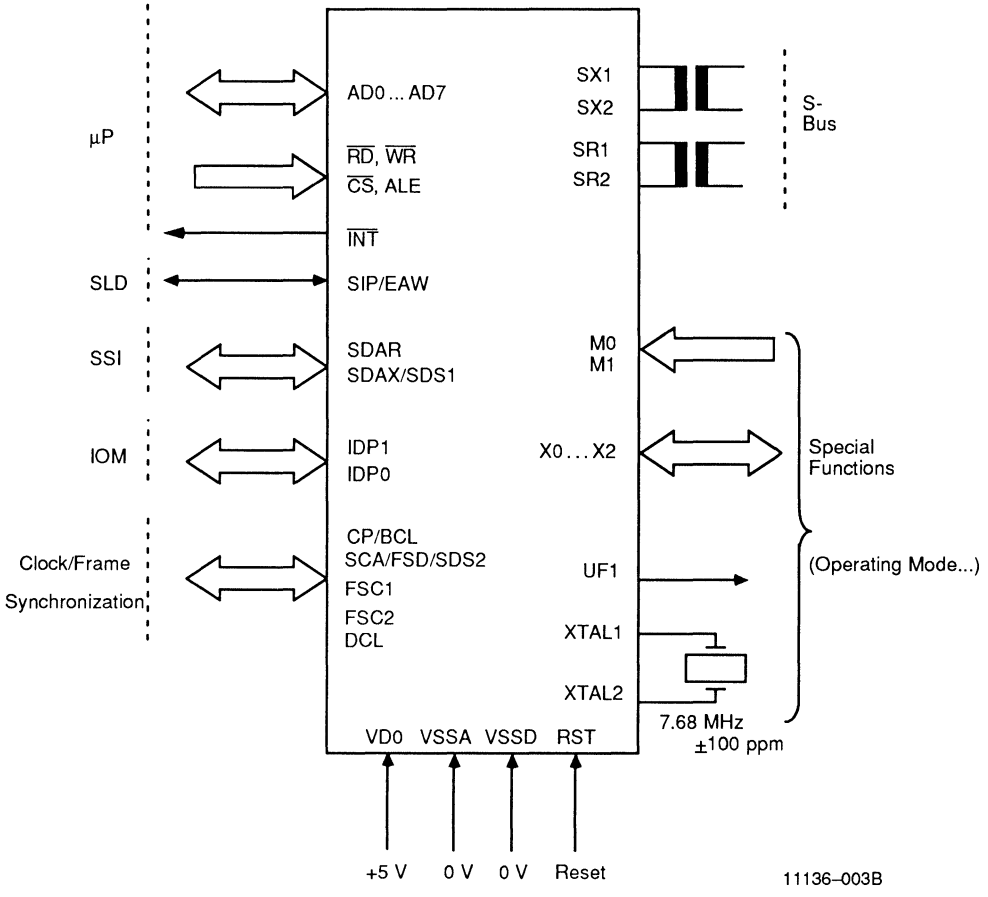
11136–002B

44-Pin PLCC



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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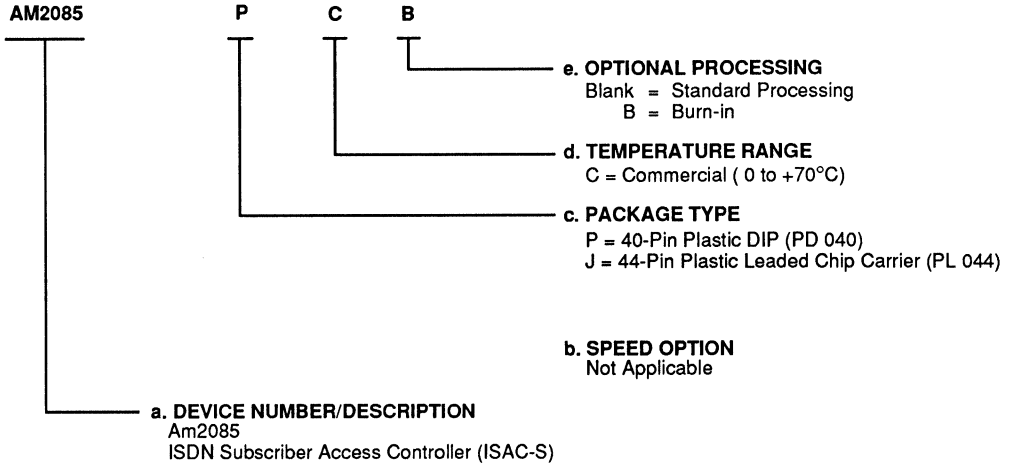


Valid Combinations	
AM2085	PCB, JCB, PC, JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Am2110
ISDN Terminal Adapter Circuit (ITAC)

Advanced Micro Devices

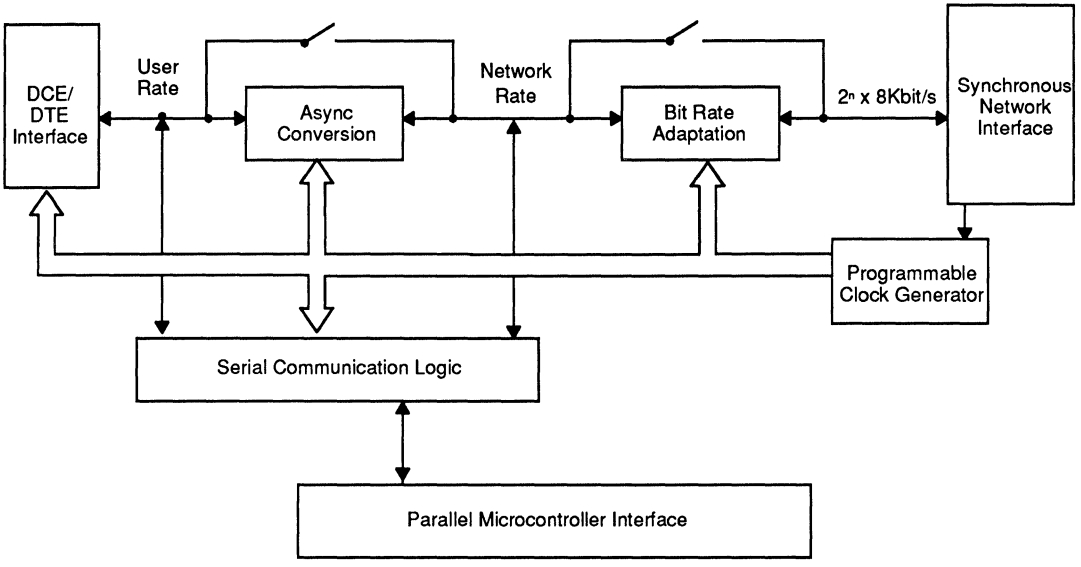
DISTINCTIVE CHARACTERISTICS

- Universal adaptor for ISDN R reference point
- Support of async and sync interfaces: X.21, X.21 bis, V.24, RS232C
- Programmable speeds from 300 bps to 64 kbps
- Bit rate adaptation according to X.30, V.110, ECMA.102, V.120 and DMI
- Programmable time slots and subchannels for intermediate rates
- Automatic calling/answering with on-chip controllers
- In-band parameter exchange support
- Parallel 8-bit microcontroller interface
- DMA support
- Single +5 V supply, low power CMOS technology

GENERAL DESCRIPTION

The ISDN Terminal Adapter Circuit (ITAC) is a monolithic, full custom circuit for interfacing standard terminals and PCs to a circuit switched data network or an ISDN. It may be programmed to perform bit rate adaptation for 64 kbps clear channels according to the newest rate adaptation protocols. The on-chip communication controllers handle signalling between data equipment and the network, effectively replacing the "smart modem" of the PSTN. The features of the ITAC make it suitable for use in advanced networking applications that require flow control, in-band parameter exchange and interworking.

BLOCK DIAGRAM



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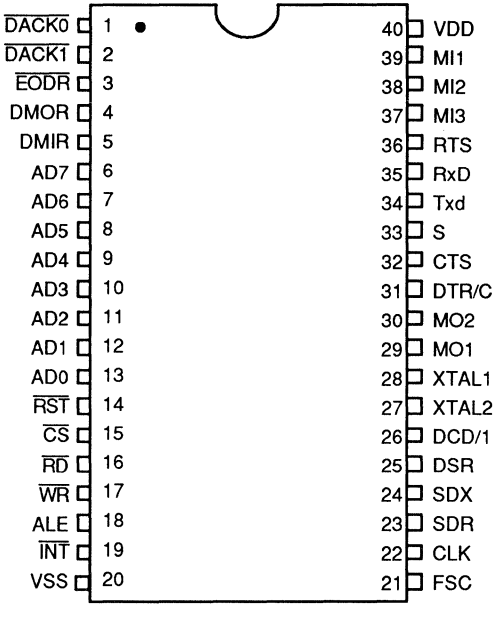
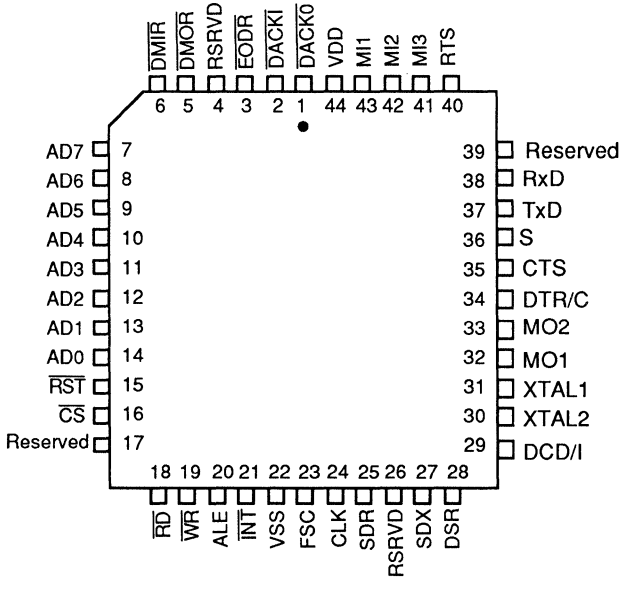
CONNECTION DIAGRAMS
Top View

40-Pin DIP

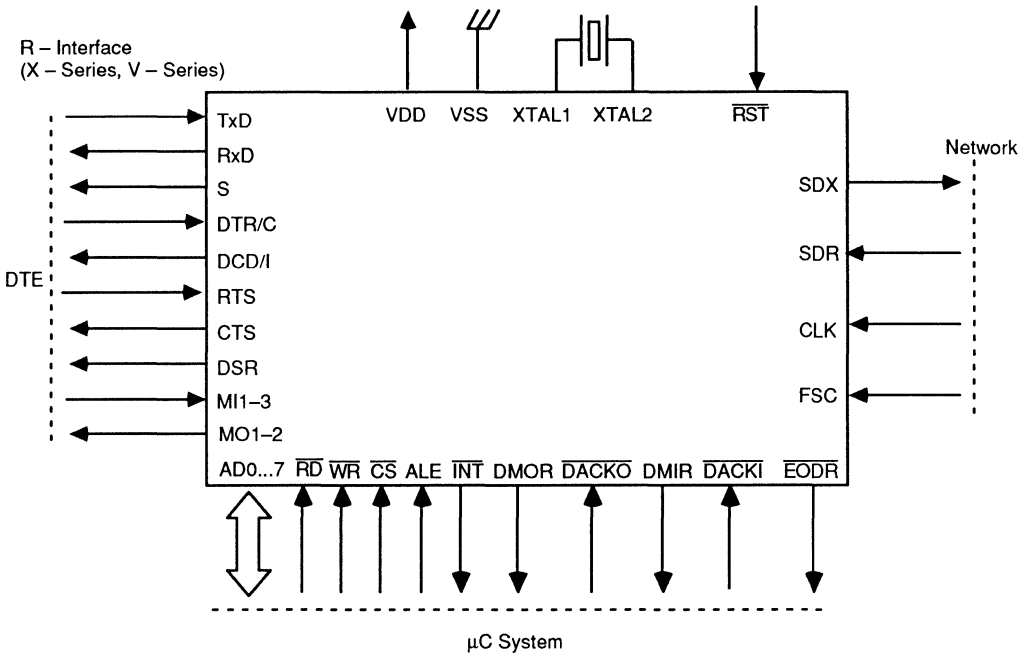


44-Pin PLCC



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



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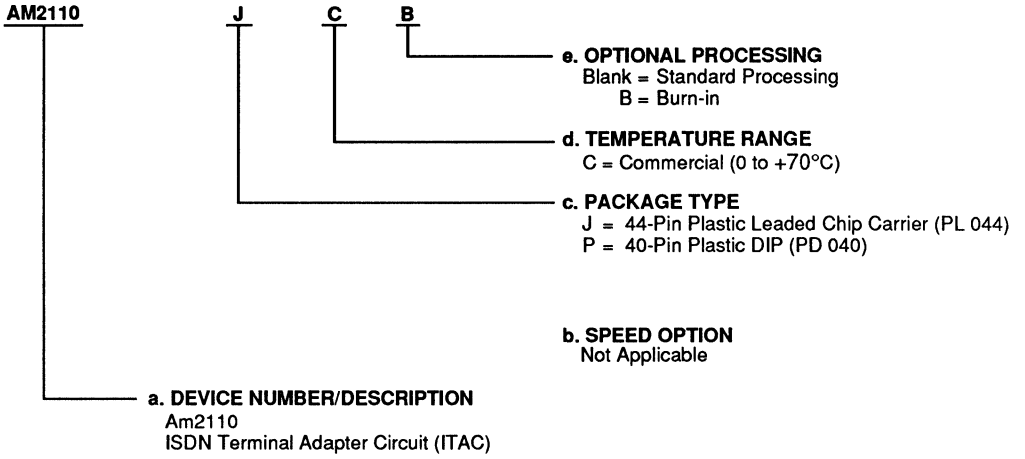


Valid Combinations	
AM2110	JC, JCB, PC, PCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Am2160

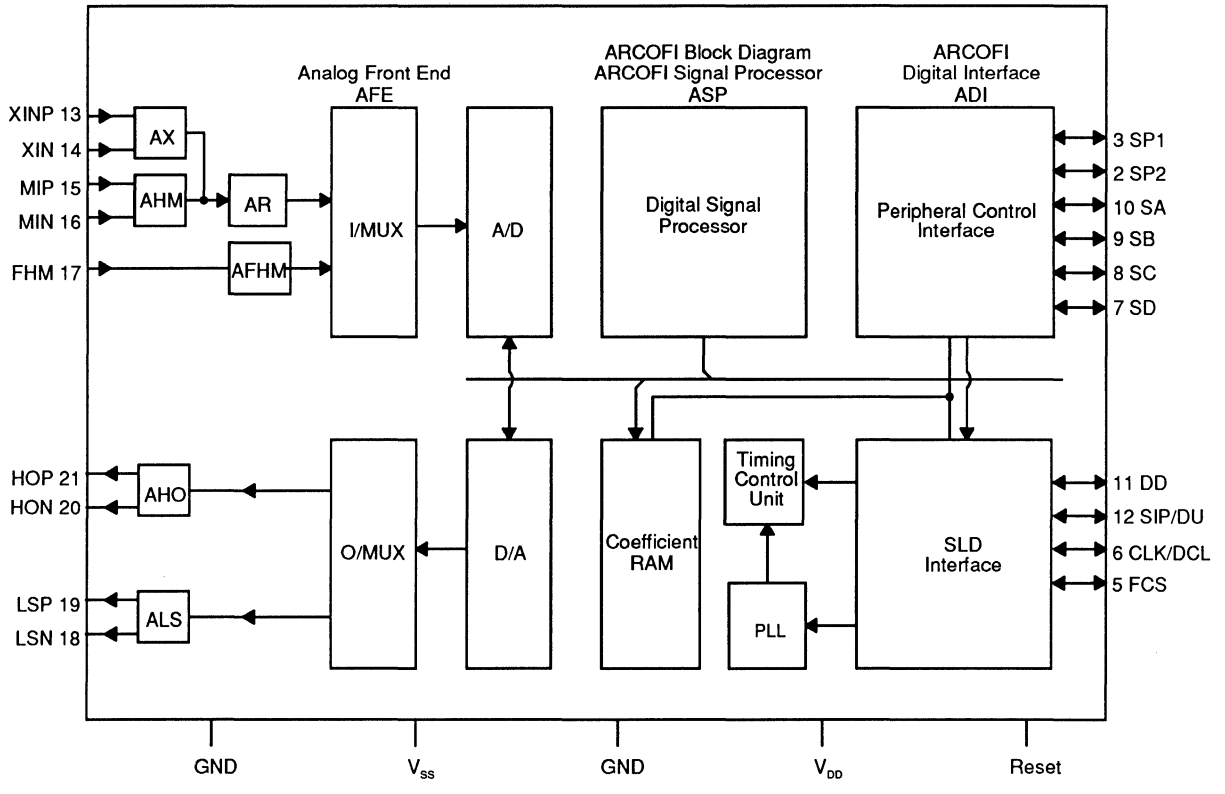
Audio Ringing Codec Filter (ARCOFI)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Applications in digital terminal equipment including a voice path
- Low power CMOS technology
- Test and maintenance loopbacks in the analog front end and the digital processor
- SLD or IOM™ Rev. 2 serial interface bus
- Flexible Peripheral Control Interface (PCI)
- CODEC filter
- DTMF, tone and ringing generators
- Separate output for a piezo ringer
- Dual analog inputs for handset and "handsfree" microphones plus an auxiliary differential analog input
- Two sets of differential outputs for a handset earpiece and loudspeaker
- Power dissipation:
  – active 150 mW
  – standby 10 mW
- Temperature range: –25 to +70°C
- Packages: 24-pin DIP
  28-pin PLCC

BLOCK DIAGRAM



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Issue Date: March 1989

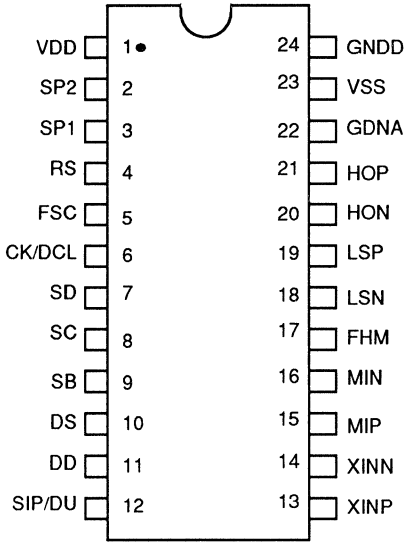
GENERAL DESCRIPTION

The Am2160 Audio Ringing Codec Filter (ARCOFI) provides the subscriber with an optimized audio, ringing, codec filter processor solution for a digital telephone. The ARCOFI fulfills all necessary requirements for the completion of a low cost digital telephone. Full featured applications including handsfree telephone are included by the addition of a voice switched speakerphone circuit. The ARCOFI performs all coding, decoding, and filtering functions according to CCITT and AT&T norms.

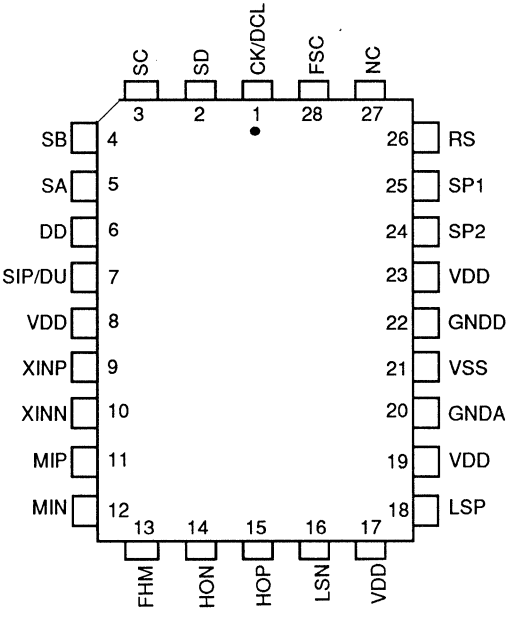
The ARCOFI integrates a DTMF generator in the transmit direction and a tone generator plus a ringing generator in the receive path. The interfacing to a handset mouth and earpiece is facilitated by a flexible analog front end. A loudspeaker output has also been integrated on chip as well as a secondary input for a handsfree microphone. The microphone analog gains is user programmable under microprocessor control.

CONNECTION DIAGRAMS
Top View

24-Pin DIP



28-Pin PLCC



Note: Pin 1 is marked for orientation.

ORDERING INFORMATION
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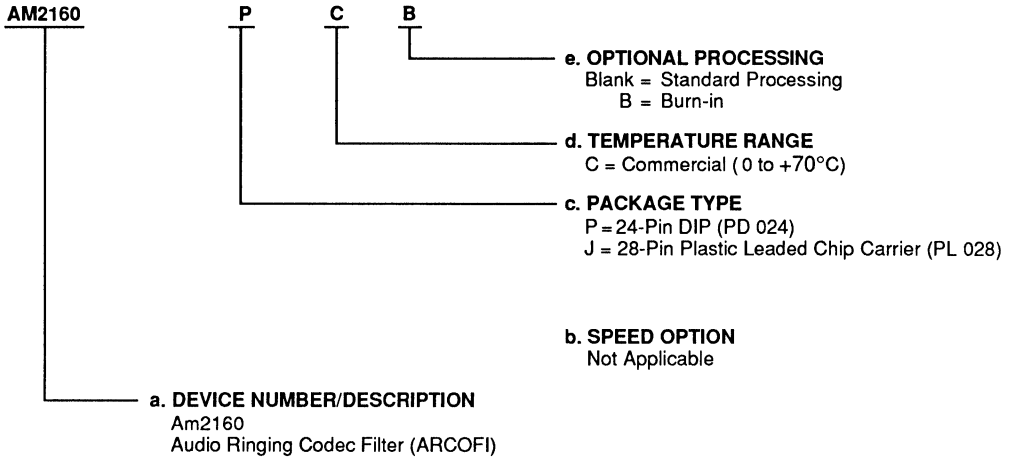


Valid Combinations	
AM2160	PC, PCB, JC, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Am82525

High-Level Serial Communications Controller Extended (HSCX)

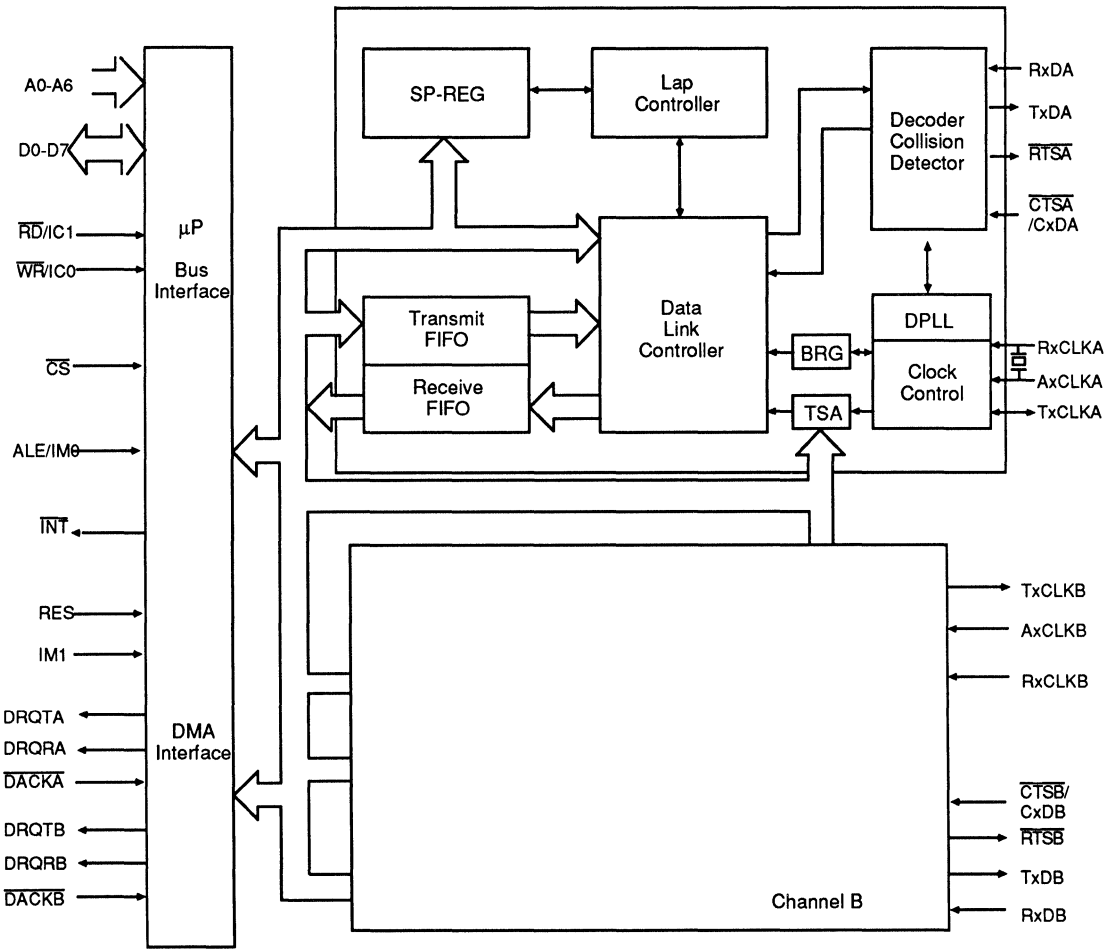
Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

Serial Interface

- Two independent full-duplex HDLC channels
- On-chip clock generation or external clock source
- On-chip DPLL for clock recovery for each channel
- On-chip baud rate generators for each channel
- Independent time slot assignment for each channel with programmable time slot length (1–256 bit)
- Different modes of data encoding (NRZI, NRZ)
- Modem control lines ($\overline{RTS}$, $\overline{CTS}$, $\overline{CD}$)
- Support of bus configuration by collision resolution

BLOCK DIAGRAM



11139–001B

Publication # 11139 Rev. Amendment /0
Issue Date: March 1989

DISTINCTIVE CHARACTERISTICS (continued)

- Programmable bit inversion
- Transparent receive/transmit of data bytes without HDLC framing
- Cyclic transmission mode (1 to 32 bytes possible)
- Data rate up to 4 Mbps

Protocol Support

- Auto mode
- Non auto mode
- Transparent mode
- Handling of bit-oriented functions in all modes
- LAPB/LAPD/SDLC/HDLC procedural support in auto mode (I- and S-frame handling)
- Modulo 8 or modulo 128 operation
- Programmable timeout and retry conditions
- Programmable maximum packet size checking

Microprocessor Interface

- 64-byte FIFOs per channel and direction
- Storage capacity of up to 17 short frames in receive direction
- Efficient transfer of data blocks from/to system memory by DMA or interrupt request
- 8-bit demultiplexed or multiplexed bus interface
- Intel or Motorola type microprocessor interface

General

- Compatible to Am82520 (HSCC)
- Advanced CMOS technology
- Low power consumption
  - active 25 mW at 4 MHz
  - standby 4 mW

GENERAL DESCRIPTION

The Am82525 HSCX is a High-Level Serial Communications Controller with extended features and functionality. The HSCX is compatible to the Am82520 HSCC.

The HSCX has been designed to implement high-speed communication links using HDLC protocols and to reduce the hardware and software overhead needed for serial synchronous communications.

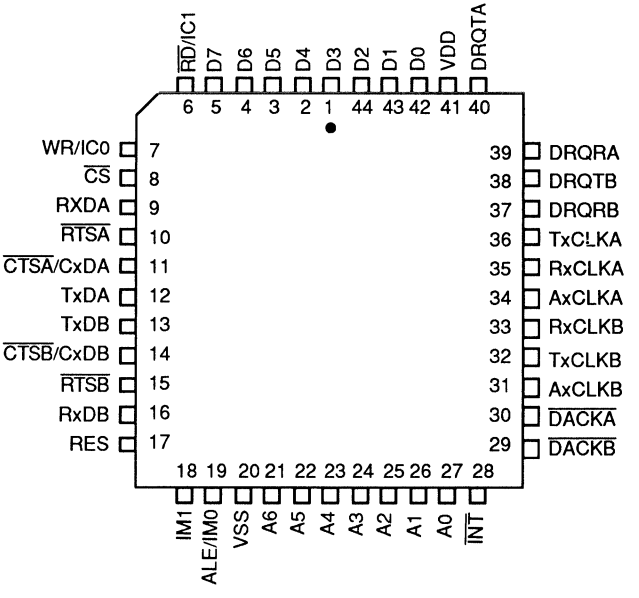
Due to its 8-bit adaptive bus interface it fits into every AMD/Siemens/Intel or Motorola 8- or 16-bit microcontroller or microprocessor system. The data throughput from/to system memory is optimized for transferring blocks of data (up to 32 bytes) by means of DMA or interrupt request. Together with the storing capacity of up to 64 bytes in on-chip FIFOs, the serial interfaces are effectively decoupled from the system bus which drastically reduces the dynamic load and reaction time of the CPU.

The HSCX directly supports the X.25 LAPB, the ISDN LAPD, and SDLC (Normal Response Mode) protocols and is capable of handling a large set of OSI layer 2 protocol functions independently from the host processor. Furthermore, the HSCX opens a wide area for applications which use time division multiplex methods; e.g, time-slot oriented PCM systems, systems designed for packet switching, and ISDN applications, by its programmable telecom-specific features.

The HSCX is available in a 44-pin PLCC package.

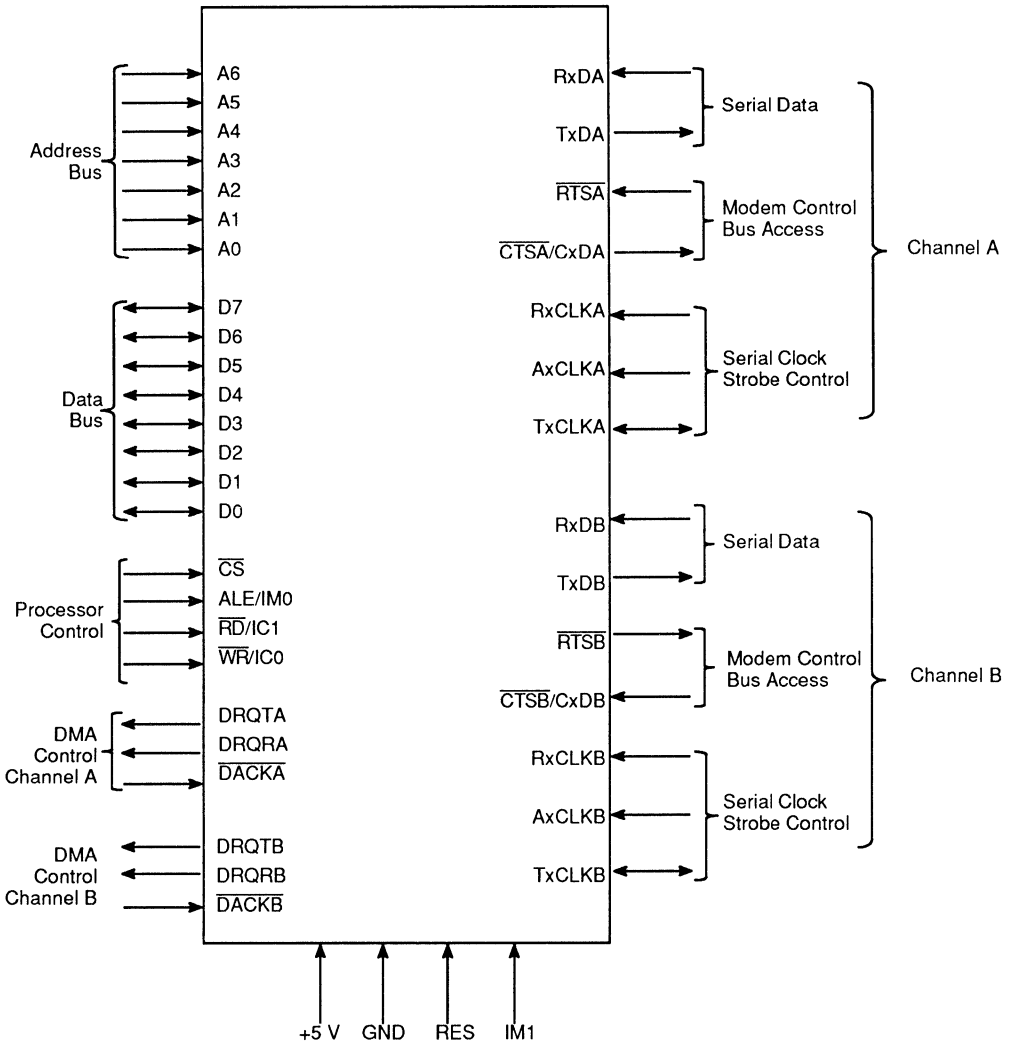
CONNECTION DIAGRAM
Top View

44-Pin PLCC



Note: Pin is marked for orientation.

LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

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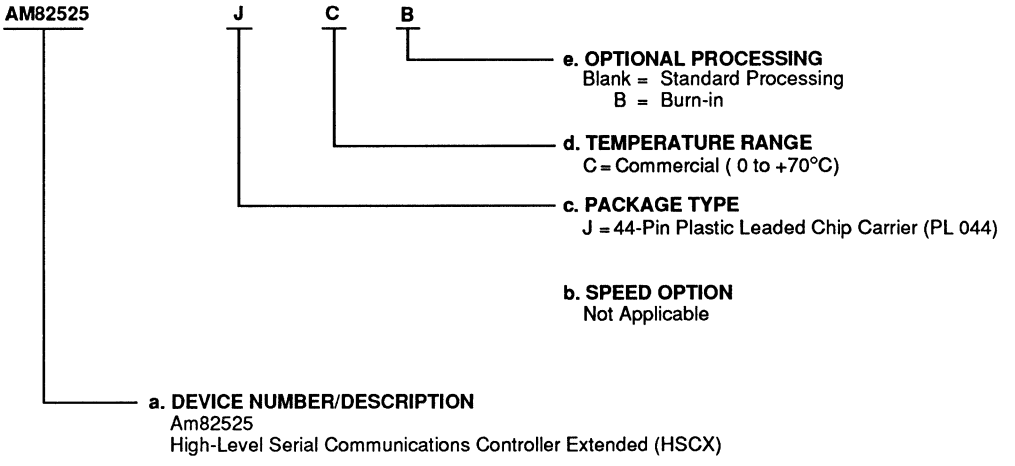


Valid Combinations	
AM82525	JC, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

INTEGRATED SERVICES DIGITAL NETWORK (ISDN)

Switch Products

Am7938

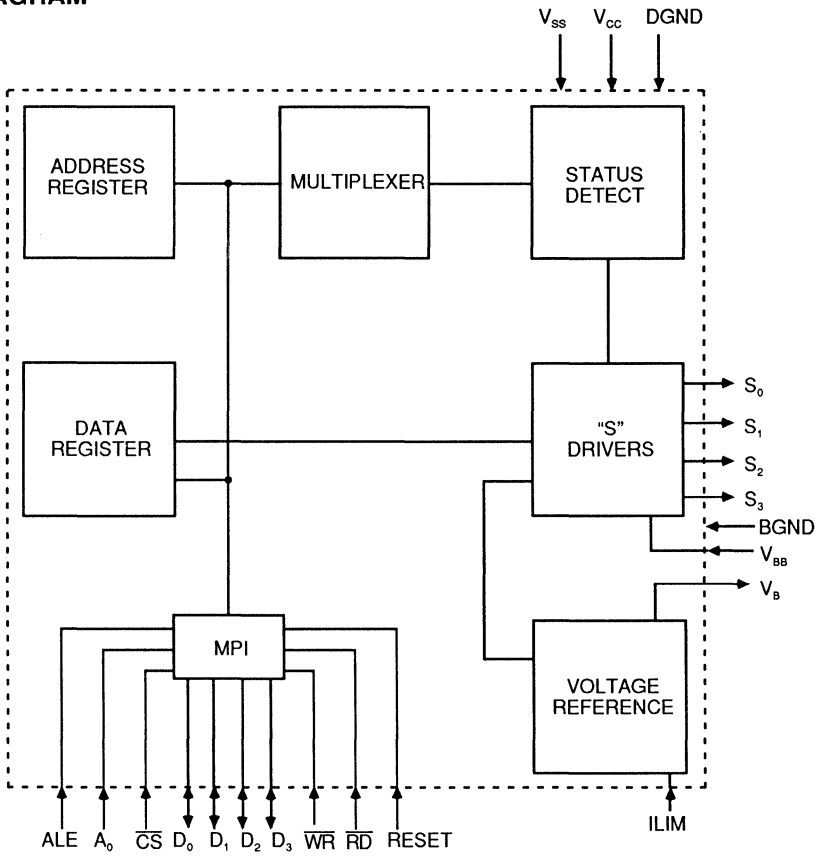
Quad Exchange Power Controller (QEPC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Supplies power for up to four digital telephone lines
- Conforms to the CCITT recommendations for power feed at the "S"or "T" reference point
- Applications for intelligent NTs and PABX/Central Office line cards
- Supports point-to-point and point-to-multipoint configurations
- Built-in battery control circuit for –40 V operation
- Each of the four lines is individually controlled
- Status detectors for each line driver; open-loop, current-overload, low output voltage, thermal overload
- Programmable current limiting
- Automatic shutdown of overloaded lines
- Automatic thermal shutdown
- Microprocessor-compatible interface
- High-voltage bipolar technology allows battery voltages up to 65 V
- Output current up to 150 mA per driver

BLOCK DIAGRAM



09153–001A

Publication # 09153 Rev. Amendment /0
Issue Date: April 1989

GENERAL DESCRIPTION

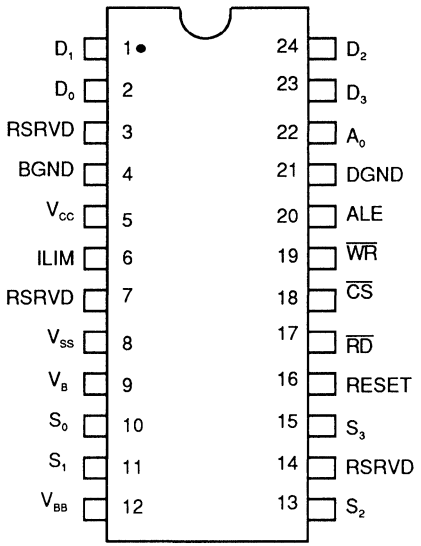
The Am7938 Quad Exchange Power Controller (QEPC) provides a power source for up to four line interfaces. The power source to the Am7938 is a local battery or a centralized regulated power supply. The Am7938 can reside in intelligent NTs or PABX/Central Office line cards. It can operate in point-to-point and point-to-multipoint configurations. Via the Am7938's microprocessor interface, each powered line is individually controlled and monitored. The power to each line can be switched off independently. Hence, overloads and faults are easy to detect and localize even in a large system. The status conditions detected by the Am7938 on each line which may be read by the microprocessor are: low output voltage, open-loop, current overload, thermal overload, and normal line conditions.

Current limit and thermal shutdown circuits protect the Am7938 against overload conditions. However, certain applications may require additional external protection circuitry.

The Am7938 has been developed specifically for CCITT-compatible ISDN configurations. It should be recognized, however, that due to its versatile design, the Am7938 can be used in numerous other applications.

CONNECTION DIAGRAM
Top View

24-Pin DIP

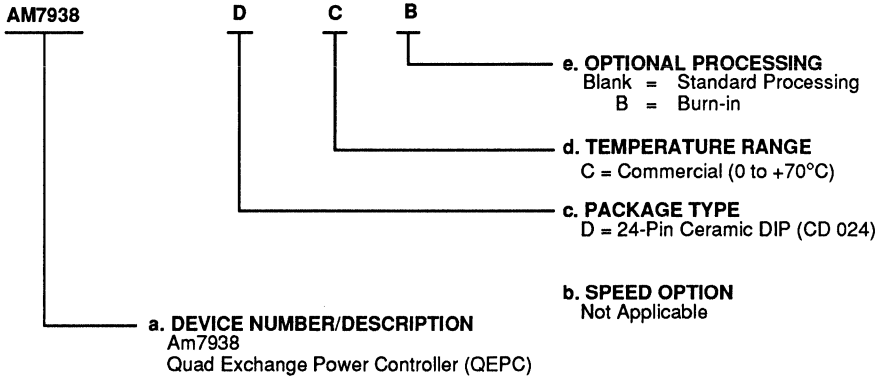


Note: 1. Pin 1 is marked for orientation.
2. Reserved (RSRVD) pins should not be connected externally to any signal or supply.

ORDERING INFORMATION

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7938	DC, DCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Am2055

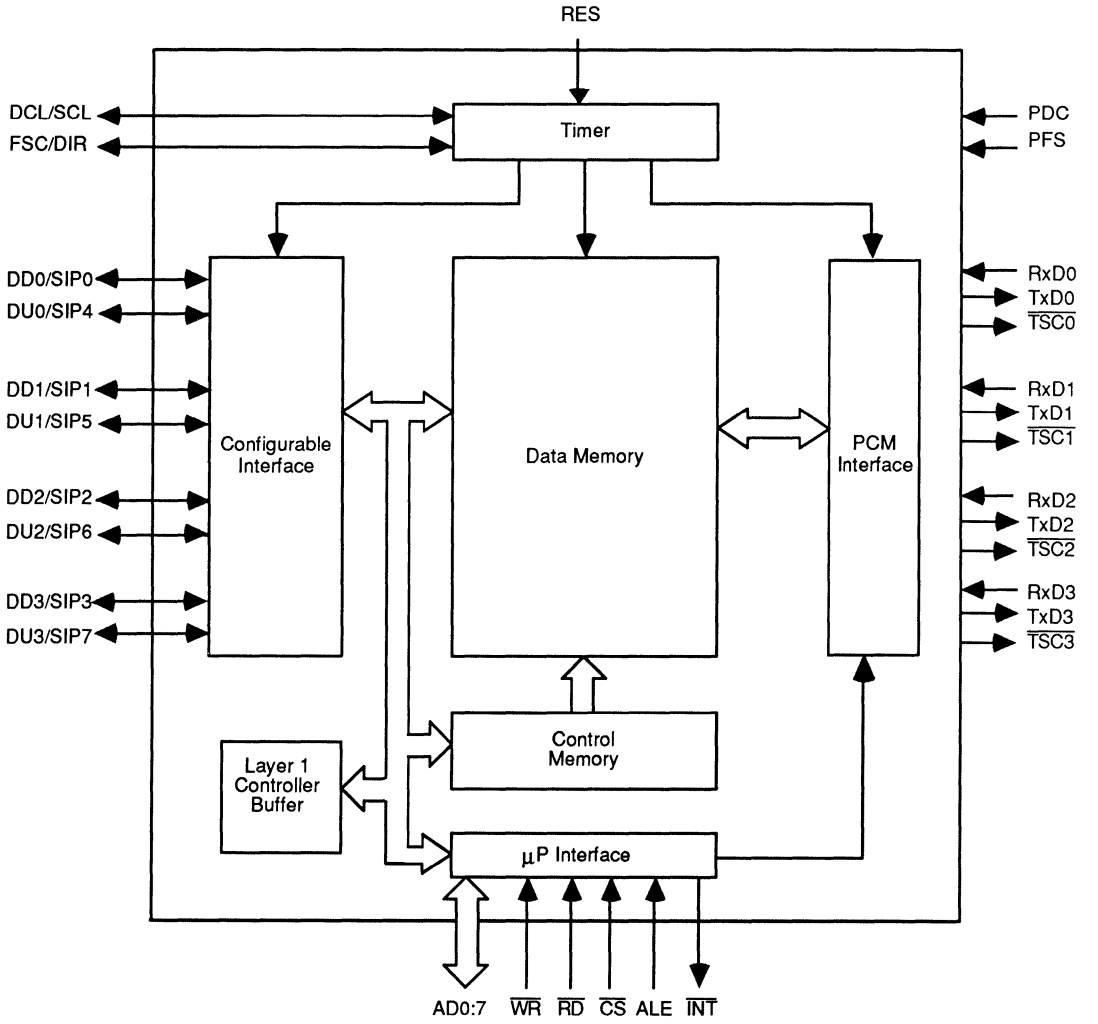
Extended PCM Interface Controller (EPIC™)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Board Controller for up to 32 ISDN or 64 voice subscribers
- Nonblocking switch for 128 channels (16, 32, or 64 kbps bandwidth or a mixture thereof)
- Two consecutive 64 kbps channels can be handled as a single quasi 128 kbps channel.
- Timeslot assignment freely programmable for all connected subscribers
- Two serial interfaces (PCM and configurable)
- Programmable for a wide range of data rates (8 to 8192 kbps)

BLOCK DIAGRAM



Publication # 11149 Rev. Amendment /0
Issue Date: March 1989

DISTINCTIVE CHARACTERISTICS (continued)

- Data rates of PCM and configurable interfaces independent from each other (data rate adaptation)
- Single and double rate clock selectable
- PCM interface
  Tri-state control signals for external drivers
  Programmable clock shift
- Configurable interface
  Configurable for IOM™ compatible devices (4 duplex ports)
  Configurable for SLD compatible devices (8 bidirectional I/O ports)
  Configurable for PCM applications
- Standard µP interface with multiplexed address /data bus or separate address and data buses (PLCC 44)
- Handling of layer 1 functions
  Change detection logic for C/I (IOM configuration) or feature control (SLD configuration) channels
  Buffered monitor (IOM configuration) or signaling channel (SLD configuration)
- Comfortable µP access to two selected channels
- 40-pin Dual-In-Line or 44-pin PLCC package
- Advanced low power CMOS technology

GENERAL DESCRIPTION

The Am2055 Extended PCM Interface Controller (EPIC) is a monolithic switching device for the path control of up to 128 channels of 16, 32 or 64 kbps bandwidth. Two consecutive 64 kbps channels may also be handled as a quasi-single 128 kbps channel. For these channels the EPIC performs non-blocking space time switching between two serial interfaces, the system and the configurable interface.

Both interfaces can be programmed to operate at different data rates between 8 and 8192 kbps. The system interface consists of up to four duplex ports with a tristate indication signal for each output line. The configurable interface can be selected to incorporate either four duplex or eight bidirectional I/O ports (SLD).

The EPIC can therefore be programmed to communicate either with SLD or with IOM (ISDN oriented modular) compatible devices. In both cases, the device handles the layer 1 functions buffering the C/I and monitor channels for IOM compatible devices and the feature control and signaling channels for SLD compatible devices.

Due to its capability to switch channels of different bandwidths, the EPIC can handle up to 32 ISDN subscribers with their 2B + D channel structure in IOM configuration or up to 16 subscribers in SLD configuration. Since its interfaces can operate at different data rates, the EPIC is an ideal device for data rate adaptation.

Moreover, the EPIC is one of the fundamental building blocks for networks with either central, de-central or mixed signaling and packet data handling architectures. The other key devices are the IDEC™ (ISDN D-Channel Exchange Controller, Am2075) and the HSCX (Enhanced High Level Serial Communication Controller, Am82525).

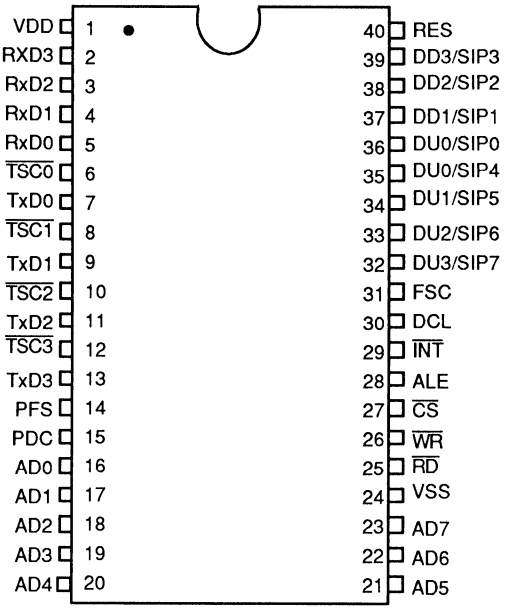
Applications of the EPIC include communication multiplexers, concentrators, central switches as well as peripheral ISDN and analog line cards.

The EPIC is available in a 40-pin DIP or a 44-pin PLCC package.

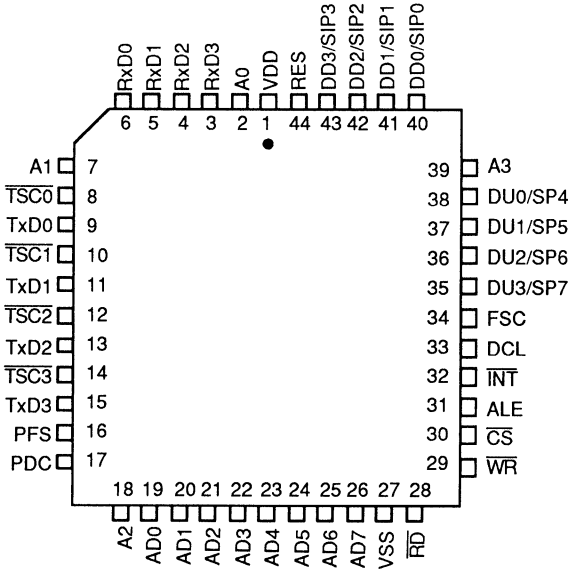
The 40-pin DIP/DIC version is controlled by a standard 8-bit parallel microprocessor interface with a multiplexed address-data bus. In the PLCC package the device may optionally be controlled by separate address and data buses.

CONNECTION DIAGRAMS
Top View

40-Pin DIP

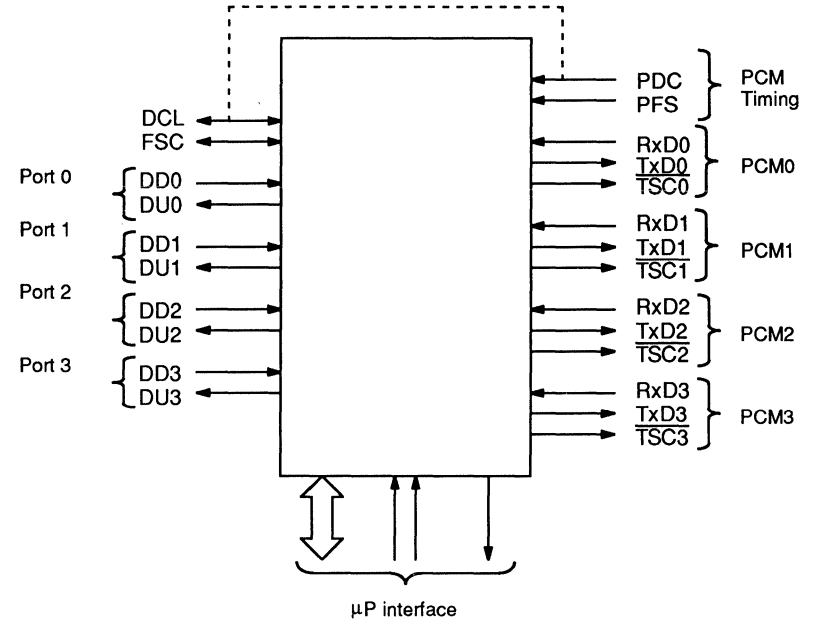


44-Pin PLCC

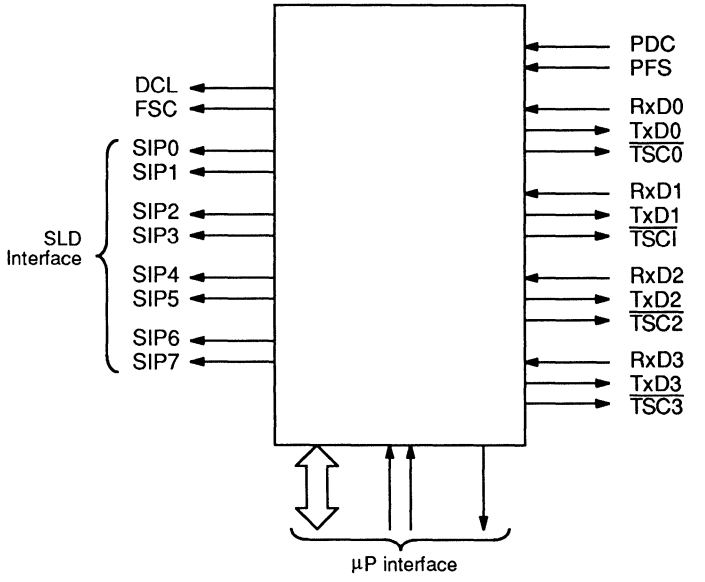


Note: Pin 1 is marked for orientation.

LOGIC SYMBOLS



Functional Symbol for the Duplex Configuration

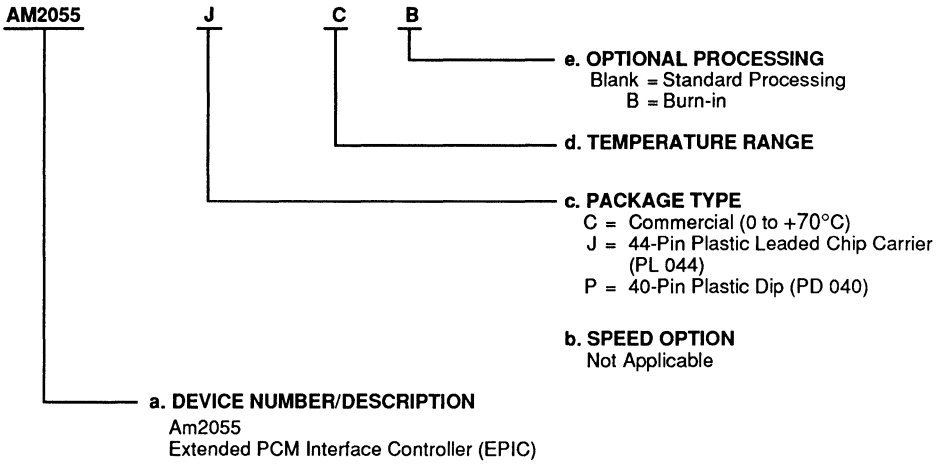


Functional Symbol for the SLD Configuration

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM2055	PC, JC, PCB, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Am2075

ISDN Digital Exchange Controller (IDEC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Four independent HDLC channels
- 64 byte FIFO storage per channel and direction
- Handling of basic HDLC functions
  - flag detection/generation
  - zero deletion/insertion
  - CRC checking/generation
  - check for abort
- Single connection and quad connection modes
- IOM™ interface or PCM interface
- Programmable time slots and channel data rates (up to 4 MBs)
- Different methods of contention resolution
- 8-bit parallel microcontroller interface with vectored interrupt
- Advanced CMOS technology
- Power consumption less than 50 mW

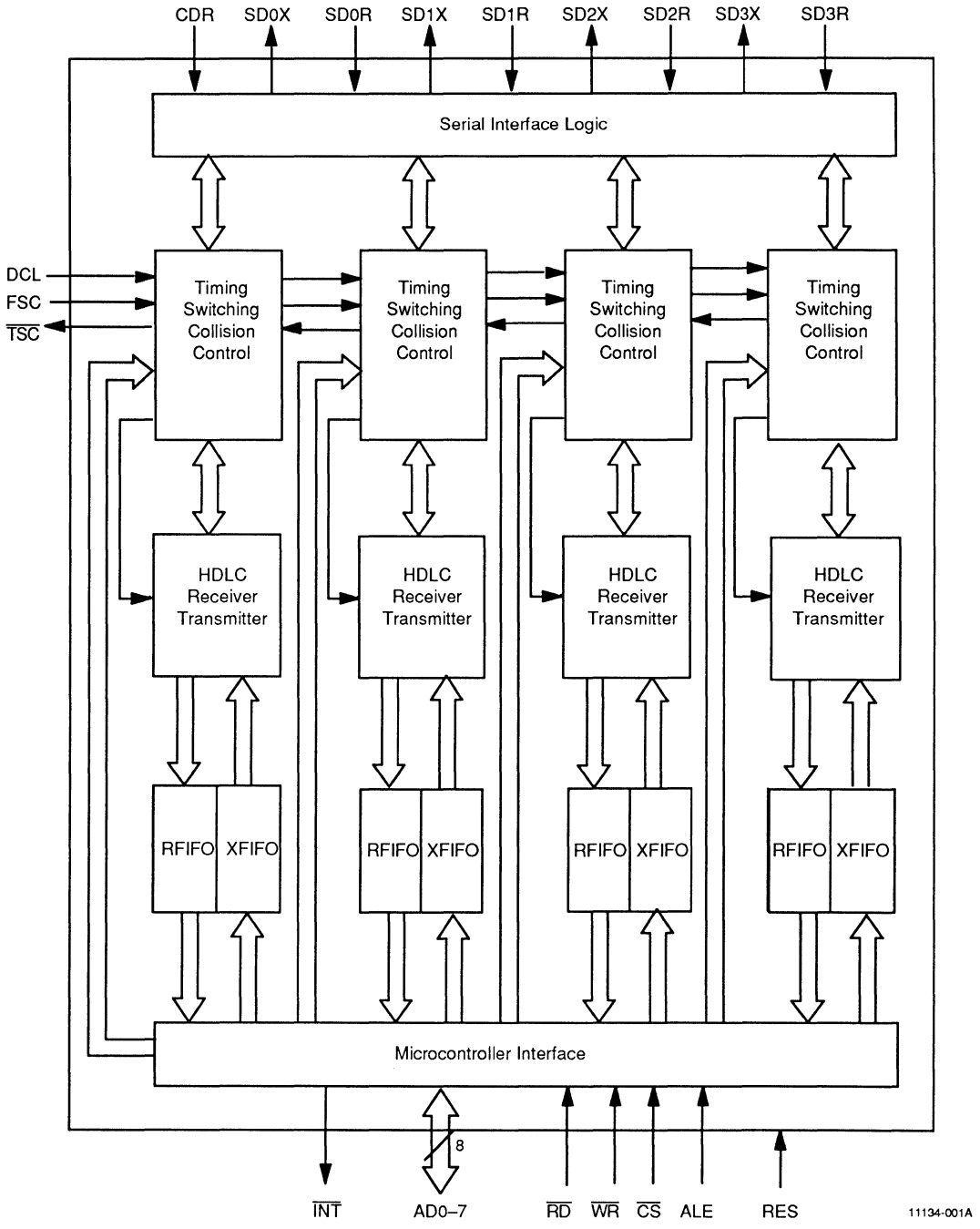
GENERAL DESCRIPTION

The Am2075, ISDN Digital Exchange Controller (IDEC), is a serial HDLC data communication circuit with four independent channels. Its telecommunication-specific features make it especially suited for use in variable data rate PCM systems. In addition, the device contains sophisticated switching functions and implements automatic contention resolution between packet data from different sources.

Its applications include communication multiplexers, peripheral ISDN line cards, packet handlers, and X.25 packet switching devices. The IDEC is a fundamental building block for networks with either centralized, decentralized, or mixed signaling packet data handling architectures.

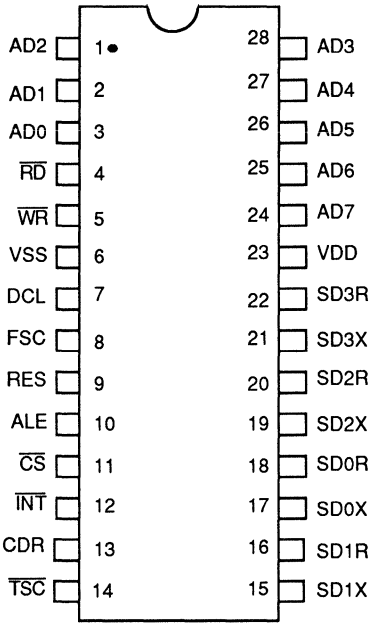
Publication # 11134 Rev. Amendment /0
Issue Date: April 1989

BLOCK DIAGRAM



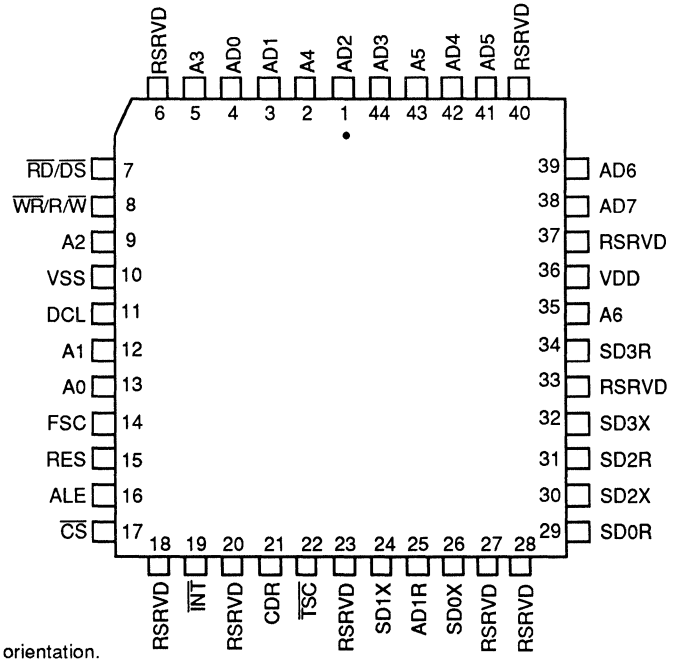
CONNECTION DIAGRAMS
Top View

28-Pin DIP



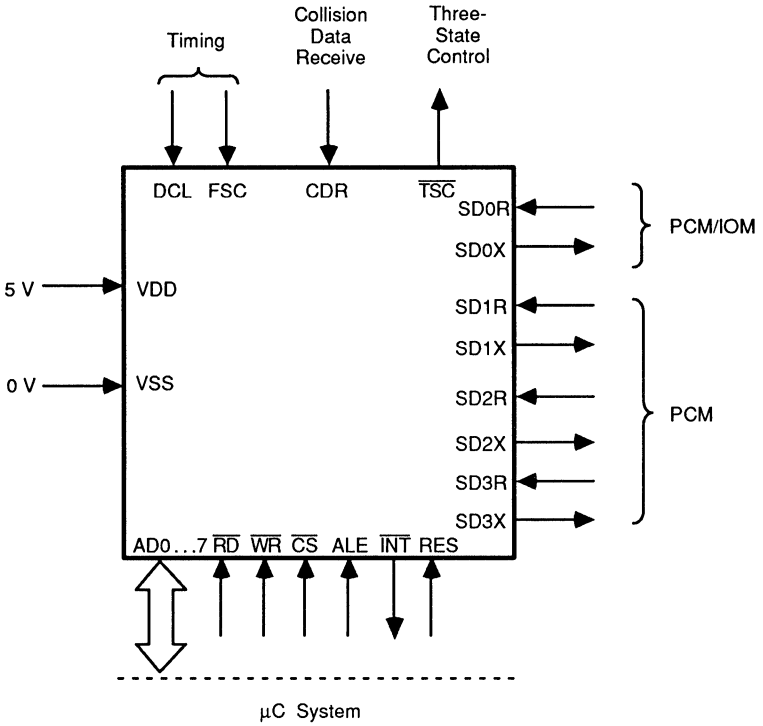
44-Pin PLCC

11134-002B



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



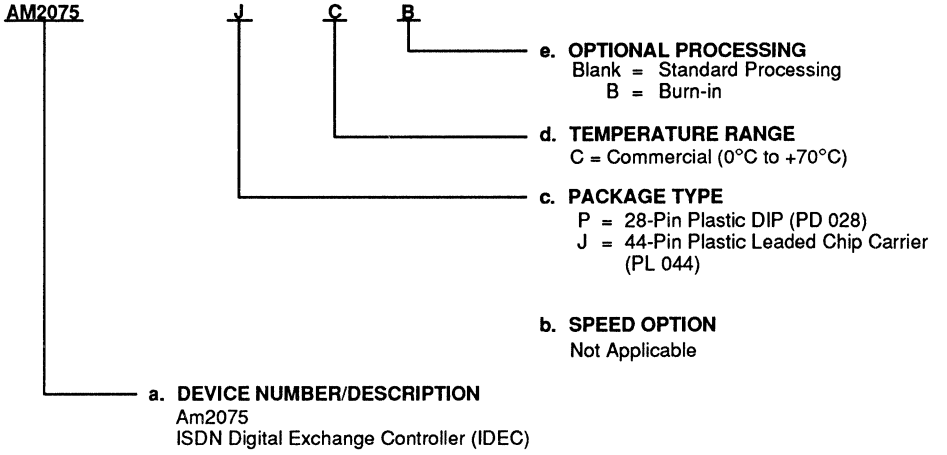
11134-003B

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM2075	PC, JC, PCB, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Am2080/B

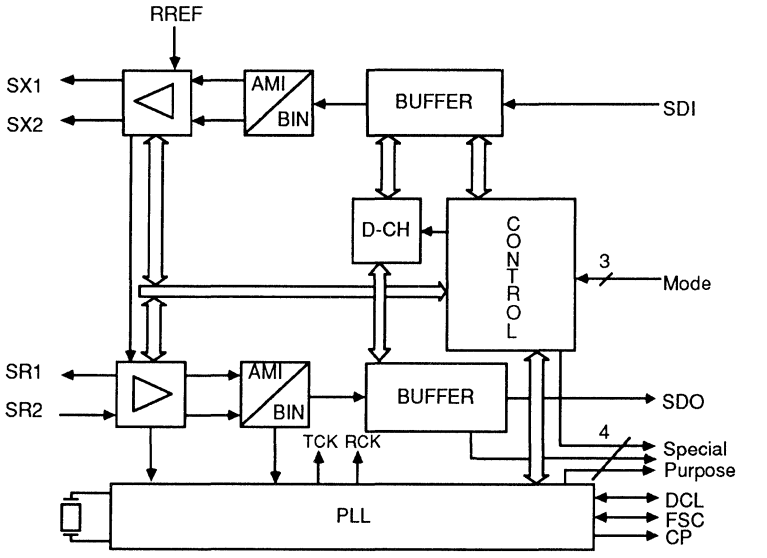
S-Bus Interface Circuit (SBC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Full duplex 2B + D S/T-interface transceiver according to CCITT I.430
- Conversion of the frame structure between the S/T and IOM™ interfaces
- D-channel access control
- Activation and deactivation procedures according to CCITT I.430
- Built-in wake-up unit for activation from power-down state
- Adaptively switched receive thresholds
- Control via IOM interface
- Several operating modes
- Receive timing recovery according to selected operating mode
- Frame alignment with absorption of phase wander in trunk line applications
- Switching of test loops
- Advanced CMOS technology
- Low power consumption:
  –standby less than 4 mW
  –active max 60 mW

BLOCK DIAGRAM



11135-001A

Publication # 11135 Rev. Amendment /0
Issue Date: March 1989

GENERAL DESCRIPTION

The Am2080 S-Bus Interface Circuit (SBC) implements the four-wire S/T-interface used to link voice/data terminals to an ISDN. Through selection of operating mode, the device may be employed in all types of applications involving an S-interface. In particular, two or more SBCs can be used to build a point-to-point, passive bus, extended passive bus, or star configuration.

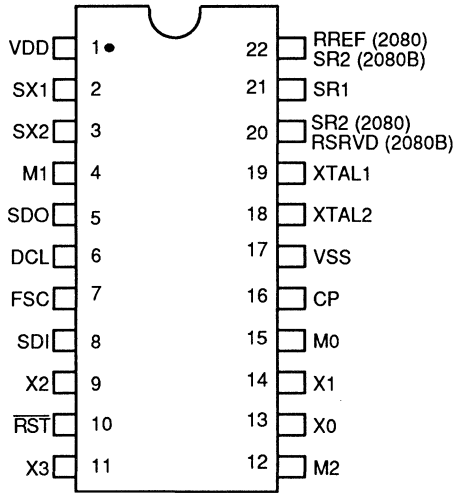
Specific ISDN applications of the SBC include: ISDN terminals, ISDN network termination (central office and PABX applications), and PABX trunk lines to central office.

The device provides all electrical and logical functions according to CCITT recommendation I.430. These include mode-dependent receive timing recovery, D-channel access and priority control, and automatic handling of activation/deactivation procedures. The SBC does not require direct microprocessor control.

The SBC is an IOM compatible part, 22-pin CMOS device. It operates from a single +5 V supply and features a power-down state with very low power consumption.

CONNECTION DIAGRAMS
Top View

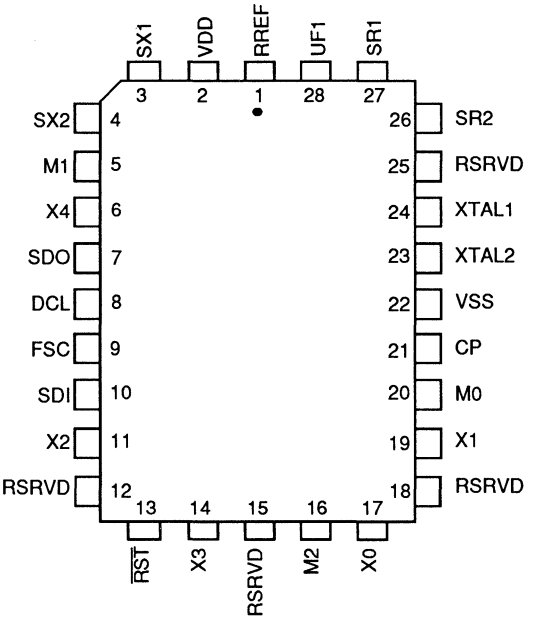
22- Pin DIP



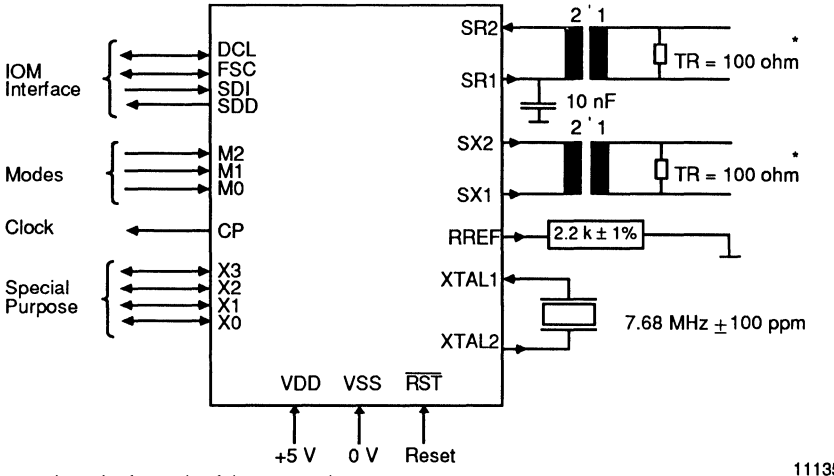
11135-002A

Note: Pin 1 is marked for orientation.

28-Pin PLCC



LOGIC SYMBOL



*Terminating resistors only at the far ends of the connection

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM2080
AM2080B

P C B

e. OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
P = 22-Pin Plastic Dip (PD 022)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am2080/B
S-Bus Interface Circuit (SBC)

Valid Combinations	
AM2080 AM2080B	PC, JC, PCB, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Am2081

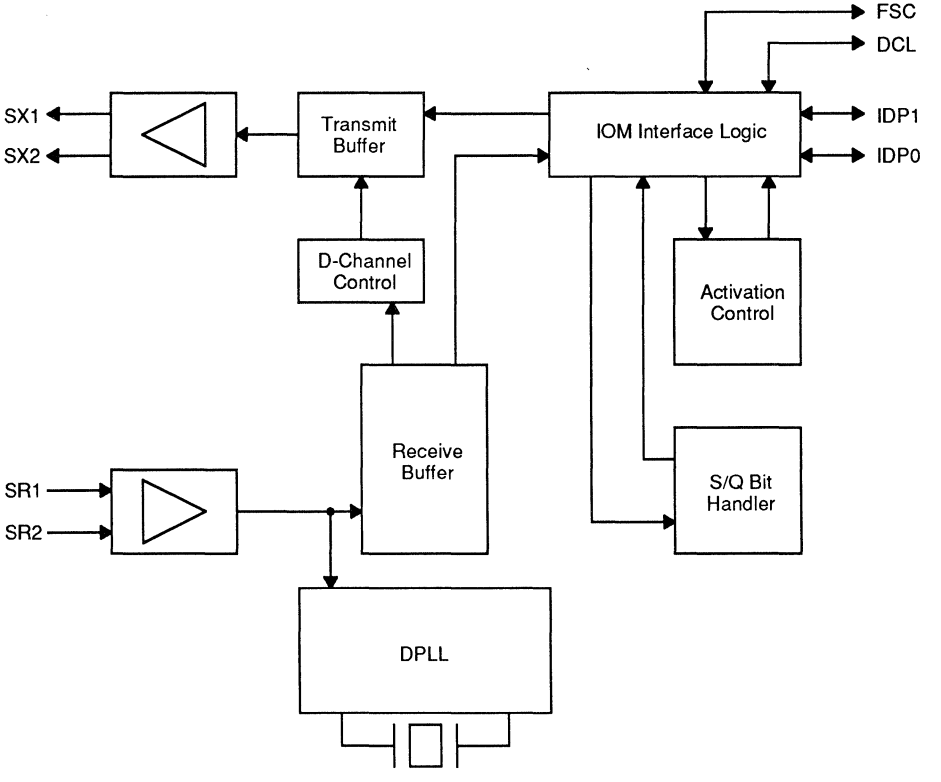
S/T Bus Interface Circuit Extended (SBCX)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Full duplex 2B + D S/T interface transceiver according to CCITT I.430
- Adaptive equalizer
- Receive timing recovery
- Built-in wake-up unit for activation from power–down state
- Conversion of the frame structure between the S/T interface and IOM™ Rev.2 Interface
- Activation and deactivation procedures according to CCITT I.430
- D-channel access control, also in trunk application
- Access to S and Q bits of S/T interface
- Automatic handling of S and Q bit messages
- Software controlled maintenance interface (I/O ports)
- Frame alignment with absorption of phase wander in NT2 network side applications
- Switching of test loops
- Several operating modes
- Advanced CMOS technology
- Low power consumption:
  – standby less than 6 mW
  – active max 80 mW

BLOCK DIAGRAM



Publication # 11150 Rev. Amendment /0
Issue Date: March 1989

GENERAL DESCRIPTION

The S/T Interface Circuit Extended (SBCX) Am2081 implements the four-wire S/T interface used to link voice/data ISDN terminals, network termination (Central Office and PABX applications), and PABX trunk lines to Central Office. Through selection of operating modes, the device may be employed in all types of applications involving an S/T interface. Two or more Am2081 SBCX can be used to build a point-to-point, passive bus, extended passive bus or star configuration.

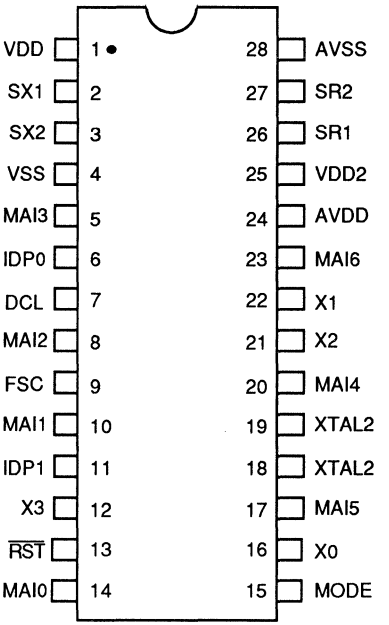
The Am2081 SBCX provides the electrical and functional link between the analog S/T interface according to CCITT recommendation I.430 and T1D1 Basic User Network Interface Specification, respectively, and the ISDN Oriented Modular (IOM) interface Rev. 2.

The Am2081 SBCX exceeds both the electrical and functional requirements of the S/T interface in order to provide high flexibility to the user with respect of S/T interface wiring configuration and implementation of layer-1 maintenance functions. By provision of some additional features at the IOM Rev. 2 interface the user is able to combine the SBCX with other IOM Rev. 2 devices in various configurations.

The Am2081 SBCX is a 28-pin CMOS device offered in both DIP and PLCC packages. It operates from a single 5 V supply and features a power-down state with very low power consumption.

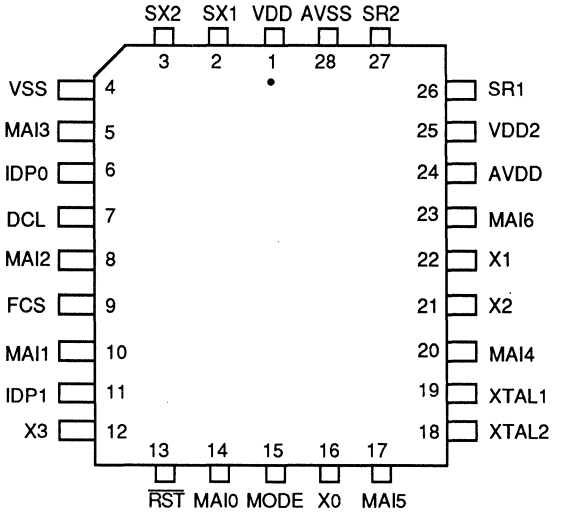
CONNECTION DIAGRAMS
Top View

28-Pin DIP



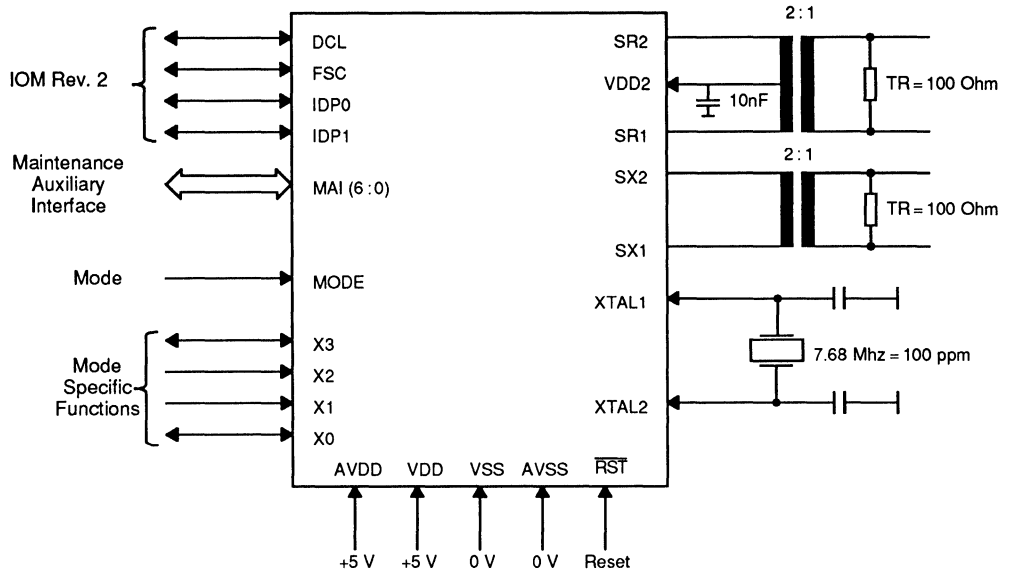
11134-002B

28-Pin PLCC



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM2081 **J** **C** **B**

e. OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
P = 28-Pin Plastic DIP (PD 028)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am2081
S/T Bus Interface Circuit Extended (SBCX)

Valid Combinations	
AM2081	JC, JCB, PC, PCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Am2095

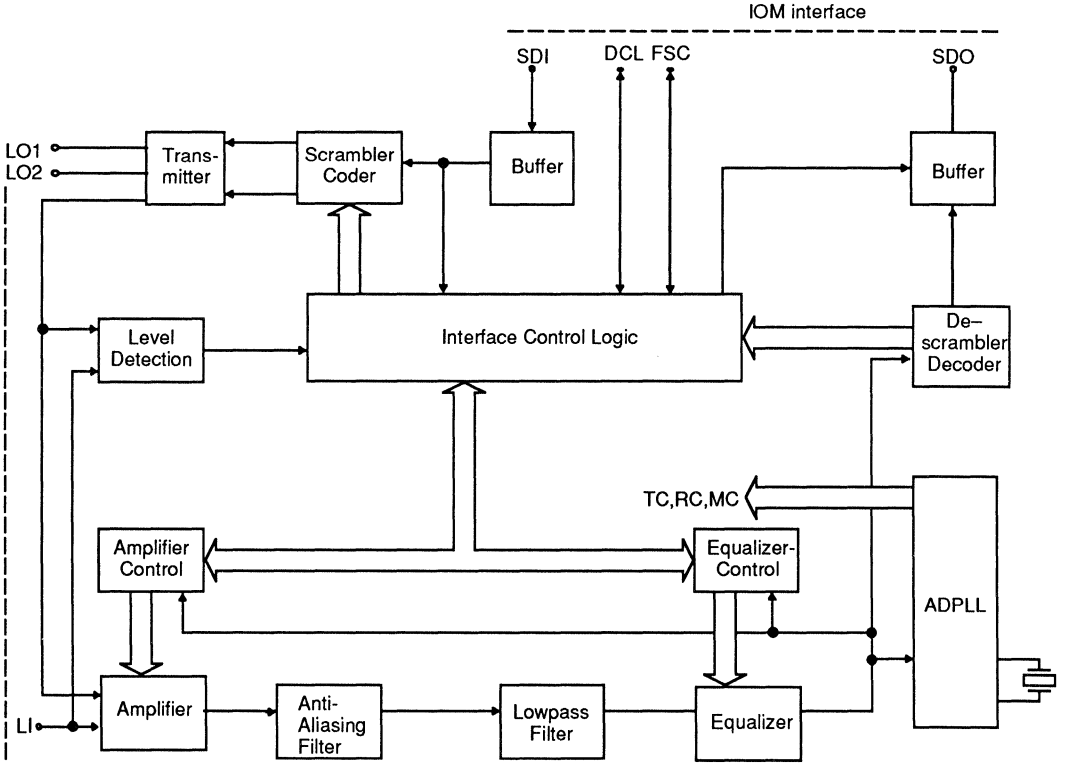
Burst Transceiver Circuit (IBC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Half-duplex burst mode 2-wire U-interface transceiver
- 144 kbps user bit rate (2B + D)
- 384 kHz line clock rate
- IOM compatible
- Clock and frame recovery
- Adaptive line equalization and amplification at receiver
- Implementation of activation/deactivation procedures
- Mode configurable to function at both ends of the line
- Built-in wake-up function for activation from power-down state
- Switching of test loops
- Typical length of loop: up to 3.5 km with 0.6 mm diameter wire
- Advanced CMOS technology
- Low power consumption •
  –6 mW power down
  –80 mW power up (maximum)

BLOCK DIAGRAM



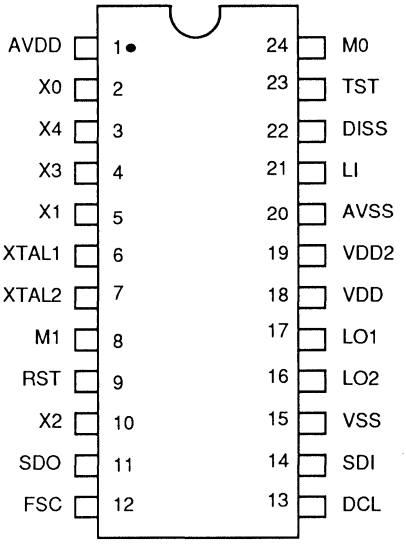
Publication # 11137 Rev. Amendment /0
Issue Date: March 1989

GENERAL DESCRIPTION

The Am2095 ISDN burst transceiver circuit (IBC) is a full duplex transceiver for the 2-wire transmission line (CCITT U-reference point). Full duplex transmission is achieved using a time compression multiplex (ping-pong) technique. The device links the 2-wire transmission line to the ISDN Oriented Modular (IOM™) interface and to the AMD family of ISDN devices. The device manages layer 1 of the interface protocol and can communicate with other layer 1 or layer 2 devices over the IOM interface.

CONNECTION DIAGRAM
Top View

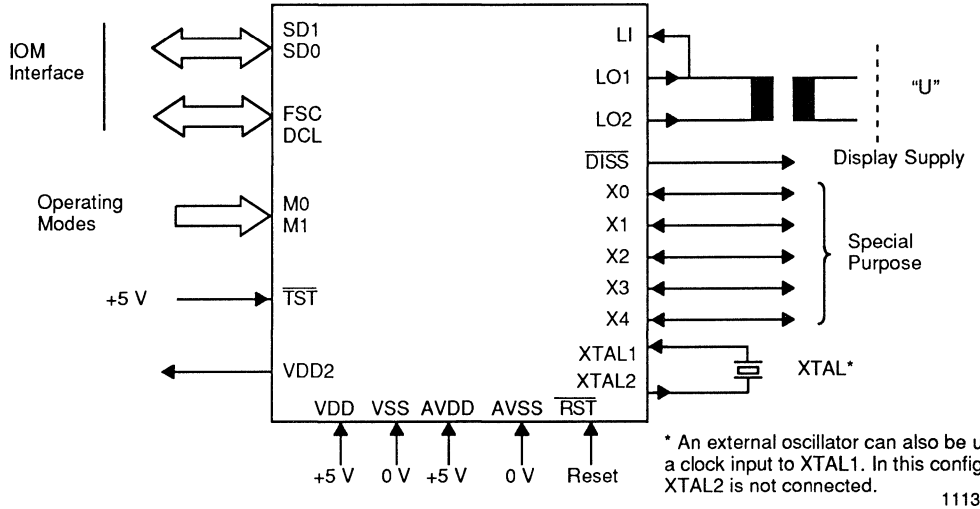
24-Pin DIP



Note: Pin 1 is marked for orientation.

11137–002B

LOGIC SYMBOL



* An external oscillator can also be used as a clock input to XTAL1. In this configuration XTAL2 is not connected.

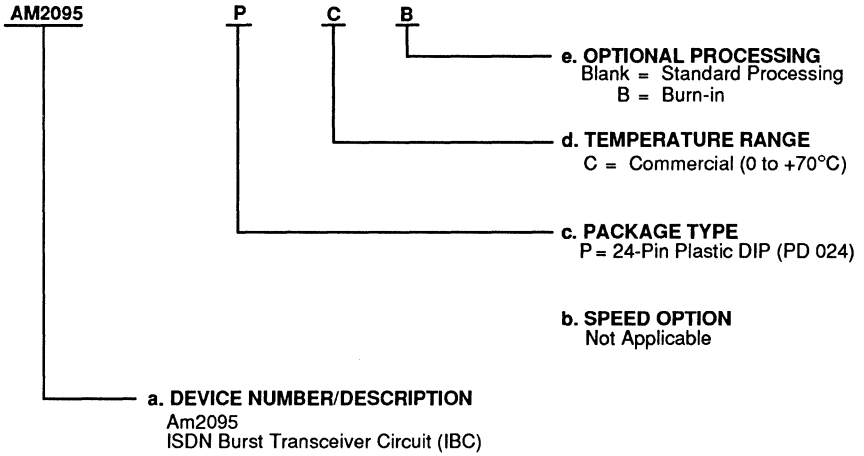
11137–003B

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM2095	PC, PCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military-grade products.

Am20901/Am20902

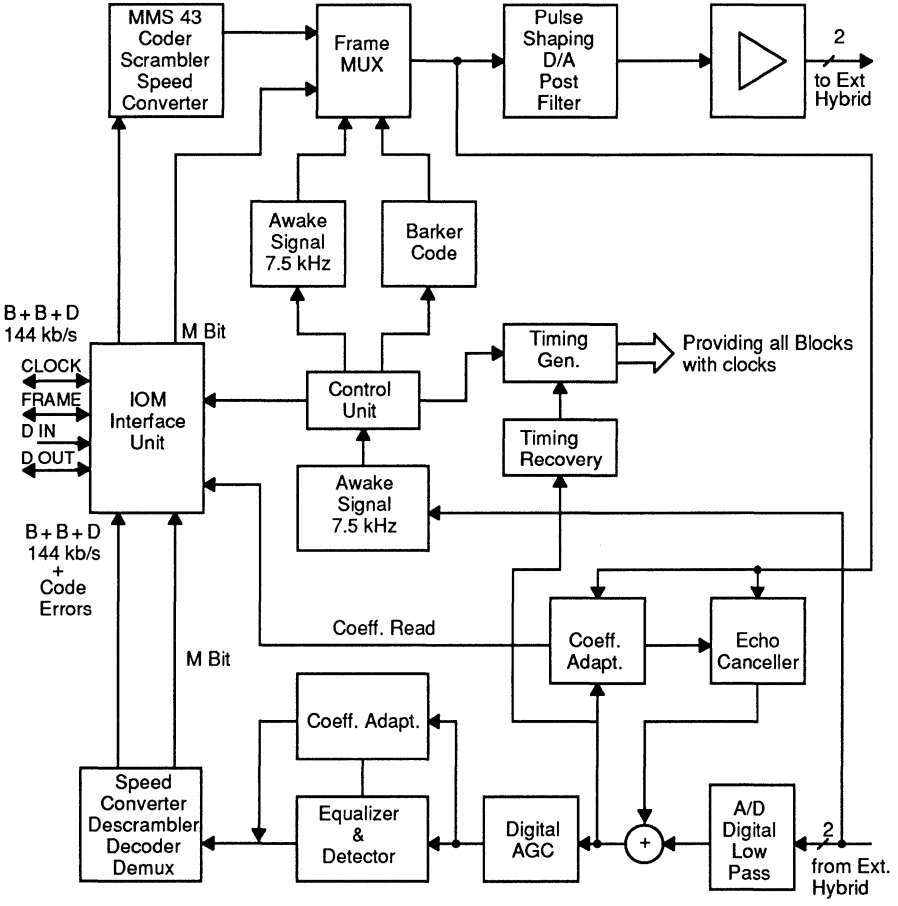
ISDN Echo Cancellation Circuit (IEC) Two-Chip Set

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Full duplex transmission and reception of the "U" (4B3T) interface signals according to the FTZ Guideline 1R 220 of the Deutsche Bundespost (DBP)
  - –144 kbps user bit rate over standard local telephone loops
  - –1 kbps maintenance channel for transmission of data loop back commands and detected transmission errors
  - –4B3T ternary block code (subscriber line symbol rate 120 kbaud)
  - –Monitoring of transmission errors
  - –Subscriber loop length without repeater:
    up to 4.2 km on 0.4 mm wire
    up to 8.0 km on 0.6 mm wire
- Adaptive echo cancellation
- Adaptive equalization
- Automatic polarity adaptation
- Clock recovery (frame and bit synchronization) in all applications

BLOCK DIAGRAM



Publication # 11152 Rev. Amendment /0
Issue Date: March 1989

DISTINCTIVE CHARACTERISTICS (continued)

- Transposition of ternary to binary data and vice versa (coding, decoding, scrambling, descrambling, phase adaptation)
- Built-in wake-up unit for activation from power-down state
- Activation and deactivation procedure according to CCITT I.430 and to FTZ Guideline 1R 210 of the DBP
- Adaptation of internal interfaces to the current signal direction by programmable operation modes:
  LT: Line Terminator in public or private exchange
  NT: Network Terminator connected to SBC
  NT-PABX: Trunk Module (TMD)
  NT-TE: Terminal equipment
  LT-RP: U Repeater unit subscriber side
  NT-RP: U Repeater unit exchange side
- Optimized for working in conjunction with SBC via IOM interface
- Data speed conversion between the U_{K0} frames and the IOM frames. In the LT and NT-PABX modes absorption of received phase-wander of up to 18 µsec peak to peak (CCITT Rec. Q.512)
- Handling of commands and indications contained in the IOM C/I channel for (de-) activation, supervision of power supply unit and equipment for wire testing
- Data availability via the MONITOR channel:
  –accumulated RDS transmission errors; in the LT mode for the whole U_{K0} link, in the NT mode only for those detected in the circuit itself
  –measurement value of the loop current
  –Echo canceller coefficients and status values, which can be used to give evidence of the state of "U" interface link
- Switching of an analog test loop at the U_{K0} interface for testing as many units of the IEC as possible (loop 1 in LT, loop 4 in the repeater and loop 3 in the NT-PABX mode in reverse direction to the public exchange)
- Switching of a digital test loop as near to IOM as possible (loop 2 in NT-PABX and NT-TE)
- Remote control of test loop switching via maintenance channel
  Test loop 2 in the SBC (NT mode)
  Test loop 2 in the IEC near to the IOM interface in the NT-PABX and TE modes
  Test loop 4 in the IEC LT-repeater mode near to the U-line
- Generation of a synchronized 7.68 MHz clock for the SBC in the mode

GENERAL DESCRIPTION

The Am20901/20902 ISDN Echo Cancellation Circuit (IEC) is an advanced CMOS circuit for transmission over the U_{K0} interface. The adaptive filter concept of the IEC is based on a highly digital approach which utilizes a sophisticated digital signal processing capability.

The Am20901/20902 enables digital full duplex voice/data transmission via the standard twisted pair telephone cable. (U interface) with a user bit rate of 144 kbps according to the ISDN standards. Together with the flexible IOM interface, it is fully compatible to operate with the Am2080 (SBC) devices and also enables a repeater (two IEC's back to back) for longer telephone loops.

The IEC is capable of operating in the following applications by means of pin strapping: the exchange, the network termination, the terminal equipment, and the trunk model connecting a PABX to the public network.

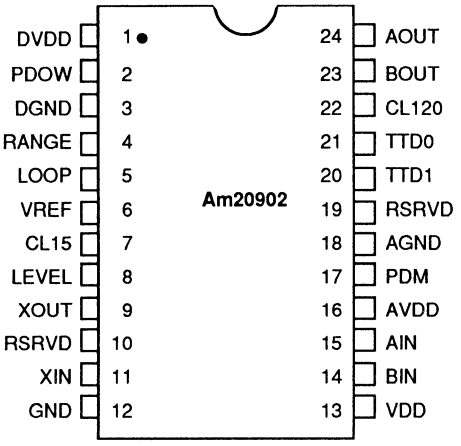
At the present the IEC is available in a two chip set only.

A "Digital" Circuit, called IEC-D (PEB 20901) contains the digital receiver functions and the IOM™ -U_{K0} interface functions.

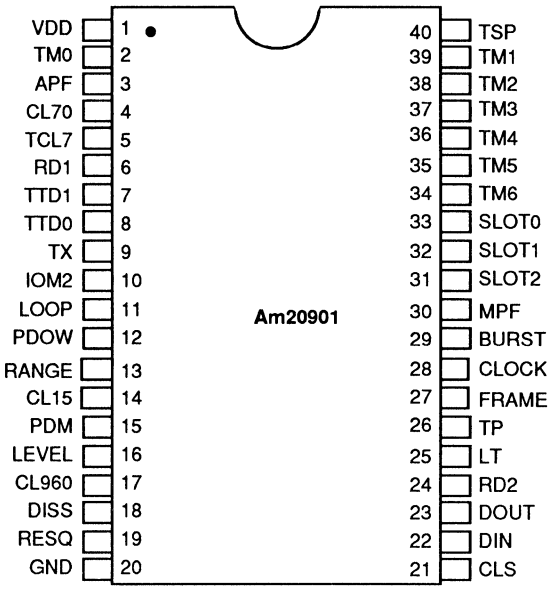
An "Analog" Circuit, called IEC-A (PEB 20902) contains the crystal oscillator and all of the analog functions of the line port, namely the A/D converter in the receive path and pulse shaping D/A converter and line driver in the transmit path.

CONNECTION DIAGRAMS
Top View

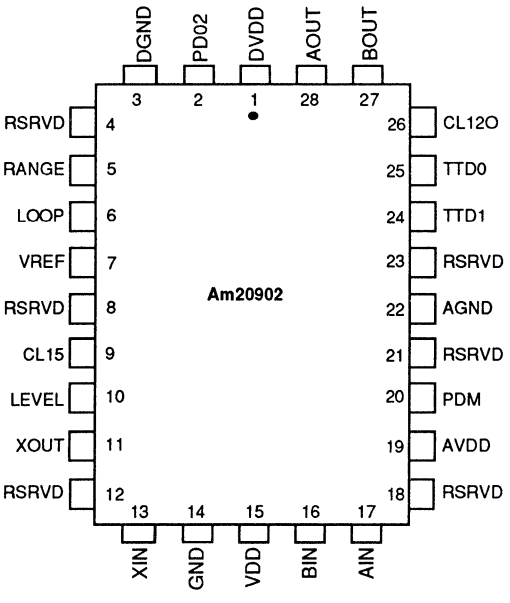
24-Pin DIP



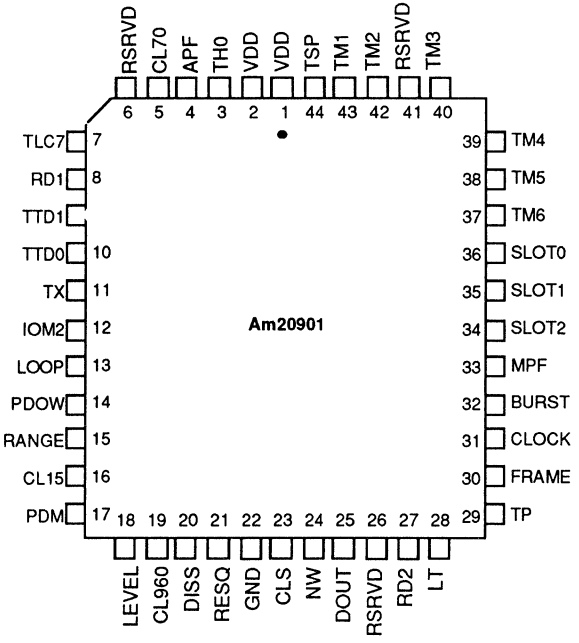
40-Pin DIP



28-Pin PLCC

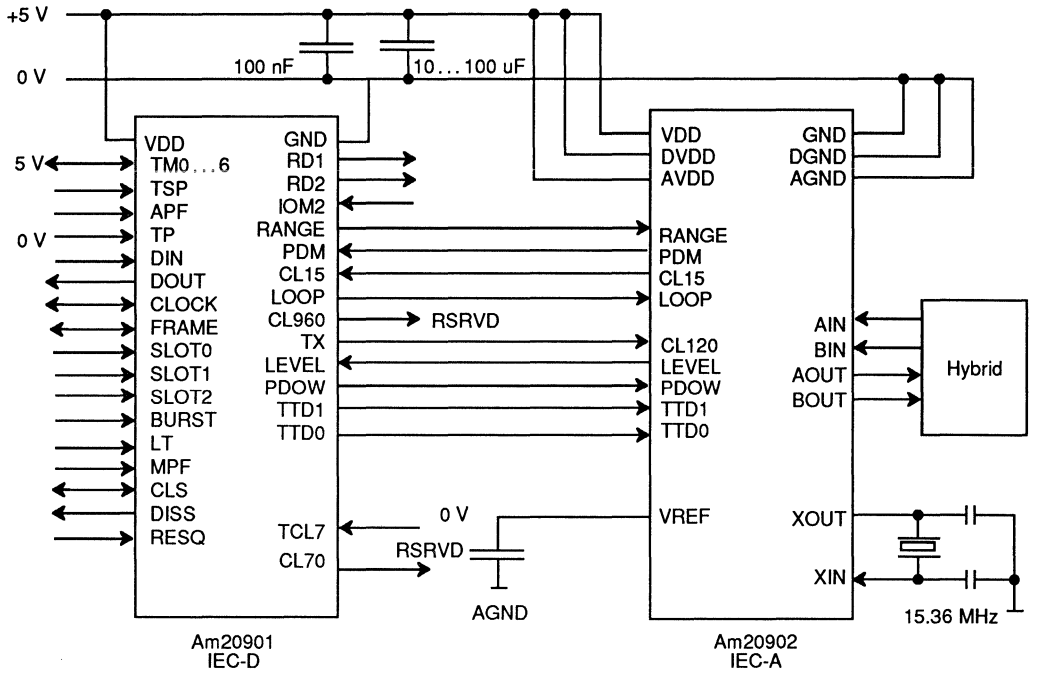


44-Pin PLCC



Note: Pin 1 is marked for orientation.

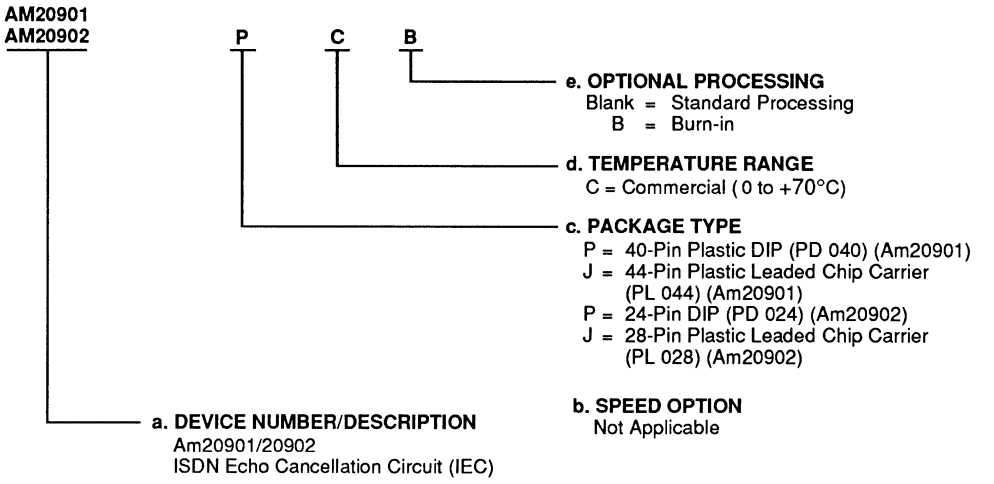
LOGIC SYMBOL



ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM20901 AM20902	PC, JC, PCB, JCB PC, JC, PCB, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

*The Am2090 is a two-chip set. It is ordered as an Am20901 and Am20902.

Am2091

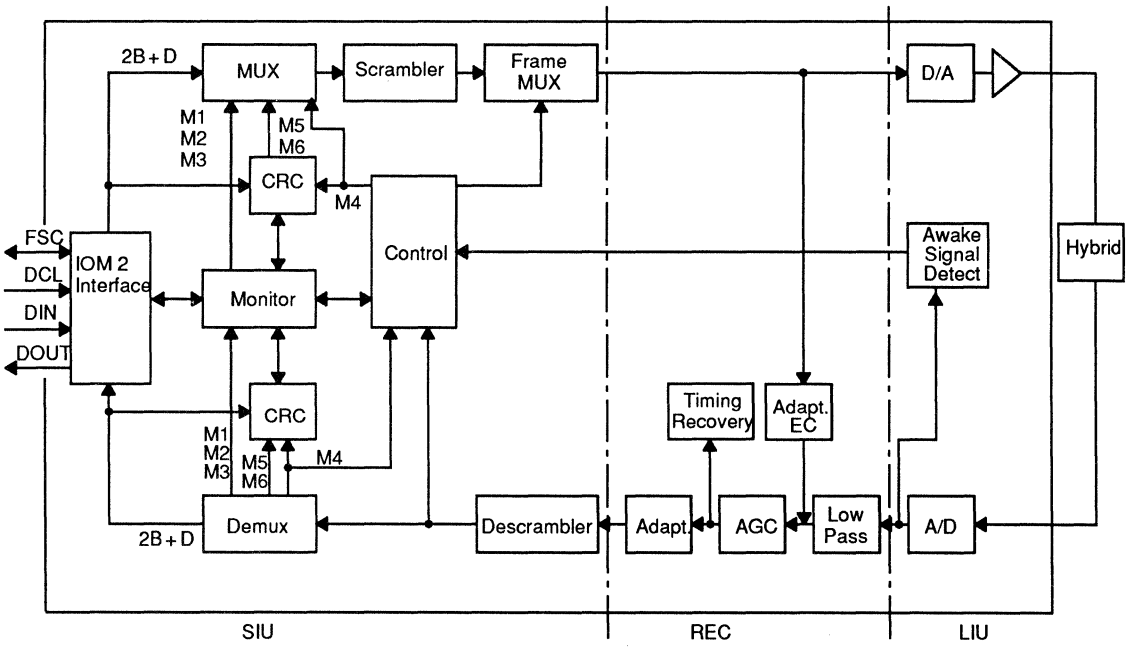
ISDN Echo Cancellation Circuit (IEC-Q)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Full duplex data transmission and reception at the
  - –U-Reference point according to the layer 1
  - –Specification of the American Standard of Telecommunications:
  - –144 kbps user bit rate over a two wire subscriber loop
  - –2B1Q block code (2 binary, 1 quaternary)
  - –4 kbps maintenance channel for transmission of data loop back commands and detected transmission errors
  - –monitoring of transmission-errors
  - –operating at telephone loop plant LOOP #1 up to LOOP #15 as defined by American National Standard
- Transposition of quaternary to binary data and vice versa (coding, decoding, scrambling, descrambling, phase adaptation)
- Built-in wake up unit for activation from power down state
- Activation and deactivation procedure according to T1D1 layer 1 Specification and CCITT I.430
- Adaptation of internal interfaces to the current signal direction by programmable operation modes:
  - –LT: Line termination in public or private exchange
  - –TE: Terminal mode
  - –NT: Network termination connected to SBCX
  - –NT-PABX: Trunk module (TDM)

BLOCK DIAGRAM



Publication # 11892 Rev. Amendment /0
Issue Date: March 1989

DISTINCTIVE CHARACTERISTICS (continued)

- Adaptive echo cancellation
- Adaptive equalization
- Clock recovery (frame and bit synchronization) in all applications
- Optimized for working in conjunction with SBCX, EPIC™ and IDEC™ Telecom ICs via IOM™2 interface
- Data speed conversion between the U-Reference Point and the IOM frame
- Handling of the Commands and Indications contained in the IOM2 C/I channel for deactivation, activation, supervision of power supply unit and equipment for testing
- Data availability via monitor-channel:

  CRC transmission error

  Measurement value of the loop current

  Echo Canceller Coefficients and Status values, which can be used to indicate the state of the loop
- Switching test loops
- Generation of synchronized 7.68 MHz clock for SBCX in NT mode
- Low power consumption:
  - standby max 30 mW
  - active max 300mW
- 40-pin DIP and 44-pin PLCC package

GENERAL DESCRIPTION

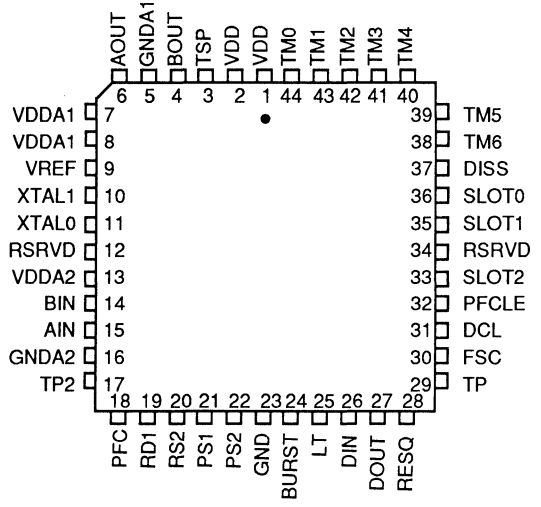
The Am2091 ISDN Echo Cancellation Circuit (IEC-Q) is an advanced CMOS single chip transceiver for ISDN Basic Access Digital Subscriber Loops with 2B1Q line code.

According to the Layer 1 Specification of the American National Standard of Telecommunication control and algorithmic requirements are implemented for a 144 kbps full duplex data transmission.

Together with the flexible IOM2 interface the IEC-Q is fully compatible with the Am2081 (SBCX). Am2055 (EPIC), and Am2075 (IDEC) devices.

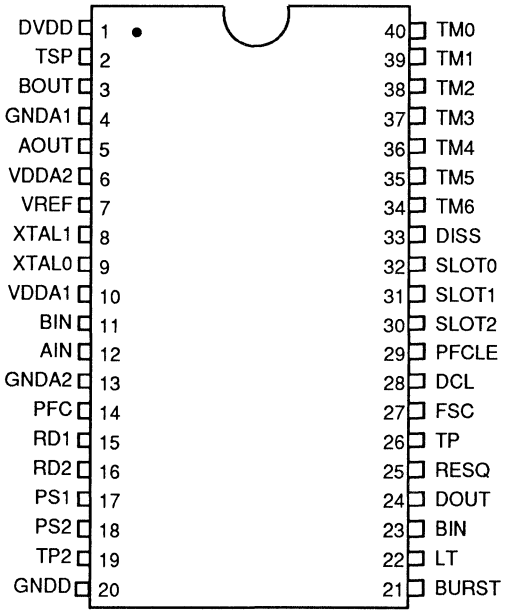
CONNECTION DIAGRAM
Top View

44-Pin PLCC



Note: Pin 1 is marked for orientation.

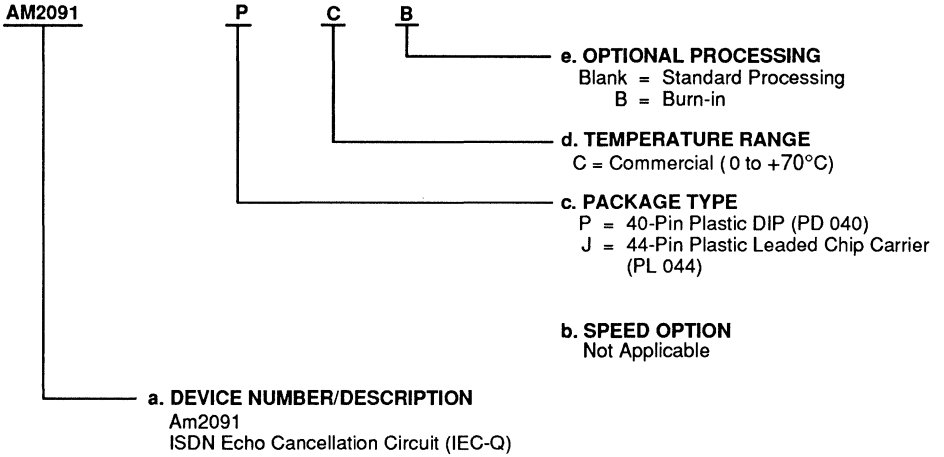
40-Pin DIP



ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM2091	PC, PCB, JC, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Am82520

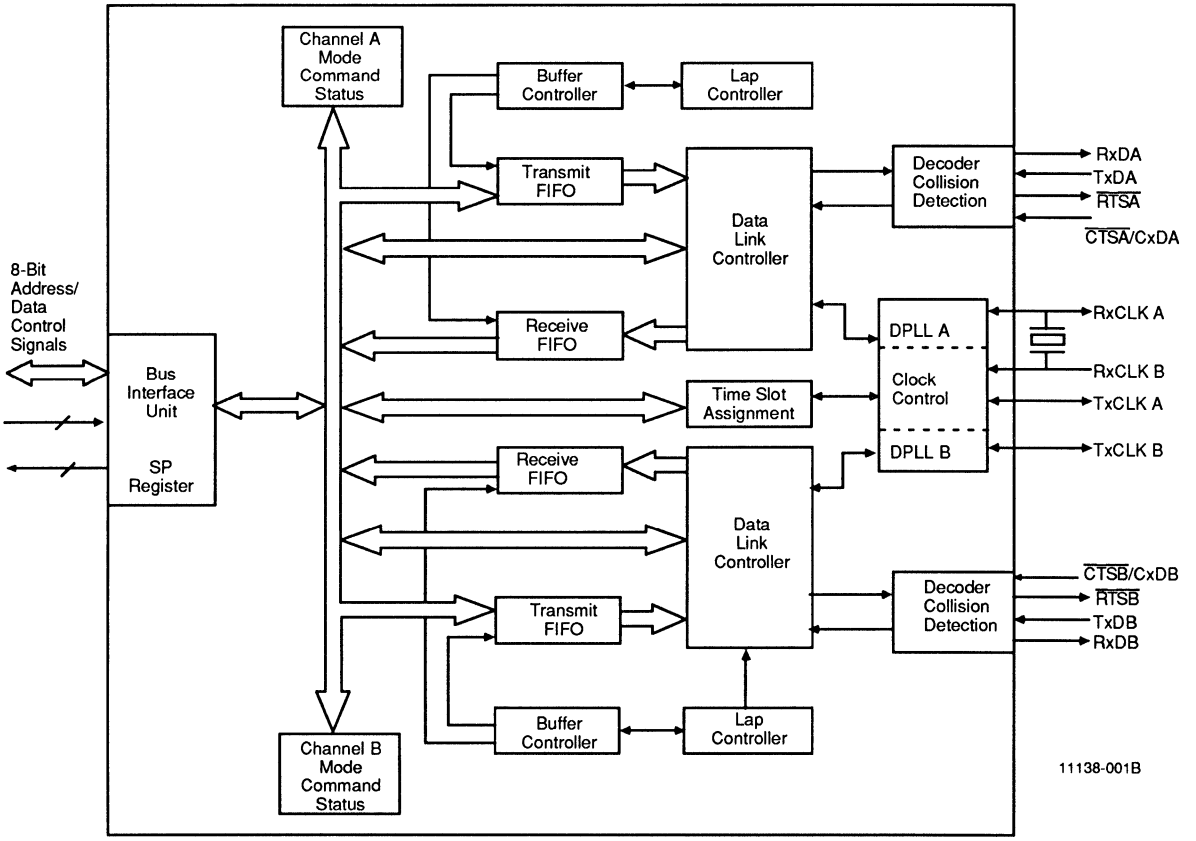
High-Level Serial Communications Controller (HSCC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Two independent HDLC channels
- Implementation of X.25 LAPB/LAPD protocol
- Programmable timeout and retry conditions
- FIFO buffers for efficient transfer of data packets
- Digital phase locked loop for each channel
- Baud rate generator and oscillator
- Different modes for clock recovery and data encoding
- High-speed data rate (up to 4 MHz)
- Supports bus configuration by collision resolution
- Telecom-specific features programmable
- 8-bit parallel µP interface
- Advanced CMOS technology
- Low power consumption;
  active: 25 mW at 4 MHz
  standby: 3 mW
- Package: 28-Pin Plastic DIP or 28-Pin Plastic Leaded Chip Carrier
- Operating temperature 0 to +70° C
- Industrial: operating temperature –40 to +85°C

BLOCK DIAGRAM



Publication # 11138 Rev. Amendment /0
Issue Date: March 1989

GENERAL DESCRIPTION

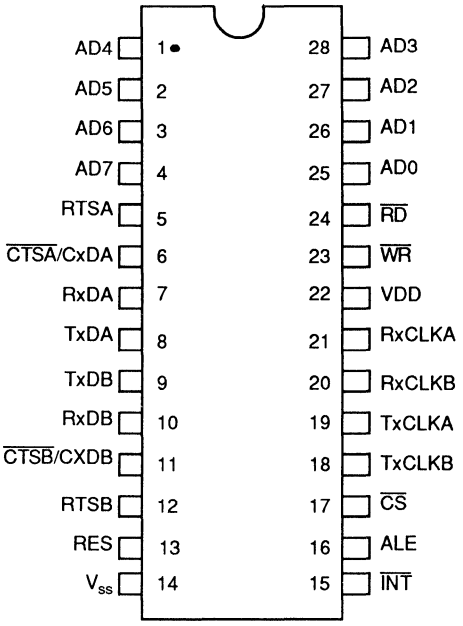
The Am82520, High-Level Serial Communications Controller (HSCC), has been designed to free the user from tasks occurring in communication with networks and trunk lines. It is an X.25 LAPB/LAPD controller which to a large degree performs communication procedures independent of CPU support.

A parallel processor bus constitutes the microprocessor system. The serial communications interface consists of two full-duplex HDLC channels that can be operated independently from one another. The HSCC is connected to the transmission line by additional line drivers or modems. The need for external hardware is reduced because of added functions on-chip. The functions incorporated include an oscillator, DPLL (one per channel), programmable baud rate generator, and time slot assigner.

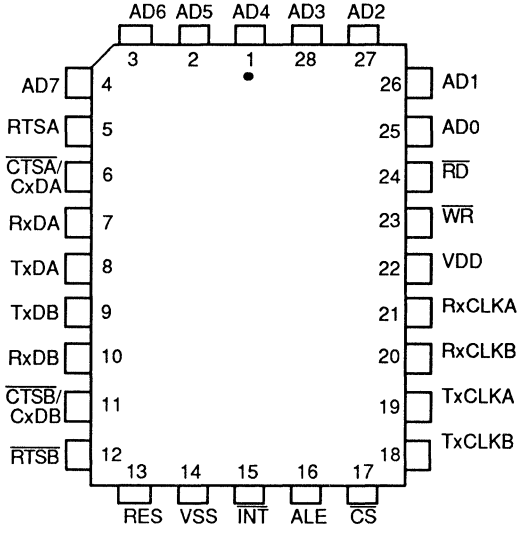
The chip contains a serial interface for two channels including a DPLL and collision-detection block, a data-link controller, and FIFO buffers. The µP interface, including the status and command registers, is used for both channels. The HSCC is implemented in a 2 micron CMOS technology.

CONNECTION DIAGRAMS
Top View

28-Pin PDIP

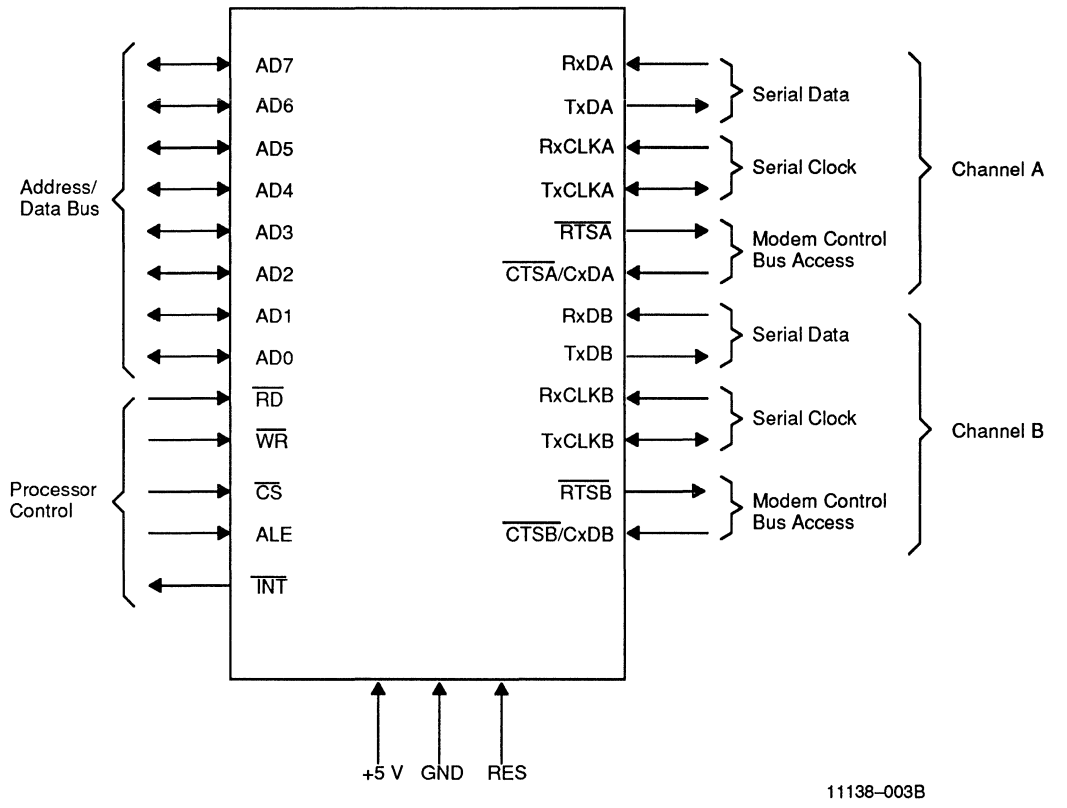


28-Pin PLCC



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

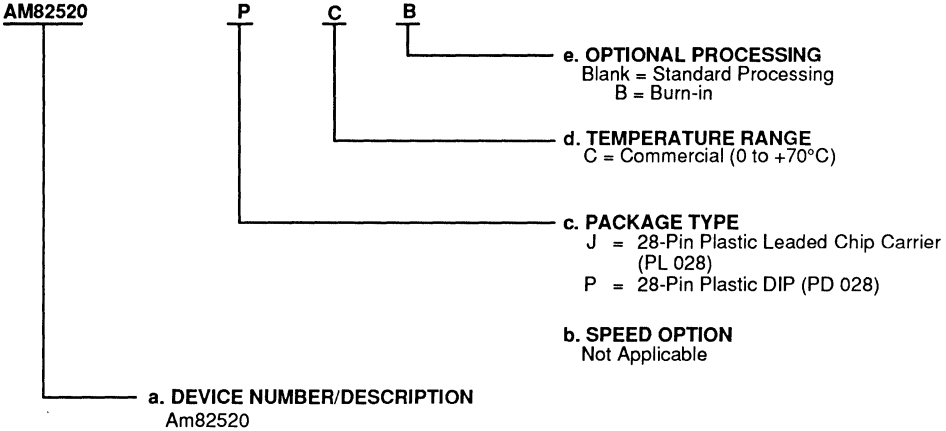


ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM82520	PC, JC, PCB, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

INTEGRATED SERVICES DIGITAL NETWORK (ISDN)

Support Tools

ISDN DEVELOPMENT/EVALUATION SYSTEM

Typically, communication designs take a considerable time to bring to market. But AMD's total product concept solves that problem by providing everything necessary to drastically cut time to market.

In communications, software challenges can be more complex than hardware design issues. AMD-supplied software gives our products a decisive advantage. Your designs become more cost-effective and easier to get to market because you don't have to generate software and hardware to make AMD products fit in your application.

In an ISDN design, we supply AmLink3™ and AmLink™ software, providing the lower layer, core communications requirements of your system. This enables you to focus your software development efforts on the application-specific aspects that give your product added value over your competitor.

There's also evaluation software to assist you in learning about, exercising and demonstrating distinctive features of selected ICs. Design time is greatly reduced when you use this software to study and evaluate components.

We understand your need to be able to rapidly evaluate our products. We offer a complete set of evaluation boards and software tools that allow you to demonstrate functions, measure key specifications and reduce design time. Most of these boards operate in a PC, eliminating the need for expensive dedicated development systems.

Development boards, like the ISDN Terminal Coprocessor Board (ITCB™), do more than demonstrate functions. The ITCB allows you to start working with an ISDN design immediately. There is breadboard space on the ITCB to customize an application. We even provide the schematics.

AmLink3/AmLink

Compliance-tested link access software such as AmLink3 and AmLink is used for linking lower OSI Model layers. This software is universally applicable because it is operating system independent.

AmLink3 has been tested for communications networks world-wide and meets the Q.921 and Q.931 CCITT recomendations. It supports LAPD (Link Access Protocol D-channel) and/or LAPB (Link Access Protocol Balanced) for both channels concurrently, as well as D-channel signalling and X.25. The software uses a state table-based implementation for structured design and flexibility.

AmLLD Low-Level Device Drivers

Each AMD ISDN component is supported by an AmLLD Low-Level Device Driver. The AmLLD's source code contains examples which illustrate how to use and access the many features of the device. They are intended to be used with AmLink or AmLink3. The interfaces provided by the AmLLD's use the same primitives so that both B-channel and D-channel can use the same layer 2 software. The AmLLD's provide a hardware independent interface to upper layer protocols, such as LAPD.

Am79B320 ITCB

A full range of ISDN evalation boards and development tools are available. Our evaluation and development boards are designed to operate on PC XT or AT personal computers with MS DOS 2.0 or greater, allowing you to develop your systems quickly and effectively. They provide a direct connection to the four-wire ISDN "S" interface. When used with the AmLink3 software, our ISDN Terminal Coprocessor Boards (ITCB) provide a convenient development vehicle for AMD products. The ITCB is an ISDN PC card design for development work, and it can even be used for manufacturing.

VOICE SWITCHING PRODUCTS

THE DUAL-CHANNEL, CMOS DSLAC JOINS THE SLAC™ IN THE FIRST CODEC-FILTER FAMILY TO USE DIGITAL SIGNAL PROCESSING TECHNOLOGY TO SOLVE YOUR LINECARD PROBLEMS

Advanced Micro Devices' Am7901 and Am7905 Subscriber Line Audio-Processing Circuits (SLAC) have been joined by the new Am79C02 Dual SLAC (DSLAC™) to form the world's most high-performance and cost-effective family of user-programmable codec-filters.

By employing state-of-the-art digital signal processing technology, AMD has integrated programmable filters and other linecard functions with the codec, and has made it possible for a single linecard design to satisfy the requirements of many different telecom environments.

The new DSLAC now provides the designer with two independently programmable channels on the same chip, in addition to the advantages of CMOS.

No other approach to linecard design offers as much efficiency, flexibility, and reliability.

THE FIRST MONOLITHIC SLIC FAMILY TO PROVIDE A BORSHT FUNCTION AND METERING SOLUTION TAILORED TO YOUR SYSTEM'S REQUIREMENTS

Designed using high-voltage bipolar process technology with precision thin-film resistors, Advanced Micro Devices Subscriber Line Interface Circuit (SLIC) family of products offers the designer a highly integrated solution for the BORSHT* and metering line-card functions. A variety of functional configurations and performance grades are available to provide a cost-effective SLIC tailored to your system's needs. Along with improved system performance, AMD's SLIC products also provide special signalling functions and dramatic power savings.

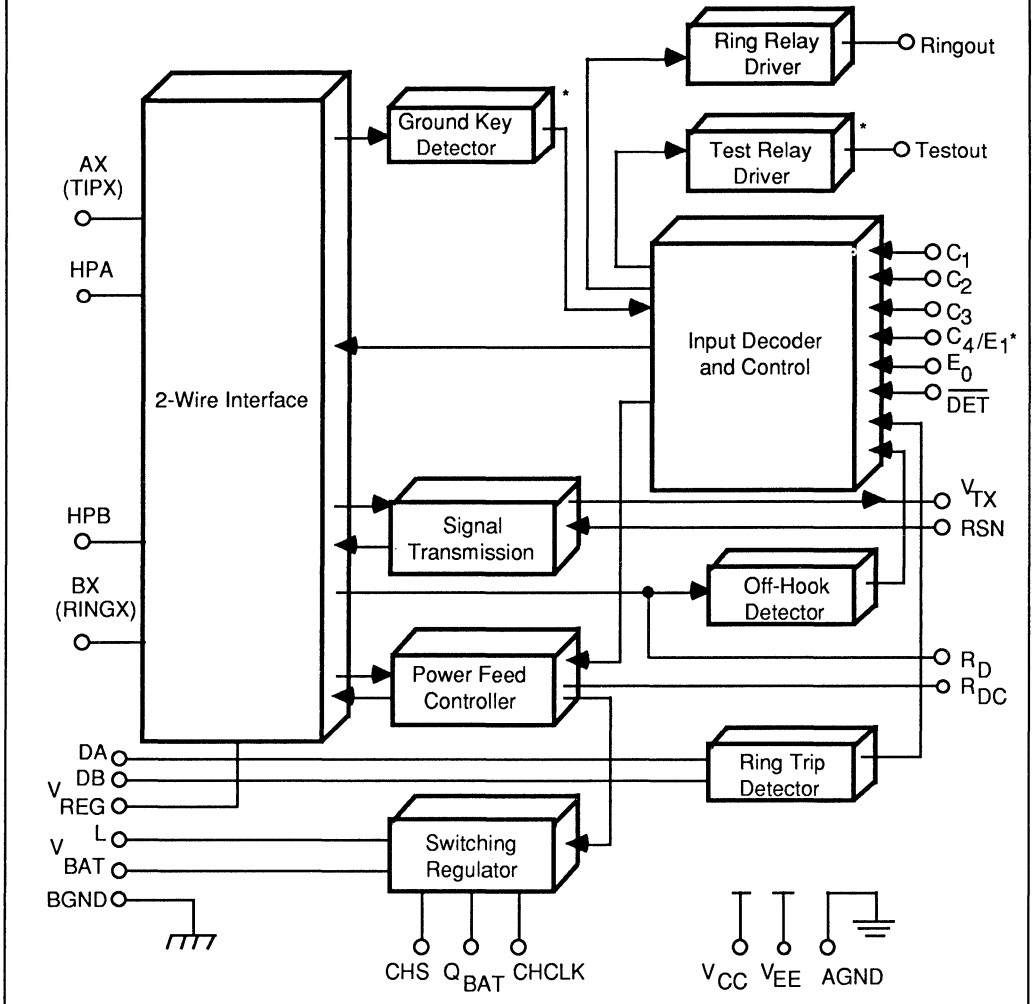
*BORSHT Functions:

–B attery feed
–O vervoltage protection
–R ing signal
–S upervision of Line
–H ybrid (two-wire to four-wire conversion)
–T est access

THE FIRST COMPLETE MONOLITHIC SLIC PERFORMS ALL BORSHT FUNCTIONS

Designed using high-voltage bipolar technology with precision thin-film resistors, Advanced Micro Devices' Am7953/7957 Subscriber Line Interface Circuits (SLICs) contain an innovative set of features, providing many benefits for system designers.

Along with improved system performance and special signalling functions, AMD's Am7953/7957 SLICs offer dramatic cost and power savings.



*May be included depending on functional configuration specified

Am7953X/7957X/79M53X/79M57X

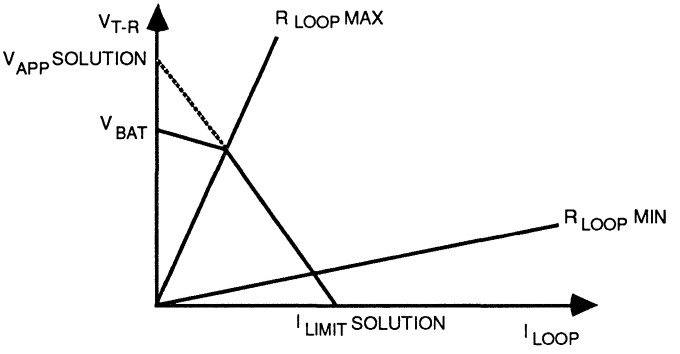
Subscriber Line Interface Circuit (SLIC)

NEW BATTERY FEED SYSTEM SOLVES POWER DISSIPATION PROBLEMS

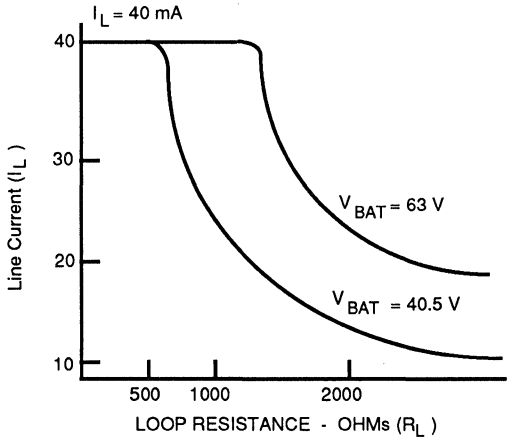
A patented new battery feed system allows users of AMD's Am7957 SLIC previously unattainable degrees of design flexibility and performance.

The Am7957 uses the DC loop current as a control variable in a feedback loop to establish a modified DC feed voltage *without excess power dissipation.* Now you can design resistive feed systems where the feed resistance is programmable and independent of the actual battery. This minimizes system power dissipation and keeps the loop current independent of the battery variations.

The Am7953 allows the DC feed current to be programmed with external resistors. The feed current is independent of battery variations and loop length.



Am7957 Line Feed Characteristics

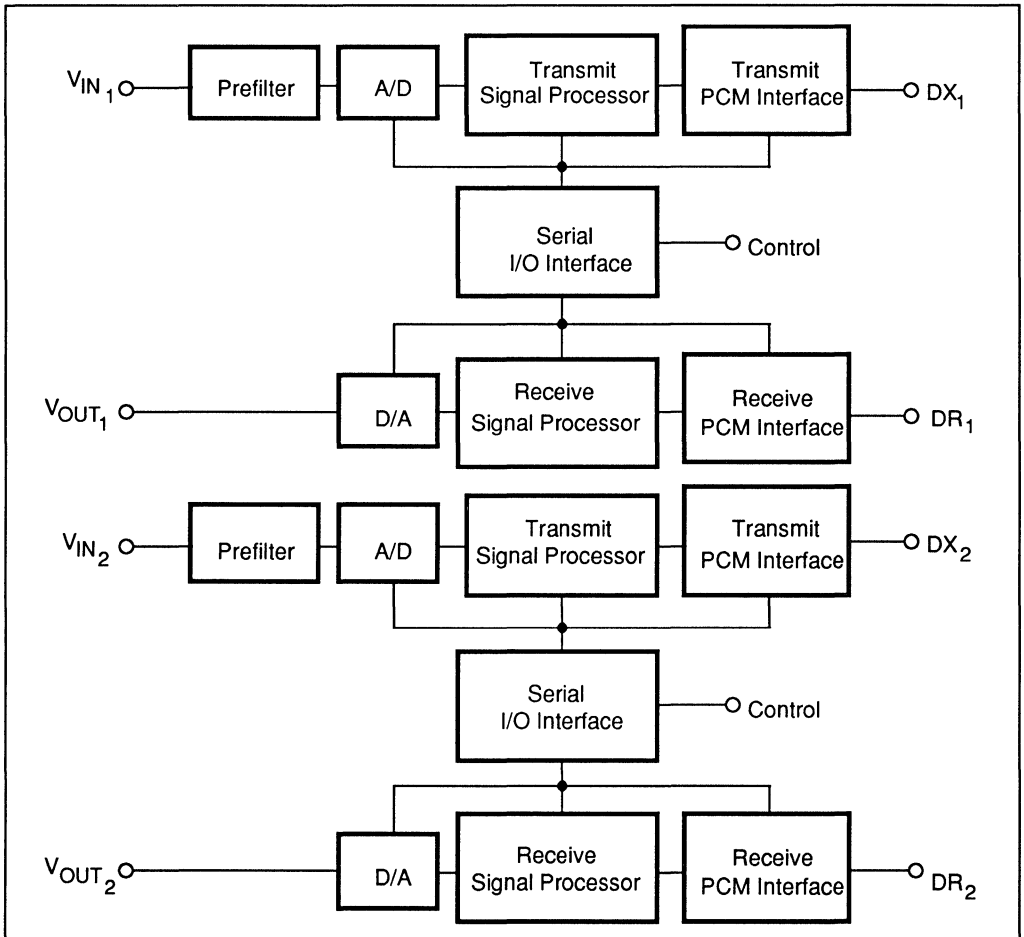


Am7953 Line Feed Characteristics

THE FIRST TELECOMMUNICATION CODEC/FILTER UTILIZING STATE-OF-THE-ART MICROPROCESSOR TECHNOLOGY TO SOLVE YOUR LINECARD PROBLEMS

Advanced Micro Devices' Am7901A/B and Am7905A Subscriber Line Audio-Processing Circuits (SLAC), designed using digital signal processing techniques, employ digital filters to provide many system advantages. Through application of advanced LSI technology, AMD has incorporated the codec/filter and other line-card functions into the SLAC. AMD's SLAC permits the digital switch designer to off-load some processing from other system processors to the linecard, and thus improve system efficiency while reducing cost.

No other approach to linecard design allows as much flexibility and reliability.



DSLAC Block Diagram

Final

Am7901B/C

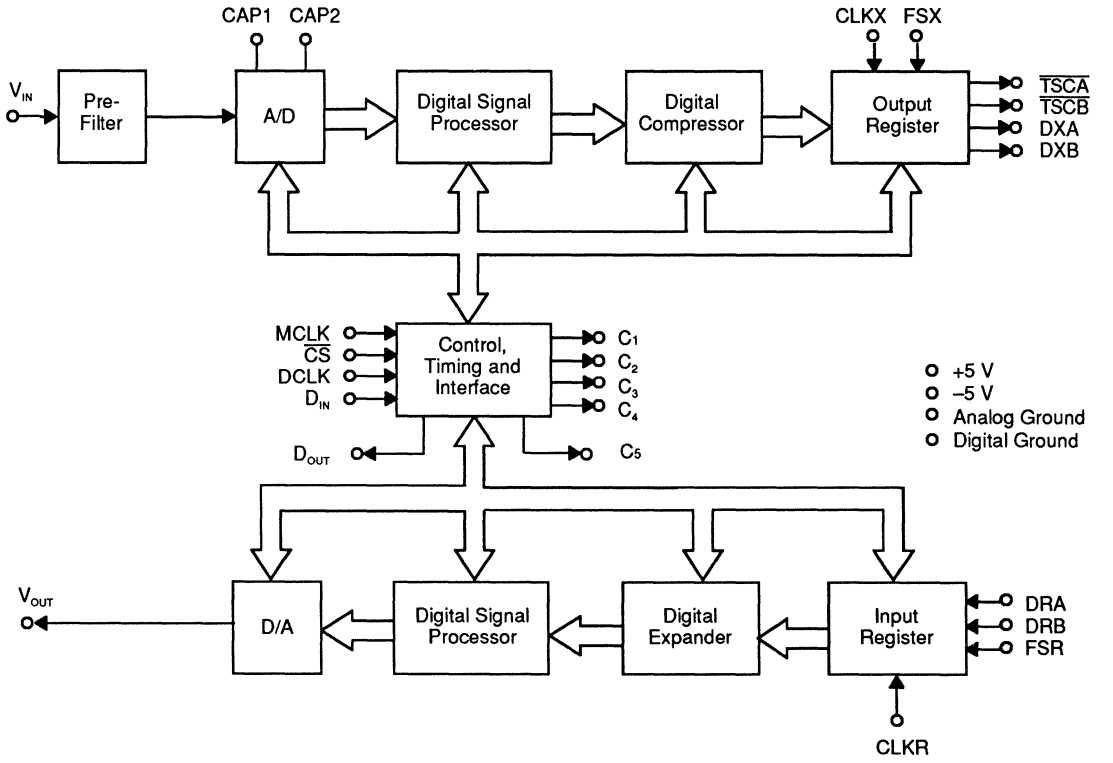
WORLD-CHIP® Subscriber Line Audio-Processing Circuit (SLAC™)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Combination CODEC and Filter
- No trimming or adjustments required
- Uses digital signal processing
- Six user-programmable digital filters
- Dynamic time slot assignment
- Only 2 external components (non-precision)
- Dual PCM ports
- 4.096 MHz, 64-channel expanded mode operation
- Built-in test modes
- Microprocessor-compatible Serial Interface
- Control interface to SLIC
- Low standby power
- Selectable μ-law, A-law (Am7901B) or linear, A-law (Am7901C)

BLOCK DIAGRAM



BD005381

Publication # 01520 Rev. Amendment /0
Issue Date: March 1989

GENERAL DESCRIPTION

The Subscriber Line Audio-Processing Circuit (SLAC) performs the codec and filtering functions necessary in digital voice switching machines. In this application, the SLAC processes voiceband analog signals into Pulse-Code Modulated (PCM) outputs and processes PCM inputs into analog outputs. The SLAC's performance is compatible with applicable AT&T and CCITT specifications. The device consists of three main sections: transmit processor, receive processor, and control logic.

The transmit section contains an anti-aliasing filter, an interpolative A/D converter and a digital signal processor. The analog signals received are converted and digitally processed to generate either 8-bit μ-law or A-law codes (Am7901B) or 16-bit linear or 8-bit A-law codes (Am7901C). Either one of two output ports may be selected for PCM data transmission.

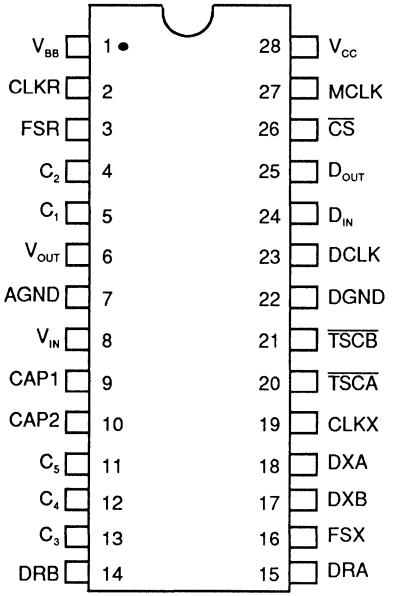
The receive section contains a digital signal processor and a D/A converter. Either 8-bit μ-law or A-law codes (Am7901B) or 16-bit linear or 8-bit A-law codes (Am7901C) are received, processed and converted to analog signals. Either one of two input ports may be selected for reception of PCM data.

The control I/O provides a microprocessor-compatible serial interface and allows the user bi-directional access to many programmable features as well as the capability to completely control the operation of the device via a comprehensive set of 32 commands.

CONNECTION DIAGRAMS

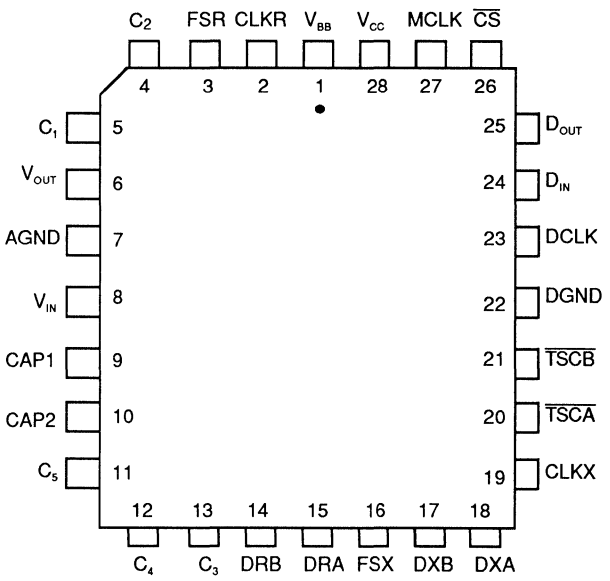
Top View

28-Pin DIP



CD007011

28-Pin PLCC



07004-002B

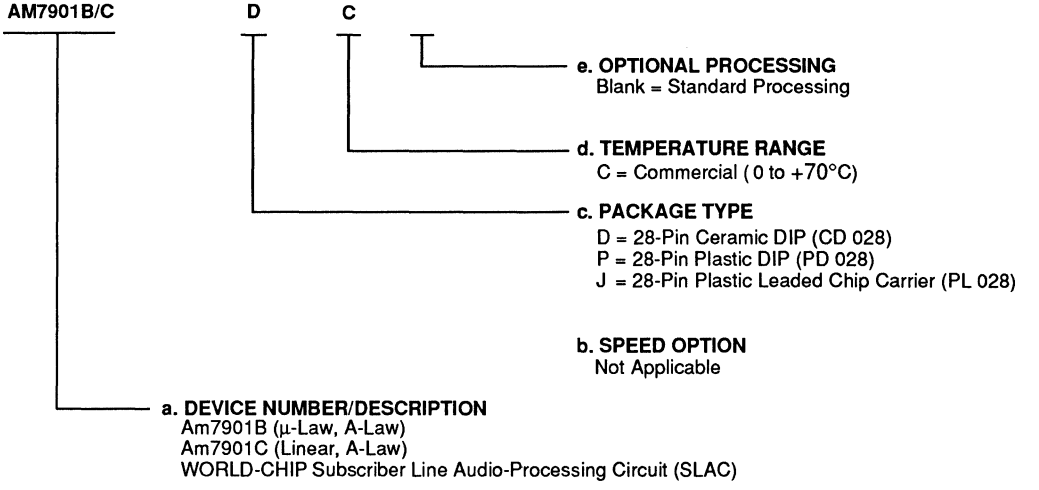
Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7901B	DC, PC, JC
AM7901C	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Am7905A

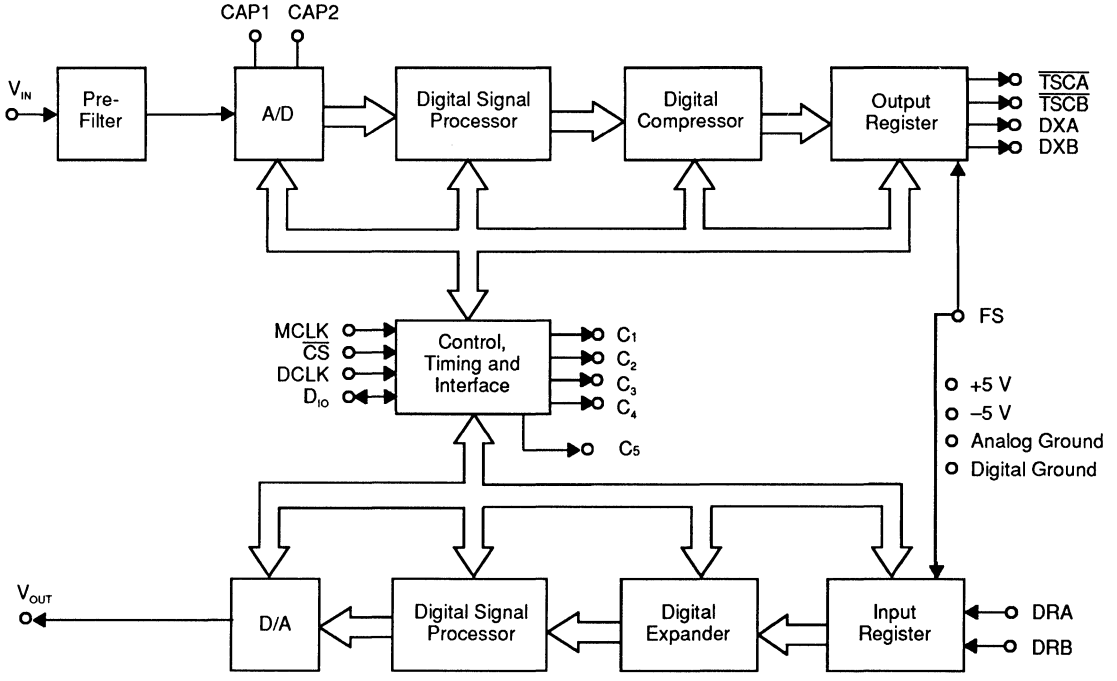
WORLD-CHIP™ Subscriber Line Audio-Processing Circuit (SLAC™) Devices

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Combination CODEC and Filter
- No trimming or adjustments required
- Uses digital signal processing
- Six user-programmable digital filters
- Dynamic Time Slot assignment
- Only 2 external components (non-precision)
- 4.096 MHz, 64-channel expanded mode operation
- Dual PCM ports
- Built-in test modes
- Microprocessor-compatible Serial Interface
- Control interface to SLIC
- Low standby power
- Selectable μ-law or A-law
- 24-pin DIP
  28-pin PLCC

BLOCK DIAGRAM



BD005381

Publication # 07004 Rev. Amendment /0
Issue Date: February 1989

GENERAL DESCRIPTION

The Subscriber Line Audio-Processing Circuit (SLAC) performs the codec and filtering functions necessary in digital voice switching machines. In this application, the SLAC processes voiceband analog signals into Pulse-Code Modulated (PCM) outputs and processes PCM inputs into analog outputs. The SLAC's performance is compatible with applicable AT&T and CCITT specifications. The device consists of three main sections: transmit processor, receive processor, and control logic.

The transmit section contains an anti-aliasing filter, an interpolative A/D converter and a digital signal processor. The analog signals received are converted and digitally processed to generate either 8-bit μ-law or A-law codes. Either one of two output ports may be selected for PCM data transmission.

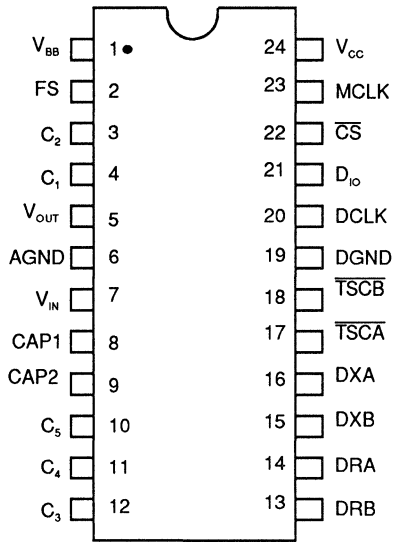
The receive section contains a digital signal processor and a D/A converter. Either 8-bit μ-law or A-law codes are received, processed and converted to analog signals. Either one of two input ports may be selected for reception of PCM data.

The control I/O provides a microprocessor-compatible serial interface and allows the user bi-directional access to many programmable features as well as the capability to completely control the operation of the device via a comprehensive set of 34 commands.

CONNECTION DIAGRAMS

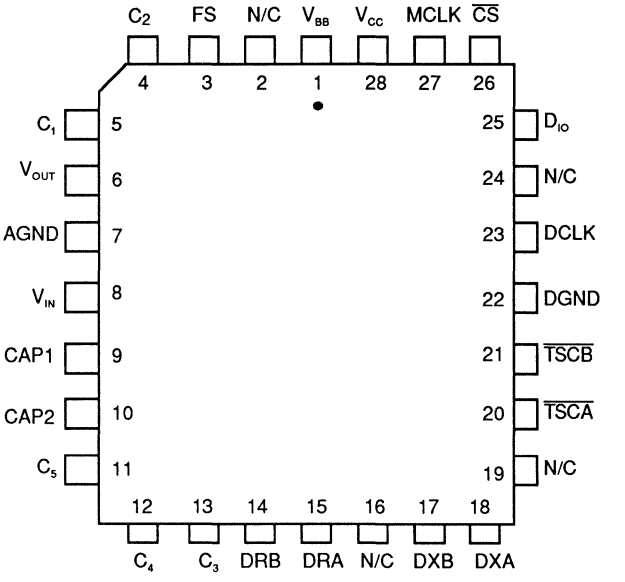
Top View

24-Pin DIP



CD007011

28-Pin PLCC



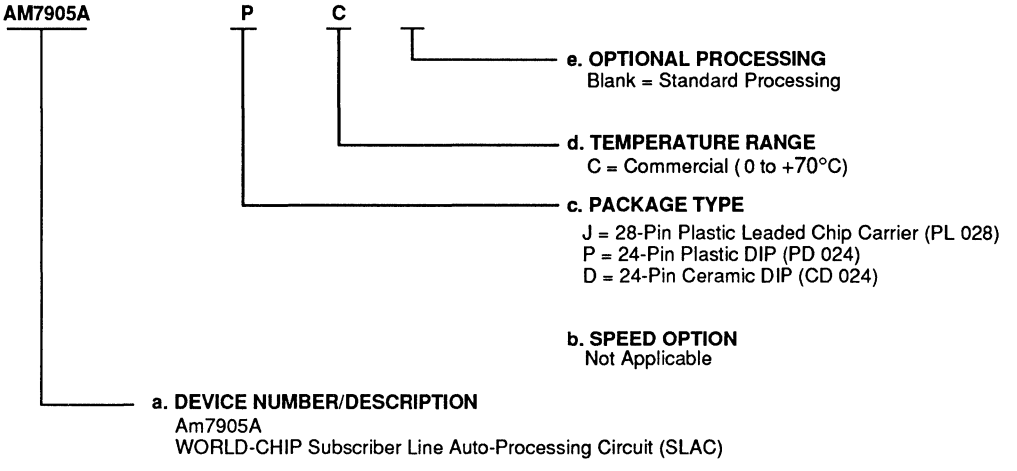
07004–002B

Note: Pin 1 is marked for orientation.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7905A	PC, DC, JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Am79C02/A

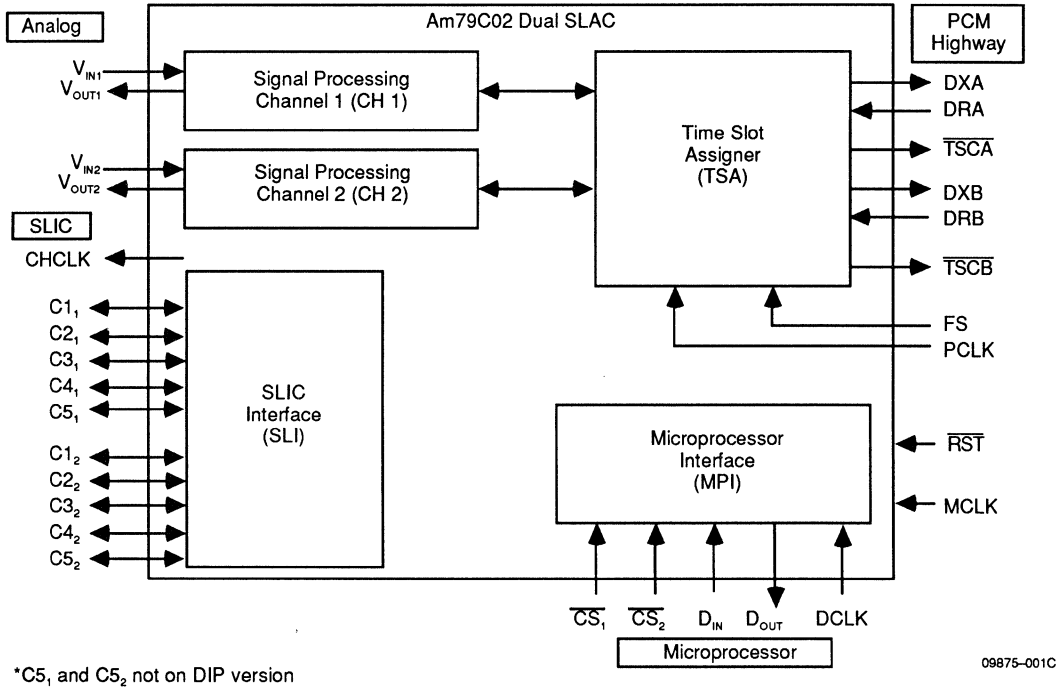
Dual Subscriber Line Audio-Processing Circuit (DSLAC™)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Software programmable:
  - –SLIC impedance
  - –Trans-hybrid balance
  - –Transmit and Receive gains
  - –Equalization
  - –Digital I/O pins
  - –Time Slot Assigner
- Adapt and freeze or fixed trans-hybrid balance filter (Am79C02 and Am79C02A)
- Continuously adapting trans-hybrid balance filter (Am79C02A only)
- A-law or μ-law coding
- Dual PCM ports
  - –Up to 8.192 MHz (128 channels per port) through the PCM interface
- 2.048 MHz or 4.096 MHz master clock
- Direct Transformer Drive
- Built-in test modes
- Low power CMOS
- Mixed mode (analog and digital) impedance scaling

BLOCK DIAGRAM



*$C5_1$ and $C5_2$ not on DIP version

09875-001C

Publication # 09875 Rev. Amendment /0
Issue Date: April 1989

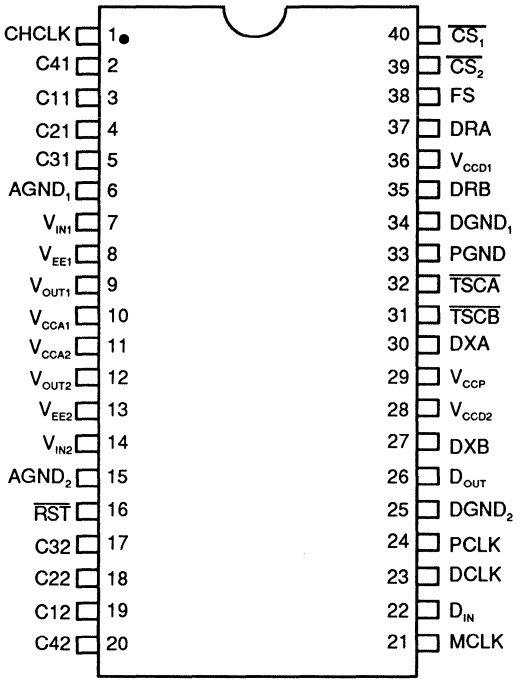
GENERAL DESCRIPTION

The Am79C02/A Dual Subscriber Line Audio-Processing Circuit (DSLAC) integrates the key functions of an analog linecard into one programmable, high-performance dual CODEC-filter device. The DSLAC is based on the proven design of the reliable Am7901A Subscriber Line Audio-Processing Circuit (SLAC™). The advanced architecture of the DSLAC implements two independent channels and employs digital filters to allow software control of transmission, thus providing a cost-effective solution for the four-wire-to-PCM section of a linecard.

Advanced CMOS technology makes the Am79C02/A DSLAC an economical device that has both the functionality and the low power consumption needed by linecard designers to maximize linecard density at minimum cost. When used with two SLICs, the DSLAC provides a complete, software-configurable solution to the BORSCHT function.

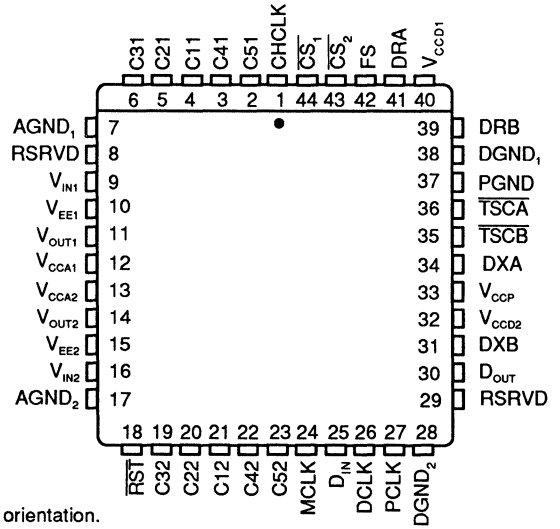
CONNECTION DIAGRAMS
Top View

40-Pin DIP



09875-002C

44-Pin PLCC



Notes: 1. Pin 1 is marked for orientation.
2. RSRVD = No connection

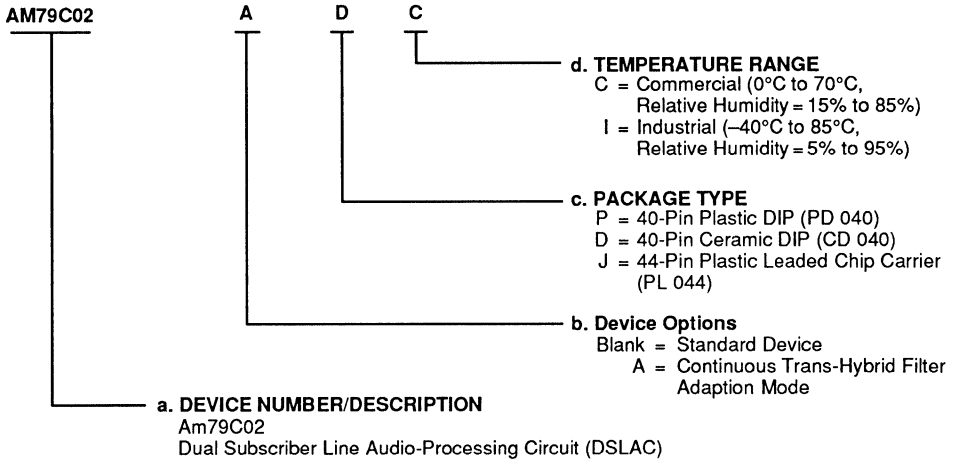
09875-003C

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range



Valid Combinations			
AM79C02	ADC	APC	AJC
	ADI	API	AJI
	DC	PC	JC
	DI	PI	JI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Preliminary

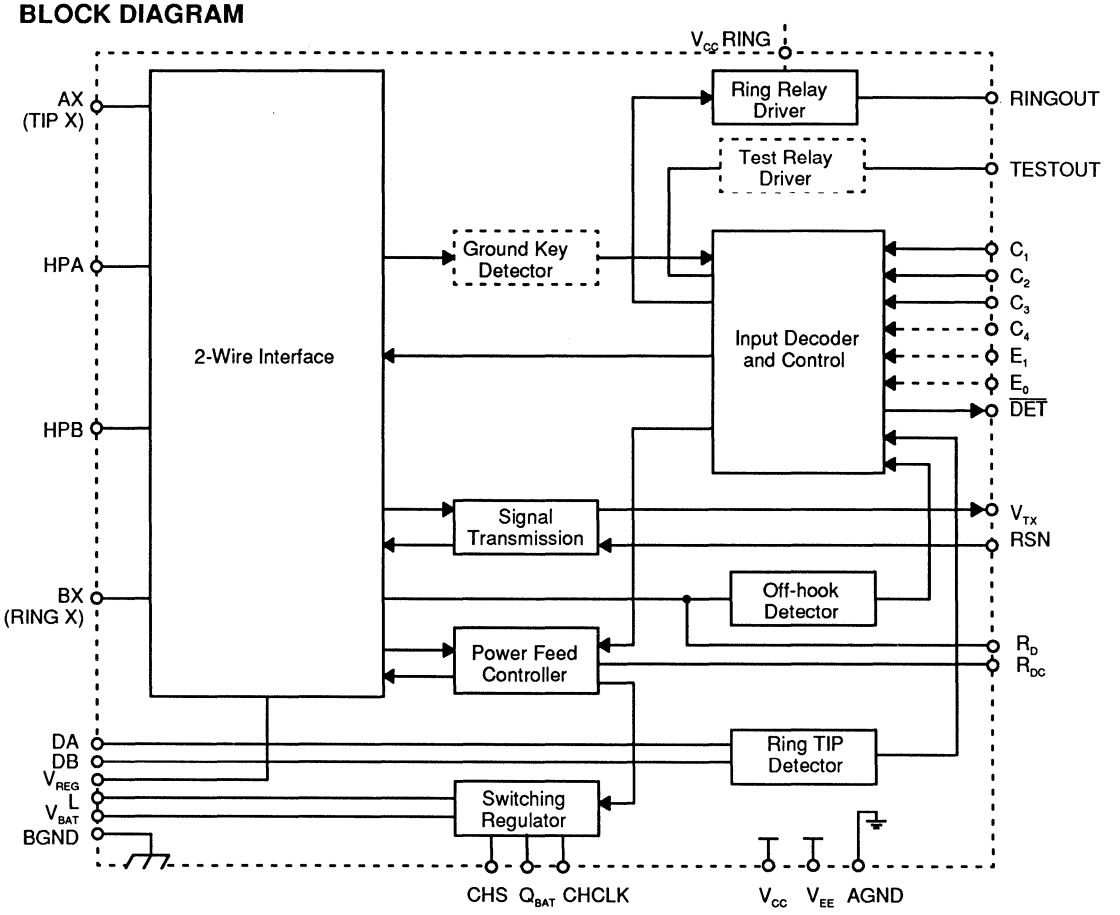
Am7953/Am7957
Am79M53/Am79M57
Subscriber Line Interface Circuit Family (SLIC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Programmable constant current or constant resistance feed versions
- Line feed characteristics independent of battery variations
- Programmable loop detect threshold
- On chip switching regulator for low active power dissipation
- Ground key detect option available
- Low standby power
- Am79M53/M57 versions support 2.2 VRMS metering (12 and 16 kHz)
- Two-wire impedance set by single external impedance
- Performs polarity reversal
- Various Ring and Test relay driver combinations available
- Tip open state for ground start lines

BLOCK DIAGRAM



Publication #11701 Rev. Amendment /0
Issue Date: March 1989

GENERAL DESCRIPTION

The Am7953/57 and Am79M53/57 family of Subscriber Line Interface Circuits (SLIC) perform the telephone line interface functions required in both Central Office and PABX environments. The full range of signal transmission, battery feed and loop supervision functions are performed. Signal transmission performance is compatible with North American and CCITT recommendations.

The signal transmission functions include both 2- to 4-wire and 4- to 2-wire conversion. The 2-wire termination impedance is programmable with a single external impedance. The companion AMD SLAC™ (Subscriber Line Audio Processing Circuit) has a digital balancing filter that provides the trans-hybrid loss function. If the SLAC is not used, most codec/filter sets provide an uncommitted op amp for this purpose.

The battery feed architecture makes the DC feed characteristics programmable with external resistors. Furthermore, these characteristics are independent of battery variations. The output amplifiers are powered by an internal, self-adjusting switching regulator to reduce power consumption to a minimum.

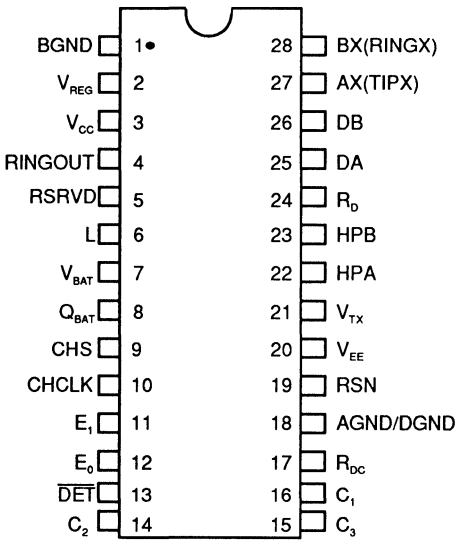
A polarity reversal function is provided which transposes the normal voltage sense of the A(Tip) and B(Ring) leads with a controlled transition time. All transmission functions continue normally following the transition. A disable mode limits loop current and cuts power dissipation while allowing the full complement of supervisory functions to be utilized.

The supervisory functions of off-hook detection and ring trip detection are read through a single, TTL compatible output. To eliminate noise induced errors, the off-hook detector signal may be filtered. Off-hook detection has a threshold that is adjusted by means of external components. Additional supervisory functions put the A lead into an open circuit or high impedance state suitable for application in ground start systems. Similarly, both the A and B leads may be open circuited to clear relays, recover from line faults, or turn off out-of-service lines. Depending on chip type, up to two relay drivers provide ring and test relay functions. The Am79M53/M57 versions can handle 12 and 16 kHz metering in addition to voice.

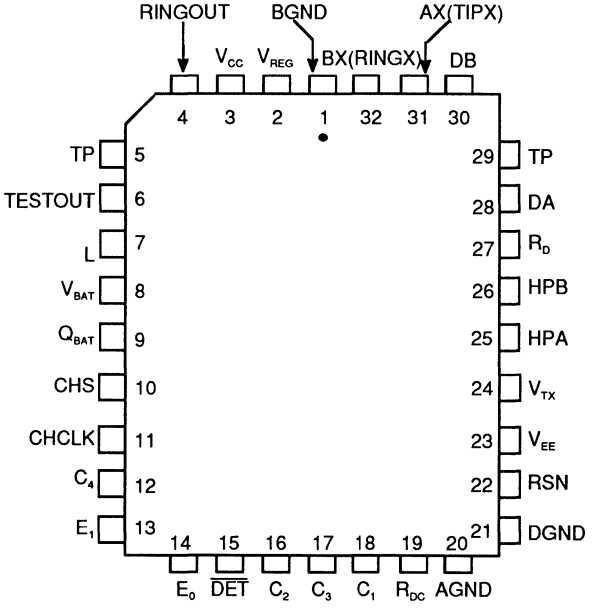
The SLIC's user programmable states are controlled by a TTL compatible code. These control inputs are designed to easily interface to popular single chip microcomputers such as the AMD Am8051 or to latched outputs from a SLAC or other processing circuit.

CONNECTION DIAGRAMS

28-Pin DIP



32-Pin PLCC



Notes: 1. Pin 1 is marked for orientation.
2. TP is a thermal conduction pin tied to substrate.
3. Pinouts will vary depending on bonding option selected. See Data Sheet for details.

PRODUCT SELECTION GUIDE

SLIC Types

There are four basic types of SLIC:

1. The Am7953 series with constant current feed
2. The Am7957 series with constant resistance feed
3. The Am79M53 series with constant current feed and metering capability
4. The Am79M57 series with constant resistance feed and metering capability

Bond-out Options

The Am7953 and Am7957 series both have four potential bond-out configurations as indicated by a fifth digit (n) in the part number (refer to the selection chart). The metering versions also have these potential bond-out configurations plus an additional configuration indicated by the absence of a fifth digit (not including the "M"). These options are as follows:

- No fifth digit (metering versions only); Am79M53 indicates that E_0 and E_1 functions (DET enable and DET ground key select) are present together with one relay driver (ring) whose collector and emitter are output to pins.
- n = 1; Am79571 indicates that both E_0 and E_1 functions are present together with one relay driver (ring) whose emitter is output to a pin and whose collector is internally sourced from V_{CC}.
- n = 2; Am79532 indicates that the E_1 function (DET ground key select) is present together with two relay drivers (ring and test) whose emitters are output to pins and whose collectors are internally sourced from V_{CC}.
- n = 3; Am79573 indicates that the E_0 function (DET enable) is present together with two relay drivers (ring and test) whose emitters are output to pins and whose collectors are internally sourced from V_{CC}.
- n = 4; Am79534 indicates that both E_0 and E_1 functions are present together with two relay drivers (ring and test) whose emitters are output to a pin and whose collectors are internally sourced from V_{CC}. This version is only available in 32-pin PLCC.

All of these SLIC versions are potentially available but not all are presently in production. Versions that are presently in production are indicated in the following chart. If you are interested in a bond-out configuration that is not indicated to be in production, please contact AMD's Communication Products Division or your local AMD sales office.

Selector Chart

Possible SLIC Products

Notes: 1. n = Bonding option designator
2. x = No designator

	Am7953n			Am7957n			Am79M53n		Am79M57n		
	n			n			n		n		
	1	2	4	1	3	4	1	4	x	1	4
Constant current feed	•	•	•				•	•			
Constant resistance feed				•	•	•			•	•	•
Metering capability							•	•	•	•	•
DET enable bit, E_0	•		•	•	•	•	•	•	•	•	•
DET GND key select bit, E_1	•	•	•	•		•	•	•	•	•	•
Ring relay driver	•	•	•	•	•	•	•	•		•	•
Ring relay driver*									•		
Test relay driver		•	•		•	•		•			•
28-pin dip	•	•		•	•		•		•	•	
32-pin PLCC			•			•		•			•

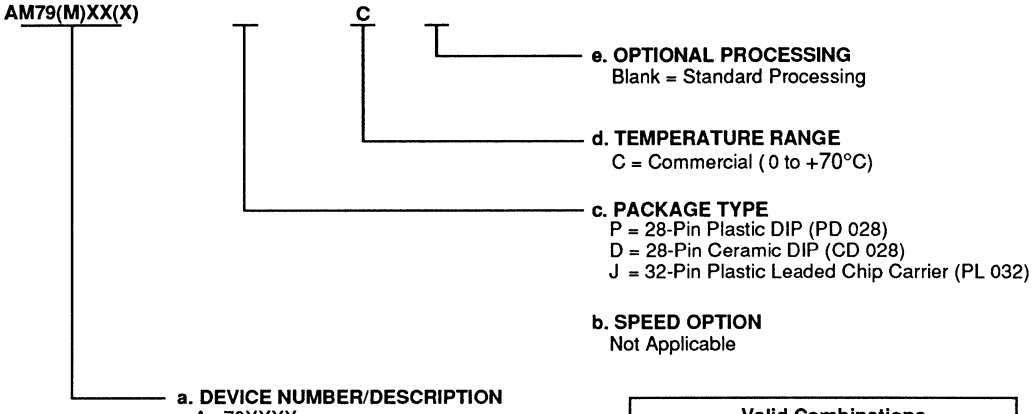
* Collector and emitter ouput to pins

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Valid Combinations	
AM79531	PC,DC
AM79532	PC,DC
AM79534	JC
AM79571	PC,DC
AM79572	PC,DC
AM79574	JC
AM79M53	PC,DC,JC
AM79M531	PC,DC
AM79M534	JC
AM79M57	PC,DC,JC
AM79M571	PC,DC
AM79M574	JC

VOICE SWITCHING PRODUCTS

Support Tools

VOICE SWITCHING EVALUATION SYSTEM

AMD's SLIC/SLAC/DSLAC Evaluation Boards provide ready-made hardware tools to create either a linecard environment or a stand-alone test fixture for the Am79XX family of SLIC/SLAC/DSLAC devices.

Two complete Evaluation Board KITs are available or boards can be purchased separately.

OPN	DESCRIPTION
Am79PROGKIT	**SLIC/SLAC Evaluation Board Kit**
• Am79CIFBD	SLAC/DSLAC Computer Interface Board
• Am79SLICBD	SLIC Evaluation Board
• Am79SLACBD	SLAC Low-Noise

OPN	DESCRIPTION
Am79PROGKIT/D	**SLIC/DSLAC Evaluation Board Kit**
• Am79CIFBD	SLAC/DSLAC Computer Interface Board
• Am79SLICBD	SLIC Evaluation Board
• Am79DSLACBD	DSLAC Low-Noise Evaluation Board

In addition to the above boards, each KIT includes the following:

- Diskette #1 and #2–Computer Interface Board Software Driver
- Diskette #3 –PC AmSLAC or PC AmSLAC II Program (see description next page)
- Technical Manuals
- Cables

Am79SLICBD—SLIC Evaluation Board

The SLIC Evalution Board provides a ready-made test setup for evaluating the performance of Am795X-Series Subscriber Line Interface Circuits. It includes a 256 kHz on-board clock to activate the switching regulator in the SLIC. The four-wire receive gain, the two-wire terminating impedance and the D.C. feed characteristics of the SLIC can be programmed by connecting appropriate impedances across binding posts fastened to the evaluation board. The four-wire analog interface is made available through BNC connectors. The two-wire port includes a protection circuitry and a means to provide the necessary ring voltage to the subscriber. This board requires a –48 V and a ±5 V power supply.

Am79CIFBD—SLAC/DSLAC Computer Interface Board

The SLAC/DSLAC Computer Interface Board provides a friendly, PC-driven interface to control up to two SLAC Low-Noise Boards or DSLAC Low-Noise Boards. The Interface Board will also attach to a PCM-channel measuring set (either a Hewlett-Packard PMA or a W&G PCM-4) to facilitate performance measurements on the SLAC or DSLAC. Resident on the PC, the software program DSLACIF, provides an easy-to-use interface for controlling the entire setup.

Am79SLACBD—SLAC Low-Noise Evaluation Board

The SLAC Low-Noise Evaluation Board provides a ready-made stand-alone test setup for the Am7901 Subscriber Line Audio Processing Circuit. A 2.048 MHz on-board clock generator supports the timing requirements of the SLAC. A pair of BNC connectors provide convenient access to the analog input and output terminals of the SLAC. Also, this board may be connected to the SLAC/DSLAC Computer Interface Board to allow the SLAC to be programmed from a Personal Computer.

Am79DSLACBD—DSLAC Low-Noise Evaluation Board

The DSLAC Low-Noise Evaluation Board is designed to demonstrate the high-performance capabilities of the DSLAC (40-pin DIP). It is designed to interface to the SLAC/DSLAC Computer Interface Board through a DB37S connector. Both boards may be placed adjacent to each other on a lab table and plugged together directly, without a connecting cable. It can also interface to two SLIC Evaluation Boards through 20-pin header connectors.

AmSLAC™ and AmSLAC II™

SLAC/DSLAC COEFFICIENT DEVELOPMENT SOFTWARE

AmSLAC and AmSLAC II software is intended to provide the user with the coefficients needed to configure the SLAC (AmSLAC) and DSLAC (AmSLAC II) for optimal performance with respect to any given set of line card specifications. Line cards using either AMD's Am7953/57 SLICs or transformer based SLICs are supported. Inputs to the menu-driven program include such parameters as line impedance, SLIC impedance, fuse resistance, minimum two-wire return loss, minimum four-wire return loss, and so on.

The AmSLAC manual provides details of the software installation, the user interface, SLAC/DSLAC design considerations, and practical design examples using various types of SLICs. The manual also provides general information on the definition of transmission parameters commonly used in the design of line cards, characterization of transformer SLICs, and measurement techniques using AMD's SLIC/SLAC/DSLAC Evaluation Boards.

AmSLAC and AmSLAC II software is available in both VAX and IBM PC or compatible versions. It is highly recommended that the PC version be used only with a PC equipped with a math co-processor to speed the execution of the program.

NETWORKING PRODUCTS

NETWORKING SYSTEM OVERVIEW

Within the World Network are many Local Area Networks. Standards such as FDDI, StarLAN and Ethernet allow multiple user's to share computing power and applications. These networks use twisted pair, coax or fiber optic cable to link equipment. Also included in the World Network is the TAXIchip™ set, which consists of a Transmitter and Receiver chip and functions as a general-purpose interface for very high-speed point-to-point communications over coaxial or fiber-optic media. These products and plans for future ones continue to show our commitment to networking.

TAXI

The Transparent Asynchronous XCVR Interface (TAXI) is a point-to-point communications link for building high-speed data channels. Operating with data rates up to 100 Mbps, TAXI is 10 times faster than conventional RS-422 line drivers and receivers, the fastest point-to-point communications standard today.

For high-speed applications, no other vendor offers an integrated communications solution with the features of our TAXIchip set. It operates much like a single parallel latch: data is loaded into one side and read from the other, except that the second side is separated by a long serial link. With the TAXIchip set, you choose the interface best suited for your equipment: direct coaxial cable interface or fiber optic cable.

TAXI allows a simple, easy to install interface to fiber optics. It replaces bulky and expensive parallel ribbon cables with a single serial cable. This results in a reliable point-to-point link with increased system throughput.

Am7968, Am7969 TAXIchip Set
AmTAXIEVAL1 Evaluation Board

- Parallel to serial conversion at a 100 Mbps maximum data rate
- Efficient encoding combines clock and data, with no clock skew problems
- Easy interface to fiber optics and coax
- Cascadable to accommodate any bus width

ETHERNET

Designed for office and automated factory systems where short data paths are common, Ethernet's flexible addressing schemes and ease of reconfiguration allow you to build a reliable, low-cost network. Ethernet is a 10 Mbps packet-switched, digital data system for local area communications. Central controllers are not required and each node has direct access to the network.

There are more Ethernet nodes using AMD chip sets than any other manufacturer. AMD as a primary IC manufacturer in the Ethernet market, became the first manufacturer to provide a complete Ethernet solution in 1985.

The Am7990 chip-set is a total hardware solution for Ethernet implementation. The three chips were designed to work together, so you don't waste time looking for other parts or trying to fit pieces together. This chip-set optimizes performance and ensures compatibility between components of the Ethernet system.

AMD is continuing its long-term commitment to Ethernet by developing a second generation Ethernet controller. The Am79C900 Integrated Local Area Communications Controller™ (ILACC) chip will essentially combine today's Am7990 and Am7992 into one chip, optimized for 16- and 32-bit systems. This CMOS device will offer better performance at a lower cost.

A PC/AT-compatible LAN demonstration board is available that illustrates a low-cost Ethernet design for an IBM PC/AT. To further support Ethernet designs, Novell-certified drivers for Novell NetWare are available, as well as interfaces to the OSI model Transport and Data Link layers.

Am7990, Am7992B, Am7996, Am79C900
ETHNEVAL5, Am7996EVAL Evaluation Boards

- On-board DMA and buffer management, 48 byte FIFO
- 24-bit wide linear addressing
- Network and packet error reporting
- Diagnostic routines, including internal/external loopback, CRC logic check, and time domain reflectometer

StarLAN

As an internationally recognized standard 1 Mbps network. StarLAN is often used for microcomputer applications. It employs standard twisted-pair telephone wire to connect intelligent devices. The ability to use previously-installed telephone wire makes StarLAN an important tool for inexpensive connections.

The Am7961 StarLAN Coded Data Transceiver is a combined Manchester encoder/decoder and high performance tranceiver. It can be used with most standard Ethernet controllers to build a StarLAN node.

Am7961 StarLAN

- Single-chip transceiver
- Direct interface to most Ethernet controller chips
- Digital receiver noise filter
- Optional fault detection modes, including loopback testing.

Coded Data Transceiver

The Am7960 Coded Data Transceiver allows you to make systems trade-offs to optimize your network. It allows the choice of a protocol, controller, size and topology best suited for your networking applications.

The Am7960 is a combined Manchester encoder/decoder and transceiver designed to maximize value and flexibility in low-speed (up to 3 Mbps) networking applications.

Am7960 Coded Data Transceiver

- Protocol transparent
- "Modem-like" controller interface
- Drives coax or twisted pair

FDDI

Fiber Distributed Data Interface (FDDI) is a new 100 Mbps fiber optic LAN standard approved by ANSI and ISO. It consists of two parallel rings of optical fiber and can connect up to 500 nodes with a ring circumference of up to 100 kilometers. The primary ring is used for data transmission. The secondary ring can also be used for data transmission or may serve as a backup ring.

The SUPERNET™ chip-set is the first commercially available integrated FDDI implementation. It is a complete system solution, employing a mixture of state-of-the-art bipolar and CMOS technologies. Bipolar technology is used for the 125 MHz transmit and receive functions while CMOS is used for the controller and memory management functions. AMD also has the fast, flexible system interface required to use the full FDDI network potential. SUPERNET supports a wide variety of system architectures, from simple to very high performance.

An IBM PC/AT-compatible evaluation board is easily configured to implement any kind of FDDI node, including wiring concentrators. The board will run FDDIMON, a monitor program for exercising the SUPERNET chip-set; FDDINET, a MAC driver and Station Management program; and FDDIDEMO, a menu-driven demo package which is intended to be used with FDDINET. Also available is FDDI CMT Emulator, a program that demonstrates and verifies CMT algorithms.

Am79C81A, Am79C82A, Am79C83, Am7984A, Am7985A SUPERNET Chip-Set AmFDDI-PC-AT Evaluation Board

- Compliant with proposed ANSI X3T9.5 specification including:
  - –100 Mbps data rate
  - –fiber optic transmission media
  - –ring topology
  - –timed token-passing protocol
- Multiple loopback modes for run-time diagnostics
- Supports 256K bytes of local frame buffer memory
- Supports up to 200 Mbps dual-port memory access

NETWORKING PRODUCTS

Point-to-Point Communications

Am7968/Am7969

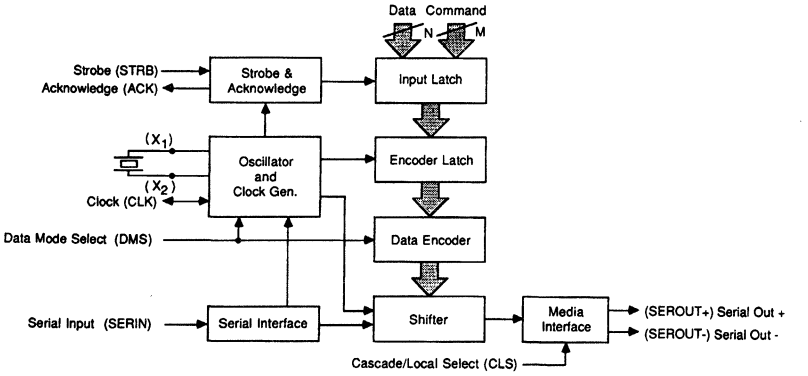
TAXIchip™ Integrated Circuits
(Transparent Asynchronous Xmitter – Receiver Interface
PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Parallel TTL bus interface
  - Eight Data and four Command Pins
  - or nine Data and three Command Pins
  - or ten Data and two Command Pins
- Transparent synchronous serial link
  - +5 V ECL Serial I/O
  - AC or DC coupled
  - NRZI 4B/5B, 5B/6B encoding/decoding
- Drive coaxial cable directly or interface with fiber optic data links
- 32-100 Mbps (4-12.5 Mbytes/sec) data throughput
- Asynchronous input using STRB/ACK
- Automatic MUX/DEMUX of Data and Command
- Cascadable for longer patterns
- Complete on-chip PLL, Crystal Oscillator
- Single +5-V supply operation
- 28-pin PLCC, LCC or DIP

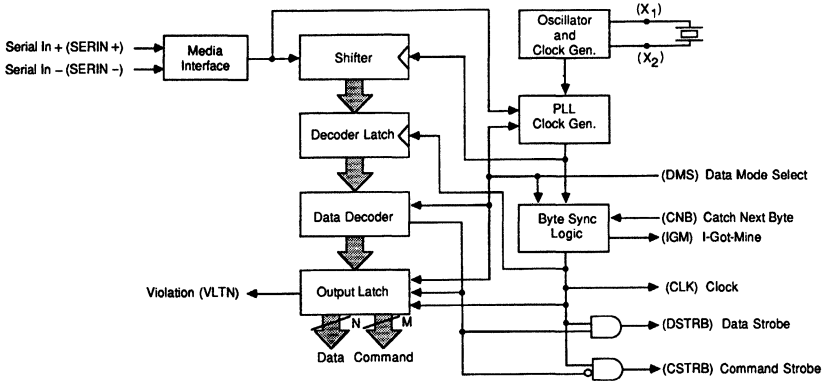
BLOCK DIAGRAMS

Am7968 TAXIchip Transmitter



BD007281

Am7969 TAXIchip Receiver



BD007291

Note: N can be 8, 9, or 10 bits
Total of N + M = 12

TAXIchip is a trademark of Advanced Micro Devices

GENERAL DESCRIPTION

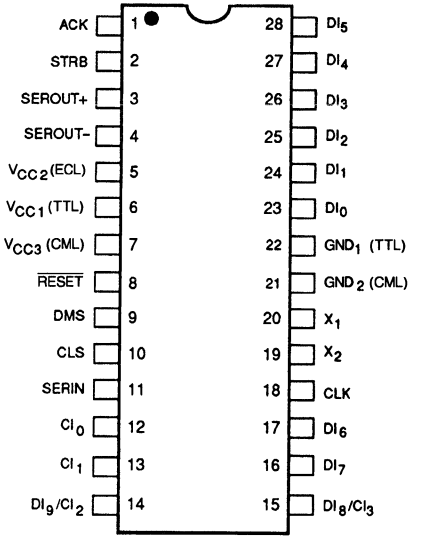
The Am7968 TAXIchip Transmitter and Am7969 TAXIchip Receiver Chipset is a general-purpose interface for very high-speed (4-12.5 Mbytes/sec, 40-125 Mbaud serially) point-to-point communications over coaxial or fiber-optic media. TAXIs emulate a pseudo-parallel register. They load data into one side and output it on the other, except in this case, the "other" side is separated by a long serial link.

The speed of a TAXIchip system is adjustable over a range of frequencies, with parallel bus transfer rates of 4 Mbytes/sec at the low end, and up to 12.5 Mbytes/sec at the high end. The TAXIchip's flexible bus interface scheme accepts bytes that are either 8, 9, or 10 bits wide. Multiple TAXIs can also be cascaded to accomodate a wider data bus. Byte transfers can be Data or Command signalling.

CONNECTION DIAGRAMS
Top View

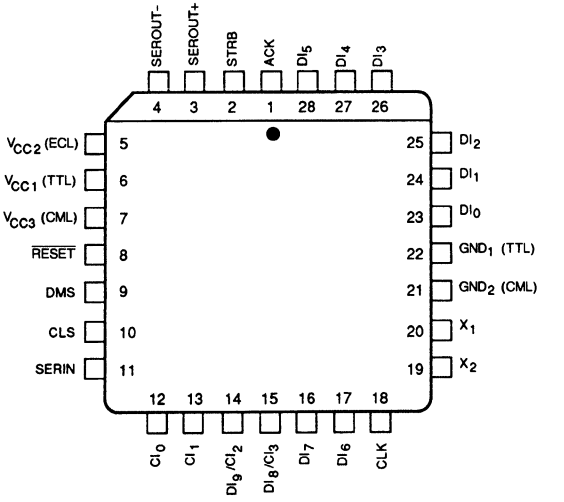
Am7968

DIPs



CD010772

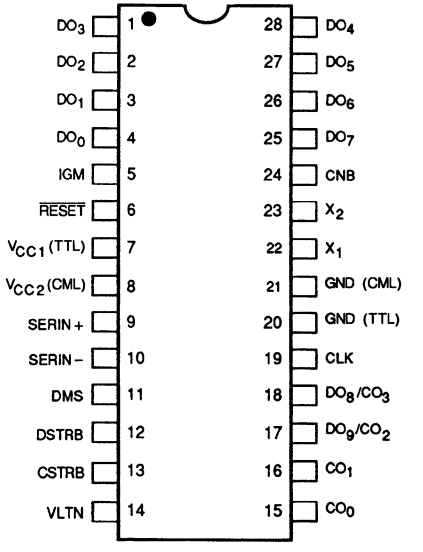
PLCC*



CD010782

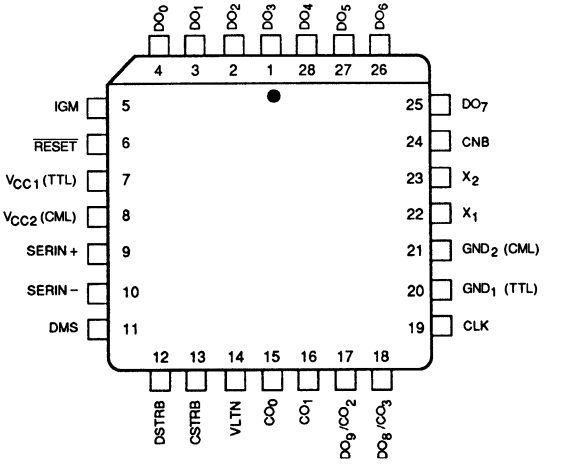
Am7969

DIPs



CD010792

PLCC*

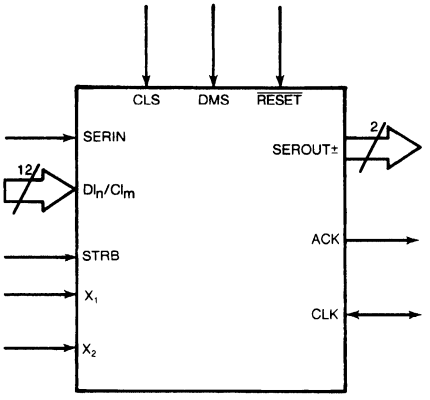


CD010802

Note: Pin 1 is marked for orientation.
* Also available in 28-Pin Ceramic Leadless Chip Carrier; pinout identical to PLCC.

LOGIC SYMBOLS

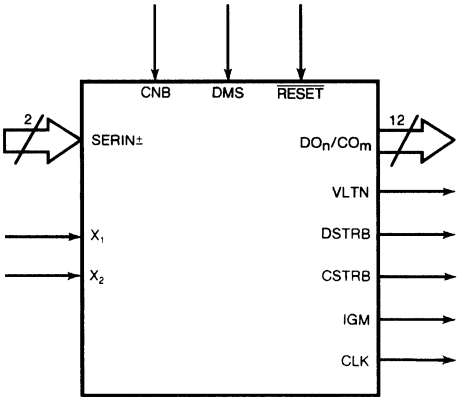
Am7968



LS002051

V_{CC} = Power Supply (3)
GND = Ground (2)

Am7969



LS002062

V_{CC} = Power Supply (2)
GND = Ground (2)

ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

AM7968 −125 D C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
P = 28-Pin Plastic DIP (PD 028)
D = 28-Pin Ceramic DIP (CD 028)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

b. SPEED OPTION
−125 = Max. Encoded Serial Data Rate is 125 Mbps

a. DEVICE NUMBER/DESCRIPTION
Am7968 TAXIchip Transmitter (Local Mode only)
AM7968C TAXIchip Transmitter (Local and Cascade Mode)
AM7969 TAXIchip Receiver

Valid Combinations	
AM7968-125	PC, PCB, DC, DCB, JC
AM7969-125	
AM7968C-125	PC, DC, JC

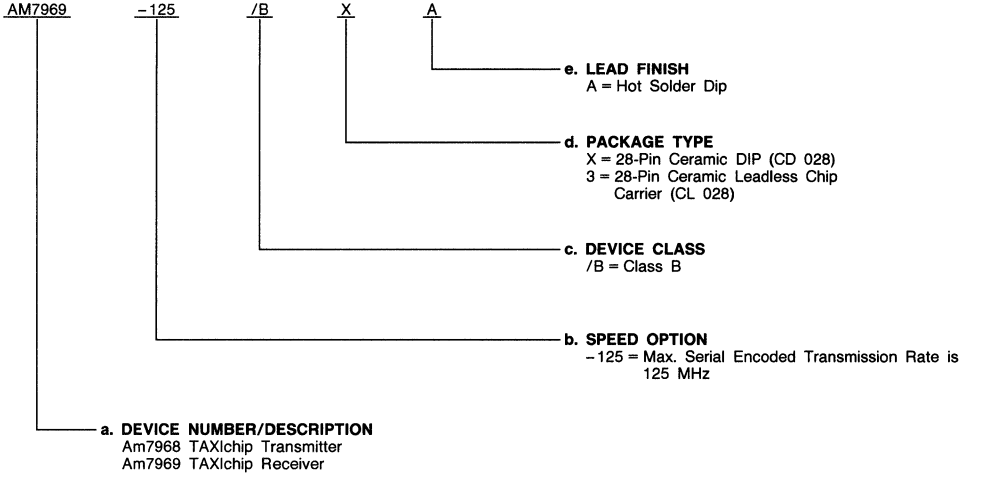
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM7968-125	/BXA, /B3A
AM7969-125	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consists of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

NETWORKING PRODUCTS

Local Area Network Products

Am7960

Coded Data Transceiver

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Universal Networking Transceiver
- High impedance interface to coupling transformer
  - User transparent Manchester encoding/decoding
  - Glitch-free power up/down
- "Modem-like" controller interface
- 32 dB dynamic range (transmit to receive)
- Transmit edge rate control
- Up to 3 Mbps data rate

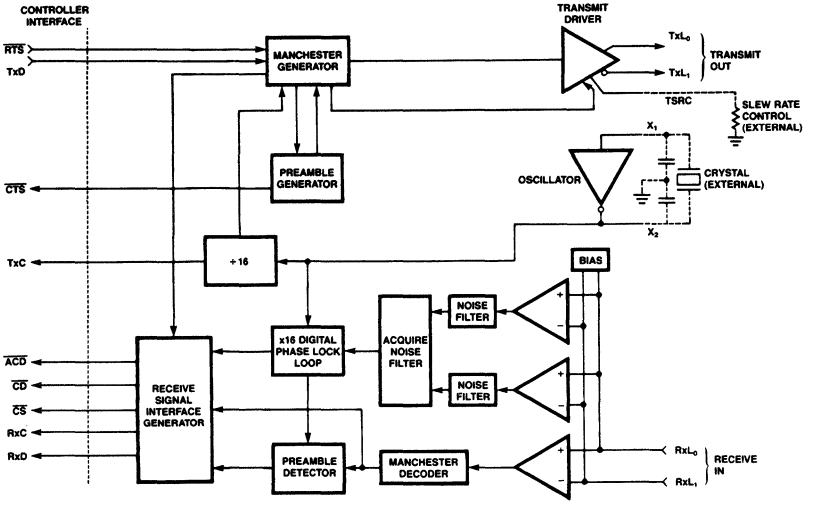
GENERAL DESCRIPTION

The Am7960 is a combined Manchester encoder/decoder and transceiver. It is designed for use in synchronous communications systems which require common mode isolation in point-to-point or common bus architecture, supporting data rates of up to 3 Mbps. This 5 V device provides 32 dB of dynamic range, and guarantees 2 V output into 37.5 Ω. A single external component controls the slew rate of the transmitter, and a signal qualifier in the receiver minimizes false starts improving reliability.

The Am7960 has a modem-like controller interface which makes it compatible with nearly every existing synchronous communications controller (USARTs, SCCs, etc).

The use of ECL circuitry to process signals internal to the Am7960 chip enhances device speed. I/O pins operate at TTL/MOS logic levels to allow convenient interfacing with other devices such as the AmZ8530* Serial Communications Controller.

BLOCK DIAGRAM

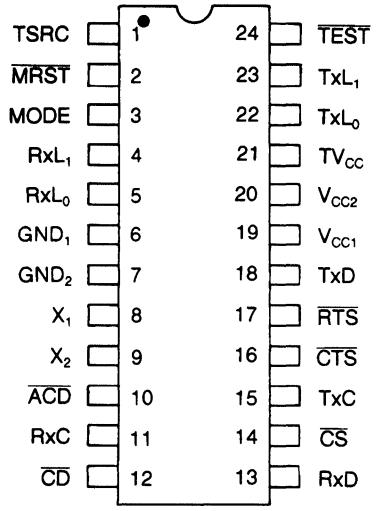


BD005440

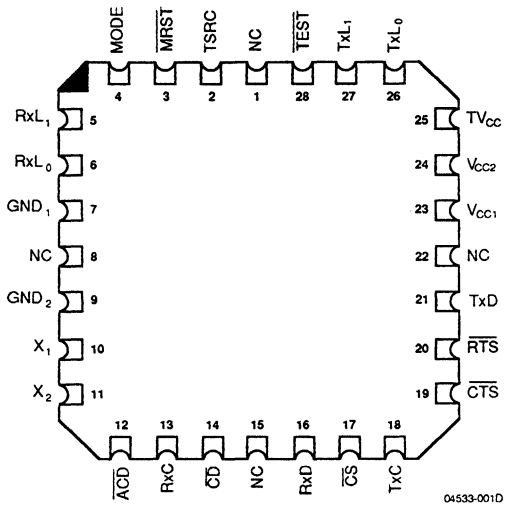
RELATED AMD PRODUCTS

Part No.	Description
Am7990	Local Area Network Controller for Ethernet
Am7992B	Serial Interface Adapter
Am7996	Ethernet Transceiver
AmZ8530	Serial Communications Controller
Am7961	StarLAN Coded Data Transceiver
Am79C900	Integrated Local Area Communication Controller

CONNECTION DIAGRAM
Top View

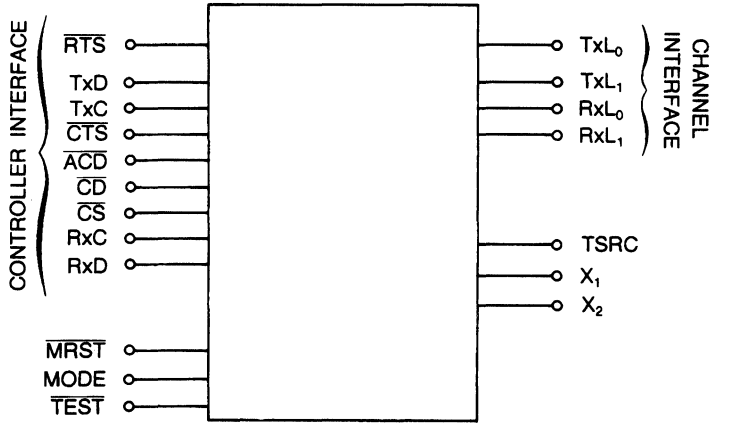


CD007050



CD011960

LOGIC SYMBOL

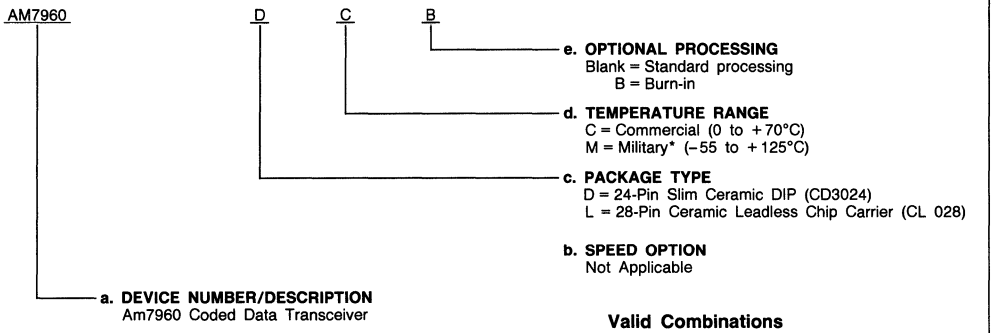


LS001950

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7960	DC, DCB, LC, DMB, LMB

*Military range products are "NPL" (Non-Compliant Products List) or Non-MIL-STD-883C Compliant products only.

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Am7961

StarLAN Coded Data Transceiver

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

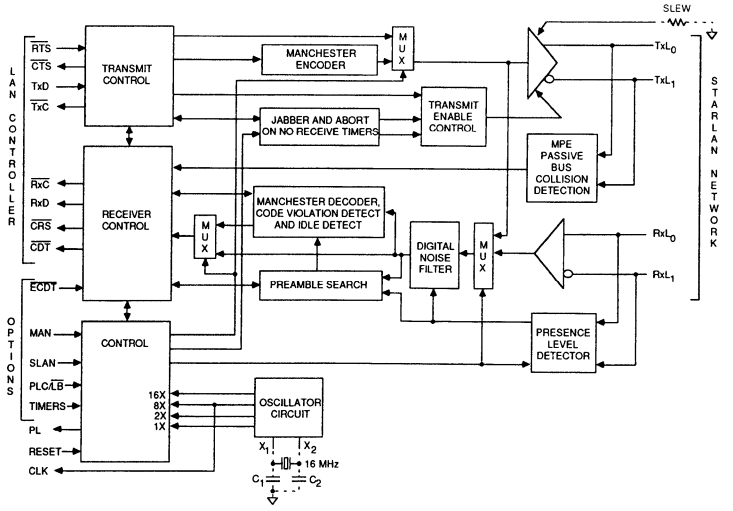
- Single-Chip Transceiver for StarLAN Networks (proposed IEEE 802.3 1BASE5 specification)
- Direct interface to Am7990, 82586, 82588, and 68802 LAN controllers
- Digital Receiver Noise Filter
- Manchester encoder/decoder may be disabled by an external control pin (MAN)
- External pin selects two different receiver input thresholds (±700 mV or ±300 mV)
- Multipoint Extension (Daisychain) Collision Detection circuit
- Transmit slew rate controlled with a single external resistor
- Optional Fault Detection Modes
  - Transmit Jabber Control
  - Abort On No Receive of carrier after transmit
  - Loopback testing capability
- Oscillator Circuit
  - Can be driven by a Crystal or External Clock
  - 8-MHz Output Clock is provided to drive LAN Controller and System Clock (no LAN Controller Crystal required)
- Fault Detection Output (PL) will drive an LED
  - Indicates that Jabber or Abort On No Receive timers have expired

GENERAL DESCRIPTION

The Am7961 is a single-chip transceiver which meets all physical layer requirements specified by the StarLAN network standard (proposed IEEE 802.3 1BASE5 specification). This +5-V device directly interfaces to most Local Area Network (LAN) Controllers. The StarLAN Coded Data Transceiver (SCDT) has two major operating modes: Manchester encoder and decoder active, or Manchester encoder and decoder bypassed. This means the SCDT can operate with Manchester-formatted data or as a simple transceiver. In either mode, the transmit slew rate and receiver presence level may be adjusted by external control pins. The SCDT has an internal digital receive filter which removes the need for external discrete filters. The SCDT is guaranteed to drive StarLAN transmit voltage levels of 2 V minimum and 3.65 V maximum into IEEE 802.3 1BASE5 heavy and light loads. This allows the SCDT to drive StarLAN hubs or operate in Multipoint Extension (daisychain) mode without a StarLAN Hub.

Used with two StarLAN isolation transformers and a LAN controller, the Am7961 is a complete solution which operates between a personal computer bus and a StarLAN network. This network is intended for office environments with either installed telephone wire or with user-installed twisted-pair wire.

BLOCK DIAGRAM



BD007150

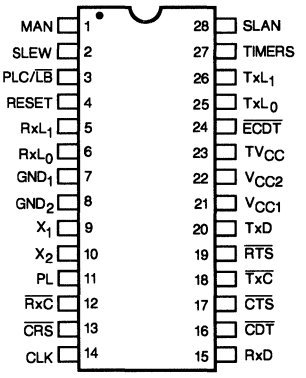
RELATED AMD PRODUCTS

Part No.	Description
Am7960	Coded Data Transceiver
Am7990	Local Area Network Controller for Ethernet
Am7992B	Serial Interface Adapter
Am7996	Ethernet Transceiver
AmZ8530	Serial Communications Controller
Am79C900	Integrated Local Area Communications Controller

CONNECTION DIAGRAMS

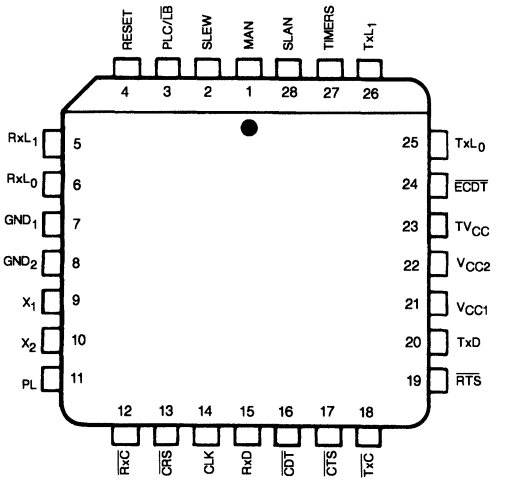
Top View

DIP



CD010571

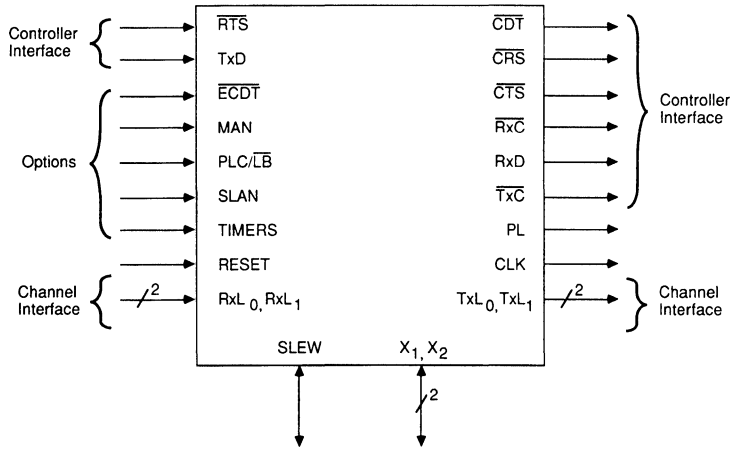
PLCC



CD010580

Note: Pin 1 is marked for orientation.

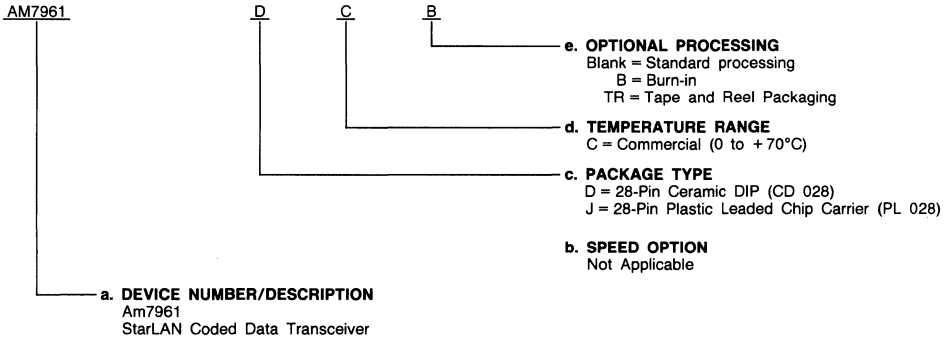
LOGIC SYMBOL



ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7961	DC, DCB, JC, JCB, JCTR

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Am7990

Local Area Network Controller for Ethernet (LANCE)

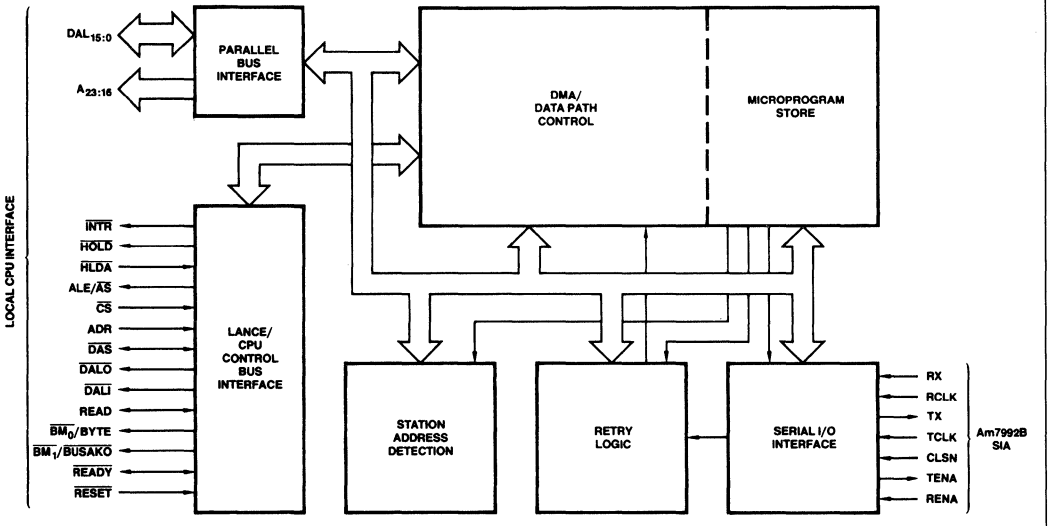
DISTINCTIVE CHARACTERISTICS

- Compatible with Ethernet and IEEE-802.3 10Base5 Type A, and 10Base2 Type B, "Cheapernet")
- Easily interfaced to 8086, 68000, Z8000*, LSI-II** microprocessors
- On-board DMA and buffer management, 48 byte FIFO
- 24-bit wide linear addressing (Bus Master Mode)
- Network and packet error reporting
- Back-to-back packet reception with as little as 4.1 μsec interpacket gap time
- Diagnostic Routines
  - Internal/external loop back
  - CRC logic check
  - Time domain reflectometer

GENERAL DESCRIPTION

The Am7990 Local Area Network Controller for Ethernet (LANCE) is a 48-pin VLSI device designed to greatly simplify interfacing a microcomputer or minicomputer to an IEEE-802.3/Ethernet Local Area Network. The LANCE, in conjunction with the Am7992B Serial Interface Adapter (SIA), Am7996 Transceiver, and closely coupled local memory and microprocessor, is intended to provide the user with a complete interface module for an Ethernet network. The Am7990 is designed using a scaled N-Channel MOS technology and is compatible with a variety of microprocessors. On-board DMA, advanced buffer management, and extensive error reporting and diagnostics facilitate design and improve system performance.

BLOCK DIAGRAM

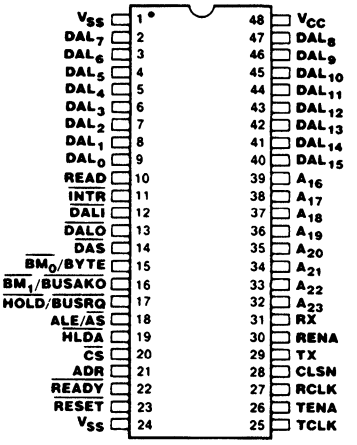


BD002063

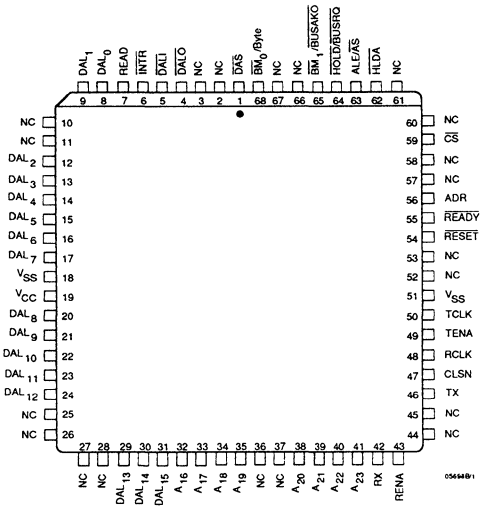
RELATED AMD PRODUCTS

Part No.	Description
Am7992B	Serial Interface Adaptor (SIA)
Am7996	IEEE-802.3/Ethernet/Cheapernet Transceiver
Am79C900	Integrated Local Area Communications Controller

CONNECTION DIAGRAMS
Top View



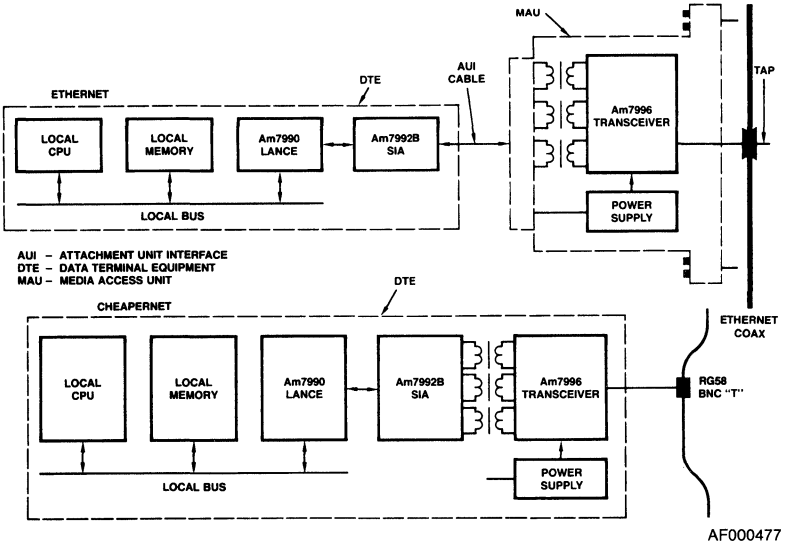
CD001450



CD011930

Note: Pin 1 is marked for orientation.

TYPICAL ETHERNET/CHEAPERNET NODE

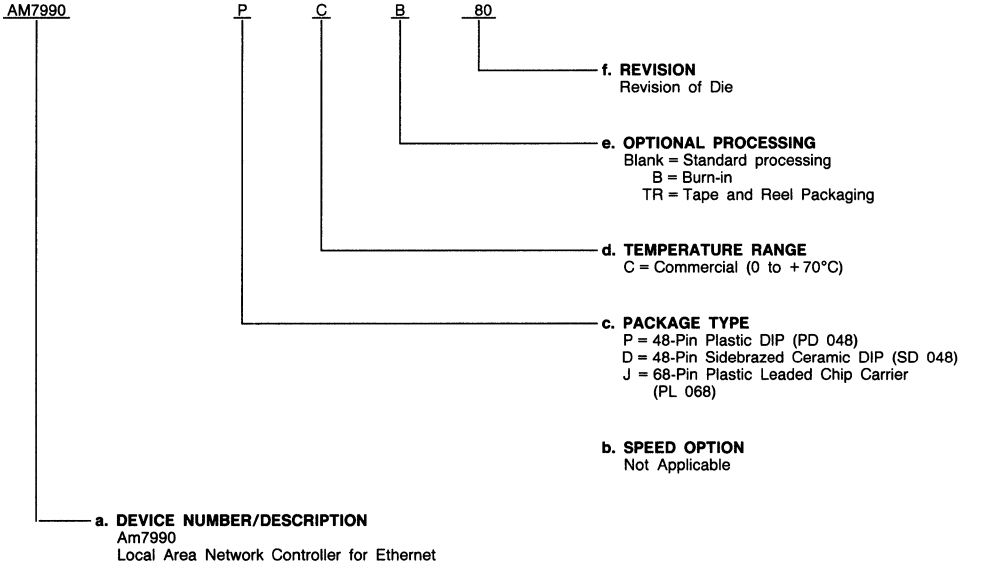


AF000477

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing
f. Revision



Valid Combinations	
AM7990	DC, DCB, PC, PCB, JC, JCB, JCTR

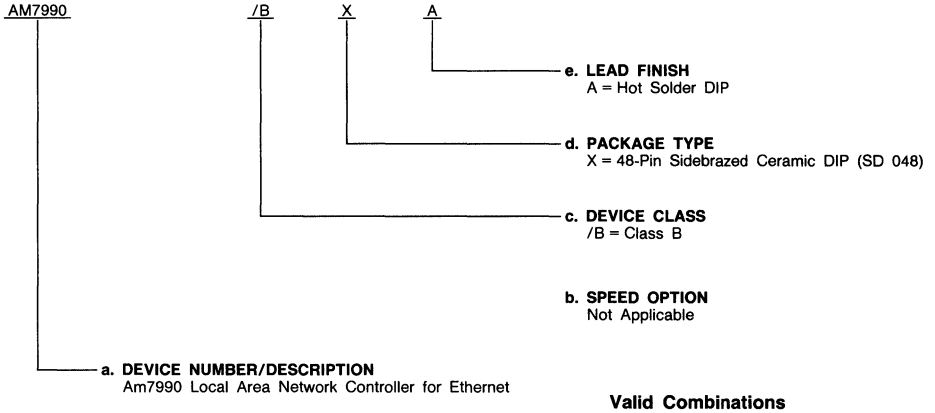
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM7990	/BXA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

Am7992B

Serial Interface Adapter (SIA)

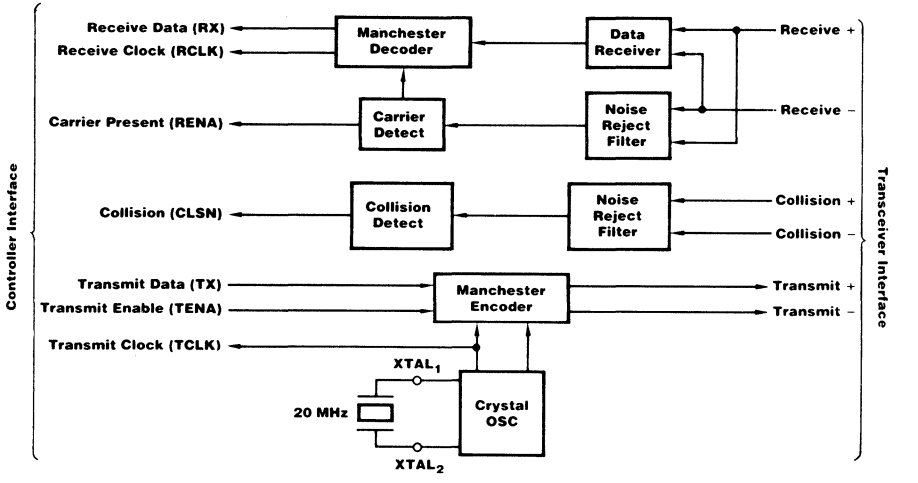
DISTINCTIVE CHARACTERISTICS

- Compatible with Ethernet/Cheapernet/IEEE-802.3 specifications
- Crystal controlled Manchester Encoder
- Manchester Decoder acquires clock and data within four bit times with an accuracy of ±3 ns
- Guaranteed carrier and collision detection squelch threshold limits
  - Carrier/collision detected for inputs greater than −275 mV
  - No carrier/collision for inputs less than −175 mV
- Input signal conditioning rejects transient noise
  - Transients < 10 ns for collision detector inputs
  - Transients < 20 ns for carrier detector inputs
- Receiver decodes Manchester data with worst case ±19 ns of clock jitter (at 10 MHz)
- TTL compatible host interface
- Transmit accuracy ±0.01% (without adjustments)

GENERAL DESCRIPTION

The Am7992B Serial Interface Adapter (SIA) is a Manchester Encoder/Decoder compatible with IEEE–802.3, Cheapernet and Ethernet specifications. In an IEEE-802.3/Ethernet application, the Am7992B interfaces the Am7990 Local Area Network Controller for Ethernet (LANCE) to the Ethernet transceiver cable, acquires clock and data within four bit times, and decodes Manchester data with worst case ±19 ns phase jitter at 10 MHz. SIA provides both guaranteed signal threshold limits and transient noise suppression circuitry in both data and collision paths to minimize false start conditions.

BLOCK DIAGRAM

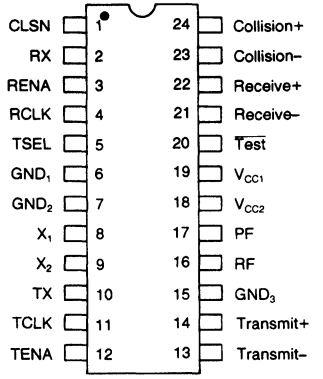


BD002071

RELATED PRODUCTS

Part No.	Description
Am7990	Local Area Network Controller for Ethernet (LANCE)
Am7996	IEEE-802.3/Ethernet/Cheapernet/Transceiver

CONNECTION DIAGRAM



CD001521

Note: Pin 1 is marked for orientation

ORDERING INFORMATION
AMD STANDARD PRODUCTS

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing

Am7992B D C B

e. OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

d. TEMPERATURE RANGE
C = Commercial (0 to +70°C)

c. PACKAGE TYPE
D = 28-Pin (Slim) Ceramic DIP (CD3024)

b. SPEED OPTION
Not Applicable

a. DEVICE NUMBER/DESCRIPTION
Am7992B
Serial Interface Adapter

Valid Combinations	
AM7992B	DC, DCB

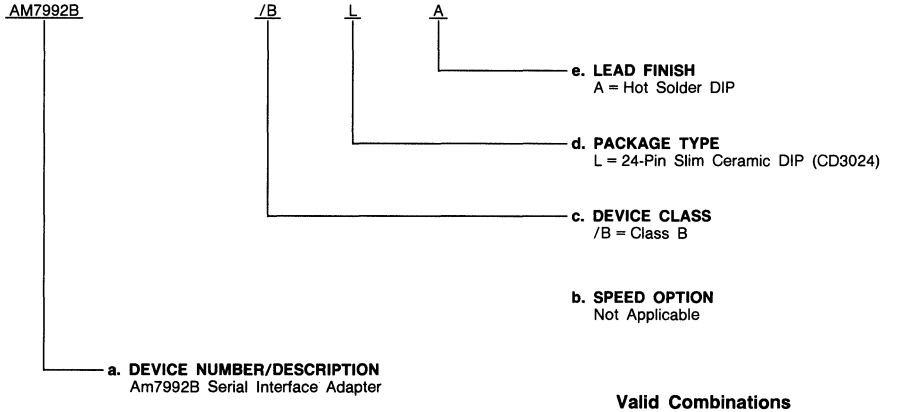
Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM7992B	/BLA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Am7996

IEEE-802.3/Ethernet/Cheapernet Transceiver

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Compatible with Ethernet Version 2 and IEEE-802.3 10Base5 (Type A) and 10Base2 (Type B) specifications
- Pin-selectable SQE Test (Heartbeat) option
- Internal Jabber Controller prevents excessive transmission time
- Noise rejection filter ensures only valid data is transmitted onto network
- Collision detection on both transmit and receive data
- Collision detect threshold levels adjustable for other networking applications

GENERAL DESCRIPTION

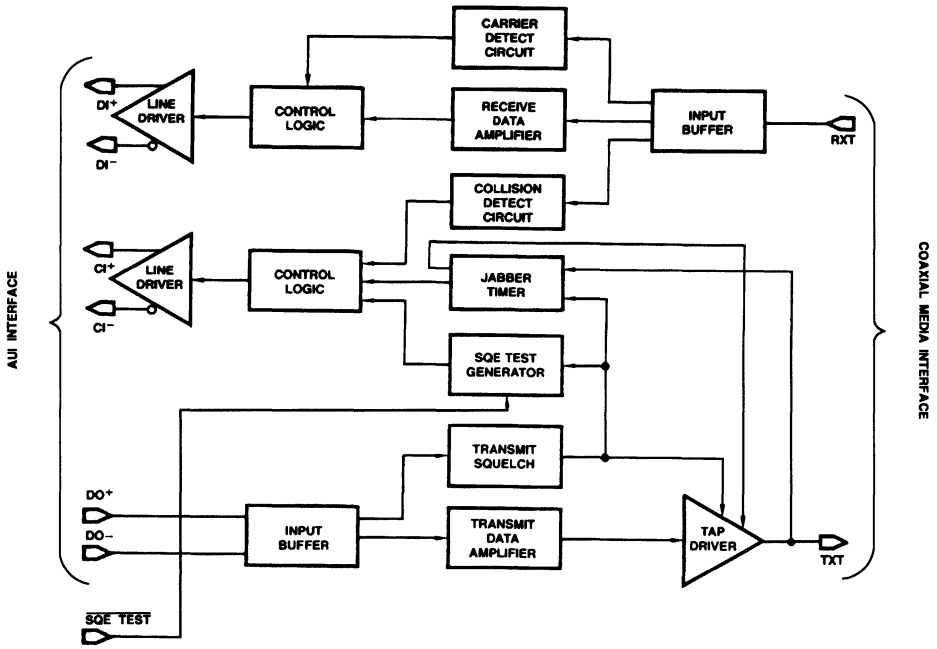
The Am7996 IEEE-802.3/Ethernet/Cheapernet Transceiver supports Ethernet Version 2, IEEE-802.3 (Type A), and IEEE-802.3 (Type B - Cheapernet) transceiver applications. Transmit, receive, and collision detect functions at the coaxial media interface to the Data Terminal Equipment (DTE) are all performed by this single device.

In an IEEE-802.3 (Type A)/Ethernet application, the Am7996 interfaces the coaxial (0.4″ diameter) media to the DTE through an isolating pulse transformer and the 78-Ω Attachment Unit Interface (AUI) cable. In IEEE-802.3 Type B – Cheapernet applications, the Am7996 typically resides inside the DTE with its signals to the DTE isolated and the coaxial (0.2″ diameter) media directly connected to the DTE. Transceiver power and ground in both applications are isolated from that of the DTE.

The Am7996's Tap Driver provides controlled skew and current drive for data signalling onto the media. The Jabber Controller prevents the node from transmitting excessively. While transmitting, collisions on the media are detected if one or more additional stations are transmitting.

The Am7996 features an optional SQE Test function that provides a signal on the *CI* pair at the end of every transmission. The SQE Test indicates the operational status of the *CI* pair to the DTE. It can also serve as an acknowledgement to the node that packet transmission onto the coax was completed.

BLOCK DIAGRAM

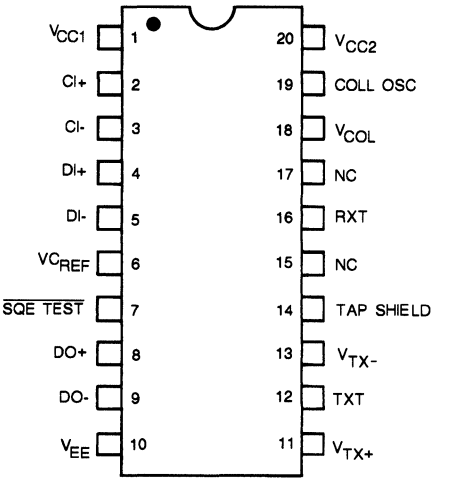


BD005820

RELATED PRODUCTS

Part No.	Description
Am7990	Local Area Network Controller for Ethernet (LANCE)
Am7992B	Serial Interface Adapter (SIA)
Am79C900	Integrated Local Area Communications Controller

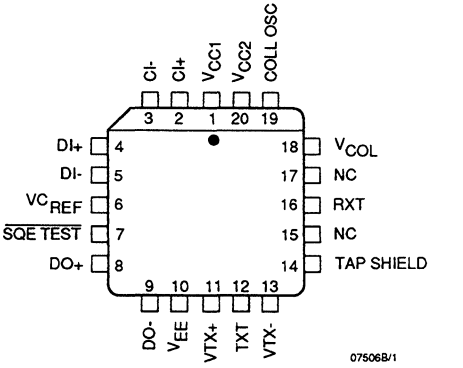
CONNECTION DIAGRAM



CD009070

Note: Pin 1 is marked for orientation.
NC = No Connection

PLCC



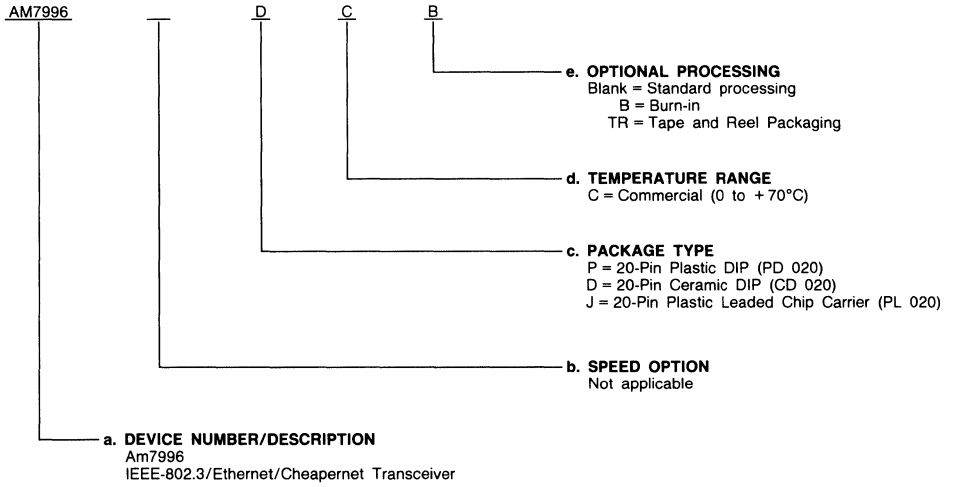
07506B/1

CD011920

ORDERING INFORMATION

Standard Products

AMD products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7996	PC, PCB, DC, DCB, JC, JCB, JCTR

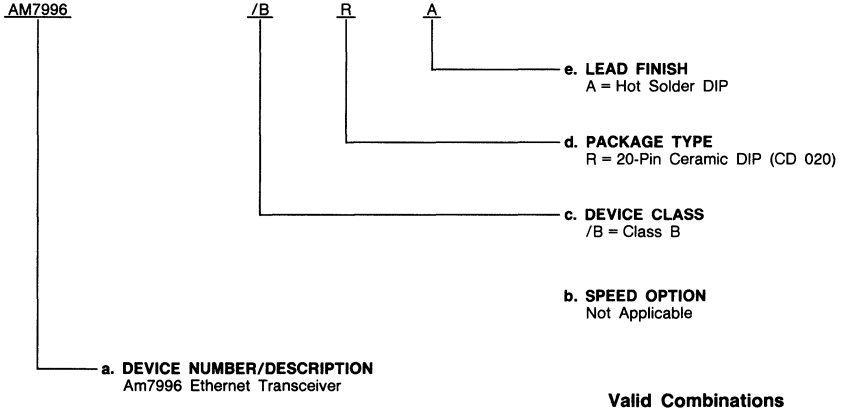
Valid Combinations

Valid combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

ORDERING INFORMATION (Cont'd.)

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM7996	/BRA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Advance Information

Am79C900

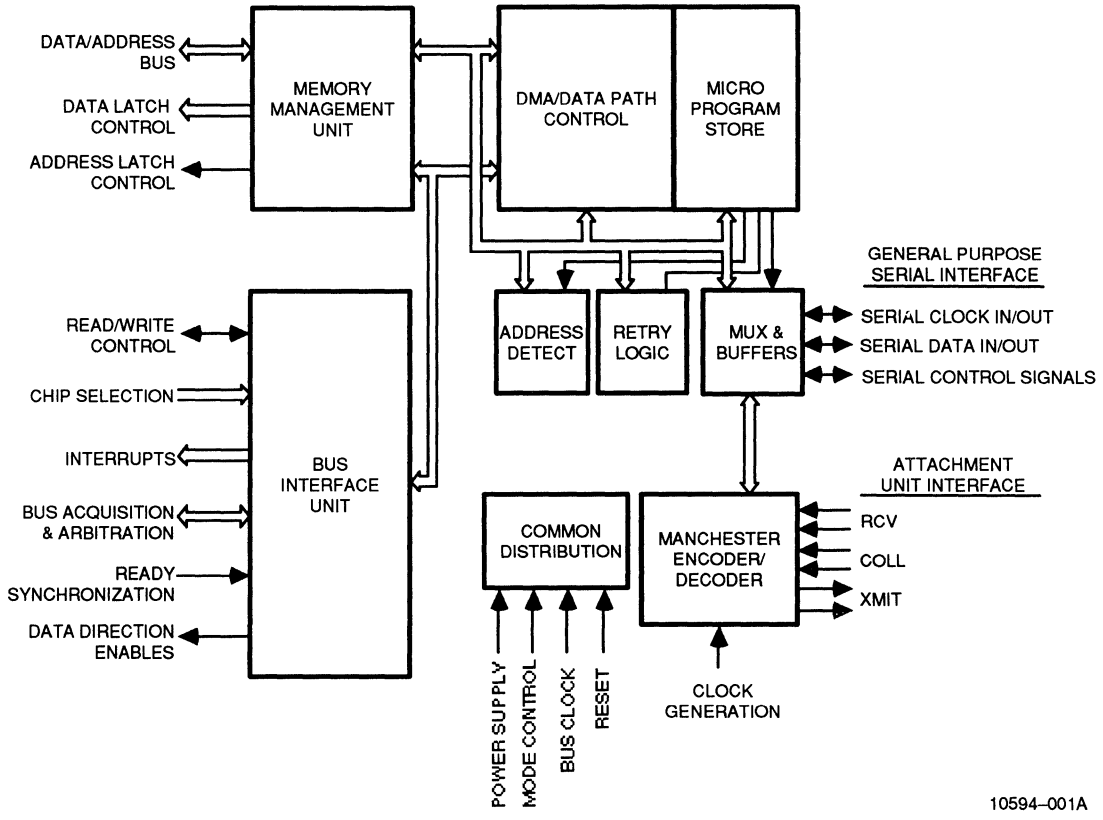
Integrated Local Area Communications Controller (ILACC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Integrated Ethernet controller and Serial Interface Adapter.
- 16 and 32-bit bus interface with programmable modes for easy interface to popular bus architectures such as: 29000, 80286, 80386, 68000, 68020, 68030,and IBM PC/AT™.
- Compatible with Ethernet and IEEE-802.3 10 Base 5, 10 Base 2, 1 Base 5, and twisted pair wire.
- On board 48 byte FIFO, DMA controller, and advanced buffer management scheme.
- Split bus and network clock signals supporting 1–10 Mbit/s networks.
- Extensive network diagnostics capabilities including: CRC, loop back, collision retry/runt packet counters, and TDR.
- Backwards software compatible with the Am7990 LANCE (in LANCE mode).
- State of the art CMOS technology and surface mount packaging.

BLOCK DIAGRAM

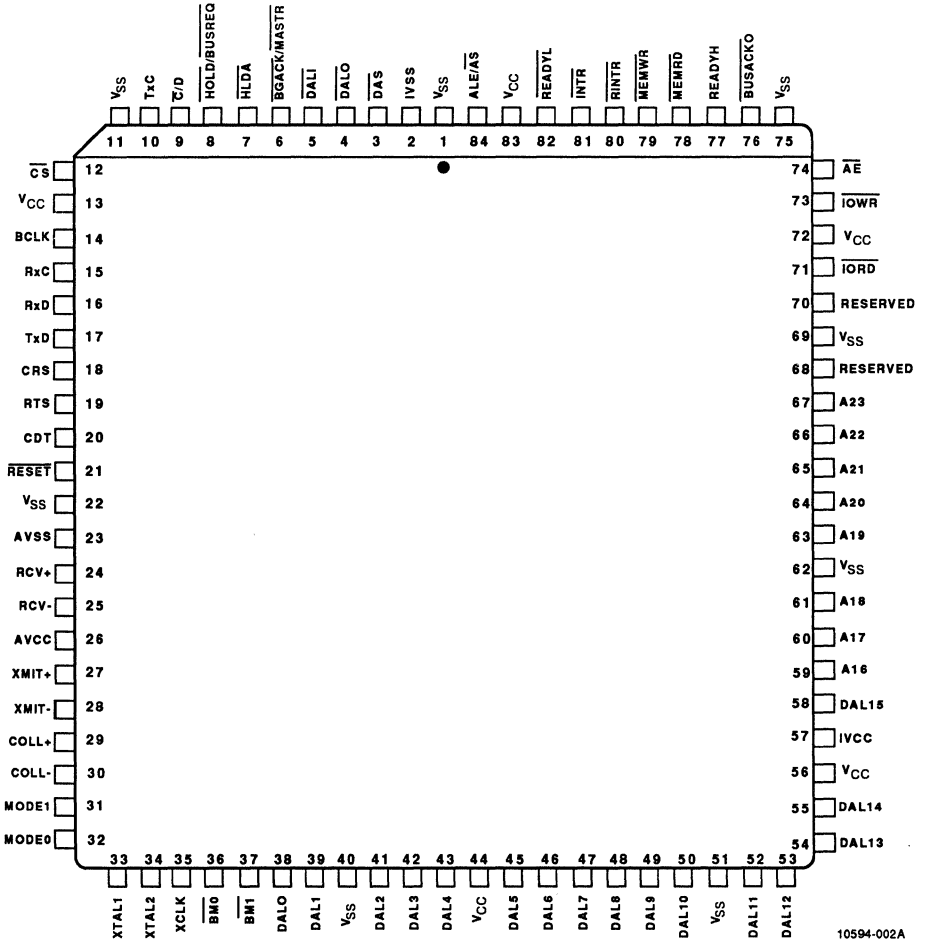


10594–001A

GENERAL DESCRIPTION

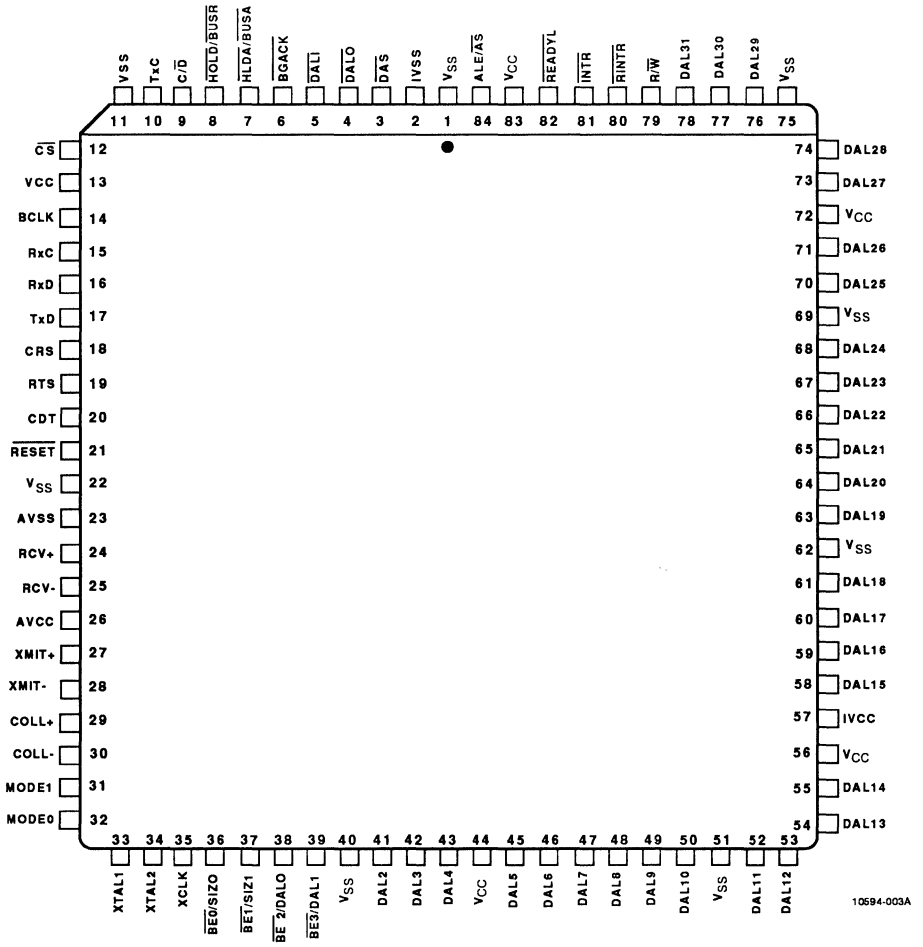
The Am79C900 Local Area Communications Controller (ILACC) is a second generation Ethernet/802.3 integrated controller and serial interface encoder/decoder. The ILACC has been designed to easily interface to popular micro processor bus architectures through it's programmable bus interface. The ILACC's on board DMA controller and it's sophisticated buffer management scheme allows the system designer to achieve maximum performance in tightly coupled systems such as PC mother board applications and node processor based adapter cards. In open bus architectures such as personal computer add-on LAN cards the ILACC gives the system designer the flexibility to chose the optimal cost-performance ratio by allowing both inexpensive bus master applications and higher performing shared memory applications. The ILACC will through it's AUI interface in conjunction with an external transceiver chip support both thick coax, thin coax, and twisted pair cable networking schemes, such as Ethernet and IEEE–802.3 10 Base 5, 10 Base 2,and 1 Base 5.

CONNECTION DIAGRAM
Am79C900JC (Mode 0 & 2)*



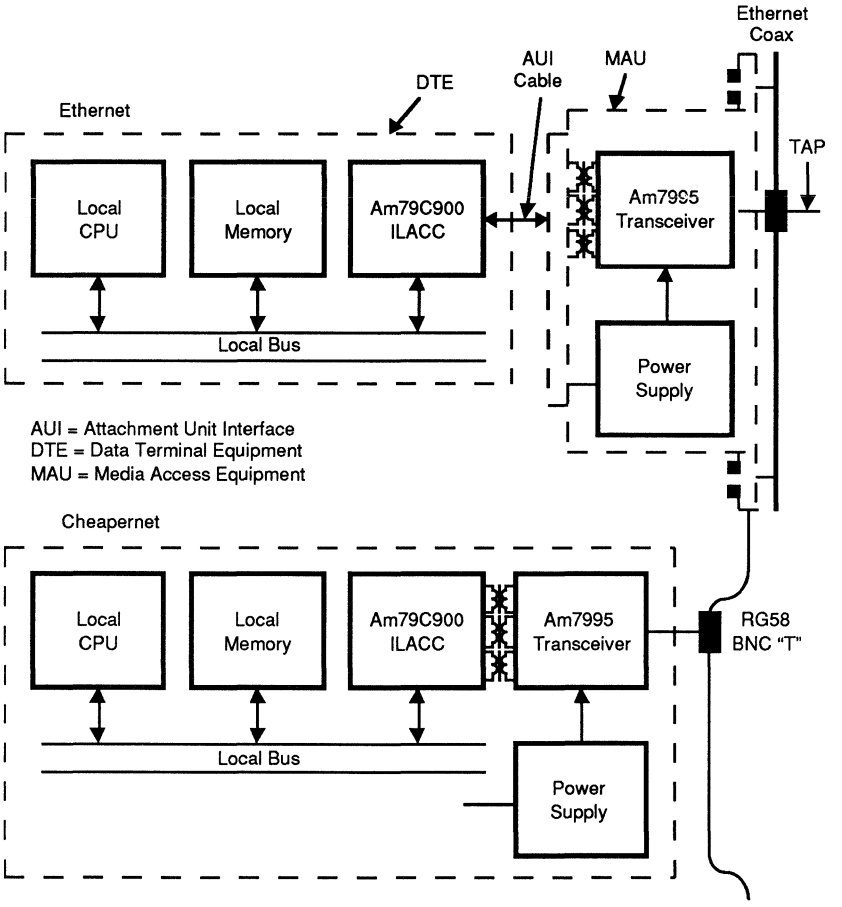
*Warning: This Pin-Out is subject to change prior to product release. AMD reserves the right to change without notice.

CONNECTION DIAGRAM
Am79C900JC (Mode 1)*



*Warning: This Pin-Out is subject to change prior to product release. AMD reserves the right to change without notice.

TYPICAL ETHERNET NODE



Nomenclature conventions

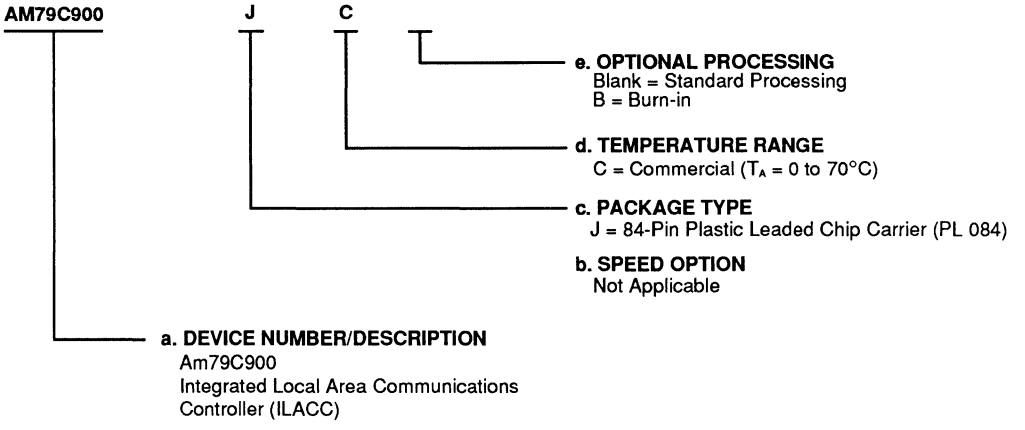
In this document the following convention for ACTIVE LOW signals is used: SIGNAL NAME (instead of SIGNAL name that is commonly used).

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM79C900	JC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

NETWORKING PRODUCTS

SUPERNET Family for FDDI

Preliminary

Am79C81A

CMOS RAM Buffer Controller (RBC)

Advanced Micro Devices

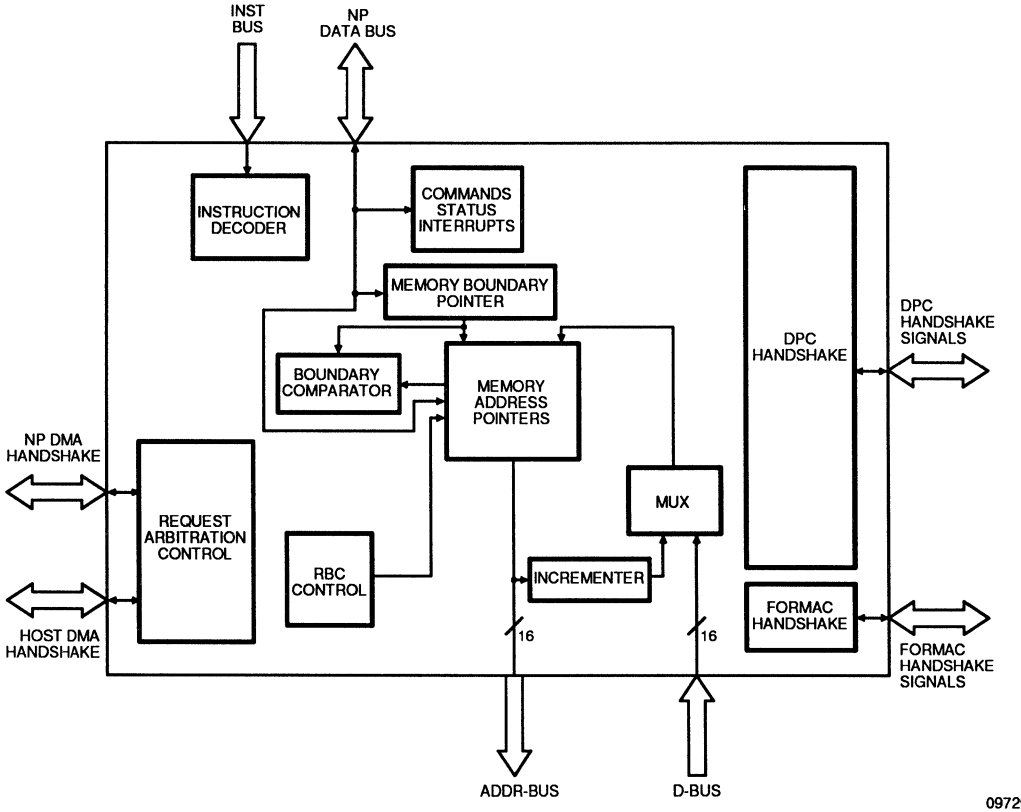
DISTINCTIVE CHARACTERISTICS

- **Total memory buffer management**
  - 16-bit address bus supports 64K words (32 bits wide) with the Am79C82A Data Path Controller (DPC)
  - Programmable registers and pointers
  - DMA arbitration between the Data Path Controller (DPC), Node Processor (NP), Memory full and empty notification and Host
- **Supports transmit link list addressing**
- **12.5-MHz byte clock**
- **TTL-Compatible I/O**
- **Single +5-V supply**
- **145-lead pin grid array package**

GENERAL DESCRIPTION

The Am79C81A RAM Buffer Controller (RBC), along with the Am79C82A Data Path Controller (DPC), manages Buffer Memory to implement a FIFO (first-in, first-out) data structure, simplifying the design of any high-speed interface. This CMOS device has TTL-compatible input and output pins which provide a straightforward interface to other external devices. Diagnostic information is also accumulated and reported by the RBC.

BLOCK DIAGRAM



09729-001A

CONNECTION DIAGRAM
PGA Bottom View (Pins facing up)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
1	NC	VCC	$\overline{CSI}$	$\overline{DS}$	NP14	NP11	NP9	NP8	NP6	NP3	NP1	NP0	$\overline{NMINTR}$	NC	CLM/$\overline{BEC}$	1
2	NC	INST0	BMODE	NC	NP15	NP12	NP10	NC	NP7	NP4	NP2	BCLK	VCC	NC	NC	2
3	INST3	INST2	INST1	$\overline{READY}$	GND	NP13	GND	GND	VCC	NP5	GND	NC	NC	NC	RCVABT	3
4	DISRBC	HSRDRQ	R/$\overline{W}$	●									GND	FSHRCVF	NC	4
5	$\overline{HSRDACK}$	NPRDRQ	$\overline{RESET}$										DWRREQ	DRDREQS	NC	5
6	$\overline{NPRDACK}$	HSWRRQ	GND										DRDREQA	BRCVFRM	ERCVFRM	6
7	VCC	NPWRRQ	$\overline{HSWRACK}$										GND	LDRPXS	LDRPXA	7
8	$\overline{NPWRACK}$	GND	GND					(Bottom View)					DISNHRQ	VCC	NC	8
9	NC	NC	TESTEN										GND	DRDACKS	DRDACKA	9
10	$\overline{NPWACKE}$	TEST	GND										DWRACK	ACKONE	PARERR	10
11	NC	$\overline{HSWACKE}$	SO										GND	MDRDACK	MDWRACK	11
12	SI	NC	VCC										XBEERR	RBFERR	INICLBN	12
13	NC	D15	D12	D9	GND	D4	D1	GND	ADDR12	ADDR9	ADDR6	ADDR4	ADDR1	$\overline{WR}$	$\overline{RD}$	13
14	NC	D14	D11	D8	D6	D3	NC	GND	ADDR13	ADDR10	ADDR7	GND	ADDR2	VCC	$\overline{CS0}$	14
15	NC	D13	D10	D7	D5	D2	D0	VCC	ADDR14	ADDR11	ADDR8	ADDR5	ADDR3	ADDR0	ADDR15	15
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

09729–002A

PIN DESIGNATIONS

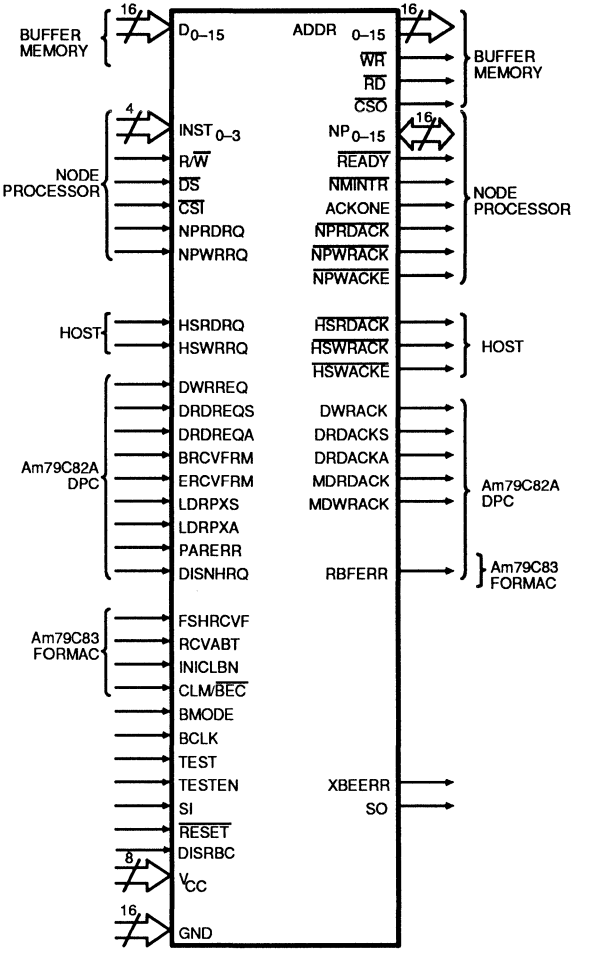
(Sorted by Pin Number)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A-1	NC	C-7	$\overline{\text{HSWRACK}}$	H-13	GND	N-10	DWRACK
A-2	NC	C-8	GND	H-14	GND	N-11	GND
A-3	INST_3	C-9	TESTEN	H-15	V_{CC}	N-12	XBEERR
A-4	DISRBC	C-10	GND	J-1	NP_6	N-13	ADDR_1
A-5	$\overline{\text{HSRDACK}}$	C-11	SO	J-2	NP_7	N-14	ADDR_2
A-6	$\overline{\text{NPRDACK}}$	C-12	V_{CC}	J-3	V_{CC}	N-15	ADDR_3
A-7	V_{CC}	C-13	D_{12}	J-13	ADDR_{12}	P-1	NC
A-8	$\overline{\text{NPWRACK}}$	C-14	D_{11}	J-14	ADDR_{13}	P-2	NC
A-9	NC	C-15	D_{10}	J-15	ADDR_{14}	P-3	NC
A-10	$\overline{\text{NPWACKE}}$	D-1	$\overline{\text{DS}}$	K-1	NP_3	P-4	FSHRCVF
A-11	NC	D-2	NC	K-2	NP_4	P-5	DRDREQS
A-12	SI	D-3	$\overline{\text{READY}}$	K-3	NP_5	P-6	BRCVFRM
A-13	NC	D-4	GUIDE PIN	K-13	ADDR_9	P-7	LDRPXS
A-14	NC	D-13	D_9	K-14	ADDR_{10}	P-8	V_{CC}
A-15	NC	D-14	D_8	K-15	ADDR_{11}	P-9	DRDACKS
B-1	V_{CC}	D-15	D_7	L-1	NP_1	P-10	ACKONE
B-2	INST_0	E-1	NP_{14}	L-2	NP_2	P-11	MDRDACK
B-3	INST_2	E-2	NP_{15}	L-3	GND	P-12	RBFERR
B-4	HSRDRQ	E-3	GND	L-13	ADDR_6	P-13	$\overline{\text{WR}}$
B-5	NPRDRQ	E-13	GND	L-14	ADDR_7	P-14	V_{CC}
B-6	HSWRRQ	E-14	D_6	L-15	ADDR_8	P-15	ADDR_0
B-7	NPWRRQ	E-15	D_5	M-1	NP_0	R-1	CLM/$\overline{\text{BEC}}$
B-8	GND	F-1	NP_{11}	M-2	BCLK	R-2	NC
B-9	NC	F-2	NP_{12}	M-3	NC	R-3	RCVABT
B-10	TEST	F-3	NP_{13}	M-13	ADDR_4	R-4	NC
B-11	$\overline{\text{HSWACKE}}$	F-13	D_4	M-14	GND	R-5	NC
B-12	NC	F-14	D_3	M-15	ADDR_5	R-6	ERCVFRM
B-13	D_{15}	F-15	D_2	N-1	$\overline{\text{NMINTR}}$	R-7	LDRPXA
B-14	D_{14}	G-1	NP_9	N-2	V_{CC}	R-8	NC
B-15	D_{13}	G-2	NP_{10}	N-3	NC	R-9	DRDACKA
C-1	$\overline{\text{CSI}}$	G-3	GND	N-4	GND	R-10	PARERR
C-2	BMODE	G-13	D_1	N-5	DWRREQ	R-11	MDWRACK
C-3	INST_1	G-14	NC	N-6	DRDREQA	R-12	INICLBN
C-4	R/$\overline{\text{W}}$	G-15	D_0	N-7	GND	R-13	$\overline{\text{RD}}$
C-5	$\overline{\text{RESET}}$	H-1	NP_8	N-8	DISNHRQ	R-14	$\overline{\text{CSO}}$
C-6	GND	H-2	NC	N-9	GND	R-15	ADDR_{15}
		H-3	GND				

PIN DESIGNATIONS
(Sorted by Pin Name)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
P-10	ACKONE	B-15	D_{13}	B-2	$INST_0$	C-5	$\overline{RESET}$
P-15	$ADDR_0$	B-14	D_{14}	C-3	$INST_1$	A-12	SI
N-13	$ADDR_1$	B-13	D_{15}	B-3	$INST_2$	C-11	SO
N-14	$ADDR_2$	N-8	DISNHRQ	A-3	$INST_3$	B-10	TEST
N-15	$ADDR_3$	A-4	DISRBC	R-7	LDRPXA	C-9	TESTEN
M-13	$ADDR_4$	R-9	DRDACKA	P-7	LDRPXS	A-7	Vcc
M-15	$ADDR_5$	P-9	DRDACKS	P-11	MDRDACK	B-1	Vcc
L-13	$ADDR_6$	N-6	DRDREQA	R-11	MDWRACK	C-12	Vcc
L-14	$ADDR_7$	P-5	DRDREQS	N-1	$\overline{NMINTR}$	H-15	Vcc
L-15	$ADDR_8$	D-1	$\overline{DS}$	M-1	NP_0	J-3	Vcc
K-13	$ADDR_9$	N-10	DWRACK	L-1	NP_1	N-2	Vcc
K-14	$ADDR_{10}$	N-5	DWRREQ	L-2	NP_2	P-14	Vcc
K-15	$ADDR_{11}$	R-6	ERCVFRM	K-1	NP_3	P-8	Vcc
J-13	$ADDR_{12}$	P-4	FSHRCVF	K-2	NP_4	P-13	$\overline{WR}$
J-14	$ADDR_{13}$	B-8	GND	K-3	NP_5	N-12	XBEERR
J-15	$ADDR_{14}$	C-10	GND	J-1	NP_6	A-1	NC
R-15	$ADDR_{15}$	C-6	GND	J-2	NP_7	A-11	NC
M-2	BCLK	C-8	GND	H-1	NP_8	A-13	NC
C-2	BMODE	E-13	GND	G-1	NP_9	A-14	NC
P-6	BRCVFRM	E-3	GND	G-2	NP_{10}	A-15	NC
R-1	CLM/$\overline{BEC}$	G-3	GND	F-1	NP_{11}	A-2	NC
C-1	$\overline{CSI}$	H-13	GND	F-2	NP_{12}	A-9	NC
R-14	$\overline{CSO}$	H-14	GND	F-3	NP_{13}	B-12	NC
G-15	D_0	H-3	GND	E-1	NP_{14}	B-9	NC
G-13	D_1	L-3	GND	E-2	NP_{15}	D-2	NC
F-15	D_2	M-14	GND	B-5	NPRDRQ	G-14	NC
F-14	D_3	N-11	GND	B-7	NPWRRQ	H-2	NC
F-13	D_4	N-4	GND	A-6	$\overline{NPRDACK}$	M-3	NC
E-15	D_5	N-7	GND	A-10	$\overline{NPWACKE}$	N-3	NC
E-14	D_6	N-9	GND	A-8	$\overline{NPWRACK}$	P-1	NC
D-15	D_7	D-4	GUIDE PIN	R-10	PARERR	P-2	NC
D-14	D_8	A-5	$\overline{HSRDACK}$	C-4	R/$\overline{W}$	P-3	NC
D-13	D_9	B-4	HSRDRQ	P-12	RBFERR	R-2	NC
C-15	D_{10}	B-6	HSWRRQ	R-3	RCVABT	R-4	NC
C-14	D_{11}	B-11	$\overline{HSWACKE}$	R-13	$\overline{RD}$	R-5	NC
C-13	D_{12}	C-7	$\overline{HSWRACK}$	D-3	$\overline{READY}$	R-8	NC
		R-12	INICLBN				

LOGIC SYMBOL



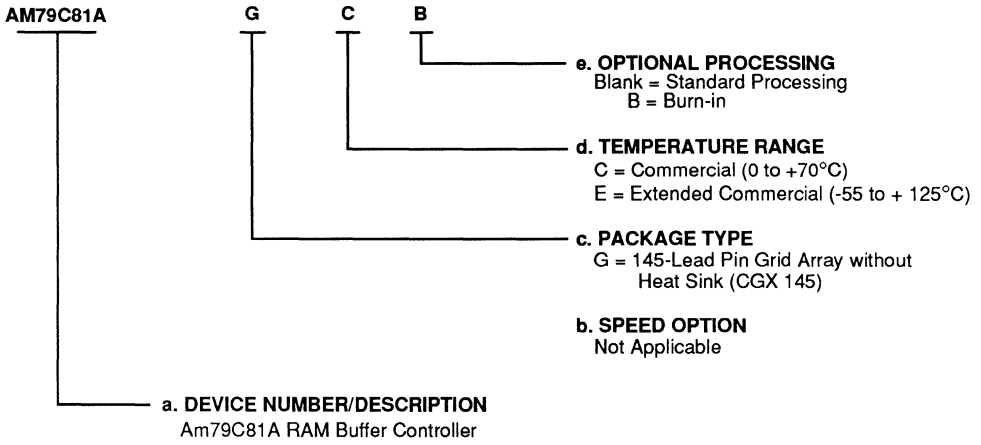
09729–003A

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM79C81A	GC, GCB, GE, GEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Preliminary

Am79C82A

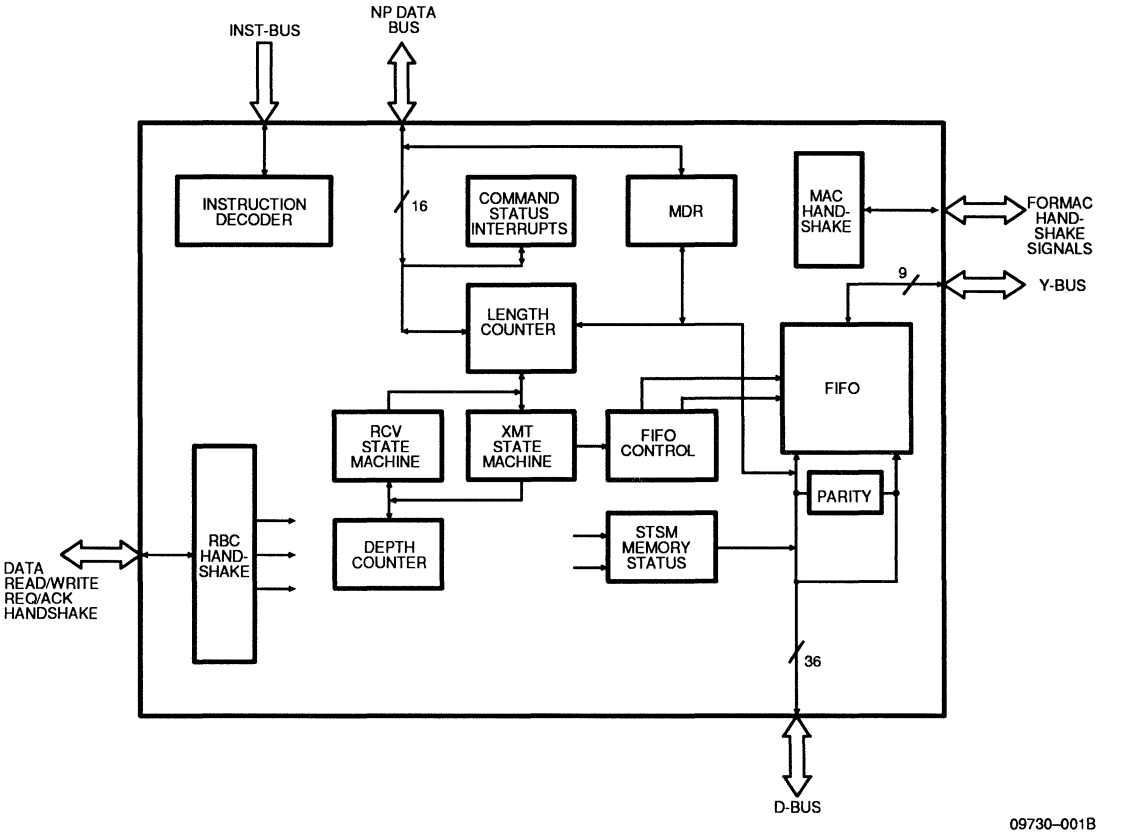
CMOS Data Path Controller (DPC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Performs reception and transmission of frames
- Byte (8 + 1 bits) to word (32 + 4 bits) conversions
- Reports error status
- Performs parity check and generation
- 12.5-MHz byte clock
- 145-lead pin grid array package
- Single +5-V supply

BLOCK DIAGRAM



09730-001B

GENERAL DESCRIPTION

The Am79C82A Data Path Controller (DPC) is a CMOS device that, along with the Am79C81A RAM Buffer Controller (RBC), performs buffer management for high-speed interfaces. It buffers and stores the received packets one after the other in Buffer Memory. It also identifies the status of the packet, including any error conditions. This +5-V device runs at 12.5 MHz rate and allows Buffer Memory throughput of 200 Mbps. All inputs and outputs are TTL-compatible, providing a simple interface to other external devices.

CONNECTION DIAGRAM
PGA Bottom View (pins facing up)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
1	NC	VCC	$\overline{CSI}$	$\overline{DS}$	NP14	NP11	NP9	NP8	NP6	NP3	NP1	NP0	$\overline{NMINTR}$	RECEIVE	Y7	1
2	NC	INST0	BMODE	NC	NP15	NP12	NP10	NC	NP7	NP4	NP2	BCLK	VCC	FSHRCVF	Y6	2
3	INST3	INST2	INST1	$\overline{READY}$	GND	NP13	GND	NC	VCC	NP5	GND	$\overline{MINTR}$	DAVALID	Y4	Y5	3
4	NC	DRDREQA	R/$\overline{W}$	●									GND	Y3	NC	4
5	DWRREQ	DRDREQS	$\overline{RESET}$										YP	Y1	Y2	5
6	LDRPXA	BRCVFRM	GND										Y0	MEDREQS	MEDREQA	6
7	VCC	LDRPXS	ERCVFRM										VCC	XMEDAVS	XMEDAVA	7
8	DWRACK	GND	GND				(Bottom View)						RDYTBYT	XFRBYTE	NC	8
9	DRDACKA	DRDACKS	PARERR										GND	XMTABTO	XMTABTI	9
10	DISNHRQ	ACKONE	MDWRACK										INICLBN	RCVABT	MISFRM	10
11	MDRDACK	RBFERR	DP2										GND	NC	TEST	11
12	DP0	DP1	GND										SI	SO	NC	12
13	ODDPAR	DP3	D28	D25	GND	D20	D17	GND	D14	D11	D8	D5	NC	NC	NC	13
14	D31	D30	D27	D24	D22	D19	D16	GND	D13	D10	D7	GND	D3	VCC	NC	14
15	VCC	D29	D26	D23	D21	D18	D15	VCC	D12	D9	D6	D4	D2	D1	D0	15
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

09730–002B

PIN DESIGNATIONS
(Sorted by Pin Number)

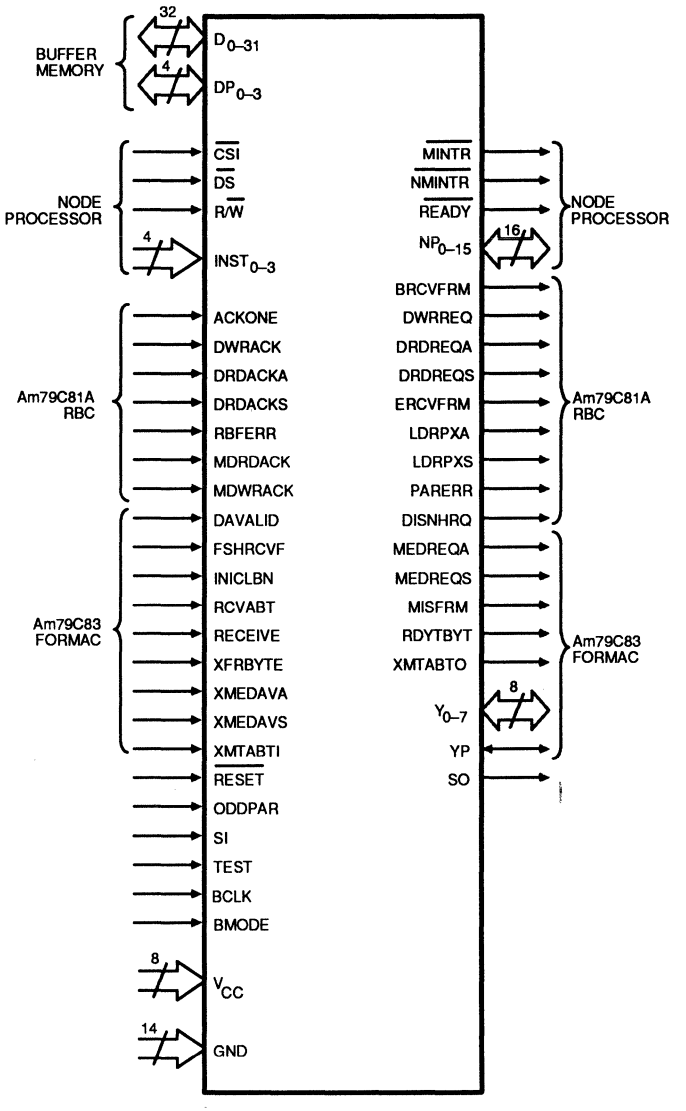
Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A–1	NC	C–7	ERCVFRM	H–13	GND	N–10	INICLBN
A–2	NC	C–8	GND	H–14	GND	N–11	GND
A–3	$INST_3$	C–9	PARERR	H–15	V_{CC}	N–12	SI
A–4	NC	C–10	MDWRACK	J–1	NP_6	N–13	NC
A–5	DWRREQ	C–11	DP_2	J–2	NP_7	N–14	D_3
A–6	LDRPXA	C–12	GND	J–3	V_{CC}	N–15	D_2
A–7	V_{CC}	C–13	D 28	J–13	D_{14}	P–1	RECEIVE
A–8	DWRACK	C–14	D 27	J–14	D_{13}	P–2	FSHRCVF
A–9	DRDACKA	C–15	D 26	J–15	D_{12}	P–3	Y_4
A–10	DISNHRQ	D–1	$\overline{DS}$	K–1	NP_3	P–4	Y_3
A–11	MDRDACK	D–2	NC	K–2	NP_4	P–5	Y_1
A–12	DP_0	D–3	$\overline{READY}$	K–3	NP_5	P–6	MEDREQS
A–13	ODDPAR	D–4	GUIDE PIN	K–13	D_{11}	P–7	XMEDAVS
A–14	D 31	D–13	D 25	K–14	D_{10}	P–8	XFRBYTE
A–15	V_{CC}	D–14	D 24	K–15	D_9	P–9	XMTABTO
B–1	V_{CC}	D–15	D 23	L–1	NP_1	P–10	RCVABT
B–2	$INST_0$	E–1	NP_{14}	L–2	NP_2	P–11	NC
B–3	$INST_2$	E–2	NP_{15}	L–3	GND	P–12	SO
B–4	DRDREQA	E–3	GND	L–13	D_8	P–13	NC
B–5	DRDREQS	E–13	GND	L–14	D_7	P–14	V_{CC}
B–6	BRCVFRM	E–14	D 22	L–15	D_6	P–15	D_1
B–7	LDRPXS	E–15	D 21	M–1	NP_0	R–1	Y_7
B–8	GND	F–1	NP_{11}	M–2	BCLK	R–2	Y_6
B–9	DRDACKS	F–2	NP_{12}	M–3	$\overline{MINTR}$	R–3	Y_5
B–10	ACKONE	F–3	NP_{13}	M–13	D_5	R–4	NC
B–11	RBFERR	F–13	D 20	M–14	GND	R–5	Y_2
B–12	DP_1	F–14	D 19	M–15	D_4	R–6	MEDREQA
B–13	DP_3	F–15	D 18	N–1	$\overline{NMINTR}$	R–7	XMEDAVA
B–14	D 30	G–1	NP_9	N–2	V_{CC}	R–8	NC
B–15	D 29	G–2	NP_{10}	N–3	DAVALID	R–9	XMTABTI
C–1	$\overline{CSI}$	G–3	GND	N–4	GND	R–10	MISFRM
C–2	BMODE	G–13	D 17	N–5	YP	R–11	TEST
C–3	$INST_1$	G–14	D 16	N–6	Y_0	R–12	NC
C–4	$R/\overline{W}$	G–15	D 15	N–7	V_{CC}	R–13	NC
C–5	$\overline{RESET}$	H–1	NP_8	N–8	RDYTBYT	R–14	NC
C–6	GND	H–2	NC	N–9	GND	R–15	D_0
		H–3	NC				

PIN DESIGNATIONS

(Sorted by Pin Name)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
B–10	ACKONE	A–14	D_{31}	B–7	LDRPXS	A–15	Vcc
M–2	BCLK	N–3	DAVALID	A–11	MDRDACK	A–7	Vcc
C–2	BMODE	A–10	DISNHRQ	C–10	MDWRACK	B–1	Vcc
B–6	BRCVFRM	A–12	DP_0	R–6	MEDREQA	H–15	Vcc
C–1	$\overline{CSI}$	B–12	DP_1	P–6	MEDREQS	J–3	Vcc
R–15	D_0	C–11	DP_2	M–3	$\overline{MINTR}$	N–2	Vcc
P–15	D_1	B–13	DP_3	R–10	MISFRM	N–7	Vcc
N–15	D_2	A–9	DRDACKA	N–1	$\overline{NMINTR}$	P–14	Vcc
N–14	D_3	B–9	DRDACKS	M–1	NP_0	P–8	XFRBYTE
M–15	D_4	B–4	DRDREQA	L–1	NP_1	R–7	XMEDAVA
M–13	D_5	B–5	DRDREQS	L–2	NP_2	P–7	XMEDAVS
L–15	D_6	D–1	$\overline{DS}$	K–1	NP_3	R–9	XMTABTI
L–14	D_7	A–8	DWRACK	K–2	NP_4	P–9	XMTABTO
L–13	D_8	A–5	DWRREQ	K–3	NP_5	N–6	Y_0
K–15	D_9	C–7	ERCVFRM	J–1	NP_6	P–5	Y_1
K–14	D_{10}	P–2	FSHRCVF	J–2	NP_7	R–5	Y_2
K–13	D_{11}	B–8	GND	H–1	NP_8	P–4	Y_3
J–15	D_{12}	C–12	GND	G–1	NP_9	P–3	Y_4
J–14	D_{13}	C–6	GND	G–2	NP_{10}	R–3	Y_5
J–13	D_{14}	C–8	GND	F–1	NP_{11}	R–2	Y_6
G–15	D_{15}	E–13	GND	F–2	NP_{12}	R–1	Y_7
G–14	D_{16}	E–3	GND	F–3	NP_{13}	N–5	YP
G–13	D_{17}	G–3	GND	E–1	NP_{14}	A–1	NC
F–15	D_{18}	H–13	GND	E–2	NP_{15}	A–2	NC
F–14	D_{19}	H–14	GND	A–13	ODDPAR	A–4	NC
F–13	D_{20}	L–3	GND	C–9	PARERR	D–2	NC
E–15	D_{21}	M–14	GND	C–4	R/$\overline{W}$	H–2	NC
E–14	D_{22}	N–11	GND	B–11	RBFERR	H–3	NC
D–15	D_{23}	N–4	GND	P–10	RCVABT	N–13	NC
D–14	D_{24}	N–9	GND	N–8	RDYTBYT	P–11	NC
D–13	D_{25}	D–4	GUIDE PIN	D–3	$\overline{READY}$	P–13	NC
C–15	D_{26}	N–10	INICLBN	P–1	RECEIVE	R–12	NC
C–14	D_{27}	B–2	$INST_0$	C–5	$\overline{RESET}$	R–13	NC
C–13	D_{28}	C–3	$INST_1$	N–12	SI	R–14	NC
B–15	D_{29}	B–3	$INST_2$	P–12	SO	R–4	NC
B–14	D_{30}	A–3	$INST_3$	R–11	TEST	R–8	NC
		A–6	LDRPXA				

LOGIC SYMBOL

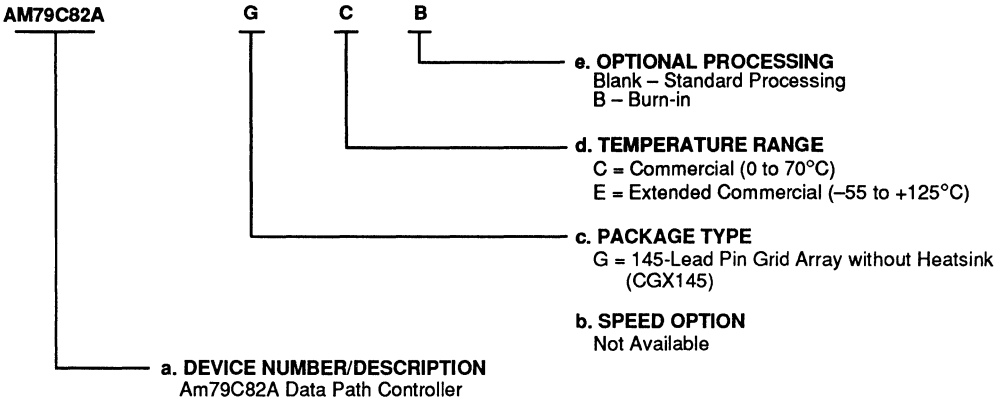


09730–003B

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM79C82A	GC, GCB, GE, GEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Preliminary

Am79C83

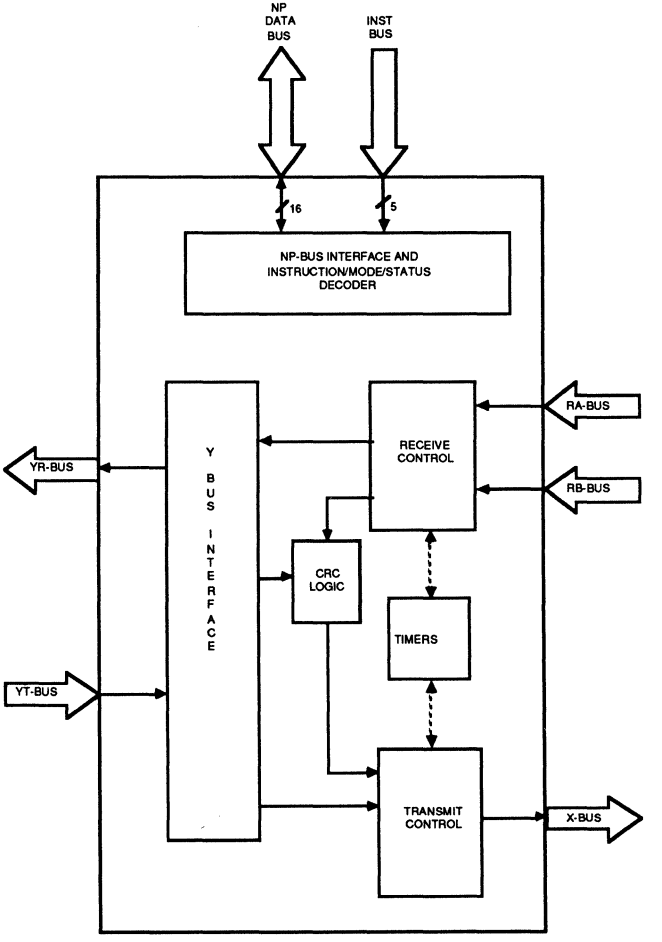
Fiber Optic Ring Media Access Controller (FORMAC)

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Implements Media Access Control (MAC) layer protocol for the ANSI X3T9.5 standard (Fiber Distributed Data Interface, FDDI)**
- **Error detection capability**
  - Cyclic redundancy checking and generation
  - Token claiming and beacon modes
- **Diagnostics Features**
  - Four loopback modes
  - Status bit collection
- **Supports data rates up to 100 Mbps**
- **Supports group, individual, and broadcast addressing**
- **Allows external address detection circuits**
  - Useful in bridge applications
- **Supports prioritized transmission of asynchronous messages**
- **Promiscuous mode for network monitoring**

BLOCK DIAGRAM



09731-001A

GENERAL DESCRIPTION

The Am79C83A Fiber Optic Ring Media Access Controller (FORMAC) is a CMOS device which implements the timed token passing protocol specified by the FDDI standard. It performs frame formation functions such as generating preamble, CRC, and status information. It facilitates error recovery with token claiming and beaconing capability. Information needed by station-management software for ring diagnostics and statistical network characterization is also provided by the FORMAC.

CONNECTION DIAGRAM
PGA Bottom View (Pins facing up)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
1	VCC	R/$\overline{W}$	INST2	INST1	$\overline{DS}$	NP15	NP13	NP11	NP8	NP4	NP2	NP1	$\overline{NMINTR}$	$\overline{READY}$	RAP	1
2	NC	$\overline{RESET}$	INST3	$\overline{CSI}$	NP14	NP12	NP10	NC	NP6	NP5	NP3	NP0	HOLD1	HOLD2	RACU	2
3	NC	YR7	BCLK	INST0	GND	BMODE	GND	NP9	VCC	NP7	GND	$\overline{MINTR}$	LPBEN	RA6	RACL	3
4	YR5	YR4	YR6	●									GND	RA7	NC	4
5	YR2	YR0	YRP										RA2	RA4	RA5	5
6	YT7	YR3	GND										RA3	RA1	RA0	6
7	VCC	YTP	YR1										VCC	RBP	RBCU	7
8	YT6	GND	GND					**Bottom View**					RBCL	RB7	NC	8
9	YT4	YT5	YT1										GND	RB5	RB6	9
10	YT2	YT0	RDYTBYT										RB4	RB3	RB2	10
11	XMTABTI	YT3	XMEDAVA										GND	RB1	RB0	11
12	XMTABTO	XMEDAVS	GND										XP	XCU	XCL	12
13	RECEIVE	XFRBYTE	FULL	MEDREQA	GND	LNGADR	$\overline{XSAMAT}$	GND	S1	LSTINC	X2	TOKISD	X7	X5	X6	13
14	DAVALID	RCVABTI	MISFRM	MEDREQS	INICLBN	$\overline{XDAMAT}$	COUT	GND	AOUT	FRINC	ERRINC	GND	X0	VCC	X4	14
15	FSHRCVF	RCVABTO	SI	TEST	CLM/$\overline{BEC}$	$\overline{FSVLD}$	SDRCVD	VCC	EOUT	S0	S2	S3	S0	X1	X3	15
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

NC = No Connection

09731–002A

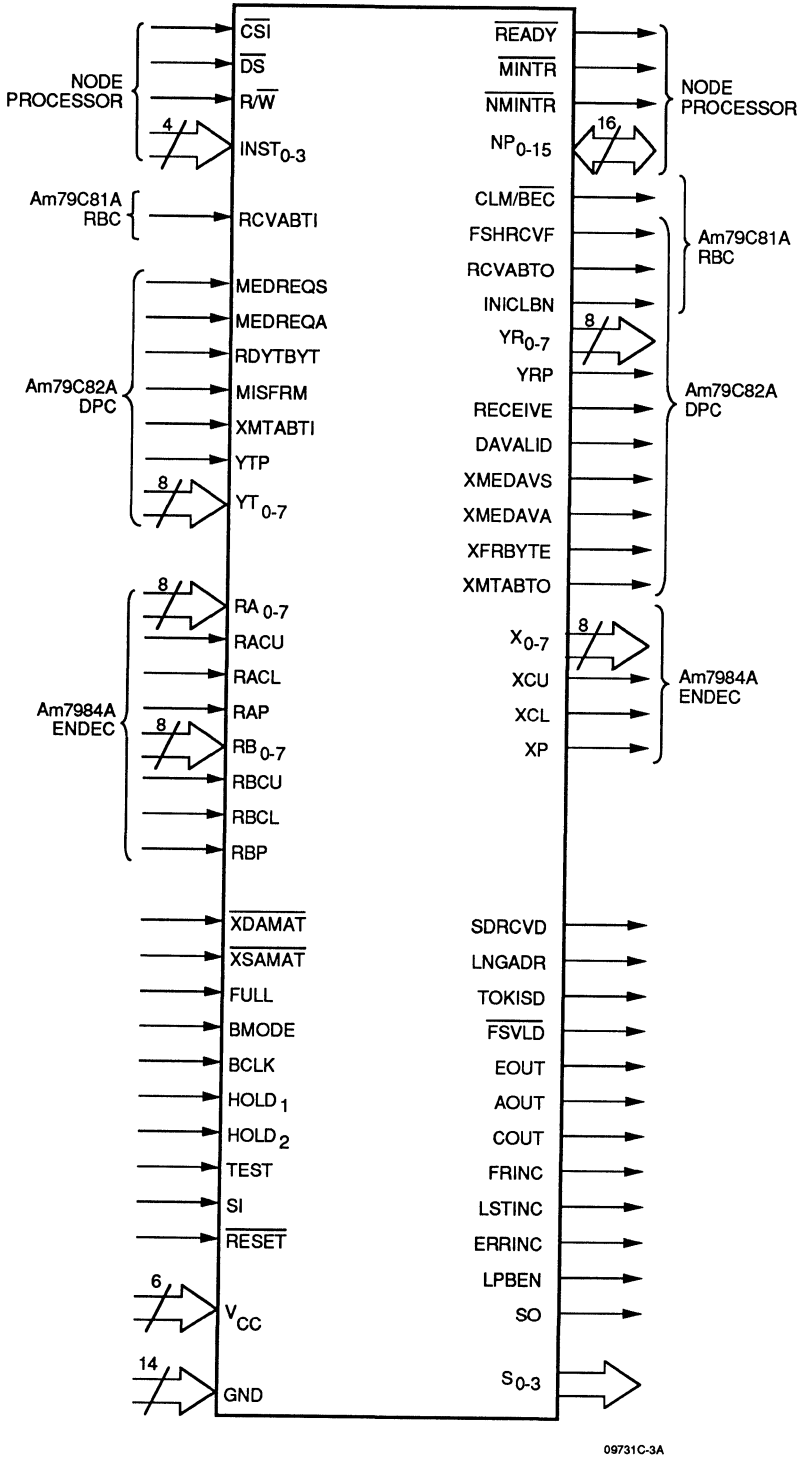
PIN DESIGNATIONS
(Sorted by Pin Number)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A–1	V_{CC}	C–7	YR_1	H–13	GND	N–10	RB_4
A–2	NC	C–8	GND	H–14	GND	N–11	GND
A–3	NC	C–9	YT_1	H–15	V_{CC}	N–12	XP
A–4	YR_5	C–10	RDYTBYT	J–1	NP_8	N–13	X_7
A–5	YR_2	C–11	XMEDAVA	J–2	NP_6	N–14	X_0
A–6	YT_7	C–12	GND	J–3	VCC	N–15	S_0
A–7	V_{CC}	C–13	FULL	J–13	S_1	P–1	$\overline{READY}$
A–8	YT_6	C–14	MISFRM	J–14	AOUT	P–2	$HOLD_2$
A–9	YT_4	C–15	SI	J–15	EOUT	P–3	RA_6
A–10	YT_2	D–1	$INST_1$	K–1	NP_4	P–4	RA_7
A–11	XMTABTI	D–2	$\overline{CSI}$	K–2	NP_5	P–5	RA_4
A–12	XMTABTO	D–3	$INST_0$	K–3	NP_7	P–6	RA_1
A–13	RECEIVE	D–4	GUIDE PIN	K–13	LSTINC	P–7	RBP
A–14	DAVALID	D–13	MEDREQA	K–14	FRINC	P–8	RB_7
A–15	FSHRCVF	D–14	MEDREQS	K–15	S_0	P–9	RB_5
B–1	$R/\overline{W}$	D–15	TEST	L–1	NP_2	P–10	RB_3
B–2	$\overline{RESET}$	E–1	$\overline{DS}$	L–2	NP_3	P–11	RB_1
B–3	YR_7	E–2	NP_{14}	L–3	GND	P–12	XCU
B–4	YR_4	E–3	GND	L–13	X_2	P–13	X_5
B–5	YR_0	E–13	GND	L–14	ERRINC	P–14	VCC
B–6	YR_3	E–14	INICLBN	L–15	S_2	P–15	X_1
B–7	YTP	E–15	CLM/$\overline{BEC}$	M–1	NP_1	R–1	RAP
B–8	GND	F–1	NP_{15}	M–2	NP_0	R–2	RACU
B–9	YT_5	F–2	NP_{12}	M–3	$\overline{MINTR}$	R–3	RACL
B–10	YT_0	F–3	BMODE	M–13	TOKISD	R–4	NC
B–11	YT_3	F–13	LNGADR	M–14	GND	R–5	RA_5
B–12	XMEDAVS	F–14	$\overline{XDAMAT}$	M–15	S_3	R–6	RA0
B–13	XFRBYTE	F–15	$\overline{FSVLD}$	N–1	$\overline{NMINTR}$	R–7	RBCU
B–14	RCVABTI	G–1	NP_{13}	N–2	$HOLD_1$	R–8	NC
B–15	RCVABTO	G–2	NP_{10}	N–3	LPBEN	R–9	RB_6
C–1	$INST_2$	G–3	GND	N–4	GND	R–10	RB_2
C–2	$INST_3$	G–13	$\overline{XSAMAT}$	N–5	RA_2	R–11	RB_0
C–3	BCLK	G–14	COUT	N–6	RA_3	R–12	XCL
C–4	YR_6	G–15	SDRCVD	N–7	VCC	R–13	X_6
C–5	YRP	H–1	NP_{11}	N–8	RBCL	R–14	X_4
C–6	GND	H–2	NC	N–9	GND	R–15	X_3
		H–3	NP_9				

PIN DESIGNATIONS
(Sorted by Pin Name)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
J–14	AOUT	F–13	LNGADR	P–11	RB_1	P–13	X_5
C–3	BCLK	N–3	LPBEN	R–10	RB2	R–13	X_6
F–3	BMODE	K–13	LSTINC	P–10	RB_3	N–13	X_7
E–15	CLM/$\overline{\text{BEC}}$	D–13	MEDREQA	N–10	RB_4	R–12	XCL
G–14	COUT	D–14	MEDREQS	P–9	RB_5	P–12	XCU
D–2	$\overline{\text{CSI}}$	M–3	$\overline{\text{MINTR}}$	R–9	RB_6	F–14	$\overline{\text{XDAMAT}}$
A–14	DAVALID	C–14	MISFRM	P–8	RB_7	B–13	XFRBYTE
E–1	$\overline{\text{DS}}$	N–1	$\overline{\text{NMINTR}}$	N–8	RBCL	C–11	XMEDAVA
J–15	EOUT	M–2	NP_0	R–7	RBCU	B–12	XMEDAVS
L–14	ERRINC	M–1	NP_1	P–7	RBP	A–11	XMTABTI
K–14	FRINC	L–1	NP_2	B–14	RCVABTI	A–12	XMTABTO
A–15	FSHRCVF	L–2	NP_3	B–15	RCVABTO	N–12	XP
F–15	$\overline{\text{FSVLD}}$	K–1	NP_4	C–10	RDYTBYT	G–13	$\overline{\text{XSAMAT}}$
C–13	FULL	K–2	NP_5	P–1	$\overline{\text{READY}}$	B–5	YR0
H–14	GND	J–2	NP_6	A–13	RECEIVE	C–7	YR_1
E–13	GND	K–3	NP_7	B–2	$\overline{\text{RESET}}$	A–5	YR_2
B–8	GND	J–1	NP_8	K–15	S_0	B–6	YR_3
G–3	GND	H–3	NP_9	J–13	S_1	B–4	YR_4
N–9	GND	G–2	NP_{10}	L–15	S_2	A–4	YR_5
E–3	GND	H–1	NP_{11}	M–15	S_3	C–4	YR_6
C–6	GND	F–2	NP_{12}	G–15	SDRCVD	B–3	YR_7
M–14	GND	G–1	NP_{13}	C–15	SI	C–5	YRP
N–11	GND	E–2	NP_{14}	N–15	SO	B–10	YT_0
C–8	GND	F–1	NP_{15}	D–15	TEST	C–9	YT_1
N–4	GND	B–1	R/$\overline{\text{W}}$	M–13	TOKISD	A–10	YT_2
C–12	GND	R–6	RA0	A–1	VCC	B–11	YT_3
H–13	GND	P–6	RA_1	N–7	V_{CC}	A–9	YT_4
L–3	GND	N–5	RA_2	J–3	V_{CC}	B–9	YT_5
D–4	GUIDE PIN	N–6	RA_3	A–7	V_{CC}	A8	YT_6
N–2	$HOLD_1$	P–5	RA_4	P–14	V_{CC}	A–6	YT_7
P–2	$HOLD_2$	R–5	RA_5	H–15	V_{CC}	B–7	YTP
E–14	INICLBN	P–3	RA_6	N–14	X_0	R–4	NC
D–3	$INST_0$	P–4	RA_7	P–15	X_1	A–3	NC
D–1	$INST_1$	R–3	RACL	L–13	X_2	A–2	NC
C–1	$INST_2$	R–2	RACU	R–15	X3	R–8	NC
C–2	$INST_3$	R–1	RAP	R–14	X_4	H–2	NC
		R–11	RB0				

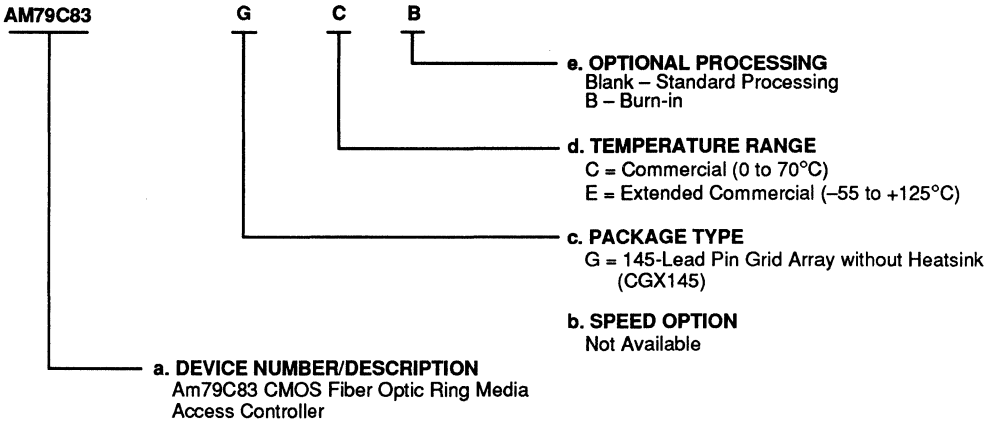
LOGIC SYMBOL



ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM79C83	GC, GCB, GE, GEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Preliminary

Am7984A

FDDI ENcoder DECoder (ENDEC)

Advanced Micro Devices

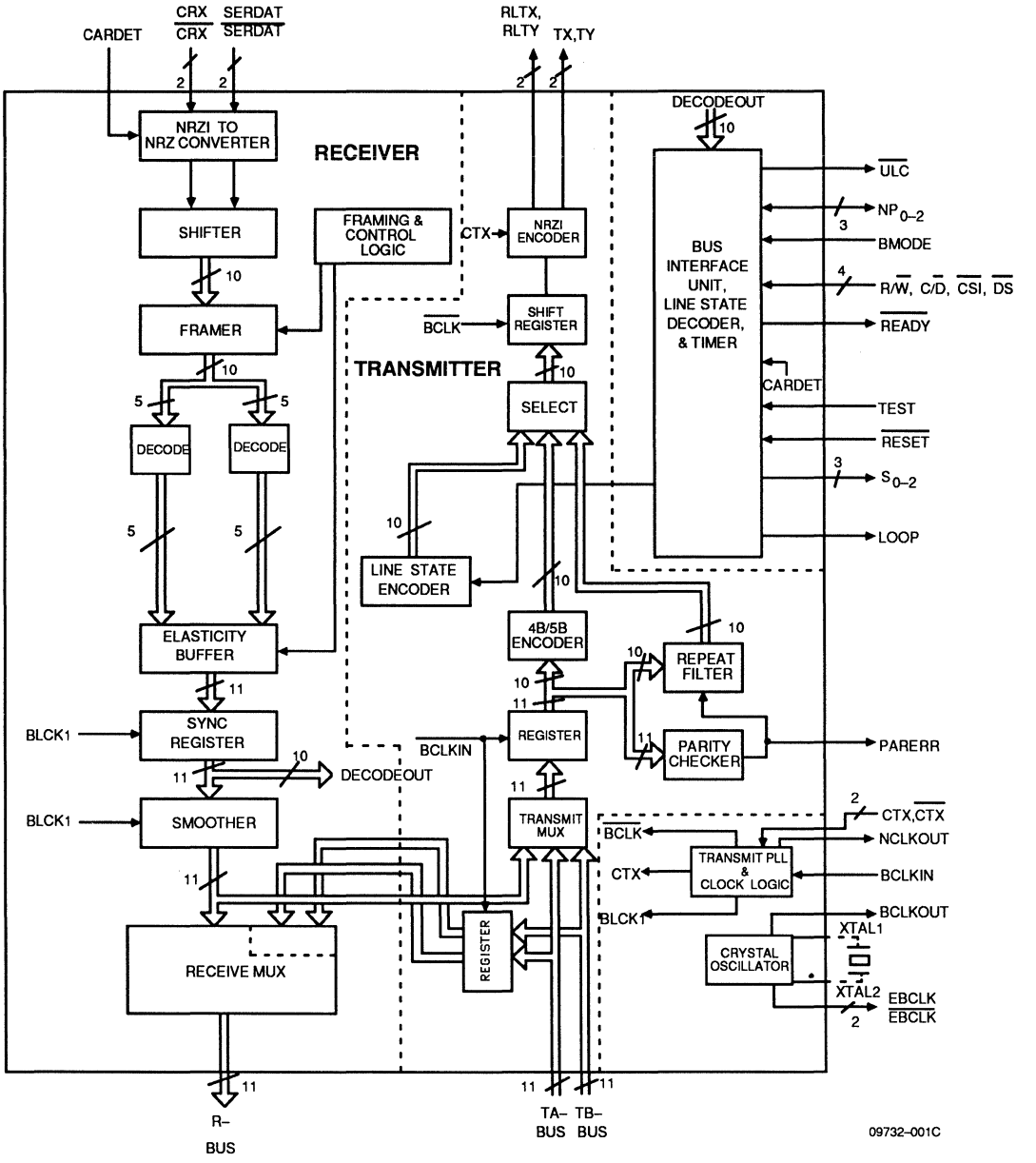
DISTINCTIVE CHARACTERISTICS

- **Implements 4B/5B encoding/decoding as specified by the ANSI X3T9.5 Fiber Distributed Data Interface (FDDI) standard**
- **100 Mbps, 125 MBaud serial data-rate**
- **Byte-clock and nibble-clock output**
- **Selectable loopback and repeat modes**
- **Elasticity Buffer**
- **Smoother**
- **Repeat filter**
- **Single +5-V supply**

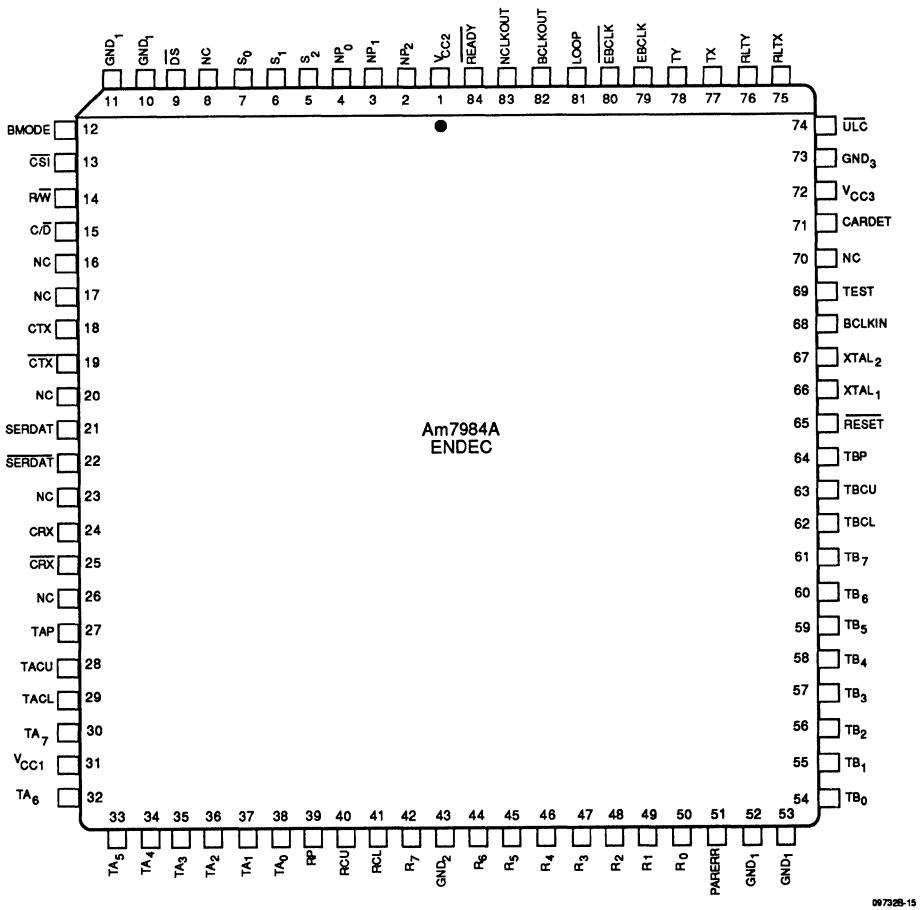
GENERAL DESCRIPTION

The Am7984A ENDEC (ENcoder DECoder) performs 4B/5B encoding on data to be transmitted from an FDDI station. The chip also performs 4B/5B decoding of received data. It has an elasticity buffer which allows a station to compensate for small differences between receive and transmit clock frequencies. There is a smoother present in the receive path to ensure with a very high probability that a minimum of 6 bytes of IDLE are received before a frame. It also decodes line state information from data that has been received from the network media, and enables line states to be forced onto the media for connection management purposes. A repeat filter replaces any invalid symbols with other symbols that are determined by the repeat filter state machine. The ENDEC interfaces to the FORMAC through two 11-bit transmit buses and one 11-bit receive bus. Data is serially transferred to an optical transmitter by a differential driver. The ENDEC interfaces to the Node Processor (NP) through a 3-bit bus and associated handshake lines. It also supplies the master clock for the network interface of the station.

BLOCK DIAGRAM

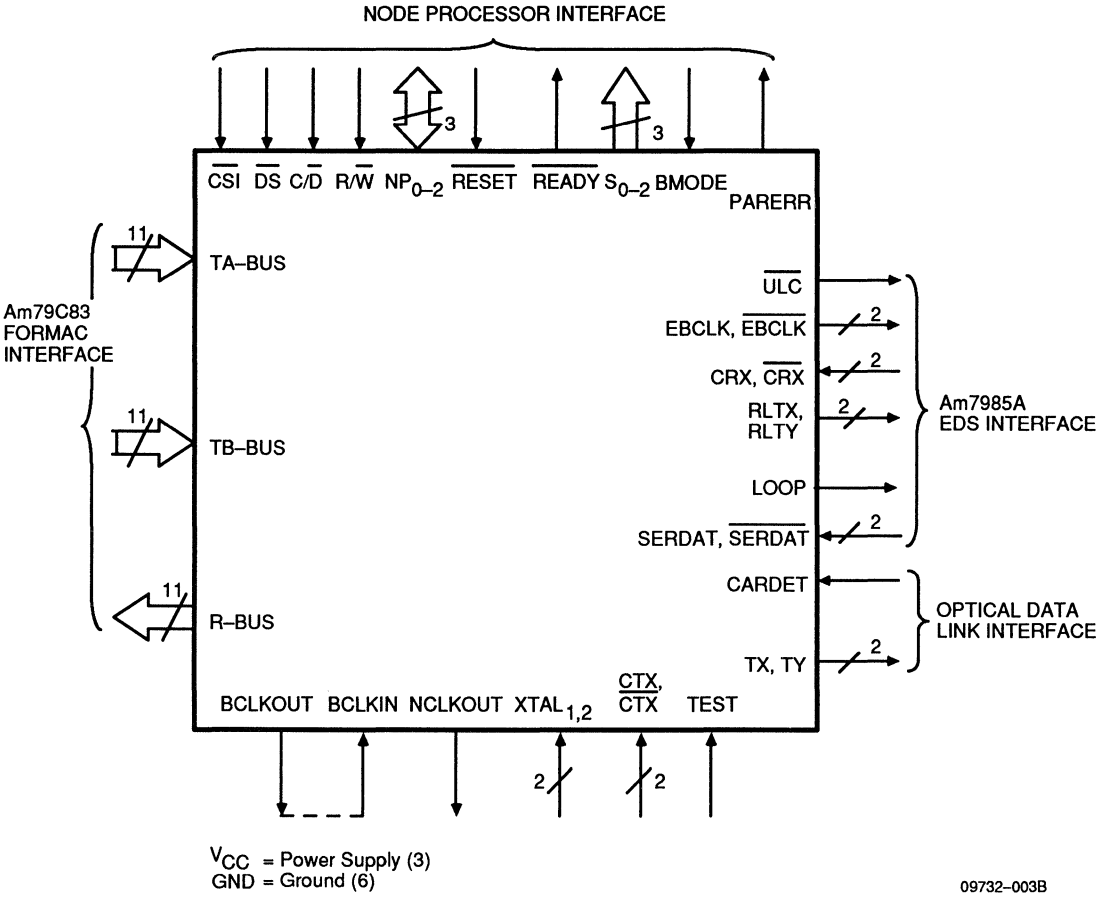


CONNECTION DIAGRAM (Top View)
PLCC 084



09732-002C

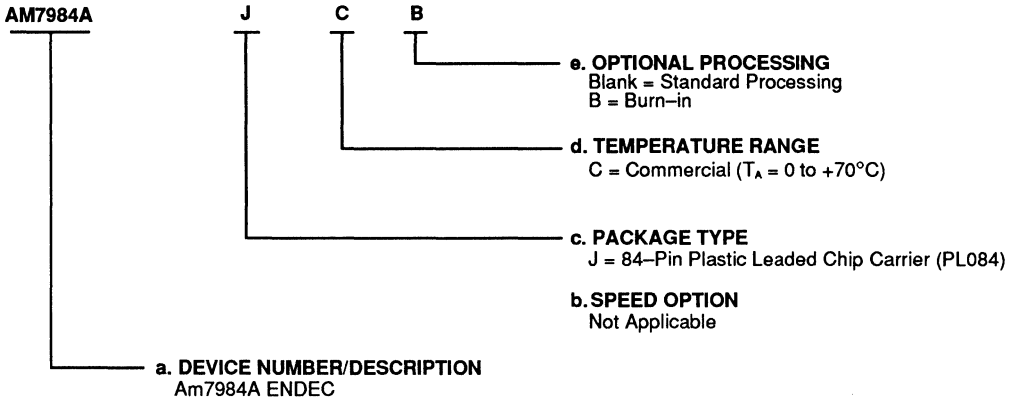
LOGIC SYMBOL



ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7984A	JC, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Preliminary

Am7985A

FDDI ENDEC Data Separator (EDS)

Advanced Micro Devices

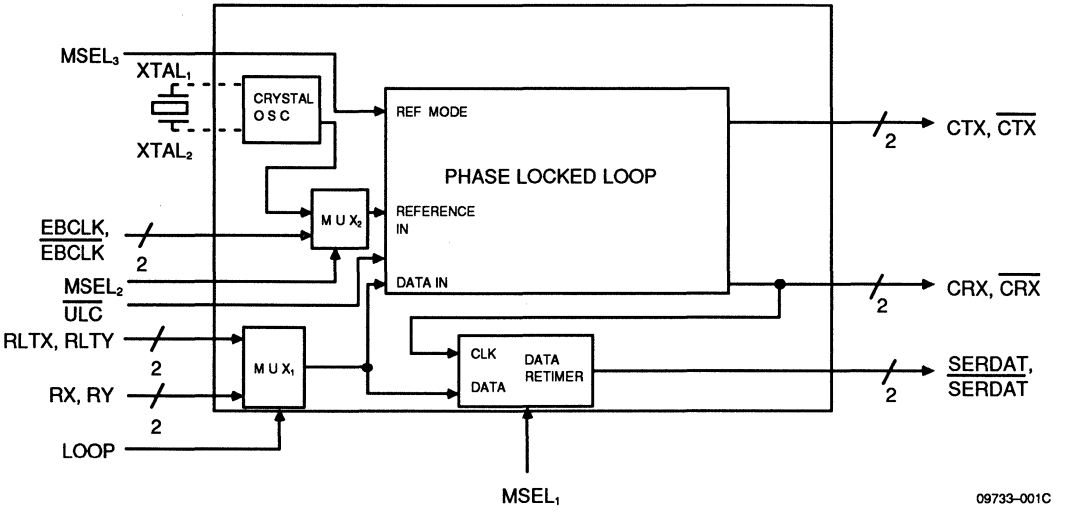
DISTINCTIVE CHARACTERISTICS

- **100 Mbps, 125 MBaud serial input**
- **Clock recovery**
- **Meets ANSI X3T9.5 Jitter Requirements**
- **Selectable loopback modes**
- **Single +5-V supply**

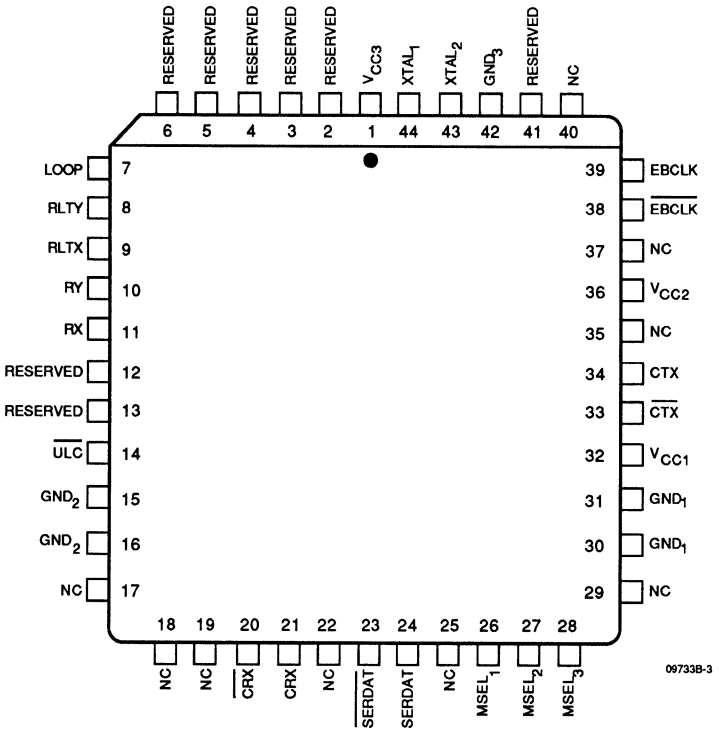
GENERAL DESCRIPTION

The Am7985A ENDEC Data Separator (EDS) recovers clock and data from an FDDI bit stream. Running from a single +5-V supply, this device needs only a clock source (generally provided by an Am7984A ENDEC) to fulfill its role in the AMD SUPERNET chip set.

BLOCK DIAGRAM

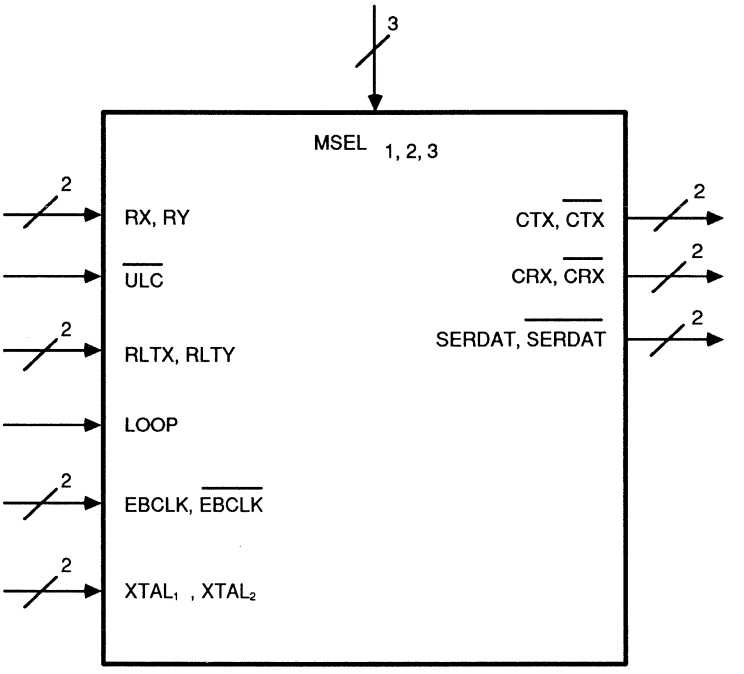


CONNECTION DIAGRAM
PL044 (Top View)



09733-002C

LOGIC SYMBOL



V_{CC} = Power (3)
GND = Ground (3)

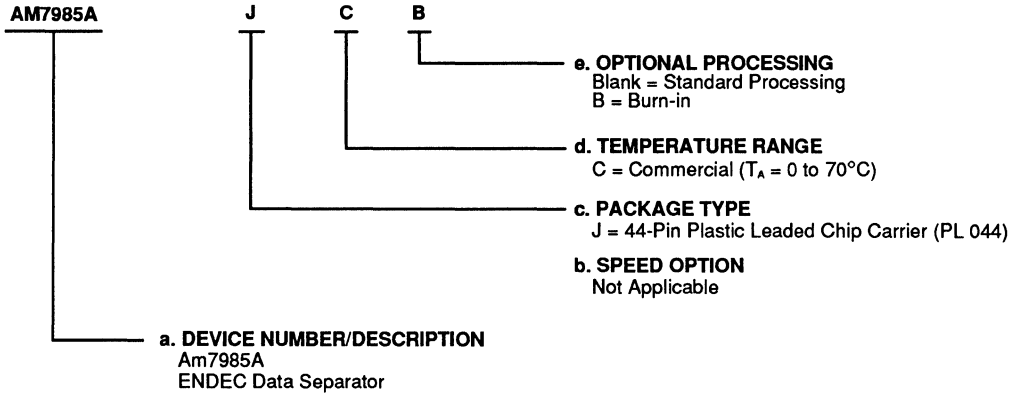
09733–003C

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7985A	JC, JCB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

NETWORKING PRODUCTS

Support Tools

TAXIchip™ EVALUATION SYSTEM

AmTAXIEVAL1: TAXI MINIcab Development Board

The AmTAXIEVAL1 MINIcab Development Board provides a versatile tool to ease the development of a high-speed point-to-point communications link. The board has been designed using independent power supplies, grounds, and crystals to emulate a realistic half-duplex environment. Parallel TTL data from any host or prototype system can be loaded into the TAXI MINIcab using a simple strobe/ACK handshake. The parallel data is serialized and transmitted across the media. Data received from the media is then re-converted to parallel form for the destination system. The MINIcab operates over the data rate range of 32 - 100 Mbp (4-12.5 Mbytes/sec) and can be used with a variety of media such as fiber optic cable or various copper cables.

ETHERNET EVALUATION SYSTEMS

ETHNEVAL5 : Ethernet/Cheapernet PC/AT Half Card Kit

The Ethernet/Cheapernet/IEEE 802.3 AT half card (ETHNEVAL5) is an evaluation tool for AMD's 7990 Ethernet/Cheapernet chipset. It is intended for use in IBM PC/AT and compatible machines, and represents a low-component count, minimum board space, and low-cost network adapter implementation. The card supports both standard Ethernet and Cheapernet with an onboard transceiver. Choice of network operation is jumper selectable.

Despite the card's low cost, it is still a high-performance design since it takes full advantage of the AT's multi-mastering I/O bus. When installed in a target machine, the system becomes a platform upon which to evaluate network hardware and to develop software for a complete node processor. The software designer can take full advantage of the many development tools available for the AT - compilers, assemblers and debuggers.

The evaluation card comes with a distribution diskette of software. The software includes a high-level demonstration program, a low-level Driver/Monitor and Novell Netware™ Driver object code. The demonstration program contains an ISO data link layer with a menu driven packet which lets the user assign physical and logical addresses, establish connections, send and receive messages. The Driver/Monitor lets the user view and change the content of the LANCE's registers, the Initialization Block and the Descriptor Rings. The program also allows the user to establish loops for data probing. The Novell Netware object code transforms the AT half card into a cost-effective, competitive and manufacturing ready commercial board-level product. Our customers can evaluate the performance of the AMD Ethernet chip set in a real PC LAN system. The AT half card is certified by Novell together with this set of software drivers. The performance of the AT half card is excellent compared to commercially available products.

In addition to the card and the software diskette, the kit comes with a user's manual including schematic diagrams, device specifications, device application notes, a local area network controller technical manual, the Am7990 Family Products Brochure and hook-up coax cable hardware.

Am7996EVAL: Stand-Alone Transceiver Kit

The Am7996EVAL is an evaluation tool for AMD's Am7996 IEEE 802.3 compatible Ethernet Transceiver. This is a very simple evaluation kit which consists of a 3 x 3 inch stand-alone evaluation card which integrates the Am7996 along with external components with a DC-DC converter into an optimized PC board layout. The board interfaces to an Ethernet controller via a 15-pin connector. It also interfaces to the coax cable, a terminated RG 58 (A/U or C/U) cable segments, via a BNC connector for communicating with other nodes in a network.

In addition to the card, the kit also comes with a device specification, device application note, schematic diagram of the board and the Am7990 Family Products Brochure.

FDDI EVALUATION SYSTEM

AmFDDI-PC-AT: Fast Card (IBM PC/AT and Compatible Demonstration Board)

The FAST Card is an evaluation tool for AMD's SUPERNET chipset. It is also an ideal vehicle for FDDI software development and interoperability testing. It is a single-attach FDDI station, but multiple boards can be connected with a ribbon cable to build dual-attach single-MAC or dual attach, dual-MAC stations or concentrators. This low-cost design contains a fiber optic transmitter and receiver, the SUPERNET chipset, buffer memory, and CMT logic.

A variety of software, written in "C", is included with the board: FDDIMON (source and binary code) is a low-level debugger, FDDINET (binary code only, source code is licensed separately) contains SUPERNET chip driver's and CMT functionality; FDDI DEMO (source and binary code) is a menu driven, higher-level demonstration package to perform file transfers etc. FDDINET and FDDIDEMO both run under the VRTX real time kernel, which is also included in the kit. Finally, CMT-Emulator is a stand-alone learning tool which illustrates how connection management (CMT) operates.

In addition to the board and software, the kit also contains 10 feet of fiber optic cables, a SUPERNET data book, technical manual and manuals for the board and each software package.

COMMUNICATION PROCESSORS

Compression/Expansion Processors

The Am7971A Compresion/Expansion Processor (CEP) and Am95C71 Video Compression/Expansion Processor (VCEP) employ internationally accepted CCITT Group III and Group IV standards for the compression and expansion of black-or-white bit-mapped images. These standards, originally written for facsimile applications, have found their way into a wide variety of applications such as scanners, laser printers, data storage and retrieval systems, and networks. In particular, the VCEP processes data in human reaction time making it well suited for high-speed document processing applications.

Burst Error Processor

AMD's Am9520 Burst Error Processor (BEP) provides error detection and correction of high-speed serial data. Industry standard polynomials and three correction algorithms are user selectable proving flexibility in a number of applications including high-performance hard- and floppy-disks.

Data Ciphering Processor

The Am9568 and Am9518/AmZ8068 DCP implements the National Bureau of Standards data encryption algorithm providing data security in sensitive high-speed telecommunication and disk applications.

Serial Communications Controller

AMD's Z85C30 is an enhanced pin-compatible version of the popular Z8530/Z85C30 Serial Communications Controller. This enhanced version is a high speed, low power, multi-protocol communications peripheral designed for use with 8- and 16-bit microprocessors. It has two independent, full duplex channels and functions as a serial-to-parallel, parallel-to-serial converter/controller. AMD's proprietary enhancements make the 85C30 more effective in high speed applications and improves system interface due to a reduction in software burden and the elimination of the need for some external gule logic. This versatile device supports virtually any serial data transfer application such as networks, modems, cassettes and tape drives.

Am7971A

Compression Expansion Processor
(CEP with image bit-boundary processing)

DISTINCTIVE CHARACTERISTICS

- Image preserving compression and expansion of two-tone image using run-length (one-dimensional) coding and relative element address (two-dimensional) coding.
- Compatible with internationally accepted CCITT Group III and IV (Recommendations T.4 and T.6) image compression standards.
- Image bit-boundary operations.
- High performance of 1 to 12 MHz pixel rates with 3, 5, and 8MHz clock.
- CPU bus and optional local Document Store Bus with on-chip DMA. The CEP can address up to 16Mbytes on each bus.
- Handles four memory buffers: source and destination buffers for both the compressor and expander.
- Full duplex mode for simultaneous compressor and expander operations with each processor independently programmable.
- On-chip error detection to catch data corruptions and support for easy error recovery.
- 46 user programmable registers allow for very easy and highly flexible system implementation. Includes:
  - Programmable page width (up to 16K pels), frame width and top, left and right margins.
  - Optional Express mode during compression and Granularity mode during expansion for vertical resolution conversion.
  - Programmable K parameter.
  - Optional Wraparound mode.
  - Transparent mode.

GENERAL DESCRIPTION

The Am7971A Compression Expansion Processor (CEP) with Image Bit-Boundary Processing capacity is a high performance peripheral which compresses and expands two-tone bit mapped images or documents in accordance with internationally accepted CCITT standards. These fully image preserving algorithms reduce storage requirements and data transmission time for systems handling bit-mapped data.

The Am7971A is a functionally enhanced version of the Am7971 offering improved negative compression and error recovery performance. The Am7971A can replace the Am7971 in existing systems without board/system/timing alterations.

The Am7971A performs one-dimensional Modified Hoffman (MH) run-length coding as well as two-dimensional Modified READ (MR/MMR) relative coding as specified in CCITT Recommendations T.4 and T.6 for Group III and Group IV compatible equipments. The typical compression ratio for the eight CCITT test documents is 5:1 to 50:1.

The compressor and expander operate not only in full duplex mode but each processor can be independently programmed for one-dimensional encoding/decoding, two-dimensional encoding/decoding, or transparent data transfer.

Equipped with an on-chip error detection mechanism, the Am7971A detects data corruptions by checking for illegal codes, negative run-lengths and incorrect line lengths. Furthermore, its architecture allows for error recovery with minimal CPU intervention.

With 46 user programmable registers, standard Am8088-like microprocessor bus interface, dual bus architecture and on-chip DMA the Am7971A offers tremendous system flexibility and ease of implementation. After initialization the Am7971A will operate with minimal CPU overhead. Its status is available through polled registers and exception conditions may be signalled using an external interrupt.

Document page width is programmable up to 16K picture elements (pels). Programmable frame width enable windowing features and programmable top, left and right margins allow image boundaries to be left blank.

Optional express mode allows one line to be skipped after every 'nth' line to accelerate compression (n = 1 to 255). On the expansion side, the granularity option allows the processor to duplicate every mth line (m = 1 to 7).

In two-dimensional mode, the programmable K-parameter (k = 1 to 255 and infinity) defines the number of lines to be encoded in 2-D coding sequence before a 1-D line is inserted. For error free environments (Group 4) K = infinity allows for maximum compression.

The CEP can address up to 16 Mbytes of memory on each bus and two buffers (source and destination) on both the compressor and expander. Starting address, buffer length and current address for image and coded data are stored in internal registers independently for both the compressor and expander.

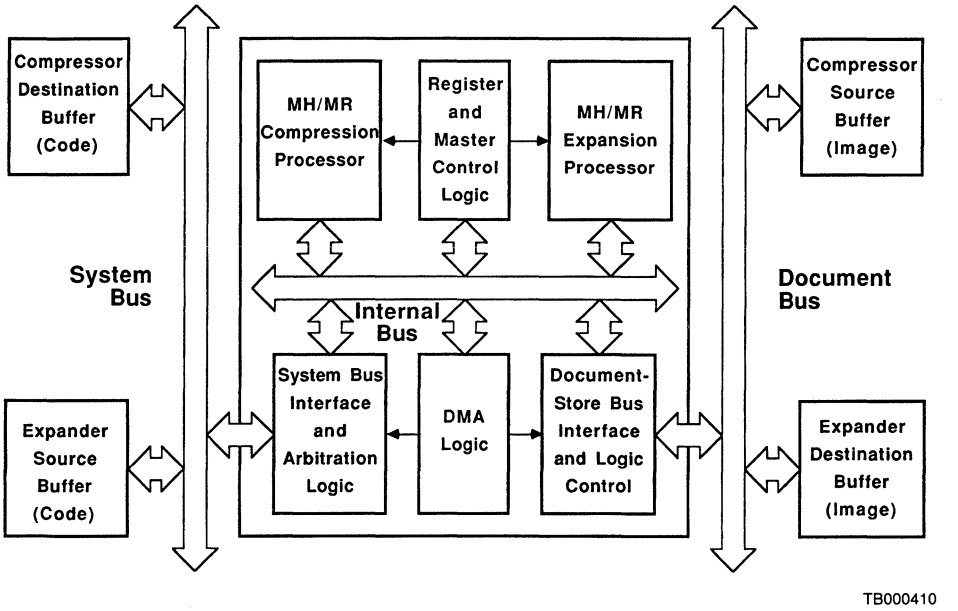


Figure 1. Am7971A Block Diagram

RELATED AMD PRODUCTS	
Part No.	**Description**
Am7971A EVAL	Am7971A Evaluation Board

CONNECTION DIAGRAMS
Top View

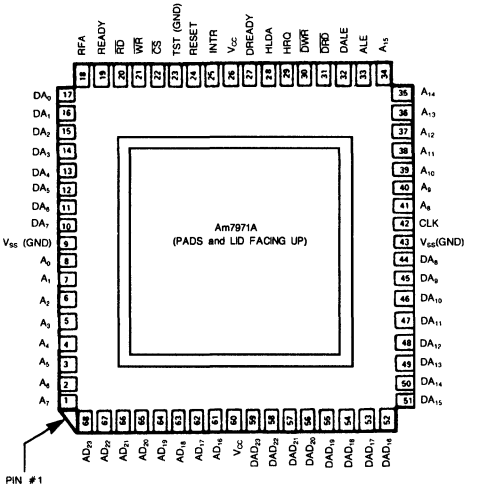


Figure 2. Am7971A Pinout for Leadless Chip Carrier (LCC)

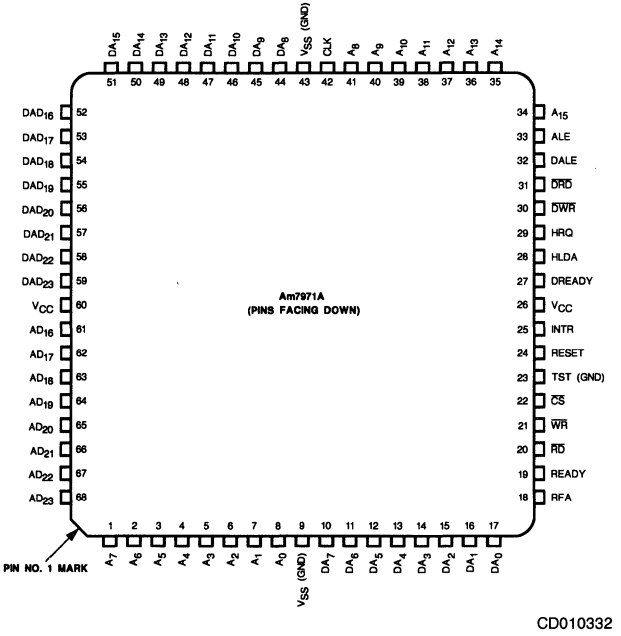


Figure 3. Am7971A Pinout for Plastic Leaded Chip Carrier (PLCC)

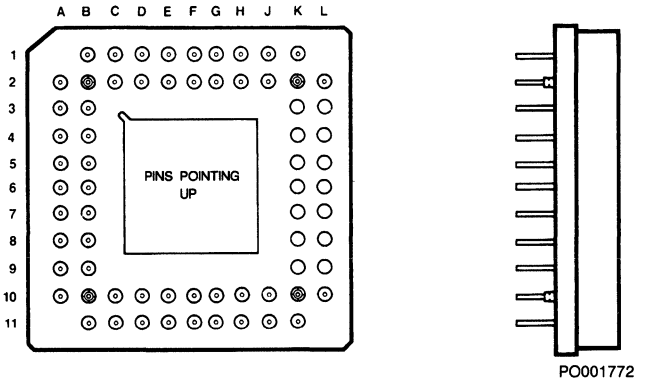


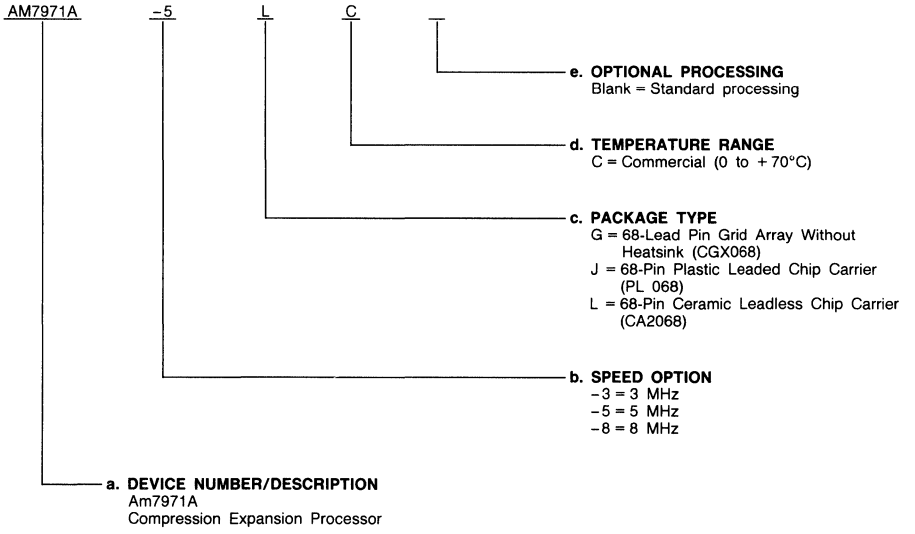
Figure 4. Am7971A (CEP) Pinout for a Pin Grid Array (PGA) Package

PIN DESIGNATIONS							
(SORTED BY PIN NAME)				(SORTED BY PIN NUMBER)			
PIN NAME	**PIN NO.**	**PIN NAME**	**PIN NO.**	**PIN NO.**	**PIN NAME**	**PIN NO.**	**PIN NAME**
A_0	E-2	**DA_7**	F-2	**A-2**	AD_{23}	**G-1**	DA_6
A_1	E-1	**DA_8**	F-10	**A-3**	AD_{21}	**G-2**	DA_5
A_2	D-2	**DA_9**	E-11	**A-4**	AD_{19}	**G-10**	CLK
A_3	D-1	**DA_{10}**	E-10	**A-5**	AD_{17}	**G-11**	A_8
A_4	C-2	**DA_{11}**	D-11	**A-6**	V_{CC}	**H-1**	DA_4
A_5	C-1	**DA_{12}**	D-10	**A-7**	DAD_{22}	**H-2**	DA_3
A_6	B-2	**DA_{13}**	C-11	**A-8**	DAD_{20}	**H-10**	A_9
A_7	B-1	**DA_{14}**	C-10	**A-9**	DAD_{18}	**H-11**	A_{10}
A_8	G-11	**DA_{15}**	B-11	**A-10**	DAD_{16}	**J-1**	DA_2
A_9	H-10	**DAD_{16}**	A-10	**B-1**	A_7	**J-2**	DA_1
A_{10}	H-11	**DAD_{17}**	B-10	**B-2**	A_6	**J-10**	A_{11}
A_{11}	J-10	**DAD_{18}**	A-9	**B-3**	AD_{22}	**J-11**	A_{12}
A_{12}	J-11	**DAD_{19}**	B-9	**B-4**	AD_{20}	**K-1**	DA_0
A_{13}	K-10	**DAD_{20}**	A-8	**B-5**	AD_{18}	**K-2**	READY
A_{14}	K-11	**DAD_{21}**	B-8	**B-6**	AD_{16}	**K-3**	$\overline{WR}$
A_{15}	L-10	**DAD_{22}**	A-7	**B-7**	DAD_{23}	**K-4**	TST (GND)
AD_{16}	B-6	**DAD_{23}**	B-7	**B-8**	DAD_{21}	**K-5**	INTR
AD_{17}	A-5	**DALE**	L-9	**B-9**	DAD_{19}	**K-6**	DREADY
AD_{18}	B-5	**$\overline{DRD}$**	K-8	**B-10**	DAD_{17}	**K-7**	HRQ
AD_{19}	A-4	**DREADY**	K-6	**B-11**	DA_{15}	**K-8**	$\overline{DRD}$
AD_{20}	B-4	**$\overline{DWR}$**	L-8	**C-1**	A_5	**K-9**	ALE
AD_{21}	A-3	**HLDA**	L-7	**C-2**	A_4	**K-10**	A_{13}
AD_{22}	B-3	**HRQ**	K-7	**C-10**	DA_{14}	**K-11**	A_{14}
AD_{23}	A-2	**INTR**	K-5	**C-11**	DA_{13}	**L-2**	RFA
ALE	K-9	**$\overline{RD}$**	L-3	**D-1**	A_3	**L-3**	$\overline{RD}$
CLK	G-10	**READY**	K-2	**D-2**	A_2	**L-4**	$\overline{CS}$
$\overline{CS}$	L-4	**RESET**	L-5	**D-10**	DA_{12}	**L-5**	RESET
DA_0	K-1	**RFA**	L-2	**D-11**	DA_{11}	**L-6**	V_{CC}
DA_1	J-2	**TST (GND)**	K-4	**E-1**	A_1	**L-7**	HLDA
DA_2	J-1	**V_{CC}**	A-6	**E-2**	A_0	**L-8**	$\overline{DWR}$
DA_3	H-2	**V_{CC}**	L-6	**E-10**	DA_{10}	**L-9**	DALE
DA_4	H-1	**V_{SS} (GND)**	F-1	**E-11**	DA_9	**L-10**	A_{15}
DA_5	G-2	**V_{SS} (GND)**	F-11	**F-1**	V_{SS}		
DA_6	G-1	**$\overline{WR}$**	K-3	**F-2**	DA_7		
				F-10	DA_8		
				F-11	V_{SS}		

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM7971A-3	JC
AM7971A-5	GC, JC, LC
AM7971A-8	GC, LC

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Am95C71

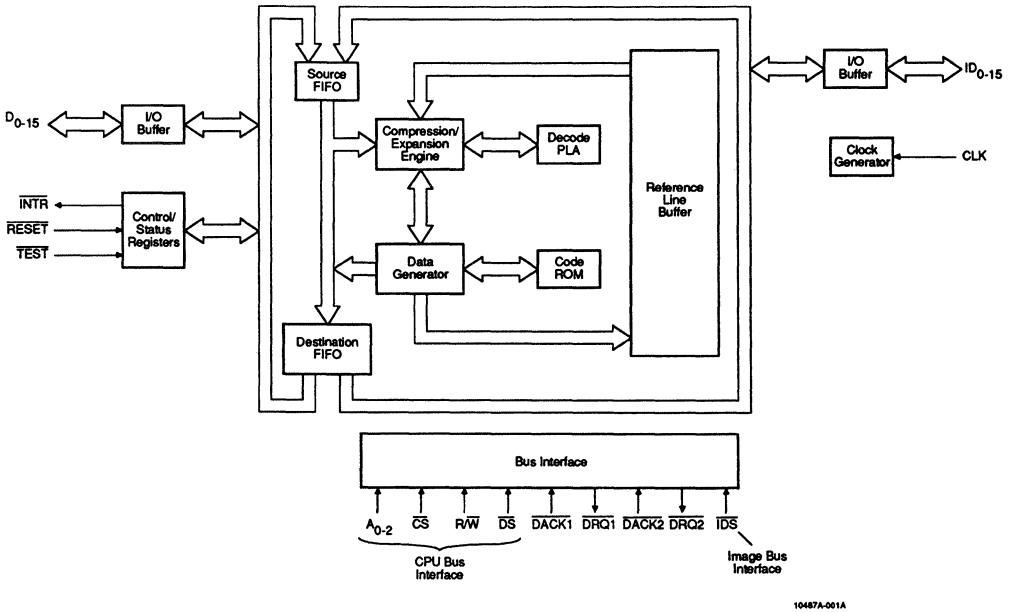
Video Compression/Expansion Processor (VCEP)

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

- Throughput exceeding an average rate of 50 Mb/s when compressing or expanding
- Full CCITT Group 3 and Group 4 compression/expansion: allows MH, MR and MMR coding and transparent mode
- Dual-bus architecture with single-bus mode option
- Supports bit-boundary image width up to 8191 pixels in one-dimensional (1D) mode and 6911 pixels in two-dimensional (2D) mode
- Has on-chip 6911-pixel reference-line buffer allowing high-performance 2D coding
- Provides error detection and recovery capability
- Supports programmable k-Parameter for 2D coding
- 16-word FIFOs on input and output
- Half-duplex operation

BLOCK DIAGRAM



BD008180

GENERAL DESCRIPTION

The Am95C71 Video Compression/Expansion Processor (VCEP) is a high-performance CMOS processor which compresses and expands binary image data using the internationally standardized CCITT Group 3 and Group 4 algorithms.

The VCEP supports the Modified Huffman (MH), Modified Read (MR), and Modified-Modified Read (MMR) coding schemes used by the CCITT Groups 3 and 4 standards. MH coding is a one-dimensional technique which identifies and then codes run-lengths of black or white pixels. MR coding compresses a single scan line using MH coding, followed by k-1 scan lines coded in such a way as to reflect differences from the pixel patterns of the previous scan line (two-dimensional or 2D coding); the value of the k-Parameter is defined by the user and will generally be set to a larger number on communication links with lower bit-error rates.

MMR coding is a full 2D-coding scheme which uses an all-white imaginary reference line when coding the first scan line. All lines on the page are coded two-dimensionally. For a typical binary image, MMR coding offers the best compression, followed by MR and then MH. Compressed data may be corrupted during transmission or storage. Error-free (or error-protected) transmission media are used with Group 4 coding, since error recovery is not possible. The CCITT standard refers to MH and MR coding as Group 3 techniques and MMR coding as a Group 4 technique. Group 3 error recovery facility is provided on the VCEP.

The extent of data compression provided by Group 3 and Group 4 compression techniques depends on the specific data patterns contained in the image. Typically, an originally black-or-white (binary) image will yield compression ratios between 5:1 and 50:1, whereas a binary image produced from a grey-scale or color original may compress poorly, even resulting in a compressed file larger than the raw image. Alternatively, the user may program the VCEP into transparent mode where data is simply passed from source FIFO to destination FIFO without compressing or modifying the data.

When 2D (MR or MMR) coding is performed, the previous scan line is used as a reference to code the current line. To significantly increase performance the VCEP stores the reference line in an on-chip buffer.

The VCEP is a slave-mode device with two 16-bit bus interfaces. The user may select either bus to be source or destination and the VCEP to compress, expand or pass through (transparent mode) data. Data is buffered on input and output by 16-word FIFOs. The VCEP, therefore, may be used as a single-bus or dual-bus device, with FIFO buffers on input and output.

The VCEP may either compress, expand, or pass through data; it cannot do these functions simultaneously or in a multiplexed fashion and is therefore termed a half-duplex device.

However, it is possible for the VCEP to multiplex data compression from several sources if a full scan line is processed from each source, and MH coding is selected. Multiplexed expansion is not supported.

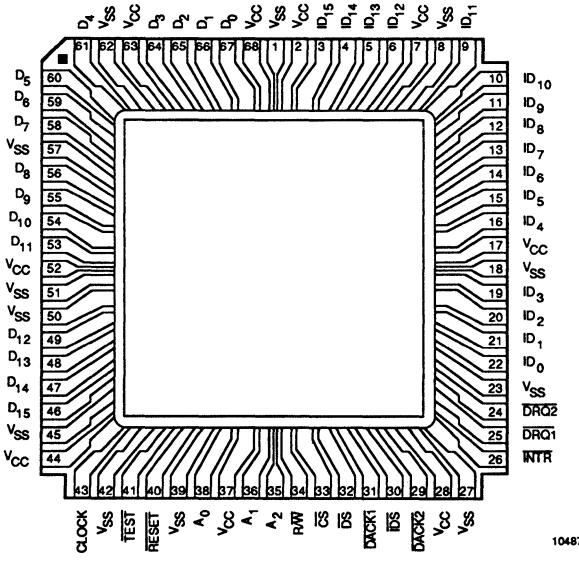
The VCEP has several mechanisms to detect data errors on expansion. For MH and MR modes, if the expanded scan line is longer or shorter than the user-programmed length, the VCEP sets a flag and halts. Illegal codes, negative run lengths in 2D coding, and other illegal fields are detected as errors. Since the VCEP has no on-chip DMA, the host CPU is responsible for error recovery; for example, by replicating the previous scan line when an error is found in the current scan line.

The VCEP has programmable bus burst and dwell counters to allow the user control over the length of the VCEP's data requests and the time between requests.

All registers on the VCEP are set up by the CPU via the VCEP's CPU bus, selecting specific registers with three address lines. In the dual-bus configuration, data is accessed on the Image bus by a slave-mode access which does not require an address.

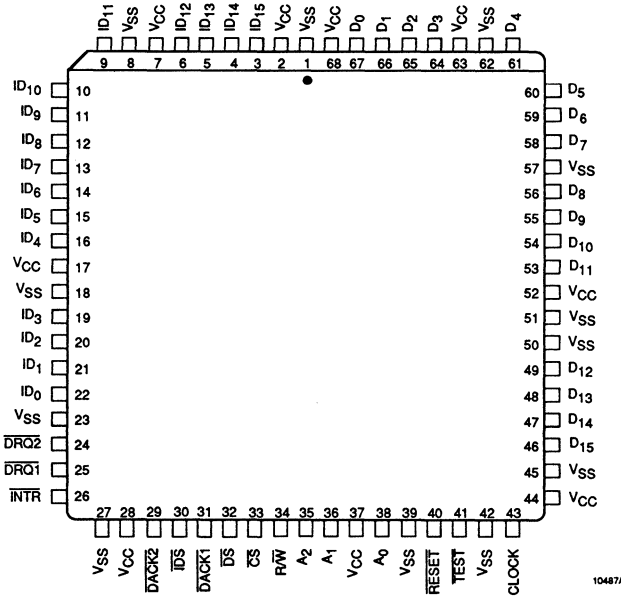
CONNECTION DIAGRAMS
Top View

LCC



CD011630

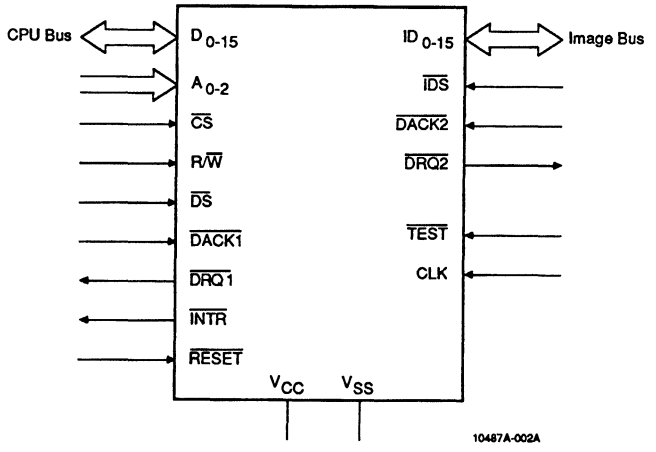
PLCC



CD011640

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

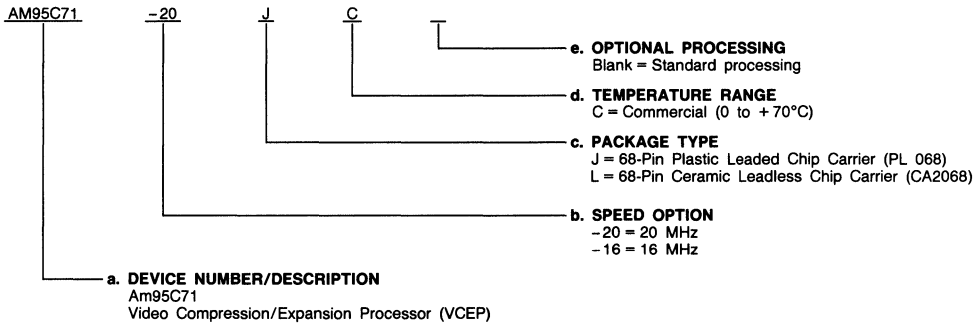


LS003291

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM95C71-20	JC, LC
AM95C71-16	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

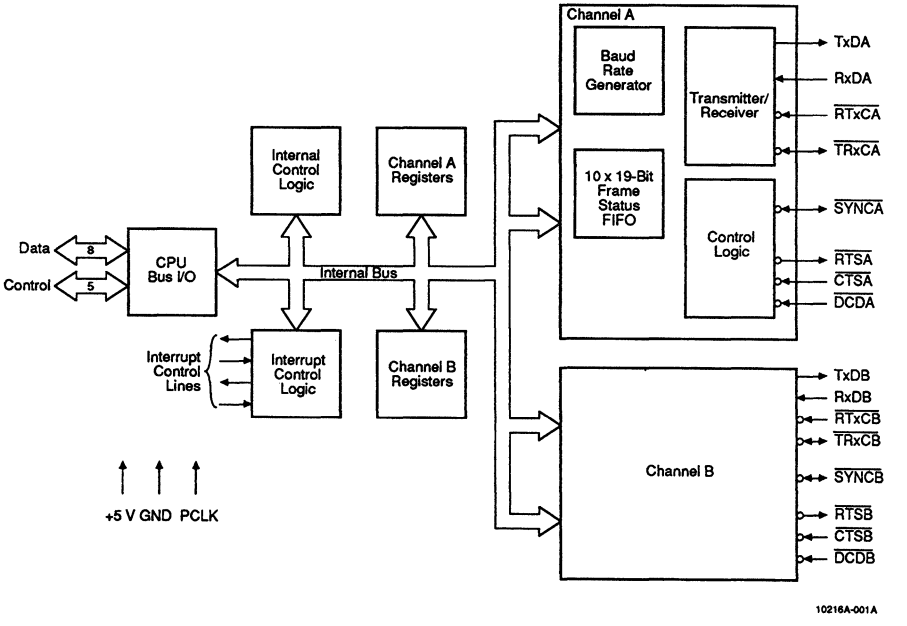
Z85C30

Enhanced Serial Communications Controller

DISTINCTIVE CHARACTERISTICS

- **Two independent full-duplex serial channels**
  Each channel has independent oscillator, baud-rate generator, and DPLL for clock recovery, dramatically reducing external components.
- **Programmable protocols**
  NRZ, NRZI, and FM data encoding/decoding supported under program control.
  - Max. Bit Rate (16 MHz)
    1) Externally clocked: 4 Mbps
    2) Self clocked:
       1 Mbps FM coding
       500 Kbps NRZI coding
- **Programmable Asynchronous Modes**
  - Programmable
    1) Stop bits
    2) Clock factor
    3) Character length (5- to 8-bit)
    4) Odd/even no parity
  - Break detection/generation
  - Error detection
    1) Framing
    2) Overrun
    3) Parity
- **Local Loopback and Auto Echo Modes**
- **Internal or external character synchronization**
- **Completely downward-compatible with the NMOS Z8530**
- **Programmable Synchronous Modes**
  SDLC/HDLC and SDLC Loop Modes supported with frame control, zero insertion and deletion, abort, and residue handling. CRC-16 and CCITT generators and checkers.
- **Compatible with non-multiplexed bus**
  The Z85C30 interfaces easily to most CPUs.
- **Enhanced SCC functions support DMA**
  - 14-bit byte counter
  - 10 x 19-bit SDLC/HDLC Frame Status FIFO
- **Low-power CMOS**

BLOCK DIAGRAM



BD008260

GENERAL DESCRIPTION

The Enhanced Serial Communications Controller (ESCC) is a dual-channel, multi-protocol data communications peripheral designed for use with 8- and 16-bit microprocessors. The ESCC functions as a serial-to-parallel, parallel-to-serial converter/controller. The ESCC can be software-configured to satisfy a wide variety of serial communications applications. The device contains a variety of new, sophisticated internal functions, including on-chip baud rate generators, digital phase-locked loops, and crystal oscillators, which dramatically reduce the need for external logic.

The ESCC handles asynchronous formats, SYNC byte-oriented protocols (such as IBM BISYNC), and SYNC bit-oriented protocols (such as HDLC and IBM SDLC). This versatile device supports virtually any serial data transfer application (cassette, diskette, tape drivers, etc.).

In addition, enhancements which allow the Z85C30 to be used more effectively in high-speed applications include:

- a 10 x 19-bit SDLC/HDLC frame status FIFO array
- a 14-bit SDLC/HDLC frame byte counter
- automatic SDLC/HDLC opening frame flag transmission
- TxD pin forced HIGH in SDLC NRZI mode after closing flag
- automatic SDLC/HDLC Tx underrun/EOM flag reset
- automatic SDLC/HDLC Tx CRC generator reset/preset
- $\overline{RTS}$ synchronization to closing SDLC/HDLC flag
- $\overline{DTR}/\overline{REQ}$ de-activation delay significantly reduced
- external PCLK to $\overline{RxC}$ or $\overline{TxC}$ synchronization requirement eliminated for PCLK divide-by-four operation

Other enhancements to improve the Z85C30 interface capabilities include:

- write data valid setup time to falling edge of $\overline{WR}$ requirement eliminated
- reduced $\overline{INT}$ response time
- reduced access recovery time (t_{RC}) to 3 PCLK best case (3 1/2 PCLK worst case)
- improved $\overline{Wait}$ timing
- write registers WR3, WR4, WR5, and WR10 made readable
- lower priority interrupt masking without $\overline{INTACK}$
- complete SDLC/HDLC CRC character reception

The device can generate and check CRC codes in any SYNC mode, and can be programmed to check data integrity in various modes. The ESCC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls can be used for general-purpose I/O.

The ESCC is designed for non-multiplexed buses and is easily interfaced with most CPUs, such as 8080, Z80®, 6800, 68000, and MULTIBUS.†

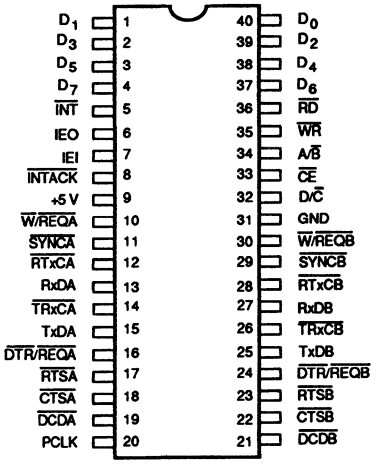
RELATED AMD PRODUCTS

Part No.	Description
Am7960	Coded Data Transceiver
80186	Highly Integrated 16-Bit Microprocessor
80286	High-Performance 16-Bit Microprocessor
Am9517A	DMA Controller

Z80 is a registerd trademark of Zilog, Inc.
†MULTIBUS is a trademark of Intel, Corp.

CONNECTION DIAGRAMS
Top View

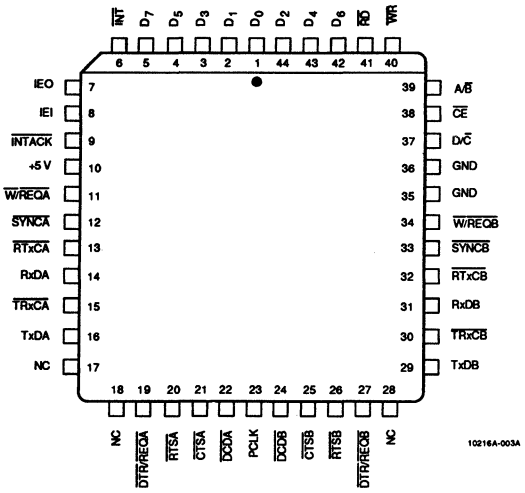
DIPs



10216A-002A

CD011530

PLCC

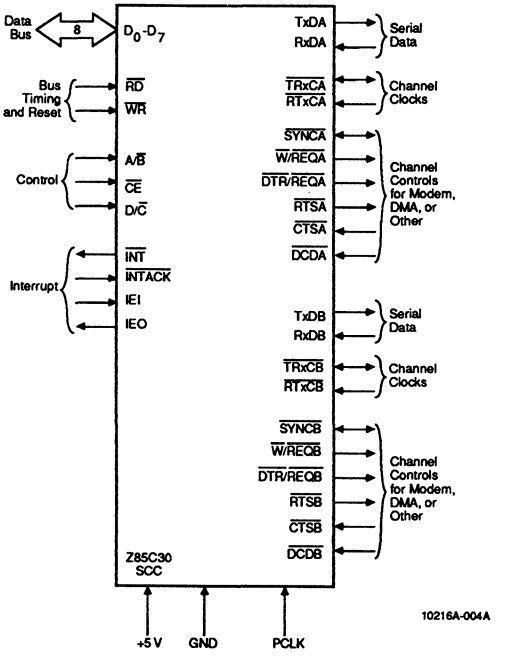


10216A-003A

CD011540

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



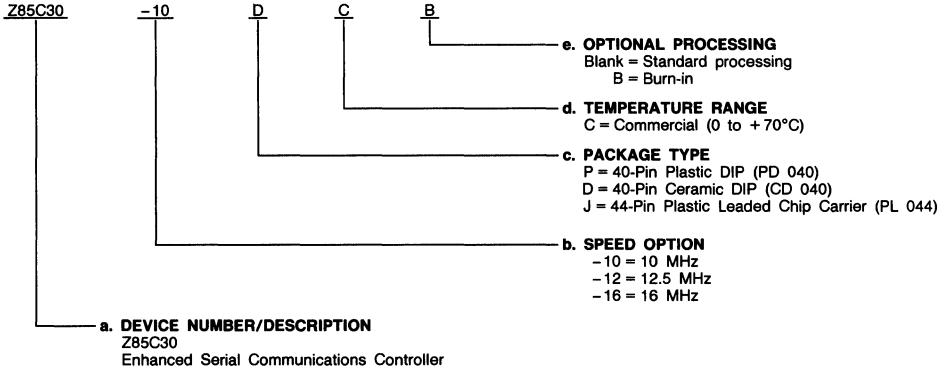
10216A-004A

LS003300

ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
Z85C30-10	PC, DC, DCB, JC
Z85C30-12	
Z85C30-16	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Am9518/AmZ8068

Data Ciphering Processor

DISTINCTIVE CHARACTERISTICS

- **Encrypts and decrypts data**
  Implements National Bureau of Standards standard data encryption algorithm.
- **High-Speed Operation**
  Am9518 and AmZ8068 throughput over 1.3 and 1.7M bytes per second, respectively. Operates at data rates fast enough for disk controllers, high-speed DMA, telecommunication channels.
- **Supports three ciphering options**
  Electronic Code Book for disk applications. Chain Block Cipher for high-speed telecommunications. Cipher Feedback for low-to-medium speed, byte-oriented communications.
- **Three separate key registers on-chip**
  Separate registers for encryption key, decryption key and master key improve system security and throughput by eliminating need to reload keys frequently.
- **Three separate data ports provide flexible interface, improved security**
  The DCP utilizes a master port, slave port and key port. Functions of the three ports can be programmed by the user to provide for simple interface to AmZ8000 and Am2900 systems and to provide total hardware separation of encrypted data, clear data and keys.

GENERAL DESCRIPTION

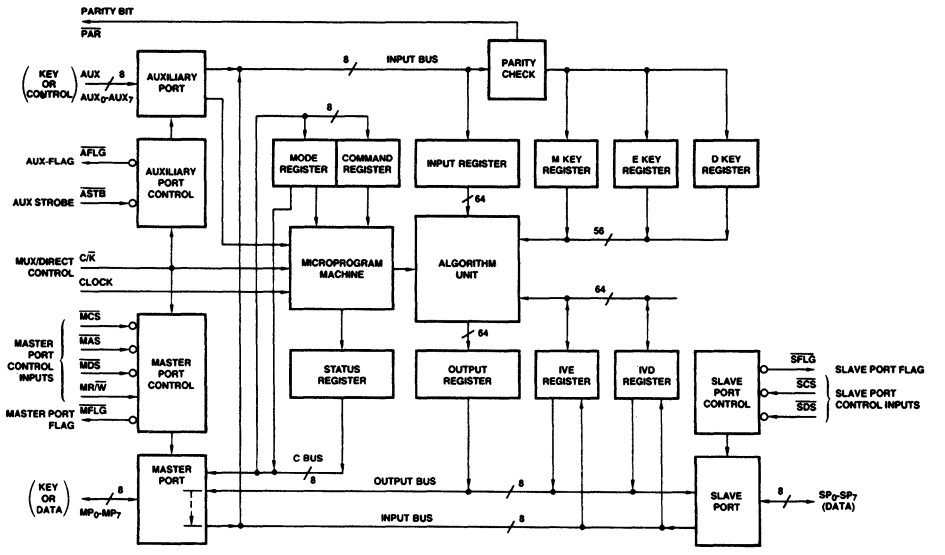
The Am9518/AmZ8068 Data Ciphering Processor is an N-channel silicon gate LSI product containing the circuitry necessary to encrypt and decrypt data using the National Bureau of Standards encryption algorithm. It is designed to be used in a variety of environments, including dedicated controllers, communication concentrators, terminals and peripheral task processors in general processor systems.

The DCP provides a high throughput rate using Cipher Feedback, Electronic Code Book or Cipher Block Chain operating modes. Separate ports for key input, clear data and enciphered data enhance security.

The system communicates with the DCP using commands entered in the master port and through auxiliary control lines. Once set up, data can flow through the DCP at high speeds because input, output and ciphering activities are all performed concurrently. External DMA control can easily be used to enhance throughput in some system configurations.

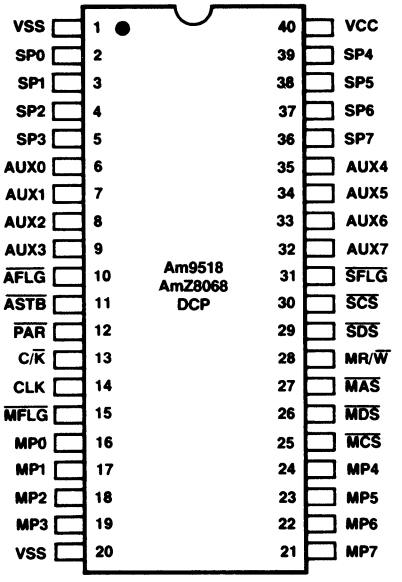
This device is designed to interface directly to the AmZ8000 CPU bus and, with a minimum of external logic, to the 2900, MC68000, 8086, 8085, and 8051 families of processors.

BLOCK DIAGRAM



BD003290

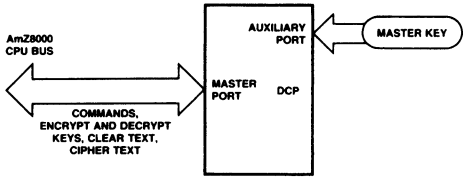
CONNECTION DIAGRAM
Top View



CD005111

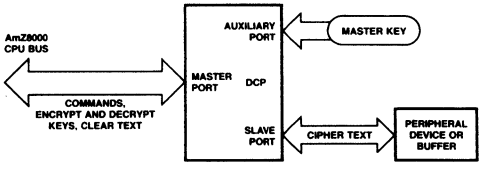
Note: Pin 1 is marked for orientation

DCP DATA FLOW OPTIONS



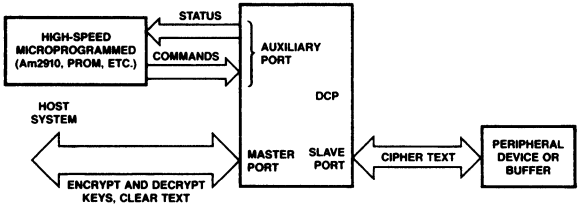
AF002220

Single-Port Configuration, Multiplexed Control



AF002230

Dual-Port Configuration, Multiplexed Control



AF002240

Dual-Port Configuration, Direct Control

Am9520/Am9521/AmZ8065

Burst Error Processor

DISTINCTIVE CHARACTERISTICS

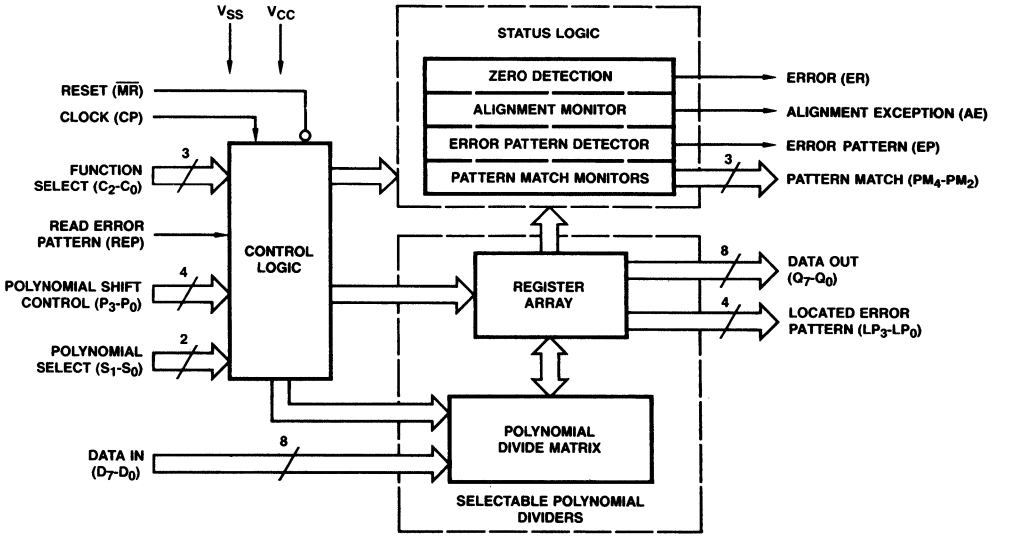
- **Provides for detection and correction of burst errors**
  Detects errors in serial data up to 585K bits long. Allows correction of error bursts of up to 12 bits.
- **High-Speed Operation**
  Effective data rates up to 20 Mbits/second for Am9520/Am9521/AmZ8065 and 30 Mbits/second for -1 versions. Fast enough for high-performance hard and soft disk systems.
- **Selectable Industry-Standard Polynomials**
  35-bit and 32-bit polynomials on Am9521. Am9520/AmZ8065 additionally has popular IBM 56-bit and 48-bit versions.
- **Three correction algorithms provide flexibility**
  !q j Full-period clock-around method for conforming to current practices. Chinese remainder theorem reduces correction time by orders of magnitude. Reciprocal polynomial makes correction possible with 48-bit code.
- **Designed for use in both microprogrammed and microprocessor disk controller systems**
  Device complements both AmZ8000 and Am2900 microprocessor families and can also be used with other microprocessors.

GENERAL DESCRIPTION

The Burst Error Processor (BEP) provides for error detection and correction for high-performance disk systems and other systems in which high-speed serial data transfer takes place. As data density and transfer rates increase in both hard and floppy disks and other storage media, error detection and correction become increasingly important. The BEP is an LSI circuit that facilitates the most common error detection and correction schemes accommodating data streams of up to 585K bits at up to 20M bits/second effective data rate.

The BEP provides a choice of four standard polynomials, including the popular 56-bit and 48-bit versions, to satisfy a broad range of applications. The device divides the data stream by the selected polynomial using the rules of algebra in polynomial fields. The resulting remainder is the check word, which is then appended to the data for writing on the disk as a record. When the record is read back, the BEP computes the syndrome for data validation. If an error is detected, the location and pattern of this burst in the data stream is determined for corrections.

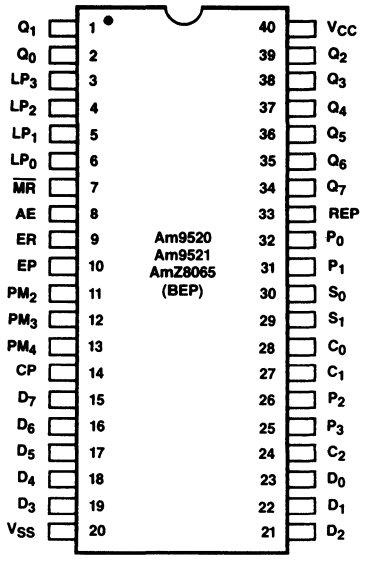
BLOCK DIAGRAM



BD003300

CONNECTION DIAGRAM
Top View

D-40

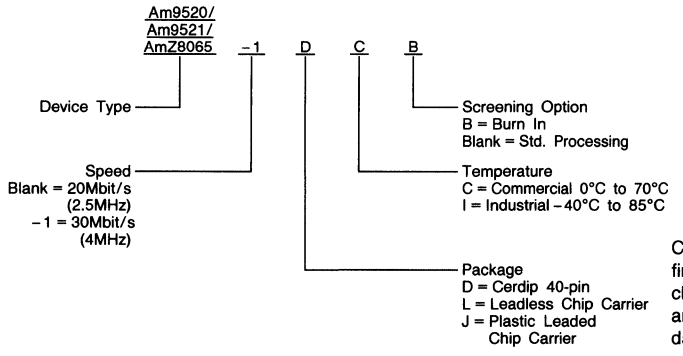


CD005121

Note: Pin 1 is marked for orientation

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Valid Combinations		
	20Mbit/s Data Rate	**30Mbit/s Data Rate**
Am9520/ Am9521/ AmZ8065/	DC, DCB, DI, DIB, LC, LCB, LI, LIB	-1DC, -1DCB, -1DI, -1DIB, -1LC, -1LCB, -1LI, -1LIB

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, check for newly released valid combinations and/or obtain additional data on AMD's standard military grade product.

TYPICAL APPLICATION DIAGRAM

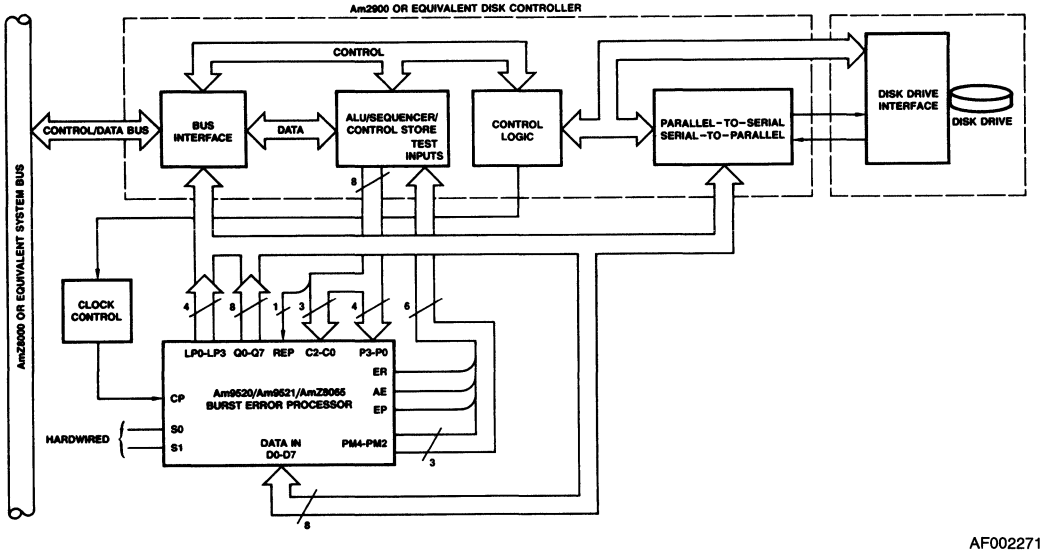


Figure 6. Am9520/Am9521/AmZ8065 Burst Error Processor

APPLICATIONS

The BEP is designed for use in both microprogrammed and microprocessor disk controller systems. Figure 6 shows the BEP interfacing to an Am2900 bipolar bit-slice microprogrammed disk controller. The BEP can be interfaced to microprocessor-driven disk controller systems as well.

The controller in these designs would implement the control and clocking signals for the BEP necessary to execute the write, read and correction functions for a given polynomial selection. The operational flow for the methods available is shown in Figure 7.

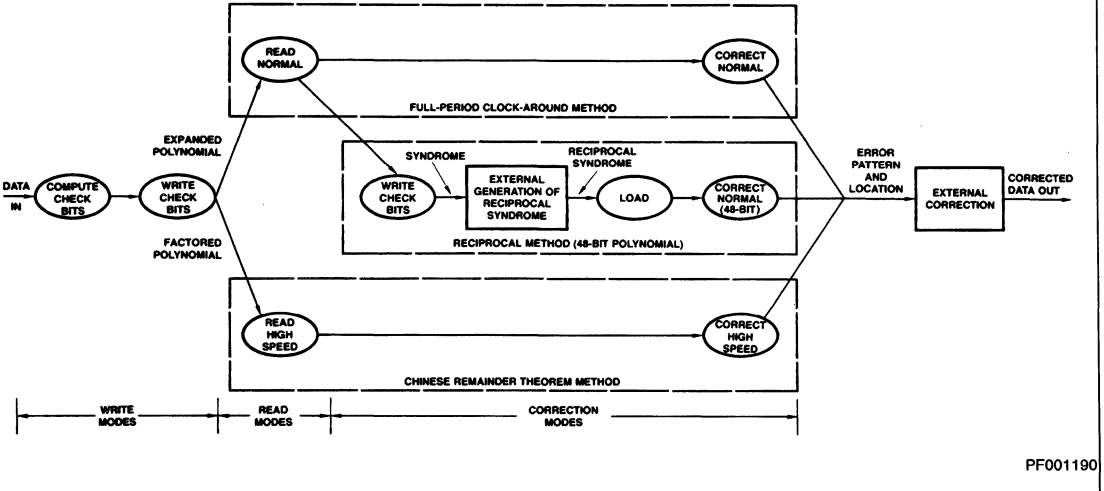


Figure 7. BEP Operational Flow Diagram

Am9568

Data Ciphering Processor
(DCP)

DISTINCTIVE CHARACTERISTICS

- **Encrypts and decrypts data**
  Implements National Bureau of Standards Data Encryption Standard (DES) algorithm
- **Throughput over 1.5M bytes per second**
  Operates at data rates fast enough for disk controllers, high-speed DMA, telecommunication channels
- **Supports three ciphering options**
  Electronic Code Book for disk applications, Cipher Block Chain for high-speed telecommunications, and Cipher Feedback for low-to-medium speed, byte-oriented communications
- **Three separate key registers on one chip**
  Separate registers for encryption key, decryption key and master key improve system security and throughput by eliminating need to reload keys frequently.
- **Three separate data ports provide flexible interface, improved security**
  The DCP utilizes a Master Port, Slave Port and Key Port. Functions of the three ports can be programmed by the user to provide for simple interface to iAPX86 and Am2900 systems and to provide total hardware separation of encrypted data, clear data and keys.

GENERAL DESCRIPTION

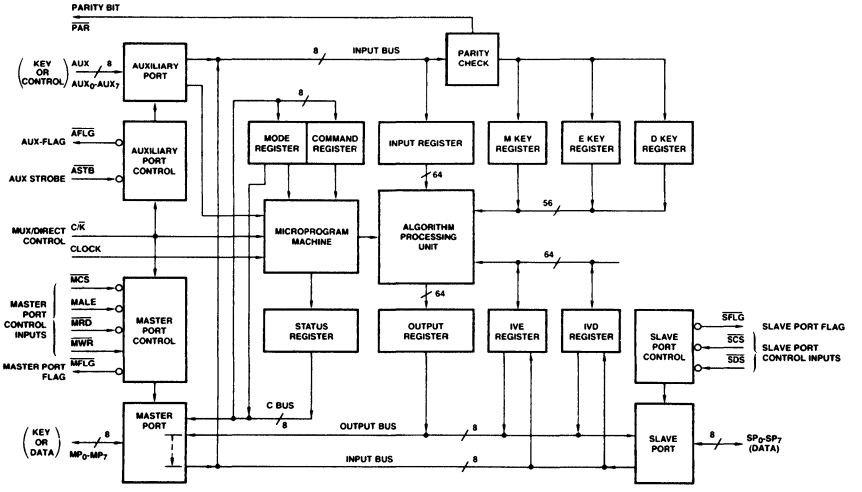
The Am9568 Data Ciphering Processor is an N-channel silicon gate LSI product containing the circuitry necessary to encrypt and decrypt data using the National Bureau of Standards Encryption Algorithm. It is designed to be used in a variety of environments, including dedicated controllers, communication concentrators, terminals and peripheral task processors in general processor systems.

The DCP provides a high throughput rate using Cipher Feedback, Electronic Code Book or Cipher Block Chain operating modes. Separate ports for key input, clear data and enciphered data enhance security.

The system communicates with the DCP using commands entered in the Master Port and through auxiliary control lines. Once set up, data can flow through the DCP at high speeds because input, output and ciphering activities are all performed concurrently. External DMA control can easily be used to enhance throughput in some system configurations.

This device is designed to interface directly to the iAPX86, 88 CPU bus and, with a minimum of external logic, to the 2900 and 8051 families of processors.

BLOCK DIAGRAM

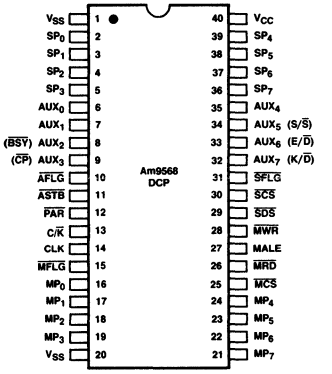


BD003370

RELATED PRODUCTS

Part No.	Description
Am9518/Z8068	Data Ciphering Processor

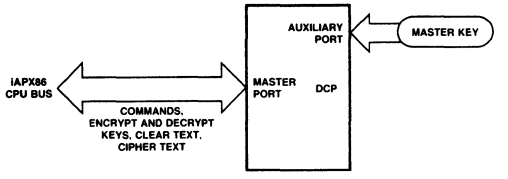
CONNECTION DIAGRAM
Top View



CD005200

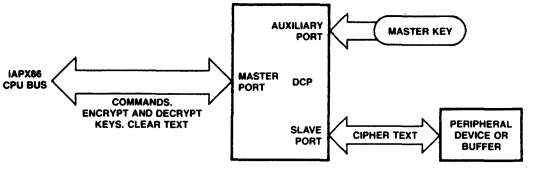
Note: Pin 1 is marked for orientation

DCP DATA FLOW OPTIONS



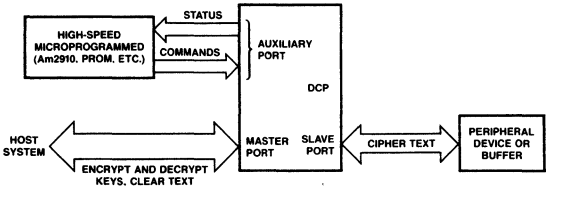
AF002480

Single-Port Configuration, Multiplexed Control



AF002490

Dual-Port Configuration, Multiplexed Control

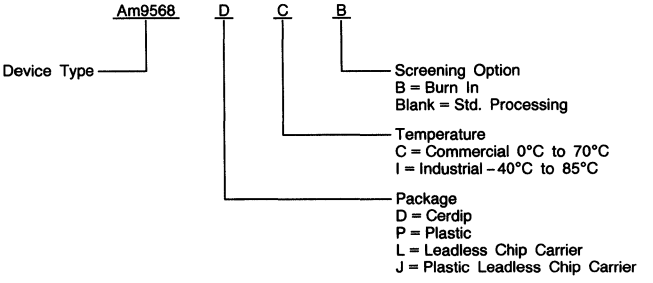


AF002500

Dual-Port Configuration, Direct Control

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).



Valid Combinations	
Am9568	DC, DCB, PC, DI, PCB, PI, PIB, DIB, LC, LCB, LI, LIB

Valid Combinations

Consult the local AMD sales office to confirm availability of specific valid combinations, check for newly released valid combinations and/or obtain additional data on AMD's standard military grade product.

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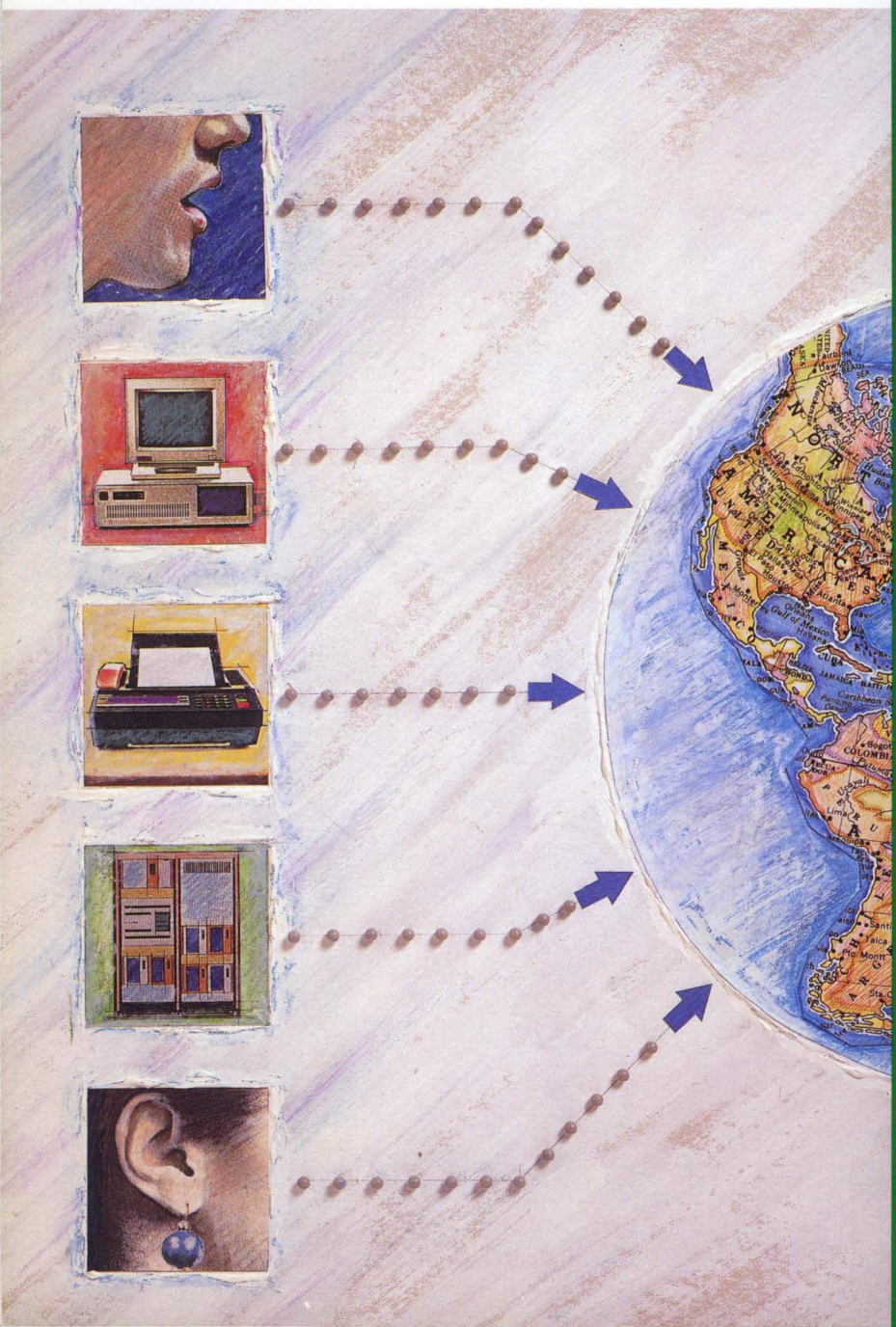

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