Flash Memory Products

1990 Data Book/Handbook

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This is your design Handbook for AMD's family of Flash memories. Included are data sheets and application notes that provide a detailed explanation of how to design this family into your new memory systems. When you use our devices you obtain the quality and reliability that you have come to expect from our EPROM and E^2PROM product lines.

AMD is the only Flash memory supplier that is also a major manufacturer of both EPROM and E^2PROM technologies. This experience base is transferred directly to our Flash memory family. This synergy is important because Flash memories were actually born out of a marriage of these two technologies. AMD also offers the highest performance and density of Flash memories available in the industry. By using less silicon than our competitors we are also positioned to be the lowest cost producer in the industry.

Flash memories are not just a new approach to non-volatile storage media. They actually offer you a more competitive way to do business. Flash memories increase your ability to bring products to market sooner. Also, you can cost effectively update systems already in the field with the latest firmware revisions that you are currently shipping. They even allow you to respond immediately to changing market demands by configuring generic hardware systems just prior to shipment. In addition, Flash memories can be used as removable media for the new exploding markets of miniaturized portable equipment and computers.

We are very excited about this Flash memory family. As you read through this handbook I think you will share this feeling.

Rich Forte

Vice President
High Performance Memory Division

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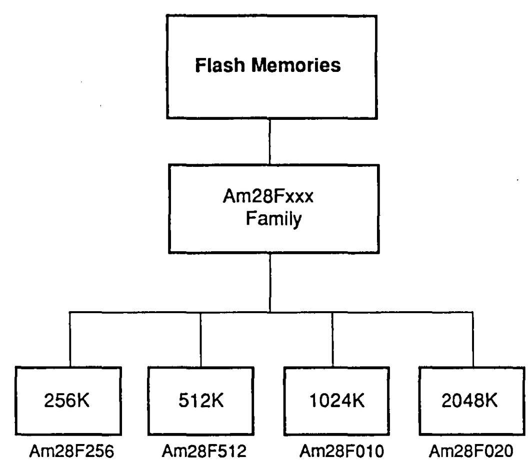
Product Selector Guide



Am28Fxxx Family

Part Number	Organization	Access Time (ns)	Temp Range[1]	Package Type[2]	Pin Count (DIP/LCC, PLCC)	Supply Voltage
Am28F256-75	32K x 8	70	C, I	D, L, P, J	32/32	5 V ± 5%
Am28F256-95	32K x 8	90	C, I	D, L, P, J	32/32	5 V ± 5%
Am28F256-90	32K x 8	90	C, I, E	D, L, P, J	32/32	5 V ± 10%
Am28F256-120	32K x 8	120	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F256-150	32K x 8	150	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F256-200	32K x 8	200	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F512-75	64K x 8	70	C, I	D, L, P, J	32/32	5 V ± 5%
Am28F512-95	64K x 8	90	C, I	D, L, P, J	32/32	5 V ± 5%
Am28F512-90	64K x 8	90	C, I, E	D, L, P, J	32/32	5 V ± 10%
Am28F512-120	64K x 8	120	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F512-150	64K x 8	150	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F512-200	64K x 8	200	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F010-95	128K x 8	90	C, I	D, L, P, J	32/32	5 V ± 5%
Am28F010-90	128K x 8	90	C, I, E	D, L, P, J	32/32	5 V ± 10%
Am28F010-120	128K x 8	120	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F010-150	128K x 8	150	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F010-200	128K x 8	200	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F020-95	256K x 8	90	C, I	D, L, P, J	32/32	5 V ± 5%
Am28F020-90	256K x 8	90	C, I, E	D, L, P, J	32/32	5 V ± 10%
Am28F020-120	256K x 8	120	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F020-150	256K x 8	150	C, I, E, M	D, L, P, J	32/32	5 V ± 10%
Am28F020-200	256K x 8	200	C, I, E, M	D, L, P, J	32/32	5 V ± 10%

Notes:

[1] Temp Range
- C = Commercial (0° to +70°C)
- I = Industrial (-40° to +85°)
- E = Extended Commercial (-55° to +125°C)
- M = Military (-55° to +125°C – most products available in both APL and DESC versions)

[2] Package Type
- C = Ceramic DIP
- L = Rectangular Ceramic Leadless Chip Carrier
- P = Plastic DIP
- J = Rectangular Plastic Leaded Chip Carrier

CHAPTER 1
An Introduction to Flash Memory

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An Introduction to Flash Memory

WHAT IS FLASH MEMORY?

Flash memories are the most cost effective non-volatile alternative for high density memory applications that require in-system reprogramming.

Flash memory is born out of a marriage of EPROM and E^2PROM technology. Accordingly, Flash memories incorporate the best characteristics of both devices. Flash memories are erased electrically just like E^2PROMs. However, Flash memories erase the entire chip at once. This is similar to UV EPROM. Unlike E^2PROM, Flash memories do not allow data to be changed on a byte by byte basis. In addition, the Am28Fxxx family of Flash memories uses a separate 12.0 V ±5% programming power supply for both program and erase operations. Absolute write protection is provided when the 12.0 V supply is disabled.

The Am28F010 one Megabit Flash memory can be completely reprogrammed in less than five seconds. Reprogramming includes both the erase and programming operations. This is even faster than a standard E^2PROM. In addition, Flash devices eliminate the need for expensive windowed packages, unplugging devices from sockets during code changes, and the 15–20 minutes required for EPROM erasure using ultraviolet light. Since Flash memories are available in plastic packages they are ideal for todays automatic manufacturing lines.

Table One compares the basic features of U.V. EPROM, Flash memories, and E^2PROMs.

Table 1

Parameter	UV EPROM	Flash	E^2PROM
Erase	UV Chip Erase	Electrical Chip Erase	Electricl Byte Erase
Program	Per Byte	Per Byte	Per Byte
Program Voltage	12.5 V	12.0 V	5.0 V
Programming Method	External Programmer	In-system	In-system
Reprogramming Time (1 Megabit)	15 – 20 Minutes	5 Seconds	10 Seconds

WHERE WILL FLASH MEMORIES BE USED?

Flash memories can be used in a wide variety of applications that today are implemented with EPROM, E^2PROM, SRAM & Battery, or DRAM & Disk memory systems.

WHY IS FLASH MEMORY COST EFFECTIVE?

In order to answer this question, the total cost of reprogramming a non-volatile memory system must be considered. There are two components of the cost structure associated with in-system reprogramming. They are the device cost and the cost of updating memory contents in-system.

The following sections illustrate the advantage of AMD's Flash memory family versus today's alternative non-volatile memories.

12.0 V Flash vs. UV EPROM

Although the current device cost of Flash memories is greater than UV EPROM, soon they will be priced at only a multiple of 1.2 times UV EPROM. The cost savings of performing in-system reprogramming with Flash memories greatly outweighs any device level cost advantage of UV EPROM. The cost savings of a Flash memory system is greatly magnified if in-system updates are repeatedly performed. The key difference as shown in table 2 is in the cost of updating memory contents.

When the code of a UV EPROM is updated the device must be removed from a socket and either erased for 15–20 minutes, reprogrammed, and then replaced, or just replaced with an entirely new device containing the updated code. This method of updating memory contents is extremely labor intensive wherever it is performed, at the prototype stage, on the manufacturing line, or especially if it is required when a system is in the field. The reoccuring cost of a service call today exceeds $150. Logistics of implementing manual code changes are complicated if they are to be transparent to the system user. The down time associated with replacing EPROMs is reflected in the end user's loss of productivity.

In addition, when system disassembly occurs in the field to replace EPROM based code storage it impacts the overall system in two ways. First, system design may compromise the most efficient use of board layout space. The placement of the EPROM device and its socket is dictated by ease of access and replacement when the system is disassembled. Second, whenever systems are disassembled the integrity of its reliability as shipped from the factory may be jeopardized. Frequently, system disassembly causes damage to boards and components. In addition, system recalibration may be required after reassembly.

Flash memories offer a superior solution. Reprogramming memory contents can be conveniently accomplished electrically in the resident system. Typically it takes only one second to erase an entire Flash memory device and only seconds to program the entire array. Memory contents may be updated in a number of ways. Reprogramming can be accomplished remotely via the communication abilities of the target system such as modem, Integrated Services Digital Networks (ISDN), or if it is part of a networked system. Updates may also be performed using existing disk drive capability. The updated code may also be distributed via floppy disks and downloaded with just a few simple strokes on the keypad.

12.0 V Flash vs. E^2PROM, 5.0 V – only Flash, and SRAM & Battery

The cost of updating memory contents for each of these alternatives is essentially equivalent. Again, existing communication links can be used. A nominal cost is assigned for this procedure as listed in table 2. In this comparison the primary advantage of AMD's Flash solution is in the device cost. AMD's Flash memories will continue to parallel the density of UV EPROMs while costing only slightly more than them. This is due to the use of our EPROM-like single transistor memory cell. Because these other devices use multiple transistor memory cells, they will be hard pressed to match the future increases in device density and the inherent cost-per-bit advantage of 12.0 V Flash memories.

Since at least 60% of a memory chip is comprised of the actual memory array, any alternative to the single transistor memory cell will suffer from limits of increasing chip density, incur a 2-4x increase in silicon real estate, and have a higher manufacturing cost structure. Today's 5.0 V-only Flash memories are really only watered down versions of standard E^2PROMs. They use complex, multiple transistor memory cells similar to E^2PROMs. This approach to Flash memories still uses charge pumps to raise internal voltages up to 18 volts and greater. This severely stresses the memory's tunnel oxide. In part, this explains the lower endurance capability of these types of devices. 5.0 V only Flash devices have at least an order of magnitude lower cycling endurance than 12.0 V Flash memory.

In addition, non-volatile 12.0 V Flash memories are not burdened by the reliability concern of battery backed SRAMs. Why try and predict battery failure? Flash memories exhibit the time tested data retention characteristics of EPROM memory devices. There is no need for battery holders or system design compromises that permit access to the battery for replacement. Batteries are also susceptible to environmental effects of temperature and mechanical shock and vibration.

12.0 V Flash vs. DRAM & Disk Drive

The new explosive growth markets of miniature portable equipment and computers along with the associated need for transportable non-volatile memory will be another driving factor for Flash memories. This will establish Flash memories as the new memory of choice. Flash offers immediate access (instant-on) to application programs without the download time associated with transfering application code from hard disk to system memory; code is executable directly from the memory. Data files may be written and altered using the Flash memory as a rewritable storage medium. A much smaller form fit and weight factor is achieved with solid state memory versus a mechanical disk drive. Power consumption is substantially reduced and reliability increased due to the greater lifetime achieved in environmentally extreme conditions.

Table Two summarizes these issues.

Table 2

Device	Device Cost (256 K Density)	Update Cost	Total Cost
EPROM	$2.00	$150.00	$152.00
E^2PROM	$20.00	$8.00	$28.00
SRAM & Battery	$18.00	$8.00	$26.00
5.0 V Flash	$10.00 – 20.00	$8.00	$18.00 – 28.00
Flash & V_{PP} Circuitry	$5.00 $3.00	$8.00	$16.00

HOW DO FLASH MEMORIES LOWER MY TOTAL SYSTEM COST?

In-System Updates

Flash memories provide immediate dividends as soon as they are reprogrammed. Code prototype time is significantly reduced because Flash memories can be updated with new code in a manner of seconds. Updates can occur on the prototype board without any disassembly. This eliminates the time required to unplug, UV erase, reprogram, and replace EPROMs.

Manufacturing Efficiency

Manufacturing processes are simplified by using Flash memories. Board level diagnostics, final system test, and customer specific configuration code can all be downloaded into the Flash memory electrically on the assembly line. Devices may be soldered directly to the system board. This eliminates the need to disassemble the system and replace socketed devices.

Time To Market

Today being first to market often separates the winners from the also rans. Since Flash memories are reprogrammable in-system, final system code is not absolutely a necessary requirement prior to shipment. As refinements and updates are made, each previously

shipped system can be updated conveniently and cost effectively. Thus your entire product line can always be as up-to-date as your newest systems rolling out the factory door.

Efficient Inventory Control

Accurate product mix forecasting is an elusive capability. Changing market conditions that deviate from even the best forecasts have real world impact on a business unit's ability to be responsive to customer demands and meet quarterly goals. Flash memories offer an innovative solution to this issue. Generic hardware systems can be planned and built without exact knowledge of final product mix. Various models of one hardware platform may be configured with customer specific code prior to shipment.

This allows you to create a more flexible and cost effective finished goods inventory. You can now respond immediately to changing market demand as soon as marketing information is available.

Field Service Savings

The prohibitive costs associated with a field service call are now a thing of the past. When updates to system code or system reconfiguration is necessary, these costly service calls may be replaced with remote updates or by distributing floppy disks with new data. In this way, systems can also be reprogrammed when usage is at a minimum. The procedures required to keep all systems up to date now become transparent to the actual end user. In addition, system reliability is not compromised when remote updates are performed. System disassembly is not required. This also eliminates handling, ESD, and component damage issues.

CHAPTER 2
Advantages of AMD's 12.0 V Flash Memory Family

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Advantages of AMD's 12.0 V Flash Memory Family

AMD'S FLASH MEMORIES CREATE A DEFACTO INDUSTRY STANDARD

AMD is the first company to address the issue of device compatibility. In the world of Flash memories today, no two device offerings can be used as 100% compatible alternate sources of supply. While 32-pin pinouts are assigned for Flash E²PROMs, programming software standards do not exist. This is one of the major issues that must be addressed in order to fuel the widespread use of Flash memories.

AMD is leading the way to promote a defacto industry standard pinout and software for Flash memories. AMD's approach allows our device to be used as a 100% alternate source with the Intel Flash memories. Our devices are 100% compatible with the Intel type of software commands while providing us the flexibility to enhance our device features. These enhancements are a natural extension of our years of experience in the E²PROM business.

The market acceptance of Flash memories is now accelerated by the availability of 100% software and pinout compatible devices from the two largest U.S. suppliers of non-volatile memories.

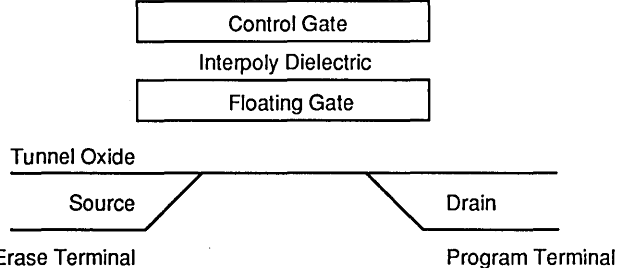
FLASH MEMORY TECHNOLOGY IS EVOLUTIONARY

AMD is the only Flash memory supplier that is also a major manufacturer of both EPROM and E²PROM technologies. We have transferred this experience base directly to our Flash memory technology and manufacturing process. This synergy is important because Flash memories were actually born out of a marriage of these two technologies.

We build our Flash memories on our state of the art 1.0 µM CMOS technology on the same high volume manufacturing line used for our current EPROM and E²PROM devices. This provides the basis for our steep learning curve that will bring the cost of our 12.0 V Flash memories to within just a slight premium over UV EPROM devices.

Our many years of experience in E²PROM design and our understanding of the issues relating to in-system write operations are incorporated into our Flash memory family. In addition, the many years of manufacturing experience and constant refinements to our thin film tunnel oxide provide immediate benefits to our Flash family.

Figure 1. The AMD Flash Memory Cell



The AMD Single Transistor Memory Cell

AMD's Flash Memory Technology

This section illustrates the fundamentals of AMD's Flash memory technology. AMD's Flash memory technology is very similar to that of our UV EPROM. The main difference is associated with the erase mechanism of Fowler-Nordheim tuneling.

Program Operations

AMD's Flash memories transfer and store charge on a floating gate in a manner similar to EPROM. This provides data retention that is equivalent to that of EPROM devices. The device is programed by raising the control gate and drain terminal to a high voltage. The source terminal is grounded.

The voltage potential across the channel attracts channel electrons from the source area toward the drain. At the drain region, some of these channel electrons become "hot." The high voltage on the control gate attracts the "hot" electrons from drain area across the thin oxide where they are trapped on the floating gate.

The Programmed State

The electrons stored on the floating gate creates an electric field which turns off the memory transistor and represents a logic zero.

Erase Operations

The Flash memory cell removes charge from the floating gate like an E²PROM. The Fowler-Nordheim tuneling mechanism is used for erase operations. High voltage is applied to the source terminal while the control gate is grounded. This voltage potential causes the stored charge on the floating gate to tunnel through the thin oxide and into the source terminal. During the erase operation high voltage is applied to the source terminals of every memory cell at once. This produces the bulk erase characteristics of Flash memory.

The Erased State

Without the presence of electrons on the floating gate, the transistor is conductive and represents a logic one.

PROGRAMMING ENDURANCE

AMD's Flash memory technology incorporates the traditional EPROM programming mechanism of hot electron injection and the standard E²PROM erase mechanism of Fowler-Nordheim tunneling. AMD achieves the highest level of endurance capability by performing each of the program and erase operations on separate terminals of the memory cell. This is because programming and erase methods employ different charge transfer mechanisms. This way the memory cell can be optimized for each separate mechanism. In addition, the V_{PP} voltage used for program and erase operations is lower than the voltages used by traditional E²PROMs. This significantly lowers the stress on the tunnel oxide during erase operations and hence extends the cycling capability of the tunnel oxide by orders of magnitude.

MANUFACTURING EFFICIENCY

AMD also leads the industry as the most cost efficient manufacturer of non-volatile memories. Our EPROM experience base again offers immediate benefits to our Flash family. We continue to the lead the competition with the smallest Flash memory chips. Thus, we are positioned to be the lowest cost Flash memory supplier in the industry. This not only ensures our viability as a long term supplier but also ensures you of a ready supply of product.

ZERO WAIT STATE SYSTEMS

AMD's Flash memories let you take full advantage of your high performance microprocessor systems. Our devices lead the industry with the fastest access times available. AMD's Am28F256 and Am28F512 devices are available at 70ns and our Am28F010 one Megabit device is available at 90ns. These devices operate at typically twice the performance of our competitors. Again, this advantage is a direct result of AMD's high performance EPROM leadership.

INADVERTANT WRITE PROTECTION

The AMD Flash memory incorporates an on-chip state machine to determine the operating mode of the device. The state machine is accessed only via the on chip command register. In turn, the command register is only enabled when the 12.0 V V_{PP} voltage is active. Without the V_{PP} voltage, memory contents can not be altered.

The command register is manipulated by a combination of three control pins. The only condition valid for a write operation is when $\overline{OE}$ is high and both $\overline{CE}$ and $\overline{WE}$ are low. Any other state is considered a non-write state. Data can not be transferred from the command register to the state machine if a non-write state condition exists.

The state machine requires a sequence of two-cycle bus commands to change the "state" of the Flash memory device. Should an improper sequence of commands be issued to the device it will interpret these as "illegal" commands and safely reset to the read only mode and terminate any current operation. The two-cycle bus commands tend to eliminate the potential for inadvertent writes should system glitches occur. It is unlikely that the proper sequence and timing of these glitches would resemble actual valid commands. This is an advantage over other approaches to Flash memories that simply use control pins to initiate write operations.

In addition, during system power transitions the Flash memory device automatically resets to the read mode. The command register may also be effectively locked out of transfering any commands to the state machine by tying the $\overline{WE}$ pin to the device V_{CC} pin. Thus, $\overline{WE}$ will always be in a non-write configuration until driven low by the system write control line.

Please refer to application note AN–101 for details regarding this issue.

EFFICIENT PROGRAMMING ALGORITHMS ALSO GUARANTEE DATA RETENTION

AMD's Flash memory programming algorithms use an interactive approach to adequately program and erase the device with a minimal number of pulses.

We guarantee data retention by using a similar margin verify concept employed by EPROM programming algorithms. During the verify mode an internally generated margin verify voltage is applied to each addressed memory location. The verify voltage is generated internally on chip from the static 12.0 V V_{PP} supply. In this way, data retention is guaranteed to equal that of EPROM memories.

GENERATING V_{PP} PROGRAMMING VOLTAGES

In many of today's systems a regulated 12.0 V supply is available. If this is not the case, there are many alternatives for generating this voltage. They vary from DC/DC or analog convertors that can pump up 5.0 V from the system V_{CC} to the regulated 12.0 V V_{PP} supply. In addition, there are many DC/DC convertors that take higher incoming voltages and step them down to the regulated V_{PP} output voltage.

The cost of implementing the voltage generation typically costs less than a fraction of the Flash memory itself and best of all it can be amortized over the entire Flash memory array. Many of these solutions offer enough programming current to program and erase four (4) devices in parallel. This would be sufficient for many of today's 32-bit word sytems.

Please refer to application note AN–102 for details regarding this issue.

CHAPTER 3 AN-101
Considerations for In-System Program

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Considerations for In-System Programming AN-101

BASIC PRINCIPLES

AMD Flash memories use 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0 V ±0.6 V power supply.

Read Only Memory

Without high V_{PP} voltage, the Flash memory functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. Two-cycle commands are required for erase and reprogramming operations. In addition, the traditional read, standby, output disable, and Auto select modes are available via the register.

The AMD Flash memory command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations.

For system design simplification, the AMD's Flash memory is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. All setup and hold times are with respect to the $\overline{WE}$ signal. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text.

Overview of Erase/Program Operations

Erase Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note:
The Flash memory array must be completely programmed prior to erasure. Refer to the Flasherase™ Algorithm.

1. **Erase Set-up:** Write the Erase/Erase Set-up command to the command register.
2. **Erase:** Write the Erase/Erase Set-up command to the command register again. The second command initiates the erase operation. Time-out the erase pulse width.
3. **Erase-verify:** Write the Erase-verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFH data (Byte erased). After successful data verification the Erase-verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Programming Sequence

A three-step command sequence (a two-cycle Program command and one-cycle verify command) is required to program a byte of the Flash array. Refer to the Flashrite™ Algorithm.

1. **Program Set-up:** Write the Program/Program Set-up command to the command register.
2. **Program:** Write the Program/Program Set-up command to the command register with the appropriate Address and Data. Time-out the program pulse width.
3. **Program-verify:** Write the Program-verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times per byte.

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CONSIDERATIONS FOR IN-SYSTEM PROGRAMMING APPLICATIONS

V_{PP} Generation and Control

Constant V_{PP} voltage of 12.0 V ±0.6 V is required for erase and programming operations. Parallel device reprogramming (either 16-bit or 32-bit data words) requires 30 mA of current for each device in the Flash memory array.

V_{PP} voltage can be generated in a number of ways:

1. Use analog circuitry to pump 5 V to V_{PP} Voltage
2. Use DC/DC, monolithic convertor to pump 5 V to V_{PP} Voltage.
3. Hardwire V_{PP} Voltage to the Flash Device
4. Umbilical Cord Programming

It is important to maintain the specified V_{PP} voltages when reprogramming the Flash memory device. All internal device voltages are generated from the V_{PP} reference. Inappropriate V_{PP} voltage may impair device performance. Internal voltages do not exceed that of external V_{PP}.

Unlike other approaches to Flash memories, AMD's devices actually verify margin for each byte during erase and programming operations. This is accomplished during the Erase-verify and Program-verify operations respectively. During these operations, the appropriate margin-verify voltages are internally tapped off of the V_{PP} voltage via the command register and internal V_{PP} circuitry. This allows for Erase/Erase-verify and Program/Program-verify operations to be performed with static V_{CC} (5 V) and V_{PP} (12 V) voltages.

V_{PP} Supply

1. Use analog circuitry to Pump 5 V to V_{PP} Voltage.

See Application Note AN-102 on V_{PP} Generation and Control for circuit schematics and more detailed discussions.

2. Use DC/DC Monolithic Convertor to Pump 5.0 V to V_{PP}.

A monolithic DC/DC convertor from Valor Electronics, the PM9006, is appropriate for the digital world to supply the 12.0 V ±0.6 V V_{PP} voltage. The V_{PP} voltage is generated on a chip using the standard system V_{CC} (5.0 V) voltage. Standard TTL commands are used to disable the 12.0 V output supply when programming or erasing operations are not intended. The enable ($\overline{E}$) function provides absolute write protection to guarantee against inadvertent program or erasure. Flash memory contents cannot be altered without the active 12.0 V V_{PP} supply. The enable pin also saves system power when the DC/DC convertor is not required. The PM9006 has a minimum efficiency of 50% at full load. The PM9006 comes in a 24-pin package.

The Valor PM9006 provides a controlled 12.0 V output that is regulated within the ±5% (±0.6 V) V_{PP} specification. The standard system V_{CC} (5.0 V) supply is converted to the V_{PP} (12.0 V) supply by the DC/DC convertor. The voltage transitions are smooth and protect against destructive positive or negative overshoot.

The PM9006 can supply 165 mA of current at the regulated 12.0 V ±0.6 V output. The 5.0 V ±0.5 V DC input supply of the DC/DC convertor uses a maximum of 840 mA of input current. The Am28F010 specifies a maximum V_{PP} current of 30 mA for either the erase or program operations. Actual current required for these operations is substantially lower than this. Given the maximum V_{PP} current of 30 mA for each device, four (4) Am28F010 may be programmed and erased in parallel with one PM9006 device. The PM9006 V_{PP} supply current = 165 mA - 4 x 30 mA of V_{PP} current required for the Flash memory array = 45 mA of additional current available from the DC/DC convertor.

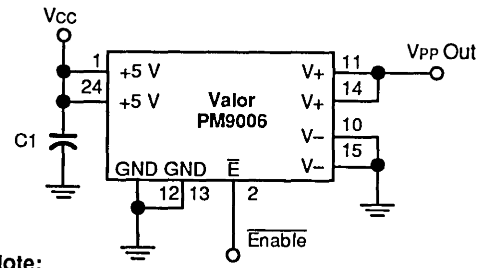
Parallel programming and erasure allows for the most efficient method to reprogram x16 or x32 bit data words. Refer to application note AN-101 for parallel program and erase flow charts.

Board Level Resets

System designs should not allow the Flash device to perform any programming or erase operations when the CPU does not have control of the Flash device. Some designs incorporate board level reset circuitry that suspends operation of the local CPU if the V_{CC} level falls below a predetermined value (such as 4.6 V). If this is the case, the reset circuitry should also disable the V_{PP} power supply whenever the CPU is held in reset.

If the local CPU is forced into reset mode while it is programming or erasing the Flash device, the system reset circuit should also terminate that operation. To accomplish this, the PM9006's enable pin should be driven high whenever the reset circuitry is active. Drive the chip enable pin of the PM9006 with the logical OR of the reset circuitry's output signal and the chip enable control line to the PM9006. This will disable the V_{PP} supply and hence termiante any programming or erase operation. The Flash device automatically resets to the read mode when V_{PP} is disabled.

Please reference the PM9006 data sheet for complete details of device operation. One method of implementing the PM9006 DC/DC convertor is illustrated on page four.



Note:

Pins 3 through 9 and 16 through 23 are not internally connected to the device and do not need to be driven.

Generate and Control 12.0 V

3. Hardwire V_{PP} Voltage to the Flash Device.

Typically this approach is used in the most cost sensitive applications. Regulated 12.0 V supplies are commonly available in many systems.

When V_{CC} = 0 V, the V_{PP} voltage is internally disabled from the device. Memory contents cannot be altered. The Flash device automatically resets to the read mode when V_{CC} rises above 2 V. This occurs even when V_{PP} = 12 V.

Power Supply sequencing is not required.

The device will only respond to the correct sequence of commands in order to change the state of the Flash memory from Read mode to any other mode. In addition, the three control pins must be in their correct state ($\overline{CE}$ = Low, $\overline{OE}$ = High, and $\overline{WE}$ = Low) in order to accept a command from the data bus.

A number of additional procedures are available to further prevent inadvertent writes should system glitches occur during system/device power transitions:

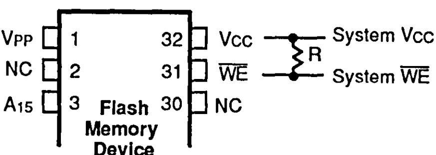
- Hold any control pin ($\overline{CE}$, $\overline{OE}$, or $\overline{WE}$) in a non-write condition. This disables the device from executing a write operation. Please refer to following example.
- Any "illegal" command (an illegal command is one that is not defined in the AMD Flash Memory data sheet under the section – Command Definitions) written to the Flash device will automatically terminate any operation and reset the device to the Read Mode.

4. Umbilical Cord Programming

Many applications perform system updates using the umbilical cord or edge connector programming method. The external programming equipment supplies the 12.0 V ±0.6 V V_{PP} voltage. When the umbilical cord is disconnected, be aware that electrostatic discharge may build up on the floating V_{PP} pin. To prevent this

Example:

Holding $\overline{WE}$ in a non-write condition during power transitions.



In systems where the V_{PP} pin is to be connected directly to the +12 V supply, $\overline{WE}$ should be held in a non-write state during power supply transitions. This will prevent against inadvertent write conditions. One way to achieve this is by pulling $\overline{WE}$ up to V_{CC} via a 2.7 K Ohm resistor.

During power supply transitions, V_{PP} voltage is internally disabled from the Flash device until V_{CC} rises above 2 V. In addition, the Flash device automatically resets to the read mode as V_{CC} rises above 2 V. The $\overline{WE}$ pin will be pulled up (V_{IH} = 2 V) via the 2.7 K Ohm resistor as V_{CC} rises. When write enable is at V_{IH} the command register is internally disabled from the internal state machine of the Flash device. When the command register is disabled, data commands can not be transferred to the state machine. Therefore the state of the Flash device will not be altered from the read mode. Access to the command register will be prevented until the $\overline{WE}$ line is driven to a logic level low by the system write control.

Note: V_{IH} Min. = 2.0 V R = 2.7 K

problem, tie the V_{PP} pin to ground via a large (10K Ω) pull-up resistor and a capacitor.

V_{PP} Layout and Circuitry

Be aware that AC current is a component of DC power switching characteristics. Design the printed circuit board traces handling this current to accommodate high frequency.

Printed Circuit Board Trace Layout: Use a single ground plane to eliminate potential loops. Keep all inductive impedances at a minimum on all high current traces.

V_{PP} Regulator Circuitry Layout: Locate the V_{PP} generation circuitry as close to the Flash memory array as possible. In addition, minimize lead lengths of the network. To help prevent noise from being picked up in feedback loops, locate all resistors and capacitors as close to the V_{PP} network as possible. In order to prevent input ground loops, use separate returns for input and output capacitors.

Device Decoupling

evice Decoupling

/itching $\overline{CE}$ inputs for memory selection causes nsient current peaks at the Flash device. The Flash emory devices should be decoupled with the propriate capacitance.

Connect a 0.1 µF ceramic capacitor between V_{CC} and V_{SS} and one between V_{PP} and V_{SS}. The capacitors should be placed as close to each device as possible.

In addition, connect a 4.7 µF electrolytic capacitor between V_{CC} and V_{SS} on the memory arrays' power supply. Do this for each set of eight memory devices. This bulk capacitor will maintain even voltage to the memory array.

ystem Initialization

uring remote code updates the possibility that the mmunication link could be disrupted during a repro- amming sequence exists. Should this occur, the state the Flash device (Erased, Partially Programmed, c.) may not be known. Bootcode should always reset e Flash memory as part of the initialization sequence. lso, status flags should be read to determine the state the Flash device upon reset.

ystems that are designed for remote updates should ontain the following as at least a subset of the ootcode program:

In-system reprogramming routines for Flash,

Standard initialization and diagnostic routines,

A set of communication routines,

s part of the boot code. The boot code can be cost ffectively stored in an AMD ExpressROM™ as a eparate memory device.

s with any logic device, the Reset command initializes ie Flash memory to a known state: the Read mode. his is accomplished by writing the Reset command vice in succession to the Flash device. This should ccur in the first part of the system initialization routine.

irst we will discuss resetting the Flash device as part of he initialization sequence. Then we will discuss the use f reprogramming flags to keep track of the state of the lash device after remote updates (i.e., does the nemory content contain valid data).

nterrupt Sequences

nterrupt sequences should always reset the Flash levice as the first part of any routine. In addition, it is advisable to disable the V_{PP} voltage during interrupts. The Reset command should be written twice in a row to all Flash devices as part of the interrupt sequence. This resets the Flash device to the Read mode. Reset the Flash device as the initial commands of any routine. This procedure is also relevant should a software or hardware reset occur while the system is in the process of reprogramming the Flash memory. By including the consecutive reset command sequence in the bootcode the erase or program operations will be terminated when the system reboots.

Hardware resets may be implemented by connecting the reset signal directly to an interrupt controller. The software interrupt sequence to reset the Flash memory is then executed by the controller.

Data Transmission

In order to guarantee accurate data updates, reprogramming protocols may include echo techniques or error-free transmission algorithms.

The echo technique is a straight forward approach to verify transmission of accurate data. The remote system sends back the Flash memory instructions (i.e. Set-up Erase/Erase) to the host system. The remote system waits for a confirmation of the instruction prior to execution. Once the memory array is reprogrammed, the remote system transmits the data to the host for verification. Upon confirmation the remote system programs the Data Valid word. This concept is explained in the Data Valid section.

Handshaking

Communication protocols for the host system in charge of remote updates should require a status check from the target system prior to sending reprogramming commands. If the system indicates it is available, the appropriate command is issued by the host system. Should the remote system indicate it is not available the host may break the communication link and wait for a request to reconnect later. Handshaking protocols are recommended in applications where system downtime is not acceptable to accommodate reprogramming routines.

Data Valid Flags

Once the Flash memory and other system components have been reset the system should check for the validity of data contained in the Flash memory devices. This is an issue when the system resets or the communication link is disrupted during remote reprogramming routines.

The system should check the Flash device for valid data upon initialization.

The Data Valid flag is a data word that is the final word programmed into the Flash array. This word is pro-

ray. The Data Valid word will not be programmed if the memory array data is invalid or the communication link was disrupted during a reprogramming sequence. During system initialization the CPU will look for the Data Valid word. If it is not programmed, the system will recognize that the Flash memory is not programmed with accurate data. The Flash memory must be accurately programmed before the system initialization routine can be completed.

Data Protection

Because AMD's Flash memories are designed to be reprogrammed in-system AMD has incorporated a number of data protection methods against inadvertent erase or program.

Software

AMD's Flash Memories require a two-cycle Write command to initiate either the erase or program operations. Refer to the Set-up Erase/Erase or Set-up Program/ Program commands. These commands drive an internal state machine that controls the device operation. The state machine is designed to expect the first Write cycle command to be a set-up command. Set-up commands will not alter the memory data. Successful execution of the appropriate second Write cycle command will initiate the erase or program operations.

Control Inputs

AMD's Flash memory devices require that $\overline{OE} = V_{IH}$ and $\overline{CE} = \overline{WE} = V_{IL}$ in order to load the register with a command. If any pin is not in the correct state a write cycle cannot be initiated.

V_{PP} Voltage

AMD's Flash device is designed to disable the command register whenever V_{PP} falls below V_{CC} + 2 V. When V_{CC} = 0 V, the command register internally disables the V_{PP} voltage from the device. When V_{PP} = 12 V, the Flash device resets to the Read mode when V_{CC} rises above 2 V. When the command register is disabled, the memory array contents cannot be altered.

Power supply sequencing is not required.

AUTO SELECT COMMAND

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Programming In-System

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto the address lines is not a generally desired system design practice.

AMD's Flash memories contain an Auto select operation to supplement traditional PROM programming methodology. The operation is initiated by writing either 80H or 90H into the command register. Following this command, a Read cycle from address 0000H retrieves the manufacturer code of 01H. A Read cycle from address 0001H returns the appropriate device code. To terminate the operation, it is necessary to write another valid command into the register.

Data Change Sequence

Flash memories perform data change cycles differently than full-featured E^2PROMs. Flash memories must always be completely programmed prior to erasure. This ensures against over-erasure, because all bytes are erased from the fully programmed state.

A data change sequence will include the following:

- Program the entire array to 00H data using the Flashrite™ Algorithm.
- Bulk-Erase the entire device using AMD's Flashrite™ Algorithm.
- Program the array with the appropriate data pattern using AMD's Flashrite™ Algorithm.

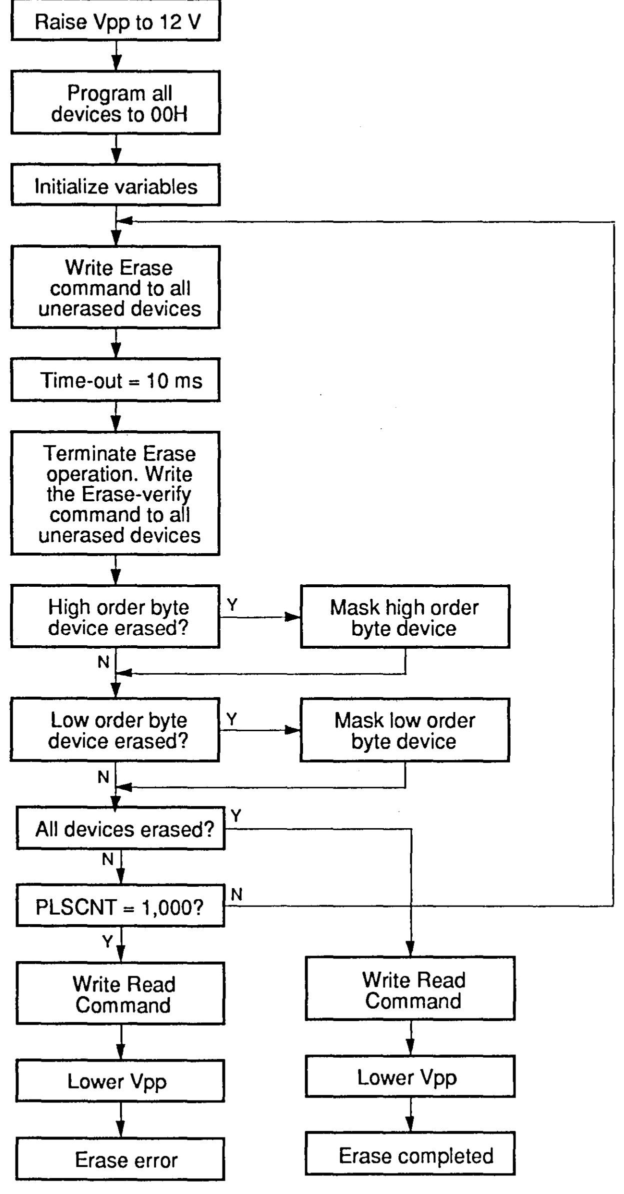
As long as the user follows AMD's Flasherase™ and Flashrite™ Algorithms, the device will not over-erase.

MULTIPLE MEMORY ARRAYS

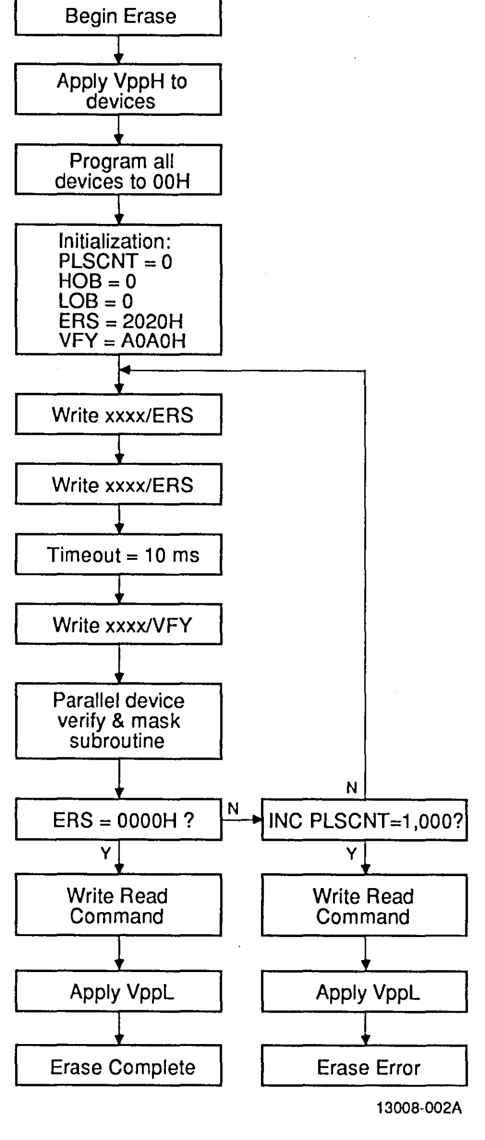
Many applications require multi-memory device arrays. AMD's Flash memories provide the standard $\overline{OE}$ and $\overline{CE}$ device control inputs. These two controls allow for specific selection of one memory device in an array and help prevent the potential for bus contention. Because all non-selected memories may be left in standby mode, the memory arrays' power dissipation is maintained at its lowest level.

The $\overline{CE}$ control pins should be driven by the outputs of an address decoder. The system's memory Read and Write signal should control the $\overline{OE}$ and $\overline{WE}$ controls of the memory array respectively.

PARALLEL DEVICE ERASURE—OVERVIEW



PARALLEL DEVICE ERASURE FLOW CHART



Activity

Allow V_{PP} to stabilize.

Follow Flashrite programming algorithm.

Initialize Erase Variables:
PLSCNT = Pulse Counter
HOB = High Order Address Byte
LOB = Low Order Address Byte
ERS = Erase Command
VFY = Erase-verify Command

xxxx = Address do not care.
Write Erase Set-up command.

Initiate erase pulse.

Duration of erase pulse.

Erase-verify command terminates the erase pulse.

See Parallel Device Erasure subroutine. Each device is independently verified. The command is masked by the Read command (00H) for all devices that are completely erased.

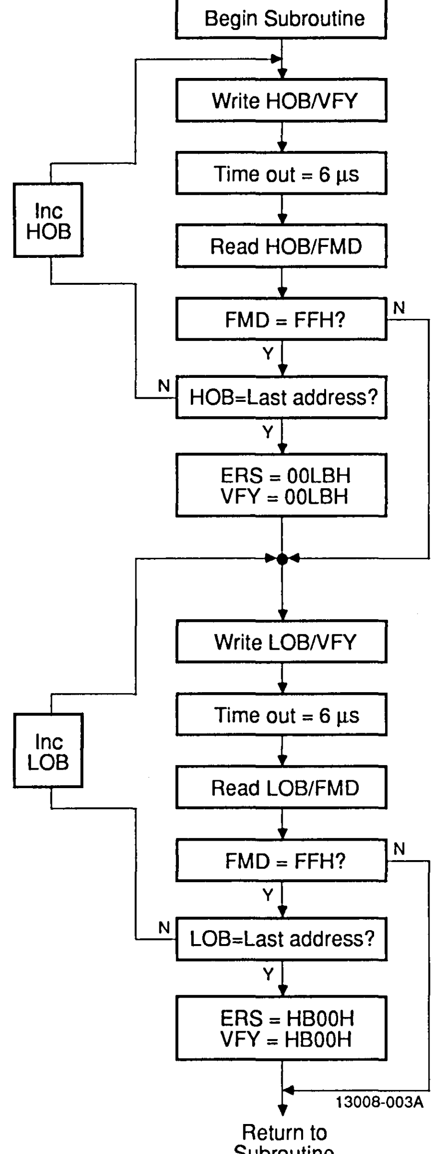
ERS = 0000H when all devices are erased.

Reset devices for read operation.

$V_{PP}L$ deactivates the command register. Device is in the Read Only Mode.

PARALLEL DEVICE ERASURE—SUBROUTINE

High Order Byte and Low Order Byte Device Program Verify and Mask Subroutine.



Activity

The Subroutine verifies each device independently and masks the completely erased device from further erasure.

Verify High Order Byte Device:
Addresses are latched (HOB) on Erase-verify command.

Internal margin verify voltages are tapped from external 12 V V_{PP} for proper byte verification.

Read HOB from previously latched Address.
FMD = Flash Memory Data.

Compare Flash Memory Data to FFH. If verified, then compare next high order byte address. If invalid, then Jump to low order byte device.

If all addresses of the high order byte device are verified, mask the Erase and Verify commands with the Read command, (00H). Low order byte (LB) device commands are not altered.

Verify Low Order Byte:
Addresses are latched (LOB) on verify command.

Internal margin verify voltages are tapped from external 12 V V_{PP} for proper byte verification.

Read LOB from previously latched address. FMD = Flash Memory Data.

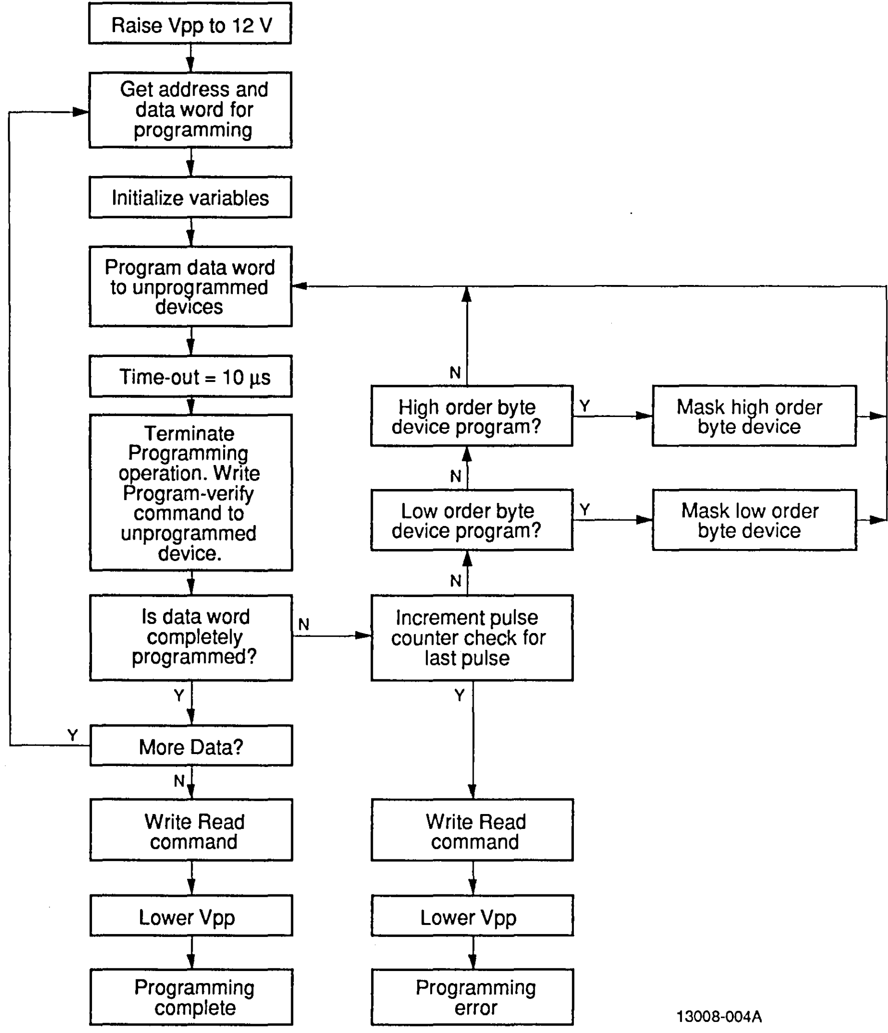
Compare Flash Memory Data to FFH. If verified, then compare next low order byte address. If invalid, return to main parallel erase flow for next erase pulse.

If all addresses of the low order byte device are verified, mask the erase and verify command with the read command (00H). High order byte (HB) device commands are not altered.

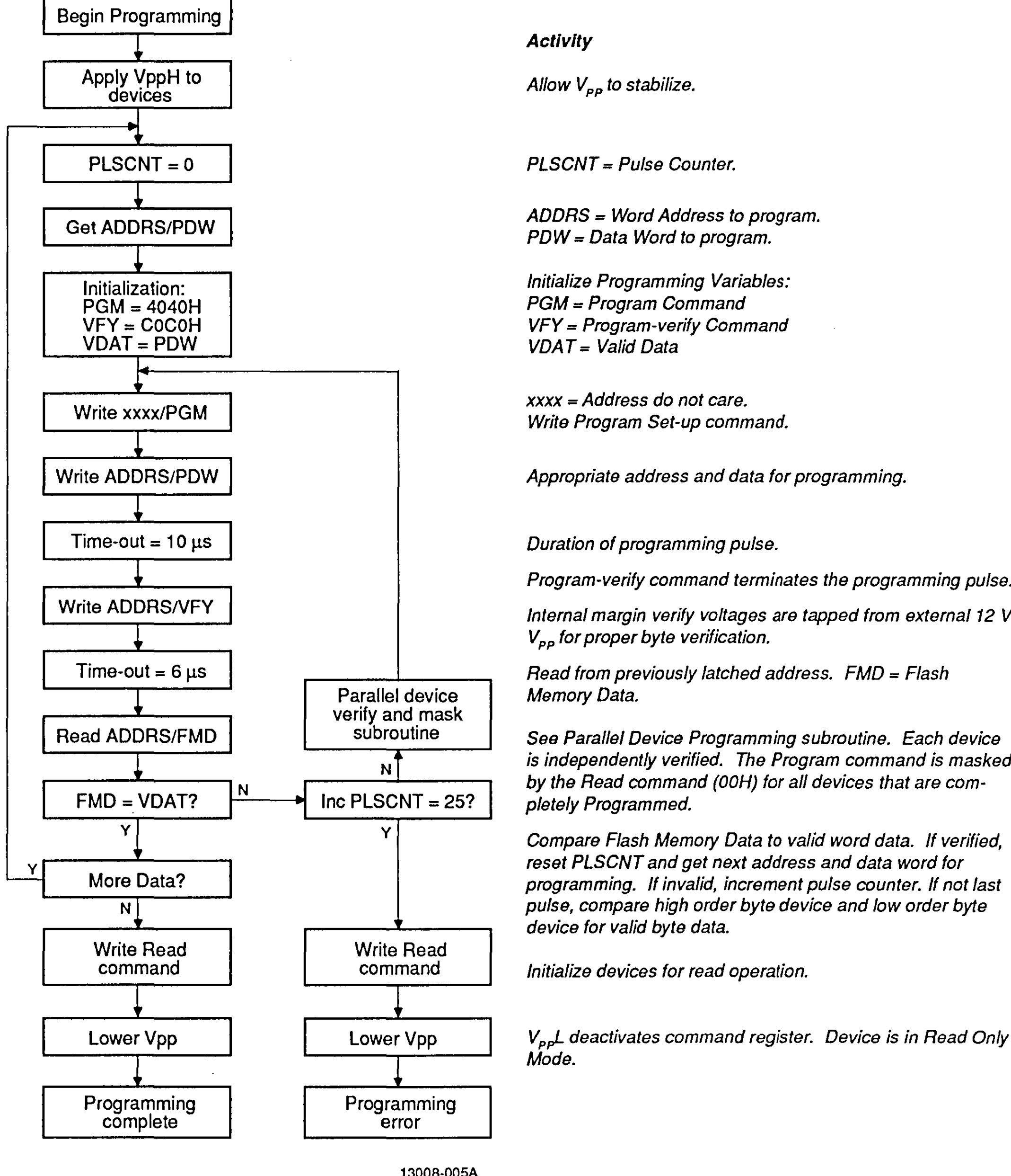
Parallel Device Erasure

A bank of Flash memories may be erased in parallel. This reduces total erase time when compared to erasing each device individually. Each Flash memory may erase at different rates. Therefore each device must be verified separately after every erase pulse. Once a device has successfully completed erasure do not issue the erase command again to that device. Issue the Read command 00H to the erased device. The Erase command sequence may be issued to each of the remaining devices that have not erased yet. In addition to the address verify register required for each device you will need an erase complete flag for each device.

PARALLEL DEVICE PROGRAMMING – OVERVIEW



PARALLEL DEVICE PROGRAMMING FLOW CHART



13008-005A

Example: Parallel Erasure and Programming for Two Devices

Parallel Erasure

The erase sequence will be followed as usual. The CPU will issue word commands. The erase word command is 2020H. Each device is independently verified and the address of the last verified byte per device is stored in separate registers. When one of the erase flags is active, indicating that a particular device has successfully completed erasure the CPU will change the command for that device from Erase to Read. This effectively masks the erased device from further erasure.

Should the high order byte device verify first, the next erase command will be 0020H. The low order byte device erases on each subsequent erase command until verified. The high order byte device remains in Read mode. During verification, write the erase verify command of 00A0H. This will enable the low order byte device for verify operations and maintains the erased high order byte device in Read mode.

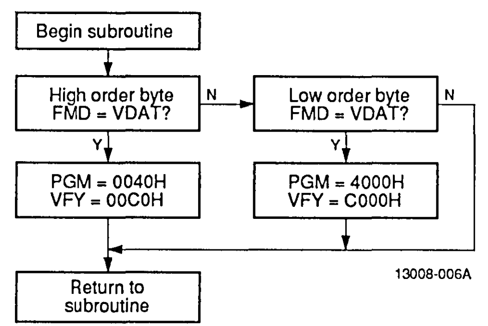
Parallel Programming

The program sequence will be followed as usual. The CPU will issue word commands. The program word command is 4040H. Each device is independently verified. When one of the program flags is active, indicating that a particular device has successfully completed programming, the CPU will change the command for that device from Program to Read. This effectively masks the programmed device from further programming.

Should the high order byte device verify first, the next program command will be 0040H. The low order byte device programs on each subsequent program command until verified. The high order byte device remains in Read mode. During verification, write the program verify command of 00C0H. This will enable the low order byte device for verify operations and maintains the programmed high order byte device in Read mode.

PARALLEL DEVICE PROGRAMMING – SUBROUTINE

High Order Byte and Low Order Byte Device Erase-verify and Mask Routine



This Subroutine verifies the high order and low order bytes independently. If either byte verifies, all commands are masked from that device.

The program command and program data are changed to a read command (00H) and null data (FFH) respectively.

The Program-verify command is changed to a Read command (00H).

Notes:

- During programming operations the FFH data is a null condition.
- If the high order byte verifies, then that byte is masked from further Program/Program-verify operations. The low order byte (LB) commands are not changed.
- If the low order byte verifies, then that byte is masked from further Program/Program-verify operations. The high order byte (HB) commands are not changed.

CHAPTER 4 AN-102
Generation and Control of V_{PP} Programming Voltage for Flash Memories

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Generation and Control of V_{PP} Programming Voltage for Flash Memories

AN–102

INTRODUCTION

Constant V_{PP} voltage of 12.0 V ±0.6 V is required for erase and programming operations. Parallel device reprogramming (either 16-bit or 32-bit data words) requires 30 mA of current for each device in the Flash memory array.

V_{PP} voltage may be generated in a number of ways. Each of these options will be discussed during the text.

1. Hardwire V_{PP} Voltage to the Flash Device.
2. Umbilical Cord Type Programming.
3. Use DC/DC Convertor to pump 5 V to V_{PP} Voltage.
4. Pump 5 V to V_{PP} Voltage with Analog Circuitry.

It is important to maintain the specified V_{PP} voltages when programming the Flash memory device. All internal device voltages are generated from the V_{PP} reference. Inappropriate V_{PP} voltage may impair device performance. Internal voltages do not exceed that of external V_{PP}.

Unlike other approaches to Flash memories, AMD's devices actually verify margin for each byte during erase and programming operations. This is accomplished during the Erase-verify and Program-verify operations respectively. During these operations, the appropriate margin-verify voltages are internally tapped off of the V_{PP} voltage via the command register and internal V_{PP} circuitry. This allows for Erase/Erase-verify and Program/Program-verify operations to be performed with static V_{CC} (5 V) and V_{PP} (12 V) voltages.

Before proceeding, a few comments regarding basic design philosophy should be mentioned. Please make note of these comments for any of the V_{PP} generation methods implemented.

V_{PP} Trace and Circuitry

Be aware that AC current is a component of DC power switching characteristics. Design the printed circuit board traces handling this current to accommodate high frequency.

Printed Circuit Board Trace Layout

Use a single ground plane to eliminate potential loops. Keep all inductive impedances at a minimum on all high current traces.

V_{PP} Regulator Circuitry Layout

Locate the V_{PP} generation circuitry as close to the Flash memory array as possible. In addition, minimize lead lengths of the network. To help prevent noise from being picked up in feedback loops, locate all resistors and capacitors as close to the V_{PP} network as possible. In order to prevent input ground loops, use separate returns for input and output capacitors.

Device Decoupling

Switching $\overline{CE}$ inputs for memory selection causes transient current peaks at the Flash device. The Flash memory devices should be decoupled with the appropriate capacitance from these transients.

- Connect 0.1µF ceramic capacitor between V_{CC} and V_{SS} and one between V_{PP} and V_{SS}. The capacitors should be placed as close to each device as possible.
- In addition, connect 4.7µF electrolytic capacitor between V_{CC} and V_{SS} on the memory array's power supply. Do this for each set of eight memory devices. this bulk capacitor will maintain even voltage to the memory array.

1. HARDWIRE V_{PP} VOLTAGE TO THE FLASH DEVICE

Typically this approach is used in the most cost sensitive applications. Regulated 12.0 V supplies are commonly available in many systems.

When V_{CC} = 0 V, the V_{PP} voltage is internally disabled from the device. Memory contents cannot be altered. The Flash device automatically resets to the read mode when V_{CC} rises above 2 V. This occurs even when V_{PP} = 12 V.

Power supply sequencing is not required.

The device will only respond to the correct sequence of commands in order to change the state of the Flash memory from Read mode to any other mode. In addition, the three control pins must be in their correct state ($\overline{CE}$ = Low, $\overline{OE}$ = High and $\overline{WE}$ = Low) in order to accept a command from the data bus.

A number of additional procedures are available to further prevent inadvertent writes should system glitches occur during system/device power transitions.

- Hold any control pin ($\overline{CE}$, $\overline{OE}$, or $\overline{WE}$) in a non-write condition. This disables the device from executing any write operation (see example on the next page).
- Any "illegal" command (an illegal command is one that is not defined in the AMD Flash data sheet under the section – Command Definitions) written to the Flash device will automatically terminate any operation and reset the device to the Read Mode.

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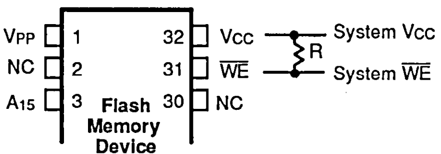
Publication #	Rev.	Amendment	Issue Date
10934	A	/0	5/90

Example:

Holding $\overline{WE}$ in a non-write condition during power transitions.



In systems where the V_{PP} pin is to be connected directly to the +12 V supply, $\overline{WE}$ should be held in a non-write state during power supply transitions. This will prevent against inadvertent write conditions. One way to achieve this is by pulling $\overline{WE}$ up to V_{CC} via a 2.7 K Ohm resistor.

During power supply transitions, V_{PP} voltage is internally disabled from the Flash device until V_{CC} rises above 2 V. In addition, the Flash device automatically resets to the read mode as V_{CC} rises above 2 V. The $\overline{WE}$ pin will be pulled up (V_{IH} = 2 V) via the 2.7 K Ohm resistor as V_{CC} rises. When write enable is at V_{IH} the command register is internally disabled from the internal state machine of the Flash device. When the command register is disabled, data commands can not be transferred to the state machine. Therefore the state of the Flash device will not be altered from the read mode. Access to the command register will be prevented until the $\overline{WE}$ line is driven to a logic level low by the system write control.

Note: V_{IH} Min. = 2.0 V R = 2.7 K

2. UMBILICAL CORD PROGRAMMING

Many applications perform system updates using the umbilical cord or edge connector programming method. The external programming equipment supplies the 12.0 V ± 0.6 V V_{PP} voltage. When the umbilical cord is disconnected, be aware that electrostatic discharge may build up on the floating V_{PP} pin. To prevent against this problem, tie the V_{PP} pin to ground via a large (10KΩ) pull-up resistor and a capacitor (see Figure 1).

3. V_{CC} (5.0 V) to V_{PP} (12.0 V) DC/DC Convertor

A monolithic DC/DC convertor from Valor Electronics, the PM9006, is appropriate for the digital world to supply the 12.0 V ±0.6 V V_{PP} voltage. The V_{PP} voltage is generated on chip using the standard system V_{CC} (5.0 V) voltage. Standard TTL commands are used to disable the 12.0 V output supply when programming or erasing operations are not intended. The enable ($\overline{E}$) function provides absolute write protection to guarantee against inadvertent program or erasure. Flash memory contentscannot be altered without the active 12.0 V V_{PP} supply. The enable pin also saves system power when DC/DC convertor is not required. The PM9006 has a minimum efficiency of 50% at full load. The PM9006 comes in a 24-pin package.

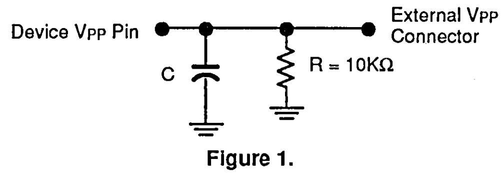


Figure 1.

The Valor PM9006 provides a controlled 12.0 V output that is regulated within the ±5% (±0.6 V) V_{PP} specification. The standard system V_{CC} (5.0 V) supply is converted to the V_{PP} (12.0 V) supply by the DC/DC convertor. The voltage transitions are smooth and protect against destructive positive or negative overshoot.

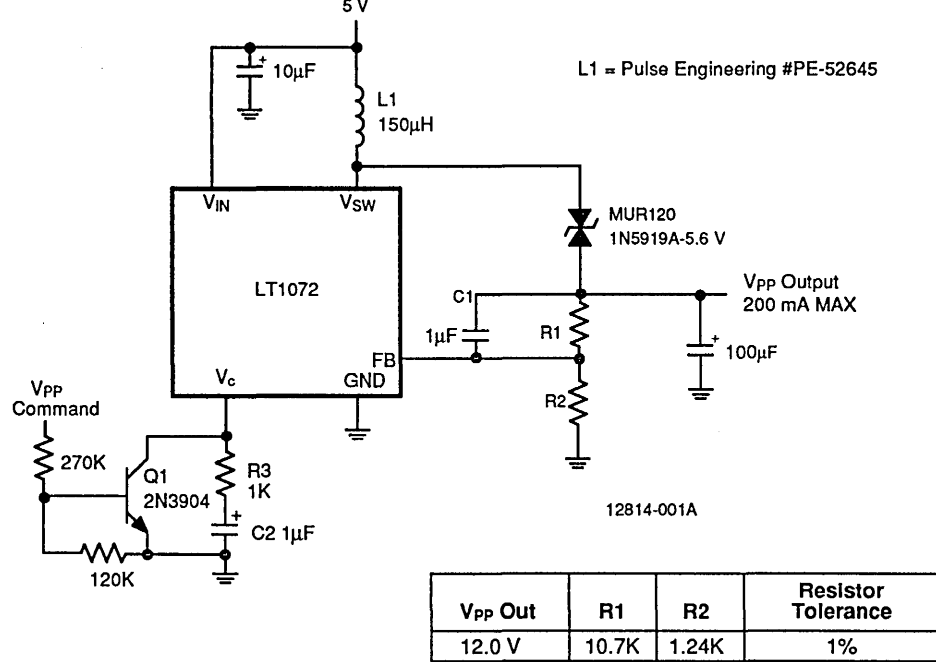
The PM9006 can supply 165 mA of current at the regulated 12.0 V ±0.6 V output. The 5.0 V ±0.5 V DC input supply of the DC/DC convertor uses a maximum of 840 mA of input current. The Am28F010 specifies a maximum V_{PP} current of 30 mA for either the erase or program operations. Actual current required for these operations is substantially lower than this. Given the maximum V_{PP} current of 30 mA for each device, four(4) Am28F010 may be programmed and erased in parallel with one PM9006 device. The PM9006 V_{PP} supply current = 165 mA – 4 x 30 mA of V_{PP} current required for the Flash memory array = 45 mA of additional current available from the DC/DC convertor.

Parallel programming and erasure allows for the most efficient method to reprogram x16 or x32-bit data words. Refer to application note AN-101 for parallel program and erasue flow charts.

Board Level Resets

System designs should not allow the Flash device to perform any programming or erase operations when the CPU does not have control of the Flash device. Some designs incorporate board level reset circuitry that suspends operation of the local CPU if the V_{CC} level falls below a predetermined value (such as 4.6 V). If this is the case, the reset circuitry should also disable the V_{PP} power supply whenever the CPU is held in reset.

If the local CPU is forced into reset mode while it is programming or erasing the Flash device, the system reset circuit should also terminate that operation. To accomplish this, the PM9006's enable pin should be driven high whenever the reset circuitry is active. Drive the chip enable pin of the PM9006 with the logical OR of the reset circuit's output signal and the chip enable control line to the PM9006. This will disable the V_{PP} supply and hence terminate any programming or erase operation. The Flash device automatically resets to the read mode when V_{PP} is disabled.



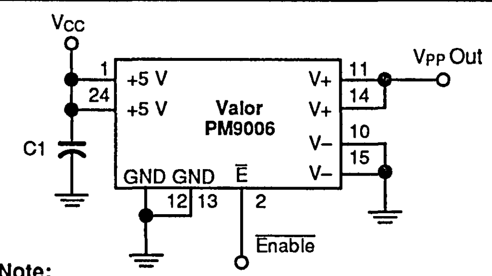
V_{PP} Out	R1	R2	Resistor Tolerance
12.0 V	10.7K	1.24K	1%

Note:

The circuit of Figure 2 will not spuriously overshoot during power-up or power-down. This prevents destruction of the device due to voltages that exceed specification. V_{PP} outputs are predictable and controllable during power supply transitions as a result of the referenced circuit designs. The compensation of the LT1072 causes a very overdamped pulse response. In addition, the control loops of the circuit are functioning even at low supply voltages. Thus the control loop is active before the memory circuits settle and prevents uncontrolled V_{PP} pulse outputs.

Figure 2. Basic Flash Memory V_{PP} Programming Voltage Supply

Please reference the PM9006 data sheet for complete details of device operation. One method of implementing the PM9006 DC/DC convertor is illustrated below.



Note:

Pins 3 through 9 and 16 through 23 are not internally connected to the device and do not need to be driven.

Generate and Control 12.0 V

4. PUMP 5 V TO V_{PP} VOLTAGE WITH ANALOG CIRCUITRY

Flash memories require a V_{PP} voltage of 12.0 V ±0.6 V. It is important to note that V_{PP} voltage must be maintained within the device specification for reliable operation. V_{PP} voltages that exceed 14 V for 20 ns or longer are likely to destroy the device. Thus, we need to carefully control the high voltage programming circuitry. It should be noted that proper design of the V_{PP} circuitry eliminates the issues of device destruction due to application of voltages outside of the specified operating range. In addition, it is preferable to control the V_{PP} voltage with a 5.0 V logic command.

The Starter Kit: V_{PP} Generation and Control

The basic circuit described in Figure 2 satisfies just about all V_{PP} requirements for Flash memories. High voltage is produced by driving the V_{PP} command low. The low V_{PP} command (Trace A, Figure 3) activates the LT1072 switching regulator to drive L1. The resistor net-

work of R1 and R2 provides the DC feedback. C1, R3 and C2 control the AC roll-off. Trace B illustrates the resulting V_{PP} voltage that rises smoothly to the required level. The values specified for R1 and R2 determine the12.0 V output. Leave the 5.6 V zener in the circuit in order to return the output to 0 V when the V_{PP} command goes high. When a 4.5 V minimum output is desired the zener may be omitted. Circuit trimming requirements are eliminated due to the tight internal references of the LT1072. Only precision resistors are required.

The table in Figure 4 gives additional information required to provide greater power output from the referenced circuit. The synchronous switch option of Figure 4 may replace the zener and eliminate its power dissipation.

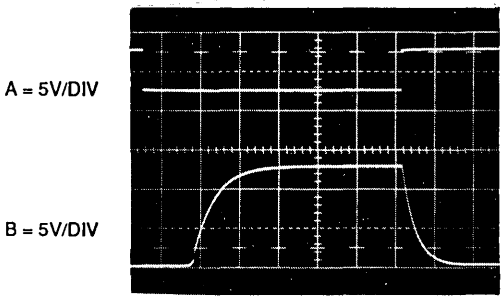
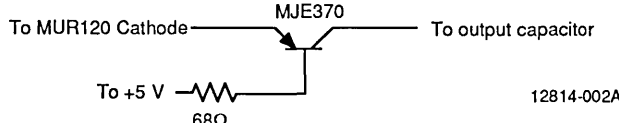


Figure 3. Waveforms for Basic Flash Programming Supply



Power Options for Basic V_{PP} Generator

Output Current	C_{OUT}	Regulator	Inductor	Zener
400mA	200 µF	LT1071	PE-52645	1N5339A or Synchronous Switch Option
800mA	400 µF	LT1070	PE-51516	1N5339A or Synchronous Switch Option

Note:
Assume each Flash device requires 30mA V_{PP} current.

Figure 4. Synchronous Switch Option

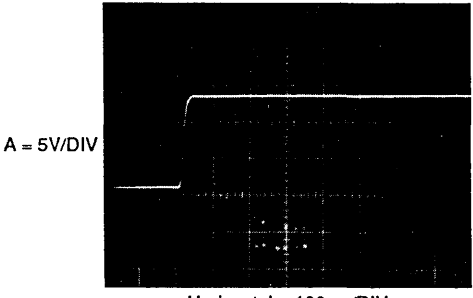


Figure B1. An "Ideal' Flash Memory V_{PP} Output

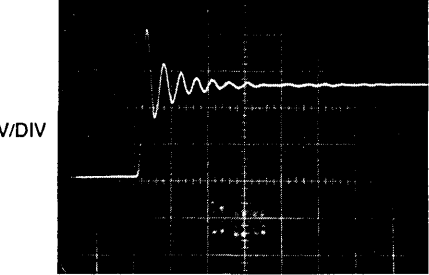


Figure B2. Rings at Destructive Voltages After a PC Trace Run

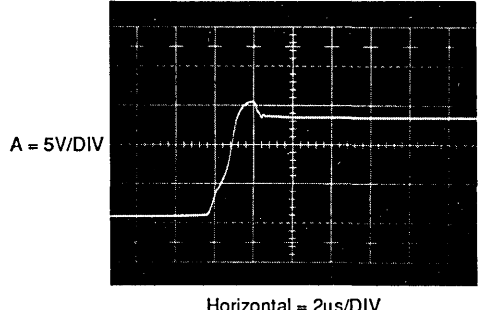


Figure B3.

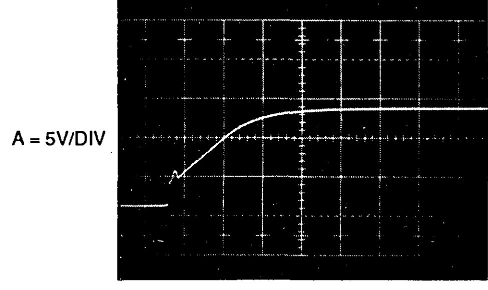


Figure B4.

Note:

Short Circuit Recovery for Poorly (Figured B3) and Properly (Figure B4) Designed Connections. Figure B3's Overshoot on Recovery Can Cause Memory Chip Failures

Transmission Line Effects of Printed Circuit Board Traces on V_{PP} Voltages

One might ask: "Why not use a simple low resistance FET to switch the output of the switching regulator when its level is correctly set?" This sounds good – too good.

In real life, the printed circuit board traces exhibit transmission line effects. Voltages seen at the memory device's pins are not the same as at the output of the regulator. Overshoots result at the junction of the printed circuit board trace and device pins. Thus voltages may exceed device specifications. This concern is compounded since the V_{PP} supply voltages are unusually close to the device's absolute maximum limit of 14V.

Figure B1 illustrates an ideal V_{PP} pulse seen at the output of a simple low loss transistor that is switching the power supply. No overshoot is observed and the V_{PP} pulse settles quickly. The same output is measured (Figure B2) at the memory device pins after running the printed circuit board trace.

Because of mismatching, the PCB trace appears as an unterminated transmission line. Ringing can exceed 20V because of reflections at the junction of the PC trace and device pin. This condition is obviously detrimental to the device. The negative overshoot occurring on the falling edge of the V_{PP} transition may cause equally destructive negative voltages at the device pins.

Properly controlled V_{PP} rise time prevents this type of overshoot. The closed loop circuits discussed earlier eliminate overshoot through controlled edge timings. In addition, the referenced circuits protect the V_{PP} generator against short circuit damage which also protects the memory device.

The V_{PP} output recovery when the diode is removed is shown in Figure B3. Contrast this with Figure B4. Here the diode is in place and the V_{PP} recovery is smooth. Similar considerations apply during power-up/down. During application or removal of power, the V_{PP} generator must not produce spurious output pulses.

V_{PP} outputs are predictable and controllable during transient power supply considerations as a result of the referenced circuit designs. The compensation of the LT1072 causes a very overdamped pulse response. In addition, the control loops of the circuit are functioning even at low supply voltages. Thus the control loop is active before the memory circuits settle and prevent uncontrolled V_{PP} pulse outputs.

Note:

The above circuitry is designed for maximum system protection. Should you desire to modify any circuity, it is advisable to contact Jim Williams of Linear Technology.

This Document was adapted from Linear Technology's Application Note 31 "Linear Circuits for Digital Sytems: Some Affable Analogs for Digital Devotees," written by Jim Williams, February, 1989.

Chapter 5
Product Data Sheets

Am28F256 32,768 x 8-Bit CMOS Flash Memory 5–1
Am28F512 65,536 x 8-Bit CMOS Flash Memory 5–30
Am28F010 131,072 x 8-Bit CMOS Flash Memory 5–59
Am28F020 262,144 x 8-Bit CMOS Flash Memory 5–88

Preliminary

Am28F256

32,768 x 8-Bit CMOS Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 70 ns maximum access time
- **Low power consumption**
  - 30 mA maximum active current
  - 100 µA maximum standby current
- **Compatible with JEDEC-standard byte-wide 32-Pin E²PROM pinouts**
  - 32-pin DIP
  - 32-pin PLCC
- **10,000 erase/program cycles**
- **Program and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to V_{CC}+1 V**
- **Flasherase™ Electrical Bulk Chip-Erase**
  - One second typical chip-erase
- **Flashrite™ programming**
  - 10 µs typical byte-program
  - Less than 0.5 second typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell

GENERAL DESCRIPTION

The Am28F256 is a 256K "Flash" electrically erasable, electrically programmable read only memory organized as 32K bytes of 8 bits each. The Am28F256 is packaged in 32-pin PDIP and PLCC versions which allow for upgrades to the 2 Megabit density. The device is also offered in ceramic DIP and LCC packages. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers.

The standard Am28F256 offers access times as fast as 70 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F256 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F256 uses a command register to manage this functionality, while maintaining a standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

AMD's Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F256 uses a 12.0 V ± 5% V_{PP} supply to perform the Flasherase and Flashrite algorithms.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from –1 V to V_{CC}+1 V.

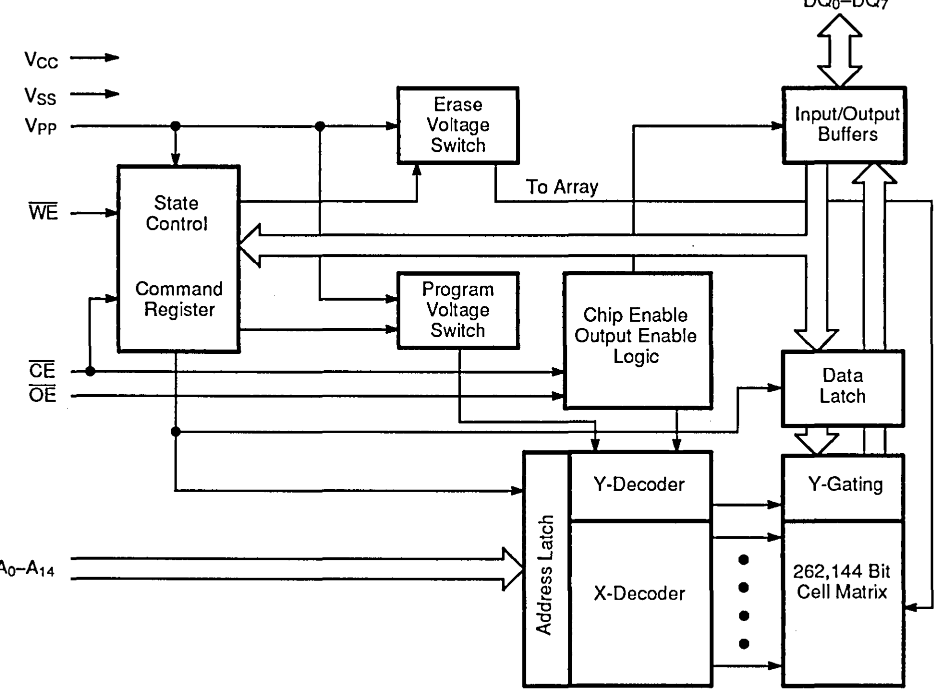
The Am28F256 is byte programmable using 10 µs programming pulses in accordance with AMD's Flashrite programming algorithm. The typical room temperature programming time of the Am28F256 is less than one half a second. The entire chip is bulk erased using 10ms erase pulses according to AMD's Flasherase algorithm. Typical erasure at room temperature is accomplished in less than one second. The windowed package and the 15–20 minutes required for EPROM erasure using ultraviolet light are eliminated.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F256 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

AMD's Flash technology combines years of EPROM and E²PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F256 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

Publication# 11560 Rev. B Amendment/0
Issue Date: June 1990

BLOCK DIAGRAM

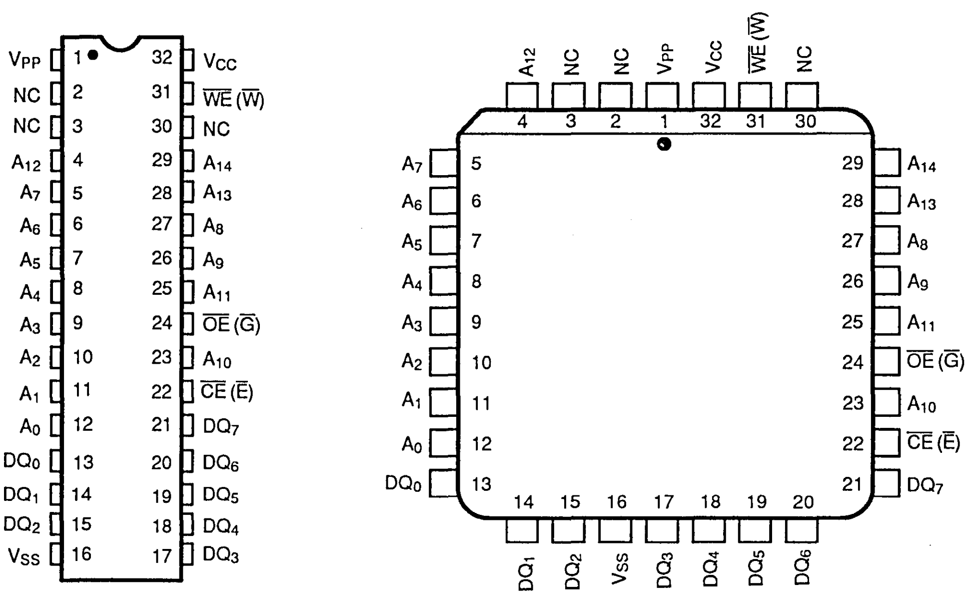


11561-001B

PRODUCT SELECTOR GUIDE

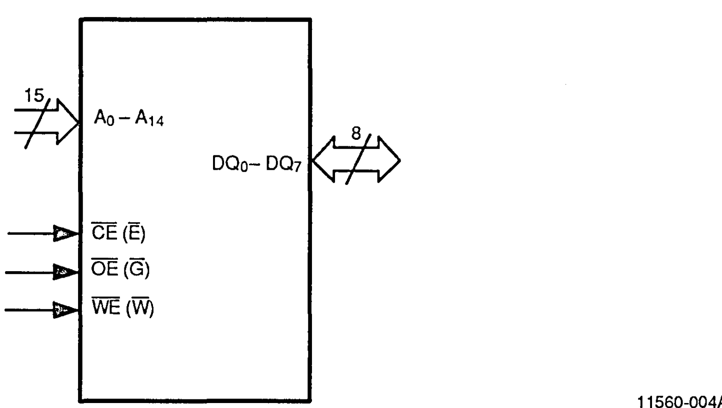
Family Part No.	Am28F256				
Ordering part No: ± 10% V_{CC} Tolerance	—	–90	–120	–150	–200
± 5% V_{CC} Tolerance	–75	–95	—	—	—
Max Access Time (ns)	70	90	120	150	200
$\overline{CE}$ ($\overline{E}$) Access (ns)	70	90	120	150	200
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	40	50	65	75

CONNECTION DIAGRAMS



Note: Pin 1 is marked for orientation

LOGIC SYMBOL



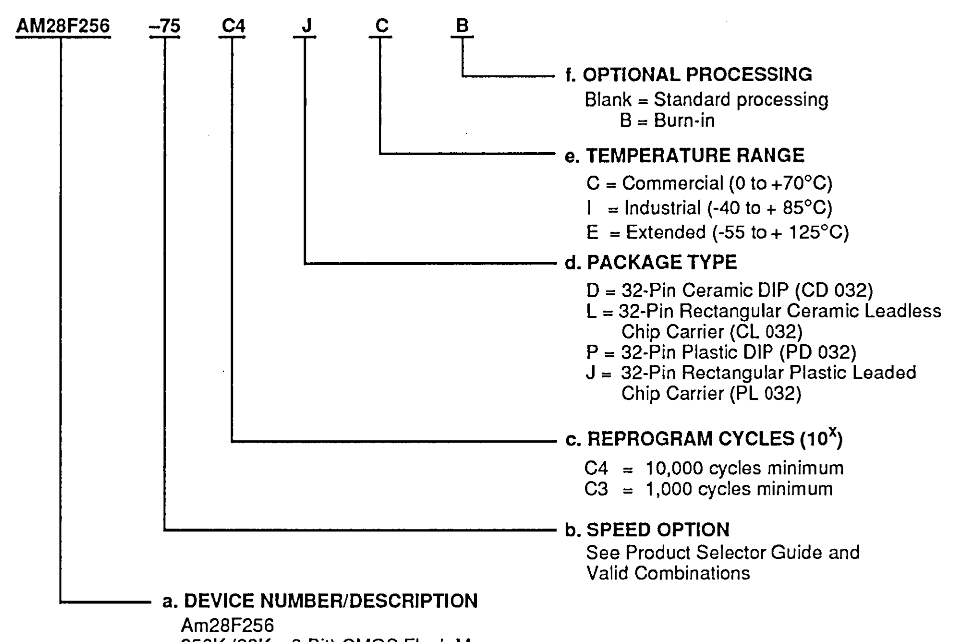
PIN DESCRIPTION

Symbol	Functional Description
$A_0 - A_{14}$	Address Inputs for memory locations. Internal latches hold addresses during write cycles.
$DQ_0 - DQ_7$	Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.
$\overline{CE}$ ($\overline{E}$)	The Chip Enable active low input activates the chip'scontrol logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.
$\overline{OE}$ ($\overline{G}$)	The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.
$\overline{WE}$ ($\overline{W}$)	The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the ap propriate data is latched on the rising edge of the pulse.
V_{PP}	Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC}$ +2V.
V_{CC}	Power supply for device operation. (5.0V ± 5% or 10%)
V_{SS}	Ground
NC	No Connect-corresponding pin is not connected internally to the die.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Reprogram Cycles
d. Package Type
e. Temperature Range
f. Optional Processing



Valid Combinations	
AM28F256-75	C4DC, C4DCB, C4DI, C4DIB, C4LC, C4LCB, C4LI, C4LIB, C4PC, C4PI, C4JC, C4JI, C3DC, C3DCB, C3DI, C3DIB,C3LC, C3LCB, C3LI, C3LIB, C3PC, C3PI,, C3JC, C3JI
AM28F256-95 AM28F256-90 AM28F256-120 AM28F256-150 AM28F256-200	C4DC, C4DCB, C4DI, C4DIB, C4DE, C4DEB, C4LC, C4LCB, C4LI, C4LIB, C4LE, C4LEB, C4PC, C4PI, C4JC, C4JI, C3DC, C3DCB, C3DI, C3DIB, C3DE, C3DEB, C3LC, C3LCB, C3LI, C3LIB, C3LE, C3LEB, C3PC, C3PI, C3JC, C3JI

Valid Combinations

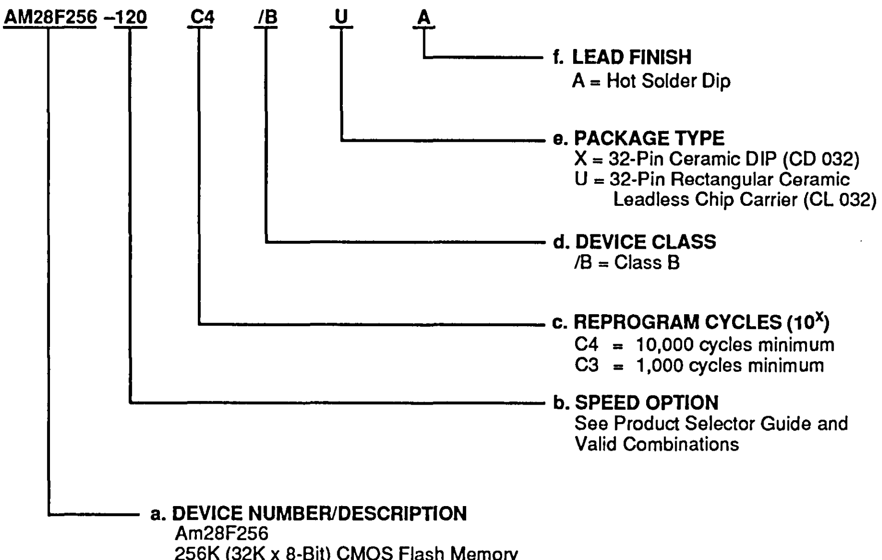
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Reprogram cycles
d. Device Class
e. Package Type
f. Lead Finish



a. DEVICE NUMBER/DESCRIPTION
Am28F256
256K (32K x 8-Bit) CMOS Flash Memory

Valid Combinations	
AM28F256-120 AM28F256-150 AM28F256-200	C4/BXA, C4/BUA C3/BXA, C3/BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

BASIC PRINCIPLES

The Am28F256 uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F256 functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F256's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F256 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Erase Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note:
The Flash memory array must be completely programmed prior to erasure. Refer to the Flasherase Algorithm.

1. **Set-up Erase:** Write the Set-up Erase command to the command register.
2. **Erase:** Write the Erase command (same as Set-up Erase command) to the command register again. The second command initiates the erase operation. The system software routines must now time-out the erase pulse width (10 ms) prior to issuing the Erase-verify command.
3. **Erase-verify:** Write the Erase-verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFH data (Byte erased). After successful data verification the Erase-verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Programming Sequence

A three step command sequence (a two-cycle Program command and one cycle Verify command) is required to program a byte of the Flash array. Refer to the Flashrite Algorithm.

1. **Set-up Program:** Write the Set-up Program command to the command register.
2. **Program:** Write the Program command to the command register with the appropriate Address and Data. The system software routines must now time-out the program pulse width (10 µs) prior to issuing the Program-verify command.
3. **Program-verify:** Write the Program-verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times.

FUNCTIONAL DESCRIPTION

Description Of User Modes

Table 1. Am28F256 User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A_0	A_9	I/O
Read-Only	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	A_0	A_9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (A1H)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A_0	A_9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A_0	A_9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2V$, See DC Characteristics for voltage levels of V_{PPH}, $0V < A_n < V_{CC} + 2V$, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC}$ +2.0V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.
3. $11.5 \leq V_{ID} \leq 13.0V$
4. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.
5. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid D_{IN} during a write operation.
7. All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A_9 and A_0 must be held at V_{IL}.

READ ONLY MODE

$V_{PP} < V_{CC} + 2V$

Command Register Inactive

Read

The Am28F256 functions as a read only memory when $V_{PP} < V_{CC} + 2V$. The Am28F256 has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC} - t_{OE}$).

Standby Mode

The Am28F256 has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5V$), consumes less than 100µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A Prom Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5V to 13.0V) on address A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to V_{CC} + 2.0V while using this Auto select mode. Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am28F256 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ_7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F256 Auto Select Code

Type	A_0	Code (HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	A1	1	0	1	0	0	0	0	1

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%

Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

Register bits $R_7 - R_0$ correspond to the data inputs $DQ_7 - DQ_0$ (Refer to Table 3). Register bits $R_7 - R_5$ store the command data. All register bits R_4 to R_0 must be zero. The only exceptions are: the reset command, when FFH is written to the register and Auto select, when 90H or 80H is written to the register.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 4 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Wait 6μs before reading the first accessed address location. All subsequent Read operations take t_{ACC}. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Command Register

Data Input/Output	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Command Register	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0
Data/Commands*	X	X	X	X	X	X	X	X

* Notes:

1. See Table 4 Am28F256 Command Definitions
2. X = Appropriate Data or Register Commands

Table 4. Am28F256 Command Definitions

Command	First Bus Cycle Operation (Note 1)	First Bus Cycle Address (Note 2)	First Bus Cycle Data (Note 3)	Second Bus Cycle Operation (Note 1)	Second Bus Cycle Address (Note 2)	Second Bus Cycle Data (Note 3)
Read Memory (Note 6)	Write	X	00H	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/A1H
Set-up Erase/Erase (Note 4)	Write	X	20H	Write	X	20H
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Set-up Program/Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Reset	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 1.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Flasherase Electrical Erase Algorithm.
5. Figure 2 illustrates the Flashrite Programming Algorithm.
6. Wait 6µs after first Read command before accessing the data. When the second bus command is a Read command, all subsequent Read operations take t_{ACC}.

Erase Sequence

Set-up Erase/Erase Commands

Set-up Erase

Set-up Erase is the first of a two-cycle erase command. It is a command-only operation that stages the device for bulk chip erase. The array contents are not altered with this command. 20H is written to the command register in order to perform the Set-up Erase operation.

Erase

The second two-cycle erase command initiates the bulk erase operation. You must write the Erase command (20H) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-verify) to the register.

This two step sequence of the Set-up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, chip erasure can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:
The Flash memory device must be fully programmed to 00H data prior to erasure. This equalizes the charge on all memory cells ensuring reliable erasure.

Erase-verify Command

The erase operation erases all bytes of the array in parallel. After the erase operation, all bytes must be sequentially verified. The Erase-verify operation is initiated by writing A0H to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-verify operation, the Am28F256 applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are properly erased.

Verify Next Address

You must write the Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$. The process continues for each byte in

the memory array until a byte does not return FFH data or all the bytes in the array are accessed and verified.

If an address is not verified to FFH data, the entire chip is erased again (refer to Set-up Erase/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The device is now ready to be programmed. At this point, the verification operation is terminated by writing a valid command (e.g. Program set-up) to the command register. Figure 1 and Table 5, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:
The erase-verify command must be written to the register in order to terminate the erase operation. During the erase operations, the local microprocessor must be dedicated to run software timing routines (erase in 10ms) as specified in AMD's Flasherase algorithm.

Should a system interrupt occur during an erase operation, always write the Erase-verify command prior to executing an interrupt sequence.

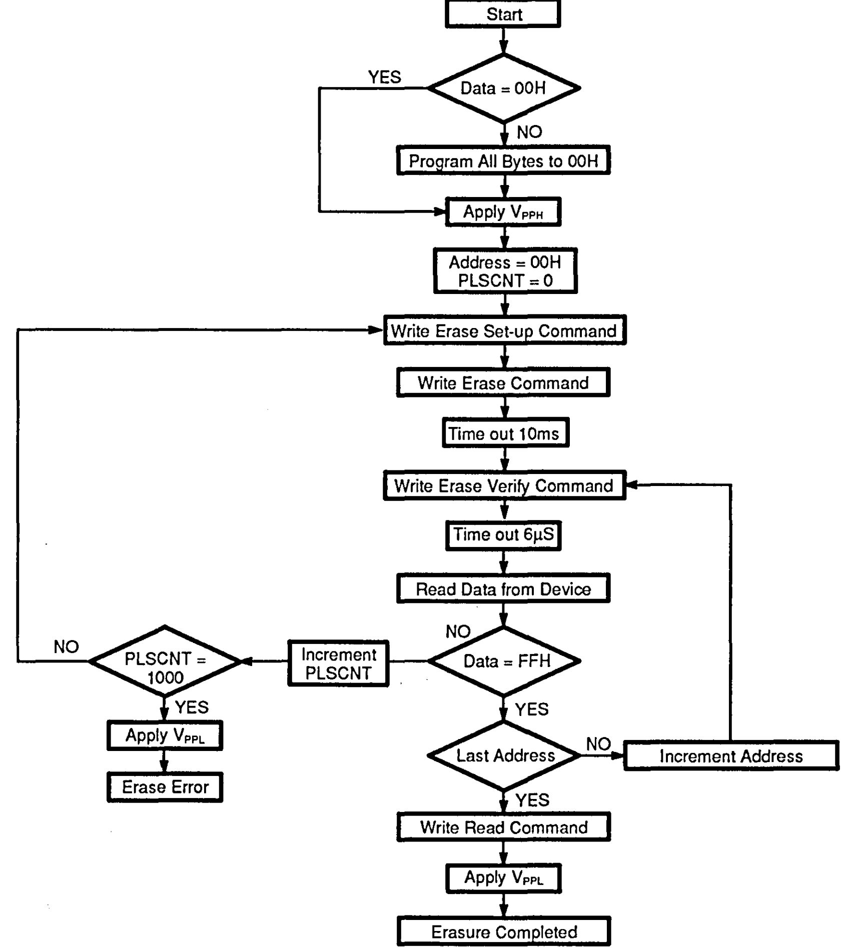


Figure 1. Flasherase Electrical Erase Algorithm

Flasherase Electrical Erase Algorithm

This Flash memory device erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the array. Erasure begins with a read of the memory contents. The Am28F256 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

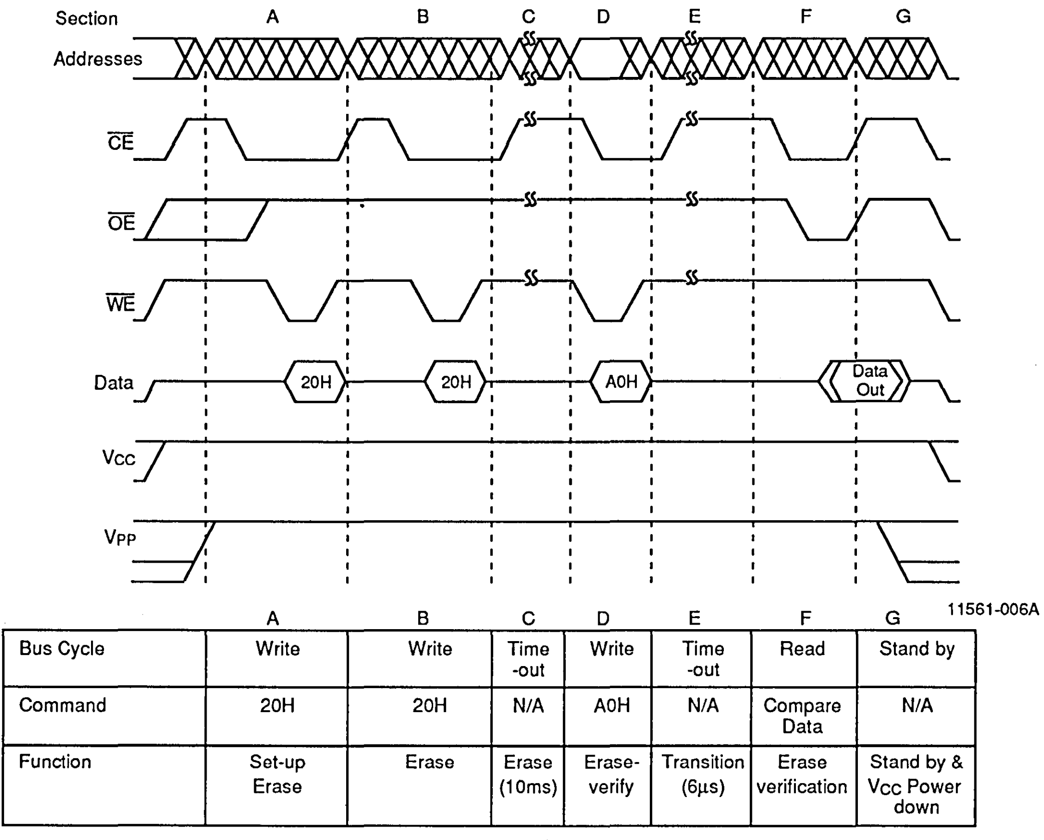
Should the device be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished using the Flashrite programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. If a byte fails to verify, the device is erased again. With each erase operation, an increasing number of bytes verify to the erased state. Typically, devices are erased in less than 100 pulses (1 second). Erase efficiency may be improved by storing the address of the last byte that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. A total of 1000 erase operations are allowed per reprogram cycle, which corresponds to approximately 10 seconds of cumulative erase time. Erasure typically occurs in one second. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 1 illustrates the electrical erase algorithm.

Table 5. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) **Note:** Use Flashrite programming algorithm (Figure 2) for programming.
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Set-Up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6µs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Read	Data = 00H, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0V.
2. Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.
3. The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	20H	20H	N/A	A0H	N/A	Compare Data	N/A
Function	Set-up Erase	Erase	Erase (10ms)	Erase-verify	Transition (6µs)	Erase verification	Stand by & V_{CC} Power down

Figure 2. A.C. Waveforms For Erase Operations

Analysis Of Erase Timing Waveform

Note:

This analysis does not include the requirement to program the entire array to 00H data prior to erasure. Refer to the Flasherase algorithm.

Set-up Erase/Erase

This analysis illustrates the use of two-cycle erase commands (section A&B). The first erase command (20H) is a set-up command and does not affect the array data (section A). The second erase command (20H) initiates the erase operation (section B) on the rising edge of this $\overline{WE}$ pulse. All bytes of the memory array are erased in parallel. No address information is required.

The erase pulse occurs in section C.

Time-out

A software timing routine (10ms duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Erase-verify

Upon completion of the erase software timing routine, the microprocessor must write the Erase-verify command (A0H). This command terminates the erase operation on the rising edge of the $\overline{WE}$ pulse (section D). The Erase-verify command also stages the device for data verification (section F).

After each erase operation each byte must be verified. The byte address to be verified must be supplied with the Erase-verify command (section D). Addresses are latched on the falling edge of the $\overline{WE}$ pulse.

Another software timing routine (6µs duration) must be executed to allow for generation of internal voltages for margin checking and read operation (section E).

During Erase-verification (section F) each address that returns FFH data is successfully erased. Each address of the array is sequentially verified in this manner by repeating sections D thru F until the entire array is verified or an address fails to verify. Should an address location fail to verify to FFH data, erase the device again. Repeat sections A thru F. Resume verification (section D) with the failed address.

Each data change sequence allows the device to use up to 1,000 erase pulses to completely erase. Typically 100 erase pulses are required.

Notes:
1. All address locations must be programmed to 00H prior to erase. This equalizes the charge on all memory cells and ensures reliable erasure.

2. The erase verify command must be written to terminate the erase operation. Should a system interrupt occur during an erase operation, always write the erase-verify command prior to executing an interrupt sequence.

Programming Sequence

Set-up Program/Program Command

Set-up Program

The Am28F256 is programmed byte by byte. Bytes may be programmed sequentially or at random. Set-up Program is the first of a two-cycle program command. It stages the device for byte programming. The Set-up Program operation is performed by writing 40H to the command register.

Program

Only after the program set-up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-verify command to terminate the programming operation. This two step sequence of the Set-up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte just programmed must be verified.

Write C0H into the command register in order to initiate the Program-verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-verify operation stages the device for verification of the last byte programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-verify operation, the Am28F256 applies an internally generated margin voltage to the addressed byte. A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte location. Should the byte fail to verify, reprogram (refer to Set-up Program/Program). Figure 3 and Table 6 indicate how instructions are combined with the bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Flashrite Programming Algorithm

The Am28F256 Flashrite programming algorithm employs an interactive closed loop flow to program data byte by byte. Bytes may be programmed sequentially or at random. The Flashrite programming algorithm uses 10 microsecond programming pulses. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 3 and Table 6 illustrate the programming algorithm.

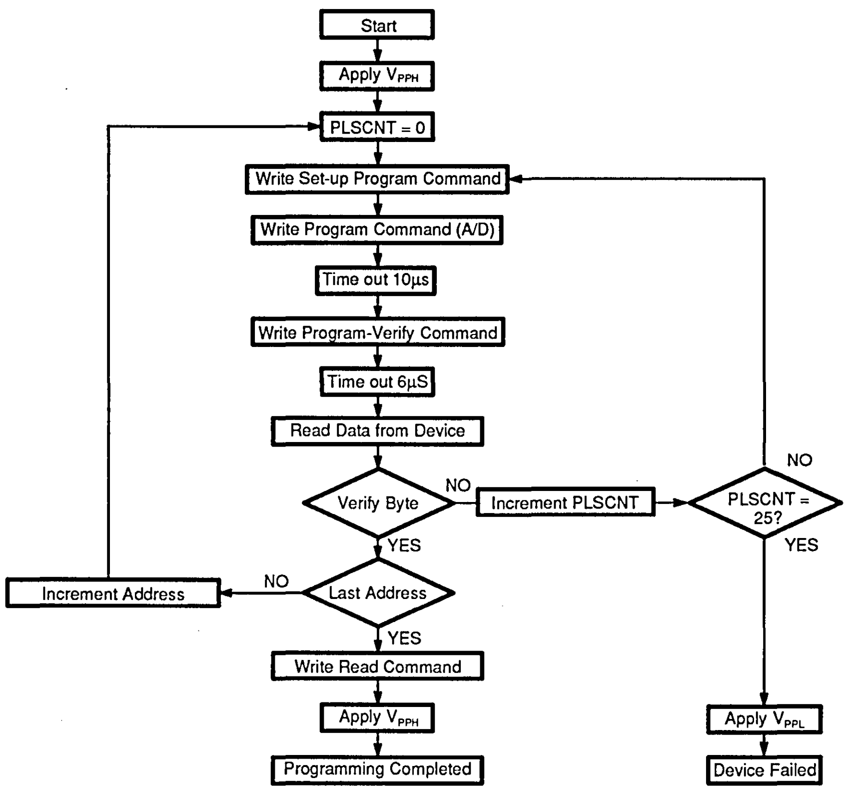


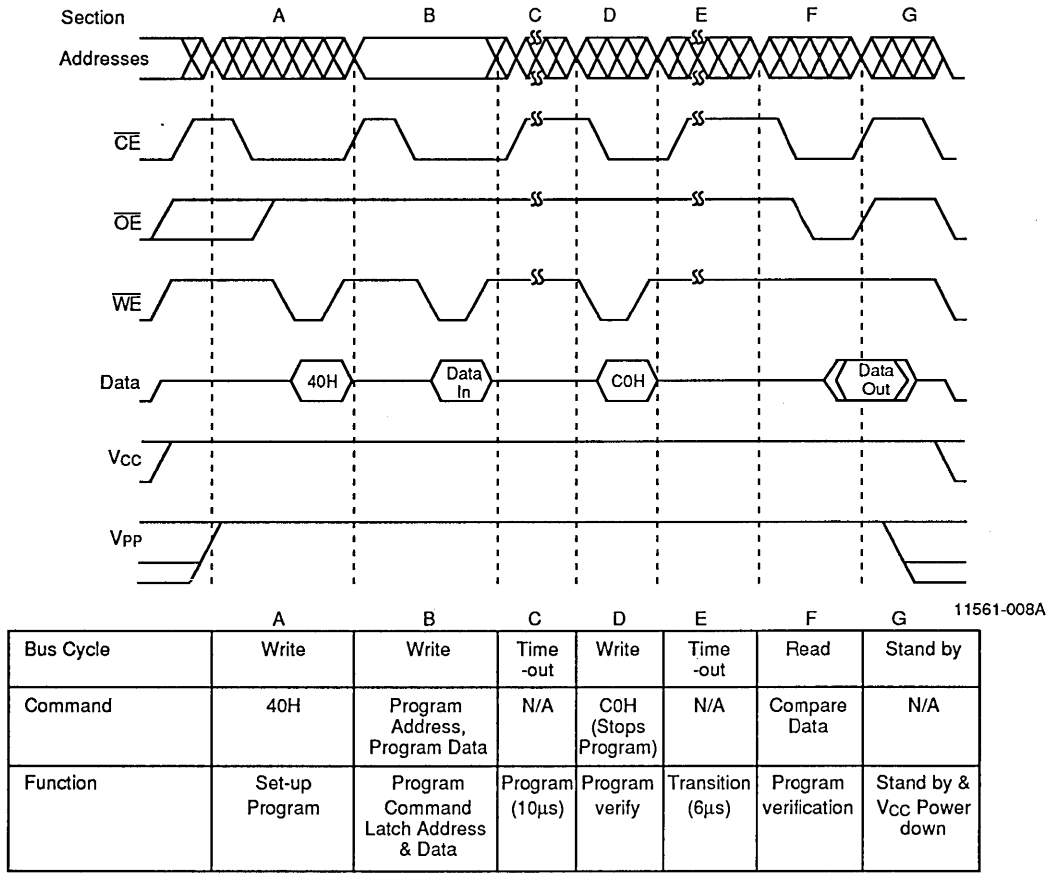
Figure 3. Flashrite Programming Algorithm

Table 6. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Set-Up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0V.
2. Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	40H	Program Address, Program Data	N/A	COH (Stops Program)	N/A	Compare Data	N/A
Function	Set-up Program	Program Command Latch Address & Data	Program (10μs)	Program verify	Transition (6μs)	Program verification	Stand by & V_{CC} Power down

Figure 4. A.C. Waveforms for Programming Operations

Analysis Of Program Timing Waveforms

Set-up Program/Program

Two-cycle write commands are required for program operations (section A&B). The first program command (40H) is a set-up command and does not affect the array data (section A). The second program command latches address and data required for programming on the falling and rising edge of $\overline{WE}$ respectively (section B). The rising edge of this $\overline{WE}$ pulse (section B) also initiates the programming pulse. The device is programmed on a byte by byte basis either sequentially or randomly.

The program pulse occurs in section C.

Time-out

A software timing routine (10μs duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Program-verify

Upon completion of the program timing routine, the microprocessor must write the program-verify command (C0H). This command terminates the programming operation on the rising edge of the $\overline{WE}$ pulse (section D). The program-verify command also stages the device for data verification (section F). Another software timing routine (6μs duration) must be executed to allow for generation of internal voltages for margin checking and read operations (section E).

During program-verification (section F) each byte just programmed is read to compare array data with original program data. When successfully verified, the next desired address is programmed. Should a byte fail to verify, reprogram the byte (repeat section A thru F). Each data change sequence allows the device to use up to 25 program pulses per byte. Typically, bytes are verified within one or two pulses.

Note:
The program-verify operation must be written to terminate the programming operation. Should a system interrupt occur during a programming operation, always write the program-verify command prior to executing an interrupt sequence.

Algorithm Timing Delays

There are four different timing delays associated with the Flasherase and Flashrite algorithms:

1. The first delay is associated with the V_{PP} rise-time when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on the V_{PP}, the delay required is proportional to the number of devices being erased and the 0.1µF/device. V_{PP} must reach its final value 100ns before commands are executed.
2. The second delay time is the erase time pulse width (10 ms). A software timing routine should be run by the local microprocessor to time out the delay. The erase operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the erase operation. To ensure proper device operation, write the Erase-verify operation after each pulse, or the device may continue to erase until the memory cells are driven into depletion (over-erasure). Should this happen the internal circuitry will no longer select unique addresses. A symptom of over-erasure is an error attempting to program the next time. Occasionally it is possible to recover over-erased devices by programming all of the locations with 00H data.
3. A third delay time is required for each programming pulse width (10 µs). The programming algorithm is interactive and verifies each byte after a program pulse. The program operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the programming operation.
4. A fourth timing delay associated with both the Flasherase and Flashrite algorithms is the write recovery time (6 µs). During this time internal circuitry is changing voltage levels from the erase/ program level to those used for margin verify and read operations. An attempt to read the device during this period will result in possible false data (it may appear the device is not properly erased or programmed).

Note:
Software timing routines should be written in machine language for each of the delays. Code written in machine language requires knowledge of the appropriate microprocessor clock speed in order to accurately time each delay.

Parallel Device Erasure

Many applications will use more than one Flash memory device. Total erase time may be minimized by implementing a parallel erase algorithm. Flash memories may erase at different rates. Therefore each device must be verified seperately. When a device is completely erased and verified use a masking code to prevent further erasure. The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-up Sequence

V_{CC} prior to V_{PP}

The Am28F256 powers-up in the Read only mode. In addition, the memory contents may only be altered after successful completion of a two step command sequence.

V_{PP} prior to V_{CC}

When V_{CC} = 0 V, the V_{PP} voltage is internally disabled from the device. Memory contents cannot be altered. With V_{PP} = 12 V, the Flash device resets to the Read mode when V_{CC} rises above 2 V.

Power supply sequencing is not required.

Reset Command

A reset command sequence is provided to initialize the Flash memory to a known state – Read mode. The Reset command sequence also provides the user with a means to safely abort the erase or program command sequences. Following either set-up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

If V_{PP} is left at high voltage during system resets, you must incorporate the device reset command into the hardware initialization code. This minimizes the potential for over erasure or programming if the device is in the middle of an erase or program operation during reset. Execute the reset command early in the initialization routine.

Auto Select Command

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Programming In-system

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F256 contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H. A read cycle from address 0001H returns the device code A1H (See Table 2). To terminate the operation, it is necessary to write another valid command into the register (See Table 3).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	
Ceramic Packages	– 65°C to +150°C
Plastic Packages	– 65°C to +125°C
Ambient Temperature with Power Applied	– 55°C to + 125°C
Voltage with Respect To Ground	
All pins except A_9 and V_{PP} (Note 1)	– 2.0V to 7.0V
V_{CC} (Note 1)	– 2.0V to 7.0V
A_9 (Note 2)	– 2.0V to 14.0V
V_{PP} (Note 2)	– 2.0V to 14.0V
Output Short Circuit Current (Note 3)	200mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*

2. *Minimum DC input voltage on A_9 and V_{PP} pins is –0.5V. During voltage transitions, A_9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*

3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

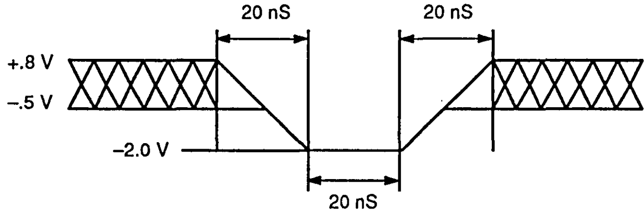
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (T_C)	0°C to +70°C
Industrial (I) Devices	
Case Temperature (T_C)	– 40°C to +85°C
Extended (E) Devices	
Case Temperature (T_C)	– 55°C to +125°C
Military (M) Devices	
Case Temperature (T_C)	– 55°C to +125°C
V_{CC} Supply Voltages	
V_{CC} for Am28F256–X5	+ 4.75V to +5.25V
V_{CC} for Am28F256–XX0	+ 4.50V to +5.50V
V_{PP} Supply Voltages	
Read	– 0.5V to +12.6V
Program, Erase, and Verify	+ 11.4V to +12.6V

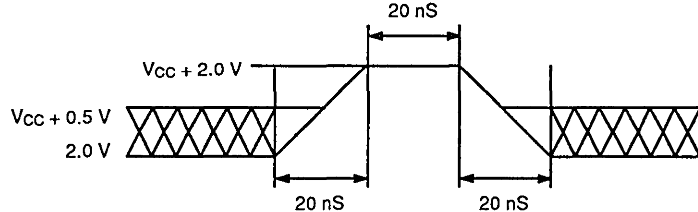
MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



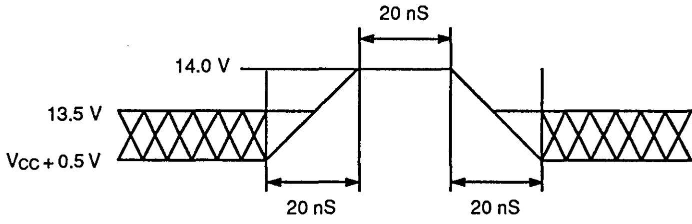
Maximum Negative Overshoot Waveform

Maximum Positive Input Overshoot



Maximum Positive Overshoot Waveform

Maximum V_{PP} Overshoot



Maximum V_{PP} Overshoot Waveform

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted). (Notes 1–3)

DC CHARACTERISTICS-TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		± 1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		± 1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{IH}		1.0	mA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}		± 1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		200	µA
		V_{PP} = V_{PPL}		± 1.0	
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		30	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA V_{CC} = V_{CC} Min.		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA V_{CC} = V_{CC} Min.	2.4		V
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5	13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/Program are inhibited when V_{PP} = V_{PPL}	0.0	V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4	12.6	V

PRELIMINARY

DC CHARACTERISTICS-CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{IN} = V_{CC}$ or V_{SS}		±1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{OUT} = V_{CC}$ or V_{SS}		±1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max. $\overline{CE} = V_{IH}$		100	µA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ I_{OUT} = 0 mA, at 6 MHz		30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress		30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress		30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$		±1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		200	µA
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress		30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress		30	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		V_{CC} – 0.5	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA $V_{CC} = V_{CC}$ Min.		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min.	0.85 V_{CC}		V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC}$ Min.	V_{CC} –0.4		
V_{ID}	A_9 Auto Select Voltage	$A_9 = V_{ID}$	11.5	13.0	V
I_{ID}	A_9 Auto Select Current	$A_9 = V_{ID}$ Max. $V_{CC} = V_{CC}$ Max.		50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/ Program are inhibited when $V_{PP} = V_{PPL}$	0.0	V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4	12.6	V

Notes:

1. **Caution:** the Am28F256 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

PRELIMINARY

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	8	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions $T_A = 25°C$, f = 1.0 MHz

SWITCHING CHARACTERISTICS over operating range unless otherwise specified.

AC CHARACTERISTICS-Read Only Operation (Notes 1– 2)

Parameter Symbols				Am28F256					
JEDEC	Standard	Parameter Description		— -75	-90 -95	-120 —	-150 —	-200 —	Unit
t_{AVAV}	t_{RC}	Read Cycle Time	Min.	70	90	120	150	200	ns
			Max.						
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min.						
			Max.	70	90	120	150	200	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min.						
			Max.	70	90	120	150	200	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min.						
			Max.	35	40	50	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z	Min.	0	0	0	0	0	ns
			Max.						
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z	Min.						
			Max.	25	25	30	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	Min.	0	0	0	0	0	ns
			Max.						
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z	Min.						
			Max.	25	25	30	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change	Min.	0	0	0	0	0	ns
			Max.						
t_{WHGL}		Write Recovery Time before Read	Min.	6	6	6	6	6	µs
			Max.						

Notes:

1. Output Load (except Am28F256-75): 1 TTL gate and C_L = 100 pF, Input Rise and Fall Times: $\leq$ 10 ns, Input Pulse levels: 0.45 to 2.4 V, Timing Measurement Reference Level - Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. The Am28F256-75 Output Load: 1 TTL gate and C_L = 30 pF
   Input Rise and Fall Times: $\leq$ 10 ns
   Input Pulse levels: 0 to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.

AC CHARACTERISTICS-Write/Erase/Program Operations (Notes 1– 4)

Parameter Symbols		Parameter Description		Am28F256					Unit
JEDEC	Standard			— –75	–90 –95	–120 —	–150 —	–200 —	
t_{AVAV}	t_{WC}	Write Cycle Time	Min. Max.	70	90	120	150	200	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min. Max.	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min. Max.	40	45	50	60	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min. Max.	40	45	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min. Max.	10	10	10	10	10	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	Min. Max.	6	6	6	6	6	µs
t_{GHWL}		Read Recovery Time before Write	Min. Max.	0	0	0	0	0	µs
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	Min. Max.	0	0	0	0	0	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min. Max.	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min. Max.	40	45	50	50	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min. Max.	20	20	20	20	20	ns
t_{WHWH1}		Duration of Programming Operation	Min. Max.	10 25	10 25	10 25	10 25	10 25	µs
t_{WHWH2}		Duration of Erase Operation	Min. Max.	9.5 10.5	9.5 10.5	9.5 10.5	9.5 10.5	9.5 10.5	ms
t_{EHVP}		Chip Enable Set-Up Time to V_{PP} Ramp	Min. Max.	100	100	100	100	100	ns
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW	Min. Max.	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time	Min. Max.	2	2	2	2	2	µs
t_{VPPR}		V_{PP} Rise Time	Min. Max.	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time	Min. Max.	500	500	500	500	500	ns

Notes:

1. Read timing characteristics during read/write operations are the same as durng read-only operations. Refer to AC Characteristics for Read Only operations.
2. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the Write Pulse Width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.
3. All devices except Am28F256-75. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V
4. Am28F256-75. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V
   Timing Measurement Reference Level: Inputs and Outputs: 1.5 V

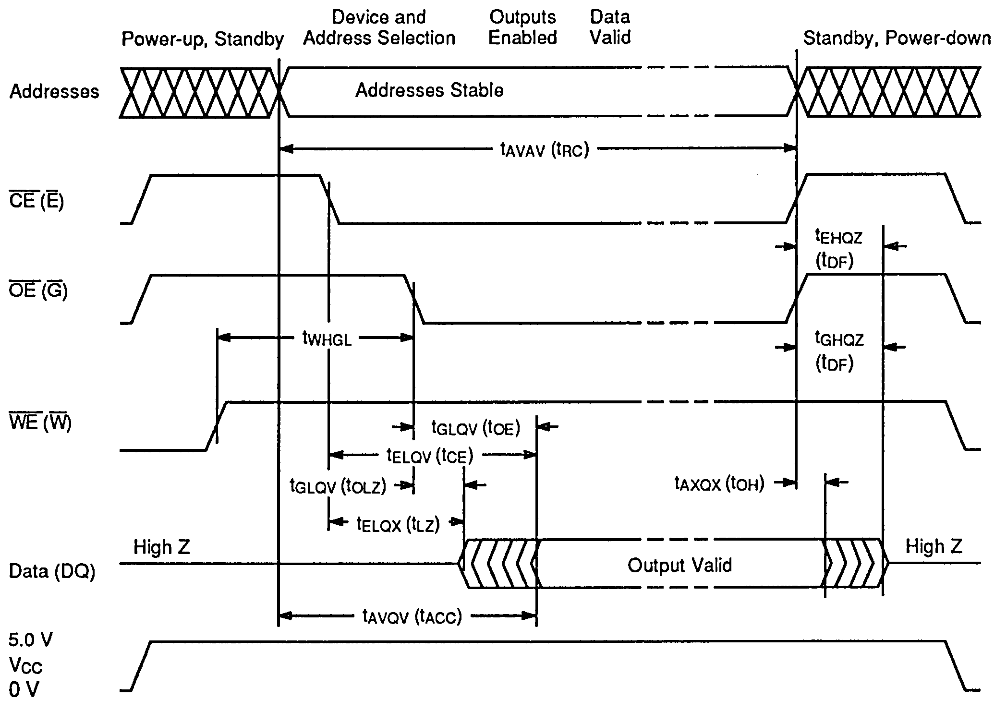


Figure 5. AC Waveforms for Read Operations

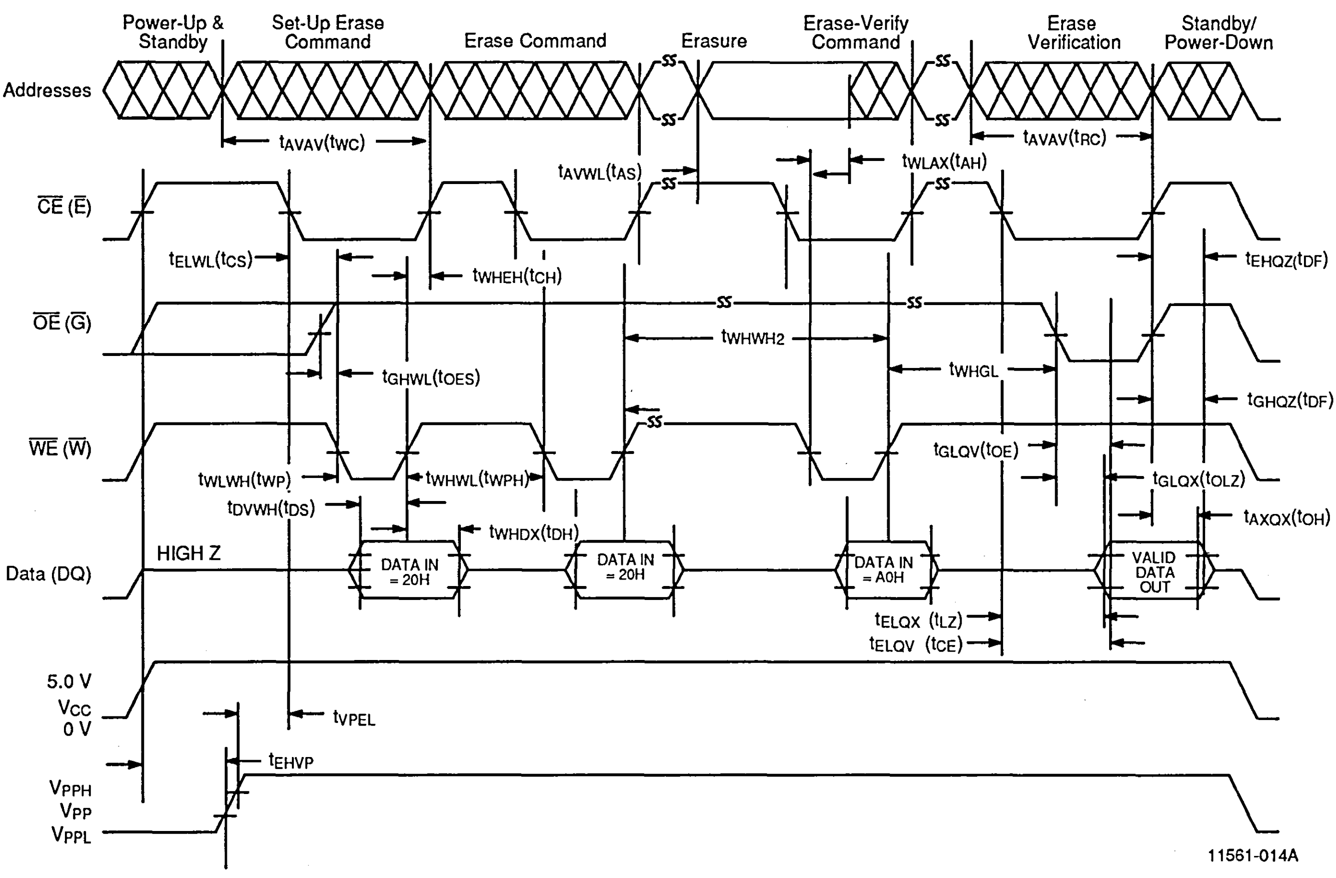


Figure 6. A.C. Waveforms for Erase Operations

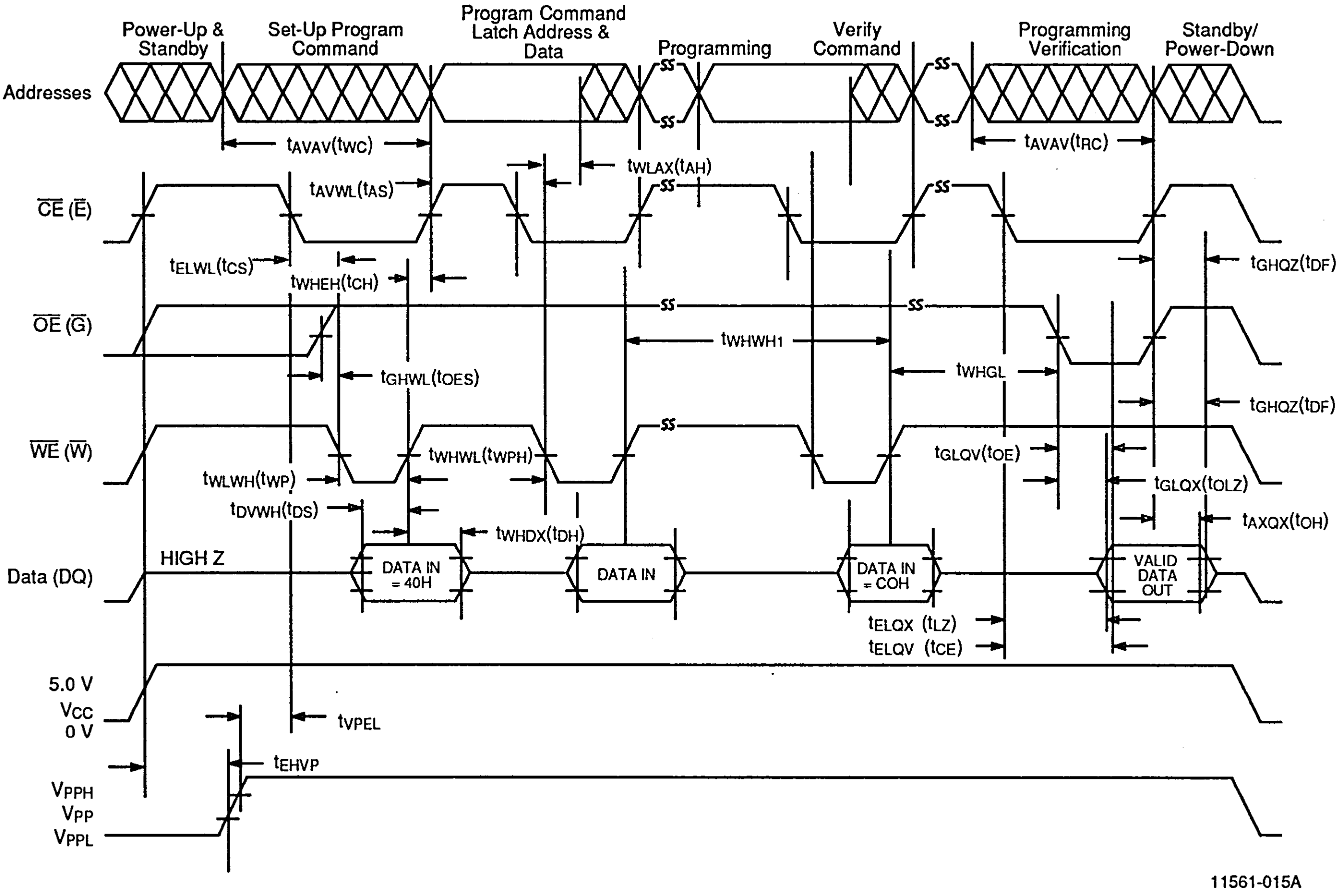
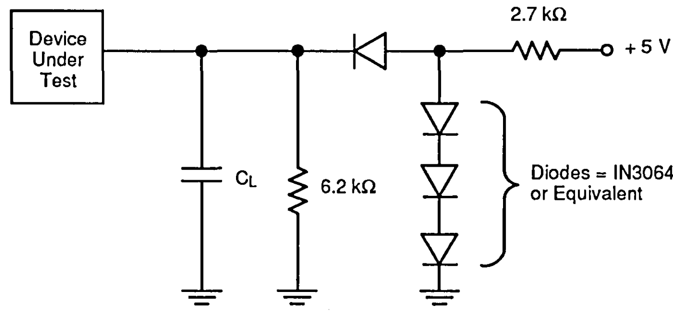


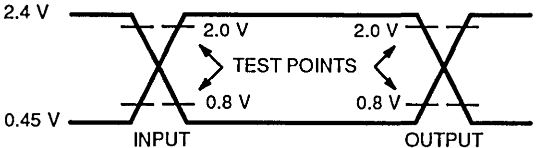
Figure 7. A.C. Waveforms for Programming Operations

SWITCHING TEST CIRCUIT



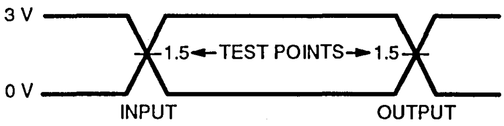
C_L = 100 pF including jig capacitance (30 pF for Am28F256-75)

SWITCHING TEST WAVEFORMS



All Devices Except Am28F256-75

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.



For Am28F256-75

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.

08007-003A

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Chip Erase Time		0.5 (Note 1)	10	S	Excludes 00H programming prior to erasure
Chip Programming Time		0.5 (Note 1)	6	S	Excludes system-level overhead
Erase/Program Cycles					
Am28F256-75C4JC	10,000			Cycles	
Am28F256-75C3JC	1,000			Cycles	

Note:

1. 25°C, 12V V_{PP}

LATCHUP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A_9 and V_{PP})	– 1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	– 1.0 V	V_{CC} + 1.0 V
Current	– 100 mA	+ 100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

Preliminary

Am28F512

65,536 x 8-Bit CMOS Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 70 ns maximum access time
- **Low power consumption**
  - 30 mA maximum active current
  - 100 µA maximum standby current
- **Compatible with JEDEC-standard byte-wide 32-Pin E²PROM pinouts**
  - 32-pin DIP
  - 32-pin PLCC
- **10,000 erase/program cycles**
- **Program and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to V_{CC} +1 V**
- **Flasherase™ Electrical Bulk Chip-Erase**
  - One second typical chip-erase
- **Flashrite™ programming**
  - 10 µs typical byte-program
  - Less than 1 second typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell

GENERAL DESCRIPTION

The Am28F512 is a 512K "Flash" electrically erasable, electrically programmable read only memory organized as 64K bytes of 8 bits each. The Am28F512 is packaged in 32-pin PDIP and PLCC versions which allow for upgrades to the 2 Megabit density. The device is also offered in ceramic DIP and LCC packages. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers.

The standard Am28F512 offers access times as fast as 70 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F512 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F512 uses a command register to manage this functionality, while maintaining a standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

AMD's Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F512 uses a 12.0 V ± 5% V_{PP} supply to perform the Flasherase and Flashrite algorithms.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from –1 V to V_{CC}+1 V.

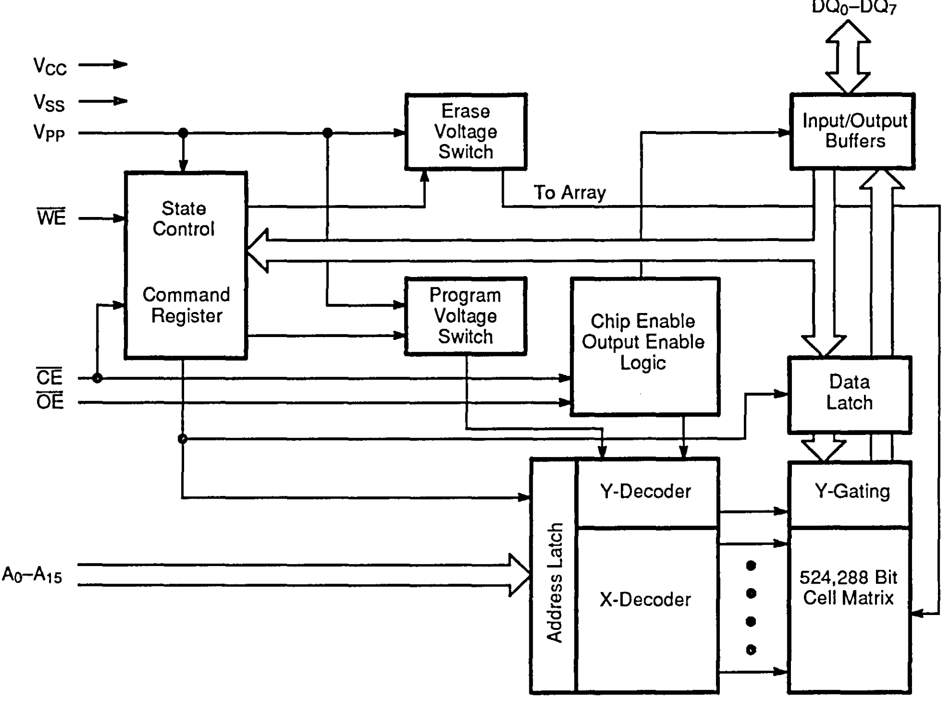
The Am28F512 is byte programmable using 10 µs programming pulses in accordance with AMD's Flashrite programming algorithm. The typical room temperature programming time of the Am28F512 is less than one second. The entire chip is bulk erased using 10ms erase pulses according to AMD's Flasherase algorithm. Typical erasure at room temperature is accomplished in less than one second. The windowed package and the 15–20 minutes required for EPROM erasure using ultraviolet light are eliminated.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F512 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

AMD's Flash technology combines years of EPROM and E²PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F512 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

Publication# 11561 Rev. B Amendment/0
Issue Date: June 1990

BLOCK DIAGRAM



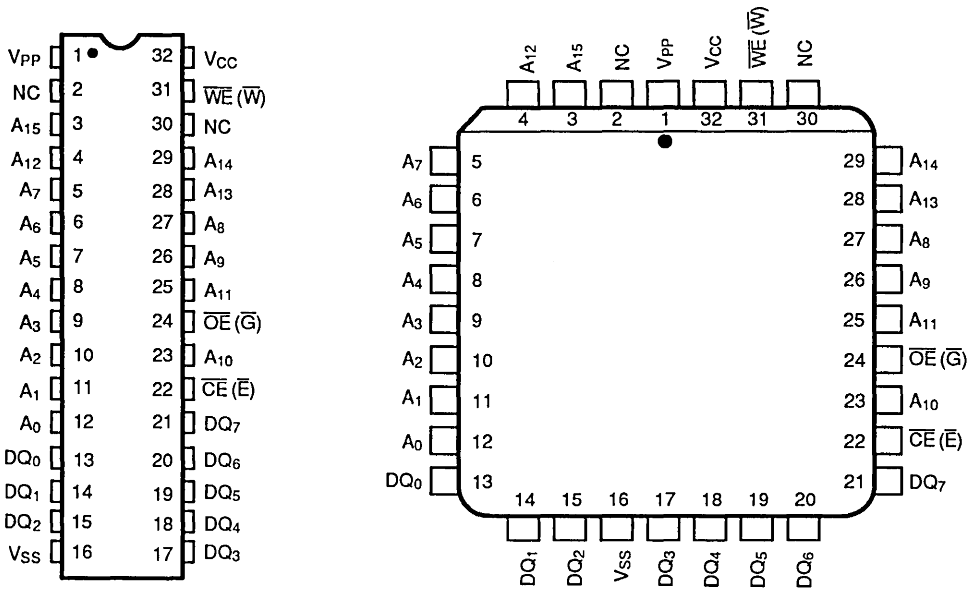
11561-001B

PRODUCT SELECTOR GUIDE

Family Part No.	Am28F512				
Ordering part No: ± 10% V_{CC} Tolerance	—	–90	–120	–150	–200
± 5% V_{CC} Tolerance	–75	–95	—	—	—
Max Access Time (ns)	70	90	120	150	200
$\overline{CE}$ ($\overline{E}$) Access (ns)	70	90	120	150	200
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	40	50	65	75

CONNECTION DIAGRAMS

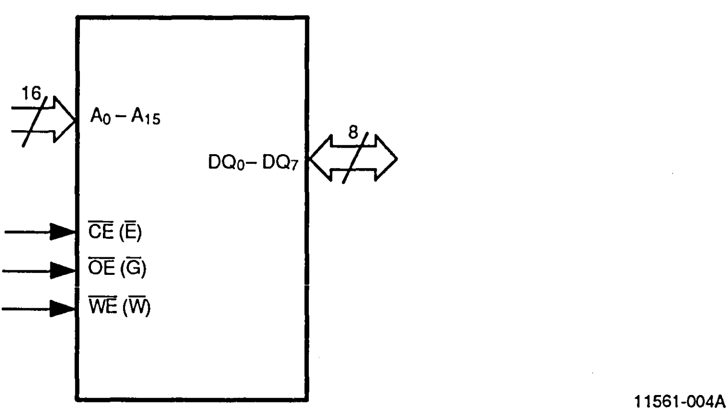
DIP | **LCC/PLCC**



11561-002B | 11561-003B

Note: Pin 1 is marked for orientation

LOGIC SYMBOL



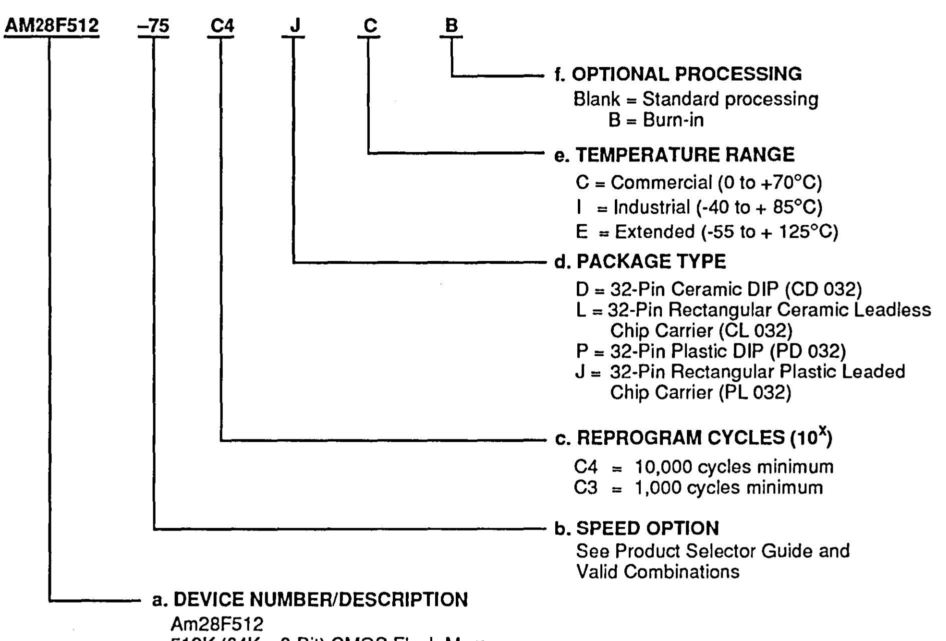
PIN DESCRIPTION

Symbol	Functional Description
$A_0 - A_{15}$	Address Inputs for memory locations. Internal latches hold addresses during write cycles.
$DQ_0 - DQ_7$	Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.
$\overline{CE}$ ($\overline{E}$)	The Chip Enable active low input activates the chip'scontrol logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.
$\overline{OE}$ ($\overline{G}$)	The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.
$\overline{WE}$ ($\overline{W}$)	The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.
V_{PP}	Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2V$.
V_{CC}	Power supply for device operation. (5.0V ± 5% or 10%)
V_{SS}	Ground
NC	No Connect-corresponding pin is not connected internally to the die.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Reprogram Cycles
d. Package Type
e. Temperature Range
f. Optional Processing



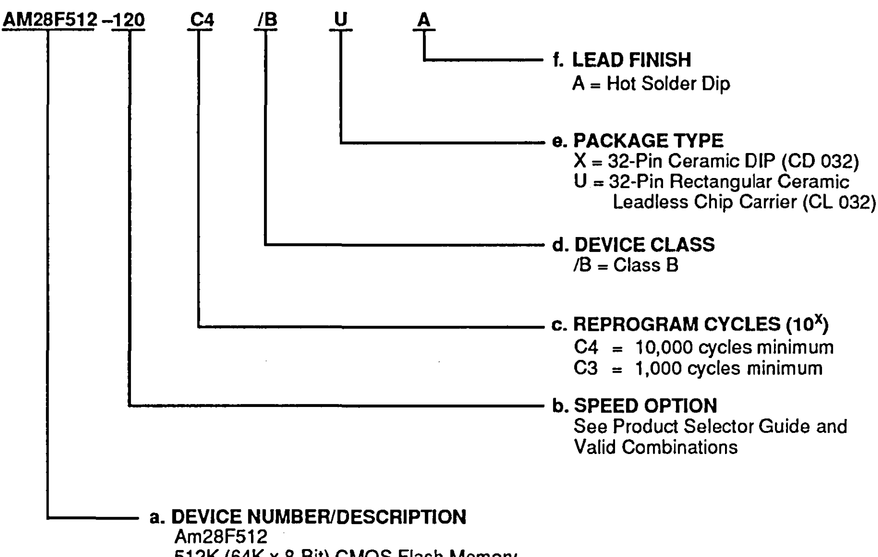
Valid Combinations	
AM28F512-75	C4DC, C4DCB, C4DI, C4DIB, C4LC, C4LCB, C4LI, C4LIB, C4PC, C4PI, C4JC, C4JI, C3DC, C3DCB, C3DI, C3DIB,C3LC, C3LCB, C3LI, C3LIB, C3PC, C3PI,, C3JC, C3JI
AM28F512-95 AM28F512-90 AM28F512-120 AM28F512-150 AM28F512-200	C4DC, C4DCB, C4DI, C4DIB, C4DE, C4DEB, C4LC, C4LCB, C4LI, C4LIB, C4LE, C4LEB, C4PC, C4PI, C4JC, C4JI, C3DC, C3DCB, C3DI, C3DIB, C3DE, C3DEB, C3LC, C3LCB, C3LI, C3LIB, C3LE, C3LEB, C3PC, C3PI, C3JC, C3JI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:
a. Device Number
b. Speed Option
c. Reprogram cycles
d. Device Class
e. Package Type
f. Lead Finish



Valid Combinations	
AM28F512-120 AM28F512-150 AM28F512-200	C4/BXA, C4/BUA C3/BXA, C3/BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

BASIC PRINCIPLES

The Am28F512 uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F512 functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F512's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F512 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Erase Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note:
The Flash memory array must be completely programmed prior to erasure. Refer to the Flasherase Algorithm.

1. **Set-up Erase:** Write the Set-up Erase command to the command register.
2. **Erase:** Write the Erase command (same as Set-up Erase command) to the command register again.

   The second command initiates the erase operation. The system software routines must now time-out the erase pulse width (10 ms) prior to issuing the Erase-verify command.
3. **Erase-verify:** Write the Erase-verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFH data (Byte erased). After successful data verification the Erase-verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Programming Sequence

A three step command sequence (a two-cycle Program command and one cycle Verify command) is required to program a byte of the Flash array. Refer to the Flashrite Algorithm.

1. **Set-up Program:** Write the Set-up Program command to the command register.
2. **Program:** Write the Program command to the command register with the appropriate Address and Data. The system software routines must now time-out the program pulse width (10 µs) prior to issuing the Program-verify command.
3. **Program-verify:** Write the Program-verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times.

FUNCTIONAL DESCRIPTION

Description Of User Modes

Table 1. Am28F512 User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A_0	A_9	I/O
Read-Only	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	A_0	A_9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (25H)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A_0	A_9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A_0	A_9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2V$, See DC Characteristics for voltage levels of V_{PPH}, $0V < An < V_{CC} + 2V$, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC}$ +2.0V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.
3. $11.5 \leq V_{ID} \leq 13.0V$
4. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.
5. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid D_{IN} during a write operation.
7. All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A_9 and A_0 must be held at V_{IL}.

READ ONLY MODE

$V_{PP} < V_{CC} + 2V$

Command Register Inactive

Read

The Am28F512 functions as a read only memory when $V_{PP} < V_{CC} + 2V$. The Am28F512 has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC} - t_{OE}$).

Standby Mode

The Am28F512 has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5V$), consumes less than 100µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A Prom Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5V to 13.0V) on address A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to V_{CC} + 2.0V while using this Auto select mode. Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am28F512 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ_7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F512 Auto Select Code

Type	A_0	Code (HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	25	0	0	1	0	0	1	0	1

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%

Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

Register bits $R_7 - R_0$ correspond to the data inputs $DQ_7 - DQ_0$ (Refer to Table 3). Register bits $R_7 - R_5$ store the command data. All register bits R_4 to R_0 must be zero. The only exceptions are: the reset command, when FFH is written to the register and Auto select, when 90H or 80H is written to the register.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 4 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Wait 6µs before reading the first accessed address location. All subsequent Read operations take t_{ACC}. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Command Register

Data Input/Output	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Command Register	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0
Data/Commands*	X	X	X	X	X	X	X	X

*** Notes:**

1. See Table 4 Am28F512 Command Definitions
2. X = Appropriate Data or Register Commands

Table 4. Am28F512 Command Definitions

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 6)	Write	X	00H	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/25H
Set-up Erase/Erase (Note 4)	Write	X	20H	Write	X	20H
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Set-up Program/Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Reset	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 1.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Flasherase Electrical Erase Algorithm.
5. Figure 2 illustrates the Flashrite Programming Algorithm.
6. Wait 6µs after first Read command before accessing the data. When the second bus command is a Read command, all subsequent Read operations take t_{ACC}.

Erase Sequence

Set-up Erase/Erase Commands

Set-up Erase

Set-up Erase is the first of a two-cycle erase command. It is a command-only operation that stages the device for bulk chip erase. The array contents are not altered with this command. 20H is written to the command register in order to perform the Set-up Erase operation.

Erase

The second two-cycle erase command initiates the bulk erase operation. You must write the Erase command (20H) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-verify) to the register.

This two step sequence of the Set-up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, chip erasure can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:
The Flash memory device must be fully programmed to 00H data prior to erasure. This equalizes the charge on all memory cells ensuring reliable erasure.

Erase-verify Command

The erase operation erases all bytes of the array in parallel. After the erase operation, all bytes must be sequentially verified. The Erase-verify operation is initiated by writing A0H to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-verify operation, the Am28F512 applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are properly erased.

Verify Next Address

You must write the Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$. The process continues for each byte in

the memory array until a byte does not return FFH data or all the bytes in the array are accessed and verified.

If an address is not verified to FFH data, the entire chip is erased again (refer to Set-up Erase/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The device is now ready to be programmed. At this point, the verification operation is terminated by writing a valid command (e.g. Program set-up) to the command register. Figure 1 and Table 5, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:
The erase-verify command must be written to the register in order to terminate the erase operation. During the erase operations, the local microprocessor must be dedicated to run software timing routines (erase in 10ms) as specified in AMD's Flasherase algorithm.

Should a system interrupt occur during an erase operation, always write the Erase-verify command prior to executing an interrupt sequence.

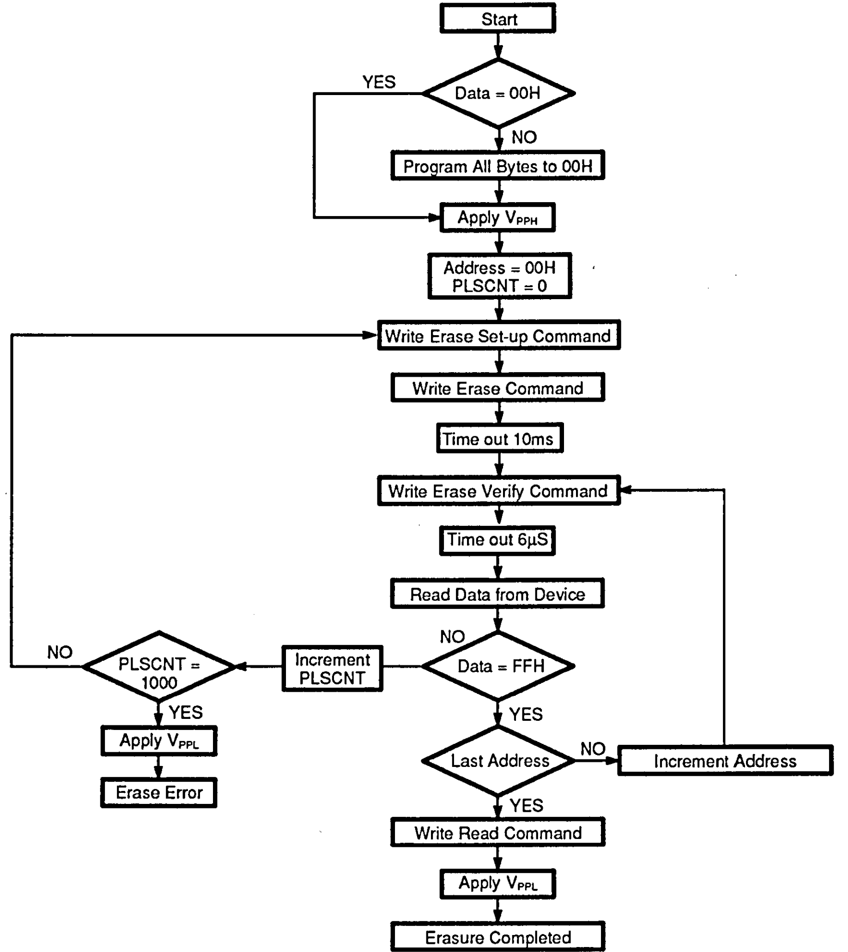


Figure 1. Flasherase Electrical Erase Algorithm

Flasherase Electrical Erase Algorithm

This Flash memory device erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the array. Erasure begins with a read of the memory contents. The Am28F512 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

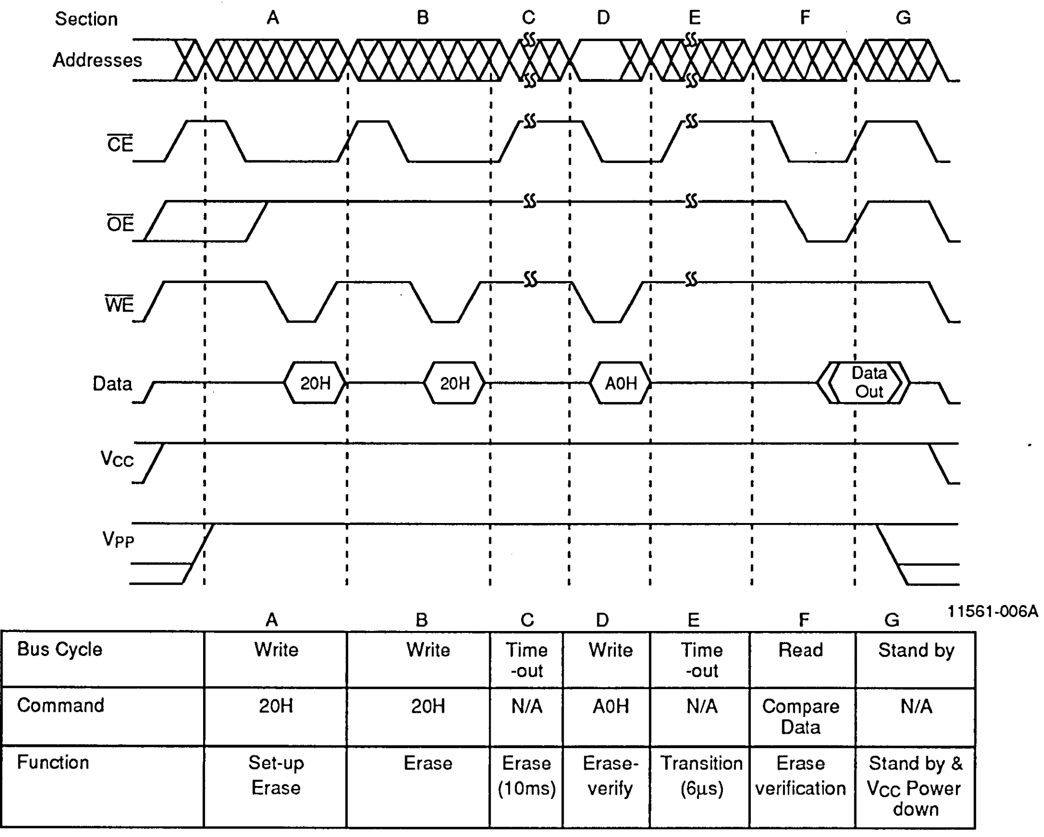
Should the device be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished using the Flashrite programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. If a byte fails to verify, the device is erased again. With each erase operation, an increasing number of bytes verify to the erased state. Typically, devices are erased in less than 100 pulses (1 second). Erase efficiency may be improved by storing the address of the last byte that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. A total of 1000 erase operations are allowed per reprogram cycle, which corresponds to approximately 10 seconds of cumulative erase time. Erasure typically occurs in one second. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 1 illustrates the electrical erase algorithm.

Table 5. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) **Note:** Use Flashrite programming algorithm (Figure 2) for programming.
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Set-Up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6µs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Read	Data = 00H, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0V.
2. Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.
3. The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	20H	20H	N/A	A0H	N/A	Compare Data	N/A
Function	Set-up Erase	Erase	Erase (10ms)	Erase-verify	Transition (6µs)	Erase verification	Stand by & V_{CC} Power down

Figure 2. A.C. Waveforms For Erase Operations

Analysis Of Erase Timing Waveform

Note:

This analysis does not include the requirement to program the entire array to 00H data prior to erasure. Refer to the Flasherase algorithm.

Set-up Erase/Erase

This analysis illustrates the use of two-cycle erase commands (section A&B). The first erase command (20H) is a set-up command and does not affect the array data (section A). The second erase command (20H) initiates the erase operation (section B) on the rising edge of this $\overline{WE}$ pulse. All bytes of the memory array are erased in parallel. No address information is required.

The erase pulse occurs in section C.

Time-out

A software timing routine (10ms duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Erase-verify

Upon completion of the erase software timing routine, the microprocessor must write the Erase-verify command (A0H). This command terminates the erase operation on the rising edge of the $\overline{WE}$ pulse (section D). The Erase-verify command also stages the device for data verification (section F).

After each erase operation each byte must be verified. The byte address to be verified must be supplied with the Erase-verify command (section D). Addresses are latched on the falling edge of the $\overline{WE}$ pulse.

Another software timing routine (6µs duration) must be executed to allow for generation of internal voltages for margin checking and read operation (section E).

During Erase-verification (section F) each address that returns FFH data is successfully erased. Each address of the array is sequentially verified in this manner by repeating sections D thru F until the entire array is verified or an address fails to verify. Should an address location fail to verify to FFH data, erase the device again. Repeat sections A thru F. Resume verification (section D) with the failed address.

Each data change sequence allows the device to use up to 1,000 erase pulses to completely erase. Typically 100 erase pulses are required.

Notes:

1. All address locations must be programmed to 00H prior to erase. This equalizes the charge on all memory cells and ensures reliable erasure.

2. The erase verify command must be written to terminate the erase operation. Should a system interrupt occur during an erase operation, always write the erase-verify command prior to executing an interrupt sequence.

Programming Sequence

Set-up Program/Program Command

Set-up Program

The Am28F512 is programmed byte by byte. Bytes may be programmed sequentially or at random. Set-up Program is the first of a two-cycle program command. It stages the device for byte programming. The Set-up Program operation is performed by writing 40H to the command register.

Program

Only after the program set-up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-verify command to terminate the programming operation. This two step sequence of the Set-up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte just programmed must be verified.

Write C0H into the command register in order to initiate the Program-verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-verify operation stages the device for verification of the last byte programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-verify operation, the Am28F512 applies an internally generated margin voltage to the addressed byte. A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte location. Should the byte fail to verify, reprogram (refer to Set-up Program/Program). Figure 3 and Table 6 indicate how instructions are combined with the bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Flashrite Programming Algorithm

The Am28F512 Flashrite programming algorithm employs an interactive closed loop flow to program data byte by byte. Bytes may be programmed sequentially or at random. The Flashrite programming algorithm uses 10 microsecond programming pulses. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 3 and Table 6 illustrate the programming algorithm.

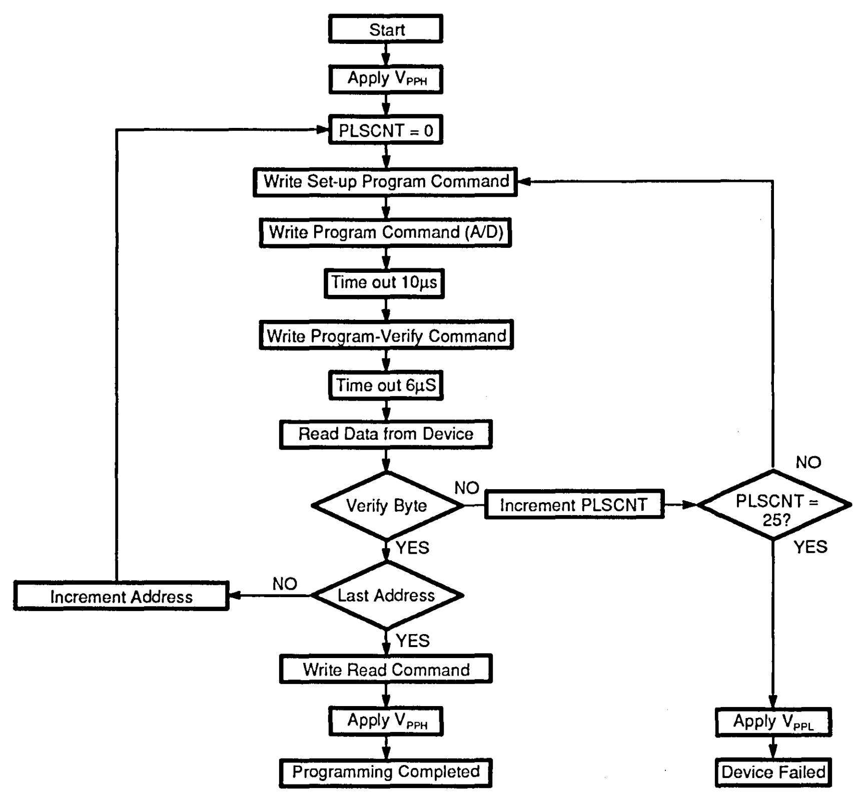


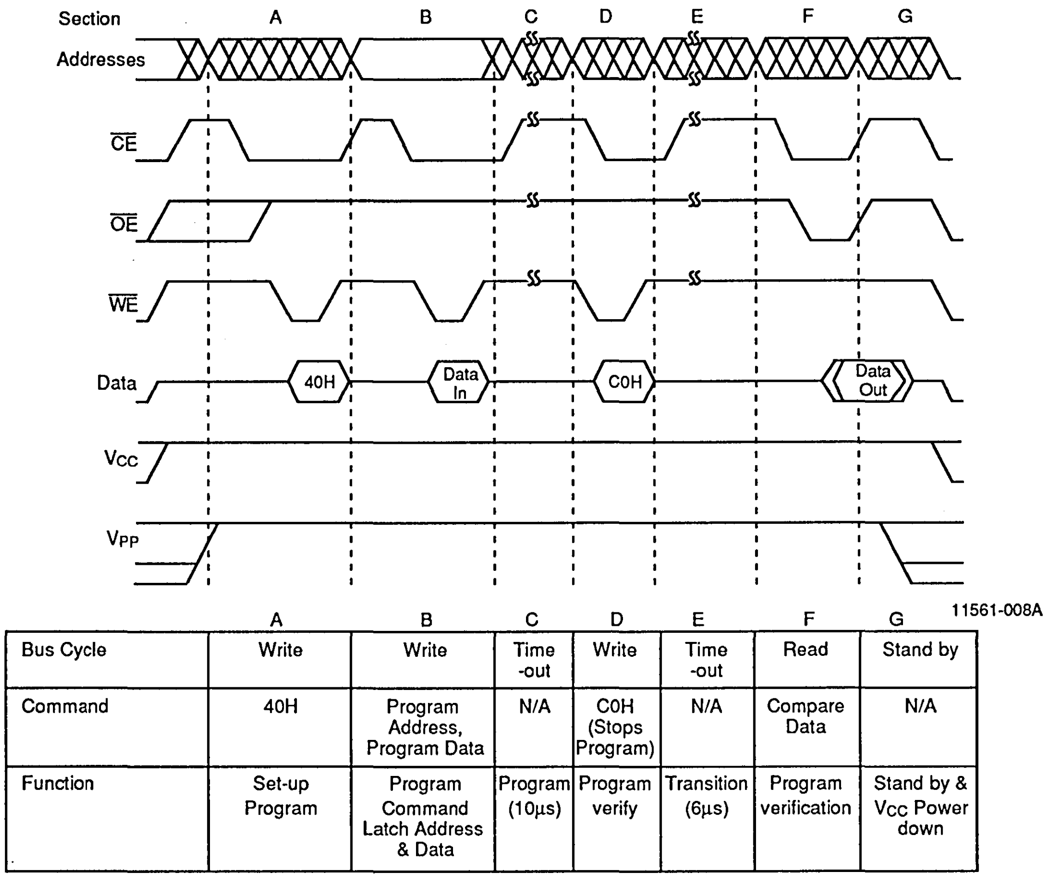
Figure 3. Flashrite Programming Algorithm

Table 6. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Set-Up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0V.
2. Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	40H	Program Address, Program Data	N/A	C0H (Stops Program)	N/A	Compare Data	N/A
Function	Set-up Program	Program Command Latch Address & Data	Program (10µs)	Program verify	Transition (6µs)	Program verification	Stand by & V_{CC} Power down

Figure 4. A.C. Waveforms for Programming Operations

Analysis Of Program Timing Waveforms

Set-up Program/Program

Two-cycle write commands are required for program operations (section A&B). The first program command (40H) is a set-up command and does not affect the array data (section A). The second program command latches address and data required for programming on the falling and rising edge of WE respectively (section B). The rising edge of this WE pulse (section B) also initiates the programming pulse. The device is programmed on a byte by byte basis either sequentially or randomly.

The program pulse occurs in section C.

Time-out

A software timing routine (10µs duration) must be initiated on the rising edge of the WE pulse of section B.

Program-verify

Upon completion of the program timing routine, the microprocessor must write the program-verify command (C0H). This command terminates the programming operation on the rising edge of the WE pulse (section D). The program-verify command also stages the device for data verification (section F). Another software timing routine (6µs duration) must be executed to allow for generation of internal voltages for margin checking and read operations (section E).

During program-verification (section F) each byte just programmed is read to compare array data with original program data. When successfully verified, the next desired address is programmed. Should a byte fail to verify, reprogram the byte (repeat section A thru F). Each data change sequence allows the device to use up to 25 program pulses per byte. Typically, bytes are verified within one or two pulses.

Note:
The program-verify operation must be written to terminate the programming operation. Should a system interrupt occur during a programming operation, always write the program-verify command prior to executing an interrupt sequence.

Algorithm Timing Delays

There are four different timing delays associated with the Flasherase and Flashrite algorithms:

1. The first delay is associated with the V_{PP} rise-time when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on the V_{PP}, the delay required is proportional to the number of devices being erased and the 0.1μF/device. V_{PP} must reach its final value 100ns before commands are executed.
2. The second delay time is the erase time pulse width (10 ms). A software timing routine should be run by the local microprocessor to time out the delay. The erase operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the erase operation. To ensure proper device operation, write the Erase-verify operation after each pulse, or the device may continue to erase until the memory cells are driven into depletion (over-erasure). Should this happen the internal circuitry will no longer select unique addresses. A symptom of over-erasure is an error attempting to program the next time. Occasionally it is possible to recover over-erased devices by programming all of the locations with 00H data.
3. A third delay time is required for each programming pulse width (10 μs). The programming algorithm is interactive and verifies each byte after a program pulse. The program operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the programming operation.
4. A fourth timing delay associated with both the Flasherase and Flashrite algorithms is the write recovery time (6 μs). During this time internal circuitry is changing voltage levels from the erase/ program level to those used for margin verify and read operations. An attempt to read the device during this period will result in possible false data (it may appear the device is not properly erased or programmed).

Note:
Software timing routines should be written in machine language for each of the delays. Code written in machine language requires knowledge of the appropriate microprocessor clock speed in order to accurately time each delay.

Parallel Device Erasure

Many applications will use more than one Flash memory device. Total erase time may be minimized by implementing a parallel erase algorithm. Flash memories may erase at different rates. Therefore each device must be verified seperately. When a device is completely erased and verified use a masking code to prevent further erasure. The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-up Sequence

V_{CC} prior to V_{PP}

The Am28F512 powers-up in the Read only mode. In addition, the memory contents may only be altered after successful completion of a two step command sequence.

V_{PP} prior to V_{CC}

When V_{CC} = 0 V, the V_{PP} voltage is internally disabled from the device. Memory contents cannot be altered. With V_{PP} = 12 V, the Flash device resets to the Read mode when V_{CC} rises above 2 V.

Power supply sequencing is not required.

Reset Command

A reset command sequence is provided to initialize the Flash memory to a known state – Read mode. The Reset command sequence also provides the user with a means to safely abort the erase or program command sequences. Following either set-up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

If V_{PP} is left at high voltage during system resets, you must incorporate the device reset command into the hardware initialization code. This minimizes the potential for over erasure or programming if the device is in the middle of an erase or program operation during reset. Execute the reset command early in the initialization routine.

Auto Select Command

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Programming In-system

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F512 contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H. A read cycle from address 0001H returns the device code 25H (See Table 2). To terminate the operation, it is necessary to write another valid command into the register (See Table 3).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	
Ceramic Packages	– 65°C to +150°C
Plastic Packages	– 65°C to +125°C
Ambient Temperature with Power Applied	– 55°C to + 125°C
Voltage with Respect To Ground	
All pins except A_9 and V_{PP} (Note 1)	– 2.0V to 7.0V
V_{CC} (Note 1)	– 2.0V to 7.0V
A_9 (Note 2)	– 2.0V to 14.0V
V_{PP} (Note 2)	– 2.0V to 14.0V
Output Short Circuit Current (Note 3)	200mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A_9 and V_{PP} pins is –0.5V. During voltage transitions, A_9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

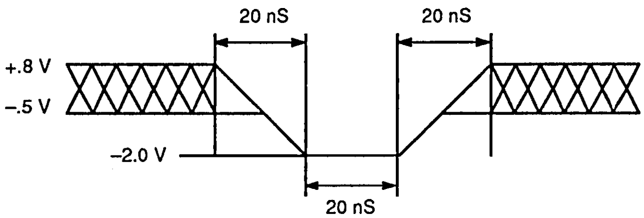
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (T_C)	0°C to +70°C
Industrial (I) Devices	
Case Temperature (T_C)	– 40°C to +85°C
Extended (E) Devices	
Case Temperature (T_C)	– 55°C to +125°C
Military (M) Devices	
Case Temperature (T_C)	– 55°C to +125°C
V_{CC} Supply Voltages	
V_{CC} for Am28F512–X5	+ 4.75V to +5.25V
V_{CC} for Am28F512–XX0	+ 4.50V to +5.50V
V_{PP} Supply Voltages	
Read	– 0.5V to +12.6V
Program, Erase, and Verify	+ 11.4V to +12.6V

MAXIMUM OVERSHOOT

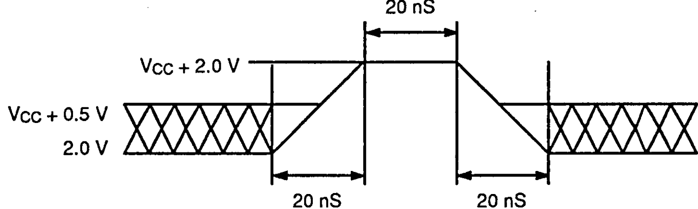
Maximum Negative Input Overshoot



11561-009A

Maximum Negative Overshoot Waveform

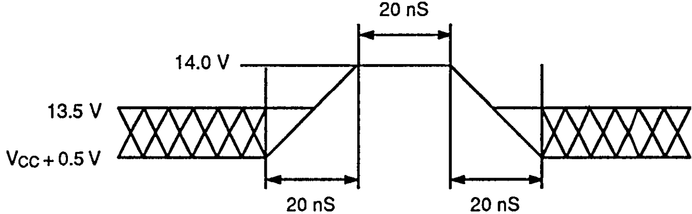
Maximum Positive Input Overshoot



11561-010A

Maximum Positive Overshoot Waveform

Maximum V_{PP} Overshoot



11561-011A

Maximum V_{PP} Overshoot Waveform

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted). (Notes 1–3)

DC CHARACTERISTICS-TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{IN} = V_{CC}$ or V_{SS}		± 1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{OUT} = V_{CC}$ or V_{SS}		± 1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max. $\overline{CE} = V_{IH}$		1.0	mA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ $I_{OUT} = 0$ mA, at 6 MHz		30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress		30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress		30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$		± 1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		200	µA
		$V_{PP} = V_{PPL}$		± 1.0	
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress		30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress		30	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA $V_{CC} = V_{CC}$ Min.		0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.5$ mA $V_{CC} = V_{CC}$ Min.	2.4		V
V_{ID}	A_9 Auto Select Voltage	$A_9 = V_{ID}$	11.5	13.0	V
I_{ID}	A_9 Auto Select Current	$A_9 = V_{ID}$ Max. $V_{CC} = V_{CC}$ Max.		50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/Program are inhibited when $V_{PP} = V_{PPL}$	0.0	V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4	12.6	V

DC CHARACTERISTICS-CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{IN} = V_{CC}$ or V_{SS}		± 1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{OUT} = V_{CC}$ or V_{SS}		± 1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max. $\overline{CE} = V_{IH}$		100	µA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ $I_{OUT} = 0$ mA, at 6 MHz		30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress		30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress		30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$		± 1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		200	µA
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress		30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress		30	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		V_{CC} – 0.5	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA $V_{CC} = V_{CC}$ Min.		0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.5$ mA, $V_{CC} = V_{CC}$ Min.	0.85 V_{CC}		V
V_{OH2}		$I_{OH} = -100$ µA, $V_{CC} = V_{CC}$ Min.	V_{CC} –0.4		
V_{ID}	A_9 Auto Select Voltage	$A_9 = V_{ID}$	11.5	13.0	V
I_{ID}	A_9 Auto Select Current	$A_9 = V_{ID}$ Max. $V_{CC} = V_{CC}$ Max.		50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/ Program are inhibited when $V_{PP} = V_{PPL}$	0.0	V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4	12.6	V

PRELIMINARY

Notes:

1. **Caution:** the Am28F512 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	8	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions $T_A = 25°C$, f = 1.0 MHz

SWITCHING CHARACTERISTICS over operating range unless otherwise specified.

AC CHARACTERISTICS-Read Only Operation (Notes 1– 2)

Parameter Symbols				Am28F512					
JEDEC	Standard	Parameter Description		— -75	-90 -95	-120 —	-150 —	-200 —	Unit
t_{AVAV}	t_{RC}	Read Cycle Time	Min.	70	90	120	150	200	ns
			Max.						
t_{ELQV}	t_{CE}	Chip Enable	Min.						
		Access Time	Max.	70	90	120	150	200	ns
t_{AVQV}	t_{ACC}	Address	Min.						
		Access Time	Max.	70	90	120	150	200	ns
t_{GLQV}	t_{OE}	Output Enable	Min.						
		Access Time	Max.	35	40	50	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to	Min.	0	0	0	0	0	ns
		Output in Low Z	Max.						
t_{EHQZ}	t_{DF}	Chip Disable to	Min.						
		Output in High Z	Max.	25	25	30	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to	Min.	0	0	0	0	0	ns
		Output in Low Z	Max.						
t_{GHQZ}	t_{DF}	Output Disable to	Min.						
		Output in High Z	Max.	25	25	30	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of	Min.	0	0	0	0	0	ns
		Address, $\overline{CE}$, or $\overline{OE}$ Change	Max.						
t_{WHGL}		Write Recovery	Min.	6	6	6	6	6	µs
		Time before Read	Max.						

Notes:

1. Output Load (except Am28F512-75): 1 TTL gate and $C_L = 100$ pF, Input Rise and Fall Times: ≤ 10 ns, Input Pulse levels: 0.45 to 2.4 V, Timing Measurement Reference Level - Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. The Am28F512-75 Output Load: 1 TTL gate and $C_L = 30$ pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0 to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.

AC CHARACTERISTICS-Write/Erase/Program Operations (Notes 1– 4)

Parameter Symbols				Am28F512					
JEDEC	Standard	Parameter Description		— –75	–90 –95	–120 —	–150 —	–200 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time	Min. Max.	70	90	120	150	200	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min. Max.	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min. Max.	40	45	50	60	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min. Max.	40	45	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min. Max.	10	10	10	10	10	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	Min. Max.	6	6	6	6	6	µs
t_{GHWL}		Read Recovery Time before Write	Min. Max.	0	0	0	0	0	µs
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	Min. Max.	0	0	0	0	0	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min. Max.	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min. Max.	40	45	50	50	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min. Max.	20	20	20	20	20	ns
t_{WHWH1}		Duration of Programming Operation	Min. Max.	10 25	10 25	10 25	10 25	10 25	µs
t_{WHWH2}		Duration of Erase Operation	Min. Max.	9.5 10.5	9.5 10.5	9.5 10.5	9.5 10.5	9.5 10.5	ms
t_{EHVP}		Chip Enable Set-Up Time to V_{PP} Ramp	Min. Max.	100	100	100	100	100	ns
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW	Min. Max.	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time	Min. Max.	2	2	2	2	2	µs
t_{VPPR}		V_{PP} Rise Time	Min. Max.	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time	Min. Max.	500	500	500	500	500	ns

Notes:

1. Read timing characteristics during read/write operations are the same as durng read-only operations. Refer to AC Characteristics for Read Only operations.
2. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the Write Pulse Width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.
3. All devices except Am28F512-75. Input Rise and Fall times: $\leq$ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V
4. Am28F512-75. Input Rise and Fall times: $\leq$ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V
   Timing Measurement Reference Level: Inputs and Outputs: 1.5 V

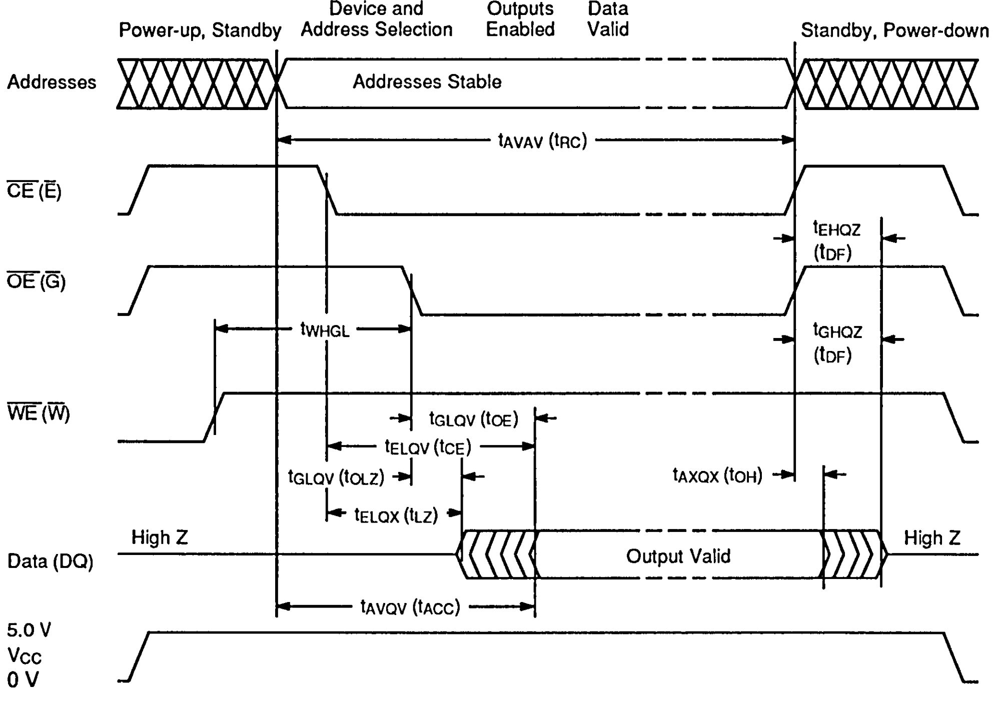


Figure 5. AC Waveforms for Read Operations

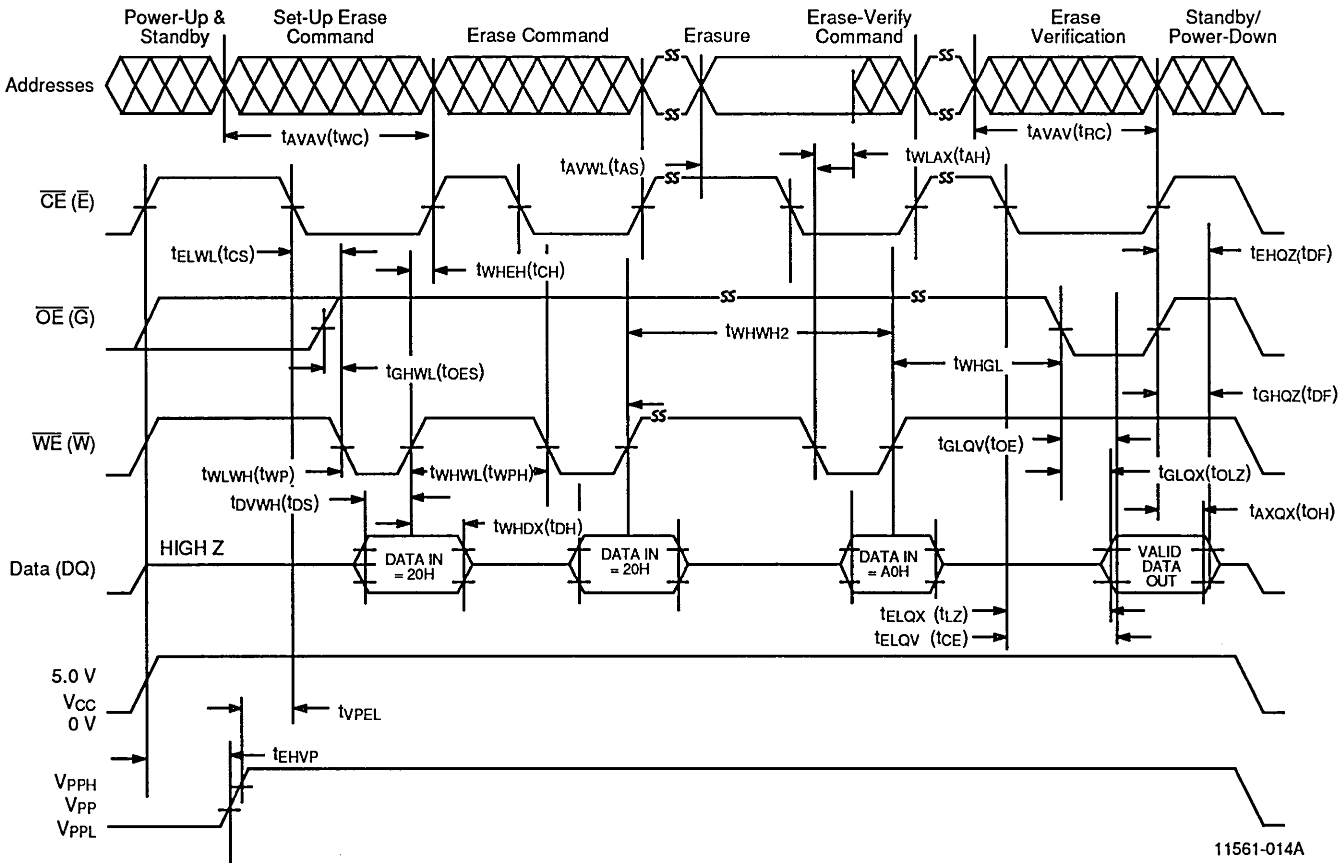


Figure 6. A.C. Waveforms for Erase Operations

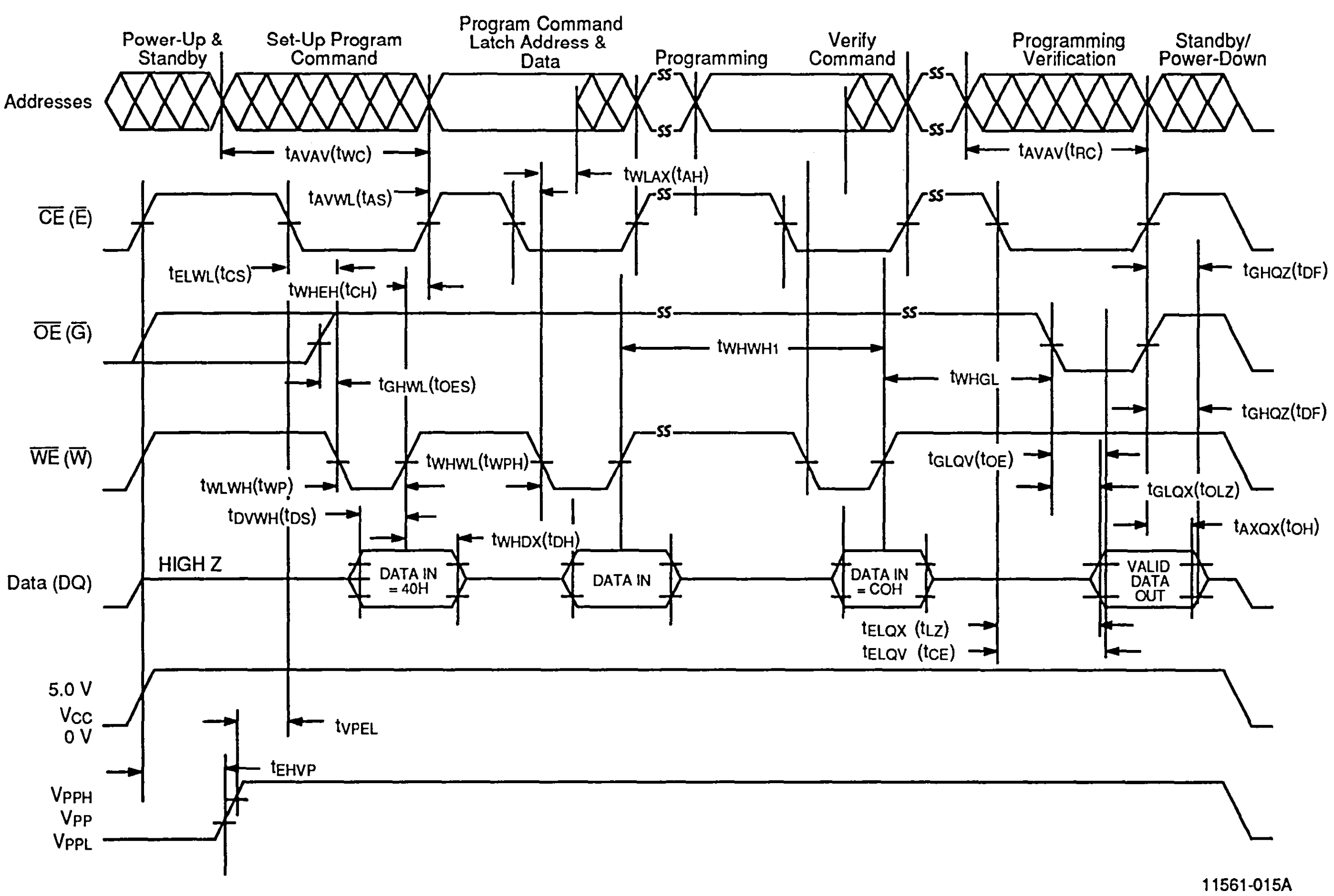
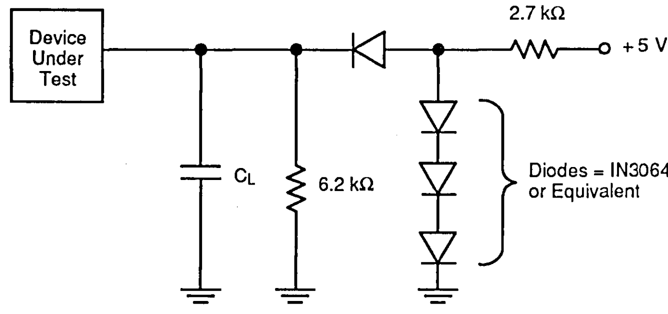


Figure 7. A.C. Waveforms for Programming Operations

SWITCHING TEST CIRCUIT



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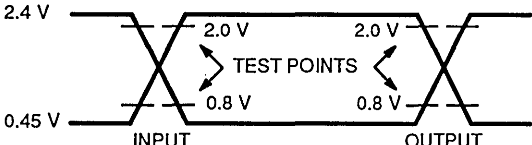
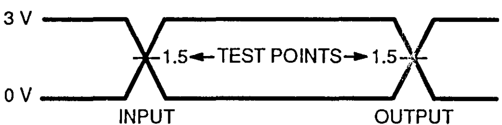
C_L = 100 pF including jig capacitance (30 pF for Am28F512-75)

SWITCHING TEST WAVEFORMS





All Devices Except Am28F512-75

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.

For Am28F512-75

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.

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ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Chip Erase Time		0.5 (Note 1)	10	S	Excludes 00H programming prior to erasure
Chip Programming Time		1 (Note 1)	12	S	Excludes system-level overhead
Erase/Program Cycles					
Am28F512-75C4JC	10,000			Cycles	
Am28F512-75C3JC	1,000			Cycles	

Note:

1. 25°C, 12V V_{PP}

LATCHUP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A_9 and V_{PP})	– 1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	– 1.0 V	V_{CC} + 1.0 V
Current	– 100 mA	+ 100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

Preliminary

Am28F010

131,072 x 8-Bit CMOS Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 90 ns maximum access time
- **Low power consumption**
  - 30 mA maximum active current
  - 100 μA maximum standby current
- **Compatible with JEDEC-standard byte-wide 32-Pin E^2PROM pinouts**
  - 32-pin DIP
  - 32-pin PLCC
- **10,000 erase/program cycles**
- **Program and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to V_{CC} +1 V**
- **Flasherase™ Electrical Bulk Chip-Erase**
  - One second typical chip-erase
- **Flashrite™ programming**
  - 10 μs typical byte-program
  - Less than 2 seconds typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell

GENERAL DESCRIPTION

The Am28F010 is a 1 Megabit "Flash" electrically erasable, electrically programmable read only memory organized as 128K bytes of 8 bits each. The Am28F010 is packaged in 32-pin PDIP and PLCC versions which allow for upgrades to the 2 Megabit density. The device is also offered in ceramic DIP and LCC packages. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers.

The standard Am28F010 offers access times as fast as 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F010 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F010 uses a command register to manage this functionality, while maintaining a standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

AMD's Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F010 uses a 12.0 V ± 5% V_{PP} supply to perform the Flasherase and Flashrite algorithms.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from –1 V to V_{CC}+1 V.

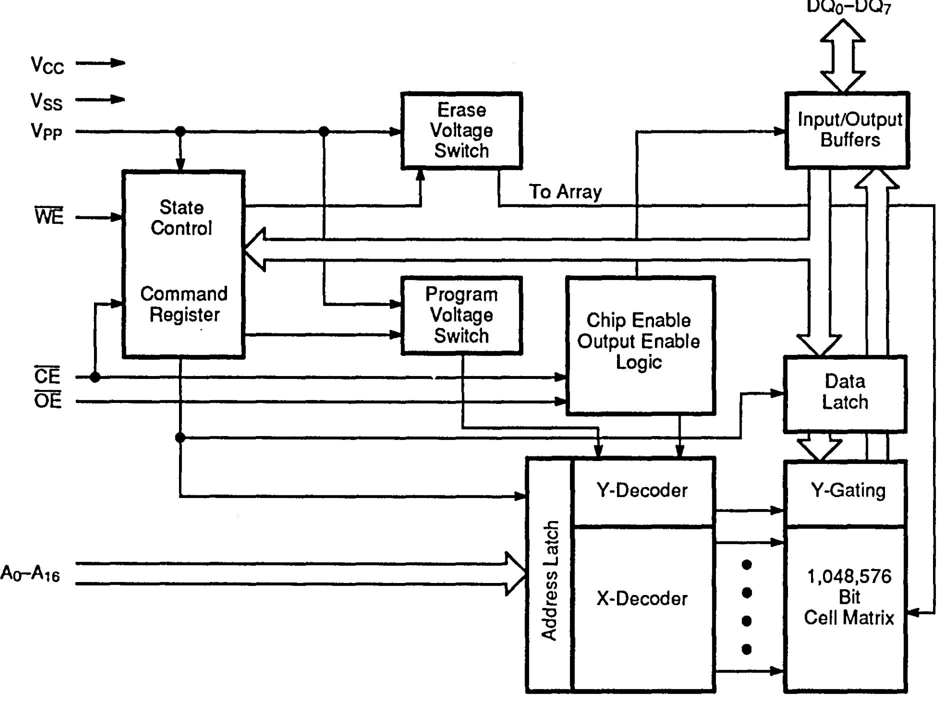
The Am28F010 is byte programmable using 10 μs programming pulses in accordance with AMD's Flashrite programming algorithm. The typical room temperature programming time of the Am28F010 is less than two seconds. The entire chip is bulk erased using 10ms erase pulses according to AMD's Flasherase algorithm. Typical erasure at room temperature is accomplished in less than one second. The windowed package and the 15–20 minutes required for EPROM erasure using ultraviolet light are eliminated.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F010 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

AMD's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F010 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

Publication# 11559 Rev. B Amendment/0
Issue Date: June 1990

BLOCK DIAGRAM



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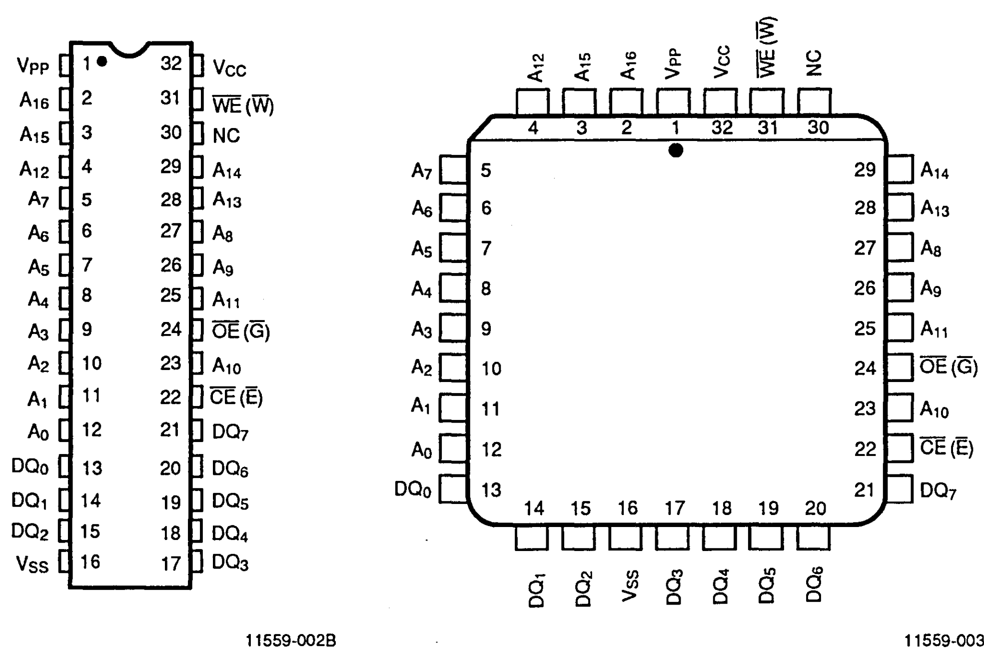
PRODUCT SELECTOR GUIDE

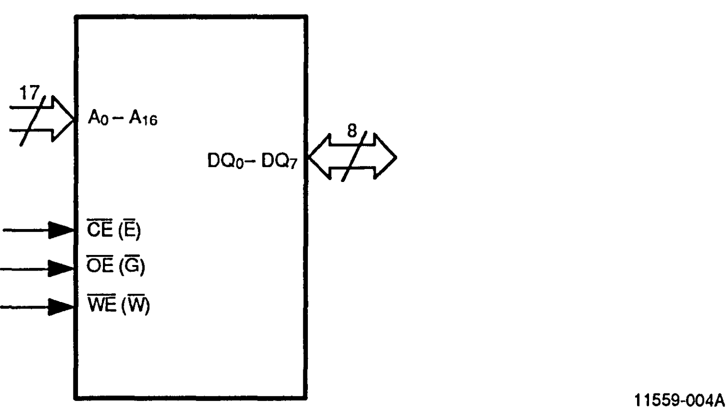
Family Part No.	**Am28F010**			
Ordering part No: ± 10% V_{CC} Tolerance	–90	–120	–150	–200
± 5% V_{CC} Tolerance	–95	—	—	—
Max Access Time (ns)	90	120	150	200
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	120	150	200
$\overline{OE}$ ($\overline{G}$) Access (ns)	40	50	65	75

CONNECTION DIAGRAMS



Note: Pin 1 is marked for orientation

LOGIC SYMBOL

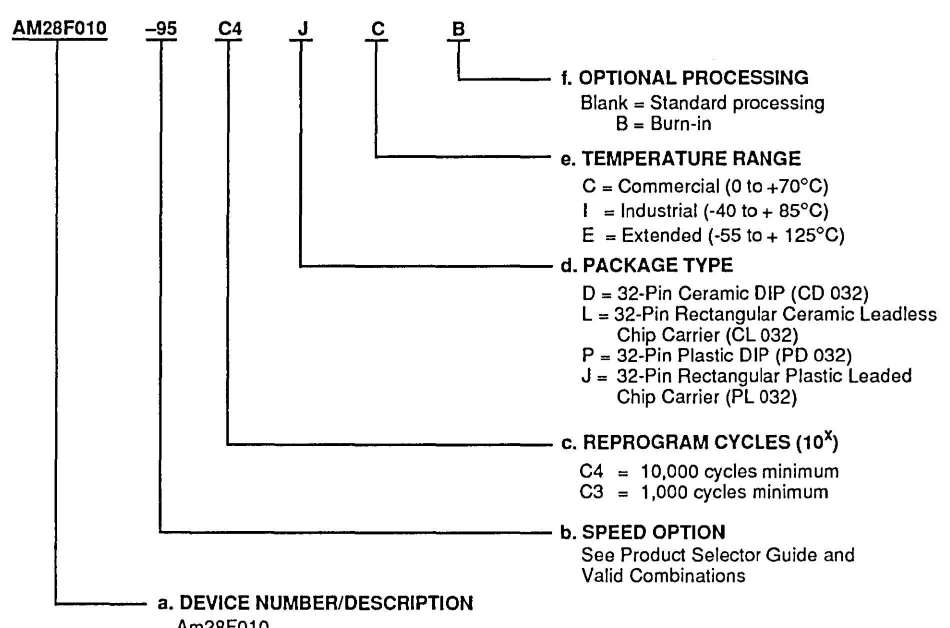


PIN DESCRIPTION

Symbol	Functional Description
$A_0 - A_{16}$	Address Inputs for memory locations. Internal latches hold addresses during write cycles.
$DQ_0 - DQ_7$	Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.
$\overline{CE}$ ($\overline{E}$)	The Chip Enable active low input activates the chip'scontrol logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.
$\overline{OE}$ ($\overline{G}$)	The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.
$\overline{WE}$ ($\overline{W}$)	The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the ap propriate data is latched on the rising edge of the pulse.
V_{PP}	Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC}$ +2V.
V_{CC}	Power supply for device operation. (5.0V ± 5% or 10%)
V_{SS}	Ground
NC	No Connect-corresponding pin is not connected internally to the die.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:
a. Device Number
b. Speed Option
c. Reprogram Cycles
d. Package Type
e. Temperature Range
f. Optional Processing



a. DEVICE NUMBER/DESCRIPTION
Am28F010
1 Megabit (128K x 8-Bit) CMOS Flash Memory

Valid Combinations	
AM28F010-95 AM28F010-90 AM28F010-120 AM28F010-150 AM28F010-200	C4DC, C4DCB, C4DI, C4DIB, C4DE, C4DEB, C4LC, C4LCB, C4LI, C4LIB, C4LE, C4LEB, C4PC, C4PI, C4JC, C4JI, C3DC, C3DCB, C3DI, C3DIB, C3DE, C3DEB, C3LC, C3LCB, C3LI, C3LIB, C3LE, C3LEB, C3PC, C3PI, C3JC, C3JI

Valid Combinations

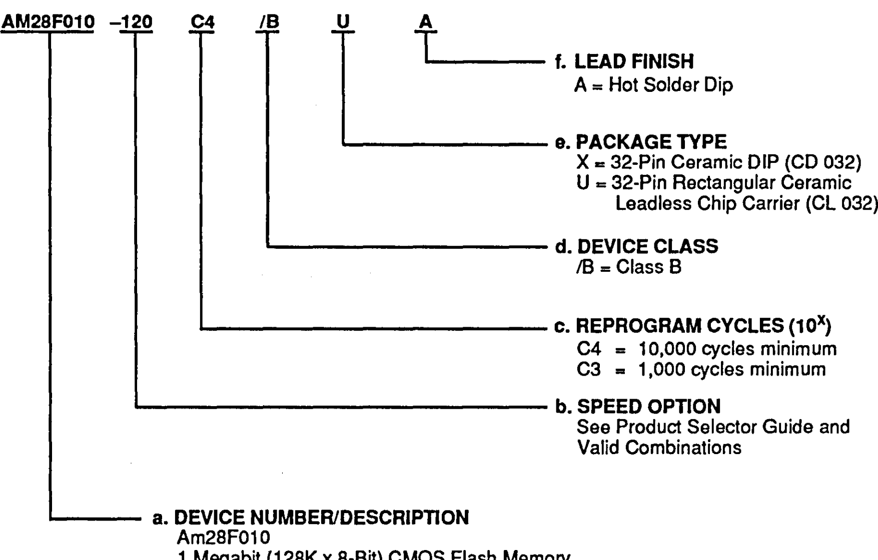
Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Reprogram cycles
d. Device Class
e. Package Type
f. Lead Finish



Valid Combinations	
AM28F010-120 AM28F010-150 AM28F010-200	C4/BXA, C4/BUA C3/BXA, C3/BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

BASIC PRINCIPLES

The Am28F010 uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F010 functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F010's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F010 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Erase Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note:
The Flash memory array must be completely programmed prior to erasure. Refer to the Flasherase Algorithm.

1. **Set-up Erase:** Write the Set-up Erase command to the command register.
2. **Erase:** Write the Erase command (same as Set-up Erase command) to the command register again. The second command initiates the erase operation. The system software routines must now time-out the erase pulse width (10 ms) prior to issuing the Erase-verify command.
3. **Erase-verify:** Write the Erase-verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFH data (Byte erased). After successful data verification the Erase-verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Programming Sequence

A three step command sequence (a two-cycle Program command and one cycle Verify command) is required to program a byte of the Flash array. Refer to the Flashrite Algorithm.

1. **Set-up Program:** Write the Set-up Program command to the command register.
2. **Program:** Write the Program command to the command register with the appropriate Address and Data. The system software routines must now time-out the program pulse width (10 µs) prior to issuing the Program-verify command.
3. **Program-verify:** Write the Program-verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times.

FUNCTIONAL DESCRIPTION

Description Of User Modes

Table 1. Am28F010 User Bus Operations

	Operation	$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A_0	A_9	I/O
Read-Only	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	A_0	A_9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (A7H)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A_0	A_9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A_0	A_9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2V$, See DC Characteristics for voltage levels of V_{PPH}, $0V < A_n < V_{CC} + 2V$, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC} + 2.0V$. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.
3. $11.5 \leq V_{ID} \leq 13.0V$
4. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.
5. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid D_{IN} during a write operation.
7. All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A_9 and A_0 must be held at V_{IL}.

READ ONLY MODE

$V_{PP} < V_{CC} + 2V$

Command Register Inactive

Read

The Am28F010 functions as a read only memory when $V_{PP} < V_{CC} + 2V$. The Am28F010 has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC} - t_{OE}$).

Standby Mode

The Am28F010 has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5V$), consumes less than 100µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A Prom Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5V to 13.0V) on address A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to $V_{CC} + 2.0V$ while using this Auto select mode. Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am28F010 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ_7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F010 Auto Select Code

Type	A_0	Code (HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	A7	1	0	1	0	0	1	1	1

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%
Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

Register bits $R_7 - R_0$ correspond to the data inputs $DQ_7 - DQ_0$ (Refer to Table 3). Register bits $R_7 - R_5$ store the command data. All register bits R_4 to R_0 must be zero. The only exceptions are: the reset command, when FFH is written to the register and Auto select, when 90H or 80H is written to the register.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 4 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Wait 6µs before reading the first accessed address location. All subsequent Read operations take t_{ACC}. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Command Register

Data Input/Output	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Command Register	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0
Data/Commands*	X	X	X	X	X	X	X	X

* **Notes:**

1. See Table 4 Am28F010 Command Definitions
2. X = Appropriate Data or Register Commands

Table 4. Am28F010 Command Definitions

Command	First Bus Cycle Operation (Note 1)	Address (Note 2)	Data (Note 3)	Second Bus Cycle Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 6)	Write	X	00H	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/A7H
Set-up Erase/Erase (Note 4)	Write	X	20H	Write	X	20H
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Set-up Program/Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Reset	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 1.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Flasherase Electrical Erase Algorithm.
5. Figure 2 illustrates the Flashrite Programming Algorithm.
6. Wait 6µs after first Read command before accessing the data. When the second bus command is a Read command, all subsequent Read operations take t_{ACC}.

Erase Sequence

Set-up Erase/Erase Commands

Set-up Erase

Set-up Erase is the first of a two-cycle erase command. It is a command-only operation that stages the device for bulk chip erase. The array contents are not altered with this command. 20H is written to the command register in order to perform the Set-up Erase operation.

Erase

The second two-cycle erase command initiates the bulk erase operation. You must write the Erase command (20H) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-verify) to the register.

This two step sequence of the Set-up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, chip erasure can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:
The Flash memory device must be fully programmed to 00H data prior to erasure. This equalizes the charge on all memory cells ensuring reliable erasure.

Erase-verify Command

The erase operation erases all bytes of the array in parallel. After the erase operation, all bytes must be sequentially verified. The Erase-verify operation is initiated by writing A0H to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-verify operation, the Am28F010 applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are properly erased.

Verify Next Address

You must write the Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$. The process continues for each byte in

the memory array until a byte does not return FFH data or all the bytes in the array are accessed and verified.

If an address is not verified to FFH data, the entire chip is erased again (refer to Set-up Erase/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The device is now ready to be programmed. At this point, the verification operation is terminated by writing a valid command (e.g. Program set-up) to the command register. Figure 1 and Table 5, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:
The erase-verify command must be written to the register in order to terminate the erase operation. During the erase operations, the local microprocessor must be dedicated to run software timing routines (erase in 10ms) as specified in AMD's Flasherase algorithm.

Should a system interrupt occur during an erase operation, always write the Erase-verify command prior to executing an interrupt sequence.

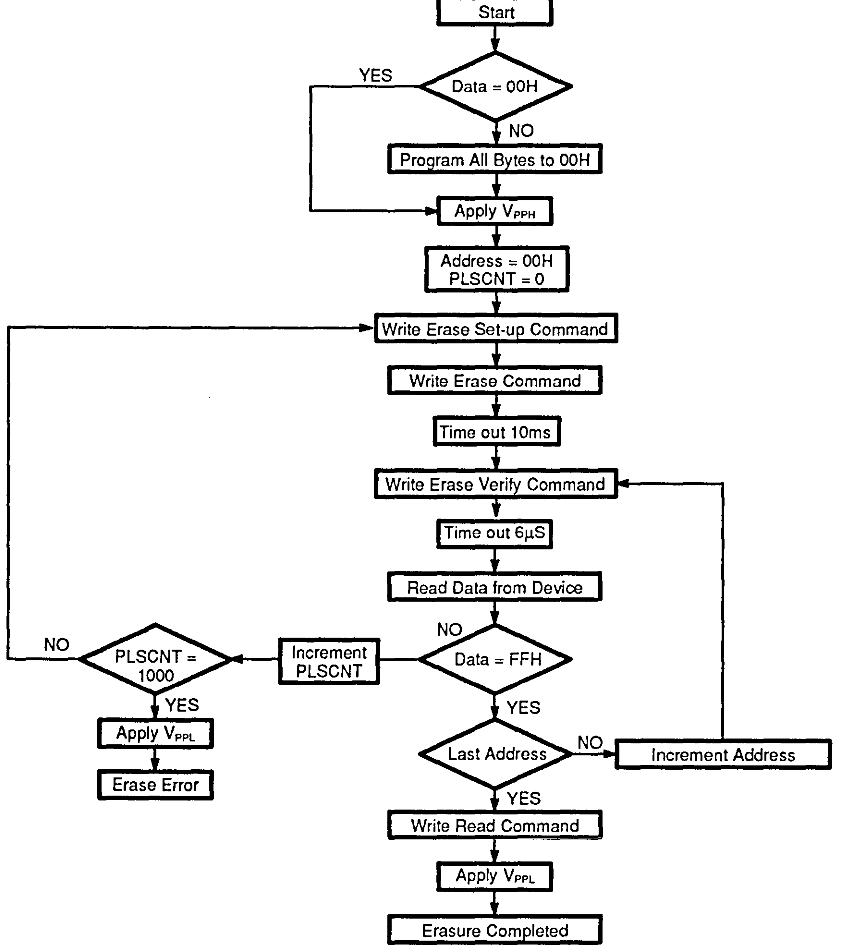


Figure 1. Flasherase Electrical Erase Algorithm

Flasherase Electrical Erase Algorithm

This Flash memory device erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the array. Erasure begins with a read of the memory contents. The Am28F010 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

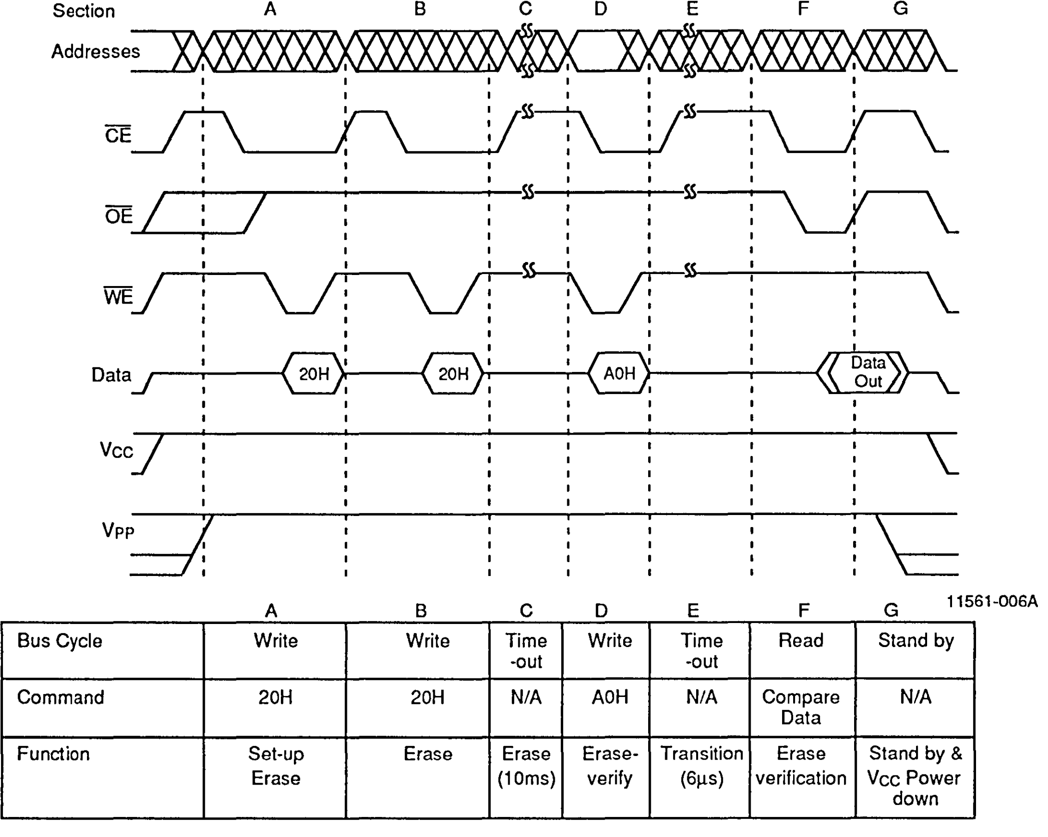
Should the device be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished using the Flashrite programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. If a byte fails to verify, the device is erased again. With each erase operation, an increasing number of bytes verify to the erased state. Typically, devices are erased in less than 100 pulses (1 second). Erase efficiency may be improved by storing the address of the last byte that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. A total of 1000 erase operations are allowed per reprogram cycle, which corresponds to approximately 10 seconds of cumulative erase time. Erasure typically occurs in one second. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 1 illustrates the electrical erase algorithm.

Table 5. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) **Note:** Use Flashrite programming algorithm (Figure 2) for programming.
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Set-Up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6µs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Read	Data = 00H, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0V.
2. Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.
3. The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	20H	20H	N/A	A0H	N/A	Compare Data	N/A
Function	Set-up Erase	Erase	Erase (10ms)	Erase-verify	Transition (6µs)	Erase verification	Stand by & V_{CC} Power down

Figure 2. A.C. Waveforms For Erase Operations

Analysis Of Erase Timing Waveform

Note:

This analysis does not include the requirement to program the entire array to 00H data prior to erasure. Refer to the Flasherase algorithm.

Set-up Erase/Erase

This analysis illustrates the use of two-cycle erase commands (section A&B). The first erase command (20H) is a set-up command and does not affect the array data (section A). The second erase command (20H) initiates the erase operation (section B) on the rising edge of this $\overline{\text{WE}}$ pulse. All bytes of the memory array are erased in parallel. No address information is required.

The erase pulse occurs in section C.

Time-out

A software timing routine (10ms duration) must be initiated on the rising edge of the $\overline{\text{WE}}$ pulse of section B.

Erase-verify

Upon completion of the erase software timing routine, the microprocessor must write the Erase-verify command (A0H). This command terminates the erase operation on the rising edge of the $\overline{\text{WE}}$ pulse (section D). The Erase-verify command also stages the device for data verification (section F).

After each erase operation each byte must be verified. The byte address to be verified must be supplied with the Erase-verify command (section D). Addresses are latched on the falling edge of the $\overline{\text{WE}}$ pulse.

Another software timing routine (6µs duration) must be executed to allow for generation of internal voltages for margin checking and read operation (section E).

During Erase-verification (section F) each address that returns FFH data is successfully erased. Each address of the array is sequentially verified in this manner by repeating sections D thru F until the entire array is verified or an address fails to verify. Should an address location fail to verify to FFH data, erase the device again. Repeat sections A thru F. Resume verification (section D) with the failed address.

Each data change sequence allows the device to use up to 1,000 erase pulses to completely erase. Typically 100 erase pulses are required.

Notes:

1. All address locations must be programmed to 00H prior to erase. This equalizes the charge on all memory cells and ensures reliable erasure.

2. The erase verify command must be written to terminate the erase operation. Should a system interrupt occur during an erase operation, always write the erase-verify command prior to executing an interrupt sequence.

Programming Sequence

Set-up Program/Program Command

Set-up Program

The Am28F010 is programmed byte by byte. Bytes may be programmed sequentially or at random. Set-up Program is the first of a two-cycle program command. It stages the device for byte programming. The Set-up Program operation is performed by writing 40H to the command register.

Program

Only after the program set-up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-verify command to terminate the programming operation. This two step sequence of the Set-up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte just programmed must be verified.

Write C0H into the command register in order to initiate the Program-verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-verify operation stages the device for verification of the last byte programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-verify operation, the Am28F010 applies an internally generated margin voltage to the addressed byte. A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte location. Should the byte fail to verify, reprogram (refer to Set-up Program/Program). Figure 3 and Table 6 indicate how instructions are combined with the bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Flashrite Programming Algorithm

The Am28F010 Flashrite programming algorithm employs an interactive closed loop flow to program data byte by byte. Bytes may be programmed sequentially or at random. The Flashrite programming algorithm uses 10 microsecond programming pulses. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 3 and Table 6 illustrate the programming algorithm.

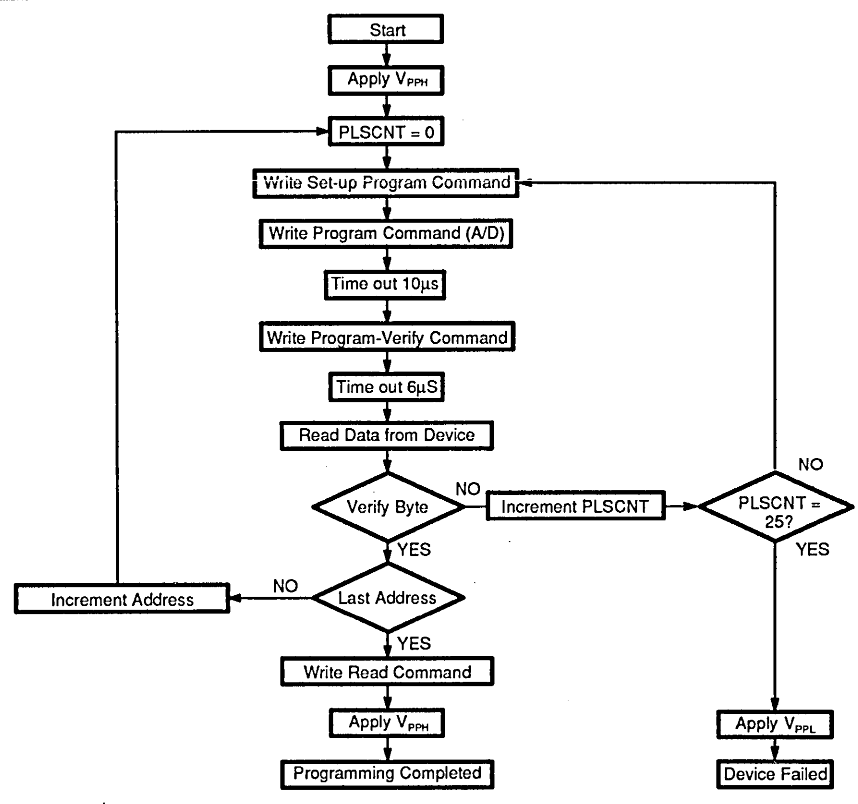


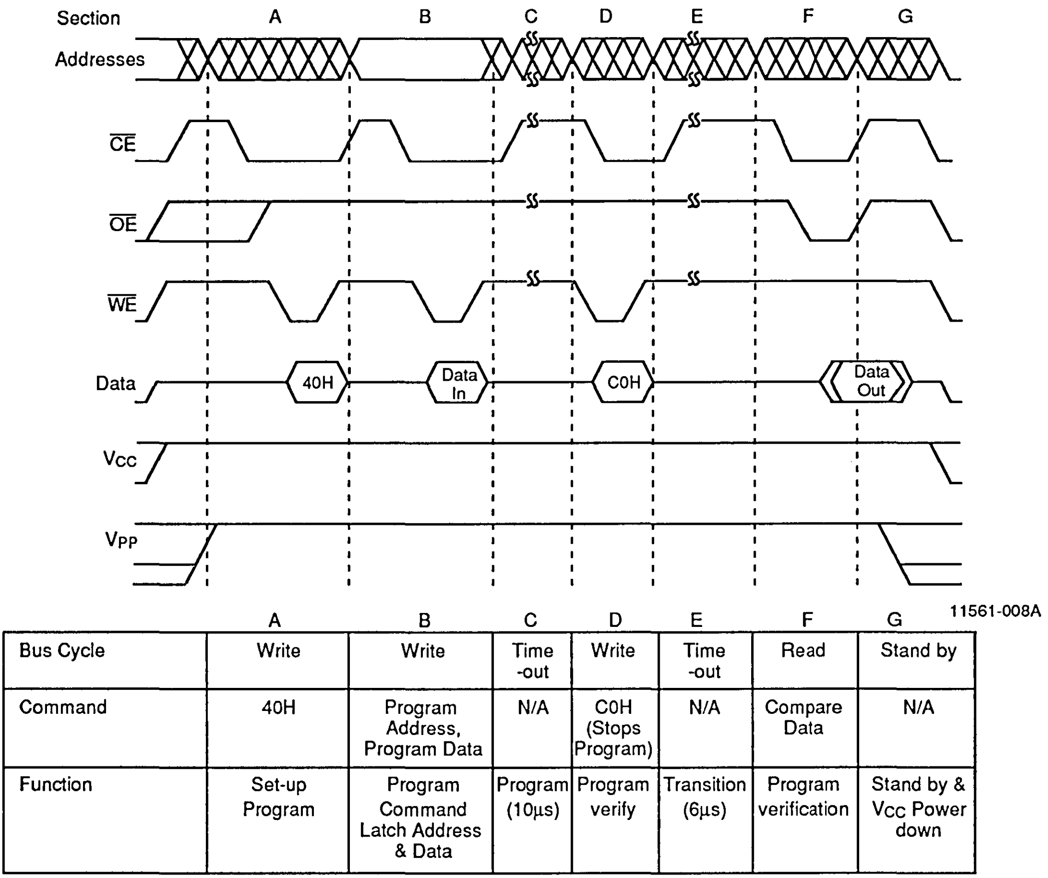
Figure 3. Flashrite Programming Algorithm

Table 6. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Set-Up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0V.
2. Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	40H	Program Address, Program Data	N/A	C0H (Stops Program)	N/A	Compare Data	N/A
Function	Set-up Program	Program Command Latch Address & Data	Program (10µs)	Program verify	Transition (6µs)	Program verification	Stand by & V_{CC} Power down

Figure 4. A.C. Waveforms for Programming Operations

Analysis Of Program Timing Waveforms

Set-up Program/Program

Two-cycle write commands are required for program operations (section A&B). The first program command (40H) is a set-up command and does not affect the array data (section A). The second program command latches address and data required for programming on the falling and rising edge of $\overline{WE}$ respectively (section B). The rising edge of this $\overline{WE}$ pulse (section B) also initiates the programming pulse. The device is programmed on a byte by byte basis either sequentially or randomly.

The program pulse occurs in section C.

Time-out

A software timing routine (10µs duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Program-verify

Upon completion of the program timing routine, the microprocessor must write the program-verify command (C0H). This command terminates the programming operation on the rising edge of the $\overline{WE}$ pulse (section D). The program-verify command also stages the device for data verification (section F). Another software timing routine (6µs duration) must be executed to allow for generation of internal voltages for margin checking and read operations (section E).

During program-verification (section F) each byte just programmed is read to compare array data with original program data. When successfully verified, the next desired address is programmed. Should a byte fail to verify, reprogram the byte (repeat section A thru F). Each data change sequence allows the device to use up to 25 program pulses per byte. Typically, bytes are verified within one or two pulses.

Note:
The program-verify operation must be written to terminate the programming operation. Should a system interrupt occur during a programming operation, always write the program-verify command prior to executing an interrupt sequence.

Algorithm Timing Delays

There are four different timing delays associated with the Flasherase and Flashrite algorithms:

1. The first delay is associated with the V_{PP} rise-time when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on the V_{PP}, the delay required is proportional to the number of devices being erased and the 0.1µF/device. V_{PP} must reach its final value 100ns before commands are executed.
2. The second delay time is the erase time pulse width (10 ms). A software timing routine should be run by the local microprocessor to time out the delay. The erase operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the erase operation. To ensure proper device operation, write the Erase-verify operation after each pulse, or the device may continue to erase until the memory cells are driven into depletion (over-erasure). Should this happen the internal circuitry will no longer select unique addresses. A symptom of over-erasure is an error attempting to program the next time. Occasionally it is possible to recover over-erased devices by programming all of the locations with 00H data.
3. A third delay time is required for each programming pulse width (10 µs). The programming algorithm is interactive and verifies each byte after a program pulse. The program operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the programming operation.
4. A fourth timing delay associated with both the Flasherase and Flashrite algorithms is the write recovery time (6 µs). During this time internal circuitry is changing voltage levels from the erase/ program level to those used for margin verify and read operations. An attempt to read the device during this period will result in possible false data (it may appear the device is not properly erased or programmed).

Note:
Software timing routines should be written in machine language for each of the delays. Code written in machine language requires knowledge of the appropriate microprocessor clock speed in order to accurately time each delay.

Parallel Device Erasure

Many applications will use more than one Flash memory device. Total erase time may be minimized by implementing a parallel erase algorithm. Flash memories may erase at different rates. Therefore each device must be verified seperately. When a device is completely erased and verified use a masking code to prevent further erasure. The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-up Sequence

V_{CC} prior to V_{PP}

The Am28F010 powers-up in the Read only mode. In addition, the memory contents may only be altered after successful completion of a two step command sequence.

V_{PP} prior to V_{CC}

When V_{CC} = 0 V, the V_{PP} voltage is internally disabled from the device. Memory contents cannot be altered. With V_{PP} = 12 V, the Flash device resets to the Read mode when V_{CC} rises above 2 V.

Power supply sequencing is not required.

Reset Command

A reset command sequence is provided to initialize the Flash memory to a known state – Read mode. The Reset command sequence also provides the user with a means to safely abort the erase or program command sequences. Following either set-up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

If V_{PP} is left at high voltage during system resets, you must incorporate the device reset command into the hardware initialization code. This minimizes the potential for over erasure or programming if the device is in the middle of an erase or program operation during reset. Execute the reset command early in the initialization routine.

Auto Select Command

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Programming In-system

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F010 contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H. A read cycle from address 0001H returns the device code A7H (See Table 2). To terminate the operation, it is necessary to write another valid command into the register (See Table 3).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	
Ceramic Packages	– 65°C to +150°C
Plastic Packages	– 65°C to +125°C
Ambient Temperature with Power Applied	– 55°C to + 125°C
Voltage with Respect To Ground	
All pins except A_9 and V_{PP} (Note 1)	– 2.0V to 7.0V
V_{CC} (Note 1)	– 2.0V to 7.0V
A_9 (Note 2)	– 2.0V to 14.0V
V_{PP} (Note 2)	– 2.0V to 14.0V
Output Short Circuit Current (Note 3)	200mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*

2. *Minimum DC input voltage on A_9 and V_{PP} pins is –0.5V. During voltage transitions, A_9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*

3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

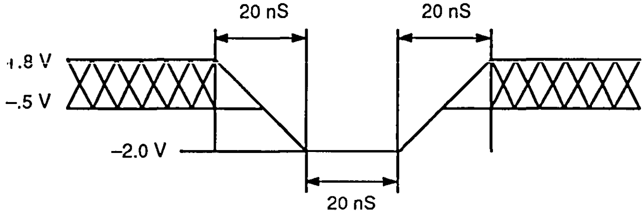
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (T_C)	0°C to +70°C
Industrial (I) Devices	
Case Temperature (T_C)	– 40°C to +85°C
Extended (E) Devices	
Case Temperature (T_C)	– 55°C to +125°C
Military (M) Devices	
Case Temperature (T_C)	– 55°C to +125°C
V_{CC} Supply Voltages	
V_{CC} for Am28F010–X5	+ 4.75V to +5.25V
V_{CC} for Am28F010–XX0	+ 4.50V to +5.50V
V_{PP} Supply Voltages	
Read	– 0.5V to +12.6V
Program, Erase, and Verify	+ 11.4V to +12.6V

MAXIMUM OVERSHOOT

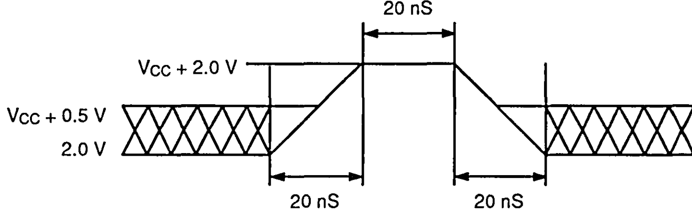
Maximum Negative Input Overshoot



11561-009A

Maximum Negative Overshoot Waveform

Maximum Positive Input Overshoot



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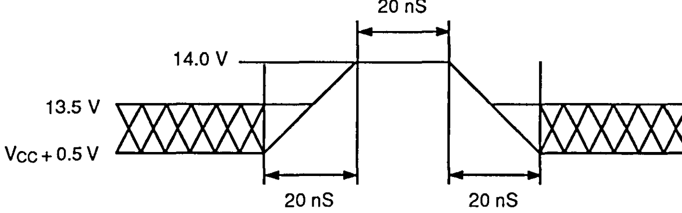
Maximum Positive Overshoot Waveform

Maximum V_{PP} Overshoot



11561-011A

Maximum V_{PP} Overshoot Waveform

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted). (Notes 1–3)

DC CHARACTERISTICS-TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{IN} = V_{CC}$ or V_{SS}		± 1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{OUT} = V_{CC}$ or V_{SS}		± 1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max. $\overline{CE} = V_{IH}$		1.0	mA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ I_{OUT} = 0 mA, at 6 MHz		30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress		30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress		30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$		± 1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		200	µA
		$V_{PP} = V_{PPL}$		± 1.0	
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress		30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress		30	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA $V_{CC} = V_{CC}$ Min.		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA $V_{CC} = V_{CC}$ Min.	2.4		V
V_{ID}	A_9 Auto Select Voltage	$A_9 = V_{ID}$	11.5	13.0	V
I_{ID}	A_9 Auto Select Current	$A_9 = V_{ID}$ Max. $V_{CC} = V_{CC}$ Max.		50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/Program are inhibited when $V_{PP} = V_{PPL}$	0.0	V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4	12.6	V

PRELIMINARY

DC CHARACTERISTICS-CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max., V_{IN} = V_{CC} or V_{SS}		± 1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max., V_{OUT} = V_{CC} or V_{SS}		± 1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max. $\overline{CE}$ = V_{IH}		100	µA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max., $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress		30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress		30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}		± 1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		200	µA
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress		30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress		30	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		V_{CC} – 0.5	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA V_{CC} = V_{CC} Min.		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min.	0.85 V_{CC}		V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min.	V_{CC} –0.4		
V_{ID}	A_9 Auto Select Voltage	A_9 = V_{ID}	11.5	13.0	V
I_{ID}	A_9 Auto Select Current	A_9 = V_{ID} Max. V_{CC} = V_{CC} Max.		50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/ Program are inhibited when V_{PP} = V_{PPL}	0.0	V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4	12.6	V

PRELIMINARY

Notes:

1. **Caution:** the Am28F010 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	8	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions $T_A = 25°C$, f = 1.0 MHz

SWITCHING CHARACTERISTICS over operating range unless otherwise specified.

AC CHARACTERISTICS-Read Only Operation (Notes 1– 2)

Parameter Symbols		Parameter Description		Am28F010				Unit
JEDEC	Standard			–90 –95	–120 —	–150 —	–200 —	
t_{AVAV}	t_{RC}	Read Cycle Time	Min.	90	120	150	200	ns
			Max.					
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min.					
			Max.	90	120	150	200	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min.					
			Max.	90	120	150	200	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min.					
			Max.	40	50	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z	Min.	0	0	0	0	ns
			Max.					
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z	Min.					
			Max.	25	30	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	Min.	0	0	0	0	ns
			Max.					
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z	Min.					
			Max.	25	30	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change	Min.	0	0	0	0	ns
			Max.					
t_{WHGL}		Write Recovery Time before Read	Min.	6	6	6	6	µs
			Max.					

Notes:

1. Output Load (except Am28F010-95): 1 TTL gate and C_L = 100 pF, Input Rise and Fall Times: ≤ 10 ns, Input Pulse levels: 0.45 to 2.4 V, Timing Measurement Reference Level - Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. The Am28F010-95 Output Load: 1 TTL gate and C_L = 30 pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0 to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.

AC CHARACTERISTICS-Write/Erase/Program Operations (Notes 1– 4)

Parameter Symbols				Am28F010				
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time	Min. Max.	90	120	150	200	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min. Max.	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min. Max.	45	50	60	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min. Max.	45	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min. Max.	10	10	10	10	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	Min. Max.	6	6	6	6	µs
t_{GHWL}		Read Recovery Time before Write	Min. Max.	0	0	0	0	µs
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	Min. Max.	0	0	0	0	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min. Max.	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min. Max.	45	50	50	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min. Max.	20	20	20	20	ns
t_{WHWH1}		Duration of Programming Operation	Min. Max.	10 25	10 25	10 25	10 25	µs
t_{WHWH2}		Duration of Erase Operation	Min. Max.	9.5 10.5	9.5 10.5	9.5 10.5	9.5 10.5	ms
t_{EHVP}		Chip Enable Set-Up Time to V_{PP} Ramp	Min. Max.	100	100	100	100	ns
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW	Min. Max.	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time	Min. Max.	2	2	2	2	µs
t_{VPPR}		V_{PP} Rise Time	Min. Max.	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time	Min. Max.	500	500	500	500	ns

Notes:

1. Read timing characteristics during read/write operations are the same as durng read-only operations. Refer to AC Characteristics for Read Only operations.
2. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the Write Pulse Width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.
3. All devices except Am28F010-95. Input Rise and Fall times: $\leq$ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V
4. Am28F010-95. Input Rise and Fall times: $\leq$ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V
   Timing Measurement Reference Level: Inputs and Outputs: 1.5 V

PRELIMINARY

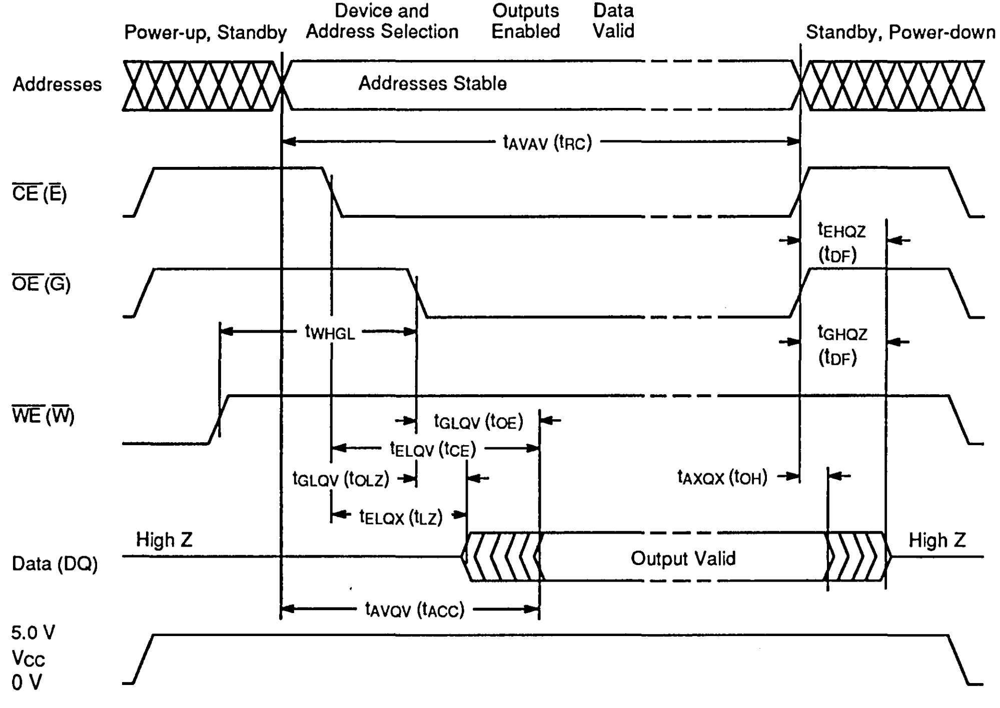


Figure 5. AC Waveforms for Read Operations

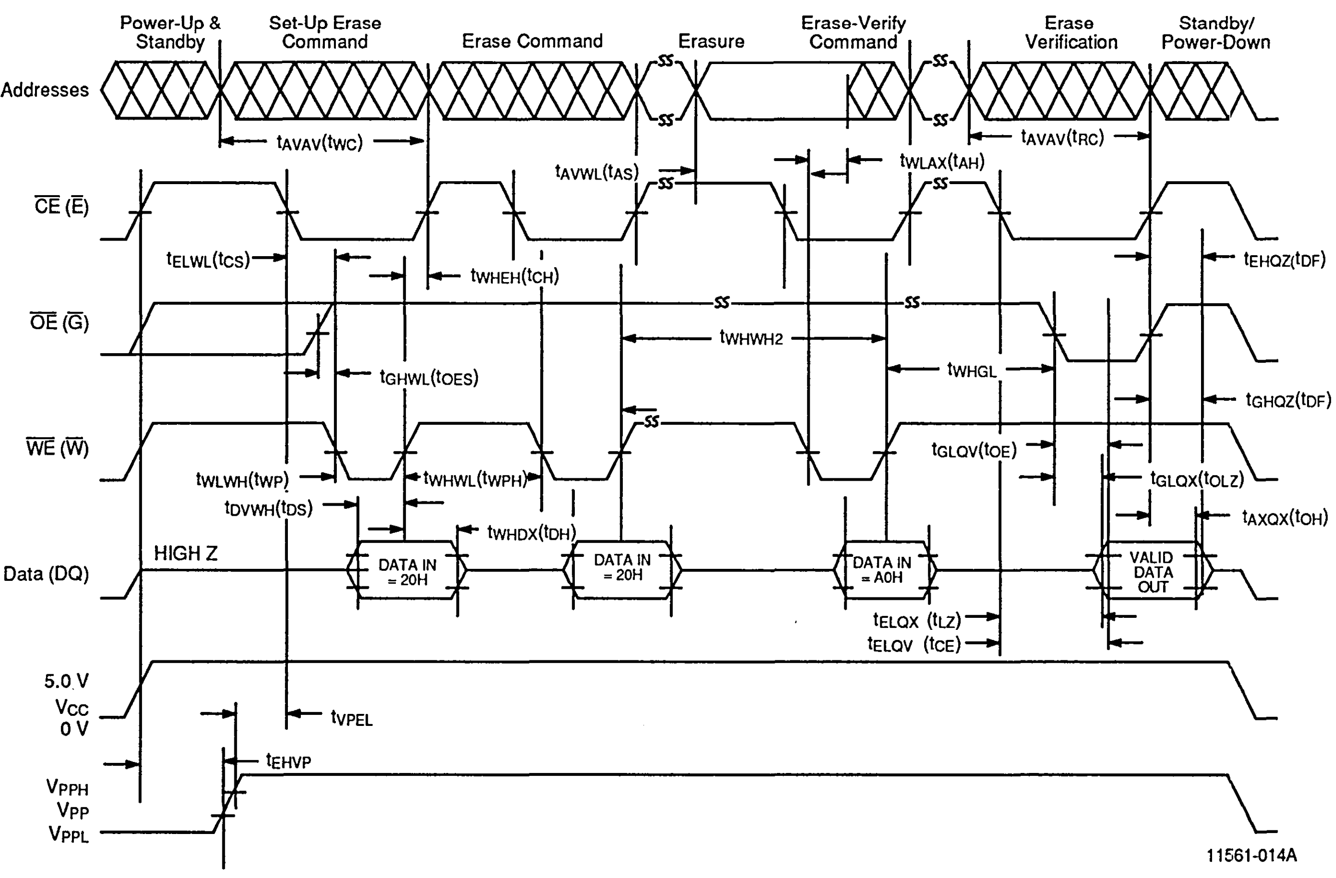


Figure 6. A.C. Waveforms for Erase Operations

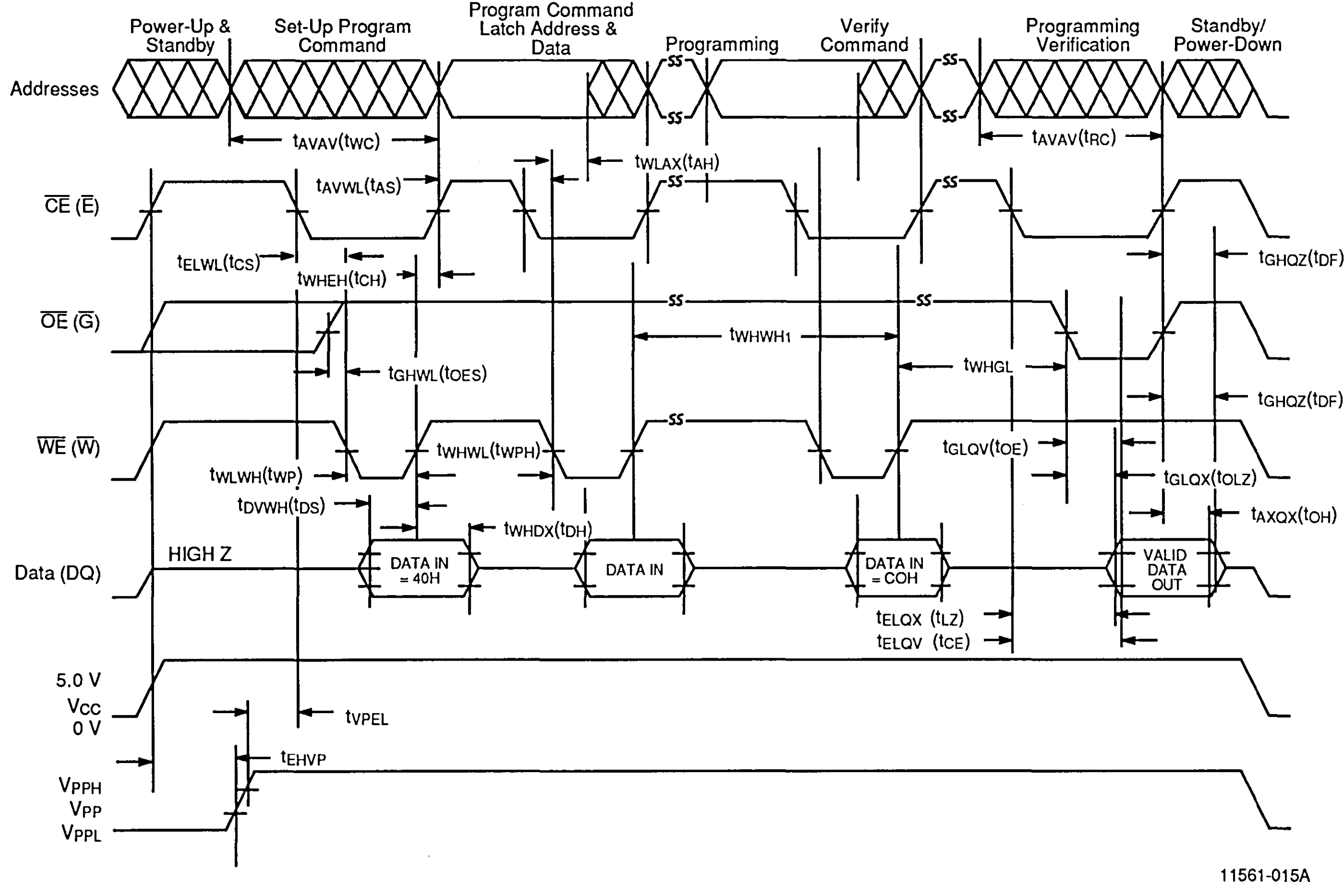
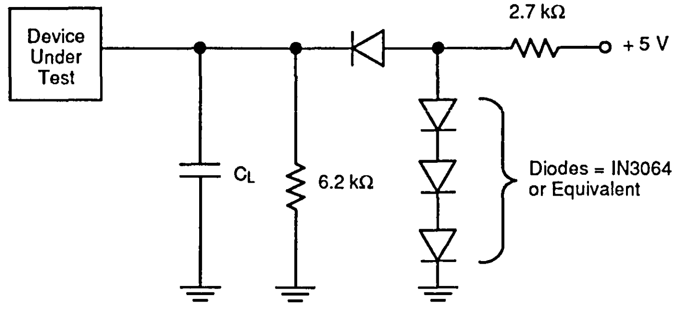


Figure 7. A.C. Waveforms for Programming Operations

SWITCHING TEST CIRCUIT



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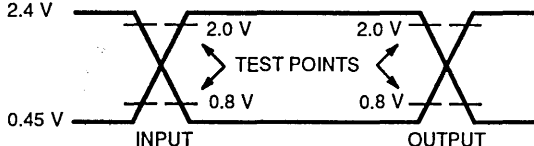
C_L = 100 pF including jig capacitance (30 pF for Am28F010-95)

SWITCHING TEST WAVEFORMS



3 V
0 V
1.5 ← TEST POINTS → 1.5
INPUT
OUTPUT

All Devices Except Am28F010-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.

For Am28F010-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.

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ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Chip Erase Time		0.5 (Note 1)	10	S	Excludes 00H programming prior to erasure
Chip Programming Time		2 (Note 1)	24	S	Excludes system-level overhead
Erase/Program Cycles					
Am28F010-95C4JC	10,000			Cycles	
Am28F010-95C3JC	1,000			Cycles	

Note:

1. 25°C, 12V V_{PP}

LATCHUP CHARACTERISTICS

	Min.	Max.
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A_9 and V_{PP})	– 1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	– 1.0 V	V_{CC} + 1.0 V
Current	– 100 mA	+ 100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

Advance Information

Am28F020

Advanced Micro Devices

65,536 x 8-Bit CMOS Flash Memory

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 90 ns maximum access time
- **Low power consumption**
  - 30 mA maximum active current
  - 100 µA maximum standby current
- **Compatible with JEDEC-standard byte-wide 32-Pin E²PROM pinouts**
  - 32-pin DIP
  - 32-pin PLCC
- **10,000 erase/program cycles**
- **Program and erase voltage 12.0 V +5%**
- **Latch-up protected to 100 mA from –1 V to V_{CC} +1 V**
- **Flasherase™ Electrical Bulk Chip-Erase**
  - Two second typical chip-erase
- **Flashrite™ programming**
  - 10 µs typical byte-program
  - Less than 3 seconds typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell

GENERAL DESCRIPTION

The Am28F020 is a 2 Megabit "Flash" electrically erasable, electrically programmable read only memory organized as 256K bytes of 8 bits each. The Am28F020 is packaged in 32-pin PDIP and PLCC versions. The device is also offered in ceramic DIP and LCC packages. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers.

The standard Am28F020 offers access times as fast as 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F020 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F020 uses a command register to manage this functionality, while maintaining a standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

AMD's Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F020 uses a 12.0 V+5% V_{PP} supply to perform the Flasherase and Flashrite algorithms.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from –1 V to V_{CC}+1 V.

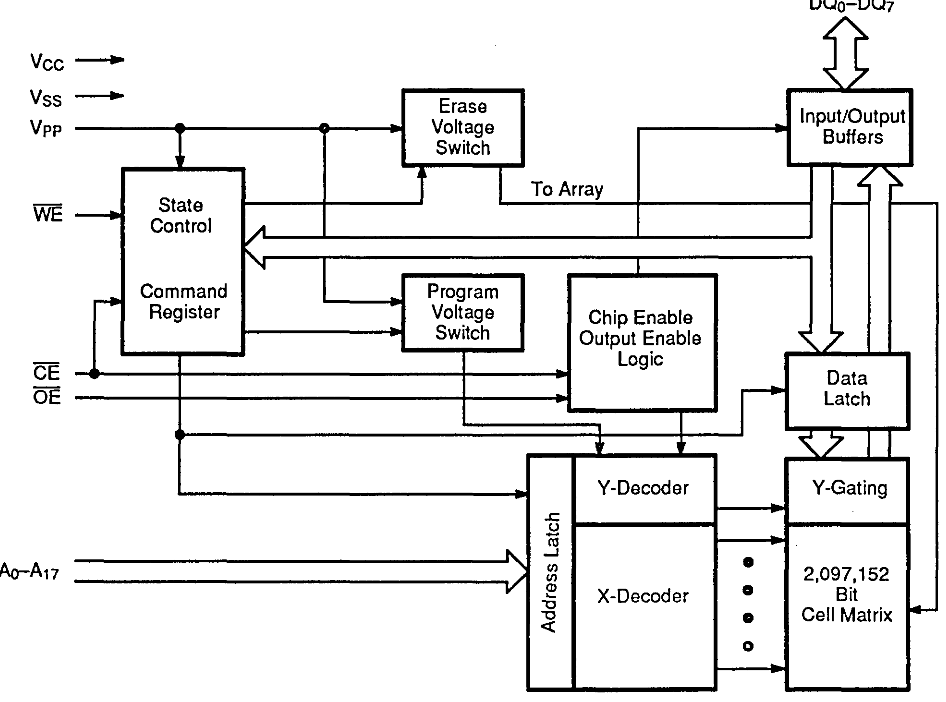
The Am28F020 is byte programmable using 10 ms programming pulses in accordance with AMD's Flashrite programming algorithm. The typical room temperature programming time of the Am28F020 is less than three seconds. The entire chip is bulk erased using 10ms erase pulses according to AMD's Flasherase algorithm. Typical erasure at room temperature is accomplished in less than two seconds. The windowed package and the 15–20 minutes required for EPROM erasure using ultraviolet light are eliminated.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F020 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

AMD's Flash technology combines years of EPROM and E²PROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F020 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

Publication# 14727 Rev. A Amendment/0
Issue Date: June 1990

BLOCK DIAGRAM



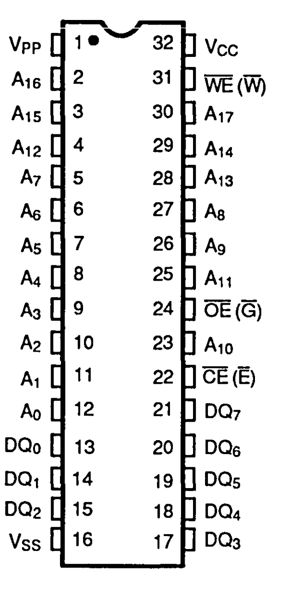
14727-001A

PRODUCT SELECTOR GUIDE

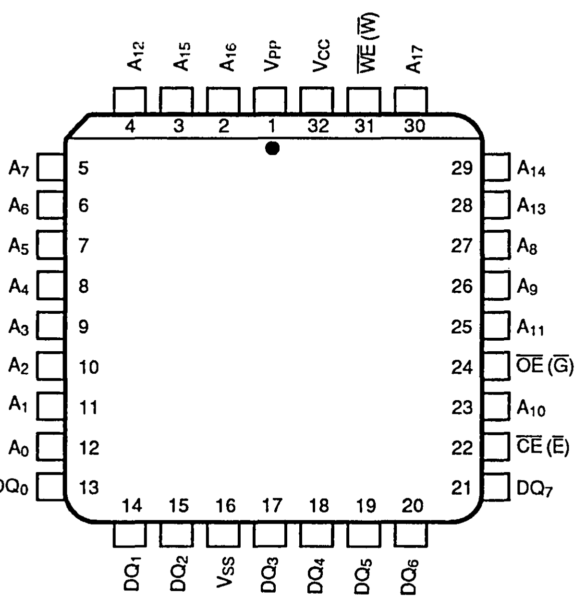
Family Part No.	Am28F020			
Ordering part No: + 10% V_{CC} Tolerance	–90	–120	–150	–200
+ 5% V_{CC} Tolerance	–95	—	—	—
Max Access Time (ns)	90	120	150	200
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	120	150	200
$\overline{OE}$ ($\overline{G}$) Access (ns)	40	50	65	75

CONNECTION DIAGRAMS

DIP

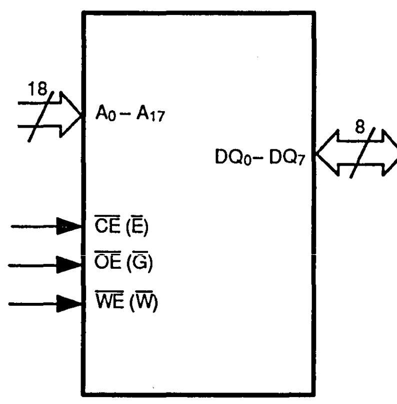


LCC/PLCC



Note: Pin 1 is marked for orientation

LOGIC SYMBOL



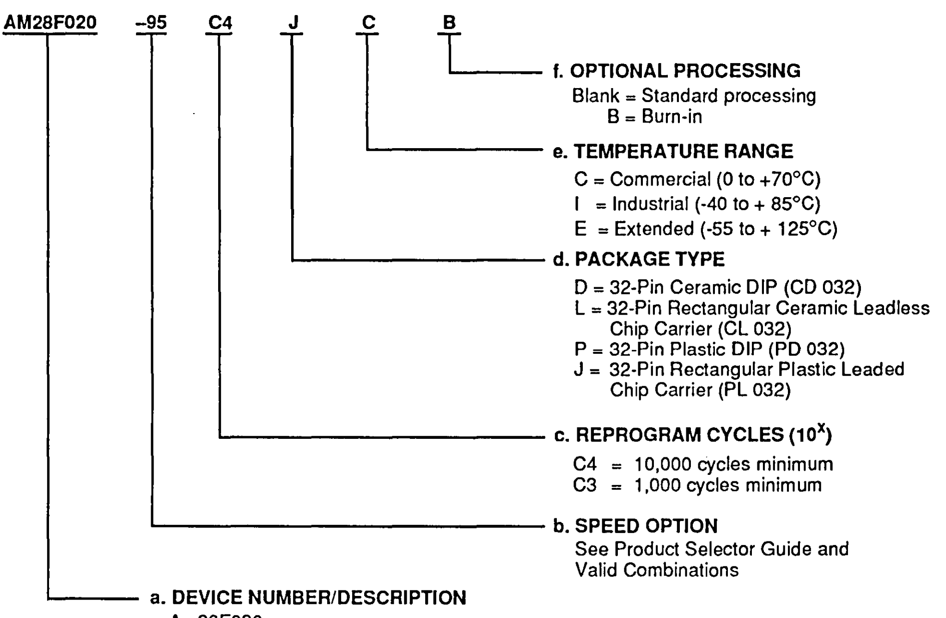
PIN DESCRIPTION

Symbol	Functional Description
$A_0 - A_{17}$	Address Inputs for memory locations. Internal latches hold addresses during write cycles.
$DQ_0 - DQ_7$	Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.
$\overline{CE}$ ($\overline{E}$)	The Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.
$\overline{OE}$ ($\overline{G}$)	The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.
$\overline{WE}$ ($\overline{W}$)	The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the ap propriate data is latched on the rising edge of the pulse.
V_{PP}	Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC}$ +2V.
V_{CC}	Power supply for device operation. (5.0V + 5% or 10%)
V_{SS}	Ground
NC	No Connect-corresponding pin is not connected internally to the die.

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Reprogram Cycles
d. Package Type
e. Temperature Range
f. Optional Processing



Valid Combinations	
AM28F020-95 AM28F020-90 AM28F020-120 AM28F020-150 AM28F020-200	C4DC, C4DCB, C4DI, C4DIB, C4DE, C4DEB, C4LC, C4LCB, C4LI, C4LIB, C4LE, C4LEB, C4PC, C4PI, C4JC, C4JI, C3DC, C3DCB, C3DI, C3DIB, C3DE, C3DEB, C3LC, C3LCB, C3LI, C3LIB, C3LE, C3LEB, C3PC, C3PI, C3JC, C3JI

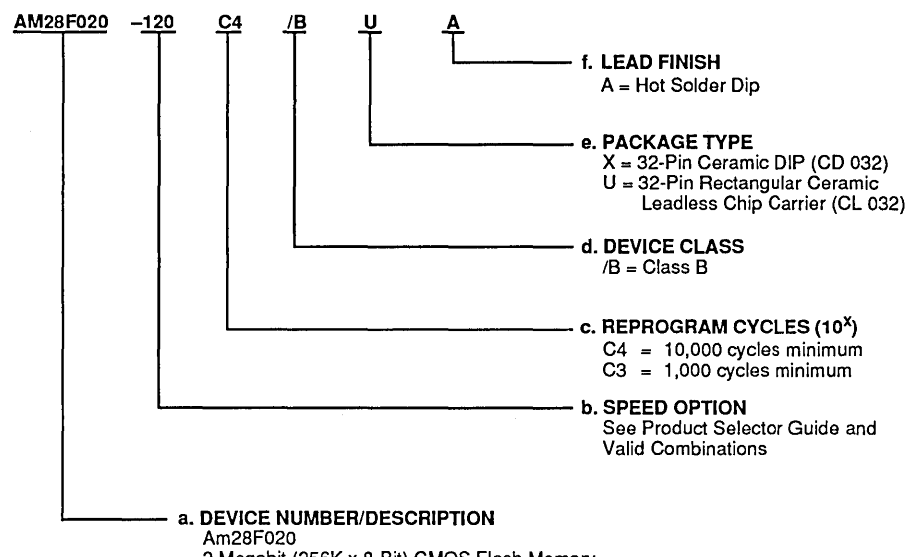
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

a. Device Number
b. Speed Option
c. Reprogram cycles
d. Device Class
e. Package Type
f. Lead Finish



Valid Combinations	
AM28F020-120 AM28F020-150 AM28F020-200	C4/BXA, C4/BUA C3/BXA, C3/BUA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

BASIC PRINCIPLES

The Am28F020 uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0V + 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F020 functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F020's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F020 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Erase Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note:
The Flash memory array must be completely programmed prior to erasure. Refer to the Flasherase Algorithm.

1. **Set-up Erase:** Write the Set-up Erase command to the command register.
2. **Erase:** Write the Erase command (same as Set-up Erase command) to the command register again. The second command initiates the erase operation. The system software routines must now time-out the erase pulse width (10 ms) prior to issuing the Erase-verify command.
3. **Erase-verify:** Write the Erase-verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFH data (Byte erased). After successful data verification the Erase-verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Programming Sequence

A three step command sequence (a two-cycle Program command and one cycle Verify command) is required to program a byte of the Flash array. Refer to the Flashrite Algorithm.

1. **Set-up Program:** Write the Set-up Program command to the command register.
2. **Program:** Write the Program command to the command register with the appropriate Address and Data. The system software routines must now time-out the program pulse width (10 μs) prior to issuing the Program-verify command.
3. **Program-verify:** Write the Program-verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times.

FUNCTIONAL DESCRIPTION

Description Of User Modes

Table 1. Am28F020 User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A_0	A_9	I/O
Read-Only	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	A_0	A_9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (2AH)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A_0	A_9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A_0	A_9	D_{IN} (Note 6)

Legend:
X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2V$, See DC Characteristics for voltage levels of V_{PPH}, $0V < An < V_{CC} + 2V$, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC} + 2.0V$. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.
2. Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.
3. $11.5 \leq V_{ID} \leq 13.0V$
4. Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.
5. With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).
6. Refer to Table 3 for valid D_{IN} during a write operation.
7. All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A_9 and A_0 must be held at V_{IL}.

READ ONLY MODE

$V_{PP} < V_{CC} + 2V$

Command Register Inactive

Read

The Am28F020 functions as a read only memory when $V_{PP} < V_{CC} + 2V$. The Am28F020 has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC} - t_{OE}$).

Standby Mode

The Am28F020 has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5V$), consumes less than 100mA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A PROM Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5V to 13.0V) on address A_9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to V_{CC} + 2.0V while using this Auto select mode. Byte 0 ($A_0 = V_{IL}$) represents the manufacturer code and byte 1 ($A_0 = V_{IH}$) the device identifier code. For the Am28F020 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ_7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F020 Auto Select Code

Type	A_0	Code (HEX)	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	2A	1	0	1	0	1	0	1	0

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%

Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

Register bits $R_7 - R_0$ correspond to the data inputs $DQ_7 - DQ_0$ (Refer to Table 3). Register bits $R_7 - R_5$ store the command data. All register bits R_4 to R_0 must be zero. The only exceptions are: the reset command, when FFH is written to the register and Auto select, when 90H or 80H is written to the register.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 4 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Wait 6µs before reading the first accessed address location. All subsequent Read operations take t_{ACC}. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Command Register

Data Input/Output	DQ_7	DQ_6	DQ_5	DQ_4	DQ_3	DQ_2	DQ_1	DQ_0
Command Register	R_7	R_6	R_5	R_4	R_3	R_2	R_1	R_0
Data/Commands*	X	X	X	X	X	X	X	X

* **Notes:**

1. See Table 4 Am28F020 Command Definitions
2. X = Appropriate Data or Register Commands

Table 4. Am28F020 Command Definitions

Command	First Bus Cycle Operation (Note 1)	First Bus Cycle Address (Note 2)	First Bus Cycle Data (Note 3)	Second Bus Cycle Operation (Note 1)	Second Bus Cycle Address (Note 2)	Second Bus Cycle Data (Note 3)
Read Memory (Note 6)	Write	X	00H	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/2AH
Set-up Erase/Erase (Note 4)	Write	X	20H	Write	X	20H
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Set-up Program/Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Reset	Write	X	FFH	Write	X	FFH

Notes:

1. Bus operations are defined in Table 1.
2. RA = Address of the memory location to be read.
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
3. RD = Data read from location RA during read operation.
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. Figure 1 illustrates the Flasherase Electrical Erase Algorithm.
5. Figure 2 illustrates the Flashrite Programming Algorithm.
6. Wait 6µs after first Read command before accessing the data. When the second bus command is a Read command, all subsequent Read operations take t_{ACC}.

Erase Sequence

Set-up Erase/Erase Commands

Set-up Erase

Set-up Erase is the first of a two-cycle erase command. It is a command-only operation that stages the device for bulk chip erase. The array contents are not altered with this command. 20H is written to the command register in order to perform the Set-up Erase operation.

Erase

The second two-cycle erase command initiates the bulk erase operation. You must write the Erase command (20H) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-verify) to the register.

This two step sequence of the Set-up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, chip erasure can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:
The Flash memory device must be fully programmed to 00H data prior to erasure. This equalizes the charge on all memory cells ensuring reliable erasure.

Erase-verify Command

The erase operation erases all bytes of the array in parallel. After the erase operation, all bytes must be sequentially verified. The Erase-verify operation is initiated by writing A0H to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-verify operation, the Am28F020 applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are properly erased.

Verify Next Address

You must write the Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$. The process continues for each byte in

the memory array until a byte does not return FFH data or all the bytes in the array are accessed and verified.

If an address is not verified to FFH data, the entire chip is erased again (refer to Set-up Erase/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The device is now ready to be programmed. At this point, the verification operation is terminated by writing a valid command (e.g. Program set-up) to the command register. Figure 1 and Table 5, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note:
The erase-verify command must be written to the register in order to terminate the erase operation. During the erase operations, the local microprocessor must be dedicated to run software timing routines (erase in 10ms) as specified in AMD's Flasherase algorithm.

Should a system interrupt occur during an erase operation, always write the Erase-verify command prior to executing an interrupt sequence.

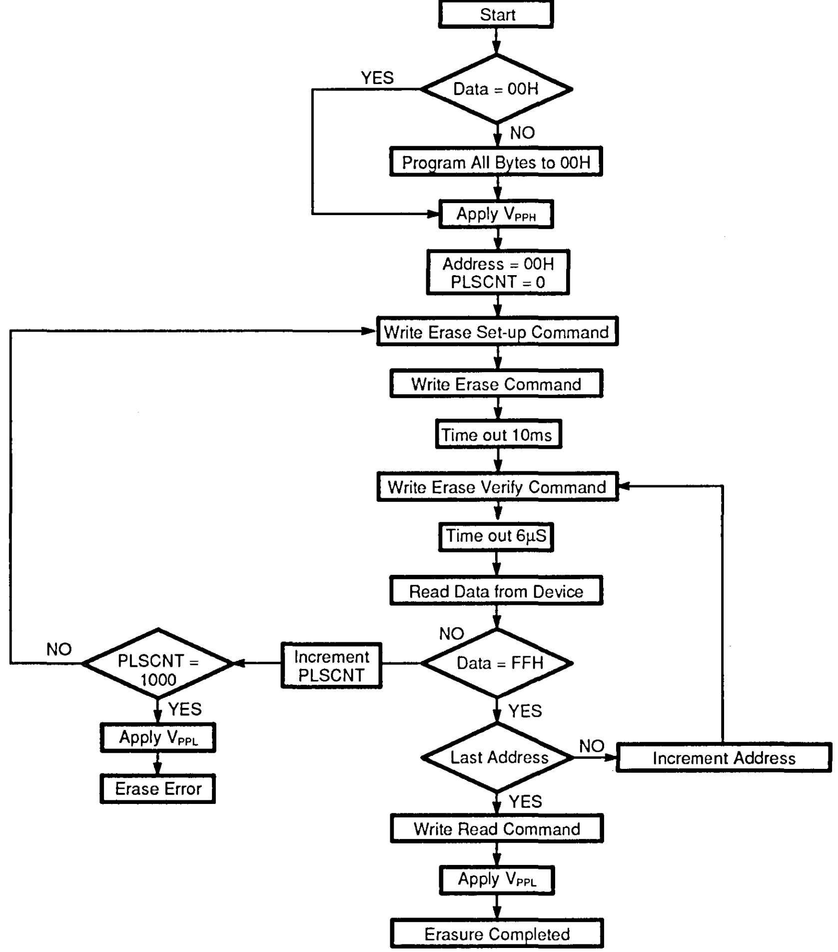


Figure 1. Flasherase Electrical Erase Algorithm

Flasherase Electrical Erase Algorithm

This Flash memory device erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the array. Erasure begins with a read of the memory contents. The Am28F020 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

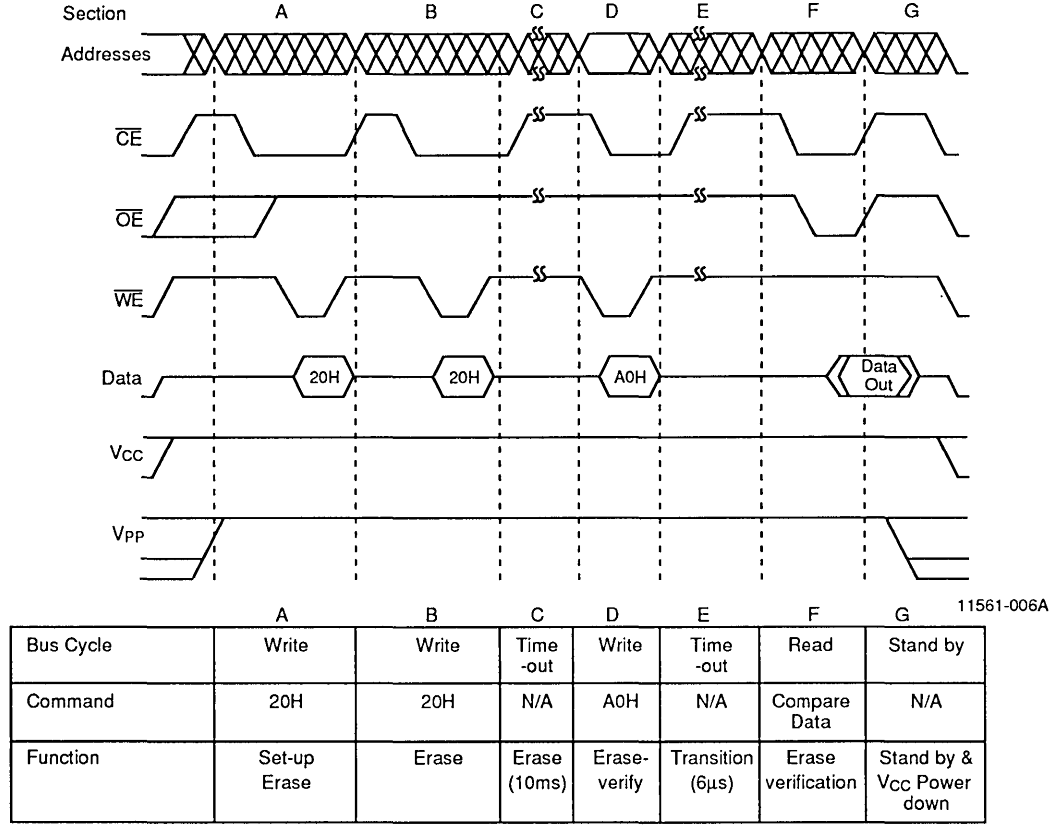
Should the device be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished using the Flashrite programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. If a byte fails to verify, the device is erased again. With each erase operation, an increasing number of bytes verify to the erased state. Typically, devices are erased in less than 200 pulses (2 seconds). Erase efficiency may be improved by storing the address of the last byte that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. A total of 1000 erase operations are allowed per reprogram cycle, which corresponds to approximately 10 seconds of cumulative erase time. Erasure typically occurs in one second. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 1 illustrates the electrical erase algorithm.

Table 5. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) **Note:** Use Flashrite programming algorithm (Figure 2) for programming.
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Set-Up Erase	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6μs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Read	Data = 00H, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0V.
2. Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.
3. The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	20H	20H	N/A	A0H	N/A	Compare Data	N/A
Function	Set-up Erase	Erase	Erase (10ms)	Erase-verify	Transition (6μs)	Erase verification	Stand by & V_{CC} Power down

Figure 2. A.C. Waveforms For Erase Operations

Analysis Of Erase Timing Waveform

Note:

This analysis does not include the requirement to program the entire array to 00H data prior to erasure. Refer to the Flasherase algorithm.

Set-up Erase/Erase

This analysis illustrates the use of two-cycle erase commands (section A&B). The first erase command (20H) is a set-up command and does not affect the array data (section A). The second erase command (20H) initiates the erase operation (section B) on the rising edge of this WE pulse. All bytes of the memory array are erased in parallel. No address information is required.

The erase pulse occurs in section C.

Time-out

A software timing routine (10ms duration) must be initiated on the rising edge of the WE pulse of section B.

Erase-verify

Upon completion of the erase software timing routine, the microprocessor must write the Erase-verify command (A0H). This command terminates the erase operation on the rising edge of the WE pulse (section D). The Erase-verify command also stages the device for data verification (section F).

After each erase operation each byte must be verified. The byte address to be verified must be supplied with the Erase-verify command (section D). Addresses are latched on the falling edge of the WE pulse.

Another software timing routine (6ms duration) must be executed to allow for generation of internal voltages for margin checking and read operation (section E).

During Erase-verification (section F) each address that returns FFH data is successfully erased. Each address of the array is sequentially verified in this manner by repeating sections D thru F until the entire array is verified or an address fails to verify. Should an address location fail to verify to FFH data, erase the device again. Repeat sections A thru F. Resume verification (section D) with the failed address.

Each data change sequence allows the device to use up to 1,000 erase pulses to completely erase. Typically 200 erase pulses are required.

Notes:

1. All address locations must be programmed to 00H prior to erase. This equalizes the charge on all memory cells and ensures reliable erasure.

2. The erase verify command must be written to terminate the erase operation. Should a system interrupt occur during an erase operation, always write the erase-verify command prior to executing an interrupt sequence.

Programming Sequence

Set-up Program/Program Command

Set-up Program

The Am28F020 is programmed byte by byte. Bytes may be programmed sequentially or at random. Set-up Program is the first of a two-cycle program command. It stages the device for byte programming. The Set-up Program operation is performed by writing 40H to the command register.

Program

Only after the program set-up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-verify command to terminate the programming operation. This two step sequence of the Set-up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte just programmed must be verified.

Write C0H into the command register in order to initiate the Program-verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-verify operation stages the device for verification of the last byte programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-verify operation, the Am28F020 applies an internally generated margin voltage to the addressed byte. A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte location. Should the byte fail to verify, reprogram (refer to Set-up Program/Program). Figure 3 and Table 6 indicate how instructions are combined with the bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Flashrite Programming Algorithm

The Am28F020 Flashrite programming algorithm employs an interactive closed loop flow to program data byte by byte. Bytes may be programmed sequentially or at random. The Flashrite programming algorithm uses 10 microsecond programming pulses. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 3 and Table 6 illustrate the programming algorithm.

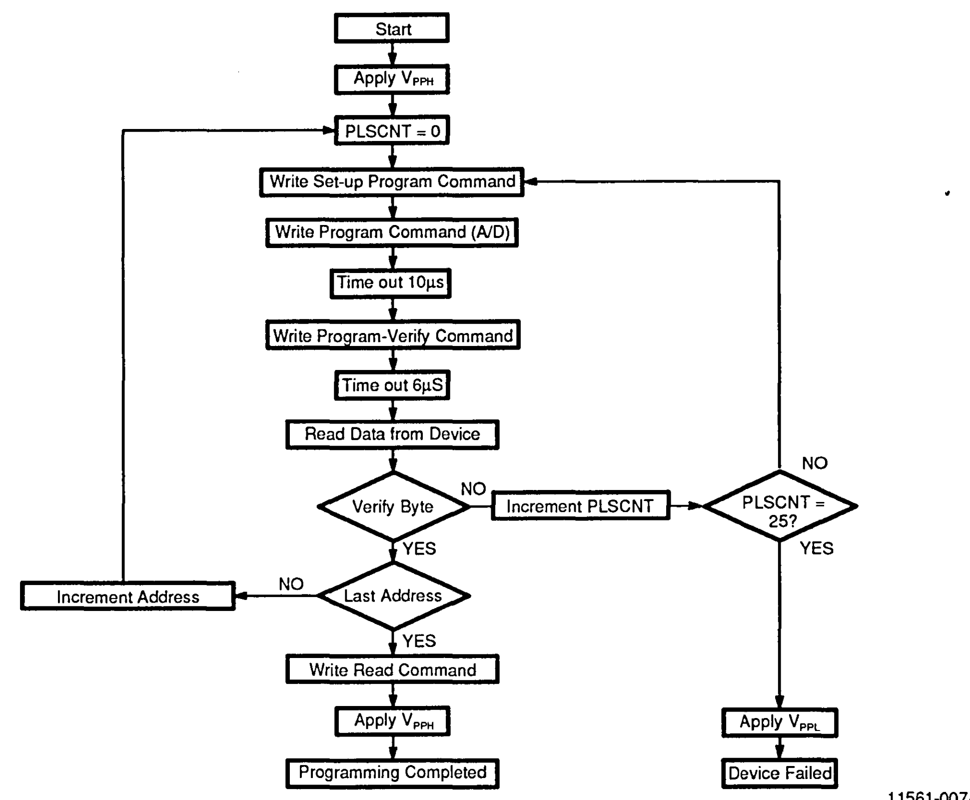


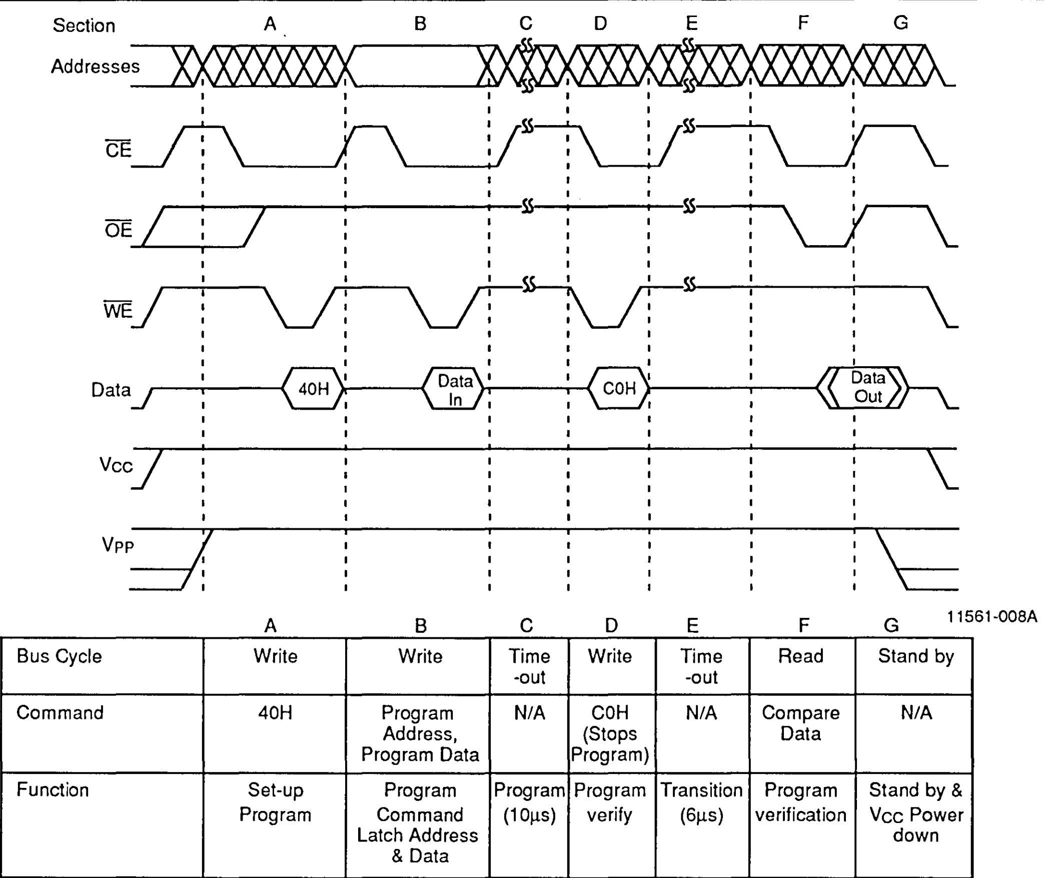
Figure 3. Flashrite Programming Algorithm

Table 6. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Set-Up Program	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Read	Data = 00H, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0V.
2. Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	40H	Program Address, Program Data	N/A	C0H (Stops Program)	N/A	Compare Data	N/A
Function	Set-up Program	Program Command Latch Address & Data	Program (10µs)	Program verify	Transition (6µs)	Program verification	Stand by & V_{CC} Power down

Figure 4. A.C. Waveforms for Programming Operations

Analysis Of Program Timing Waveforms

Set-up Program/Program

Two-cycle write commands are required for program operations (section A&B). The first program command (40H) is a set-up command and does not affect the array data (section A). The second program command latches address and data required for programming on the falling and rising edge of $\overline{WE}$ respectively (section B). The rising edge of this $\overline{WE}$ pulse (section B) also initiates the programming pulse. The device is programmed on a byte by byte basis either sequentially or randomly.

The program pulse occurs in section C.

Time-out

A software timing routine (10ms duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Program-verify

Upon completion of the program timing routine, the microprocessor must write the program-verify command (C0H). This command terminates the programming operation on the rising edge of the $\overline{WE}$ pulse (section D). The program-verify command also stages the device for data verification (section F). Another software timing routine (6ms duration) must be executed to allow for generation of internal voltages for margin checking and read operations (section E).

During program-verification (section F) each byte just programmed is read to compare array data with original program data. When successfully verified, the next desired address is programmed. Should a byte fail to verify, reprogram the byte (repeat section A thru F). Each data change sequence allows the device to use up to 25 program pulses per byte. Typically, bytes are verified within one or two pulses.

Note:
The program-verify operation must be written to terminate the programming operation. Should a system interrupt occur during a programming operation, always write the program-verify command prior to executing an interrupt sequence.

Algorithm Timing Delays

There are four different timing delays associated with the Flasherase and Flashrite algorithms:

1. The first delay is associated with the V_{PP} rise-time when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on the V_{PP}, the delay required is proportional to the number of devices being erased and the 0.1mF/device. V_{PP} must reach its final value 100ns before commands are executed.
2. The second delay time is the erase time pulse width (10 ms). A software timing routine should be run by the local microprocessor to time out the delay. The erase operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the erase operation. To ensure proper device operation, write the Erase-verify operation after each pulse, or the device may continue to erase until the memory cells are driven into depletion (over-erasure). Should this happen the internal circuitry will no longer select unique addresses. A symptom of over-erasure is an error attempting to program the next time. Occasionally it is possible to recover over-erased devices by programming all of the locations with 00H data.
3. A third delay time is required for each programming pulse width (10 µs). The programming algorithm is interactive and verifies each byte after a program pulse. The program operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the programming operation.
4. A fourth timing delay associated with both the Flasherase and Flashrite algorithms is the write recovery time (6 µs). During this time internal circuitry is changing voltage levels from the erase/ program level to those used for margin verify and read operations. An attempt to read the device during this period will result in possible false data (it may appear the device is not properly erased or programmed).

Note:
Software timing routines should be written in machine language for each of the delays. Code written in machine language requires knowledge of the appropriate microprocessor clock speed in order to accurately time each delay.

Parallel Device Erasure

Many applications will use more than one Flash memory device. Total erase time may be minimized by implementing a parallel erase algorithm. Flash memories may erase at different rates. Therefore each device must be verified seperately. When a device is completely erased and verified use a masking code to prevent further erasure. The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-up Sequence

V_{CC} prior to V_{PP}

The Am28F020 powers-up in the Read only mode. In addition, the memory contents may only be altered after successful completion of a two step command sequence.

V_{PP} prior to V_{CC}

When V_{CC} = 0 V, the V_{PP} voltage is internally disabled from the device. Memory contents cannot be altered. With V_{PP} = 12 V, the Flash device resets to the Read mode when V_{CC} rises above 2 V.

Power supply sequencing is not required.

Reset Command

A reset command sequence is provided to initialize the Flash memory to a known state – Read mode. The Reset command sequence also provides the user with a means to safely abort the erase or program command sequences. Following either set-up command (erase or program) with two consecutive writes of FFH will safely abort the operation. Memory contents will not be altered. A valid command must then be written to place the device in the desired state.

If V_{PP} is left at high voltage during system resets, you must incorporate the device reset command into the hardware initialization code. This minimizes the potential for over erasure or programming if the device is in the middle of an erase or program operation during reset. Execute the reset command early in the initialization routine.

Auto Select Command

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Programming In-system

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A_9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F020 contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H. A read cycle from address 0001H returns the device code 2AH (See Table 2). To terminate the operation, it is necessary to write another valid command into the register (See Table 3).

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	
Ceramic Packages	– 65°C to +150°C
Plastic Packages	– 65°C to +125°C
Ambient Temperature with Power Applied	– 55°C to + 125°C
Voltage with Respect To Ground	
All pins except A_9 and V_{PP} (Note 1)	– 2.0V to 7.0V
V_{CC} (Note 1)	– 2.0V to 7.0V
A_9 (Note 2)	– 2.0V to 14.0V
V_{PP} (Note 2)	– 2.0V to 14.0V
Output Short Circuit Current (Note 3)	200mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A_9 and V_{PP} pins is –0.5V. During voltage transitions, A_9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A_9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

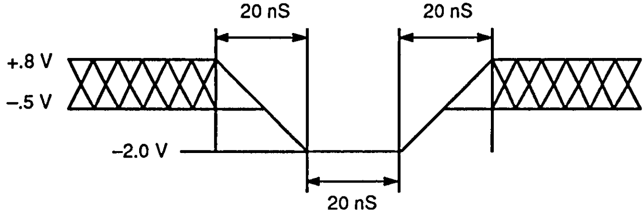
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (T_C)	0°C to +70°C
Industrial (I) Devices	
Case Temperature (T_C)	– 40°C to +85°C
Extended (E) Devices	
Case Temperature (T_C)	– 55°C to +125°C
Military (M) Devices	
Case Temperature (T_C)	– 55°C to +125°C
V_{CC} Supply Voltages	
V_{CC} for Am28F020-X5	+ 4.75V to +5.25V
V_{CC} for Am28F020-XX0	+ 4.50V to +5.50V
V_{PP} Supply Voltages	
Read	– 0.5V to +12.6V
Program, Erase, and Verify	+ 11.4V to +12.6V

MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



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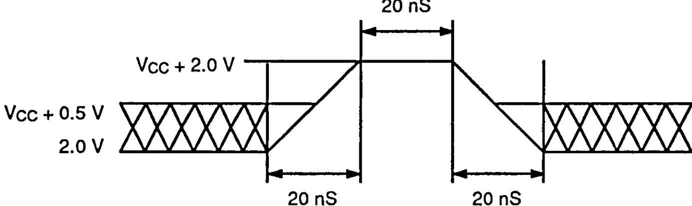
Maximum Negative Overshoot Waveform

Maximum Positive Input Overshoot



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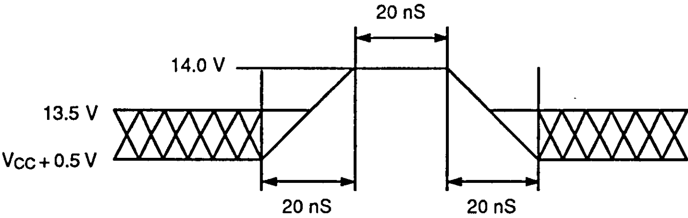
Maximum Positive Overshoot Waveform

Maximum V_{PP} Overshoot



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Maximum V_{PP} Overshoot Waveform

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted). (Notes 1–3)

DC CHARACTERISTICS-TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{IN} = V_{CC}$ or V_{SS}		+1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{OUT} = V_{CC}$ or V_{SS}		+1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max. $\overline{CE} = V_{IH}$		1.0	mA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ I_{OUT} = 0 mA, at 6 MHz		30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress		30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress		30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$		+1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$ $V_{PP} = V_{PPL}$		200 +1.0	µA
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress		30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress		50	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA $V_{CC} = V_{CC}$ Min.		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA $V_{CC} = V_{CC}$ Min.	2.4		V
V_{ID}	A_9 Auto Select Voltage	$A_9 = V_{ID}$	11.5	13.0	V
I_{ID}	A_9 Auto Select Current	$A_9 = V_{ID}$ Max. $V_{CC} = V_{CC}$ Max.		50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/Program are inhibited when $V_{PP} = V_{PPL}$	0.0	V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4	12.6	V

DC CHARACTERISTICS-CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{IN} = V_{CC}$ or V_{SS}		+ 1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max., $V_{OUT} = V_{CC}$ or V_{SS}		+ 1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max. $\overline{CE} = V_{IH}$		100	µA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max., $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ I_{OUT} = 0 mA, at 6 MHz		30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress		30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress		50	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$		+ 1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		200	µA
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress		30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress		30	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		V_{CC} – 0.5	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA $V_{CC} = V_{CC}$ Min.		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min.	0.85 V_{CC}		V
V_{OH2}		I_{OH} = –100 mA, $V_{CC} = V_{CC}$ Min.	V_{CC} –0.4		
V_{ID}	A_9 Auto Select Voltage	$A_9 = V_{ID}$	11.5	13.0	V
I_{ID}	A_9 Auto Select Current	$A_9 = V_{ID}$ Max. $V_{CC} = V_{CC}$ Max.		50	µA
V_{PPL}	V_{PP} during Read-Only Operations	**Note:** Erase/ Program are inhibited when $V_{PP} = V_{PPL}$	0.0	V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4	12.6	V

Notes:

1. **Caution:** the Am28F020 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.
2. I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.
3. Maximum active power usage is the sum of I_{CC} and I_{PP}.

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	8	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. Sampled, not 100% tested.
2. Test conditions $T_A = 25°C$, f = 1.0 MHz

SWITCHING CHARACTERISTICS over operating range unless otherwise specified.

AC CHARACTERISTICS-Read Only Operation (Notes 1– 2)

Parameter Symbols				Am28F020				
				–90	–120	–150	–200	
JEDEC	Standard	Parameter Description		–95	—	—	—	Unit
t_{AVAV}	t_{RC}	Read Cycle Time	Min. Max.	90	120	150	200	ns
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min. Max.	90	120	150	200	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min. Max.	90	120	150	200	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min.. Max.	40	50	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z	Min. Max.	0	0	0	0	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z	Min. Max.	25	30	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	Min. Max.	0	0	0	0	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z	Min. Max.	25	30	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change	Min. Max.	0	0	0	0	ns
t_{WHGL}		Write Recovery Time before Read	Min. Max.	6	6	6	6	µs

Note: in the rows for t_{ELQV}, t_{AVQV}, t_{GLQV}, t_{EHQZ} and t_{GHQZ} the values are printed on the Max. line; in the other rows they are on the Min. line.

Notes:

1. Output Load (except Am28F020-95): 1 TTL gate and C_L = 100 pF, Input Rise and Fall Times: ≤ 10 ns, Input Pulse levels: 0.45 to 2.4 V, Timing Measurement Reference Level - Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. The Am28F020-95 Output Load: 1 TTL gate and C_L = 30 pF
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0 to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.

AC CHARACTERISTICS-Write/Erase/Program Operations (Notes 1– 4)

Parameter Symbols				Am28F020				
JEDEC	Standard	Parameter Description		–90 –95	–120 —	–150 —	–200 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time	Min. Max.	90	120	150	200	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min. Max.	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min. Max.	45	50	60	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min. Max.	45	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min. Max.	10	10	10	10	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	Min. Max.	6	6	6	6	µs
t_{GHWL}		Read Recovery Time before Write	Min. Max.	0	0	0	0	µs
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	Min. Max.	0	0	0	0	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min. Max.	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min. Max.	45	50	50	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min. Max.	20	20	20	20	ns
t_{WHWH1}		Duration of Programming Operation	Min. Max.	10 25	10 25	10 25	10 25	µs
t_{WHWH2}		Duration of Erase Operation	Min. Max.	9.5 10.5	9.5 10.5	9.5 10.5	9.5 10.5	ms
t_{EHVP}		Chip Enable Set-Up Time to V_{PP} Ramp	Min. Max.	100	100	100	100	ns
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW	Min. Max.	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time	Min. Max.	2	2	2	2	µs
t_{VPPR}		V_{PP} Rise Time	Min. Max.	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time	Min. Max.	500	500	500	500	ns

Notes:

1. Read timing characteristics during read/write operations are the same as durng read-only operations. Refer to AC Characteristics for Read Only operations.
2. Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the Write Pulse Width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.
3. All devices except Am28F020-95. Input Rise and Fall times: $\leq$ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V
4. Am28F020-95. Input Rise and Fall times: $\leq$ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V
   Timing Measurement Reference Level: Inputs and Outputs: 1.5 V

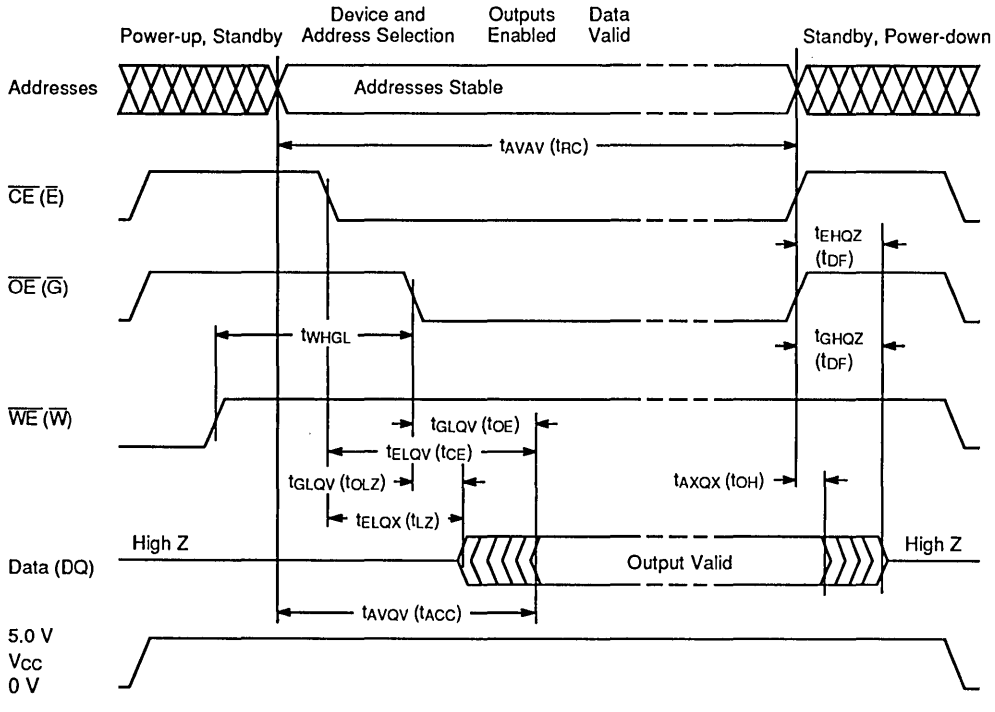


Figure 5. AC Waveforms for Read Operations

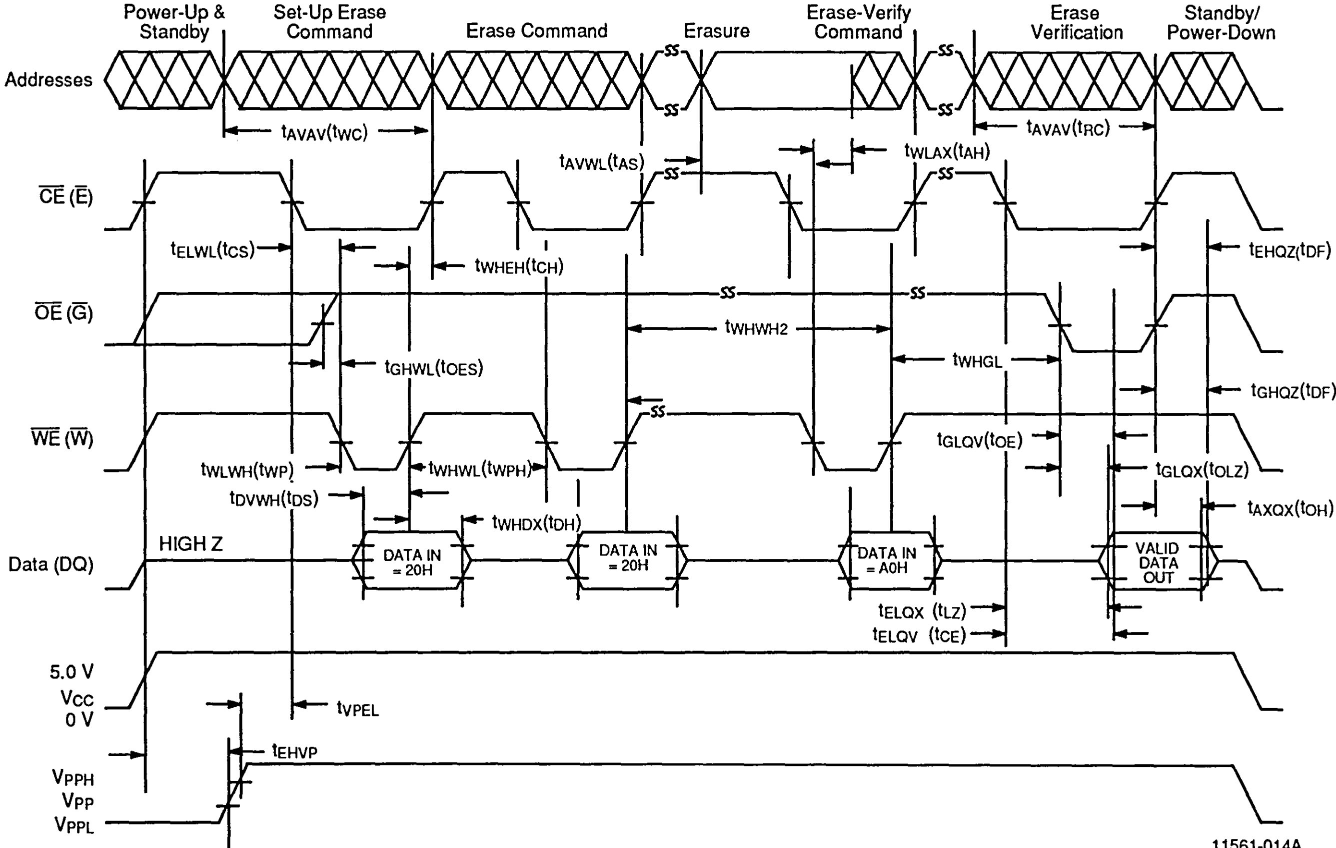


Figure 6. A.C. Waveforms for Erase Operations

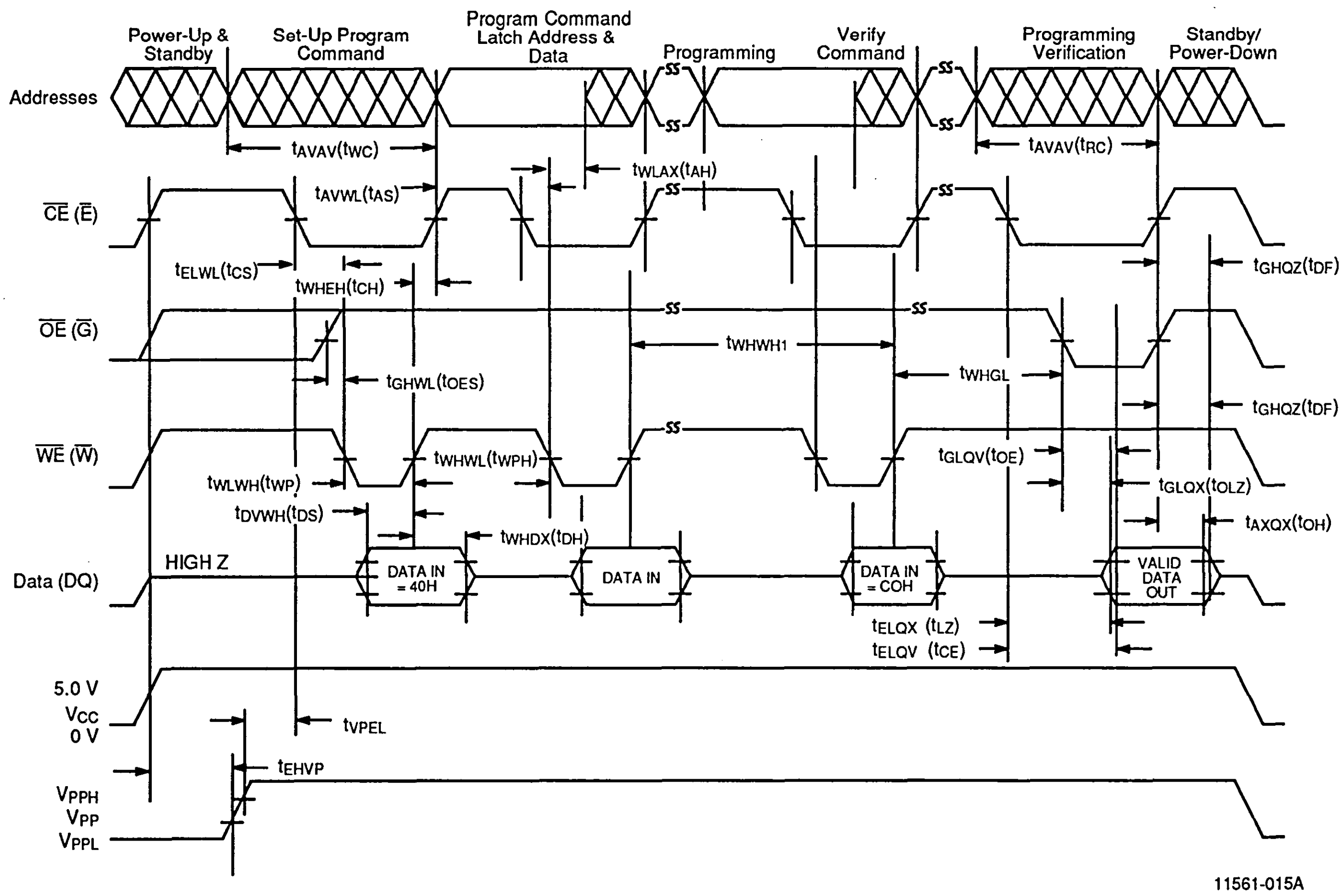
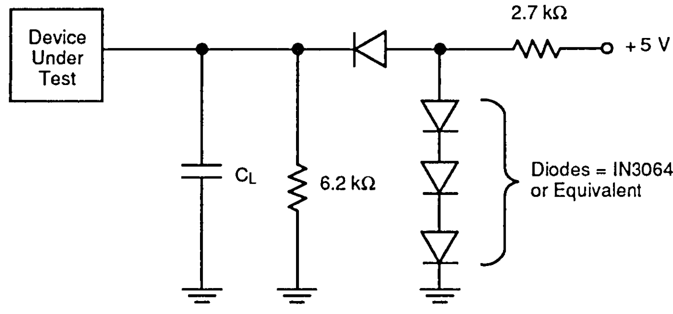


Figure 7. A.C. Waveforms for Programming Operations

SWITCHING TEST CIRCUIT



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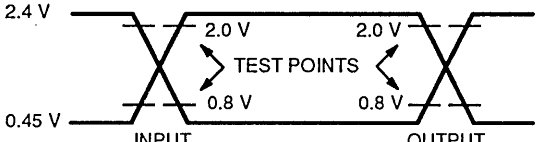
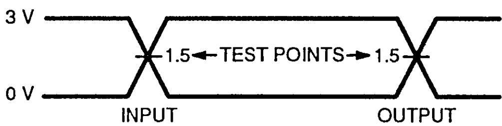
C_L = 100 pF including jig capacitance (30 pF for Am28F020-95)

SWITCHING TEST WAVEFORMS



All Devices Except Am28F020-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.



For Am28F020-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are ≤ 10 ns.

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ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min.	Typ.	Max.		
Chip Erase Time		0.2 (Note 1)	20	S	Excludes 00H programming prior to erasure
Chip Programming Time		3 (Note 1)	36	S	Excludes system-level overhead
Erase/Program Cycles					
Am28F020-95C4JC	10,000			Cycles	
Am28F020-95C3JC	1,000			Cycles	

Note:

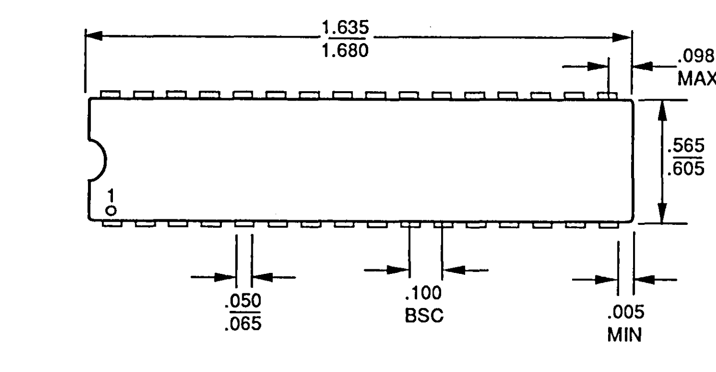
1. 25°C, 12V V_{PP}

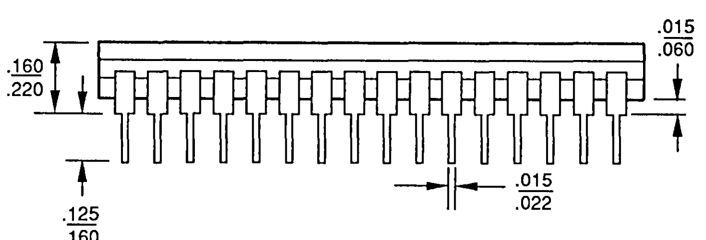
LATCHUP CHARACTERISTICS

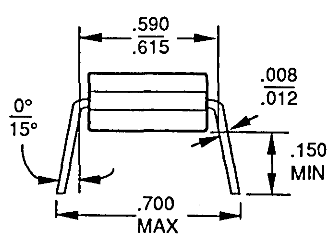
	Min.	Max.
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A_9 and V_{PP})	– 1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	– 1.0 V	V_{CC} + 1.0 V
Current	– 100 mA	+ 100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

CHAPTER 6
Physical Dimensions

PHYSICAL DIMENSIONS*
CD 032**







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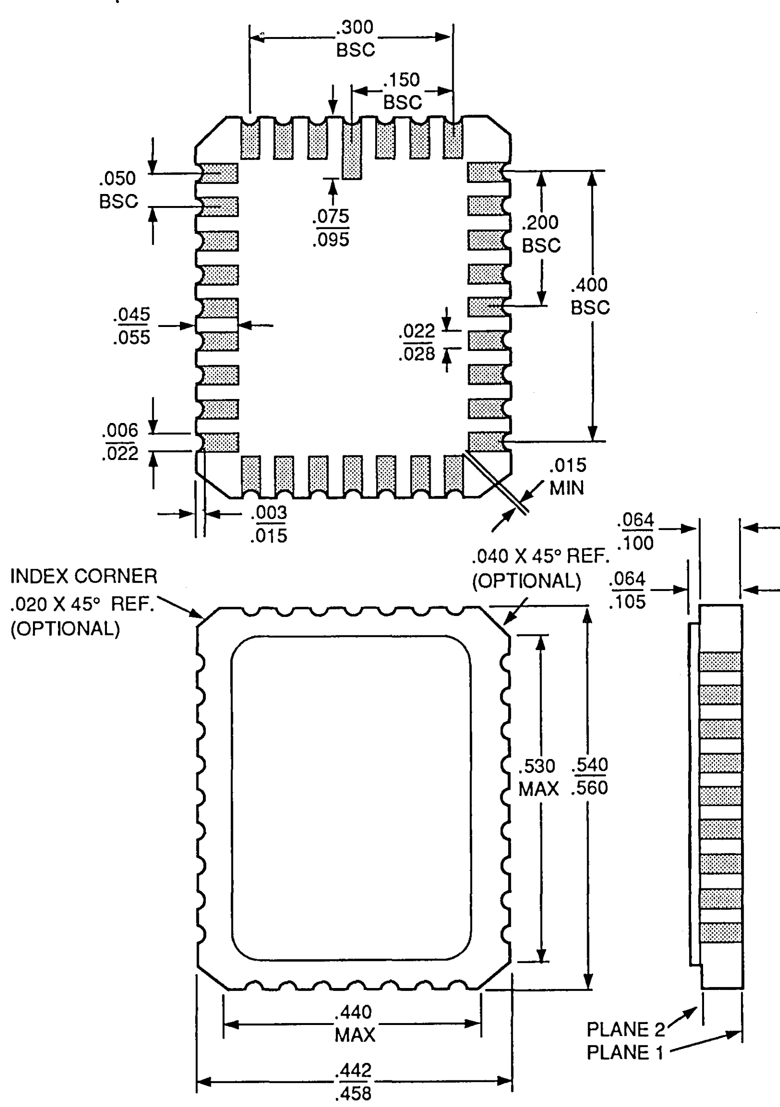
* For reference only. All measurements measured in inches. BSC is an ANSI standard for Basic Space Centering.
** Package in Development.


.300
BSC
.150
BSC
.050
BSC
.075
.095
.200
BSC
.400
BSC
.045
.055
.022
.028
.006
.022
.015
MIN
.003
.015
.064
.100
INDEX CORNER
.020 X 45° REF.
(OPTIONAL)
.040 X 45° REF.
(OPTIONAL)
.064
.105
.530
MAX
.540
.560
.440
MAX
.442
.458
PLANE 2
PLANE 1
14824A

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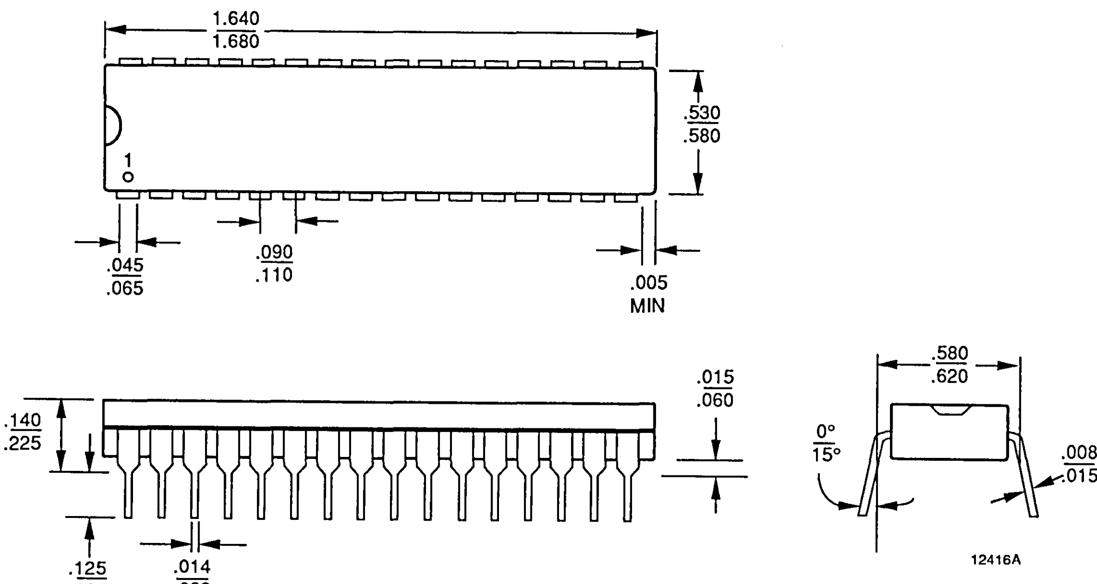
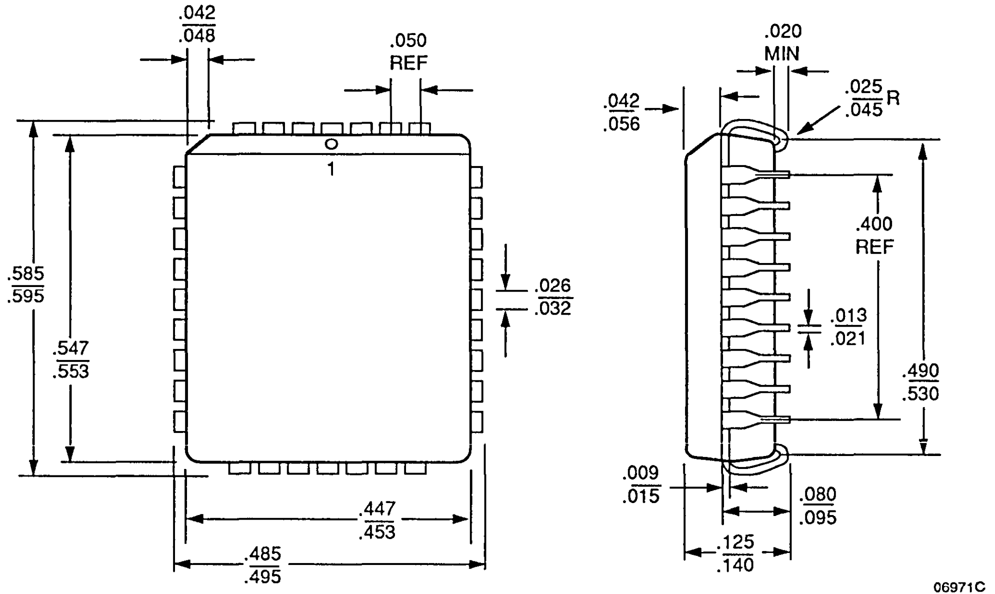


PL 032



Sales Offices

North American

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Woodland Hills	(818) 992-4155
CANADA, Ontario,	
Kanata	(613) 592-0060
Willowdale	(416) 224-5193
COLORADO	(303) 741-2900
CONNECTICUT	(203) 264-7800
FLORIDA,	
Clearwater	(813) 530-9971
Ft. Lauderdale	(305) 776-2001
Orlando (Longwood)	(407) 862-9292
GEORGIA	(404) 449-7920
ILLINOIS,	
Chicago (Itasca)	(708) 773-4422
Naperville	(708) 505-9517
KANSAS	(913) 451-3115
MARYLAND	(301) 381-3790
MASSACHUSETTS	(617) 273-3970
MICHIGAN	(313) 347-1522
MINNESOTA	(612) 938-0001
NEW JERSEY,	
Cherry Hill	(609) 662-2900
Parsippany	(201) 299-0002
NEW YORK,	
Liverpool	(315) 457-5400
Poughkeepsie	(914) 471-8180
Rochester	(716) 272-9020
NORTH CAROLINA	(919) 878-8111
OHIO,	
Columbus (Westerville)	(614) 891-6455
OREGON	(503) 245-0080
PENNSYLVANIA	(215) 398-8006
SOUTH CAROLINA	(803) 772-6760
TEXAS,	
Austin	(512) 346-7830
Dallas	(214) 934-9099
Houston	(713) 785-9001
UTAH	(801) 264-2900

International

Location	Type	Number
BELGIUM, Bruxelles	TEL	(02) 771-91-42
	FAX	(02) 762-37-12
	TLX	846-61028
FRANCE, Paris	TEL	(1) 49-75-10-10
	FAX	(1) 49-75-10-13
	TLX	263282F
WEST GERMANY,		
Hannover area	TEL	(0511) 736085
	FAX	(0511) 721254
	TLX	922850
München	TEL	(089) 4114-0
	FAX	(089) 406490
	TLX	523883
Stuttgart	TEL	(0711) 62 33 77
	FAX	(0711) 625187
	TLX	721882
HONG KONG,	TEL	852-5-8654525
Wanchai	FAX	852-5-8654335
	TLX	67955AMDAPHX
ITALY, Milan	TEL	(02) 3390541
		(02) 3533241
	FAX	(02) 3498000
	TLX	843-315286
JAPAN,		
Atsugi	TEL	462-29-8460
	FAX	462-29-8458
Kanagawa	TEL	462-47-2911
	FAX	462-47-1729
Tokyo	TEL	(03) 346-7550
	FAX	(03) 342-5196
	TLX	J24064AMDTKOJ

International *(Continued)*

Location	Type	Number
Osaka	TEL	06-243-3250
	FAX	06-243-3253
KOREA, Seoul	TEL	822-784-0030
	FAX	822-784-8014
LATIN AMERICA,		
Ft. Lauderdale	TEL	(305) 484-8600
	FAX	(305) 485-9736
	TLX	5109554261 AMDFTL
NORWAY, Hovik	TEL	(03) 010156
	FAX	(02) 591959
	TLX	79079HBCN
SINGAPORE	TEL	65-3481188
	FAX	65-3480161
	TLX	55650 AMDMMI
SWEDEN,		
Stockholm	TEL	(08) 733 03 50
(Sundbyberg)	FAX	(08) 733 22 85
	TLX	11602
TAIWAN	TEL	886-2-7213393
	FAX	886-2-7723422
	TLX	886-2-7122066
UNITED KINGDOM,		
Manchester area	TEL	(0925) 828008
(Warrington)	FAX	(0925) 827693
	TLX	851-628524
London area	TEL	(0483) 740440
(Woking)	FAX	(0483) 756196
	TLX	851-859103

North American Representatives

Location / Representative	Telephone
CANADA	
Burnaby, B.C.	
DAVETEK MARKETING	(604) 430-3680
Calgary, Alberta	
DAVETEK MARKETING	(403) 291-4984
Kanata, Ontario	
VITEL ELECTRONICS	(613) 592-0060
Mississauga, Ontario	
VITEL ELECTRONICS	(416) 676-9720
Lachine, Quebec	
VITEL ELECTRONICS	(514) 636-5951
IDAHO	
INTERMOUNTAIN TECH MKTG, INC	(208) 888-6071
ILLINOIS	
HEARTLAND TECH MKTG, INC	(312) 577-9222
INDIANA	
Huntington - ELECTRONIC MARKETING CONSULTANTS, INC	(317) 921-3450
Indianapolis - ELECTRONIC MARKETING CONSULTANTS, INC	(317) 921-3450
IOWA	
LORENZ SALES	(319) 377-4666
KANSAS	
Merriam – LORENZ SALES	(913) 469-1312
Wichita – LORENZ SALES	(316) 721-0500
KENTUCKY	
ELECTRONIC MARKETING CONSULTANTS, INC	(317) 921-3452
MICHIGAN	
Birmingham - MIKE RAICK ASSOCIATES	(313) 644-5040
Holland – COM-TEK SALES, INC	(616) 392-7100
Novi – COM-TEK SALES, INC	(313) 344-1409
MINNESOTA	
Mel Foster Tech. Sales, Inc.	(612) 941-9790
MISSOURI	
LORENZ SALES	(314) 997-4558
NEBRASKA	
LORENZ SALES	(402) 475-4660
NEW MEXICO	
THORSON DESERT STATES	(505) 293-8555
NEW YORK	
East Syracuse – NYCOM, INC	(315) 437-8343
Woodbury – COMPONENT CONSULTANTS, INC	(516) 364-8020
OHIO	
Centerville – DOLFUSS ROOT & CO	(513) 433-6776
Columbus – DOLFUSS ROOT & CO	(614) 885-4844
Strongsville – DOLFUSS ROOT & CO	(216) 238-0300
PENNSYLVANIA	
DOLFUSS ROOT & CO	(412) 221-4420
PUERTO RICO	
COMP REP ASSOC, INC	(809) 746-6550
UTAH, R² MARKETING	(801) 595-0631
WASHINGTON	
ELECTRA TECHNICAL SALES	(206) 821-7442
WISCONSIN	
HEARTLAND TECH MKTG, INC	(414) 792-0920

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