Flash Memory Products

1994/1995 Data Book/Handbook

Advanced Micro Devices

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Flash Memory Products

Data Book/Handbook

1994/1995

A D V A N C E D M I C R O D E V I C E S

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Over the last five years, Flash memory products have revolutionized how designers think about storing control code in computers, peripherals, communication devices, and a wealth of other applications. In fact, Flash memory is seen as an enabling technology in many new microprocessor-based designs. The features of Flash memory, including non-volatility, in-system re-programmability, and high density, have made it the fastest growing IC memory type in the 1990s. AMD's Flash memory products are ideally suited for use in a wide array of microprocessor-based products.

The first generation of Flash memory devices required 12.0 Volts to program and erase and 5.0 Volts to read. Today, however, system designers are asking for single-voltage Flash memory products. Other Flash memory features being requested by system designers include: fast read access time, the ability to erase portions of the memory array, simplified program and erase algorithms, high endurance and reliability. The Am29Fxxx Flash family is addressing these requests from system designers **today**.

AMD is the leader in providing cost effective 5.0 Volt-only Flash memory devices with its Am29Fxxx Flash family. These devices meet the JEDEC (Joint Electron Devices Engineering Council) pin-out and software standards for single voltage supply Flash. AMD achieves 5.0 Volt–only operation in its Am29Fxxx family Flash devices using patented Negative Gate Erase technology. AMD has seen overwhelming acceptance of the Am29Fxxx Flash architecture from designers representing many applications.

AMD offers Flash memory cards that meet the PCMCIA and JEIDA standards. This data book contains condensed data sheets of AMD's Flash memory card offerings.

AMD is the world leader in non-volatile memory devices. The market's acceptance of our Flash components and memory cards has strengthened our position as a major Flash memory supplier.

Walid Maghribi
Vice President and General Manager
Non-Volatile Memroy Division

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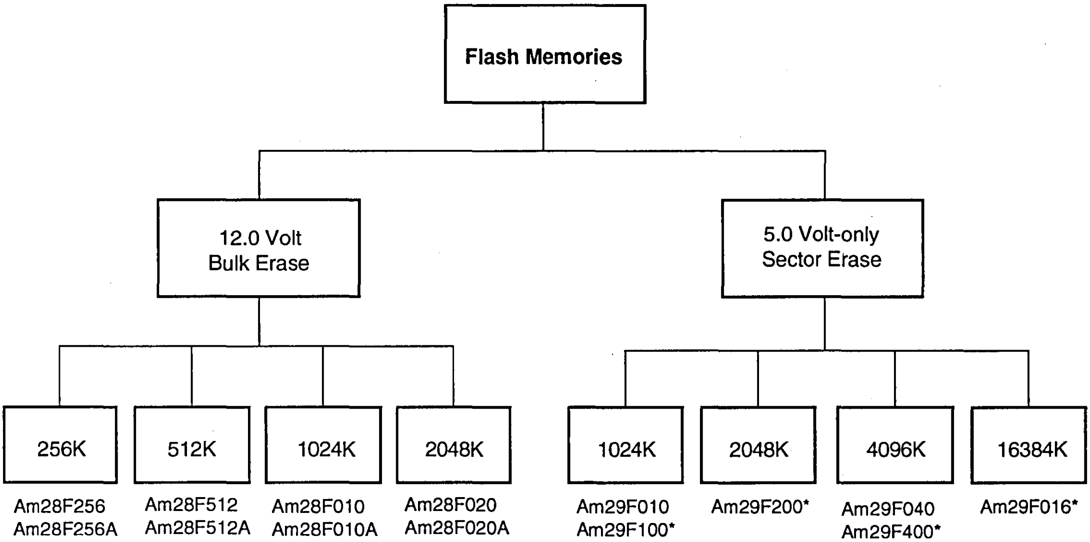
FLASH MEMORIES SELECTOR GUIDE



12.0 Volt Flash, Flashrite™/Flasherase™ Algorithms, 10K Cycle Endurance

Part Number	Organization	Access Time (ns)	Temp Range[1]	Package Type[2]	Pin Count	Supply Voltage	Programming Voltage
Am28F256-75	32K x 8	70	C, I	D, L, P, J, E, F	32	5 V ± 5%	12 V
Am28F256-90	32K x 8	90	C, I	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F256-95	32K x 8	90	C, I	D, L, P, J, E, F	32	5 V ± 5%	12 V
Am28F256-120	32K x 8	120	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F256-150	32K x 8	150	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F256-200	32K x 8	200	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F512-75	64K x 8	70	C, I	D, L, P, J, E, F	32	5 V ± 5%	12 V
Am28F512-90	64K x 8	90	C, I	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F512-95	64K x 8	90	C, I	D, L, P, J, E, F	32	5 V ± 5%	12 V
Am28F512-120	64K x 8	120	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F512-150	64K x 8	150	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F512-200	64K x 8	200	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F010-90	128K x 8	90	C, I	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F010-95	128K x 8	90	C, I	D, L, P, J, E, F	32	5 V ± 5%	12 V
Am28F010-120	128K x 8	120	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F010-150	128K x 8	150	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F010-200	128K x 8	200	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F020-90	256K x 8	90	C	P, J, E, F	32	5 V ± 10%	12 V
Am28F020-95	256K x 8	90	C	P, J, E, F	32	5 V ± 5%	12 V
Am28F020-120	256K x 8	120	C, I, E, M	P, J, E, F	32	5 V ± 10%	12 V
Am28F020-150	256K x 8	150	C, I, E, M	P, J, E, F	32	5 V ± 10%	12 V
Am28F020-200	256K x 8	200	C, I, E, M	P, J, E, F	32	5 V ± 10%	12 V

Notes: see notes on next page.

12.0 Volt Flash, Embedded Algorithms, 100K Cycle Endurance

Part Number	Organization	Access Time (ns)	Temp Range[1]	Package Type[2]	Pin Count	Supply Voltage	Programming Voltage
Am28F256A-75	32K x 8	70	C, I	D, L, P, J, E, F	32	5 V ± 5%	12 V
Am28F256A-90	32K x 8	90	C, I	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F256A-95	32K x 8	90	C, I	D, L, P, J, E, F	32	5 V ± 5%	12 V
Am28F256A-120	32K x 8	120	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F256A-150	32K x 8	150	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F256A-200	32K x 8	200	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F512A-75	64K x 8	70	C, I	D, L, P, J, E, F	32	5 V ± 5%	12 V
Am28F512A-90	64K x 8	90	C, I	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F512A-95	64K x 8	90	C, I	D, L, P, J, E, F	32	5 V ± 5%	12 V
Am28F512A-120	64K x 8	120	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F512A-150	64K x 8	150	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F512A-200	64K x 8	200	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F010A-90	128K x 8	90	C, I	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F010A-95	128K x 8	90	C, I	D, L, P, J, E, F	32	5 V ± 5%	12 V
Am28F010A-120	128K x 8	120	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F010A-150	128K x 8	150	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F010A-200	128K x 8	150	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	12 V
Am28F020A-90	256K x 8	90	C	D, P, J, E, F	32	5 V ± 10%	12 V
Am28F020A-95	256K x 8	90	C	D, P, J, E, F	32	5 V ± 5%	12 V
Am28F020A-120	256K x 8	120	C, I, E, M	D, P, J, E, F	32	5 V ± 10%	12 V
Am28F020A-150	256K x 8	150	C, I, E, M	D, P, J, E, F	32	5 V ± 10%	12 V
Am28F020A-200	256K x 8	200	C, I, E, M	D, P, J, E, F	32	5 V ± 10%	12 V

5.0 Volt-only Flash, Embedded Algorithms, Sector Erase, 100K Cycle Endurance

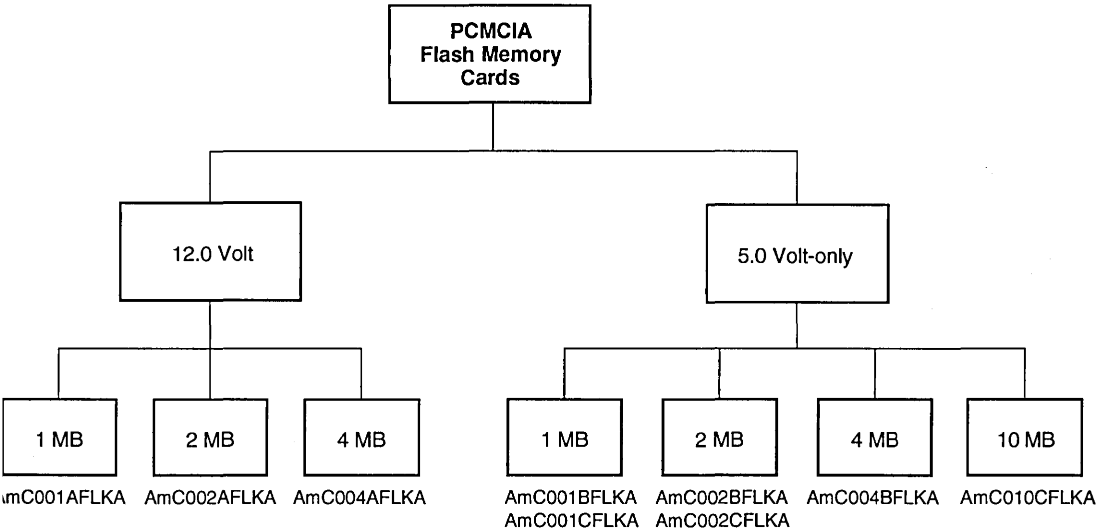
Part Number	Organization	Access Time (ns)	Temp Range[1]	Package Type[2]	Pin Count	Supply Voltage	Programming Voltage
Am29F010-45	128K x 8	45	C, I	D, L, P, J, E, F	32	5 V ± 5%	5 V
Am29F010-55	128K x 8	55	C, I	D, L, P, J, E, F	32	5 V ± 10%	5 V
Am29F010-70	128K x 8	70	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	5 V
Am29F010-90	128K x 8	90	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	5 V
Am29F010-120	128K x 8	120	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	5 V
Am29F100-75*	128K x 8, 64K x 16	70	C	E, F, S	44/48	5 V ± 5%	5 V
Am29F100-90*	128K x 8, 64K x 16	90	C, I, E	E, F, S	44/48	5 V ± 10%	5 V
Am29F100-120*	128K x 8, 64K x 16	120	C, I, E	E, F, S	44/48	5 V ± 10%	5 V
Am29F100-150*	128K x 8, 64K x 16	150	C, I, E	E, F, S	44/48	5 V ± 5%	5 V
Am29F200-75*	256K x 8, 128K x 16	70	C	E, F, S	44/48	5 V ± 5%	5 V
Am29F200-90*	256K x 8, 128K x 16	90	C, I, E	E, F, S	44/48	5 V ± 10%	5 V
Am29F200-120*	256K x 8, 128K x 16	120	C, I, E	E, F, S	44/48	5 V ± 10%	5 V
Am29F200-150*	256K x 8, 128K x 16	150	C, I, E	E, F, S	44/48	5 V ± 5%	5 V
Am29F040-75	512K x 8	70	C	D, L, P, J, E, F	32	5 V ± 5%	5 V
Am29F040-90	512K x 8	90	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	5 V
Am29F040-120	512K x 8	120	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	5 V
Am29F040-150	512K x 8	150	C, I, E, M	D, L, P, J, E, F	32	5 V ± 10%	5 V
Am29F400-75*	512K x 8, 256K x 16	70	C	E, F, S	44/48	5 V ± 5%	5 V
Am29F400-90*	512K x 8, 256K x 16	90	C, I, E	E, F, S	44/48	5 V ± 10%	5 V
Am29F400-120*	512K x 8, 256K x 16	120	C, I, E	E, F, S	44/48	5 V ± 10%	5 V
Am29F400-150*	512K x 8, 256K x 16	150	C, I, E	E, F, S	44/48	5 V ± 10%	5 V
Am29F016-90*	2M x 8	90	C	E, F	48	5 V ± 10%	5 V
Am29F016-120*	2M x 8	120	C, I, E	E, F	48	5 V ± 10%	5 V
Am29F016-150*	2M x 8	150	C	E, F	48	5 V ± 10%	5 V

Notes:

1. Temperature Range
   - C = Commercial (0°C to 70°C)
   - I = Industrial (–40°C to +85°C)
   - E = Extended Commercial (–55°C to +125°C)
   - M = Military (–55°C to +125°C) most products available in both APL and DESC versions.

2. Package Type
   - **DIP (Dual In-Line Packages)**
   - D = Ceramic DIP
   - P = Plastic DIP
   - **SMT (Surface Mount Technology)**
   - L = Rectangular Ceramic Leadless Chip Carrier
   - J = Rectangular Plastic Leaded Chip Carrier
   - E = Thin Small Outline Package – standard pin-out
   - F = Thin Small Outline Package – reverse pin-out
   - S = Small Outline Package

*Contact the local AMD sales office for availability of this device.



2.0 Volt Flash Memory Cards

Part Number	Density (Mbytes)	Access Time (ns)	Temp Range[1]	Package Type (PCMCIA)	Minimum Write Cycles	Automated Write/Erase Operations	Read Voltage	Write Voltage
AmC001AFLKA	1	250 ns	C	68-Pin, Type 1	100,000	Yes	5 V ± 5%	12 V ± 5%
AmC002AFLKA	2	250 ns	C	68-Pin, Type 1	100,000	Yes	5 V ± 5%	12 V ± 5%
AmC004AFLKA	4	250 ns	C	68-Pin, Type 1	100,000	Yes	5 V ± 5%	12 V ± 5%

.0 Volt-only Flash Memory Cards

Part Number	Density (Mbytes)	Access Time (ns)	Temp Range[1]	Package Type (PCMCIA)	Minimum Write Cycles	Automated Write/Erase Operations	Read Voltage	Write Voltage
AmC001BFLKA	1	200 ns	C	68-Pin, Type 1	100,000	Yes	5 V ± 5%	5 V ± 5%
AmC002BFLKA	2	200 ns	C	68-Pin, Type 1	100,000	Yes	5 V ± 5%	5 V ± 5%
AmC001CFLKA	1	150 ns	C	68-Pin, Type 1	100,000	Yes	5 V ± 5%	5 V ± 5%
AmC002CFLKA	2	150 ns	C	68-Pin, Type 1	100,000	Yes	5 V ± 5%	5 V ± 5%
AmC004CFLKA	4	150 ns	C	68-Pin, Type 1	100,000	Yes	5 V ± 5%	5 V ± 5%
AmC010CFLKA	10	150 ns	C	68-Pin, Type 1	100,000	Yes	5 V ± 5%	5 V ± 5%

Introduction to AMD's ExpressFlash™ Service

Advanced Micro Devices

INTRODUCTION

AMD's ExpressFlash service is a helpful new way to offer the system manufacturer flexibility and lower cost in the manufacturing process. No matter how Flash memory is used in your system, AMD's ExpressFlash service will benefit your manufacturing process. Flash devices procured via the ExpressFlash program are rigorously tested with your code under both AC and DC operating conditions at worse case temperature prior to shipment. Because Flash products ordered through the ExpressFlash service are shipped board-ready with factory guaranteed quality, your ship-to-stock or Just-In-Time programs can be easily implemented.

AMD's ExpressFlash service offers the same pre-programming convenience as AMD's ExpressROM™ Memories with the added advantage of in-system reprogrammability. Whether your entire code is finalized by the time you place your order or not, AMD's ExpressFlash service will work for you. After AMD's Flash devices are delivered and installed in your system—you have the added flexibility to reprogram the devices *in-system at any time.*

AMD's ExpressFlash service is ideally suited for a variety of applications. For example, with AMD's ExpressFlash service, a PC manufacturer's boot code can be programmed in a portion of the AMD Flash device while the rest of the device remains blank. Upon delivery the Flash devices can be directly installed in your systems. After the remainder of the code is finalized, it can then be loaded *in-system. At this point, even the original boot code can be altered should a "bug" be discovered or a change be required. This process reduces manufacturing cycle time, overhead, and improves both time-to-market and system availability.*

For systems requiring fully protected blocks of code, AMD's Am29F family is ideal. With AMD's ExpressFlash service, your code can be protected from further alteration right at AMD's factory. In the system, the protected portion of code looks just like a ROM. Please refer to AMD's Am29F family of data sheets for further details.

Since Flash devices are fully tested in the plastic packages, all speed grades offered for standard Flash devices are available through the ExpressFlash program as well.

ExpressFlash Service Lowers Cost

The ExpressFlash service eliminates or reduces costs in several areas. These include programming, testing, marking and labeling. Standard programming of blank devices may reveal other hidden expenses such as costs associated with possible programming yield losses, capacity constraints, labels and other supplies, rework, inventory and associated queue time, handling, maintenance, labor and personnel, transit costs, inspections, floor space and other overhead. AMD's ExpressFlash service adds value by eliminating or reducing all these costs.

Our mission at AMD is to provide services and products which enable you to build the cost-competitive systems you need to win in your markets. The ExpressFlash service is yet another value-added program offered by AMD to help you accomplish your goals. As the world's #1 supplier of EPROMs and Flash, AMD appreciates the value of cost-efficient manufacturing. Compressing time-to-market cycles, improving yields and providing the highest levels of quality are invaluable strategies for today's system manufacturer. At AMD we are proud to offer another tool to give our customers this strategic advantage.

ExpressFlash Flow

AMD's ExpressFlash service takes Flash devices from inventory in our off-shore testing facility and continues the processing as shown in Figure 1. This process is offered for all package types and speed grades. Please refer to AMD's Flash data sheets for valid combinations. For die orders, please contact your local AMD sales representative.

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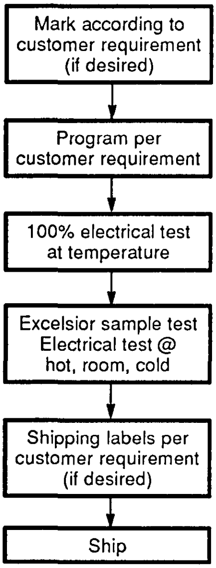
Issue Date: March 1994



17125B-1

Figure 1. ExpressFlash Flow

Ordering Flash Devices Using the ExpressFlash Service

The following procedure outlines the method for ordering a Flash device using the ExpressFlash service. For more information, please contact your local AMD sales representative.

1) Fill out the ExpressFlash Code Approval Form

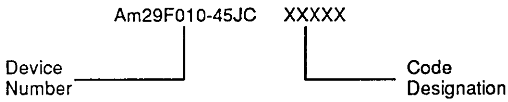
An example of the ExpressFlash Code Approval Form is shown in Figure 2. **Please have your field sales representative provide you with the latest version of the ExpressFlash Code Approval Form.** This form will provide all the necessary information required for processing your order. After receiving this form, fill out the Code Transmittal and Ordering Information sections. **Do not** fill out the Approval Section Terms and Conditions. For sector erase flash devices that require sector protection, a sector map will be provided with the ExpressFlash Code Approval Form. On the sector map, indicate which sectors need to be protected. A detailed description of how to fill out the sector map will be provided with the form.

2) Send in the Code

Send in the form with two (2) master copies of each code being ordered to your field sales representative. To minimize the verification turnaround process, supply two master copies of each code using standard Flash devices identical in architecture and density as the Flash device being ordered. Two master copies per code are required in order to guarantee proper code transmission. Please be sure the checksum is clearly identified on each master Flash device.

3) AMD Checks the Code and Generates a Verification Flash Device

We check that both Flash devices contain the same code to make certain there was not a mix-up in shipping your codes to the factory as well as ensuring that the integrity of your code has been preserved. After confirming this, a unique 5-digit code designation is assigned. The AMD part number is formed by adding the 5-digit code designation as a suffix to the Flash device number. See below:



17125B-2

AMD then logs in your code with the 5-digit code designation and generates a verification Flash device. The verification Flash device along with one of your master Flash devices and the ExpressFlash Code Approval Form should be back in your hand for final approval within 2–3 days. The other master Flash device remains at AMD for our records. Please note: the verification Flash device is simply a means of transferring the code and is not necessarily indicative of the Flash device being ordered.

4) Confirm the Copy and Place the Order

Once the verification Flash device is approved, sign the Approval Section of the ExpressFlash Code Approval Form and return it to AMD with your purchase order. Upon receipt of the signed form and a purchase order, AMD enters the order and begins production. Logged codes are maintained for 60 days and then deleted if there is no purchase order placed.

5) Customer Special Shipping Labels (optional)

AMD can provide labels on the shipping boxes that indicate that the boxes contain ExpressFlash devices. To designate that you want special shipping labels, please provide specific instructions with your ExpressFlash purchase order.

TERMS AND CONDITIONS

You should be aware of the following when ordering Flash devices using the ExpressFlash service.

1. AMD will maintain customer code confidentiality.
2. AMD will absorb all initial set-up costs.
3. All orders are subject to minimum quantities. The minimum quantity for initial orders is 5,000 pieces.
4. AMD may begin production 14 days in advance of the AMD scheduled ship date covered by a purchase order and requires 14 days minimum notification from the AMD scheduled ship date for code changes. The customer is liable for all work-in-process covered by the same purchase order.
5. No schedule changes may be made within 14 days of AMD scheduled ship date.
6. All unpackaged die product procured by the customer is for use exclusively in the customer's end products. Any other use of die product must be approved in writing by AMD.
7. Code changes with Work-In-Process will require additional charges and may affect delivery schedules.
8. All other terms and conditions which normally apply to AMD's Flash devices (if any) also apply using AMD's ExpressFlash service.

ExpressFlash™ Code Approval Form

CODE TRANSMITTAL AND ORDERING INFORMATION SECTION Rev. 1 5/12/92

Please complete items 1 thru 9. To minimize the verfication turn-around process, supply 2 master copies of each code using Flash Devices of the same architecture and density as the Flash Device being ordered. Also, be sure the checksum is clearly identified on each master Flash Device.

CODE TRANSMITTAL SECTION

1. Company Name: ____________________ 2. Date: ____________________
3. Incoming Master's Part #: ____________________ 4. Master's Checksum: ____________________

ORDERING INFORMATION SECTION

Please check the appropriate Flash Device data sheet for valid combinations and mark appropriate boxes below; V_{CC} is +/–10% unless otherwise noted with an * for +/–5%.

5. Part #: Am____________________

 ❑ Sector information ____________________ Protected? ❑ Yes ❑ No
 ❑ Other ____________________

6. Package and Temperature: ❑ Plastic DIP ❑ Commercial (0°C to +70°C)
 ❑ PLCC ❑ Industrial (–40°C to +85°C)
 ❑ TSOP Standard Pinout
 ❑ TSOP Reverse Pinout
 ❑ SOIC
 ❑ Other ____________________

7. AMD Standard Part Number: ____________________
8. Customer Ordering Part Number: ____________________
9. Please indicate the exact **marking** and complete the blank sections (10 characters per line including spaces, © = 2 spaces if required).

AMD Logo

____

____

____

Date Code

SAMPLE

APPROVAL SECTION TERMS AND CONDITIONS
(This section to be completed after samples are returned for customer verification)

AMD will maintain customer code confidentially. AMD will absorb all initial set-up costs.
AMD may begin production 14 days in advanced of the AMD scheduled ship date covered by a purchase order and requires 14 days minimum notification from the AMD scheduled ship date for code changes.
The customer is liable for all work-in-process covered by the same purchase order.
No schedule changes may be made within 14 days of AMD scheduled ship date.
All unpackaged die product procured by the customer is for use exclusively in the customer's end products.
Any other use of die product must be approved in writing by AMD.
All orders are subject to minimum quantities.
Code changes with Work In Process will require additional charges and may affect delivery schedules.

AMD Standard Part #: Am____________________ Checksum: ____________________
Customer Signature: ____________________ Date: ____________________
Name (Print): ____________________ Title: ____________________

Contact your local AMD sales office for approval form.

Figure 2 17125B-3

PRELIMINARY

Flash Memories in Die Form

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Testing of AC and DC parameters
- Operating temperature ranges:
  - — Commercial 0°C to 70°C
  - — Industrial –40°C to +85°C
  - — Military –55°C to +125°C
- Advanced CMOS Flash memory technology
- High typical yield—98% after assembly
- Full data sheet compatibility
- Die visual inspection per MIL-STD-883, Method 2010 Condition B

GENERAL DESCRIPTION

AMD offers it's family of flash products in die form for hybrid or multichip module applications requiring superior performance and in-system reprogrammability in addition to small die size. Each die is AC and DC tested at wafer sort to guarantee full device functionality over commercial through military temperature ranges. AMD's Flash technology reliably stores memory contents even after 100,000 erase and program cycles.

Features such as "5.0 Volt-only" program and erase, Sector erase architecture and Embedded Program™ and Embedded Erase™ algorithms are also available. Specific product information is available in the product data sheets.

Please refer to the notes below for die handling considerations.

PRODUCT SELECTOR GUIDE

Die Ordering Part Number	Organization	Access Time	Endurance Cycles	Program/ Erase Voltage	Embedded Algorithms	Data Sheet Reference
Am28F256A-XC/3	256K (32K x 8)	200 ns	100,000	12 V ± 5%	Yes	Am28F256A
Am28F512A-XC/2	512K (64K x 8)	200 ns	100,000	12 V ± 5%	Yes	Am28F512A
Am28F010A-XC/6	1M (128K x 8)	200 ns	100,000	12 V ± 5%	Yes	Am28F010A
Am29F010-XC/4	1M (128K x 8)	90 ns	100,000	5 V ± 10%	Yes	Am29F010
Am28F020A-XC/3	2M (256K x 8)	200 ns	100,000	12 V ± 5%	Yes	Am28F020A
Am29F200-XC/1**	2M (131K x 16)	120 ns	100,000	5 V ± 10%	Yes	Am29F200
Am29F040-XC/1	4M (512K x 8)	120 ns	100,000	5 V ± 10%	Yes	Am29F040
Am29F400-XC/1**	4M (512K x 16)	120 ns	100,000	5 V ± 10%	Yes	Am29F400

Notes:

1. *NVD only guarantees die, which is processed by the customers, at temperatures less than 250° C. If the die is hermetically sealed, NVD will not be liable for die failure.*
2. *Exposure of Flash die to ultraviolet light may effect device functionality.*

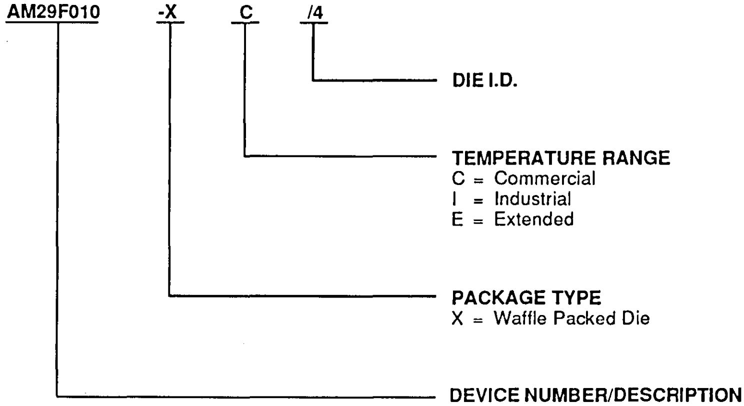
***Contact sales office for availability.*

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

Publication# 17126 Rev. B Amendment/0
Issue Date: March 1994

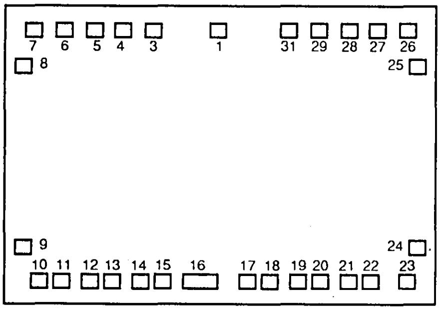
ORDERING INFORMATION

AMD Flash Memories are available in several operating ranges. The order number (Valid Combination) is formed by a combination of:

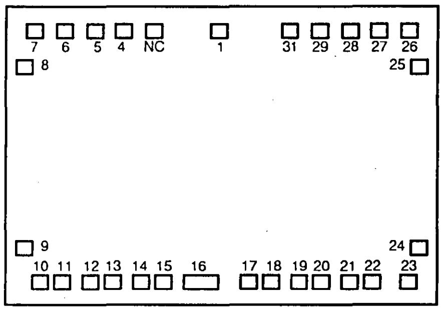


Note: *Exposure of Flash die to ultraviolet light may effect device functionality.*

DIE SIZE AND BONDING PAD LOCATIONS

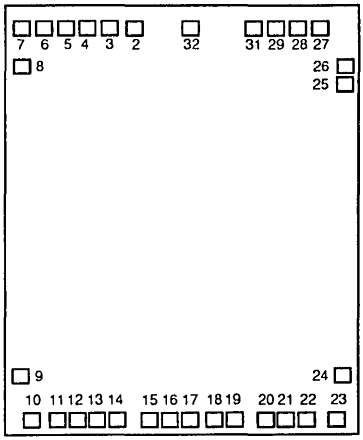


Am28F256A-XC/3
256K (32K x 8) Flash Memory
100K endurance cycles
Embedded Algorithms
Die Size: 0.160 x 0.156 inches
Technology: 0.85 μm
Reference: Am28F256A data sheet

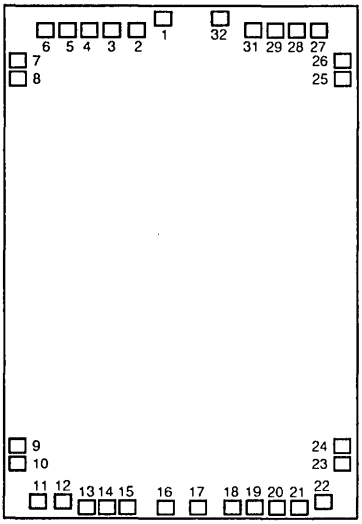


Am28F512A-XC/2
512K (64K x 8) Flash Memory
100K endurance cycles
Embedded Algorithms
Die Size: 0.160 x 0.156 inches
Technology: 0.85 μm
Reference: Am28F512A data sheet

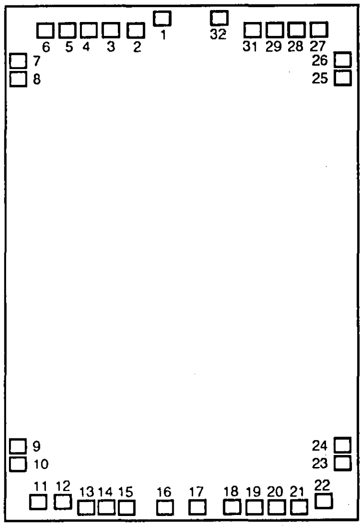
DIE SIZE AND BONDING PAD LOCATIONS



Am29F010-XC/4
1 Megabit (128K x 8) Flash Memory
5 Volt-only program & erase
100K endurance cycles
Embedded Algorithms
Die Size: 0.174 x 0.189 inches
Technology: 0.85 µm (non-SAS)
Reference: Am29F010 data sheet

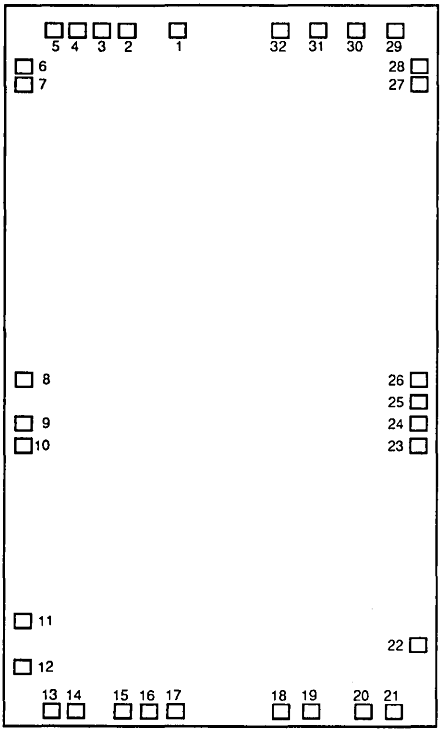


Am28F010A-XC/5
1 Megabit (128K x 8) Flash Memory
100K endurance cycles
Embedded Algorithms
Die Size: 0.187 x 0.252 inches
Technology: 1 µm
Reference: Am28F010A data sheet

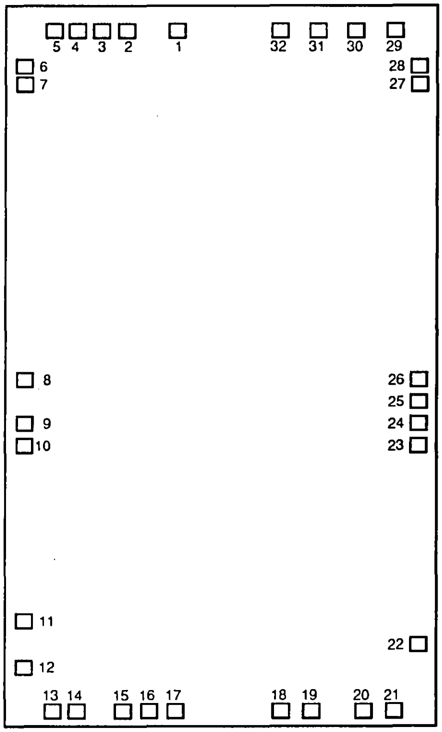


Am28F010A-XC/6
1 Megabit (128K x 8) Flash Memory
100K endurance cycles
Embedded Algorithms
Die Size: 0.160 x 0.217 inches
Technology: 0.85 µm
Reference: Am28F010A data sheet

DIE SIZE AND BONDING PAD LOCATIONS



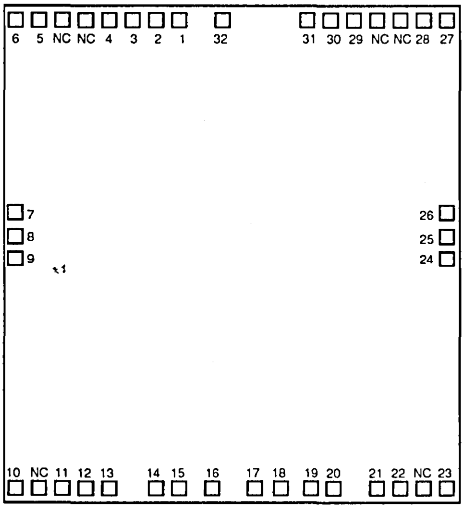
Am28F020A-XC/2
1 Megabit (256K x 8) Flash Memory
100K endurance cycles
Embedded Algorithms
Die Size: 0.213 x 0.374 inches
Technology: 1 µm
Reference: Am28F020A data sheet



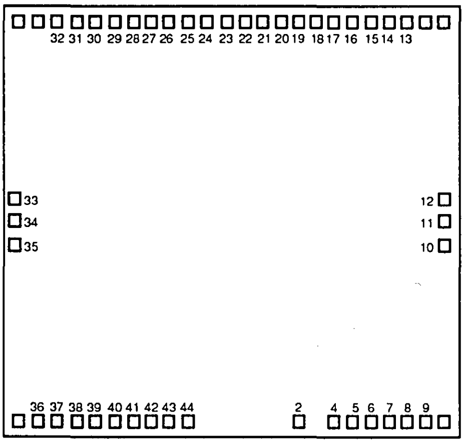
Am28F020A-XC/3
2 Megabit (256K x 8) Flash Memory
100K endurance cycles
Embedded Algorithms
Die Size: 0.190 x 0.318 inches
Technology: 0.85 µm
Reference: Am28F020A data sheet

Note:
1.0 µm products will not be in production after 1994.

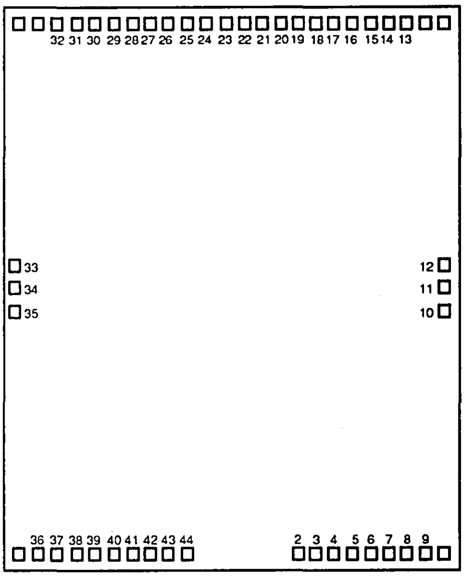
DIE SIZE AND BONDING PAD LOCATIONS



Am29F040-XC/1
4 Megabit (512K x 8) Flash Memory
100K endurance cycles
Embedded Algorithms
Die Size: 0.262 x 0.297 inches
Technology: 0.85 µm
Reference: Am29F040 data sheet



Am29F200-XC/1
2 Megabit (262,144 x 8-Bit/131,072 x 16-Bit)
100K endurance cycles
Embedded Algorithms
Die Size: 0.266 x 0.203 inches
Technology: 0.85 µm
Reference: Am29F200 data sheet



Am29F400-XC/1
4 Megabit (524,288 x 8-Bit/262,144 x 16-Bit)
100K endurance cycles
Embedded Algorithms
Die Size: 0.266 x 0.312 inches
Technology: 0.85 µm
Reference: Am29F400 data sheet

TERMS AND CONDITIONS OF SALE FOR AMD NON-VOLATILE MEMORY DIE

All transactions relating to AMD Products under this agreement shall be subject to AMD's standard terms and conditions of sale, or any revisions thereof, which revisions AMD reserves the right to make at any time and from time to time. In the event of conflict between the provisions of AMD's standard terms and conditions of sale and this agreement, the terms of this agreement shall be controlling.

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AMD products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in a personal injury. Buyer's use of AMD products for use in life support applications is at Buyers own risk and Buyer agrees to fully indemnify AMD for any damages resulting in such use or sale.

SECTION

1 5.0 Volt-only, SECTOR ERASE FLASH MEMORIES

FINAL

Am29F010

Advanced Micro Devices

1 Megabit (131,072 x 8-Bit) CMOS 5.0 Volt-only, Sector Erase Flash Memory

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% read, write, and erase**
  - Minimizes system level power consumption
- **Compatible with JEDEC-standard commands**
  - Uses same software commands as E^{2}PROMs
- **Compatible with JEDEC-standard byte-wide pinouts**
  - 32-pin PLCC/LCC
  - 32-pin TSOP
  - 32-pin DIP
- **Minimum 100,000 write/erase cycles**
- **High performance**
  - 45 ns maximum access time
- **Sector erase architecture**
  - 8 equal size sectors of 16K bytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase
- **Embedded Erase™ Algorithms**
  - Automatically pre-programs and erases the chip or any sector
- **Embedded Program™ Algorithms**
  - Automatically programs and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Low power consumption**
  - 20 mA typical active read current
  - 30 mA typical program/erase current
  - 25 µA typical standby current
- **Low V_{CC} write inhibit ≤ 3.2 V**
- **Sector Protection**
  - Hardware method disables any combination of sectors from program or erase operations

GENERAL DESCRIPTION

The Am29F010 is a 1Mbit, 5.0 V-only Flash memory organized as 128K bytes of 8 bits each. The Am29F010 is offered in a 32-pin package which allows for upgrades to 4 Mbit densities in the same pin out. This device is designed to be programmed or erased in-system with the standard system 5.0 V V_{CC} supply. 12.0 V V_{PP} is not required for program or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The Am29F010 offers access times between 45 ns and 120 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$) and output enable ($\overline{OE}$) controls.

The Am29F010 is entirely pin and command set compatible with JEDEC standard 1 Mbit E^{2}PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

The Am29F010 is programmed by executing the program command sequence. This will invoke the Embedded Program algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than 0.3 seconds. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase algorithm which is an internal algorithm that automatically preprograms the array if it is not already

PRODUCT SELECTOR GUIDE

Family Part No:	**Am29F010**				
Ordering Part No: V_{CC} = 5.0 V ± 5%	**-45**				
Read Voltage V_{CC} = 5.0 V ± 10%		**-55**	**-70**	**-90**	**-120**
Max Access Time (ns)	45	55	70	90	120
$\overline{CE}$ ($\overline{E}$) Access (ns)	45	55	70	90	120
$\overline{OE}$ ($\overline{G}$) Access (ns)	25	30	30	35	50

Publication# 16736 Rev. E Amendment /0
Issue Date: March 1993

programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin. The entire memory is typically erased and verified in three seconds (including pre-programming).

Any individual sector is typically erased and verified in 1.3 seconds (including pre-programming).

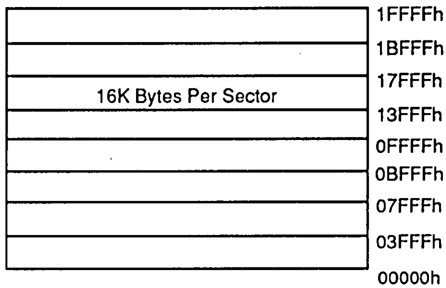
This device also features a sector erase architecture. The sector mode allows for 16K byte blocks of memory to be erased and reprogrammed without affecting other blocks. The Am29F010 is erased when shipped from the factory.

The device features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations during power transitions. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ7 or by the Toggle Bit feature on DQ6. Once the program or erase cycle has been completed, the device internally resets to the read mode.

AMD's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability and cost effectiveness. The Am29F010 memory electrically erases the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

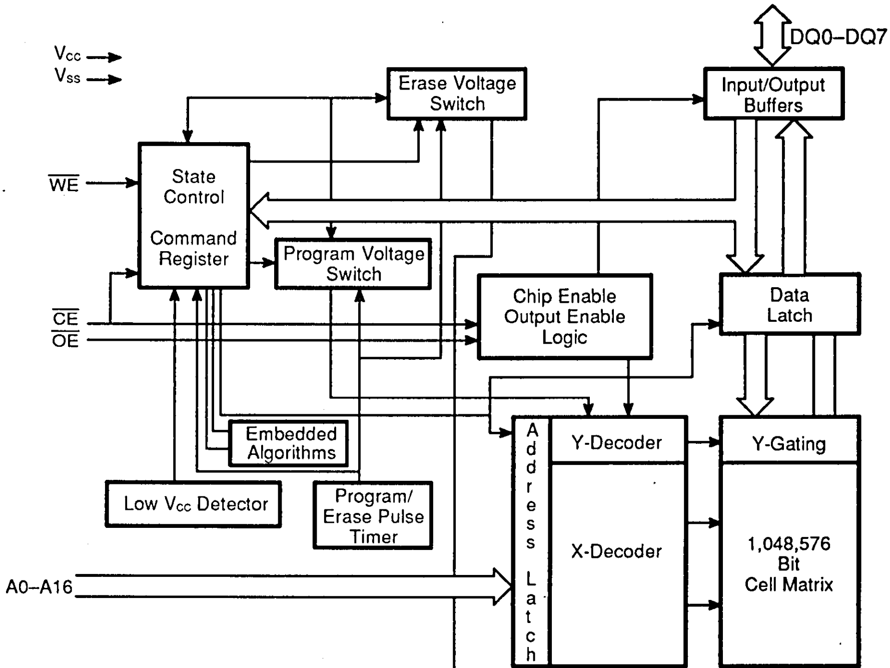
Flexible Sector-Erase Architecture

- 16K bytes per sector
- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user definable



16736E-2

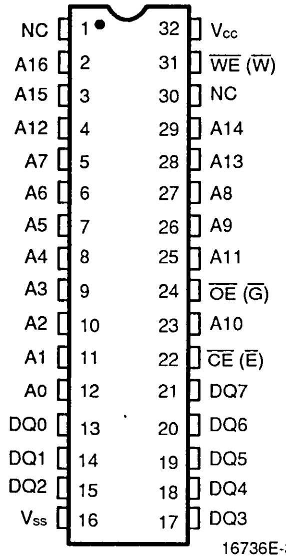
BLOCK DIAGRAM



16736E-1

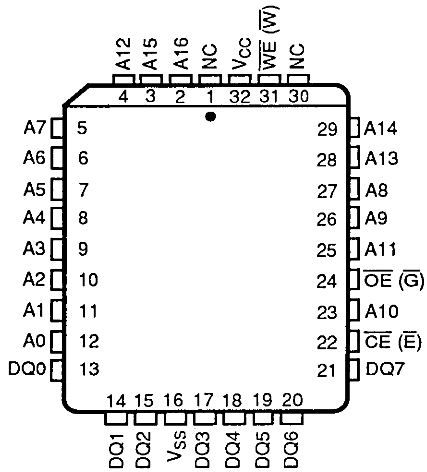
CONNECTION DIAGRAMS

CERDIP/PDIP



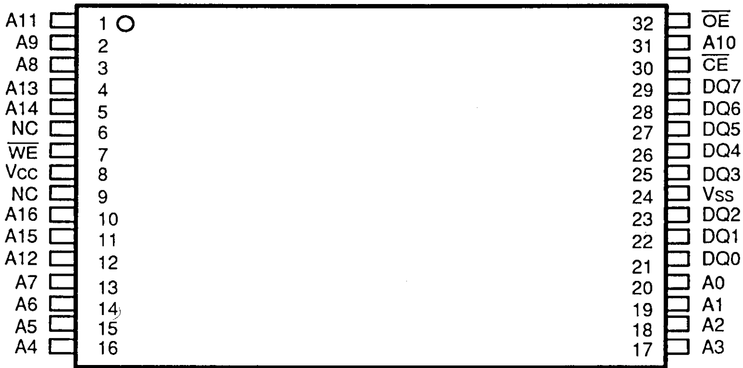
16736E-3

PLCC/LCC



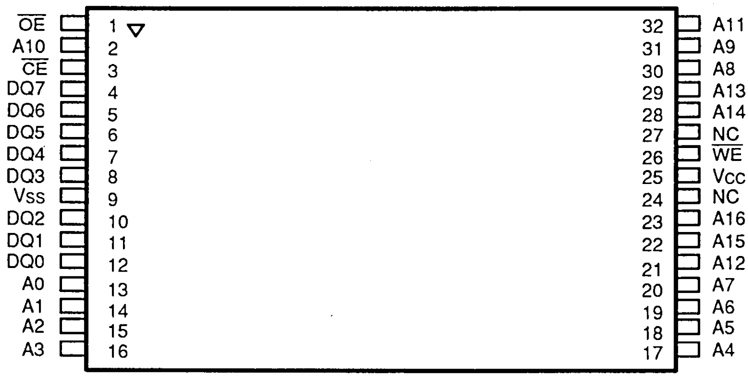
16736E-4

TSOP



29F010 Standard Pinout

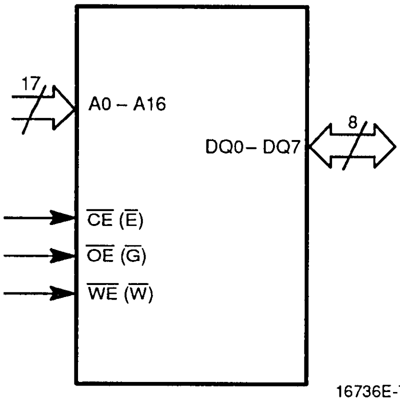
16736E-5



29F010 Reverse Pinout

16736E-6

LOGIC SYMBOL



16736E-7

Table 1. Am29F010 Pin Configuration

Pin	Function
A0–A16	Address Inputs
DQ0–DQ7	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{SS}	Device Ground
V_{CC}	Device Power Supply (5.0 V ± 10% or ± 5%)
NC	No Internal Connection

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

AM29F010 -45 J C B

OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-In

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended (–55°C to +125°C)

PACKAGE TYPE
P = 32-Pin Plastic DIP (PD 032)
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)
E = 32-Pin Thin Small Outline Package (TSOP) Standard Pinout (TS 032)
F = 32-Pin Thin Small Outline Package (TSOP) Reverse Pinout (TSR 032)

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am29F010
1 Megabit (128K x 8-Bit) CMOS Flash Memory
5.0 V Program and Erase
16K Byte Sectors

Valid Combinations	
AM29F010-45	JC, EC, FC
AM29F010-55	PC, PI, JC, JI, EC, EI, FC, FI
AM29F010-70 AM29F010-90 AM29F010-120	PC, PI, JC, JI, PCB, PIB, JCB, JIB, PE, PEB, JE, JEB, EC, EI, FC, FI, EE, EEB, FE, FEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

MILITARY ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

AM29F010 -70 /B X A

LEAD FINISH
A = Hot Solder Dip

PACKAGE TYPE
X = 32-Pin Ceramic DIP (CD 032)
U = 32-Pin Rectangular Ceramic Leadless Chip Carrier (CLR 032)

DEVICE CLASS
/B = Class B

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am29F010
1 Megabit (128K x 8-Bit) CMOS Flash Memory
5.0 V Program and Erase
16K Byte Sectors

Valid Combinations	
AM29F010-70	/BXA, /BUA
AM29F010-90	
AM29F010-120	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Table 2. Am29F010 User Bus Operations

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A9	I/O
Auto-Select Manufacturer Code (1)	L	L	H	L	L	V_{ID}	Code
Auto-Select Device Code (1)	L	L	H	H	L	V_{ID}	Code
Read	L	L	H	A0	A1	A9	D_{OUT}
Standby	H	X	X	X	X	X	HIGH Z
Output Disable	L	H	H	X	X	X	HIGH Z
Write	L	H	L	A0	A1	A9	D_{IN}(2)
Enable Sector Protect	L	V_{ID}	L	X	X	V_{ID}	X
Verify Sector Protect (3)	L	L	H	L	H	V_{ID}	Code

Legend:

L = V_{IL}, H = V_{IH}, X = Don't Care. See DC Characteristics for voltage levels

Notes:

1. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Tables 3 and 4.*
2. *Refer to Table 4 for valid D_{IN} during a write operation.*
3. *Refer to the section on Sector Protection*

Read Mode

The Am29F010 has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least t_{ACC}–t_{OE} time).

Standby Mode

The Am29F010 has two standby modes, a CMOS standby mode ($\overline{CE}$ input held at Vcc + 0.5 V), when the current consumed is less than 100 µA; and a TTL standby mode ($\overline{CE}$ is held at V_{IH}) when the current required is reduced to approximately 1 mA. In the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All addresses are don't cares except A0 and A1.

The manufacturer and device codes may also be read via the command register, for instances when the Am29F010 is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 4 (refer to Autoselect Command section).

Byte 0 (A0 = V_{IL}) represents the manufacture's code (AMD=01H) and byte 1 (A0 = V_{IH}) the device identifier code (Am29F010=20H). These two bytes are given in the table below. All identifiers for manufactures and device will exhibit odd parity with the MSB (DQ7) defined as the parity bit. In order to read the proper device codes when executing the autoselect, A1 must be V_{IL} (see Table 3).

Table 3. Am29F010 Autoselect and Sector Protection Verify Codes

Type	A16	A15	A14	A1	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer Code	X	X	X	V_{IL}	V_{IL}	01H	0	0	0	0	0	0	0	1
Am29F010 Device Code	X	X	X	V_{IL}	V_{IH}	20H	0	0	1	0	0	0	0	0
Sector Protection Verify	Sector Addresses			V_{IH}	V_{IL}	01H*	0	0	0	0	0	0	0	1

**Outputs 01H at protected sector addresses. Outputs 00H at unprotected sector addresses.*

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Protection

The Am29F010 features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 7). The sector protect feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected. Alternatively, AMD may program and protect sectors in the factory prior to shipping the device (see AMD's *ExpressFlash Service* section in the data book).

To activate this mode, the programming equipment must force V_{ID} on address pin A9 and control pin $\overline{OE}$. The sector addresses (A16, A15, and A14) should be set to the sector to be protected. Table 4 defines the sector addresses for each of the eight (8) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Reading the device at a particular sector address (A16, A15 and A14) will produce 01H at data outputs (DQ0–DQ7) for a protected sector. Otherwise the device will read 00H for unprotected sector. In this mode, the lower order addresses, except for A0 and A1, are don't care. Address location 02H is reserved to verify sector protection of the device. Address pin A1 must be held at V_{IH} and A0 at V_{IL} (please refer to Table 3). Address location 00H and 01H are reserved for autoselect codes. If a verify of the sector protection circuitry were done at these addresses, the device would output the manufacturer and device codes respectively.

Table 4. Sector Addresses Table

	A16	A15	A14	Addr Range
SA0	0	0	0	00000h-03FFFh
SA1	0	0	1	04000h-07FFFh
SA2	0	1	0	08000h-0BFFFh
SA3	0	1	1	0C000h-0FFFFh
SA4	1	0	0	10000h-13FFFh
SA5	1	0	1	14000h-17FFFh
SA6	1	1	0	18000h-1BFFFh
SA7	1	1	1	1C000h-1FFFFh

It is also possible to determine if a sector is protected in the system by writing the autoselect command. Performing a read operation at particular sector addresses (A16, A15, A14) and with A1 = V_{IH} and A0 = V_{IL} (other addresses are a don't care) will produce 01H data if those sectors are protected. (Please refer to Table 3). Otherwise the device will read 00H for an unprotected sector. Please refer to the section on Sector Protection Algorithms for more details.

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Table 5 defines these register command sequences.

Table 5. Am29F010 Command Definitions

Command Sequence	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Autoselect	4	5555H	AAH	2AAAH	55H	5555H	90H	00H/01H	01H/20H				
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	PD				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H

Notes:

1. *Address bit A15 = X = Don't Care. Write Sequences may be initiated with A15 in either state.*
2. *Address bit A16 = X = Don't Care for all address commands except for Program Address (PA) and Sector Address (SA).*
3. *Bus operations are defined in Table 2.*
4. *RA = Address of the memory location to be read.*
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the sector to be erased. The combination of A16, A15, A14 will uniquely select any sector.
5. *RD = Data read from location RA during read operation.*
   PD = Data to be programmed at location PA. Data is latched on the falling edge of $\overline{WE}$.

Read/Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an autoselect operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XXX0H retrieves the manufacturer code of 01H. A read cycle from address XXX1H returns the device code 20H (see Table 3). A read cycle from address XXX2H returns information as to which sectors are protected. All manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit.

To terminate the operation, it is necessary to write the read/reset command sequence into the register.

Byte Programming

The device is programmed on a byte-by-byte basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence the system is *not* required to provide further controls or timings. The device will automatically provide internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to the read mode and addresses are no longer latched. Therefore, the device requires that a valid address to the device be supplied by the system at this particular time. Hence, $\overline{\text{Data}}$ Polling must be performed at the memory location which is being programmed.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so will hang up the device, or result in an apparent success according to the data polling algorithm. However, a read from reset/read mode will show that the data is still "0". Only erase operations can convert "0"s to "1"s.

Figure 1 illustrates the Embedded Programming Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does *not* require the user to program the device prior to erase. Upon executing the Embedded Erase™ Algorithm command sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to read the mode.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (data) is latched on the rising edge of $\overline{WE}$. A time-out of 80 µs from the rising edge of the last sector erase command will initiate the sector erase command(s).

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the Sector Erase command (30H) to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 80 µs, otherwise that command will not be accepted. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 80 µs from the rising edge of the last $\overline{WE}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{WE}$ occurs within the 80 µs time-out window, the timer is reset. (Monitor DQ3 to determine if the sector erase timer window is stil open, see section DQ3, Sector Erase Timer.) Any command other than Sector Erase during this period will reset the device to read mode, ignoring the previous command string. Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 7).

Sector erase does *not* require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is *not* required to provide any controls or timings during these operations.

The automatic sector erase begins after the 100 µs time out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to read mode. $\overline{Data}$ Polling must be performed at an address within any of the sectors being erased.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Write Operation Status

Table 6. Hardware Sequence Flags

	Status	DQ7	DQ6	DQ5	DQ3	DQ2–DQ0
In Progress	Auto-Programming	$\overline{DQ7}$	Toggle	0	0	Reserved for future use
	Program/Erase in Auto Erase	0	Toggle	0	1	
Exceeded Time Limits	Auto-Programming	$\overline{DQ7}$	Toggle	1	0	Reserved for future use
	Program/Erase in Auto-Erase	0	Toggle	1	1	

Note: *DQ4 for AMD internal use only.*

DQ7
$\overline{\text{Data}}$ Polling

The Am29F010 features $\overline{\text{Data}}$ Polling as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During the Embedded Programming Algorithm, an attempt to read the device will produce complement data of the data last written to DQ7. Upon completion of the Embedded Programming Algorithm an attempt to read the device will produce the true data last written to DQ7. $\overline{\text{Data}}$ Polling is valid after the rising edge of the fourth $\overline{\text{WE}}$ pulse in the four write pulse sequence.

During the Embedded Erase Algorithm, DQ7 will be "0" until the erase operation is completed. Upon completion data at DQ7 is "1". For chip erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For sector erase, the $\overline{\text{Data}}$ Polling is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse.

The $\overline{\text{Data}}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time-out (see Table 6).

See Figure 11 for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

DQ6
Toggle Bit

The Am29F010 also features the "Toggle Bit" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{OE}}$ toggling) data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on the next successive attempt. During programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{\text{WE}}$ pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. The Toggle Bit is active during the sector time out.

It should be noted that either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause DQ6 to toggle. See Figure 12 for the Toggle Bit timing specifications and diagrams.

DQ5
Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ5 will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the device under this condition. The $\overline{\text{CE}}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in Table 2.

If this failure condition occurs during the sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for additional program or erase operations. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute the program or erase command sequence.

If this failure condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this failure condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused (other sectors are still functional and can be reused). The device must be reset to use other sectors.

The DQ5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the system never reads valid data on the DQ7 bit and DQ6 never stops toggling. Once the device has exceeded timing limits, the DQ5 bit will indicate a "1." Please note that this is not a device failure condition since the device was incorrectly used. The device must be reset to continue using the device.

DQ3
Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ3 will remain low until the time-out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence is completed.

If $\overline{\text{Data}}$ Polling or the Toggle Bit indicates that the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit. If DQ3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 were high on the second status check, the command may not have been accepted.

PARALLEL DEVICE ERASURE

Since the device is completely self-timed, devices can be erased or programmed in parallel without consideration of other devices in the system.

Data Protection

The Am29F010 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features described below to prevent inadvertent write cycles resulting from Vcc power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when Vcc is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$, or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

Sector Protect

Sectors of the Am29F010 may be hardware protected at the users factory. The protection circuitry will disable both program and erase functions for the protected sector(s). Requests to program or erase a protected sector will be ignored by the device.

EMBEDDED ALGORITHMS

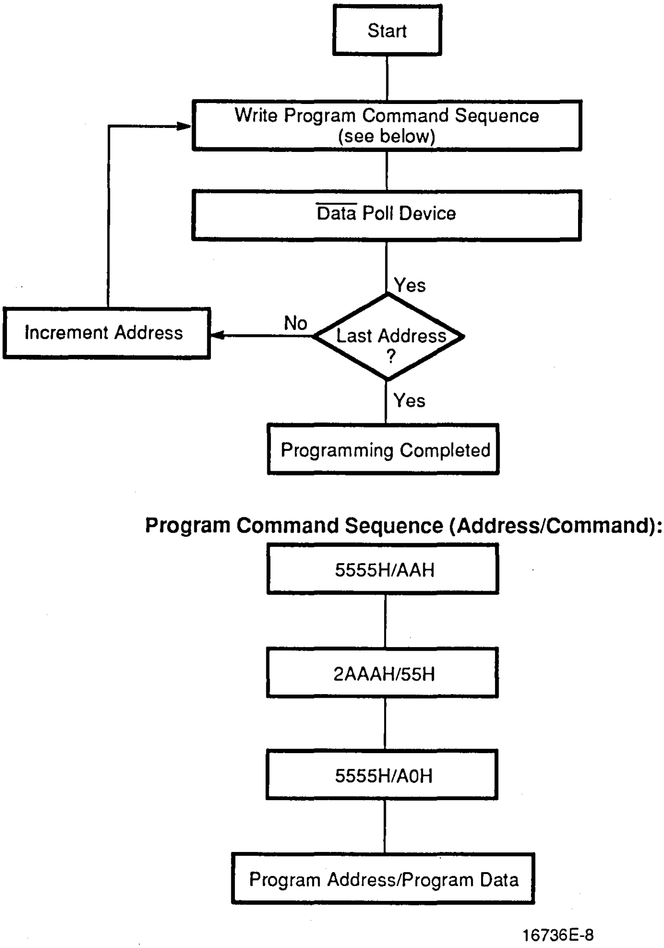


Figure 1. Embedded Programming Algorithm

Table 7. Embedded Programming Algorithm

Bus Operations	Command Sequence	Comments
Standby		
Write	Embedded Programming Algorithm	Valid Address/Data Sequence
Read		$\overline{\text{Data}}$ Polling to Verify Programming

EMBEDDED ALGORITHMS

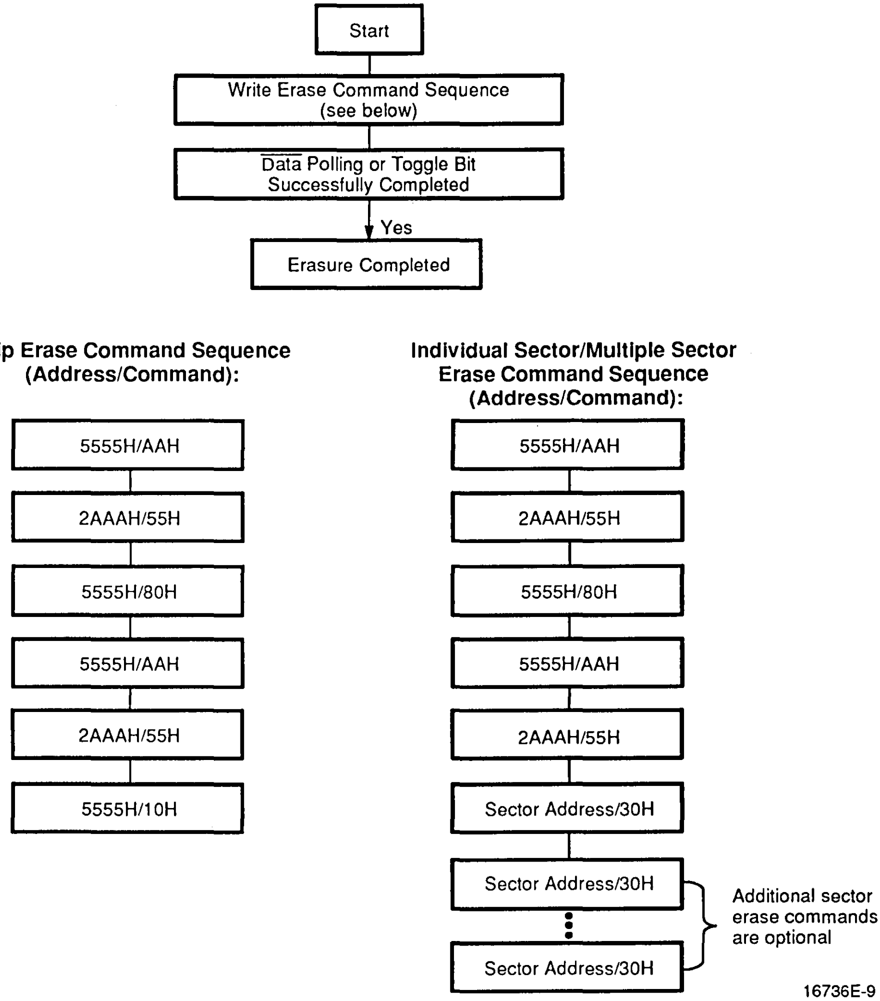
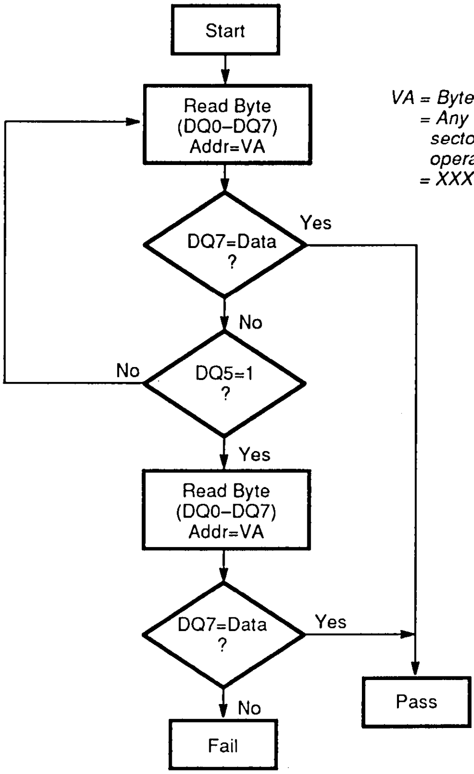


Figure 2. Embedded Erase Algorithm

Table 8. Embedded Erase Algorithm

Bus Operations	Command Sequence	Comments
Standby		
Write	Embedded Erase Algorithm	
Read		$\overline{\text{Data}}$ Polling to Verify Erasure



VA = Byte address for programming
= Any of the sector addresses within the sector being erased during sector erase operation
= XXXXH during chip erase

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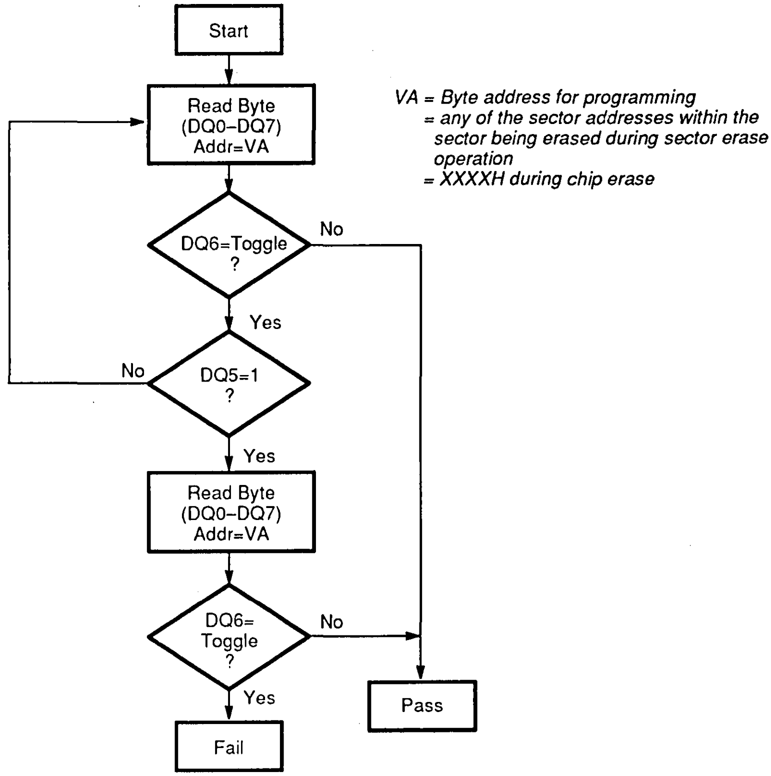
Note:
1. *DQ7 is rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 3. $\overline{\text{Data}}$ Polling Algorithm



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Note:

1. *DQ6 is rechecked even if DQ5 = "1" because DQ6 may stop toggling at the same time as DQ5 changing to "1".*

Figure 4. Toggle Bit Algorithm

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages . . . . –65°C to +150°C
Plastic Packages . . . . –65°C to +125°C

Ambient Temperature
with Power Applied . . . . –55°C to + 125°C

Voltage with Respect To Ground
All pins except A9 (Note 1) . . . . –2.0 V to +7.0 V

V_{CC} (Note 1) . . . . –2.0 V to +7.0 V

A9 (Note 2) . . . . –2.0 V to +14.0 V

Output Short Circuit Current (Note 3) . . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A9 pin is –0.5 V. During voltage transitions, A9 may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) . . . . 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) . . . . –40°C to +85°C

Extended (E) Devices
Case Temperature (T_C) . . . . –55°C to +125°C

Military (M) Devices
Case Temperature (T_C) . . . . –55°C to +125°C

V_{CC} Supply Voltages
V_{CC} for Am29F010-45 . . . . +4.75 V to +5.25 V

V_{CC} for Am29F010-55, 70,
90, 120 . . . . +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

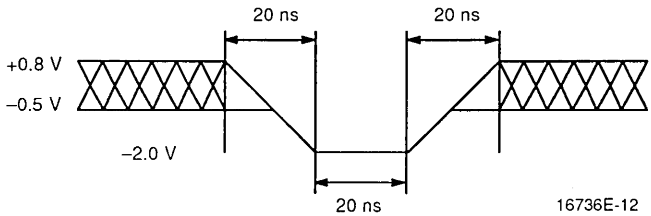


Figure 5. Maximum Negative Overshoot Waveform

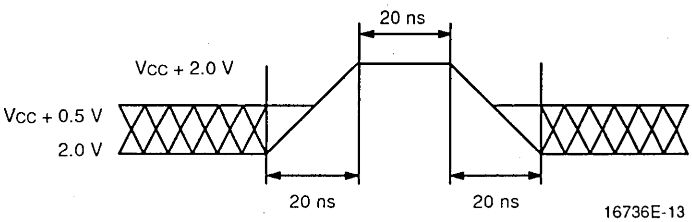


Figure 6. Maximum Positive Overshoot Waveform

DC CHARACTERISTICS—TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		± 1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.5 V		50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		± 1.0	µA
I_{CC1}	V_{CC} Active Current for Read (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	mA
I_{CC2}	V_{CC} Active Current for Program or Erase (Notes 2, 3)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		50	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IH}$		1.0	mA
V_{IL}	Input Low Level		–0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.5	V
V_{ID}	A9 Voltage for Autoselect	V_{CC} = 5.0 V	11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, $V_{CC} = V_{CC}$ Min		0.45	V
V_{OH}	Output High Level	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min	2.4		V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2		V

Notes:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *I_{CC} active while Embedded Algorithm (program or erase) is in progress.*
3. *Not 100% tested.*

DC CHARACTERISTICS—CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{LI}	Input Load Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{SS}$ to V_{CC}		±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.5 V		50	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{SS}$ to V_{CC}		±1.0	µA
I_{CC1}	V_{CC} Active Current for Read (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	mA
I_{CC2}	V_{CC} Active Current for Program or Erase (Notes 2, 3)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		50	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{CC} \pm 0.5$ V		100	µA
V_{IL}	Input Low Level		–0.5	0.8	V
V_{IH}	Input High Level		0.7 V_{CC}	V_{CC} +0.5	V
V_{ID}	A9 Voltage for Autoselect	$V_{CC} = 5.0$ V	11.5	12.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 12.0$ mA $V_{CC} = V_{CC}$ Min		0.45	V
V_{OH1}		$I_{OH} = -2.5$ mA, $V_{CC} = V_{CC}$ Min	0.85 V_{CC}		V
V_{OH2}	Output High Voltage	$I_{OH} = -100$ µA, $V_{CC} = V_{CC}$ Min	V_{CC}–0.4		V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2		V

Notes:

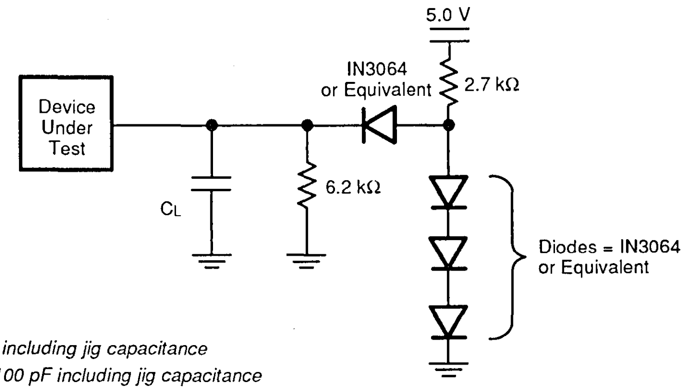
1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *I_{CC} active while Embedded Algorithm (program or erase) is in progress.*
3. *Not 100% tested.*

AC CHARACTERISTICS—READ ONLY OPERATIONS CHARACTERISTICS

Parameter Symbols JEDEC	Parameter Symbols Standard	Description	Test Setup		-45 (1)	-55 (2)	-70 (2)	-90 (2)	-120 (2)	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)		Min	45	55	70	90	120	ns
t_{AVQV}	t_{ACC} (max)	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max	45	55	70	90	120	ns
t_{ELQV}	t_{CE} (max)	Chip Enable to Output	$\overline{OE} = V_{IL}$	Max	45	55	70	90	120	ns
t_{GLQV}	t_{OE} (max)	Output Enable to Output		Max	25	30	30	35	50	ns
t_{EHQZ}	t_{DF} (max)	Chip Enable to Output High Z (Notes 3, 4)		Max	10	15	20	20	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 3, 4)		Max	10	15	20	20	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		Max	0	0	0	0	0	ns

Notes:

1. *Test Conditions:*
   Output Load: 1 TTL gate and 30 pF
   Input rise and fall times: 5 ns
   Input pulse levels: 0.0 V to 3.0 V
   Timing measurement reference level
   Input: 1.5 V
   Output: 1.5 V
2. *Test Conditions:*
   Output Load: 1 TTL gate and 100 pF
   Input rise and fall times: 20 ns
   Input pulse levels: 0.45 V to 2.4 V
   Timing measurement reference level
   Input: 0.8 and 2.0 V
   Output: 0.8 and 2.0 V
3. *Output driver disable time.*
4. *Not 100% tested.*



Note:

For –45: C_L = 30 pF including jig capacitance
For all others: C_L = 100 pF including jig capacitance

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Figure 7. Test Conditions

AC CHARACTERISTICS—WRITE/ERASE/PROGRAM OPERATIONS

Parameter Symbol JEDEC	Parameter Symbol Standard	Description			-45	-55	-70	-90	-120	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 4)		Min	45	55	70	90	120	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	35	45	45	45	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	20	20	30	45	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time		Min	0	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read (Note 4)	Min	0	0	0	0	0	ns
			Toggle and $\overline{\text{Data}}$ Polling (Note 4)	Min	10	10	10	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write		Min	0	0	0	0	0	ns
t_{ELWL}	t_{CS}	$\overline{\text{CE}}$ Setup Time		Min	0	0	0	0	0	ns
t_{WHEH}	t_{CH}	$\overline{\text{CE}}$ Hold Time		Min	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	25	30	35	45	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	20	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation		Min	14	14	14	14	14	µs
t_{WHWH2}	t_{WHWH2}	Erase Operation (Note 1)		Min	2.2	2.2	2.2	2.2	2.2	sec
	t_{VCS}	V_{CC} Set Up Time (Note 4)		Min	50	50	50	50	50	µs
	t_{VLHT}	Voltage Transition Time (Notes 2, 4)		Min	4	4	4	4	4	µs
	t_{WPP}	Write Pulse Width (Note 2)		Min	10	10	10	10	10	ms
	t_{OESP}	$\overline{\text{OE}}$ Setup Time to $\overline{\text{WE}}$ Active (Notes 2, 4)		Min	4	4	4	4	4	µs
	t_{CSP}	$\overline{\text{CE}}$ Setup Time to $\overline{\text{WE}}$ Active (Notes 3, 4)		Min	4	4	4	4	4	µs

Notes:

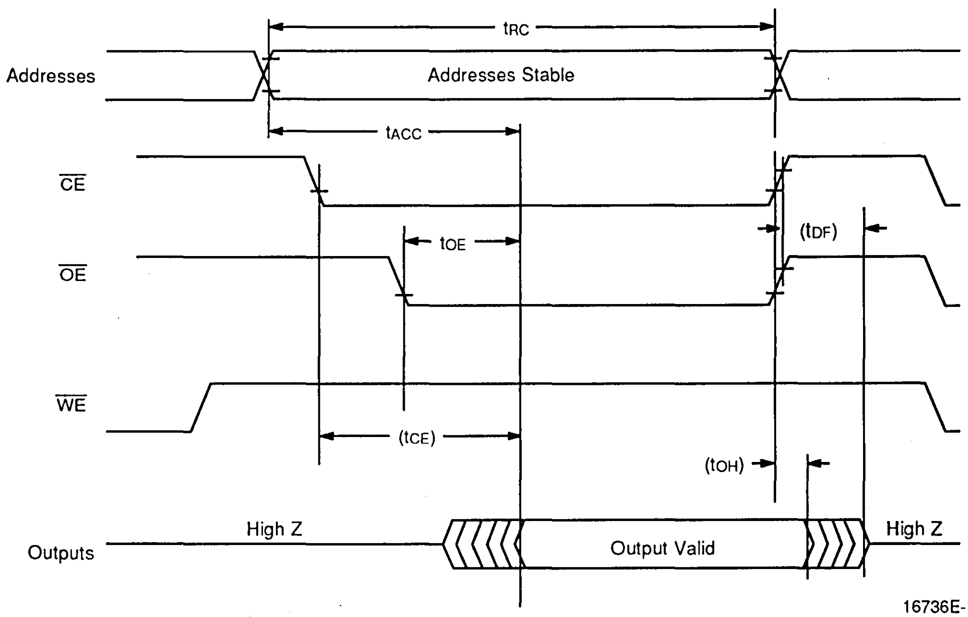
1. *This also includes the preprogramming time.*
2. *These timings are for Sector Protect/Unprotect operations.*
3. *This timing is only for Sector Unprotect.*
4. *Not 100% tested.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

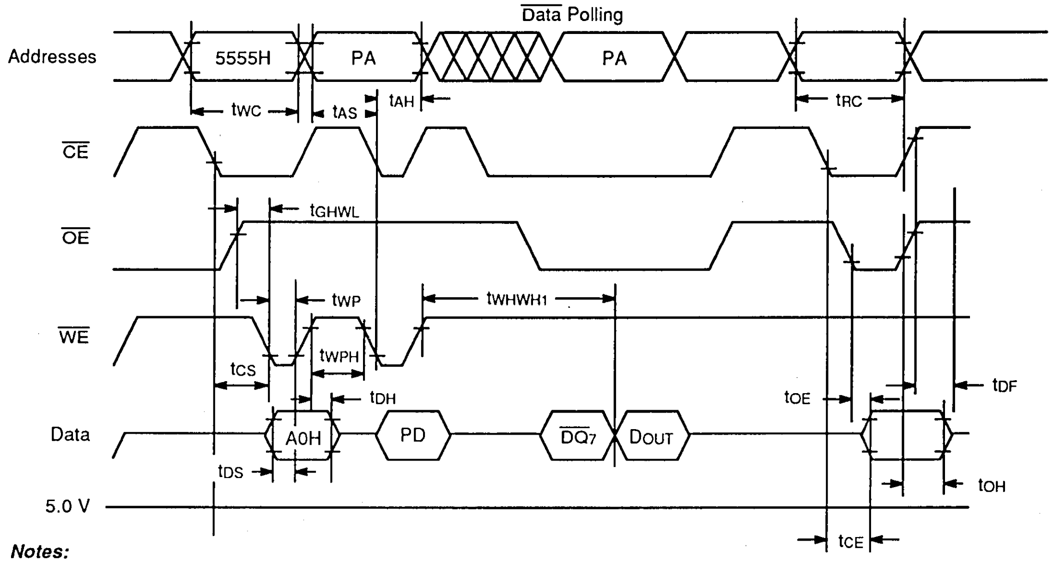
SWITCHING WAVEFORMS



16736E-15

Figure 8. AC Waveforms for Read Operations

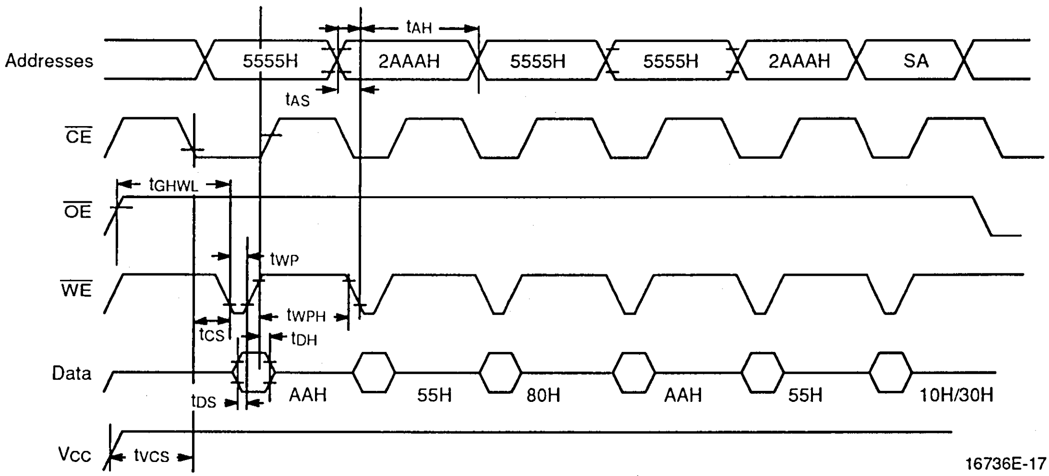
SWITCHING WAVEFORMS



Notes:

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
4. *DOUT is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*

Figure 9. Program Operation Timings

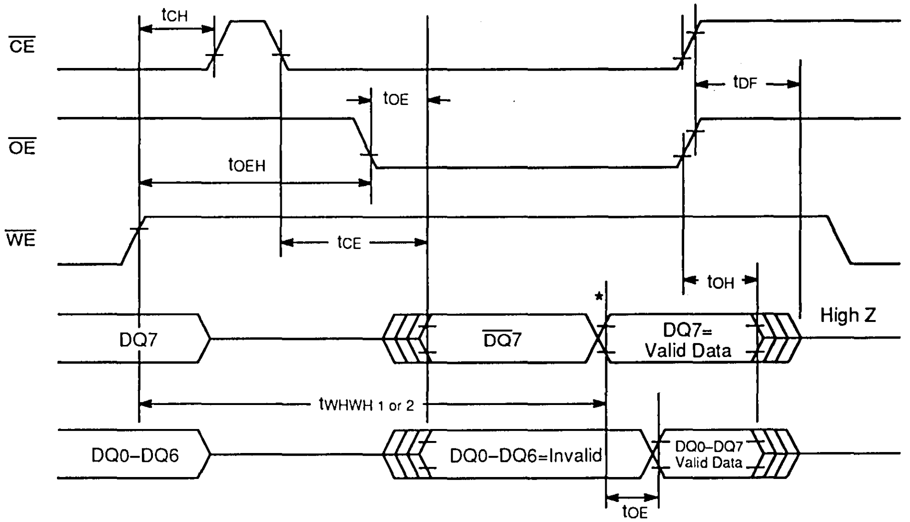


Note:

1. *SA is the sector address for Sector Erase. Addresses = don't care for Chip Erase.*

Figure 10. AC Waveforms Chip/Sector Erase Operations

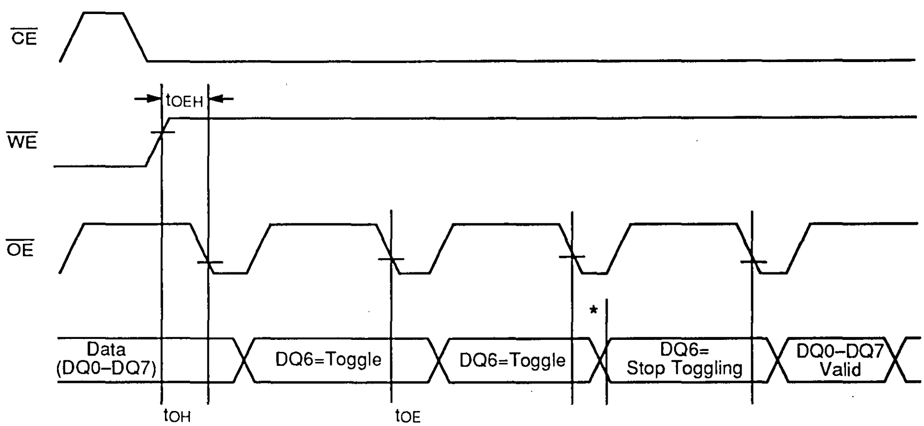
SWITCHING WAVEFORMS



DQ7=Valid Data (The device has completed the Embedded operation).

16736E-18

Figure 11. AC Waveforms for Data Polling During Embedded Algorithm Operations



16736E-19

Note:

**DQ6 stops toggling (The device has completed the Embedded operation).*

Figure 12. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

SECTOR PROTECTION ALGORITHMS

Sector Protection

The Am29F010 features hardware sector protection which will disable both program and erase operations to an individual sector or any group of sectors. To activate this mode, the programming equipment must force V_{ID} on control pin $\overline{OE}$ and address pin A9. The sector addresses should be set using higher address lines A16, A15, and A14. The protection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to verify if a sector is protected during the sector protection operation. This is done by setting $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH} (A9 remains high at V_{ID}). Reading the device at address location XXX2H, where the higher order addresses (A16, A15, and A14) define a particular sector, will produce 01H at data outputs (DQ0–DQ7) for a protected sector.

Sector Unprotect

The Am29F010 also features a sector unprotect mode, so that a protected sector may be unprotected to incorporate any changes in the code. All sectors should be protected prior to unprotecting any sector.

To activate this mode, the programming equipment must force V_{ID} on control pins $\overline{OE}$, $\overline{CE}$, and address pin A9. The address pins A6, A7, and A12 should be set to A7 = A12 = V_{IH}, and A6 = V_{IL}. The unprotection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to determine if a sector is unprotected in the system by writing the autoselect command. Performing a read operation at address location XXX2H, where the higher order addresses (A16, A15, and A14) define a particular sector address, will produce 00H at data outputs (DQ0–DQ7) for an unprotected sector.

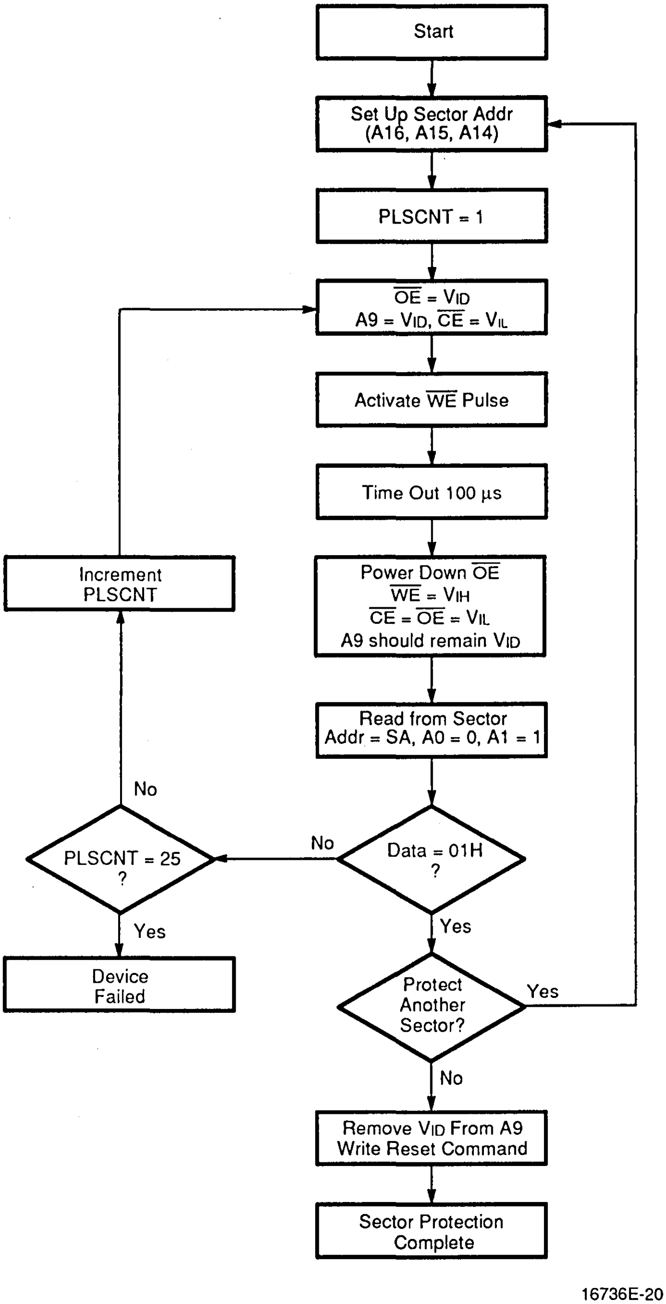


Figure 13. Sector Protection Algorithm

SWITCHING WAVEFORMS

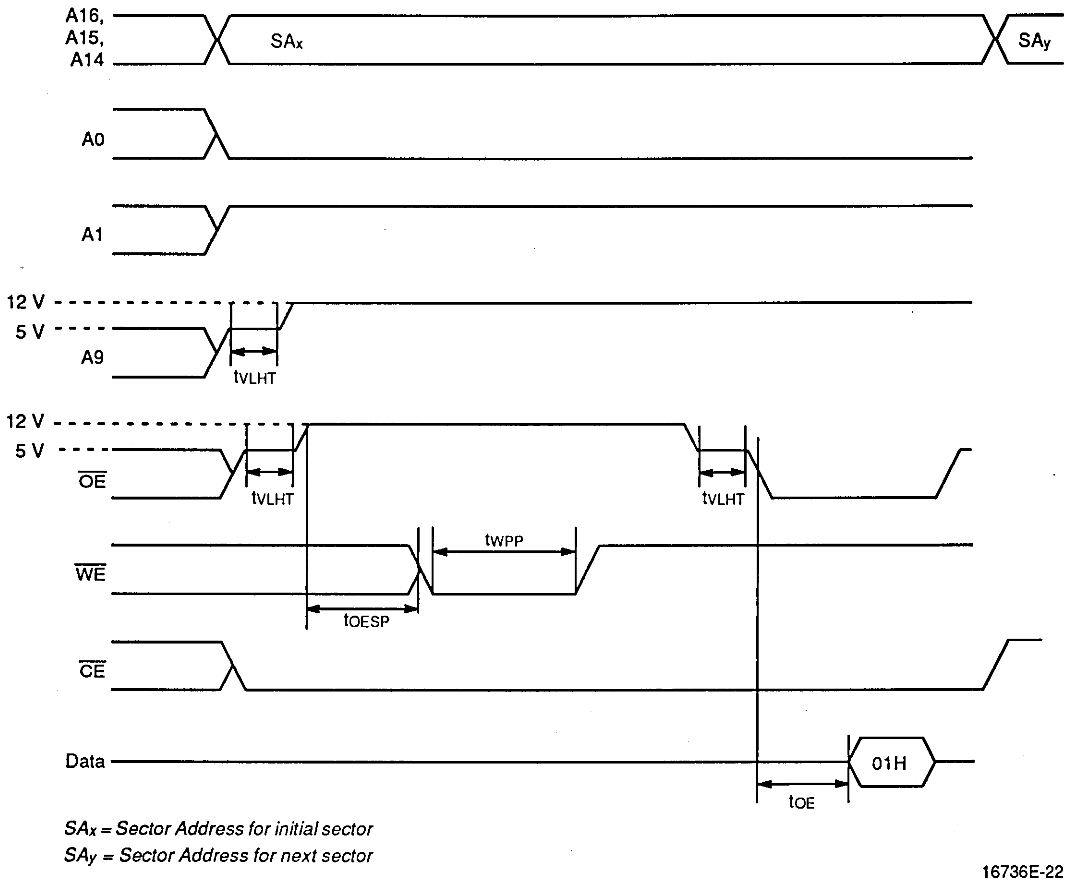
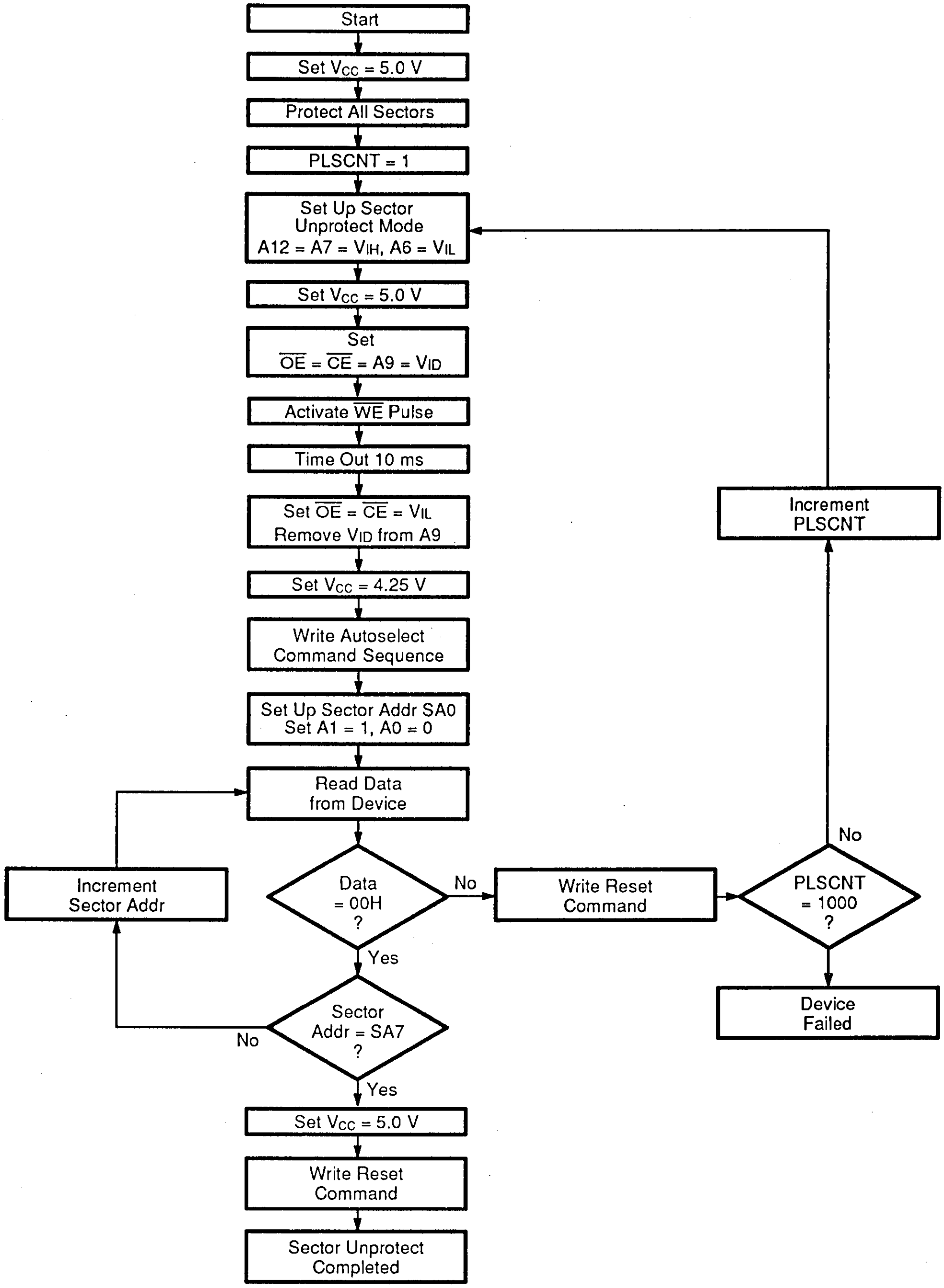


Figure 14. AC Waveforms for Sector Protection



Notes:
SA0 = Sector Address for initial sector
SA7 = Sector Address for last sector
Please refer to Table 4 for details.

Figure 15. Sector Unprotect Algorithm

SWITCHING WAVEFORMS

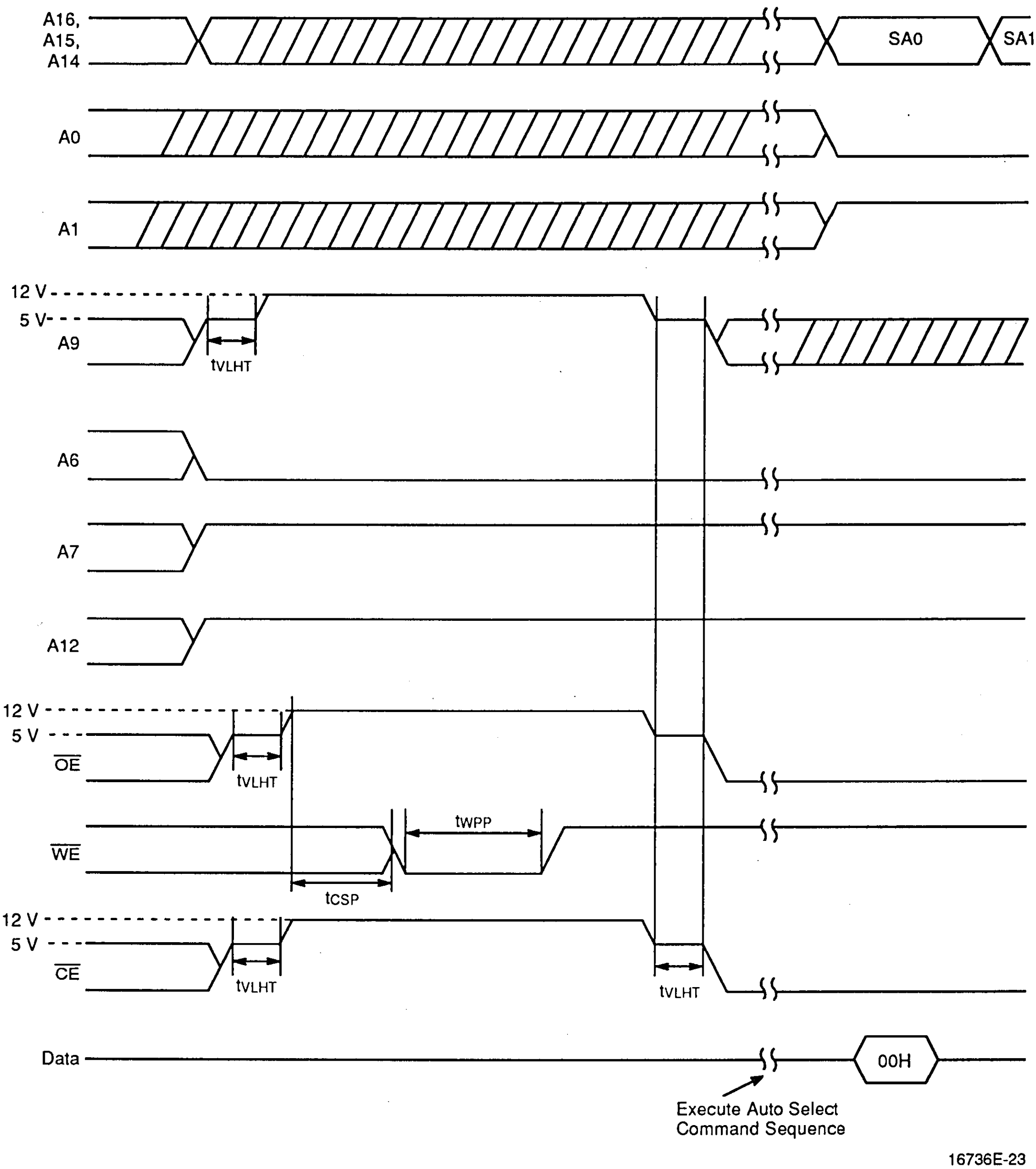


Figure 16. AC Waveforms for Sector Unprotect

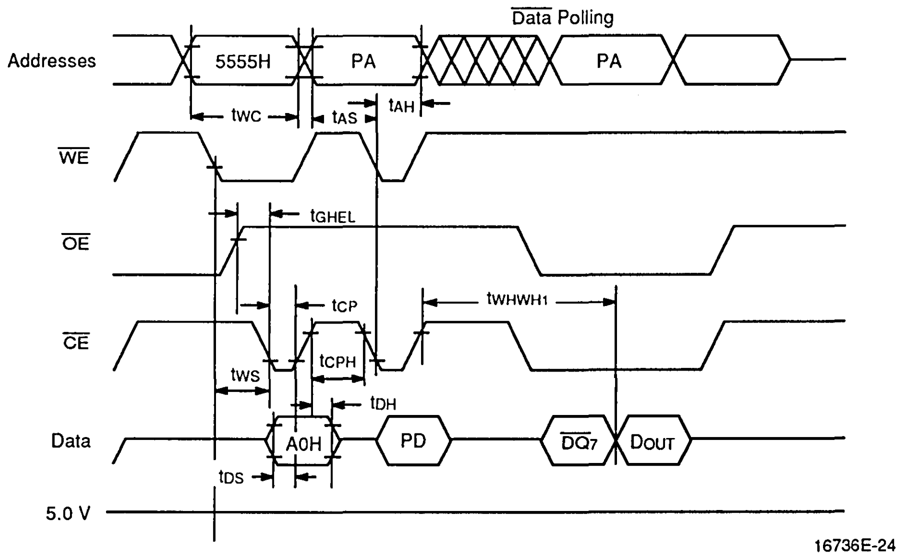
AC CHARACTERISTICS—WRITE/ERASE/PROGRAM OPERATIONS

Alternate $\overline{CE}$ Controlled Writes

Parameter Symbol JEDEC	Parameter Symbol Standard	Description			-45	-55	-70	-90	-120	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 2)		Min	45	55	70	90	120	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	35	45	45	45	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	20	20	30	45	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time		Min	0	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read (Note 2)	Min	0	0	0	0	0	ns
			Toggle and $\overline{Data}$ Polling (Note 2)	Min	10	10	10	10	10	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write		Min	0	0	0	0	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time		Min	0	0	0	0	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		Min	0	0	0	0	0	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width		Min	25	30	35	45	50	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High		Min	20	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation		Min	14	14	14	14	14	µs
t_{WHWH2}	t_{WHWH2}	Erase Operation (Note 1)		Min	2.2	2.2	2.2	2.2	2.2	sec
	t_{VCS}	V_{CC} Set Up Time (Note 2)		Min	2	2	2	2	2	µs

Notes:

1. *This also includes the preprogramming time.*
2. *Not 100% tested.*



Notes:

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
4. *DOUT is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*

Figure 17. Alternate $\overline{CE}$ Controlled Program Operation Timings

ERASE AND PROGRAMMING PERFORMANCE (Note 2)

Parameter	Limits Min	Typ	Max	Unit	Comments
Chip/Sector Erase Time		1	10 (Note 1)	sec	Excludes 00H programming prior to erasure
Sector Programming Time		0.3		sec	
Chip Programming Time		2	12.5	sec	Excludes system-level overhead
Erase/Program Cycles	100,000	1,000,000		Cycles	
Byte Program Time		14		µs	
			60 (Notes 3, 4)	ms	

Notes:

1. *The Embedded Algorithm allows for 60 second erase time for military temperature range operations.*
2. *The Embedded Algorithms allow for a longer chip program and erase time. However, the actual time will be considerably less since bytes program or erase significantly faster than the worst case byte.*
3. *DQ5 = "1" only after a byte takes longer than 60 ms to program.*
4. *A minimal number of bytes may require significantly more programming pulses then the typical byte. The majority of bytes will program within one or two pulses. This is demonstrated by the Typical and Maximum Chip Programming Times listed above.*

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A9)	–1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
Current	–100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

LCC PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz*

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	6	7.5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	8.5	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	7.5	9	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz*

PLCC PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	Control Pin Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A = 25°C$, $f = 1.0$ MHz*

PDIP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	Control Pin Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A = 25°C$, $f = 1.0$ MHz*

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

Data Sheet Revision Summary for Am29F010

Title

Data sheet is now Final, and not Preliminary.

Specify "1 Megabit" density.

General Description

Include statement "Am29F040 is erased when shipped from factory."

Write Operation Status, Table 6. Hardware Sequence Flags

Remove listing of DQ4 and made DQ4 as AMD's internal use only.

Remove paragraph on DQ4, Hardware Sequence Flag.

DC Characteristics TTL/NMOS Compatible

Add parameter I_{LIT}: "A9 Input Load Current"

Delete parameter I_{OS}: Output Short Curcuit Current.

DC Characteristics: CMOS Compatible

Add parameter I_{LIT}: "A9 Input Load Current."

Delete parameter I_{OS}: Output Short Curcuit Current.

AC Characteristics: Write/Erase/Program Operations

Correct t_{VCS}: V_{CC} Set Up Time from 2 m to 50 m.

Figure 13. Sector Protect Algorithm Flow Chart

Correct Time Out value from 10 m to 100 m.

Am29F100T/Am29F100B

1 Megabit (131,072 x 8-Bit/65,536 x 16-Bit) CMOS 5.0 Volt-only, Sector Erase Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% read, write, and erase**
  - — Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  - — Uses same software commands as E^2PROMs
- **Compatible with JEDEC-standard word-wide pinouts**
  - — 44-pin SO
  - — 48-pin TSOP
- **Minimum 100,000 write/erase cycles**
- **High performance**
  - — 70 ns maximum access time
- **Sector erase architecture**
  - — One 16 Kbyte, two 8 Kbytes, one 32 Kbyte, and one 64 Kbyte
  - — Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Embedded Erase Algorithms**
  - — Automatically pre-programs and erases the chip or any sector
- **Embedded Program Algorithms**
  - — Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Low power consumption**
  - — 20 mA typical active read current for Byte Mode
  - — 28 mA typical active read current for Word Mode
  - — 30 mA typical write/erase current
  - — 25 µA typical standby current
- **Low V_{CC} write inhibit ≤ 3.2 V**
- **Sector protection**
  - — Hardware method disables any combination of sectors from write or erase operations
- **Erase Suspend/Resume**
  - — Suspend the erase operation to allow a read in another sector within the same device
- **Boot Code Sector Architecture**
  - — T = Top sector
  - — B = Bottom sector

GENERAL DESCRIPTION

The Am29F100 is a 1 Mbit, 5.0 V-only Flash memory organized as 128K bytes of 8 bits each or 64K words of 16 bits each. The Am29F100 is offered in 44-pin SO and 48-pin TSOP packages. This device is designed to be programmed in-system with the standard system 5.0 V V_{CC} supply. A 12.0 V V_{PP} is not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers. The Am29F100 is erased when shipped from the factory.

The standard Am29F100 offers access times between 70 ns and 150 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$) and output enable ($\overline{OE}$) controls.

The Am29F100 is pin and command set compatible with JEDEC standard 1 Mbit E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

PRODUCT SELECTOR GUIDE

Family Part No:	**Am29F100**			
Ordering Part No: V_{CC} = 5.0 V ± 5%	**-75**			
V_{CC} = 5.0 V ± 10%		**-90**	**-120**	**-150**
Max Access Time (ns)	70	90	120	150
$\overline{CE}$ ($\overline{E}$) Access (ns)	70	90	120	150
$\overline{OE}$ ($\overline{G}$) Access (ns)	30	35	50	55

Publication# 18926 Rev. A Amendment/0
Issue Date: March 1994

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

The Am29F100 is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than one second. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The entire chip or any individual sector is typically erased and verified in 1.5 seconds (if already completely preprogrammed).

This device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors.

The device features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ7, by the Toggle Bit feature on DQ6, or the RY/$\overline{\text{BY}}$ pin. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

AMD's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability and cost effectiveness. The Am29F100 memory electrically erases the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

Flexible Sector-Erase Architecture

- One 16 Kbyte, two 8 Kbytes, one 32 Kbyte, and one 64 Kbyte
- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user definable

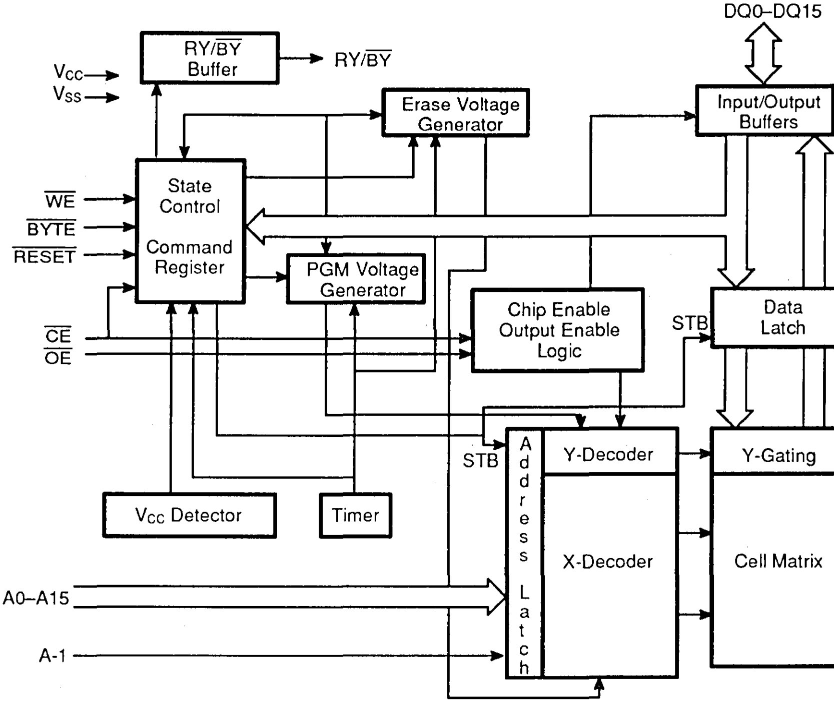
Sector	Address
	1FFFFh
16 Kbyte	
	1BFFFh
8 Kbyte	
	19FFFh
8 Kbyte	
	17FFFh
32 Kbyte	
	0FFFFh
64 Kbyte	
	00000h

Am29F100T Sector Architecture 18926A-1

Sector	Address
	1FFFFh
64 Kbyte	
	0FFFFh
32 Kbyte	
	07FFFh
8 Kbyte	
	05FFFh
8 Kbyte	
	03FFFh
16 Kbyte	
	00000h

Am29F100B Sector Architecture 18926A-2

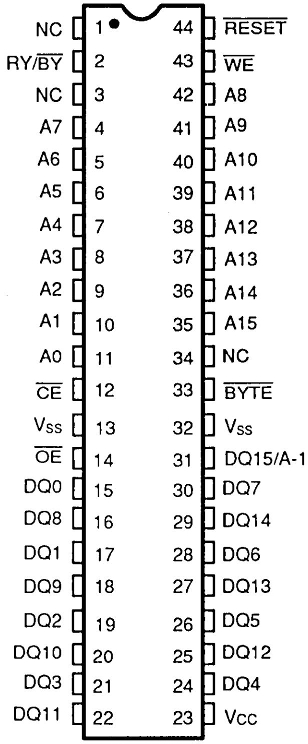
BLOCK DIAGRAM



18926A-3

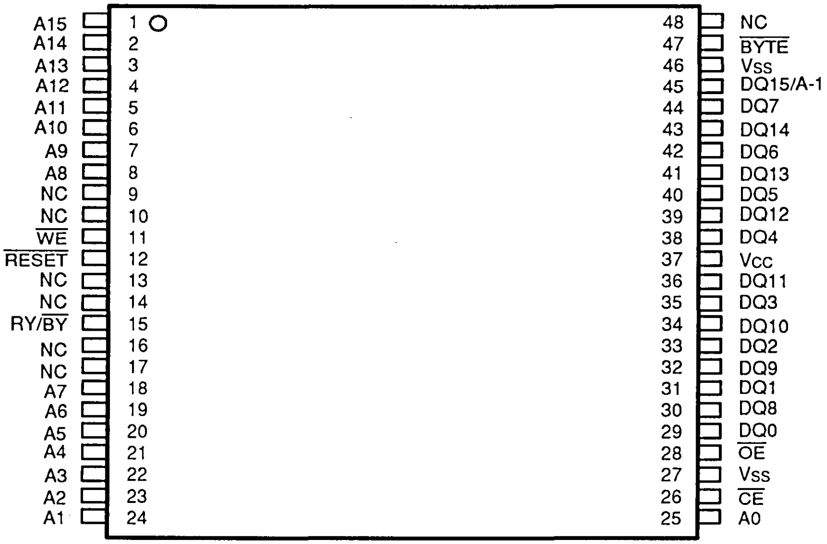
CONNECTION DIAGRAMS

SO



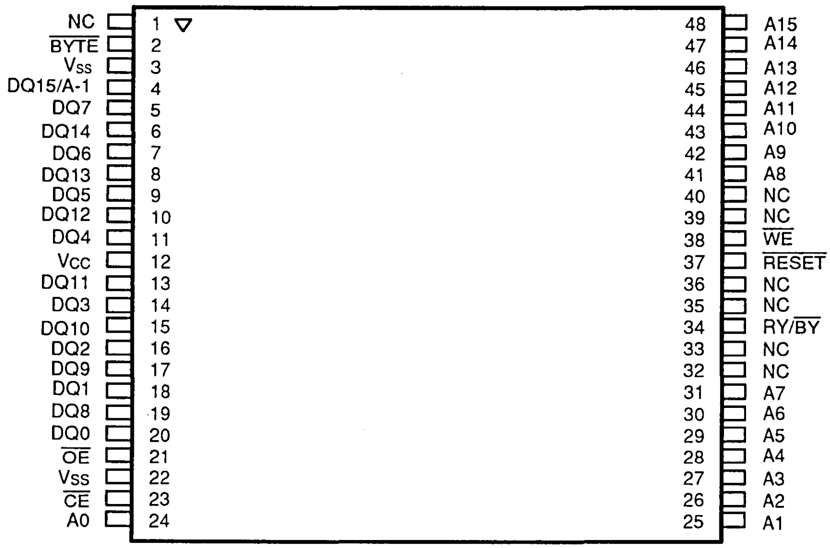
18926A-4

CONNECTION DIAGRAMS



Standard TSOP

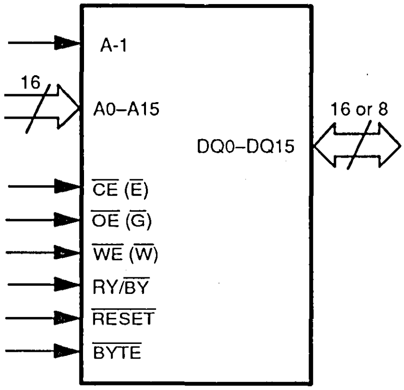
18926A-5



Reverse TSOP

18926A-6

LOGIC SYMBOL



18926A-7

Table 1. Am29F100 Pin Configuration

Pin	Function
A-1, A0–A15	Address Inputs
DQ0–DQ15	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RY/$\overline{BY}$	Ready-Busy Input
$\overline{RESET}$	Hardware Reset Pin/Sector Protect Unlock
$\overline{BYTE}$	Selects 8-bit or 16-bit mode
NC	No Internal Connection
V_{SS}	Device Ground
V_{CC}	Device Power Supply (5.0 V ± 10% or ± 5%)

PRELIMINARY

Am29F200T/Am29F200B

2 Megabit (262,144 x 8-Bit/131,072 x 16-Bit) CMOS 5.0 Volt-only, Sector Erase Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% write and erase, read**
  — Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  — Uses same software commands as E^2PROMs
- **Compatible with JEDEC-standard word-wide pinouts**
  — 44-pin SO
  — 48-pin TSOP
- **Minimum 100,000 write/erase cycles**
- **High performance**
  — 70 ns maximum access time
- **Sector erase architecture**
  — Three 64 Kbytes, one 32 Kbyte, one 16 Kbyte and two 8 Kbytes
  — Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Embedded Erase Algorithms**
  — Automatically pre-programs and erases the chip or any sector
- **Embedded Program Algorithms**
  — Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Low power consumption**
  — 20 mA typical active read current for Byte Mode
  — 28 mA typical active read current for Word Mode
  — 30 mA typical write/erase current
  — 25 µA typical standby current
- **Low V_{CC} write inhibit ≤ 3.2 V**
- **Sector protection**
  — Hardware method disables any combination of sectors from write or erase operations
- **Erase Suspend/Resume**
  — Suspends the erase operation to allow a read in another sector within the same device
- **Boot Code Sector Architecture**
  — T = Top sector
  — B = Bottom sector

GENERAL DESCRIPTION

The Am29F200 is a 2 Mbit, 5.0 V-only Flash memory organized as 256K bytes of 8 bits each or 128K words of 16 bits each. The Am29F200 is offered in 44-pin SO and 48-pin TSOP packages. This device is designed to be programmed in-system with the standard system 5.0 V V_{CC} supply. A 12.0 V V_{PP} is not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers. The Am29F200 is erased when shipped from the factory.

The standard Am29F200 offers access times between 70 ns and 150 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$) and output enable ($\overline{OE}$) controls.

The Am29F200 is pin and command set compatible with JEDEC standard 2 Mbit E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

PRODUCT SELECTOR GUIDE

Family Part No:		**Am29F200**			
Ordering Part No:	V_{CC} = 5.0 V ± 5%	**-75**			
	V_{CC} = 5.0 V ± 10%		**-90**	**-120**	**-150**
Max Access Time (ns)		70	90	120	150
$\overline{CE}$ ($\overline{E}$) Access (ns)		70	90	120	150
$\overline{OE}$ ($\overline{G}$) Access (ns)		30	35	50	55

Publication# 18608 Rev. A Amendment/0
Issue Date: March 1994

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

The Am29F200 is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than one second. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The entire chip or any individual sector is typically erased and verified in 1.5 seconds (if already completely preprogrammed).

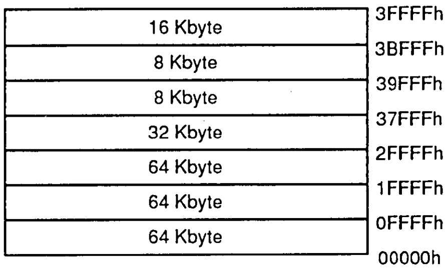
This device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors.

The device features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ7, by the Toggle Bit feature on DQ6, or the RY/$\overline{\text{BY}}$ pin. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

AMD's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability and cost effectiveness. The Am29F200 memory electrically erases the entire chip or all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

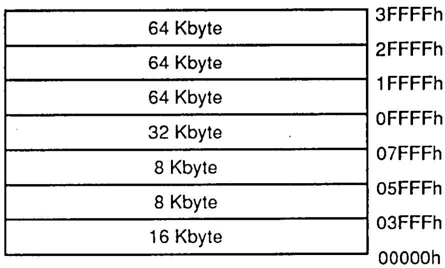
Flexible Sector-Erase Architecture

- Three 64 Kbytes, one 32 Kbyte, one 16 Kbyte, and two 8 Kbytes
- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user-definable



Am29F200T Sector Architecture

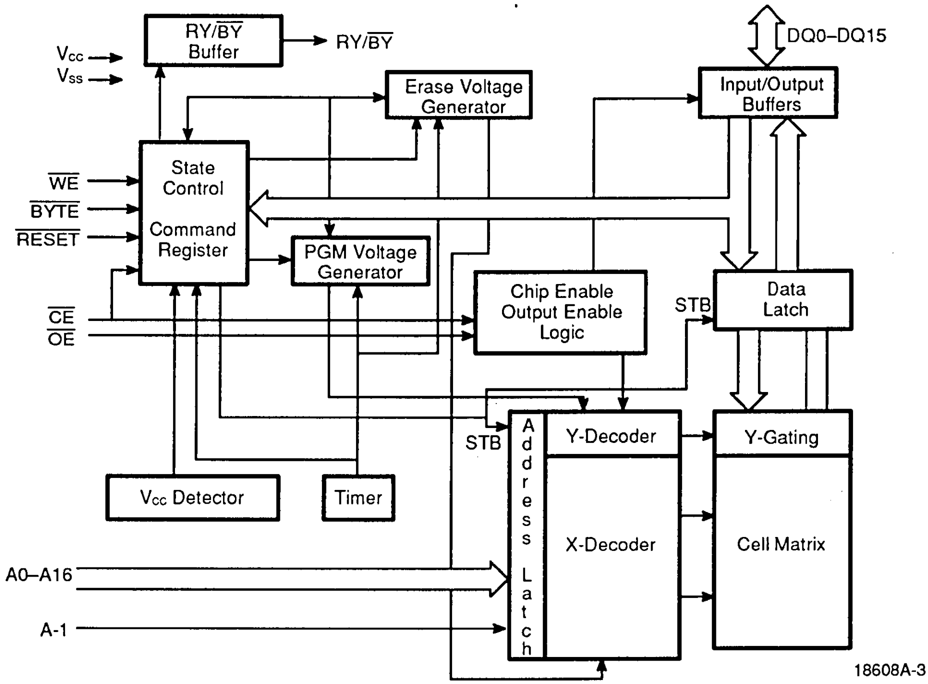
18608A-1



Am29F200B Sector Architecture

18608A-2

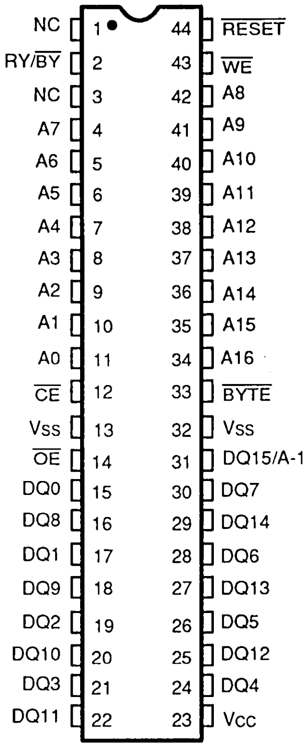
BLOCK DIAGRAM



18608A-3

CONNECTION DIAGRAMS

SO



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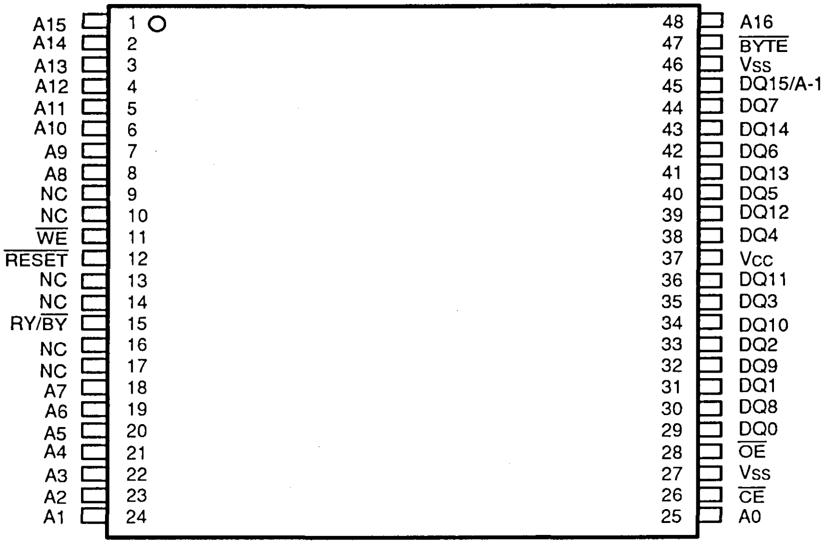
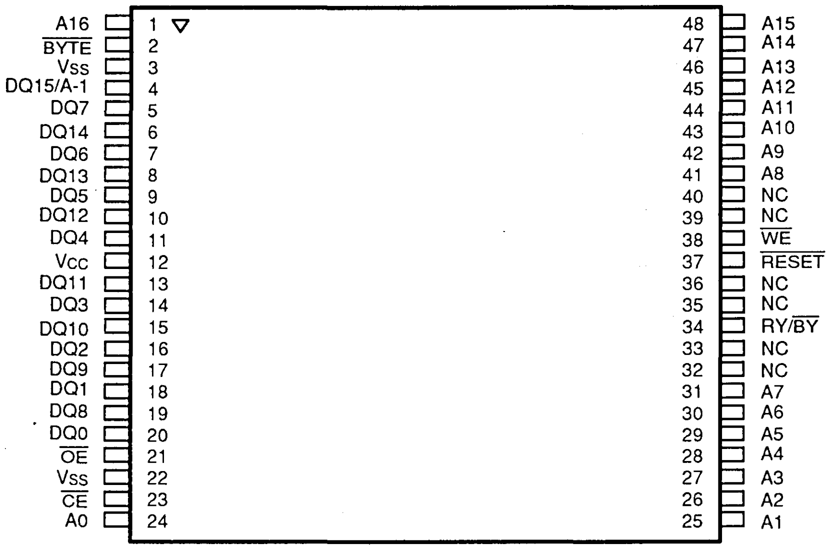
CONNECTION DIAGRAMS



18608A-5

Standard TSOP



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Reverse TSOP

LOGIC SYMBOL

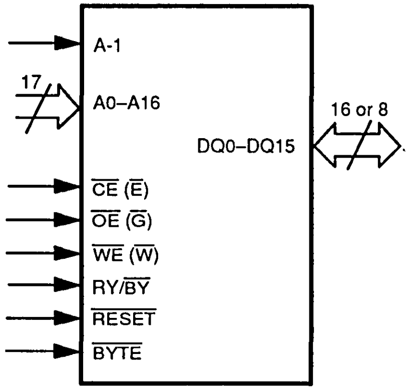

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Table 1. Am29F200 Pin Configuration

Pin	Function
A-1, A0–A16	Address Inputs
DQ0–DQ15	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RY/$\overline{BY}$	Ready-Busy Input
$\overline{RESET}$	Hardware Reset Pin/Sector Protect Unlock
$\overline{BYTE}$	Selects 8-bit or 16-bit mode
NC	No Internal Connection
Vss	Device Ground
Vcc	Device Power Supply (5.0 V ± 10% or ± 5%)

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

Am29F200 T -75 E C B

OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-In

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended (–55°C to +125°C)

PACKAGE TYPE
E = 48-Pin Thin Small Outline Package (TSOP) Standard Pinout (TS 048)
F = 48-Pin Thin Small Outline Package (TSOP) Reverse Pinout (TSR 048)
S = 44-Pin Small Outline Package, (SO 044)

SPEED OPTION
See Product Selector Guide and Valid Combinations

BOOT CODE SECTOR ARCHITECTURE
T = Top sector
B = Bottom sector

DEVICE NUMBER/DESCRIPTION
Am29F200
2 Megabit (256K x 8-Bit or 128K x 16-Bit) CMOS Flash Memory
5.0 V-only Program and Erase

Valid Combinations	
Am29F200T/B-75	EC, FC, SC
Am29F200T/B-90	EC, EI, FC, FI, EE, EEB, FE, FEB, SC, SI, SE, SEB
Am29F200T/B-120	
Am29F200T/B-150	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 2. Am29F200 User Bus Operations ($\overline{BYTE}$ = V_{IH})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	DQ0–DQ15	$\overline{RESET}$
Auto-Select Manufacturer Code (1)	L	L	H	L	L	L	V_{ID}	Code	H
Auto-Select Device Code (1)	L	L	H	H	L	L	V_{ID}	Code	H
Read (3)	L	L	H	A0	A1	A6	A9	D_{OUT}	H
Standby	H	X	X	X	X	X	X	HIGH Z	H
Output Disable	L	H	H	X	X	X	X	HIGH Z	X
Write	L	H	L	A0	A1	A6	A9	D_{IN}	H
Enable Sector Protect	L	V_{ID}	L	X	X	X	V_{ID}	X	H
Verify Sector Protect (2)	L	L	H	L	H	L	V_{ID}	Code	H
Temporary Sector Unprotect	X	X	X	X	X	X	X	X	V_{ID}
Reset (Hardware)	X	X	X	X	X	X	X	HIGH Z	L

Table 3. Am29F200 User Bus Operations ($\overline{BYTE}$ = V_{IL})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	DQ0–DQ7	$\overline{RESET}$
Auto-Select Manufacturer Code (1)	L	L	H	L	L	L	V_{ID}	Code	H
Auto-Select Device Code (1)	L	L	H	H	L	L	V_{ID}	Code	H
Read (3)	L	L	H	A0	A1	A6	A9	D_{OUT}	H
Standby	H	X	X	X	X	X	X	HIGH Z	H
Output Disable	L	H	H	X	X	X	X	HIGH Z	X
Write	L	H	L	A0	A1	A6	A9	D_{IN}	H
Enable Sector Protect	L	V_{ID}	L	X	X	X	V_{ID}	X	H
Verify Sector Protect (2)	L	L	H	L	H	L	V_{ID}	Code	H
Temporary Sector Unprotect	X	X	X	X	X	X	X	X	V_{ID}
Reset (Hardware)	X	X	X	X	X	X	X	HIGH Z	L

Legend:

L = V_{IL}, H = V_{IH}, X = Don't Care. See DC Characteristics for voltage levels.

Notes:

1. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 7.*
2. *Refer to the section on Sector Protection.*
3. *$\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.*

Read Mode

The Am29F200 has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least t_{ACC}–t_{OE} time).

Standby Mode

The Am29F200 has two standby modes, a CMOS standby mode ($\overline{CE}$ input held at Vcc ± 0.5 V), when the current consumed is less than 100 µA; and a TTL standby mode ($\overline{CE}$ is held at V_{IH}) when the current required is reduced to approximately 1 mA. In the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All addresses are don't cares except A0, A1, and A6.

The manufacturer and device codes may also be read via the command register, for instances when the Am29F200 is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 7 (refer to Autoselect Command section).

Byte 0 (A0 = V_{IL}) represents the manufacturer's code (AMD=01H) and byte 1 (A0 = V_{IH}) the device identifier code (Am29F200T = 51H and Am29F200B = 52H for x8 mode; Am29F200T = 2251H and Am29F200B = 2252H for x16 mode). These two bytes/words are given in the table below. All identifiers for manufacturer and device will exhibit odd parity with the DQ7 defined as the parity bit. In order to read the proper device codes when executing the autoselect, A1 must be V_{IL} (see Tables 4.1 and 4.2).

Table 4.1 Am29F200 Sector Protection Verify Autoselect Codes

Type			A12–A16	A6	A1	A0	Code (HEX)
Manufacturer's Code			X	V_{IL}	V_{IL}	V_{IL}	01H
Am29F200 Device Code	Am29F200T	Byte	X	V_{IL}	V_{IL}	V_{IH}	51H
		Word					2251H
	Am29F200B	Byte	X	V_{IL}	V_{IL}	V_{IH}	52H
		Word					2252H
Sector Protection			Sector Addresses	V_{IL}	V_{IH}	V_{IL}	01H*

**Outputs 01H at protected sector addresses*

Table 4.2 Expanded Autoselect Code Table

Type		Code	DQ15	DQ14	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer's Code		01H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Am29F200 Device Code	Am29F200T(B)	51H	A–1	HI–Z	HI–Z	HI–Z	HI–Z	HI–Z	HI–Z	HI–Z	0	1	0	1	0	0	0	1
	(W)	2251H	0	0	1	0	0	0	1	0	0	1	0	1	0	0	0	1
	Am29F200B(B)	52H	A–1	HI–Z	HI–Z	HI–Z	HI–Z	HI–Z	HI–Z	HI–Z	0	1	0	1	0	0	1	0
	(W)	2252H	0	0	1	0	0	0	1	0	0	1	0	1	0	0	1	0
Sector Protection		01H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(B) – Byte mode

(W) – Word mode

Table 5. Sector Address Tables (Am29F200T)

	A16	A15	A14	A13	A12	Address Range
SA0	0	0	X	X	X	00000h–0FFFFh
SA1	0	1	X	X	X	10000h–1FFFFh
SA2	1	0	X	X	X	20000h–2FFFFh
SA3	1	1	0	X	X	30000h–37FFFh
SA4	1	1	1	0	0	38000h–39FFFh
SA5	1	1	1	0	1	3A000h–3BFFFh
SA6	1	1	1	1	X	3C000h–3FFFFh

Table 6. Sector Address Tables (Am29F200B)

	A16	A15	A14	A13	A12	Address Range
SA0	0	0	0	0	X	00000h–03FFFh
SA1	0	0	0	1	0	04000h–05FFFh
SA2	0	0	0	1	1	06000h–07FFFh
SA3	0	0	1	X	X	08000h–0FFFFh
SA4	0	1	X	X	X	10000h–1FFFFh
SA5	1	0	X	X	X	20000h–2FFFFh
SA6	1	1	X	X	X	30000h–3FFFFh

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written to by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Protection

The Am29F200 features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 6). The sector protect feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected. Alternatively, AMD may program and protect sectors in the factory prior to shipping the device (AMD's ExpressFlash™ Service).

To activate this mode, the programming equipment must force V_{ID} on address pin A9 and control pin $\overline{OE}$, (suggest V_{ID} = 11.5 V) and $\overline{CE}$ = V_{IL}. The sector addresses (A16, A15, A14, A13, and A12) should be set to the sector to be protected. Tables 5 and 6 define the sector address for each of the seven (7) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse. Refer to figures 17 and 18 for sector protect algorithm and waveforms.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector addresses (A16, A15, A14, A13, and A12) while (A6, A1, A0) = (0, 1, 0) will produce a logical "1" code at device output DQ0 for a protected sector. Otherwise the device will produce 00H for an unprotected sector. In this mode, the lower order addresses, except for A0, A1, and A6 are don't care. Address locations with A1 = V_{IL} are reserved for Autoselect manufacturer and device codes.

It is also possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order addresses (A16, A15, A14, A13, and A12) are the sector address will produce a logical "1" at DQ0 for a protected sector. See Tables 4.1 and 4.2 for Autoselect codes.

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors of the Am29F200 device in order to change data. The Sector Unprotect mode is activated by setting the $\overline{RESET}$ pin to high voltage (12V). During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once the 12V is taken away from the $\overline{RESET}$ pin, all the previously protected sectors will be protected again.

Sector Unprotect

The Am29F200 also features a sector unprotect mode, so that a protected sector may be unprotected to incorporate any changes in the code. All sectors should be protected prior to unprotecting any sector.

To activate this mode, the programming equipment must force V_{ID} on control pin $\overline{OE}$ and address pin A9. The $\overline{CE}$ and A0 pins must be set at V_{IL}. Pins A6 and A1 must be set to V_{IH}. Refer to Figure 19 for the sector unprotect algorithm. The unprotection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to determine if a sector is unprotected in the system by writing the autoselect command and A6 is set at V_{IL}. Performing a read operation at address location XXX2H, where the higher order addresses (A16, A15, A14, A13, and A12) define a particular sector address, will produce 00H at data outputs (DQ0–DQ7) for an unprotected sector.

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. **Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode**. Table 7 defines the valid register command sequences. Note that the Erase Suspend (B0) and Erase Resume (30) commands are valid only while the Sector Erase operation is in progress. Either of the two reset commands will reset the device (when applicable). Please note that commands are always written at DQ0–DQ7 and DQ8–DQ15 bits are ignored.

Table 7. Am29F200 Command Definitions

Command Sequence Read/Reset		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset		1	XXXH	F0H										
Read/Reset	Word	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
	Byte		AAAAH		5555H		AAAAH							
Autoselect	Word	4	5555H	AAH	2AAAH	55H	5555H	90H						
	Byte		AAAAH		5555H		AAAAH							
Program	Word	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	Data				
	Byte		AAAAH		5555H		AAAAH							
Chip Erase	Word	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
	Byte		AAAAH		5555H		AAAAH		AAAAH		5555H		AAAAH	
Sector Erase	Word	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
	Byte		AAAAH		5555H		AAAAH		AAAAH		5555H			
Sector Erase Suspend			Erase can be suspended during sector erase with Addr (don't care), Data (B0H)											
Sector Erase Resume			Erase can be resumed after suspend with Addr (don't care), Data (30H)											

Notes:

1. *Address bit A15 = X = Don't Care for all address commands except for Program Address (PA) and Sector Address (SA) Write Sequences may be initiated with A15 in either state.*
2. *Address bits A16 = X = Don't Care for all address commands except for Program Address (PA) and Sector Address (SA).*
3. *Bus operations are defined in Table 2.*
4. *RA = Address of the memory location to be read.*
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the sector to be erased. The combination of A16, A15, A14, A13, and A12 will uniquely select any sector.
5. *RD = Data read from location RA during read operation.*
   PD = Data to be programmed at location PA. Data is latched on the falling edge of $\overline{WE}$.
6. *The system should generate the following address patterns:*
   Word Mode: 5555H or 2AAAH to addresses A0 – A14
   Byte Mode: AAAAH or 5555H to addresses A-1 – A14.

Read/Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacture code of 01H. A read cycle from address XX01H returns the device code (Am29F200T = 51H and Am29F200B = 52H for x8 mode; Am29F200T = 2251H and Am29F200B = 2252H for x16 mode) (see Tables 4.1 and 4.2).

All manufacturer and device codes will exhibit odd parity with DQ7 defined as the parity bit.

Scanning the sector addresses (A16, A15, A14, A13, and A12) while (A6, A1, A0) = (0, 1, 0) will produce a logical "1" at device output DQ0 for a protected sector.

To terminate the operation, it is necessary to write the read/reset command sequence into the register.

Byte/Word Programming

The device is programmed on a byte-by-byte (or word-by-word) basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence the system is *not* required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to the read mode and addresses are no longer latched. Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time. Hence, $\overline{\text{Data}}$ Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from reset/read mode will show that the data is still "0". Only erase operations can convert "0"s to "1"s.

Figure 1 illustrates the Embedded Programming Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does *not* require the user to program the device prior to erase. Upon executing the Embedded Erase™ Algorithm command sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to read the mode.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (30H) is latched on the rising edge of $\overline{WE}$. A time-out of 80 µs from the rising edge of the last sector erase command will initiate the sector erase command(s).

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 80 µs, otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 80 µs from the rising edge of the last $\overline{WE}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{WE}$ occurs within the 80 µs time-out window the timer is reset. (Monitor DQ3 to determine if the sector erase timer window is still open, see section DQ3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this period will reset the device to the read mode, ignoring the previous command string. Resetting the device once execution has begun will corrupt the data in that sector. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to 6).

Sector erase does *not* require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is *not* required to provide any controls or timings during these operations.

The automatic sector erase begins after the 80 µs time out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to the read mode. $\overline{Data}$ Polling must be performed at an address within any of the sectors being erased.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Erase Suspend

Erase Suspend command allows the user to interrupt the chip and then perform data reads (not program) from a non-busy sector during a Sector Erase operation (which may take up to several seconds). This command is applicable ONLY during the Sector Erase operation and will be ignored if written during the Chip Erase or Programming operation. The Erase Suspend command (B0H) which is allowed only during the Sector Erase Operation includes the sector erase time-out period after the Sector Erase commands (30H). Writing this command during the time-out will result in immediate termination of the time-out period. Any subsequent writes of the Sector Erase command will be ignored as such, but instead will be taken as the Erase Resume command. Note that any other commands during the time out will reset the device to read mode. The addresses are don't-cares when writing the erase Suspend or Erase Resume commands.

When the Erase Suspend command is written during a Sector Erase operation, the chip will take between 0.1 µs to 15 µs to suspend the erase operation and go into erase suspended read mode (pseudo-read mode), during which the user can read from a sector that is NOT being erased. A read from a sector being erased may result in invalid data. The user must monitor the toggle bit (DQ6) to determine if the chip has entered the pseudo-read mode, at which time the toggle bit stops toggling. An address of a sector NOT being erased must be used to read the toggle bit, otherwise the user may encounter intermittent problems. Note that the user must keep track of what state the chip is in since there is no external indication of whether the chip is in pseudo-read mode or actual read mode. After the user writes the Erase Suspend command, the user must wait until the toggle bit stops toggling before data reads from the device can be performed. Any further writes of the Erase Suspend command at this time will be ignored.

Every time an Erase Suspend command followed by an Erase Resume command is written, the internal (pulse) counters are reset. These counters are used to count the number of high voltage pulses the memory cell requires to program or erase. If the count exceeds a certain limit, then the DQ5 bit will be set (Exceeded Time Limit flag). This resetting of the counters is necessary since the Erase Suspend command can potentially interrupt or disrupt the high voltage pulses.

To resume the operation of Sector Erase, the Resume command (30H) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Write Operation Status

Table 8. Hardware Sequence Flags

	Status	DQ7	DQ6	DQ5	DQ3	DQ2–DQ0
In Progress	Auto-Programming	$\overline{DQ7}$	Toggle	0	0	($\overline{D}$) (Note 1)
	Program/Erase in Auto Erase	0	Toggle	0	1	
Exceeded Time Limits	Auto-Programming	$\overline{DQ7}$	Toggle	1	1	($\overline{D}$) (Note 1)
	Program/Erase in Auto-Erase	0	Toggle	1	1	

Notes:

1. *DQ0, DQ1, and DQ2 are reserve pins for future use.*
2. *DQ8–DQ15 = Don't Care for x16 mode.*
3. *DQ4 for AMD internal use only.*

DQ7
$\overline{\text{Data}}$ Polling

The Am29F200 device features $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read the device will produce the complement of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7. During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a "1" at the DQ7 output. The flowchart for $\overline{\text{Data}}$ Polling (DQ7) is shown in Figure 3.

For chip erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For sector erase, the $\overline{\text{Data}}$ Polling is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. $\overline{\text{Data}}$ Polling must be performed at sector address within any of the sectors being erased and **not** a protected sector. Otherwise, the status may not be valid. Once the Embedded Algorithm operation is close to being completed, the Am29F200 data pins (DQ7) may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and DQ7 has a valid data, the data outputs on DQ0–DQ6 may be still invalid. The valid data on DQ0–DQ7 will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time-out (see Table 8).

See Figure 11 for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

DQ6
Toggle Bit

The Am29F200 also features the "Toggle Bit" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{OE}}$ toggling) data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on *the next* successive attempts. During programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{\text{WE}}$ pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. The Toggle Bit is active during the sector time out.

In programming, if the sector being written to is protected, the toggle bit will toggle for about 2 µs and then stop toggling without the data having changed. In erase, the device will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 100 µs and then drop back into read mode, having changed none of the data.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause the DQ6 to toggle. In addition, an Erase Suspend/Resume command will cause DQ6 to toggle.

See Figure 12 for the Toggle Bit timing specifications and diagrams.

DQ5
Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ5 will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the device under this condition. The $\overline{\text{CE}}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in Table 2.

If this failure condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this failure condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this failure condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The DQ5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ7 bit and DQ6 never stops toggling. Once the device has exceeded timing limits, the DQ5 bit will indicate a "1." Please note that this is not a device failure condition since the device was incorrectly used.

DQ3
Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ3 will remain low until the time-out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If Data Polling or the Toggle Bit indicates the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If DQ3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 were high on the second status check, the command may not have been accepted.

Refer to Table 8: Hardware Sequence Flags.

RY/BY
Ready/Busy

The Am29F200 provides a RY/BY output pin as a way to indicate to the host system that the Embedded Algorithms are either in progress or completed. If the output is low, the device is busy with either a program or erase operation. If the output is high, the device is ready to accept any read/write or erase operation. When the RY/BY pin is low, the device will not accept any additional program or erase commands. If the Am29F200 is placed in an Erase Suspend mode, the RY/BY output will be high. Also, since this is an open drain output, many RY/BY pins can be tied together in parallel with a pull up resistor to V_{CC}.

During programming, the RY/BY pin is driven low after the rising edge of the fourth WE pulse. During an erase operation, the RY/BY pin is driven low after the rising edge of the sixth WE pulse. The RY/BY pin should be ignored while RESET is at V_{IL}. Refer to Figure 13 for a detailed timing diagram.

RESET
Hardware Reset

The Am29F200 device may be reset by driving the RESET pin to V_{IL}. The RESET pin has a pulse requirement and has to be kept low (V_{IL}) for at least 500 ns in order to properly reset the internal state machine. Any operation in the process of being executed will be terminated and the internal state machine will be reset 20 µs after the RESET pin is driven low. Furthermore, once the RESET pin goes high, the device requires an additional 50 ns before it will allow read access. When the RESET pin is low, the device will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be corrupted. Please note that the RY/BY output signal should be ignored during the RESET pulse. Refer to Figure 14 for the timing diagram.

Byte/Word Configuration

The BYTE pin selects the byte (8-bit) mode or word (16 bit) mode for the Am29F200 device. When this pin is driven high, the device operates in the word (16 bit) mode. The data is read and programmed at DQ0–DQ15. When this pin is driven low, the device operates in byte (8 bit) mode. Under this mode, the DQ15/A-1 pin becomes the lowest address bit and DQ8–DQ14 bits are tristated. However, the command bus cycle is always an 8-bit operation and hence commands are written at DQ0–DQ7 and the DQ8–DQ15 bits are ignored. Refer to Figures 15 and 16 for the timing diagram.

Data Protection

The Am29F200 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting form V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on OE, CE or WE will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of OE = V_{IL}, CE = V_{IH} or WE = V_{IH}. To initiate a write cycle CE and WE must be a logical zero while OE is a logical one.

Power-Up Write Inhibit

Power-up of the device with WE = CE = V_{IL} and OE = V_{IH} will not accept commands on the rising edge of WE. The internal state machine is automatically reset to the read mode on power-up.

EMBEDDED ALGORITHMS

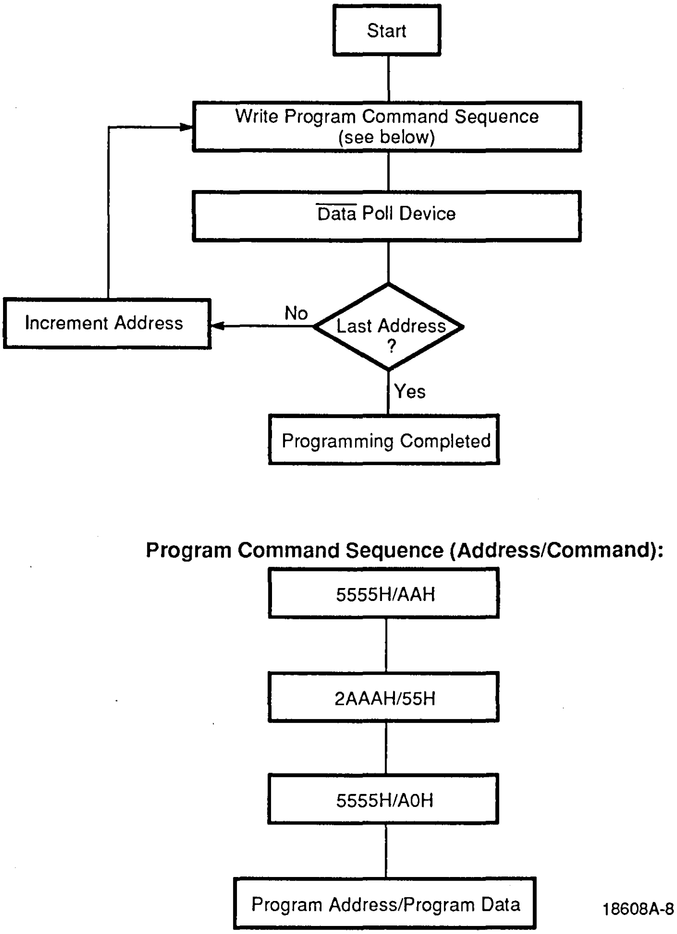


Figure 1. Embedded Programming Algorithm

Table 9. Embedded Programming Algorithm

Bus Operations	Command Sequence	Comments
Standby (Note 1)		
Write	Program	Valid Address/Data Sequence
Read		$\overline{\text{Data}}$ Polling to Verify Programming
Standby (Note 1)		Compare Data Output to Data Expected

Note:

1. Device is either powered-down, erase inhibit or program inhibit.

EMBEDDED ALGORITHMS

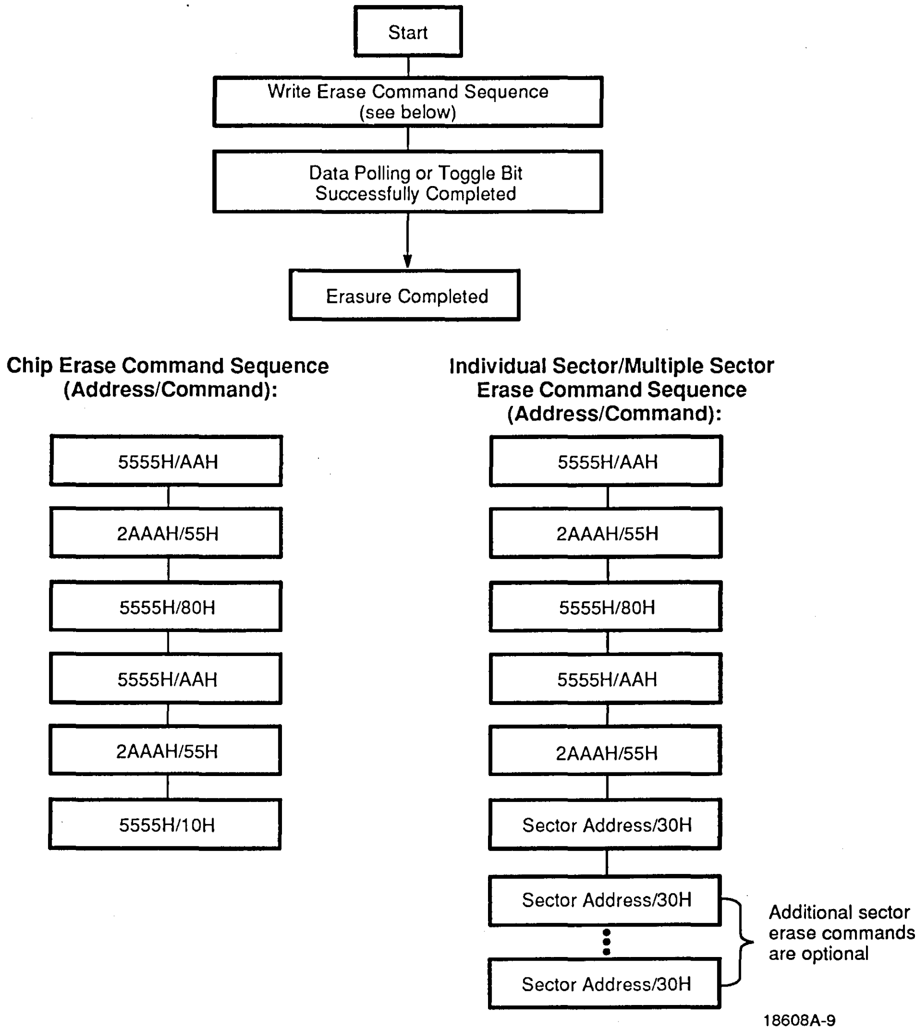


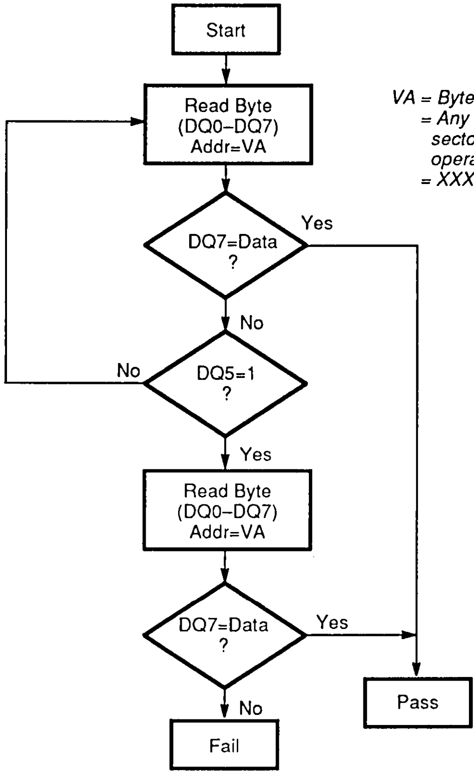
Figure 2. Embedded Erase Algorithm

Table 10. Embedded Erase Algorithm

Bus Operations	Command Sequence	Comments
Standby (Note 1)		
Write	Erase	
Read		$\overline{\text{Data}}$ Polling to Verify Erasure
Standby (Note 1)		Compare Output to FFH

Note:

1. Device is either powered-down, erase inhibit or program inhibit.



VA = Byte address for programming
= Any of the sector addresses within the sector being erased during sector erase operation
= XXXXH during chip erase

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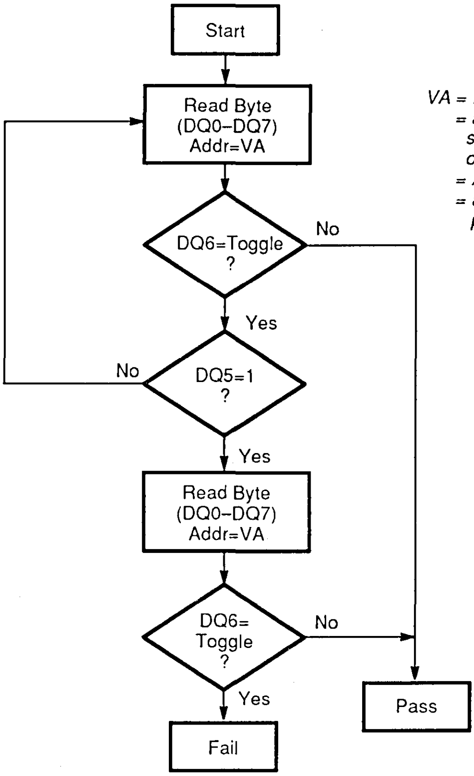
Note:

1. *DQ7 is rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 3. $\overline{\text{Data}}$ Polling Algorithm



VA = Byte address for programming
= any of the sector addresses within the sector being erased during sector erase operation
= XXXXH during chip erase
= any address not within the sector in the process of an Erase Suspend operation

18608A-11

Note:

1. *DQ6 is rechecked even if DQ5 = "1" because DQ6 may stop toggling at the same time as DQ5 changing to "1".*

Figure 4. Toggle Bit Algorithm

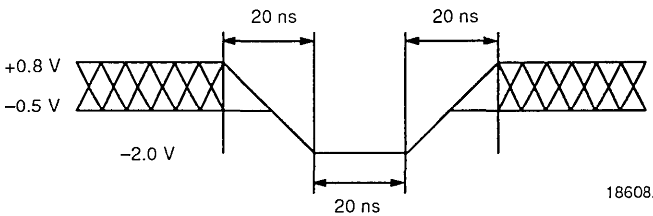


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Figure 5. Maximum Negative Overshoot Waveform

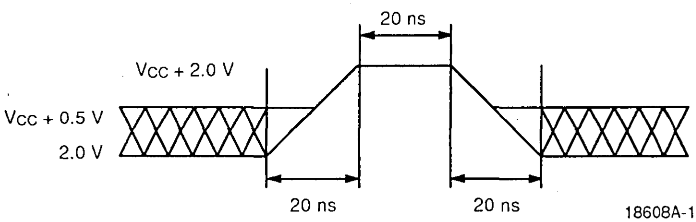

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Figure 6. Maximum Positive Overshoot Waveform

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages . . . . −65°C to +150°C
Plastic Packages . . . . −65°C to +125°C

Ambient Temperature
with Power Applied . . . . −55°C to +125°C

Voltage with Respect to Ground
All pins except A9 (Note 1) . . . . −2.0 V to +7.0 V

V_{CC} (Note 1) . . . . −2.0 V to +7.0 V

A9 (Note 2) . . . . −2.0 V to +14.0 V

Output Short Circuit Current (Note 3) . . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A9 pin is –0.5 V. During voltage transitions, A9 may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) . . . . 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) . . . . −40°C to +85°C

Extended (E) Devices
Case Temperature (T_C) . . . . −55°C to +125°C

Military (M) Devices
Case Temperature (T_C) . . . . −55°C to +125°C

V_{CC} Supply Voltages
V_{CC} for Am29F200T/B-75 . . . . +4.75 V to +5.25 V

V_{CC} for Am29F200T/B-90, 120 . . . +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS
TTL/NMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.5 V			50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	Byte		40	mA
			Word		50	
I_{CC2}	V_{CC} Active Current (Notes 2, 3)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$			60	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$			1.0	mA
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 0.5	V
V_{ID}	Voltage for Autoselect and Sector Protect	V_{CC} = 5.0 V		11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA, $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH}	Output High Level	I_{OH} = −2.5 mA $V_{CC} = V_{CC}$ Min		2.4		V
V_{LKO}	Low V_{CC} Lock-Out Voltage			3.2	4.2	V

Notes:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *I_{CC} active while Embedded Algorithm (program or erase) is in progress.*
3. *Not 100% tested.*

DC CHARACTERISTICS (continued)
CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
I_{LI}	Input Load Current	V_{IN} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max			±1.0	µA
I_{LIT}	A9 Input Load Current	V_{CC} = V_{CC} Max, A9 = 12.5 V			50	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = V_{CC} Max			±1.0	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}	Byte		40	mA
			Word		50	
I_{CC2}	V_{CC} Active Current (Notes 2, 3)	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}			60	mA
I_{CC3}	V_{CC} Standby Current	V_{CC} = V_{CC} Max, $\overline{CE}$ = V_{CC} ± 0.5 V, $\overline{OE}$ = V_{IH}			100	µA
V_{IL}	Input Low Level			–0.5	0.8	V
V_{IH}	Input High Level			0.7x V_{CC}	V_{CC} +0.3	V
V_{ID}	Voltage for Autoselect and Sector Protect	V_{CC} = 5.0 V		11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA, V_{CC} = V_{CC} Min			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min		0.85 V_{CC}		V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min		V_{CC} –0.4		V
V_{LKO}	Low V_{CC} Lock-out Voltage			3.2	4.2	V

Notes:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *I_{CC} active while Embedded Algorithm (program or erase) is in progress.*
3. *Not 100% tested.*

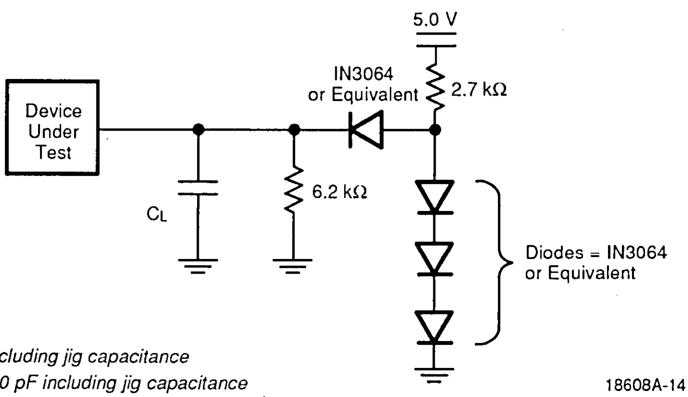
AC CHARACTERISTICS

Read Only Operations Characteristics

Parameter Symbols									
JEDEC	Standard	Description	Test Setup		-75 (Note 1)	-90 (Note 2)	-120 (Note 2)	-150 (Note 2)	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)		Min	70	90	120	150	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE}$ = V_{IL} $\overline{OE}$ = V_{IL}	Max	70	90	120	150	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE}$ = V_{IL}	Max	70	90	120	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max	30	35	50	55	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 3, 4)		Max	20	20	30	35	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 3, 4)		Max	20	20	30	35	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		Min	0	0	0	0	ns
	t_{Ready}	$\overline{RESET}$ pin low to read mode		Max	20	20	20	20	µs
	t_{ELFL} t_{ELFH}	$\overline{CE}$ to $\overline{BYTE}$ switching low or high		Max	5	5	5	5	ns

Notes:

1. *Test Conditions:*
   Output Load: 1 TTL gate and 30 pF
   Input rise and fall times: 5 ns
   Input pulse levels: 0.0 V to 3.0 V
   Timing measurement reference level
   Input: 1.5 V
   Output: 1.5 V
2. *Test Conditions:*
   Output Load: 1 TTL gate and 100 pF
   Input rise and fall times: 20 ns
   Input pulse levels: 0.45 V to 2.4 V
   Timing measurement reference level
   Input: 0.8 and 2.0 V
   Output: 0.8 and 2.0 V
3. *Output driver disable time.*
4. *Not 100% tested.*



Notes:

For -70: C_L = 30 pF including jig capacitance
For all others: C_L = 100 pF including jig capacitance

Figure 7. Test Conditions

AC CHARACTERISTICS

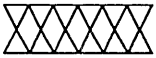
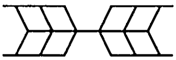
Write/Erase/Program Operations

Parameter Symbols JEDEC	Parameter Symbols Standard	Description			-70	-90	-120	-150	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (3)		Min	70	90	120	150	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	45	50	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	30	45	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time (3)		Min	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read (3)	Min	0	0	0	0	ns
			Toggle and $\overline{\text{Data}}$ Polling (3)	Min	10	10	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write		Min	0	0	0	0	ns
t_{ELWL}	t_{CS}	$\overline{\text{CE}}$ Setup Time		Min	0	0	0	0	ns
t_{WHEH}	t_{CH}	$\overline{\text{CE}}$ Hold Time		Min	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35	45	50	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ	16	16	16	16	µs
t_{WHWH2}	t_{WHWH2}	Erase Operation (1)		Typ	1.5	1.5	1.5	1.5	sec
				Max	30	30	30	30	sec
	t_{VCS}	V_{CC} Set Up Time (3)		Min	50	50	50	50	µs
	t_{VLHT}	Voltage Transition Time (2, 3, 5)		Min	4	4	4	4	µs
	t_{WPP}	Write Pulse Width (2)		Min	100	100	100	100	µs
	t_{WPP2}	Write Pulse Width (5)		Min	10	10	10	10	ms
	t_{OESP}	$\overline{\text{OE}}$ Setup Time to $\overline{\text{WE}}$ Active (2, 3, 5)		Min	4	4	4	4	µs
	t_{CSP}	$\overline{\text{CE}}$ Setup Time to $\overline{\text{WE}}$ Active (3)		Min	4	4	4	4	µs
	t_{RP}	$\overline{\text{RESET}}$ Pulse Width		Min	500	500	500	500	ns
	t_{FLQZ}	$\overline{\text{BYTE}}$ Switching Low to Output High Z (3, 4)		Max	20	30	30	30	ns
	t_{BUSY}	Program/Erase Valid to RD/$\overline{\text{BY}}$ delay (3)		Min	30	35	50	55	ns

Notes:

1. *This does not include the preprogramming time.*
2. *These timings are for Sector Protect operation.*
3. *Not 100% tested.*
4. *Output Driver Disable Time*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS

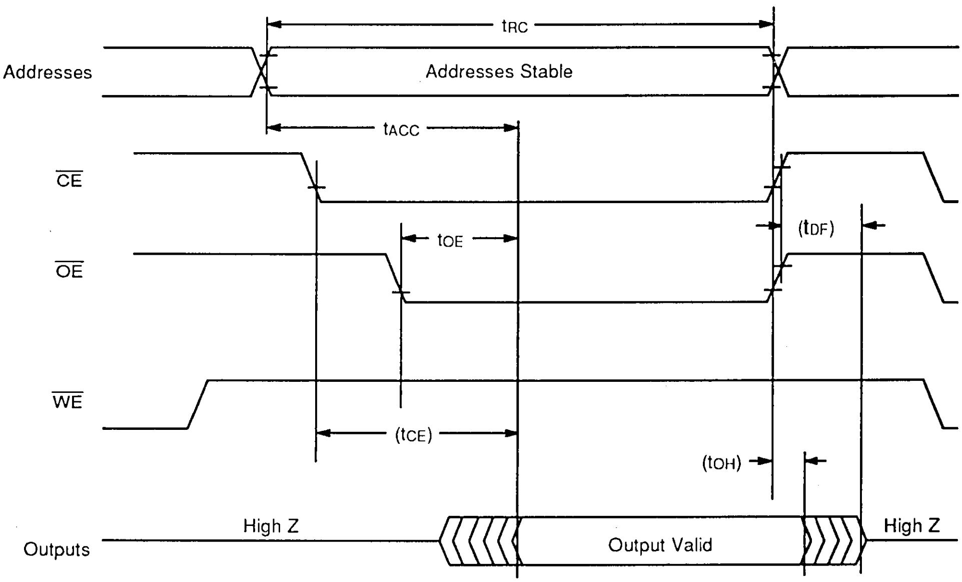


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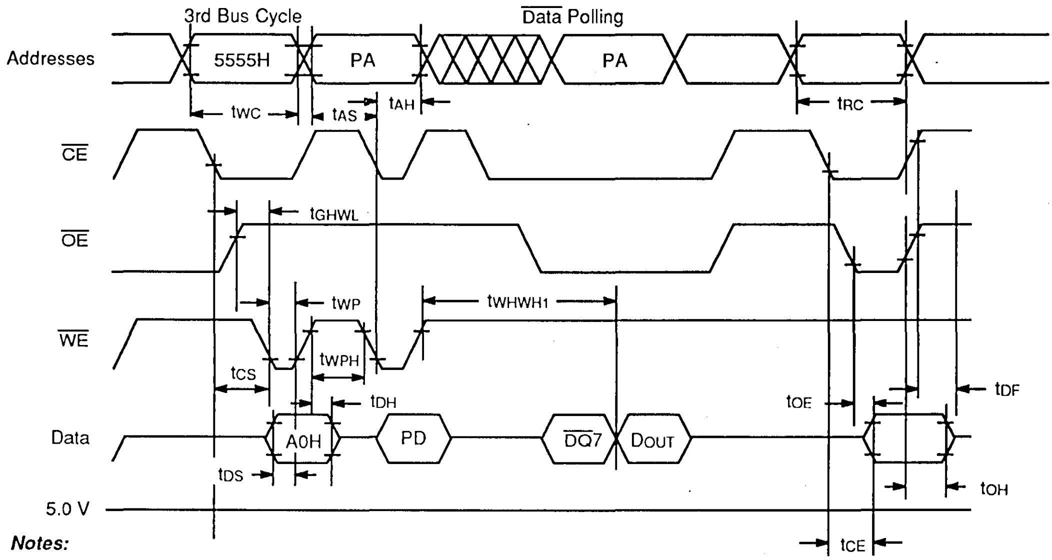
Figure 8. AC Waveforms for Read Operations

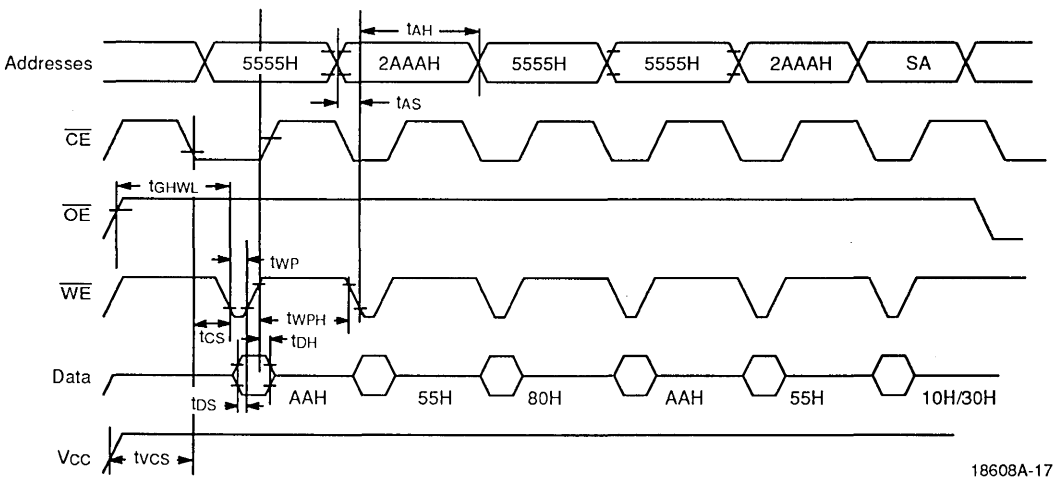
SWITCHING WAVEFORMS



Notes:

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
4. *DOUT is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*
6. *These waveforms are for the x16 mode.*

Figure 9. Program Operation Timings

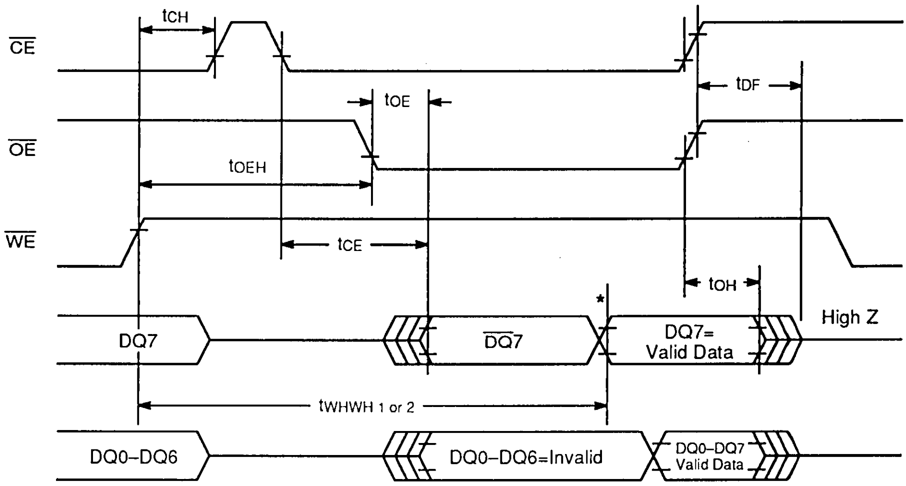


Notes:

1. *SA is the sector address for Sector Erase. Addresses = don't care for Chip Erase.*
2. *These waveforms are for the x16 mode.*

Figure 10. AC Waveforms Chip/Sector Erase Operations

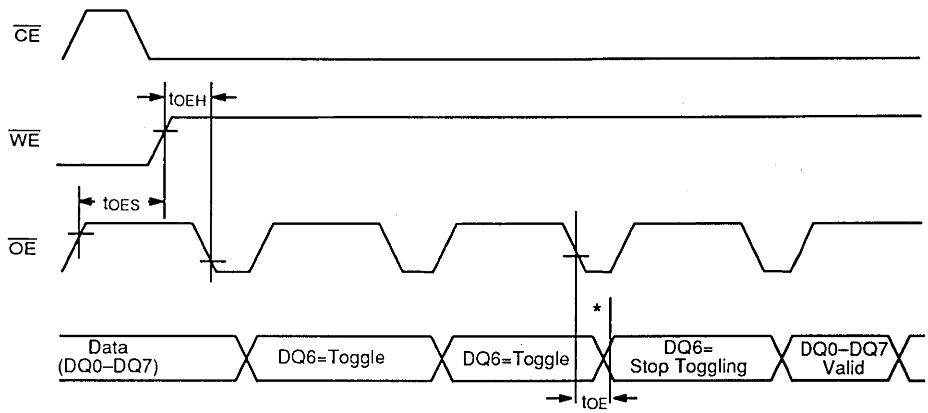
SWITCHING WAVEFORMS



*DQ7=Valid Data (The device has completed the Embedded operation).

18608A-18

Figure 11. AC Waveforms for Data Polling During Embedded Algorithm Operations



18608A-19

Note:

**DQ6 stops toggling (The device has completed the Embedded operation).*

Figure 12. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

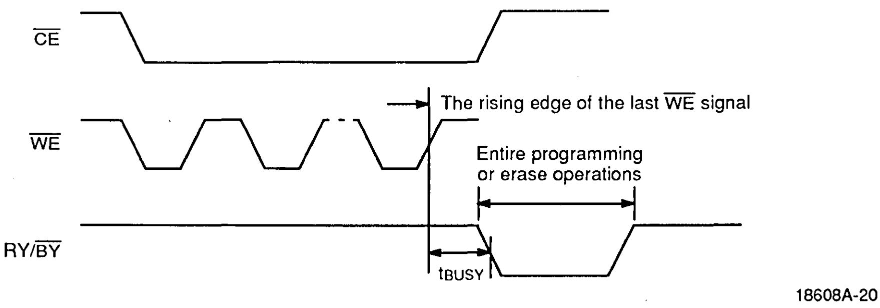


Figure 13. RY/$\overline{\text{BY}}$ Timing Diagram During Program/Erase Operations

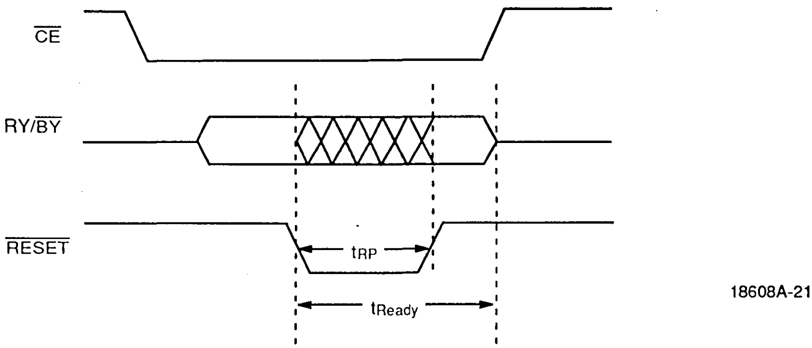


Figure 14. $\overline{\text{RESET}}$/RY/$\overline{\text{BY}}$ Timing Diagram

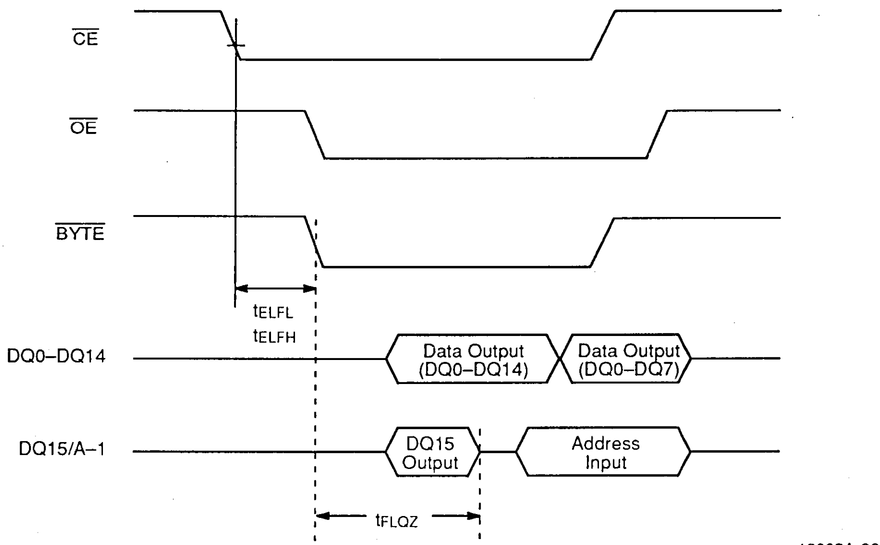


Figure 15. $\overline{\text{BYTE}}$ Timing Diagram for Read Operation

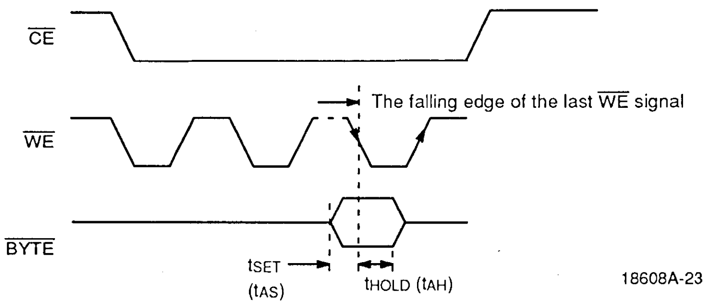


Figure 16. $\overline{\text{BYTE}}$ Timing Diagram for Write Operations

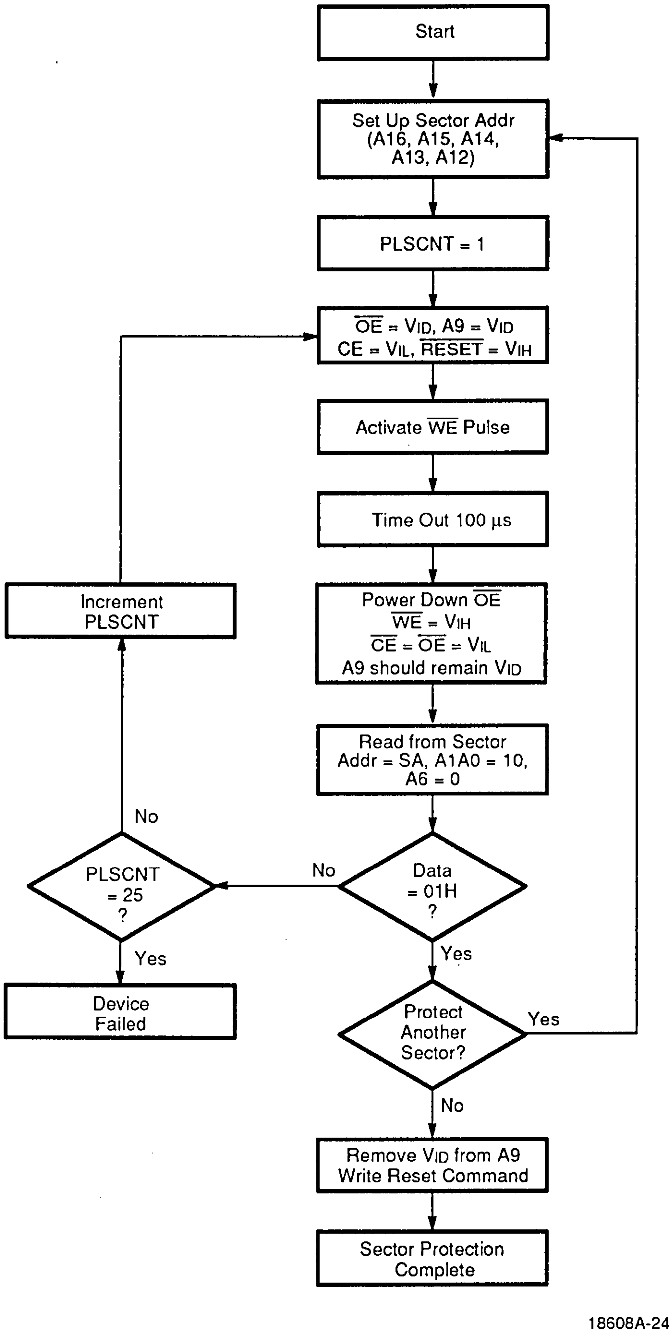
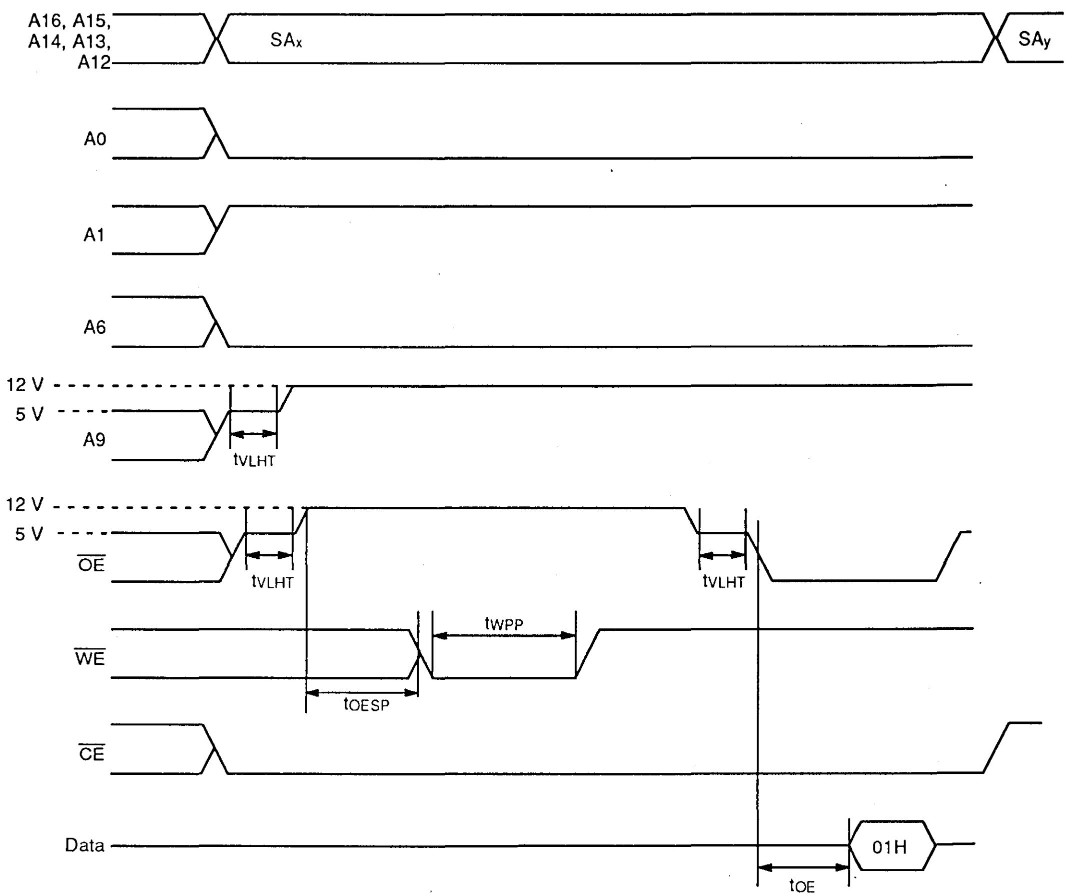


Figure 17. Sector Protection Algorithm

SWITCHING WAVEFORMS



SA_x = Sector Address for initial sector

SA_y = Sector Address for next sector

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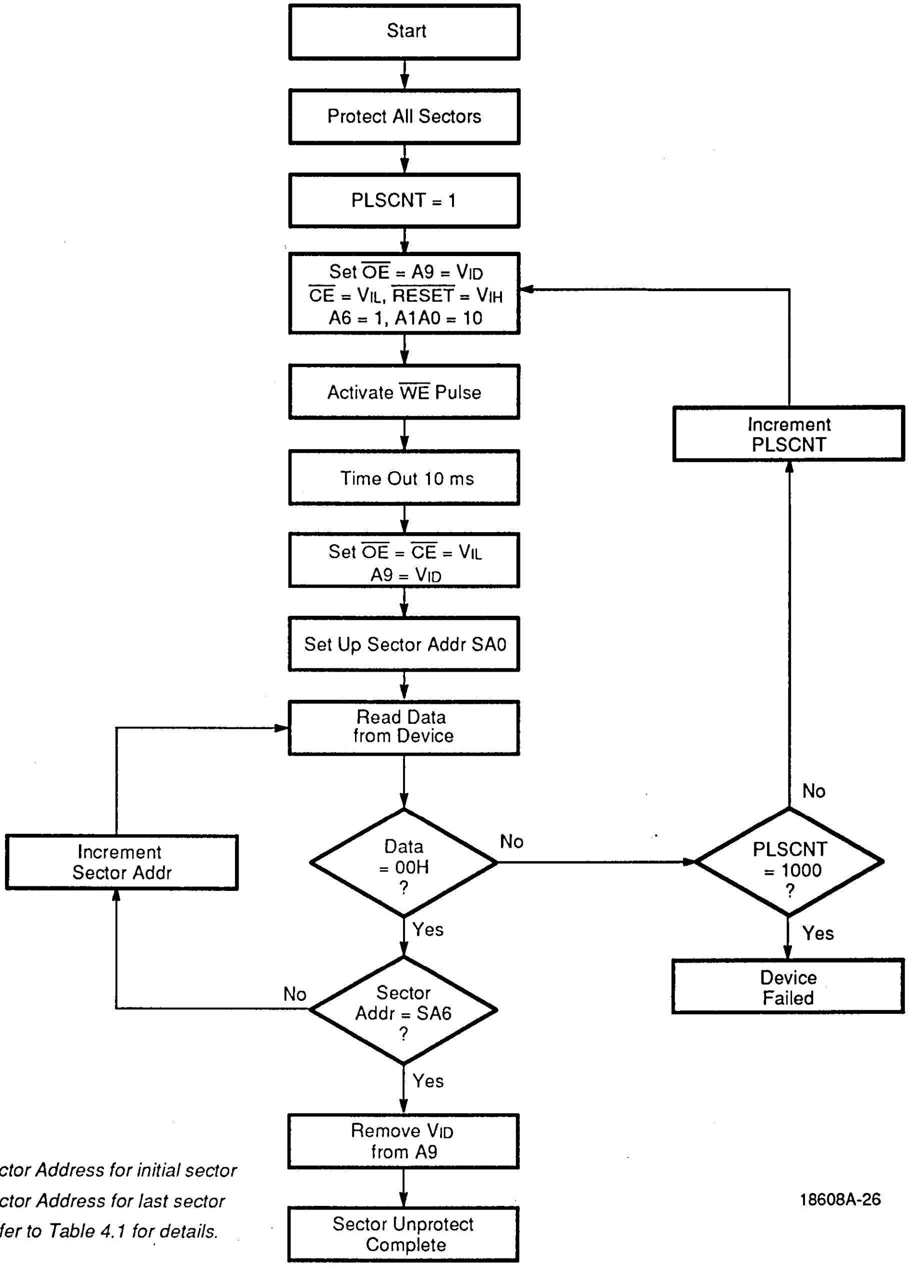
Figure 18. AC Waveforms for Sector Protection



Notes:

SA0 = Sector Address for initial sector

SA6 = Sector Address for last sector

Please refer to Table 4.1 for details.

Figure 19. Sector Unprotect Algorithm

SWITCHING WAVEFORMS

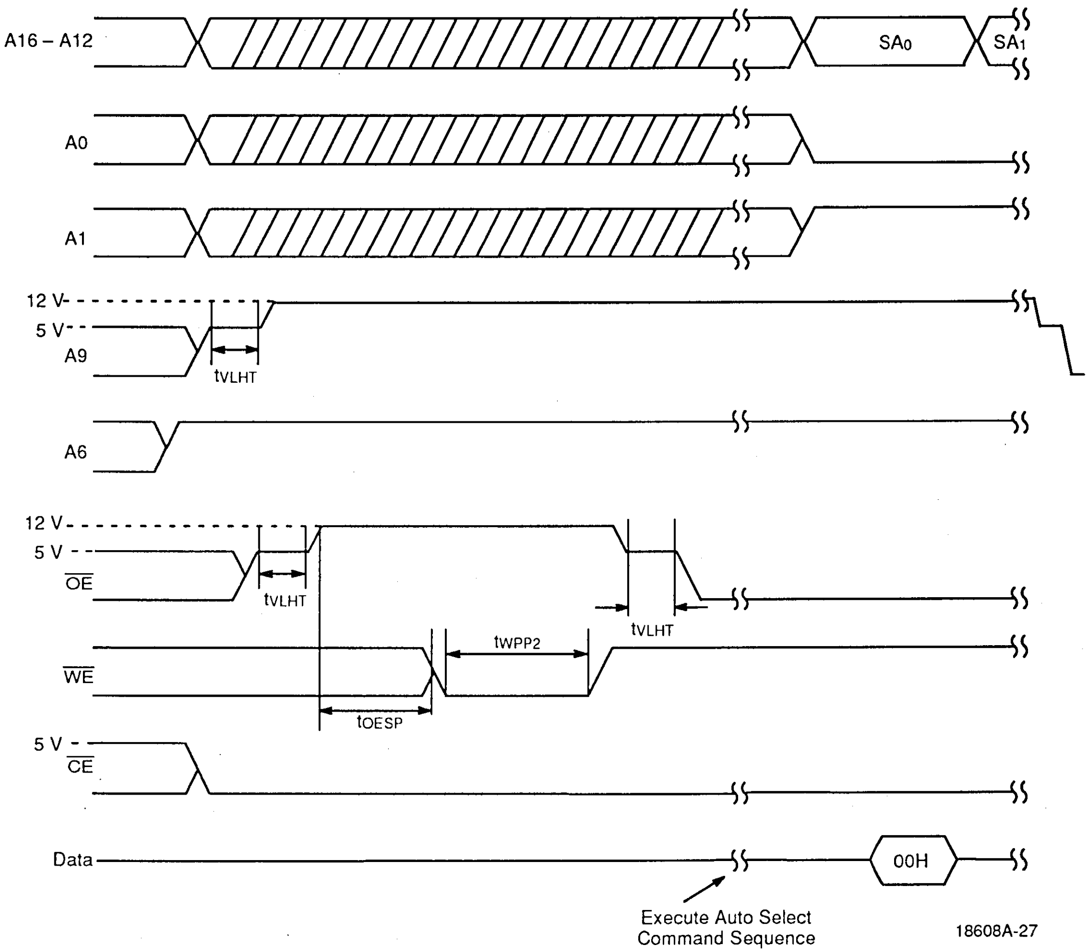


Figure 20. AC Waveforms for Sector Unprotect

AC CHARACTERISTICS

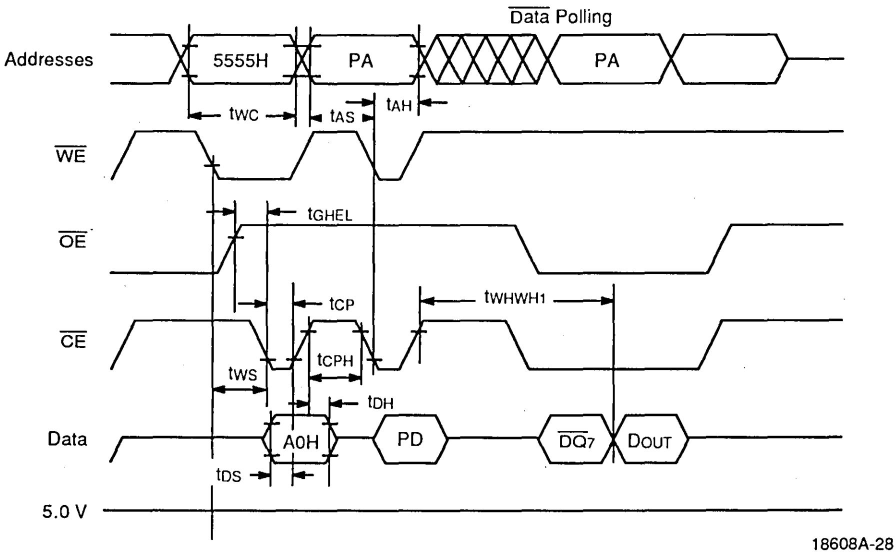
Write/Erase/Program Operations

Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols JEDEC	Standard	Description			-70	-90	-120	-150	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (4)		Min	70	90	120	150	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	45	50	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	30	45	50	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time		Min	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time (4)	Read (4)	Min	0	0	0	0	ns
			Toggle and $\overline{Data}$ Polling	Min	10	10	10	10	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write		Min	0	0	0	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time		Min	0	0	0	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		Min	0	0	0	0	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width		Min	35	45	50	50	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High		Min	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ	16	16	16	16	µs
t_{WHWH2}	t_{WHWH2}	Erase Operation (1)		Typ	1.5	1.5	1.5	1.5	sec
				Max	30	30	30	30	sec
	t_{VCS}	V_{CC} Set Up Time (4)		Typ	50	50	50	50	µs
	t_{RP}	$\overline{RESET}$ Pulse Width		Min	500	500	500	500	ns
	t_{FLQZ}	$\overline{BYTE}$ Switching Low to Output High Z (3, 4)		Max	20	30	30	30	ns
	t_{BUSY}	Program/Erase Valid to RD/$\overline{BY}$ Delay (4)		Min	30	35	50	55	ns

Notes:

1. *This does not include the preprogramming time.*
2. *These timings are for Sector Protect/Unprotect operations.*
3. *This timing is only for Sector Unprotect.*
4. *Not 100% tested.*



Notes:

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
4. *DOUT is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*
6. *These waveforms are for the x16 mode.*

Figure 21. Alternate $\overline{CE}$ Controlled Program Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max		
Chip and Sector Erase Time		1.5 (Note 1)	30	sec	Excludes 00H programming prior to erasure
Byte Programming Time		16	1000 (Note 2)	µs	Excludes system-level overhead
Chip Programming Time		8.5 (Note 1)	50	sec	Excludes system-level overhead
Erase/Program Cycles	100,000	1,000,000		Cycles	

Notes:

1. *25°C, 5 V V_{CC}, 100,000 cycles*
2. *The Embedded Algorithms allow for 48 ms byte program time.*

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	6	7.5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8.5	12	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	8	10	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz*

SO PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	6	7.5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8.5	12	pF
C_{IN2}	Control Pin Capacitance	$V_{PP} = 0$	8	10	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz*

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

PRELIMINARY

Am29F040

Advanced Micro Devices

4 Megabit (524,288 x 8-Bit) CMOS 5.0 Volt-only, Sector Erase Flash Memory

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% read, write, and erase**
  - Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  - Uses same software commands as E^2PROMs
- **Compatible with JEDEC-standard byte-wide pinouts**
  - 32-pin PLCC/LCC
  - 32-pin TSOP
  - 32-pin DIP
- **Minimum 100,000 write/erase cycles**
- **High performance**
  - 70 ns maximum access time
- **Sector erase architecture**
  - 8 equal size sectors of 64K bytes each
  - Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Embedded Erase Algorithms**
  - Automatically pre-programs and erases the chip or any sector
- **Embedded Program Algorithms**
  - Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Low power consumption**
  - 20 mA typical active read current
  - 30 mA typical write/erase current
  - 25 µA typical standby current
- **Low V_{CC} write inhibit ≤ 3.2 V**
- **Sector protection**
  - Hardware method disables any combination of sectors from write or erase operations
- **Suspend Erase/Resume**
  - Suspend the erase operation to allow a read data in another sector within the same device

GENERAL DESCRIPTION

The Am29F040 is a 4 Mbit, 5.0 V-only Flash memory organized as 512K bytes of 8 bits each. The Am29F040 is offered in a 32-pin package. This device is designed to be programmed in-system with the standard system 5.0 V V_{CC} supply. A 12.0 V V_{PP} is not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The standard Am29F040 offers access times between 70 ns and 150 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$) and output enable ($\overline{OE}$) controls.

The Am29F040 is entirely pin and command set compatible with JEDEC standard 4 Mbit E^2PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

The Am29F040 is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than one

PRODUCT SELECTOR GUIDE

Family Part No:	Am29F040			
Ordering Part No: V_{CC} = 5.0 V ± 5%	-75			
V_{CC} = 5.0 V ± 10%		-90	-120	-150
Max Access Time (ns)	70	90	120	150
$\overline{CE}$ ($\overline{E}$) Access (ns)	70	90	120	150
$\overline{OE}$ ($\overline{G}$) Access (ns)	30	35	50	55

Publication# 17113 Rev. C Amendment/0
Issue Date: March 1994

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

second. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The entire chip or any individual sector is typically erased and verified in 1.5 seconds (if already completely preprogrammed).

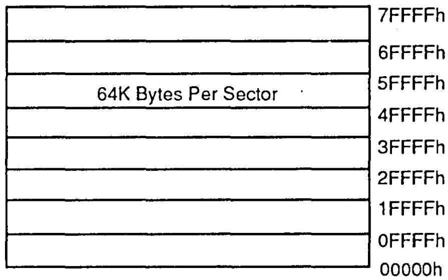
This device also features a sector erase architecture. The sector mode allows for 64K byte blocks of memory to be erased and reprogrammed without affecting other blocks. The Am29F040 is erased when shipped from the factory.

The device features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ7 or by the Toggle Bit feature on DQ6. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

AMD's Flash technology combines years of EPROM and E^2PROM experience to produce the highest levels of quality, reliability and cost effectiveness. The Am29F040 memory electrically erases the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

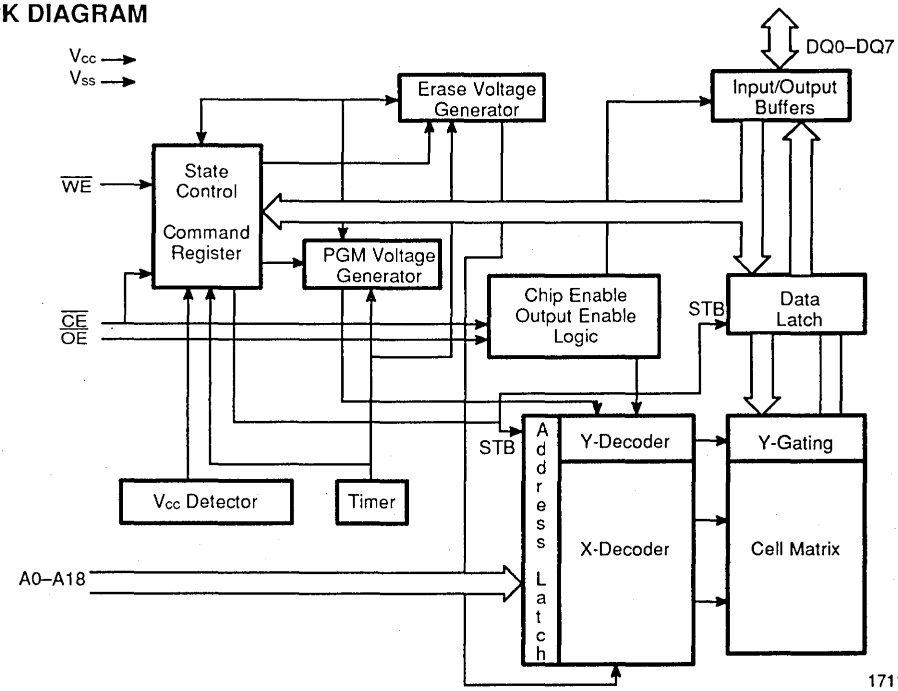
Flexible Sector-Erase Architecture

- 64K Bytes per sector
- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user definable



17113C-1

BLOCK DIAGRAM



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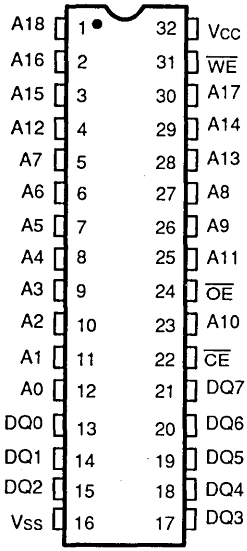
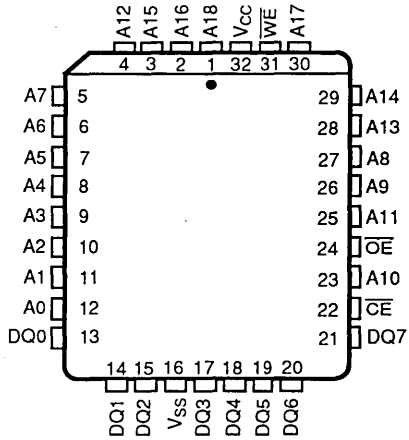
CONNECTION DIAGRAMS

CERDIP/PDIP



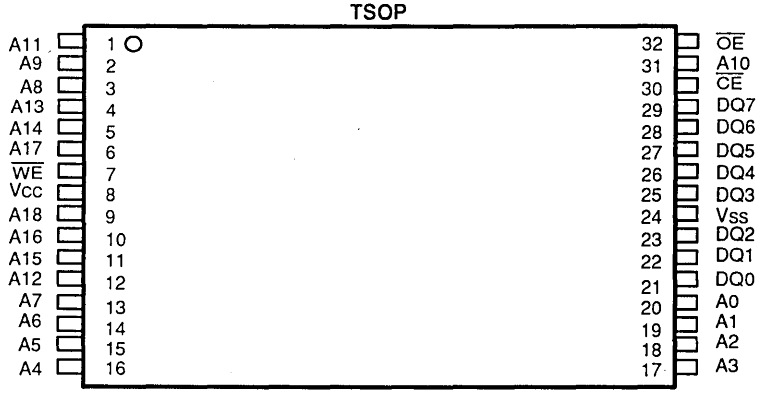
17113C-3

PLCC/LCC

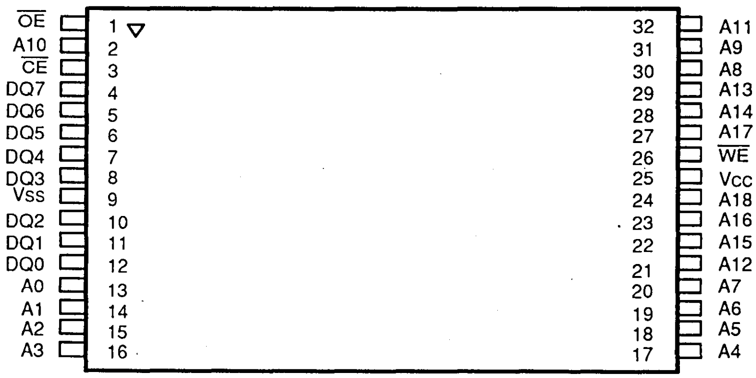


17113C-4

TSOP



29F040 Standard Pinout 17113C-5



29F040 Reverse Pinout 17113C-6

LOGIC SYMBOL

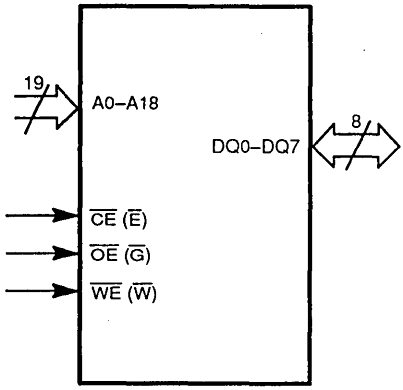


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Table 1. Am29F040 Pin Configuration

Pin	Function
A0–A18	Address Inputs
DQ0–DQ7	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
Vss	Device Ground
Vcc	Device Power Supply (5.0 V ± 10% or ± 5%)

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

AM29F040 -75 J C B

OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-In

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended (–55°C to +125°C)

PACKAGE TYPE
P = 32-Pin Plastic DIP (PD 032)
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)
E = 32-Pin Thin Small Outline Package (TSOP) Standard Pinout (TS 032)
F = 32-Pin Thin Small Outline Package (TSOP) Reverse Pinout (TSR 032)

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am29F040
4 Megabit (512K x 8-Bit) CMOS Flash Memory
5.0 V Program and Erase
64K Byte Sectors

Valid Combinations	
AM29F040-75	JC, EC, FC
AM29F040-90 AM29F040-120 AM29F040-150	DE, DEB, LE, LEB, PC, PI, JC, JI, PCB, PIB, JCB, JIB, PE, PEB, JE, JEB, EC, EI, FC, FI, EE, EEB, FE, FEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

AM29F040 -90 /B X , A

LEAD FINISH
A = Hot Solder Dip

PACKAGE TYPE
X = 32-Pin Ceramic DIP (CD 032)
U = 32-Pin Rectangular Ceramic Leadless Chip Carrier (CLR 032)

DEVICE CLASS
/B = Class B

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am29F040
4 Megabit (512K x 8-Bit) CMOS Flash Memory
5.0 V Program and Erase
64K Byte Sectors

Valid Combinations	
AM29F040-90	/BXA, /BUA
AM29F040-120	
AM29F040-150	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Table 2. Am29F040 User Bus Operations

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	I/O
Auto-Select Manufacturer Code (1)	L	L	H	L	L	L	V_{ID}	Code
Auto-Select Device Code (1)	L	L	H	H	L	L	V_{ID}	Code
Read (4)	L	L	H	A0	A1	A6	A9	D_{OUT}
Standby	H	X	X	X	X	X	X	HIGH Z
Output Disable	L	H	H	X	X	X	X	HIGH Z
Write	L	H	L	A0	A1	A6	A9	D_{IN} (2)
Enable Sector Protect	L	V_{ID}	L	X	X	X	V_{ID}	X
Verify Sector Protect (3)	L	L	H	L	H	L	V_{ID}	Code

Legend:
L = V_{IL}, H = V_{IH}, X = Don't Care. See DC Characteristics for voltage levels.

Notes:
1. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Tables 3 and 4.*
2. *Refer to Table 4 for valid D_{IN} during a write operation.*
3. *Refer to the section on Sector Protection*
4. *$\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.*

Read Mode

The Am29F040 has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least t_{ACC}–t_{OE} time).

Standby Mode

The Am29F040 has two standby modes, a CMOS standby mode ($\overline{CE}$ input held at Vcc ± 0.5 V), when the current consumed is less than 100 µA; and a TTL standby mode ($\overline{CE}$ is held at V_{IH}) when the current required is reduced to approximately 1 mA. In the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All addresses are don't cares except A0, A1, and A6.

The manufacturer and device codes may also be read via the command register, for instances when the AM29F040 is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 5 (refer to Autoselect Command section).

Byte 0 (A0 = V_{IL}) represents the manufacture's code (AMD=01H) and byte 1 (A0 = V_{IH}) the device identifier code (Am29F040=A4H). These two bytes are given in the table below. All identifiers for manufactures and device will exhibit odd parity with the MSB (DQ7) defined as the parity bit. In order to read the proper device codes when executing the autoselect, A1 must be V_{IL} (see Table 3).

Table 3. Am29F040 Sector Protection Verify Autoselect Codes

Type	A18	A17	A16	A6	A1	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacture Code	X	X	X	V_{IL}	V_{IL}	V_{IL}	01H	0	0	0	0	0	0	0	1
Am29F040 Device Code	X	X	X	V_{IL}	V_{IL}	V_{IH}	A4H	1	0	1	0	0	1	0	0
Sector Protection	Sector Addresses			V_{IL}	V_{IH}	V_{IL}	01H*	0	0	0	0	0	0	0	1

**Outputs 01H at protected sector addresses*

Table 4. Sector Address Tables

	A18	A17	A16	Address Range
SA0	0	0	0	00000h–0FFFFh
SA1	0	0	1	10000h–1FFFFh
SA2	0	1	0	20000h–2FFFFh
SA3	0	1	1	30000h–3FFFFh
SA4	1	0	0	40000h–4FFFFh
SA5	1	0	1	50000h–5FFFFh
SA6	1	1	0	60000h–6FFFFh
SA7	1	1	1	70000h–7FFFFh

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Protection

The Am29F040 features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 8). The sector protect feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected. Alternatively, AMD may program and protect sectors in the factory prior to shipping the device (AMD's ExpressFlash™ Service).

To activate this mode, the programming equipment must force V_{ID} on address pin A9 and control pin $\overline{OE}$, (suggest V_{ID} = 11 V) and $\overline{CE} = V_{IH}$. The sector addresses (A18, A17, and A16) should be set to the sector to be protected. Table 4 defines the sector address for each of the eight (8) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector addresses (A16, A17, and A18) while (A6, A1, A0) = (0, 1, 0) will produce a logical "1" code at device output DQ0 for a protected sector. Otherwise the device will read 00H for unprotected sector. In this mode, the lower order addresses, except for A0, A1, and A6 are don't care. Address locations with A1 = V_{IL} are reserved for Autoselect manufacturer and device codes.

It is also possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order addresses (A16, A17, and A18) are the sector address will produce a logical "1" at DQ0 for a protected sector. See Table 3 for Autoselect codes.

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. Writing incorrect address and data values or writing them in the improper sequence will reset the device to read mode. Table 5 defines the valid register command sequences. Note that the Erase Suspend (B0) and Erase Resume (30) commands are valid only while the Sector Erase operation is in progress. Either of the two reset commands will reset the device (when applicable).

Table 5. Am29F040 Command Definitions

Command Sequence Read/Reset	Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	XXXH	F0H										
Read/Reset	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
Autoselect	4	5555H	AAH	2AAAH	55H	5555H	90H						
Byte Program	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	Data				
Chip Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
Sector Erase Suspend		Erase can be suspended during sector erase with Addr (don't care), Data (B0H)											
Sector Erase Resume		Erase can be resumed after suspend with Addr (don't care), Data (30H)											

Notes:

1. *Address bits A15, A16, A17, and A18 = X = Don't Care. Write Sequences may be initiated with A15 in either state.*
2. *Address bits A15, A16, A17, and A18 = X = Don't Care for all address commands except for Program Address (PA) and Sector Address (SA).*
3. *Bus operations are defined in Table 2.*
4. *RA = Address of the memory location to be read.*
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the sector to be erased. The combination of A18, A17, A16 will uniquely select any sector.
5. *RD = Data read from location RA during read operation.*
   PD = Data to be programmed at location PA. Data is latched on the falling edge of $\overline{WE}$.

Read/Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains a command autoselect operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacture code of 01H. A read cycle from address XX01H returns the device code A4H (see Table 3). All manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit.

Scanning the sector addresses (A16, A17, A18) while (A6, A1, A0) = (0, 1, 0) will produce a logical "1" at device output DQ0 for a protected sector.

To terminate the operation, it is necessary to write the read/reset command sequence into the register.

Byte Programming

The device is programmed on a byte-by-byte basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence the system is *not* required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to the read mode and addresses are no longer latched. Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time. Hence, $\overline{\text{Data}}$ Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so will probably hang up the device (exceed timing limits), or perhaps result in an apparent success according to the data polling algorithm but a read from reset/read mode will show that the data is still "0". Only erase operations can convert "0"s to "1"s.

Figure 1 illustrates the Embedded Programming Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does *not* require the user to program the device prior to erase. Upon executing the Embedded Erase™ Algorithm command sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to read the mode.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (data) is latched on the rising edge of $\overline{WE}$. A time-out of 80 µs from the rising edge of the last sector erase command will initiate the sector erase command(s). ***Please note:*** *Do not attempt to write an invalid command sequence during the sector erase operation. Otherwise, it will terminate the sector erase operation and the device will reset back into the read mode.*

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 80 µs, otherwise that command will not be accepted. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 80 µs from the rising edge of the last $\overline{WE}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{WE}$ occurs within the 80 µs time-out window the timer is reset. (Monitor DQ3 to determine if the sector erase window is still open, see section DQ3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this period and afterwards will reset the device to read mode, ignoring the previous command string. Resetting the device after it has begun execution will result in the data of the operated sectors being undefined (messed up). In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (1 to 8).

Sector erase does *not* require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is *not* required to provide any controls or timings during these operations.

The automatic sector erase begins after the 100 µs time out from the rising edge of the $\overline{WE}$ pulse for the last sector erase command pulse and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to read mode. *During the execution of the Sector Erase command, only the Erase Suspend and Erase Resume commands are allowed. All other commands will reset the device to read mode.* $\overline{\text{Data}}$ polling must be performed at an address within any of the sectors being erased.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Erase Suspend

Erase Suspend command allows the user to interrupt the chip and then do data reads (not program) from a non-busy sector while it is in the middle of a Sector Erase operation (which may take up to several seconds). This command is applicable ONLY during the Sector Erase operation and will be ignored if written during the chip Erase or Programming operation. The Erase Suspend command (B0) will be allowed only during the Sector Erase Operation that will include the sector erase time-out period after the Sector Erase commands (30). Writing this command during the time-out will result in immediate termination of the time-out period. Any subsequent writes of the Sector Erase command will be taken as the Erase Resume command. Note that any other commands during the time out will reset the device to read mode. The addresses are don't-cares in writing the erase Suspend or Erase Resume commands.

When the Erase Suspend command is written during a Sector Erase operation, the chip will take between 0.1 µs to 15 µs to suspend the erase operation and go into erase suspended read mode (pseudo-read mode), during which the user can read from a sector that is NOT being erased. A read from a sector being erased may result in invalid data. The user must monitor the toggle bit to determine if the chip has entered the pseudo-read mode, at which time the toggle bit stops toggling. An address of a sector NOT being erased must be used to read the toggle bit, otherwise the user may encounter intermittent problems. Note that the user must keep track of what state the chip is in since there is no external indication of whether the chip is in pseudo-read mode or actual read mode. After the user writes the Erase Suspend command and waits until the toggle bit stops toggling, data reads from the device may then be performed. Any further writes of the Erase Suspend command at this time will be ignored.

Every time an Erase Suspend command followed by an Erase Resume command is written, the internal (pulse) counters are reset. These counters are used to count the number of high voltage pulses the memory cell requires to program or erase. If the count exceeds a certain limit, then the DQ5 bit will be set (Exceeded Time Limit flag). This resetting of the counters is necessary since the Erase Suspend command can potentially interrupt or disrupt the high voltage pulses.

To resume the operation of Sector Erase, the Resume command (30) should be written. Any further writes of the Resume command at this point will be ignore. Another Erase Suspend command can be written after the chip has resumed.

Write Operation Status

Table 6. Hardware Sequence Flags

	Status	DQ7	DQ6	DQ5	DQ3	DQ2–DQ0
In Progress	Auto-Programming	$\overline{\text{DQ7}}$	Toggle	0	0	($\overline{\text{D}}$)
	Program/Erase in Auto Erase	0	Toggle	0	1	
Exceeded Time Limits	Auto-Programming	$\overline{\text{DQ7}}$	Toggle	1	1	($\overline{\text{D}}$)
	Program/Erase in Auto-Erase	0	Toggle	1	1	

Note: *DQ0, DQ1, and DQ2 are reserve pins for future use. DQ4 is for AMD internal use only.*

DQ7
$\overline{\text{Data}}$ Polling

The Am29F040 device features $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read the device will produce the compliment of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7. During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a "1" at the DQ7 output. The flowchart for $\overline{\text{Data}}$ Polling (DQ7) is shown in Figure 3.

For chip erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For sector erase, the $\overline{\text{Data}}$ Polling is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. Data Polling must be performed at sector address within any of the sectors being erased and **not** a protected sector. Otherwise, the status may not be valid. Once the Embedded Algorithm operation is close to being completed, the Am29F040 data pins (DQ7) may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and DQ7 has a valid data, the data outputs on DQ0–DQ6 may be still invalid. The valid data on DQ0–DQ7 will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time-out (see Table 6).

See Figure 11 for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

DQ6
Toggle Bit

The Am29F040 also features the "Toggle Bit" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{OE}}$ toggling) data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on *the next* successive attempts. During programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{\text{WE}}$ pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. The Toggle Bit is active during the sector time out.

In programming, if the sector being written to is protected, the toggle bit will toggle for about 2 µs and then stop toggling without the data having changed. In erase, the device will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 100 µs and then drop back into read mode, having changed none of the data.

Either $\overline{CE}$ or $\overline{OE}$ toggling will cause the DQ6 to toggle.

See Figure 12 for the Toggle Bit timing specifications and diagrams.

DQ5
Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ5 will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the device under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in Table 2.

If this failure condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused, however, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this failure condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this failure condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The DQ5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ7 bit and DQ6 never stops toggling. Once the device has exceeded timing limits, the DQ5 bit will indicate a "1." Please note that this is not a device failure condition since the device was incorrectly used.

DQ3
Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ3 will remain low until the time-out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit indicates the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit. If DQ3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 were high on the second status check, the command may not have been accepted.

Refer to Table 6: Hardware Sequence Flags.

Data Protection

The Am29F040 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting form V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

Sector Protect

Sectors of the Am29F040 may be hardware protected at the users factory. The protection circuitry will disable both program and erase functions for the protected sector(s). Requests to program or erase a protected sector will be ignored by the device.

EMBEDDED ALGORITHMS

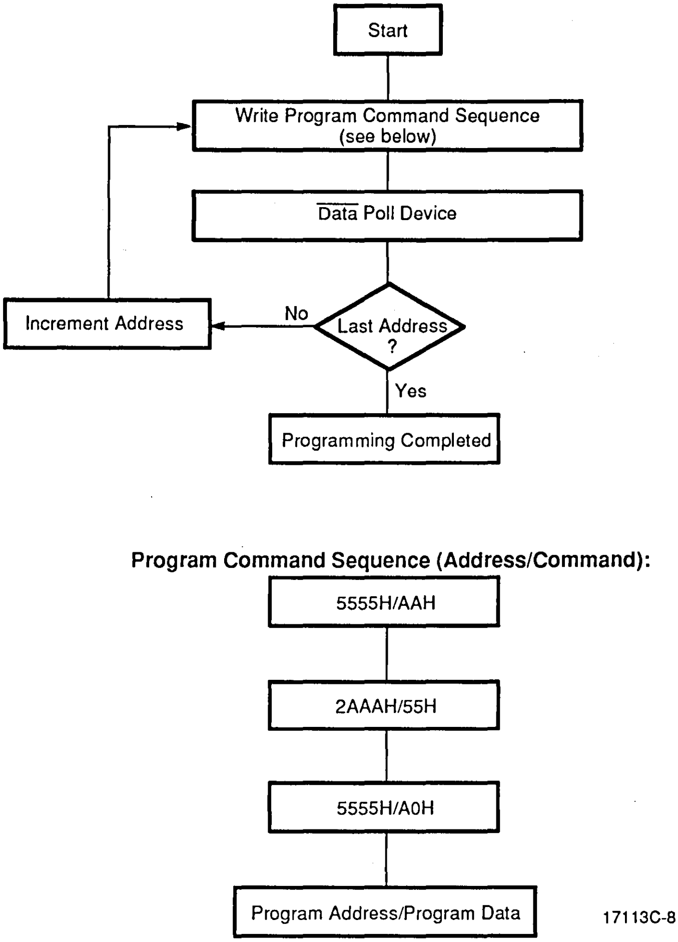


Figure 1. Embedded Programming Algorithm

Table 7. Embedded Programming Algorithm

Bus Operations	**Command Sequence**	**Comments**
Standby (Note 1)		
Write	Program	Valid Address/Data Sequence
Read		$\overline{\text{Data}}$ Polling to Verify Programming
Standby (Note 1)		Compare Data Output to Data Expected

Note: *Device is either powered-down, erase inhibit or program inhibit.*

EMBEDDED ALGORITHMS

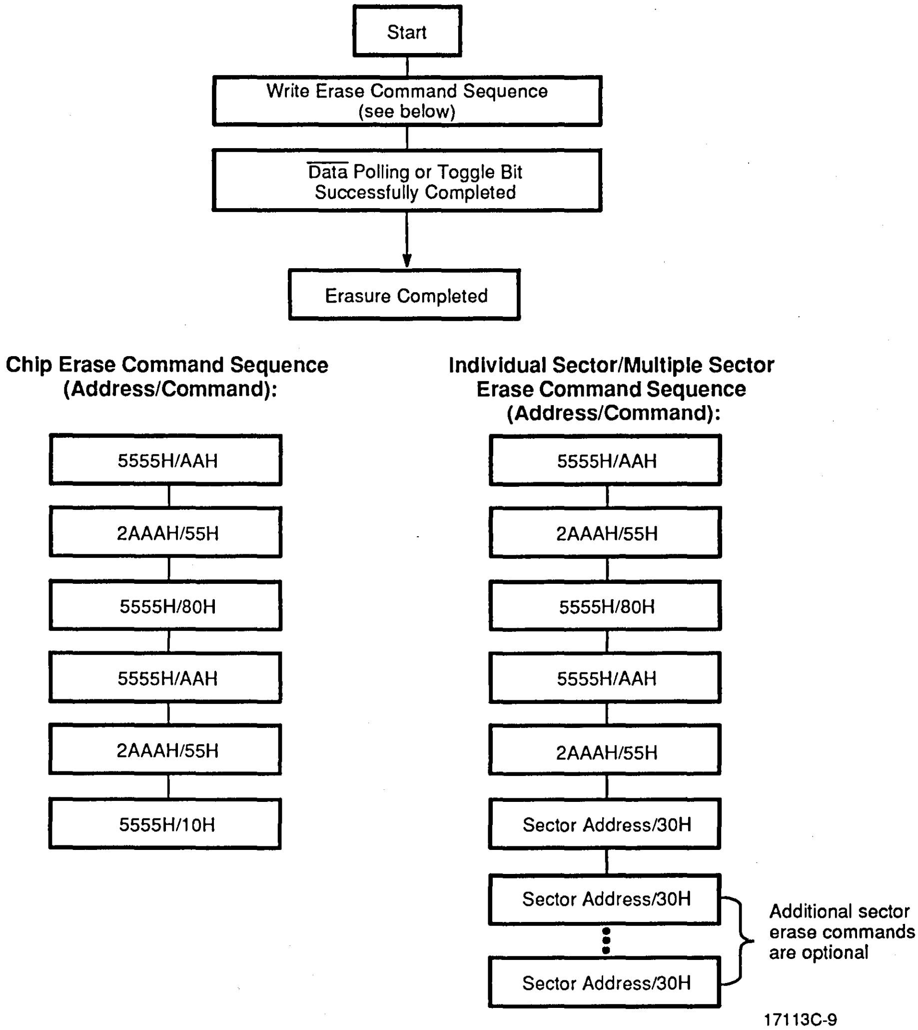
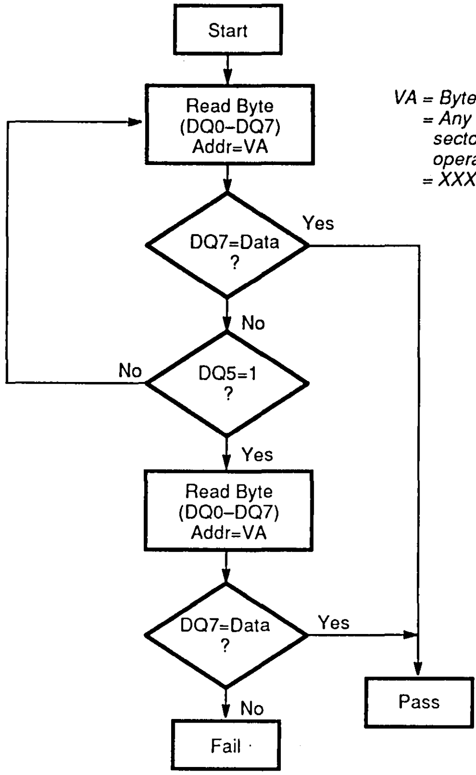


Figure 2. Embedded Erase Algorithm

Table 8. Embedded Programming Algorithm

Bus Operations	Command Sequence	Comments
Standby		
Write	Erase	
Read		Data Polling to Verify Erasure
Standby		Compare Output to FFH

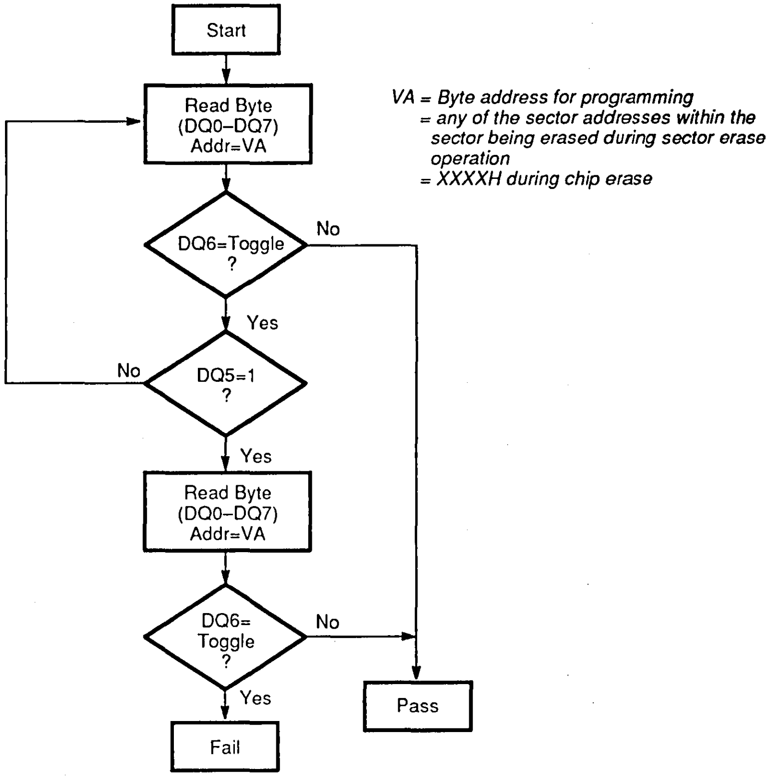


VA = Byte address for programming
= Any of the sector addresses within the sector being erased during sector erase operation
= XXXXH during chip erase

17113C-10

Note: *DQ7 is rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 3. $\overline{\text{Data}}$ Polling Algorithm

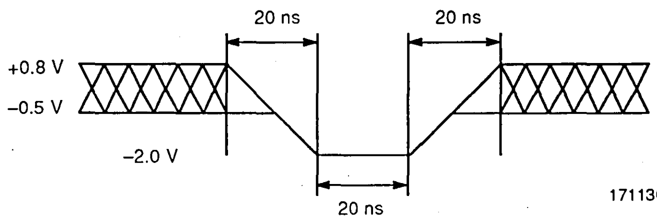


17113C-11

Note:

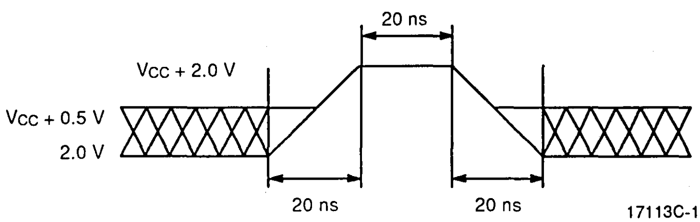
DQ6 is rechecked even if DQ5 = "1" because DQ6 may stop toggling at the same time as DQ5 changing to "1".

Figure 4. Toggle Bit Algorithm



17113C-12

Figure 5. Maximum Negative Overshoot Waveform



17113C-13

Figure 6. Maximum Positive Overshoot Waveform

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages .... –65°C to +150°C
Plastic Packages .... –65°C to +125°C

Ambient Temperature
with Power Applied .... –55°C to +125°C

Voltage with Respect to Ground
All pins except A9 (Note 1) .... –2.0 V to +7.0 V

V_{CC} (Note 1) .... –2.0 V to +7.0 V

A9 (Note 2) .... –2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ...... 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may undershoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A9 pin is –0.5 V. During voltage transitions, A9 may undershoot V to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 is +13.5 V which may overshoot to 14.0 V_{SS} for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) .... 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) .... –40°C to +85°C

Extended (E) Devices
Case Temperature (T_C) .... –55°C to +125°C

Military (M) Devices
Case Temperature (T_C) .... –55°C to +125°C

V_{CC} Supply Voltages
V_{CC} for Am29F040-75 .... +4.75 V to +5.25 V

V_{CC} for Am29F040
90, 120, 150 .... +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS

TTL/NMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.5 V		50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		±1.0	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		40	mA
I_{CC2}	V_{CC} Active Current (Notes 2, 3)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		60	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$		1.0	mA
V_{IL}	Input Low Level		–0.5	0.8	V
V_{IH}	Input High Level		2.0	V_{CC} + 0.5	V
V_{ID}	Voltage for Autoselect and Sector Protect	V_{CC} = 5.0 V	11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12 mA, $V_{CC} = V_{CC}$ Min		0.45	V
V_{OH}	Output High Level	I_{OH} = –2.5 mA $V_{CC} = V_{CC}$ Min	2.4		V
V_{LKO}	Low V_{CC} Lock-Out Voltage		3.2	4.2	V

Notes:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *I_{CC} active while Embedded Algorithm (program or erase) is in progress.*
3. *Not 100% tested.*

DC CHARACTERISTICS (continued)
CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.5 V		50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max		±1.0	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		40	mA
I_{CC2}	V_{CC} Active Current (Notes 2, 3)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		60	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{CC} \pm 0.5$ V, $\overline{OE} = V_{IL}$		100	µA
V_{IL}	Input Low Level		–0.5	0.8	V
V_{IH}	Input High Level		0.7x V_{CC}	V_{CC} +0.3	V
V_{ID}	Voltage for Autoselect and Sector Protect	V_{CC} = 5.0 V	11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 12.0 mA, $V_{CC} = V_{CC}$ Min		0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min	0.85 V_{CC}		V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC}$ Min	V_{CC} –0.4		V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2	4.2	V

Notes:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *I_{CC} active while Embedded Algorithm (program or erase) is in progress.*
3. *Not 100% tested.*

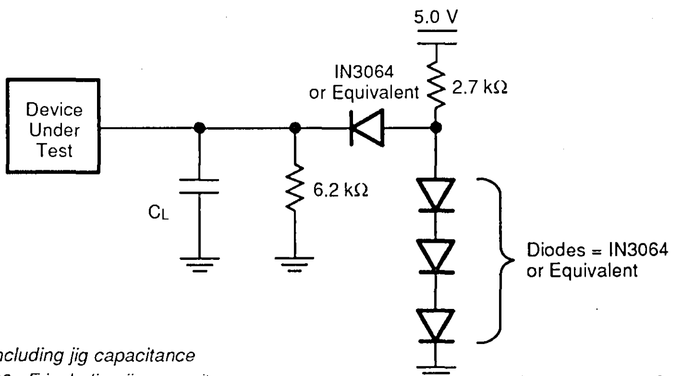
AC CHARACTERISTICS

Read Only Operations Characteristics

Parameter Symbols									
JEDEC	Standard	Description	Test Setup		-75 (Note 1)	-90 (Note 2)	-120 (Note 2)	-150 (Note 2)	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)		Min	70	90	120	150	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max	70	90	120	150	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Max	70	90	120	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max	30	35	50	55	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 3, 4)		Max	20	20	30	35	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 3, 4)			20	20	30	35	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		Min	0	0	0	0	ns

Notes:

1. *Test Conditions:*
   Output Load: 1 TTL gate and 30 pF
   Input rise and fall times: 5 ns
   Input pulse levels: 0.0 V to 3.0 V
   Timing measurement reference level
   Input: 1.5 V
   Output: 1.5 V
2. *Test Conditions:*
   Output Load: 1 TTL gate and 100 pF
   Input rise and fall times: 20 ns
   Input pulse levels: 0.45 V to 2.4 V
   Timing measurement reference level
   Input: 0.8 and 2.0 V
   Output: 0.8 and 2.0 V
3. *Output driver disable time.*
4. *Not 100% tested.*



Notes:

For –75: C_L = 30 pF including jig capacitance
For all others: C_L = 100 pF including jig capacitance

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Figure 7. Test Conditions

AC CHARACTERISTICS

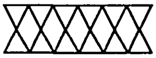
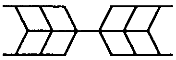
Write/Erase/Program Operations

Parameter Symbols JEDEC	Standard	Description		-75	-90	-120	-150	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 4)	Min	70	90	120	150	ns
t_{AVWL}	t_{AS}	Address Setup Time	Min	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min	45	45	50	50	ns
t_{DVWH}	t_{DS}	Data Setup Time	Min	30	45	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time	Min	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time: Read (Note 4)	Min	0	0	0	0	ns
		Output Enable Hold Time: Toggle and $\overline{Data}$ Polling (Note 4)	Min	10	10	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write	Min	0	0	0	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time	Min	0	0	0	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time	Min	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min	35	45	50	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High	Min	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation	Min	16	16	16	16	µs
t_{WHWH2}	t_{WHWH2}	Erase Operation (Note 1)	Min	1.5	1.5	1.5	1.5	sec
			Max	30	30	30	30	sec
	t_{VCS}	V_{CC} Set Up Time (Note 4)	Min	50	50	50	50	µs
	t_{VLHT}	Voltage Transition Time (Notes 2, 4)	Min	4	4	4	4	µs
	t_{WPP}	Write Pulse Width (Note 2)	Min	100	100	100	100	µs
	t_{OESP}	$\overline{OE}$ Setup Time to $\overline{WE}$ Active (Notes 2, 4)	Min	4	4	4	4	µs
	t_{CSP}	$\overline{CE}$ Setup Time to $\overline{WE}$ Active (Notes 3, 4)	Min	4	4	4	4	µs

Notes:

1. *This does not include the preprogramming time.*
2. *These timings are for Sector Protect/Unprotect operations.*
3. *This timing is only for Sector Unprotect.*
4. *Not 100% tested.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS

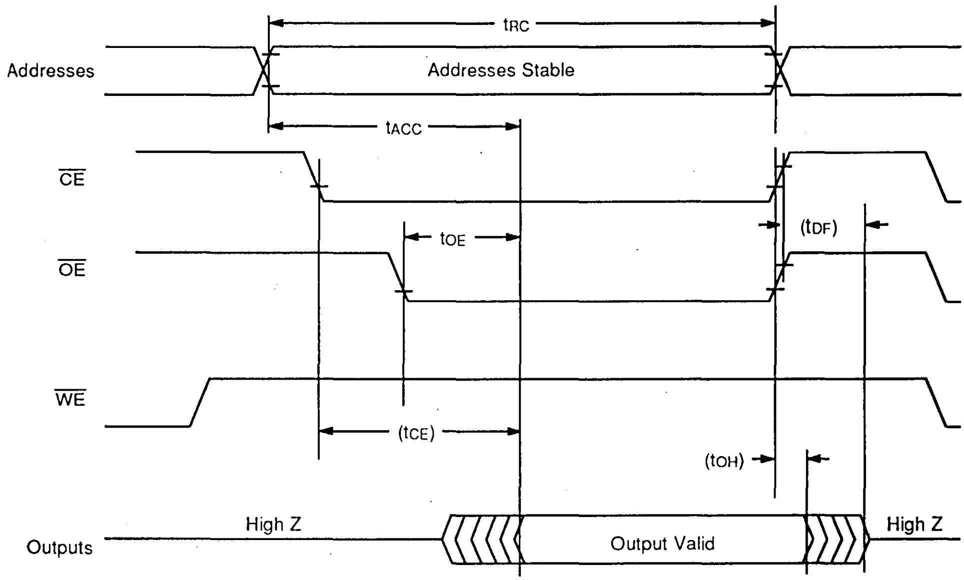


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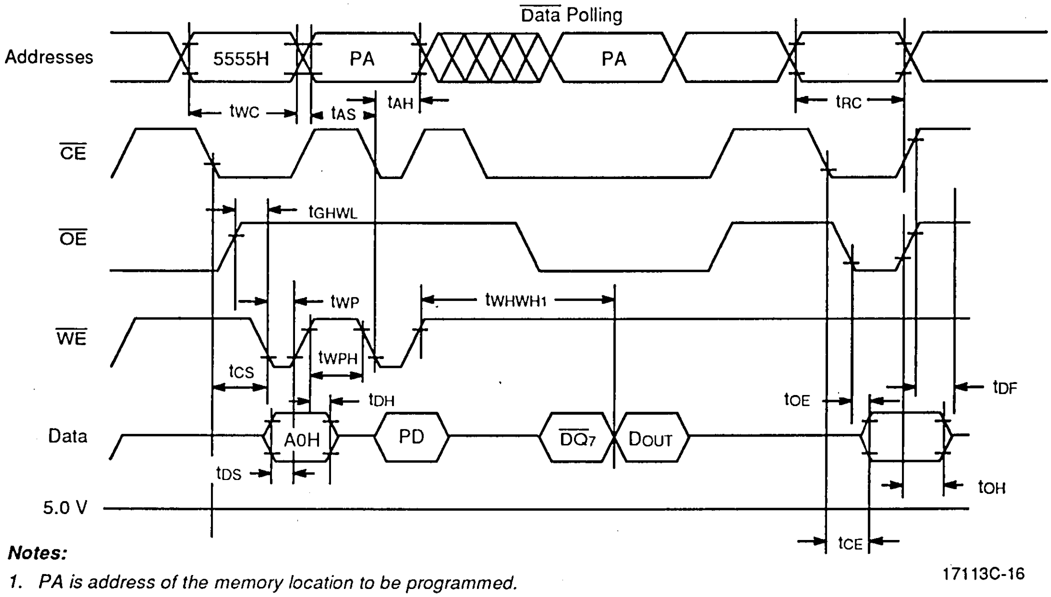
Figure 8. AC Waveforms for Read Operations

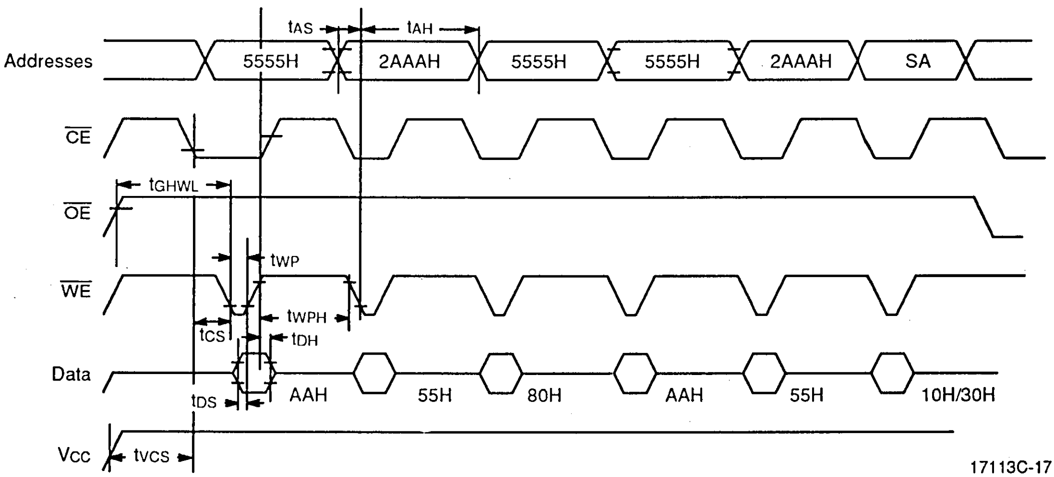
SWITCHING WAVEFORMS



Notes:

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
4. *DOUT is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*

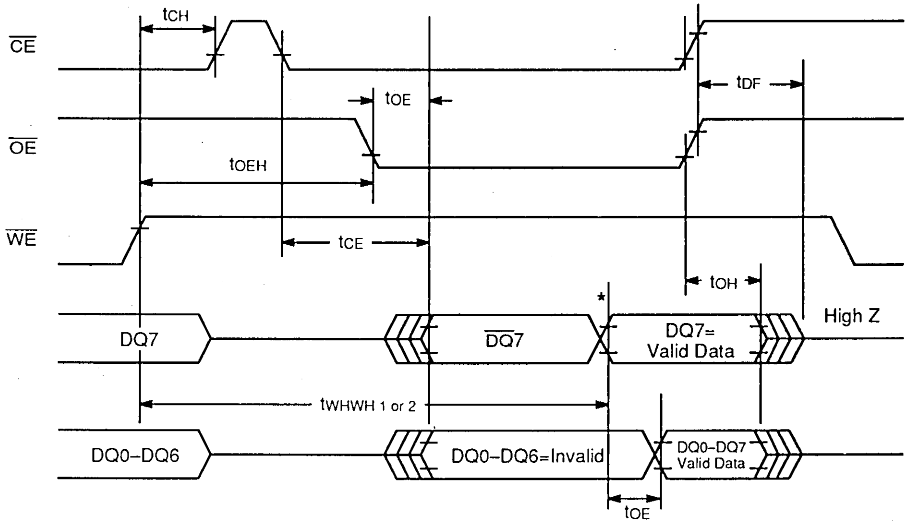
Figure 9. Program Operation Timings



Note: *SA is the sector address for Sector Erase. Addresses = don't care for Chip Erase.*

Figure 10. AC Waveforms Chip/Sector Erase Operations

SWITCHING WAVEFORMS



*DQ7=Valid Data (The device has completed the Embedded operation).

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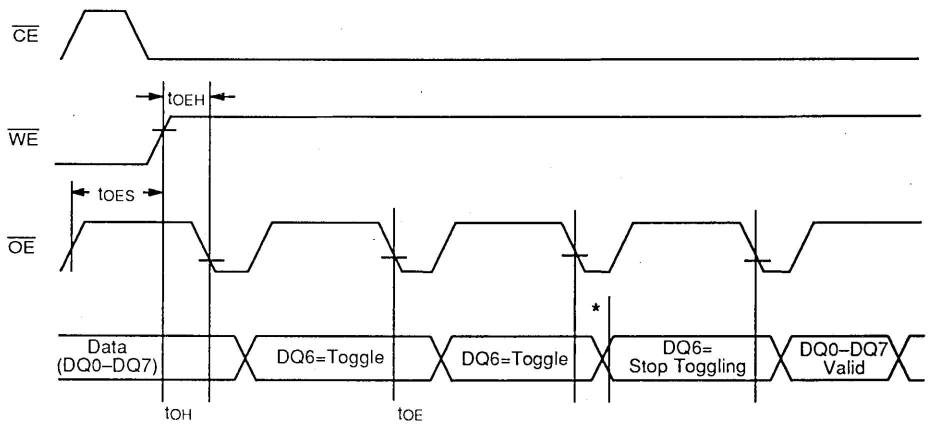
Figure 11. AC Waveforms for Data Polling during Embedded Algorithm Operations



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Note: **DQ6 stops toggling (The device has completed the Embedded operation).*

Figure 12. AC Waveforms for Toggle Bit during Embedded Algorithm Operations

SECTOR PROTECTION ALGORITHMS

Sector Protection

The Am29F040 features hardware sector protection which will disable both program and erase operations to an individual sector or any group of sectors. To activate this mode, the programming equipment must force V_{ID} on control pin $\overline{OE}$ and address pin A9. The sector addresses should be set using higher address lines A18, A17, and A16. The protection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to verify if a sector is protected during the sector protection operation. This is done by setting A6 = $\overline{CE}$ = $\overline{OE}$ = V_{IL} and $\overline{WE}$ = V_{IH} (A9 remains high at V_{ID}). Reading the device at address location XXX2H, where the higher order addresses (A18, A17, and A16) define a particular sector, will produce 01H at data outputs (DQ0–DQ7) for a protected sector.

Sector Unprotect

The Am29F040 also features a sector unprotect mode, so that a protected sector may be unprotected to incorporate any changes in the code. All sectors should be protected prior to unprotecting any sector.

To activate this mode, the programming equipment must force V_{ID} on control pins $\overline{OE}$, $\overline{CE}$, and address pin A9. The address pins A6, A16, and A12 should be set to V_{IH}. The unprotection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to determine if a sector is unprotected in the system by writing the autoselect command and A6 is set at V_{IH}. Performing a read operation at address location XXX2H, where the higher order addresses (A18, A17, and A16) define a particular sector address, will produce 00H at data outputs (DQ0–DQ7) for an unprotected sector.

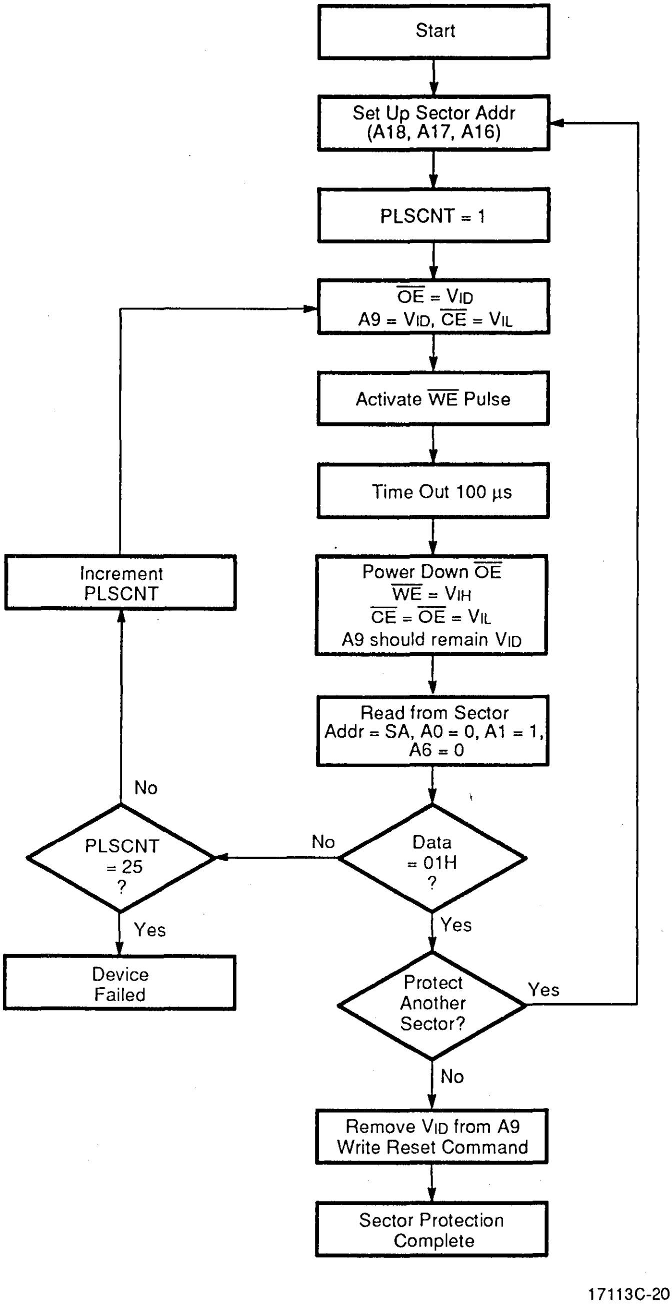
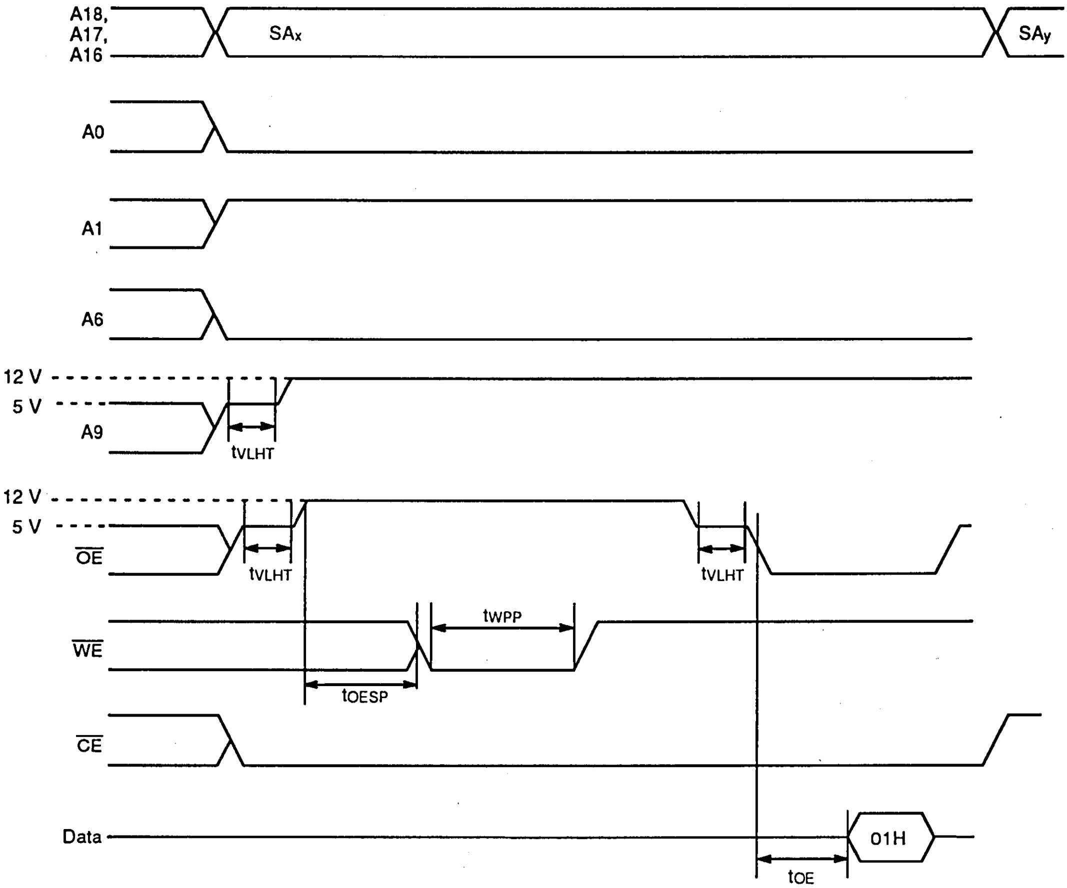


Figure 13. Sector Protection Algorithm

SWITCHING WAVEFORMS



SA_x = Sector Address for initial sector
SA_y = Sector Address for next sector

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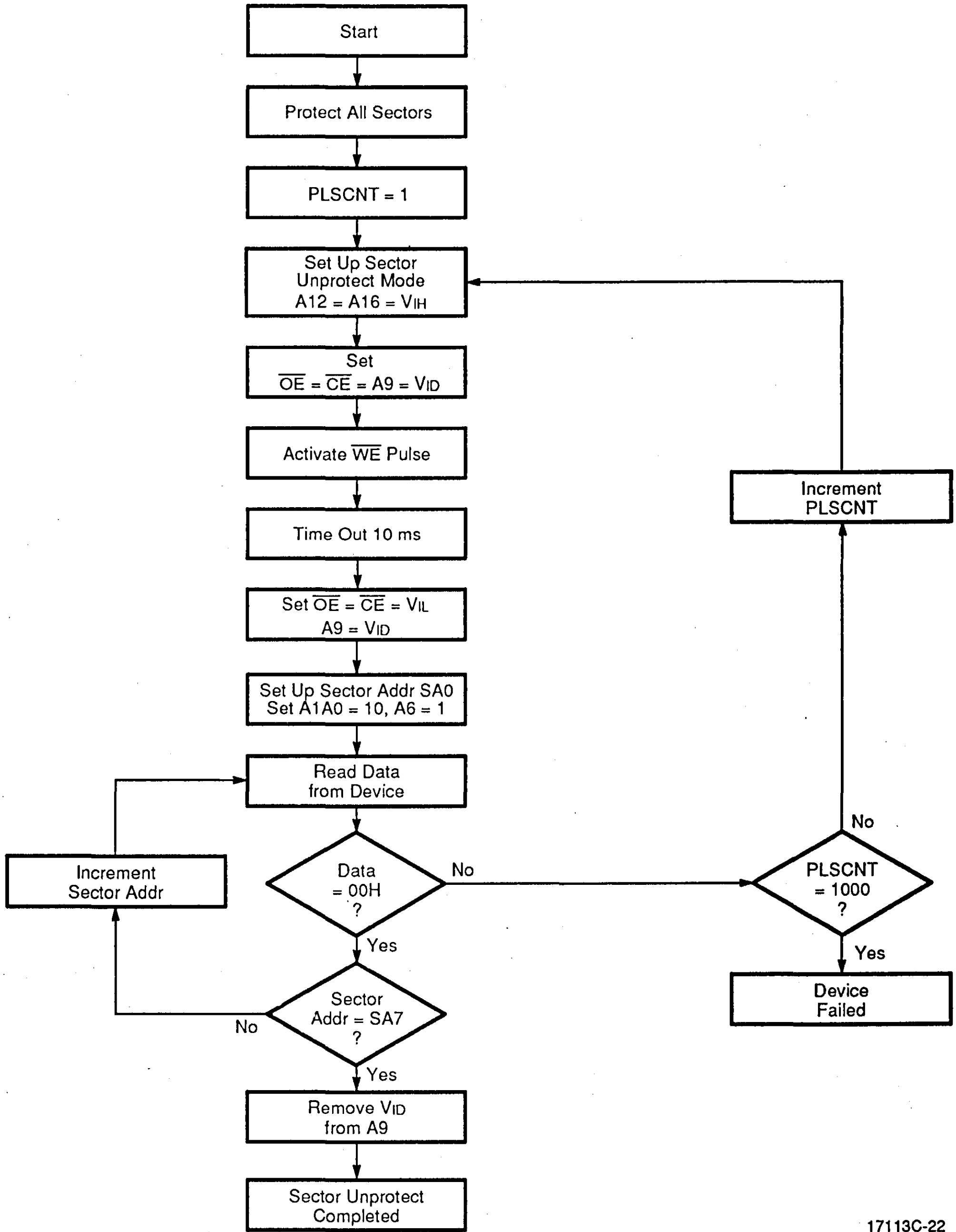
Figure 14. AC Waveforms for Sector Protection



Notes:

SA0 = Sector Address for initial sector
SA7 = Sector Address for last sector
Please refer to Table 4 for details.

Figure 15. Sector Unprotect Algorithm

SWITCHING WAVEFORMS

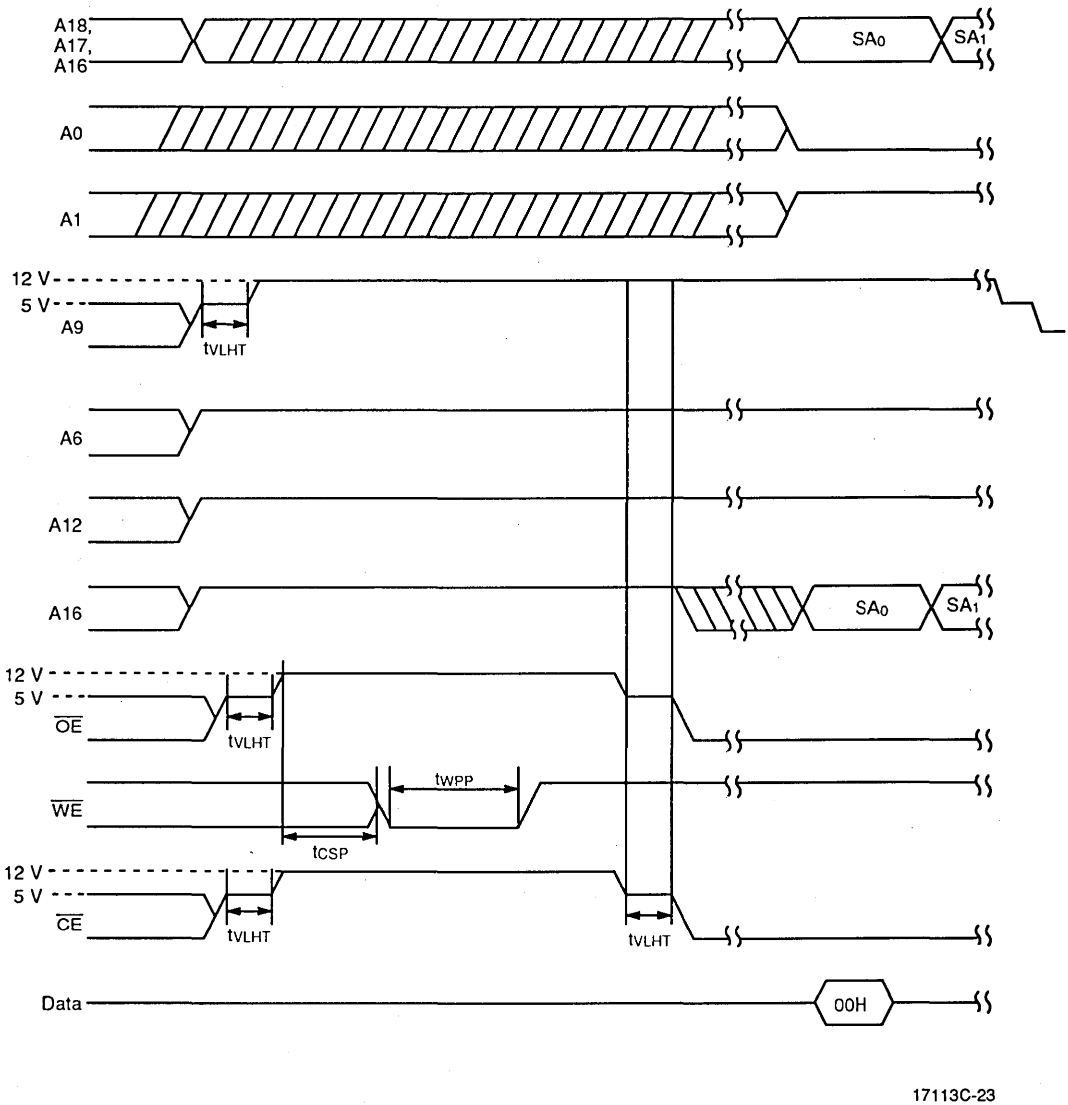


Figure 16. AC Waveforms for Sector Unprotect

AC CHARACTERISTICS

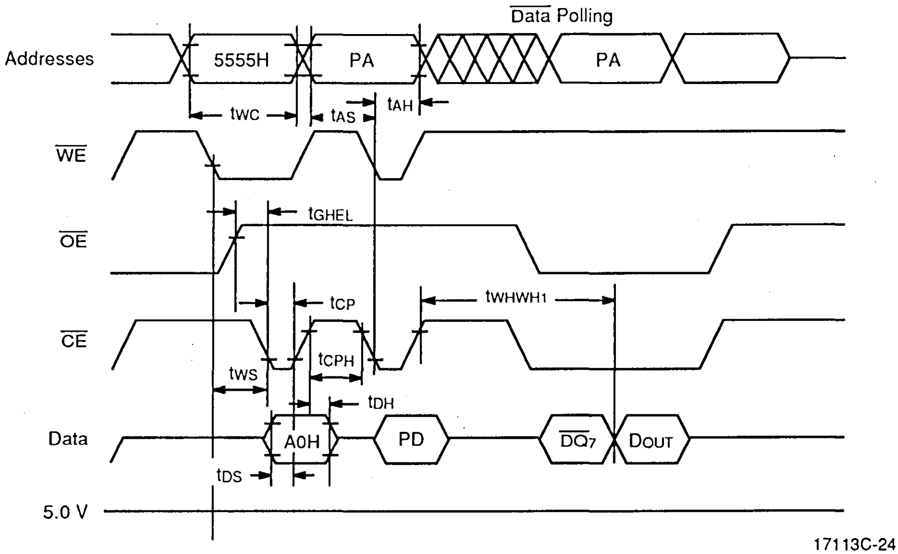
Write/Erase/Program Operations

Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols JEDEC	Standard	Description			-75	-90	-120	-150	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 4)		Min	70	90	120	150	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	45	50	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	30	45	50	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time		Min	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read (Note 4)	Min	0	0	0	0	ns
			Toggle and $\overline{Data}$ Polling (Note 4)	Min	10	10	10	10	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write		Min	0	0	0	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time		Min	0	0	0	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		Min	0	0	0	0	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width		Min	35	45	50	50	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High		Min	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Min	16	16	16	16	µs
t_{WHWH2}	t_{WHWH2}	Erase Operation (Note 1)		Min	1.5	1.5	1.5	1.5	sec
				Max	30	30	30	30	sec
	t_{VCS}	Vcc Set Up Time (Note 4)		Min	50	50	50	50	µs

Notes:

1. *This does not include the preprogramming time.*
2. *These timings are for Sector Protect/Unprotect operations.*
3. *This timing is only for Sector Unprotect.*
4. *Not 100% tested.*



Notes:

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *$\overline{DQ_7}$ is the output of the complement of the data written to the device.*
4. *DOUT is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*

Figure 17. Alternate $\overline{CE}$ Controlled Program Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits Min	Typ	Max	Unit	Comments
Chip and Sector Erase Time		1.5 (Note 1)	30	sec	Excludes 00H programming prior to erasure
Byte Programming Time		16	1000 (Note 2)	µs	Excludes system-level overhead
Chip Programming Time		8.5 (Note 1)	50	sec	Excludes system-level overhead
Erase/Program Cycles	100,000	1,000,000		Cycles	

Notes:

1. *25°C, 5 V V_{CC}, 100,000 cycles*
2. *When programming a "1" over a "0", the Embedded Algorithms allow for 48 ms byte program time.*

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.

LCC PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	6	7.5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8.5	12	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	7.5	9	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz*

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	6	7.5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8.5	12	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	7.5	9	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz*

PLCC PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	Control Pin Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A = 25°C$, $f = 1.0$ MHz*

PDIP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	Control Pin Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A = 25°C$, $f = 1.0$ MHz*

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

DATA SHEET REVISION SUMMARY FOR Am29F040

Title

Specify "4 Megabit" density.

Distinctive Characteristics

Include "Read" under first bullet.

General Description

Include statement "Am29F040 is erased when shipped from factory."

Autoselect

Correction in text (V_{ID}) from 13 V to 12.5 V.

Table 5. Am29F040 Command Definition

Clarify Note 1, remove A16, A17, and A18 in second sentence.

Byte Programming

Clarify the statement "hang up the device" by including "exceed timing limits."

DC Characteristics CMOS Compatible Table

Add parameters I_{LI}: "Input Load Current" and I_{LIT}: "A9 Input Load Current" to be consistent with TTL/NMOS compatible table.

Figure 12. AC Waveforms for Toggle Bit during Embedded Algorithm Operations

Identify parameter "t_{OES}"

Figure 15. AC Waveforms for Sector Protection

$\overline{CE}$ Waveform is altered to show preferred method; this change is also reflected in Figure 13. Sector Protection Algorithm flow chart.

Data Retention Table

Added to be consistent with all other data sheets.

PRELIMINARY

Am29F400T/Am29F400B

4 Megabit (524,288 x 8-Bit/262,144 x 16-Bit) CMOS 5.0 Volt-only, Sector Erase Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% read, write, and erase**
  - Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  - Uses same software commands as E²PROMs
- **Compatible with JEDEC-standard word-wide pinouts**
  - 44-pin SO
  - 48-pin TSOP
- **Minimum 100,000 write/erase cycles**
- **High performance**
  - 70 ns maximum access time
- **Sector erase architecture**
  - One 16 Kbyte, two 8 Kbytes, one 32 Kbyte, and seven 64 Kbytes
  - Any combination of sectors can be concurrently erased. Also supports full chip erase.
- **Embedded Erase Algorithms**
  - Automatically pre-programs and erases the chip or any sector
- **Embedded Program Algorithms**
  - Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Low power consumption**
  - 20 mA typical active read current for Byte Mode
  - 28 mA typical active read current for Word Mode
  - 30 mA typical write/erase current
  - 25 µA typical standby current
- **Low V_{CC} write inhibit ≤ 3.2 V**
- **Sector protection**
  - Hardware method disables any combination of sectors from write or erase operations
- **Erase Suspend/Resume**
  - Suspends the erase operation to allow a read in another sector within the same device
- **Boot Code Sector Architecture**
  - T = Top sector
  - B = Bottom sector

GENERAL DESCRIPTION

The Am29F400 is a 4 Mbit, 5.0 V-only Flash memory organized as 512K bytes of 8 bits each or 256K words of 16 bits each. The Am29F400 is offered in 44-pin SO and 48-pin TSOP packages. This device is designed to be programmed in-system with the standard system 5.0 V V_{CC} supply. A 12.0 V V_{PP} is not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers. The Am29F400 is erased when shipped from the factory.

The standard Am29F400 offers access times between 70 ns and 150 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{CE}$), write enable ($\overline{WE}$) and output enable ($\overline{OE}$) controls.

The Am29F400 is pin and command set compatible with JEDEC standard 4 Mbit E²PROMs. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

PRODUCT SELECTOR GUIDE

Family Part No:		Am29F400			
Ordering Part No:	V_{CC} = 5.0 V ± 5%	**-75**			
	V_{CC} = 5.0 V ± 10%		**-90**	**-120**	**-150**
Max Access Time (ns)		70	90	120	150
$\overline{CE}$ ($\overline{E}$) Access (ns)		70	90	120	150
$\overline{OE}$ ($\overline{G}$) Access (ns)		30	35	50	55

Publication# **18612** Rev. **A** Amendment/**0**
Issue Date: **March 1994**

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

The Am29F400 is programmed by executing the program command sequence. This will invoke the Embedded Program Algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Typically, each sector can be programmed and verified in less than one second. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase Algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The entire chip or any individual sector is typically erased and verified in 1.5 seconds (if already completely preprogrammed).

This device also features a sector erase architecture. The sector mode allows each sector to be erased and reprogrammed without affecting other sectors.

The device features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by $\overline{\text{Data}}$ Polling of DQ7, by the Toggle Bit feature on DQ6, or the RY/$\overline{\text{BY}}$ pin. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

AMD's Flash technology combines years of EPROM and E²PROM experience to produce the highest levels of quality, reliability and cost effectiveness. The Am29F400 memory electrically erases the entire chip or all bits within a sector simultaneously via Fowler-Nordhiem tunneling. The bytes/words are programmed one byte/word at a time using the EPROM programming mechanism of hot electron injection.

Flexible Sector-Erase Architecture

- One 16 Kbyte, two 8 Kbytes, one 32 Kbyte, and seven 64 Kbytes,
- Individual-sector, multiple-sector, or bulk-erase capability
- Individual or multiple-sector protection is user definable

Sector	Address
16 Kbyte	7FFFFh
8 Kbyte	7BFFFh
8 Kbyte	79FFFh
32 Kbyte	77FFFh
64 Kbyte	6FFFFh
64 Kbyte	5FFFFh
64 Kbyte	4FFFFh
64 Kbyte	3FFFFh
64 Kbyte	2FFFFh
64 Kbyte	1FFFFh
64 Kbyte	0FFFFh
	00000h

Am29F400T Sector Architecture

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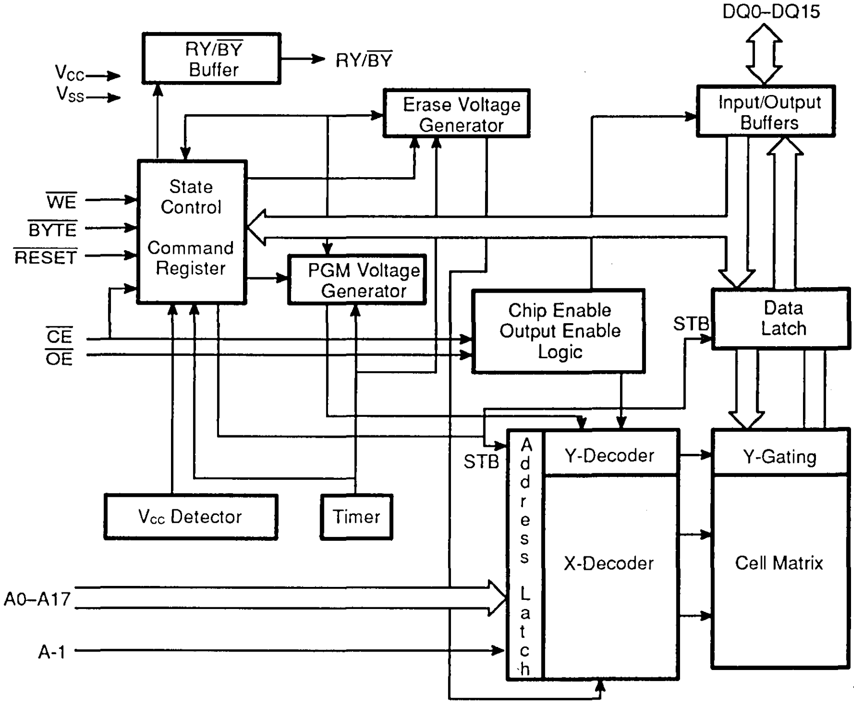
Sector	Address
64 Kbyte	7FFFFh
64 Kbyte	6FFFFh
64 Kbyte	5FFFFh
64 Kbyte	4FFFFh
64 Kbyte	3FFFFh
64 Kbyte	2FFFFh
64 Kbyte	1FFFFh
32 Kbyte	0FFFFh
8 Kbyte	07FFFh
8 Kbyte	05FFFh
16 Kbyte	03FFFh
	00000h

Am29F400B Sector Architecture

18612A-2

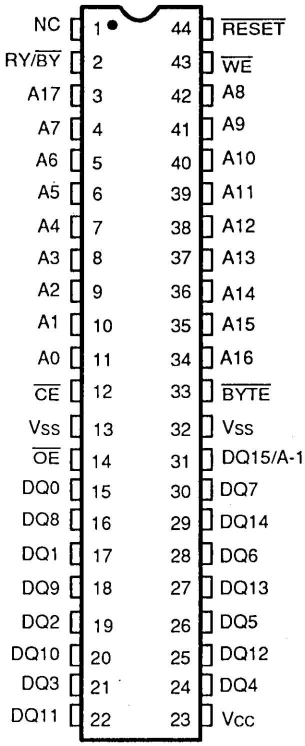
BLOCK DIAGRAM



18612A-3

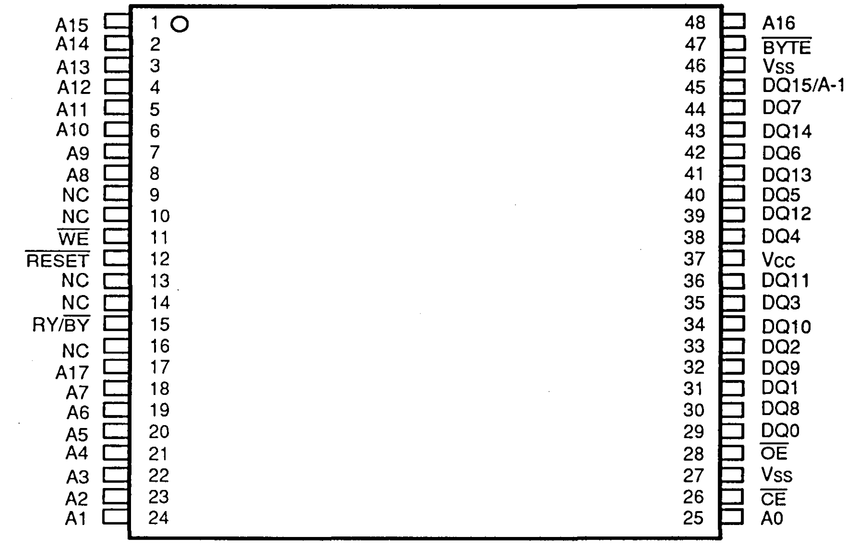
CONNECTION DIAGRAMS

SO



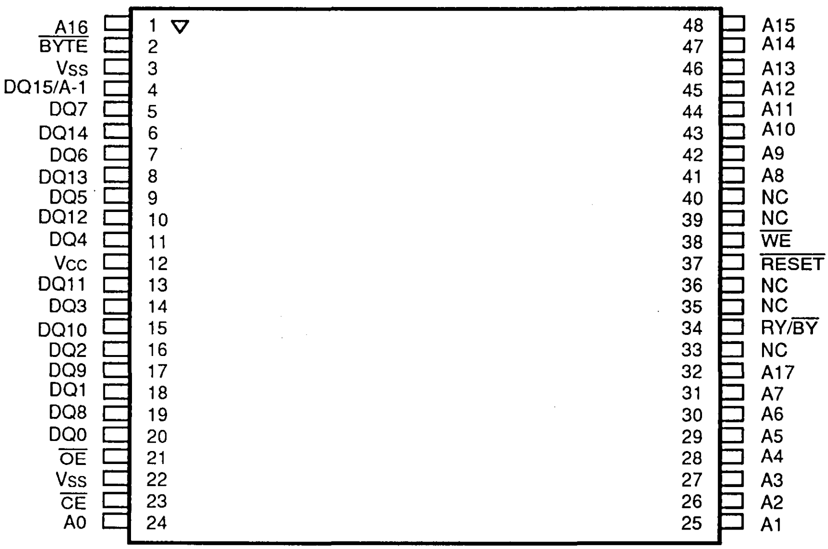
18612A-4

CONNECTION DIAGRAMS



Standard TSOP

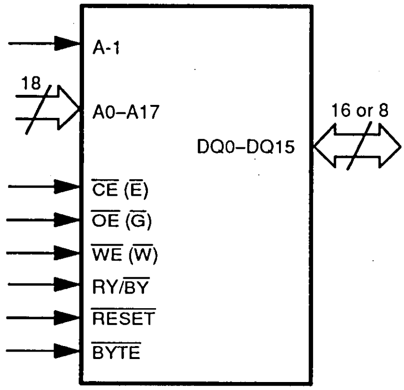
18612A-5



Reverse TSOP

18612A-6

LOGIC SYMBOL



18612A-7

Table 1. Am29F400 Pin Configuration

Pin	Function
A-1, A0–A17	Address Inputs
DQ0–DQ15	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
RY/$\overline{BY}$	Ready-Busy Input
$\overline{RESET}$	Hardware Reset Pin/Sector Protect Unlock
$\overline{BYTE}$	Selects 8-bit or 16-bit mode
NC	No Internal Connection
V_{SS}	Device Ground
V_{CC}	Device Power Supply (5.0 V ± 10% or ± 5%)

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

Am29F400 T -75 E C B

OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-In

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended (–55°C to +125°C)

PACKAGE TYPE
E = 48-Pin Thin Small Outline Package (TSOP) Standard Pinout (TS 048)
F = 48-Pin Thin Small Outline Package (TSOP) Reverse Pinout (TSR 048)
S = 44-Pin Small Outline Package, (SO 044)

SPEED OPTION
See Product Selector Guide and Valid Combinations

BOOT CODE SECTOR ARCHITECTURE
T = Top sector
B = Bottom sector

DEVICE NUMBER/DESCRIPTION
Am29F400
4 Megabit (512K x 8-Bit or 256K x 16-Bit) CMOS Flash Memory
5.0 V-only Program and Erase

Valid Combinations	
Am29F400T/B-75	EC, FC, SC
Am29F400T/B-90	EC, EI, FC, FI, EE, EEB, FE, FEB, SC, SI, SE, SEB
Am29F400T/B-120	
Am29F400T/B-150	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 2. Am29F400 User Bus Operations ($\overline{BYTE}$ = V_{IH})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	DQ0–DQ15	$\overline{RESET}$
Auto-Select Manufacturer Code (1)	L	L	H	L	L	L	V_{ID}	Code	H
Auto-Select Device Code (1)	L	L	H	H	L	L	V_{ID}	Code	H
Read (3)	L	L	H	A0	A1	A6	A9	D_{OUT}	H
Standby	H	X	X	X	X	X	X	HIGH Z	H
Output Disable	L	H	H	X	X	X	X	HIGH Z	X
Write	L	H	L	A0	A1	A6	A9	D_{IN}	H
Enable Sector Protect	L	V_{ID}	L	X	X	X	V_{ID}	X	H
Verify Sector Protect (2)	L	L	H	L	H	L	V_{ID}	Code	H
Temporary Sector Unprotect	X	X	X	X	X	X	X	X	V_{ID}
Reset (Hardware)	X	X	X	X	X	X	X	HIGH Z	L

Table 3. Am29F400 User Bus Operations ($\overline{BYTE}$ = V_{IL})

Operation	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A0	A1	A6	A9	DQ0–DQ7	$\overline{RESET}$
Auto-Select Manufacturer Code (1)	L	L	H	L	L	L	V_{ID}	Code	H
Auto-Select Device Code (1)	L	L	H	H	L	L	V_{ID}	Code	H
Read (3)	L	L	H	A0	A1	A6	A9	D_{OUT}	H
Standby	H	X	X	X	X	X	X	HIGH Z	H
Output Disable	L	H	H	X	X	X	X	HIGH Z	X
Write	L	H	L	A0	A1	A6	A9	D_{IN}	H
Enable Sector Protect	L	V_{ID}	L	X	X	X	V_{ID}	X	H
Verify Sector Protect (2)	L	L	H	L	H	L	V_{ID}	Code	H
Temporary Sector Unprotect	X	X	X	X	X	X	X	X	V_{ID}
Reset (Hardware)	X	X	X	X	X	X	X	HIGH Z	L

Legend:

L = V_{IL}, H = V_{IH}, X = Don't Care. See DC Characteristics for voltage levels.

Notes:

1. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 7.*
2. *Refer to the section on Sector Protection.*
3. *$\overline{WE}$ can be V_{IL} if $\overline{OE}$ is V_{IL}, $\overline{OE}$ at V_{IH} initiates the write operations.*

Read Mode

The Am29F400 has two control functions which must be satisfied in order to obtain data at the outputs. $\overline{CE}$ is the power control and should be used for device selection. $\overline{OE}$ is the output control and should be used to gate data to the output pins if a device is selected.

Address access time (t_{ACC}) is equal to the delay from stable addresses to valid output data. The chip enable access time (t_{CE}) is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable for at least t_{ACC}–t_{OE} time).

Standby Mode

The Am29F400 has two standby modes, a CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), when the current consumed is less than 100 µA; and a TTL standby mode ($\overline{CE}$ is held at V_{IH}) when the current required is reduced to approximately 1 mA. In the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure or programming, the device will draw active current until the operation is completed.

Output Disable

With the $\overline{OE}$ input at a logic high level (V_{IH}), output from the device is disabled. This will cause the output pins to be in a high impedance state.

Autoselect

The autoselect mode allows the reading out of a binary code from the device and will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 12.5 V) on address pin A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All addresses are don't cares except A0, A1, and A6.

The manufacturer and device codes may also be read via the command register, for instances when the Am29F400 is erased or programmed in a system without access to high voltage on the A9 pin. The command sequence is illustrated in Table 7 (refer to Autoselect Command section).

Byte 0 (A0 = V_{IL}) represents the manufacturer's code (AMD=01H) and byte 1 (A0 = V_{IH}) the device identifier code (Am29F400T = 23H and Am29F400B = ABH for x8 mode; Am29F400T = 2223H and Am29F400B = 22ABH for x16 mode). These two bytes/words are given in the table below. All identifiers for manufacturer and device will exhibit odd parity with DQ7 defined as the parity bit. In order to read the proper device codes when executing the autoselect, A1 must be V_{IL} (see Tables 4.1 and 4.2).

Table 4.1 Am29F400 Sector Protection Verify Autoselect Codes

Type			A12–A17	A6	A1	A0	Code (HEX)
Manufacturer's Code			X	V_{IL}	V_{IL}	V_{IL}	01H
Am29F400 Device Code	Am29F400T	Byte	X	V_{IL}	V_{IL}	V_{IH}	23H
		Word					2223H
	Am29F400B	Byte	X	V_{IL}	V_{IL}	V_{IH}	ABH
		Word					22ABH
Sector Protection			Sector Addresses	V_{IL}	V_{IH}	V_{IL}	01H*

**Outputs 01H at protected sector addresses*

Table 4. 2 Expanded Autoselect Code Table

Type		Code	DQ15	DQ14	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer's Code		01H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Am29F400 Device Code	Am29F400T(B)	23H	A–1	HI–Z	HI–Z	HI–Z	HI–Z	HI–Z	HI–Z	HI–Z	0	0	1	0	0	0	1	1
	(W)	2223H	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1
	Am29F400B(B)	ABH	A–1	HI–Z	HI–Z	HI–Z	HI–Z	HI–Z	HI–Z	HI–Z	1	0	1	0	1	0	1	1
	(W)	22ABH	0	0	1	0	0	0	1	0	1	0	1	0	1	0	1	1
Sector Protection		01H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

(B) – Byte mode

(W) – Word mode

Table 5. Sector Address Tables (Am29F400T)

	A17	A16	A15	A14	A13	A12	Address Range
SA0	0	0	0	X	X	X	00000h–0FFFFh
SA1	0	0	1	X	X	X	10000h–1FFFFh
SA2	0	1	0	X	X	X	20000h–2FFFFh
SA3	0	1	1	X	X	X	30000h–3FFFFh
SA4	1	0	0	X	X	X	40000h–4FFFFh
SA5	1	0	1	X	X	X	50000h–5FFFFh
SA6	1	1	0	X	X	X	60000h–6FFFFh
SA7	1	1	1	0	X	X	70000h–77FFFh
SA8	1	1	1	1	0	0	78000h–79FFFh
SA9	1	1	1	1	0	1	7A000h–7BFFFh
SA10	1	1	1	1	1	X	7C000h–7FFFFh

Table 6. Sector Address Tables (Am29F400B)

	A17	A16	A15	A14	A13	A12	Address Range
SA0	0	0	0	0	0	X	00000h–03FFFh
SA1	0	0	0	0	1	0	04000h–05FFFh
SA2	0	0	0	0	1	1	06000h–07FFFh
SA3	0	0	0	1	X	X	08000h–0FFFFh
SA4	0	0	1	X	X	X	10000h–1FFFFh
SA5	0	1	0	X	X	X	20000h–2FFFFh
SA6	0	1	1	X	X	X	30000h–3FFFFh
SA7	1	0	0	X	X	X	40000h–4FFFFh
SA8	1	0	1	X	X	X	50000h–5FFFFh
SA9	1	1	0	X	X	X	60000h–6FFFFh
SA10	1	1	1	X	X	X	70000h–7FFFFh

Write

Device erasure and programming are accomplished via the command register. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device.

The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The command register is written to by bringing $\overline{WE}$ to V_{IL}, while $\overline{CE}$ is at V_{IL} and $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later; while data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Sector Protection

The Am29F400 features hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 10). The sector protect feature is enabled using programming equipment at the user's site. The device is shipped with all sectors unprotected. Alternatively, AMD may program and protect sectors in the factory prior to shipping the device (AMD's ExpressFlash™ Service).

To activate this mode, the programming equipment must force V_{ID} on address pin A9 and control pin $\overline{OE}$, (suggest V_{ID} = 11.5 V) and $\overline{CE}$ = V_{IL}. The sector addresses (A17, A16, A15, A14, A13, and A12) should be set to the sector to be protected. Tables 5 and 6 define the sector address for each of the eleven (11) individual sectors. Programming of the protection circuitry begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same. Sector addresses must be held constant during the $\overline{WE}$ pulse. Refer to figures 17 and 18 for sector protection algorithm and waveforms.

To verify programming of the protection circuitry, the programming equipment must force V_{ID} on address pin A9 with $\overline{CE}$ and $\overline{OE}$ at V_{IL} and $\overline{WE}$ at V_{IH}. Scanning the sector addresses (A17, A16, A15, A14, A13, and A12) while (A6, A1, A0) = (0, 1, 0) will produce a logical "1" code at device output DQ0 for a protected sector. Otherwise the device will produce 00H for an unprotected sector. In this mode, the lower order addresses, except for A0, A1, and A6 are don't care. Address locations with A1 = V_{IL} are reserved for Autoselect manufacturer and device codes.

It is also possible to determine if a sector is protected in the system by writing an Autoselect command. Performing a read operation at the address location XX02H, where the higher order addresses (A17, A16, A15, A14, A13, and A12) are the sector address will produce a logical "1" at DQ0 for a protected sector. See Table 4.1 for Autoselect codes.

Temporary Sector Unprotect

This feature allows temporary unprotection of previously protected sectors of the Am29F400 device in order to change data. The Sector Unprotect mode is activated by setting the $\overline{RESET}$ pin to high voltage (12 V). During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once the 12 V is taken away from the $\overline{RESET}$ pin, all the previously protected sectors will be protected again.

Sector Unprotect

The Am29F400 also features a sector unprotect mode, so that a protected sector may be unprotected to incorporate any changes in the code. All sectors should be protected prior to unprotecting any sector.

To activate this mode, the programming equipment must force V_{ID} on control pin $\overline{OE}$ and address pin A9. The $\overline{CE}$ and A0 pins must be set at V_{IL}. Pins A6 and A1 must be set to V_{IH}. Refer to Figure 19 for the sector unprotect algorithm. The unprotection mechanism begins on the falling edge of the $\overline{WE}$ pulse and is terminated with the rising edge of the same.

It is also possible to determine if a sector is unprotected in the system by writing the autoselect command and A6 is set at V_{IL}. Performing a read operation at address location XXX2H, where the higher order addresses (A17, A16, A15, A14, A13, and A12) define a particular sector address, will produce 00H at data outputs (DQ0–DQ7) for an unprotected sector.

Command Definitions

Device operations are selected by writing specific address and data sequences into the command register. **Writing incorrect address and data values or writing them in the improper sequence will reset the device to the read mode**. Table 7 defines the valid register command sequences. Note that the Erase Suspend (B0) and Erase Resume (30) commands are valid only while the Sector Erase operation is in progress. Either of the two reset commands will reset the device (when applicable). Please note that commands are always written at DQ0–DQ7 and DQ8–DQ15 bits are ignored.

Table 7. Am29F400 Command Definitions

Command Sequence Read/Reset		Bus Write Cycles Req'd	First Bus Write Cycle		Second Bus Write Cycle		Third Bus Write Cycle		Fourth Bus Read/Write Cycle		Fifth Bus Write Cycle		Sixth Bus Write Cycle	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset		1	XXXXH	F0H										
Read/Reset	Word	4	5555H	AAH	2AAAH	55H	5555H	F0H	RA	RD				
	Byte		AAAAH		5555H		AAAAH							
Autoselect	Word	4	5555H	AAH	2AAAH	55H	5555H	90H						
	Byte		AAAAH		5555H		AAAAH							
Program	Word	4	5555H	AAH	2AAAH	55H	5555H	A0H	PA	Data				
	Byte		AAAAH		5555H		AAAAH							
Chip Erase	Word	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
	Byte		AAAAH		5555H		AAAAH		AAAAH		5555H		AAAAH	
Sector Erase	Word	6	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	SA	30H
	Byte		AAAAH		5555H		AAAAH		AAAAH		5555H			
Sector Erase Suspend			Erase can be suspended during sector erase with Addr (don't care), Data (B0H)											
Sector Erase Resume			Erase can be resumed after suspend with Addr (don't care), Data (30H)											

Notes:

1. *Address bit A15 = X = Don't Care for all address commands except for Program Address (PA) and Sector Address (SA). Write Sequences may be initiated with A15 in either state.*
2. *Address bits A16 = X = Don't Care for all address commands except for Program Address (PA) and Sector Address (SA).*
3. *Bus operations are defined in Table 2.*
4. *RA = Address of the memory location to be read.*
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   SA = Address of the sector to be erased. The combination of A16, A15, A14, A13, and A12 will uniquely select any sector.
5. *RD = Data read from location RA during read operation.*
   PD = Data to be programmed at location PA. Data is latched on the falling edge of $\overline{WE}$.
6. *The system should generate the following address patterns:*
   Word Mode: 5555H or 2AAAH to addresses A0 – A14
   Byte Mode: AAAAH or 5555H to addresses A-1 – A14.

Read/Reset Command

The read or reset operation is initiated by writing the read/reset command sequence into the command register. Microprocessor read cycles retrieve array data from the memory. The device remains enabled for reads until the command register contents are altered.

The device will automatically power-up in the read/reset state. In this case, a command sequence is not required to read data. Standard microprocessor read cycles will retrieve array data. This default value ensures that no spurious alteration of the memory content occurs during the power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Autoselect Command

Flash memories are intended for use in applications where the local CPU alters memory contents. As such, manufacture and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto the address lines is not generally desired system design practice.

The device contains an autoselect command operation to supplement traditional PROM programming methodology. The operation is initiated by writing the autoselect command sequence into the command register. Following the command write, a read cycle from address XX00H retrieves the manufacture code of 01H. A read cycle from address XX01H returns the device code (Am29F400T = 23H and Am29F400B = ABH for x8 mode; Am29F400T = 2223H and Am29F400B = 22ABH for x16 mode) (see Tables 4.1 and 4.2).

All manufacturer and device codes will exhibit odd parity with DQ7 defined as the parity bit.

Scanning the sector addresses (A17, A16, A15, A14, A13, and A12) while (A6, A1, A0) = (0, 1, 0) will produce a logical "1" at device output DQ0 for a protected sector.

To terminate the operation, it is necessary to write the read/reset command sequence into the register.

Byte/Word Programming

The device is programmed on a byte-by-byte (or word-by-word) basis. Programming is a four bus cycle operation. There are two "unlock" write cycles. These are followed by the program set-up command and data write cycles. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever happens later and the data is latched on the rising edge of $\overline{CE}$ or $\overline{WE}$, whichever happens first. The rising edge of $\overline{CE}$ or $\overline{WE}$ (whichever happens first) begins programming. Upon executing the Embedded Program Algorithm command sequence the system is *not* required to provide further controls or timings. The device will automatically provide adequate internally generated program pulses and verify the programmed cell margin.

The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to the read mode and addresses are no longer latched. Therefore, the device requires that a valid address to the device be supplied by the system at this particular instance of time. Hence, $\overline{\text{Data}}$ Polling must be performed at the memory location which is being programmed.

Any commands written to the chip during this period will be ignored.

Programming is allowed in any sequence and across sector boundaries. Beware that a data "0" cannot be programmed back to a "1". Attempting to do so may either hang up the device or result in an apparent success according to the data polling algorithm but a read from reset/read mode will show that the data is still "0". Only erase operations can convert "0"s to "1"s.

Figure 1 illustrates the Embedded Programming Algorithm using typical command strings and bus operations.

Chip Erase

Chip erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the chip erase command.

Chip erase does *not* require the user to program the device prior to erase. Upon executing the Embedded Erase™ Algorithm command sequence the device automatically will program and verify the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to read the mode.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Sector Erase

Sector erase is a six bus cycle operation. There are two "unlock" write cycles. These are followed by writing the "set-up" command. Two more "unlock" write cycles are then followed by the sector erase command. The sector address (any address location within the desired sector) is latched on the falling edge of $\overline{WE}$, while the command (30H) is latched on the rising edge of $\overline{WE}$. A time-out of 80 µs from the rising edge of the last sector erase command will initiate the sector erase command(s).

Multiple sectors may be erased concurrently by writing the six bus cycle operations as described above. This sequence is followed with writes of the Sector Erase command to addresses in other sectors desired to be concurrently erased. The time between writes must be less than 80 µs otherwise that command will not be accepted and erasure will start. It is recommended that processor interrupts be disabled during this time to guarantee this condition. The interrupts can be re-enabled after the last Sector Erase command is written. A time-out of 80 µs from the rising edge of the last $\overline{WE}$ will initiate the execution of the Sector Erase command(s). If another falling edge of the $\overline{WE}$ occurs within the 80 µs time-out window the timer is reset. (Monitor DQ3 to determine if the sector erase timer window is still open, see section DQ3, Sector Erase Timer.) Any command other than Sector Erase or Erase Suspend during this period will reset the device to the read mode, ignoring the previous command string. Resetting the device once execution has begun will corrupt the data in that sector. In that case, restart the erase on those sectors and allow them to complete. (Refer to the Write Operation Status section for Sector Erase Timer operation.) Loading the sector erase buffer may be done in any sequence and with any number of sectors (0 to10).

Sector erase does *not* require the user to program the device prior to erase. The device automatically programs all memory locations in the sector(s) to be erased prior to electrical erase. When erasing a sector or sectors the remaining unselected sectors are not affected. The system is *not* required to provide any controls or timings during these operations.

The automatic sector erase begins after the 80 µs time out from the rising edge of the $\overline{\text{WE}}$ pulse for the last sector erase command pulse and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to the read mode. $\overline{\text{Data}}$ Polling must be performed at an address within any of the sectors being erased.

Figure 2 illustrates the Embedded Erase Algorithm using typical command strings and bus operations.

Erase Suspend

Erase Suspend command allows the user to interrupt the chip and then perform data reads (not program) from a non-busy sector during a Sector Erase operation (which may take up to several seconds). This command is applicable ONLY during the Sector Erase operation and will be ignored if written during the Chip Erase or Programming operation. The Erase Suspend command (B0H) which is allowed only during the Sector Erase Operation includes the sector erase time-out period after the Sector Erase commands (30H). Writing this command during the time-out will result in immediate termination of the time-out period. Any subsequent writes of the Sector Erase command will be taken as the Erase Resume command. Note that any other commands during the time out will reset the device to read mode. The addresses are don't-cares when writing the Erase Suspend or Erase Resume commands.

When the Erase Suspend command is written during a Sector Erase operation, the chip will take between 0.1 µs to 15 µs to suspend the erase operation and go into erase suspended read mode (pseudo-read mode), during which the user can read from a sector that is NOT being erased. A read from a sector being erased may result in invalid data. The user must monitor the toggle bit (DQ6) to determine if the chip has entered the pseudo-read mode, at which time the toggle bit stops toggling. An address of a sector NOT being erased must be used to read the toggle bit, otherwise the user may encounter intermittent problems. Note that the user must keep track of what state the chip is in since there is no external indication of whether the chip is in pseudo-read mode or actual read mode. After the user writes the Erase Suspend command, the user must wait until the toggle bit stops toggling before data reads from the device can be performed. Any further writes of the Erase Suspend command at this time will be ignored.

Every time an Erase Suspend command followed by an Erase Resume command is written, the internal (pulse) counters are reset. These counters are used to count the number of high voltage pulses the memory cell requires to program or erase. If the count exceeds a certain limit, then the DQ5 bit will be set (Exceeded Time Limit flag). This resetting of the counters is necessary since the Erase Suspend command can potentially interrupt or disrupt the high voltage pulses.

To resume the operation of Sector Erase, the Resume command (30H) should be written. Any further writes of the Resume command at this point will be ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Write Operation Status

Table 8. Hardware Sequence Flags

	Status	DQ7	DQ6	DQ5	DQ3	DQ2–DQ0
In Progress	Auto-Programming	$\overline{DQ7}$	Toggle	0	0	($\overline{D}$) (Note 1)
	Program/Erase in Auto Erase	0	Toggle	0	1	
Exceeded Time Limits	Auto-Programming	$\overline{DQ7}$	Toggle	1	1	($\overline{D}$) (Note 1)
	Program/Erase in Auto-Erase	0	Toggle	1	1	

Notes:

1. *DQ0, DQ1, DQ2 are reserve pins for future use.*
2. *DQ8 – DQ15 = Don't Care for X16 mode.*
3. *DQ4 for AMD internal use only.*

DQ7
$\overline{\text{Data}}$ Polling

The Am29F400 device features $\overline{\text{Data}}$ Polling as a method to indicate to the host that the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read the device will produce the complement of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7. During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ7 output. Upon completion of the Embedded Erase Algorithm an attempt to read the device will produce a "1" at the DQ7 output. The flowchart for $\overline{\text{Data}}$Polling (DQ7) is shown in Figure 3.

For chip erase, the $\overline{\text{Data}}$ Polling is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For sector erase, the $\overline{\text{Data}}$ Polling is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. Data Polling must be performed at sector address within any of the sectors being erased and **not** a protected sector. Otherwise, the status may not be valid. Once the Embedded Algorithm operation is close to being completed, the Am29F400 data pins (DQ7) may change asynchronously while the output enable ($\overline{\text{OE}}$) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and then that byte's valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the Embedded Algorithm operation and DQ7 has a valid data, the data outputs on DQ0–DQ6 may be still invalid. The valid data on DQ0–DQ7 will be read on the successive read attempts.

The $\overline{\text{Data}}$ Polling feature is only active during the Embedded Programming Algorithm, Embedded Erase Algorithm, or sector erase time-out (see Table 8).

See Figure 11 for the $\overline{\text{Data}}$ Polling timing specifications and diagrams.

DQ6
Toggle Bit

The Am29F400 also features the "Toggle Bit" as a method to indicate to the host system that the Embedded Algorithms are in progress or completed.

During an Embedded Program or Erase Algorithm cycle, successive attempts to read ($\overline{\text{OE}}$ toggling) data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Algorithm cycle is completed, DQ6 will stop toggling and valid data will be read on *the next* successive attempts. During programming, the Toggle Bit is valid after the rising edge of the fourth $\overline{\text{WE}}$ pulse in the four write pulse sequence. For chip erase, the Toggle Bit is valid after the rising edge of the sixth $\overline{\text{WE}}$ pulse in the six write pulse sequence. For Sector erase, the Toggle Bit is valid after the last rising edge of the sector erase $\overline{\text{WE}}$ pulse. The Toggle Bit is active during the sector time out.

In programming, if the sector being written to is protected, the toggle bit will toggle for about 2 µs and then stop toggling without the data having changed. In erase, the device will erase all the selected sectors except for the ones that are protected. If all selected sectors are protected, the chip will toggle the toggle bit for about 100 µs and then drop back into read mode, having changed none of the data.

Either $\overline{\text{CE}}$ or $\overline{\text{OE}}$ toggling will cause the DQ6 to toggle. In addition, an Erase Suspend/Resume command will cause DQ6 to toggle.

See Figure 12 for the Toggle Bit timing specifications and diagrams.

DQ5
Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits (internal pulse count). Under these conditions DQ5 will produce a "1". This is a failure condition which indicates that the program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the device under this condition. The $\overline{\text{CE}}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in Table 2.

If this failure condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused. However, other sectors are still functional and may be used for the program or erase operation. The device must be reset to use other sectors. Write the Reset command sequence to the device, and then execute program or erase command sequence. This allows the system to continue to use the other active sectors in the device.

If this failure condition occurs during the chip erase operation, it specifies that the entire chip is bad or combination of sectors are bad.

If this failure condition occurs during the byte programming operation, it specifies that the entire sector containing that byte is bad and this sector may not be reused, (other sectors are still functional and can be reused).

The DQ5 failure condition may also appear if a user tries to program a non blank location without erasing. In this case the device locks out and never completes the Embedded Algorithm operation. Hence, the system never reads a valid data on DQ7 bit and DQ6 never stops toggling. Once the device has exceeded timing limits, the DQ5 bit will indicate a "1." Please note that this is not a device failure condition since the device was incorrectly used.

DQ3
Sector Erase Timer

After the completion of the initial sector erase command sequence the sector erase time-out will begin. DQ3 will remain low until the time-out is complete. $\overline{\text{Data}}$ Polling and Toggle Bit are valid after the initial sector erase command sequence.

If $\overline{\text{Data}}$ Polling or the Toggle Bit indicates the device has been written with a valid erase command, DQ3 may be used to determine if the sector erase timer window is still open. If DQ3 is high ("1") the internally controlled erase cycle has begun; attempts to write subsequent commands to the device will be ignored until the erase operation is completed as indicated by $\overline{\text{Data}}$ Polling or Toggle Bit. If DQ3 is low ("0"), the device will accept additional sector erase commands. To insure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 were high on the second status check, the command may not have been accepted.

Refer to Table 8: Hardware Sequence Flags.

RY/$\overline{\text{BY}}$
Ready/Busy

The Am29F400 provides a RY/$\overline{\text{BY}}$ output pin as a way to indicate to the host system that the Embedded™ Algorithms are either in progress or completed. If the output is low, the device is busy with either a program or erase operation. If the output is high, the device is ready to accept any read/write or erase operation. When the RY/$\overline{\text{BY}}$ pin is low, the device will not accept any additional program or erase commands. If the Am29F400 is placed in an Erase Suspend mode, the RY/$\overline{\text{BY}}$ output will be high. Also, since this is an open drain output, many RY/$\overline{\text{BY}}$ pins can be tied together in parallel with a pull up resistor to V_{CC}.

During programming, the RY/$\overline{\text{BY}}$ pin is driven low after the rising edge of the fourth $\overline{\text{WE}}$ pulse. During an erase operation, the RY/$\overline{\text{BY}}$ pin is driven low after the rising edge of the sixth $\overline{\text{WE}}$ pulse. The RY/$\overline{\text{BY}}$ pin should be ignored while RESET is at V_{IL}. Refer to Figure 13 for a detailed timing diagram.

$\overline{\text{RESET}}$
Hardware Reset

The Am29F400 device may be reset by driving the $\overline{\text{RESET}}$ pin to V_{IL}. The $\overline{\text{RESET}}$ pin has a pulse requirement and has to be kept low (V_{IL}) for at least 500 ns in order to properly reset the internal state machine. Any operation in the process of being executed will be terminated and the internal state machine will be reset 20 µs after the $\overline{\text{RESET}}$ pin is driven low. Furthermore, once the $\overline{\text{RESET}}$ pin goes high, the device requires an additional 50 ns before it will allow read access. When the $\overline{\text{RESET}}$ pin is low, the device will be in the standby mode for the duration of the pulse and all the data output pins will be tri-stated. If a hardware reset occurs during a program or erase operation, the data at that particular location will be corrupted. Please note that the RY/$\overline{\text{BY}}$ output signal should be ignored during the $\overline{\text{RESET}}$ pulse. Refer to Figure 14 for the timing diagram. Refer to Temporary Sector Unprotect for additional functionality.

Byte/Word Configuration

The $\overline{\text{BYTE}}$ pin selects the byte (8-bit) mode or word (16 bit) mode for the Am29F400 device. When this pin is driven high, the device operates in the word (16 bit) mode. The data is read and programmed at DQ0–DQ15. When this pin is driven low, the device operates in byte (8 bit) mode. Under this mode, the DQ15/A-1 pin becomes the lowest address bit and DQ8–DQ14 bits are tristated. However, the command bus cycle is always an 8-bit operation and hence commands are written at DQ0–DQ7 and the DQ8–DQ15 bits are ignored. Refer to Figures 15 and 16 for the timing diagram.

Data Protection

The Am29F400 is designed to offer protection against accidental erasure or programming caused by spurious system level signals that may exist during power transitions. During power up the device automatically resets the internal state machine in the Read mode. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific multi-bus cycle command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. Under this condition the device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 5 ns (typical) on $\overline{\text{OE}}$, $\overline{\text{CE}}$ or $\overline{\text{WE}}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{\text{OE}} = V_{IL}$, $\overline{\text{CE}} = V_{IH}$ or $\overline{\text{WE}} = V_{IH}$. To initiate a write cycle $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be a logical zero while $\overline{\text{OE}}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{\text{WE}} = \overline{\text{CE}} = V_{IL}$ and $\overline{\text{OE}} = V_{IH}$ will not accept commands on the rising edge of $\overline{\text{WE}}$. The internal state machine is automatically reset to the read mode on power-up.

EMBEDDED ALGORITHMS

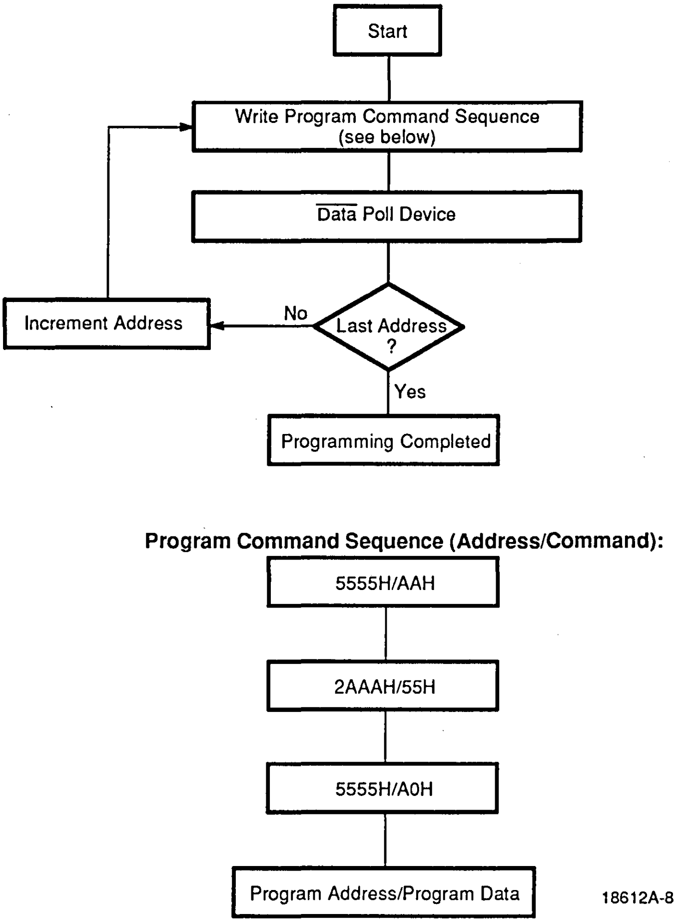


Figure 1. Embedded Programming Algorithm

Table 9. Embedded Programming Algorithm

Bus Operations	Command Sequence	Comments
Standby (Note 1)		
Write	Program	Valid Address/Data Sequence
Read		$\overline{\text{Data}}$ Polling to Verify Programming
Standby (Note 1)		Compare Data Output to Data Expected

Note:

1. Device is either powered-down, erase inhibit or program inhibit.

EMBEDDED ALGORITHMS

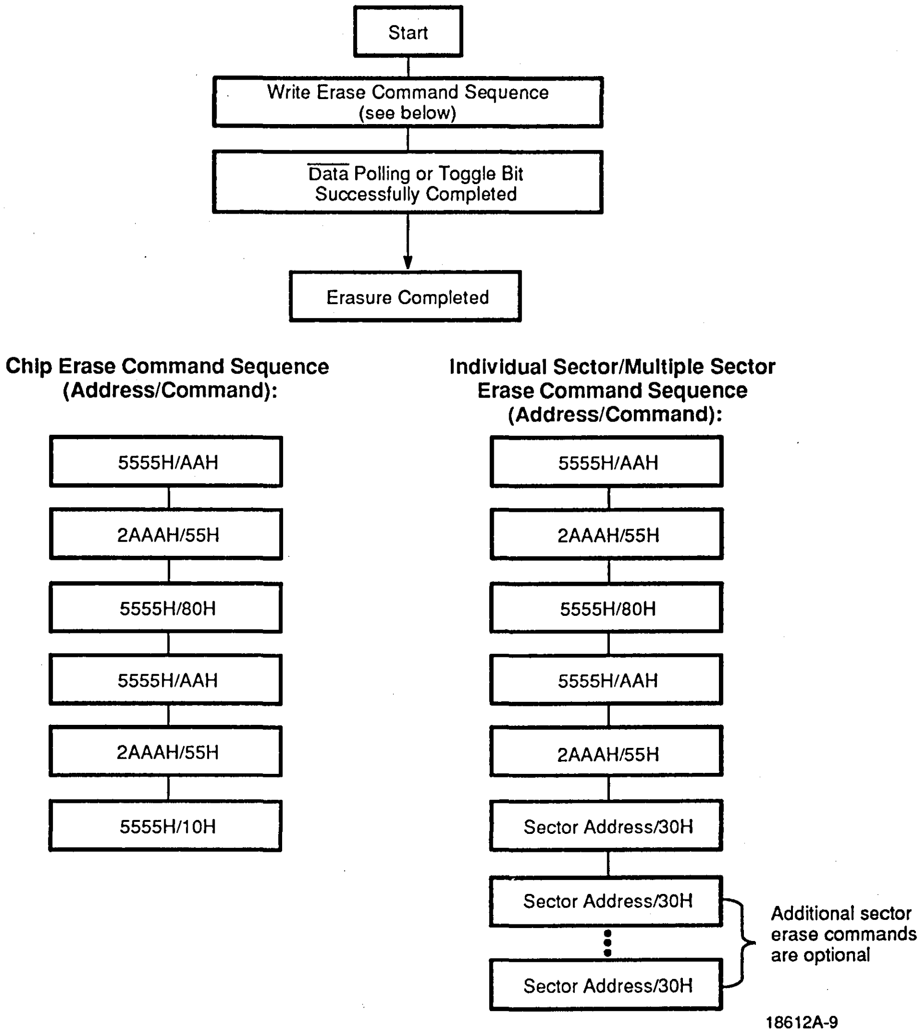
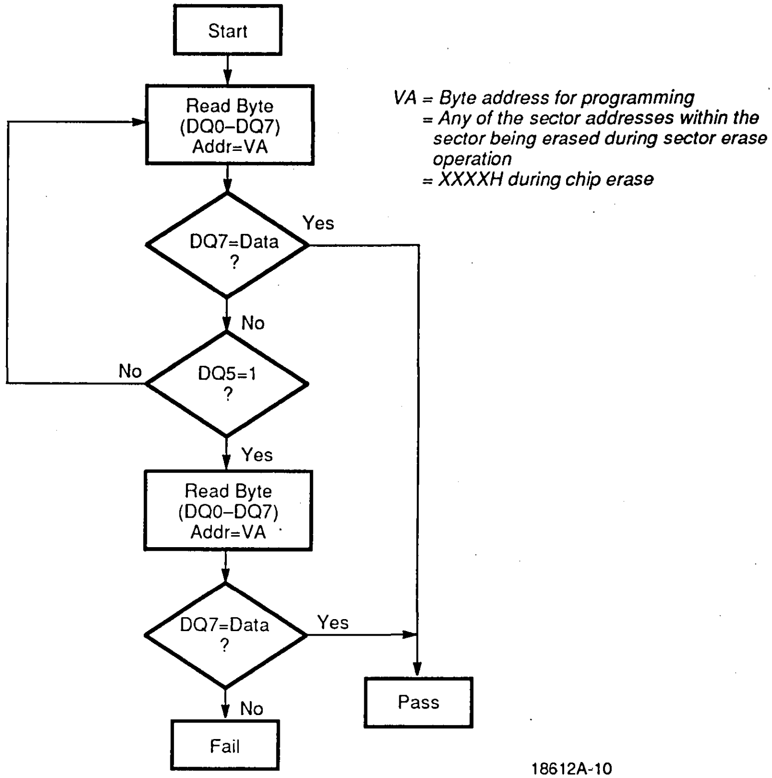


Figure 2. Embedded Erase Algorithm

Table 10. Embedded Erase Algorithm

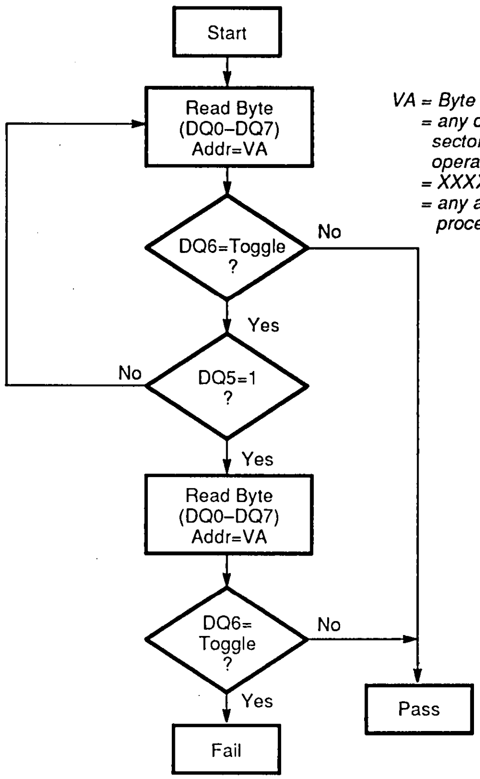
Bus Operations	Command Sequence	Comments
Standby (Note 1)		
Write	Erase	
Read		$\overline{\text{Data}}$ Polling to Verify Erasure
Standby (Note 1)		Compare Output to FFH

Note:
1. Device is either powered-down, erase inhibit or program inhibit.



Note:
1. DQ7 is rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.

Figure 3. $\overline{\text{Data}}$ Polling Algorithm



VA = Byte address for programming
= any of the sector addresses within the sector being erased during sector erase operation
= XXXXH during chip erase
= any address not within the sector in the process of an Erase Suspend operation.

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Note:

1. DQ6 is rechecked even if DQ5 = "1" because DQ6 may stop toggling at the same time as DQ5 changing to "1".

Figure 4. Toggle Bit Algorithm

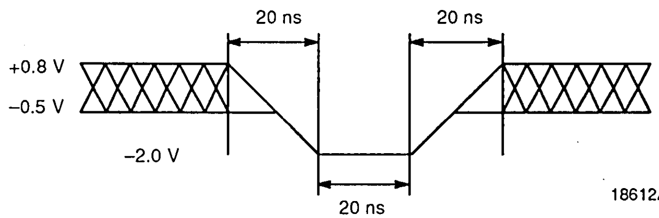

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Figure 5. Maximum Negative Overshoot Waveform

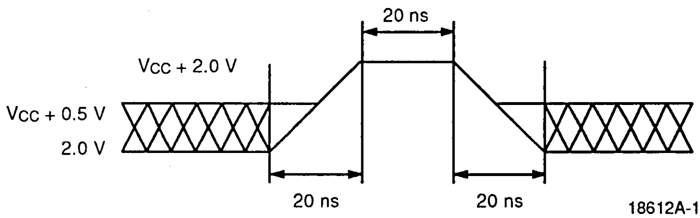

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Figure 6. Maximum Positive Overshoot Waveform

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages . . . . –65°C to +150°C
Plastic Packages . . . . –65°C to +125°C

Ambient Temperature
with Power Applied . . . . –55°C to +125°C

Voltage with Respect to Ground
All pins except A9 (Note 1) . . . . –2.0 V to +7.0 V

Vcc (Note 1) . . . . –2.0 V to +7.0 V

A9 (Note 2) . . . . –2.0 V to +14.0 V

Output Short Circuit Current (Note 3) . . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A9 pin is –0.5 V. During voltage transitions, A9 may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (Tc) . . . . 0°C to +70°C

Industrial (I) Devices
Case Temperature (Tc) . . . . –40°C to +85°C

Extended (E) Devices
Case Temperature (Tc) . . . . –55°C to +125°C

Military (M) Devices
Case Temperature (Tc) . . . . –55°C to +125°C

Vcc Supply Voltages
Vcc for Am29F400T/B-75 . . . . +4.75 V to +5.25 V

Vcc for Am29F400T/B-90, 120 . . . +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS
TTL/NMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.5 V			50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$	Byte		40	mA
			Word		50	
I_{CC2}	V_{CC} Active Current (Notes 2, 3)	$\overline{CE} = V_{IL}, \overline{OE} = V_{IH}$			60	mA
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IH}, \overline{OE} = V_{IH}$			1.0	mA
V_{IL}	Input Low Level			−0.5	0.8	V
V_{IH}	Input High Level			2.0	V_{CC} + 0.5	V
V_{ID}	Voltage for Autoselect and Sector Protect	V_{CC} = 5.0 V		11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA, $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH}	Output High Level	I_{OH} = −2.5 mA $V_{CC} = V_{CC}$ Min		2.4		V
V_{LKO}	Low V_{CC} Lock-Out Voltage			3.2	4.2	V

Notes:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *I_{CC} active while Embedded Algorithm (program or erase) is in progress.*
3. *Not 100% tested.*

DC CHARACTERISTICS (continued)
CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{LIT}	A9 Input Load Current	$V_{CC} = V_{CC}$ Max, A9 = 12.5 V			50	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC}$ Max			±1.0	µA
I_{CC1}	V_{CC} Active Current (Note 1)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	Byte		40	mA
			Word		50	
I_{CC2}	V_{CC} Active Current (Notes 2, 3)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		60	mA	
I_{CC3}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{CC} \pm 0.5$ V, $\overline{OE} = V_{IH}$			100	µA
V_{IL}	Input Low Level			–0.5	0.8	V
V_{IH}	Input High Level			0.7x V_{CC}	V_{CC} +0.3	V
V_{ID}	Voltage for Autoselect and Sector Protect	V_{CC} = 5.0 V		11.5	12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA, $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, $V_{CC} = V_{CC}$ Min		0.85 V_{CC}		V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC}$ Min		V_{CC} –0.4		V
V_{LKO}	Low V_{CC} Lock-out Voltage			3.2	4.2	V

Notes:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 6 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *I_{CC} active while Embedded Algorithm (program or erase) is in progress.*
3. *Not 100% tested.*

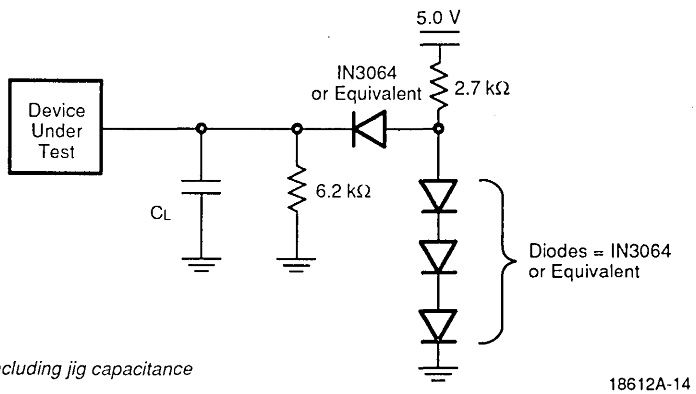
AC CHARACTERISTICS

Read Only Operations Characteristics

Parameter Symbols JEDEC	Parameter Symbols Standard	Description	Test Setup		-75 (Note 1)	-90 (Note 2)	-120 (Note 2)	-150 (Note 2)	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)		Min	70	90	120	150	ns
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = V_{IL}$ $\overline{OE} = V_{IL}$	Max	70	90	120	150	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Max	70	90	120	150	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay		Max	30	35	50	55	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 3, 4)		Max	20	20	30	35	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 3, 4)		Max	20	20	30	35	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurs First		Min	0	0	0	0	ns
	t_{Ready}	$\overline{RESET}$ pin low to read mode		Max	20	20	20	20	µs
	t_{ELFL} t_{ELFH}	$\overline{CE}$ to $\overline{BYTE}$ switching low or high		Max	5	5	5	5	ns

Notes:

1. *Test Conditions:*
   Output Load: 1 TTL gate and 30 pF
   Input rise and fall times: 5 ns
   Input pulse levels: 0.0 V to 3.0 V
   Timing measurement reference level
   Input: 1.5 V
   Output: 1.5 V
2. *Test Conditions:*
   Output Load: 1 TTL gate and 100 pF
   Input rise and fall times: 20 ns
   Input pulse levels: 0.45 V to 2.4 V
   Timing measurement reference level
   Input: 0.8 and 2.0 V
   Output: 0.8 and 2.0 V
3. ***Output driver disable time.***
4. ***Not 100% tested.***



Notes:

For -70: C_L = 30 pF including jig capacitance

For all others: C_L = 100 pF including jig capacitance

Figure 7. Test Conditions

AC CHARACTERISTICS

Write/Erase/Program Operations

Parameter Symbols JEDEC	Standard	Description			-70	-90	-120	-150	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (3)		Min	70	90	120	150	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	45	50	50	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	30	45	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time (3)		Min	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time	Read (Note 3)	Min	0	0	0	0	ns
			Toggle and $\overline{Data}$ Polling (3)	Min	10	10	10	10	ns
t_{GHWL}	t_{GHWL}	Read Recover Time Before Write		Min	0	0	0	0	ns
t_{ELWL}	t_{CS}	$\overline{CE}$ Setup Time		Min	0	0	0	0	ns
t_{WHEH}	t_{CH}	$\overline{CE}$ Hold Time		Min	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35	45	50	50	ns
t_{WHWL}	t_{WPH}	Write Pulse Width High		Min	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ	16	16	16	16	µs
t_{WHWH2}	t_{WHWH2}	Erase Operation (1)		Typ	1.5	1.5	1.5	1.5	sec
				Max	30	30	30	30	sec
	t_{VCS}	V_{CC} Set Up Time (3)		Min	50	50	50	50	µs
	t_{VLHT}	Voltage Transition Time (2, 3, 5)		Min	4	4	4	4	µs
	t_{WPP}	Write Pulse Width (2)		Min	100	100	100	100	µs
	t_{WPP2}	Write Pulse Width (5)		Min	10	10	10	10	ms
	t_{OESP}	$\overline{OE}$ Setup Time to $\overline{WE}$ Active (2, 3, 5)		Min	4	4	4	4	µs
	t_{CSP}	$\overline{CE}$ Setup Time to $\overline{WE}$ Active (3)		Min	4	4	4	4	µs
	t_{RP}	$\overline{RESET}$ Pulse Width		Min	500	500	500	500	ns
	t_{FLQZ}	$\overline{BYTE}$ Switching Low to Output High Z (3, 4)		Max	20	30	30	30	ns
	t_{BUSY}	Program/Erase Valid to RD/$\overline{BY}$ Delay (3)		Min	30	35	50	55	ns

Notes:

1. *This does not include the preprogramming time.*
2. *These timings are for Sector Protect operation.*
3. *Not 100% tested.*
4. *Output Driver Disable Time.*
5. *These timings are for Sector Unprotect operation.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

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SWITCHING WAVEFORMS

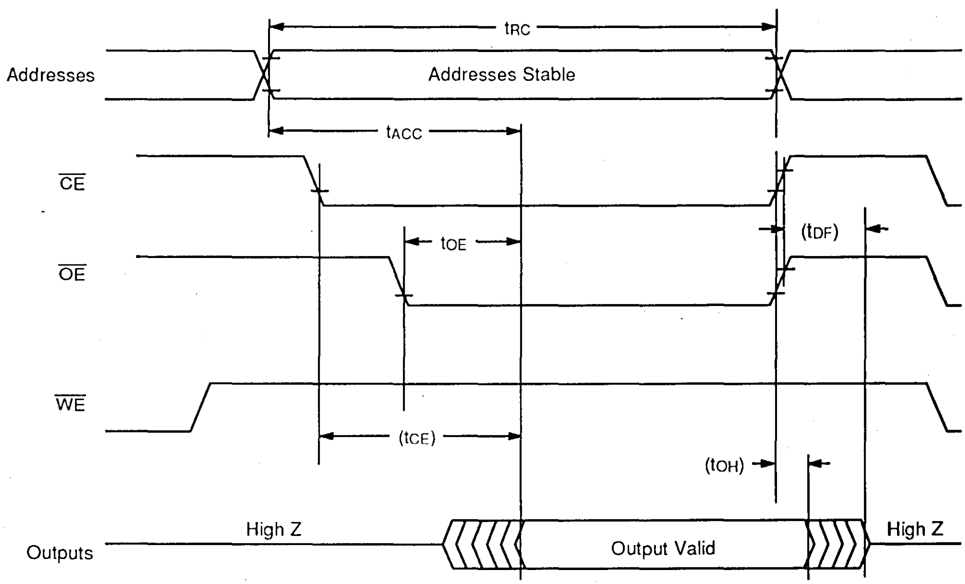

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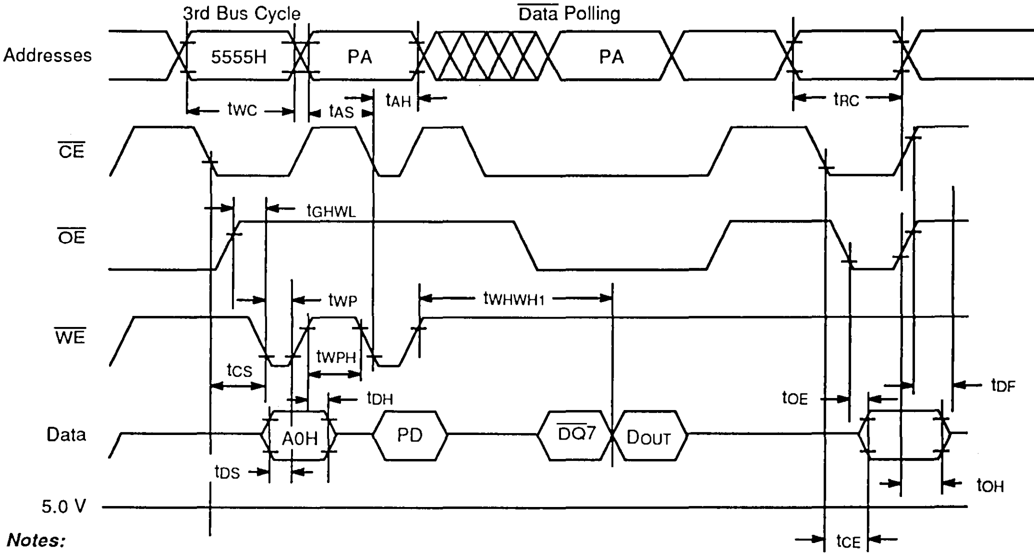
Figure 8. AC Waveforms for Read Operations

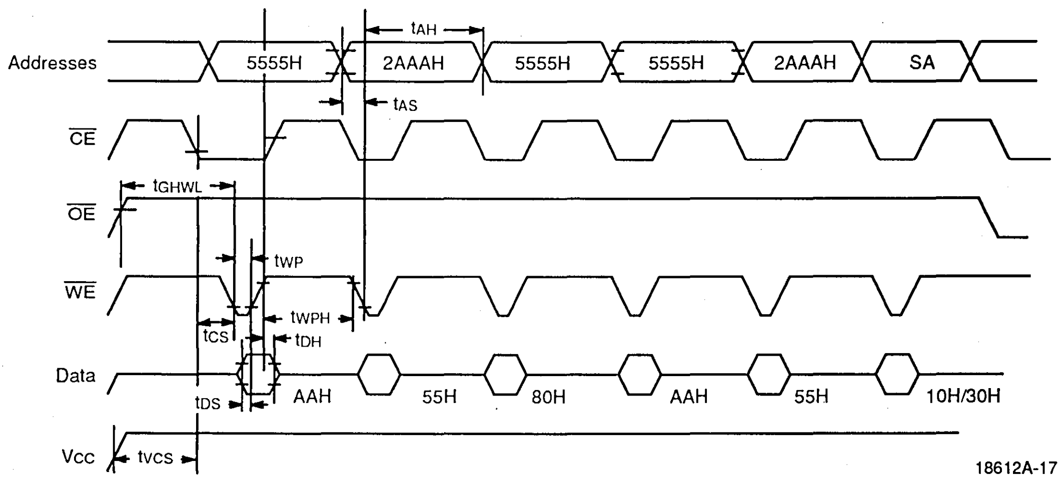
SWITCHING WAVEFORMS



Notes:

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
4. *DOUT is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*
6. *These waveforms are for the x16 mode.*

Figure 9. Program Operation Timings

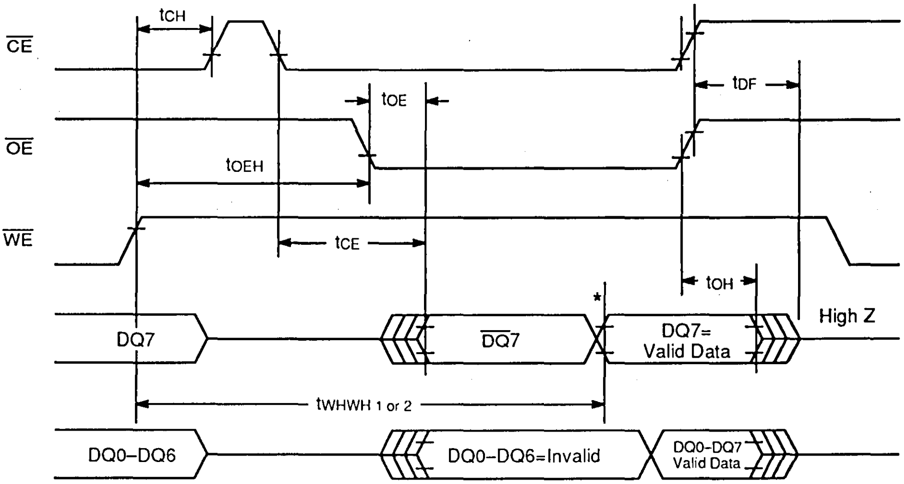


Notes:

1. *SA is the sector address for Sector Erase. Addresses = don't care for Chip Erase.*
2. *These waveforms are for the x16 mode.*

Figure 10. AC Waveforms Chip/Sector Erase Operations

SWITCHING WAVEFORMS



*DQ7=Valid Data (The device has completed the Embedded operation).

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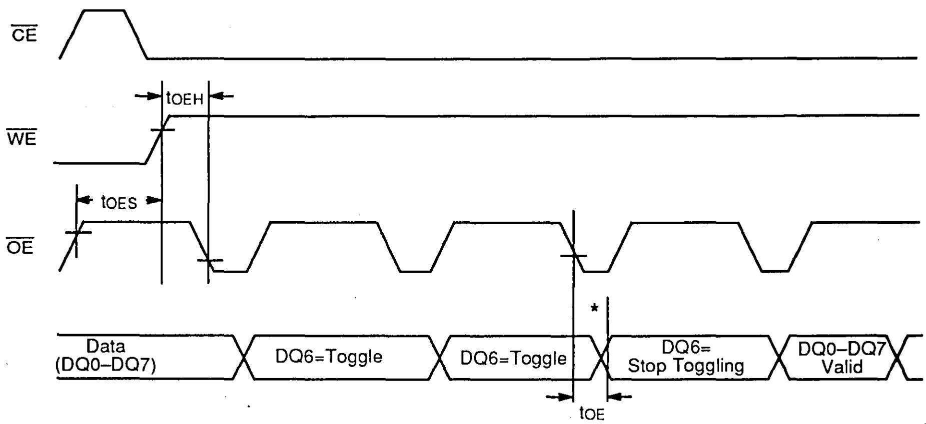
Figure 11. AC Waveforms for Data Polling During Embedded Algorithm Operations



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Note:

DQ6 stops toggling (The device has completed the Embedded operation).

Figure 12. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

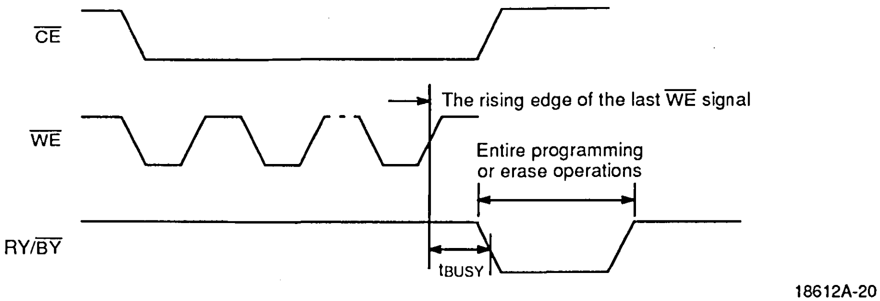


Figure 13. RY/BY Timing Diagram During Program/Erase Operations

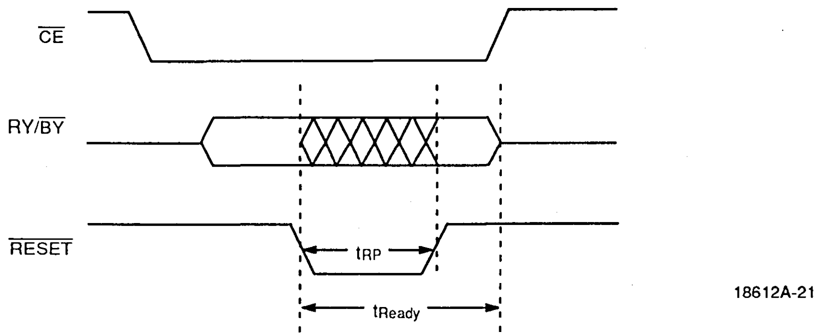


Figure 14. RESET/RY/BY Timing Diagram

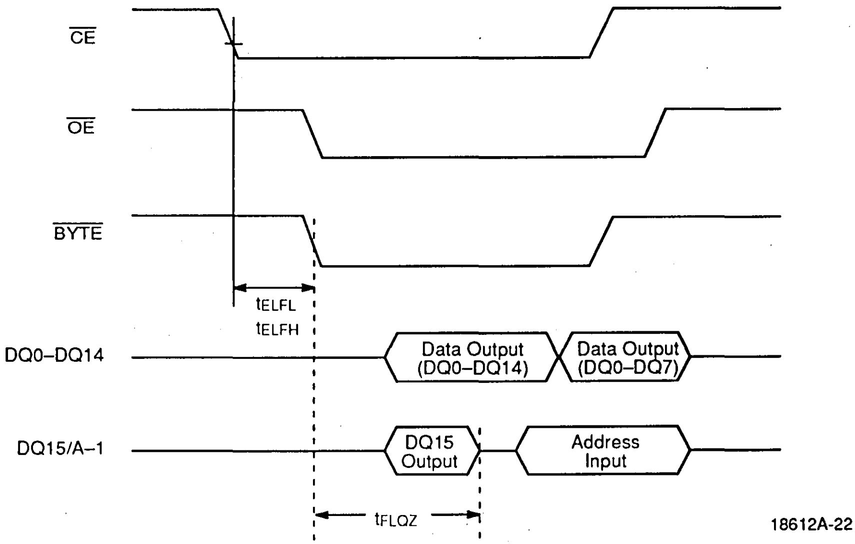


Figure 15. BYTE Timing Diagram for Read Operation

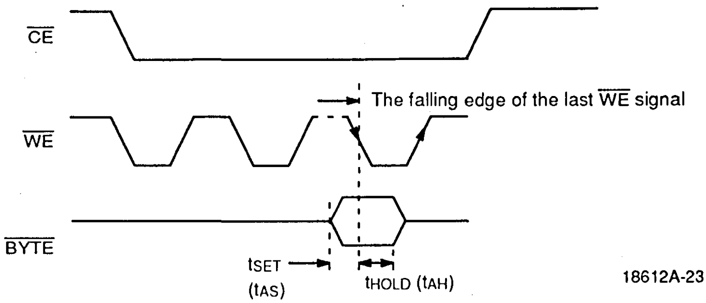


Figure 16. BYTE Timing Diagram for Write Operations

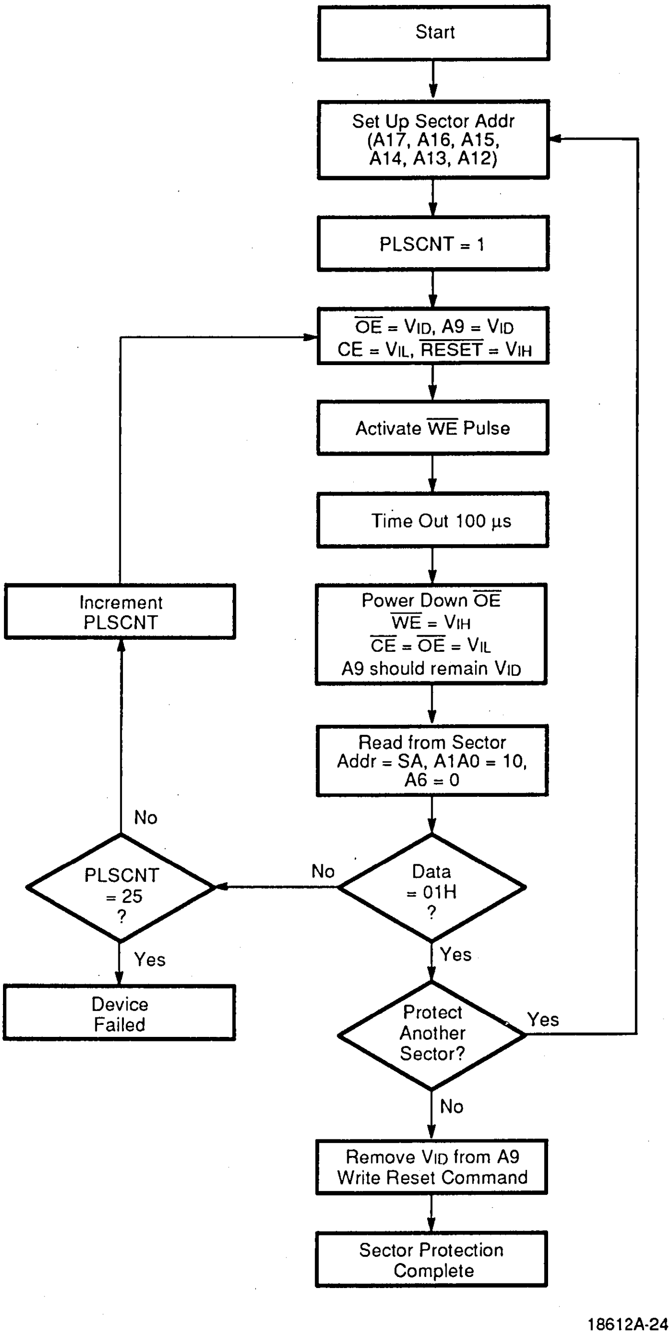
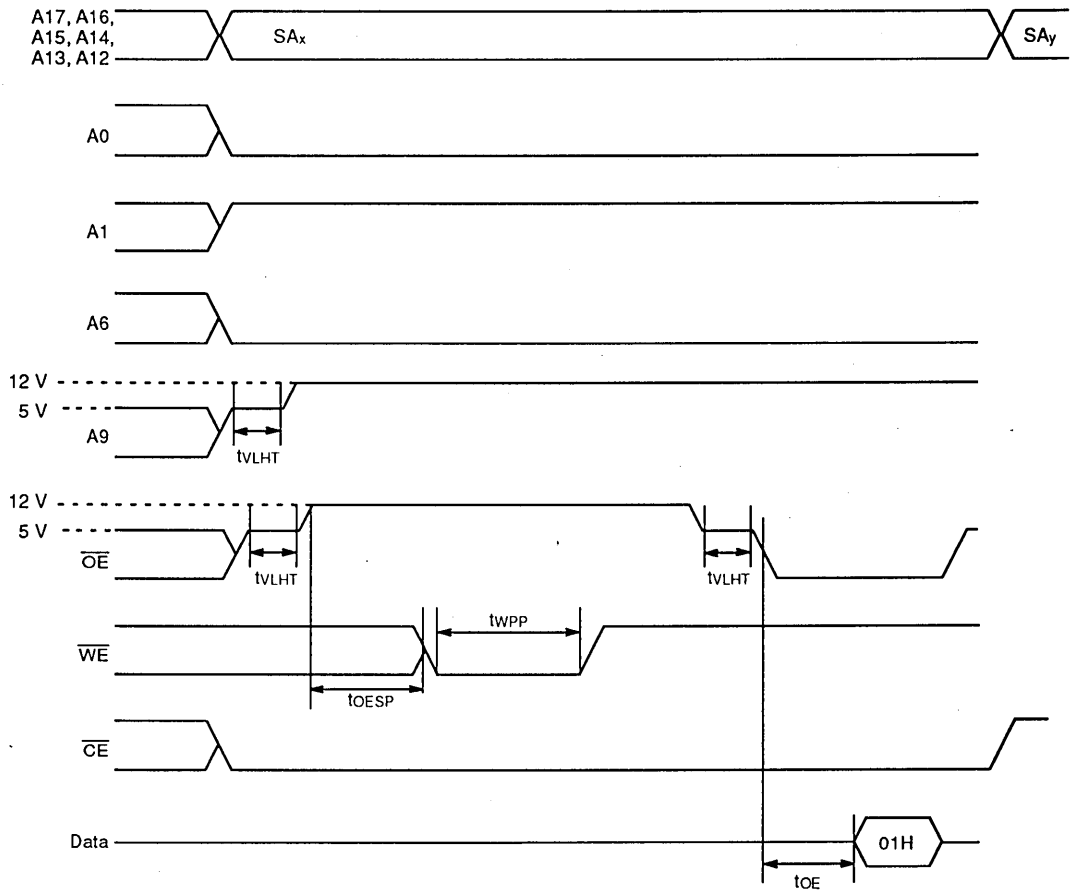


Figure 17. Sector Protection Algorithm

SWITCHING WAVEFORMS

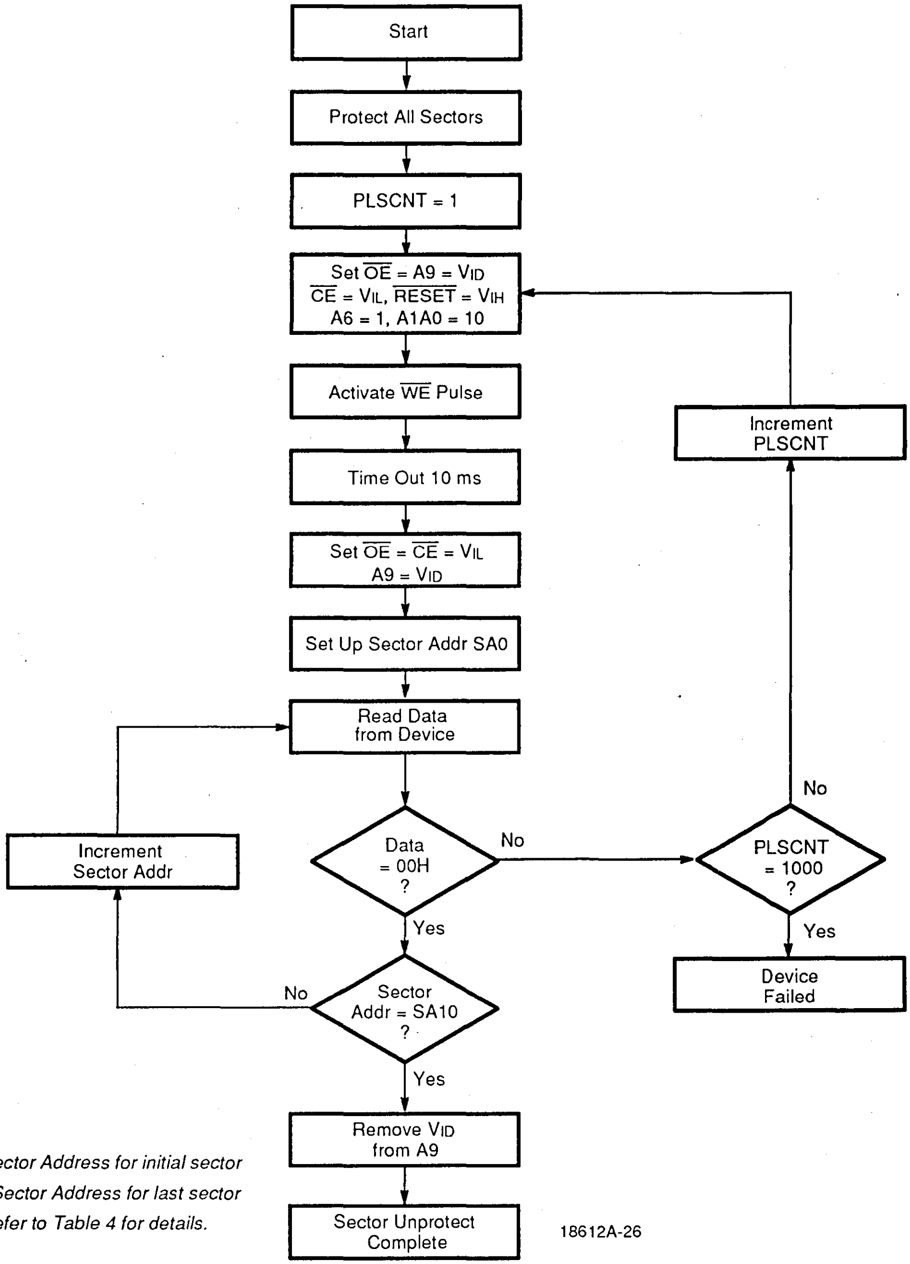


SA_x = Sector Address for initial sector

SA_y = Sector Address for next sector

18612A-25

Figure 18. AC Waveforms for Sector Protection



Notes:
SA0 = Sector Address for initial sector
SA10 = Sector Address for last sector
Please refer to Table 4 for details.

18612A-26

Figure 19. Sector Unprotect Algorithm

SWITCHING WAVEFORMS

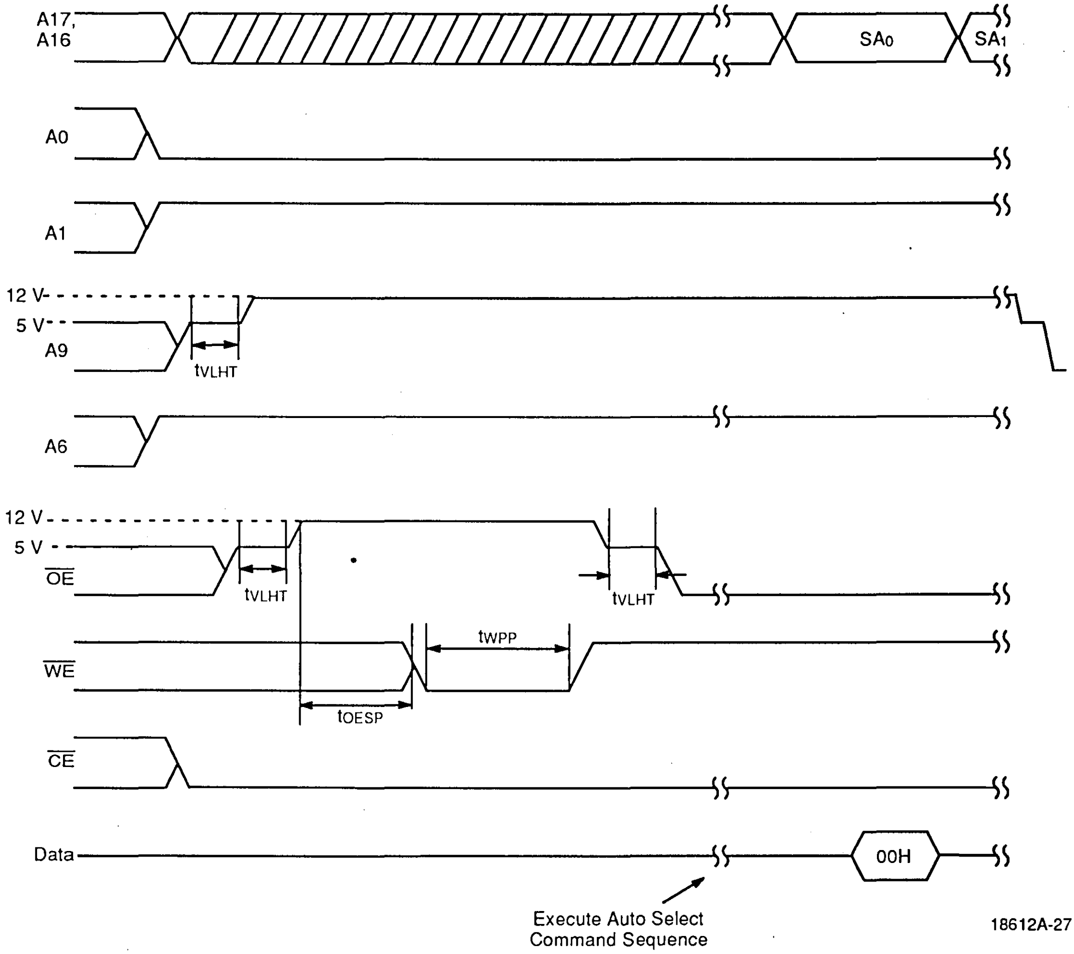


Figure 20. AC Waveforms for Sector Unprotect

AC CHARACTERISTICS

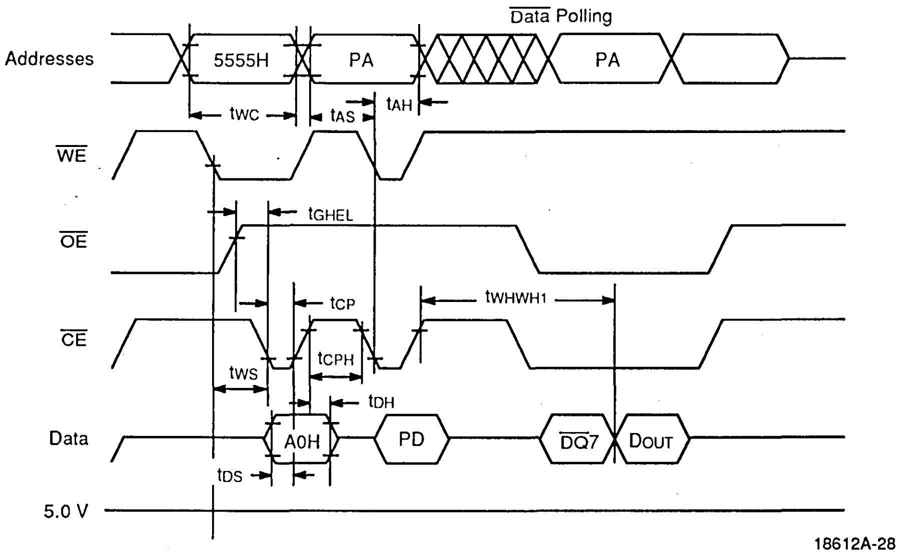
Write/Erase/Program Operations

Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols JEDEC	Standard	Description			-70	-90	-120	-150	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (4)		Min	70	90	120	150	ns
t_{AVEL}	t_{AS}	Address Setup Time		Min	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	45	50	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	30	45	50	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0	0	0	0	ns
	t_{OES}	Output Enable Setup Time		Min	0	0	0	0	ns
	t_{OEH}	Output Enable Hold Time (4)	Read (4)	Min	0	0	0	0	ns
			Toggle and $\overline{Data}$ Polling	Min	10	10	10	10	ns
t_{GHEL}	t_{GHEL}	Read Recover Time Before Write		Min	0	0	0	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time		Min	0	0	0	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		Min	0	0	0	0	ns
t_{ELEH}	t_{CP}	$\overline{CE}$ Pulse Width		Min	35	45	50	50	ns
t_{EHEL}	t_{CPH}	$\overline{CE}$ Pulse Width High		Min	20	20	20	20	ns
t_{WHWH1}	t_{WHWH1}	Byte Programming Operation		Typ	16	16	16	16	µs
t_{WHWH2}	t_{WHWH2}	Erase Operation (Note 1)		Typ	1.5	1.5	1.5	1.5	sec
				Max	30	30	30	30	sec
	t_{VCS}	V_{CC} Set Up Time (Note 4)		Typ	50	50	50	50	µs
	t_{RP}	$\overline{RESET}$ Pulse Width		Min	500	500	500	500	ns
	t_{FLQZ}	$\overline{BYTE}$ Switching Low to Output High Z (3, 4)		Max	20	30	30	30	ns
	t_{BUSY}	Program/Erase Valid to RD/$\overline{BY}$ Delay (4)		Min	30	35	50	55	ns

Notes:

1. *This does not include the preprogramming time.*
2. *These timings are for Sector Protect/Unprotect operations.*
3. *This timing is only for Sector Unprotect.*
4. *Not 100% tested.*



Notes:

1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
4. *DOUT is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*
6. *These waveforms are for the x16 mode.*

Figure 21. Alternate $\overline{CE}$ Controlled Program Operation Timings

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits Min	Limits Typ	Limits Max	Unit	Comments
Chip and Sector Erase Time		1.5 (Note 1)	30	sec	Excludes 00H programming prior to erasure
Byte Programming Time		16	1000 (Note 2)	µs	Excludes system-level overhead
Chip Programming Time		8.5 (Note 1)	50	sec	Excludes system-level overhead
Erase/Program Cycles	100,000	1,000,000		Cycles	

Notes:

1. *25°C, 5 V V_{CC}, 100,000 cycles*
2. *The Embedded Algorithms allow for 48 ms byte program time.*

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.

TSOP PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	6	7.5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8.5	12	pF
C_{IN2}	Control Pin Capacitance	$V_{IN} = 0$	8	10	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz*

SO PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	6	7.5	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8.5	12	pF
C_{IN2}	Control Pin Capacitance	$V_{PP} = 0$	8	10	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz*

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

ADVANCE INFORMATION

Am29F016

Advanced Micro Devices

16-Megabit (2,097,152 x 8-Bit) CMOS 5.0 Volt-only, Sector Erase Flash Memory

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% read, write, and erase**
  - Minimizes system level power requirements
- **Compatible with JEDEC-standard commands**
  - Pinout and software compatible with single-supply Flash
- **48-pin TSOP pinout**
- **Minimum 100,000 write/erase cycles**
- **High performance**
  - 90 ns maximum access time
- **Sector erase architecture**
  - Uniform sectors of 64 Kbytes each
  - Any combination of sectors can be erased. Also supports full chip erase
- **Embedded Erase Algorithms**
  - Automatically pre-programs and erases the chip or any sector
- **Embedded Program Algorithms**
  - Automatically writes and verifies data at specified address
- **$\overline{\text{Data}}$ Polling and Toggle Bit feature for detection of program or erase cycle completion**
- **Ready/$\overline{\text{BUSY}}$ output**
  - Hardware method for detection of program or erase cycle completion
- **Erase Suspend Resume**
  - This feature supports reading or programming data to a non-busy sector
- **Low power consumption**
  - 30 mA maximum active read current
  - 60 mA maximum write/erase current
  - 1 μA typical standby current
- **Low V_{CC} write inhibit ≤ 3.2 V**
- **Block protection**
  - Hardware method that disables any combination of blocks from write or erase operations
- **Hardware $\overline{\text{RESET}}$ pin**
  - Resets internal state machine to the read mode

GENERAL DESCRIPTION

The Am29F016 is a 16 Mbit, 5.0 V-only Flash memory organized as 2 Mbytes of 8 bits each. The 2 Mbytes of data is organized in 32 sectors of 64 Kbytes for flexible erase capability. The 8 bits of data will appear on DQ0–DQ7. The Am29F016 is offered in a 48-pin TSOP package. This device is designed to be programmed in-system with the standard system 5.0 V V_{CC} supply. 12.0 V V_{PP} is not required for write or erase operations. The device can also be reprogrammed in standard EPROM programmers.

The standard Am29F016 offers access times between 90 ns, 120 ns, and 150 ns allowing operation of high-speed microprocessors without wait states. To eliminate bus contention the device has separate chip enable ($\overline{\text{CE}}$), write enable ($\overline{\text{WE}}$), and output enable ($\overline{\text{OE}}$) controls.

The Am29F016 is entirely command set compatible with JEDEC standard single-supply Flash. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from 12.0 V Flash or EPROM devices.

The Am29F016 is programmed by executing the program command sequence. This will invoke the Embedded Program algorithm which is an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. Erase is accomplished by executing the erase command sequence. This will invoke the Embedded Erase algorithm which is an internal algorithm that automatically preprograms the array if it is not already programmed before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.
Publication# 18805 Rev. A Amendment/0
Issue Date: March 1994

GENERAL DESCRIPTION

This device also features a sector erase architecture. The sector mode allows for sectors of memory to be erased and reprogrammed without affecting other sectors. A sector is typically erased and verified within 1 second. The Am29F016 is erased when shipped from the factory.

The Am29F016 device also features hardware block protection. This feature will disable both program and erase operations in any combination of eight blocks of memory. A block consists of four adjacent sectors grouped in the following pattern: sectors 0–3, 4–7, 8–11, 12–15, 16–19, 20–23, 24–27, and 28–31.

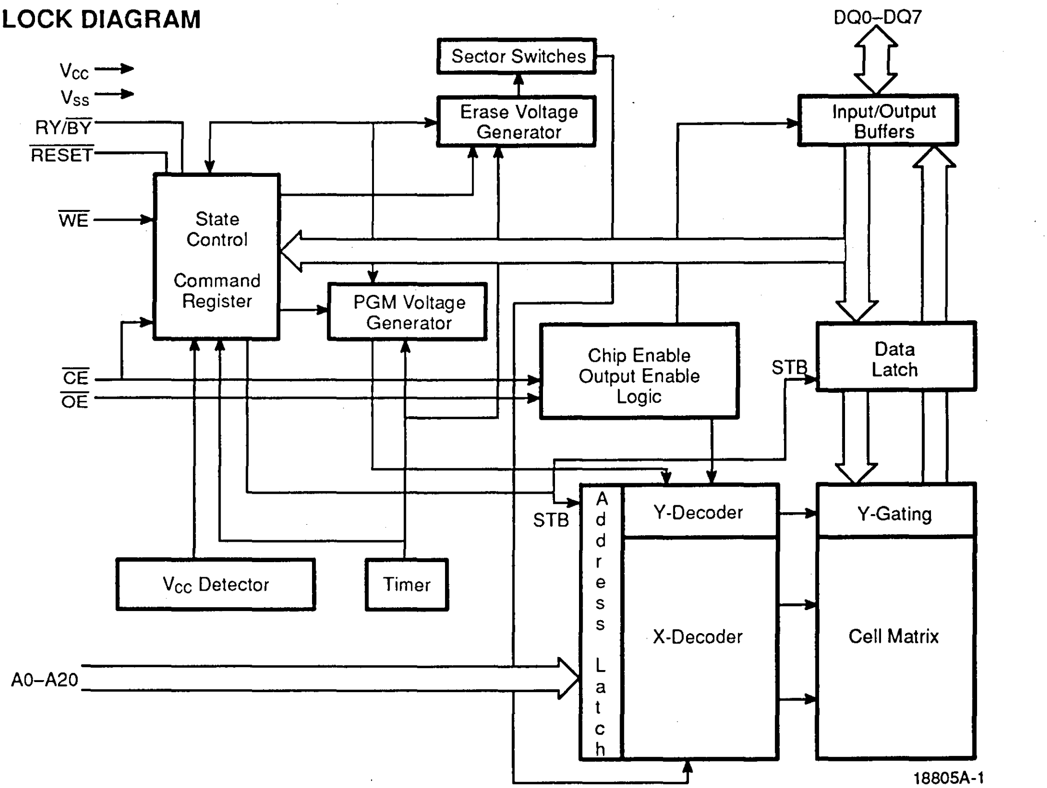
AMD has implemented an Erase Suspend feature that enables the user to put erase on hold for any period of time to read data or program data to a non-busy sector. Thus, true background erase can be achieved.

The device features single 5.0 V power supply operation for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations. A low V_{CC} detector automatically inhibits write operations on the loss of power. The end of program or erase is detected by the Ready/$\overline{\text{BUSY}}$ pin, $\overline{\text{Data}}$ Polling of DQ7 or by the Toggle Bit feature on DQ6. Once the end of a program or erase cycle has been completed, the device internally resets to the read mode.

The Am29F016 also has a hardware $\overline{\text{RESET}}$ pin. When this pin is driven low, execution of any Embedded Program or Embedded Erase operations will be terminated. The internal state machine will then be reset into the read mode. The $\overline{\text{RESET}}$ pin may be tied to the system reset input. Therefore, if a system reset occurs during the Embedded Program or Embedded Erase operation, the device will be automatically reset to a read mode. This will enable the system microprocessor to read the boot-up firmware from the Flash memory.

AMD's Flash technology combines years of EPROM and E²PROM experience to produce the highest levels of quality, reliability and cost effectiveness. The Am29F016 memory electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

BLOCK DIAGRAM



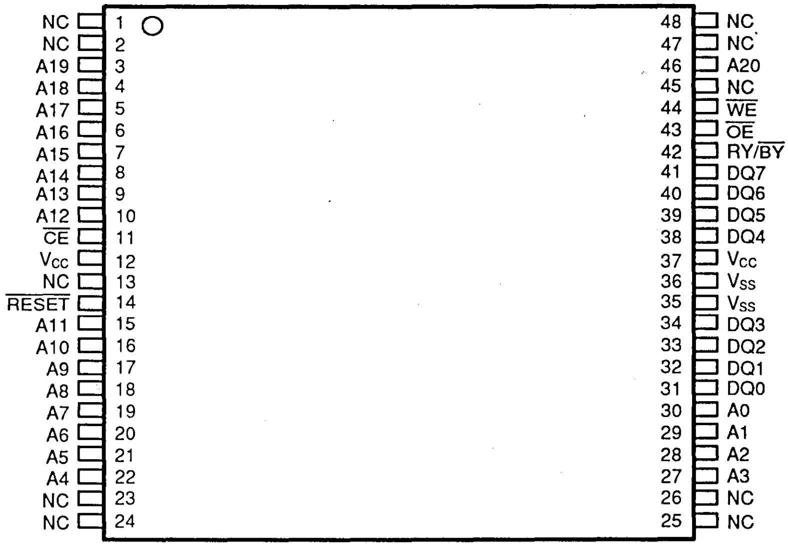
18805A-1

PRODUCT SELECTOR GUIDE

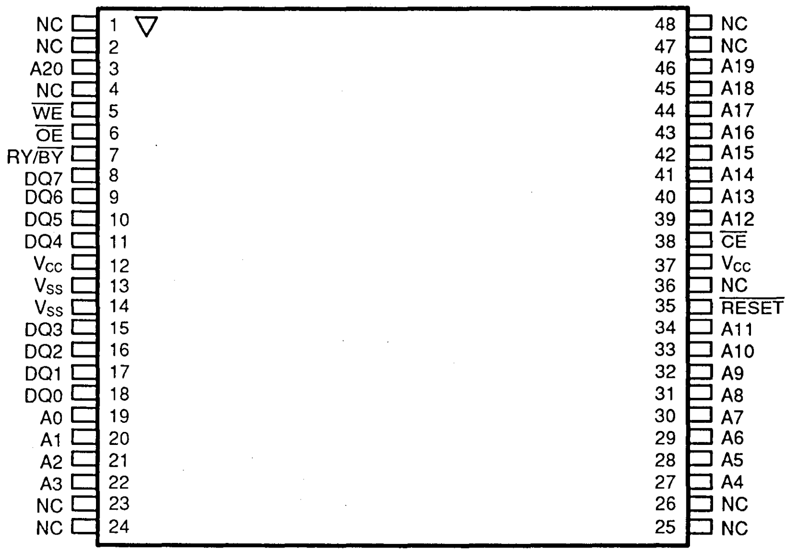
Family Part No.	Am29F016		
Ordering Part No: V_{CC} = 5.0 V ± 10%	-90	-120	-150
Max Access Time (ns)	90	120	150
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	120	150
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	50	75

CONNECTION DIAGRAMS

16 Mbit Pinout



Standard TSOP



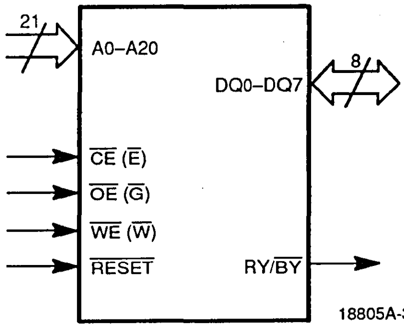
Reverse TSOP

18805A-2

PIN CONFIGURATION

A0–A20	=	21 Addresses
DQ0–DQ7	=	8 Data Inputs/Outputs
NC	=	Pin Not Connected
$\overline{CE}$	=	Chip Enable
$\overline{OE}$	=	Output Enable
$\overline{WE}$	=	Write Enable
$\overline{RESET}$	=	Hardware Reset Pin, Active Low
RY/$\overline{BY}$	=	Ready/$\overline{BUSY}$ Output
Vcc	=	+5 V Supply (±10% V)
Vss	=	Device Ground

LOGIC SYMBOL



18805A-3

SECTION

2 12.0 Volt, BULK ERASE FLASH MEMORIES

FINAL

Am28F256

Advanced Micro Devices

256 Kilobit (32,768 x 8-Bit) CMOS 12.0 Volt, Bulk Erase Flash Memory

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 70 ns maximum access time
- **CMOS Low power consumption**
  - 30 mA maximum active current
  - 100 µA maximum standby current
  - No data retention power consumption
- **Compatible with JEDEC-standard byte-wide 32-Pin EPROM pinouts**
  - 32-pin DIP
  - 32-pin PLCC
  - 32-pin TSOP
  - 32-pin LCC
- **10,000 write/erase cycles minimum**
- **Write and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to V_{CC} +1 V**
- **Flasherase Electrical Bulk Chip-Erase**
  - One second typical chip-erase
- **Flashrite Programming**
  - 10 µs typical byte-program
  - 0.5 second typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell
- **Automatic write/erase pulse stop timer**

GENERAL DESCRIPTION

The Am28F256 is a 256K Flash memory organized as 32K bytes of 8 bits each. AMD's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The Am28F256 is packaged in 32-pin PDIP, PLCC, and TSOP versions. The device is also offered in the ceramic LCC package. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers. The Am28F256 is erased when shipped from the factory.

The standard Am28F256 offers access times as fast as 70 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F256 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F256 uses a command register to manage this functionality, while maintaining a standard JEDEC Flash Standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming.

AMD's Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F256 uses a 12.0 V ± 5% V_{PP} supply to perform the Flasherase and Flashrite algorithms.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from –1 V to V_{CC}+1 V.

The Am28F256 is byte programmable using 10 µs programming pulses in accordance with AMD's Flashrite programming algorithm. The typical room temperature programming time of the Am28F256 is a half a second. The entire chip is bulk erased using 10 ms erase pulses according to AMD's Flasherase alrogithm. Typical erasure at room temperature is accomplished in less than one second. The windowed package and the 15–20 minutes required for EPROM erasure using ultra-violet light are eliminated.

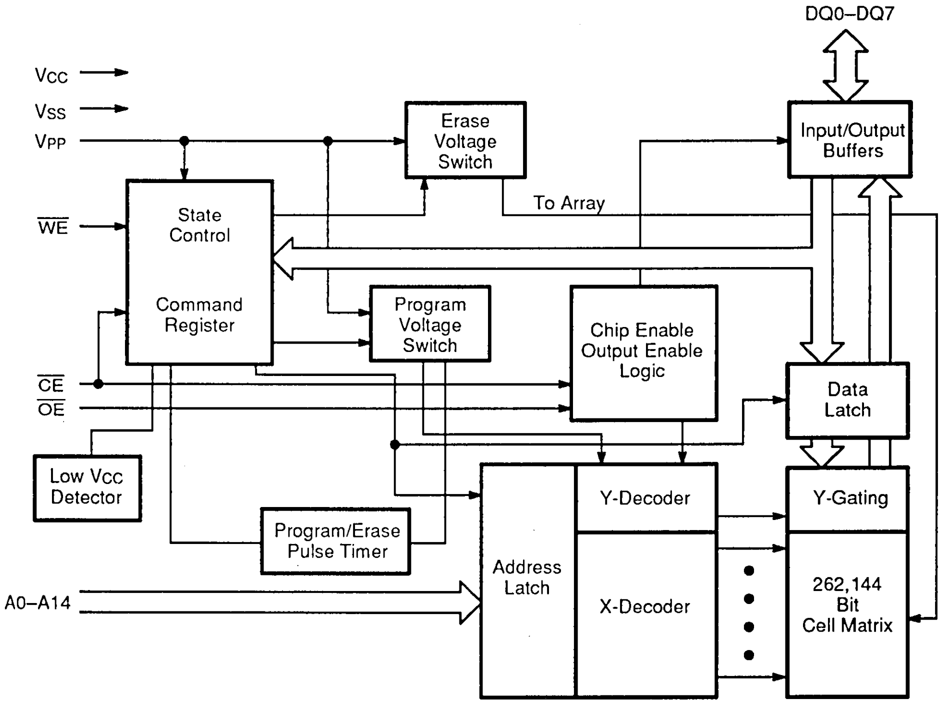
Publication# 11560 Rev. E Amendment/0
Issue Date: March 1994

GENERAL DESCRIPTION

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F256 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

AMD's Flash technology combines years of EPROM and EEPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F256 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

BLOCK DIAGRAM



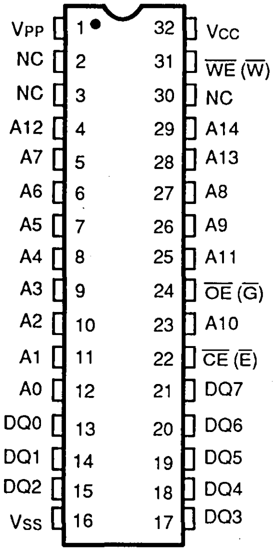
11560E-1

PRODUCT SELECTOR GUIDE

Family Part No.:	**Am28F256**					
Ordering Part No.: ±10% Vcc Tolerance	—	**-90**	**-120**	**-150**	**-200**	**-250**
±5% Vcc Tolerance	**-75**	**-95**	—	—	—	—
Max Access Time (ns)	70	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	70	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	35	50	55	55	55

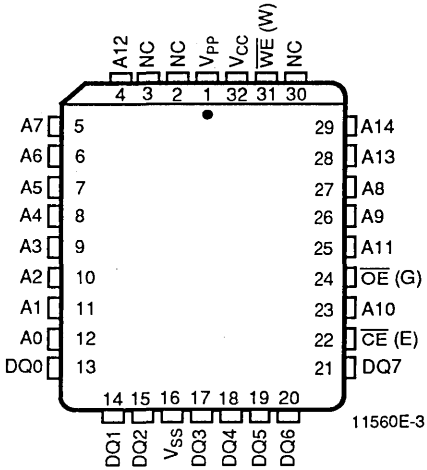
CONNECTION DIAGRAMS

DIP



11560E-2

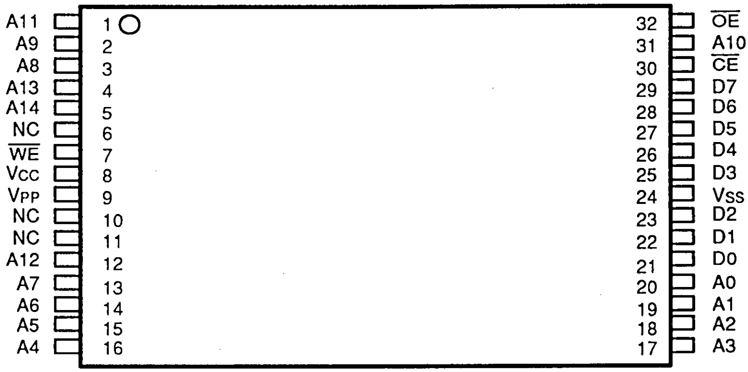
PLCC*



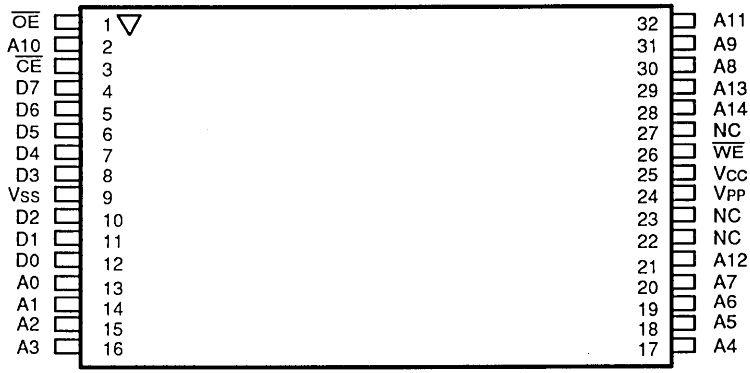
11560E-3

Note: *Pin 1 is marked for orientation.*
**Also available in LCC.*

TSOP PACKAGES



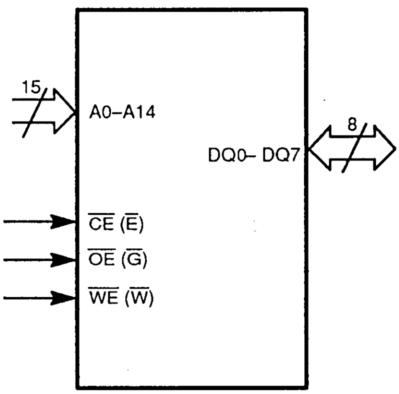
28F256 Standard Pinout



28F256 Reverse Pinout 11560E-4

28F256 32K x 8 Flash Memory in 32-Lead TSOP

LOGIC SYMBOL



11560E-5

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

AM28F256 -75 J C B

OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-In

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to + 85°C)
E = Extended (–55°C to + 125°C)

PACKAGE TYPE
P = 32-Pin Plastic DIP (PD 032)
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)
L = 32-Pin Rectangular Ceramic Leadless Chip Carrier (CLR 032)
E = 32-Pin TSOP Standard Pinout (TS 032)
F = 32-Pin TSOP Reverse Pinout (TSR 032)

SPEED
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am28F256
256 Kilobit (32K x 8-Bit) CMOS Flash Memory

Valid Combinations	
Am28F256-75 Am28F256-90 Am28F256-95	PC, JC, LC, EC, FC
Am28F256-120 Am28F256-150 Am28F256-200	PC, PI, PE, PEB, JC, JI, JE, JEB, LC, LI, LE, LEB, EC, FC, EI, FI, EE, FE, EEB, FEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTION

A0–A14
Address Inputs for memory locations. Internal latches hold addresses during write cycles.

$\overline{CE}$ (E)
The Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.

DQ0–DQ7
Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

NC
No Connect-corresponding pin is not connected internally to the die.

$\overline{OE}$ (G)
The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

V_{CC}
Power supply for device operation. (5.0 V ± 5% or 10%)

V_{PP}
Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2$ V.

V_{SS}
Ground

$\overline{WE}$ (W)
The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

BASIC PRINCIPLES

The Am28F256 uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0 V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F256 functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F256's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F256 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Flasherase Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note: *The Flash memory array must be completely programmed to 0's prior to erasure. Refer to the Flashrite Algorithm.*

1. **Erase Set-Up:** Write the Set-up Erase command to the command register.
2. **Erase:** Write the Erase command (same as Set-up Erase command) to the command register again. The second command initiates the erase operation. The system software routines must now time-out the erase pulse width (10 ms) prior to issuing the Erase-verify command. An integrated stop timer prevents any possibility of overerasure.
3. **Erase-Verify:** Write the Erase-verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFH data (Byte erased). After successful data verification the Erase-verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Flashrite Programming Sequence

A three step command sequence (a two-cycle Program command and one cycle Verify command) is required to program a byte of the Flash array. Refer to the Flashrite Algorithm.

1. **Program Set-Up:** Write the Set-up Program command to the command register.
2. **Program:** Write the Program command to the command register with the appropriate Address and Data. The system software routines must now time-out the program pulse width (10 µs) prior to issuing the Program-verify command. An integrated stop timer prevents any possibility of overprogramming.
3. **Program-Verify:** Write the Program-verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified successfully, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times.

Data Protection

The Am28F256 is designed to offer protection against accidental erasure or programming, caused by spurious system level signals that may exist during power transitions. The Am28F256 powers up in its read only state. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. The device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 10 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

FUNCTIONAL DESCRIPTION

Description Of User Modes

Table 1. Am28F256 User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A0	A9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A0	A9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (A1H)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A0	A9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A0	A9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < $A_n < V_{CC} + 2$ V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. *V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} +2.0 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.*
2. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.*
3. *$11.5 < V_{ID} < 13.0$ V*
4. *Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.*
5. *With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).*
6. *Refer to Table 3 for valid D_{IN} during a write operation.*
7. *All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A_9 and A_0 must be held at V_{IL}.*

READ ONLY MODE

$V_{PP} < V_{CC} + 2$ V
Command Register Inactive

Read

The Am28F256 functions as a read only memory when $V_{PP} < V_{CC} + 2$ V. The Am28F256 has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC}-t_{OE}$).

Standby Mode

The Am28F256 has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), consumes less than 100 µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1 mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A PROM Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13.0 V) on address A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to V_{CC} + 2.0 V while using this Auto select mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the Am28F256 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F256 Auto Select Code

Type	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	A1	1	0	1	0	0	0	0	1

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%

Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 3 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Am28F256 Command Definitions

	First Bus Cycle			Second Bus Cycle		
Command	**Operation (Note 1)**	**Address (Note 2)**	**Data (Note 3)**	**Operation (Note 1)**	**Address (Note 2)**	**Data (Note 3)**
Read Memory (Note 6)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/A1H
Erase Set-up/EraseWrite (Note 4)	Write	X	20H	Write	X	20H
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Program Set-up/ Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Reset (Note 6)	Write	X	FFH	Write	X	FFH

Notes:

1. *Bus operations are defined in Table 1.*
2. *RA = Address of the memory location to be read.*
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   X = Don't care.
   Addresses are latched on the falling edge of the WE pulse.
3. *RD = Data read from location RA during read operation.*
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of WE.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. *Figure 1 illustrates the Flasherase Electrical Erase Algorithm.*
5. *Figure 3 illustrates the Flashrite Programming Algorithm.*
6. *Please reference Reset Command section.*

FLASH MEMORY PROGRAM/ERASE OPERATIONS

AMD's Flasherase and Flashrite Algorithms

Flasherase Erase Sequence

Erase Set-Up/Erase Commands

Erase Set-Up

Erase Set-up is the first of a two-cycle erase command. It is a command-only operation that stages the device for bulk chip erase. The array contents are not altered with this command. 20H is written to the command register in order to perform the Erase Set-up operation.

Erase

The second two-cycle erase command initiates the bulk erase operation. You must write the Erase command (20H) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-verify) to the register.

This two step sequence of the Set-up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, chip erasure can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note: *The Flash memory device must be fully programmed to 00H data prior to erasure. This equalizes the charge on all memory cells ensuring reliable erasure.*

Erase-Verify Command

The erase operation erases all bytes of the array in parallel. After the erase operation, all bytes must be sequentially verified. The Erase-verify operation is initiated by writing A0H to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse or $\overline{CE}$ pulse, whichever occurs later. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-verify operation, the Am28F256 applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are properly erased.

Verify Next Address

You must write the Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ pulse, whichever occurs later. The process continues for each byte in the memory array until a byte does not return FFH data or all the bytes in the array are accessed and verified.

If an address is not verified to FFH data, the entire chip is erased again (refer to Erase Set-up/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The device is now ready to be programmed. At this point, the verification operation is terminated by writing a valid command (e.g. Program set-up) to the command register. Figure 1 and Table 4, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

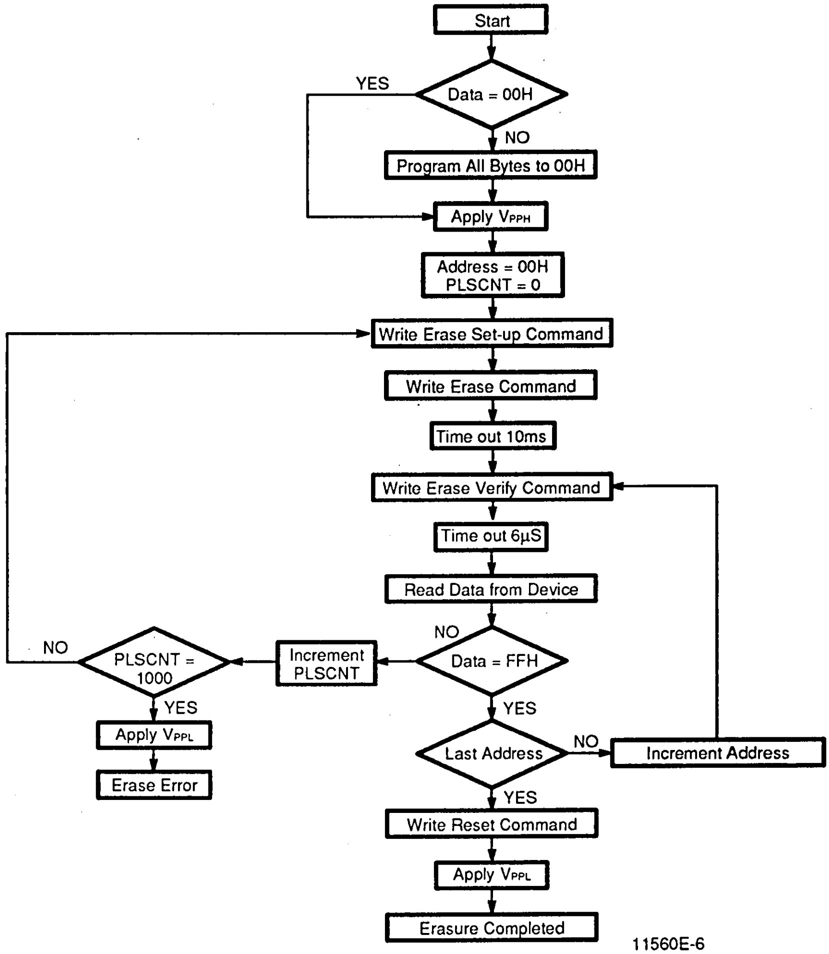


Figure 1. Flasherase Electrical Erase Algorithm

Flasherase Electrical Erase Algorithm

This Flash memory device erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the array. Erasure begins with a read of the memory contents. The Am28F256 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

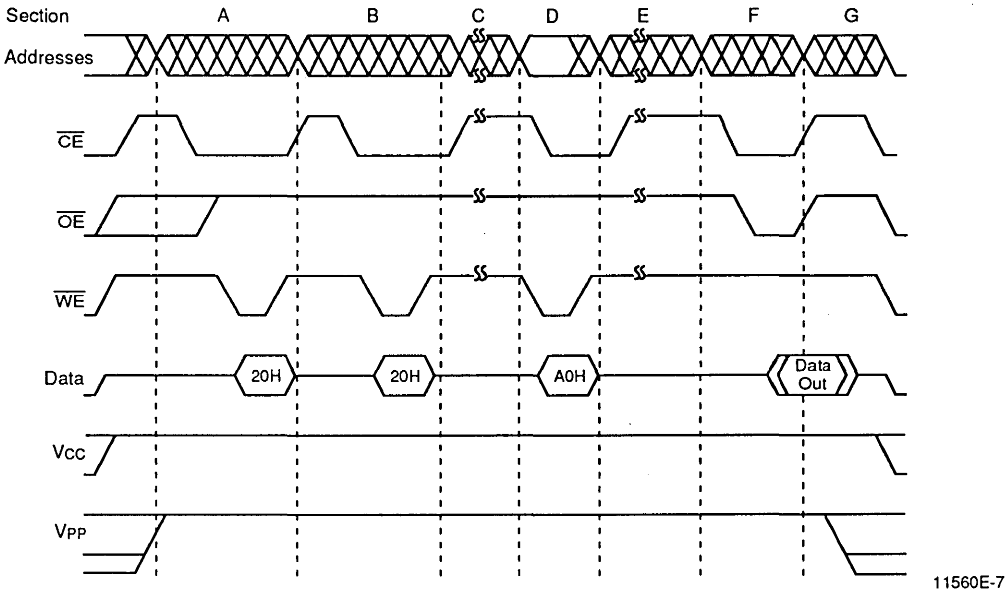
Should the device be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished using the Flashrite Programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. If a byte fails to verify, the device is erased again. With each erase operation, an increasing number of bytes verify to the erased state. Typically, devices are erased in less than 100 pulses (one second). Erase efficiency may be improved by storing the address of the last byte that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. A total of 1000 erase pulses are allowed per reprogram cycle, which corresponds to approximately 10 seconds of cumulative erase time. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 1 illustrates the electrical erase algorithm.

Table 4. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) ***Note:*** *Use Flashrite programming algorithm (Figure 3) for programming.*
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Erase Set-Up	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-Verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Reset	Data = FFH, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. *See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.*
2. *Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.*
3. *The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.*



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time-out	Write	Time-out	Read	Standby
Command	20H	20H	N/A	A0H	N/A	Compare Data	N/A
Function	Erase Set-up	Erase	Erase (10 ms)	Erase-Verify	Transition (6 µs)	Erase Verification	Proceed per Erase Algorithm

Figure 2. AC Waveforms For Erase Operations

Analysis of Erase Timing Waveform

Note: *This analysis does not include the requirement to program the entire array to 00H data prior to erasure. Refer to the Flashrite algorithm.*

Erase Set-Up/Erase

This analysis illustrates the use of two-cycle erase commands (section A and B). The first erase command (20H) is a set-up command and does not affect the array data (section A). The second erase command (20H) initiates the erase operation (section B) on the rising edge of this $\overline{WE}$ pulse. All bytes of the memory array are erased in parallel. No address information is required.

The erase pulse occurs in section C.

Time-Out

A software timing routine (10 ms duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Note: *An integrated stop timer prevents any possibility of overerasure by limiting each time-out period of 10 ms.*

Erase-Verify

Upon completion of the erase software timing routine, the microprocessor must write the Erase-verify command (A0H). This command terminates the erase operation on the rising edge of the $\overline{WE}$ pulse (section D). The Erase-verify command also stages the device for data verification (section F).

After each erase operation each byte must be verified. The byte address to be verified must be supplied with the Erase-verify command (section D). Addresses are latched on the falling edge of the $\overline{WE}$ pulse.

Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operation (section E).

During Erase-verification (section F) each address that returns FFH data is successfully erased. Each address of the array is sequentially verified in this manner by repeating sections D thru F until the entire array is verified or an address fails to verify. Should an address location fail to verify to FFH data, erase the device again. Repeat sections A thru F. Resume verification (section D) with the failed address.

Each data change sequence allows the device to use up to 1,000 erase pulses to completely erase. Typically 100 erase pulses are required.

Note: *All address locations must be programmed to 00H prior to erase. This equalizes the charge on all memory cells and ensures reliable erasure.*

Flashrite Programming Sequence

Program Set-Up/Program Command

Program Set-Up

The Am28F256 is programmed byte by byte. Bytes may be programmed sequentially or at random. Program Set-up is the first of a two-cycle program command. It stages the device for byte programming. The Program Set-up operation is performed by writing 40H to the command register.

Program

Only after the program set-up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-verify command to terminate the programming operation. This two step sequence of the Set-up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte just programmed must be verified.

Write C0H into the command register in order to initiate the Program-verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-verify operation stages the device for verification of the last byte programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-verify operation, the Am28F256 applies an internally generated margin voltage to the addressed byte. A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte location. Should the byte fail to verify, reprogram (refer to Program Set-up/Program). Figure 3 and Table 5 indicate how instructions are combined with the bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Flashrite Programming Algorithm

The Am28F256 Flashrite Programming algorithm employs an interactive closed loop flow to program data byte by byte. Bytes may be programmed sequentially or at random. The Flashrite Programming algorithm uses 10 microsecond programming pulses. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 3 and Table 5 illustrate the programming algorithm.

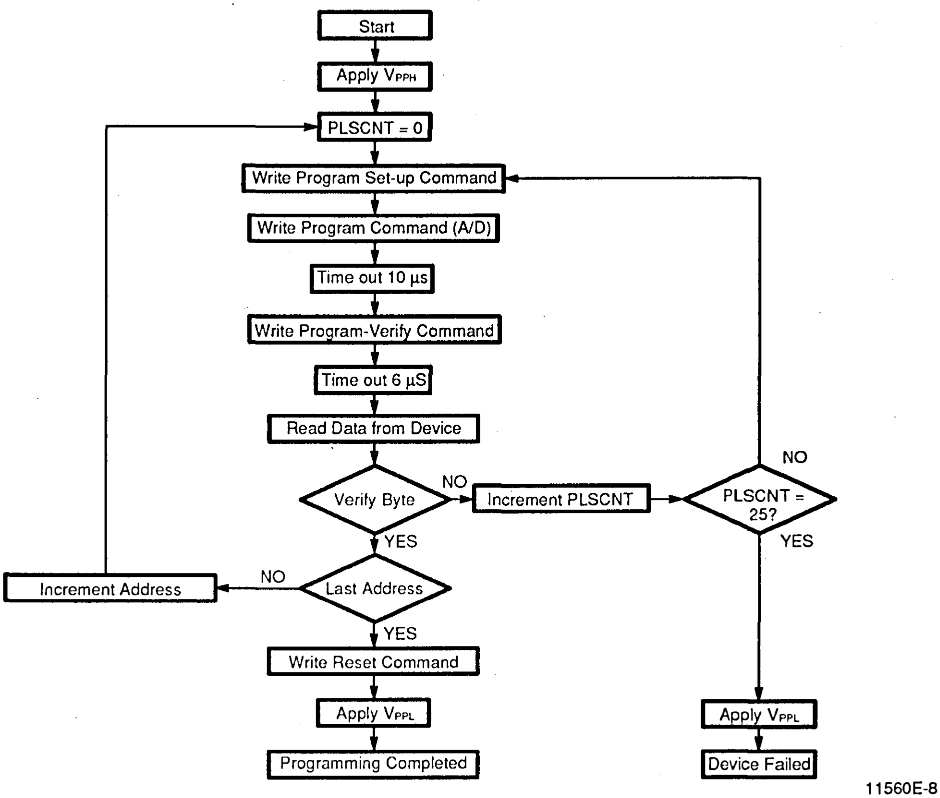


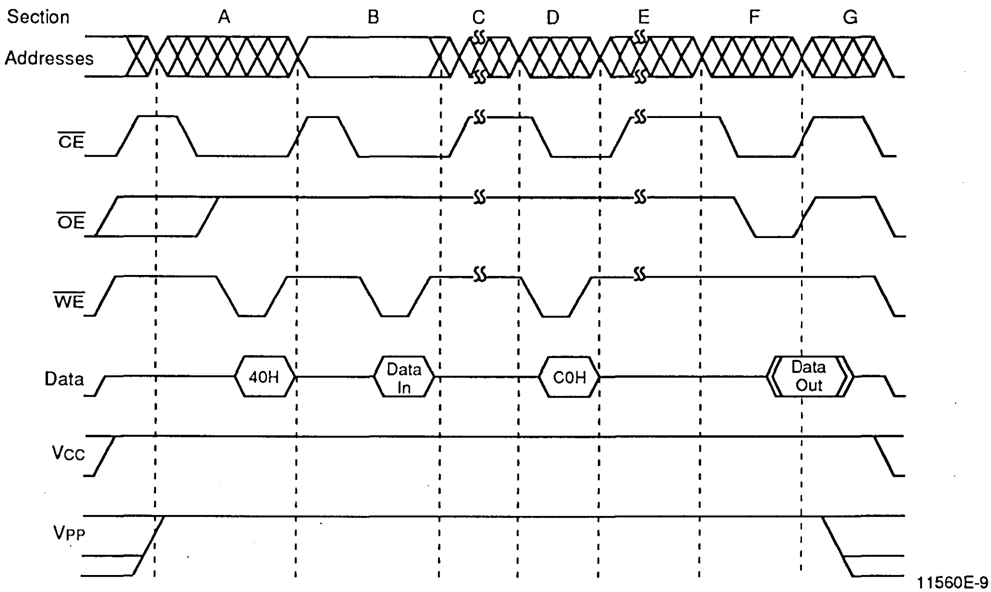
Figure 3. Flashrite Programming Algorithm

Table 5. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Program Set-Up	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Reset	Data = FFH, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. *See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.*
2. *Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.*



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time-out	Write	Time-out	Read	Standby
Command	40H	Program Address, Program Data	N/A	C0H (Stops Program)	N/A	Compare Data	N/A
Function	Program Set-up	Program Command Latch Address & Data	Program (10 µs)	Program Verify	Transition (6 µs)	Program Verification	Proceed per Programming Algorithm

Figure 4. A.C. Waveforms for Programming Operations

Analysis of Program Timing Waveforms

Program Set-Up/Program

Two-cycle write commands are required for program operations (section A and B). The first program command (40H) is a set-up command and does not affect the array data (section A). The second program command latches address and data required for programming on the falling and rising edge of $\overline{WE}$ respectively (section B). The rising edge of this $\overline{WE}$ pulse (section B) also initiates the programming pulse. The device is programmed on a byte by byte basis either sequentially or randomly.

The program pulse occurs in section C.

Time-Out

A software timing routine (10 µs duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Note: *An integrated stop timer prevents any possibility of overprogramming by limiting each time-out period of 10 µs.*

Program-Verify

Upon completion of the program timing routine, the microprocessor must write the program-verify command (C0H). This command terminates the programming operation on the rising edge of the $\overline{WE}$ pulse (section D). The program-verify command also stages the device for data verification (section F). Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operations (section E).

During program-verification (section F) each byte just programmed is read to compare array data with original program data. When successfully verified, the next desired address is programmed. Should a byte fail to verify, reprogram the byte (repeat section A thru F). Each data change sequence allows the device to use up to 25 program pulses per byte. Typically, bytes are verified within one or two pulses.

Algorithm Timing Delays

There are four different timing delays associated with the Flasherase and Flashrite algorithms:

1. The first delay is associated with the V_{PP} rise-time when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on the V_{PP}, the delay required is proportional to the number of devices being erased and the 0.1 μF/device. V_{PP} must reach its final value 100 ns before commands are executed.
2. The second delay time is the erase time pulse width (10 ms). A software timing routine should be run by the local microprocessor to time out the delay. The erase operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the erase operation. To ensure proper device operation, write the Erase-verify operation after each pulse.
3. A third delay time is required for each programming pulse width (10 μs). The programming algorithm is interactive and verifies each byte after a program pulse. The program operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the programming operation.
4. A fourth timing delay associated with both the Flasherase and Flashrite algorithms is the write recovery time (6 μs). During this time internal circuitry is changing voltage levels from the erase/ program level to those used for margin verify and read operations. An attempt to read the device during this period will result in possible false data (it may appear the device is not properly erased or programmed).

Note:
Software timing routines should be written in machine language for each of the delays. Code written in machine language requires knowledge of the appropriate microprocessor clock speed in order to accurately time each delay.

Parallel Device Erasure

Many applications will use more than one Flash memory device. Total erase time may be minimized by implementing a parallel erase algorithm. Flash memories may erase at different rates. Therefore each device must be verified separately. When a device is completely erased and verified use a masking code to prevent further erasure. The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-Up Sequence

The Am28F256 powers-up in the Read only mode. Power supply sequencing is not required.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset command must be written two consecutive times after the set-up Program command (40H). This will reset the device to the Read mode.

Following any other Flash command write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The set-up Program command (40H) is the only command that requires a two sequence reset cycle. The first Reset command is interpreted as program data. However, FFH data is considered null data during programming operations (memory cells are only programmed from a logical "1" to "0"). The second Reset command safely aborts the programming operation and resets the device to the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the set-up Program state or not.

Programming In-System

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Auto Select Command

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F256 contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H. A read cycle from address 0001H returns the device code A1H (see Table 2). To terminate the operation, it is necessary to write another valid command, such as Reset (FFH), into the register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	
Ceramic Packages	–65°C to +150°C
Plastic Packages	–65°C to +125°C
Ambient Temperature with Power Applied	–55°C to + 125°C
Voltage with Respect To Ground	
All pins except A9 and V_{PP} (Note 1)	–2.0 V to +7.0 V
V_{CC} (Note 1)	–2.0 V to +7.0 V
A9 (Note 2)	–2.0 V to +14.0 V
V_{PP} (Note 2)	–2.0 V to +14.0 V
Output Short Circuit Current (Note 3)	200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*

2. *Minimum DC input voltage on A9 and V_{PP} pins is –0.5 V. During voltage transitions, A9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*

3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

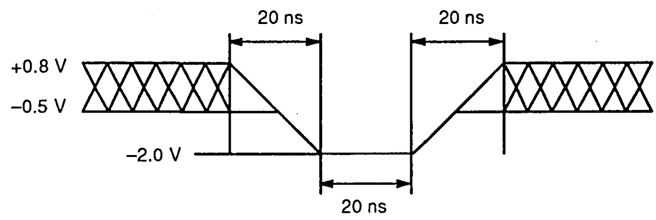
OPERATING RANGES

Commercial (C) Devices	
Case Temperature (T_C)	0°C to +70°C
Industrial (I) Devices	
Case Temperature (T_C)	–40°C to +85°C
Extended (E) Devices	
Case Temperature (T_C)	–55°C to +125°C
Military (M) Devices	
Case Temperature (T_C)	–55°C to +125°C
V_{CC} Supply Voltages	
V_{CC} for Am28F256–X5	+4.75 V to +5.25 V
V_{CC} for Am28F256–XX0	+4.50 V to +5.50 V
V_{PP} Supply Voltages	
Read	–0.5 V to +12.6 V
Program, Erase, and Verify	+11.4 V to +12.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



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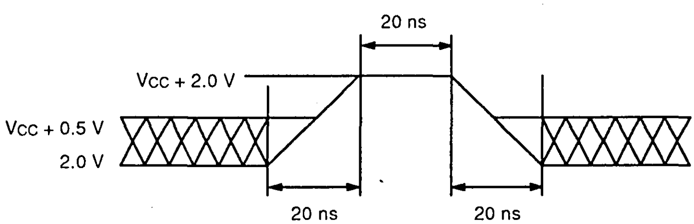
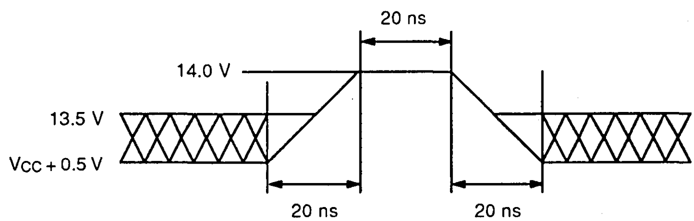
Maximum Positive Input Overshoot



11560E-11

Maximum V_{PP} Overshoot



11560E-12

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1–4)

DC CHARACTERISTICS—TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{IH}$		0.2	1.0	mA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ $I_{OUT} = 0$ mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress (Note 4)		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress (Note 4)		10	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			±1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	µA
		$V_{PP} = V_{PPL}$			±1.0	
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 5.8$ mA $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.5$ mA $V_{CC} = V_{CC}$ Min	2.4			V
V_{ID}	A9 Auto Select Voltage	A9 = V_{ID}	11.5		13.0	V
I_{ID}	A9 Auto Select Current	A9 = V_{ID} Max $V_{CC} = V_{CC}$ Max		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:*** *Erase/Program are inhibited when* $V_{PP} = V_{PPL}$	0.0		V_{CC} +2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. ***Caution:*** *the Am28F256 must not be removed from (or inserted into) a socket when* V_{CC} *or* V_{PP} *is applied.*
2. I_{CC1} *is tested with* $\overline{OE} = V_{IH}$ *to simulate open outputs.*
3. *Maximum active power usage is the sum of* I_{CC} *and* I_{PP}.
4. *Not 100% tested.*

DC CHARACTERISTICS—CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	V_{CC} = V_{CC} Max, V_{IN} = V_{CC} or V_{SS}			± 1.0	µA
I_{LO}	Output Leakage Current	V_{CC} = V_{CC} Max, V_{OUT} = V_{CC} or V_{SS}			± 1.0	µA
I_{CCS}	V_{CC} Standby Current	V_{CC} = V_{CC} Max $\overline{CE}$ = V_{CC} + 0.5 V		15	100	µA
I_{CC1}	V_{CC} Active Read Current	V_{CC} = V_{CC} Max, $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH} I_{OUT} = 0 mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE}$ = V_{IL} Programming in Progress (Note 4)		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE}$ = V_{IL} Erasure in Progress (Note 4)		10	30	mA
I_{PPS}	V_{PP} Standby Current	V_{PP} = V_{PPL}			± 1.0	µA
I_{PP1}	V_{PP} Read Current	V_{PP} = V_{PPH}		70	200	µA
I_{PP2}	V_{PP} Programming Current	V_{PP} = V_{PPH} Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	V_{PP} = V_{PPH} Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8 mA V_{CC} = V_{CC} Min			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.5 mA, V_{CC} = V_{CC} Min	0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, V_{CC} = V_{CC} Min	V_{CC} –0.4			
V_{ID}	A9 Auto Select Voltage	A9 = V_{ID}	11.5		13.0	V
I_{ID}	A9 Auto Select Current	A9 = V_{ID} Max V_{CC} = V_{CC} Max		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:*** *Erase/ Program are inhibited when V_{PP} = V_{PPL}*	0.0		V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. ***Caution:*** *the Am28F256 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
2. *I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.*
3. *Maximum active power usage is the sum of I_{CC} and I_{PP}.*
4. *Not 100% tested.*

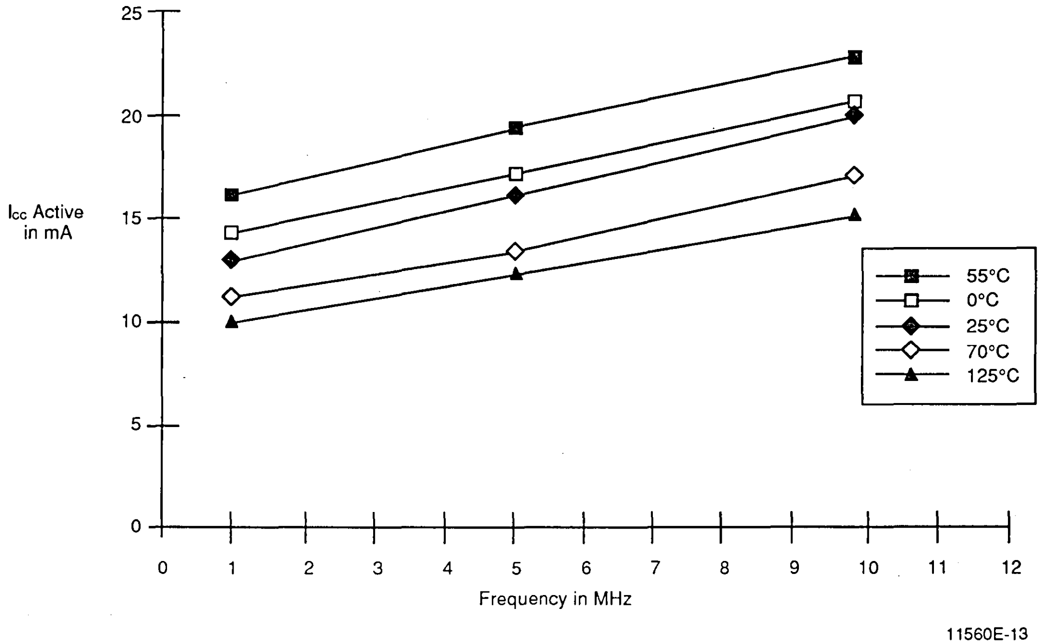


Figure 5. Am28F256–Average I_{CC} Active vs. Frequency
V_{CC} = 5.5 V, Addressing Pattern = Minmax
Data Pattern = Checkerboard

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	8	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A = 25°C$, $f = 1.0$ MHz*

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

AC CHARACTERISTICS—Read Only Operation (Notes 1–4)

Parameter Symbols				Am28F256						
JEDEC	Standard	Parameter Description		— / -75	-90 / -95	-120 / —	-150 / —	-200 / —	-250 / —	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)	Min	70	90	120	150	200	250	ns
			Max							
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min							
			Max	70	90	120	150	200	250	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min							
			Max	70	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min							
			Max	35	35	50	55	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z (Note 4)	Min	0	0	0	0	0	0	ns
			Max							
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z (Note 3)	Min							
			Max	20	20	30	35	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z (Note 4)	Min	0	0	0	0	0	0	ns
			Max							
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z (Note 4)	Min							
			Max	20	20	30	35	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change (Note 4)	Min	0	0	0	0	0	0	ns
			Max							
t_{WHGL}		Write Recovery Time before Read	Min	6	6	6	6	6	6	µs
			Max							
t_{VCS}		V_{CC} Set-up Time to Valid Read (Note 4)	Min	50	50	50	50	50	50	µs
			Max							

Notes:

1. *Output Load: 1 TTL gate and $C_L = 100$ pF*
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. *The Am28F256-75 and Am28F256-95 Output Load: 1 TTL gate and $C_L = 100$ pF*
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0 V to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. *Guaranteed by design not tested.*
4. *Not 100% tested.*

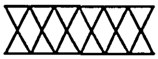
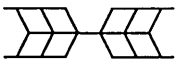
AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1– 6)

Parameter Symbols				Am28F256						
				—	-90	-120	-150	-200	-250	
JEDEC	Standard	Parameter Description		-75	-95	—	—	—	—	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 6)	Min Max	70	90	120	150	200	250	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min Max	0	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min Max	45	45	50	60	75	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min Max	45	45	50	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min Max	10	10	10	10	10	10	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	Min Max	6	6	6	6	6	6	µs
t_{GHWL}		Read Recovery Time before Write	Min Max	0	0	0	0	0	0	µs
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	Min Max	0	0	0	0	0	0	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min Max	0	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min Max	45	45	50	60	60	60	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min Max	20	20	20	20	20	20	ns
t_{WHWH1}		Duration of Programming Operation (Note 4)	Min Max	10	10	10	10	10	10	µs
t_{WHWH2}		Duration of Erase Operation (Note 4)	Min Max	9.5	9.5	9.5	9.5	9.5	9.5	ms
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	100	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	50	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 6)	Min Max	500	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 10% V_{PPL} (Note 6)	Min Max	500	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 6)	Min Max	100	100	100	100	100	100	ns

Notes:

1. *Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.*
2. *All devices except Am28F256-75 and Am28F256-95. Input Rise and Fall times: < 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V*
3. *Am28F256-75 and Am28F256-95. Input Rise and Fall times: < 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V*
4. *Maximum pulse widths not required because the on-chip program/erase stop timer will terminate the pulse widths internally on the device.*
5. *Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the Write Pulse Width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.*
6. *Not 100% tested.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS

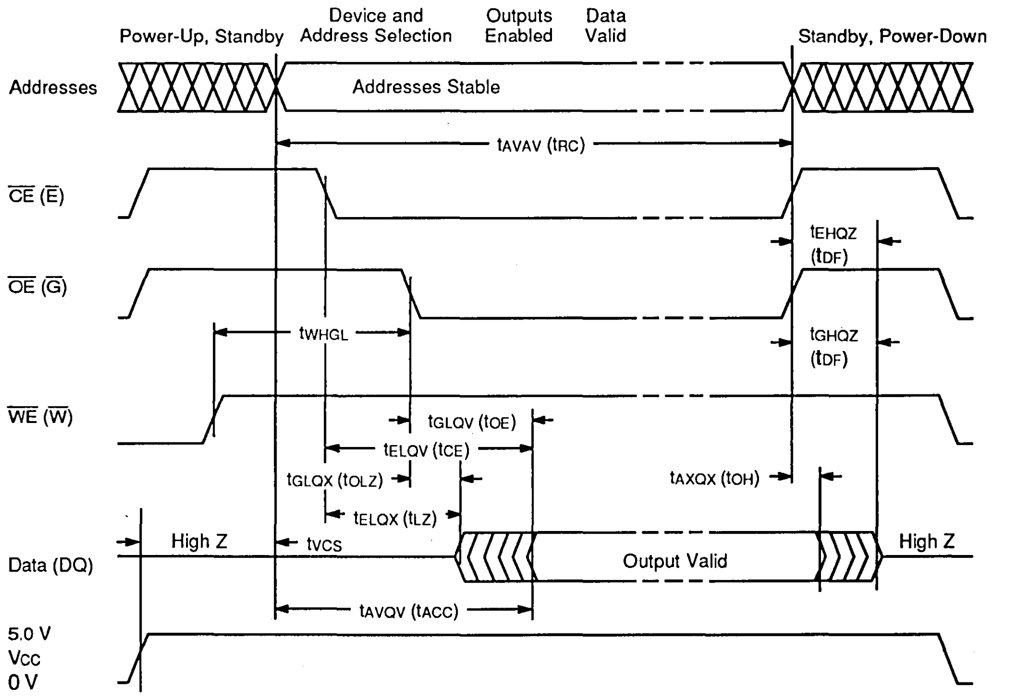


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Figure 6. AC Waveforms for Read Operations

SWITCHING WAVEFORMS

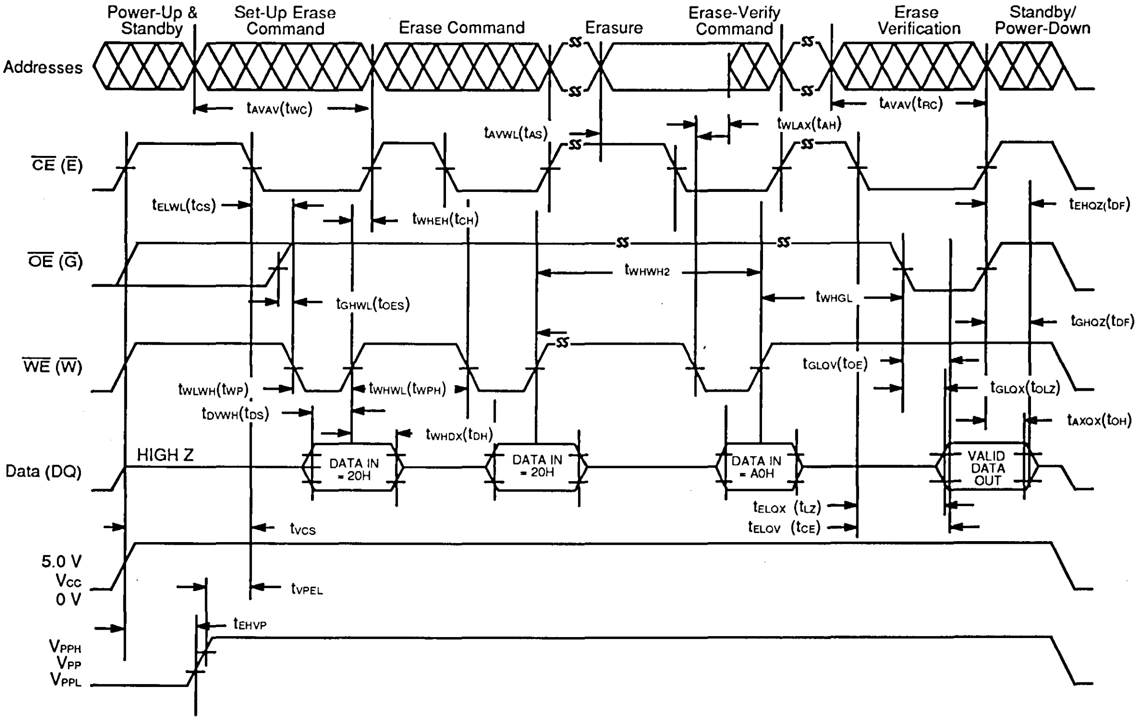

Figure 7. AC Waveforms for Erase Operations

SWITCHING WAVEFORMS

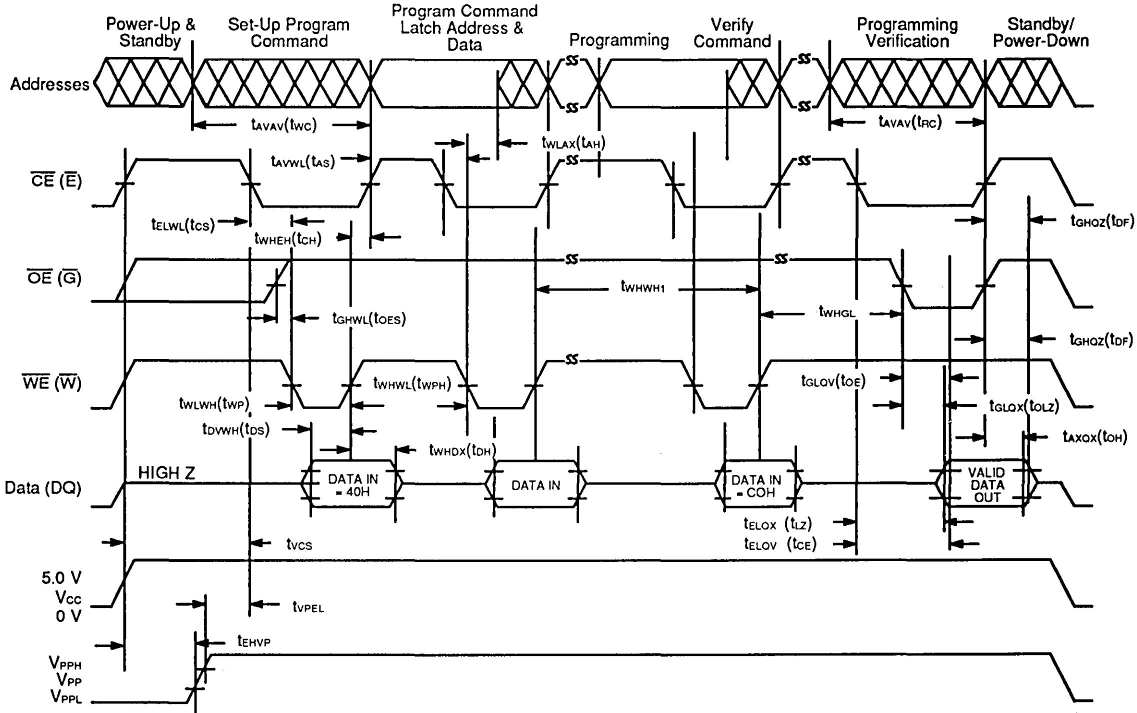

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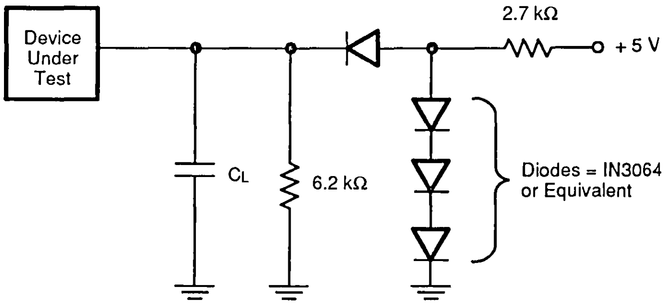
Figure 8. AC Waveforms for Programming Operations

SWITCHING TEST CIRCUIT



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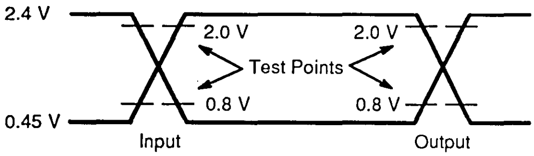
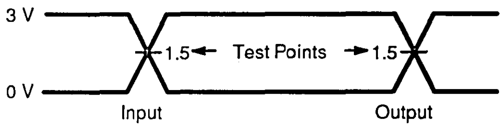
C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORMS



All Devices Except Am28F256-75 and Am28F256-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are < 10 ns.



For Am28F256-75 and Am28F256-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are < 10 ns.

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ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max (Note 3)		
Chip Erase Time		1 (Note 1)	10 (Note 2)	s	Excludes 00H programming prior to erasure
Chip Programming Time		0.5 (Note 1)	3	s	Excludes system-level overhead
Write/Erase Cycles	10,000			Cycles	

Notes:

1. *25°C, 12 V V_{PP}*
2. *The Flasherase/Flashrite algorithms allows for 60 second erase time for military temperature range operations.*
3. *Maximum time specified is lower than worst case. Worst case is derived from the Flasherase/Flashrite pulse count (Flasherase = 1000 max and Flashrite = 25 max). Typical worst case for program and erase operations is significantly less than the actual device limit.*

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A9 and V_{PP})	−1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	−1.0 V	V_{CC} + 1.0 V
Current	−100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

DATA SHEET REVISION SUMMARY FOR Am28F256

Data sheet is Final now, and not Preliminary.

Product Selector Guide

Added -75 ns speed grade at 5% V_{CC} Tolerance.

Ordering Information – Standard Products

Added -75 ns speed grade to the Valid Combinations table. Removed DC package from Am28F256-75, -90, and -95. Removed DC, DI, DE, and DEB packages from Am28F256 from -120, -150, and -200. Removed Package Type D.

Ordering Information – APL Products

This page was removed.

Erase, Program and Read Mode – Write Operations

Removed Command Register Table and Bit assignments.

Erase, Program and Read Mode – Read Command

The statement requiring a 6 µs wait before accessing the first addressed location was removed.

Table 3 – Am28F256 Command Definitions

The note describing a 6 µs wait before accessing the first addressed location was removed.

Flasherase Erase Sequence – Erase Verify Command

The address latched also depends on the falling edge of $\overline{CE}$, whichever happens later.

Flasherase Erase Sequence – Verify Next Address

The new address latched also depends on the falling edge of $\overline{CE}$. whichever happens later.

Auto Select Command

Programming In-System

Titles for each section were switched.

Programming In-System

It is necessary to write a valid command, such as Reset, into the register.

DC Characteristics – TTL/NMOS Compatible

Added Note 4. Those characteristics are not 100% tested.

DC Characteristics – CMOS Compatible

Added Note 4. Those characteristics are not 100% tested.

AC Characteristics – Read Only Operation (Notes 1 and 2)

Added -75 timings. Added Am28F256-75 to Note 2.

AC Characteristics – Write/Erase/Program Operations (Notes 1–5)

Added Am28F256-75 to Notes 2 and 3.

Switching Test Waveforms

For Test Point figures also apply to Am28F256-75.

PRELIMINARY

Am28F256A

256 Kilobit (32,768 x 8-Bit) CMOS 12.0 Volt, Bulk Erase Flash Memory with Embedded Algorithms

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 70 ns maximum access time
- **CMOS low power consumption**
  - 30 mA maximum active current
  - 100 µA maximum standby current
  - No data retention power consumption
- **Compatible with JEDEC-standard byte-wide 32-Pin EPROM pinouts**
  - 32-pin DIP
  - 32-pin PLCC
  - 32-pin TSOP
  - 32-pin LCC
- **100,000 write/erase cycles minimum**
- **Write and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Embedded Erase Electrical Bulk Chip-Erase**
  - 1.5 seconds typical chip-erase including pre-programming
- **Embedded Program**
  - 14 µs typical byte-program including time-out
  - 0.5 second typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell
- **Embedded algorithms for completely self-timed write/erase operations**

GENERAL DESCRIPTION

The Am28F256A is a 256K Flash memory organized as 32K bytes of 8 bits each. AMD's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The Am28F256A is packaged in 32-pin PDIP, PLCC, and TSOP versions. The device is also offered in the ceramic LCC package. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers. The Am28F256A is erased when shipped from the factory

The standard Am28F256A offers access times as fast as 70ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F256A has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F256A uses a command register to manage this functionality, while maintaining a standard JEDEC Flash Standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming.

AMD's Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F256A uses a 12.0 V ± 5% V_{PP} supply to perform the erase and programming functions.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from –1 V to Vcc +1 V.

Embedded Program

The Am28F256A is byte programmable using the Embedded Programming algorithm. The Embedded Programming algorithm does not require the system to time-out or verify the data programmed. The typical room temperature programming time of the Am28F256A is one half second.

Publication# 18879 Rev. A Amendment/0
Issue Date: March 1994

GENERAL DESCRIPTION

Embedded Erase

The entire chip is bulk erased using the Embedded Erase algorithm. The Embedded Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internal to the device. Typical erasure at room temperature is accomplished in one second.

AMD's Am28F256A is entirely pin and software compatible with AMD's Am28F020A, Am28F010A and Am28F512A Flash memories.

Embedded Programming Algorithm vs. Flashrite Programming Algorithm

The Flashrite Programming algorithm requires the user to write a program set-up command, a program command (program data and address), and a program verify command followed by a read and compare operation. The user is required to time the programming pulse width in order to issue the program verify command. An integrated stop timer prevents any possibility of overprogramming. Upon completion of this sequence the data is read back from the device and compared by the user with the data intended to be written; if there is not a match, the sequence is repeated until there is a match or the sequence has been repeated 25 times.

AMD's Embedded Programming algorithm requires the user to only write a program set-up command and a program command (program data and address). The device automatically times the programming pulse width, provides the program verify and counts the number of sequences. A status bit, $\overline{\text{Data}}$ Polling, provides feedback to the user as to the status of the programming operation.

Embedded Erase Algorithm vs. Flasherase Erase Algorithm

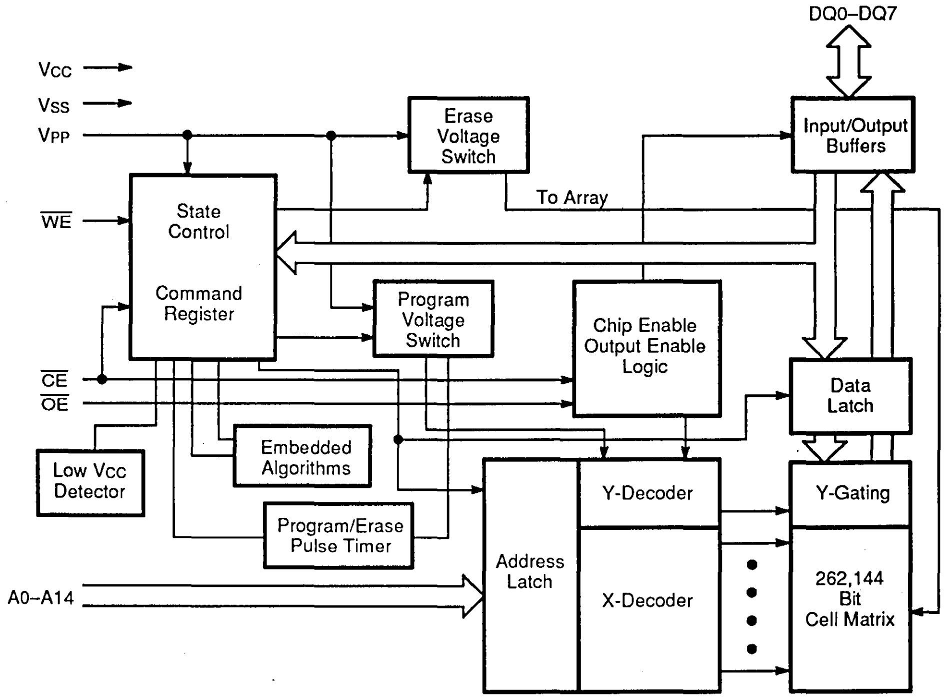
The Flasherase Erase algorithm requires the device to be completely programmed prior to executing an erase command. To invoke the erase operation the user writes an erase set-up command, an erase command, and an erase verify command. The user is required to time the erase pulse width in order to issue the erase verify command. An integrated stop timer prevents any possibility of overerasure. Upon completion of this sequence the data is read back from the device and compared by the user with erased data. If there is not a match, the sequence is repeated until there is a match or the sequence has been repeated 1,000 times.

AMD's Embedded Erase algorithm requires the user to only write an erase set-up command and erase command. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verify and counts the number of sequences. A status bit, $\overline{\text{Data}}$ Polling, provides feedback to the user as to the status of the erase operation.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F256A is designed to support either $\overline{\text{WE}}$ or $\overline{\text{CE}}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$ whichever occurs last. Data is latched on the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$ whichever occurs first. To simplify the following discussion, the $\overline{\text{WE}}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{\text{WE}}$ signal.

AMD's Flash technology combines years of EPROM and EEPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F256A electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

BLOCK DIAGRAM



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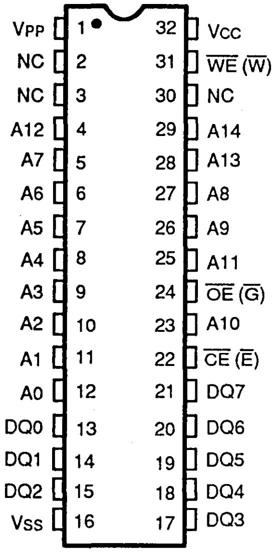
PRODUCT SELECTOR GUIDE

Family Part No.:	**Am28F256A**				
Ordering Part No.:					
±10% VCC Tolerance		**-90**	**-120**	**-150**	**-200**
±5% VCC Tolerance	**-75**	**-95**			
Max Access Time (ns)	70	90	120	150	20
$\overline{CE}$ ($\overline{E}$) Access (ns)	70	90	120	150	200
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	35	50	55	55

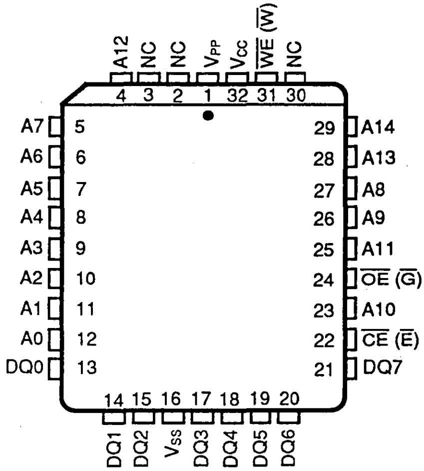
CONNECTION DIAGRAMS

DIP



18879A-2

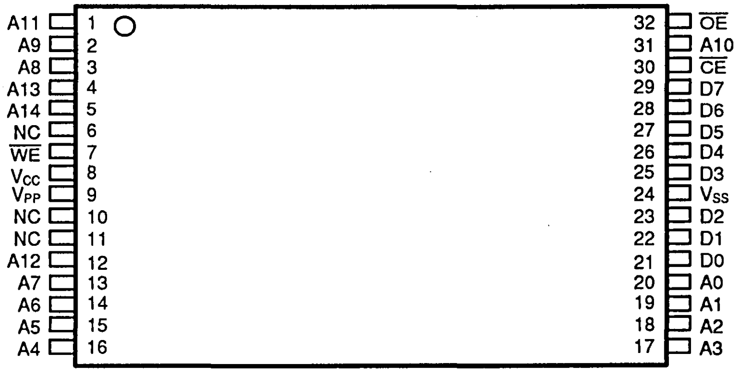
PLCC*



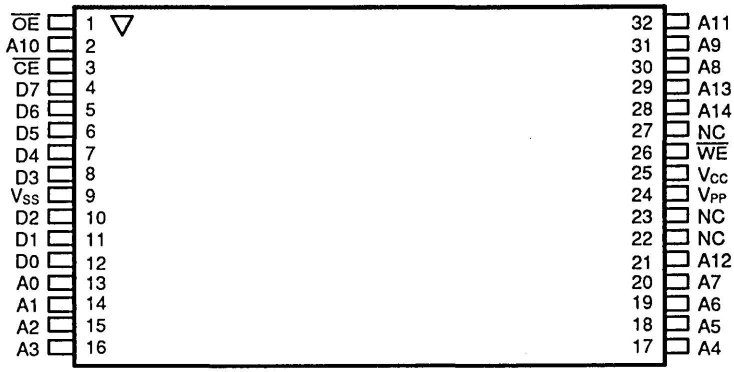
18879A-3

Note: *Pin 1 is marked for orientation.*
**Also available in LCC.*

TSOP PACKAGES



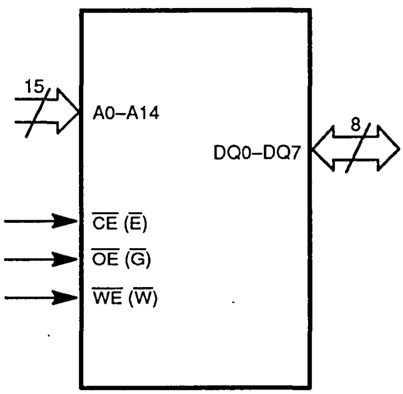
28F256A Standard Pinout



28F256A Reverse Pinout 18879A-4

28F256A 32K x 8 Flash Memory in 32-Lead TSOP

LOGIC SYMBOL



18879A-5

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

AM28F256A **-75** **J** **C** **B**

OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-In

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended (–55°C to +125°C)

PACKAGE TYPE
P = 32-Pin Plastic DIP (PD 032)
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)
E = 32-Pin TSOP Standard Pinout (TS 032)
F = 32-Pin TSOP Reverse Pinout (TSR 032)
L = 32-Pin Rectangular Leadless Chip Carrier (CLR 032)

SPEED
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am28F256A
256 Kilobit (32K x 8-Bit) CMOS Flash Memory with Embedded Algorithms

Valid Combinations	
Am28F256A-75 Am28F256A-90 Am28F256A-95	PC, JC, EC, FC, LC
Am28F256A-120 Am28F256A-150 Am28F256A-200	PC, PI, JC, JI, PE, PEB, JE, JEB, EC, FC, EI, FI, EE, FE, EEB, FEB, DI, LC, LI, LE, LEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTION

A0–A14
Address Inputs for memory locations. Internal latches hold addresses during write cycles.

$\overline{CE}$ (E)
The Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.

DQ0–DQ7
Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

NC
No Connect-corresponding pin is not connected internally to the die.

$\overline{OE}$ (G)
The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

V_{CC}
Power supply for device operation. (5.0 V ± 5% or 10%)

V_{PP}
Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2$ V.

V_{SS}
Ground

$\overline{WE}$ (W)
The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

BASIC PRINCIPLES

The Am28F256A uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0 V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F256A functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F256A's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F256A is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Embedded Erase Algorithm

AMD now makes erasure extremely simple and reliable. The Embedded Erase algorithm requires the user to only write an erase set-up command and erase command. The device will automatically pre-program and verify the entire array. The device automatically times the erase pulse width, provides the erase verify and counts the number of sequences. A status bit, $\overline{\text{Data}}$ Polling, provides feedback to the user as to the status of the erase operation.

Embedded Programming Algorithm

AMD now makes programming extremely simple and reliable. The Embedded Programming algorithm requires the user to only write a program set-up command and a program command. The device automatically times the programming pulse width, provides the program verify and counts the number of sequences. A status bit, $\overline{\text{Data}}$ Polling, provides feedback to the user as to the status of the programming operation.

Data Protection

The Am28F256A is designed to offer protection against accidental erasure or programming, caused by spurious system level signals that may exist during power transitions. The Am28F256A powers up in its read only state. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. The device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 10 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

FUNCTIONAL DESCRIPTION

Description of User Modes

Table 1. Am28F256A User Bus Operations

Operation		$\overline{CE}$ (E)	$\overline{OE}$ (G)	$\overline{WE}$ (W)	V_{PP} (Note 1)	A0	A9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A0	A9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (2FH)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A0	A9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A0	A9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} \leq V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An < V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. *V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC}$ +2.0 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.*
2. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.*
3. *$11.5 \leq V_{ID} \leq 13.0$ V*
4. *Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.*
5. *With V_{PP} at high voltage, the standby current is I_{CC} + I_{PP} (standby).*
6. *Refer to Table 3 for valid D_{IN} during a write operation.*
7. *All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A9 and A0 must be held at V_{IL}.*

READ ONLY MODE

$V_{PP} < V_{CC} + 2$ V
Command Register Inactive

Read

The Am28F256A functions as a read only memory when $V_{PP} < V_{CC} + 2$ V. The Am28F256A has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC} - t_{OE}$).

Standby Mode

The Am28F256A has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), consumes less than 100 µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1 mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A PROM Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13.0 V) on address A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to $V_{CC} + 2.0$ V while using this Auto select mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the Am28F256A these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F256A Auto Select Code

Type	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	2F	0	0	1	0	1	1	1	1

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%

Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 3 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Am28F256A Command Definitions

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 4)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/2FH
Embedded Erase Set-up/ Embedded Erase	Write	X	30H	Write	X	30H
Embedded Program Set-up/ Embedded Program	Write	X	10H or 50H	Write	PA	PD
Reset (Note 4)	Write	X	FFH	Write	X	FFH

Notes:

1. *Bus operations are defined in Table 1.*
2. *RA = Address of the memory location to be read.*
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   X = Don't care.
3. *RD = Data read from location RA during read operation.*
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
4. *Please reference Reset Command section.*

FLASH MEMORY PROGRAM/ERASE OPERATIONS

AMD's Embedded Program and Erase Operations

Embedded Erase Algorithm

The automatic chip erase does not require the device to be entirely pre-programmed prior to executing the Embedded set-up erase command and Embedded erase command. Upon executing the Embedded erase command the device automatically will program and verify the entire memory for an all zero data pattern. The system is not required to provide any controls or timing during these operations.

When the device is automatically verified to contain an all zero pattern, a self-timed chip erase and verify begin. The erase and verify operation are complete when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to Read mode. The system is not required to provide any control or timing during these operations.

When using the Embedded Erase algorithm, the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard erase verify command is used.

The Embedded Erase Set-Up command is a command only operation that stages the device for automatic electrical erasure of all bytes in the array. Embedded Erase Set-Up is performed by writing 30H to the command register.

To commence automatic chip erase, the command 30H must be written again to the command register. The automatic erase begins on the rising edge of the $\overline{WE}$ and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to Read mode.

Figure 5 and Table 4 illustrate the Embedded Erase algorithm, a typical command string and bus operation.

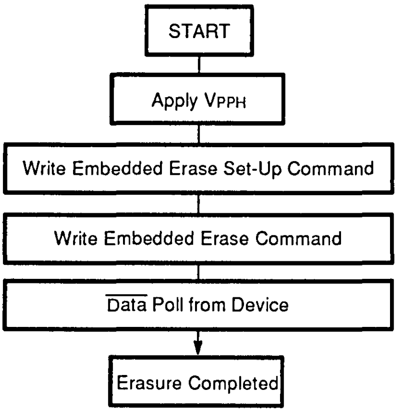


Figure 5. Embedded Erase Algorithm

Table 4. Embedded Erase Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Erase Set-Up Command	Data = 30H
Write	Embedded Erase Command	Data = 30H
Read		$\overline{\text{Data}}$ Polling to Verify Erasure
Standby		Compare Output to FFH
Read		Available for Read Operations

Note:

1. *See DC Characteristics for value of V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Functional Description.*

Embedded Programming Algorithm

The Embedded Program Set-Up is a command only operation that stages the device for automatic programming. Embedded Program Set-Up is performed by writing 10H or 50H to the command register.

Once the Embedded Set-Up Program operation is performed, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ pulse, whichever happens later. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. The rising edge of $\overline{WE}$ also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin. The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to Read mode.

Figure 6 and Table 5 illustrate the Embedded Program algorithm, a typical command string, and bus operation.

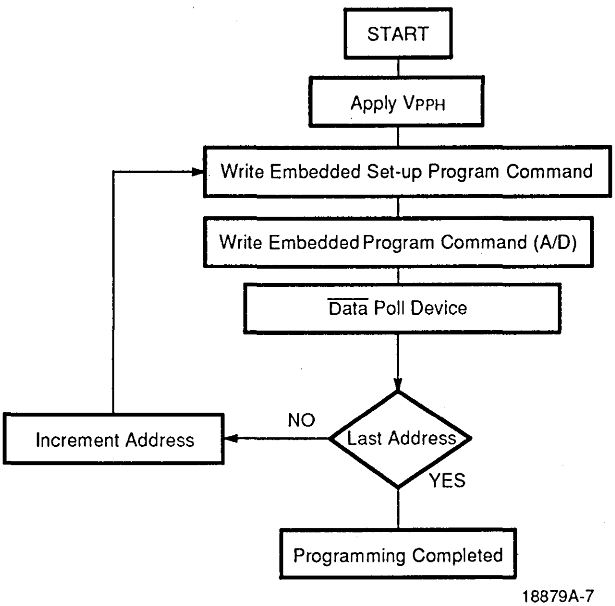


Figure 6. Embedded Programming Algorithm

Table 5. Embedded Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Program Set-Up Command	Data = 10H or 50H
Write	Embedded Program Command	Valid Address/Data
Read		$\overline{\text{Data}}$ Polling to Verify Completion
Read		Available for Read Operations

Note:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Functional Description. Device is either powered-down, erase inhibit or program inhibit.

Write Operation Status

$\overline{\text{Data}}$ Polling—DQ7

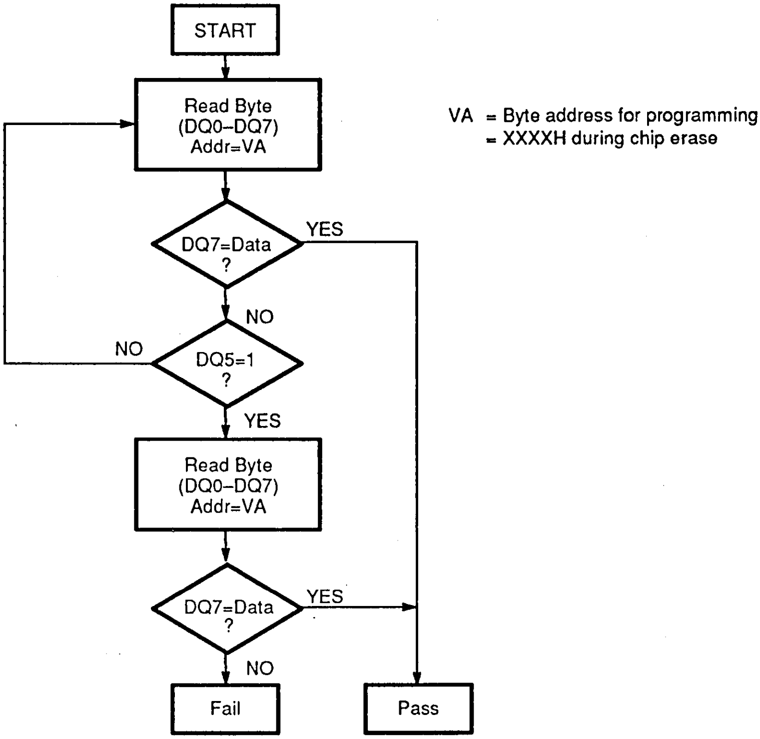
The Am28F256A features $\overline{\text{Data}}$ Polling as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Programming algorithm is in operation, an attempt to read the device at a valid address will produce the complement of expected Valid data on DQ7. Upon completion of the Embedded Program algorithm an attempt to read the device at a valid address will produce Valid data on DQ7. The $\overline{\text{Data}}$ Polling feature is valid after the rising edge of the second $\overline{\text{WE}}$ pulse of the two write pulse sequence.

While the Embedded Erase algorithm is in operation, DQ7 will read "0" until the erase operation is completed. Upon completion of the erase operation, the data on DQ7 will read "1." The $\overline{\text{Data}}$ Polling feature is valid after the rising edge of the second $\overline{\text{WE}}$ pulse of the two Write pulse sequence.

The $\overline{\text{Data}}$ Polling feature is only active during Embedded Programming or erase algorithms.

See Figures 7a and 8a for the $\overline{\text{Data}}$ Polling timing specifications and diagrams. $\overline{\text{Data}}$ Polling is the standard method to check the write operation status, however, an alternative method is available using Toggle Bit.



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Note:

1. DQ7 is rechecked even if DQ5="1" because DQ7 may change simultaneously with DQ5 or after DQ5.

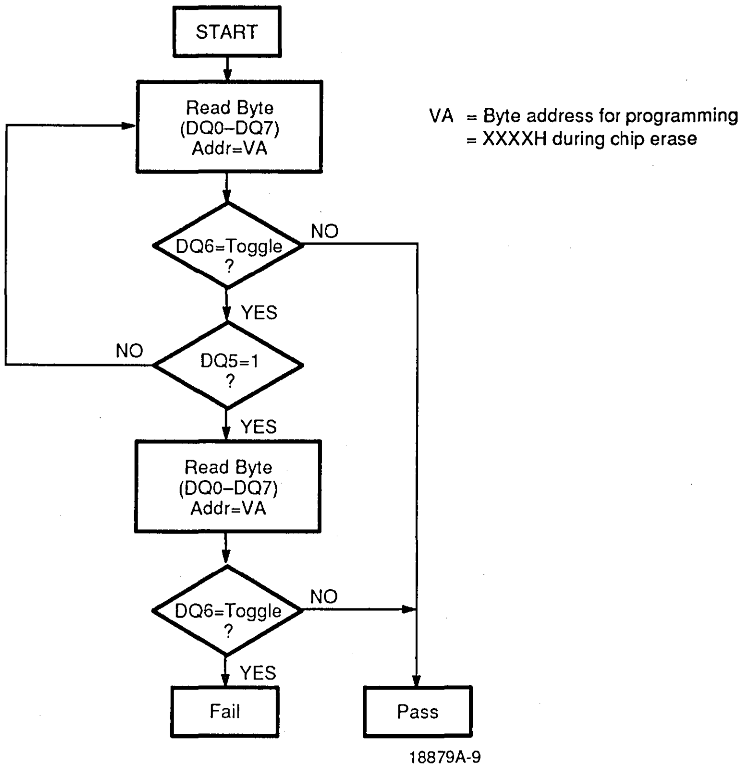
Figure 7a. $\overline{\text{Data}}$ Polling Algorithm

Toggle Bit—DQ6

The Am28F256A also features a "Toggle Bit" as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

Successive attempts to read data from the device at a valid address, while the Embedded Program algorithm is in progress, or at any address while the Embedded Erase algorithm is in progress, will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase algorithm is completed, DQ6 will stop toggling to indicate the completion of either Embedded operation. Only on the next read cycle will valid data be obtained. The toggle bit is valid after the rising edge of the first $\overline{WE}$ pulse of the two write pulse sequence, unlike $\overline{Data}$ Polling which is valid after the rising edge of the second $\overline{WE}$ pulse. This feature allows the user to determine if the device is partially through the two write pulse sequence.

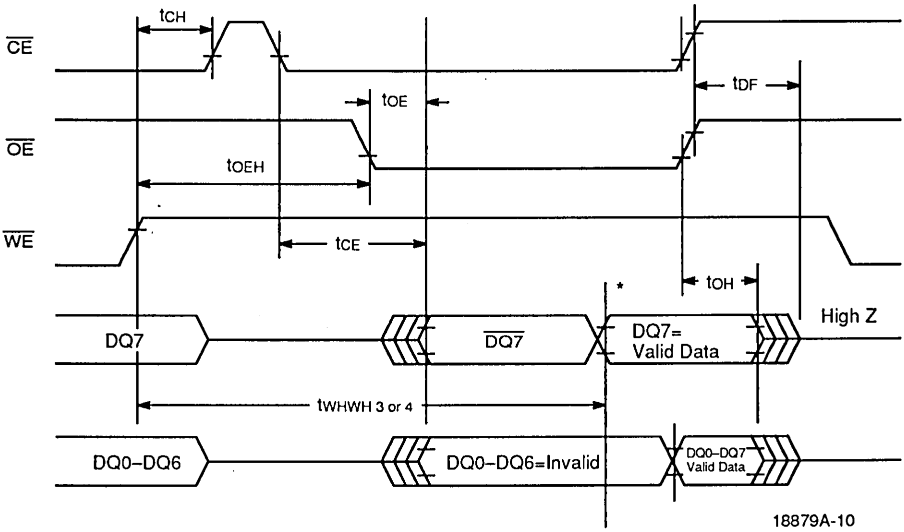
See Figures 7b and 8b for the Toggle Bit timing specifications and diagrams.



Note:

1. DQ6 is rechecked even if DQ5="1" because DQ6 may stop toggling at the same time as DQ5 changing to "1".

Figure 7b. Toggle Bit Algorithm



Note:

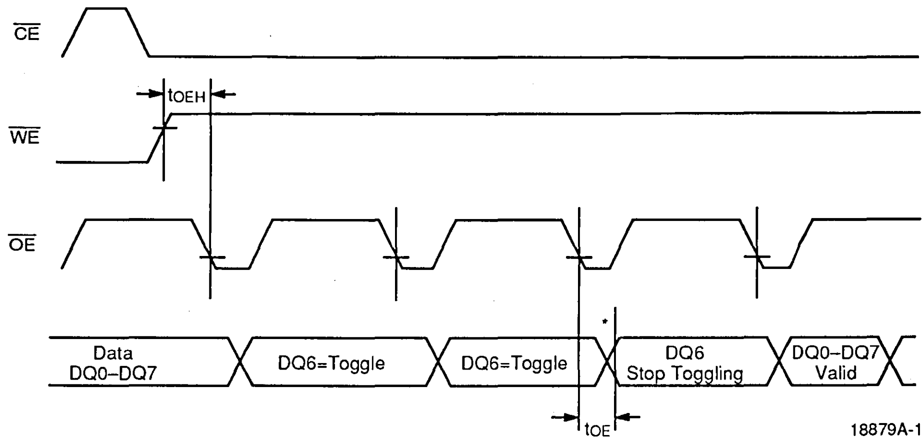
**DQ7=Valid Data (The device has completed the Embedded operation).*

Figure 8a. AC Waveforms for $\overline{\text{Data}}$ Polling During Embedded Algorithm Operations

DQ5

Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits. This is a failure condition and the device may not be used again (internal pulse count exceeded). Under these conditions DQ5 will produce a "1." The program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the device under this condition. The $\overline{\text{CE}}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in Table 1.



Note:

**DQ6 stops toggling (The device has completed the Embedded operation).*

Figure 8b. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

Parallel Device Erasure

The Embedded Erase algorithm greatly simplifies parallel device erasure. Since the erase process is internal to the device, a single erase command can be given to multiple devices concurrently. By implementing a parallel erase algorithm, total erase time may be minimized.

Note that the Flash memories may erase at different rates. If this is the case, when a device is completely erased, use a masking code to prevent further erasure (over-erasure). The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-Up Sequence

The Am28F256A powers-up in the Read only mode. Power supply sequencing is not required.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset must be written two consecutive times after the Set-up Program command (10H or 50H). This will reset the device to the Read mode.

Following any other Flash command, write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The Set-up Program command (10H or 50H) is the only command that requires a two-sequence reset cycle. The first Reset command is interpreted as program data. However, FFH data is considered as null data during programming operations (memory cells are only programmed from a logical "1" to "0"). The second Reset command safely aborts the programming operation and resets the device to the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the Set-up Program state or not.

In-System Programming Considerations

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the circuit board.

Auto Select Command

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. In order to correctly program any Flash memories in-system, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F256A contains an Auto Select operation to supplement traditional PROM programming methodologies. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H (AMD). A read cycle from address 0001H returns the device code 2FH (see Table 2). To terminate the operation, it is necessary to write another valid command, such as Reset (FFH), into the register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages . . . . –65°C to +150°C
Plastic Packages . . . . –65°C to +125°C

Ambient Temperature
with Power Applied . . . . –55°C to + 125°C

Voltage with Respect To Ground
All pins except A9 and V_{PP}
(Note 1) . . . . –2.0 V to +7.0 V

V_{CC} (Note 1) . . . . –2.0 V to +7.0 V

A9 (Note 2) . . . . –2.0 V to +14.0 V

V_{PP} (Note 2) . . . . –2.0 V to +14.0 V

Output Short Circuit Current (Note 3) . . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A9 and V_{PP} pins is –0.5 V. During voltage transitions, A9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) . . . . 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) . . . . –40°C to +85°C

Extended (E) Devices
Case Temperature (T_C) . . . . –55°C to +125°C

Military (M) Devices
Case Temperature (T_C) . . . . –55°C to +125°C

V_{CC} Supply Voltages
V_{CC} for Am28F256A–X5 . . . . +4.75 V to +5.25 V

V_{CC} for Am28F256A–XX0 . . . . +4.50 V to +5.50 V

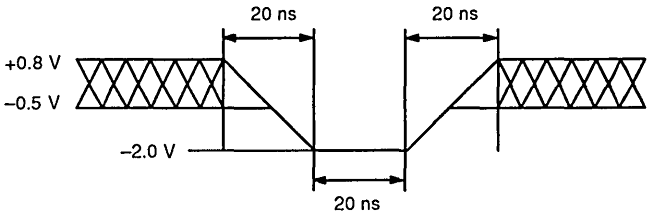
V_{PP} Supply Voltages
Read . . . . –0.5 V to +12.6 V

Program, Erase, and Verify . . . . . +11.4 V to +12.6 V

Operating ranges define those limits between which the funtionality of the device is guaranteed.

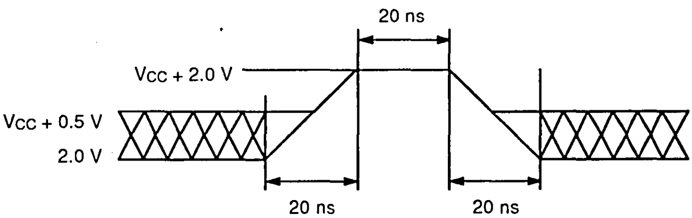
MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



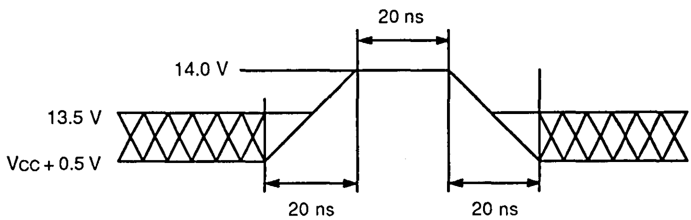
18879A-12

Maximum Positive Input Overshoot



18879A-13

Maximum V_{PP} Overshoot



18879A-14

DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1–4)

DC CHARACTERISTICS-TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS}			±1.0	μA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}			±1.0	μA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{IH}$		0.2	1.0	mA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ $I_{OUT} = 0$ mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress (Note 4)		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress (Note 4)		10	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			±1.0	μA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	μA
		$V_{PP} = V_{PPL}$			±1.0	
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 5.8$ mA $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.5$ mA $V_{CC} = V_{CC}$ Min	2.4			V
V_{ID}	A9 Auto Select Voltage	A9 = V_{ID}	11.5		13.0	V
I_{ID}	A9 Auto Select Current	A9 = V_{ID} Max $V_{CC} = V_{CC}$ Max		5	50	μA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:*** *Erase/Program are inhibited when $V_{PP} = V_{PPL}$*	0.0		V_{CC} +2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. ***Caution:*** *the Am28F256A must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
2. *I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.*
3. *Maximum active power usage is the sum of I_{CC} and I_{PP}.*
4. *Not 100% tested.*

DC CHARACTERISTICS—CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS}			± 1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}			± 1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{CC} + 0.5$ V		15	100	µA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ $I_{OUT} = 0$ mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress (Note 4)		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress (Note 4)		10	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			± 1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	µA
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 5.8$ mA $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.5$ mA, $V_{CC} = V_{CC}$ Min	0.85 V_{CC}			V
V_{OH2}		$I_{OH} = -100$ µA, $V_{CC} = V_{CC}$ Min	V_{CC} –0.4			
V_{ID}	A9 Auto Select Voltage	A9 = V_{ID}	11.5		13.0	V
I_{ID}	A9 Auto Select Current	A9 = V_{ID} Max $V_{CC} = V_{CC}$ Max		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:*** *Erase/Program are inhibited when $V_{PP} = V_{PPL}$*	0.0		V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. ***Caution:*** *the Am28F256A must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
2. *I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.*
3. *Maximum active power usage is the sum of I_{CC} and I_{PP}.*
4. *Not 100% tested.*

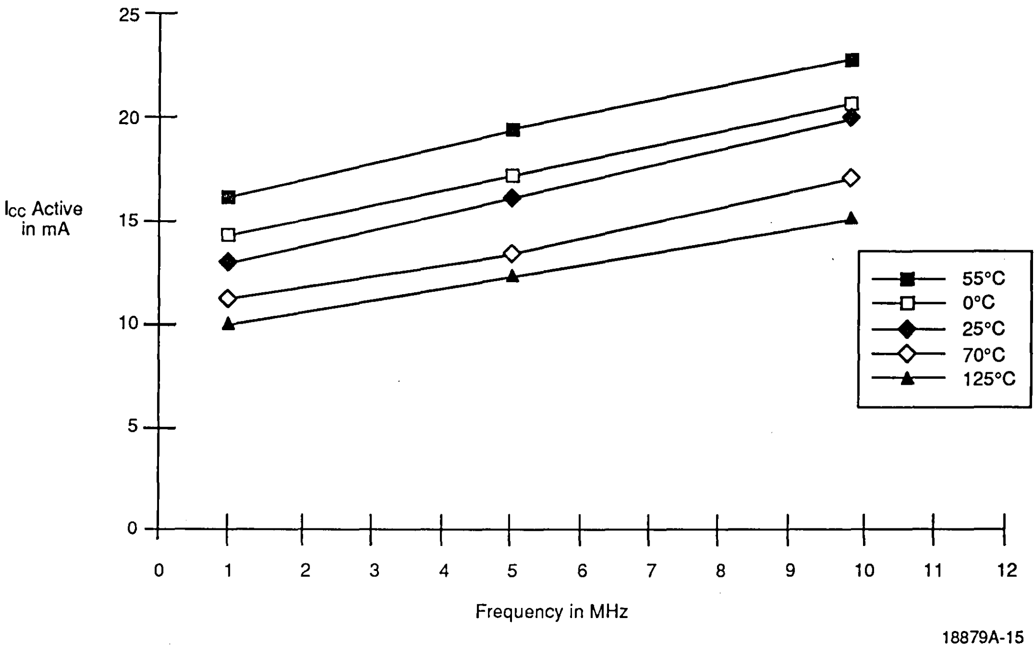


Figure 9. Am28F256A – Average I_{CC} Active vs. Frequency
V_{CC} = 5.5 V, Addressing Pattern = Minmax
Data Pattern = Checkerboard

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	8	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A = 25°C$, $f = 1.0$ MHz*

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

AC CHARACTERISTICS—Read Only Operation (Notes 1–4)

Parameter Symbols				Am28F256A						
JEDEC	Standard	Parameter Description		— -75	-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)	Min	70	90	120	150	200	250	ns
			Max							
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min							
			Max	70	90	120	150	200	250	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min							
			Max	70	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min							
			Max	35	35	50	55	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z (Note 4)	Min	0	0	0	0	0	0	ns
			Max							
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z (Note 3)	Min							
			Max	20	20	30	35	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z (Note 4)	Min	0	0	0	0	0	0	ns
			Max							
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z (Note 4)	Min							
			Max	20	20	30	35	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change (Note 4)	Min	0	0	0	0	0	0	ns
			Max							
t_{WHGL}		Write Recovery Time before Read	Min	6	6	6	6	6	6	µs
			Max							
t_{VCS}		V_{CC} Set-up Time to Valid Read (Note 4)	Min	50	50	50	50	50	50	µs
			Max							

Notes:

1. *Output Load: 1 TTL gate and $C_L = 100$ pF*
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. *The Am28F256A-75 and Am28F256A-95 Output Load: 1 TTL gate and $C_L = 100$ pF*
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0 V to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. *Guaranteed by design not tested.*
4. *Not 100% tested.*

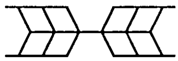
AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1–6)

Parameter Symbols				Am28F256A						
				—	-90	-120	-150	-200	-250	
JEDEC	Standard	Parameter Description		-75	-95	—	—	—	—	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 6)	Min Max	70	90	120	150	200	250	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min Max	0	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min Max	45	45	50	60	75	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min Max	45	45	50	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min Max	10	10	10	10	10	10	ns
t_{OEH}		Output Enable Hold Time for Embedded Algorithm only (See Figure 8)	Min Max	10	10	10	10	10	10	ns
t_{GHWL}		Read Recovery Time before Write	Min Max	0	0	0	0	0	0	µs
t_{ELWLE}	t_{CSE}	Chip Enable Embedded Algorithm Setup Time	Min Max	20	20	20	20	20	20	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min Max	0	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min Max	45	45	50	60	60	60	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min Max	20	20	20	20	20	20	ns
t_{WHWH3}		Embedded Programming Operation (Note 4)	Min Max	14	14	14	14	14	14	µs
t_{WHWH4}		Embedded Erase Operation (Note 5)	Typ Max	3	5	5	5	5	5	s
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	100	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	50	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 6)	Min Max	500	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 90% V_{PPL} (Note 6)	Min Max	500	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 6)	Min Max	100	100	100	100	100	100	ns

Notes:

1. *Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.*
2. *All devices except Am28F256A-75 and Am28F256A-95. Input Rise and Fall times: $\leq$ 10 ns; Input Pulse Levels: 0.45 V t o 2.4 V. Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V*
3. *Am28F256A-75 and Am28F256A-95. Input Rise and Fall times: $\leq$ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V*
4. *Embedded Program Operation of 14 µs consists of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.*
5. *Embedded erase operation of 5 sec consists of 4 sec array pre-programming time and one sec array erase time. This is a typical time for one embedded erase operation.*
6. *Not 100% tested.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS

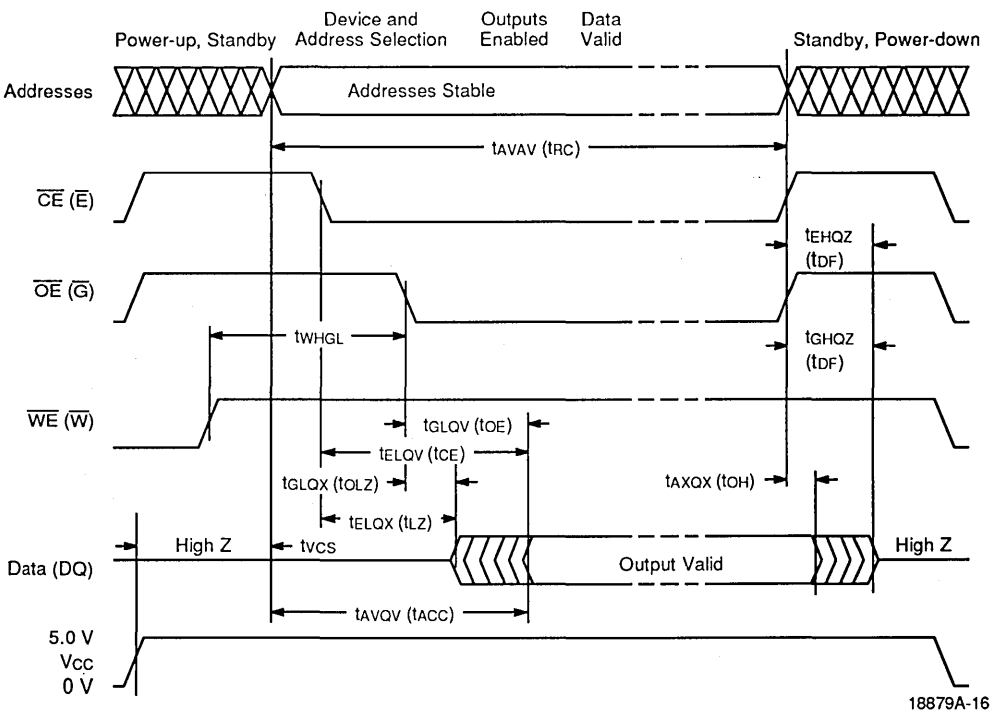
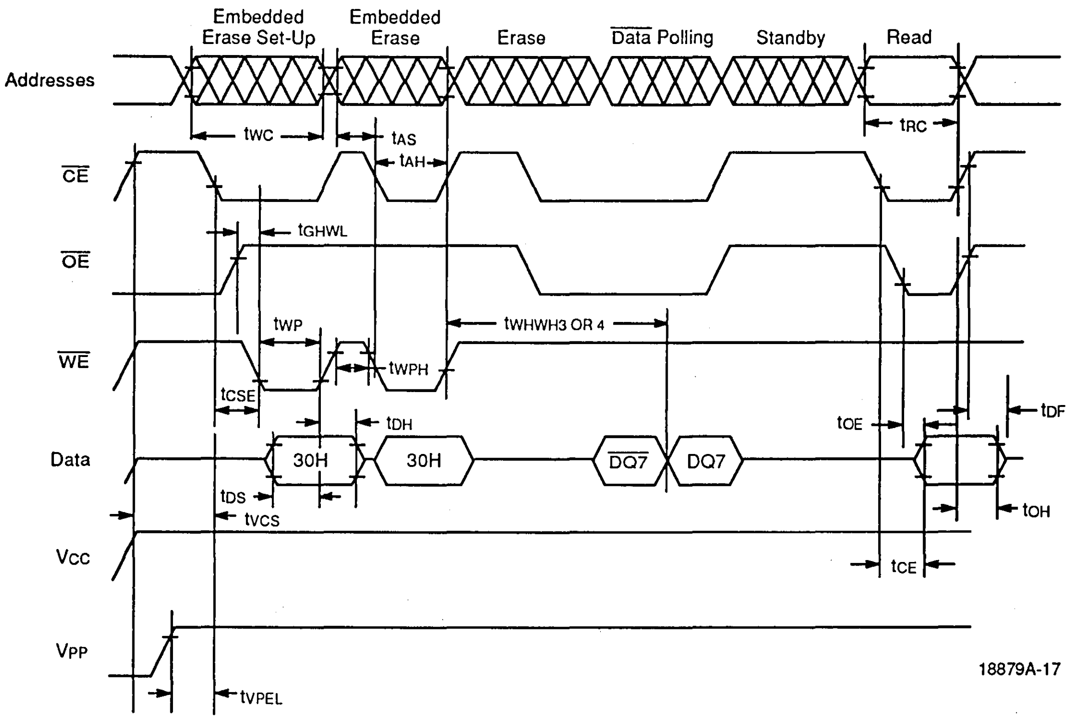


Figure 10. AC Waveforms for Read Operations

SWITCHING WAVEFORMS

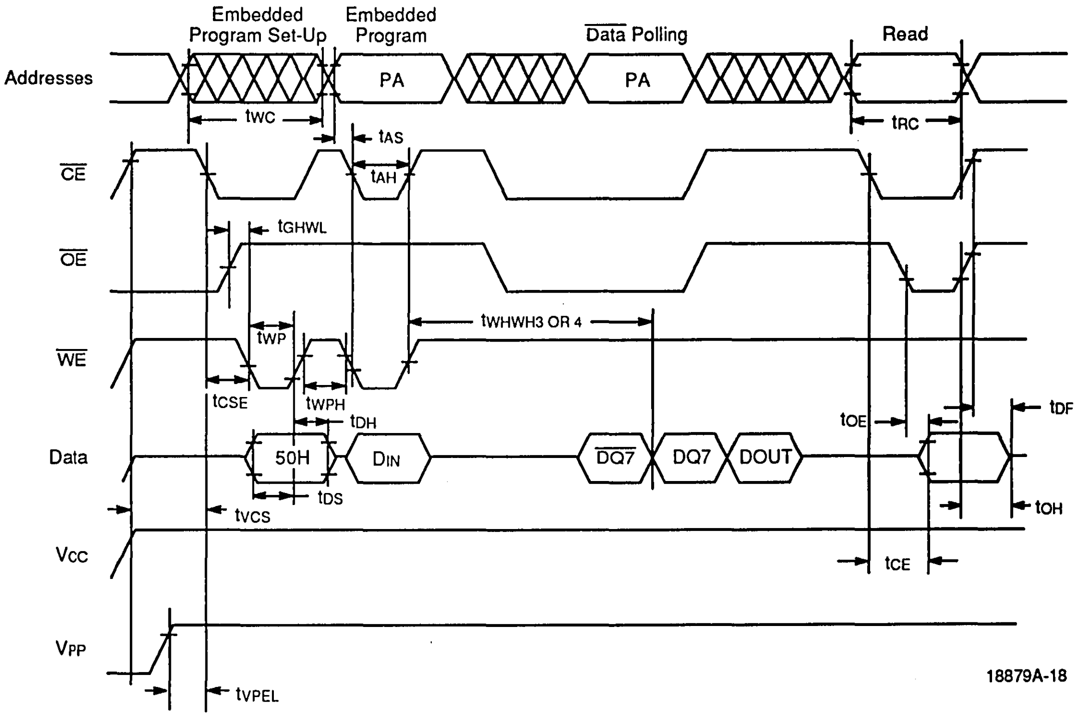


Note:

1. $\overline{DQ7}$ is the output of the complement of the data written to the device.

Figure 11. AC Waveforms for Embedded Erase Operation

SWITCHING WAVEFORMS



Notes:

1. *DIN is data input to the device.*
2. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
3. *DOUT is the output of the data written to the device.*

Figure 12. AC Waveforms for Embedded Programming Operation

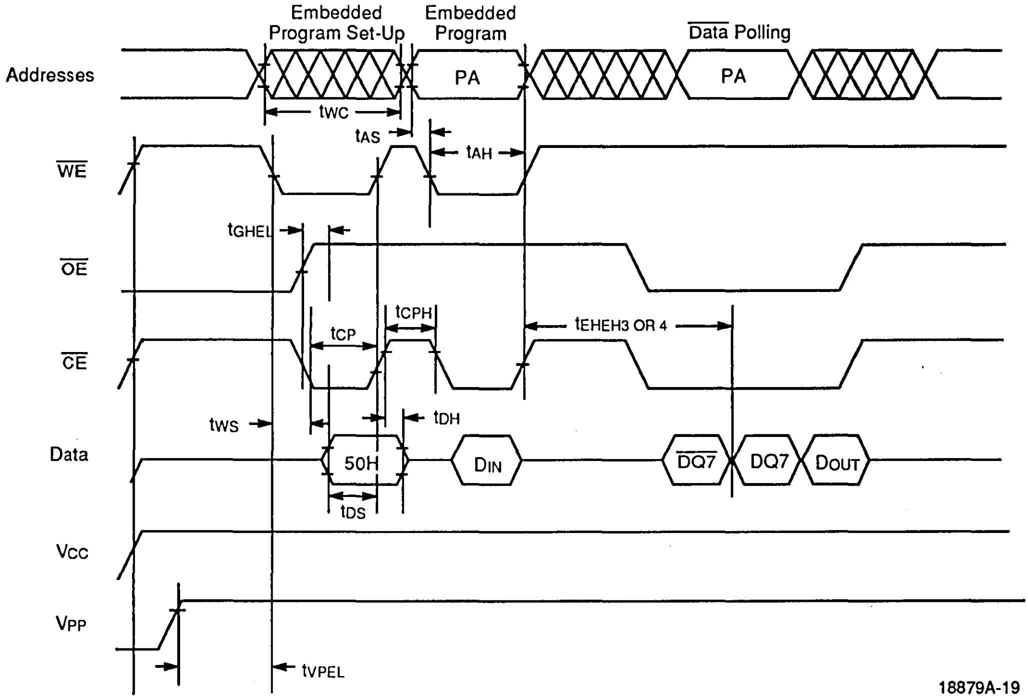
AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1– 6)
Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols				Am28F256A						
JEDEC	Standard	Parameter Description		— -75	-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 6)	Min Max	70	90	120	150	200	250	ns
t_{AVEL}	t_{AS}	Address Set-Up Time	Min Max	0	0	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min Max	45	45	50	60	75	75	ns
t_{DVEH}	t_{DS}	Data Set-Up Time	Min Max	45	45	50	50	50	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min Max	10	10	10	10	10	10	ns
t_{OEH}		Output Enable Hold Time for Embedded Algorithm only (See Figure 8)	Min Max	10	10	10	10	10	10	ns
t_{GHEL}		Read Recovery Time Before Write	Min Max	0	0	0	0	0	0	µs
t_{WLEL}	t_{WS}	WE Set-Up Time by $\overline{CE}$	Min Max	0	0	0	0	0	0	ns
t_{EHWK}	t_{WH}	WE Hold Time	Min Max	0	0	0	0	0	0	ns
t_{ELEH}	t_{CP}	Write Pulse Width	Min Max	65	65	70	80	80	80	ns
t_{EHEL}	t_{CPH}	Write Pulse Width HIGH	Min Max	20	20	20	20	20	20	ns
t_{EHEH3}		Embedded Programming Operation (Note 4)	Min Max	14	14	14	14	14	14	µs
t_{EHEH4}		Embedded Erase Operation (Note 5)	Min Max	3	3	3	3	3	3	s
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	100	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	50	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 6)	Min Max	500	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 90% V_{PPL} (Note 6)	Min Max	500	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 6)	Min Max	100	100	100	100	100	100	ns

Notes:

1. *Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.*
2. *All devices except Am28F256A-75 and Am28F256A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V. Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V*
3. *Am28F256A-75 and Am28F256A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V*
4. *Embedded Program Operation of 14 µs consists of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.*
5. *Embedded erase operation of 5 sec consists of 4 sec array pre-programming time and one sec array erase time. This is a typical time for one embedded erase operation.*
6. *Not 100% tested.*

SWITCHING WAVEFORMS

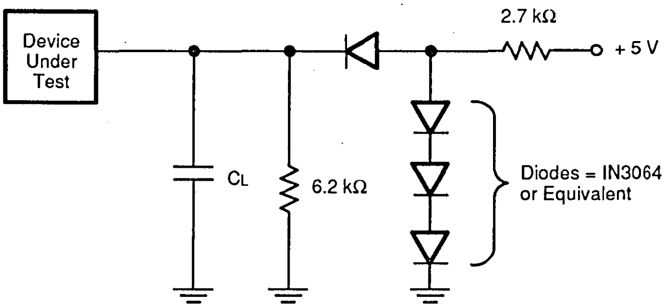


Notes:

1. *DIN is data input to the device.*
2. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
3. *DOUT is the output of the data written to the device.*

Figure 13. AC Waveforms for Embedded Programming Operation Using $\overline{CE}$ Controlled Writes

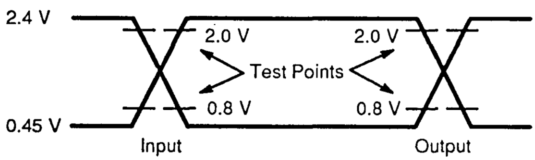
SWITCHING TEST CIRCUIT



18879A-20

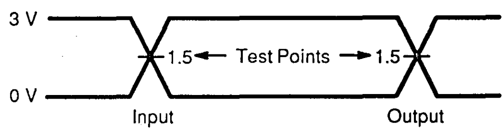
C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORMS



All Devices Except Am28F256A-75 and Am28F256A-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are < 10 ns.



For Am28F256A-75 and Am28F256A-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are < 10 ns.

18879A-21

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits Min	Limits Typ	Limits Max (Note 3)	Unit	Comments
Chip Erase Time		1 (Note 1)	10 (Note 2)	s	Excludes 00H programming prior to erasure
Chip Programming Time		0.5 (Note 1)	4	s	Excludes system-level overhead
Write/Erase Cycles	100,000			Cycles	
Byte Program Time		14		µs	
			96 (Note 4)	ms	

Notes:

1. *25°C, 12 V V_{PP}*
2. *The Embedded algorithm allows for 60 second erase time for military temperature range operations.*
3. *Maximum time specified is lower than worst case. Worst case is derived from the Embedded Algorithm internal counter which allows for a maximum 6000 pulses for both program and erase operations. Typical worst case for program and erase is significantly less than the actual device limit.*
4. *Typical worst case = 84 µs. DQ5 = "1" only after a byte takes longer than 96 ms to program.*

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A9 and V_{PP})	−1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	−1.0 V	V_{CC} + 1.0 V
Current	−100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

FINAL

Am28F512

512 Kilobit (65,536 x 8-Bit) CMOS 12.0 Volt, Bulk Erase Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - — 70 ns maximum access time
- **CMOS Low power consumption**
  - — 30 mA maximum active current
  - — 100 µA maximum standby current
  - — No data retention power consumption
- **Compatible with JEDEC-standard byte-wide 32-Pin EPROM pinouts**
  - — 32-pin DIP
  - — 32-pin PLCC
  - — 32-pin TSOP
  - — 32-pin LCC
- **10,000 write/erase cycles minimum**
- **Write and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Flasherase Electrical Bulk Chip-Erase**
  - — One second typical chip-erase
- **Flashrite Programming**
  - — 10 µs typical byte-program
  - — One second typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - — Low cost single transistor memory cell
- **Automatic write/erase pulse stop timer**

GENERAL DESCRIPTION

The Am28F512 is a 512K bit Flash memory organized as 64K bytes of 8 bits each. AMD's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The Am28F512 is packaged in 32-pin PDIP, PLCC, and TSOP versions. The device is also offered in the ceramic LCC package. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers. The Am28F512 is erased when shipped from the factory.

The standard Am28F512 offers access times as fast as 70 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F512 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F512 uses a command register to manage this functionality, while maintaining a standard JEDEC Flash Standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming.

AMD's Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F512 uses a 12.0 V ± 5% V_{PP} supply to perform the Flasherase and Flashrite algorithms.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1 V to Vcc +1 V.

The Am28F512 is byte programmable using 10 µs programming pulses in accordance with AMD's Flashrite programming algorithm. The typical room temperature programming time of the Am28F512 is one second. The entire chip is bulk erased using 10 ms erase pulses according to AMD's Flasherase alrogithm. Typical erasure at room temperature is accomplished in less than one second. The windowed package and the 15–20 minutes required for EPROM erasure using ultra-violet light are eliminated.

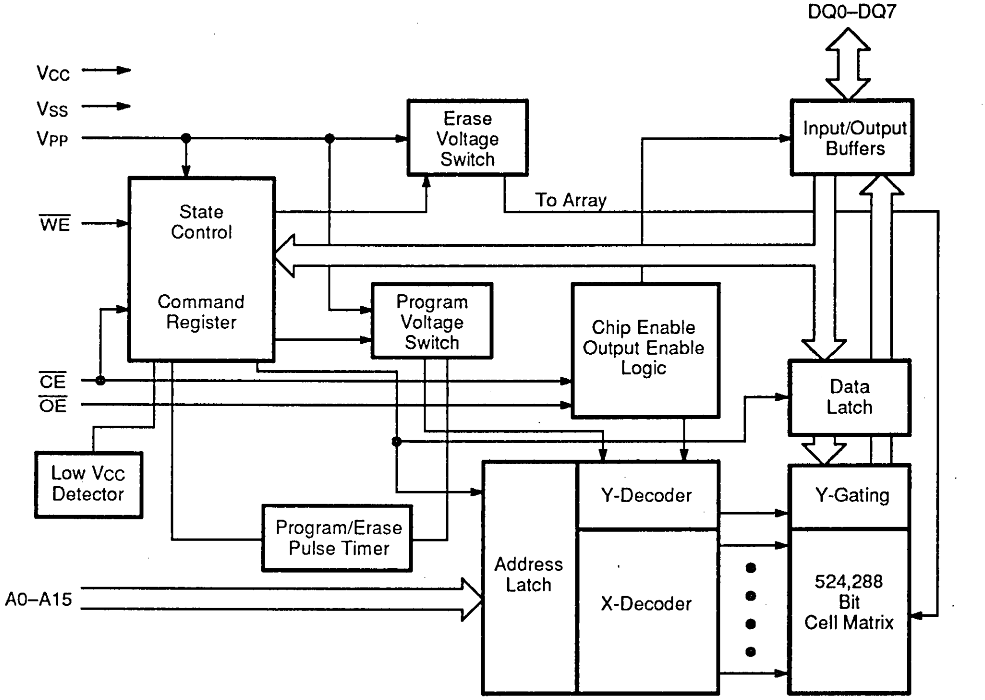
Publication# 11561 Rev. E Amendment/0
Issue Date: March 1994

GENERAL DESCRIPTION

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F512 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

AMD's Flash technology combines years of EPROM and EEPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F512 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

BLOCK DIAGRAM



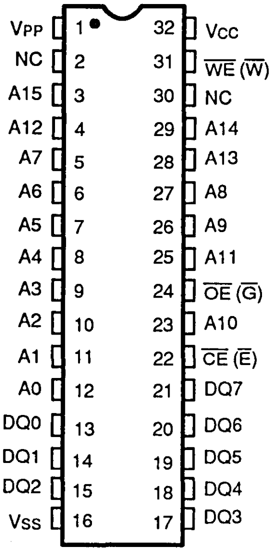
11561E-1

PRODUCT SELECTOR GUIDE

Family Part No.:	Am28F512				
Ordering Part No.: ±10% Vcc Tolerance		**-90**	**-120**	**-150**	**-200**
±5% Vcc Tolerance	**-75**	**-95**			
Max Access Time (ns)	70	90	120	150	200
$\overline{CE}$ ($\overline{E}$) Access (ns)	70	90	120	150	200
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	35	50	55	55

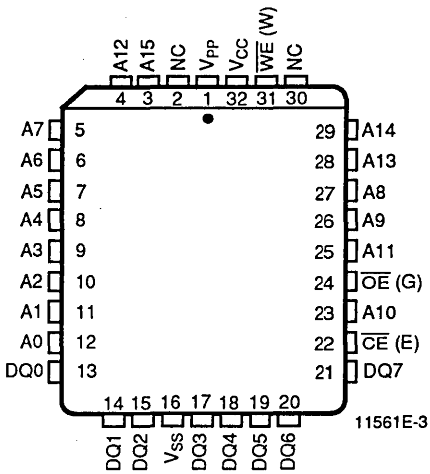
CONNECTION DIAGRAMS

DIP



11561E-2

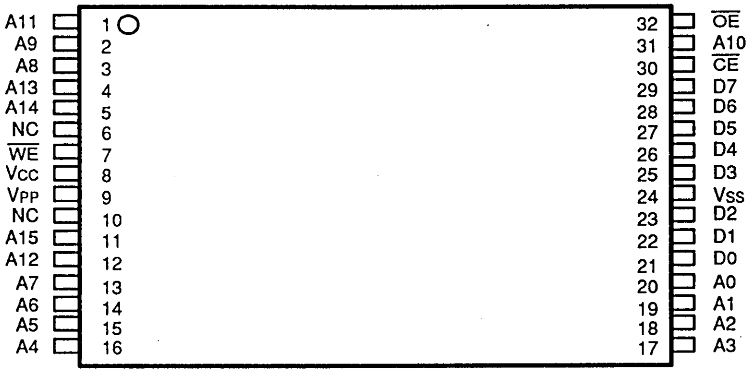
PLCC*



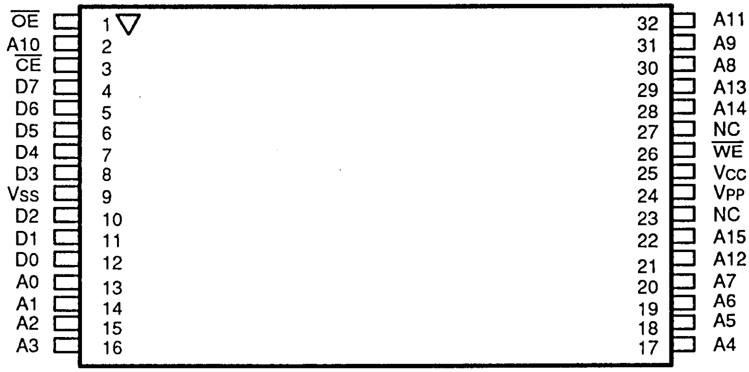
11561E-3

Note: *Pin 1 is marked for orientation.*
**Also available in LCC.*

TSOP PACKAGES



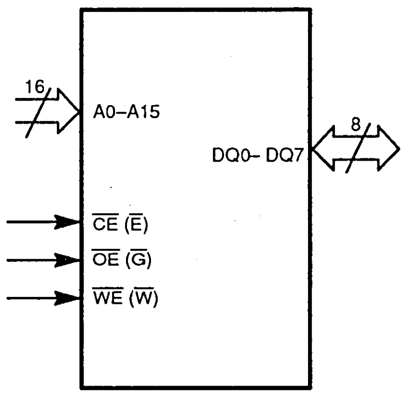
28F512 Standard Pinout



28F512 Reverse Pinout 11561E-4

28F512 64K x 8 Flash Memory in 32-Lead TSOP

LOGIC SYMBOL



11561E-5

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

AM28F512 -75 J C B

OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-In

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to + 85°C)
E = Extended (–55°C to + 125°C)

PACKAGE TYPE
P = 32-Pin Plastic DIP (PD 032)
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)
L = 32-Pin Rectangular Ceramic Leadless Chip Carrier (CLR 032)
E = 32-Pin TSOP Standard Pinout (TS 032)
F = 32-Pin TSOP Reverse Pinout (TSR 032)

SPEED
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am28F512
512 Kilobit (64K x 8-Bit) CMOS Flash Memory

Valid Combinations	
AM28F512-75 AM28F512-90 AM28F512-95	PC, JC, LC, EC, FC
AM28F512-120 AM28F512-150 AM28F512-200	PC, PI, PE, PEB, JC, JI, JE, JEB, LC, LI, LE, LEB, EC, FC, EI, FI, EE, FE, EEB, FEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTION

A0–A15
Address Inputs for memory locations. Internal latches hold addresses during write cycles.

$\overline{CE}$ (E)
The Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.

DQ0–DQ7
Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

NC
No Connect-corresponding pin is not connected internally to the die.

$\overline{OE}$ (G)
The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

V_{CC}
Power supply for device operation. (5.0 V ± 5% or 10%)

V_{PP}
Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2$ V.

V_{SS}
Ground

$\overline{WE}$ (W)
The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

BASIC PRINCIPLES

The Am28F512 uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0 V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F512 functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F512's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F512 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Flasherase Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note: *The Flash memory array must be completely programmed to 0's prior to erasure. Refer to the Flashrite Programming Algorithm.*

1. **Erase Set-Up:** Write the Set-Up Erase command to the command register.
2. **Erase:** Write the Erase command (same as Set-Up Erase command) to the command register again. The second command initiates the erase operation. The system software routines must now time-out the erase pulse width (10 ms) prior to issuing the Erase-verify command. An integrated stop timer prevents any possibility of overerasure.
3. **Erase-Verify:** Write the Erase-verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFH data (Byte erased). After successful data verification the Erase-verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Flashrite Programming Sequence

A three step command sequence (a two-cycle Program command and one cycle Verify command) is required to program a byte of the Flash array. Refer to the Flashrite Algorithm.

1. **Program Set-Up:** Write the Set-Up Program command to the command register.
2. **Program:** Write the Program command to the command register with the appropriate Address and Data. The system software routines must now time-out the program pulse width (10 µs) prior to issuing the Program-verify command. An integrated stop timer prevents any possibility of overprogramming.
3. **Program-Verify:** Write the Program-verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified successfully, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times.

Data Protection

The Am28F512 is designed to offer protection against accidental erasure or programming, caused by spurious system level signals that may exist during power transitions. The Am28F512 powers up in its read only state. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. The device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 10 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

FUNCTIONAL DESCRIPTION

Description of User Modes

Table 1. Am28F512 User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A0	A9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A0	A9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (25H)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A0	A9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A0	A9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An < V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. *V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} +2.0 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.*
2. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.*
3. *$11.5 < V_{ID} < 13.0$ V*
4. *Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.*
5. *With V_{PP} at high voltage, the standby current is I_{CC} + I_{PP} (standby).*
6. *Refer to Table 3 for valid D_{IN} during a write operation.*
7. *All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A9 and A0 must be held at V_{IL}.*

READ ONLY MODE

$V_{PP} < V_{CC} + 2$ V
Command Register Inactive

Read

The Am28F512 functions as a read only memory when $V_{PP} < V_{CC} + 2$ V. The Am28F512 has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least t_{ACC}–t_{OE}).

Standby Mode

The Am28F512 has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), consumes less than 100 µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A PROM Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13.0 V) on address A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to $V_{CC} + 2.0$ V while using this Auto select mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the Am28F512 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F512 Auto Select Code

Type	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	25	0	0	1	0	0	1	0	1

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%

Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 3 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Am28F512 Command Definitions

	First Bus Cycle			Second Bus Cycle		
Command	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 6)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/25H
Erase Set-up/EraseWrite (Note 4)	Write	X	20H	Write	X	20H
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Program Set-up/ Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Reset (Note 6)	Write	X	FFH	Write	X	FFH

Notes:

1. *Bus operations are defined in Table 1.*
2. *RA = Address of the memory location to be read.*
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   X = Don't care.
   Addresses are latched on the falling edge of the WE pulse.
3. *RD = Data read from location RA during read operation.*
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of WE.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. *Figure 1 illustrates the Flasherase Electrical Erase Algorithm.*
5. *Figure 3 illustrates the Flashrite Programming Algorithm.*
6. *Please reference Reset Command section.*

FLASH MEMORY PROGRAM/ERASE OPERATIONS

AMD's Flasherase and Flashrite Algorithms

Flasherase Erase Sequence

Erase Set-Up/Erase Commands

Erase Set-Up

Erase Set-up is the first of a two-cycle erase command. It is a command-only operation that stages the device for bulk chip erase. The array contents are not altered with this command. 20H is written to the command register in order to perform the Erase Set-up operation.

Erase

The second two-cycle erase command initiates the bulk erase operation. You must write the Erase command (20H) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-verify) to the register.

This two step sequence of the Set-up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, chip erasure can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note: *The Flash memory device must be fully programmed to 00H data prior to erasure. This equalizes the charge on all memory cells ensuring reliable erasure.*

Erase-Verify Command

The erase operation erases all bytes of the array in parallel. After the erase operation, all bytes must be sequentially verified. The Erase-verify operation is initiated by writing A0H to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse or $\overline{CE}$ pulse, whichever occurs later. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-verify operation, the Am28F512 applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are properly erased.

Verify Next Address

You must write the Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ pulse, whichever occurs later. The process continues for each byte in the memory array until a byte does not return FFH data or all the bytes in the array are accessed and verified.

If an address is not verified to FFH data, the entire chip is erased again (refer to Erase Set-up/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The device is now ready to be programmed. At this point, the verification operation is terminated by writing a valid command (e.g. Program set-up) to the command register. Figure 1 and Table 5, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

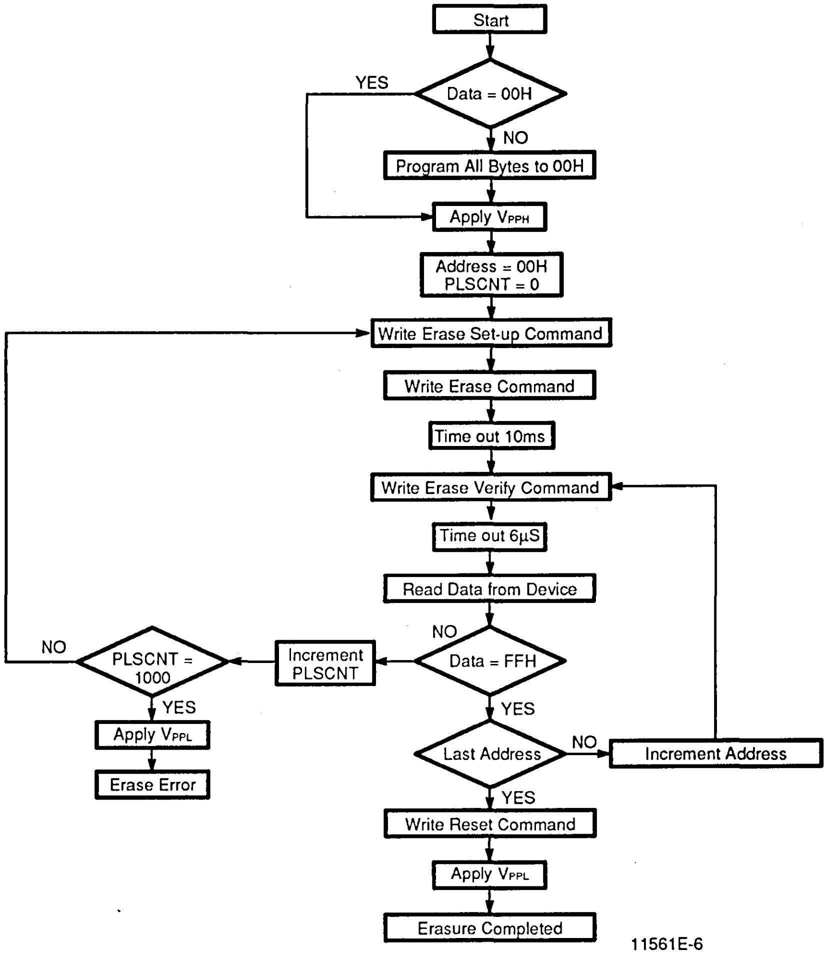


Figure 1. Flasherase Electrical Erase Algorithm

Flasherase Electrical Erase Algorithm

This Flash memory device erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the array. Erasure begins with a read of the memory contents. The Am28F512 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

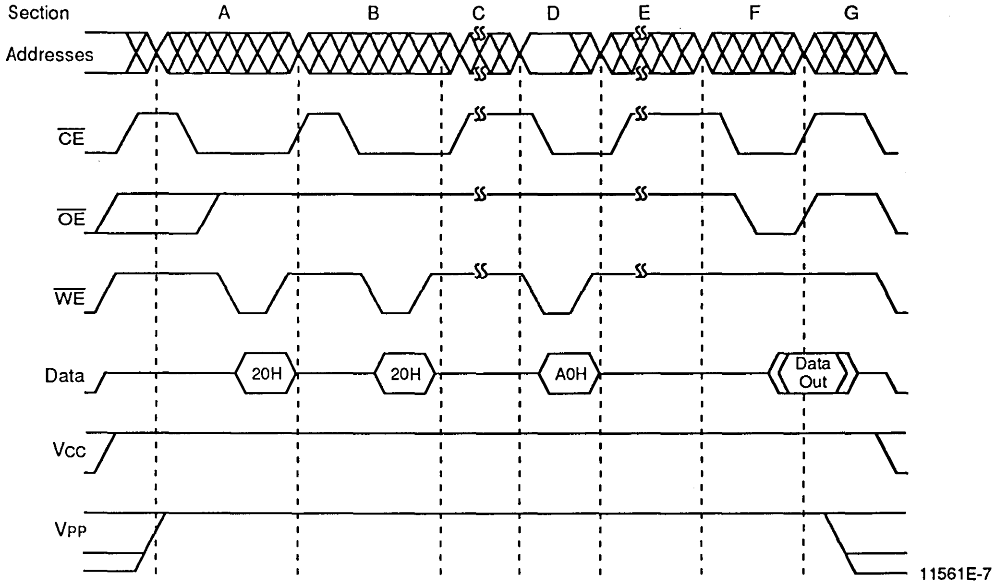
Should the device be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished using the Flashrite Programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. If a byte fails to verify, the device is erased again. With each erase operation, an increasing number of bytes verify to the erased state. Typically, devices are erased in less than 100 pulses (one second). Erase efficiency may be improved by storing the address of the last byte that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. A total of 1000 erase pulses are allowed per reprogram cycle, which corresponds to approximately 10 seconds of cumulative erase time. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 1 illustrates the electrical erase algorithm.

Table 4. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) ***Note:*** *Use Flashrite programming algorithm (Figure 3) for programming.*
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Erase Set-Up	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-Verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Reset	Data = FFH, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. *See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.*
2. *Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.*
3. *The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.*



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time-out	Write	Time-out	Read	Standby
Command	20H	20H	N/A	A0H	N/A	Compare Data	N/A
Function	Erase Set-up	Erase	Erase (10 ms)	Erase-Verify	Transition (6 µs)	Erase Verification	Proceed per Erase Algorithm

Figure 2. AC Waveforms For Erase Operations

Analysis of Erase Timing Waveform

Note: *This analysis does not include the requirement to program the entire array to 00H data prior to erasure. Refer to the Flashrite Programming algorithm.*

Erase Set-Up/Erase

This analysis illustrates the use of two-cycle erase commands (section A and B). The first erase command (20H) is a set-up command and does not affect the array data (section A). The second erase command (20H) initiates the erase operation (section B) on the rising edge of this $\overline{WE}$ pulse. All bytes of the memory array are erased in parallel. No address information is required.

The erase pulse occurs in section C.

Time-Out

A software timing routine (10 ms duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Note: *An integrated stop timer prevents any possibility of overerasure by limiting each time-out period of 10 ms.*

Erase-Verify

Upon completion of the erase software timing routine, the microprocessor must write the Erase-verify command (A0H). This command terminates the erase operation on the rising edge of the $\overline{WE}$ pulse (section D). The Erase-verify command also stages the device for data verification (section F).

After each erase operation each byte must be verified. The byte address to be verified must be supplied with the Erase-verify command (section D). Addresses are latched on the falling edge of the $\overline{WE}$ pulse.

Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operation (section E).

During Erase-verification (section F) each address that returns FFH data is successfully erased. Each address of the array is sequentially verified in this manner by repeating sections D thru F until the entire array is verified or an address fails to verify. Should an address location fail to verify to FFH data, erase the device again. Repeat sections A thru F. Resume verification (section D) with the failed address.

Each data change sequence allows the device to use up to 1,000 erase pulses to completely erase. Typically 100 erase pulses are required.

Note: *All address locations must be programmed to 00H prior to erase. This equalizes the charge on all memory cells and ensures reliable erasure.*

Flashrite Programming Sequence

Program Set-Up/Program Command

Program Set-Up

The Am28F512 is programmed byte by byte. Bytes may be programmed sequentially or at random. Program Set-up is the first of a two-cycle program command. It stages the device for byte programming. The Program Set-up operation is performed by writing 40H to the command register.

Program

Only after the program set-up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-verify command to terminate the programming operation. This two step sequence of the Set-up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte just programmed must be verified.

Write C0H into the command register in order to initiate the Program-verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-verify operation stages the device for verification of the last byte programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-verify operation, the Am28F512 applies an internally generated margin voltage to the addressed byte. A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte location. Should the byte fail to verify, reprogram (refer to Program Set-up/Program). Figure 3 and Table 5 indicate how instructions are combined with the bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Flashrite Programming Algorithm

The Am28F512 Flashrite Programming algorithm employs an interactive closed loop flow to program data byte by byte. Bytes may be programmed sequentially or at random. The Flashrite Programming algorithm uses 10 microsecond programming pulses. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 3 and Table 5 illustrate the programming algorithm.

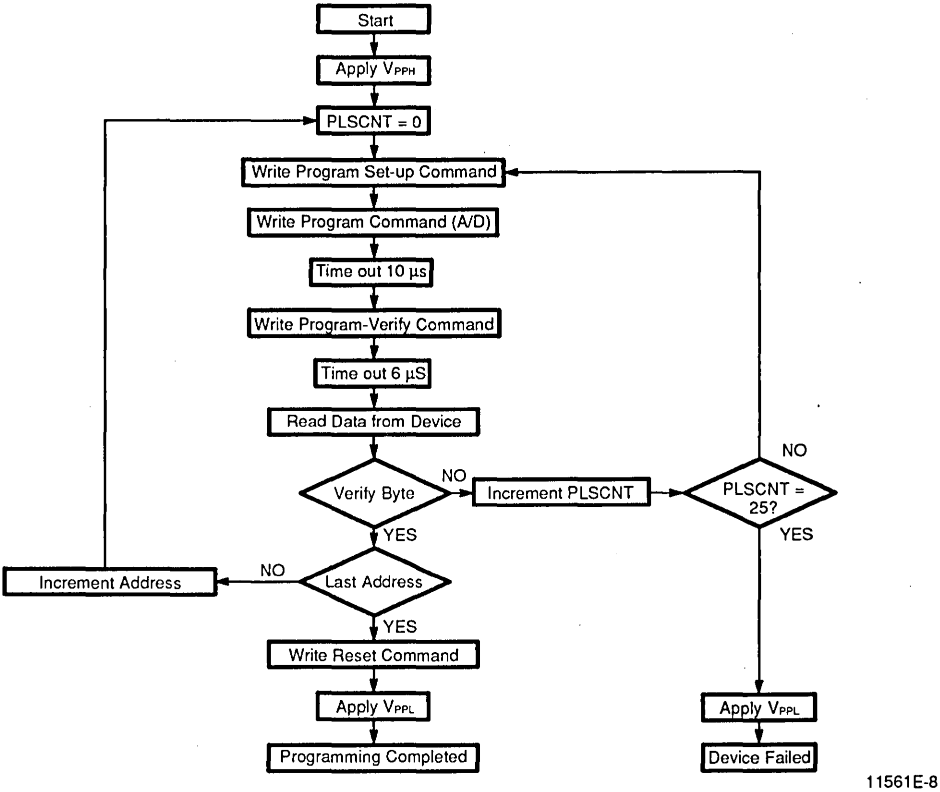


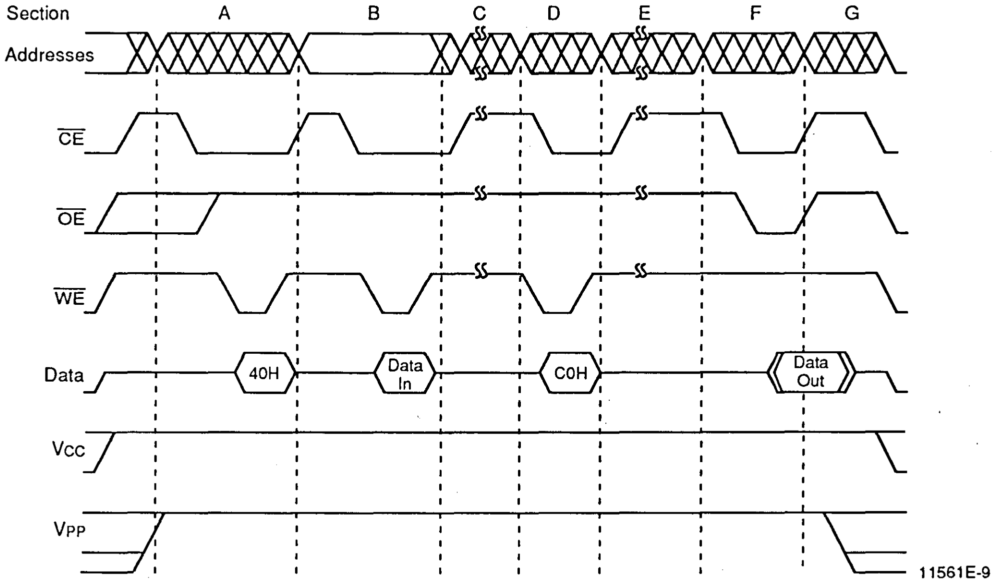
Figure 3. Flashrite Programming Algorithm

Table 5. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Program Set-Up	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Reset	Data = FFH, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. *See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.*
2. *Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.*



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time-out	Write	Time-out	Read	Standby
Command	40H	Program Address, Program Data	N/A	C0H (Stops Program)	N/A	Compare Data	N/A
Function	Program Set-up	Program Command Latch Address & Data	Program (10 µs)	Program Verify	Transition (6 µs)	Program Verification	Proceed per Programming Algorithm

Figure 4. A.C. Waveforms for Programming Operations

Analysis of Program Timing Waveforms

Program Set-Up/Program

Two-cycle write commands are required for program operations (section A and B). The first program command (40H) is a set-up command and does not affect the array data (section A). The second program command latches address and data required for programming on the falling and rising edge of $\overline{WE}$ respectively (section B). The rising edge of this $\overline{WE}$ pulse (section B) also initiates the programming pulse. The device is programmed on a byte by byte basis either sequentially or randomly.

The program pulse occurs in section C.

Time-Out

A software timing routine (10 µs duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Note: *An integrated stop timer prevents any possibility of overprogramming by limiting each time-out period of 10 µs.*

Program-Verify

Upon completion of the program timing routine, the microprocessor must write the program-verify command (C0H). This command terminates the programming operation on the rising edge of the $\overline{WE}$ pulse (section D). The program-verify command also stages the device for data verification (section F). Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operations (section E).

During program-verification (section F) each byte just programmed is read to compare array data with original program data. When successfully verified, the next desired address is programmed. Should a byte fail to verify, reprogram the byte (repeat section A thru F). Each data change sequence allows the device to use up to 25 program pulses per byte. Typically, bytes are verified within one or two pulses.

Algorithm Timing Delays

There are four different timing delays associated with the Flasherase and Flashrite algorithms:

1. The first delay is associated with the V_{PP} rise-time when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on the V_{PP}, the delay required is proportional to the number of devices being erased and the 0.1 µF/device. V_{PP} must reach its final value 100 ns before commands are executed.
2. The second delay time is the erase time pulse width (10 ms). A software timing routine should be run by the local microprocessor to time out the delay. The erase operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the erase operation. To ensure proper device operation, write the Erase-verify operation after each pulse.
3. A third delay time is required for each programming pulse width (10 µs). The programming algorithm is interactive and verifies each byte after a program pulse. The program operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the programming operation.
4. A fourth timing delay associated with both the Flasherase and Flashrite algorithms is the write recovery time (6 µs). During this time internal circuitry is changing voltage levels from the erase/ program level to those used for margin verify and read operations. An attempt to read the device during this period will result in possible false data (it may appear the device is not properly erased or programmed).

Note: *Software timing routines should be written in machine language for each of the delays. Code written in machine language requires knowledge of the appropriate microprocessor clock speed in order to accurately time each delay.*

Parallel Device Erasure

Many applications will use more than one Flash memory device. Total erase time may be minimized by implementing a parallel erase algorithm. Flash memories may erase at different rates. Therefore each device must be verified separately. When a device is completely erased and verified use a masking code to prevent further erasure. The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-Up Sequence

The Am28F512 powers-up in the Read only mode. Power supply sequencing is not required.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset command must be written two consecutive times after the set-up Program command (40H). This will reset the device to the Read mode.

Following any other Flash command write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The set-up Program command (40H) is the only command that requires a two sequence reset cycle. The first Reset command is interpreted as program data. However, FFH data is considered null data during programming operations (memory cells are only programmed from a logical "1" to "0"). The second Reset command safely aborts the programming operation and resets the device to the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the set-up Program state or not.

Programming In-System

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Auto Select Command

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F512 contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H. A read cycle from address 0001H returns the device code 25H (see Table 2). To terminate the operation, it is necessary to write another valid command, such as Reset (FFH), into the register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages .... −65°C to +150°C
Plastic Packages .... −65°C to +125°C

Ambient Temperature
with Power Applied .... −55°C to + 125°C

Voltage with Respect To Ground
All pins except A9 and V_{PP} (Note 1) −2.0 V to +7.0 V

V_{CC} (Note 1) .... −2.0 V to +7.0 V

A9 (Note 2) .... −2.0 V to +14.0 V

V_{PP} (Note 2) .... −2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ...... 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A9 and V_{PP} pins is −0.5 V. During voltage transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) .... 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) .... −40°C to +85°C

Extended (E) Devices
Case Temperature (T_C) .... −55°C to +125°C

Military (M) Devices
Case Temperature (T_C) .... −55°C to +125°C

V_{CC} Supply Voltages
V_{CC} for Am28F512–X5 .... +4.75 V to +5.25 V

V_{CC} for Am28F512–XX0 .... +4.50 V to +5.50 V

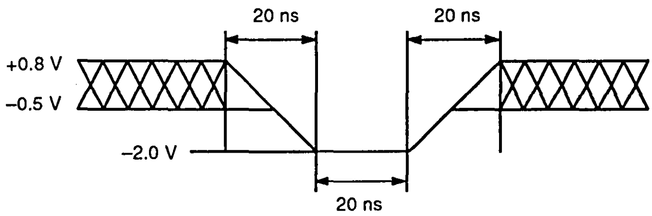
V_{PP} Supply Voltages
Read .... −0.5 V to +12.6 V

Program, Erase, and Verify ..... +11.4 V to +12.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



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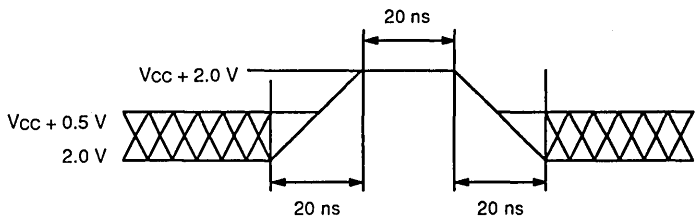
Maximum Positive Input Overshoot



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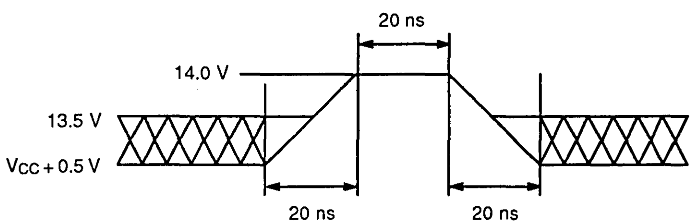
Maximum V_{PP} Overshoot



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DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1–4)

DC CHARACTERISTICS—TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IH}$		0.2	1.0	mA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, $I_{OUT} = 0$ mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress (Note 4)		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress (Note 4)		10	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			±1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	µA
		$V_{PP} = V_{PPL}$			±1.0	µA
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 5.8$ mA, $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.5$ mA, $V_{CC} = V_{CC}$ Min	2.4			V
V_{ID}	A9 Auto Select Voltage	A9 = V_{ID}	11.5		13.0	V
I_{ID}	A9 Auto Select Current	A9 = V_{ID} Max, $V_{CC} = V_{CC}$ Max		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:*** *Erase/Program are inhibited when $V_{PP} = V_{PPL}$*	0.0		V_{CC} +2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. ***Caution:*** *the Am28F512 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
2. *I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.*
3. *Maximum active power usage is the sum of I_{CC} and I_{PP}.*
4. *Not 100% tested.*

DC CHARACTERISTICS—CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{CC} + 0.5$ V		15	100	µA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ $I_{OUT} = 0$ mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress (Note 4)		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress (Note 4)		10	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			±1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	µA
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 5.8$ mA $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.5$ mA, $V_{CC} = V_{CC}$ Min	0.85 V_{CC}			V
V_{OH2}		$I_{OH} = -100$ µA, $V_{CC} = V_{CC}$ Min	V_{CC} –0.4			
V_{ID}	A9 Auto Select Voltage	A9 = V_{ID}	11.5		13.0	V
I_{ID}	A9 Auto Select Current	A9 = V_{ID} Max $V_{CC} = V_{CC}$ Max		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:*** *Erase/ Program are inhibited when $V_{PP} = V_{PPL}$*	0.0		V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. ***Caution:*** *the Am28F512 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
2. *I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.*
3. *Maximum active power usage is the sum of I_{CC} and I_{PP}.*
4. *Not 100% tested.*

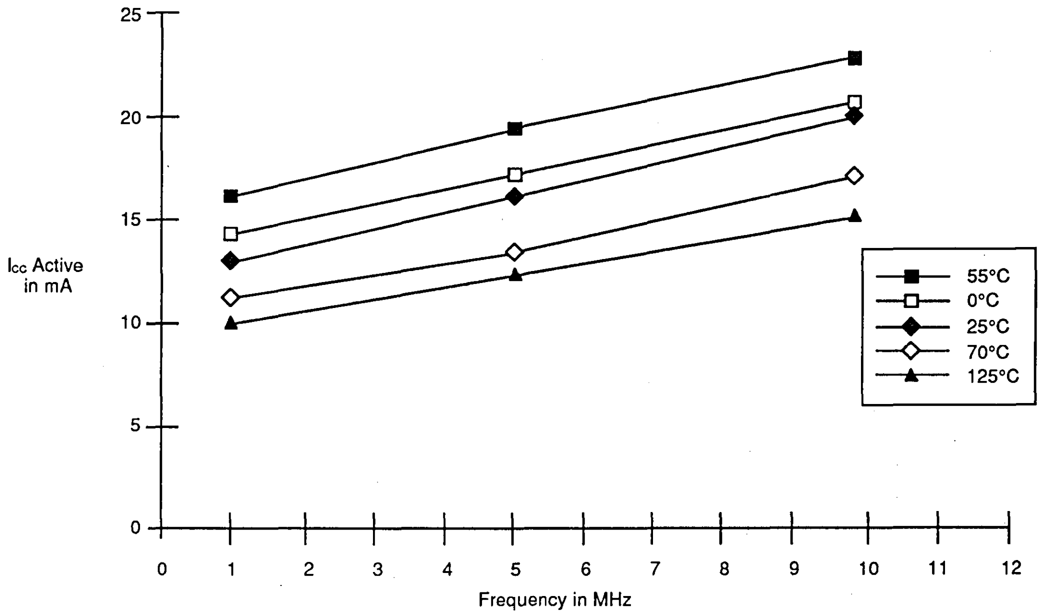

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Figure 5. Am28F512–Average I_{CC} Active vs. Frequency
V_{CC} = 5.5 V, Addressing Pattern = Minmax
Data Pattern = Checkerboard

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	8	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A = 25°C$, $f = 1.0$ MHz*

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

AC CHARACTERISTICS—Read Only Operation (Notes 1–4)

Parameter Symbols				Am28F512						
JEDEC	Standard	Parameter Description		— -75	-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)	Min	70	90	120	150	200	250	ns
			Max							
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min							
			Max	70	90	120	150	200	250	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min							
			Max	70	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min							
			Max	35	35	50	55	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z (Note 4)	Min	0	0	0	0	0	0	ns
			Max							
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z (Note 3)	Min							
			Max	20	20	30	35	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z (Note 4)	Min	0	0	0	0	0	0	ns
			Max							
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z (Note 4)	Min							
			Max	20	20	30	35	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change (Note 4)	Min	0	0	0	0	0	0	ns
			Max							
t_{WHGL}		Write Recovery Time before Read	Min	6	6	6	6	6	6	µs
			Max							
t_{VCS}		V_{CC} Set-up Time to Valid Read (Note 4)	Min	50	50	50	50	50	50	µs
			Max							

Notes:

1. *Output Load: 1 TTL gate and $C_L = 100$ pF*
   Input Rise and Fall Times: < 10 ns
   Input Pulse levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. *The Am28F512-75 amd Am28F512-95 Output Load: 1 TTL gate and $C_L = 100$ pF*
   Input Rise and Fall Times: < 10 ns
   Input Pulse levels: 0 V to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. *Guaranteed by design not tested.*
4. *Not 100% tested.*

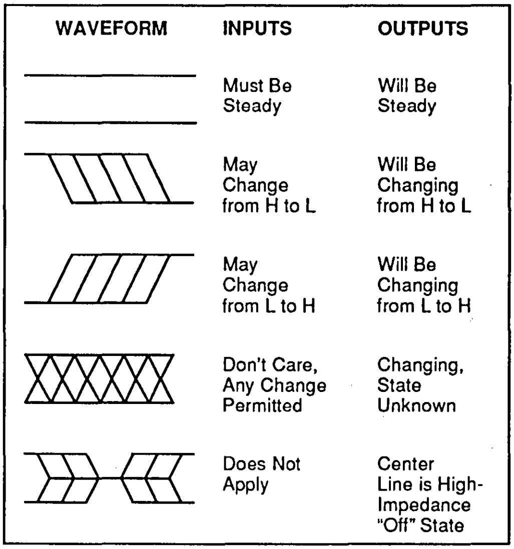
AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1– 6)

Parameter Symbols				Am28F512						
JEDEC	Standard	Parameter Description		— -75	-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 6)	Min Max	70	90	120	150	200	250	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min Max	0	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min Max	45	45	50	60	75	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min Max	45	45	50	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min Max	10	10	10	10	10	10	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	Min Max	6	6	6	6	6	6	µs
t_{GHWL}		Read Recovery Time before Write	Min Max	0	0	0	0	0	0	µs
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	Min Max	0	0	0	0	0	0	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min Max	0	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min Max	45	45	50	60	60	60	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min Max	20	20	20	20	20	20	ns
t_{WHWH1}		Duration of Programming Operation (Note 4)	Min Max	10	10	10	10	10	10	µs
t_{WHWH2}		Duration of Erase Operation (Note 4)	Min Max	9.5	9.5	9.5	9.5	9.5	9.5	ms
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	100	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	50	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 6)	Min Max	500	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 10% V_{PPL} (Note 6)	Min Max	500	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 6)	Min Max	100	100	100	100	100	100	ns

Notes:

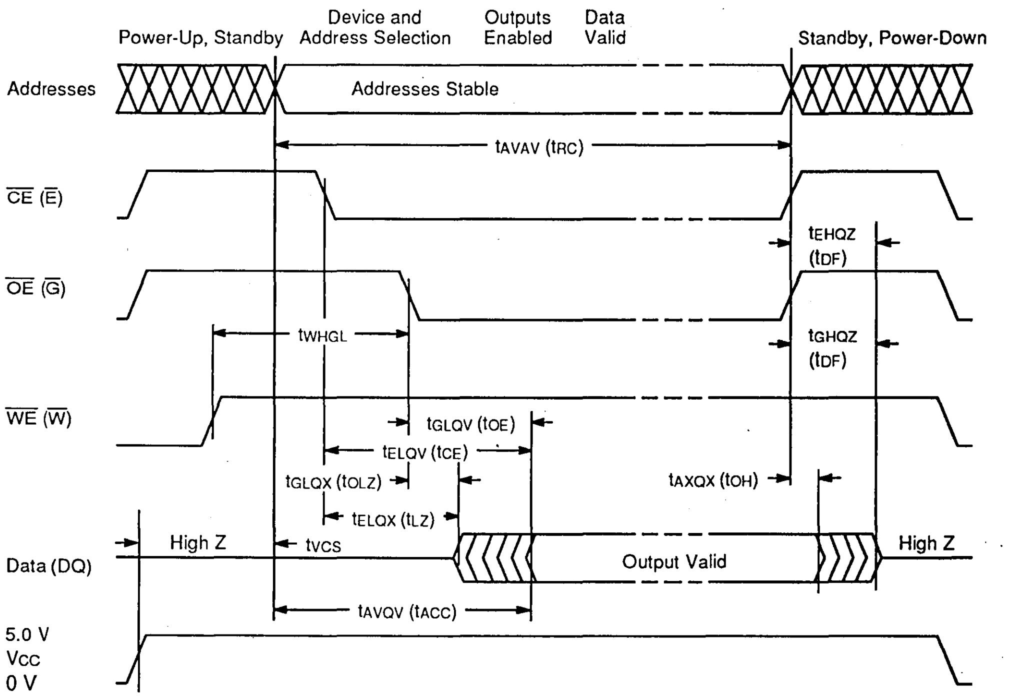
1. *Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.*
2. *All devices except Am28F512-75 and Am28F512-95 Input Rise and Fall times: < 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V.*
3. *Am28F512-75 and Am28F512-95 Input Rise and Fall times: < 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V*
4. *Maximum pulse widths not required because the on-chip program/erase stop timer will terminate the pulse widths internally on the device.*
5. *Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the Write Pulse Width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.*
6. *Not 100% tested.*

KEY TO SWITCHING WAVEFORMS



KS000010

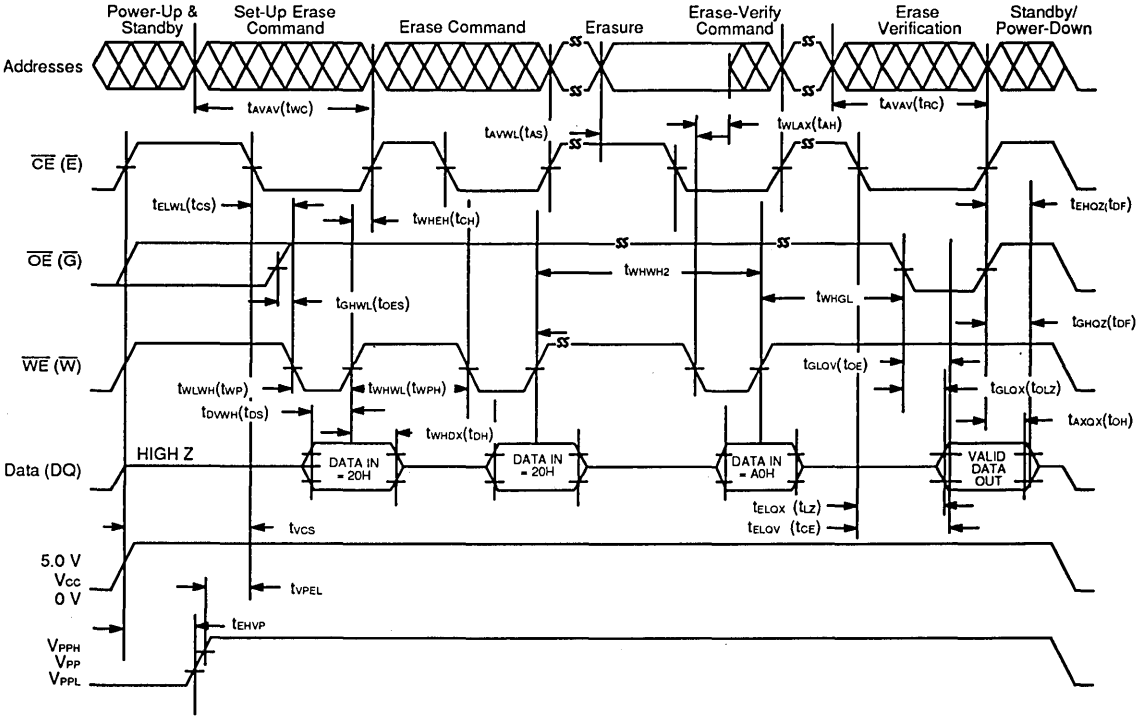
SWITCHING WAVEFORMS



11561E-14

Figure 6. AC Waveforms for Read Operations

SWITCHING WAVEFORMS



11561E-15

Figure 7. AC Waveforms for Erase Operations

SWITCHING WAVEFORMS

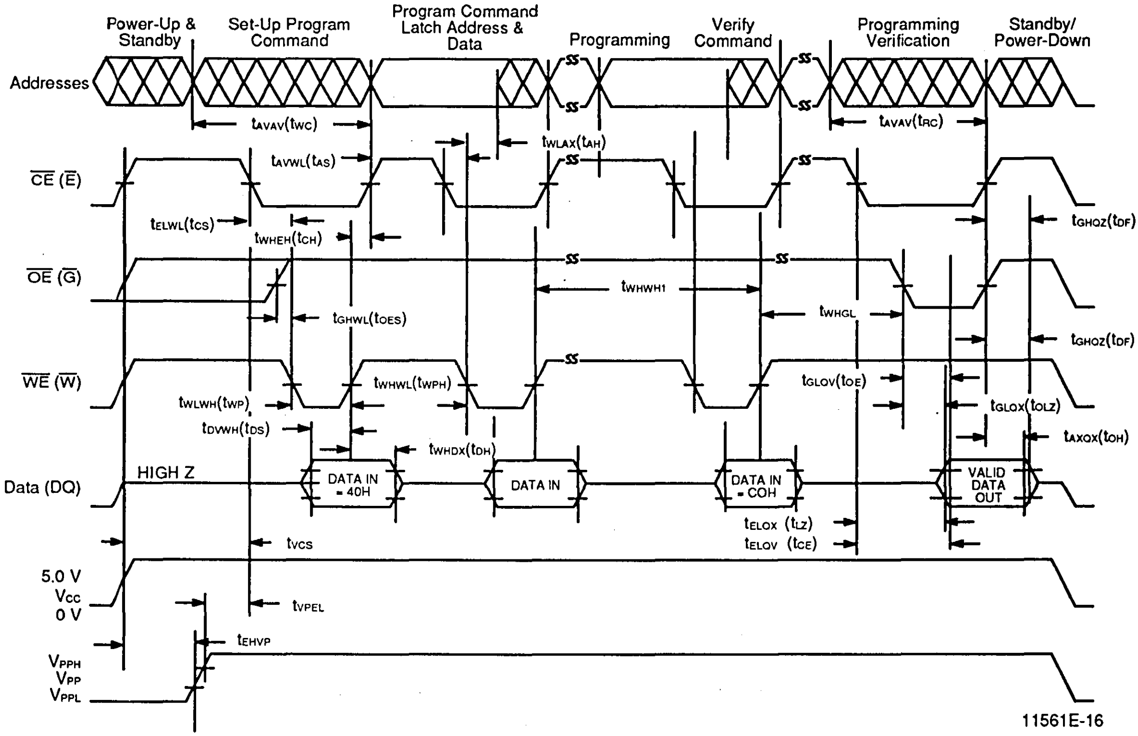
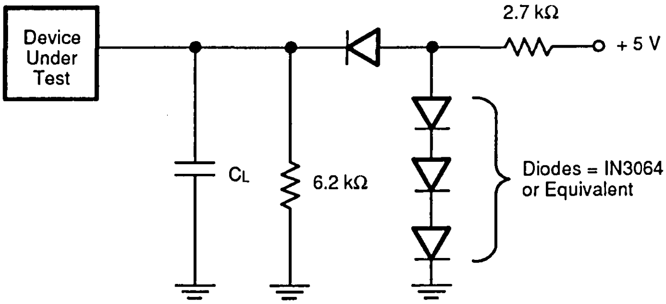


Figure 8. AC Waveforms for Programming Operations

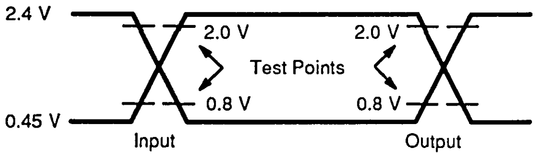
SWITCHING TEST CIRCUIT



11561E-17

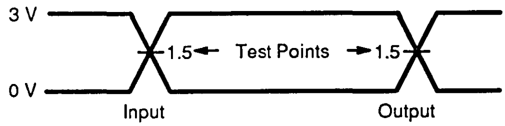
C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORMS



All Devices Except Am28F512-75 and Am28F512-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are < 10 ns.



For Am28F512-75 and Am28F512-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are < 10 ns.

11561E-18

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max (Note 3)		
Chip Erase Time		1 (Note 1)	10 (Note 2)	S	Excludes 00H programming prior to erasure
Chip Programming Time		1 (Note 1)	6	S	Excludes system-level overhead
Write/Erase Cycles	10,000			Cycles	

Notes:

1. *25°C, 12 V V_{PP}*
2. *The Flasherase/Flashrite algorithms allows for 60 second erase time for military temperature range operations.*
3. *Maximum time specified is lower than worst case. Worst case is derived from the Flasherase/Flashrite pulse count (Flasherase = 1000 max and Flashrite = 25 max). Typical worst case for program and erase operations is significantly less than the actual device limit.*

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A9 and V_{PP})	–1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	–1.0 V	V_{CC} + 1.0 V
Current	–100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

DATA SHEET REVISION SUMMARY FOR Am28F512

Data sheet is Final now, and not Preliminary.

Product Selector Guide

Added -75 ns speed grade at 5% V_{CC} Tolerance.

Ordering Information – Standard Products

Added -75 ns speed grade to the Valid Combinations table. Removed DC package from Am28F512-75, -90, and -95. Removed DC, DI, DE and DEB packages from Am28F512 from -120, -150, and -200. Removed Package Type D.

Ordering Information – APL Products

This page was removed.

Erase, Program and Read Mode – Write Operations

Removed Command Register Table and Bit assignments.

Erase, Program and Read Mode – Read Command

The statement requiring a 6 µs wait before accessing the first addressed location was removed.

Table 3 – Am28F512 Command Definitions

The note describing a 6 µs wait before accessing the first addressed location was removed.

Flasherase Erase Sequence – Erase Verify Command

The address latched also depends on the falling edge of $\overline{CE}$, whichever happens later.

Flasherase Erase Sequence – Verify Next Address

The new address latched also depends on the falling edge of $\overline{CE}$. whichever happens later.

Auto Select Command

Programming In-System

Titles for each section were switched.

Programming In-System

It is necessary to write a valid command, such as Reset, into the register.

DC Characteristics – TTL/NMOS Compatible

Added Note 4. Those characteristics are not 100% tested.

DC Characteristics – CMOS Compatible

Added Note 4. Those characteristics are not 100% tested.

AC Characteristics – Read Only Operation (Notes 1 and 2)

Added -75 timings. Added Am28F512-75 to Note 2.

AC Characteristics – Write/Erase/Program Operations (Notes 1–5)

Added Am28F512-75 to Notes 2 and 3.

Switching Test Waveforms

For Test Point figures also apply to Am28F512-75.

PRELIMINARY

Am28F512A

512 Kilobit (65,536 x 8-Bit) CMOS 12.0 Volt, Bulk Erase Flash Memory with Embedded Algorithms

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 70 ns maximum access time
- **CMOS low power consumption**
  - 30 mA maximum active current
  - 100 µA maximum standby current
  - No data retention power consumption
- **Compatible with JEDEC-standard byte-wide 32-Pin EPROM pinouts**
  - 32-pin DIP
  - 32-pin PLCC
  - 32-pin TSOP
  - 32-pin LCC
- **100,000 write/erase cycles minimum**
- **Write and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from −1 V to V_{CC} +1 V**
- **Embedded Erase Electrical Bulk Chip-Erase**
  - Two seconds typical chip-erase including pre-programming
- **Embedded Program**
  - 14 µs typical byte-program including time-out
  - One second typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell
- **Embedded algorithms for completely self-timed write/erase operations**

GENERAL DESCRIPTION

The Am28F512A is a 512K bit Flash memory organized as 64K bytes of 8 bits each. AMD's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The Am28F512A is packaged in 32-pin PDIP, PLCC, and TSOP versions. The device is also offered in the ceramic LCC package. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers. The Am28F512A is erased when shipped from the factory.

The standard Am28F512A offers access times as fast as 70 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F512A has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F512A uses a command register to manage this functionality, while maintaining a JEDEC Flash standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming.

AMD's Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F512A uses a 12.0 V ± 5% V_{PP} supply to perform the erase and programming functions.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from −1 V to V_{CC} +1 V.

Embedded Program

The Am28F512A is byte programmable using the Embedded Programming algorithm. The Embedded Programming algorithm does not require the system to time-out or verify the data programmed. The typical room temperature programming time of the Am28F512A is one second.

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.
Publication# 18880 Rev. A Amendment/0
Issue Date: March 1994

GENERAL DESCRIPTION

Embedded Erase

The entire chip is bulk erased using the Embedded Erase algorithm. The Embedded Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internal to the device. Typical erasure at room temperature is accomplished in one second.

AMD's Am28F512A is entirely pin and software compatible with AMD Am28F020A, Am28F010A, and Am28F256A Flash memories.

Embedded Programming Algorithm vs. Flashrite Programming Algorithm

The Flashrite Programming algorithm requires the user to write a program set-up command, a program command (program data and address), and a program verify command followed by a read and compare operation. The user is required to time the programming pulse width in order to issue the program verify command. An integrated stop timer prevents any possibility of overprogramming. Upon completion of this sequence the data is read back from the device and compared by the user with the data intended to be written; if there is not a match, the sequence is repeated until there is a match or the sequence has been repeated 25 times.

AMD's Embedded Programming algorithm requires the user to only write a program set-up command and a program command (program data and address). The device automatically times the programming pulse width, provides the program verify and counts the number of sequences. A status bit, $\overline{\text{Data}}$ Polling, provides feedback to the user as to the status of the programming operation.

Embedded Erase Algorithm vs. Flasherase Erase Algorithm

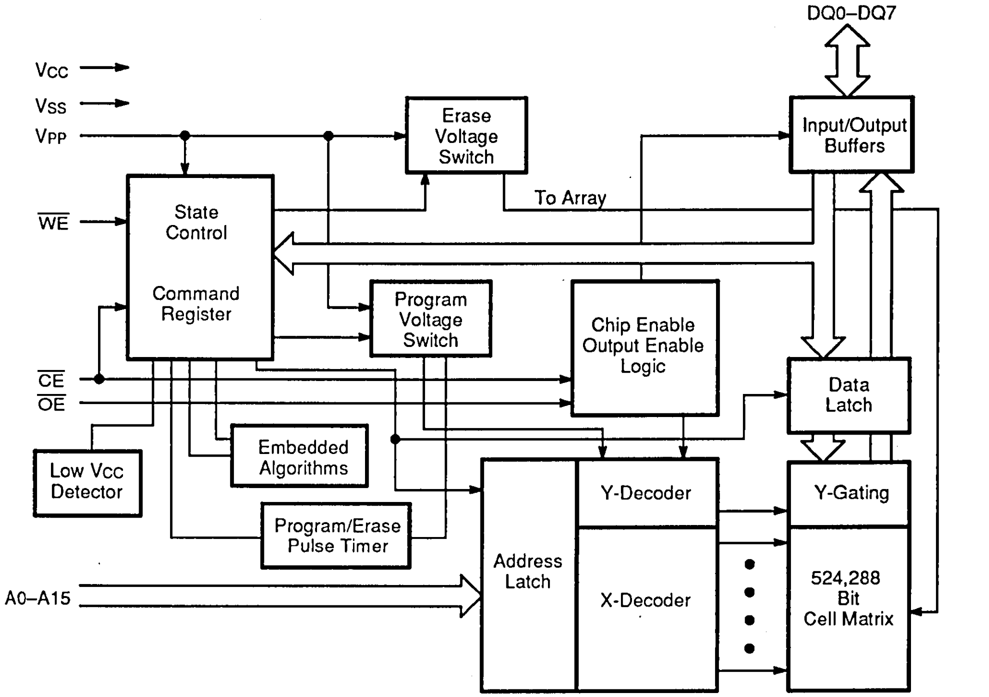
The Flasherase Erase algorithm requires the device to be completely programmed prior to executing an erase command. To invoke the erase operation the user writes an erase set-up command, an erase command, and an erase verify command. The user is required to time the erase pulse width in order to issue the erase verify command. An integrated stop timer prevents any possibility of overerasure. Upon completion of this sequence the data is read back from the device and compared by the user with erased data. If there is not a match, the sequence is repeated until there is a match or the sequence has been repeated 1,000 times.

AMD's Embedded Erase algorithm requires the user to only write an erase set-up command and erase command. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verify and counts the number of sequences. A status bit, $\overline{\text{Data}}$ Polling, provides feedback to the user as to the status of the erase operation.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F512A is designed to support either $\overline{\text{WE}}$ or $\overline{\text{CE}}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$ whichever occurs last. Data is latched on the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$ whichever occurs first. To simplify the following discussion, the $\overline{\text{WE}}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{\text{WE}}$ signal.

AMD's Flash technology combines years of EPROM and EEPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F512A electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

BLOCK DIAGRAM



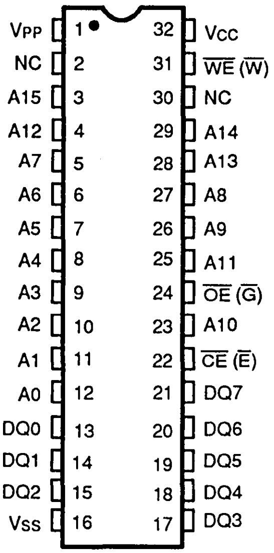
18880A-1

PRODUCT SELECTOR GUIDE

Family Part No.	Am28F512A				
Ordering Part No: ±10% Vcc Tolerance		-90	-120	-150	-200
±5% Vcc Tolerance	-75	-95			
Max Access Time (ns)	70	90	120	150	200
$\overline{CE}$ ($\overline{E}$) Access (ns)	70	90	120	150	200
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	35	50	55	55

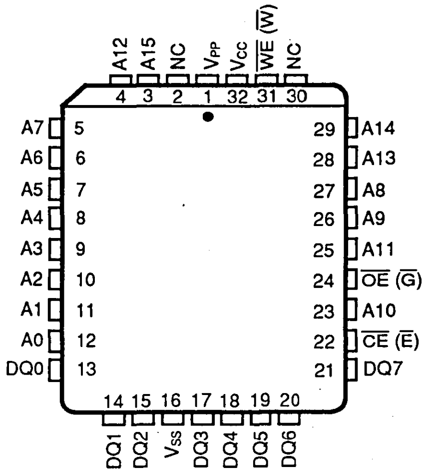
CONNECTION DIAGRAMS

DIP



18880A-2

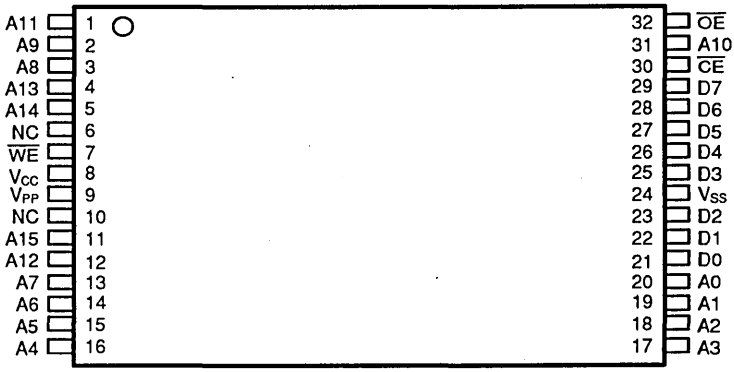
PLCC*



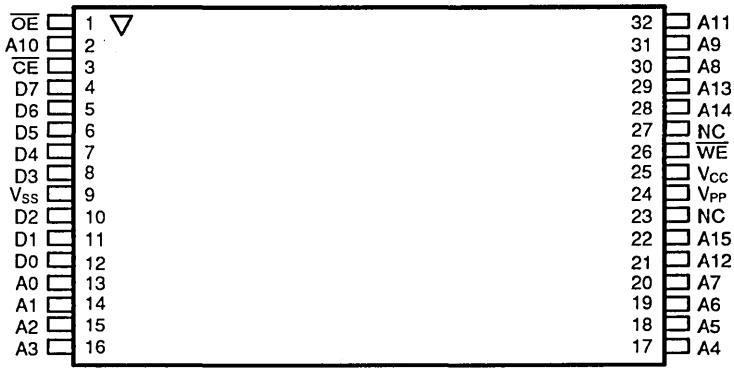
18880A-3

Note: *Pin 1 is marked for orientation.*
**Also available in LCC.*

CONNECTION DIAGRAMS



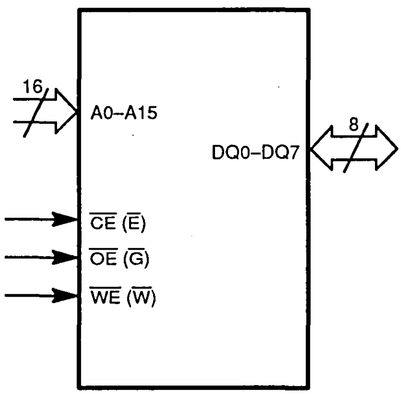
28F512A Standard Pinout



28F512A Reverse Pinout 18880A-4

28F512A 64K x 8 Flash Memory in 32-Lead TSOP

LOGIC SYMBOL



18880A-5

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

AM28F512A -75 J C B

OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-In

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended (–55°C to +125°C)

PACKAGE TYPE
P = 32-Pin Plastic DIP (PD 032)
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)
E = 32-Pin TSOP Standard Pinout (TS 032)
F = 32-Pin TSOP Reverse Pinout (TSR 032)
L = 32-Pin Rectangular Leadless Chip Carrier (CLR 032)

SPEED
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am28F512A
512Kbit (64K x 8-Bit) CMOS Flash Memory with Embedded Algorithms

Valid Combinations	
AM28F512A-75 AM28F512A-90 AM28F512A-95	PC, JC, EC, FC, LC
AM28F512A-120 AM28F512A-150 AM28F512A-200	PC, PI, JC, JI, PE, PEB, JE, JEB, EC, FC, EI, FI, EE, FE, EEB, FEB, LC, LI, LE, LEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PIN DESCRIPTION

A0–A15
Address Inputs for memory locations. Internal latches hold addresses during write cycles.

$\overline{CE}$ (E)
The Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.

DQ0–DQ7
Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

NC
No Connect-corresponding pin is not connected internally to the die.

$\overline{OE}$ (G)
The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

V_{CC}
Power supply for device operation. (5.0 V ± 5% or 10%)

V_{PP}
Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \le V_{CC} + 2$ V.

V_{SS}
Ground

$\overline{WE}$ (W)
The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

BASIC PRINCIPLES

The Am28F512A uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0 V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F512A functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F512A's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F512A is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Embedded Erase Algorithm

AMD now makes erasure extremely simple and reliable. The Embedded Erase algorithm requires the user to only write an erase set-up command and erase command. The device will automatically pre-program and verify the entire array. The device automatically times the erase pulse width, provides the erase verify and counts the number of sequences. A status bit, $\overline{\text{Data}}$ Polling, provides feedback to the user as to the status of the erase operation.

Embedded Programming Algorithm

AMD now makes programming extremely simple and reliable. The Embedded Programming algorithm requires the user to only write a program set-up command and a program command. The device automatically times the programming pulse width, provides the program verify and counts the number of sequences. A status bit, $\overline{\text{Data}}$ Polling, provides feedback to the user as to the status of the programming operation.

Data Protection

The Am28F512A is designed to offer protection against accidental erasure or programming, caused by spurious system level signals that may exist during power transitions. The Am28F512A powers up in its read only state. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. The device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 10 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

FUNCTIONAL DESCRIPTION

Description of User Modes

Table 1. Am28F512A User Bus Operations

Operation		$\overline{CE}$ (E)	$\overline{OE}$ (G)	$\overline{WE}$ (W)	V_{PP} (Note 1)	A0	A9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A0	A9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-Select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-Select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (AEH)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A0	A9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A0	A9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} \leq V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An < V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. *V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC}$ +2.0 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.*
2. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.*
3. *$11.5 \leq V_{ID} \leq 13.0$ V*
4. *Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.*
5. *With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).*
6. *Refer to Table 3 for valid D_{IN} during a write operation.*
7. *All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A9 and A0 must be held at V_{IL}.*

READ ONLY MODE

$V_{PP} < V_{CC} + 2$ V
Command Register Inactive

Read

The Am28F512A functions as a read only memory when $V_{PP} < V_{CC} + 2$ V. The Am28F512A has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC} - t_{OE}$).

Standby Mode

The Am28F512A has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), consumes less than 100 µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1 mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A PROM Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13.0 V) on address A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to $V_{CC} + 2.0$ V while using this Auto select mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the Am28F512A these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F512A Auto Select Code

Type	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	AE	1	0	1	0	1	1	1	0

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%

Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 3 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Am28F512A Command Definitions

	First Bus Cycle			Second Bus Cycle		
Command	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 4)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/AEH
Embedded Erase Set-up/ Embedded Erase	Write	X	30H	Write	X	30H
Embedded Program Set-up/ Embedded Program	Write	X	10H or 50H	Write	PA	PD
Reset (Note 4)	Write	X	FFH	Write	X	FFH

Notes:

1. *Bus operations are defined in Table 1.*
2. *RA = Address of the memory location to be read.*
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   X = Don't care.
3. *RD = Data read from location RA during read operation.*
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
4. *Please reference Reset Command section.*

FLASH MEMORY PROGRAM/ERASE OPERATIONS

AMD's Embedded Program and Erase Operations

Embedded Erase Algorithm

The automatic chip erase does not require the device to be entirely pre-programmed prior to executing the Embedded set-up erase command and Embedded erase command. Upon executing the Embedded erase command the device automatically will program and verify the entire memory for an all zero data pattern. The system is not required to provide any controls or timing during these operations.

When the device is automatically verified to contain an all zero pattern, a self-timed chip erase and verify begin. The erase and verify operation are complete when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to Read mode. The system is not required to provide any control or timing during these operations.

When using the Embedded Erase algorithm, the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard erase verify command is used.

The Embedded Erase Set-Up command is a command only operation that stages the device for automatic electrical erasure of all bytes in the array. Embedded Erase Set-Up is performed by writing 30H to the command register.

To commence automatic chip erase, the command 30H must be written again to the command register. The automatic erase begins on the rising edge of the $\overline{WE}$ and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to Read mode.

Figure 5 and Table 4 illustrate the Embedded Erase algorithm, a typical command string and bus operation.

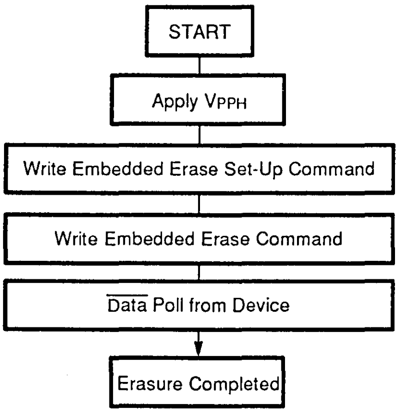


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Figure 5. Embedded Erase Algorithm

Table 4. Embedded Erase Algorithm

Bus Operations	Command	Comments
Standby		Wait for VPP Ramp to VPPH (1)
Write	Embedded Erase Set-Up Command	Data = 30H
Write	Embedded Erase Command	Data = 30H
Read		$\overline{\text{Data}}$ Polling to Verify Erasure
Standby		Compare Output to FFH
Read		Available for Read Operations

Note:

1. *See DC Characteristics for value of VPPL. The VPP power supply can be hard-wired to the device or switchable. When VPP is switched, VPPL may be ground, no connect with a resistor tied to ground, or less than Vcc + 2.0 V. Refer to Functional Description.*

Embedded Programming Algorithm

The Embedded Program Set-Up is a command only operation that stages the device for automatic programming. Embedded Program Set-Up is performed by writing 10H or 50H to the command register.

Once the Embedded Set-Up Program operation is performed, the next $\overline{\text{WE}}$ pulse causes a transition to an active programming operation. Addresses are latched on the falling edge of $\overline{\text{CE}}$ or $\overline{\text{WE}}$ pulse, whichever happens later. Data is latched on the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$, whichever happens first. The rising edge of $\overline{\text{WE}}$ also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin. The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to Read mode.

Figure 6 and Table 5 illustrate the Embedded Program algorithm, a typical command string, and bus operation.

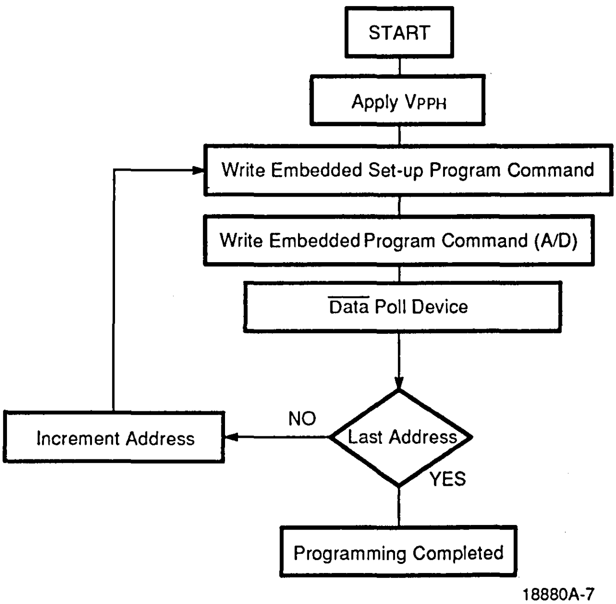


Figure 6. Embedded Programming Algorithm

Table 5. Embedded Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Program Set-Up Command	Data = 10H or 50H
Write	Embedded Program Command	Valid Address/Data
Read		$\overline{\text{Data}}$ Polling to Verify Completion
Read		Available for Read Operations

Note:

1. *See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Functional Description. Device is either powered-down, erase inhibit or program inhibit.*

Write Operation Status

$\overline{\text{Data}}$ Polling—DQ7

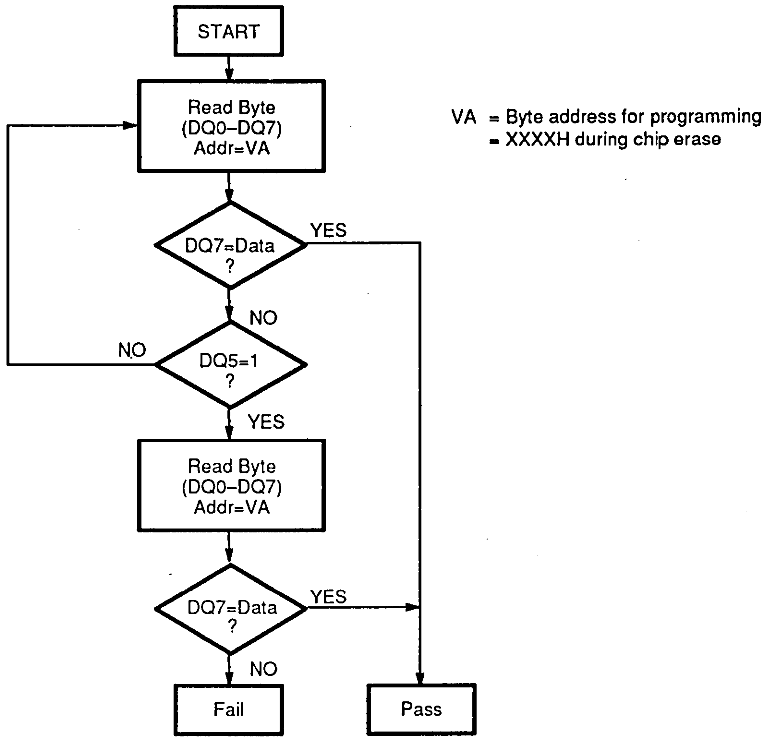
The Am28F512A features $\overline{\text{Data}}$ Polling as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Programming algorithm is in operation, an attempt to read the device at a valid address will produce the complement of expected Valid data on DQ7. Upon completion of the Embedded Program algorithm an attempt to read the device at a valid address will produce Valid data on DQ7. The $\overline{\text{Data}}$ Polling feature is valid after the rising edge of the second $\overline{\text{WE}}$ pulse of the two write pulse sequence.

While the Embedded Erase algorithm is in operation, DQ7 will read "0" until the erase operation is completed. Upon completion of the erase operation, the data on DQ7 will read "1." The $\overline{\text{Data}}$ Polling feature is valid after the rising edge of the second $\overline{\text{WE}}$ pulse of the two Write pulse sequence.

The $\overline{\text{Data}}$ Polling feature is only active during Embedded Programming or erase algorithms.

See Figures 7a and 8a for the $\overline{\text{Data}}$ Polling timing specifications and diagrams. $\overline{\text{Data}}$ Polling is the standard method to check the write operation status, however, an alternative method is available using Toggle Bit.



Note:

1. DQ7 is rechecked even if DQ5="1" because DQ7 may change simultaneously with DQ5 or after DQ5.

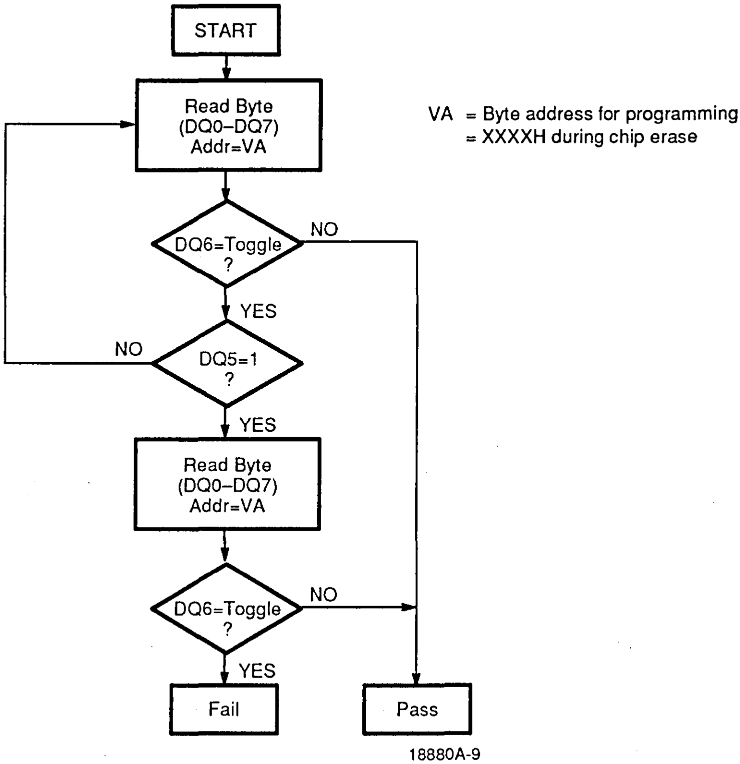
Figure 7a. $\overline{\text{Data}}$ Polling Algorithm

Toggle Bit—DQ6

The Am28F512A also features a "Toggle Bit" as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

Successive attempts to read data from the device at a valid address, while the Embedded Program algorithm is in progress, or at any address while the Embedded Erase algorithm is in progress, will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase algorithm is completed, DQ6 will stop toggling to indicate the completion of either Embedded operation. Only on the next read cycle will valid data be obtained. The toggle bit is valid after the rising edge of the first $\overline{WE}$ pulse of the two write pulse sequence, unlike $\overline{\text{Data}}$ Polling which is valid after the rising edge of the second $\overline{WE}$ pulse. This feature allows the user to determine if the device is partially through the two write pulse sequence.

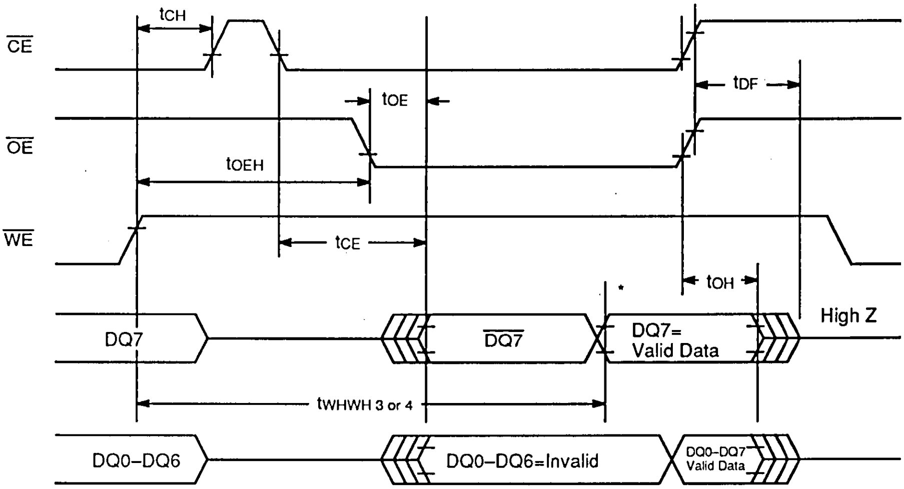
See Figures 7b and 8b for the Toggle Bit timing specifications and diagrams.



Note:

1. *DQ6 is rechecked even if DQ5="1" because DQ6 may stop toggling at the same time as DQ5 changing to "1".*

Figure 7b. Toggle Bit Algorithm



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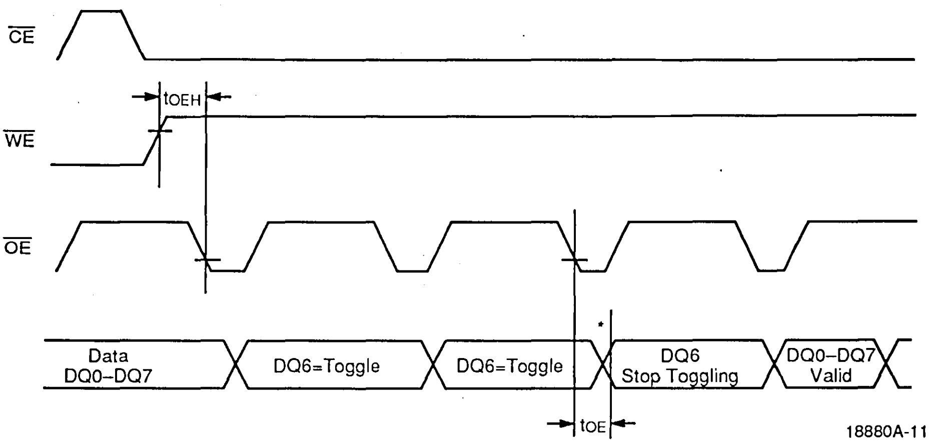
Note:
**DQ7=Valid Data (The device has completed the Embedded operation).*

Figure 8a. AC Waveforms for $\overline{\text{Data}}$ Polling During Embedded Algorithm Operations

DQ5
Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits. This is a failure condition and the device may not be used again (internal pulse count exceeded). Under these conditions DQ5 will produce a "1." The program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the device under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in Table 1.



Note:

**DQ6 stops toggling (The device has completed the Embedded operation).*

Figure 8b. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

Parallel Device Erasure

The Embedded Erase algorithm greatly simplifies parallel device erasure. Since the erase process is internal to the device, a single erase command can be given to multiple devices concurrently. By implementing a parallel erase algorithm, total erase time may be minimized.

Note that the Flash memories may erase at different rates. If this is the case, when a device is completely erased, use a masking code to prevent further erasure (over-erasure). The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-Up Sequence

The Am28F512A powers-up in the Read only mode. Power supply sequencing is not required.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset must be written two consecutive times after the Set-up Program command (10H or 50H). This will reset the device to the Read mode.

Following any other Flash command, write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The Set-up Program command (10H or 50H) is the only command that requires a two-sequence reset cycle. The first Reset command is interpreted as program data. However, FFH data is considered as null data during programming operations (memory cells are only programmed from a logical "1" to "0"). The second Reset command safely aborts the programming operation and resets the device to the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the Set-up Program state or not.

In-System Programming Considerations

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the circuit board.

Auto Select Command

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. In order to correctly program any Flash memories in-system, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F512A contains an Auto Select operation to supplement traditional PROM programming methodologies. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H (AMD). A read cycle from address 0001H returns the device code AE (see Table 2). To terminate the operation, it is necessary to write another valid command, such as Reset (FFH), into the register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages .... –65°C to +150°C
Plastic Packages .... –65°C to +125°C

Ambient Temperature
with Power Applied .... –55°C to + 125°C

Voltage with Respect To Ground
All pins except A9 and V_{PP}
(Note 1) .... –2.0 V to +7.0 V

V_{CC} (Note 1) .... –2.0 V to +7.0 V

A9 (Note 2) .... –2.0 V to +14.0 V

V_{PP} (Note 2) .... –2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ...... 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A9 and V_{PP} pins is –0.5 V. During voltage transitions, A9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) .... 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) .... –40°C to +85°C

Extended (E) Devices
Case Temperature (T_C) .... –55°C to +125°C

Military (M) Devices
Case Temperature (T_C) .... –55°C to +125°C

V_{CC} Supply Voltages
V_{CC} for Am28F512A-X5 .... +4.75 V to +5.25 V

V_{CC} for Am28F512A-XX0 .... +4.50 V to +5.50 V

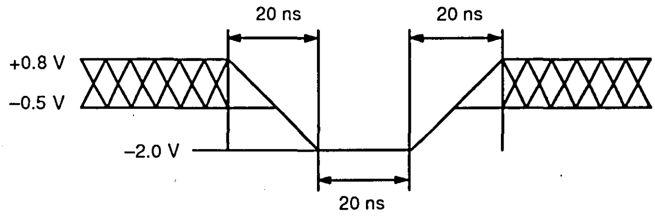
V_{PP} Supply Voltages
Read .... –0.5 V to +12.6 V

Program, Erase, and Verify ..... +11.4 V to +12.6 V

Operating ranges define those limits between which the funtionality of the device is guaranteed.

MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



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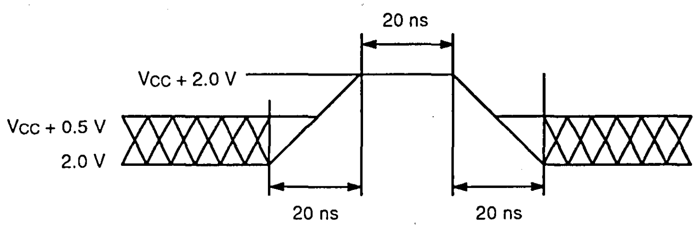
Maximum Positive Input Overshoot



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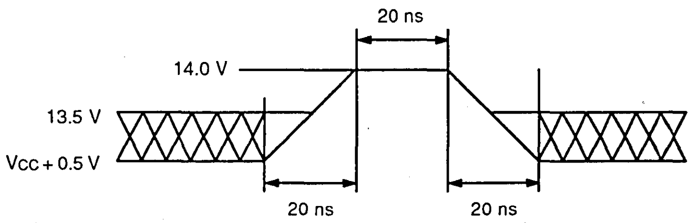
Maximum V_{PP} Overshoot



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DC CHARACTERISTICS over operating range unless otherwise specified (Notes 1–4)

DC CHARACTERISTICS-TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{IH}$		0.2	1.0	mA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ $I_{OUT} = 0$ mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress (Note 4)		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress (Note 4)		10	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			±1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	µA
		$V_{PP} = V_{PPL}$			±1.0	
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 5.8$ mA $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.5$ mA $V_{CC} = V_{CC}$ Min	2.4			V
V_{ID}	A9 Auto Select Voltage	$A9 = V_{ID}$	11.5		13.0	V
I_{ID}	A9 Auto Select Current	$A9 = V_{ID}$ Max $V_{CC} = V_{CC}$ Max		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:*** *Erase/Program are inhibited when* $V_{PP} = V_{PPL}$	0.0		V_{CC} +2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. ***Caution:*** *the Am28F512A must not be removed from (or inserted into) a socket when* V_{CC} *or* V_{PP} *is applied.*
2. I_{CC1} *is tested with* $\overline{OE} = V_{IH}$ *to simulate open outputs.*
3. *Maximum active power usage is the sum of* I_{CC} *and* I_{PP}.
4. *Not 100% tested.*

DC CHARACTERISTICS—CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS}			± 1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}			± 1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{CC} + 0.5$ V		15	100	µA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ $I_{OUT} = 0$ mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress (Note 4)		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress (Note 4)		10	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			± 1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	µA
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 5.8$ mA $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.5$ mA, $V_{CC} = V_{CC}$ Min	0.85 V_{CC}			V
V_{OH2}		$I_{OH} = -100$ µA, $V_{CC} = V_{CC}$ Min	V_{CC} –0.4			
V_{ID}	A9 Auto Select Voltage	A9 = V_{ID}	11.5		13.0	V
I_{ID}	A9 Auto Select Current	A9 = V_{ID} Max $V_{CC} = V_{CC}$ Max		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:*** *Erase/Program are inhibited when $V_{PP} = V_{PPL}$*	0.0		V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. ***Caution:*** *the Am28F512A must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
2. *I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.*
3. *Maximum active power usage is the sum of I_{CC} and I_{PP}.*
4. *Not 100% tested.*

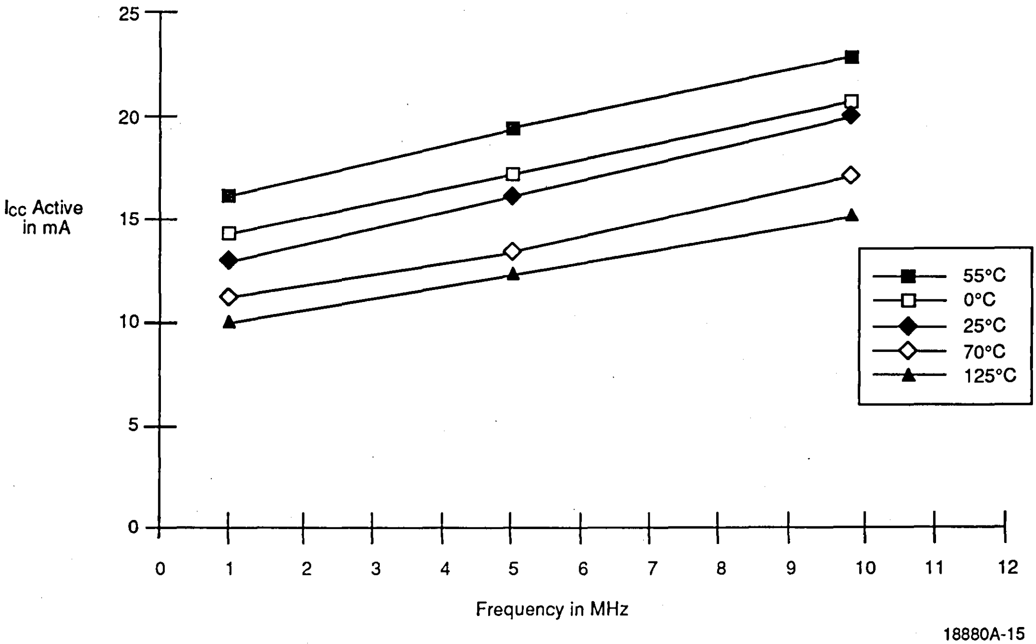


Figure 9. Am28F512A – Average I_{CC} Active vs. Frequency
V_{CC} = 5.5 V, Addressing Pattern = Minmax
Data Pattern = Checkerboard

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	8	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A = 25°C$, $f = 1.0$ MHz*

SWITCHING CHARACTERISTICS over operating range unless otherwise specified
AC CHARACTERISTICS—Read Only Operation (Notes 1–4)

Parameter Symbols JEDEC	Parameter Symbols Standard	Parameter Description		Am28F512A —/-75	-90/-95	-120/—	-150/—	-200/—	-250/—	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)	Min	70	90	120	150	200	250	ns
			Max							
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min							
			Max	70	90	120	150	200	250	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min							
			Max	70	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min							
			Max	35	35	50	55	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z (Note 4)	Min	0	0	0	0	0	0	ns
			Max							
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z (Note 3)	Min							
			Max	20	20	30	35	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z (Note 4)	Min	0	0	0	0	0	0	ns
			Max							
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z (Note 4)	Min							
			Max	20	20	30	35	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change (Note 4)	Min	0	0	0	0	0	0	ns
			Max							
t_{WHGL}		Write Recovery Time before Read	Min	6	6	6	6	6	6	µs
			Max							
t_{VCS}		V_{CC} Set-up Time to Valid Read (Note 4)	Min	50	50	50	50	50	50	µs
			Max							

Notes:

1. *Output Load: 1 TTL gate and $C_L = 100$ pF*
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0.45 to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. *The Am28F512A-75 and Am28F512A-95 Output Load: 1 TTL gate and $C_L = 100$ pF*
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0 V to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. *Guaranteed by design not tested.*
4. *Not 100% tested.*

AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1–6)

Parameter Symbols JEDEC	Parameter Symbols Standard	Parameter Description		Am28F512A — -75	-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 6)	Min Max	70	90	120	150	200	250	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min Max	0	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min Max	45	45	50	60	75	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min Max	45	45	50	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min Max	10	10	10	10	10	10	ns
t_{OEH}		Output Enable Hold Time for Embedded Algorithm only (See Figure 8)	Min Max	10	10	10	10	10	10	ns
t_{GHWL}		Read Recovery Time before Write	Min Max	0	0	0	0	0	0	µs
t_{ELWLE}	t_{CSE}	Chip Enable Embedded Algorithm Setup Time	Min Max	20	20	20	20	20	20	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min Max	0	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min Max	45	45	50	60	60	60	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min Max	20	20	20	20	20	20	ns
t_{WHWH3}		Embedded Programming Operation (Note 4)	Min Max	14	14	14	14	14	14	µs
t_{WHWH4}		Embedded Erase Operation (Note 5)	Typ Max	5	5	5	5	5	5	s
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	100	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	50	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 6)	Min Max	500	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 90% V_{PPL} (Note 6)	Min Max	500	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 6)	Min Max	100	100	100	100	100	100	ns

Notes:

1. *Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.*
2. *All devices except Am28F512A-75 and Am28F512A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V*
3. *Am28F512A-75 and Am28F512A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V*
4. *Embedded Program Operation of 14 µs consists of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.*
5. *Embedded erase operation of 5 sec consists of 4 sec array pre-programming time and one sec array erase time. This is a typical time for one embedded erase operation.*
6. *Not 100% tested.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS

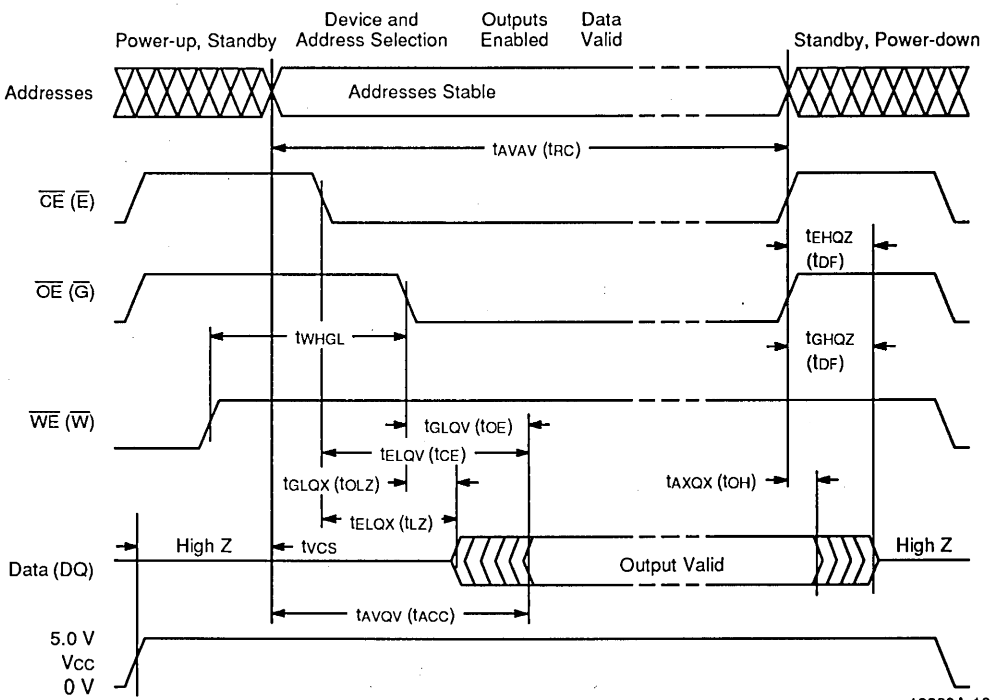
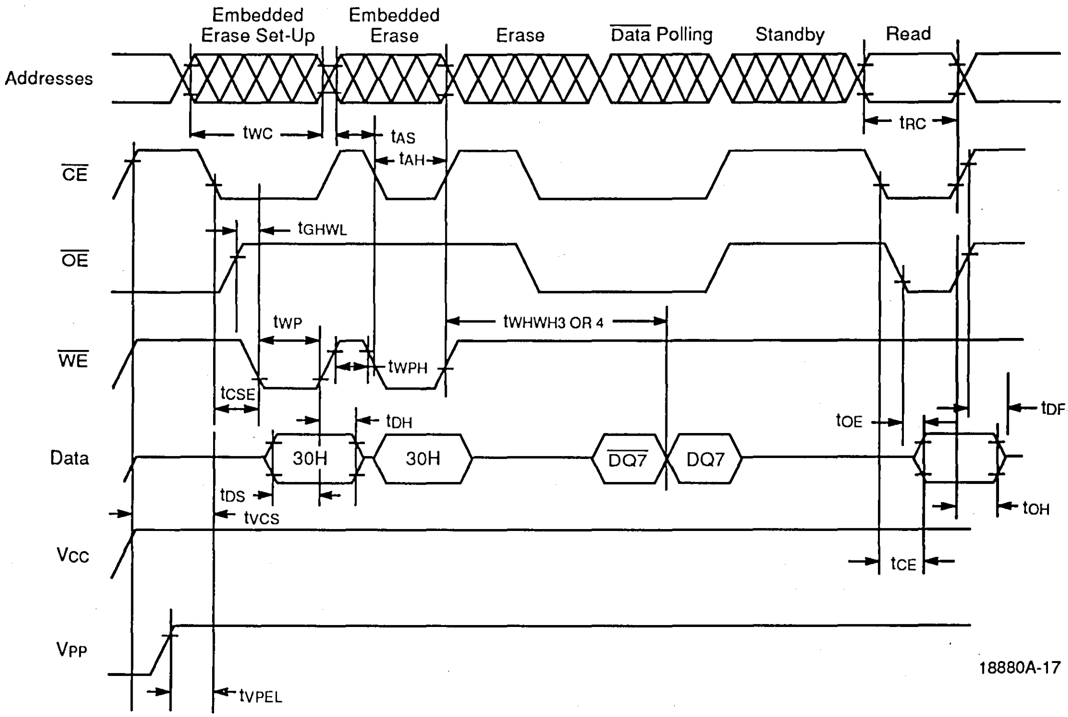


Figure 10. AC Waveforms for Read Operations

SWITCHING WAVEFORMS

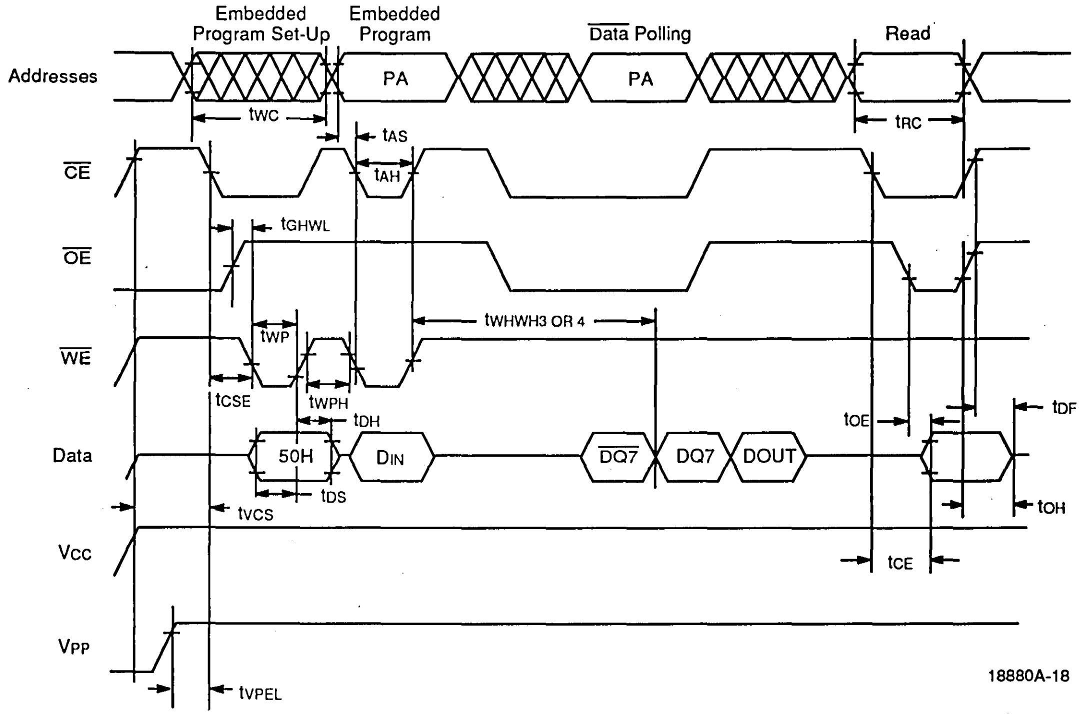


Note:

1. $\overline{DQ7}$ is the output of the complement of the data written to the device.

Figure 11. AC Waveforms for Embedded Erase Operation

SWITCHING WAVEFORMS



Notes:

1. *DIN is data input to the device.*
2. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
3. *DOUT is the output of the data written to the device.*

Figure 12. AC Waveforms for Embedded Programming Operation

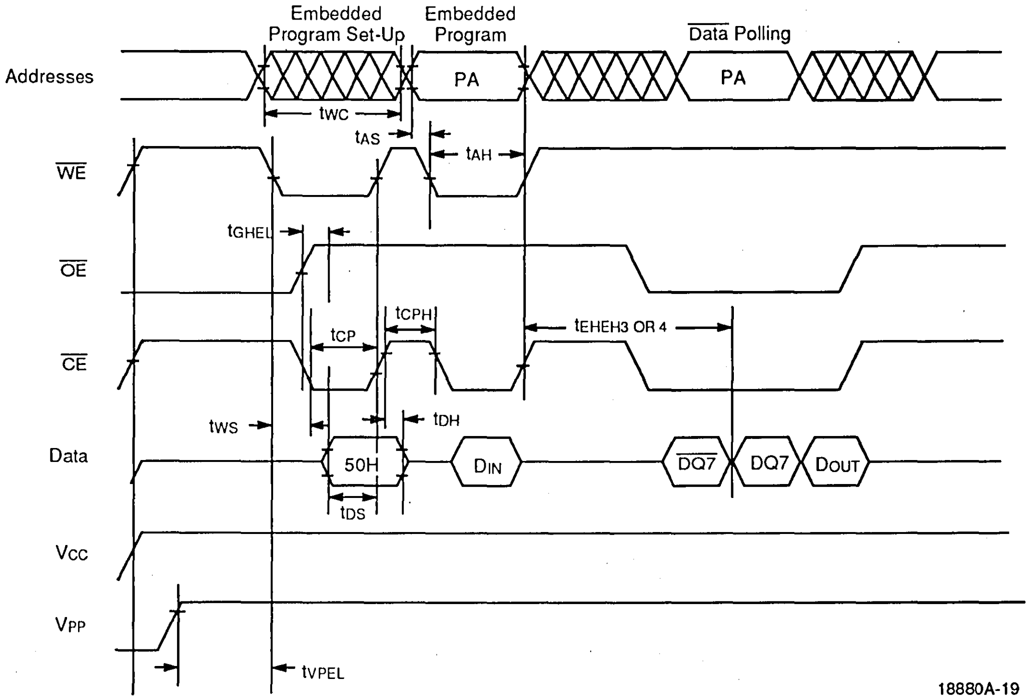
AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1–6) Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols JEDEC	Standard	Parameter Description		Am28F512A — -75	-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 6)	Min Max	70	90	120	150	200	250	ns
t_{AVEL}	t_{AS}	Address Set-Up Time	Min Max	0	0	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min Max	45	45	50	60	75	75	ns
t_{DVEH}	t_{DS}	Data Set-Up Time	Min Max	45	45	50	50	50	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min Max	10	10	10	10	10	10	ns
t_{OEH}		Output Enable Hold Time for Embedded Algorithm only (See Figure 8)	Min Max	10	10	10	10	10	10	ns
t_{GHEL}		Read Recovery Time Before Write	Min Max	0	0	0	0	0	0	µs
t_{WLEL}	t_{WS}	WE Set-Up Time by $\overline{CE}$	Min Max	0	0	0	0	0	0	ns
t_{EHWK}	t_{WH}	WE Hold Time	Min Max	0	0	0	0	0	0	ns
t_{ELEH}	t_{CP}	Write Pulse Width	Min Max	65	65	70	80	80	80	ns
t_{EHEL}	t_{CPH}	Write Pulse Width HIGH	Min Max	20	20	20	20	20	20	ns
t_{EHEH3}		Embedded Programming Operation (Note 4)	Min Max	14	14	14	14	14	14	µs
t_{EHEH4}		Embedded Erase Operation (Note 5)	Min Max	3	3	3	3	3	3	s
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	100	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	50	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 6)	Min Max	500	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 90% V_{PPL} (Note 6)	Min Max	500	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 6)	Min Max	100	100	100	100	100	100	ns

Notes:

1. *Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.*
2. *All devices except Am28F512A-75 and Am28F512A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V*
3. *Am28F512A-75 and Am28F512A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V*
4. *Embedded Program Operation of 14 µs consists of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.*
5. *Embedded erase operation of 5 sec consists of 4 sec array pre-programming time and one sec array erase time. This is a typical time for one embedded erase operation.*
6. *Not 100% tested.*

SWITCHING WAVEFORMS

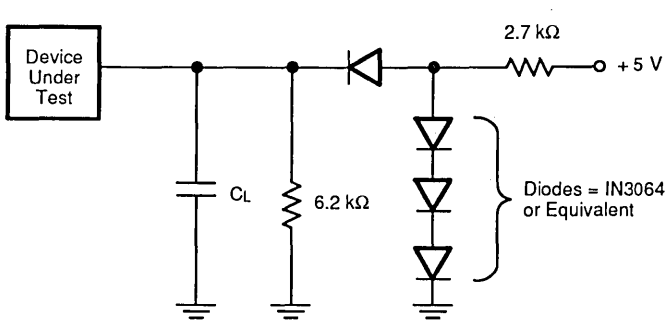


Notes:

1. *D_{IN} is data input to the device.*
2. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
3. *D_{OUT} is the output of the data written to the device.*

Figure 13. AC Waveforms for Embedded Programming Operation Using $\overline{CE}$ Controlled Writes

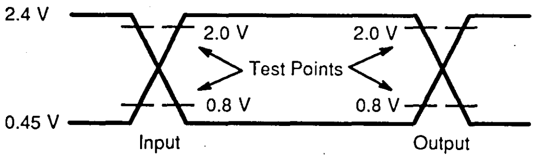
SWITCHING TEST CIRCUIT



18880A-20

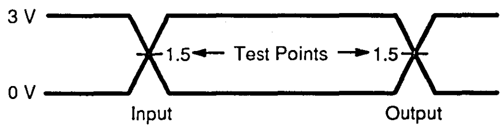
C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORMS



All Devices Except Am28F512A-75 and Am28F512A-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are < 10 ns.



For Am28F512A-75 and Am28F512A-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are < 10 ns.

18880A-21

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits Min	Limits Typ	Limits Max (Note 3)	Unit	Comments
Chip Erase Time		1 (Note 1)	10 (Note 2)	s	Excludes 00H programming prior to erasure
Chip Programming Time		1 (Note 1)	7	s	Excludes system-level overhead
Write/Erase Cycles	100,000			Cycles	
Byte Program Time		14		µs	
			96 (Note 4)	ms	

Notes:

1. *25°C, 12 V V_{PP}*
2. *The Embedded algorithm allows for 60 second erase time for military temperature range operations.*
3. *Maximum time specified is lower than worst case. Worst case is derived from the Embedded Algorithm internal counter which allows for a maximum 6000 pulses for both program and erase operations. Typical worst case for program and erase is significantly less than the actual device limit.*
4. *Typical worst case = 84 µs. DQ5 = "1" only after a byte takes longer than 96 ms to program.*

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A9 and V_{PP})	−1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	−1.0 V	V_{CC} + 1.0 V
Current	−100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

FINAL

Am28F010

1 Megabit (131,072 x 8-Bit) CMOS 12.0 Volt, Bulk Erase Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 90 ns maximum access time
- **CMOS Low power consumption**
  - 30 mA maximum active current
  - 100 µA maximum standby current
  - No data retention power consumption
- **Compatible with JEDEC-standard byte-wide 32-Pin EPROM pinouts**
  - 32-pin DIP
  - 32-pin PLCC
  - 32-pin TSOP
  - 32-pin LCC
- **10,000 write/erase cycles minimum**
- **Write and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from −1 V to V_{CC} +1 V**
- **Flasherase Electrical Bulk Chip-Erase**
  - One second typical chip-erase
- **Flashrite Programming**
  - 10 µs typical byte-program
  - Two seconds typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell
- **Automatic write/erase pulse stop timer**

GENERAL DESCRIPTION

The Am28F010 is a 1 Megabit Flash memory organized as 128K bytes of 8 bits each. AMD's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The Am28F010 is packaged in 32-pin PDIP, PLCC, and TSOP versions. The device is also offered in the ceramic DIP and LCC packages. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers. The Am28F010 is erased when shipped from the factory.

The standard Am28F010 offers access times as fast as 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F010 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F010 uses a command register to manage this functionality, while maintaining a JEDEC Flash Standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

AMD's Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F010 uses a 12.0 V ± 5% V_{PP} supply to perform the Flasherase and Flashrite algorithms.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from −1 V to V_{CC} +1 V.

The Am28F010 is byte programmable using 10 µs programming pulses in accordance with AMD's Flashrite programming algorithm. The typical room temperature programming time of the Am28F010 is two seconds. The entire chip is bulk erased using 10 ms erase pulses according to AMD's Flasherase alrogithm. Typical erasure at room temperature is accomplished in less than one second. The windowed package and the 15–20 minutes required for EPROM erasure using ultra-violet light are eliminated.

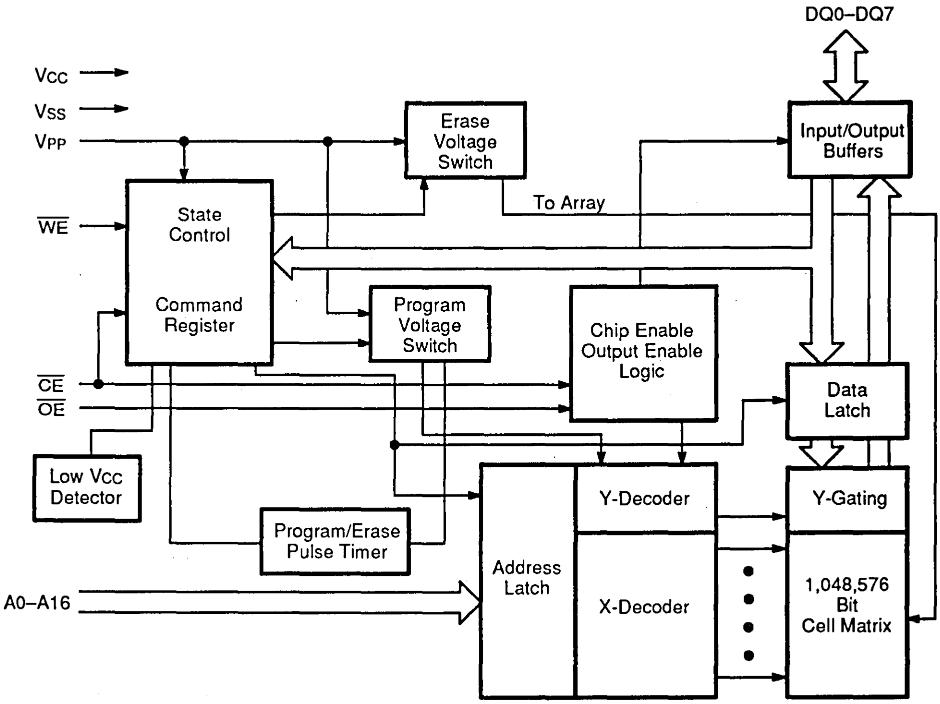
Publication# 11559 Rev. F Amendment/0
Issue Date: March 1994

GENERAL DESCRIPTION

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F010 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

AMD's Flash technology combines years of EPROM and EEPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F010 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

BLOCK DIAGRAM



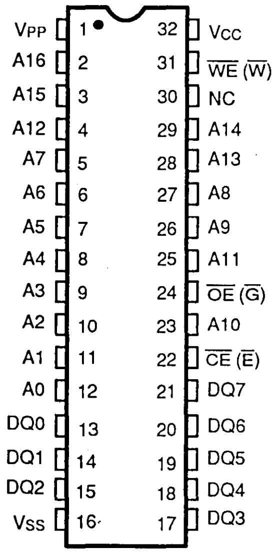
11559F-1

PRODUCT SELECTOR GUIDE

Family Part No.:	Am28F010				
Ordering Part No.: ±10% Vcc Tolerance	-90	-120	-150	-200	-250
±5% Vcc Tolerance	-95				
Max Access Time (ns)	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	50	55	55	55

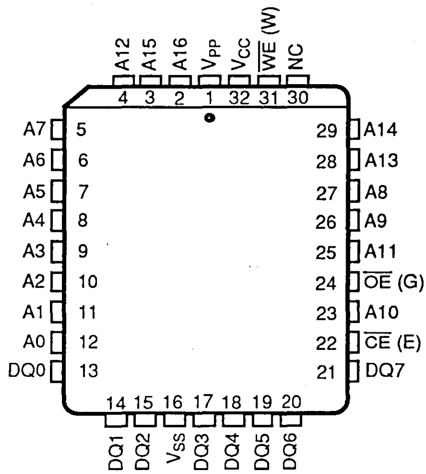
CONNECTION DIAGRAMS

DIP



11559F-2

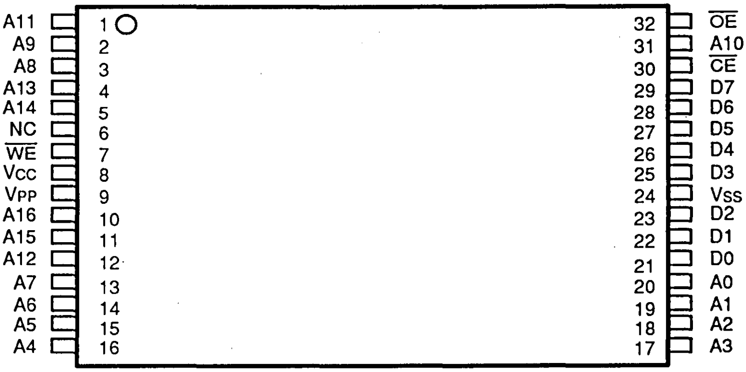
PLCC*



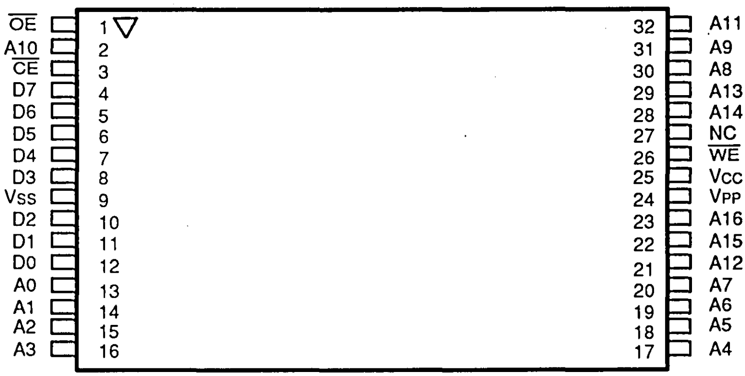
11559F-3

Note: *Pin 1 is marked for orientation.*
**Also available in LCC.*

TSOP PACKAGES



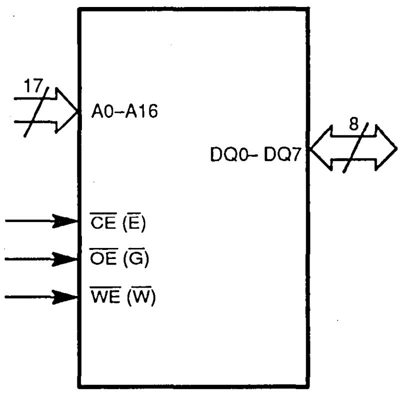
28F010 Standard Pinout



28F010 Reverse Pinout 11559F-4

28F010 128K x 8 Flash Memory in 32-Lead TSOP

LOGIC SYMBOL



11559F-5

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

AM28F010 -95 J C B

OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-In

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to + 85°C)
E = Extended (–55°C to + 125°C)

PACKAGE TYPE
P = 32-Pin Plastic DIP (PD 032)
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)
D = 32-Pin Ceramic DIP (CD 032)
L = 32-Pin Rectangular Ceramic Leadless Chip Carrier (CLR 032)
E = 32-Pin TSOP Standard Pinout (TS 032)
F = 32-Pin TSOP Reverse Pinout (TSR 032)

SPEED
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am28F010
1 Megabit (128K x 8-Bit) CMOS Flash Memory

Valid Combinations	
AM28F010-90 AM28F010-95	PC, JC, DC, LC, EC, FC
AM28F010-120 AM28F010-150 AM28F010-200	PC, PI, PE, PEB, JC, JI, JE, JEB, DC, DI, DE, DEB, LC, LI, LE, LEB, EC, FC, EI, FI, EE, FE, EEB, FEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

AM28F010 -120 /B X A

LEAD FINISH
A = Hot Solder Dip

PACKAGE TYPE
X = 32-Pin Ceramic DIP (CD 032)
U = 32-Pin Rectangular Ceramic Leadless Chip Carrier (CLR 032)

DEVICE CLASS
/B = Class B

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am28F010
1 Megabit (128K x 8-Bit) CMOS Flash Memory

Valid Combinations	
AM28F010-120	/BXA, /BUA
AM28F010-150	
AM28F010-200	
AM78F010-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

A0–A16
Address Inputs for memory locations. Internal latches hold addresses during write cycles.

$\overline{CE}$ (E)
The Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.

DQ0–DQ7
Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

NC
No Connect-corresponding pin is not connected internally to the die.

$\overline{OE}$ (G)
The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

V_{CC}
Power supply for device operation. (5.0 V ± 5% or 10%)

V_{PP}
Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2$ V.

V_{SS}
Ground

$\overline{WE}$ (W)
The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

BASIC PRINCIPLES

The Am28F010 uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0 V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F010 functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F010's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F010 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Flasherase Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note: *The Flash memory array must be completely programmed to 0's prior to erasure. Refer to the Flashrite Programming Algorithm.*

1. **Erase Set-Up:** Write the Set-up Erase command to the command register.
2. **Erase:** Write the Erase command (same as Set-up Erase command) to the command register again. The second command initiates the erase operation. The system software routines must now time-out the erase pulse width (10 ms) prior to issuing the Erase-verify command. An integrated stop timer prevents any possibility of overerasure.
3. **Erase-Verify:** Write the Erase-verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFH data (Byte erased). After successful data verification the Erase-verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Flashrite Programming Sequence

A three step command sequence (a two-cycle Program command and one cycle Verify command) is required to program a byte of the Flash array. Refer to the Flashrite Algorithm.

1. **Program Set-Up:** Write the Set-up Program command to the command register.
2. **Program:** Write the Program command to the command register with the appropriate Address and Data. The system software routines must now time-out the program pulse width (10 µs) prior to issuing the Program-verify command. An integrated stop timer prevents any possibility of overprogramming.
3. **Program-Verify:** Write the Program-verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified successfully, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times.

Data Protection

The Am28F010 is designed to offer protection against accidental erasure or programming, caused by spurious system level signals that may exist during power transitions. The Am28F010 powers up in its read only state. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. The device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 10 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

FUNCTIONAL DESCRIPTION

Description of User Modes

Table 1. Am28F010 User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A0	A9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A0	A9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (A7H)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A0	A9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A0	A9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An < V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. *V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} +2.0 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.*
2. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.*
3. *$11.5 < V_{ID} < 13.0$ V*
4. *Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.*
5. *With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).*
6. *Refer to Table 3 for valid D_{IN} during a write operation.*
7. *All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A9 and A0 must be held at V_{IL}.*

READ ONLY MODE

$V_{PP} < V_{CC} + 2$ V
Command Register Inactive

Read

The Am28F010 functions as a read only memory when $V_{PP} < V_{CC} + 2$ V. The Am28F010 has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC}-t_{OE}$).

Standby Mode

The Am28F010 has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), consumes less than 100 µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1 mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A PROM Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13.0 V) on address A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A_0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to V_{CC} + 2.0 V while using this Auto select mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the Am28F010 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F010 Auto Select Code

Type	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	A7	1	0	1	0	0	1	1	1

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%

Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 3 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Am28F010 Command Definitions

	First Bus Cycle			Second Bus Cycle		
Command	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 6)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/A7H
Erase Set-up/Erase Write (Note 4)	Write	X	20H	Write	X	20H
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Program Set-up/ Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Reset (Note 6)	Write	X	FFH	Write	X	FFH

Notes:

1. *Bus operations are defined in Table 1.*
2. *RA = Address of the memory location to be read.*
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   X = Don't care.
   Addresses are latched on the falling edge of the WE pulse.
3. *RD = Data read from location RA during read operation.*
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of WE.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. *Figure 1 illustrates the Flasherase Electrical Erase Algorithm.*
5. *Figure 3 illustrates the Flashrite Programming Algorithm.*
6. *Please reference Reset Command section.*

FLASH MEMORY PROGRAM/ERASE OPERATIONS

AMD's Flasherase and Flashrite Algorithms

Flasherase Erase Sequence

Erase Set-Up/Erase Commands

Erase Set-Up

Erase Set-up is the first of a two-cycle erase command. It is a command-only operation that stages the device for bulk chip erase. The array contents are not altered with this command. 20H is written to the command register in order to perform the Erase Set-up operation.

Erase

The second two-cycle erase command initiates the bulk erase operation. You must write the Erase command (20H) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-verify) to the register.

This two step sequence of the Set-up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, chip erasure can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note: *The Flash memory device must be fully programmed to 00H data prior to erasure. This equalizes the charge on all memory cells ensuring reliable erasure.*

Erase-Verify Command

The erase operation erases all bytes of the array in parallel. After the erase operation, all bytes must be sequentially verified. The Erase-verify operation is initiated by writing A0H to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse or $\overline{CE}$ pulse, whichever occurs later. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-verify operation, the Am28F010 applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are properly erased.

Verify Next Address

You must write the Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ pulse, whichever occurs later. The process continues for each byte in the memory array until a byte does not return FFH data or all the bytes in the array are accessed and verified.

If an address is not verified to FFH data, the entire chip is erased again (refer to Erase Set-up/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The device is now ready to be programmed. At this point, the verification operation is terminated by writing a valid command (e.g. Program set-up) to the command register. Figure 1 and Table 4, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

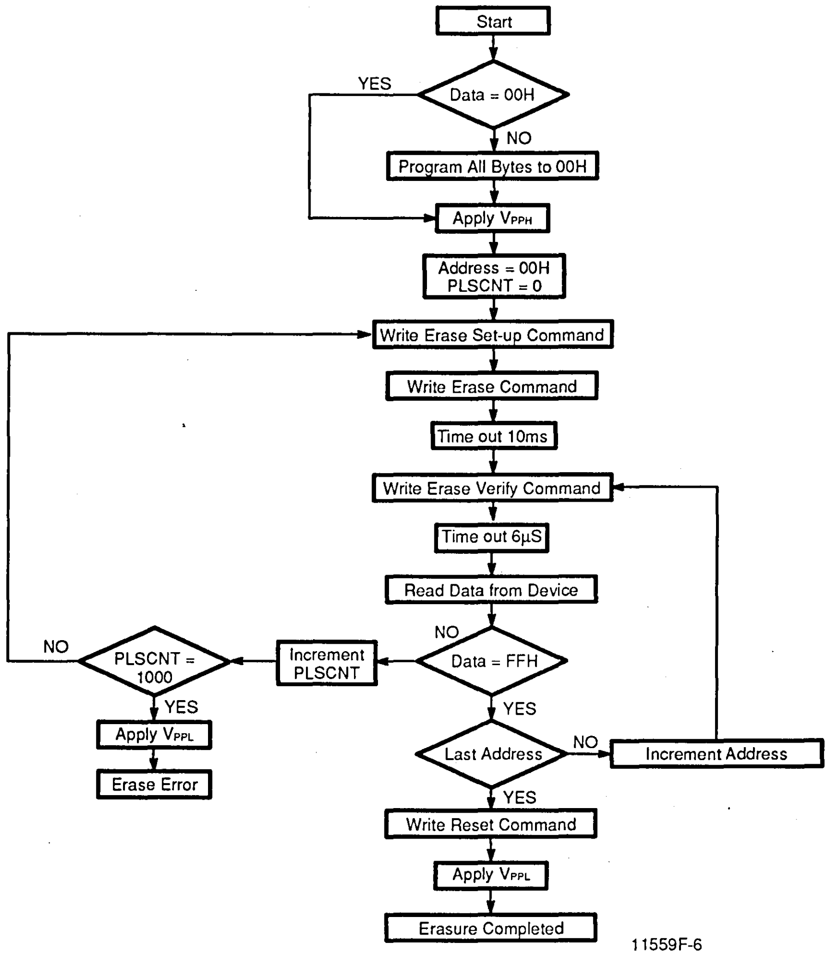


Figure 1. Flasherase Electrical Erase Algorithm

Flasherase Electrical Erase Algorithm

This Flash memory device erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the array. Erasure begins with a read of the memory contents. The Am28F010 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

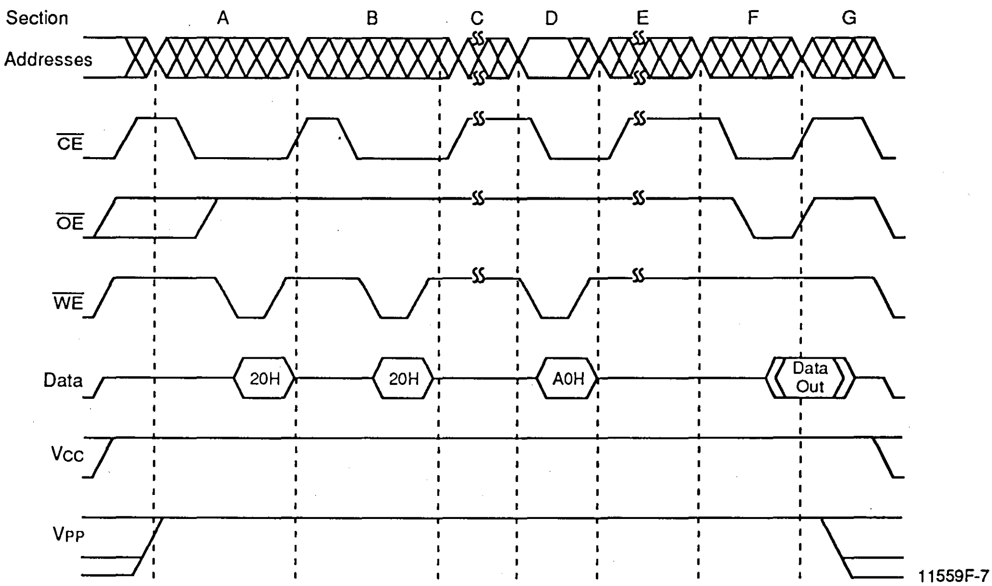
Should the device be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished using the Flashrite Programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. If a byte fails to verify, the device is erased again. With each erase operation, an increasing number of bytes verify to the erased state. Typically, devices are erased in less than 100 pulses (one second). Erase efficiency may be improved by storing the address of the last byte that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. A total of 1000 erase pulses are allowed per reprogram cycle, which corresponds to approximately 10 seconds of cumulative erase time. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 1 illustrates the electrical erase algorithm.

Table 4. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) ***Note:*** *Use Flashrite programming algorithm (Figure 3) for programming.*
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Erase Set-Up	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-Verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Reset	Data = FFH, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. *See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.*
2. *Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.*
3. *The erase algorithm **Must Be Followed** to ensure proper and reliable operation of the device.*



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time-out	Write	Time-out	Read	Standby
Command	20H	20H	N/A	A0H	N/A	Compare Data	N/A
Function	Erase Set-up	Erase	Erase (10 ms)	Erase-Verify	Transition (6 µs)	Erase Verification	Proceed per Erase Algorithm

Figure 2. AC Waveforms For Erase Operations

Analysis of Erase Timing Waveform

Note: *This analysis does not include the requirement to program the entire array to 00H data prior to erasure. Refer to the Flashrite Programming algorithm.*

Erase Set-Up/Erase

This analysis illustrates the use of two-cycle erase commands (section A and B). The first erase command (20H) is a set-up command and does not affect the array data (section A). The second erase command (20H) initiates the erase operation (section B) on the rising edge of this $\overline{WE}$ pulse. All bytes of the memory array are erased in parallel. No address information is required.

The erase pulse occurs in section C.

Time-Out

A software timing routine (10 ms duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Note: *An integrated stop timer prevents any possibility of overerasure by limiting each time-out period of 10 ms.*

Erase-Verify

Upon completion of the erase software timing routine, the microprocessor must write the Erase-verify command (A0H). This command terminates the erase operation on the rising edge of the $\overline{WE}$ pulse (section D). The Erase-verify command also stages the device for data verification (section F).

After each erase operation each byte must be verified. The byte address to be verified must be supplied with the Erase-verify command (section D). Addresses are latched on the falling edge of the $\overline{WE}$ pulse.

Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operation (section E).

During Erase-verification (section F) each address that returns FFH data is successfully erased. Each address of the array is sequentially verified in this manner by repeating sections D thru F until the entire array is verified or an address fails to verify. Should an address location fail to verify to FFH data, erase the device again. Repeat sections A thru F. Resume verification (section D) with the failed address.

Each data change sequence allows the device to use up to 1,000 erase pulses to completely erase. Typically 100 erase pulses are required.

Note: *All address locations must be programmed to 00H prior to erase. This equalizes the charge on all memory cells and ensures reliable erasure.*

Flashrite Programming Sequence

Program Set-Up/Program Command

Program Set-Up

The Am28F010 is programmed byte by byte. Bytes may be programmed sequentially or at random. Program Set-up is the first of a two-cycle program command. It stages the device for byte programming. The Program Set-up operation is performed by writing 40H to the command register.

Program

Only after the program set-up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-verify command to terminate the programming operation. This two step sequence of the Set-up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte just programmed must be verified.

Write C0H into the command register in order to initiate the Program-verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-verify operation stages the device for verification of the last byte programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-verify operation, the Am28F010 applies an internally generated margin voltage to the addressed byte. A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte location. Should the byte fail to verify, reprogram (refer to Program Set-up/Program). Figure 3 and Table 5 indicate how instructions are combined with the bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Flashrite Programming Algorithm

The Am28F010 Flashrite Programming algorithm employs an interactive closed loop flow to program data byte by byte. Bytes may be programmed sequentially or at random. The Flashrite Programming algorithm uses 10 µs programming pulses. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 3 and Table 5 illustrate the programming algorithm.

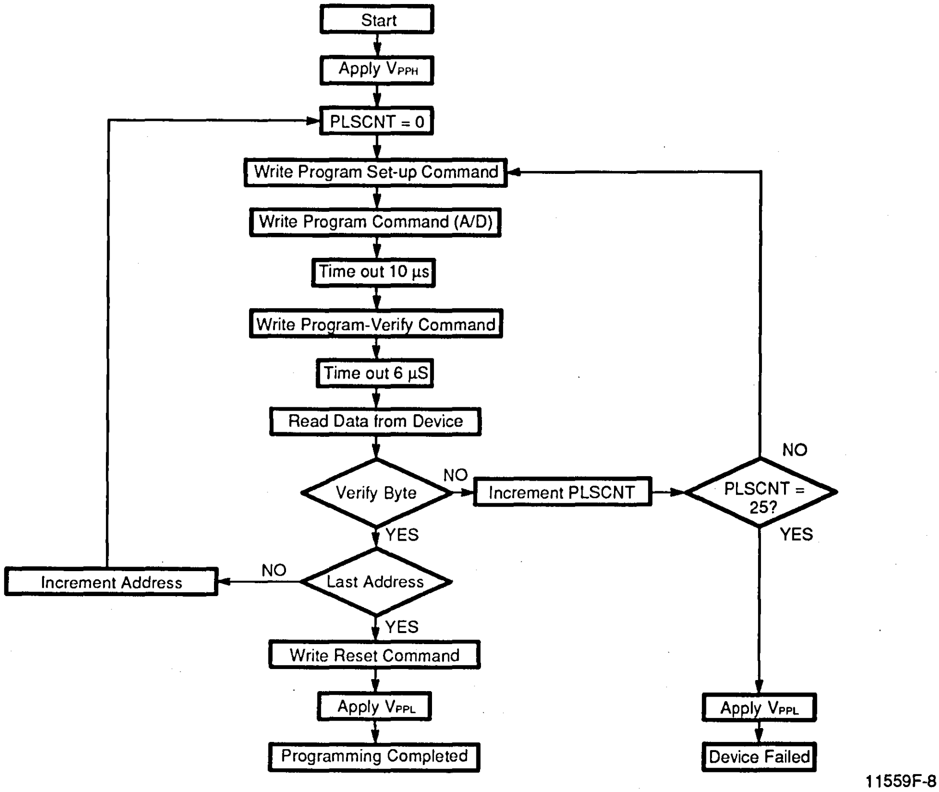


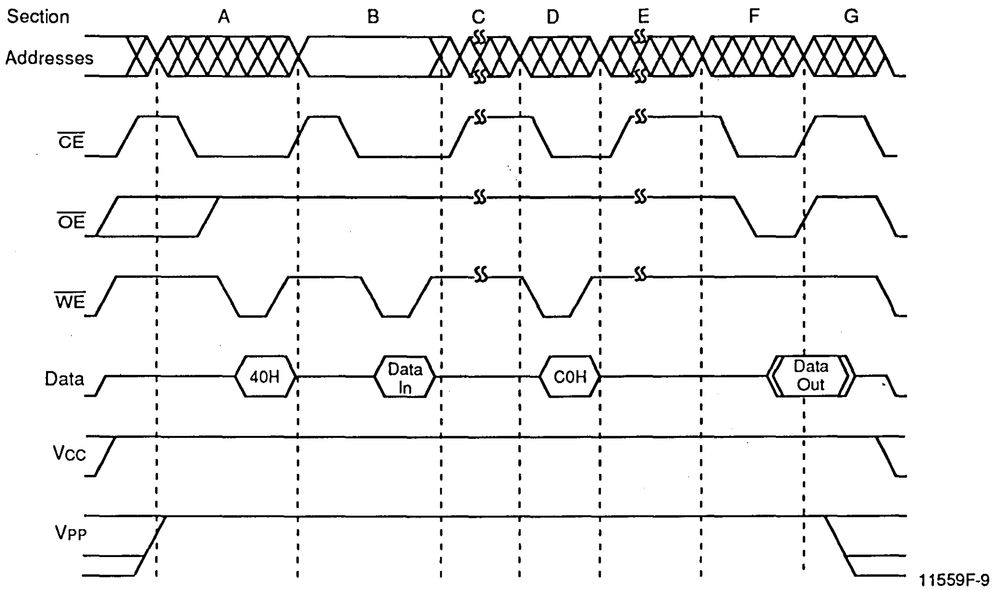
Figure 3. Flashrite Programming Algorithm

Table 5. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Program Set-Up	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Reset	Data = FFH, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. *See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.*
2. *Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.*



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time-out	Write	Time-out	Read	Standby
Command	40H	Program Address, Program Data	N/A	C0H (Stops Program)	N/A	Compare Data	N/A
Function	Program Set-up	Program Command Latch Address & Data	Program (10 µs)	Program Verify	Transition (6 µs)	Program Verification	Proceed per Programming Algorithm

Figure 4. A.C. Waveforms for Programming Operations

Analysis of Program Timing Waveforms

Program Set-Up/Program

Two-cycle write commands are required for program operations (section A and B). The first program command (40H) is a set-up command and does not affect the array data (section A). The second program command latches address and data required for programming on the falling and rising edge of $\overline{WE}$ respectively (section B). The rising edge of this $\overline{WE}$ pulse (section B) also initiates the programming pulse. The device is programmed on a byte by byte basis either sequentially or randomly.

The program pulse occurs in section C.

Time-Out

A software timing routine (10 µs duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Note: *An integrated stop timer prevents any possibility of overprogramming by limiting each time-out period of 10 µs.*

Program-Verify

Upon completion of the program timing routine, the microprocessor must write the program-verify command (C0H). This command terminates the programming operation on the rising edge of the $\overline{WE}$ pulse (section D). The program-verify command also stages the device for data verification (section F). Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operations (section E).

During program-verification (section F) each byte just programmed is read to compare array data with original program data. When successfully verified, the next desired address is programmed. Should a byte fail to verify, reprogram the byte (repeat section A thru F). Each data change sequence allows the device to use up to 25 program pulses per byte. Typically, bytes are verified within one or two pulses.

Algorithm Timing Delays

There are four different timing delays associated with the Flasherase and Flashrite algorithms:

1. The first delay is associated with the V_{PP} rise-time when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on the V_{PP}, the delay required is proportional to the number of devices being erased and the 0.1 µF/device. V_{PP} must reach its final value 100 ns before commands are executed.
2. The second delay time is the erase time pulse width (10 ms). A software timing routine should be run by the local microprocessor to time out the delay. The erase operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the erase operation. To ensure proper device operation, write the Erase-verify operation after each pulse.
3. A third delay time is required for each programming pulse width (10 µs). The programming algorithm is interactive and verifies each byte after a program pulse. The program operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the programming operation.
4. A fourth timing delay associated with both the Flasherase and Flashrite algorithms is the write recovery time (6 µs). During this time internal circuitry is changing voltage levels from the erase/ program level to those used for margin verify and read operations. An attempt to read the device during this period will result in possible false data (it may appear the device is not properly erased or programmed).

Note: *Software timing routines should be written in machine language for each of the delays. Code written in machine language requires knowledge of the appropriate microprocessor clock speed in order to accurately time each delay.*

Parallel Device Erasure

Many applications will use more than one Flash memory device. Total erase time may be minimized by implementing a parallel erase algorithm. Flash memories may erase at different rates. Therefore each device must be verified separately. When a device is completely erased and verified use a masking code to prevent further erasure. The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-Up Sequence

The Am28F010 powers-up in the Read only mode. Power supply sequencing is not required.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset command must be written two consecutive times after the set-up Program command (40H). This will reset the device to the Read mode.

Following any other Flash command write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The set-up Program command (40H) is the only command that requires a two sequence reset cycle. The first Reset command is interpreted as program data. However, FFH data is considered null data during programming operations (memory cells are only programmed from a logical "1" to "0"). The second Reset command safely aborts the programming operation and resets the device to the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the set-up Program state or not.

Programming In-System

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Auto Select Command

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F010 contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H. A read cycle from address 0001H returns the device code A7H (see Table 2). To terminate the operation, it is necessary to write another valid command, such as Reset (FFH), into the register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages . . . . −65°C to +150°C
Plastic Packages . . . . −65°C to +125°C

Ambient Temperature
with Power Applied . . . . −55°C to + 125°C

Voltage with Respect To Ground
All pins except A9 and V_{PP} (Note 1) −2.0 V to +7.0 V

V_{CC} (Note 1) . . . . −2.0 V to +7.0 V

A9 (Note 2) . . . . −2.0 V to +14.0 V

V_{PP} (Note 2) . . . . −2.0 V to +14.0 V

Output Short Circuit Current (Note 3) . . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A9 and V_{PP} pins is −0.5 V. During voltage transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) . . . . 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) . . . . −40°C to +85°C

Extended (E) Devices
Case Temperature (T_C) . . . . −55°C to +125°C

Military (M) Devices
Case Temperature (T_C) . . . . −55°C to +125°C

V_{CC} Supply Voltages
V_{CC} for Am28F010−X5 . . . . +4.75 V to +5.25 V

V_{CC} for Am28F010−XX0 . . . . +4.50 V to +5.50 V

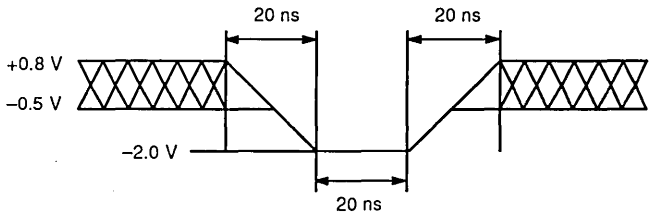
V_{PP} Supply Voltages
Read . . . . −0.5 V to +12.6 V

Program, Erase, and Verify . . . . . +11.4 V to +12.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



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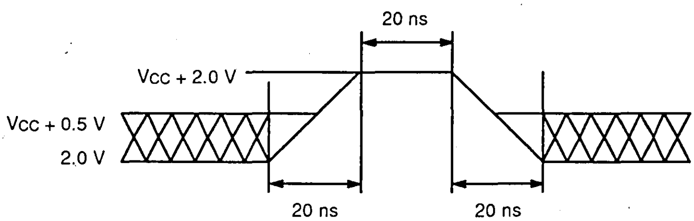
Maximum Positive Input Overshoot



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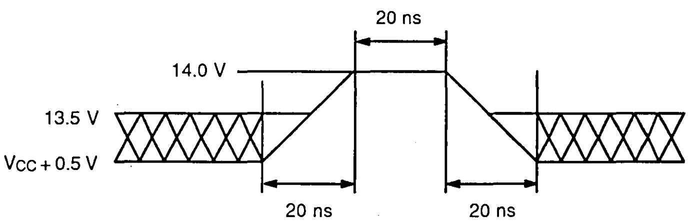
Maximum V_{PP} Overshoot



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DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted) (Notes 1–4)

DC CHARACTERISTICS—TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{IH}$		0.2	1.0	mA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ $I_{OUT} = 0$ mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress (Note 4)		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress (Note 4)		10	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			±1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	µA
		$V_{PP} = V_{PPL}$			±1.0	
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 5.8$ mA $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.5$ mA $V_{CC} = V_{CC}$ Min	2.4			V
V_{ID}	A9 Auto Select Voltage	$A9 = V_{ID}$	11.5		13.0	V
I_{ID}	A9 Auto Select Current	$A9 = V_{ID}$ Max $V_{CC} = V_{CC}$ Max		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:*** *Erase/Program are inhibited when* $V_{PP} = V_{PPL}$	0.0		V_{CC} +2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. ***Caution:*** *the Am28F010 must not be removed from (or inserted into) a socket when* V_{CC} *or* V_{PP} *is applied.*
2. I_{CC1} *is tested with* $\overline{OE} = V_{IH}$ *to simulate open outputs.*
3. *Maximum active power usage is the sum of* I_{CC} *and* I_{PP}.
4. *Not 100% tested.*

DC CHARACTERISTICS—CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS}			± 1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}			± 1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{CC} + 0.5$ V		15	100	µA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ $I_{OUT} = 0$ mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress (Note 4)		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress (Note 4)		10	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			± 1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	µA
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 5.8$ mA $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.5$ mA, $V_{CC} = V_{CC}$ Min	0.85 V_{CC}			V
V_{OH2}		$I_{OH} = -100$ µA, $V_{CC} = V_{CC}$ Min	V_{CC} –0.4			
V_{ID}	A9 Auto Select Voltage	A9 = V_{ID}	11.5		13.0	V
I_{ID}	A9 Auto Select Current	A9 = V_{ID} Max $V_{CC} = V_{CC}$ Max		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:*** *Erase/Program are inhibited when* $V_{PP} = V_{PPL}$	0.0		V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. ***Caution:*** *the Am28F010 must not be removed from (or inserted into) a socket when* V_{CC} *or* V_{PP} *is applied.*
2. I_{CC1} *is tested with* $\overline{OE} = V_{IH}$ *to simulate open outputs.*
3. *Maximum active power usage is the sum of* I_{CC} *and* I_{PP}.
4. *Not 100% tested.*

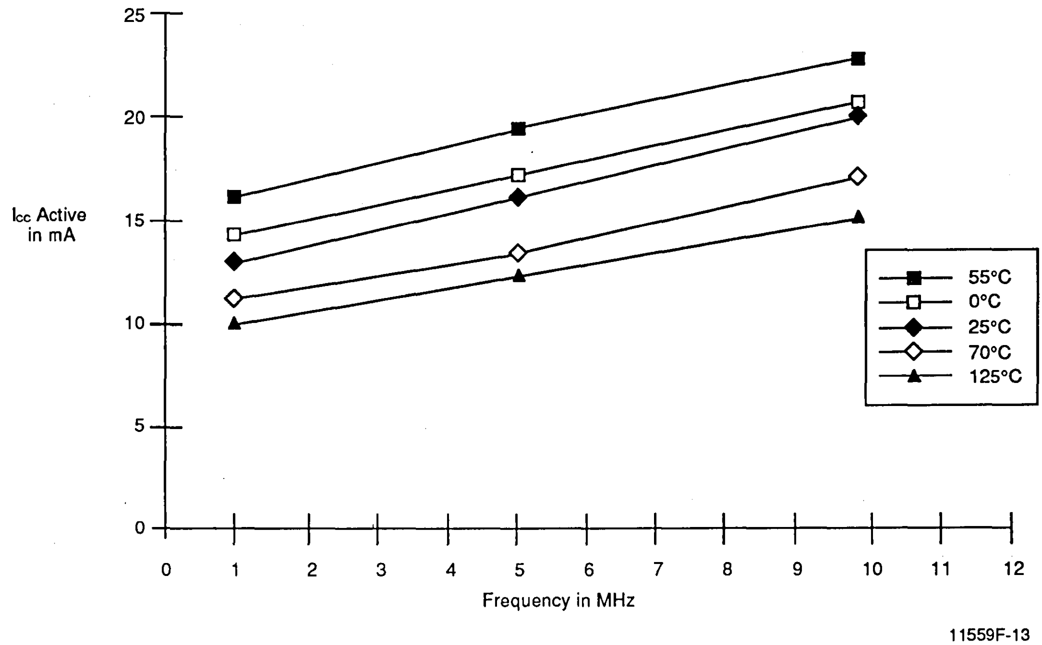

Figure 5. Am28F010–Average Icc Active vs. Frequency
Vcc = 5.5 V, Addressing Pattern = Minmax
Data Pattern = Checkerboard

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	8	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A = 25°C$, $f = 1.0$ MHz*

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

AC CHARACTERISTICS—Read Only Operation (Notes 1–4)

Parameter Symbols				Am28F010					
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)	Min	90	120	150	200	250	ns
			Max						
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min						
			Max	90	120	150	200	250	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min						
			Max	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min						
			Max	35	50	55	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z (Note 4)	Min	0	0	0	0	0	ns
			Max						
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z (Note 3)	Min						
			Max	20	30	35	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z (Note 4)	Min	0	0	0	0	0	ns
			Max						
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z (Note 4)	Min						
			Max	20	30	35	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change (Note 4)	Min	0	0	0	0	0	ns
			Max						
t_{WHGL}		Write Recovery Time before Read	Min	6	6	6	6	6	µs
			Max						
t_{VCS}		V_{CC} Set-up Time to Valid Read (Note 4)	Min	50	50	50	50	50	µs
			Max						

Notes:

1. *Output Load: 1 TTL gate and $C_L = 100$ pF*
   Input Rise and Fall Times: < 10 ns
   Input Pulse levels: 0.45 V to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. *The Am28F010-95 Output Load: 1 TTL gate and $C_L = 100$ pF*
   Input Rise and Fall Times: < 10 ns
   Input Pulse levels: 0 V to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. *Guaranteed by design not tested.*
4. *Not 100% tested.*

AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1– 6)

Parameter Symbols JEDEC	Parameter Symbols Standard	Parameter Description		Am28F010 -90 -95	-120	-150	-200	-250	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 6)	Min Max	90	120	150	200	250	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min Max	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min Max	45	50	60	75	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min Max	45	50	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min Max	10	10	10	10	10	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	Min Max	6	6	6	6	6	µs
t_{GHWL}		Read Recovery Time before Write	Min Max	0	0	0	0	0	µs
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	Min Max	0	0	0	0	0	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min Max	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min Max	45	50	60	60	60	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min Max	20	20	20	20	20	ns
t_{WHWH1}		Duration of Programming Operation (Note 4)	Min Max	10	10	10	10	10	µs
t_{WHWH2}		Duration of Erase Operation (Note 4)	Min Max	9.5	9.5	9.5	9.5	9.5	ms
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 6)	Min Max	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 10% V_{PPL} (Note 6)	Min Max	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 6)	Min Max	100	100	100	100	100	ns

Notes:

1. *Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.*
2. *All devices except Am28F010-95. Input Rise and Fall times: < 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V*
3. *Am28F010-95. Input Rise and Fall times: < 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V*
4. *Maximum pulse widths not required because the on-chip program/erase stop timer will terminate the pulse widths internally on the device.*
5. *Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the Write Pulse Width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.*
6. *Not 100% tested.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS

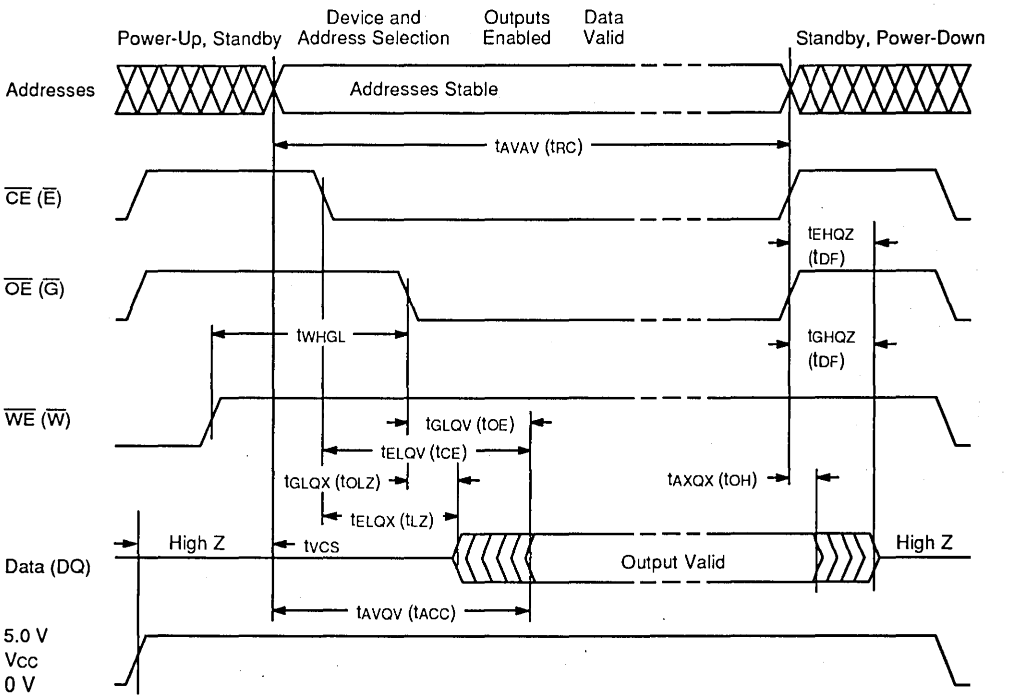

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Figure 6. AC Waveforms for Read Operations

SWITCHING WAVEFORMS

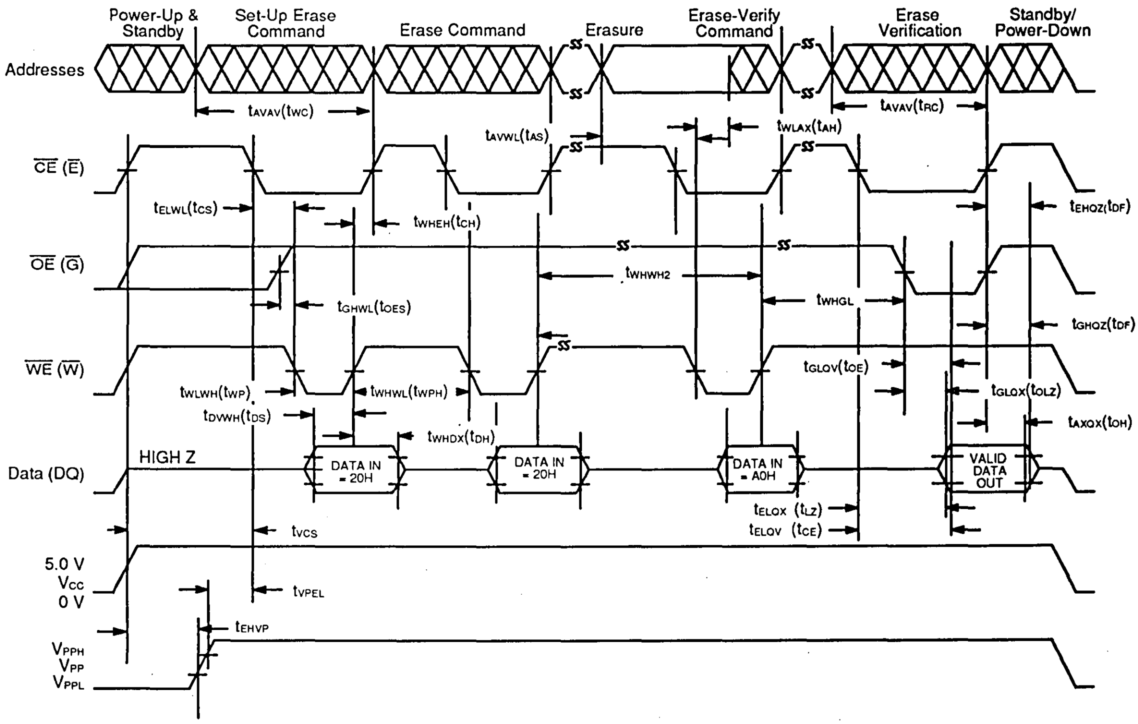


Figure 7. AC Waveforms for Erase Operations

SWITCHING WAVEFORMS

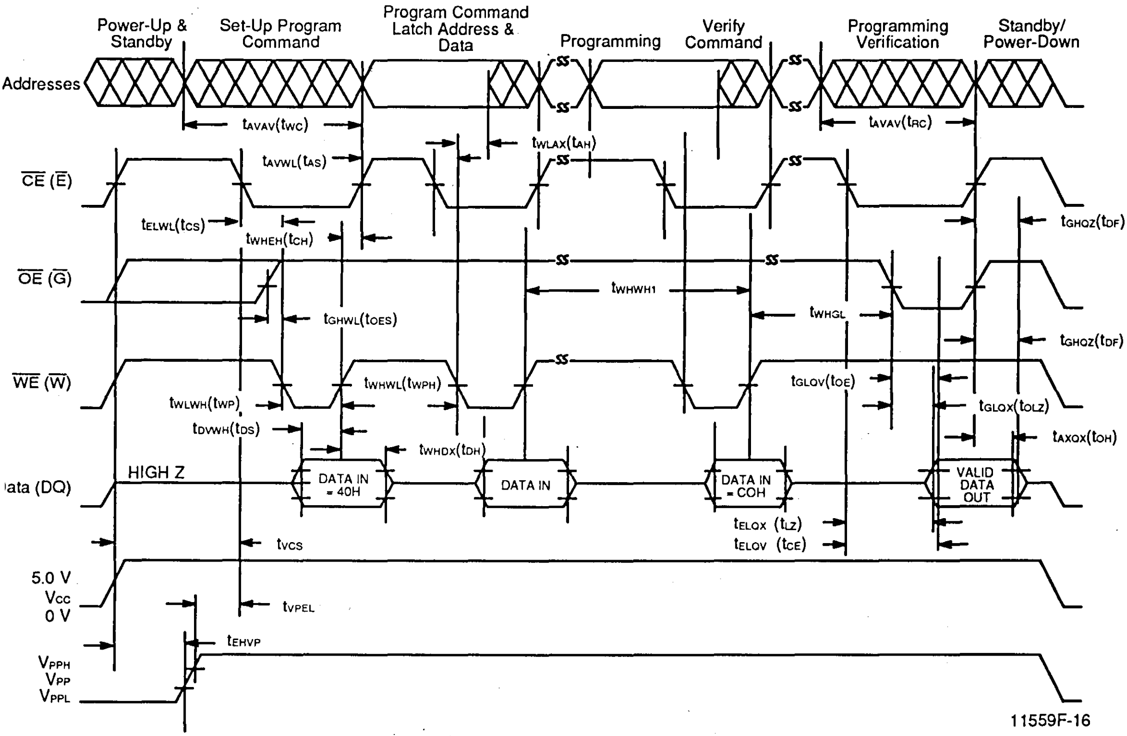
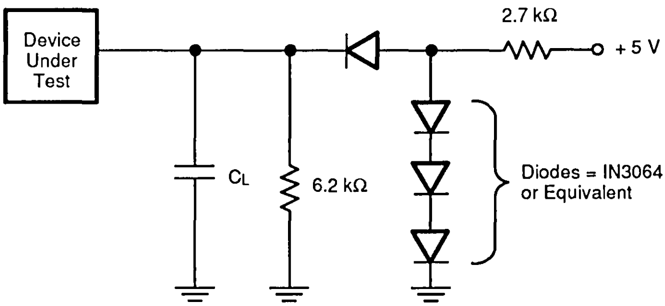


Figure 8. AC Waveforms for Programming Operations

SWITCHING TEST CIRCUIT



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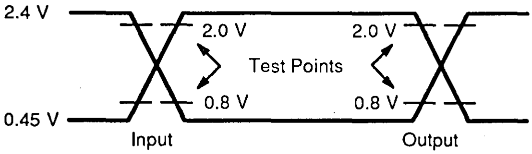
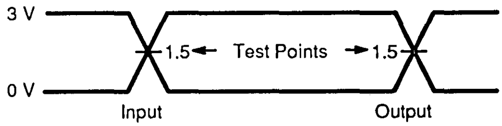
C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORMS



All Devices Except Am28F010-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are < 10 ns.



For Am28F010-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are < 10 ns.

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ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits Min	Limits Typ	Limits Max (Note 3)	Unit	Comments
Chip Erase Time		1 (Note 1)	10 (Note 2)	s	Excludes 00H programming prior to erasure
Chip Programming Time		2 (Note 1)	12.5	s	Excludes system-level overhead
Write/Erase Cycles	10,000			Cycles	

Notes:

1. *25°C, 12 V V_{PP}*
2. *The Flasherase/Flashrite algorithms allows for 60 second erase time for military temperature range operations.*
3. *Maximum time specified is lower than worst case. Worst case is derived from the Flasherase/Flashrite pulse count (Flasherase = 1000 max and Flashrite = 25 max). Typical worst case for program and erase operations is significantly less than the actual device limit.*

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A9 and V_{PP})	−1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	−1.0 V	V_{CC} + 1.0 V
Current	−100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

DATA SHEET REVISION SUMMARY FOR Am28F010

Data sheet is Final now, and not Preliminary.

Erase, Program and Read Mode – Write Operations

Removed Command Register Table and Bit assignments.

Erase, Program and Read Mode – Read Command

The statement requiring a 6 μs wait before accessing the first addressed location was removed.

Table 3 – Am28F010 Command Definitions

The note describing a 6 μs wait before accessing the first addressed location was removed.

Flasherase Erase Sequence – Erase Verify Command

The address latched also depends on the falling edge of $\overline{CE}$, whichever happens later.

Flasherase Erase Sequence – Verify Next Address

The new address latched also depends on the falling edge of $\overline{CE}$. whichever happens later.

Auto Select Command

Programming In-System

Titles for each section were switched.

Programming In-System

It is necessary to write a valid command, such as Reset, into the register.

DC Characteristics – TTL/NMOS Compatible

Added Note 4. Those characteristics are not 100% tested.

DC Characteristics – CMOS Compatible

Added Note 4. Those characteristics are not 100% tested.

FINAL

Am28F010A

1 Megabit (131,072 x 8-Bit) CMOS 12.0 Volt, Bulk Erase Flash Memory with Embedded Algorithms

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 90 ns maximum access time
- **CMOS low power consumption**
  - 30 mA maximum active current
  - 100 μA maximum standby current
  - No data retention power consumption
- **Compatible with JEDEC-standard byte-wide 32-Pin EPROM pinouts**
  - 32-pin DIP
  - 32-pin PLCC
  - 32-pin TSOP
  - 32-pin LCC
- **100,000 write/erase cycles minimum**
- **Write and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **Embedded Erase Electrical Bulk Chip-Erase**
  - Three seconds typical chip-erase including pre-programming
- **Embedded Program**
  - 14 μs typical byte-program including time-out
  - Two seconds typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell
- **Embedded algorithms for completely self-timed write/erase operations**

GENERAL DESCRIPTION

The Am28F010A is a 1 Megabit Flash memory organized as 128K bytes of 8 bits each. AMD's Flash memories offer the most cost-effective and reliable read/write non- volatile random access memory. The Am28F010A is packaged in 32-pin PDIP, PLCC, and TSOP versions. The device is also offered in the ceramic DIP and LCC packages. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers. The Am28F010A is erased when shipped from the factory.

The standard Am28F010A offers access times as fast as 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F010A has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F010A uses a command register to manage this functionality, while maintaining a standard JEDEC Flash standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

AMD's Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F010A uses a 12.0 V ± 5% V_{PP} supply to perform the erase and programming functions.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 milliamps on address and data pins from –1 V to Vcc +1 V.

Embedded Program

The Am28F010A is byte programmable using the Embedded Programming algorithm. The Embedded Programming algorithm does not require the system to time-out or verify the data programmed. The typical room temperature programming time of the Am28F010A is two seconds.

Publication# 16778 Rev. B Amendment/0
Issue Date: March 1994

GENERAL DESCRIPTION

Embedded Erase

The entire chip is bulk erased using the Embedded Erase algorithm. The Embedded Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internal to the device. Typical erasure at room temperature is accomplished in one second.

AMD's Am28F010A is entirely pin and software compatible with AMD Am28F020A Flash memory.

Embedded Programming Algorithm vs. Flashrite Programming Algorithm

The Flashrite Programming algorithm requires the user to write a program set-up command, a program command (program data and address), and a program verify command followed by a read and compare operation. The user is required to time the programming pulse width in order to issue the program verify command. An integrated stop timer prevents any possibility of overprogramming. Upon completion of this sequence the data is read back from the device and compared by the user with the data intended to be written; if there is not a match, the sequence is repeated until there is a match or the sequence has been repeated 25 times.

AMD's Embedded Programming algorithm requires the user to only write a program set-up command and a program command (program data and address). The device automatically times the programming pulse width, provides the program verify and counts the number of sequences. A status bit, $\overline{\text{Data}}$ Polling, provides feedback to the user as to the status of the programming operation.

Embedded Erase Algorithm vs. Flasherase Erase Algorithm

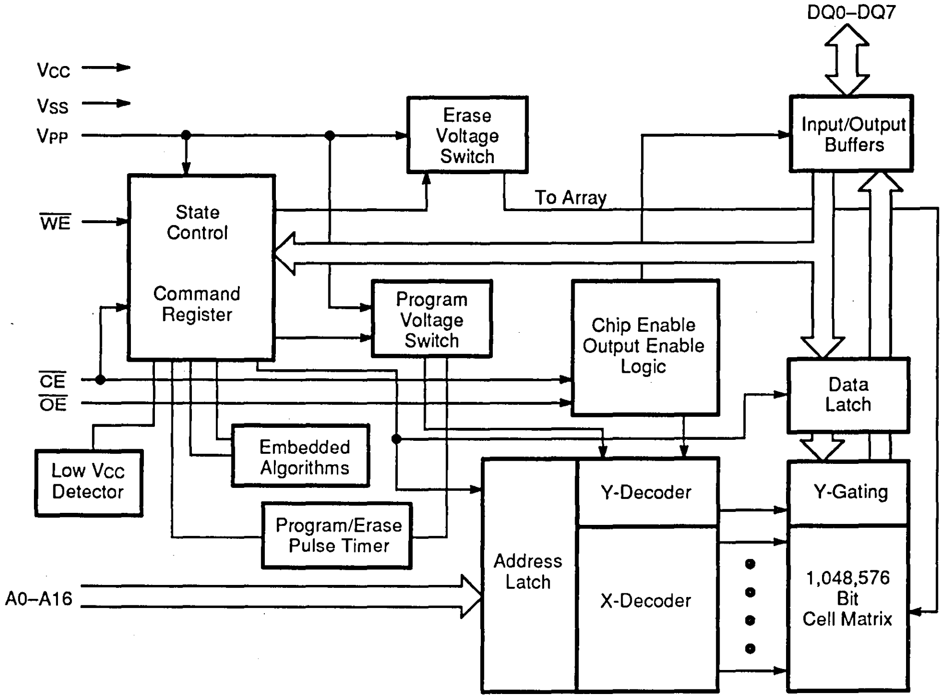
The Flasherase Erase algorithm requires the device to be completely programmed prior to executing an erase command. To invoke the erase operation the user writes an erase set-up command, an erase command, and an erase verify command. The user is required to time the erase pulse width in order to issue the erase verify command. An integrated stop timer prevents any possibility of overerasure. Upon completion of this sequence the data is read back from the device and compared by the user with erased data. If there is not a match, the sequence is repeated until there is a match or the sequence has been repeated 1,000 times.

AMD's Embedded Erase algorithm requires the user to only write an erase set-up command and erase command. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verify and counts the number of sequences. A status bit, $\overline{\text{Data}}$ Polling, provides feedback to the user as to the status of the erase operation.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F010A is designed to support either $\overline{\text{WE}}$ or $\overline{\text{CE}}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$ whichever occurs last. Data is latched on the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$ whichever occurs first. To simplify the following discussion, the $\overline{\text{WE}}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{\text{WE}}$ signal.

AMD's Flash technology combines years of EPROM and EEPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F010A electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

BLOCK DIAGRAM



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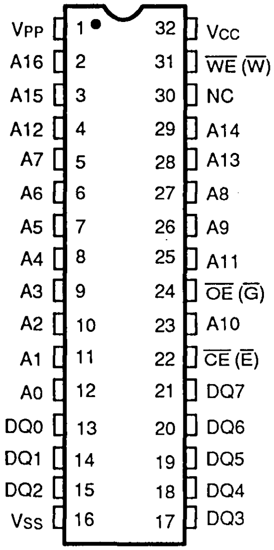
PRODUCT SELECTOR GUIDE

Family Part No.	Am28F010A				
Ordering Part No: ±10% Vcc Tolerance	**-90**	**-120**	**-150**	**-200**	**-250**
±5% Vcc Tolerance	**-95**				
Max Access Time (ns)	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	50	55	55	55

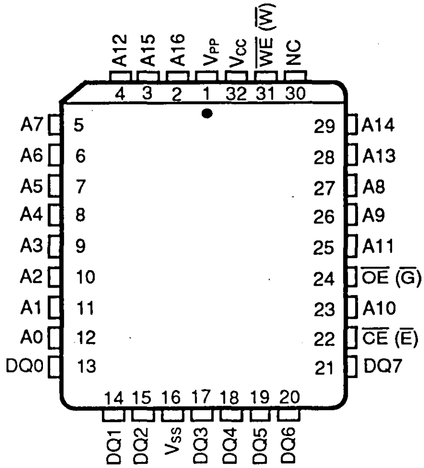
CONNECTION DIAGRAMS

DIP



16778B-2

PLCC*



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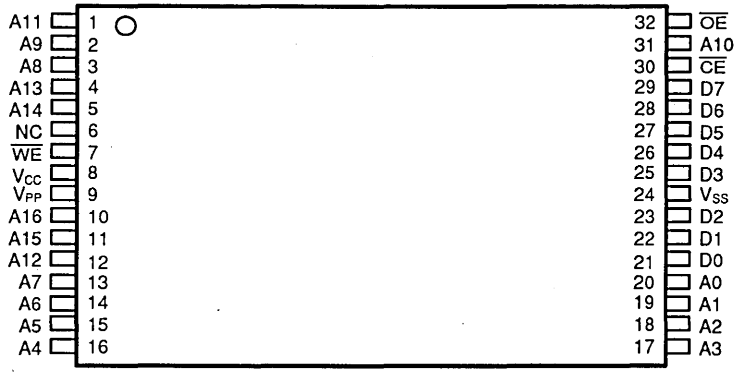
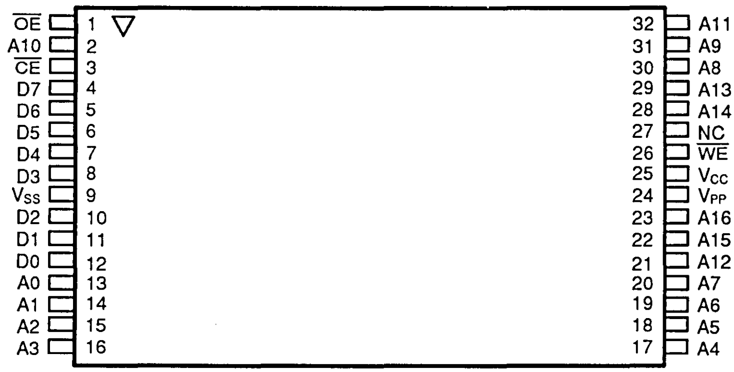
Note: *Pin 1 is marked for orientation.*
**Also available in LCC.*

TSOP PACKAGES



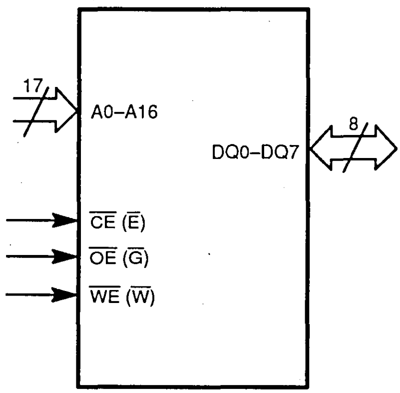
28F010A Standard Pinout



28F010A Reverse Pinout 16778B-4

28F010A 128K x 8 Flash Memory in 32-Lead TSOP

LOGIC SYMBOL



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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

AM28F010A -95 J C B

OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-In

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended (–55°C to +125°C)

PACKAGE TYPE
P = 32-Pin Plastic DIP (PD 032)
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)
E = 32-Pin TSOP Standard Pinout (TS 032)
F = 32-Pin TSOP Reverse Pinout (TSR 032)
D = 32-Pin Ceramic DIP (CD 032)
L = 32-Pin Rectangular Leadless Chip Carrier (CLR 032)

SPEED
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am28F010A
1 Megabit (128K x 8-Bit) CMOS Flash Memory with Embedded Algorithms

Valid Combinations	
AM28F010A-90 AM28F010A-95	PC, JC, EC, FC, DC, LC
AM28F010A-120 AM28F010A-150 AM28F010A-200	PC, PI, JC, JI, PE, PEB, JE, JEB, EC, FC, EI, FI, EE, FE, EEB, FEB, DC, DI, DE, DEB, LC, LI, LE, LEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

AM28F010A -120 /B X A

LEAD FINISH
A = Hot Solder Dip

PACKAGE TYPE
X = 32-Pin Ceramic DIP (CD 032)
U = 32-Pin Rectangular Ceramic Leadless Chip Carrier (CLR 032)

DEVICE CLASS
/B = Class B

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am28F010A
1 Megabit (128K x 8-Bit) CMOS Flash Memory with Embedded Algorithms

Valid Combinations	
AM28F010A-120	/BXA, /BUA
AM28F010A-150	
AM28F010A-200	
AM78F010A-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

A0–A16
Address Inputs for memory locations. Internal latches hold addresses during write cycles.

$\overline{CE}$ ($\overline{E}$)
The Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.

DQ0–DQ7
Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

NC
No Connect-corresponding pin is not connected internally to the die.

$\overline{OE}$ ($\overline{G}$)
The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

V_{CC}
Power supply for device operation. (5.0 V ± 5% or 10%)

V_{PP}
Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2$ V.

V_{SS}
Ground

$\overline{WE}$ ($\overline{W}$)
The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

BASIC PRINCIPLES

The Am28F010A uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0 V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F010A functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F010A's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F010A is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Embedded Erase Algorithm

AMD now makes erasure extremely simple and reliable. The Embedded Erase algorithm requires the user to only write an erase set-up command and erase command. The device will automatically pre-program and verify the entire array. The device automatically times the erase pulse width, provides the erase verify and counts the number of sequences. A status bit, similar to $\overline{\text{Data}}$ Polling, provides feedback to the user as to the status of the erase operation.

Embedded Programming Algorithm

AMD now makes programming extremely simple and reliable. The Embedded Programming algorithm requires the user to only write a program set-up command and a program command. The device automatically times the programming pulse width, provides the program verify and counts the number of sequences. A status bit, similar to $\overline{\text{Data}}$ Polling, provides feedback to the user as to the status of the programming operation.

Data Protection

The Am28F010A is designed to offer protection against accidental erasure or programming, caused by spurious system level signals that may exist during power transitions. The Am28F010A powers up in its read only state. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting form V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. The device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 10 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

FUNCTIONAL DESCRIPTION

Description of User Modes

Table 1. Am28F010A User Bus Operations

Operation		$\overline{CE}$ (E)	$\overline{OE}$ (G)	$\overline{WE}$ (W)	V_{PP} (Note 1)	A0	A9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A0	A9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (A2H)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A0	A9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A0	A9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} \leq V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An < V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. *V_{PPL} may be grounded, connected with a resistor to ground, or $\leq V_{CC}$ +2.0 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.*
2. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.*
3. *$11.5 \leq V_{ID} \leq 13.0$ V*
4. *Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.*
5. *With V_{PP} at high voltage, the standby current is I_{CC} + I_{PP} (standby).*
6. *Refer to Table 3 for valid D_{IN} during a write operation.*
7. *All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A9 and A0 must be held at V_{IL}.*

READ ONLY MODE

$V_{PP} < V_{CC} + 2$ V
Command Register Inactive

Read

The Am28F010A functions as a read only memory when $V_{PP} < V_{CC} + 2$ V. The Am28F010A has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC} - t_{OE}$).

Standby Mode

The Am28F010A has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), consumes less than 100 µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1 mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A PROM Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13.0 V) on address A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to $V_{CC} + 2.0$ V while using this Auto select mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the Am28F010A these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F010A Auto Select Code

Type	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	A2	1	0	1	0	0	0	1	0

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%

Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 3 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Am28F010A Command Definitions

	First Bus Cycle			Second Bus Cycle		
Command	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 4)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/A2H
Embedded Erase Set-up/ Embedded Erase	Write	X	30H	Write	X	30H
Embedded Program Set-up/ Embedded Program	Write	X	10H or 50H	Write	PA	PD
Reset (Note 4)	Write	X	FFH	Write	X	FFH

Notes:

1. *Bus operations are defined in Table 1.*
2. *RA = Address of the memory location to be read.*
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   X = Don't care.
3. *RD = Data read from location RA during read operation.*
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
4. *Please reference Reset Command section.*

FLASH MEMORY PROGRAM/ERASE OPERATIONS

AMD's Embedded Program and Erase Operations

Embedded Erase Algorithm

The automatic chip erase does not require the device to be entirely pre-programmed prior to executing the Embedded set-up erase command and Embedded erase command. Upon executing the Embedded erase command the device automatically will program and verify the entire memory for an all zero data pattern. The system is not required to provide any controls or timing during these operations.

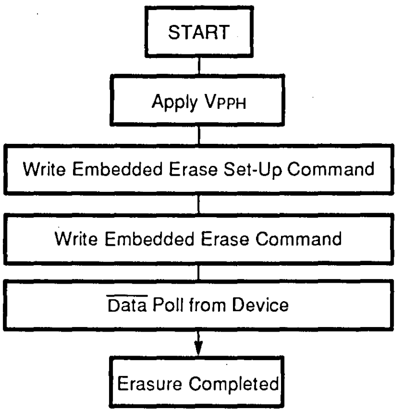
When the device is automatically verified to contain an all zero pattern, a self-timed chip erase and verify begin. The erase and verify operation are complete when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to Read mode. The system is not required to provide any control or timing during these operations.

When using the Embedded Erase algorithm, the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard erase verify command is used.

The Embedded Erase Set-Up command is a command only operation that stages the device for automatic electrical erasure of all bytes in the array. Embedded Erase Set-Up is performed by writing 30H to the command register.

To commence automatic chip erase, the command 30H must be written again to the command register. The automatic erase begins on the rising edge of the $\overline{WE}$ and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to Read mode.

Figure 5 and Table 4 illustrate the Embedded Erase algorithm, a typical command string and bus operation.



16778B-6

Figure 5. Embedded Erase Algorithm

Table 4. Embedded Erase Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Erase Set-Up Command	Data = 30H
Write	Embedded Erase Command	Data = 30H
Read		$\overline{\text{Data}}$ Polling to Verify Erasure
Standby		Compare Output to FFH
Read		Available for Read Operations

Note:

1. *See DC Characteristics for value of V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Functional Description.*

Embedded Programming Algorithm

The Embedded Program Set-Up is a command only operation that stages the device for automatic programming. Embedded Program Set-Up is performed by writing 10H or 50H to the command register.

Once the Embedded Set-Up Program operation is performed, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ pulse, whichever happens later. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. The rising edge of $\overline{WE}$ also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin. The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to Read mode.

Figure 6 and Table 5 illustrate the Embedded Program algorithm, a typical command string, and bus operation.

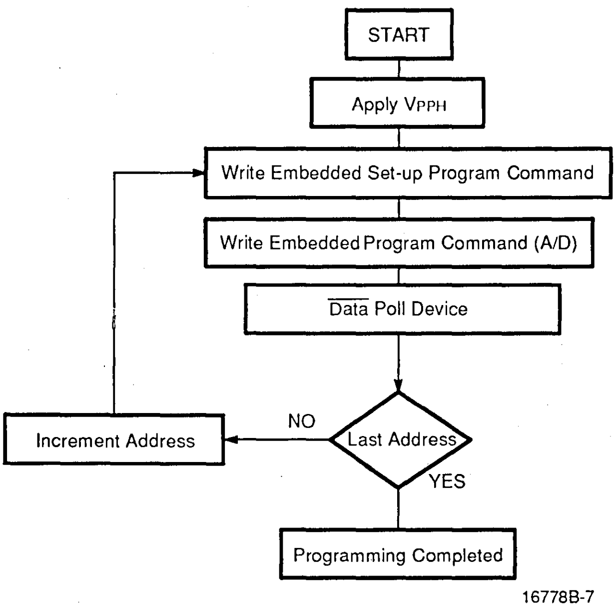


Figure 6. Embedded Program Algorithm

Table 5. Embedded Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Program Set-Up Command	Data = 10H or 50H
Write	Embedded Program Command	Valid Address/Data
Read		$\overline{\text{Data}}$ Polling to Verify Completion
Read		Available for Read Operations

Note:

1. See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Functional Description. Device is either powered-down, erase inhibit or program inhibit.

Write Operation Status

$\overline{\text{Data}}$ Polling—DQ7

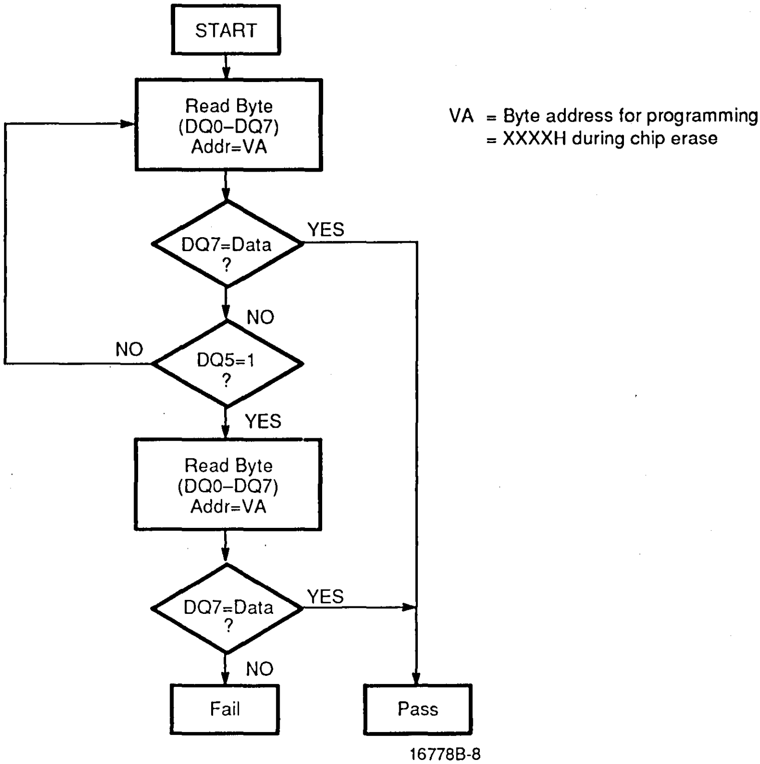
The Am28F010A features $\overline{\text{Data}}$ Polling as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Programming algorithm is in operation, an attempt to read the device at a valid address will produce the complement of expected Valid data on DQ7. Upon completion of the Embedded Program algorithm an attempt to read the device at a valid address will produce Valid data on DQ7. The $\overline{\text{Data}}$ Polling feature is valid after the rising edge of the second $\overline{\text{WE}}$ pulse of the two write pulse sequence.

While the Embedded Erase algorithm is in operation, DQ7 will read "0" until the erase operation is completed. Upon completion of the erase operation, the data on DQ7 will read "1." The $\overline{\text{Data}}$ Polling feature is valid after the rising edge of the second $\overline{\text{WE}}$ pulse of the two Write pulse sequence.

The $\overline{\text{Data}}$ Polling feature is only active during Embedded Programming or erase algorithms.

See Figures 7a and 8a for the $\overline{\text{Data}}$ Polling timing specifications and diagrams. $\overline{\text{Data}}$ Polling is the standard method to check the write operation status, however, an alternative method is available using Toggle Bit.



Note:

1. DQ7 is rechecked even if DQ5="1" because DQ7 may change simultaneously with DQ5 or after DQ5.

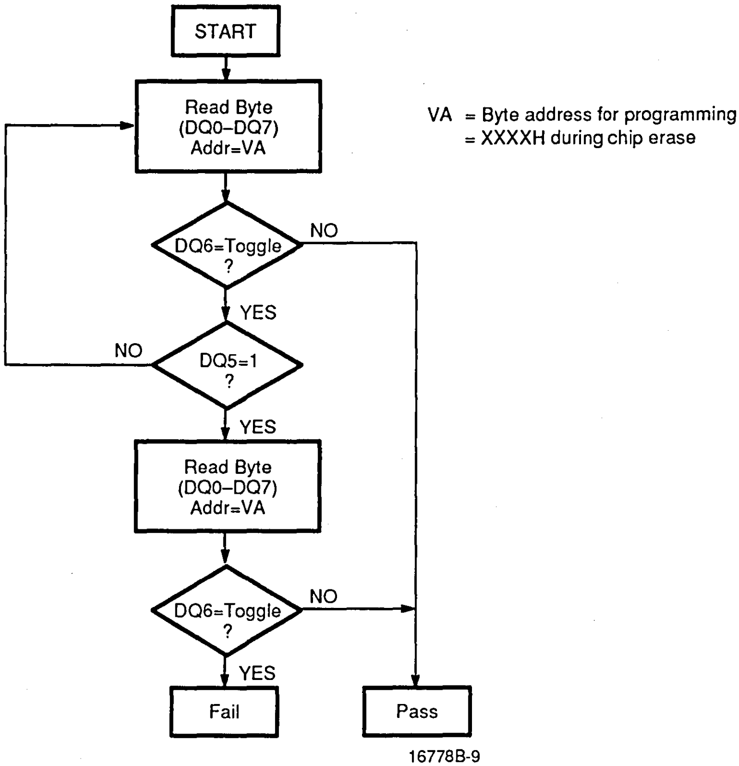
Figure 7a. $\overline{\text{Data}}$ Polling Algorithm

Toggle Bit—DQ6

The Am28F010A also features a "Toggle Bit" as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

Successive attempts to read data from the device at a valid address, while the Embedded Program algorithm is in progress, or at any address while the Embedded Erase algorithm is in progress, will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase algorithm is completed, DQ6 will stop toggling to indicate the completion of either Embedded operation. Only on the next read cycle will valid data be obtained. The toggle bit is valid after the rising edge of the first $\overline{WE}$ pulse of the two write pulse sequence, unlike $\overline{Data}$ Polling which is valid after the rising edge of the second $\overline{WE}$ pulse. This feature allows the user to determine if the device is partially through the two write pulse sequence.

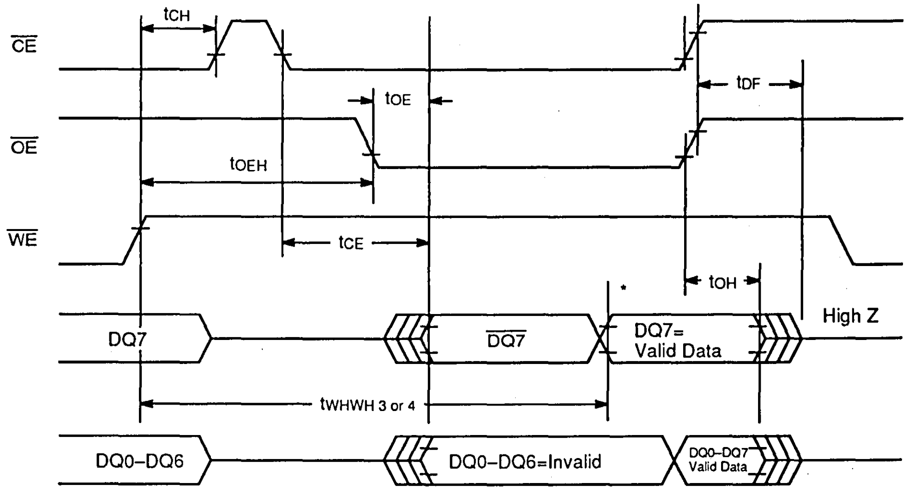
See Figures 7b and 8b for the Toggle Bit timing specifications and diagrams.



Note:

1. DQ6 is rechecked even if DQ5="1" because DQ6 may stop toggling at the same time as DQ5 changing to "1".

Figure 7b. Toggle Bit Algorithm



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Note:

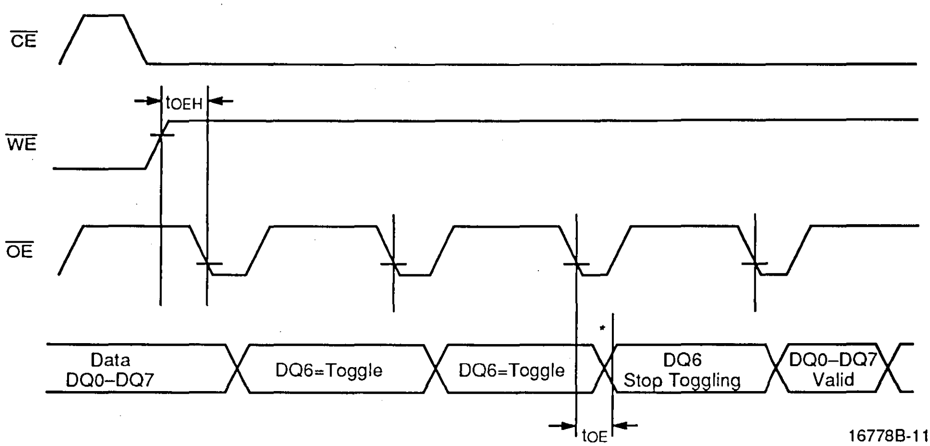
**DQ7=Valid Data (The device has completed the Embedded operation).*

Figure 8a. AC Waveforms for Data Polling During Embedded Algorithm Operations

DQ5

Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits. This is a failure condition and the device may not be used again (internal pulse count exceeded). Under these conditions DQ5 will produce a "1." The program or erase cycle was not successfully completed. $\overline{Data}$ Polling is the only operating function of the device under this condition. The $\overline{CE}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{OE}$ and $\overline{WE}$ pins will control the output disable functions as described in Table 1.



Note:

**DQ6 stops toggling (The device has completed the Embedded operation).*

Figure 8b. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

Parallel Device Erasure

The Embedded Erase algorithm greatly simplifies parallel device erasure. Since the erase process is internal to the device, a single erase command can be given to multiple devices concurrently. By implementing a parallel erase algorithm, total erase time may be minimized.

Note that the Flash memories may erase at different rates. If this is the case, when a device is completely erased, use a masking code to prevent further erasure (over-erasure). The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-Up Sequence

The Am28F010A powers-up in the Read only mode. Power supply sequencing is not required.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset must be written two consecutive times after the Set-up Program command (10H or 50H). This will reset the device to the Read mode.

Following any other Flash command, write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The Set-up Program command (10H or 50H) is the only command that requires a two-sequence reset cycle. The first Reset command is interpreted as program data. However, FFH data is considered as null data during programming operations (memory cells are only programmed from a logical "1" to "0"). The second Reset command safely aborts the programming operation and resets the device to the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the Set-up Program state or not.

In-System Programming Considerations

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the circuit board.

Auto Select Command

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. In order to correctly program any Flash memories in-system, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F010A contains an Auto Select operation to supplement traditional PROM programming methodologies. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H (AMD). A read cycle from address 0001H returns the device code A2H (see Table 2). To terminate the operation, it is necessary to write another valid command, such as Reset (FFH), into the register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages . . . . −65°C to +150°C
Plastic Packages . . . . −65°C to +125°C

Ambient Temperature
with Power Applied . . . . −55°C to + 125°C

Voltage with Respect To Ground
All pins except A9 and V_{PP}
(Note 1) . . . . −2.0 V to +7.0 V

V_{CC} (Note 1) . . . . −2.0 V to +7.0 V

A9 (Note 2) . . . . −2.0 V to +14.0 V

V_{PP} (Note 2) . . . . −2.0 V to +14.0 V

Output Short Circuit Current (Note 3) . . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is −0.5 V. During voltage transitions, inputs may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A9 and V_{PP} pins is −0.5 V. During voltage transitions, A9 and V_{PP} may overshoot V_{SS} to −2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) . . . . 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) . . . . −40°C to +85°C

Extended (E) Devices
Case Temperature (T_C) . . . . −55°C to +125°C

Military (M) Devices
Case Temperature (T_C) . . . . −55°C to +125°C

V_{CC} Supply Voltages
V_{CC} for Am28F010A–X5 . . . . +4.75 V to +5.25 V

V_{CC} for Am28F010A–XX0 . . . . +4.50 V to +5.50 V

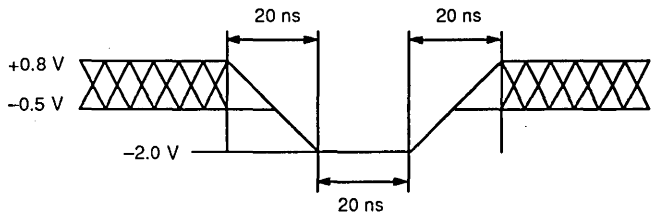
V_{PP} Supply Voltages
Read . . . . −0.5 V to +12.6 V

Program, Erase, and Verify . . . . . +11.4 V to +12.6 V

Operating ranges define those limits between which the funtionality of the device is guaranteed.

MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



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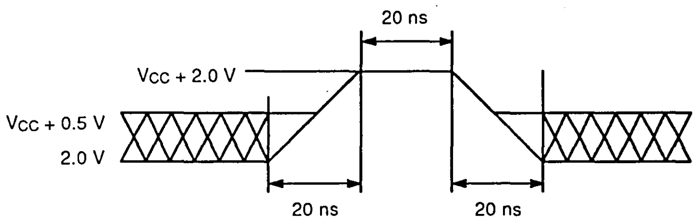
Maximum Positive Input Overshoot



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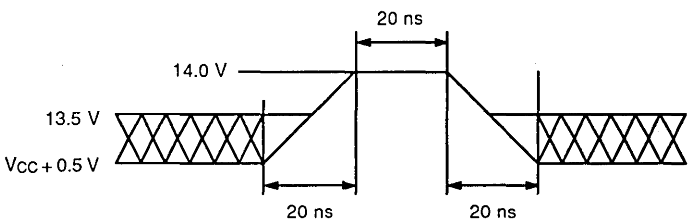
Maximum V_{PP} Overshoot



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DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7, and 8 are tested unless otherwise noted) (Notes 1–4)

DC CHARACTERISTICS-TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{IH}$		0.2	1.0	mA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ $I_{OUT} = 0$ mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress (Note 4)		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress (Note 4)		10	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			±1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	µA
		$V_{PP} = V_{PPL}$			±1.0	µA
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 5.8$ mA $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.5$ mA $V_{CC} = V_{CC}$ Min	2.4			V
V_{ID}	A9 Auto Select Voltage	$A9 = V_{ID}$	11.5		13.0	V
I_{ID}	A9 Auto Select Current	$A9 = V_{ID}$ Max $V_{CC} = V_{CC}$ Max		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:*** *Erase/Program are inhibited when $V_{PP} = V_{PPL}$*	0.0		V_{CC} +2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. ***Caution:*** *the Am28F010A must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
2. *I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.*
3. *Maximum active power usage is the sum of I_{CC} and I_{PP}.*
4. *Not 100% tested.*

DC CHARACTERISTICS—CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS}			± 1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}			± 1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{CC} + 0.5$ V		15	100	µA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ $I_{OUT} = 0$ mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress (Note 4)		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress (Note 4)		10	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			± 1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	µA
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 5.8$ mA $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.5$ mA, $V_{CC} = V_{CC}$ Min	0.85 V_{CC}			V
V_{OH2}		$I_{OH} = -100$ µA, $V_{CC} = V_{CC}$ Min	V_{CC} –0.4			
V_{ID}	A9 Auto Select Voltage	A9 = V_{ID}	11.5		13.0	V
I_{ID}	A9 Auto Select Current	A9 = V_{ID} Max $V_{CC} = V_{CC}$ Max		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:*** *Erase/Program are inhibited when* $V_{PP} = V_{PPL}$	0.0		V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. ***Caution:*** *the Am28F010A must not be removed from (or inserted into) a socket when* V_{CC} *or* V_{PP} *is applied.*
2. I_{CC1} *is tested with* $\overline{OE} = V_{IH}$ *to simulate open outputs.*
3. *Maximum active power usage is the sum of* I_{CC} *and* I_{PP}.
4. *Not 100% tested.*

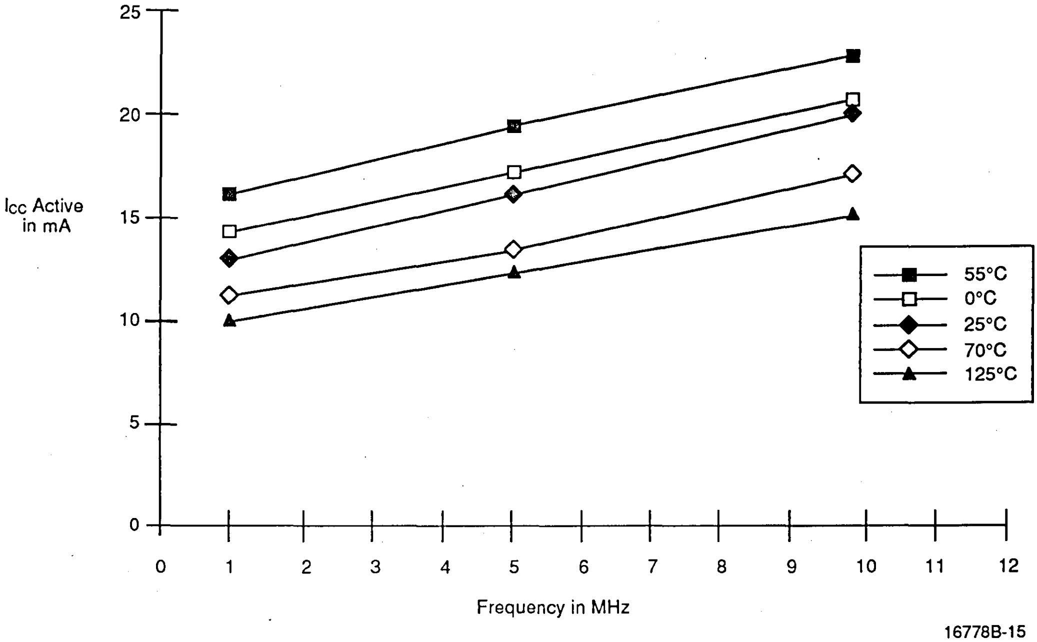


Figure 9. Am28F010A – Average I_{CC} Active vs. Frequency
V_{CC} = 5.5 V, Addressing Pattern = Minmax
Data Pattern = Checkerboard

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	8	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A = 25°C$, $f = 1.0$ MHz*

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

AC CHARACTERISTICS—Read Only Operation (Notes 1–4)

Parameter Symbols				Am28F010A					
JEDEC	Standard	Parameter Description		-90 -95	-120 –	-150 –	-200 –	-250 –	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)	Min Max	90	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min Max	90	120	150	200	250	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min Max	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min Max	35	50	55	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z (Note 4)	Min Max	0	0	0	0	0	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z (Note 3)	Min Max	20	30	35	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z (Note 4)	Min Max	0	0	0	0	0	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z (Note 4)	Min Max	20	30	35	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change (Note 4)	Min Max	0	0	0	0	0	ns
t_{WHGL}		Write Recovery Time before Read	Min Max	6	6	6	6	6	µs
t_{VCS}		V_{CC} Set-up Time to Valid Read (Note 4)	Min Max	50	50	50	50	50	µs

Notes:

1. *Output Load: 1 TTL gate and $C_L = 100$ pF*
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0.45 to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. *The Am28F010A-95 Output Load: 1 TTL gate and $C_L = 100$ pF*
   Input Rise and Fall Times: ≤ 10 ns
   Input Pulse levels: 0 V to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. *Guaranteed by design not tested.*
4. *Not 100% tested.*

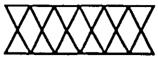
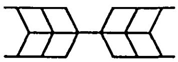
AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1–6)

Parameter Symbols JEDEC	Parameter Symbols Standard	Parameter Description		Am28F010A -90 -95	-120	-150	-200	-250	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 6)	Min Max	90	120	150	200	250	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min Max	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min Max	45	50	60	75	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min Max	45	50	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min Max	10	10	10	10	10	ns
t_{OEH}		Output Enable Hold Time for Embedded Algorithm only (See Figure 8)	Min Max	10	10	10	10	10	ns
t_{GHWL}		Read Recovery Time before Write	Min Max	0	0	0	0	0	µs
t_{ELWLE}	t_{CSE}	Chip Enable Embedded Algorithm Setup Time	Min Max	20	20	20	20	20	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min Max	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min Max	45	50	60	60	60	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min Max	20	20	20	20	20	ns
t_{WHWH3}		Embedded Programming Operation (Note 4)	Min Max	14	14	14	14	14	µs
t_{WHWH4}		Embedded Erase Operation (Note 5)	Typ Max	5	5	5	5	5	s
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 6)	Min Max	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 90% V_{PPL} (Note 6)	Min Max	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 6)	Min Max	100	100	100	100	100	ns

Notes:

1. *Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.*
2. *All devices except Am28F010A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V*
3. *Am28F010A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V*
4. *Embedded Program Operation of 14 µs consists of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.*
5. *Embedded erase operation of 5 sec consists of 4 sec array pre-programming time and one sec array erase time. This is a typical time for one embedded erase operation.*
6. *Not 100% tested.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS

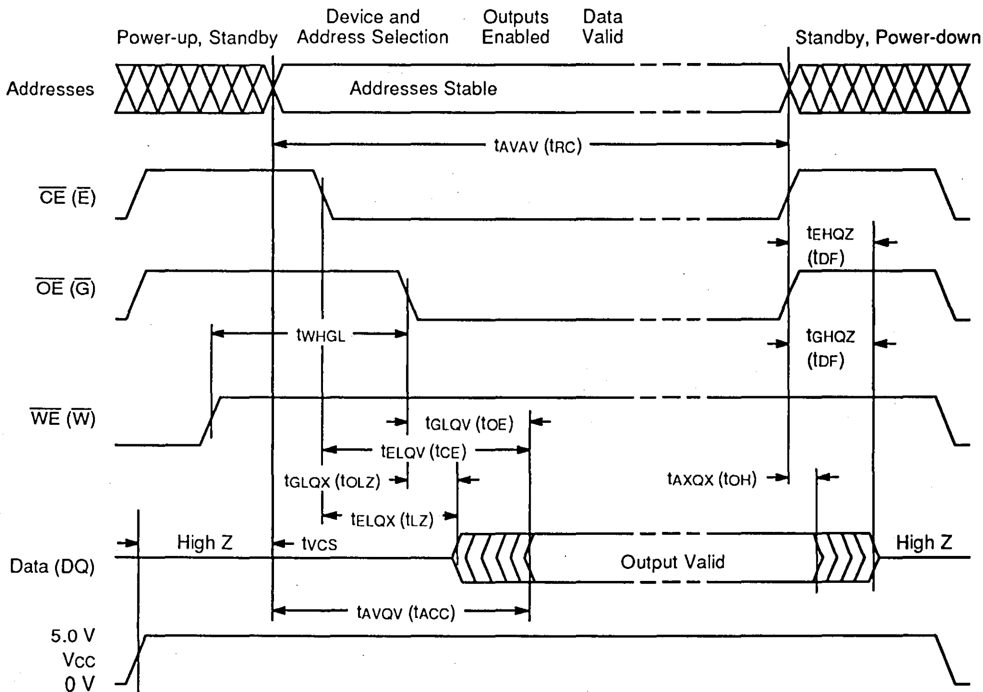


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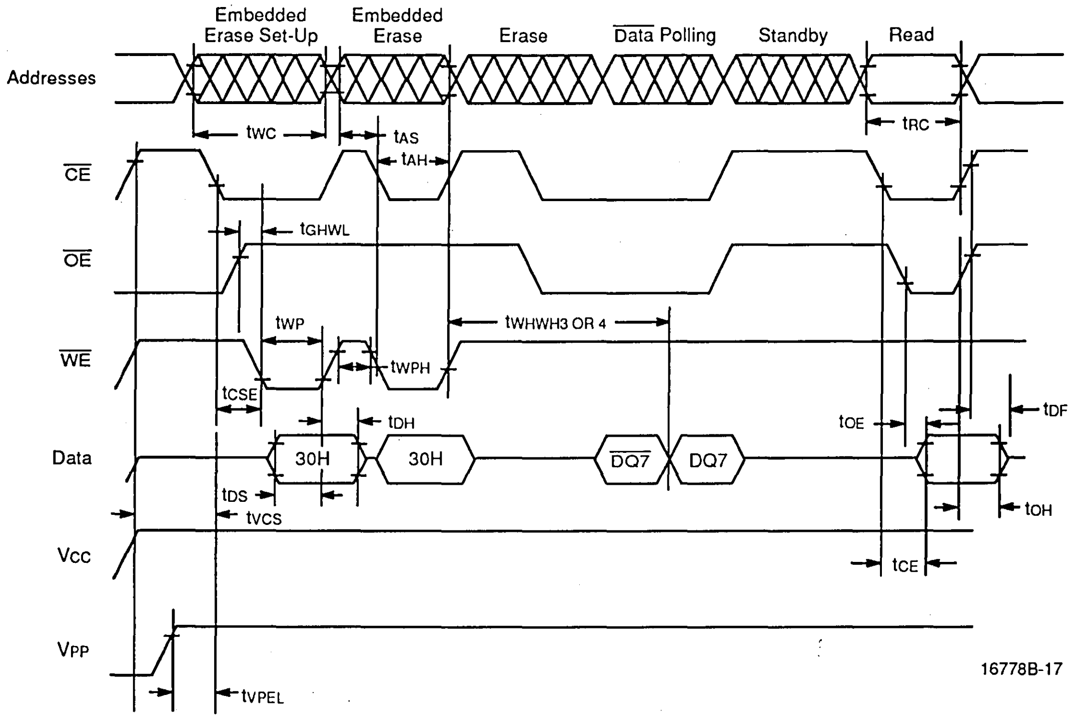
Figure 10. AC Waveforms for Read Operations

SWITCHING WAVEFORMS

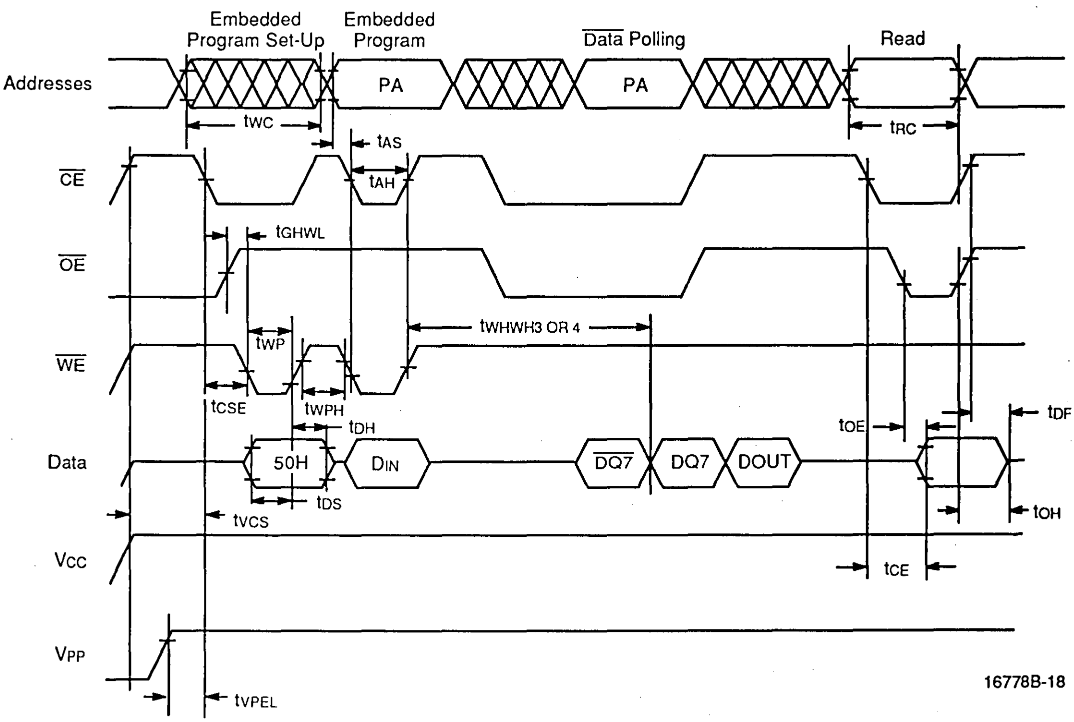


Note:

1. $\overline{DQ7}$ is the output of the complement of the data written to the device.

Figure 11. AC Waveforms for Embedded Erase Operation

SWITCHING WAVEFORMS



Notes:

1. *DIN is data input to the device.*
2. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
3. *DOUT is the output of the data written to the device.*

Figure 12. AC Waveforms for Embedded Programming Operation

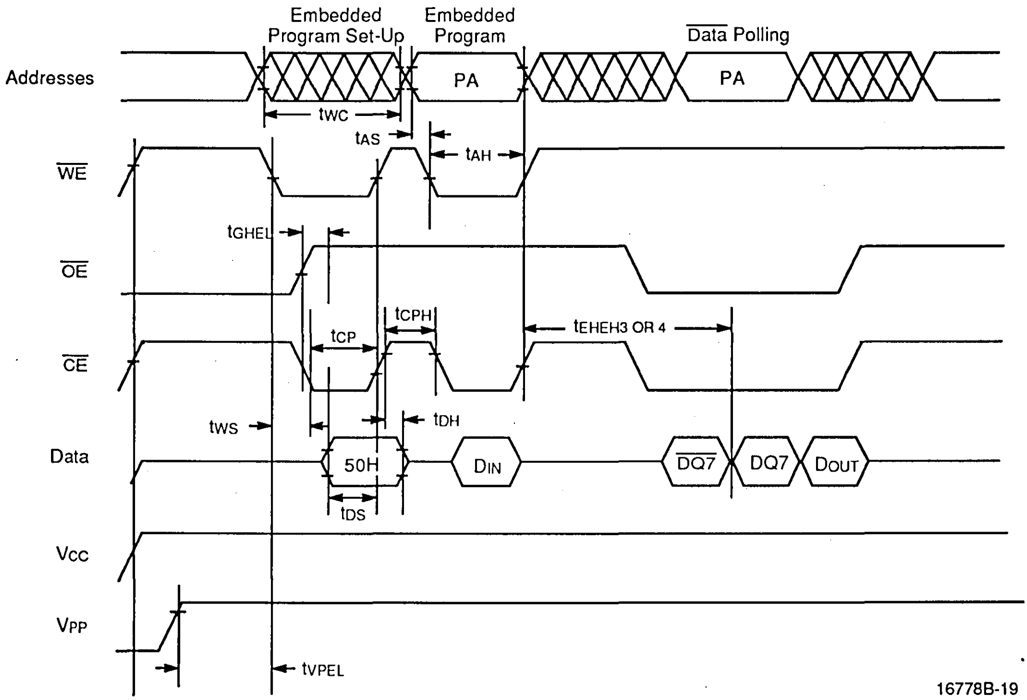
AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1– 6)
Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols				Am28F010A					
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 6)	Min Max	90	120	150	200	250	ns
t_{AVEL}	t_{AS}	Address Set-Up Time	Min Max	0	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min Max	45	50	60	75	75	ns
t_{DVEH}	t_{DS}	Data Set-Up Time	Min Max	45	50	50	50	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min Max	10	10	10	10	10	ns
t_{OEH}		Output Enable Hold Time for Embedded Algorithm only (See Figure 8)	Min Max	10	10	10	10	10	ns
t_{GHEL}		Read Recovery Time Before Write	Min Max	0	0	0	0	0	µs
t_{WLEL}	t_{WS}	WE Set-Up Time by $\overline{CE}$	Min Max	0	0	0	0	0	ns
t_{EHWK}	t_{WH}	WE Hold Time	Min Max	0	0	0	0	0	ns
t_{ELEH}	t_{CP}	Write Pulse Width	Min Max	65	70	80	80	80	ns
t_{EHEL}	t_{CPH}	Write Pulse Width HIGH	Min Max	20	20	20	20	20	ns
t_{EHEH3}		Embedded Programming Operation (Note 4)	Min Max	14	14	14	14	14	µs
t_{EHEH4}		Embedded Erase Operation (Note 5)	Min Max	3	3	3	3	3	s
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 6)	Min Max	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 90% V_{PPL} (Note 6)	Min Max	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 6)	Min Max	100	100	100	100	100	ns

Notes:

1. *Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.*
2. *All devices except Am28F010A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V*
3. *Am28F010A-95. Input Rise and Fall times: ≤ 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V*
4. *Embedded Program Operation of 14 µs consists of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.*
5. *Embedded erase operation of 5 sec consists of 4 sec array pre-programming time and one sec array erase time. This is a typical time for one embedded erase operation.*
6. *Not 100% tested.*

SWITCHING WAVEFORMS

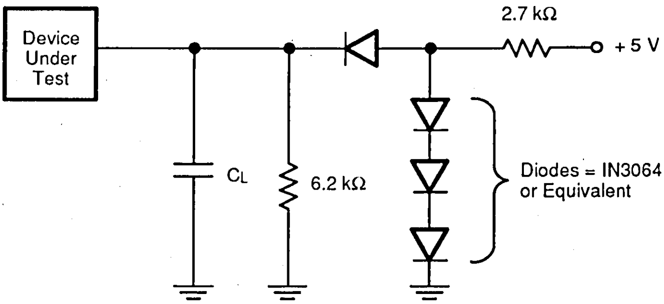


Notes:

1. *D_{IN} is data input to the device.*
2. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
3. *D_{OUT} is the output of the data written to the device.*

Figure 13. AC Waveforms for Embedded Programming Operation Using $\overline{CE}$ Controlled Writes

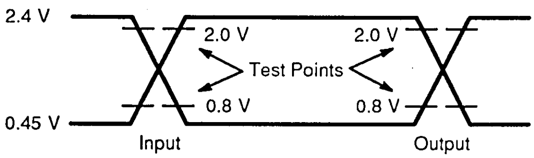
SWITCHING TEST CIRCUIT



16778B-20

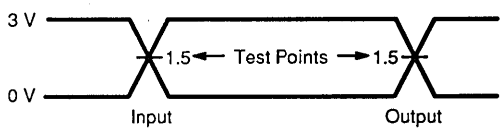
C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORMS



All Devices Except Am28F010A-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are < 10 ns.



For Am28F010A-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are < 10 ns.

16778B-21

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max (Note 3)		
Chip Erase Time		1 (Note 1)	10 (Note 2)	s	Excludes 00H programming prior to erasure
Chip Programming Time		2 (Note 1)	12.5	s	Excludes system-level overhead
Write/Erase Cycles	100,000			Cycles	
Byte Program Time		14		µs	
			96 (Note 4)	ms	

Notes:

1. *25°C, 12 V V_{PP}*
2. *The Embedded algorithm allows for 60 second erase time for military temperature range operations.*
3. *Maximum time specified is lower than worst case. Worst case is derived from the Embedded Algorithm internal counter which allows for a maximum 6000 pulses for both program and erase operations. Typical worst case for program and erase is significantly less than the actual device limit.*
4. *Typical worst case = 84 µs. DQ5 = "1" only after a byte takes longer than 96 ms to program.*

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A9 and V_{PP})	–1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	–1.0 V	V_{CC} + 1.0 V
Current	–100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

DATA SHEET REVISION SUMMARY FOR Am28F010A

Data sheet is Final now, and not Preliminary.

Functional Description – Table 1

Legend: V_{PP} should be less than or equal to V_{CC} + 2 V

Erase, Program, and Read Mode – Write Operations

Removed Command Register Table and Bit assignments.

Erase, Program and Read Mode – Read Command

The statement requiring a 6 µs wait before accessing the first addressed location was removed.

Table 3 – Am28F010A Command Definitions

The note describing a 6 µs wait before accessing the first addressed location was removed.

Figure 5 – Embedded Erase Algorithm

Clarified figure to illustrate the Embedded Erase Algorithm.

Embedded Programming Algorithm

Added references that addresses are also latched on the falling edge of $\overline{CE}$, and data is also latched on the rising edge of $\overline{CE}$, whichever happens later.

Figure 6 – Embedded Programming Algorithm

Clarified figure to illustrate the Embedded Erase Algorithm.

Write Operation Status – $\overline{Data}$ Polling DQ7

Added statement that an attempt to read the device at a valid address will produce valid data on DQ7.

Figure 7a – $\overline{Data}$ Polling Algorithm

Clarified figure to illustrate the $\overline{Data}$ Polling Algorithm.

Write Operation Status – Toggle Bit DQ6

Added statement that successive reads from the device will result in DQ6 toggling between '1' and '0'.

Figure 7b – Toggle Bit Algorithm

Clarified figure to illustrate the Toggle Bit Algorithm

Figure 8a – AC Waveforms for Data Polling During Embedded Algorithm Operations

Clarified figure to illustrate the $\overline{Data}$ Polling Algorithm.

DQ5 – Exceeded Timing Limits

Added statement that this is a failure condition and the device may not be used again.

Figure 8b – AC Waveforms for Toggle Bit During Embedded Algorithm Operations

Clarified figure to illustrate the Toggle Bit Algorithm.

Parallel Device Erasure

Removed erroneous reference.

Reset Command

Added this section.

In-System Programming Considerations

Title was changed.

Auto Select Command

Added second paragraph describing the Auto select command.

DC Characteristics – TTL/NMOS Compatible

Added Note 4 – those characteristics are not 100% tested.

DC Characteristics – CMOS Compatible

Added Note 4 – those characteristics are not 100% tested.

AC Characteristics – Write/Erase/Program Operations (Notes 1–6)

Embedded Programming Operation (t_{WHWH3}) requires minimum of 14 µs

Figure 11 – AC Waveforms for Embedded Erase Operation

$\overline{Data}$ Polling section does not require a Program Address. DQ7 was inserted.

Figure 12 – AC Waveforms for Embedded Programming Operation

Embedded Program section needs a Program Address. DQ7 was inserted.

AC Characteristics – Write/Erase/Program Operations (Notes 1–6)

Alternate $\overline{CE}$ Controlled Writes

Embedded Programming Operation (t_{EHEH3}) requires minimum of 14 µs.

Figure 13 – AC Waveforms for Embedded Programming Operation Using $\overline{CE}$ Controlled Writes

Embedded Program section requires Program Address. DQ7 was inserted. Changed t_{WHWH3} to t_{EHEH3}.

FINAL

Am28F020

2 Megabit (262,144 x 8-Bit) CMOS 12.0 Volt, Bulk Erase Flash Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 90 ns maximum access time
- **CMOS Low power consumption**
  - 30 mA maximum active current
  - 100 µA maximum standby current
  - No data retention power
- **Compatible with JEDEC-standard byte-wide 32-Pin EPROM pinouts**
  - 32-pin DIP
  - 32-pin PLCC
  - 32-pin TSOP
- **10,000 write/erase cycles minimum**
- **Write and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to V_{CC} +1 V**
- **Flasherase Electrical Bulk Chip-Erase**
  - One second typical chip-erase
- **Flashrite Programming**
  - 10 µs typical byte-program
  - Four seconds typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell
- **Automatic write/erase pulse stop timer**

GENERAL DESCRIPTION

The Am28F020 is a 2 Megabit Flash memory organized as 256K bytes of 8 bits each. AMD's Flash memories offer the most cost-effective and reliable read/write non-volatile random access memory. The Am28F020 is packaged in 32-pin PDIP, PLCC, and TSOP versions. The device is also offered in the ceramic DIP package. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers. The Am28F020 is erased when shipped from the factory.

The standard Am28F020 offers access times as fast as 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F020 has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F020 uses a command register to manage this functionality, while maintaining a JEDEC Flash standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming.

AMD's Flash technology reliably stores memory contents even after 10,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F020 uses a 12.0 V ± 5% V_{PP} supply to perform the Flasherase and Flashrite algorithms.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1 V to V_{CC} +1 V.

The Am28F020 is byte programmable using 10 µs programming pulses in accordance with AMD's Flashrite programming algorithm. The typical room temperature programming time of the Am28F020 is four seconds. The entire chip is bulk erased using 10 ms erase pulses according to AMD's Flasherase alrogithm. Typical erasure at room temperature is accomplished in less than one second. The windowed package and the 15–20 minutes required for EPROM erasure using ultra-violet light are eliminated.

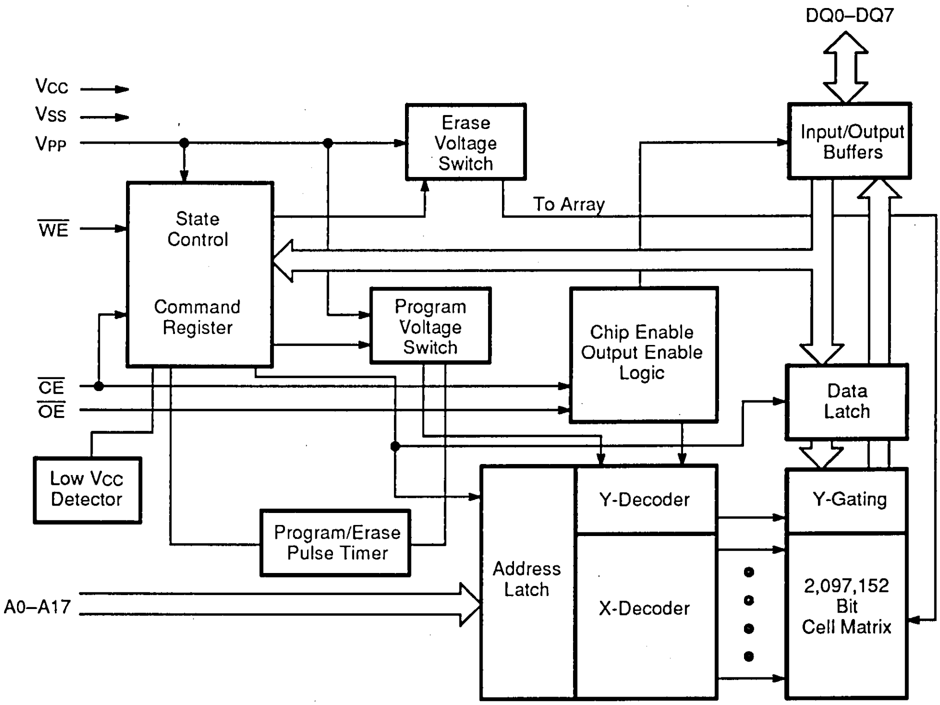
Publication# 14727 Rev. D Amendment/0
Issue Date: March 1994

GENERAL DESCRIPTION

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F020 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

AMD's Flash technology combines years of EPROM and EEPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F020 electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

BLOCK DIAGRAM



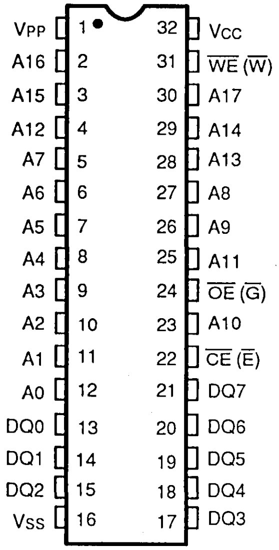
14727D-1

PRODUCT SELECTOR GUIDE

Family Part No.	Am28F020				
Ordering Part No: Vcc ±5%	-90	-120	-150	-200	-250
Vcc ±10%	-95				
Max Access Time (ns)	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	50	55	55	55

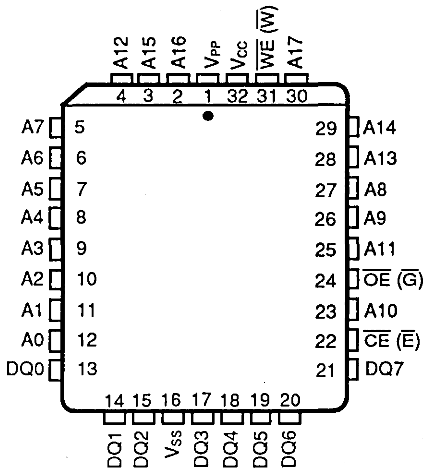
CONNECTION DIAGRAMS

DIP



14727D-2

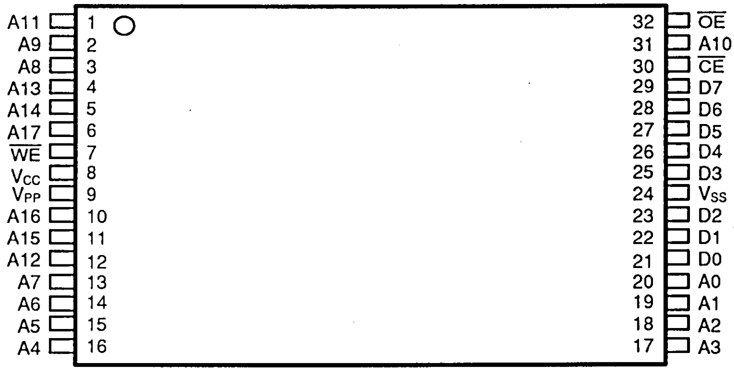
PLCC



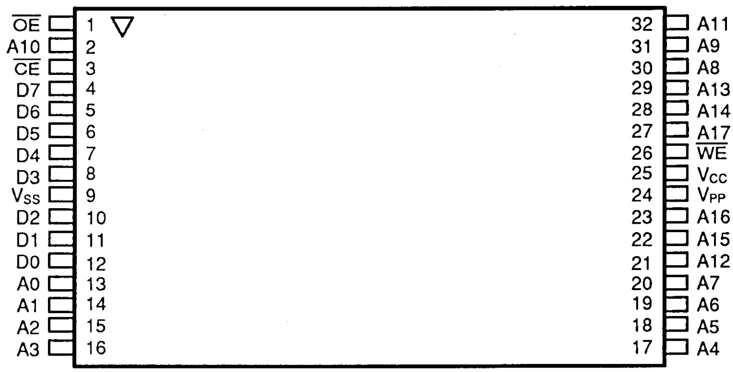
14727D-3

Note: *Pin 1 is marked for orientation.*

TSOP PACKAGES



28F020 Standard Pinout

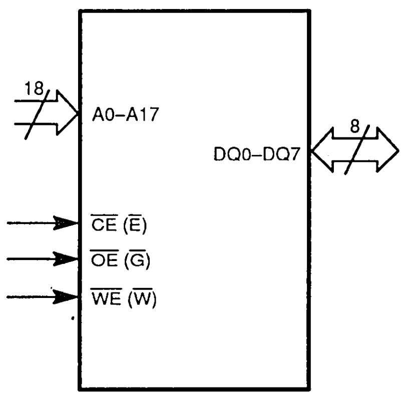


28F020 Reverse Pinout

14727D-4

28F020 256K x 8 Flash Memory in 32-Lead TSOP

LOGIC SYMBOL



14727D-5

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

AM28F020 -95 J C B

OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-In

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to + 85°C)
E = Extended (–55°C to + 125°C)

PACKAGE TYPE
P = 32-Pin Plastic DIP (PD 032)
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)
D = 32-Pin Ceramic DIP (CD 032)
E = 32-Pin TSOP Standard Pinout (TS 032)
F = 32-Pin TSOP Reverse Pinout (TSR 032)

SPEED
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am28F020
2 Megabit (256K x 8-Bit) CMOS Flash Memory

Valid Combinations	
AM28F020-90 AM28F020-95	PC, JC, DC, EC, FC
AM28F020-120 AM28F020-150 AM28F020-200	PC, PI, PE, PEB, JC, JI, JE, JEB, DC, DI, DE, DEB, EC, FC, EI, FI, EE, FE, EEB, FEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

AM28F020 -120 /B X A

LEAD FINISH
A = Hot Solder Dip

PACKAGE TYPE
X = 32-Pin Ceramic DIP (CD 032)

DEVICE CLASS
/B = Class B

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am28F020
2 Megabit (256K x 8-Bit) CMOS Flash Memory

Valid Combinations	
AM28F020-120	/BXA
AM28F020-150	
AM28F020-200	
AM28F020-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

A0–A17
Address Inputs for memory locations. Internal latches hold addresses during write cycles.

$\overline{CE}$ ($\overline{E}$)
The Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.

DQ0–DQ7
Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

NC
No Connect-corresponding pin is not connected internally to the die.

$\overline{OE}$ ($\overline{G}$)
The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

V_{CC}
Power supply for device operation. (5.0 V ± 5% or 10%)

V_{PP}
Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2$ V.

V_{SS}
Ground

$\overline{WE}$ ($\overline{W}$)
The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

BASIC PRINCIPLES

The Am28F020 uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0 V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F020 functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F020's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F020 is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Flasherase Sequence

A multiple step command sequence is required to erase the Flash device (a two-cycle Erase command and repeated one cycle verify commands).

Note: *The Flash memory array must be completely programmed to O's prior to erasure. Refer to the Flashrite Programming.*

1. **Erase Set-Up:** Write the Set-up Erase command to the command register.
2. **Erase:** Write the Erase command (same as Set-up Erase command) to the command register again. The second command initiates the erase operation. The system software routines must now time-out the erase pulse width (10 ms) prior to issuing the Erase-verify command. An integrated stop timer prevents any possibility of overerasure.
3. **Erase-Verify:** Write the Erase-verify command to the command register. This command terminates the erase operation. After the erase operation, each byte of the array must be verified. Address information must be supplied with the Erase-verify command. This command verifies the margin and outputs the addressed byte in order to compare the array data with FFH data (Byte erased). After successful data verification the Erase-verify command is written again with new address information. Each byte of the array is sequentially verified in this manner.

If data of the addressed location is not verified, the Erase sequence is repeated until the entire array is successfully verified or the sequence is repeated 1000 times.

Flashrite Programming Sequence

A three step command sequence (a two-cycle Program command and one cycle Verify command) is required to program a byte of the Flash array. Refer to the Flashrite Algorithm.

1. **Program Set-Up:** Write the Set-up Program command to the command register.
2. **Program:** Write the Program command to the command register with the appropriate Address and Data. The system software routines must now time-out the program pulse width (10 µs) prior to issuing the Program-verify command. An integrated stop timer prevents any possibility of overprogramming.
3. **Program-Verify:** Write the Program-verify command to the command register. This command terminates the programming operation. In addition, this command verifies the margin and outputs the byte just programmed in order to compare the array data with the original data programmed. After successful data verification, the programming sequence is initiated again for the next byte address to be programmed.

If data is not verified successfully, the Program sequence is repeated until a successful comparison is verified or the sequence is repeated 25 times.

Data Protection

The Am28F020 is designed to offer protection against accidental erasure or programming, caused by spurious system level signals that may exist during power transitions. The Am28F020 powers up in its read only state. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting from V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. The device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 10 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

FUNCTIONAL DESCRIPTION

Description of User Modes

Table 1. Am28F020 User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A0	A9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A0	A9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (2AH)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A0	A9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A0	A9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} < V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An < V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. *V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} +2.0 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.*
2. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.*
3. *$11.5 < V_{ID} < 13.0$ V*
4. *Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.*
5. *With V_{PP} at high voltage, the standby current is $I_{CC} + I_{PP}$ (standby).*
6. *Refer to Table 3 for valid D_{IN} during a write operation.*
7. *All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A9 and A0 must be held at V_{IL}.*

READ ONLY MODE

$V_{PP} < V_{CC} + 2$ V
Command Register Inactive

Read

The Am28F020 functions as a read only memory when $V_{PP} < V_{CC} + 2$ V. The Am28F020 has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least t_{ACC}–t_{OE}).

Standby Mode

The Am28F020 has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), consumes less than 100 µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A PROM Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13.0 V) on address A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to V_{CC} + 2.0 V while using this Auto select mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the Am28F020 these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F020 Auto Select Code

Type	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	2A	0	0	1	0	1	0	1	0

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%

Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 3 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Am28F020 Command Definitions

Command	First Bus Cycle			Second Bus Cycle		
	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 6)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/2AH
Erase Set-up/EraseWrite (Note 4)	X	20H	Write	X	20H	
Erase-Verify (Note 4)	Write	EA	A0H	Read	X	EVD
Program Set-up/ Program (Note 5)	Write	X	40H	Write	PA	PD
Program-Verify (Note 5)	Write	X	C0H	Read	X	PVD
Reset (Note 6)	Write	X	FFH	Write	X	FFH

Notes:

1. *Bus operations are defined in Table 1.*
2. *RA = Address of the memory location to be read.*
   EA = Address of the memory location to be read during erase-verify.
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   X = Don't care.
3. *RD = Data read from location RA during read operation.*
   EVD = Data read from location EA during erase-verify.
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
   PVD = Data read from location PA during program-verify. PA is latched on the Program command.
4. *Figure 1 illustrates the Flasherase Electrical Erase Algorithm.*
5. *Figure 3 illustrates the Flashrite Programming Algorithm.*
6. *Please reference Reset Command section.*

FLASH MEMORY PROGRAM/ERASE OPERATIONS

AMD's Flasherase and Flashrite Algorithms

Flasherase Erase Sequence

Erase Set-Up/Erase Commands

Erase Set-Up

Erase Set-up is the first of a two-cycle erase command. It is a command-only operation that stages the device for bulk chip erase. The array contents are not altered with this command. 20H is written to the command register in order to perform the Erase Set-up operation.

Erase

The second two-cycle erase command initiates the bulk erase operation. You must write the Erase command (20H) again to the register. The erase operation begins with the rising edge of the $\overline{WE}$ pulse. The erase operation must be terminated by writing a new command (Erase-verify) to the register.

This two step sequence of the Set-up and Erase commands helps to ensure that memory contents are not accidentally erased. Also, chip erasure can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be altered. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

Note: *The Flash memory device must be fully programmed to 00H data prior to erasure. This equalizes the charge on all memory cells ensuring reliable erasure.*

Erase-Verify Command

The erase operation erases all bytes of the array in parallel. After the erase operation, all bytes must be sequentially verified. The Erase-verify operation is initiated by writing A0H to the register. The byte address to be verified must be supplied with the command. Addresses are latched on the falling edge of the $\overline{WE}$ pulse or $\overline{CE}$ pulse, whichever happens later. The rising edge of the $\overline{WE}$ pulse terminates the erase operation.

Margin Verify

During the Erase-verify operation, the Am28F020 applies an internally generated margin voltage to the addressed byte. Reading FFH from the addressed byte indicates that all bits in the byte are properly erased.

Verify Next Address

You must write the Erase-verify command with the appropriate address to the register prior to verification of each address. Each new address is latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later. The process continues for each byte in the memory array until a byte does not return FFH data or all the bytes in the array are accessed and verified.

If an address is not verified to FFH data, the entire chip is erased again (refer to Erase Set-up/Erase). Erase verification then resumes at the address that failed to verify. Erase is complete when all bytes in the array have been verified. The device is now ready to be programmed. At this point, the verification operation is terminated by writing a valid command (e.g. Program set-up) to the command register. Figure 1 and Table 4, the Flasherase electrical erase algorithm, illustrate how commands and bus operations are combined to perform electrical erasure. Refer to AC Erase Characteristics and Waveforms for specific timing parameters.

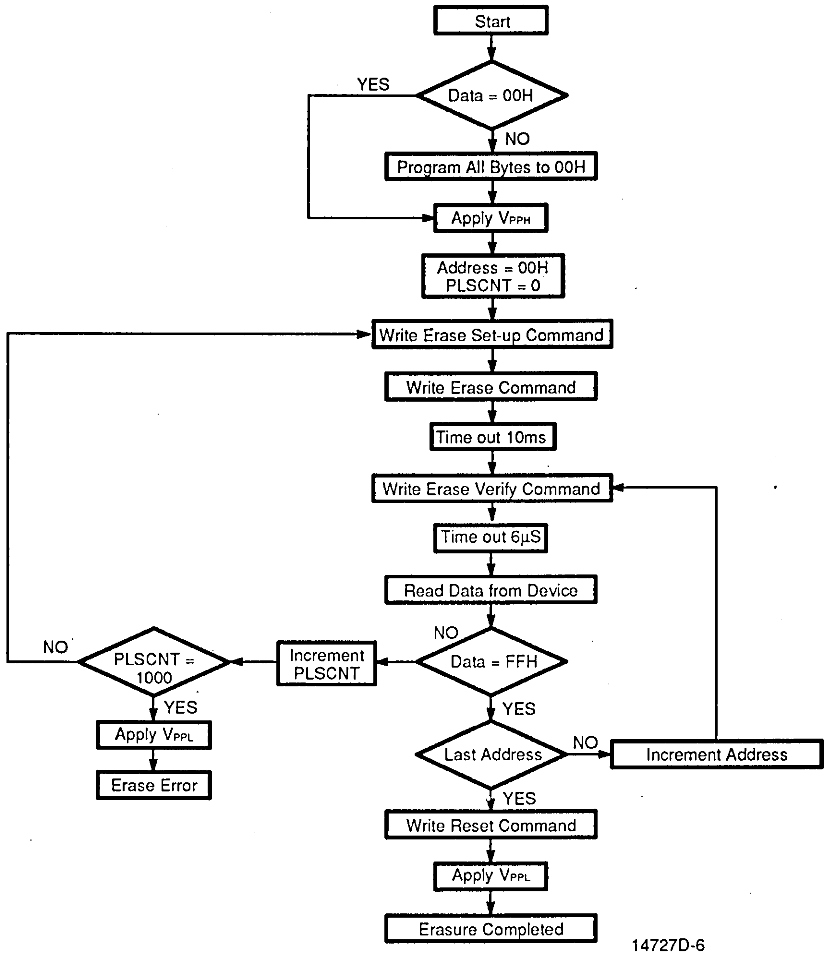


Figure 1. Flasherase Electrical Erase Algorithm

Flasherase Electrical Erase Algorithm

This Flash memory device erases the entire array in parallel. The erase time depends on V_{PP}, temperature, and number of erase/program cycles on the device. In general, reprogramming time increases as the number of erase/program cycles increases.

The Flasherase electrical erase algorithm employs an interactive closed loop flow to simultaneously erase all bits in the array. Erasure begins with a read of the memory contents. The Am28F020 is erased when shipped from the factory. Reading FFH data from the device would immediately be followed by executing the Flashrite programming algorithm with the appropriate data pattern.

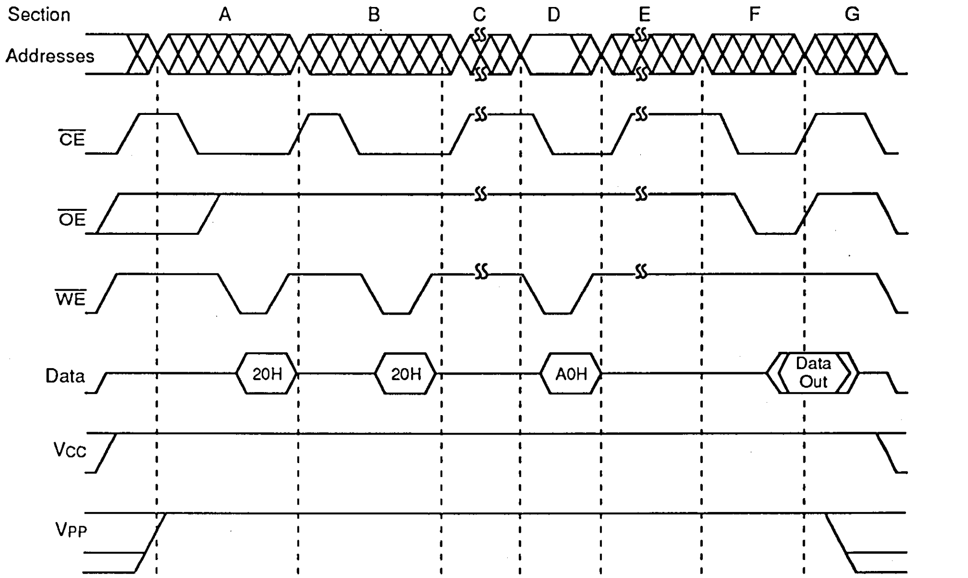
Should the device be currently programmed, data other than FFH will be returned from address locations. Follow the Flasherase algorithm. Uniform and reliable erasure is ensured by first programming all bits in the device to their charged state (Data = 00H). This is accomplished using the Flashrite Programming algorithm. Erasure then continues with an initial erase operation. Erase verification (Data = FFH) begins at address 0000H and continues through the array to the last address, or until data other than FFH is encountered. If a byte fails to verify, the device is erased again. With each erase operation, an increasing number of bytes verify to the erased state. Typically, devices are erased in less than 100 pulses (one second). Erase efficiency may be improved by storing the address of the last byte that fails to verify in a register. Following the next erase operation, verification may start at the stored address location. A total of 1000 erase pulses are allowed per reprogram cycle, which corresponds to approximately 10 seconds of cumulative erase time. The entire sequence of erase and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 1 illustrates the electrical erase algorithm.

Table 4. Flasherase Electrical Erase Algorithm

Bus Operations	Command	Comments
		Entire memory must = 00H before erasure (Note 3) ***Note:*** *Use Flashrite programming algorithm (Figure 3) for programming.*
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize: Addresses PLSCNT (Pulse count)
Write	Erase Set-Up	Data = 20H
Write	Erase	Data = 20H
Standby		Duration of Erase Operation (t_{WHWH2})
Write	Erase-Verify (Note 2)	Address = Byte to Verify Data = A0H Stops Erase Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify erasure
Standby		Compare output to FFH Increment pulse count
Write	Reset	Data = FFH, reset the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. *See DC Characteristics for value of V_{PPH} or V_{PPL}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.*
2. *Erase Verify is performed only after chip erasure. A final read compare may be performed (optional) after the register is written with the read command.*
3. *The erase algorithm* ***Must Be Followed*** *to ensure proper and reliable operation of the device.*



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	20H	20H	N/A	A0H	N/A	Compare Data	N/A
Function	Erase Set-up	Erase	Erase (10 ms)	Erase-Verify	Transition (6 µs)	Erase Verification	Proceed per Erase Algorithm

Figure 2. A.C. Waveforms For Erase Operations

Analysis of Erase Timing Waveform

Note: *This analysis does not include the requirement to program the entire array to 00H data prior to erasure. Refer to the Flashrite Programming.*

Erase Set-Up/Erase

This analysis illustrates the use of two-cycle erase commands (section A and B). The first erase command (20H) is a set-up command and does not affect the array data (section A). The second erase command (20H) initiates the erase operation (section B) on the rising edge of this $\overline{WE}$ pulse. All bytes of the memory array are erased in parallel. No address information is required.

The erase pulse occurs in section C.

Time-Out

A software timing routine (10 ms duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Note: *An integrated stop timer prevents any possibility of overerasure by limiting each time-out period of 10 ms.*

Erase-Verify

Upon completion of the erase software timing routine, the microprocessor must write the Erase-verify command (A0H). This command terminates the erase operation on the rising edge of the $\overline{WE}$ pulse (section D). The Erase-verify command also stages the device for data verification (section F).

After each erase operation each byte must be verified. The byte address to be verified must be supplied with the Erase-verify command (section D). Addresses are latched on the falling edge of the $\overline{WE}$ pulse.

Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operation (section E).

During Erase-verification (section F) each address that returns FFH data is successfully erased. Each address of the array is sequentially verified in this manner by repeating sections D thru F until the entire array is verified or an address fails to verify. Should an address location fail to verify to FFH data, erase the device again. Repeat sections A thru F. Resume verification (section D) with the failed address.

Each data change sequence allows the device to use up to 1,000 erase pulses to completely erase. Typically 100 erase pulses are required.

Note: *All address locations must be programmed to 00H prior to erase. This equalizes the charge on all memory cells and ensures reliable erasure.*

Flashrite Programming Sequence

Program Set-Up/Program Command

Program Set-Up

The Am28F020 is programmed byte by byte. Bytes may be programmed sequentially or at random. Program Set-up is the first of a two-cycle program command. It stages the device for byte programming. The Program Set-up operation is performed by writing 40H to the command register.

Program

Only after the program set-up operation is completed will the next $\overline{WE}$ pulse initiate the active programming operation. The appropriate address and data for programming must be available on the second $\overline{WE}$ pulse. Addresses and data are internally latched on the falling and rising edge of the $\overline{WE}$ pulse respectively. The rising edge of $\overline{WE}$ also begins the programming operation. You must write the Program-verify command to terminate the programming operation. This two step sequence of the Set-up and Program commands helps to ensure that memory contents are not accidentally written. Also, programming can only occur when high voltage is applied to the V_{PP} pin and all control pins are in their proper state. In absence of this high voltage, memory contents cannot be programmed.

Refer to AC Characteristics and Waveforms for specific timing parameters.

Program Verify Command

Following each programming operation, the byte just programmed must be verified.

Write C0H into the command register in order to initiate the Program-verify operation. The rising edge of this $\overline{WE}$ pulse terminates the programming operation. The Program-verify operation stages the device for verification of the last byte programmed. Addresses were previously latched. No new information is required.

Margin Verify

During the Program-verify operation, the Am28F020 applies an internally generated margin voltage to the addressed byte. A normal microprocessor read cycle outputs the data. A successful comparison between the programmed byte and the true data indicates that the byte was successfully programmed. The original programmed data should be stored for comparison. Programming then proceeds to the next desired byte location. Should the byte fail to verify, reprogram (refer to Program Set-up/Program). Figure 3 and Table 5 indicate how instructions are combined with the bus operations to perform byte programming. Refer to AC Programming Characteristics and Waveforms for specific timing parameters.

Flashrite Programming Algorithm

The Am28F020 Flashrite Programming algorithm employs an interactive closed loop flow to program data byte by byte. Bytes may be programmed sequentially or at random. The Flashrite Programming algorithm uses 10 ms programming pulses. Each operation is followed by a byte verification to determine when the addressed byte has been successfully programmed. The program algorithm allows for up to 25 programming operations per byte per reprogramming cycle. Most bytes verify after the first or second pulse. The entire sequence of programming and byte verification is performed with high voltage applied to the V_{PP} pin. Figure 3 and Table 5 illustrate the programming algorithm.

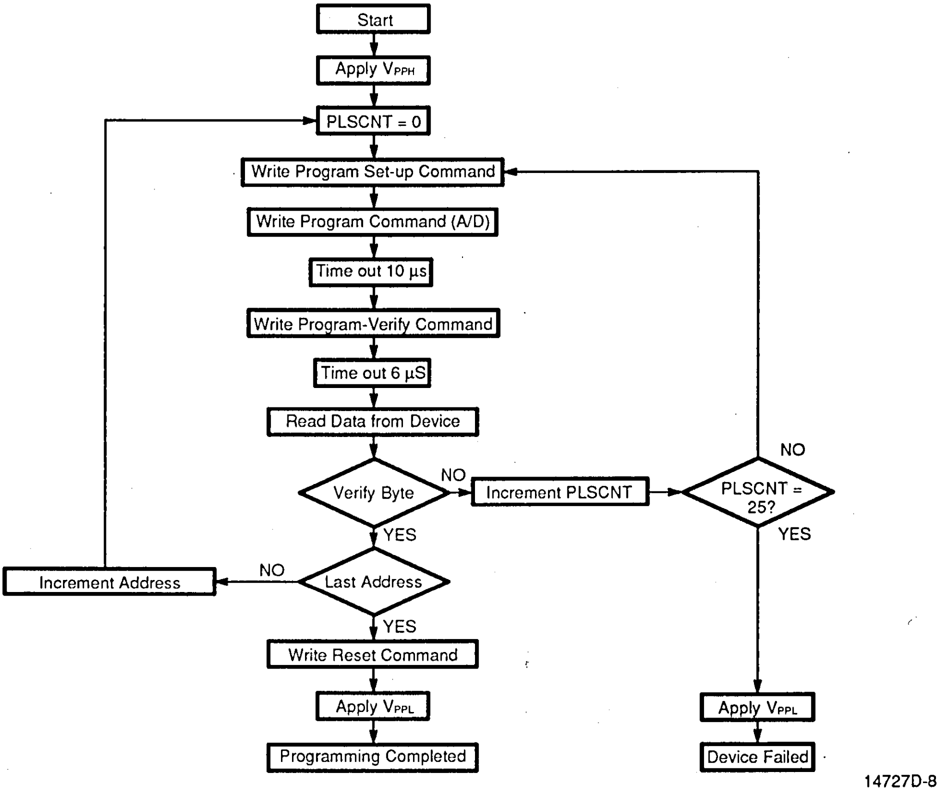


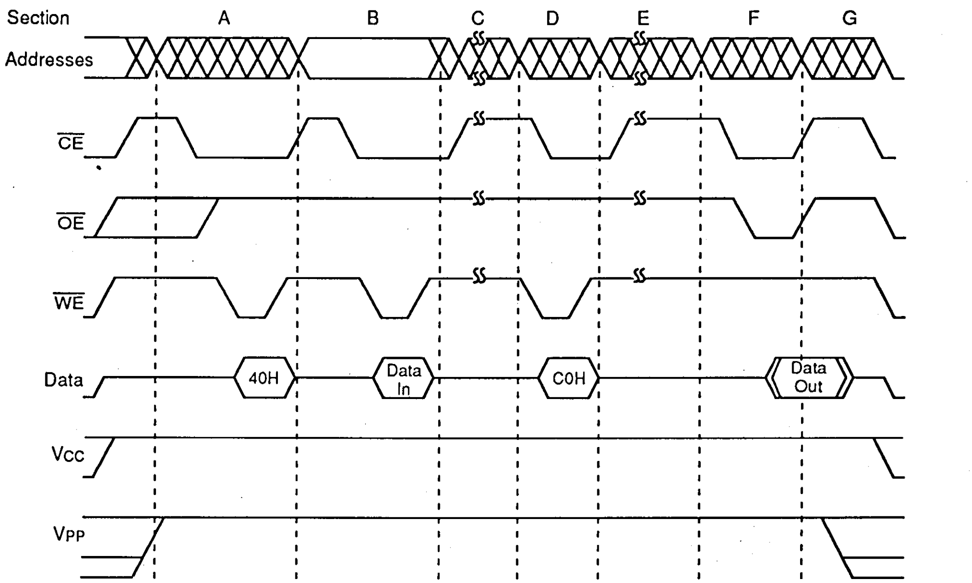
Figure 3. Flashrite Programming Algorithm

Table 5. Flashrite Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} ramp to V_{PPH} (Note 1) Initialize pulse counter
Write	Program Set-Up	Data = 40H
Write	Program	Valid Address/Data
Standby		Duration of Programming Operation (t_{WHWH1})
Write	Program-Verify (2)	Data = C0H Stops Program Operation
Standby		Write Recovery Time before Read = 6 µs
Read		Read byte to verify programming
Standby		Compare data output to data expected
Write	Reset	Data = FFH, resets the register for read operations.
Standby		Wait for V_{PP} ramp to V_{PPL} (Note 1)

Notes:

1. *See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V.*
2. *Program Verify is performed only after byte programming. A final read/compare may be performed (optional) after the register is written with the read command.*



	A	B	C	D	E	F	G
Bus Cycle	Write	Write	Time -out	Write	Time -out	Read	Stand by
Command	40H	Program Address, Program Data	N/A	C0H (Stops Program)	N/A	Compare Data	N/A
Function	Program Set-up	Program Command Latch Address & Data	Program (10 µs)	Program Verify	Transition (6 µs)	Program Verification	Proceed per Programming Algorithm

Figure 4. A.C. Waveforms for Programming Operations

Analysis of Program Timing Waveforms

Program Set-Up/Program

Two-cycle write commands are required for program operations (section A and B). The first program command (40H) is a set-up command and does not affect the array data (section A). The second program command latches address and data required for programming on the falling and rising edge of $\overline{WE}$ respectively (section B). The rising edge of this $\overline{WE}$ pulse (section B) also initiates the programming pulse. The device is programmed on a byte by byte basis either sequentially or randomly.

The program pulse occurs in section C.

Time-Out

A software timing routine (10 µs duration) must be initiated on the rising edge of the $\overline{WE}$ pulse of section B.

Note: *An integrated stop timer prevents any possibility of overprogramming by limiting each time-out period of 10 µs.*

Program-Verify

Upon completion of the program timing routine, the microprocessor must write the program-verify command (C0H). This command terminates the programming operation on the rising edge of the $\overline{WE}$ pulse (section D). The program-verify command also stages the device for data verification (section F). Another software timing routine (6 µs duration) must be executed to allow for generation of internal voltages for margin checking and read operations (section E).

During program-verification (section F) each byte just programmed is read to compare array data with original program data. When successfully verified, the next desired address is programmed. Should a byte fail to verify, reprogram the byte (repeat section A thru F). Each data change sequence allows the device to use up to 25 program pulses per byte. Typically, bytes are verified within one or two pulses.

Algorithm Timing Delays

There are four different timing delays associated with the Flasherase and Flashrite algorithms:

1. The first delay is associated with the V_{PP} rise-time when V_{PP} first turns on. The capacitors on the V_{PP} bus cause an RC ramp. After switching on the V_{PP}, the delay required is proportional to the number of devices being erased and the 0.1µF/device. V_{PP} must reach its final value 100 ns before commands are executed.
2. The second delay time is the erase time pulse width (10 ms). A software timing routine should be run by the local microprocessor to time out the delay. The erase operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the erase operation. To ensure proper device operation, write the Erase-verify operation after each pulse.
3. A third delay time is required for each programming pulse width (10 µs). The programming algorithm is interactive and verifies each byte after a program pulse. The program operation must be terminated at the conclusion of the timing routine or prior to executing any system interrupts that may occur during the programming operation.
4. A fourth timing delay associated with both the Flasherase and Flashrite algorithms is the write recovery time (6 µs). During this time internal circuitry is changing voltage levels from the erase/program level to those used for margin verify and read operations. An attempt to read the device during this period will result in possible false data (it may appear the device is not properly erased or programmed).

Note: *Software timing routines should be written in machine language for each of the delays. Code written in machine language requires knowledge of the appropriate microprocessor clock speed in order to accurately time each delay.*

Parallel Device Erasure

Many applications will use more than one Flash memory device. Total erase time may be minimized by implementing a parallel erase algorithm. Flash memories may erase at different rates. Therefore each device must be verified separately. When a device is completely erased and verified use a masking code to prevent further erasure. The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-Up Sequence

The Am28F020 powers-up in the Read only mode. Power supply sequencing is not required.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset command must be written two consecutive times after the set-up Program command (40H). This will reset the device to the Read mode.

Following any other Flash command write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The set-up Program command (40H) is the only command that requires a two sequence reset cycle. The first Reset command is interpreted as program data. However, FFH data is considered null data during programming operations (memory cells are only programmed from a logical "1" to "0"). The second Reset command safely aborts the programming operation and resets the device to the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue the Reset command two consecutive times. This eliminates the need to determine if you are in the set-up Program state or not.

Programming In-System

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

Auto Select Command

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. Accordingly, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F020 contains an Auto Select operation to supplement traditional PROM programming methodology. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H. A read cycle from address 0001H returns the device code 2AH (see Table 2). To terminate the operation, it is necessary to write another valid command, such as Reset (FFH), into the register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages .... –65°C to +150°C
Plastic Packages .... –65°C to +125°C

Ambient Temperature
with Power Applied .... –55°C to + 125°C

Voltage with Respect To Ground
All pins except A9 and V_{PP}
(Note 1) .... –2.0 V to +7.0 V

V_{CC} (Note 1) .... –2.0 V to +7.0 V

A9 (Note 2) .... –2.0 V to +14.0 V

V_{PP} (Note 2) .... –2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ...... 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A_9 and V_{PP} pins is –0.5 V. During voltage transitions, A9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) .... 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) .... –40°C to +85°C

Extended (E) Devices
Case Temperature (T_C) .... –55°C to +125°C

Military (M) Devices
Case Temperature (T_C) .... –55°C to +125°C

V_{CC} Supply Voltages
V_{CC} for Am28F020–X5 .... +4.75 V to +5.25 V

V_{CC} for Am28F020–XX0 .... +4.50 V to +5.50 V

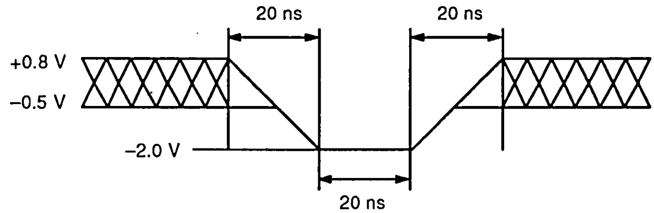
V_{PP} Supply Voltages
Read .... –0.5 V to +12.6 V

Program, Erase, and Verify ..... +11.4 V to +12.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

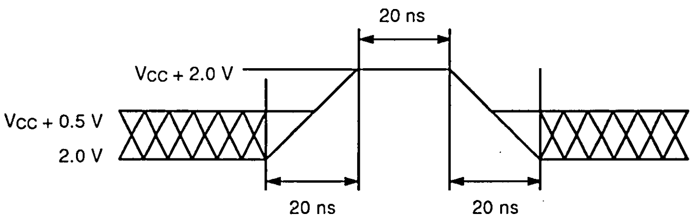
MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



14727D-10

Maximum Positive Input Overshoot



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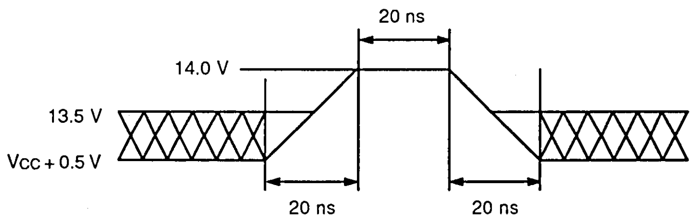
Maximum V_{PP} Overshoot



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DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7, and 8 are tested unless otherwise noted) (Notes 1–4)

DC CHARACTERISTICS—TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{IH}$		0.2	1.0	mA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ $I_{OUT} = 0$ mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress (Note 4)		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress (Note 4)		10	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			±1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	µA
		$V_{PP} = V_{PPL}$			±1.0	
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 5.8$ mA $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.5$ mA $V_{CC} = V_{CC}$ Min	2.4			V
V_{ID}	A9 Auto Select Voltage	$A9 = V_{ID}$	11.5		13.0	V
I_{ID}	A9 Auto Select Current	$A9 = V_{ID}$ Max $V_{CC} = V_{CC}$ Max		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:*** *Erase/Program are inhibited when $V_{PP} = V_{PPL}$*	0.0		V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. ***Caution:*** *the Am28F020 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
2. *I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.*
3. *Maximum active power usage is the sum of I_{CC} and I_{PP}.*
4. *Not 100% tested.*

DC CHARACTERISTICS—CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS}			± 1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}			± 1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{CC} + 0.5$ V		15	100	µA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ $I_{OUT} = 0$ mA, at 6 MHz		10	30	mA
I_{CC2}	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress (Note 4)		10	30	mA
I_{CC3}	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress (Note 4)		10	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			± 1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	µA
I_{PP2}	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress (Note 4)		10	30	mA
I_{PP3}	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress (Note 4)		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 5.8$ mA $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.5$ mA, $V_{CC} = V_{CC}$ Min	0.85 V_{CC}			V
V_{OH2}		$I_{OH} = -100$ µA, $V_{CC} = V_{CC}$ Min	V_{CC} –0.4			
V_{ID}	A9 Auto Select Voltage	A9 = V_{ID}	11.5		13.0	V
I_{ID}	A9 Auto Select Current	A9 = V_{ID} Max $V_{CC} = V_{CC}$ Max		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:** Erase/ Program are inhibited when $V_{PP} = V_{PPL}$*	0.0		V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. ***Caution:** the Am28F020 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
2. *I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.*
3. *Maximum active power usage is the sum of I_{CC} and I_{PP}.*
4. *Not 100% tested.*

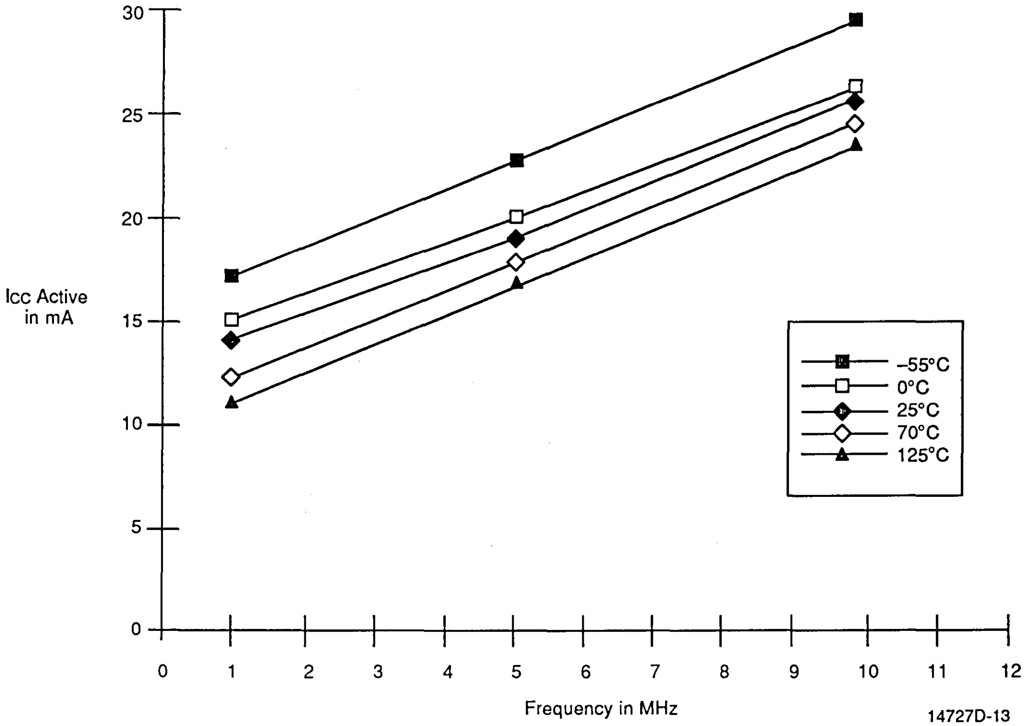


Figure 5. Am28F020–Average Icc Active vs. Frequency
Vcc = 5.5 V, Addressing Pattern = Minmax
Data Pattern = Checkerboard

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	8	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A = 25°C$, $f = 1.0$ MHz*

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

AC CHARACTERISTICS—Read Only Operation (Notes 1–4)

Parameter Symbols		Parameter Description		Am28F020					Unit
JEDEC	Standard			-90 -95	-120 —	-150 —	-200 —	-250 —	
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)	Min	90	120	150	200	250	ns
			Max						
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min						
			Max	90	120	150	200	250	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min						
			Max	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min						
			Max	35	50	55	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z (Note 4)	Min	0	0	0	0	0	ns
			Max						
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z (Note 3)	Min						
			Max	20	30	35	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z (Note 4)	Min	0	0	0	0	0	ns
			Max						
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z (Note 4)	Min						
			Max	20	30	35	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change (Note 4)	Min	0	0	0	0	0	ns
			Max						
t_{WHGL}		Write Recovery Time before Read	Min	6	6	6	6	6	µs
			Max						
t_{VCS}		V_{CC} Set-up Time to Valid Read (Note 4)	Min	50	50	50	50	50	µs
			Max						

Notes:

1. *Output Load: 1 TTL gate and $C_L = 100$ pF*
   Input Rise and Fall Times: < 10 ns
   Input Pulse levels: 0.45 to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. *The Am28F020-95 Output Load: 1 TTL gate and $C_L = 100$ pF*
   Input Rise and Fall Times: < 10 ns
   Input Pulse levels: 0 to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. *Guaranteed by design not tested.*
4. *Not 100% tested.*

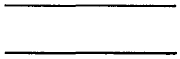
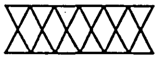
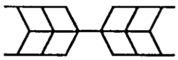
AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1–6)

Parameter Symbols				Am28F020					
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 6)	Min Max	90	120	150	200	250	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min Max	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min Max	45	50	60	75	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min Max	45	50	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min Max	10	10	10	10	10	ns
t_{WHGL}	t_{WR}	Write Recovery Time before Read	Min Max	6	6	6	6	6	µs
t_{GHWL}		Read Recovery Time before Write	Min Max	0	0	0	0	0	µs
t_{ELWL}	t_{CS}	Chip Enable Set-Up Time	Min Max	0	0	0	0	0	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min Max	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min Max	45	50	60	60	60	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min Max	20	20	20	20	20	ns
t_{WHWH1}		Duration of Programming Operation (Note 4)	Min Max	10	10	10	10	10	µs
t_{WHWH2}		Duration of Erase Operation(Note 4)	Min Max	9.5	9.5	9.5	9.5	9.5	ms
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 6)	Min Max	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 10% V_{PPL} (Note 6)	Min Max	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 6)	Min Max	100	100	100	100	100	ns

Notes:

1. *Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.*
2. *All devices except Am28F020-95. Input Rise and Fall times: < 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V*
3. *Am28F020-95. Input Rise and Fall times: < 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V*
4. *Maximum pulse widths not required because the on-chip program/erase stop timer will terminate the pulse widths internally on the device.*
5. *Chip-Enable Controlled Writes: Write operations are driven by the valid combination of Chip-Enable and Write-Enable. In systems where Chip-Enable defines the Write Pulse Width (within a longer Write-Enable timing waveform) all set-up, hold and inactive Write-Enable times should be measured relative to the Chip-Enable waveform.*
6. *Not 100% tested.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS

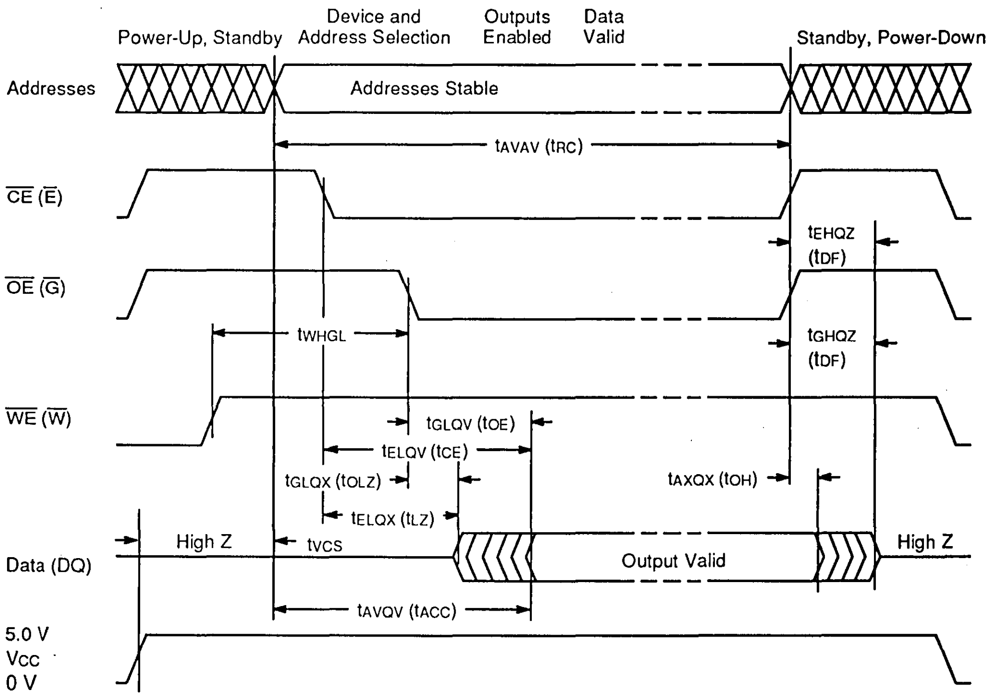


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Figure 6. AC Waveforms for Read Operations

SWITCHING WAVEFORMS

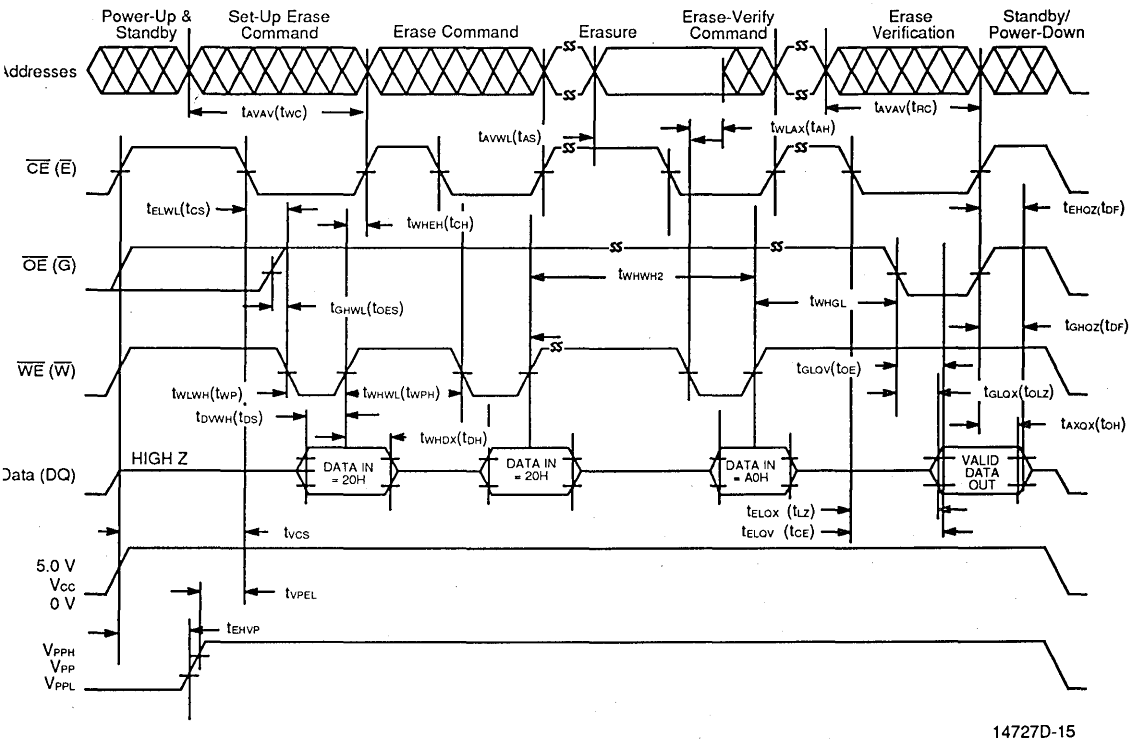


Figure 7. AC Waveforms for Erase Operations

SWITCHING WAVEFORMS

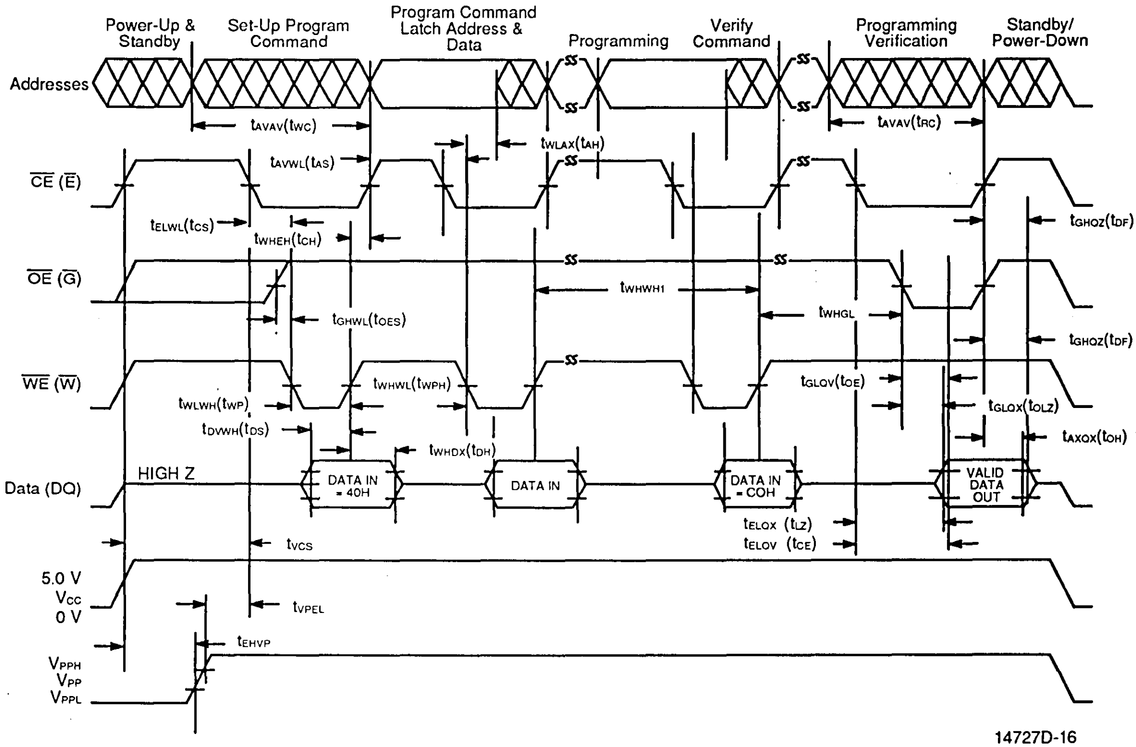
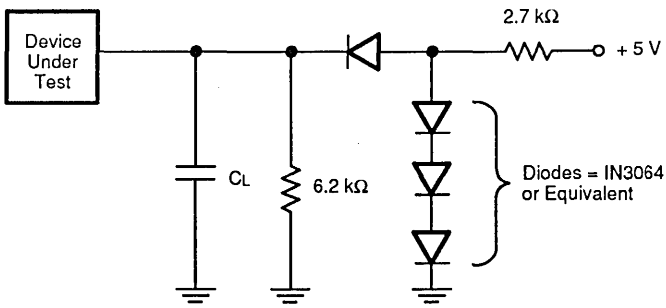


Figure 8. AC Waveforms for Programming Operations

SWITCHING TEST CIRCUIT



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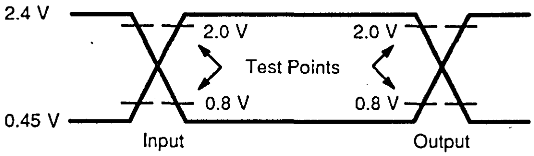
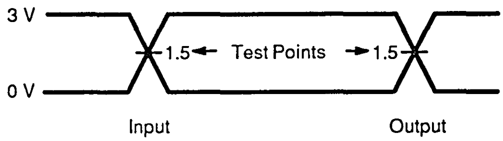
C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORMS



All Devices Except Am28F020-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are < 10 ns.



For Am28F020-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are < 10 ns.

14727D-18

ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max (Note 3)		
Chip Erase Time		1 (Note 1)	10 (Note 2)	s	Excludes 00H programming prior to erasure
Chip Programming Time		4 (Note 1)	25	s	Excludes system-level overhead
Write/Erase Cycles	10,000			Cycles	

Notes:

1. *25°C, 12 V V_{PP}*
2. *The Flasherase/Flashrite algorithms allows for 60 second erase time for military temperature range operations.*
3. *Maximum time specified is lower than worst case. Worst case is derived from the Flasherase/Flashrite pulse count (Flasherase = 1000 max and Flashrite = 25 max). Typical worst case for program and erase operations is significantly less than the actual device limit.*

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to V_{SS} on all pins except I/O pins (Including A9 and V_{PP})	–1.0 V	13.5 V
Input Voltage with respect to V_{SS} on all pins I/O pins	–1.0 V	V_{CC} + 1.0 V
Current	–100 mA	+100 mA
Includes all pins except V_{CC}. Test conditions: V_{CC} = 5.0 V, one pin at a time.		

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

DATA SHEET REVISION SUMMARY FOR Am28F020

Data sheet is Final now, and not Preliminary.

Erase, Program and Read Mode – Write Operations

Removed Command Register Table and Bit assignments.

Erase, Program and Read Mode – Read Command

The statement requiring a 6 µs wait before accessing the first addressed location was removed.

Table 3 – Am28F020 Command Definitions

The note describing a 6 µs wait before accessing the first addressed location was removed.

Flasherase Erase Sequence – Erase Verify Command

The address latched also depends on the falling edge of $\overline{CE}$, whichever happens later.

Flasherase Erase Sequence – Verify Next Address

The new address latched also depends on the falling edge of $\overline{CE}$. whichever happens later.

Auto Select Command

Programming In-System

Titles for each section were switched.

Programming In-System

It is necessary to write a valid command, such as Reset, into the register.

DC Characteristics – TTL/NMOS Compatible

Added Note 4. Those characteristics are not 100% tested.

DC Characteristics – CMOS Compatible

Added Note 4. Those characteristics are not 100% tested.

FINAL

Am28F020A

Advanced Micro Devices

2 Megabit (262,144 x 8-Bit) CMOS 12.0 Volt, Bulk Erase Flash Memory with Embedded Algorithms

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 90 ns maximum access time
- **CMOS Low power consumption**
  - 30 mA maximum active current
  - 100 µA maximum standby current
  - No data retention power consumption
- **Compatible with JEDEC-standard byte-wide 32-Pin EPROM pinouts**
  - 32-pin DIP
  - 32-pin PLCC
  - 32-pin TSOP
- **100,000 write/erase cycles minimum**
- **Write and erase voltage 12.0 V ±5%**
- **Latch-up protected to 100 mA from –1 V to V_{CC} +1 V**
- **Embedded Erase Electrical Bulk Chip-Erase**
  - Five seconds typical chip erase including preprogramming
- **Embedded Program**
  - 14 µs typical byte-program
  - Four seconds typical chip program
- **Command register architecture for microprocessor/microcontroller compatible write interface**
- **On-chip address and data latches**
- **Advanced CMOS flash memory technology**
  - Low cost single transistor memory cell
- **Embedded algorithms for completely self-timed write/erase operations**
- **Automatic write/erase pulse stop timer**

GENERAL DESCRIPTION

The Am28F020A is a 2 Megabit Flash memory organized as 256K bytes of 8 bits each. AMD's Flash memories offer the most cost-effective and reliable read/write non- volatile random access memory. The Am28F020A is packaged in 32-pin PDIP, PLCC, and TSOP versions. The device is also offered in ceramic DIP package. It is designed to be reprogrammed and erased in-system or in standard EPROM programmers. The Am28F020A is erased when shipped from the factory.

The standard Am28F020A offers access times as fast as 90 ns, allowing operation of high-speed microprocessors without wait states. To eliminate bus contention, the Am28F020A has separate chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) controls.

AMD's Flash memories augment EPROM functionality with in-circuit electrical erasure and programming. The Am28F020A uses a command register to manage this functionality, while maintaining a standard JEDEC Flash standard 32-pin pinout. The command register allows for 100% TTL level control inputs and fixed power supply levels during erase and programming, while maintaining maximum EPROM compatibility.

AMD's Flash technology reliably stores memory contents even after 100,000 erase and program cycles. The AMD cell is designed to optimize the erase and programming mechanisms. In addition, the combination of advanced tunnel oxide processing and low internal electric fields for erase and programming operations produces reliable cycling. The Am28F020A uses a 12.0 V ± 5% V_{PP} supply to perform the erase and programming functions.

The highest degree of latch-up protection is achieved with AMD's proprietary non-epi process. Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1 V to V_{CC} +1 V.

Embedded Program

The Am28F020A is byte programmable using the Embedded Programming algorithm. The Embedded Programming algorithm does not require the system to time-out or verify the data programmed. The typical room temperature programming time of the Am28F020A is four seconds.

Publication# 17502 Rev. B Amendment /0
Issue Date: March 1994

GENERAL DESCRIPTION

Embedded Erase

The entire chip is bulk erased using the Embedded Erase algorithm. The Embedded Erase algorithm automatically programs the entire array prior to electrical erase. The timing and verification of electrical erase are controlled internal to the device. Typical erasure at room temperature is accomplished in one second.

AMD's Am28F020A is entirely pin and software compatible with AMD Am28F010A Flash memory.

Embedded Programming Algorithm vs. Flashrite Programming Algorithm

The Flashrite Programming algorithm requires the user to write a program set-up command, a program command (program data and address), and a program verify command followed by a read and compare operation. The user is required to time the programming pulse width in order to issue the program verify command. An integrated stop timer prevents any possibility of overprogramming. Upon completion of this sequence the data is read back from the device and compared by the user with the data intended to be written; if there is not a match, the sequence is repeated until there is a match or the sequence has been repeated 25 times.

AMD's Embedded Programming algorithm requires the user to only write a program set-up command and a program command (program data and address). The device automatically times the programming pulse width, provides the program verify and counts the number of sequences. A status bit, $\overline{\text{Data}}$ Polling, provides feedback to the user as to the status of the programming operation.

Embedded Erase Algorithm vs. Flasherase Erase Algorithm

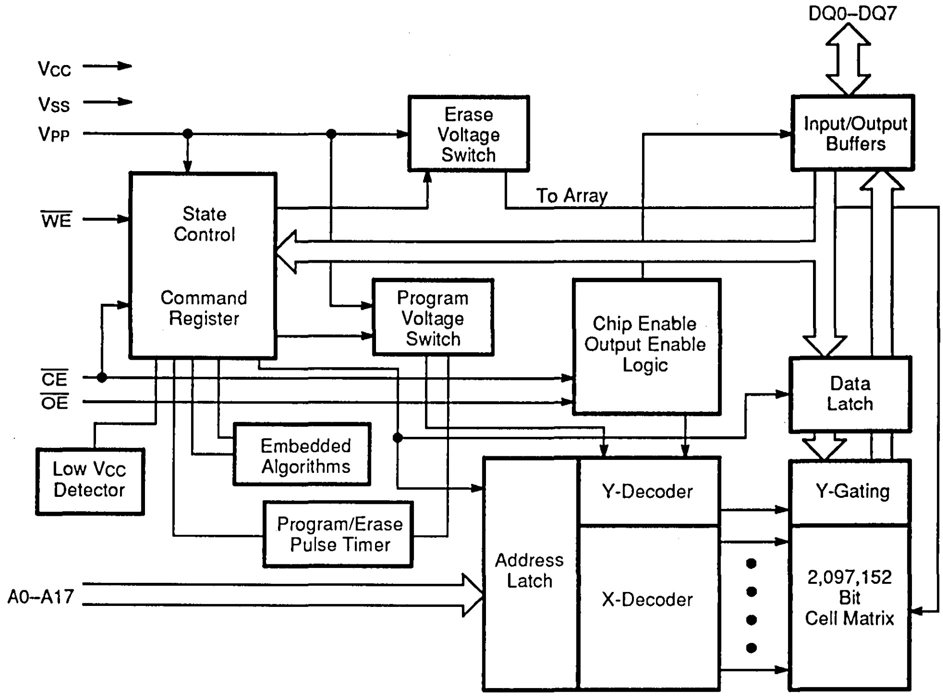
The Flasherase Erase algorithm requires the device to be completely programmed prior to executing an erase command. To invoke the erase operation the user writes an erase set-up command, an erase command, and an erase verify command. The user is required to time the erase pulse width in order to issue the erase verify command. An integrated stop timer prevents any possibility of overerasure. Upon completion of this sequence the data is read back from the device and compared by the user with erased data. If there is not a match, the sequence is repeated until there is a match or the sequence has been repeated 1,000 times.

AMD's Embedded Erase algorithm requires the user to only write an erase set-up command and erase command. The device will automatically pre-program and verify the entire array. Then the device automatically times the erase pulse width, provides the erase verify and counts the number of sequences. A status bit, $\overline{\text{Data}}$ Polling, provides feedback to the user as to the status of the erase operation.

Commands are written to the command register using standard microprocessor write timings. Register contents serve as inputs to an internal state-machine which controls the erase and programming circuitry. During write cycles, the command register internally latches address and data needed for the programming and erase operations. For system design simplification, the Am28F020A is designed to support either $\overline{\text{WE}}$ or $\overline{\text{CE}}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$ whichever occurs last. Data is latched on the rising edge of $\overline{\text{WE}}$ or $\overline{\text{CE}}$ whichever occurs first. To simplify the following discussion, the $\overline{\text{WE}}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{\text{WE}}$ signal.

AMD's Flash technology combines years of EPROM and EEPROM experience to produce the highest levels of quality, reliability, and cost effectiveness. The Am28F020A electrically erases all bits simultaneously using Fowler-Nordheim tunneling. The bytes are programmed one byte at a time using the EPROM programming mechanism of hot electron injection.

BLOCK DIAGRAM



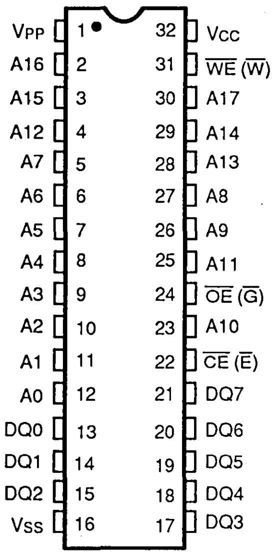
17502B-1

PRODUCT SELECTOR GUIDE

Family Part No.	**Am28F020A**				
Ordering Part No:					
±10% Vcc Tolerance	**-90**	**-120**	**-150**	**-200**	**-250**
±5% Vcc Tolerance	**-95**				
Max Access Time (ns)	90	120	150	200	250
$\overline{CE}$ ($\overline{E}$) Access (ns)	90	120	150	200	250
$\overline{OE}$ ($\overline{G}$) Access (ns)	35	50	55	55	55

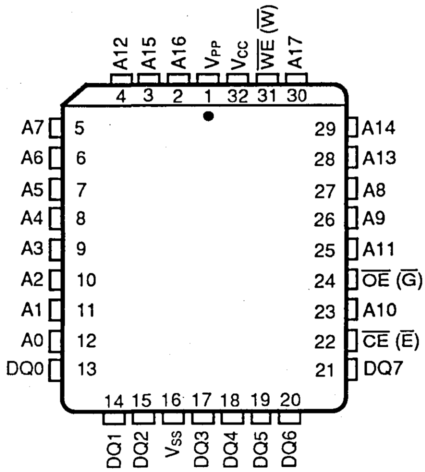
CONNECTION DIAGRAMS

DIP



17502B-2

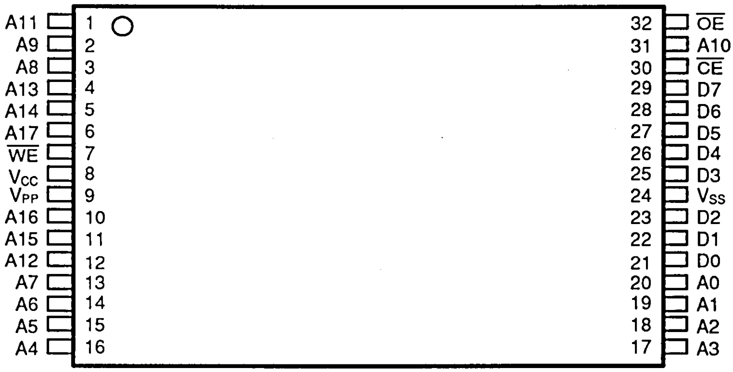
PLCC



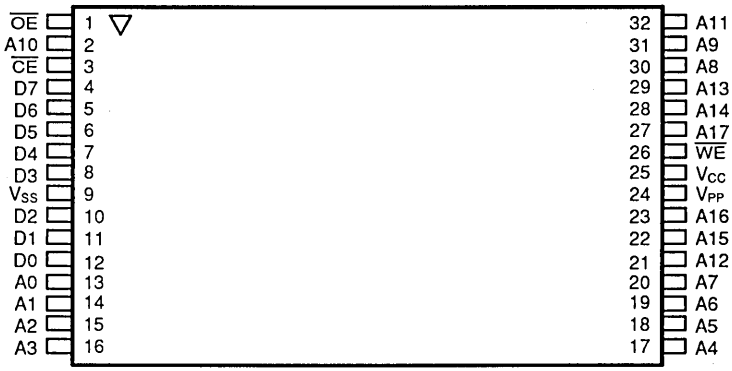
17502B-3

Note: *Pin 1 is marked for orientation.*

CONNECTION DIAGRAMS



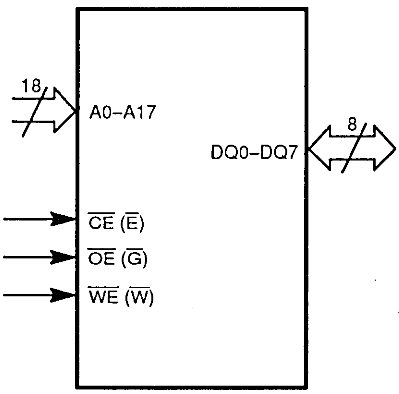
28F020A Standard Pinout



28F020A Reverse Pinout 17502B-4

28F020A 256K x 8 Flash Memory in 32-Lead TSOP

LOGIC SYMBOL



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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

AM28F020A -95 J C B

OPTIONAL PROCESSING
Blank = Standard Processing
B = Burn-In

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to + 85°C)
E = Extended (–55°C to + 125°C)

PACKAGE TYPE
P = 32-Pin Plastic DIP (PD 032)
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)
E = 32-Pin TSOP Standard Pinout (TS 032)
F = 32-Pin TSOP Reverse Pinout (TSR 032)
D = 32-Pin Ceramic DIP (CD 032)

SPEED
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am28F020A
2 Megabit (256K x 8-Bit) CMOS Flash Memory with Embedded Algorithms

Valid Combinations	
AM28F020A-90 AM28F020A-95	PC, JC, EC, FC, DC
AM28F020A-120 AM28F020A-150 AM28F020A-200	PC, PI, JC, JI, PE, PEB, JE, JEB, EC, FC, EI, FI, EE, FE, EEB, FEB, DC, DI, DE, DEB

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) is formed by a combination of:

AM28F020A -120 /B X A

A — LEAD FINISH
A = Hot Solder Dip

X — PACKAGE TYPE
X = 32-Pin Ceramic DIP (CD 032)

/B — DEVICE CLASS
/B = Class B

-120 — SPEED OPTION
See Product Selector Guide and Valid Combinations

AM28F020A — DEVICE NUMBER/DESCRIPTION
Am28F020A
2 Megabit (256K x 8-Bit) CMOS Flash Memory with Embedded Algorithms

Valid Combinations	
AM28F020A-120	/BXA
AM28F020A-150	
AM28F020A-200	
AM28F020A-250	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

A0–A17

Address Inputs for memory locations. Internal latches hold addresses during write cycles.

$\overline{CE}$ ($\overline{E}$)

The Chip Enable active low input activates the chip's control logic and input buffers. Chip Enable high will deselect the device and operates the chip in stand-by mode.

DQ0–DQ7

Data Inputs during memory write cycles. Internal latches hold data during write cycles. Data Outputs during memory read cycles.

NC

No Connect-corresponding pin is not connected internally to the die.

$\overline{OE}$ ($\overline{G}$)

The Output Enable active low input gates the outputs of the device through the data buffers during memory read cycles.

V_{PP}

Power supply for erase and programming. V_{PP} must be at high voltage in order to write to the command register. The command register controls all functions required to alter the memory array contents. Memory contents cannot be altered when $V_{PP} \leq V_{CC} + 2$ V.

V_{CC}

Power supply for device operation. (5.0 V ± 5% or 10%)

V_{SS}

Ground

$\overline{WE}$ ($\overline{W}$)

The Write Enable active low input controls the write function of the command register to the memory array. The target address is latched on the falling edge of the Write Enable pulse and the appropriate data is latched on the rising edge of the pulse.

BASIC PRINCIPLES

The Am28F020A uses 100% TTL-level control inputs to manage the command register. Erase and reprogramming operations use a fixed 12.0V ± 5% power supply.

Read Only Memory

Without high V_{PP} voltage, the Am28F020A functions as a read only memory and operates like a standard EPROM. The control inputs still manage traditional read, standby, output disable, and Auto select modes.

Command Register

The command register is enabled only when high voltage is applied to the V_{PP} pin. The erase and reprogramming operations are only accessed via the register. In addition, two-cycle commands are required for erase and reprogramming operations. The traditional read, standby, output disable, and Auto select modes are available via the register.

The Am28F020A's command register is written using standard microprocessor write timings. The register controls an internal state machine that manages all device operations. For system design simplification, the Am28F020A is designed to support either $\overline{WE}$ or $\overline{CE}$ controlled writes. During a system write cycle, addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$ whichever occurs last. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$ whichever occur first. To simplify the following discussion, the $\overline{WE}$ pin is used as the write cycle control pin throughout the rest of this text. All setup and hold times are with respect to the $\overline{WE}$ signal.

Overview of Erase/Program Operations

Embedded Erase Algorithm

AMD now makes erasure extremely simple and reliable. The Embedded Erase algorithm requires the user to only write and erase set-up command and erase command. The device will automatically pre-program and verify the entire array. The device automatically times the erase pulse width, provides the erase verify and counts the number of sequences. A status bit, $\overline{\text{Data}}$ Polling, provides feedback to the user as to the status of the erase operation.

Embedded Programming Algorithm

AMD now makes programming extremely simple and reliable. The Embedded Programming algorithm requires the user to only write a program set-up command and a program command. The device automatically times the programming pulse width, provides the program verify and counts the number of sequences. A status bit, $\overline{\text{Data}}$ Polling, provides feedback to the user as to the status of the programming operation.

Data Protection

The Am28F020A is designed to offer protection against accidental erasure or programming, caused by spurious system level signals that may exist during power transitions. The Am28F020A powers up in its read only state. Also, with its control register architecture, alteration of the memory contents only occurs after successful completion of specific command sequences.

The device also incorporates several features to prevent inadvertent write cycles resulting form V_{CC} power-up and power-down transitions or system noise.

Low V_{CC} Write Inhibit

To avoid initiation of a write cycle during V_{CC} power-up and power-down, a write cycle is locked out for V_{CC} less than 3.2 V (typically 3.7 V). If $V_{CC} < V_{LKO}$, the command register is disabled and all internal program/erase circuits are disabled. The device will reset to the read mode. Subsequent writes will be ignored until the V_{CC} level is greater than V_{LKO}. It is the users responsibility to ensure that the control pins are logically correct to prevent unintentional writes when V_{CC} is above 3.2 V.

Write Pulse "Glitch" Protection

Noise pulses of less than 10 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ will not initiate a write cycle.

Logical Inhibit

Writing is inhibited by holding any one of $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IH}$. To initiate a write cycle $\overline{CE}$ and $\overline{WE}$ must be a logical zero while $\overline{OE}$ is a logical one.

Power-Up Write Inhibit

Power-up of the device with $\overline{WE} = \overline{CE} = V_{IL}$ and $\overline{OE} = V_{IH}$ will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode on power-up.

FUNCTIONAL DESCRIPTION

Description of User Modes

Table 1. Am28F020A User Bus Operations

Operation		$\overline{CE}$ ($\overline{E}$)	$\overline{OE}$ ($\overline{G}$)	$\overline{WE}$ ($\overline{W}$)	V_{PP} (Note 1)	A0	A9	I/O
Read-Only	Read	V_{IL}	V_{IL}	X	V_{PPL}	A0	A9	D_{OUT}
	Standby	V_{IH}	X	X	V_{PPL}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPL}	X	X	HIGH Z
	Auto-select Manufacturer Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IL}	V_{ID} (Note 3)	CODE (01H)
	Auto-select Device Code (Note 2)	V_{IL}	V_{IL}	V_{IH}	V_{PPL}	V_{IH}	V_{ID} (Note 3)	CODE (29H)
Read/Write	Read	V_{IL}	V_{IL}	V_{IH}	V_{PPH}	A0	A9	D_{OUT} (Note 4)
	Standby (Note 5)	V_{IH}	X	X	V_{PPH}	X	X	HIGH Z
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{PPH}	X	X	HIGH Z
	Write	V_{IL}	V_{IH}	V_{IL}	V_{PPH}	A0	A9	D_{IN} (Note 6)

Legend:

X = Don't care, where Don't Care is either V_{IL} or V_{IH} levels, $V_{PPL} = V_{PP} \leq V_{CC} + 2$ V, See DC Characteristics for voltage levels of V_{PPH}, 0 V < An < V_{CC} + 2 V, (normal TTL or CMOS input levels, where n = 0 or 9).

Notes:

1. *V_{PPL} may be grounded, connected with a resistor to ground, or < V_{CC} +2.0 V. V_{PPH} is the programming voltage specified for the device. Refer to the DC characteristics. When $V_{PP} = V_{PPL}$, memory contents can be read but not written or erased.*
2. *Manufacturer and device codes may also be accessed via a command register write sequence. Refer to Table 2.*
3. *$11.5 \leq V_{ID} \leq 13.0$ V*
4. *Read operation with $V_{PP} = V_{PPH}$ may access array data or the Auto select codes.*
5. *With V_{PP} at high voltage, the standby current is I_{CC} + I_{PP} (standby).*
6. *Refer to Table 3 for valid D_{IN} during a write operation.*
7. *All inputs are Don't Care unless otherwise stated, where Don't Care is either V_{IL} or V_{IH} levels. In the Auto select mode all addresses except A9 and A0 must be held at V_{IL}.*

READ ONLY MODE

$V_{PP} < V_{CC} + 2$ V
Command Register Inactive

Read

The Am28F020A functions as a read only memory when $V_{PP} < V_{CC} + 2$ V. The Am28F020A has two control functions. Both must be satisfied in order to output data. $\overline{CE}$ controls power to the device. This pin should be used for specific device selection. $\overline{OE}$ controls the device outputs and should be used to gate data to the output pins if a device is selected.

Address access time t_{ACC} is equal to the delay from stable addresses to valid output data. The chip enable access time t_{CE} is the delay from stable addresses and stable $\overline{CE}$ to valid data at the output pins. The output enable access time is the delay from the falling edge of $\overline{OE}$ to valid data at the output pins (assuming the addresses have been stable at least $t_{ACC} - t_{OE}$).

Standby Mode

The Am28F020A has two standby modes. The CMOS standby mode ($\overline{CE}$ input held at $V_{CC} \pm 0.5$ V), consumes less than 100 µA of current. TTL standby mode ($\overline{CE}$ is held at V_{IH}) reduces the current requirements to less than 1 mA. When in the standby mode the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

If the device is deselected during erasure, programming, or program/erase verification, the device will draw active current until the operation is terminated.

Output Disable

Output from the device is disabled when $\overline{OE}$ is at a logic high level. When disabled, output pins are in a high impedance state.

Auto Select

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the board.

The Auto select mode allows the reading out of a binary code from the device that will identify its manufacturer and type. This mode is intended for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional over the entire temperature range of the device.

Programming In A PROM Programmer

To activate this mode, the programming equipment must force V_{ID} (11.5 V to 13.0 V) on address A9. Two identifier bytes may then be sequenced from the device outputs by toggling address A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL}, and V_{PP} must be less than or equal to $V_{CC} + 2.0$ V while using this Auto select mode. Byte 0 (A0 = V_{IL}) represents the manufacturer code and byte 1 (A0 = V_{IH}) the device identifier code. For the Am28F020A these two bytes are given in the table below. All identifiers for manufacturer and device codes will exhibit odd parity with the MSB (DQ7) defined as the parity bit.

(Refer to the AUTO SELECT paragraph in the ERASE, PROGRAM, and READ MODE section for programming the Flash memory device in-system).

Table 2. Am28F020A Auto Select Code

Type	A0	Code (HEX)	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Manufacturer Code	V_{IL}	01	0	0	0	0	0	0	0	1
Device Code	V_{IH}	29	0	0	1	0	1	0	0	1

ERASE, PROGRAM, AND READ MODE

V_{PP} = 12.0 V ± 5%

Command Register Active

Write Operations

High voltage must be applied to the V_{PP} pin in order to activate the command register. Data written to the register serves as input to the internal state machine. The output of the state machine determines the operational function of the device.

The command register does not occupy an addressable memory location. The register is a latch that stores the command, along with the address and data information needed to execute the command. The register is written by bringing $\overline{WE}$ and $\overline{CE}$ to V_{IL}, while $\overline{OE}$ is at V_{IH}. Addresses are latched on the falling edge of $\overline{WE}$, while data is latched on the rising edge of the $\overline{WE}$ pulse. Standard microprocessor write timings are used.

The device requires the $\overline{OE}$ pin to be V_{IH} for write operations. This condition eliminates the possibility for bus contention during programming operations. In order to write, $\overline{OE}$ must be V_{IH}, and $\overline{CE}$ and $\overline{WE}$ must be V_{IL}. If any pin is not in the correct state a write command will not be executed.

Refer to AC Write Characteristics and the Erase/Programming Waveforms for specific timing parameters.

Command Definitions

The contents of the command register default to 00H (Read Mode) in the absence of high voltage applied to the V_{PP} pin. The device operates as a read only memory. High voltage on the V_{PP} pin enables the command register. Device operations are selected by writing specific data codes into the command register. Table 3 defines these register commands.

Read Command

Memory contents can be accessed via the read command when V_{PP} is high. To read from the device, write 00H into the command register. Standard microprocessor read cycles access data from the memory. The device will remain in the read mode until the command register contents are altered.

The command register defaults to 00H (read mode) upon V_{PP} power-up. The 00H (Read Mode) register default helps ensure that inadvertent alteration of the memory contents does not occur during the V_{PP} power transition. Refer to the AC Read Characteristics and Waveforms for the specific timing parameters.

Table 3. Am28F020A Command Definitions

	First Bus Cycle			Second Bus Cycle		
Command	Operation (Note 1)	Address (Note 2)	Data (Note 3)	Operation (Note 1)	Address (Note 2)	Data (Note 3)
Read Memory (Note 4)	Write	X	00H/FFH	Read	RA	RD
Read Auto select	Write	X	80H or 90H	Read	00H/01H	01H/29H
Embedded Erase Set-up/ Embedded Erase	Write	X	30H	Write	X	30H
Embedded Program Set-up/ Embedded Program	Write	X	10H or 50H	Write	PA	PD
Reset (Note 4)	Write	X	FFH	Write	X	FFH

Notes:

1. *Bus operations are defined in Table 1.*
2. *RA = Address of the memory location to be read.*
   PA = Address of the memory location to be programmed.
   Addresses are latched on the falling edge of the $\overline{WE}$ pulse.
   X = Don't care.
3. *RD = Data read from location RA during read operation.*
   PD = Data to be programmed at location PA. Data latched on the rising edge of $\overline{WE}$.
4. *Please reference Reset Command section.*

FLASH MEMORY PROGRAM/ERASE OPERATIONS

AMD's Embedded Program and Erase Operations

Embedded Erase Algorithm

The automatic chip erase does not require the device to be entirely pre-programmed prior to executing the Embedded set-up erase command and Embedded erase command. Upon executing the Embedded erase command the device automatically will program and verify the entire memory for an all zero data pattern. The system is not required to provide any controls or timing during these operations.

When the device is automatically verified to contain an all zero pattern, a self-timed chip erase and verify begin. The erase and verify operation are complete when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to Read mode. The system is not required to provide any control or timing during these operations.

When using the Embedded Erase algorithm, the erase automatically terminates when adequate erase margin has been achieved for the memory array (no erase verify command is required). The margin voltages are internally generated in the same manner as when the standard erase verify command is used.

The Embedded Erase Set-up command is a command only operation that stages the device for automatic electrical erasure of all bytes in the array. Embedded Erase Set-up is performed by writing 30H to the command register.

To commence automatic chip erase, the command 30H must be written again to the command register. The automatic erase begins on the rising edge of the $\overline{WE}$ and terminates when the data on DQ7 is "1" (see Write Operation Status section) at which time the device returns to Read mode.

Figure 5 and Table 4 illustrate the Embedded Erase algorithm, a typical command string and bus operation.

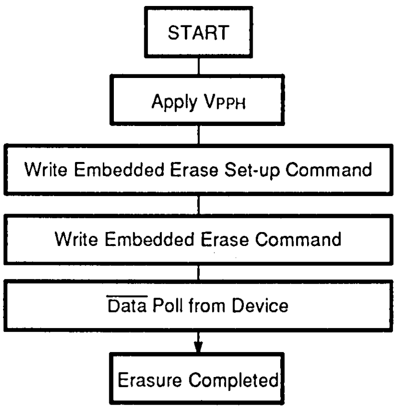


Figure 5. Embedded Erase Algorithm

Table 4. Embedded Erase Algorithm

Bus Operations	Command	Comments
Standby		Wait for VPP Ramp to VPPH (1)
Write	Embedded Erase Set-Up Command	Data = 30H
Write	Embedded Erase Command	Data = 30H
Read		$\overline{\text{Data}}$ Polling to Verify Erasure
Standby		Compare Output to FFH
Read		Available for Read Operations

Note:

1. *See DC Characteristics for value of VPPL. The VPP power supply can be hard-wired to the device or switchable. When VPP is switched, VPPL may be ground, no connect with a resistor tied to ground, or less than Vcc + 2.0 V. Refer to Functional Description.*

Embedded Programming Algorithm

The Embedded Program Set-up is a command only operation that stages the device for automatic programming. Embedded Program Set-up is performed by writing 50H to the command register.

Once the Embedded Set-up Program operation is performed, the next $\overline{WE}$ pulse causes a transition to an active programming operation. Addresses are latched on the falling edge of $\overline{CE}$ or $\overline{WE}$ pulse, whichever happens later. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. The rising edge of $\overline{WE}$ also begins the programming operation. The system is not required to provide further controls or timings. The device will automatically provide an adequate internally generated program pulse and verify margin. The automatic programming operation is completed when the data on DQ7 is equivalent to data written to this bit (see Write Operation Status section) at which time the device returns to Read mode.

Figure 6 and Table 5 illustrate the Embedded Program algorithm, a typical command string, and bus operation.

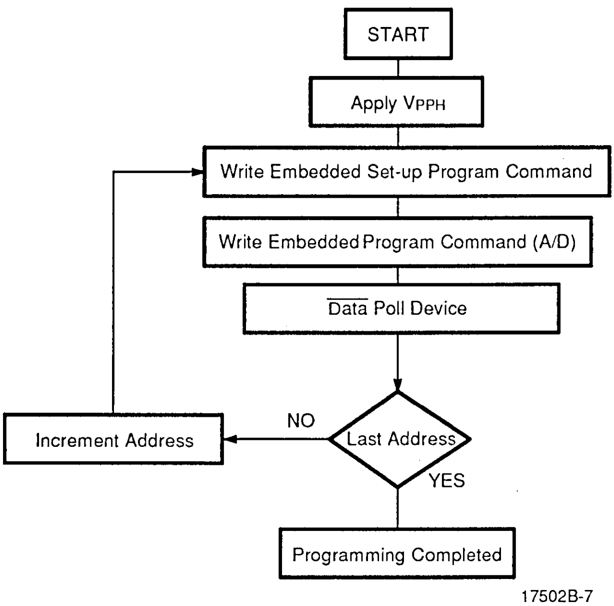


Figure 6. Embedded Programming Algorithm

Table 5. Embedded Programming Algorithm

Bus Operations	Command	Comments
Standby		Wait for V_{PP} Ramp to V_{PPH} (1)
Write	Embedded Program Set-Up Command	Data = 50H
Write	Embedded Program Command	Valid Address/Data
Read		$\overline{\text{Data}}$ Polling to Verify Completion
Read		Available for Read Operations

Note:

1. *See DC Characteristics for value of V_{PPH}. The V_{PP} power supply can be hard-wired to the device or switchable. When V_{PP} is switched, V_{PPL} may be ground, no connect with a resistor tied to ground, or less than V_{CC} + 2.0 V. Refer to Functional Description. Device is either powered-down, erase inhibit or program inhibit.*

Write Operation Status

$\overline{\text{Data}}$ Polling—DQ7

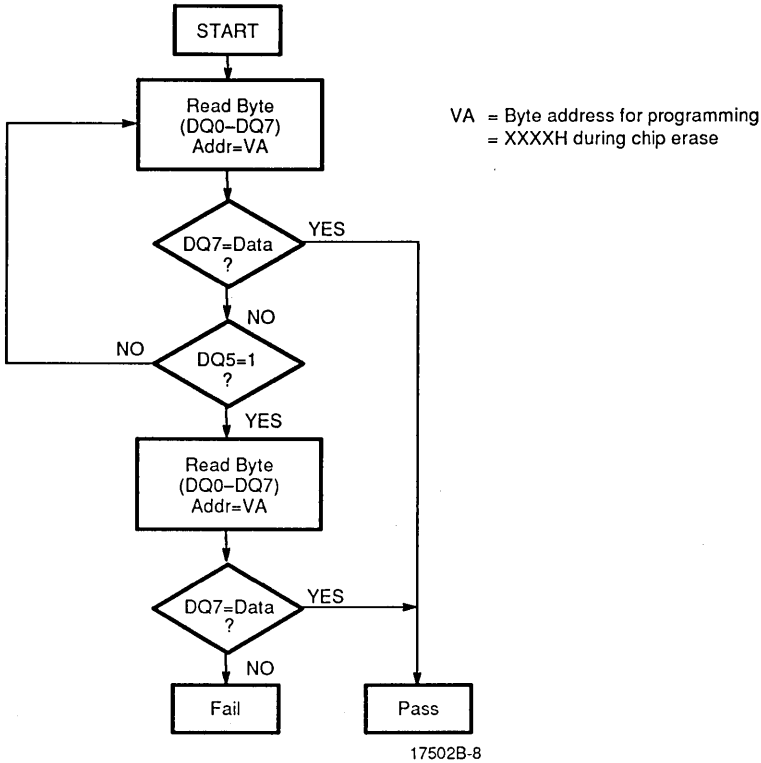
The Am28F020A features $\overline{\text{Data}}$ Polling as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

While the Embedded Programming algorithm is in operation, an attempt to read the device at a valid address will produce the complement of expected Valid data on DQ7. Upon completion of the Embedded Program algorithm an attempt to read the device at a valid address will produce Valid data on DQ7. The $\overline{\text{Data}}$ Polling feature is valid after the rising edge of the second $\overline{\text{WE}}$ pulse of the two write pulse sequence.

While the Embedded Erase algorithm is in operation, DQ7 will read "0" until the erase operation is completed. Upon completion of the erase operation, the data on DQ7 will read "1". The $\overline{\text{Data}}$ Polling feature is valid after the rising edge of the second $\overline{\text{WE}}$ pulse of the two Write pulse sequence.

The $\overline{\text{Data}}$ Polling feature is only active during Embedded Programming or erase algorithms.

See Figure 7a and 8a for the $\overline{\text{Data}}$ Polling timing specifications and diagrams. $\overline{\text{Data}}$ Polling is the standard method to check the write operation status, however, an alternative method is available using Toggle Bit.



Note:

1. *DQ7 is rechecked even if DQ5="1" because DQ7 may change simultaneously with DQ5 or after DQ5.*

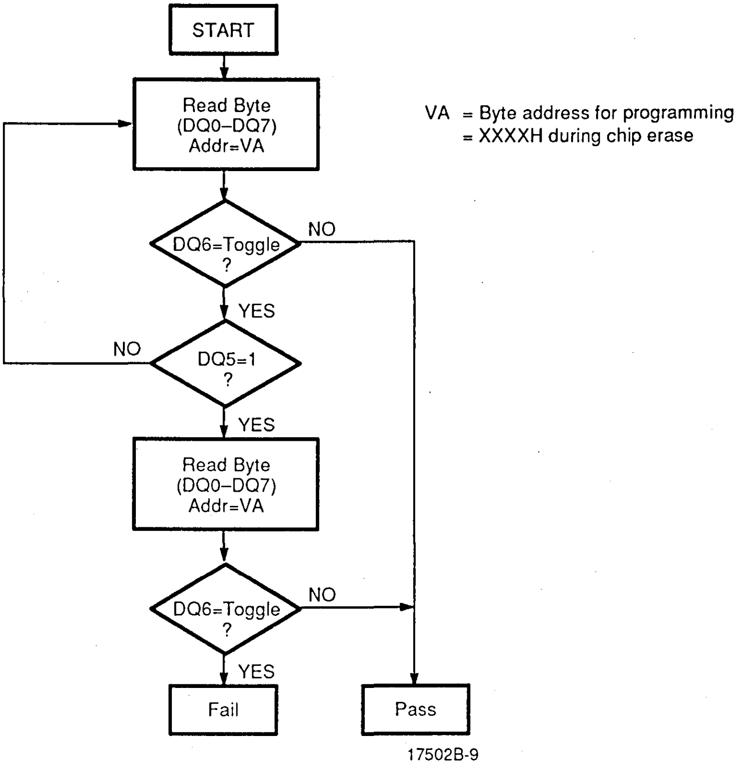
Figure 7a. $\overline{\text{Data}}$ Polling Algorithm

Toggle Bit—DQ6

The Am28F020A also features a "Toggle Bit" as a method to indicate to the host system that the Embedded algorithms are either in progress or completed.

Successive attempts to read data from the device at a valid address, while the Embedded Program algorithm is in progress, or at any address while the Embedded Erase algorithm is in progress, will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase algorithm is completed, DQ6 will stop toggling to indicate the completion of either Embedded operation. Only on the next read cycle will valid data be obtained. The toggle bit is valid after the rising edge of the first $\overline{WE}$ pulse of the two write pulse sequence, unlike $\overline{Data}$ Polling which is valid after the rising edge of the second $\overline{WE}$ pulse. This feature allows the user to determine if the device is partially through the two write pulse sequence.

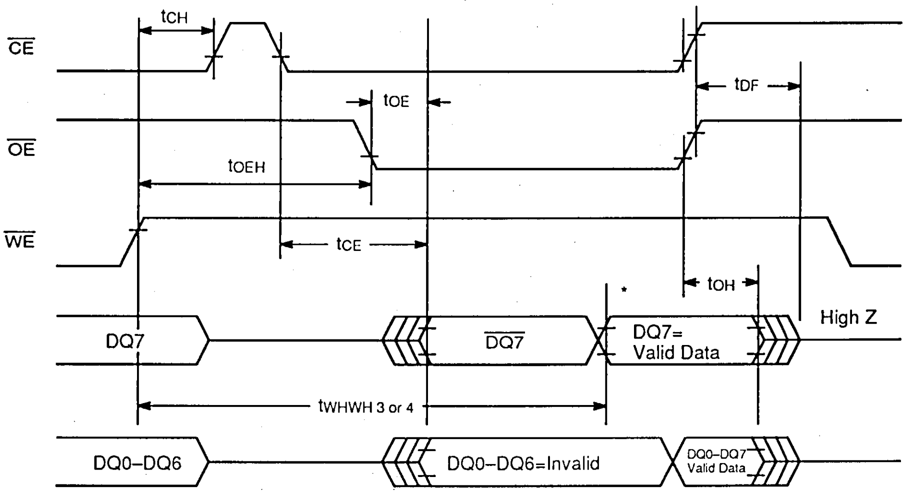
See Figures 7b and 8b for the Toggle Bit timing specifications and diagrams.



Note:

1. DQ6 is rechecked even if DQ5="1" because DQ6 may stop toggling at the same time as DQ5 changing to "1".

Figure 7b. Toggle Bit Algorithm



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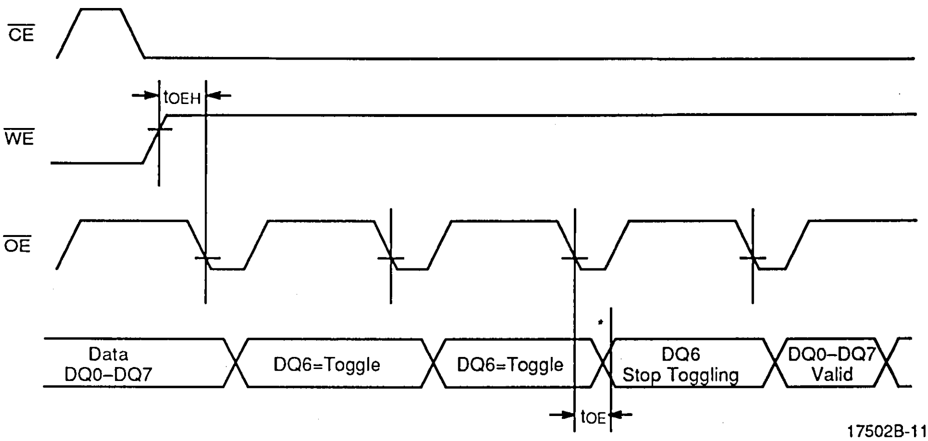
Note:
**DQ7=Valid Data (The device has completed the Embedded operation).*

Figure 8a. AC Waveforms for $\overline{\text{Data}}$ Polling During Embedded Algorithm Operations

DQ5
Exceeded Timing Limits

DQ5 will indicate if the program or erase time has exceeded the specified limits. This is a failure condition and the device may not be used again (internal pulse count exceeded). Under these conditions DQ5 will produce a "1". The program or erase cycle was not successfully completed. $\overline{\text{Data}}$ Polling is the only operating function of the device under this condition. The $\overline{\text{CE}}$ circuit will partially power down the device under these conditions (to approximately 2 mA). The $\overline{\text{OE}}$ and $\overline{\text{WE}}$ pins will control the output disable functions as described in Table 1.



Note:

**DQ6 stops toggling (The device has completed the Embedded operation).*

Figure 8b. AC Waveforms for Toggle Bit During Embedded Algorithm Operations

Parallel Device Erasure

The Embedded Erase algorithm greatly simplifies parallel device erasure. Since the erase process is internal to the device, a single erase command can be given to multiple devices concurrently. By implementing a parallel erase algorithm, total erase time may be minimized.

Note that the Flash memories may erase at different rates. If this is the case, when a device is completely erased, use a masking code to prevent further erasure (over-erasure). The other devices will continue to erase until verified. The masking code applied could be the read command (00H).

Power-Up Sequence

The Am28F020A powers-up in the Read only mode. Power supply sequencing is not required.

Reset Command

The Reset command initializes the Flash memory device to the Read mode. In addition, it also provides the user with a safe method to abort any device operation (including program or erase).

The Reset must be written two consecutive times after the Set-up Program command (50H). This will reset the device to the Read mode.

Following any other Flash command, write the Reset command once to the device. This will safely abort any previous operation and initialize the device to the Read mode.

The Set-up Program command (50H) is the only command that requires a two-sequence reset cycle. The first Reset command is interpreted as program data. However, FFH data is considered as null data during programming operations (memory cells are only programmed from a logical "1" to "0"). The second Reset command safely aborts the programming operation and resets the device to the Read mode.

Memory contents are not altered in any case.

This detailed information is for your reference. It may prove easier to always issue The Reset command two consecutive times. This eliminates the need to determine if you are in the Set-up Program state or not.

In-System Programming Considerations

Flash memories can be programmed in-system or in a standard PROM programmer. The device may be soldered to the circuit board upon receipt of shipment and programmed in-system. Alternatively, the device may initially be programmed in a PROM programmer prior to soldering the device to the circuit board.

Auto Select Command

AMD's Flash memories are designed for use in applications where the local CPU alters memory contents. In order to correctly program any Flash memories in-system, manufacturer and device codes must be accessible while the device resides in the target system. PROM programmers typically access the signature codes by raising A9 to a high voltage. However, multiplexing high voltage onto address lines is not a generally desired system design practice.

The Am28F020A contains an Auto Select operation to supplement traditional PROM programming methodologies. The operation is initiated by writing 80H or 90H into the command register. Following this command, a read cycle address 0000H retrieves the manufacturer code of 01H (AMD). A read cycle from address 0001H returns the device code 29H (see Table 2). To terminate the operation, it is necessary to write another valid command, such as Reset (FFH), into the register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Ceramic Packages .... –65°C to +150°C
Plastic Packages .... –65°C to +125°C

Ambient Temperature
with Power Applied .... –55°C to + 125°C

Voltage with Respect To Ground
All pins except A9 and V_{PP} (Note 1) –2.0 V to +7.0 V

V_{CC} (Note 1) .... –2.0 V to +7.0 V

A9 (Note 2) .... –2.0 V to +14.0 V

V_{PP} (Note 2) .... –2.0 V to +14.0 V

Output Short Circuit Current (Note 3) ...... 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, inputs may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on output and I/O pins is V_{CC} + 0.5 V. During voltage transitions, outputs may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *Minimum DC input voltage on A9 and V_{PP} pins is –0.5V. During voltage transitions, A9 and V_{PP} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC input voltage on A9 and V_{PP} is +13.5 V which may overshoot to 14.0 V for periods up to 20 ns.*
3. *No more than one output shorted at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Case Temperature (T_C) .... 0°C to +70°C

Industrial (I) Devices
Case Temperature (T_C) .... –40°C to +85°C

Extended (E) Devices
Case Temperature (T_C) .... –55°C to +125°C

Military (M) Devices
Case Temperature (T_C) .... –55°C to +125°C

V_{CC} Supply Voltages
V_{CC} for Am28F020A-X5 .... +4.75 V to +5.25 V

V_{CC} for Am28F020A-XX0 .... +4.50 V to +5.50 V

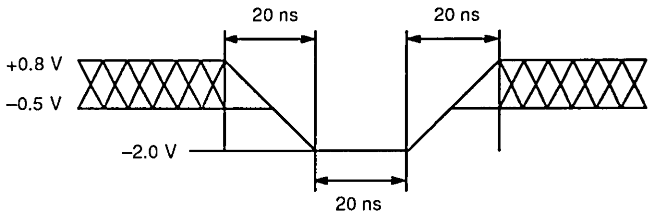
V_{PP} Supply Voltages
Read .... –0.5 V to +12.6 V

Program, Erase, and Verify ..... +11.4 V to +12.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

MAXIMUM OVERSHOOT

Maximum Negative Input Overshoot



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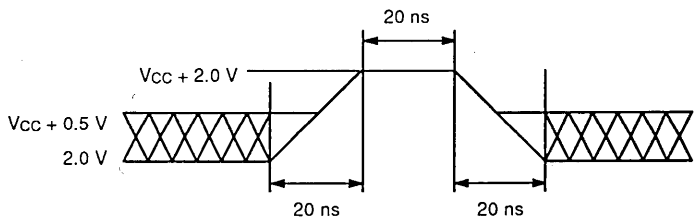
Maximum Positive Input Overshoot



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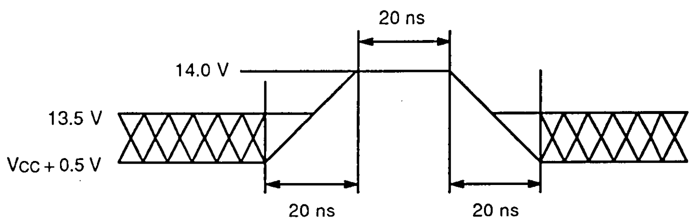
Maximum V_{PP} Overshoot



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DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3, 7, and 8 are tested unless otherwise noted) (Notes 1–4)

DC CHARACTERISTICS-TTL/NMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS}			±1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}			±1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{IH}$		0.2	1.0	mA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ $I_{OUT} = 0$ mA, at 6 MHz		10	30	mA
I_{CC2} (Note 4)	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress		10	30	mA
I_{CC3} (Note 4)	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress		10	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			±1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	µA
		$V_{PP} = V_{PPL}$			±1.0	
I_{PP2} (Note 4)	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress		10	30	mA
I_{PP3} (Note 4)	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 5.8$ mA $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.5$ mA $V_{CC} = V_{CC}$ Min	2.4			V
V_{ID}	A9 Auto Select Voltage	$A9 = V_{ID}$	11.5		13.0	V
I_{ID}	A9 Auto Select Current	$A9 = V_{ID}$ Max $V_{CC} = V_{CC}$ Max		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:*** *Erase/Program are inhibited when* $V_{PP} = V_{PPL}$	0.0		V_{CC} +2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. ***Caution:*** *the Am28F020A must not be removed from (or inserted into) a socket when* V_{CC} *or* V_{PP} *is applied.*
2. I_{CC1} *is tested with* $\overline{OE} = V_{IH}$ *to simulate open outputs.*
3. *Maximum active power usage is the sum of* I_{CC} *and* I_{PP}.
4. *Not 100% tested.*

DC CHARACTERISTICS—CMOS COMPATIBLE

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{IN} = V_{CC}$ or V_{SS}			± 1.0	µA
I_{LO}	Output Leakage Current	$V_{CC} = V_{CC}$ Max, $V_{OUT} = V_{CC}$ or V_{SS}			± 1.0	µA
I_{CCS}	V_{CC} Standby Current	$V_{CC} = V_{CC}$ Max $\overline{CE} = V_{CC} + 0.5$ V		15	100	µA
I_{CC1}	V_{CC} Active Read Current	$V_{CC} = V_{CC}$ Max, $\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$ $I_{OUT} = 0$ mA, at 6 MHz		10	30	mA
I_{CC2} (Note 4)	V_{CC} Programming Current	$\overline{CE} = V_{IL}$ Programming in Progress		10	30	mA
I_{CC3} (Note 4)	V_{CC} Erase Current	$\overline{CE} = V_{IL}$ Erasure in Progress		10	30	mA
I_{PPS}	V_{PP} Standby Current	$V_{PP} = V_{PPL}$			± 1.0	µA
I_{PP1}	V_{PP} Read Current	$V_{PP} = V_{PPH}$		70	200	µA
I_{PP2} (Note 4)	V_{PP} Programming Current	$V_{PP} = V_{PPH}$ Programming in Progress		10	30	mA
I_{PP3} (Note 4)	V_{PP} Erase Current	$V_{PP} = V_{PPH}$ Erasure in Progress		10	30	mA
V_{IL}	Input Low Voltage		–0.5		0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	$I_{OL} = 5.8$ mA $V_{CC} = V_{CC}$ Min			0.45	V
V_{OH1}	Output High Voltage	$I_{OH} = -2.5$ mA, $V_{CC} = V_{CC}$ Min	0.85 V_{CC}			V
V_{OH2}	Output High Voltage	$I_{OH} = -100$ µA, $V_{CC} = V_{CC}$ Min	V_{CC} –0.4			V
V_{ID}	A_9 Auto Select Voltage	$A9 = V_{ID}$	11.5		13.0	V
I_{ID}	A_9 Auto Select Current	$A9 = V_{ID}$ Max $V_{CC} = V_{CC}$ Max		5	50	µA
V_{PPL}	V_{PP} during Read-Only Operations	***Note:** Erase/Program are inhibited when $V_{PP} = V_{PPL}$*	0.0		V_{CC} + 2.0	V
V_{PPH}	V_{PP} during Read/Write Operations		11.4		12.6	V
V_{LKO}	Low V_{CC} Lock-out Voltage		3.2			V

Notes:

1. ***Caution:** the Am28F020A must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
2. *I_{CC1} is tested with $\overline{OE} = V_{IH}$ to simulate open outputs.*
3. *Maximum active power usage is the sum of I_{CC} and I_{PP}.*
4. *Not 100% tested.*

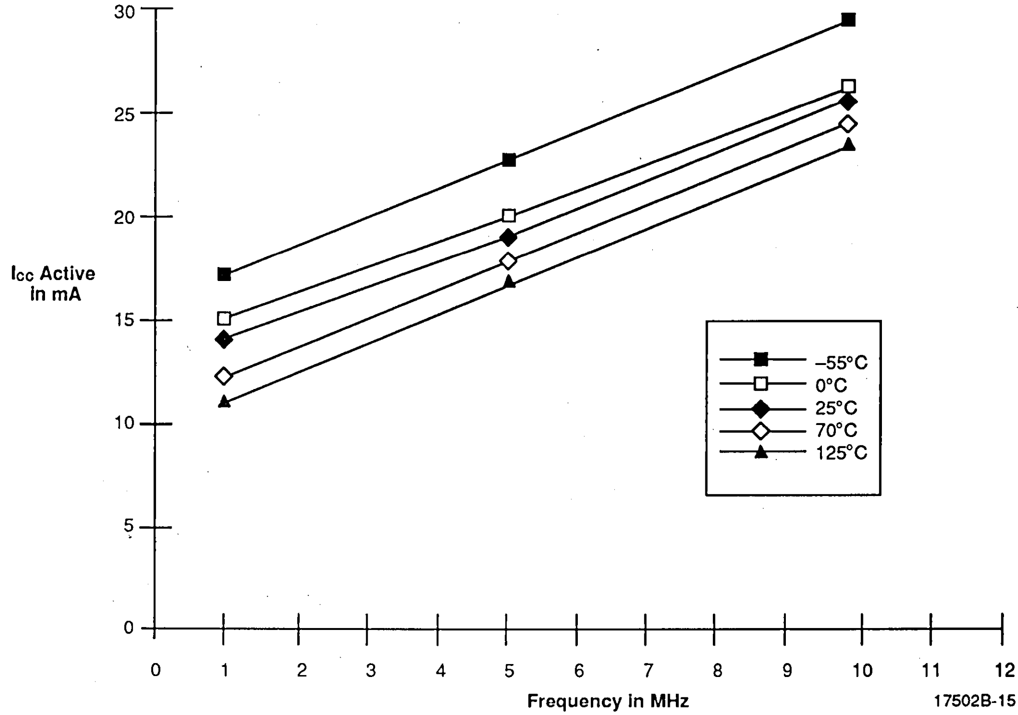


Figure 9. Am28F020A - Average Icc Active vs. Frequency
Vcc = 5.5 V, Addressing Pattern = Minmax
Data Pattern = Checkerboard

PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ	Max	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0$	8	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$	8	12	pF
C_{IN2}	V_{PP} Input Capacitance	$V_{PP} = 0$	8	12	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions $T_A = 25°C$, $f = 1.0$ MHz*

SWITCHING CHARACTERISTICS over operating range unless otherwise specified

AC CHARACTERISTICS—Read Only Operation (Notes 1–4)

Parameter Symbols				Am28F020A					
JEDEC	Standard	Parameter Description		-90 -95	-120 –	-150 –	-200 –	-250 –	Unit
t_{AVAV}	t_{RC}	Read Cycle Time (Note 4)	Min Max	90	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable Access Time	Min Max	90	120	150	200	250	ns
t_{AVQV}	t_{ACC}	Address Access Time	Min Max	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable Access Time	Min Max	35	50	55	55	55	ns
t_{ELQX}	t_{LZ}	Chip Enable to Output in Low Z (Note 4)	Min Max	0	0	0	0	0	ns
t_{EHQZ}	t_{DF}	Chip Disable to Output in High Z (Note 3)	Min Max	20	30	35	35	35	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z (Note 4)	Min Max	0	0	0	0	0	ns
t_{GHQZ}	t_{DF}	Output Disable to Output in High Z (Note 4)	Min Max	20	30	35	35	35	ns
t_{AXQX}	t_{OH}	Output Hold from first of Address, $\overline{CE}$, or $\overline{OE}$ Change (Note 4)	Min Max	0	0	0	0	0	ns
t_{WHGL}		Write Recovery Time before Read	Min Max	6	6	6	6	6	µs
t_{VCS}		V_{CC} Set-up Time to Valid Read (Note 4)	Min Max	50	50	50	50	50	µs

Notes:

1. *Output Load: 1 TTL gate and $C_L = 100$ pF*
   Input Rise and Fall Times: < 10 ns
   Input Pulse levels: 0.45 to 2.4 V
   Timing Measurement Reference Level: Inputs: 0.8 V and 2 V
   Outputs: 0.8 V and 2 V
2. *The Am28F020A-95 Output Load: 1 TTL gate and $C_L = 100$ pF*
   Input Rise and Fall Times: < 10 ns
   Input Pulse levels: 0 to 3 V
   Timing Measurement Reference Level: 1.5 V inputs and outputs.
3. *Guaranteed by design not tested.*
4. *Not 100% tested.*

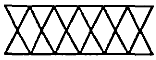
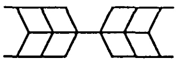
AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1–6)

Parameter Symbols				Am28F020A					
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 6)	Min Max	90	120	150	200	250	ns
t_{AVWL}	t_{AS}	Address Set-Up Time	Min Max	0	0	0	0	0	ns
t_{WLAX}	t_{AH}	Address Hold Time	Min Max	45	50	60	75	75	ns
t_{DVWH}	t_{DS}	Data Set-Up Time	Min Max	45	50	50	50	50	ns
t_{WHDX}	t_{DH}	Data Hold Time	Min Max	10	10	10	10	10	ns
t_{OEH}		Output Enable Hold Time for Embedded Algorithm only (See Figure 8)	Min Max	10	10	10	10	10	ns
t_{GHWL}		Read Recovery Time before Write	Min Max	0	0	0	0	0	µs
t_{ELWLE}	t_{CSE}	Chip Enable Embedded Algorithm Setup Time	Min Max	20	20	20	20	20	ns
t_{WHEH}	t_{CH}	Chip Enable Hold Time	Min Max	0	0	0	0	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width	Min Max	45	50	60	60	60	ns
t_{WHWL}	t_{WPH}	Write Pulse Width HIGH	Min Max	20	20	20	20	20	ns
t_{WHWH3}		Embedded Programming Operation (Note 4)	Min Max	14	14	14	14	14	µs
t_{WHWH4}		Embedded Erase Operation (Note 5)	Typ Max	5	5	5	5	5	S
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable LOW (Note 6)	Min Max	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 6)	Min Max	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time 90% V_{PPL} (Note 6)	Min Max	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 6)	Min Max	100	100	100	100	100	ns

Notes:

1. *Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.*
2. *All devices except Am28F020A-95. Input Rise and Fall times: < 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V*
3. *Am28F020A-95. Input Rise and Fall times: < 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V*
4. *Embedded Program Operation of 14 µs consists of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.*
5. *Embedded erase operation of 5 sec consists of 4 sec array pre-programming time and one sec array erase time. This is a typical time for one embedded erase operation.*
6. *Not 100% tested.*

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010

SWITCHING WAVEFORMS

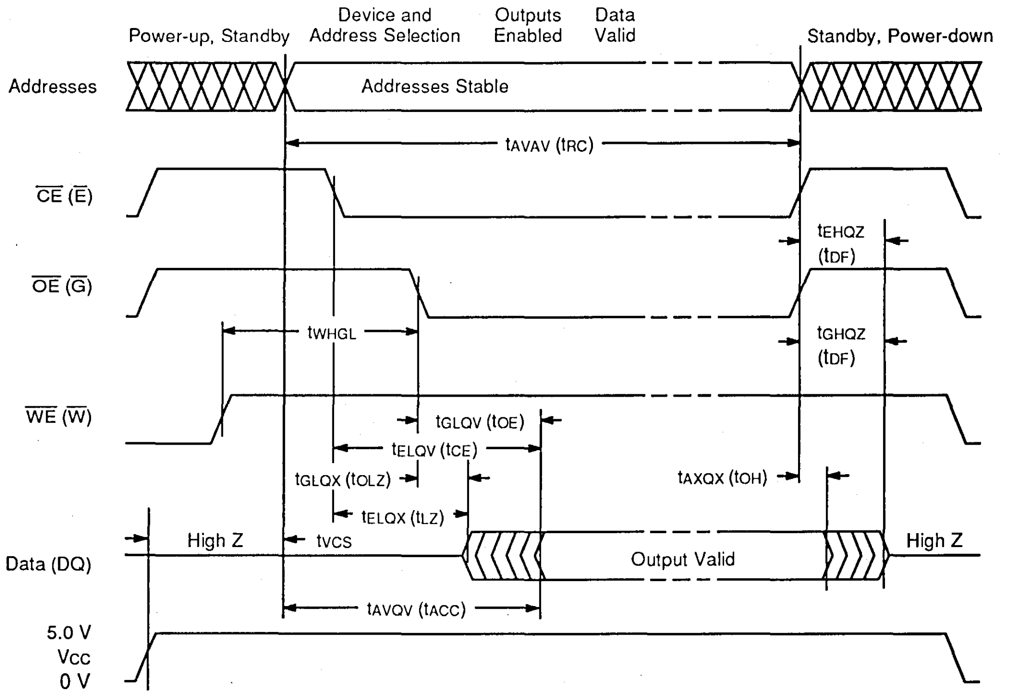


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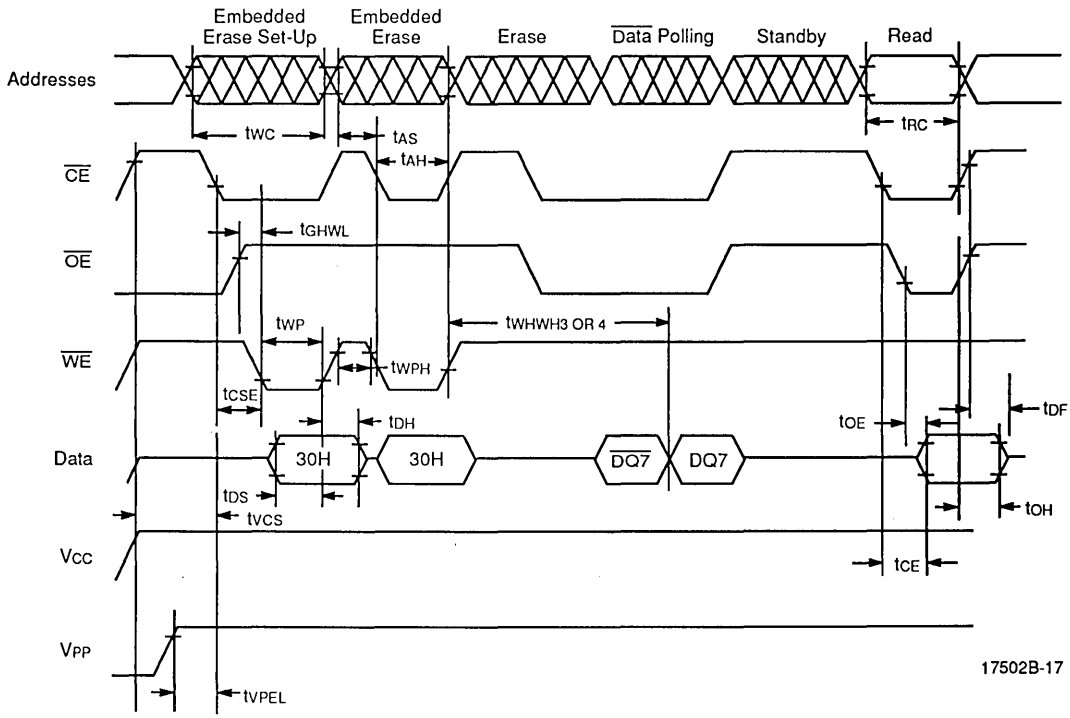
Figure 10. AC Waveforms for Read Operations

SWITCHING WAVEFORMS

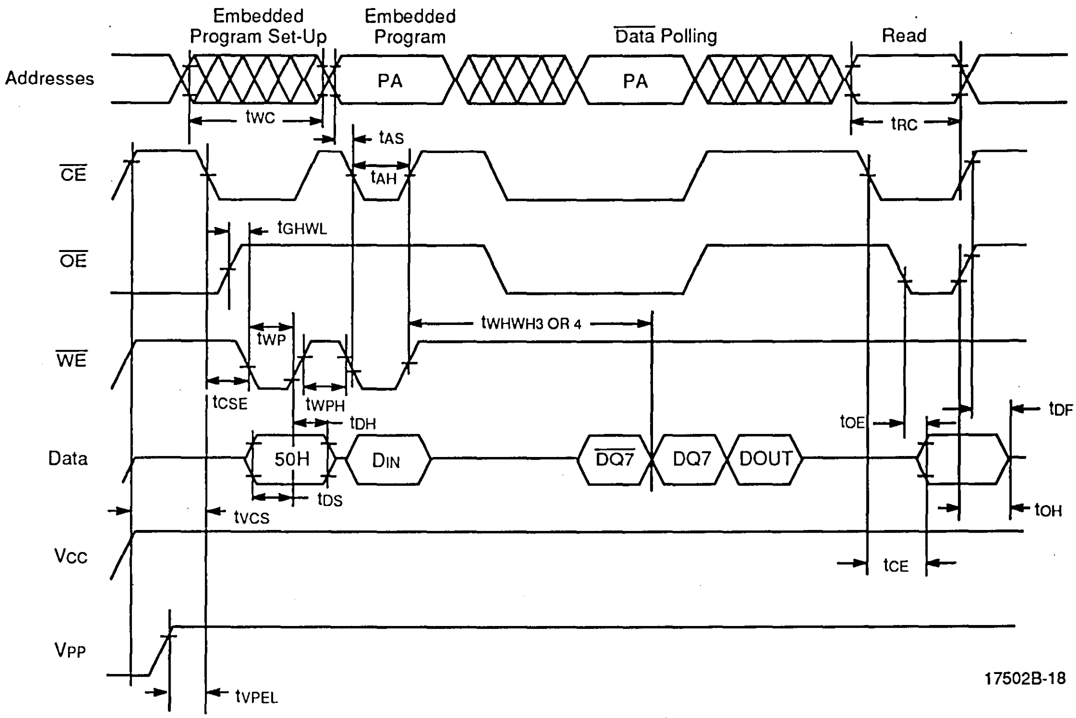


Note:

1. $\overline{DQ7}$ is the output of the complement of the data written to the device.

Figure 11. AC Waveforms for Embedded Erase Operation

SWITCHING WAVEFORMS



Notes:

1. *DIN is data input to the device.*
2. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
3. *DOUT is the output of the data written to the device.*

Figure 12. AC Waveforms for Embedded Programming Operation

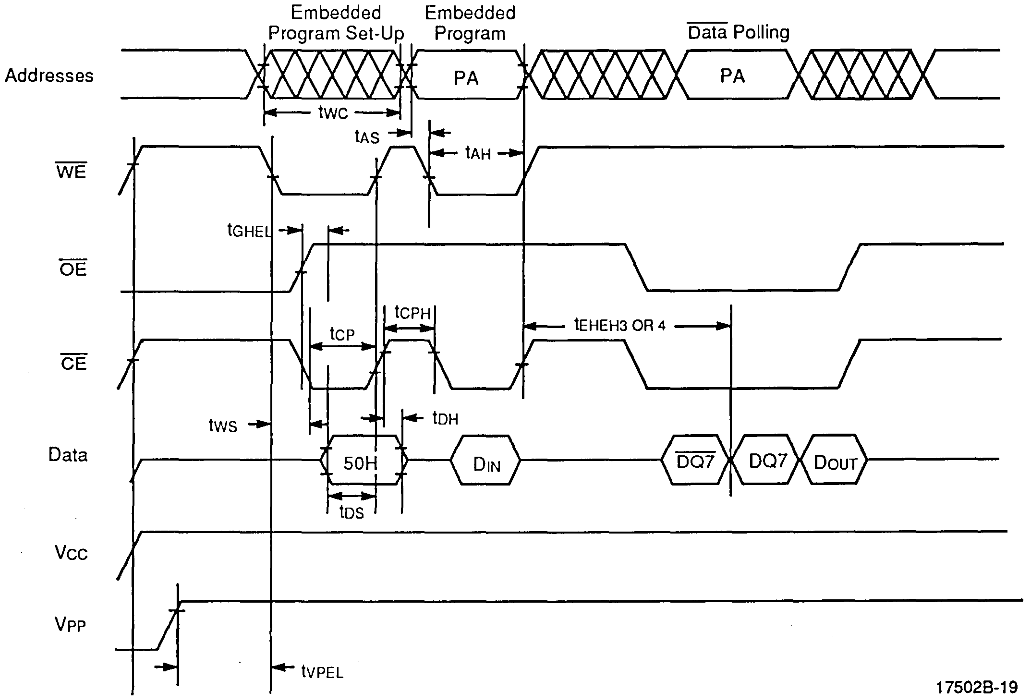
AC CHARACTERISTICS—Write/Erase/Program Operations (Notes 1–6) Alternate $\overline{CE}$ Controlled Writes

Parameter Symbols				Am28F020A					
JEDEC	Standard	Parameter Description		-90 -95	-120 —	-150 —	-200 —	-250 —	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (Note 6)	Min Max	90	120	150	200	250	ns
t_{AVEL}	t_{AS}	Address Set-Up Time	Min Max	0	0	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time	Min Max	45	50	60	75	75	ns
t_{DVEH}	t_{DS}	Data Set-Up Time	Min Max	45	50	50	50	50	ns
t_{EHDX}	t_{DH}	Data Hold Time	Min Max	10	10	10	10	10	ns
t_{OEH}		Output Enable Hold Time for Embedded Algorithm only (See Figure 8)	Min Max	10	10	10	10	10	ns
t_{GHEL}		Read Recovery Time before Write	Min Max	0	0	0	0	0	µs
t_{WLEL}	t_{WS}	WE Set-Up Time by $\overline{CE}$	Min Max	0	0	0	0	0	ns
t_{EHWK}	t_{WH}	WE Hold Time	Min Max	0	0	0	0	0	ns
t_{ELEH}	t_{CP}	Write Pulse Width	Min Max	65	70	80	80	80	ns
t_{EHEL}	t_{CPH}	Write Pulse Width HIGH	Min Max	20	20	20	20	20	ns
t_{EHEH3}		Embedded Programming Operation (Note 4)	Min Max	14	14	14	14	14	µs
t_{EHEH4}		Embedded Erase Operation (Note 5)	Typ Max	5	5	5	5	5	S
t_{VPEL}		V_{PP} Set-Up Time to Chip Enable LOW (Note 6)	Typ Max	100	100	100	100	100	ns
t_{VCS}		V_{CC} Set-Up Time to Chip Enable LOW (Note 6)	Typ Max	50	50	50	50	50	µs
t_{VPPR}		V_{PP} Rise Time 90% V_{PPH} (Note 6)	Typ Max	500	500	500	500	500	ns
t_{VPPF}		V_{PP} Fall Time	Min Max	500	500	500	500	500	ns
t_{LKO}		$V_{CC} < V_{LKO}$ to Reset (Note 6)	Min Max	100	100	100	100	100	ns

Notes:

1. *Read timing characteristics during read/write operations are the same as during read-only operations. Refer to AC Characteristics for Read Only operations.*
2. *All devices except Am28F020A-95. Input Rise and Fall times: < 10 ns; Input Pulse Levels: 0.45 V to 2.4 V Timing Measurement Reference Level: Inputs: 0.8 V and 2.0 V; Outputs: 0.8 V and 2.0 V*
3. *Am28F020A-95. Input Rise and Fall times: < 10 ns; Input Pulse Levels: 0.0 V to 3.0 V Timing Measurement Reference Level: Inputs and Outputs: 1.5 V*
4. *Embedded Program Operation of 14 µs consists of 10 µs program pulse and 4 µs write recovery before read. This is the minimum time for one pass through the programming algorithm.*
5. *Embedded erase operation of 5 sec consists of 4 sec array pre-programming time and one sec array erase time. This is a typical time for one embedded erase operation.*
6. *Not 100% tested.*

SWITCHING WAVEFORMS

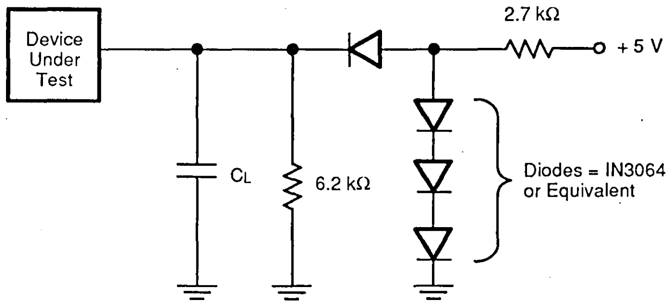


Notes:

1. *DIN is data input to the device.*
2. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
3. *DOUT is the output of the data written to the device.*

Figure 13. AC Waveforms for Embedded Programming Operation Using $\overline{CE}$ Controlled Writes

SWITCHING TEST CIRCUIT



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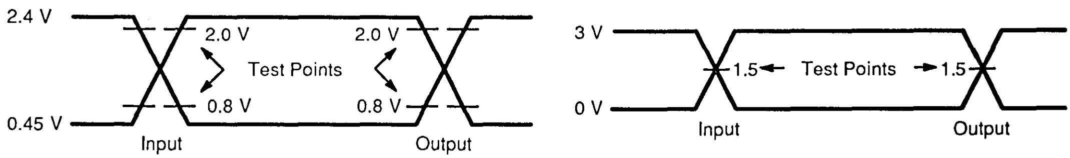
C_L = 100 pF including jig capacitance

SWITCHING TEST WAVEFORMS



All Devices Except Am28F020A-95

AC Testing: Inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Input pulse rise and fall times are < 10 ns.

For Am28F020A-95

AC Testing: Inputs are driven at 3.0 V for a logic "1" and 0 V for a logic "0". Input pulse rise and fall times are < 10 ns.

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ERASE AND PROGRAMMING PERFORMANCE

Parameter	Limits			Unit	Comments
	Min	Typ	Max (Note 3)		
Chip Erase Time		1 (Note 1)	10 (Note 2)	s	Excludes 00H programming prior to erasure
Chip Programming Time		4 (Note 1)	25	s	Excludes system-level overhead
Write/Erase Cycles	100,000			Cycles	
Byte Program Time		14		µs	
			96 (Note 4)	ms	

Notes:

1. *25°C, 12 V VPP*
2. *The Embedded algorithm allows for 60 second erase time for military temperature range operations.*
3. *Maximum time specified is lower than worst case. Worst case is derived from the Embedded Algorithm internal counter which allows for a maximum 6000 pulses for both program and erase operations. Typical worst case for program and erase is significantly less than the actual device limit.*
4. *Typical worst case = 84 µs. DQ5 = "1" only after a byte takes longer than 96 ms to program.*

LATCHUP CHARACTERISTICS

	Min	Max
Input Voltage with respect to VSS on all pins except I/O pins (Including A9 and VPP)	–1.0 V	13.5 V
Input Voltage with respect to VSS on all pins I/O pins	–1.0 V	VCC + 1.0 V
Current	–100 mA	+100 mA
Includes all pins except VCC. Test conditions: VCC = 5.0 V, one pin at a time.		

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

DATA SHEET REVISION SUMMARY FOR Am28F020A

Data sheet is Final now, and not Preliminary.

Functional Description – Table 1

Legend: V_{PP} should be less than or equal to V_{CC} + 2 V

Erase, Program and Read Mode – Write Operations

Removed Command Register Table and Bit assignments.

Erase, Program and Read Mode – Read Command

The statement requiring a 6 µs wait before accessing the first addressed location was removed.

Table 3 – Am28F010A Command Definitions

The note describing a 6 µs wait before accessing the first addressed location was removed.

Figure 5 – Embedded Erase Algorithm

Clarified figure to illustrate the Embedded Erase Algorithm.

Embedded Programming Algorithm

Added references that addresses are also latched on the falling edge of $\overline{CE}$, and data is also latched on the rising edge of $\overline{CE}$, whichever happens later.

Figure 6 – Embedded Programming Algorithm

Clarified figure to illustrate the Embedded Erase Algorithm.

Write Operation Status – Data Polling DQ7

Added statement that an attempt to read the device at a valid address will produce valid data on DQ7.

Figure 7a – $\overline{\text{Data}}$ Polling Algorithm

Clarified figure to illustrate the $\overline{\text{Data}}$ Polling Algorithm.

Write Operation Status – Toggle Bit DQ6

Added statement that successive reads from the device will result in DQ6 toggling between '1' and '0'.

Figure 7b – Toggle Bit Algorithm

Clarified figure to illustrate the Toggle Bit Algorithm.

Figure 8a – AC Waveforms for $\overline{\text{Data}}$ Polling During Embedded Algorithm Operations

Clarified figure to illustrate the $\overline{\text{Data}}$ Polling Algorithm.

DQ5 – Exceeded Timing Limits

Added statement that this is a failure condition and the device may not be used again.

Figure 8b – AC Waveforms for Toggle Bit During Embedded Algorithm Operations

Clarified figure to illustrate the Toggle Bit Algorithm.

Parallel Device Erasure

Removed erroneous reference.

Reset Command

Added this section.

In-System Programming Considerations

Title was changed.

Auto Select Command

Added second paragraph describing the Auto select command.

DC Characteristics – TTL/NMOS Compatible

Added Note 4. Those characteristics are not 100% tested.

DC Characteristics – CMOS Compatible

Added Note 4. Those characteristics are not 100% tested.

AC Characteristics – Write/Erase/Program Operations (Notes 1–6)

Embedded Programming Operation (t_{WHWH3}) requires minimum of 14 µs.

Figure 11 – AC Waveforms for Embedded Erase Operation

$\overline{\text{Data}}$ Polling section does not require a Program Address. DQ7 was inserted.

Figure 12 – AC Waveforms for Embedded Programming Operation

Embedded Program section needs a Program Address. DQ7 was inserted.

AC Characteristics – Write/Erase/Program Operations (Notes 1–6)

Alternate $\overline{CE}$ Controlled Writes

Embedded Programming Operation (t_{EHEH3}) requires minimum of 14 µs.

Figure 13 – AC Waveforms for Embedded Programming Operation Using $\overline{CE}$ Controlled Writes

Embedded Program section requires Program Address. DQ7 was inserted. Changed t_{WHWH3} to t_{EHEH3}.

SECTION

3 GENERAL INFORMATION AND APPLICATION NOTES

Embedded Algorithms In Flash Memories

Advanced Micro Devices

Application Note
by Mike Harris

Despite their instant popularity, the first 12.0 V Flash memories introduced in the late 80s had several drawbacks. One of the concerns most often voiced by system software designers was the need for cumbersome programming sequences to program and erase the devices. Embedded Algorithms were developed to eliminate these concerns.

THE DRAWBACKS OF PROGRAMMING WITH FIRST GENERATION ALGORITHMS

Figure 1 shows the flowchart for programming Flash devices using first generation algorithms. The steps needed to program a single byte of memory are illustrated in simplistic block diagram form. The programming code itself is obviously much more complex. The erase sequence is similar except Flash devices must first be programmed to all zeros prior to being erased.

A completed listing of code performing all of the program/erase functions for a Flash memory typically contains 100–200 lines. Although sample code can be obtained from the device manufacturer, designers usually need to generate their own code specific to the individuality of their application.

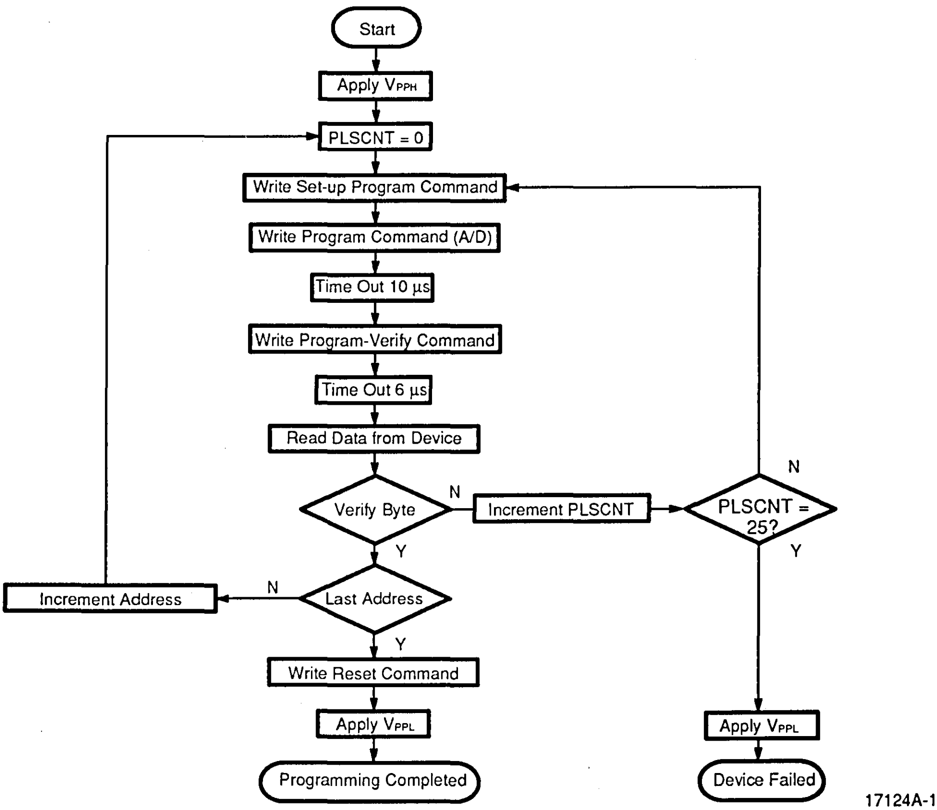

Figure 1. First Generation Programming Algorithm

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This extensive programming requirement has many disadvantages and can be quite costly. First, of course, is the amount of time required to generate and debug this code. Since prior designs utilizing EPROMs were programmed offline, most software engineers are not familiar with the programming of Flash memories. They find that the programming process is initially lengthy and error prone. The cost to the user includes not only the obvious cost of software development but also the lost opportunity costs resulting from time to market delays.

Another concern is the potential long term impact on system reliability caused by overstressing a Flash device. Since cycling endurance can be affected by improper writing or erasing, software bugs can cause latent field failures even in systems that appear error free in development. In fact, most customer returns at AMD have been traced to software errors generated during system development.

SIMPLIFYING FLASH PROGRAMMING

AMD was the first company to recognize the need to simplify programming of Flash memories and incorporated it in the design of its first 2 Mbit Flash memory. Figure 2 illustrates the Embedded Program™ Algorithm. The system processor simply issues the write set-up command followed by the write command and the internal state machine on the device takes over control of the write operation. The system processor simply does $\overline{\text{DATA}}$ polling until the device indicates that the write operation is complete. This simplicity is even more pronounced during an erase operation since each byte of the memory must be individually programmed prior to erase. The Embedded Erase™ Algorithm internally writes all zeros to each byte and then performs the erase. This entire sequence is controlled internally and is transparent to the host processor.

OTHER ADVANTAGES OF EMBEDDED ALGORITHMS

Besides simplifying the complex programming of Flash memories, Embedded Algorithms offer these other important advantages to the designer:

Reduced system overhead – Since the Embedded Algorithms are completely automatic, the system processor is free to perform other functions, such as servicing interrupts, during the write or erase operations.

Improved program/erase time – The Embedded Algorithms are designed to perform write/erase operations in the most efficient way possible. All system overhead is eliminated.

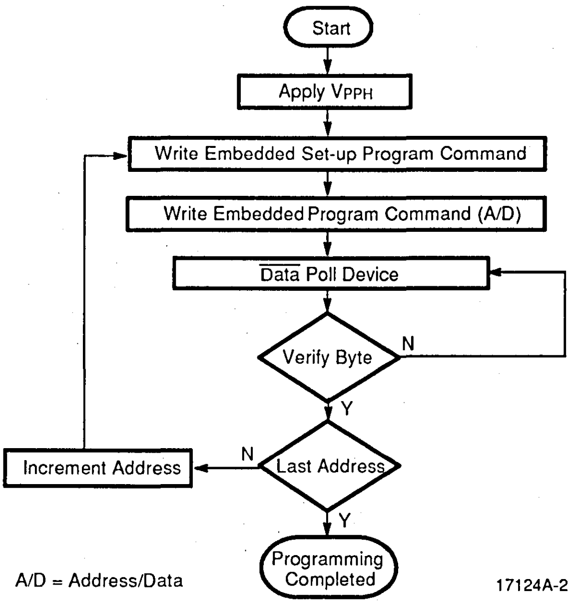

Figure 2. Embedded Programming Algorithm

Increased cycling endurance – By including a self correcting mechanism, Flash memories incorporating AMD's Embedded Algorithms will operate to a minimum of 100,000 endurance cycles.

JEDEC standards for self programming of Flash devices are now being developed. The Embedded Algorithms incorporated in all of AMD's Flash devices conform to these standards.

SUMMARY

The benefits of Embedded Algorithms are available today from AMD on first generation 12.0 V devices (Am28F010A and the Am28F020A) and well as the 5.0 V, fully sectored Am29F family. Employing these algorithms in existing designs will allow you to increase your system's endurance to over 100K cycles. In new designs, system development will be simplified and time to market reduced.

Achieving 100,000 Cycle Endurance: A Report on Flash Endurance and Reliability

Advanced Micro Devices

This article discusses the Advanced Micro Devices approach to achieving and guaranteeing superior Flash endurance. The data presented will prove that AMD's 100,000 cycle Flash devices provide the highest endurance and reliability levels in the industry.

Today's typical Flash applications are perfectly suited to 10,000 cycle endurance devices. This industry standard level of endurance is appropriate for applications such as PC BIOS and other designs that require infrequent code updates. At the same time, new Flash applications are currently being developed which require data to be reprogrammed more than 10,000 times. For applications of this sort, such as solid state hard disks, industry standard Flash devices cannot be counted on to perform reliably. AMD has revolutionized this segment of the Flash market with the new Embedded Program™ and Embedded Erase™ Algorithms, which guarantee 100,000 write/erase cycles.

What is Endurance?

Endurance is a popular term in the Flash industry. What exactly does endurance mean, and how should it be measured?

AMD defines *endurance* as the number of write/erase cycles a Flash device can withstand without failure. Endurance must be measured under the worst-case conditions of the system environment, in order to guarantee products which operate across the range of data sheet specifications.

Understanding endurance is essential for AMD, in order to manufacture superior Flash devices. Flash consumers must also understand the issues involved in achieving and guaranteeing endurance, so that they are assured of choosing the best devices on the market. In particular, consumers whose designs require extended endurance, i.e., more than 10,000 cycles, should be especially concerned with these issues.

Two failure modes are typically associated with Flash memories: hard failures and soft failures. *Hard failures* are complete and unrecoverable, and their root cause lies in the manufacturing process. Closely controlled manufacturing processes eliminate hard failures in AMD's Flash devices, increasing the level of device quality and reliability.

Flash memory endurance is typically limited by *soft failures.* Soft failures occur when random bits erase too quickly. Flash memories are erased in blocks, and since not all bits exhibit identical erase characteristics, a fast-erasing bit must be exposed to the erase voltage until the slowest bit is erased. As a result, the fast bits can be erased "too much," forcing the transistor cells into depletion mode. This condition is called *over-erase.* An over-erased bit produces a *leakage current* which causes an entire column to malfunction. The result seen by the user is a system failure.

AMD's Embedded Algorithm: The Key to Extended Endurance

The soft failures described above occur in all Flash memories. These failures are precisely the reason that today's Flash devices are currently limited to 10,000 cycles. Applications which perform more than 10,000 write/erase cycles may jeopardize system reliability if standard rated 10,000 cycle Flash devices are designed in.

Now, Advanced Micro Devices makes extended endurance Flash applications possible with the introduction of the Embedded Program and Embedded Erase Algorithms. AMD's Embedded Algorithm incorporates a function which *seeks out and corrects soft failures,* allowing these devices to be guaranteed for *100,000 write/erase cycles* (actual device performance may be orders of magnitude greater). The Embedded Algorithm extends endurance by automatically recovering over-erased bits, making soft failures transparent to the system. Flash devices that do not support these algorithms are incapable of recovering soft failures; thus, they cannot guarantee 100,000 write/erase cycle endurance. Only AMD offers this self-correcting mechanism that makes extended endurance Flash applications possible.

Failure Rate Comparison

Figure 1 illustrates AMD's significant endurance advantage over other standard rated 10,000 cycle Flash products. The graph shows that the endurance of AMD's 100,000 cycle Embedded Algorithm devices represent a significant breakthrough in Flash endurance, as illustrated by the nearly flat failure rate curve.

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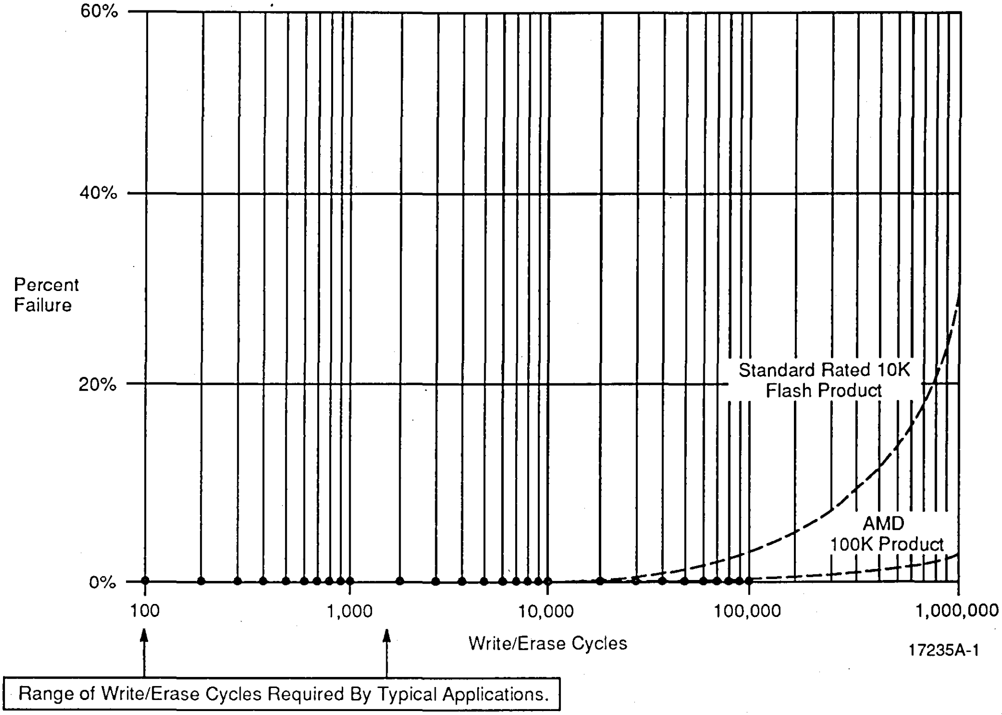

Figure 1. Failure Rate Comparison: Standard Rated 10K Cycle Flash Product vs. AMD 100K Rated Product

AMD's Embedded Algorithm devices represent a significant technology advancement in Flash endurance.

Test results prove that AMD's Flash technology produces superior endurance. As Table 1 shows, the endurance failure rate at 100,000 cycles for AMD's Embedded Algorithm devices is less than 0.25%.

Table 1. AMD Embedded Algorithm Endurance Data

Device	No. of Lots	Initial Qty	Failures @ 10K	Failures @ 25K	Failures @ 50K	Failures @ 100K
Am28F010A	5	1159	0/1159	0/445	0/445	1/445
Am28F020A	2	420	2/420	1/418	0/248	0/248

Endurance and Reliability

Endurance and reliability are equally important issues, though not exactly synonymous. Reliability refers to the absence of hard failure mechanisms, which can be eliminated during processing. AMD's Flash manufacturing processes are carefully controlled to produce products with immunity from hard failures. Endurance, as discussed earlier, relates to the occurrence of soft failures. AMD's Embedded Algorithm guarantees superior endurance by correcting soft failures in-system.

AMD understands that from a customer's perspective, all failures are unacceptable, regardless of their cause. For this reason, AMD's Flash devices combine unsurpassed reliability and endurance for protection against hard failures as well as soft failures. Reliability tests show that AMD's Flash process technology provides unmatched immunity from hard failures: *less than 10 FITs* on both High Temperature Operating Life (HTOL, 150°C, V_{CC} = 6.5 V) and Data Retention Bake (DRB, 150°C, unbiased) using the 60% UCL calculation at 55°C.

Reliability data also prove that AMD's unparalleled endurance is achieved without sacrificing reliability. HTOL and DRB reliability tests were performed on the same Embedded Algorithm devices that had been cycled 100,000 times. *Table 2 shows that even after 100,000 cycles, there were NO reliability failures.* Flash endurance and reliability are two distinct and important issues, and the data proves that AMD is superior in both.

Table 2a. Unbiased DRB @ 150°C after 100,000 Write/Erase Cycles

Device	Initial Qty	Failures @ 48 Hrs	168 Hrs	500 Hrs	1000 Hrs
Am28F010A	100	0/100	0/100	0/100	0/100

Table 2b. HTOL Reliability Results @ 6.5 V V_{CC}, 150°C after 100,000 Write/Erase Cycles

Device	Initial Qty	Failures @ 48 Hrs	168 Hrs	500 Hrs	1000 Hrs
Am28F010A	180	0/180	0/180	0/180	0/180

AMD is the technology leader in Flash memories. At the 10,000 cycle level, AMD offers devices compatible with the industry standard. At the 100,000 cycle level, AMD's Embedded Algorithm devices are unmatched in the industry, truly guaranteeing 100,000 cycle endurance. For leadership in higher endurance, reliability, and quality in Flash memories, look to AMD: your Flash leader!

For further information, please contact your local AMD sales representative.

5.0 Volt-only Flash Memory Negative Gate Erase Technology

Advanced Micro Devices

Application Note

Advanced Micro Devices' Negative Gate Erase, 5.0 V-only technology is the most cost-effective and reliable approach to single-supply Flash memories. The innovative approach AMD has taken to 5.0 V-only technology provides designed-in reliability that is equal to that of its 12.0 V devices. In fact, transistor oxides are not subjected to any voltages higher than on AMD's 12.0 V devices. This approach minimizes internal power generating requirements which results in a negligible impact on die size because of the 5.0 V-only reprogramming capability.

The minimal power requirement of AMD's Negative Gate Erase, 5.0 V-only technology is made possible by design techniques which use the systems' Vcc power supply to provide the 10-20 mA (peak) current for Band-to-Band tunneling. Erase operations are performed when the system Vcc voltage is applied to the source terminal and the gate is pumped to a negative voltage. Less than 10 µA of current is required on the gate to enable Fowler-Nordheim tunneling.

Negative Gate Erase uses the same mechanism to erase a cell as the company's 12.0 V devices. Programming operations are performed with positive voltage pumped on the gate terminal at less than 10 µA of current. Hot channel electrons are injected into the floating gate in the same manner as 12.0 V devices.

The 5.0 V-only cell layout and geometry are comparable to the 12.0 V Flash memory cell. This ensures long term scalability equal to conventional 12.0 V flash designs without any penalty in die size. AMD added Dual Layer Metal (DLM) technology to implement its flexible sector erase architecture. AMD's unique sector isolation ensures reliable endurance cycling of at least 100K cycles for each sector whether erased individually or in combination.

AMD's innovative charge pump design techniques allow this device to consume less power than 12.0 V devices during write operations. Approximately 90% charge pump efficiency is achieved with AMD's unique diode V_t cancellation techniques. In addition, the charge pump design minimizes noise and ripple associated with voltage conversion circuits.

The culmination of these innovative design techniques makes this device ideal for power sensitive portable applications.

CHARGE PUMP CHARACTERISTICS—OVERVIEW

Before discussing the details of AMD's 5.0 V-only technology it is helpful to review the basic concepts of charge pump design. These concepts apply to stand alone DC/DC converters as well as charge pumps integrated into the device silicon. All charge pump designs share common characteristics. For instance the available current from a voltage pump is determined by the Z_{out} and V_{out} of the circuit.

- Z_{out} is proportional to n/(C*F)
  - — n = # of charge pump stages
  - — C = capacitor size of each stage
  - — F = clock rate
- V_{out} is proportional to n · (V_{CC} – V_{Diode})
  - — n = # of charge pump stages
  - — V_{out} = Device Vcc
  - — V_{Diode} = voltage drop of charge pump blocking diode
- Noise is proportional to L · (di/dt)
  - — L = bond wire inductance
  - — di/dt = rate of current change

There are a number of issues to note about these relationships.

The silicon area of the charge pump is determined by the product of n and C (number of stages times the capacitor size). Efficient use of chip silicon requires this product to be as small as possible.

The efficiency of the voltage generated by the pump circuitry is increased as the effective voltage drop of the charge pump blocking diode is reduced (V_{CC} – V_{Diode}).

The voltage available at the output of the pump (when current is drawn) increases when Z_{out} decreases. Z_{out} decreases as either n is reduced or the product C * F increases. In addition, once a given Z_{out} is determined the values of C and F may vary in inverse proportion while maintaining the same product value.

Noise generated by the charge pump is minimized with a lower F (when n · C is large). But as F decreases C must increase in order to keep the product C*F constant.

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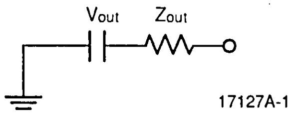


Charge Pump Model

Negative Gate Erase Technology

Negative Gate Erase is used for erase operations in order to minimize the current drawn from the erase charge pump. In order to illustrate the importance of this, it is beneficial to first describe how today's 12.0 V V_{PP} Flash devices operate. Then conventional techniques of generating 12.0 V from a 5.0 V V_{CC} internally will be examined before discussing the benefits of Negative Gate Erase.

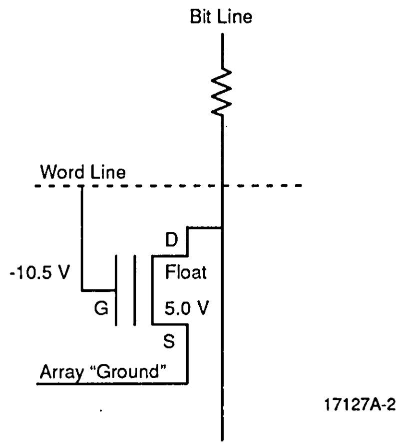
Today's 12.0 V Flash devices erase the memory cell at the Source terminal with 12.0 V applied. The gate is grounded and the drain is left floating. The external Vpp circuit supplies the Vpp current required for erase operations. This provides the 10–20 mA (peak) Band-to-Band tunneling current along with the Fowler-Nordheim tunneling current required to remove charge off the floating gate.

Conventional techniques in generating 12.0 V at the source terminal from a 5.0 V V_{CC} internal supply require huge charge pumps in order to supply the 10-20 mA (peak) of Band-to-Band tunneling current. This approach requires significant silicon real estate (charge pump area = n*C) and consumes large amounts of power [(12.0 V * 30 mA) ÷ Efficiency ≥ 360 mW].

Multiple transistor EEPROM 5.0 V-only technology uses charge pumps to internally raise the gate voltages to between 18 and 20 V at < 10 µA. A multiple transistor approach requires one and a half to twice the silicon real estate as single-transister approaches. Both conventional 12.0 V Flash and AMD's 5.0 V-only technology produce approximately half the electric field on the tunnel oxide as with EEPROM technology. The lower tunnel oxide fields extend the life of the oxide by orders of magnitude. In addition, EEPROM technology implements uniform channel tunneling instead of source-side tunneling as with conventional 12.0 V and AMD's 5.0 V-only technology. Uniform channel tunneling stresses the entire oxide region while source-side tunneling only stresses a small region of the oxide.

AMD's Negative Gate Erase technique actually provides the same electric fields to the Flash memory cell and uses the same erase mechanisms as its 12.0 V Flash devices. Negative Gate Erase is used in order to reduce the current drawn from the erase charge pump. The Band-to-Band tunneling current (10-20 mA peak) comes directly from the system V_{CC} through the Array Ground terminal. This is the most efficient way to use an existing system V_{CC} supply. The current required from the Negative Gate Erase charge pump is less than 10 µA at -10.5 V. This reduces the internal power consumption in relation to conventional 12.0 V approaches.

A circuit diagram of Negative Gate Erase is illustrated below.



5.0 V-Only Negative Gate Erase Circuitry

Notes:

1. *Gate terminal is pumped to -10.5 V @ <10 mA current*
2. *10 mA – 20 mA (peak) erase current is provided to the Source terminal by the system's Vcc supply*

Key:

D = Drain terminal

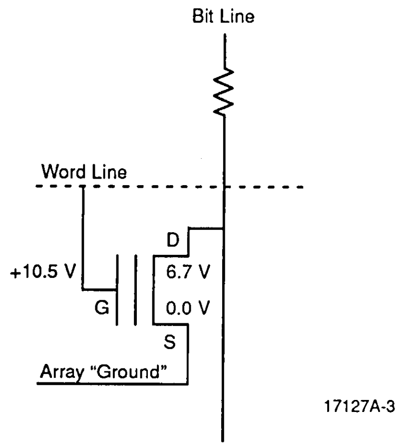
G = Gate terminal

S = Source terminal

5.0 V-only Programming

AMD's 5.0 V-only programming technique provides the same electric fields to the memory cell and uses the same programming mechanisms as its 12.0 V Flash devices. The drain is pumped to 6.7 V from 5.0 V and supplies approximately 0.5 mA of current per cell. The internal power generation required for the Channel Hot Electron injection mechanism is minimized because the charge pump only delivers a 34% voltage increase from the base Vcc supply. This also provides the benefit that the cell's programming characteristics remain constant even if the system Vcc supply varies. This current supplies the Channel Hot Electrons that are injected into the floating gate in order to program the memory cell. The current required by the gate voltage charge pump is less than 10 µA. This minimizes internal power consumption.

A circuit diagram of the programming circuitry is illustrated below.



5.0 V-only Drain Programming

Notes:

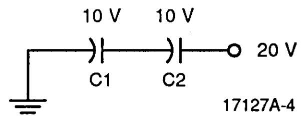
1. *Gate terminal is pumped to +10.5 V @ < 10 mA current*
2. *Drain terminal is pumped to 6.7 V from 5.0 V Vcc supply @ 0.5 mA*

AMD's 5.0 V-ONLY DEVICE EQUALS THE RELIABILITY OF 12.0 V DEVICES

Equivalent Electric Fields Charge Pump Circuitry

One component of device reliability is related to the electric fields applied across internal device transistors. Very high electric fields may cause oxide breakdown and hence reliability problems. One of the main design and reliability requirements in AMD's 5.0 V-only circuit implementation was the maintenance of electric fields across the charge pump oxides equivalent to those of the oxides subject to high voltage in the 12.0 V device. AMD's techniques minimize the electric fields across the oxides to be equivalent to those across the device transistor oxides during standard Read operations of the 12.0 V device. This ensures that the 5.0 V-only design will not be more susceptible to oxide failures than 12.0 V devices. There has never been any physical damage to an oxide from the high voltages internal to AMD's 12.0 V Flash device.

One way to maintain low electric fields across transistor oxides is to stack multiple capacitors together. This circuit technique delivers a large output voltage while maintaining low electric fields across each oxide. As an example, with an oxide that is able to reliably withstand voltages of 10 V, a circuit can be constructed to provide 20 V by stacking (in series) two capacitors with 10 V across each oxide. This circuit ensures that the electric fields remain within the specified limits.



Capacitors Charge Pump Model

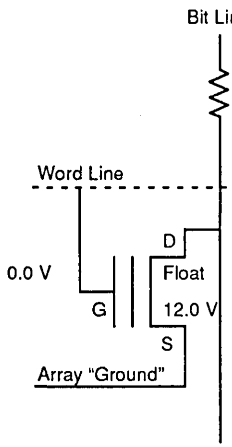
Memory Cell Circuitry

It is important to note that the electric fields applied to the data storage memory cells of the 5.0 V-only device are the same as that of the 12.0 V device. This ensures that the 5.0 V-only design will not be more susceptible to oxide failures than 12.0 V devices. An observable measure that the electric fields are indeed the same is found in the erase time parameter. Erase time depends upon the electric field across the floating gate and the thickness of the tunnel oxide (T_{OX}). T_{OX} and the erase time of the 5.0 V-only device are the same as in the 12.0 V device. Therefore the electric field is the same in both devices.

The electric fields of the 5.0 V circuit are also demonstrated by analyzing the coupling ratios in the memory cell transistor. However, it is first beneficial to discuss the coupling ratios of standard 12.0 V Flash circuitry. We will use the erase circuit as an example. The same concepts apply to the programming circuitry.

Electric Fields in Standard 12.0 V V_{PP} Erase Circuits

The standard Flash memory cell applies 12.0 V to the Source terminal. The Gate terminal is grounded and the drain is left floating. The actual electric field seen by the tunnel oxide is a superposition of three components. One is because the field generated by the trapped electrons on the floating gate. This is the state of a programmed memory cell prior to erase. The other two result from coupling of the voltage between the word line (Gate terminal)/floating gate and between the source terminal/ floating gate. In the case of standard 12.0 V Vpp programming, the only component from the voltage coupling is between the source terminal and the floating gate. There is no coupling from the word line because it is at a zero voltage potential. The resulting electric field never exceeds a peak value of 10 mV/cm.



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Standard 12.0 V V_{PP} Erase

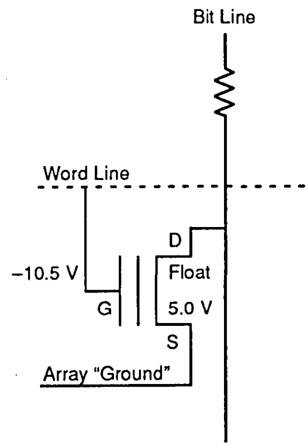
Notes:

1. *Tunnel oxide (Tox) electric field is determined by superposition.*
- *Floating Gate Voltage from stored electrons reduces voltage across Tox*
- *Source Coupling Voltage on the floating gate reduces the voltage across the Tox*
2. *Total electric field across Tox due to superposition is <10 m V/cm.*

Equivalent Electric Fields in AMD's 5.0 V-only Negative Gate Erase Ciruitry

AMD's Negative Gate Erase circuitry applies the same electric fields to the memory cell as the 12.0 V device. The Gate terminal is negatively pumped to –10.5 V and the source terminal is at 5.0 V supplied by the system V_{CC} supply. The drain terminal is left floating. The actual electric field seen by the tunnel oxide is a superposition of three components. One is due to the field generated by the trapped electrons on the floating gate. This is the state of a programmed memory cell prior to erase. The other two result from coupling of the voltage between the word line (Gate terminal)/ floating gate and between the source terminal/ floating gate. This time there is voltage coupling from both the Source terminal and word line. The resulting electric field is the same as in the 12.0 V device. The electric field is always ≤ 10 mV/cm.

In addition, the Negative Gate Erase approach actually produces a lower electric field across the cell junctions. This is because the source terminal is subjected to 5.0 V levels instead of 12.0 V.



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5.0 V-only Negative Gate Erase

Notes:

1. *Tunnel oxide Tox electric fields determined by superposition.*
   - *Floating Gate Voltage from stored electrons reduces the voltage across the Tox*
   - *Gate Coupling Voltage on the floating gate reduces the voltage across the Tox*
   - *Source Coupling Voltage on the floating gate reduces the voltage across the Tox*
2. *Total electric field across the Tox due to superposition is < 10 m V/cm.*

DATA INTEGRITY

Ruggedized Programmability

AMD's 5.0 V-only approach is designed not to be sensitive to variations in the system Vcc supply during programming operations.

This is achieved by pumping the drain terminal to 6.7 V. The device actually compensates for any system level variations in the Vcc supply. During programming the word line is pumped to +10.5 V and the source terminal is grounded. These voltage conditions and resulting electric field are the same as in 12.0 V devices.

Sector Write Protection

AMD implements a Dual Layer Metal (DLM) bussing technique in order to provide the most cost-effective and reliable method to individually isolate sectors during sector erase operations. This technique inhibits the presence of high voltage in non-addressed sectors from disturbing fixed data. Data in non-addressed sectors is isolated from all other sector program and erase operations.

MINIMIZING CHARGE PUMP NOISE AND VOLTAGE RIPPLE

Minimizing Noise

AMD's charge pump circuitry minimizes noise with a multi-stage pump design. Each stage has the same clock rate but is out of phase with all other stages. The phase shifting minimizes potential noise from any of the individual pumps. This technique delivers a very smooth and constant source of power. A V-8 automobile engine serves as an excellent analogy. Each of the eight stages of the charge pump is 45° out of phase. Each packet of charge is delivered in a way to provide a smooth flow of current.

Troubleshooter's Guide to Flash Software Implementation Issues

Advanced Micro Devices

Application Note

by Amita Patel

AMD has found that the vast majority of flash failures result from software or V_{PP} implementation issues. Over 80% of Flash Customer Corrective Action Requests (CCARs) that we receive result from software implementation errors. The balance of the Flash failures are due to Electrical Over Stress on the V_{PP} pin. In this application note, we will focus on the most common cause of software implementation failures. Please use this information to troubleshoot your Flash memory design. The intent of the information contained in this application note is to allow you to quickly resolve incorrect software implementation issues. In the majority of cases, the following guidelines will enable you to identify and resolve the cause of failure.

Types of Software Implementation Issues

There are two types of Flash endurance cycling failures: hard failures and soft failures. Hard failures are unrecoverable and occur in Flash, EPROM, and EEPROM technologies where high voltages are generated in the peripheral circuitry. Closely controlled manufacturing processes, design techniques, and test methodologies are used to minimize hard failures in AMD's Flash devices. Soft failures are the dominant flash failure mode, and they are recoverable. Although hard failures do exist, the failure rate is orders of magnitude less than soft failures.

The most common failures are soft failures that occur as a result of incorrect implementation of the program and erase algorithms. This document will address the following failures: over erase, incorrect implementation of the programming algorithm, and under erase.

Over Erase

There are three ways to detect over erase. First, over erase may cause programmed bits to appear erased when V_{CC} is varied between 4.5 V and 5.5 V. Second, an over erased bit is usually detected during the succeeding programming cycle. This condition will manifest itself as an inability to program verify bits in-system during the programming. Finally, an extreme case of over erasure will result in the inability to read the manufacturing ID.

Incorrect Implementation of the Programming Algorithm

A programming algorithm failure results in incorrect data or inability to program the device.

Under Erase

During the read operation an under erase failure will result in the bits appearing programmed after they have been erased with an incorrect algorithm.

All of the software implementation failures discussed within this document can be resolved by using AMD's Embedded Algorithms. Over erase failures can be eliminated by AMD's Embedded Algorithm devices, which insure correct implementation of both the program and erase algorithms. Programming algorithm implementation failures can be eliminated by the on chip Embedded Algorithms that internally monitor the successful programming of all bytes. The under erase failure can be eliminated by the on chip Embedded Algorithms that internally monitor the successful erasure of all bytes.

AMD created the Embedded Algorithms to simplify the program and erase algorithms. The Embedded Algorithms were created with the program and erase algorithm firmware built on the chip. Therefore, Embedded Algorithms simplify algorithm implementation so that only an initial command sequence is necessary to initiate program or erase. By using the Toggle Bit or $\overline{\text{Data}}$ Polling bit, the program or erase algorithm can be monitored for completion. With AMD's Embedded Algorithms, device level code generation is minimized, reducing overall system level code development and debug time. AMD's Embedded Algorithms offer the most reliable solution for all firmware implementation issues!

Over Erasure

The primary cause of over erasure is incorrect erase algorithm implementation. An over-erased bit causes the internal circuitry of the device to read a programmed bit as if it were erased.

How to Detect Over Erase

- Over erase results in failure to correctly read programmed bits in-system when V_{CC} is varied between 4.5 V and 5.5 V.
- Failure to verify during the program verify command occurs when the device is over erased.
- An extreme case of over erase will result in the inability to read the manufacturing ID.

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Common Errors that Result in Over Erase

Failure to Pre-Program the Device Before Erasure

Flash devices require that all bytes be pre-programmed before erase. There are two common software implementation errors associated with the pre-programming step in the erase algorithm:

- Ignoring implementation of the pre-program algorithm before erasing the entire array
- Pre-programming only a portion of the memory array (e.g., some users will only pre-program the address locations that will later be programmed with data)

In either of these cases, some bits in the array will be programmed while other bits will remain erased. It is critical that all bytes be pre-programmed before erase since all bits in the array will see the same number of erase pulses during the erase operation.

Recall, a Flash device programs a byte at a time. During the erase operation, the entire Flash array is erased in a bulk erase Flash device. Due to the nature of a bulk erase Flash device, all bytes in the array see the same number of erase pulses during an erase operation. Pre-programming of a Flash device is required before erase so that all bits in the array are in a tight distribution. By not pre-programming all bytes in the array, some bits may be in an erased state before erasing. These erased bits when exposed to additional erase pulses can be driven into an over erased state. An over erased bit causes the internal circuitry of the device to read some programmed bits as erased.

Therefore, it is important that all address locations be pre-programmed before erase. For more information on other common program implementation errors please refer to the "Incorrect Implementation of the Programming Algorithm" section of this document.

Failure to Implement Program Verify Correctly In the Pre-Program Algorithm

Flash devices require that the every byte in the memory array is program verified in the pre-program algorithm before erasing the device. There are two common software implementation errors associated with program verifying in the pre-program portion of the erase algorithm.

- Ignoring implementation of program verify in the pre-program algorithm.
- Program verifying only a portion of the memory array in the pre-program algorithm.

In either of these cases, some bits in the array will be programmed, while other bits will not be programmed. Since all bits in the array will see the same number of erase pulses during the erase operation, it is critical that all bytes in the memory array are program verified to assure complete programming of the memory array before erasure.

Recall, a Flash device programs a byte at a time. During the erase operation, the entire Flash array is erased in a bulk erase Flash device. Due to the nature of a bulk erase Flash device, all bytes in the array see the same number of erase pulses during the erase operation. Program verify of all bytes in the memory array with the program verify command is necessary to assure that the entire memory array is pre-programmed before erasure. Pre-programming of a Flash device is required before erase so that all bits in the array are in tight distribution. By not program verifying all bytes in the array, some bits may be in an erased state before erasing. These erased bits when exposed to additional erase pulses can be driven into an over erased state. An over erased bit causes the internal circuitry of the device to read some programmed bits as erased.

Therefore, it is important that all address locations are program verified using the program verify command during the pre-program portion of erase to assure complete pre-programming of the memory array before erasure. For more information on other common program implementation errors please refer to the "Incorrect Implementation of the Programming Algorithm" section of this document.

Issuing More Erase Pulses than Required

Some customers will issue a fixed number of erase pulses to the Flash device. In other words, the erase verify portion of the algorithm has been ignored until the memory array receives the fixed number of erase pulses. Therefore, the entire memory array may receive more erase pulses than required, causing the device to go into over erasure. Each byte must receive a sufficient number of erase pulses to ensure erasure without driving the byte into over erase. The only way to ensure this is to continue to erase verify the memory array after each erase pulse and discontinue erase pulsing the device once FFH data is verified in all address locations.

Exceeding the Erase Algorithm Time-Out

Stop timers were created as a protection against erase pulses greater than 10 ms and failure to issue the erase verify command. The stop timer is a safety feature that guards against one cause of over erasure. The current versions of the Am28F256 and Am28F512 do not have stoptimers. If an erase pulse is applied to either device for greater than the datasheet specified limit, the device will go into an over erase condition. For example, a Flash device receives a system interrupt during an erase pulse. The device will continue to erase and will be driven into an over erase condition. The new versions of the Am28F256 and Am28F512, which incorporate stoptimers, will be available in 2Q94.

Parallel Erasure

Over erase can occur during parallel erasure from incorrectly masking multiple devices once they have been completely erased. For example, there are two devices in a system that will be erased in parallel. Device 1 erases before device 2. Over erasure will occur on device 1 if it is not masked correctly. For a more in-depth understanding of this scenario, please reference *"Recommended Parallel Programming Routine For Flash Memory Devices,"* Appendix A.

Successive Erase (20h) Commands to the Device

The state machines on the current Am28F256, Am28F512, Am28F010, and Am28F020 devices do not require an erase-verify or Reset command to be executed before accepting the next erase command. An erase verify command is required following an erase command in the Flasherase algorithm, but the state machine in these devices does not require the erase verify command before accepting the next erase command. If a 20H pattern (Erase command) is written repeatedly to the Flash device, such as with the 80C196 micro-controller when powering up, the Flash will accept each erase command causing the device to go into an over erase condition. The state machine of these devices will be modified with improved protection on the 0.85 µm process shrink versions of these devices as follows:

Device	Production Availability
Am28F020	1Q94
Am28F010	2Q94
Am28F512	2Q94
Am28F256	2Q94

Incorrect Implementation of the Programming Algorithm

The second most common cause of failures is incorrect implementation of the programming algorithm.

How to Detect Programming Failures

A programming algorithm failure results in incorrect data or inability to program the device.

Common Errors that Result in Programming Failures

Bypass Program Verify

Every byte that has been programmed in a Flash device must be program verified on a byte by byte basis. It is incorrect to issue a fixed number of program pulses and to bypass program verify. Some customers issue a fixed number of program pulses and assume that the entire memory array has been programmed. In fact, some bits in the array will be programmed while other bits may still be erased. Therefore, program verify after each program pulse is required to guarantee complete byte programming on each byte that is programmed in the Flash device.

Program Verify Only A Portion of the Memory Array

By verifying only a portion of the memory array, the customer may believe he is reducing the programming time. By not program verifying each byte, some of the unverified bytes will not be programmed. These bytes that were thought to be programmed, but are in fact not programmed, will appear erased when read.

Verifying with the Read Command

The customer must implement the program verify command after programming each byte. When the byte is verified with the program verify command, the device must produce valid data when each bit is subjected to a internal gate voltage of greater than 6.5 V. Therefore, marginally programmed bytes will fail verification and will be given another program pulse.

If the byte is verified with the read command (00H or FFH), the voltage level of each bit would be compared to system V_{CC}, which may vary from 4.5 V to 5.5 V. Therefore, marginally programmed bytes may pass verification and fail in-system later when V_{CC} is greater than the V_{CC} voltage used during programming.

Programming Voltage Out of Spec

If the programming voltage is below the specified 11.4 V for Am28Fxxx devices, the device may require more than the number of program pulses specified in the algorithm. If the voltage is significantly lower than this value, the voltage may be too weak to generate the correct electric fields required for programming resulting in the inability to program.

Incorrectly Implementing Parallel Programming

Parallel programming issues generally occur when the devices are incorrectly masked. If a device, once it has been programmed, is masked incorrectly, the device may interpret the data as a command. Specifically, this will happen when the data to be programmed into a device is any program set-up command code such as 40H, 10H, or 50H. One common scenario occurs when the program data is 40H and the program and program verify commands are correctly masked with FFH. Since the program data was not masked, the device recognizes it as the program command. Thus, the device initiates program and tries to program FFH into the address location. The data is not altered because FFH can not be programmed into a device. The Flash device can only be programmed to a "0" data state and erased to a "1" data state. The system reads undefined/invalid data. If the system is reset the correct data at the address location will be read.

For a more detailed explanation of this scenario, please reference *"Recommended Parallel Programming Routine For Flash Memory Devices,"* Appendix A. Although not detailed in the Appendix, two similar scenarios exist. These scenarios are listed below:

- If the program command is masked with FFH and both the program data (i.e., 40H) and program verify command are not masked with FFH, the device will program the program verify command (data=C0H) into the address location.
- If the program command and program verify command is masked with 00H and the program data is not masked, the device will recognize 00H as data and program the address location with 00H.

Under Erasure

Another common Flash failure is under erase. Under erased bytes appear to be erased during the erase algorithm, but fail to read as erased in the read mode. Incorrect implementation of the erase algorithm generally results in under erase.

How to Detect Under Erase

In the read mode, bytes that were erased will appear programmed.

Common Failures that Result in Under Erase Failures

Failure to Issue the Erase Verify Command

The erase verify command is used after each erase pulse to check if the array has been completely erased. If a customer fails to erase verify or erase verifies only a portion of the memory array, under erased bits may go undetected. Therefore, in the read mode partially erased bytes will appear programmed. ***Every byte*** within the memory array must be erase verified. Please note the byte address to be verified must be supplied with the erase-verify command.

Verifying Erased Bytes with the Read Command

The customer must implement the erase verify command once the memory array has been given an erase pulse. When the byte is verified with the erase verify command, the device must produce valid data when each bit is subjected to an internal gate voltage of less than 3.5 V. Therefore, marginally erased bytes will fail verification and the memory array will be given another erase pulse. If the byte is verified with the read command, the voltage level of each bit would be compared to the system V_{CC}, which may vary from 4.5 V to 5.5 V. Therefore, marginally erased bytes will pass verification yet may fail to read as erased during system operation.

CCAR

This document has been created to offer immediate assistance in understanding flash failures. For flash failures that need further investigation, a CCAR should be filed. The CCAR, Customer Corrective Action Request, was designed to offer a method of device failure analysis for AMD customers. The AMD Field contact must complete a CCAR form and return it to the AMD corporate quality contact.

CONCLUSION

In conclusion, there are three failures addressed in this document: over erase failures, program algorithm implementation failures, and under erase failures. These failures combined constitute over 80% of all Flash failures that AMD has seen in the CCAR process. The balance of the Flash failures result from Electrical Over Stress on the V_{PP} pin.

All of the software implementation failures discussed within this document can be resolved by using AMD's Embedded Algorithms. AMD created the Embedded Algorithms to simplify implementation of the program and erase operations. The Embedded Algorithms were created with the program and erase algorithm firmware built on the chip. Therefore, Embedded Algorithms simplify the algorithm implementation so that only an initial command sequence is necessary to initiate program or erase. By using the Toggle Bit or $\overline{\text{Data}}$ Polling bit, the program or erase algorithm can be monitored for completion. With AMD's Embedded Algorithms, device level code generation is minimized, reducing overall system level code development and debug time.

Recommended Parallel Programming Routine For Flash Memory Devices

Recently, there has been some questions regarding a specific situation that may occur during parallel programming. Some customers have found difficulties understanding the data sheet specifications on how to mask off a parallel programmed device from one requiring more programming pulses. Specifically, the difficulty arises when the customer's data is equivalent to the program set-up code, 40H.

Description of Scenario

The following conditions must exists:

1. The customer's data is equivalent to the programming set-up code.
2. One device requires more programming pulses than the other to be programmed.

Below is an example of two devices in parallel where one device is considered the Upper Byte of the word and the other device is the Lower Byte of the word. Assume that the $\overline{WE}$ pins are tied together and $\overline{CE}$ pins are tied together to obtain the word configuration (see Figure 1).

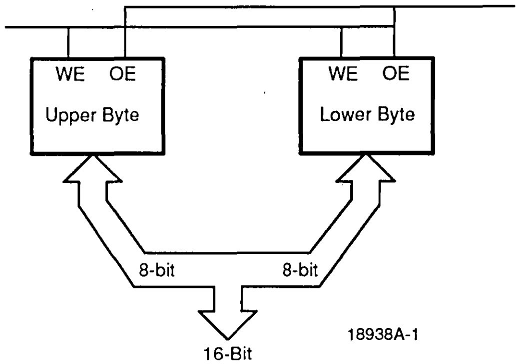


Figure 1. Parallel Programming Example

Table 1. Flash Parallel Programming Scenario

Programming Routine	Upper Byte	Lower Byte	Comments
1) Program Set-Up	40H	40H	
2) Program Data	40H	XXH	Customer data
3) Verify	COH	COH	
4) Verified Data	40H	YYH	Upper Byte has valid data. Lower Byte requires another programming pulse.
5) Program Set-Up	FFH	40H	Upper Byte intended to be masked by FFH; however, masking actually requires two bus cycles of FFH. Lower Byte receives program set-up command.
6) Program Data	40H	XXH	Customer believes that the Upper Byte device is masked and that the programming operation has been safely aborted. Actually, the Upper Byte receives a program set-up command.
7) Program Verify	FFH	COH	Upper Byte intended to be masked, but actually programs data of FFH.
8) Verified Data	??H	XXH	Upper Byte undefined because programming operation tried to program FFH data, to an erased data state, to the device. Lower Byte verified.

As shown in Table 1, the customer will experience difficulty reading the verified data from the Upper Byte device. Further confusing the situation in the above example, the customer would read correct data on both devices if the system was reset since FFH data did not alter the original programmed data on the Upper Byte device.

Solution

Reset into the read mode is a **two** bus cycle command, where FFH must be written for each cycle. To correctly mask the Upper Byte device, the customer should mask the program data in a second cycle at step 6 in Table 1. Effectively, this **resets** the Upper Byte device. Thus, the best means to protect against this situation is to mask the programmed byte with FFH in the parallel device programming subroutine. This is simply implemented as follows:

- **Initialize FD=PDW** in Figure 2, "Parallel Device Programming Flow Chart"
- **If FMD=VDAT then set FD=FFXXH** in Figure 3, "Parallel Device Programming Subroutine"

By using the subroutines, the user will not face the circumstance in step 8, Table 1. The superior solution for our customers is the Embedded Program and Embedded Erase Algorithms. With AMD's Embedded Algorithms, the customer need only give the proper command and data to multiple devices concurrently and the devices will program or erase independently, but in parallel.

Causes of Increased Programming Pulses

Although AMD specifies a maximum of 25 programming pulses to program a Flash device, one can typically program the devices within one programming pulse. Lot to lot process variance of die, charge trapping in the tunnel oxide towards the high end of the endurance life, and a below specification V_{PP} voltage are all factors that can cause devices to require additional programming pulses.

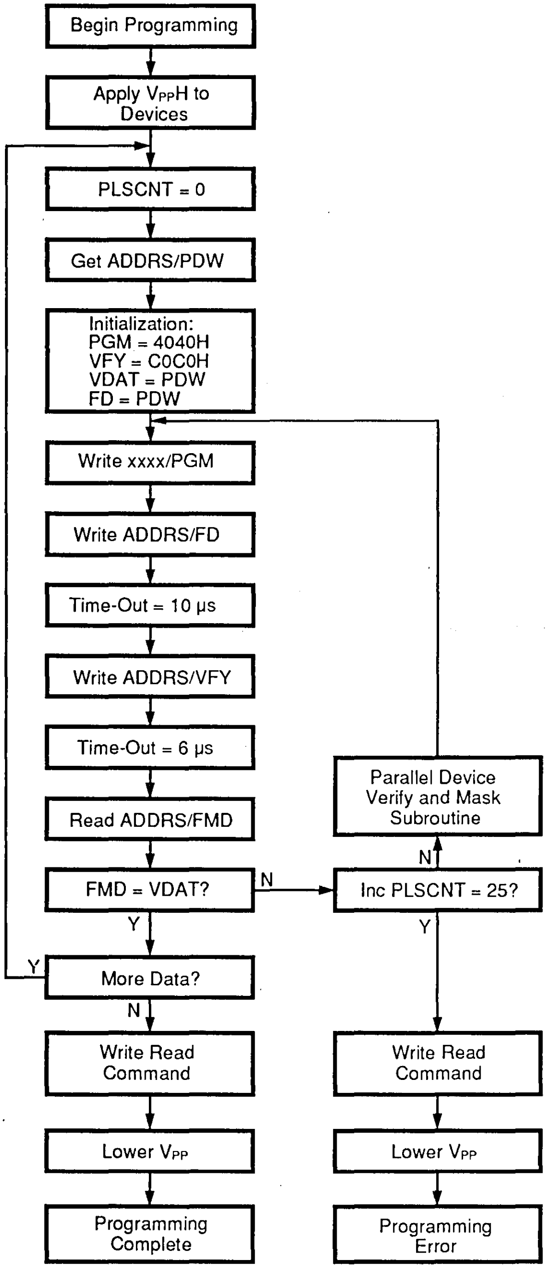
It is important to note that when the device reaches the higher end of its endurance capability, it becomes more susceptible to charge trapping in the tunnel oxide layer, increasing the number of programming and erasure pulses required to program or erase the device. Therefore, the better the device endurance capability the less likely the customer will experience the charge trapping mechanism. Thus, once again it is to the customer's advantage to use AMD's Embedded Algorithm devices with a 100K write cycles of endurance minimum.

Verification of the Correct Parallel Programming Routine

Many customers may wonder whether their parallel programming routine has been implemented correctly. A recommended method for verification is to set V_{PP} to a low voltage of 11.4 V. The customer will see an increase in programming pulses and must implement the software fix to the parallel programming routine. If the devices have been programmed correctly then no further software changes must be implemented.

Summary

Systems using Flash devices may encounter the parallel programming issue described on the previous pages when data being programmed is equivalent to the program set-up code, 40H, and there is an inconsistency in programming pulses required to program separate devices. It can be quickly remedied by a simple fix to the parallel programming subroutine or by using AMD's Embedded Algorithm devices.



Activity

Allow V_{PP} to stabilize.

PLSCNT = Pulse Counter.

ADDRS = Word Address to program.
PDW = Data Word to program.

Initialize Programming Variables:
PGM = Program command
VFY = Program-Verify command
VDAT = Valid Data
FD = Flash Data

xxxx = Address do not care.
Write Program Set-Up command.

Appropriate address and data for programming.

Duration of programming pulse.

Program-Verify command terminates the programming pulse.

Internal margin verify voltages are tapped from external 12 V V_{PP} for proper byte verfication.

Read from previously latched address. FMD = Flash Memory Data.

See Parallel Device Programming subroutine. Each device is independently verified. The Program command is masked by the Reset command (FFH) for all devices that are completely programmed. Please see note on next page.

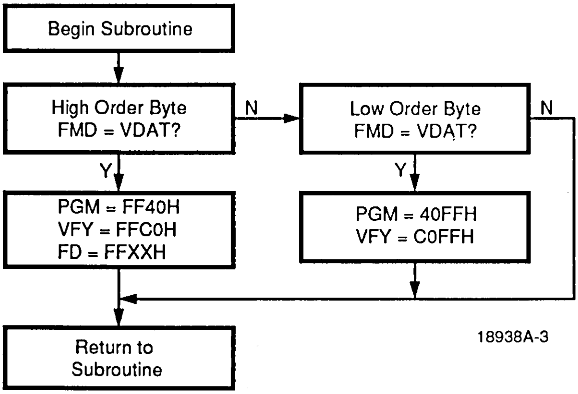
Compare Flash Memory Data to valid word data. If verified, reset PLSCNT and get next address and data word for programming. If invalid, increment pulse counter. If not last pulse, compare high order byte device and low order byte device for valid data.

Reset devices for read operation.

V_{PP}L deactivates command register. Device is in Read Only Mode.

18938A-2

Figure 2. Parallel Device Programming Flow Chart



This Subroutine verifies the high order and low order bytes independently. If either byte verifies, all commands are masked from that device.

The program command and program data are changed to a Reset command (FFH) and null data (FFH) respectively. Please see note below.

The Program-Verfiy command is changed to a Read command (00H).

Notes:

1. *During programming operations, FFH data is null condition. Only "0's" can be programmed into Flash memory cells.*
2. *If the high order byte verifies, then that byte is masked from further Program/Program-Verify operations. The low order byte (LB) commands are not changed.*
3. *If the a low order byte verifies, then that byte is masked from further Program/Program-Verify operations. The high order byte (HB) commands are not changed.*
4. *Although the Reset command (FFH) is recommended, the Read command (00H) will also mask any device from Program/ Program-Verify operations.*

Figure 3. Parallel Device Programming Subroutine

How to Design with Am29Fxxx Embedded Algorithm

Advanced Micro Devices

Application Note

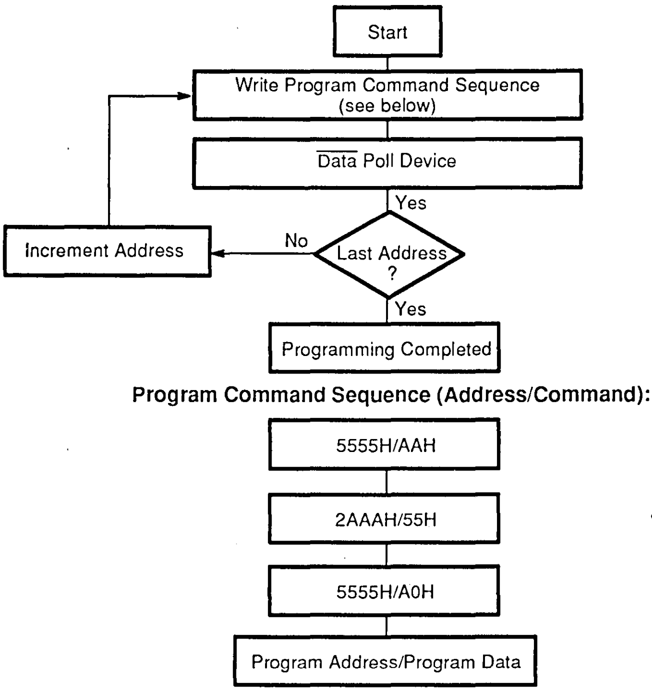
by Kumar Prabhat

This design note provides a general overview of the Embedded Algorithm and write operation status bits (DQ7–DQ3) that are incorporated in AMD's Flash memory devices and discusses any system level implementation issues associated with them. The Am29F010, a 5.0 Volt-only 1 Mbit Flash device is used as an example. It is highly recommended that this design note be used with the Am29F010 datasheet. Please note that the details on write operation status bits (DQ7–DQ5) provided in this design note may also be used with the Am28F010A and Am28F020A flash devices.

EMBEDDED PROGRAMMING OPERATION

Overview

The Am29F010 device is programmed on a byte per byte basis using a four bus cycle command sequence. Addresses are latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever happens later. Data is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever happens first. The rising edge of $\overline{WE}$ (or $\overline{CE}$) begins the programming operation. The Am29F010 device supports both $\overline{WE}$ or $\overline{CE}$ controlled write operations. Upon executing the Embedded Programming command sequence, the system is not required to provide further controls or timings. The device will automatically provide internally generated program pulses and verify the programmed cell margin. An Embedded Programming operation is completed when the data on DQ7 is equivalent to the data written, at which time the device returns to the read mode. The flowchart for Embedded Programming is shown below.



18929A-1

Figure 1. Embedded Programming Flowchart

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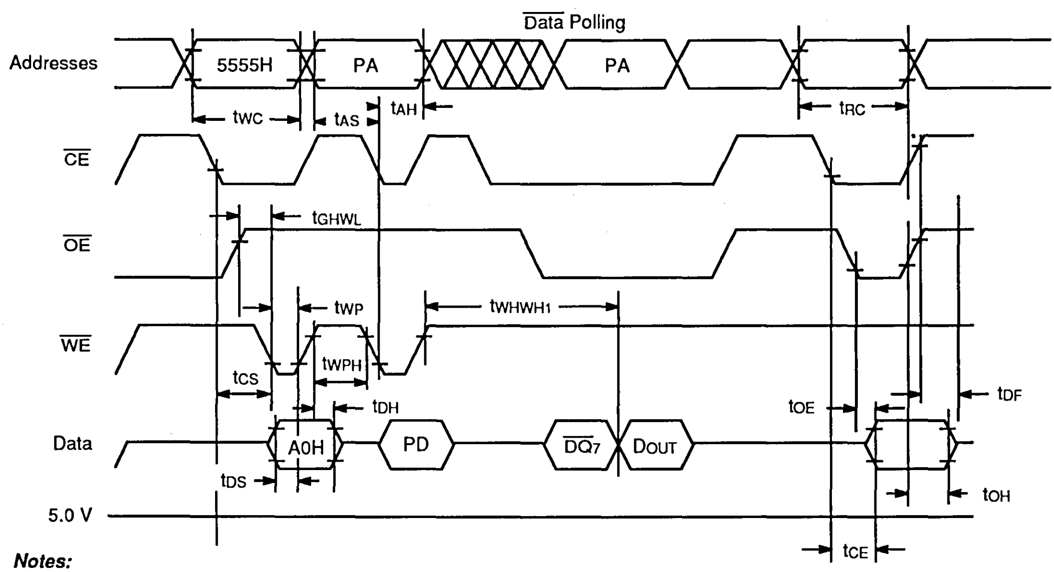
Implementation

Addresses are latched on the falling edge of $\overline{WE}$ during the Embedded Program command execution. Hence the system is not required to keep the address stable during the entire Programming operation. However, once the device completes the Embedded Programming operation, it returns to the read mode and address is no longer latched. Therefore, the device requires that valid address to the device be supplied by the system at this particular instant of time. Otherwise, the system will never read valid data on DQ7.

A system designer has two design alternatives to implement the Embedded Programming Algorithm:

- The system may initiate the $\overline{Data}$ Polling operation immediately after the the Embedded Programming command sequence is written.
- Once the system executes the Embedded Programming command sequence, the system microprocessor may take away the address from the device and thus is free to perform other tasks. In this case, the system microprocessor is required to keep track of the valid address which can be done by loading the address into a temporary register or any memory location. When the system microprocessor comes back to perform the $\overline{Data}$ Polling operation, it should reassert the same address.

However, since the Embedded Programming operation takes only 14–28 µs, it may be easier for the system microprocessor to start the $\overline{Data}$ Polling operation immediately after it has written an Embedded Programming Command instead of coming back and reasserting the valid address during the $\overline{Data}$ Polling operation. The option of either method is left to the system designer's choice. The following figure illustrates the timing diagram for the Embedded Programming operation.



Notes:

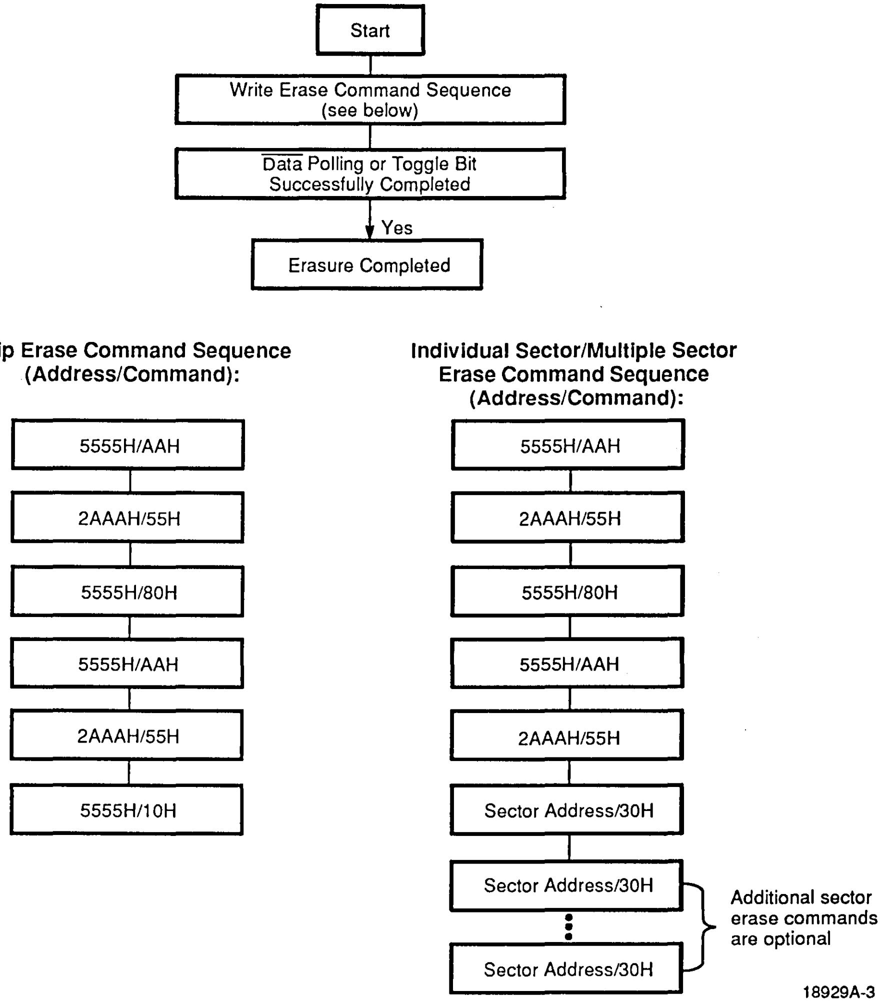
1. *PA is address of the memory location to be programmed.*
2. *PD is data to be programmed at byte address.*
3. *$\overline{DQ7}$ is the output of the complement of the data written to the device.*
4. *DOUT is the output of the data written to the device.*
5. *Figure indicates last two bus cycles of four bus cycle sequence.*

Figure 2. Embedded Programming Operation

EMBEDDED ERASE

Overview

When executing the Embedded Erase Algorithm command sequence the device automatically will preprogram and verify the entire memory array for an all 'zero' data pattern prior to electrical erase. The system is not required to provide any controls or timings during this operation. The automatic erase begins on the rising edge of the last $\overline{WE}$ pulse in the command sequence and terminates when the data on DQ7 is '1'. The flowchart for the Embedded Erase operation is shown below.



18929A-3

Figure 3. Embedded Erase Flowchart

Implementation

Similar to the Embedded Programming operation, once the device completes the Embedded Erase operation it returns to the read mode and addresses are no longer latched. Therefore, the device requires that a valid address input (sector address within any of the sectors being erased) to the device be supplied by the system at this particular instant of time. Otherwise, the system will never read a "1" on the DQ7 bit.

A system designer has two design alternatives to implement the Embedded Erase Algorithm:

- The system may initiate the $\overline{\text{Data}}$ Polling operation immediately after the Embedded Erase command sequence is written
- Once the system executes the Embedded Erase command sequence, the system microprocessor takes away the address from the device and thus is free to perform other tasks. In this case, the system microprocessor is required to keep track of one of the valid sector addresses (sectors being erased) and when it comes back for performing the $\overline{\text{Data}}$ Polling operation, it should reassert the same address.

Since the Embedded Erase operation takes a significant amount of time (typically 1 second), the second method would provide better system performance by freeing up the CPU for other system level tasks. The system can generate an interrupt on a regular interval to initiate the $\overline{\text{Data}}$ Polling operation to determine the status of the Embedded Erase operation. However, the choice of either option has been left to the system designer.

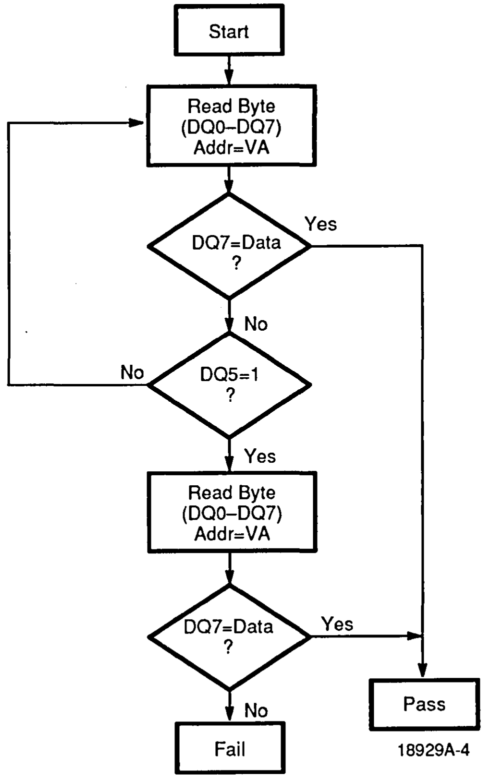
For the chip erase operation, if the device does not include any protected sectors, $\overline{\text{Data}}$ Polling may be performed at any address. When sectors are protected, $\overline{\text{Data}}$ Polling should be performed at any of the sector addresses which represent an unprotected sector.

WRITE OPERATION STATUS BITS

This section describes the operation of the Am29F010 write operation status bits (DQ3–DQ7). This section also describes the timing diagrams for the $\overline{\text{Data}}$ Polling (DQ7) and Toggle Bit (DQ6) operation.

DQ7–$\overline{\text{Data}}$ Polling

The Am29F010 device features the $\overline{\text{Data}}$ Polling operation as a method to indicate to the host system whether the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm, any attempt to read the device at address VA (Valid Address) will produce the compliment of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7. During the Embedded Erase Algorithm, an attempt to read the device will produce a "0" at the DQ7 output. Upon completion of the Embedded Erase Algorithm, an attempt to read the device will produce a "1" at the DQ7 output. The flowchart for the Data Polling operation (DQ7) is shown below.



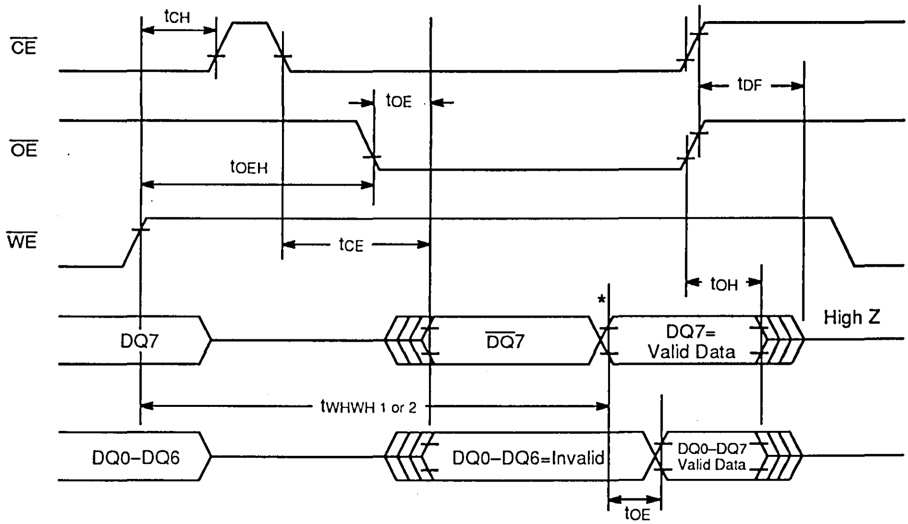
VA = Byte address for programming
= Any of the sector addresses within the sector being erased during sector erase operation
= XXXXH during chip erase

Note:

1. DQ7 is rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.

Figure 4. DQ7—$\overline{\text{Data}}$ Polling Flowchart

Once the Embedded Algorithm operation is close to being completed, the Am29F010 data pins (DQ0–DQ7) may change asynchronously while the output enable ($\overline{OE}$) is asserted low. This means that the device is driving status information on DQ7 at one instant of time and then changing to the byte's valid data at the next instant of time. Depending on when the system samples the DQ7 output, it may read the status or the valid data. Even if the device has completed the Embedded operation and DQ7 has a valid data, the data outputs on DQ0–DQ6 may still be invalid since the switching time for the individual data bits (DQ0–DQ7) may not be the same. This is due to the fact that the internal delay paths for the individual data bits (DQ0–DQ7) are different. The valid data will be provided only after a certain time delay (<t_{OE}). This has been explained in the timing diagram shown below.



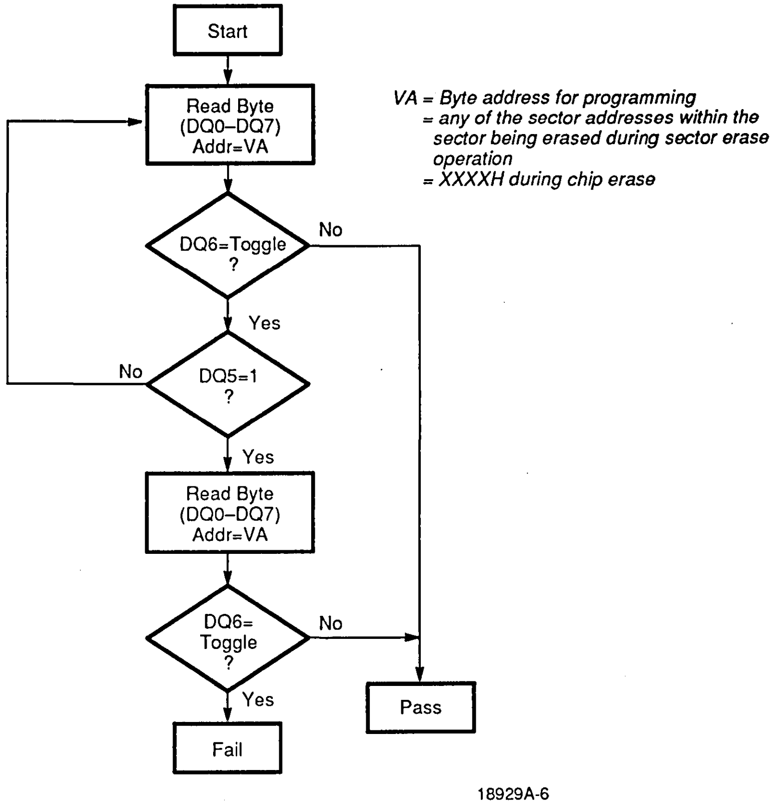
**DQ7=Valid Data (The device has completed the Embedded operation).*

18929A-5

Figure 5. DQ7—$\overline{\text{Data}}$ Polling Timing Diagram

DQ6—Toggle Bit

The device also features a "Toggle Bit" operation as another method that indicates the status of the Embedded Algorithm operations to the host system. During an Embedded Algorithm Program or Erase cycle, successive attempts to read (toggling $\overline{OE}$ or $\overline{CE}$) data from the device will result in DQ6 toggling between one and zero. Once the Embedded Algorithm Program or Erase cycle is completed, DQ6 will stop toggling and valid data on DQ0–DQ7 will be read on the next successive read attempt ($\overline{OE}$ going low). The flowchart for the Toggle Bit operation (DQ6) is shown below.

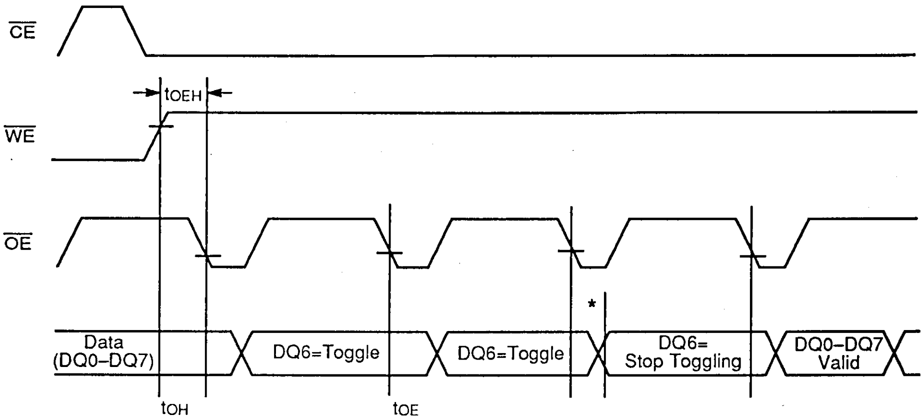


Note:

1. DQ6 is rechecked even if DQ5 = "1" because DQ6 may stop toggling at the same time as DQ5 changing to "1".

Figure 6. DQ6—Toggle Bit Flowchart

Please note that even if the device completes the Embedded Algorithm operation and DQ6 stops toggling, data bits DQ0–DQ7 may not be valid during the current bus cycle. This happens since the internal circuitry may be switching from a status mode to the read mode. Since this time delay is always less than tOE ($\overline{OE}$ access time), the next successive read attempt ($\overline{OE}$ going low) will provide the valid data on DQ0–DQ7. This has been explained in the timing diagram shown below.



Note:

**DQ6 stops toggling (The device has completed the Embedded operation).*

Figure 7. DQ6—Toggle Bit Timing Diagram

The Am29F010 provides the Data Polling (DQ7) and Toggle Bit (DQ6) operations as two alternatives to determine the write operation status. However, a system designer is free to perform the complete byte verification instead of implementing either of these two methods.

DQ5—EXCEEDED TIMING LIMITS

The Am29F010 will also be able to indicate through DQ5 if the program or erase time has exceeded the specified limits **(internal pulse count)**. Under these conditions DQ5 will produce a “1”. This is a failure condition which indicates that either the program or erase cycle was not successfully completed.

- If this failure condition occurs during sector erase operation, it specifies that a particular sector is bad and it may not be reused; however, other sectors are still functional and may be used for the program or erase operation. To use other sectors, reset the device by writing the Reset command sequence and then executing the program or erase command sequence. This allows the system to continue to use other active sectors in the device.
- If this failure condition occurs during the chip erase operation, it indicates one of the following:
  - The entire chip is bad and should not be reused
  - One or more sectors are bad. The system should be able to determine bad sectors by reading the DQ5 bit for individual sectors.
- If this failure condition occurs during the Byte Programming operation, it specifies that the entire sector containing that byte is bad and may not be reused.

The DQ5 failure condition may also appear if a user tries to program a non-blank location without first erasing it. In this case, the device locks out and never completes the Embedded Algorithm operation. Hence the system never reads a valid data on DQ7 bit and DQ6 never stops toggling. Once the device exceeds timing limits (internal pulse counts), the DQ5 bit will indicate a “1”. Please note that this is *not* a device failure condition since the device was incorrectly used. Under this illegal condition, the system is required to reset the device by writing the Reset command sequence before the device can be used again.

DQ3—SECTOR ERASE COMMAND TIME-OUT FLAG

Overview

Sector erase is a six bus cycle operation similar to that used by standard E2PROMs. There are two unlock write cycles followed by writing the "set-up" command. Two more unlock write cycles are then followed by writing the sector erase command. On this sixth bus cycle, the sector address is latched on the falling edge of $\overline{WE}$ while the sector erase command (30h) is latched on the rising edge of $\overline{WE}$. Multiple sectors may be erased by writing the above six bus cycle operations followed by subsequent writes of sector erase commands to all other addresses in the sectors that need to be erased concurrently. The following is an example:

7th Bus Cycle	8th Bus Cycle	9th Bus Cycle
SA1/30H	SA2/30H	SA3/30H

After the completion of the initial sector erase command sequence, the sector erase time-out of 100 µs will begin. Every time the system writes an additional sector erase command, the time-out window is reset. The device will indicate this time-out through the DQ3 bit. If the DQ3 bitis high, the internally controlled erase cycle has begun. Any attempts to write additional commands to the device will be ignored until the erase operation is completed as indicated by Data Polling or Toggle Bit. If DQ3 is low, the sector erase timer window is still open and the device will accept additional sector erase commands provided that these additional sector erase commands are written within the 100 µs time-out window.

Implementation

Once the first sector erase command sequence is written and the sector erase time out has begun, the system software should read the status of DQ3 (at any address) prior to writing any sector erase command to determine whether the 100 µs time-out window is still open. The system software should also read the status of DQ3 following each sector erase command to verify that the command has been accepted.

DQ2–DQ0

Reserved for the future use.

Design-In with AMD's Am29F010

Advanced Micro Devices

Application Note

by Kumar Prabhat

This application note describes the key features and system level benefits of using AMD's Am29F010, 5.0 V-only Sector Erase Flash Memory. It also explains how to use AMD's Am29F010 in an existing Intel Boot Block 28F010BX Flash based design and discusses the various hardware and software issues.

BENEFITS OF AMD'S Am29F010

- Since the Am29F010 is a 5.0 V-only device it eliminates the need for DC to DC converter circuitry to translate the system voltage level from 5.0 V to 12.0 V, for write and erase operations. This simplifies the hardware design, results in reduced board space, and lowers the system cost by approximately $4.00 to $5.00. Please refer to Appendix B for DC/DC converter circuitry required for 12 V flash device. 5.0 V-only programming also reduces the total system level power consumption. Below is a summary of the system level power calculations for the Am29F010 vs. 12.0 V Flash devices during reprogramming.

Device Level Reprogramming Power Consumption

Am29F010	12.0 V Flash Memory
Vcc Power = 5.0 V (Vcc) x 50 mA (Icc) = 250 mW	Vcc Power = 5.0 V (Vcc) x 30 mA (Icc) = 150 mW

DC/DC Converter Reprogramming Power Consumption

Am29F010	12.0 V Flash Memory
VPP Power not required	VPP Power = 12.0 V (VPP) x 30 mA (IPP) ÷ DC to DC converter efficiency = 450 – 720 mW

12.0 V Flash memories require more system level power since 5.0 V to 12.0 V conversion circuitry is not 100% efficient. The typical efficiency of the DC to DC converter is between 50% to 80%.

Total System Level Power Consumption (Reprogramming)

Flash Memory Type	Device Level	DC/DC Converter	Total System Level Power
Am29F010	250 mW	0	250 mW
12.0 V Flash	150 mW	450 – 720 mW	600 – 870 mW

- The Am29F010 provides a minimum of 100,000 write endurance cycles per sector. This kind of high endurance is especially important in the emerging markets of embedded Flash disks and removable memory cards. Typical endurance last well beyond the 100,000 cycle minimum.
- The 16 Kbyte sector erase architecture is another added advantage which is valued by many system designers. This feature provides the capability to selectively rewrite portions of the memory array while leaving the rest of the memory contents fixed. This architecture simplifies the design and debugging process by providing program modularity to the system. Individual sectors may also be hardware protected.
- The Am29F010 has an access time of as fast as 45 ns which will provide true 0 wait state performance in very high speed designs.
- The device incorporates AMD's Embedded Algorithm which reduces software overhead for the system designer. It also increases system level performance since the CPU will be free to do other tasks during reprogramming operations.
- The device also incorporates several features to prevent inadvertent write cycles.
  - During power-up and power-down, write cycles are locked out when Vcc is less than 3.2 V (typically 3.7 V). Under these conditions, the command register is disabled and all internal program/erase circuits are disabled.
  - The device ignores noise pulses or glitches of less than 5 ns (typically) on control signals $\overline{OE}$, $\overline{CE}$ and $\overline{WE}$ and will not initiate a write cycle.
  - During power-up of the device even with $\overline{WE}$ = $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IH}, the state machine will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode.

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DESIGN-IN WITH AMD'S Am29F010

Hardware Pin-Out Details

The Am29F010 is available in 32-pin DIP/PLCC/TSOP packages. The pin-out is compatible with JEDEC standard 1 Mbit E^2PROMs and also provides for easy upgrades to 4 Mbit densities. Below is the DIP pin-out for the AMD's Am29F010 and upcoming 4 Mbit 5.0 V-only, sector erase Flash memory device.

The only differences in pin-out are Pin 1 and Pin 30 which are NC in the Am29F010 pin-out and used as higher address lines A18 and A17 for the 4 Mbit Flash device. A system designer may design with a 1 Mbit part today and upgrade it with a 4 Mbit memory without any layout change in the board.

In fact, Am29F010 may be also used as an ideal upgrade to a 28F010 Flash-based design without any layout change. The only difference between Am29F010 and 28F010 pin-out is Pin 1 which is NC in Am29F010 and used as V_{PP} pin for 28F010.

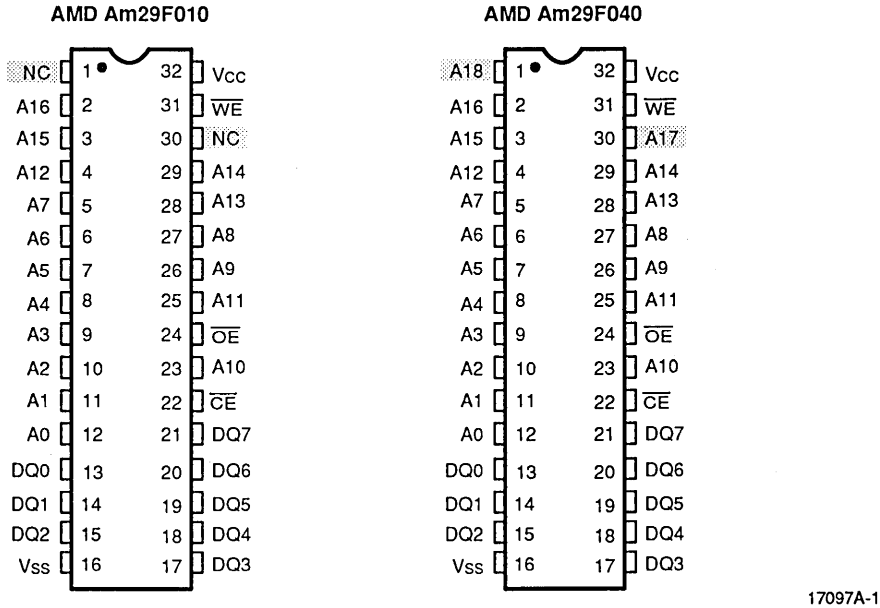


Figure 1

Replacing the 28F001BX with Am29F010

By changing the software only, AMD's Am29F010 may be used to upgrade a system using Intel's 12.0 V 28F001BX, 1 Mbit boot block flash device to 5.0 V only operation. Please refer to Figure 2 for a pin-out comparison between the Am29F010 and the 28F001BX.

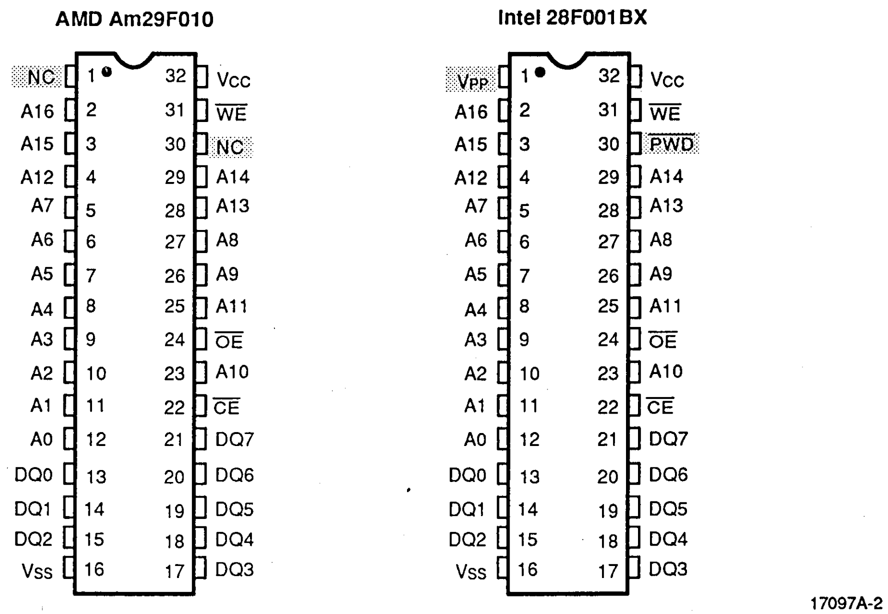


Figure 2

Hardware Pin Out Comparison

There are two differences in pin-out for AMD Am29F010 and Intel 28F001BX:

— The Am29F010 does not use V_{PP} (Pin 1) and it is not connected internally to the device.

— Intel's 28F001BX has added pin $\overline{PWD}$ (Pin 30) to support deep power-down mode. AMD's Am29F010 does not support the power-down function.

Since Pin 1 and Pin 30 are NC for AMD's Am29F010, it is 100% hardware compatible with the 28F001BX Flash device and may be used as a drop in replacement if the power down function is not required.

Software Command Structure

AMD's Am29F010 uses the JEDEC standard 1 Mbit E^2PROM 5.0 V-only multi-sequence command set. Please refer to Table 1 for Am29F010 command definitions.

Table 1.
Am29F010 Bus Command Structure

Command Sequence	Bus Write Cycles Required	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	4	5555H	AAH	2AAH	55H	5555H	F0H						
Read I.D.	4	5555H	AAH	2AAH	55H	5555H	90H						
Byte Program	4	5555H	AAH	2AAH	55H	5555H	A0H	Byte Addr	Data				
Chip Erase	6	5555H	AAH	2AAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Sector Erase	6	5555H	AAH	2AAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	Sector Addr	30H

These commands allow the user to program data on a byte by byte basis and erase any combination of sectors or even the entire device at once.

Common Device I.D. Command for AMD's Am29F010 and Intel's 28F001BX

Although the specific commands used to implement the program and erase algorithms are different between the Am29F010 and the 28F001BX, one command sequence may be used to determine whether the AMD or Intel device is in the system. The flow chart below shows how to determine the device I.D. and then jump to the appropriate algorithm.

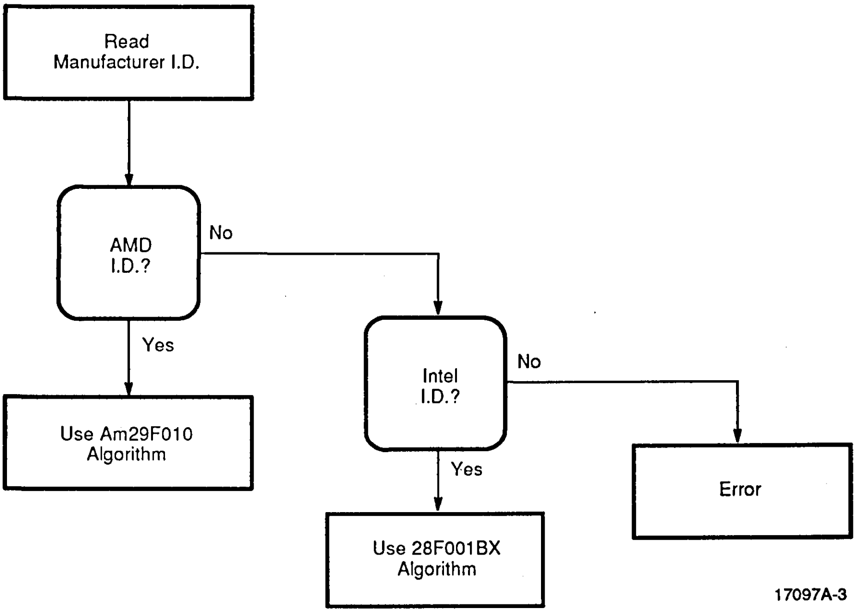


Figure 3

Table 2 details a common software sequence that allows the system to determine which device is on board and shows how to use the appropriate algorithm.

Note that the sectoring differences between the two devices must be considered in the software design to replace the 28F001BX with Am29F010. We have not discussed it in this application note since it is an application specific implementation.

Table 2

	1st Bus Cycle (Write Cycle)		2nd Bus Cycle (Write Cycle)		3rd Bus Cycle (Write Cycle)		4th Bus Cycle (Write Cycle)	
	Addr	Data	Addr	Data	Addr	Data	Addr	Data
	5555H	AAH	2AAAH	55H	5555H	90H	0000H	Mfg. I.D.
AMD	Unlock Cycle		Unlock Cycle		I.D. Command			0001H
Intel	Ignored		Ignored		I.D. Command			0089H

Embedded Algorithm – Write Operation Status

The Am29F010 features $\overline{\text{Data}}$ Polling and Toggle Bit methods as ways to indicate to the host system when the Embedded Algorithms are in progress or completed. The status is available from the device once the Embedded Algorithm has begun.

$\overline{\text{Data}}$ Polling: During the embedded operation, an attempt to read the device will produce complement data of the true data being written to DQ7. Once the embedded operation is completed, an attempt to read the device will produce the true data expected from the device. Upon the completion of an Embedded Algorithm operation the device returns to the read mode.

Toggle Bit: During and embedded operation, successive attempts to read data from the device will result in DQ6 toggling between one and zero. Once the embedded operation is completed, DQ6 will stop toggling and valid data will be read. Upon completion of an Embedded Algorithm operation the device returns to the read mode.

Sector Architecture

The AMD Am29F010 is a 1 Mbit Flash Memory device organized as 128K bytes of 8 bits each. It is divided into eight equal size sectors of 16K bytes each. Any combination of sectors can be individually or concurrently erased.

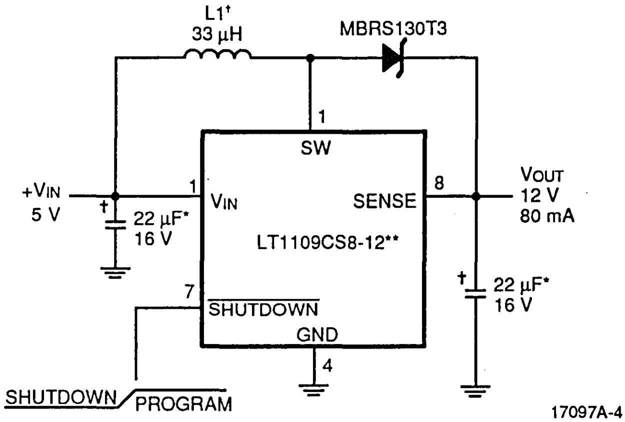
In addition, any combination of sectors or any individual sector may be write protected. Since the sector protect feature of the Am29F010 requires 12.0 V, it is typically done by using the external programming equipment at the user's site. Alternatively, AMD will program and protect the sectors as desired prior to shipment. In the protect mode, any individual sector may be selected. Protected sectors may also be unprotected if it is desired. Please refer to the data sheet for more details on sector protection and unprotection.

The fully-sectored architecture of the Am29F010 provides a system designer a much higher degree of design flexibility. It also simplifies the design and debugging process by permitting a system designer to erase a single sector only during code modification. This reduces the development cycle and results in shorter time to market.

Comparison Chart Am29F010 and 28F001BX

Features	AMD Am29F010	Intel 28F001BX
Density	128 Kbyte	128 Kbyte
Architecture	Fully Sectored	Block based
Sector/Block size	16 Kbyte	8, 4, 4 & 112 KByte
Automatic Algorithm	Yes	Yes
Power Supply	5.0 V only	5.0 V/12.0 V
Standby Mode	Yes	Yes
Deep Power Down Mode	No	Yes
Sector Protect	All Sectors	Only Boot Block
Sector Unprotect	Yes	Yes
Write Operation Status	$\overline{\text{Data}}$ Polling, Toggle Bit	Status Register
Chip Erase Time	1 second	10.10 seconds
Chip Program Time	3 seconds	2.39 seconds
Erase Suspend	No	Yes
Power Consumption (Programming)	250 mW	600 mW – 870 mW
Fastest Speed	45 ns	120 ns
Inadvertent Write Protect	No write for $V_{CC}<V_{LKO}$ 5 ns glitches ignored Read mode during Power up Four/Six bus cycle software command	No write for $V_{PP}<V_{LKO}$ Two bus cycle software command
Package	32-Pin DIP/PLCC/TSOP	32-Pin DIP/PLCC/LCC & TSOP
	Easy upgrade to 4Mbit	No upgrade path
JEDEC Pin Out	Yes	$\overline{\text{PWD}}$ Pin not defined
Endurance	100,000 cycles mininum per sector	10,000 cycles minimum

12.0 Volt Flash Memory V_{PP} Generation Circuitry



† L1 = SUMIDA CD54-330N (708-956-0666)

*Hilton CSTDD226M016TC (813-371-2600)

**Use LT1109A for 120 mA Output (Consult LTC Factory)

Figure 4

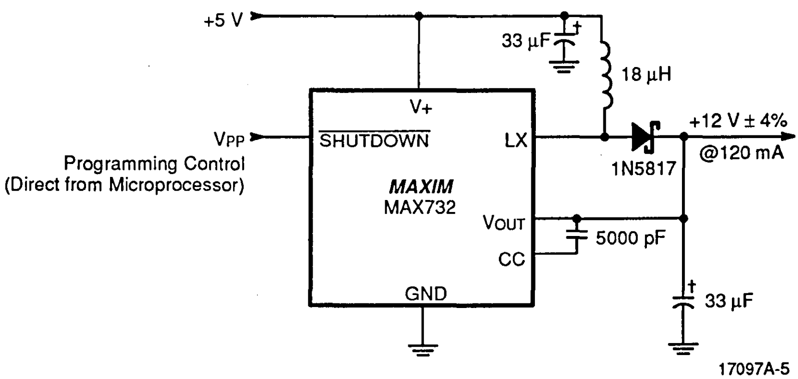


Figure 5

Reprogrammable Flash BIOS Design Using AMD's Am29F010

Advanced Micro Devices

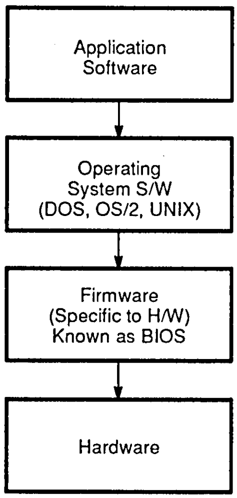
Application Note

by Kumar Prabhat

This application note describes the general overview and various system level issues for a reprogrammable Flash BIOS design. Any system designer, whether notebook or desktop system, will benefit from this discussion. This application note also describes the AMD Am29F010 5.0 V-only, sector erase part and why it is an ideal choice for a reprogrammable BIOS design.

INTRODUCTION TO BIOS

Every individual computer system consists of three basic blocks—Hardware, Hardware Specific Firmware commonly named BIOS and System Software.



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BIOS is a hardware dependent software normally stored in an EPROM, which provides an interface between specific hardware and system software. It interfaces with various hardware components like core logic chipset, graphics controller, the keyboard and disk drive. Any application software and operating system software (i.e., DOS, OS/2 and UNIX) runs above it and uses various BIOS procedures. IBM has defined various BIOS procedures to control specific peripheral functions. Some of them are mentioned as follows:

INT 13H	Disk Drive Control
INT 17H	Printer Control
INT 10H	VGA Control
INT 16H	Keyboard Control
INT 14H	Serial Communication Control

To use the BIOS procedure you load the parameters required by the procedure and then execute the INT# instruction that accesses that procedure. For example, you can use the BIOS INT 10H procedure for 15 different functions related to the CRT display. Some of these functions are: set display mode, set color palette, write dot and write character to screen. You specify the function you want by loading the number for that function in the AH register before executing the INT 10H instruction.

All of the 80X86 procedures boot up from the BIOS located at the very top of the 1 Mbyte memory map which is F0000H – FFFFFH. In addition 64K bytes of space lying in the address range E0000H – EFFFFH is provided for any BIOS extension.

The BIOS also contains various initialization routines to initialize system components like the serial port, DMA Controller and Interrupt Controller. During power-on it does the Power On Self Test (POST) routines. It also checks for basic system RAM functionality. If the system passes the RAM functionality, the BIOS will copy itself to the top 64K byte area of 1 Mbyte main memory. This is known as shadowing BIOS which improves the system performance since the BIOS code is run at DRAM speeds instead of slower ROM speeds.

WHY THE NEED FOR REPROGRAMMABLE BIOS

The concept of a personal computer is changing rapidly as technology progresses. Yesterday's high-end systems are becoming today's standard platforms and new technologies have brought enhanced system capabilities into the user's hands. The fastest growing segments of the computer market are in Notebooks and other portable PCs. Increasing demands for sophisticated hardware and intelligent power saving algorithms have increased the complexity of BIOS code. In the desktop computers area, the enhanced support of Ethernet/ SCSI Controller on the PC motherboard also increases the need for BIOS modifications to support sophisticated peripherals. On the high-end, EISA systems need to store hardware specific configurations which are traditionally stored in battery-backed-up SRAMs. Today's

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PC BIOS is no longer a standard product except for the basic 64K byte compatibility portion. The remaining 64K byte area has a significant potential to change with the addition of Power Management software and new setup utilities. To summarize, we see the potential change in BIOS code at every stage of manufacturing like design, debugging, testing and production. Code modifications with EPROMs do not provide a cost effective and timely solution since a UV Eraser and a separate EPROM programmer are required.

Flash Memories offer a superior solution for this kind of application. Code prototyping time is significantly reduced because Flash Memories can be updated with new code in a manner of seconds while still in the system. Board level diagnostics, final system test, and customer specific configuration code can all be down-loaded into the Flash memory electrically on the assembly line. Devices may be soldered directly to the system board. This reduces the cost associated with the BIOS socket and also eliminates the need to disassemble the system and replace socketed devices. Moreover, it will remove the prohibitive costs associated with a field service call. When updates to system code or system reconfiguration is necessary, these costly service calls may be replaced with remote updates or by distributing floppy disks with new data.

AMD FLASH MEMORY

This section provides a brief overview of AMD's 5.0 V-only Flash memory and in particular, AMD's Am29F010 5 V-only, Sector Erase part.

AMD's 5.0 Volt-only Flash Memory Technology

This section illustrates the fundamentals of AMD's Flash Memory Technology. AMD's Flash memory technology is very similar to that of our UV EPROM. The main difference is associated with the Fowler-Nordheim tunneling erase mechanism.

During program operations AMD's Flash memories transfer and store charge on a floating gate in a manner similar to EPROM. This provides data retention that is equivalent to that of EPROM devices. The device is programmed by raising the control gate and drain terminal to a high voltage. The source terminal is grounded. The voltage potential across the channel attracts channel electrons from the source area towards the drain. At the drain region, some of these channel electrons become "hot" electrons and are swept up through the thin oxide where they are trapped on the floating gate. The electrons stored on the floating gate create an electric field which turns off the memory transistor and represents a logic zero.

AMD's 5.0 V-only, Flash memory uses Negative Gate Erase Technology for erase operations in order to minimize the current drawn from the erase change pump. AMD's Negative Gate Erase technique actually provides the same electric fields to the Flash memory cell and uses the same erase mechanism as its 12.0 V Flash devices. A negative voltage of –10.5 V is applied to the control gate while the source terminal is at 5.0 V supplied by the system Vcc supply. Negative Gate Erase is used in order to reduce the current drawn from the erase charge pump. The band-to-band tunneling current (10–20 mA peak) comes directly from the system Vcc supply through the Array around terminal. This is the most efficient way to use an existing system Vcc supply. The current required from the Negative Gate Erase charge pump is less than 10 µA at –10.5 V. This significantly reduces the internal power consumption in relation to conventional 12.0 V approaches.

The Am29F010

This section describes the various features of the Am29F010.

General Description

The Am29F010 is a 1 Mbit 5.0 V-only "Flash" electrically erasable, electrically programmable read only memory organized as 128K x 8 bits. It is a 32-pin device which allows upgrades to 4 Mbit densities. The device has uniform sector architecture with 100,000 minimum endurance cycles per sector.

The Am29F010 is entirely pin and software compatible with the 5.0 V-only JEDEC standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine which controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. With the appropriate command sequence written to the register, standard microprocessor read timings output array data, access the auto-select codes or output data for erase and program verification. Reading data out of the device is similar to reading from 12 V Flash or EPROM devices.

Embedded Algorithms

The Am29F010 is programmed and erased using Embedded Algorithms, which completely automates the program and erase operation. The Am29F010 is programmed by executing the Program Command sequence. The Embedded Programming™ Algorithm automatically times the programming pulse width and verifies the proper cell margin. Chip erase is done by executing the erase command sequence. The Embedded Erase™ Algorithm automatically verifies if the entire array is programmed and if it is not, the algorithm will automatically pre-program it before beginning electrical erase.

The Am29F010 features $\overline{\text{Data}}$ Polling and Toggle Bit functions as a method to indicate to the host system when the Embedded Algorithms are in progress or completed. During the Embedded Program Algorithm an attempt to read the device will produce compliment data of the data last written to DQ7. Upon completion of the Embedded Program Algorithm, an attempt to read the device will produce the true data last written to DQ7. During the Embedded Erase Algorithm, DQ7 will be "0" until the erase operation is completed. Upon completion of Embedded Erase Algorithm data at DQ7 will be "1". The device also features a "Toggle Bit" as another method to indicate to the host system when the Embedded Algorithms are in progress or completed. During an Embedded Program or Erase Operation, successive attempts to read data from the device will result in DQ6 toggling between one and zero. Once the Embedded Program or Erase Operation is completed, DQ6 will stop toggling and valid data will be read. Upon completion of the Embedded Algorithm the device returns to the read mode. The Am29F010 will also indicate through DQ5, if the program or erase time has exceeded the specified limits. Under these conditions DQ5 will produce "1" which will indicate that the program or erase cycle was not successfully completed. Then DQ4 will indicate which algorithm exceeded the limits. A "0" in DQ4 indicates a programming failure, a "1" indicates an erase failure.

The automatic nature of the Embedded Algorithms provide various benefits over standard algorithms. Embedded Algorithms increase the system level performance significantly by reducing the CPU's overhead associated with the repetitive nature of standard algorithmic commands. This frees up the CPU to execute other system level tasks.

Sector Based Architecture

The Am29F010 also features a sector erase architecture. The whole memory content of the device is divided into eight sectors of equal size. The sector architecture allows for 16K byte segments of memory to be erased and reprogrammed without affecting other sectors. The device also supports hardware sector protection. This feature will disable both program and erase operations in any number of sectors (0 through 7). Please refer to the data sheet for more details on sector protection.

Sector erase requires a six bus cycle command similar to standard E^2PROMs. There are two unlock write cycles followed by writing the "set-up" command. Two more unlock write cycles are then followed by the sector erase command. On this sixth bus cycle, sector address defined by higher address lines A16, A15 and A14 is latched on the falling edge of $\overline{WE}$, while the sector erase command (30h) is latched on the rising edge of $\overline{WE}$. Multiple sectors may be erased concurrently by writing the six bus cycle command as described above followed by a sector erase command with other sector addresses. A time-out of 100 µs from the rising edge of the $\overline{WE}$ pulse of the last sector erase command will initiate the sector erase operation. If another sector erase command is written within the 100 µs time-out window the timer is reset. Any command other than sector erase within the time-out window will reset the device to the read mode, ignoring the previous command string. The device will indicate this time-out through the DQ3 pin. If DQ3 is high the internally controlled erase cycle has begun, and attempts to write additional commands to the device will be ignored until the erase operation is completed as indicated by the $\overline{\text{Data}}$ Polling or Toggle Bit. If DQ3 is low, the sector erase timer window is still open and the device will accept additional sector erase commands. The system software should check the status of DQ3 prior to and following each sector erase command.

Am29F010—An Ideal Choice

- The Am29F010 has an access time of as fast as 45 ns which will provide true 0 wait state performance in very high speed designs without downloading the code to the Shadow RAM.
- The device incorporates Embedded Algorithms which reduces software overhead for system designer and it also increases system performance since CPU will be free to do other tasks during reprogramming operations.
- The device provides a minimum of 100,000 write endurance cycles per sector. This kind of high endurance is especially important in the emerging markets of embedded flash disks and removable cards.
- Since the Am29F010 is a 5.0 V-only device, it eliminates the need for DC to DC converter circuitry to translate the system level voltage level from 5.0 V to 12.0 V for write and erase operations. This also simplifies the hardware design, results in reduced board space and reduces the system cost by approximately $2.00 to $4.00.
- As the power consumption is proportional to the square of operation voltage, 5.0 V operation reduces the power consumption significantly during programming and erase operation.
- Sector erase architecture is another added advantage which is valued by many system designers. The Am29F010 provides a system designer eight sectors to use in their designs in order to add more functions to the system. It also eases the design and debugging process by allowing a system designer to erase a single sector during code modification. This brings the program modularity to the system.
- The device also incorporates several features to prevent inadvertent writing of the part.
  - During the power-up and power-down, a write cycle is locked out for Vcc less than 3.2 V (typically 3.7 V). Under these conditions, the

command register is disabled and all internal program/erase circuits are disabled.

— The device ignores the noise pulses or glitches of less than 5 ns (typical) on $\overline{OE}$, $\overline{CE}$ or $\overline{WE}$ and will not initiate a write cycle.

— During power-up of the device even with $\overline{WE}$ = $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IH}, the device will not accept commands on the rising edge of $\overline{WE}$. The internal state machine is automatically reset to the read mode.

Packaging Details

AMD's Am29F010 is being offered in three standard 32-pin packages: Plastic Dual In-Line Package (PDIP), Plastic Leaded Chip Carrier (PLCC), Leadless Chip Carrier (LCC) and Thin Small Outline Package (TSOP). See Figures 1 and 2 for pin-out details.

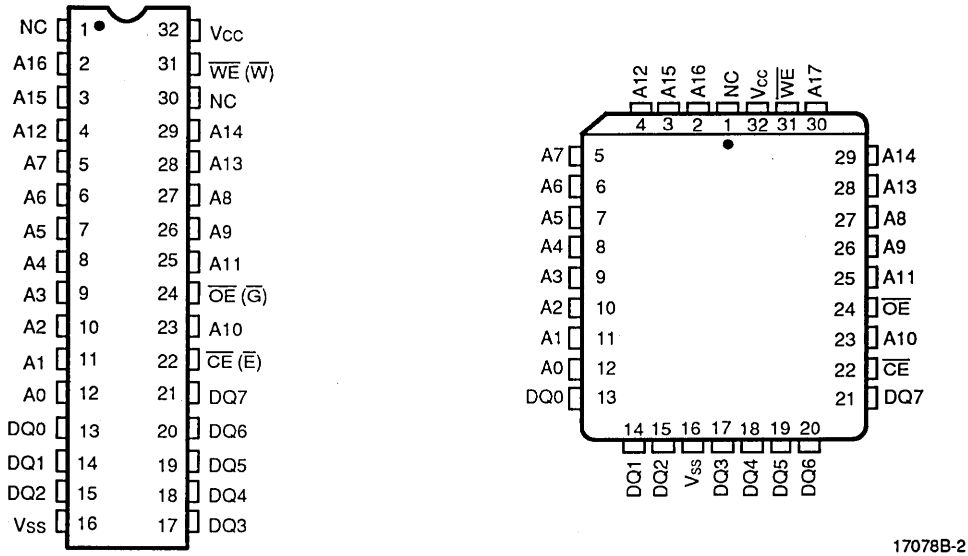
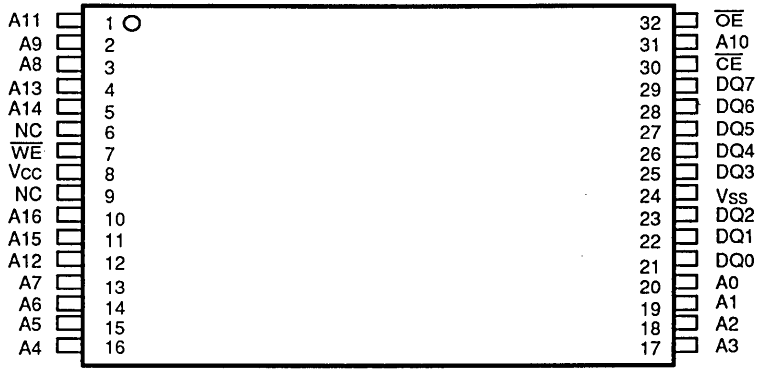
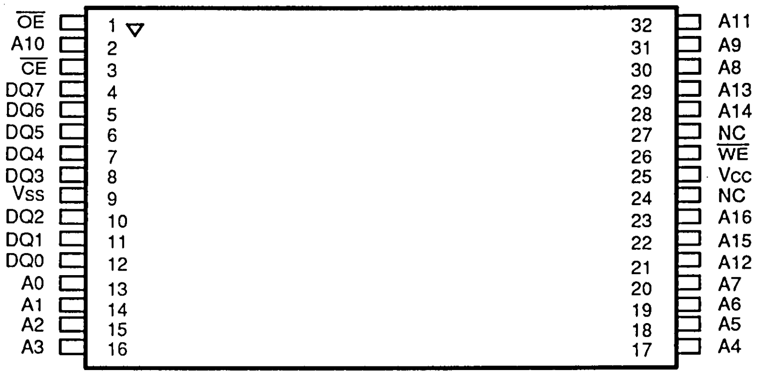


Figure 1. Am29F010 DIP, PLCC and LCC Pin-Out



29F010 Standard Pinout



29F010 Reverse Pinout

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Figure 2. Am29F010 TSOP Pin-Out

Thin Small Outline Package

The TSOP is the industry's leading edge plastic, surface mountable memory package. System requirements for higher density and smaller, high density memory arrays are driving this packaging trend. It is becoming the standard choice for hand-held equipment and palmtop/ laptop computers as well as memory cards. This package comes in standard and reverse 32-pin options and is available in the 8 mm x 20 mm x 1.27 mm package outline. In addition to the TSOP's low height profile, maximum board space is achieved with the dual-in-line and standard/reverse pinouts. Board layers can be reduced because traces are routed under the two sides of the package that do not have leads. This allows packages to be mounted side-by-side and end-to-end. All pins except chip enable pins can be connected in parallel. This is accomplished by using standard and reverse pin-out packages in an alternating sequence as shown in Figure 3.

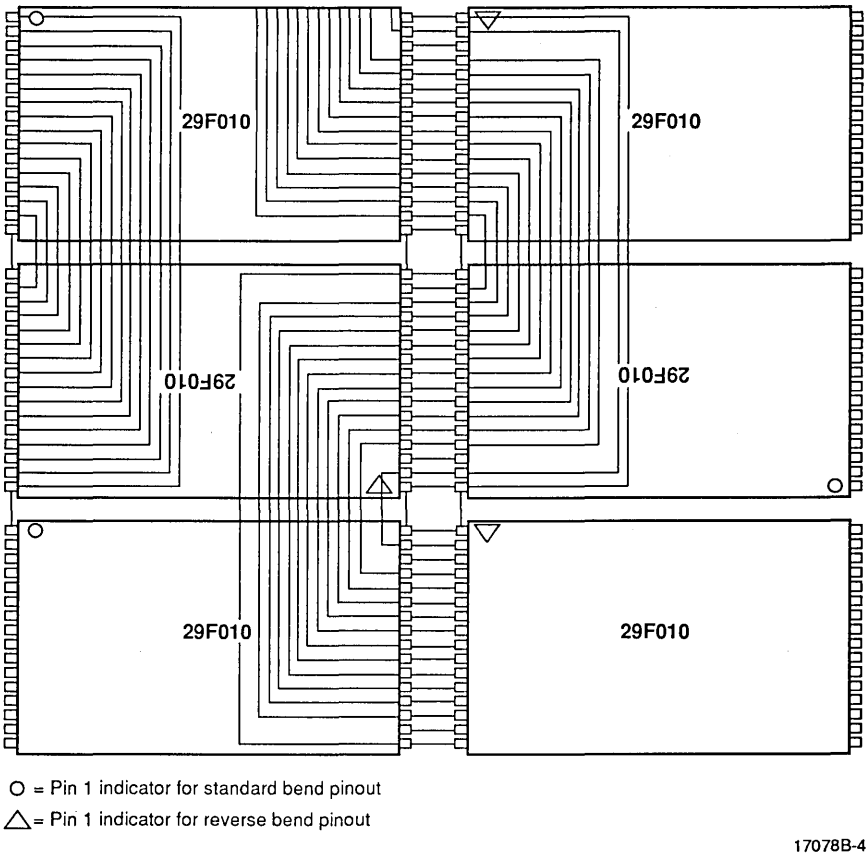


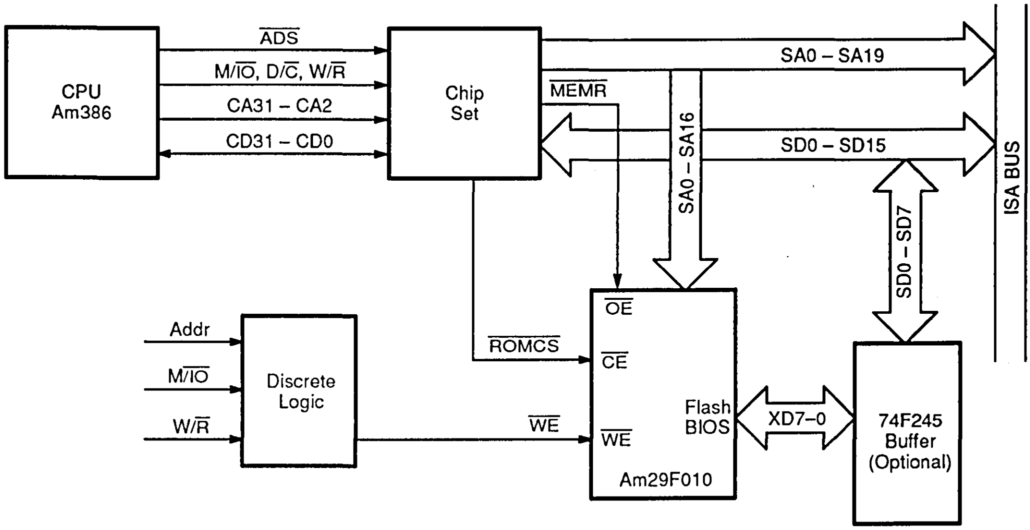
Figure 3. Optimum Board Layout with TSOP

SYSTEM LEVEL DESIGN ISSUES

This section describes various system level design considerations for the support of reprogrammable BIOS.

Hardware Design Consideration

This section describes the modifications required in the standard PC-AT motherboard to support the Flash BIOS. Below is the block level diagram of a PC-AT motherboard supporting reprogrammable Flash BIOS.



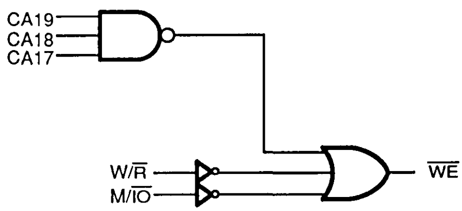
17078B-5

Figure 4. PC-AT Motherboard with Flash BIOS

Looking at the above block diagram we come across two main considerations for supporting the Flash based reprogrammable BIOS:

- All write accesses to EPROM address space are directed to the ISA bus and effectively discarded. Since standard PC chip sets do not generate $\overline{\text{MEMWR}}$ with $\overline{\text{ROMCS}}$. $\overline{\text{WE}}$ for Flash EPROM must be generated externally.
- Standard PC motherboards do not support writes to the BIOS EPROM. If the chip set data buffer works only in one direction, a data buffer is required that works in both read and write directions in order to support Flash BIOS.

$\overline{\text{WE}}$ generation for Flash EPROM can be generated by using simple discrete circuitry to decode the BIOS addresses range (E0000H – FFFFFH), M/$\overline{\text{IO}}$, and W/$\overline{\text{R}}$. Figure 5 shows the generation of $\overline{\text{WE}}$ signal.



17078B-6

Figure 5. $\overline{\text{WE}}$ Generation Circuit

Considerations for In-System Programming

In traditional PC motherboard design, the EPROM containing BIOS, is normally socketed and disassembled from the board. Flash EPROMs eliminate the need to disassemble the system and replace the socketed device in order to update System BIOS. Flash devices may be soldered directly to a printed circuit board since they support in-system programming.

Before soldering the Flash memory on the board, the manufacturer may initially program the boot code and any other codes which have to be protected. Boot codes may be protected using external programming equipment or by AMD. To activate these modes, the programming equipment must force 12 V on the device. The particular sector will be selected using high order address lines A14, A15 and A16. Once the device is soldered into the board, the rest of the programming is done by using the local CPU. The Boot code is not meant to be changed once it is protected. However, its content may be altered by using the Sector Unprotect feature of the device and then reprogram the device with a new code. Please refer to the data sheet for more details on sector protect and unprotect.

Software Design Consideration

Let us take the BIOS design example using the AMD's Flash device Am29F010 as shown in Figure 6. BIOS Code has been divided into various modules like Boot Code, System BIOS, VGA BIOS, Power Management Code etc., and each sector may be used for individual modules.

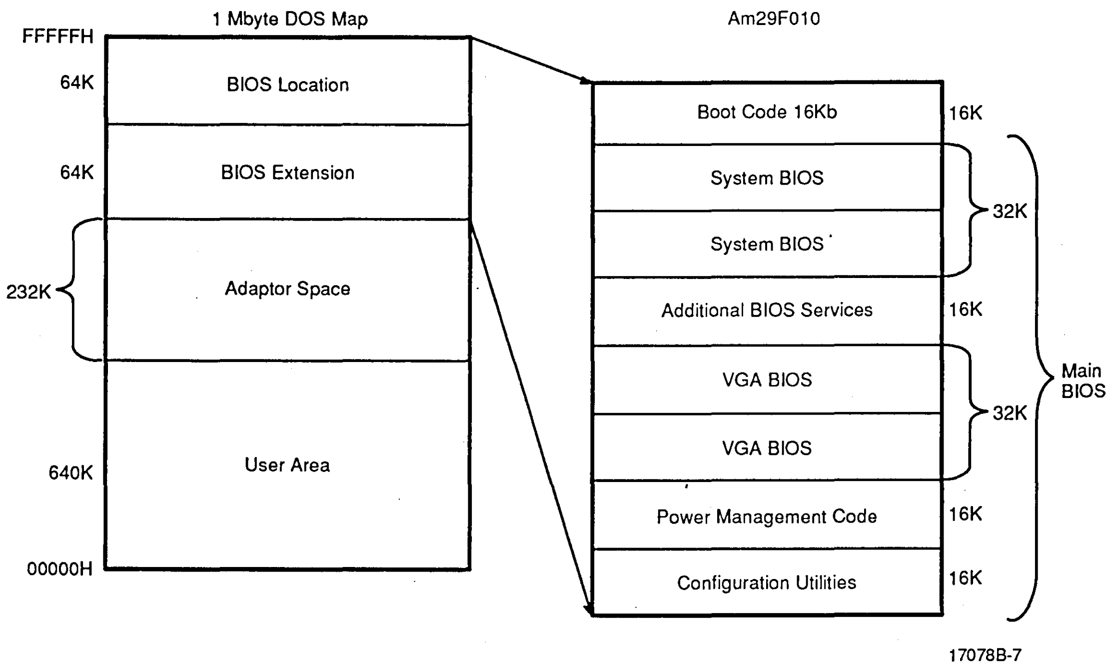


Figure 6. BIOS Design with Am29F010

Please note that the only difference between the standard BIOS and Flash BIOS is the addition of Boot Code located in a separate sector. The Boot Code resides in the system address FC000h – FFFFFh and contains the minimum code needed to boot up the system so that other blocks can be reprogrammed if required. Boot Code consists of:

- 16-byte jump vector
- BIOS check sum routine
- Recovery code

The Recovery Code contains various initialization routines and basic minimum routines for system start-up.

- — System timer
- — DMA/Interrupt function
- — Keyboard
- — Floppy drives

- During power on Boot Code takes control of the system
  - — It uses the BIOS checksum routine to check for valid main BIOS.
- If the main BIOS is valid, system RAM is checked and the main BIOS code is copied into the system DRAM memory and continue the boot operation. This feature is known as shadow memory and is used by most PC designs.
- If BIOS checksum determines an invalid BIOS, the system gives control to the recovery code for boot operation. The recovery code initializes the system RAM and floppy drive. Using basic minimum routines, it boots up the system from floppy drive and displays the message to insert the BIOS update diskette.
- The BIOS update diskette will contain:
  - — Reprogramming utility
  - — BIOS code
- The reprogramming utility is loaded into system RAM and used to reprogram the main BIOS from the diskette.

The above procedure may be also used to modify the main BIOS code.

Generation and Control of V_{PP} Programming Voltage for Flash Memories

Application Note

Advanced Micro Devices

INTRODUCTION

Constant V_{PP} voltage of 12.0 V ± 0.6 V is required for erase and programming operations. Parallel device reprogramming (either 16-bit or 32-bit data words) requires 30 mA of current for each device in the Flash memory array.

V_{PP} voltage may be generated in a number of ways. Each of these options will be discussed during the text.

1. Hardwire V_{PP} Voltage to the Flash Device.
2. Umbilical Cord Type Programming.
3. Use DC/DC Convertor to pump 5 V to V_{PP} Voltage.
4. Pump 5 V to V_{PP} Voltage with Analog Circuitry.

It is important to maintain the specified V_{PP} voltages when programming the Flash memory device. All internal device voltages are generated from the V_{PP} reference. Inappropriate V_{PP} voltage may impair device performance. Internal voltages do not exceed that of external V_{PP}.

Unlike other approaches to Flash memories, AMD's devices actually verify margin for each byte during erase and programming operations. This is accomplished during the Erase-verify and Program-verify operations respectively. During these operations, the appropriate margin-verify voltages are internally tapped off of the V_{PP} voltage via the command register and internal V_{PP} circuitry. This allows for Erase/Erase-verify and Program/Program-verify operations to be performed with static V_{CC} (5 V) and V_{PP} (12 V) voltages.

Before proceeding, a few comments regarding basic design philosophy should be mentioned. Please make note of these comments for any of the V_{PP} generation methods implemented.

V_{PP} Trace and Circuitry

Be aware that AC current is a component of DC power switching characteristics. Design the printed circuit board traces handling this current to accommodate high frequency.

Printed Circuit Board Trace Layout

Use a single ground plane to eliminate potential loops. Keep all inductive impedances at a minimum on all high current traces.

V_{PP} Regulator Circuitry Layout

Locate the V_{PP} generation circuitry as close to the Flash memory array as possible. In addition, minimize lead lengths of the network. To help prevent noise from being picked up in feedback loops, locate all resistors and capacitors as close to the V_{PP} network as possible. In order to prevent input ground loops, use separate returns for input and output capacitors.

Device Decoupling

Switching $\overline{CE}$ inputs for memory selection causes transient current peaks at the Flash device. The Flash memory devices should be decoupled with the appropriate capacitance from these transients.

- Connect 0.1µF ceramic capacitor between V_{CC} and V_{SS} and one between V_{PP} and V_{SS}. The capacitors should be placed as close to each device as possible.
- In addition, connect 4.7µF electrolytic capacitor between V_{CC} and V_{SS} on the memory array's power supply. Do this for each set of eight memory devices. this bulk capacitor will maintain even voltage to the memory array.

1. HARDWIRE V_{PP} VOLTAGE TO THE FLASH DEVICE

Typically this approach is used in the most cost sensitive applications. Regulated 12.0 V supplies are commonly available in many systems.

When V_{CC} = 0 V, the V_{PP} voltage is internally disabled from the device. Memory contents cannot be altered. The Flash device automatically resets to the read mode when V_{CC} rises above 2 V. This occurs even when V_{PP} = 12 V.

Power supply sequencing is not required.

The device will only respond to the correct sequence of commands in order to change the state of the Flash memory from Read mode to any other mode. In addition, the three control pins must be in their correct state ($\overline{CE}$ = Low, $\overline{OE}$ = High and $\overline{WE}$ = Low) in order to accept a command from the data bus.

A number of additional procedures are available to further prevent inadvertent writes should system glitches occur during system/device power transitions.

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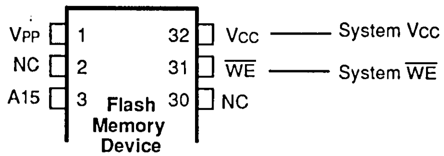
Issue Date: March 1991

- Hold any control pin ($\overline{CE}$, $\overline{OE}$, or $\overline{WE}$) in a non-write condition. This disables the device from executing any write operation (see example on the next page).
- Any "illegal" command (an illegal command is one that is not defined in the AMD Flash data sheet under the section – Command Definitions) written to the Flash device will automatically terminate any operation and reset the device to the Read Mode.

Example:

Holding $\overline{WE}$ in a non-write condition during power transitions.



In systems where the V_{PP} pin is to be connected directly to the +12 V supply, $\overline{WE}$ should be held in a non-write state during power supply transitions. This will prevent against inadvertent write conditions.

During power supply transitions, V_{PP} voltage is internally disabled from the Flash device until V_{CC} rises above 2 V. In addition, the Flash device automatically resets to the read mode as V_{CC} rises above 2 V. When write enable is at V_{IH} the command register is internally disabled from the internal state machine of the Flash device. When the command register is disabled, data commands can not be transferred to the state machine. Therefore the state of the Flash device will not be altered from the read mode. Access to the command register will be prevented until the $\overline{WE}$ line is driven to a logic level low by the system write control.

Note: V_{IH} Min = 2.0 V.

2. UMBILICAL CORD PROGRAMMING

Many applications perform system updates using the umbilical cord or edge connector programming method. The external programming equipment supplies the 12.0 V ± 0.6 V V_{PP} voltage. When the umbilical cord is disconnected, be aware that electrostatic discharge may build up on the floating V_{PP} pin. To prevent against this problem, tie the V_{PP} pin to ground via a large (10KΩ) pull-up resistor and a capacitor (see Figure 1).

3. V_{CC} (5.0 V) to V_{PP} (12.0 V) DC/DC CONVERTER

A monolithic DC/DC convertor from Valor Electronics, the PM9006, is appropriate for the digital world to supply the 12.0 V +0.6 V V_{PP} voltage. The V_{PP} voltage is generated on chip using the standard system V_{CC} (5.0 V) voltage. Standard TTL commands are used to disable the 12.0 V output supply when programming or erasing operations are not intended. The enable ($\overline{E}$) function provides absolute write protection to guarantee against inadvertent program or erasure. Flash memory contentscannot be altered without the active 12.0 V V_{PP} supply. The enable pin also saves system power when DC/DC convertor is not required. The PM9006 has a minimum efficiency of 50% at full load. The PM9006 comes in a 24-pin package.

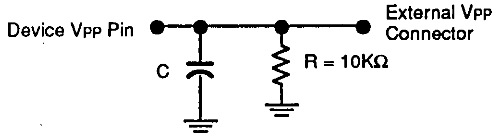


Figure 1.

The Valor PM9006 provides a controlled 12.0 V output that is regulated within the +5% (+0.6 V) V_{PP} specification. The standard system V_{CC} (5.0 V) supply is converted to the V_{PP} (12.0 V) supply by the DC/DC convertor. The voltage transitions are smooth and protect against destructive positive or negative overshoot.

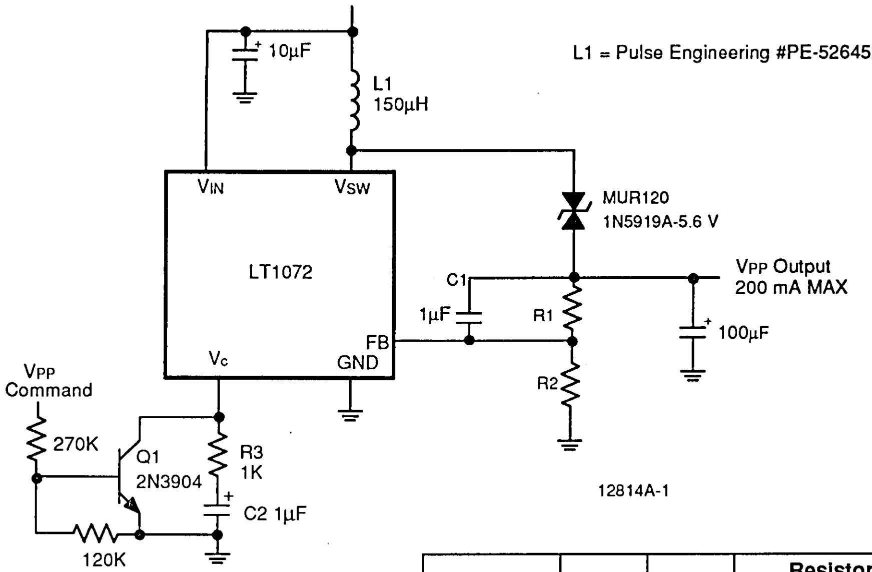
The PM9006 can supply 165 mA of current at the regulated 12.0 V +0.6 V output. The 5.0 V +0.5 V DC input supply of the DC/DC convertor uses a maximum of 840 mA of input current. The Am28F010 specifies a maximum V_{PP} current of 30 mA for either the erase or program operations. Actual current required for these operations is substantially lower than this. Given the maximum V_{PP} current of 30 mA for each device, four(4) Am28F010 may be programmed and erased in parallel with one PM9006 device. The PM9006 V_{PP} supply current = 165 mA – 4 x 30 mA of V_{PP} current required for the Flash memory array = 45 mA of additional current available from the DC/DC convertor.

Parallel programming and erasure allows for the most efficient method to reprogram x16 or x32-bit data words. Refer to the previous application note for parallel program and erasue flow charts.

Board Level Resets

System designs should not allow the Flash device to perform any programming or erase operations when the CPU does not have control of the Flash device. Some designs incorporate board level reset circuitry that suspends operation of the local CPU if the V_{CC} level falls below a predetermined value (such as 4.6 V). If this is the case, the reset circuitry should also disable the V_{PP} power supply whenever the CPU is held in reset.

If the local CPU is forced into reset mode while it is programming or erasing the Flash device, the system reset circuit should also terminate that operation. To accomplish this, the PM9006's enable pin should be driven high whenever the reset circuitry is active. Drive the chip enable pin of the PM9006 with the logical OR of the reset circuit's output signal and the chip enable control line to the PM9006. This will disable the V_{PP} supply and hence terminate any programming or erase operation. The Flash device automatically resets to the read mode when V_{PP} is disabled.



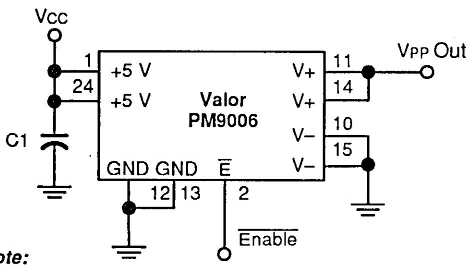
V_{PP} Out	R1	R2	Resistor Tolerance
12.0 V	10.7K	1.24K	1%

Note:

The circuit of Figure 2 will not spuriously overshoot during power-up or power-down. This prevents destruction of the device due to voltages that exceed specification. V_{PP} outputs are predictable and controllable during power supply transitions as a result of the referenced circuit designs. The compensation of the LT1072 causes a very overdamped pulse response. In addition, the control loops of the circuit are functioning even at low supply voltages. Thus the control loop is active before the memory circuits settle and prevents uncontrolled V_{PP} pulse outputs.

Figure 2. Basic Flash Memory V_{PP} Programming Voltage Supply

Please reference the PM9006 data sheet for complete details of device operation. One method of implementing the PM9006 DC/DC convertor is illustrated below.



Note:

Pins 3 through 9 and 16 through 23 are not internally connected to the device and do not need to be driven.

Generate and Control 12.0 V

4. PUMP 5 V TO V_{PP} VOLTAGE WITH ANALOG CIRCUITRY

Flash memories require a V_{PP} voltage of 12.0 V +0.6 V. It is important to note that V_{PP} voltage must be maintained within the device specification for reliable operation. V_{PP} voltages that exceed 14 V for 20 ns or longer are likely to destroy the device. Thus, we need to carefully control the high voltage programming circuitry. It should be noted that proper design of the V_{PP} circuitry eliminates the issues of device destruction due to application of voltages outside of the specified operating range. In addition, it is preferable to control the V_{PP} voltage with a 5.0 V logic command.

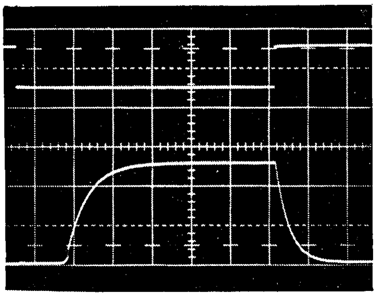
The Starter Kit: V_{PP} Generation and Control

The basic circuit described in Figure 2 satisfies just about all V_{PP} requirements for Flash memories. High voltage is produced by driving the V_{PP} command low. The low V_{PP} command (Trace A, Figure 3) activates the LT1072 switching regulator to drive L1. The resistor network of R1 and R2 provides the DC feedback. C1, R3 and C2 control the AC roll-off. Trace B illustrates the resulting V_{PP} voltage that rises smoothly to the required level. The values specified for R1 and R2 determine the12.0 V output. Leave the 5.6 V zener in the circuit in order to return the output to 0 V when the V_{PP} command goes high. When a 4.5 V minimum output is desired the zener may be omitted. Circuit trimming requirements are eliminated due to the tight internal references of the LT1072. Only precision resistors are required.

The table in Figure 4 gives additional information required to provide greater power output from the referenced circuit. The synchronous switch option of Figure 4 may replace the zener and eliminate its power dissipation.

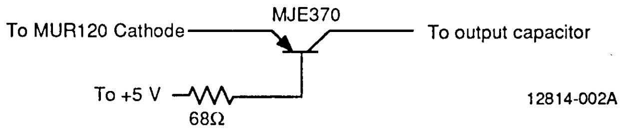
A = 5V/DIV

B = 5V/DIV



Horizontal = 20ms/DIV

Figure 3. Waveforms for Basic Flash Programming Supply



Power Options for Basic V_{PP} Generator

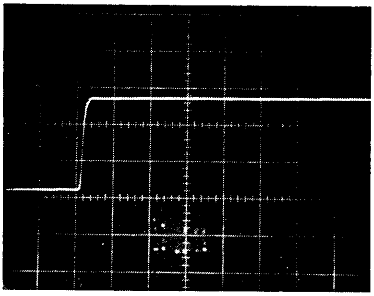
Output Current	C_{OUT}	Regulator	Inductor	Zener
400mA	200 µF	LT1071	PE-52645	1N5339A or Synchronous Switch Option
800mA	400 µF	LT1070	PE-51516	1N5339A or Synchronous Switch Option

Note:

Assume each Flash device requires 30mA VPP current.

Figure 4. Synchronous Switch Option

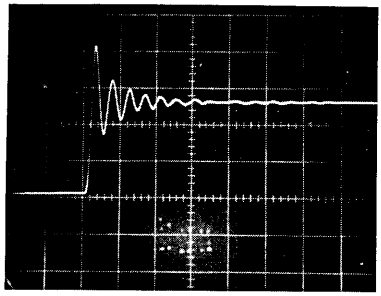
A = 5V/DIV



Horizontal = 100 ns/DIV

Figure B1. An "Ideal" Flash Memory V_{PP} Output

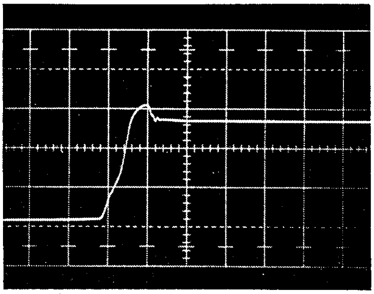
A = 5V/DIV



Horizontal = 100 ns/DIV

Figure B2. Rings at Destructive Voltages After a PC Trace Run

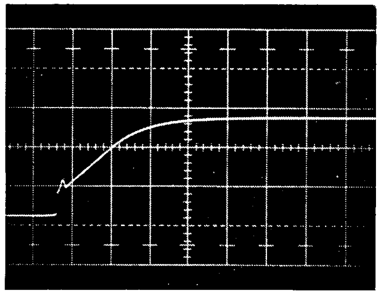
A = 5V/DIV



Horizontal = 2µs/DIV

Figure B3.

A = 5V/DIV



Horizontal = 10µs/DIV

Figure B4.

Note:

Short Circuit Recovery for Poorly (Figured B3) and Properly (Figure B4) Designed Connections. Figure B3's Overshoot on Recovery Can Cause Memory Chip Failures

Transmission Line Effects of Printed Circuit Board Traces on V_{PP} Voltages

One might ask: "Why not use a simple low resistance FET to switch the output of the switching regulator when its level is correctly set?" This sounds good – too good.

In real life, the printed circuit board traces exhibit transmission line effects. Voltages seen at the memory device's pins are not the same as at the output of the regulator. Overshoots result at the junction of the printed circuit board trace and device pins. Thus voltages may exceed device specifications. This concern is compounded since the V_{PP} supply voltages are unusually close to the device's absolute maximum limit of 14V.

Figure B1 illustrates an ideal V_{PP} pulse seen at the output of a simple low loss transistor that is switching the power supply. No overshoot is observed and the V_{PP} pulse settles quickly. The same output is measured (Figure B2) at the memory device pins after running the printed circuit board trace.

Because of mismatching, the PCB trace appears as an unterminated transmission line. Ringing can exceed 20V because of reflections at the junction of the PC trace and device pin. This condition is obviously detrimental to the device. The negative overshoot occurring on the falling edge of the V_{PP} transition may cause equally destructive negative voltages at the device pins.

Properly controlled V_{PP} rise time prevents this type of overshoot. The closed loop circuits discussed earlier eliminate overshoot through controlled edge timings. In addition, the referenced circuits protect the V_{PP} generator against short circuit damage which also protects the memory device.

The V_{PP} output recovery when the diode is removed is shown in Figure B3. Contrast this with Figure B4. Here the diode is in place and the V_{PP} recovery is smooth. Similar considerations apply during power-up/down. During application or removal of power, the V_{PP} generator must not produce spurious output pulses.

V_{PP} outputs are predictable and controllable during transient power supply considerations as a result of the referenced circuit designs. The compensation of the LT1072 causes a very overdamped pulse response. In addition, the control loops of the circuit are functioning even at low supply voltages. Thus the control loop is active before the memory circuits settle and prevent uncontrolled V_{PP} pulse outputs.

Note: *The above circuitry is designed for maximum system protection. Should you desire to modify any circuity, it is advisable to contact Jim Williams of Linear Technology.*

This Document was adapted from Linear Technology's Application Note 31 "Linear Circuits for Digital Sytems: Some Affable Analogs for Digital Devotees," written by Jim Williams, February, 1989.

THIN SMALL OUTLINE PACKAGE (TSOP) DESCRIPTION

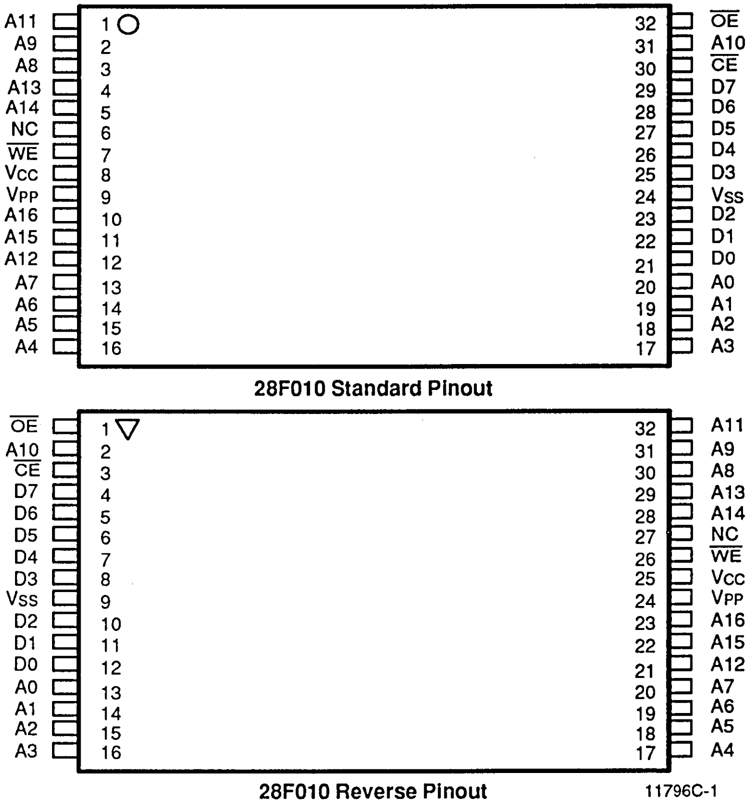
AMD presents the Thin Small Outline Package. The TSOP is the industry's leading edge plastic, surface mountable memory package today. System requirements for higher density and smaller form fit memory arrays are driving this package evolution. TSOP offers a form fit close to that of bare die yet provides the added benefit of being shipped from the factory completely tested, something not available with bare die. This increases system yield because there is no loss due to cleanroom assembly related defects and/or parametric failures.

Primary Characteristics

- JEDEC/EIAJ standard dimensions and 32-pin pinout
- Standard and reverse pinout options
- Maximum package thickness of 1.20 mm

This is AMD's initial offering in state of the art small form fit packaging. The 32-pin package is available in the 8 mm x 20 mm x 1.20 mm package outline. As densities increase, package leadcount will also.

Figure 1-1 28F010 128K x 8 Flash Memory in 32 Lead TSOP



Packaging Evolution

The continuing trend toward smaller systems and/or higher density memory arrays has led to a significant evolution in newer small form fit packaging. This trend is outlined below.

Computers:	Desktop	Notebook	Palmtop
Disk drives:	3-1/2″	2-1/2″/Flash "Disk"	Flash "Disk"
Instrumentation:	Benchtop	Portable	Handheld

Package Type	Package Volume (cubic inches)
PDIP (100 mil Pitch)	0.18
Slim DIP (100 mil Pitch)	0.09
ZIP (100 mil Pitch)	0.072
SOIC/SOJ (50 mil Pitch)	0.075
PLCC (50 mil Pitch)	0.045
TSOP (20 mil Pitch)	0.01

The TSOP is not only suited for standard printed circuit board and Single In-line Memory Module (SIMM) applications, but is the package of choice in the exploding new growth area of solid state memory cards.

TSOP packaging is well suited to high density, small form fit systems. This latest evolution offers significant packaging volume savings in comparison with the above alternatives. Increasingly, TSOP is being used in disk drive controller boards, notebook and palm top PCs, high density memory subsystems, and PCMCIA 68-pin standard memory cards. This is just the beginning.

An emerging market segment with explosive growth is the PCMCIA 68-pin memory card standard. The TSOP can be used to pack both sides of a memory board in order to increase the memory density available within a given space constraint. In addition, the TSOP packaged devices are tested to AMD's standard test flows. This allows AMD to guarantee the highest level of quality and long term reliability.

Minimal Space Requirements

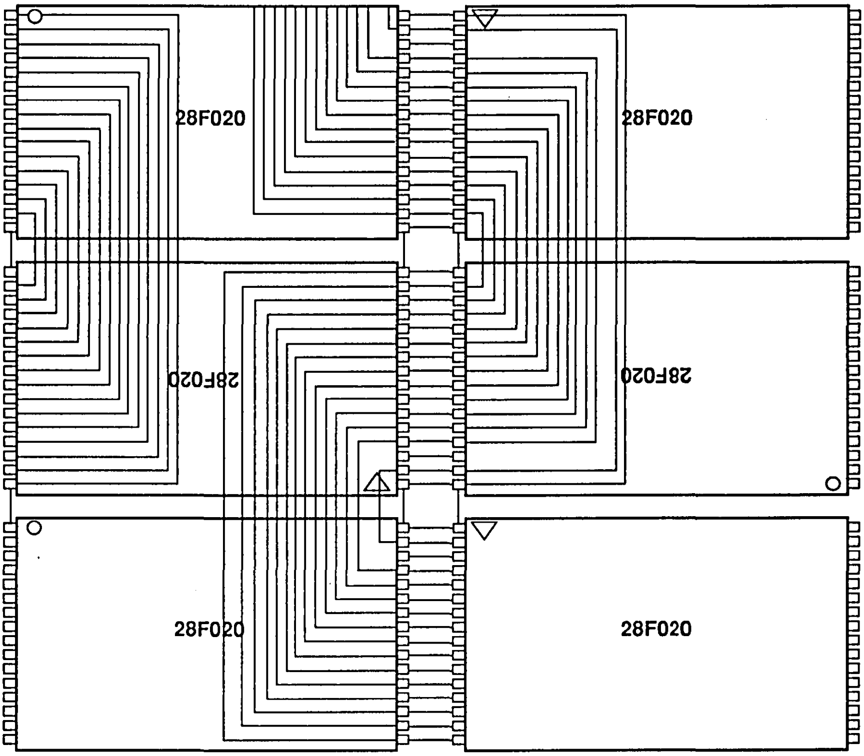
In addition to the TSOP's low height profile, maximum board space saving is achieved with the dual-in-line and standard/reverse pinouts. Board layers can be reduced because traces are routed under the two sides of the package that do not have leads. This allows packages to be mounted side by side and end to end. Packages can be mounted end to end because AMD offers both standard and mirror image reverse pinout packages (see Figure 1-1). All pins except chip enable pins can be connected in parallel. This is accomplished by using standard and reverse pinout packages in an alternating sequence as in Figure 1-2.

HANDLING AND SHIPPING

Shipping Trays

AMD's 32-pin TSOP are shipped in high temperature resistance trays (max. 150°C) having 156 positions per tray. The trays are in compliance with standard JEDEC outlines. JEDEC trays all have the same outside dimensions for easy stacking for use in manufacturing and storage. Trays are designed to prevent TSOP leads from touching any part of the holding tub.

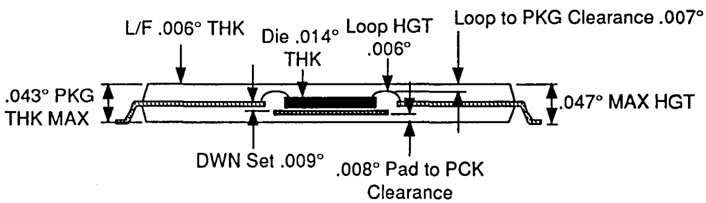
Figure 1-2 OPTIMAL BOARD LAYOUT WITH TSOP



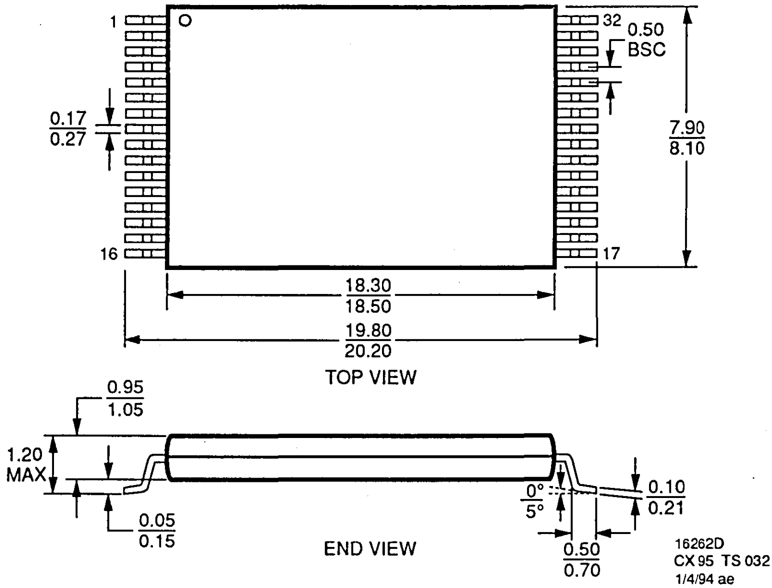
O = Pin 1 indicator for standard bend pinout

△ = Pin 1 indicator for reverse bend pinout

TSOP Cross-Section



PACKAGE DRAWING*



**For the standard form/pin-out, the pin one is a round dimple. For the reverse form/pin-out, an inverted triangle will be marked here indicating pin one.*

**For reference only. All measurements in millimeters. BSC is an ANSI Standard for Basic Space Centering.*

SECTION

4 PUBLISHED FLASH ARTICLES

SEMICONDUCTOR MEMORIES

Making EPROM/flash trade-offs

BY DATAR LALVANI
STRATEGIC MARKETING MANAGER
AND KURT WOLF
SENIOR PRODUCT
MARKETING ENGINEER
ADVANCED MICRO DEVICES INC.
SUNNYVALE, CALIF.

The non-volatile memory market, long the bastion of the UV EPROM, has been fissured with the recent emergence of in-system reprogrammable flash memories as a viable technology. Today, both EPROMs and flash memories coexist and they will continue to run parallel paths, with the choice of technology influenced by the requirements of the end product.

Flash memories were born of the marriage between EPROM and E²PROM devices. Flash incorporates the same programming capability as an EPROM with the added benefit of E²PROM-like electrical erasability, so it can be reprogrammed without removing it from the circuit board. This makes flash an ideal choice for applications that require in-system reprogrammability. While the same benefit can be obtained from either E²PROM or battery-backed SRAM, flash memories are less expensive than both.

In light of the projected rapid growth in demand for flash, the product-development plans announced by the ever-increasing number of vendors, and the recent public announcements by some large vendors—who have stated that their strategy is to "de-emphasize" EPROMs in favor of flash memories—the future of EPROMs has become unclear. This has caused some confusion in the memory marketplace. Technical factors such as scalability, die cost, erasure and package considerations—as well as market-based factors such as demand, applications and features—factor into the decisions to build and use either EPROM or flash products.

EPROMs and flash memories will coexist with the choice of technology influenced by the requirements of the end product as used by the customer. While some vendors have stated that flash memories are more scalable than EPROMs with the addition of double-layer metal,even down at 0.5-micron geometries, Advanced Micro Devices Inc. sees no need for multilayer metal for EPROMs. AMD's single-layer metal process for EPROMs using 0.5-micron technology not only will provide the high density—up to the 16-Mbit level—but is also capable of generating the smallest die size and highest performance in the industry.

It is a fact that, at the same density, the flash-memory die is more expensive than an EPROM because it has the slightly larger cell size required to support high endurance. Also, the flash process complexity is greater due to additional masking steps, and it requires longer test times to perform electrical erasure in the tester, as opposed to UV-erase in an oven.

Flash pricing today remains at a multiple of EPROM. However, flash pricing will continue to drop until it settles at around a 20 percent to 30 percent premium over a comparable EPROM. Memory designers are not going to increase the cost of their systems by using flash when there is no need for future reprogramming. In these designs, reprogrammability does not represent value to the customer. Consequently, flash technology will not ubiquitously replace OTP EPROM designs.

The market's demand for various price/performance products supports the coexistence of both EPROM and flash technology.

There is no question that flash technology has already reserved a bright spot in the history of non-volatile memories. In some designs, however, EPROM and flash memories can coexist comfortably. Laser-printer designs are becoming commodity-oriented items. Memory-design requirements are dictated by the pages-per-minute output of the printer. Memory designers can make a trade-off between designing interleaved systems with slower/less expensive devices or non-interleaved systems using faster/higher-cost devices. The software requirements for these systems are also fairly straightforward. Firmware that typically does not change in this system are the PCL-5 and/or Postscript engine-control codes.

In addition, the code for font types does not typically change. The density requirements for this code range from 2 to 4 Mbytes of storage, depending on the font types available and the number of scaling options. EPROMs instead of ROMs are used to provide manufacturing flexibility. The EPROMs are programmed just-in-time, depending on the printer engine and font options

Datar Lalvani holds a BSEE from the University of Madras, India, and an MBA from the Wharton Graduate School of Business, University of Pennsylvania. Kurt Wolf holds a BSEE from the University of Michigan.

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SEMICONDUCTOR MEMORIES

Choosing flash or EPROM

Continued

required for that day's manufacturing run. Flash memory is then incorporated as an option that allows end users to store customized fonts or screen images in the printer. This eliminates the repetitive delay associated with transferring the bit-map-generated images between the computer and printer. This decrease in productivity is eliminated when the code is resident on the printer in flash memory, a clear example of a very high-volume product that requires both high-density EPROM and flash-memory devices.

Each technology is employed to take advantage of its strengths. OTP EPROMs are used in the most cost-sensitive portion of the memory system where the code typically does not change once the system is shipped. OTP EPROMs also allow for smooth transitions between manufacturing runs that incorporate different printer engines and/or font type options.

The higher-priced flash devices provide customers with the ability to personalize their systems. The value of this functionality more than offsets the incremental cost of the devices.

REPROGRAMMING ADDS SOME FLASH TO CELLULAR COMMUNICATION

BY IAN WILLIAMS
AND KURT WOLF
MARKETING MGRS.
AMD INC.
SUNNYVALE, CALIF.

Adding value such as easy reprogrammability to a cellular communications system can bring about another market surge in this popular technology. It is a given that cellular phones allow people to make more efficient use of their driving time. However, if a user wants to change cellular carrier companies for more competitive rates and/or features or move to an area not covered by his/her current carrier, the cellular phone must be reprogrammed at a cellular service service center, a procedure that can cause many hours of unproductive phone downtime.

The use of Flash memory in cellular phones can speed up that update process. For example, a customer who doesn't have the use of Flash memory who decides to change cellular has to bring his phone to the shop, where the phone is disassembled to remove and replace the old EPROM with a newly programmed device, then reassembled and, finally, reinstalled in the car. This is a time-consuming process and involves the expense of new components.The total cost includes the labor costs associated with manually changing code that is typically stored in EPROM and the lost productivity that occurs when the customer's phone is unavailable.

Remote memory updates with a Flash memory-based system are more cost-effective than any other non-volatile memory system. The piece-part price of Flash memories is greater than EPROM- and ROM-based memories. However, the cost of updating memory contents in a remote memory system that is EPROM- and ROM-based is orders of magnitude more costly than performing remote updates on a Flash memory-based system. This cost difference is driven primarily by the cost of the labor required to update firmware in EPROM- and ROM-based systems.

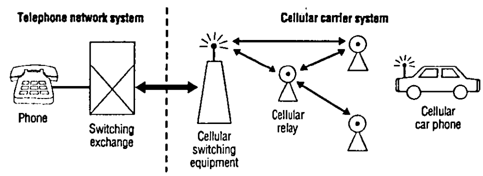
The Flash memory-based system evolves to one that employs a combination of both Flash and other non-volatile memory alternatives. Over time, more and more of a system's firmware becomes stable and does not require future updates. This usually includes the basic structure of the firmware program but not the specialized subroutines it may call.

At this point, a lower-cost memory system is implemented with a combination of Flash and other non-volatile memory. The Flash memory stores those portions of code that many change in the future.

Subroutines that allow the host system to interact with other remote external systems are examples of code segments that may be periodically updated. The alternate non-volatile memory devices store the main structure of the firmware that remains stable.

In fact, Flash memories offer benefits throughout the entire cellular communications system, which is comprised of the main switching equipment, the site relay, and the phones themselves (see figure).

Cellular communication system ripe for flash-memory use



The main cellular switching equipment serves as a link between the telephone network system to provide access for the customer. The switch equipment acts as a controller for the cellular relays, which convert the RF phone signals to analog. The relays also employ transceivers to send and receive the phone communications. The main system switch monitors its network of relays and determines call placement and routing.

The cellular switching equipment is responsible for connecting calls into the telephone network system and for monitoring and controlling its cellular relays. The switches contain the routing algorithms for call placement. These algorithms take into account the traffic load of the cellular sites and the geographic terrain that may affect relay of the transmitted signals. The main switching equipment also keeps track of customer databases, which maintain a file of phone service features that are active for each customer. Among these features are call waiting, call forwarding, and voice mail.

The cellular phone itself contains the basic communication techniques between the phone and the cellular relays, the system parameters that allow communication with the customer's specific cellular carrier. The caller's phone number is also contained within the phone in order to identify which customer is accessing the system and which features should be activated. The Digital Tone Modulated Frequency (DTMF) parameters are also stored in order to allow for automated touch-tone functions such as voice mail.

Another application for Flash memories in a cellular communications system is the customer database, which resides in another part of the switching equipment's memory system. Customer databases may be set up as a file structure in the Flash memory space. Each customer file may consist of multiple bytes of address space. Multiple account files may reside on a single Flash device by maintaining files that have an I.D. associated with each customer's account (i.e., the customer's phone number).

This link allows the system to access each user's file during a call to determine which phone service features the customer is entitled to use. Separate codes may exist for both the activation and deactivation of particular service features (i.e., call waiting). An activated service feature may be canceled by adding the deactivation code to the customer's file. Before establishing the phone connection, the system scans the customer file to look for active service features and to check if any features have been canceled.

Today each cellular phone model must be uniquely programmed at the dealer's installation site. Typically, these phones use socketed EPROMs. The installation department programs these EPROMs with appropriate system parameters and DTMF codes to function with the specific carrier chosen.

By contrast, when the user wants to change carriers or moves to a town outside of his current service area, his/her phone must be reprogrammed at a cellular service center.

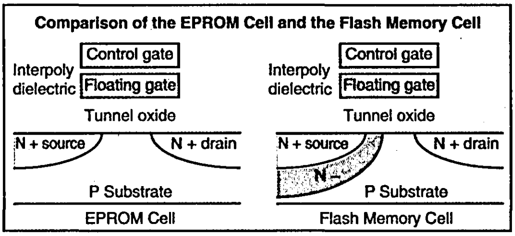
Flash memories offer an innovative solution to the inconvenience of bringing in your car phone in order to change carriers or when you move from one cellular service area to another., Flash memories, which are electrically programmable in-system, allow code changes to be performed by transferring data over the cellular network.

For instance, a user could schedule his/her phone to be reprogrammed during a morning commute. The cellular service station then dials the user's phone to establish a data link for transmitting data, thus optimizing the inherent communications capability of the cellular system. ■

16609A

Flash widens scope for code storage

Patrick Henry charts the progress in features and endurance of some of the latest flash memory chips



Flash memory has revolutionised how designers think about storing control code in computers, peripherals and communications devices. In-system re-programmability, low voltage and high speed help design objectives to be met in a wide range of microprocessor and microcontroller-based products. It has become the preferred choice where any of the following is true;

—the control code is not stable or is in the prototyping stage;

—a standard diagnostic test is used during testing and end-user code is reprogrammed into the device only at the final assembly stage;

—the code could potentially be altered in-system, due to code revisions, customisation by the end user or the systems being dynamically self-configuring;

—there is a standard hardware platform and customer-specific code across the product line.

Features which add value include in-system re-programmability, 5V only operation, sector erase with protection and high reliability.

In-system re-programmable code has several advantages including time to market and improved manufacturing and inventory efficiencies, with improved flexibility for the end-user. Not only has the 12V requirement been eliminated, but the devices will tolerate ±10percent on the 5V Vcc. Typical erase sector sizes now range from 8k to 64kBytes; per-sector protection allows protection of boot code from inadvertent erasure, and can eliminate a separate boot ROM.

Where hardware and software development takes place in parallel, the hardware can be developed with early version software and re-loaded with later versions as the project progresses, easing the path of both and removing the need to remove socketed UVPROM or conventional EPROM for reprogramming, scrap early production boards or rework them. Once the code is finally stable it can be switched into OTP EPROM or even mask ROM to reduce costs without interrupting production.

100percent testing can be carried out with diagnostic code, replaced before shipping with the final functional code; reliability monitoring is also assisted in this way.

Standard hardware units can be customised for different markets, reducing inventory costs; cellular phones semi-customised with firmware for different countries is an example of this approach. End-users can re-configure the code, to add features or update to a later version of the complete code. PC BIOS is a case in point, where new PCMCIA socket services, VGA commands and advanced power management can all be included as BIOS extensions.

Reliability

High reliability is essential in microcontroller-based products due to the high cost of field failures and their effect on the manufacturer's reputation. The latest flash memory devices can provide the required degree of reliability. As shown in Fig. 1, the memory cell of the industry standard single transistor NOR-type flash device is nearly identical in design and processing to the cell on mature UV EPROM products, with only two differences;

—the flash cell uses a graded double diffusion on the source;

—and has a thinner tunnel oxide, about 100Angstroms (against 150 Angstroms for the EPROM cell).

Double diffusion on the source and a thinner tunnel oxide help Fowler-Nordheim tunneling during erase. A great deal of reliability data exists on EPROM cell technology, including verified data retention of a minimum of 10years at 150C and 20years at 125C.

The most advanced flash chips use an on-chip state machine to control program and erase; with this on-chip a minimum amount of assembly code must be written to program and erase the device compared to earlier generation devices. Mis-implementation of first generation manual flash algorithms is in fact the cause of most flash device problems. The two most common specific errors were mis-implementation of the timing algorithms and skipping the pre-programming step in the erase algorithm. With the software on the silicon, both of these issues and many other have been resolved.

Endurance is also an important measure of reliability; endurance is the number of erase cycles that a device can withstand. This has been raised from 1000 to the present 10 000 cycles with a failure rate of 0.5percent. The most advanced devices now achieve 100 000 erase cycles; devices supplied with the "Embedded Program" and "Embedded Erase" algorithms offer a minimum of 100 000 write cycles at a failure rate of 0.3percent.

With these devices the failure rate is linear ie the failure mechanism is random and equally likely to occur at any time in the life of the device; so the equivalent failure rate at 10 000 cycles can be expressed as 0.03percent, or some 17 times better than the previous standard 10 000cycle endurance. Additionally, the embedded algorithms detect and correct soft errors caused by over-erased bits.

In a population of equipments with equivalent numbers of flash devices, the use of this new generation of devices—again, because the failure rate is linear—will result in a direct reduction of product returns by the same factor of 17.

Flash memory should still not be used in all systems, as there are still trade-offs; but in most instances designers have to make fewer sacrifices when flash is used for control code storage.

Patrick Henry is Product Marketing Manager with AMD in Sunnyvale; in the UK call 0483 740440.

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SECTION

5 FLASH MEMORY PC CARDS

CONDENSED

AmC001AFLKA

1 Megabyte 12.0 Volt Flash Memory PC Card

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - — 250 ns maximum access time
- **CMOS low power consumption**
  - — 25 mA typical active current (X8)
  - — 400 µA typical standby current
- **PCMCIA/JEIDA 68-pin standard**
  - — Selectable byte or word-wide configuration
- **Write protect switch**
  - — Prevents accidental data loss
- **High re-programmable endurance**
  - — Minimum 100,000 erase/write cycles
- **Zero data retention power**
  - — Batteries not required for data storage
- **Separate attribute memory**
  - — 512 byte EEPROM
- **Automated write and erase operations (increases system write performance)**
  - — 128K byte memory segment
  - — Typically <1 second per single memory segment erase
  - — Random address writes to previously erased bytes (10 µs typical per byte)
- **Total system integration solution**
  - — Support from independent software and hardware vendors
- **Insertion and removal force**
  - — State of art connector allows for minimum card insertion and removal effort
- **Write and erase voltage, 12.0 V ± 5%**
- **Read voltage, 5 V ± 5%**
- **Manufactured by Berg Electronics**

GENERAL DESCRIPTION

AMD's Flash Memory PC Card provides the highest system level performance for data and file storage solutions to the portable PC market segment. Data files and application programs can be stored on the AmC001AFLKA. This allows OEM manufacturers of portable system to eliminate the weight, extreme power consumption and reliability issues associated with electro-mechanical disk-based systems. The AmC001AFLKA also allows today's bulky and heavy battery packs to be reduced in weight and size. Typically only two "AA" alkaline batteries are required for total system operation. AMD's Flash Memory PC Cards provide the most efficient method to transfer useful work between different hardware platforms. The enabling technology of the AmC001AFLKA enhances the productivity of mobile workers.

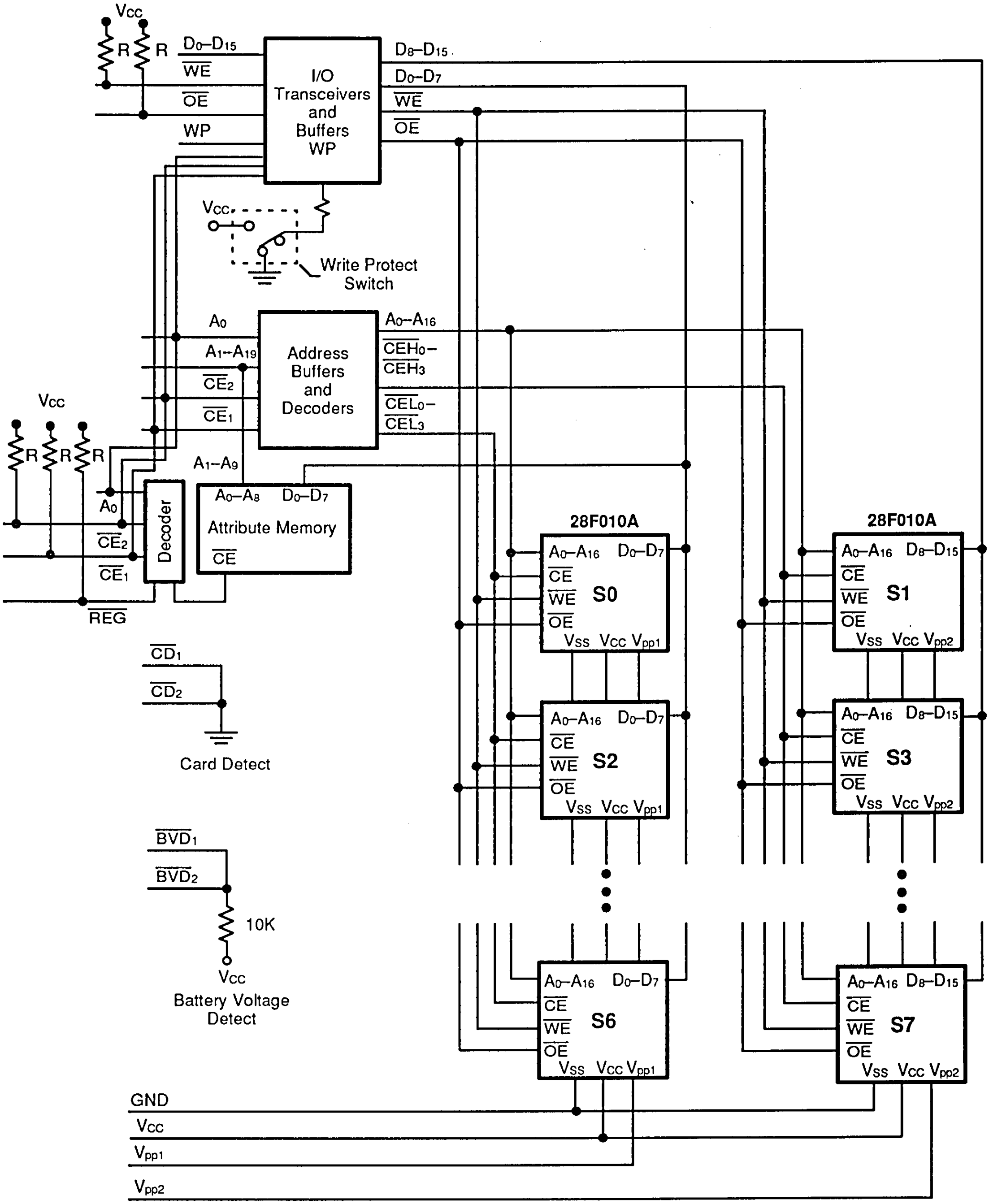
Widespread acceptance of the AmC001AFLKA is assured due to its compatibility with the 68-pin PCMCIA/JEIDA international standard. AMD's Flash Memory Cards can be read in either a byte-wide or word-wide mode which allows for flexible integration into various system platforms. Compatibility is assured at the hardware interface and software interchange specification. The Card Information Structure (CIS) or Metaformat, can be written by the OEM at the Memory Card's attribute memory address space beginning at address 00000H by using a format utility. The CIS appears at the beginning of the Card's attribute memory space and defines the low-level organization of data on the PC Card. The AmC001AFLKA contains a separate 512 byte EEPROM memory for the card's attribute memory space. This allows all of the Flash Memory to be used for the common memory space.

Third party software solutions such as Microsoft's Flash File System (FFS), enable AMD's Flash Memory PC Card to replicate the function of traditional disk-based memory systems.

Manufactured by Berg Electronics BERG

Publication# C17120 Rev. A Amendment/0
Issue Date: March 1994

BLOCK DIAGRAM



R=33K

C17120A-1

PC CARD PIN ASSIGNMENTS

Pin#	Signal	I/O	Function	Pin#	Signal	I/O	Function
1	GND		Ground	35	GND		Ground
2	D_3	I/O	Data Bit 3	36	$\overline{CD_1}$	O	Card Detect (Note 1)
3	D_4	I/O	Data Bit 4	37	D_{11}	I/O	Data Bit 11
4	D_5	I/O	Data Bit 5	38	D_{12}	I/O	Data Bit 12
5	D_6	I/O	Data Bit 6	39	D_{13}	I/O	Data Bit 13
6	D_7	I/O	Data Bit 7	40	D_{14}	I/O	Data Bit 14
7	$\overline{CE_1}$	I	Card Enable (Note 1)	41	D_{15}	I/O	Data Bit 15
8	A_{10}	I	Address Bit 10	42	$\overline{CE_2}$	I	Card Enable 2 (Note 1)
9	$\overline{OE}$	I	Output Enable	43	NC		No Connect
10	A_{11}	I	Address Bit 11	44	NC		No Connect
11	A_9	I	Address Bit 9	45	NC		No Connect
12	A_8	I	Address Bit 8	46	A_{17}	I	Address Bit 17
13	A_{13}	I	Address Bit 13	47	A_{18}	I	Address Bit 18
14	A_{14}	I	Address Bit 14	48	A_{19}	I	Address Bit 19
15	$\overline{WE}$	I	Write Enable	49	NC		No Connect
16	NC		No Connect	50	NC		No Connect
17	Vcc		Power Supply	51	V_{cc}		Power Supply
18	Vpp1		Pgm Sply Vltg 1	52	V_{pp2}		Pgm Sply Vltg 2
19	A_{16}	I	Address Bit 16	53	NC		No Connect
20	A_{15}	I	Address Bit 15	54	NC		No Connect
21	A_{12}	I	Address Bit 12	55	NC		No Connect
22	A_7	I	Address Bit 7	56	NC		No Connect
23	A_6	I	Address Bit 6	57	NC		No Connect
24	A_5	I	Address Bit 5	58	NC		No Connect
25	A_4	I	Address Bit 4	59	NC		No Connect
26	A_3	I	Address Bit 3	60	NC		No Connect
27	A_2	I	Address Bit 2	61	$\overline{REG}$	I	Register Select
28	A_1	I	Address Bit 1	62	$\overline{BVD_2}$	O	Battery Vltg Detect 2 (Note 2)
29	A_0	I	Address Bit 0	63	$\overline{BVD_1}$	O	Battery Vltg Detect 1 (Note 2)
30	D_0	I/O	Data Bit 0	64	D_8	I/O	Data Bit 8
31	D_1	I/O	Data Bit 1	65	D_9	I/O	Data Bit 9
32	D_2	I/O	Data Bit 2	66	D_{10}	I/O	Data Bit 10
33	WP	O	Write Protect (Note 1)	67	$\overline{CD_2}$	O	Card Detect
34	GND		Ground	68	GND		Ground

Notes:

I = Input to card, O = Output from card
I/O = Bi-directional
NC = No connect
In systems which switch Vcc individually to cards, no signal should be directly connected between cards other than ground.
1. Signal must not be connected between cards
2. BVD = Internally pulled-up

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

Am C 001 A FL K A -250, CSxxxxx

- **CUSTOMER SPECIFIC IDENTIFICATION NUMBER**
- **SPEED OPTION**
- **REVISION LEVEL**
- **OUTPUT CONFIGURATION:** (x16/x8)
- **FLASH TECHNOLOGY**
- **100,000 ERASE/PROGRAM CYCLES MINIMUM**
- **MEMORY CARD DENSITY** 001 = One Megabyte
- **PC MEMORY CARD**
- **AMD**

CONDENSED

AmC002AFLKA

2 Megabyte 12.0 Volt Flash Memory PC Card

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 250 ns maximum access time
- **CMOS low power consumption**
  - 25 mA typical active current (X8)
  - 400 µA typical standby current
- **PCMCIA/JEIDA 68-pin standard**
  - Selectable byte or word-wide configuration
- **Write protect switch**
  - Prevents accidental data loss
- **High re-programmable endurance**
  - Minimum 100,000 erase/write cycles
- **Zero data retention power**
  - Batteries not required for data storage
- **Separate attribute memory**
  - 512 byte EEPROM
- **Automated Write and Erase Operations (Increases System Write Performance)**
  - 256K byte memory segment
  - Typically <1.5 seconds per single memory segment erase
  - Random address writes to previously erased bytes (14 µs typical per byte)
- **Total system integration solution**
  - Support from independent software and hardware vendors
- **Insertion and removal force**
  - State of art connector allows for minimum card insertion and removal effort
- **Write and erase voltage, 12.0 V ± 5%**
- **Read voltage, 5 V ± 5%**
- **Manufactured by Berg Electronics**

GENERAL DESCRIPTION

AMD's Flash Memory PC Card provides the highest system level performance for data and file storage solutions to the portable PC market segment. Data files and application programs can be stored on the AmC002AFLKA. This allows OEM manufacturers of portable system to eliminate the weight, extreme power consumption and reliability issues associated with electro-mechanical disk-based systems. The AmC002AFLKA also allows today's bulky and heavy battery packs to be reduced in weight and size. Typically only two "AA" alkaline batteries are required for total system operation. AMD's Flash Memory PC Cards provide the most efficient method to transfer useful work between different hardware platforms. The enabling technology of the AmC002AFLKA enhances the productivity of mobile workers.

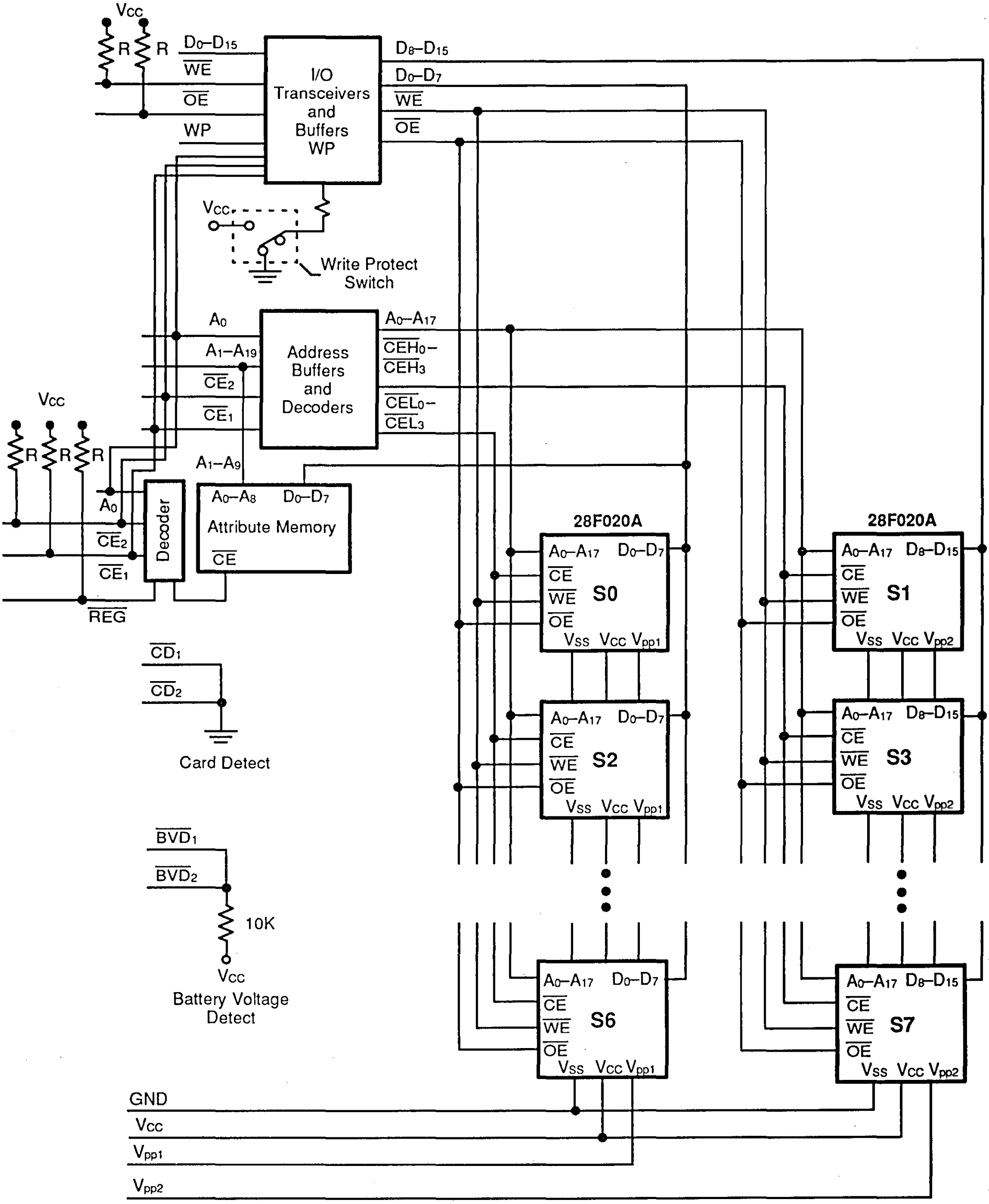
Widespread acceptance of the AmC002AFLKA is assured due to its compatibility with the 68-pin PCMCIA/JEIDA international standard. AMD's Flash Memory Cards can be read in either a byte-wide or word-wide mode which allows for flexible integration into various system platforms. Compatibility is assured at the hardware interface and software interchange specification. The Card Information Structure (CIS) or Metaformat, can be written by the OEM at the Memory Card's attribute memory address space beginning at address 00000H by using a format utility. The CIS appears at the beginning of the Card's attribute memory space and defines the low-level organization of data on the PC Card. The AmC002AFLKA contains a separate 512 byte EEPROM memory for the card's attribute memory space. This allows all of the Flash Memory to be used for the common memory space.

Third party software solutions such as Microsoft's Flash File System (FFS), enable AMD's Flash Memory PC Card to replicate the function of traditional disk-based memory systems.

Manufactured by Berg Electronics BERG

Publication# C17273 Rev. A Amendment/0
Issue Date: September 1992

BLOCK DIAGRAM



R=33K

C17273A-1

PC CARD PIN ASSIGNMENTS

Pin#	Signal	I/O	Function	Pin#	Signal	I/O	Function
1	GND		Ground	35	GND		Ground
2	D_3	I/O	Data Bit 3	36	$\overline{CD_1}$	O	Card Detect (Note 1)
3	D_4	I/O	Data Bit 4	37	D_{11}	I/O	Data Bit 11
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13	A_{13}	I	Address Bit 13	47	A_{18}	I	Address Bit 18
14	A_{14}	I	Address Bit 14	48	A_{19}	I	Address Bit 19
15	$\overline{WE}$	I	Write Enable	49	A_{20}	I	Address Bit 20
16	NC		No Connect	50	NC		No Connect
17	Vcc		Power Supply	51	V_{CC}		Power Supply
18	Vpp1		Pgm Sply Vltg 1	52	V_{PP2}		Pgm Sply Vltg 2
19	A_{16}	I	Address Bit 16	53	NC		No Connect
20	A_{15}	I	Address Bit 15	54	NC		No Connect
21	A_{12}	I	Address Bit 12	55	NC		No Connect
22	A_7	I	Address Bit 7	56	NC		No Connect
23	A_6	I	Address Bit 6	57	NC		No Connect
24	A_5	I	Address Bit 5	58	NC		No Connect
25	A_4	I	Address Bit 4	59	NC		No Connect
26	A_3	I	Address Bit 3	60	NC		No Connect
27	A_2	I	Address Bit 2	61	$\overline{REG}$	I	Register Select
28	A_1	I	Address Bit 1	62	$\overline{BVD_2}$	O	Battery Vltg Detect 2 (Note 2)
29	A_0	I	Address Bit 0	63	$\overline{BVD_1}$	O	Battery Vltg Detect 1 (Note 2)
30	D_0	I/O	Data Bit 0	64	D_8	I/O	Data Bit 8
31	D_1	I/O	Data Bit 1	65	D_9	I/O	Data Bit 9
32	D_2	I/O	Data Bit 2	66	D_{10}	I/O	Data Bit 10
33	WP	O	Write Protect (Note 1)	67	$\overline{CD_2}$	O	Card Detect
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ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

Am C 002 A FL K A -250, CSxxxxx

- **CSxxxxx** — CUSTOMER SPECIFIC IDENTIFICATION NUMBER
- **-250** — SPEED OPTION
- **A** — REVISION LEVEL
- **K** — OUTPUT CONFIGURATION: (x16/x8)
- **FL** — FLASH TECHNOLOGY
- **A** — 100,000 ERASE/PROGRAM CYCLES MINIMUM
- **002** — MEMORY CARD DENSITY
  - 001 = One Megabyte
  - 002 = Two Megabyte
- **C** — PC MEMORY CARD
- **Am** — AMD

CONDENSED

AmC004AFLKA

4 Megabyte 12.0 Volt Flash Memory PC Card

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 250 ns maximum access time
- **CMOS low power consumption**
  - 25 mA typical active current (X8)
  - 400 µA typical standby current
- **PCMCIA/JEIDA 68-pin standard**
  - Selectable byte or word-wide configuration
- **Write protect switch**
  - Prevents accidental data loss
- **High re-programmable endurance**
  - Minimum 100,000 erase/write cycles
- **Zero data retention power**
  - Batteries not required for data storage
- **Separate Attribute Memory**
  - 512 byte EEPROM
- **Automated write and erase operations (increases system write performance)**
  - 256K byte memory segment
  - Typically <1.5 seconds per single memory segment erase
  - Random address writes to previously erased bytes (14 µs typical per byte)
- **Total system integration solution**
  - Support from independent software and hardware vendors
- **Insertion and removal force**
  - State of art connector allows for minimum card insertion and removal effort
- **Write and erase voltage, 12.0 V ± 5%**
- **Read voltage, 5 V ± 5%**
- **Manufactured by Berg Electronics**

GENERAL DESCRIPTION

AMD's Flash Memory PC Card provides the highest system level performance for data and file storage solutions to the portable PC market segment. Data files and application programs can be stored on the AmC004AFLKA. This allows OEM manufacturers of portable system to eliminate the weight, extreme power consumption and reliability issues associated with electro-mechanical disk-based systems. The AmC004AFLKA also allows today's bulky and heavy battery packs to be reduced in weight and size. Typically only two "AA" alkaline batteries are required for total system operation. AMD's Flash Memory PC Cards provide the most efficient method to transfer useful work between different hardware platforms. The enabling technology of the AmC004AFLKA enhances the productivity of mobile workers.

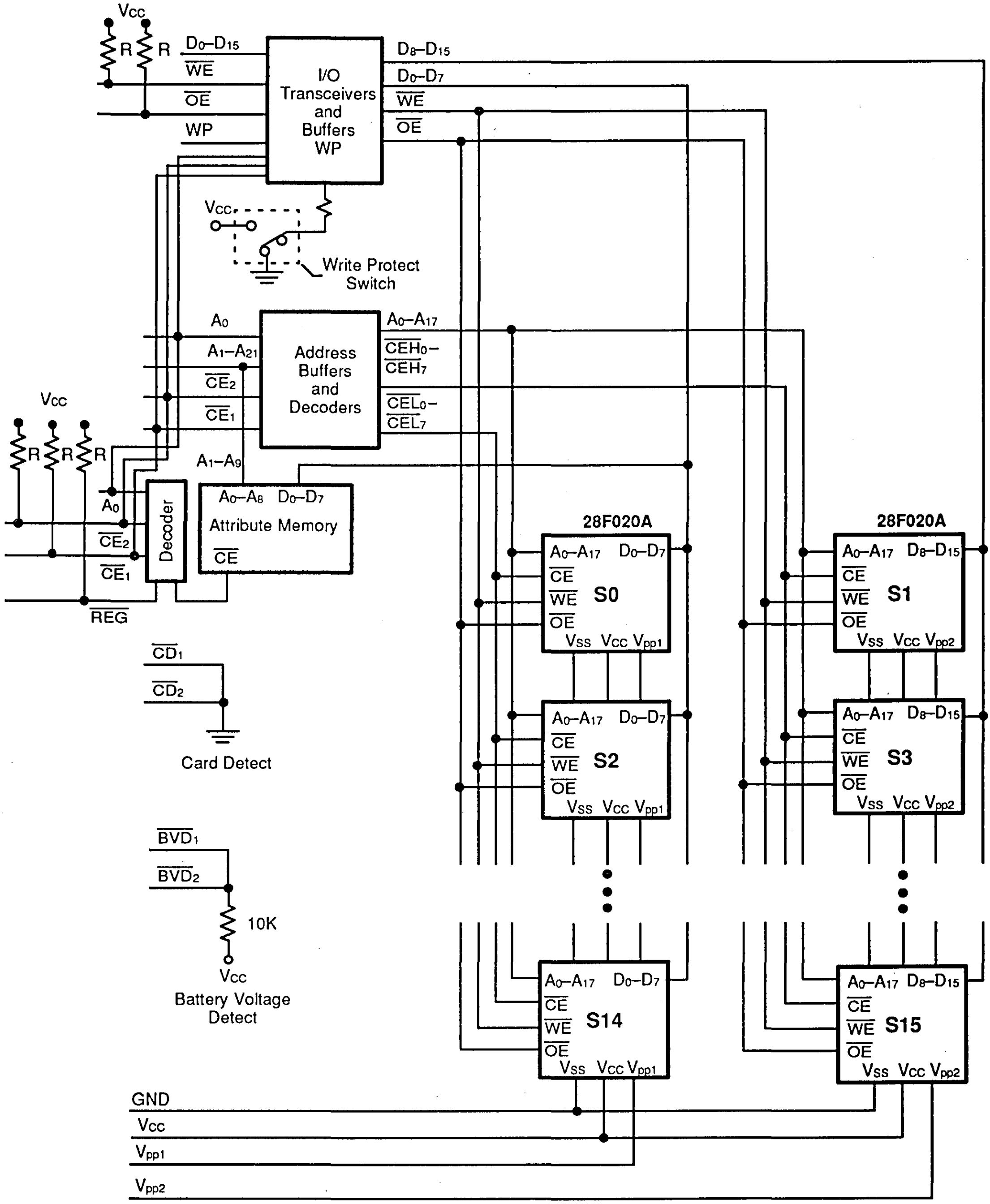
Widespread acceptance of the AmC004AFLKA is assured due to its compatibility with the 68-pin PCMCIA/JEIDA international standard. AMD's Flash Memory Cards can be read in either a byte-wide or word-wide mode which allows for flexible integration into various system platforms. Compatibility is assured at the hardware interface and software interchange specification. The Card Information Structure (CIS) or Metaformat, can be written by the OEM at the Memory Card's attribute memory address space beginning at address 00000H by using a format utility. The CIS appears at the beginning of the Card's attribute memory space and defines the low-level organization of data on the PC Card. The AmC004AFLKA contains a separate 512 byte EEPROM memory for the card's attribute memory space. This allows all of the Flash Memory to be used for the common memory space.

Third party software solutions such as Microsoft's Flash File System (FFS), enable AMD's Flash Memory PC Card to replicate the function of traditional disk-based memory systems.

Manufactured by Berg Electronics BERG

Publication# C17274 Rev. A Amendment/0
Issue Date: September 1992

BLOCK DIAGRAM



R=33K

C17274A-1

PC CARD PIN ASSIGNMENTS

Pin#	Signal	I/O	Function	Pin#	Signal	I/O	Function
1	GND		Ground	35	GND		Ground
2	D_3	I/O	Data Bit 3	36	$\overline{CD}_1$	O	Card Detect (Note 1)
3	D_4	I/O	Data Bit 4	37	D_{11}	I/O	Data Bit 11
4	D_5	I/O	Data Bit 5	38	D_{12}	I/O	Data Bit 12
5	D_6	I/O	Data Bit 6	39	D_{13}	I/O	Data Bit 13
6	D_7	I/O	Data Bit 7	40	D_{14}	I/O	Data Bit 14
7	$\overline{CE}_1$	I	Card Enable (Note 1)	41	D_{15}	I/O	Data Bit 15
8	A_{10}	I	Address Bit 10	42	$\overline{CE}_2$	I	Card Enable 2 (Note 1)
9	$\overline{OE}$	I	Output Enable	43	NC		No Connect
10	A_{11}	I	Address Bit 11	44	NC		No Connect
11	A_9	I	Address Bit 9	45	NC		No Connect
12	A_8	I	Address Bit 8	46	A_{17}	I	Address Bit 17
13	A_{13}	I	Address Bit 13	47	A_{18}	I	Address Bit 18
14	A_{14}	I	Address Bit 14	48	A_{19}	I	Address Bit 19
15	$\overline{WE}$	I	Write Enable	49	A_{20}	I	Address Bit 20
16	NC		No Connect	50	A_{21}	I	Address Bit 21
17	Vcc		Power Supply	51	V_{CC}		Power Supply
18	Vpp1		Pgm Sply Vltg 1	52	V_{PP2}		Pgm Sply Vltg 2
19	A_{16}	I	Address Bit 16	53	NC		No Connect
20	A_{15}	I	Address Bit 15	54	NC		No Connect
21	A_{12}	I	Address Bit 12	55	NC		No Connect
22	A_7	I	Address Bit 7	56	NC		No Connect
23	A_6	I	Address Bit 6	57	NC		No Connect
24	A_5	I	Address Bit 5	58	NC		No Connect
25	A_4	I	Address Bit 4	59	NC		No Connect
26	A_3	I	Address Bit 3	60	NC		No Connect
27	A_2	I	Address Bit 2	61	$\overline{REG}$	I	Register Select
28	A_1	I	Address Bit 1	62	$\overline{BVD}_2$	O	Battery Vltg Detect 2 (Note 2)
29	A_0	I	Address Bit 0	63	$\overline{BVD}_1$	O	Battery Vltg Detect 1 (Note 2)
30	D_0	I/O	Data Bit 0	64	D_8	I/O	Data Bit 8
31	D_1	I/O	Data Bit 1	65	D_9	I/O	Data Bit 9
32	D_2	I/O	Data Bit 2	66	D_{10}	I/O	Data Bit 10
33	WP	O	Write Protect (Note 1)	67	$\overline{CD}_2$	O	Card Detect
34	GND		Ground	68	GND		Ground

Notes:

I = Input to card, O = Output from card
I/O = Bi-directional
NC = No connect
In systems which switch Vcc individually to cards, no signal should be directly connected between cards other than ground.
1. Signal must not be connected between cards
2. BVD = Internally pulled-up

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

Am C 004 A FL K A -250, CSxxxxx

- **CSxxxxx** — **CUSTOMER SPECIFIC IDENTIFICATION NUMBER**
- **-250** — **SPEED OPTION**
- **A** — **REVISION LEVEL**
- **K** — **OUTPUT CONFIGURATION:** (x16/x8)
- **FL** — **FLASH TECHNOLOGY**
- **A** — **100,000 ERASE/PROGRAM CYCLES MINIMUM**
- **004** — **MEMORY CARD DENSITY**
  001 = One Megabyte
  004 = Four Megabyte
- **C** — **PC MEMORY CARD**
- **Am** — **AMD**

CONDENSED

AmC001BFLKA

1 Megabyte 5.0 Volt-only Flash Memory PC Card

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 200 ns maximum access time
- **Single supply operation**
  - Write and erase voltage, 5.0 V ± 5%
  - Read voltage, 5.0 V ± 5%
- **CMOS low power consumption**
  - 31 mA maximum active read current (x8 mode)
  - 1 mA maximum standby current
- **High write endurance**
  - Minimum 100,000 erase/write cycles
- **PCMCIA/JEIDA 68-pin standard**
  - Selectable byte or word-wide configuration
- **Write protect switch**
  - Prevents accidental data loss
- **Zero data retention power**
  - Batteries not required for data storage
- **Separate attribute memory**
  - 512 byte EEPROM
- **Automated write and erase operations increase system write performance**
  - 64 x 16K byte memory sectors for faster automated erase speed
  - Typically 1.3 seconds per single memory sector erase
  - Random address writes to previously erased bytes (14 µs typical per byte)
- **Total system integration solution**
  - Support from independent software and hardware vendors
- **Low insertion and removal force**
  - State-of-the-art connector allows for minimum card insertion and removal effort
- **Manufactured by Berg Electronics**

GENERAL DESCRIPTION

AMD's 5.0 V-only Flash Memory PC Card provides the highest system level performance for data and file storage solutions to the portable PC market segment. Manufactured with AMD's Negative Gate Erase, 5.0 V-only technology, the AMD 5.0 V-only Flash Memory Cards are the most cost-effective and reliable approach to single-supply Flash memory cards. Data files and application programs can be stored on the AmC001BFLKA. This allows OEM manufacturers of portable systems to eliminate the weight, high-power consumption and reliability issues associated with electro-mechanical disk-based systems. The AmC001BFLKA also allows today's bulky and heavy battery packs to be reduced in weight and size. Typically only two "AA" alkaline batteries are required for total system operation. AMD's Flash Memory PC Cards provide the most efficient method to transfer useful work between different hardware platforms. The enabling technology of the AmC001BFLKA enhances the productivity of mobile workers.

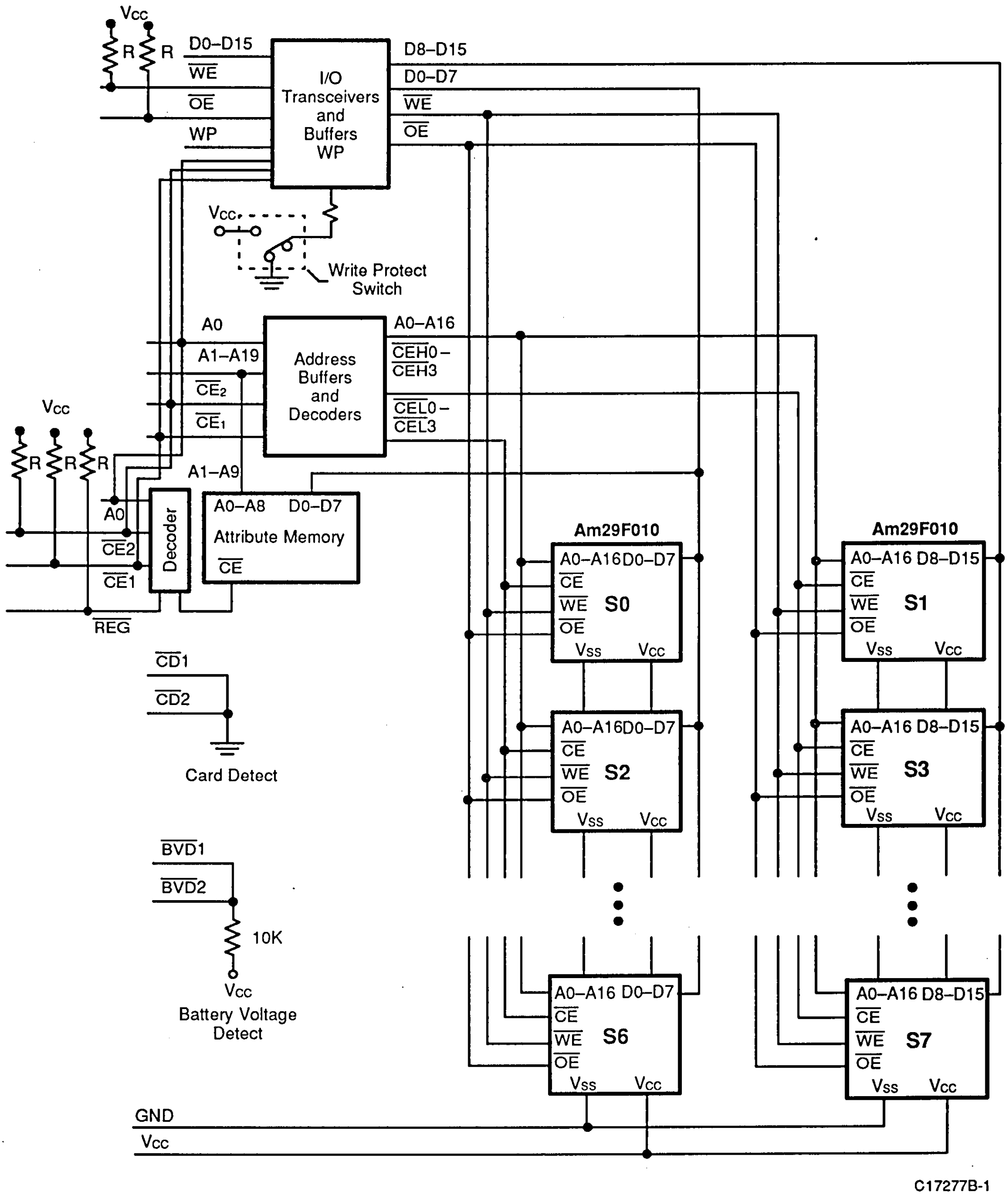
Widespread acceptance of the AmC001BFLKA is assured due to its compatibility with the 68-pin PCMCIA/JEIDA international standard. AMD's Flash Memory Cards can be read in either a byte-wide or word-wide mode which allows for flexible integration into various system platforms. Compatibility is assured at the hardware interface and software interchange specification. The Card Information Structure (CIS) or Metaformat, can be written by the OEM at the memory card's attribute memory address space beginning at address 00000H by using a format utility. The CIS appears at the beginning of the Card's attribute memory space and defines the low-level organization of data on the PC Card. The AmC001BFLKA contains a separate 512 byte EEPROM memory for the card's attribute memory space. This allows all of the Flash memory to be used for the common memory space.

Third party software solutions such as Microsoft's Flash File System (FFS), enable AMD's Flash Memory PC Card to replicate the function of traditional disk-based memory systems.

Manufactured by Berg Electronics BERG

Publication# C17277 Rev. B Amendment/0
Issue Date: March 1994

BLOCK DIAGRAM



R = 33K

PC CARD PIN ASSIGNMENTS

Pin#	Signal	I/O	Function	Pin#	Signal	I/O	Function
1	GND		Ground	35	GND		Ground
2	D3	I/O	Data Bit 3	36	$\overline{CD1}$	O	Card Detect (Note 3)
3	D4	I/O	Data Bit 4	37	D11	I/O	Data Bit 11
4	D5	I/O	Data Bit 5	38	D12	I/O	Data Bit 12
5	D6	I/O	Data Bit 6	39	D13	I/O	Data Bit 13
6	D7	I/O	Data Bit 7	40	D14	I/O	Data Bit 14
7	$\overline{CE1}$	I	Card Enable (Note 3)	41	D15	I/O	Data Bit 15
8	A10	I	Address Bit 10	42	$\overline{CE2}$	I	Card Enable 2 (Note 3)
9	$\overline{OE}$	I	Output Enable	43	NC		No Connect
10	A11	I	Address Bit 11	44	RFU		Reserved
11	A9	I	Address Bit 9	45	RFU		Reserved
12	A8	I	Address Bit 8	46	A17	I	Address Bit 17
13	A13	I	Address Bit 13	47	A18	I	Address Bit 18
14	A14	I	Address Bit 14	48	A19	I	Address Bit 19
15	$\overline{WE}$	I	Write Enable	49	A20		Address Bit 20
16	NC		No Connect	50	NC		No Connect
17	V_{CC1}		Power Supply	51	V_{CC2}		Power Supply
18	NC		No Connect (Note 1)	52	NC		No Connect (Note 1)
19	A16	I	Address Bit 16	53	NC		No Connect
20	A15	I	Address Bit 15	54	NC		No Connect
21	A12	I	Address Bit 12	55	NC		No Connect
22	A7	I	Address Bit 7	56	NC		No Connect
23	A6	I	Address Bit 6	57	NC		No Connect
24	A5	I	Address Bit 5	58	NC		No Connect
25	A4	I	Address Bit 4	59	NC		No Connect
26	A3	I	Address Bit 3	60	NC		No Connect
27	A2	I	Address Bit 2	61	$\overline{REG}$	I	Register Select
28	A1	I	Address Bit 1	62	$\overline{BVD2}$	O	Battery Vltg Detect 2 (Note 2)
29	A0	I	Address Bit 0	63	$\overline{BVD1}$	O	Battery Vltg Detect 1 (Note 2)
30	D0	I/O	Data Bit 0	64	D8	I/O	Data Bit 8
31	D1	I/O	Data Bit 1	65	D9	I/O	Data Bit 9
32	D2	I/O	Data Bit 2	66	D10	I/O	Data Bit 10
33	WP	O	Write Protect (Note 3)	67	$\overline{CD2}$	O	Card Detect (Note 3)
34	GND		Ground	68	GND		Ground

Notes:

I = Input to card, O = Output from card

I/O = Bi-directional

NC = No connect

In systems which switch V_{CC} individually to cards, no signal should be directly connected between cards other than ground.

1. *V_{PP} not required for Programming or Reading operations.*
2. *$\overline{BVD}$ = Internally pulled-up*
3. *Signal must not be connected between cards.*

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

AM C 001 B FL K A -200 CSxxxxx

- **CSxxxxx** — CUSTOMER SPECIFIC IDENTIFICATION NUMBER
- **-200** — SPEED OPTION
- **A** — REVISION LEVEL
- **K** — OUTPUT CONFIGURATION: (x16/x8)
- **FL** — FLASH TECHNOLOGY
- **B** — 5.0 V-ONLY OPERATION WITH 100,000 ERASE/PROGRAM CYCLES MINIMUM
- **001** — MEMORY CARD DENSITY
  001 = One Megabyte
- **C** — PC MEMORY CARD
- **AM** — AMD

CONDENSED

AmC002BFLKA

2 Megabyte 5.0 Volt-only Flash Memory PC Card

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - — 200 ns maximum access time
- **Single supply operation**
  - — Write and erase voltage, 5.0 V ± 5%
  - — Read voltage, 5.0 V ± 5%
- **CMOS low power consumption**
  - — 31 mA maximum active read current (x8 mode)
  - — 1.75 mA maximum standby current
- **High write endurance**
  - — Minimum 100,000 erase/write cycles
- **PCMCIA/JEIDA 68-pin standard**
  - — Selectable byte or word-wide configuration
- **Write protect switch**
  - — Prevents accidental data loss
- **Zero data retention power**
  - — Batteries not required for data storage
- **Separate attribute memory**
  - — 512 byte EEPROM
- **Automated write and erase operations increase system write performance**
  - — 128 x 16K byte memory sectors for faster automated erase speed
  - — Typically 1.3 seconds per single memory sector erase
  - — Random address writes to previously erased bytes (14 µs typical per byte)
- **Total system integration solution**
  - — Support from independent software and hardware vendors
- **Low insertion and removal force**
  - — State-of-the-art connector allows for minimum card insertion and removal effort
- **Manufactured by Berg Electronics**

GENERAL DESCRIPTION

AMD's 5.0 V-only Flash Memory PC Card provides the highest system level performance for data and file storage solutions to the portable PC market segment. Manufactured with AMD's Negative Gate Erase, 5.0 V-only technology, the AMD 5.0 V-only Flash Memory Cards are the most cost-effective and reliable approach to single-supply Flash memory cards. Data files and application programs can be stored on the AmC002BFLKA. This allows OEM manufacturers of portable systems to eliminate the weight, high-power consumption and reliability issues associated with electro-mechanical disk-based systems. The AmC002BFLKA also allows today's bulky and heavy battery packs to be reduced in weight and size. Typically only two "AA" alkaline batteries are required for total system operation. AMD's Flash Memory PC Cards provide the most efficient method to transfer useful work between different hardware platforms. The enabling technology of the AmC002BFLKA enhances the productivity of mobile workers.

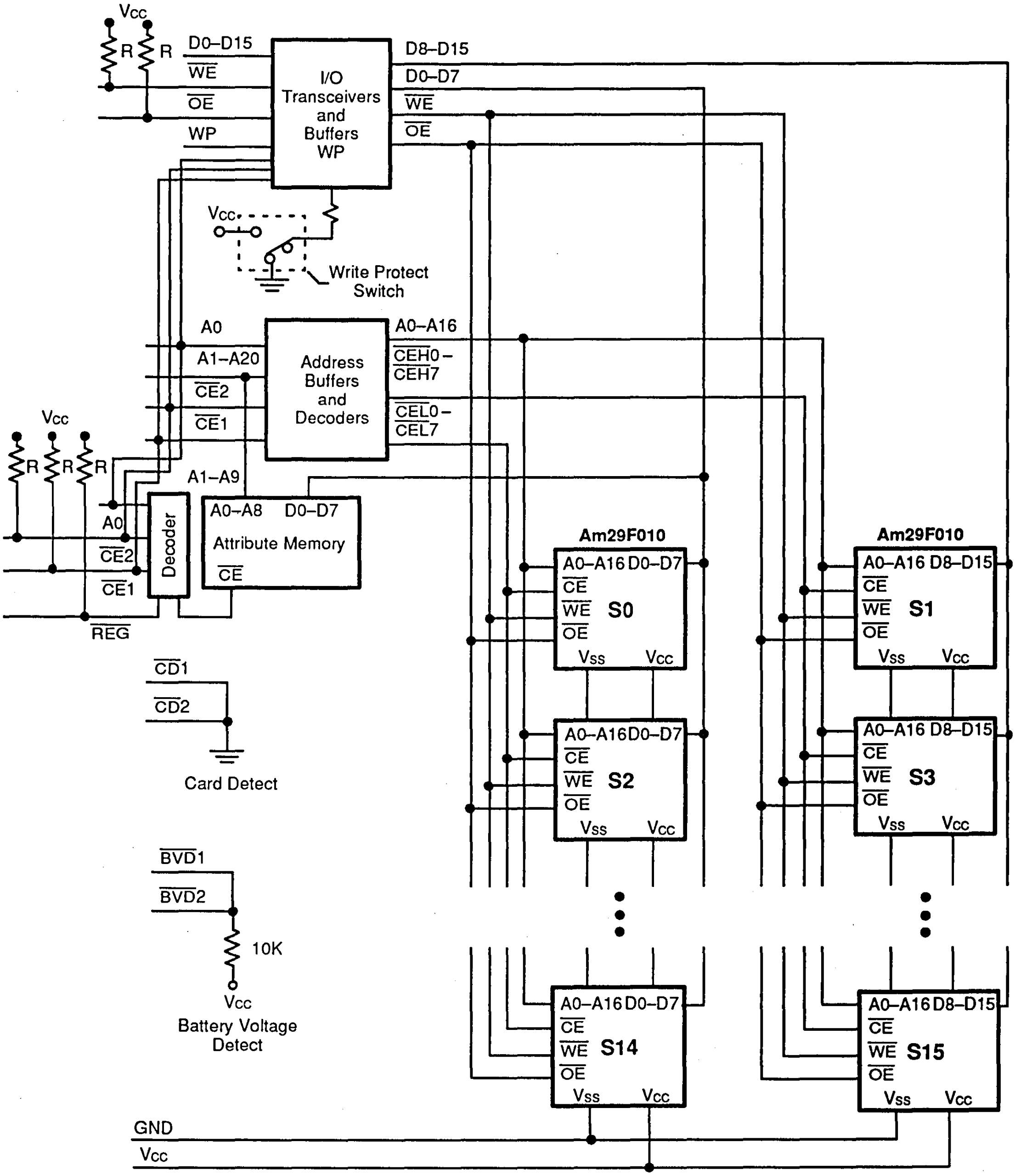
Widespread acceptance of the AmC002BFLKA is assured due to its compatibility with the 68-pin PCMCIA/JEIDA international standard. AMD's Flash Memory Cards can be read in either a byte-wide or word-wide mode which allows for flexible integration into various system platforms. Compatibility is assured at the hardware interface and software interchange specification. The Card Information Structure (CIS) or Metaformat, can be written by the OEM at the memory card's attribute memory address space beginning at address 00000H by using a format utility. The CIS appears at the beginning of the Card's attribute memory space and defines the low-level organization of data on the PC Card. The AmC002BFLKA contains a separate 512 byte EEPROM memory for the card's attribute memory space. This allows all of the Flash memory to be used for the common memory space.

Third party software solutions such as Microsoft's Flash File System (FFS), enable AMD's Flash Memory PC Card to replicate the function of traditional disk-based memory systems.

Manufactured by Berg Electronics BERG

Publication# C17278 Rev. B Amendment/0
Issue Date: March 1994

BLOCK DIAGRAM



R = 33K

17278B-1

PC CARD PIN ASSIGNMENTS

Pin#	Signal	I/O	Function	Pin#	Signal	I/O	Function
1	GND		Ground	35	GND		Ground
2	D3	I/O	Data Bit 3	36	$\overline{CD}$1	O	Card Detect (Note 3)
3	D4	I/O	Data Bit 4	37	D11	I/O	Data Bit 11
4	D5	I/O	Data Bit 5	38	D12	I/O	Data Bit 12
5	D6	I/O	Data Bit 6	39	D13	I/O	Data Bit 13
6	D7	I/O	Data Bit 7	40	D14	I/O	Data Bit 14
7	$\overline{CE}$1	I	Card Enable (Note 3)	41	D15	I/O	Data Bit 15
8	A10	I	Address Bit 10	42	$\overline{CE}$2	I	Card Enable 2 (Note 3)
9	$\overline{OE}$	I	Output Enable	43	NC		No Connect
10	A11	I	Address Bit 11	44	NC		No Connect
11	A9	I	Address Bit 9	45	NC		No Connect
12	A8	I	Address Bit 8	46	A17	I	Address Bit 17
13	A13	I	Address Bit 13	47	A18	I	Address Bit 18
14	A14	I	Address Bit 14	48	A19	I	Address Bit 19
15	$\overline{WE}$	I	Write Enable	49	A20		Address Bit 20
16	NC		No Connect	50	NC		No Connect
17	V_{CC1}		Power Supply	51	V_{CC2}		Power Supply
18	NC		No Connect (Note 1)	52	NC		No Connect (Note 1)
19	A16	I	Address Bit 16	53	NC		No Connect
20	A15	I	Address Bit 15	54	NC		No Connect
21	A12	I	Address Bit 12	55	NC		No Connect
22	A7	I	Address Bit 7	56	NC		No Connect
23	A6	I	Address Bit 6	57	NC		No Connect
24	A5	I	Address Bit 5	58	NC		No Connect
25	A4	I	Address Bit 4	59	NC		No Connect
26	A3	I	Address Bit 3	60	NC		No Connect
27	A2	I	Address Bit 2	61	$\overline{REG}$	I	Register Select
28	A1	I	Address Bit 1	62	$\overline{BVD}$2	O	Battery Vltg Detect 2 (Note 2)
29	A0	I	Address Bit 0	63	$\overline{BVD}$1	O	Battery Vltg Detect 1 (Note 2)
30	D0	I/O	Data Bit 0	64	D8	I/O	Data Bit 8
31	D1	I/O	Data Bit 1	65	D9	I/O	Data Bit 9
32	D2	I/O	Data Bit 2	66	D10	I/O	Data Bit 10
33	WP	O	Write Protect (Note 3)	67	$\overline{CD}$2	O	Card Detect (Note 3)
34	GND		Ground	68	GND		Ground

Notes:

I = Input to card, O = Output from card

I/O = Bi-directional

NC = No connect

In systems which switch V_{CC} individually to cards, no signal should be directly connected between cards other than ground.

1. *V_{PP} not required for Programming or Reading operations.*
2. *$\overline{BVD}$ = Internally pulled-up*
3. *Signal must not be connected between cards.*

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

AM C 002 B FL K A -200 CSxxxxx

- **CSxxxxx** — **CUSTOMER SPECIFIC IDENTIFICATION NUMBER**
- **-200** — **SPEED OPTION**
- **A** — **REVISION LEVEL**
- **K** — **OUTPUT CONFIGURATION:** (x16/x8)
- **FL** — **FLASH TECHNOLOGY**
- **B** — **5.0 V-ONLY OPERATION WITH 100,000 ERASE/PROGRAM CYCLES MINIMUM**
- **002** — **MEMORY CARD DENSITY**
  001 = One Megabyte
  002 = Two Megabyte
- **C** — **PC MEMORY CARD**
- **AM** — **AMD**

CONDENSED

AmC0XXCFLKA

1, 2, 4, or 10 Megabyte 5.0 Volt-only Flash Memory PC Card

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **High performance**
  - 150 ns maximum access time
- **Single supply operation**
  - Write and erase voltage, 5.0 V ± 5%
  - Read voltage, 5.0 V ± 5%
- **CMOS low power consumption**
  - 40 mA maximum active read current (x8 mode)
  - 60 mA maximum active erase/write current (x8 mode)
- **High write endurance**
  - Minimum 100,000 erase/write cycles
- **PCMCIA/JEIDA 68-pin standard**
  - Selectable byte or word-wide configuration
- **Write protect switch**
  - Prevents accidental data loss
- **Zero data retention power**
  - Batteries not required for data storage
- **Separate attribute memory**
  - 512 byte EEPROM
- **Automated write and erase operations increase system write performance**
  - 64K byte memory sectors for faster automated erase speed
  - Typically 1.5 seconds per single memory sector erase
  - Random address writes to previously erased bytes (16 µs typical per byte)
- **Total system integration solution**
  - Support from independent software and hardware vendors
- **Low insertion and removal force**
  - State-of-the-art connector allows for minimum card insertion and removal effort
- **Sector erase suspend/resume**
  - Suspend the erase operation to allow a read operation in another sector within the same device
- **Manufactured by Berg Electronics**

GENERAL DESCRIPTION

AMD's 5.0 V-only Flash Memory PC Card provides the highest system level performance for data and file storage solutions to the portable PC market segment. Manufactured with AMD's Negative Gate Erase, 5.0 V-only technology, the AMD 5.0 V-only Flash Memory Cards are the most cost-effective and reliable approach to single-supply Flash memory cards. Data files and application programs can be stored on the "C" series card. This allows OEM manufacturers of portable systems to eliminate the weight, high-power consumption and reliability issues associated with electro-mechanical disk-based systems. The "C" series card also allows today's bulky and heavy battery packs to be reduced in weight and size. Typically only two "AA" alkaline batteries are required for total system operation. AMD's Flash Memory PC Cards provide the most efficient method to transfer useful work between different hardware platforms. The enabling technology of the "C" series card enhances the productivity of mobile workers.

Widespread acceptance of the "C" series card is assured due to its compatibility with the 68-pin PCMCIA/JEIDA international standard. AMD's Flash Memory Cards can be read in either a byte-wide or word-wide mode which allows for flexible integration into various system platforms. Compatibility is assured at the hardware interface and software interchange specification. The Card Information Structure (CIS) or Metaformat, can be written by the OEM at the memory card's attribute memory address space beginning at address 00000H by using a format utility. The CIS appears at the beginning of the Card's attribute memory space and defines the low-level organization of data on the PC Card. The "C" series card contains a separate 512 byte EEPROM memory for the card's attribute memory space. This allows all of the Flash memory to be used for the common memory space.

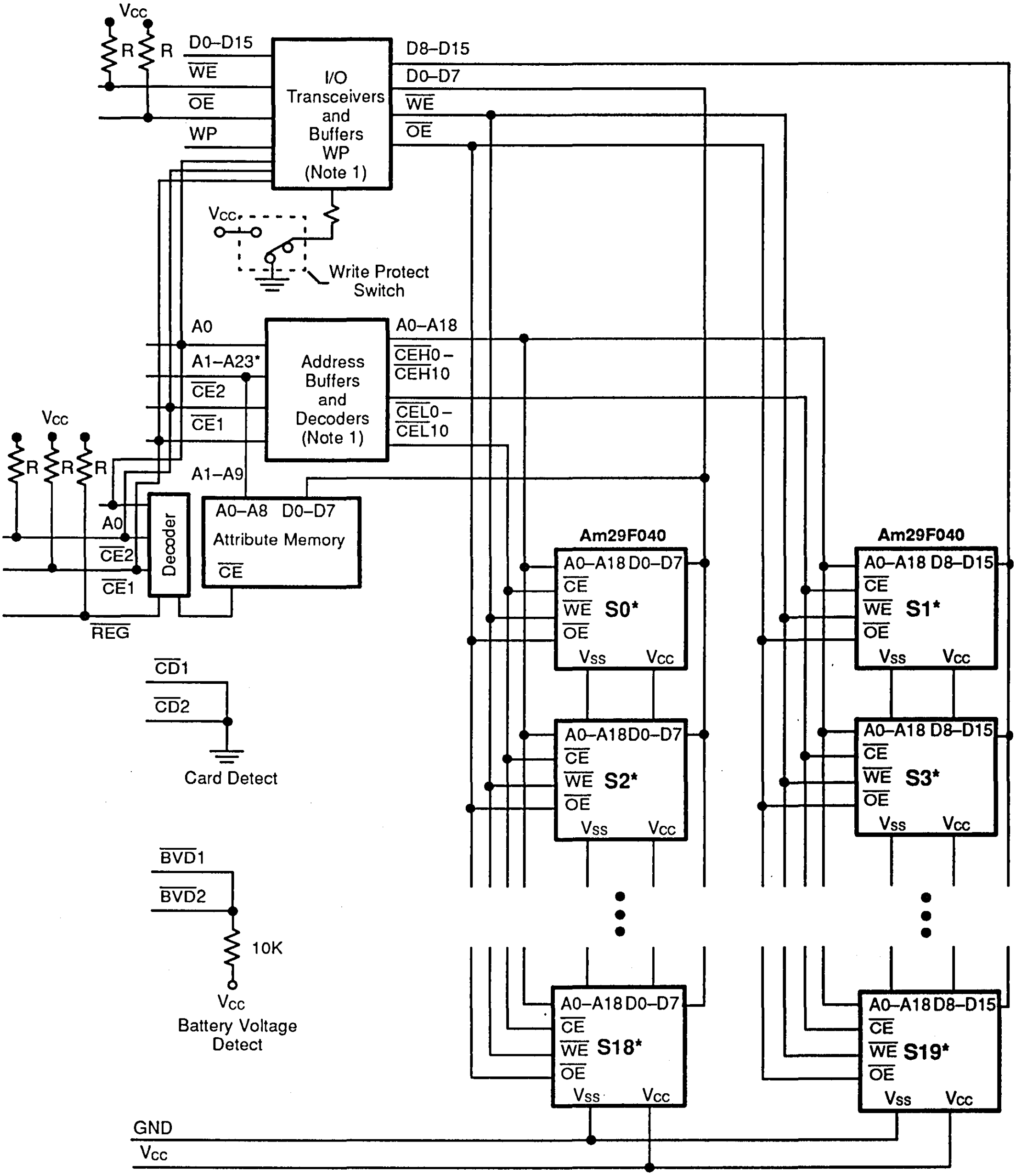
Third party software solutions such as Microsoft's Flash File System (FFS), M-System's True FFS, and SCM's SCM-FFS, enable AMD's Flash Memory PC Card to replicate the function of traditional disk-based memory systems.

Manufactured by Berg Electronics BERG

Publication# C18723 Rev. A Amendment/0
Issue Date: March 1994

This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

BLOCK DIAGRAM



R = 20 K(min)/140K Ω (max)

**1 Mbyte card = S0 + S1*

**2 Mbyte card = S0....S3*

**4 Mbyte card = S0....S7*

**10 Mbyte card = S0....S19*

Note:

1. *The function of these two blocks are combined in one ASIC.*

C18723A-1

PC CARD PIN ASSIGNMENTS

Pin#	Signal	I/O	Function	Pin#	Signal	I/O	Function
1	GND		Ground	35	GND		Ground
2	D3	I/O	Data Bit 3	36	$\overline{CD}1$	O	Card Detect (Note 3)
3	D4	I/O	Data Bit 4	37	D11	I/O	Data Bit 11
4	D5	I/O	Data Bit 5	38	D12	I/O	Data Bit 12
5	D6	I/O	Data Bit 6	39	D13	I/O	Data Bit 13
6	D7	I/O	Data Bit 7	40	D14	I/O	Data Bit 14
7	$\overline{CE}1$	I	Card Enable (Note 3)	41	D15	I/O	Data Bit 15
8	A10	I	Address Bit 10	42	$\overline{CE}2$	I	Card Enable 2 (Note 3)
9	$\overline{OE}$	I	Output Enable	43	NC		No Connect
10	A11	I	Address Bit 11	44	NC		No Connect
11	A9	I	Address Bit 9	45	NC		No Connect
12	A8	I	Address Bit 8	46	A17	I	Address Bit 17
13	A13	I	Address Bit 13	47	A18	I	Address Bit 18
14	A14	I	Address Bit 14	48	A19	I	Address Bit 19 (Note 4)
15	$\overline{WE}$	I	Write Enable	49	A20		Address Bit 20 (Note 5)
16	NC		No Connect	50	A21		Address Bit 21 (Note 6)
17	V_{CC1}		Power Supply	51	V_{CC2}		Power Supply
18	NC		No Connect (Note 1)	52	NC		No Connect (Note 1)
19	A16	I	Address Bit 16	53	A22		Address Bit 22
20	A15	I	Address Bit 15	54	A23		Address Bit 23 (Note 7)
21	A12	I	Address Bit 12	55	NC		No Connect
22	A7	I	Address Bit 7	56	NC		No Connect
23	A6	I	Address Bit 6	57	NC		No Connect
24	A5	I	Address Bit 5	58	NC		No Connect
25	A4	I	Address Bit 4	59	NC		No Connect
26	A3	I	Address Bit 3	60	NC		No Connect
27	A2	I	Address Bit 2	61	$\overline{REG}$	I	Register Select
28	A1	I	Address Bit 1	62	$\overline{BVD}2$	O	Battery Vltg Detect 2 (Note 2)
29	A0	I	Address Bit 0	63	$\overline{BVD}1$	O	Battery Vltg Detect 1 (Note 2)
30	D0	I/O	Data Bit 0	64	D8	I/O	Data Bit 8
31	D1	I/O	Data Bit 1	65	D9	I/O	Data Bit 9
32	D2	I/O	Data Bit 2	66	D10	I/O	Data Bit 10
33	WP	O	Write Protect (Note 3)	67	$\overline{CD}2$	O	Card Detect (Note 3)
34	GND		Ground	68	GND		Ground

Notes:

I = Input to card, O = Output from card

I/O = Bi-directional

NC = No connect

In systems which switch V_{CC} individually to cards, no signal should be directly connected between cards other than ground.

1. *V_{PP} not required for Programming or Reading operations.*
2. *$\overline{BVD}$ = Internally pulled-up*
3. *Signal must not be connected between cards.*
4. *Highest address bit for 1 Mbyte card.*
5. *Highest address bit for 2 Mbyte card.*
6. *Highest address bit for 4 Mbyte card.*
7. *Highest address bit for 10 Mbyte card.*

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

AM C 0XX C FL K A -150 CSxxxxx

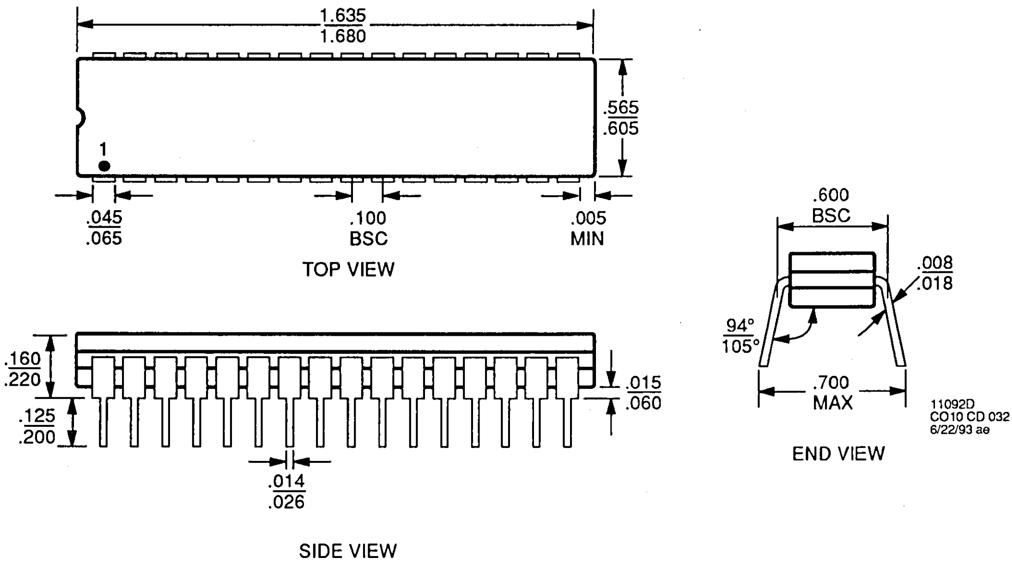
- CSxxxxx — **CUSTOMER SPECIFIC IDENTIFICATION NUMBER**
- -150 — **SPEED OPTION**
- A — **REVISION LEVEL**
- K — **OUTPUT CONFIGURATION:** (x16/x8)
- FL — **FLASH TECHNOLOGY**
- C — **5.0 V-ONLY OPERATION WITH 100,000 ERASE/PROGRAM CYCLES MINIMUM**
- 0XX — **MEMORY CARD DENSITY**
  - 001 = One Megabyte
  - 002 = Two Megabyte
  - 004 = Four Megabyte
  - 010 = Ten Megabyte
- C — **PC MEMORY CARD**
- AM — **AMD**

SECTION

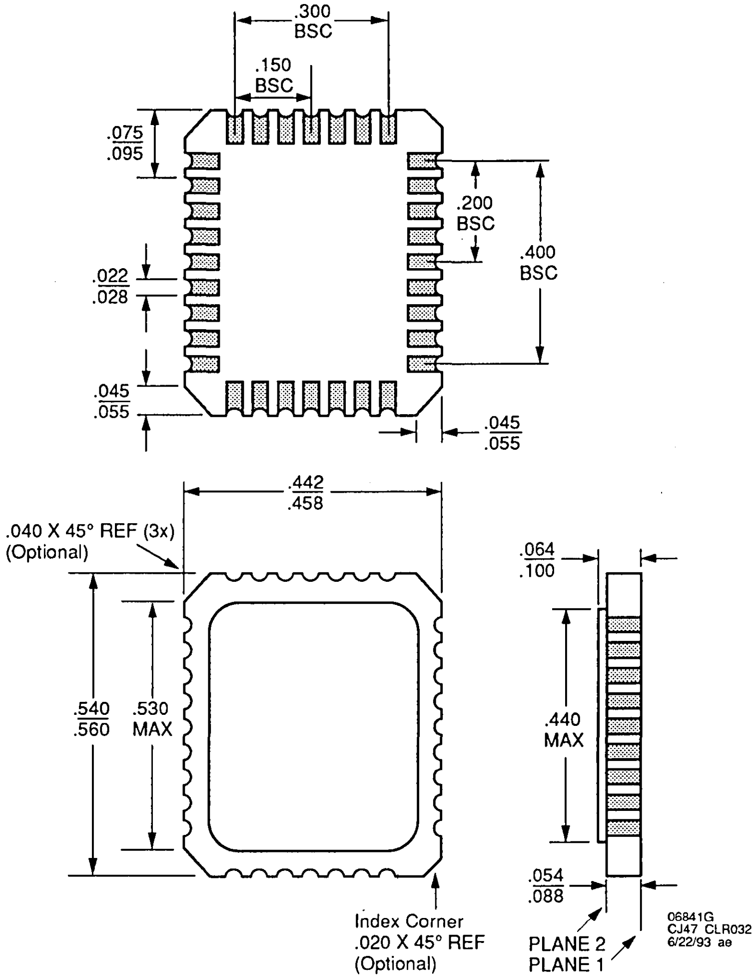
6 PHYSICAL DIMENSIONS*

For reference only. BSC is an ANSI standard for Basic Space Centering.

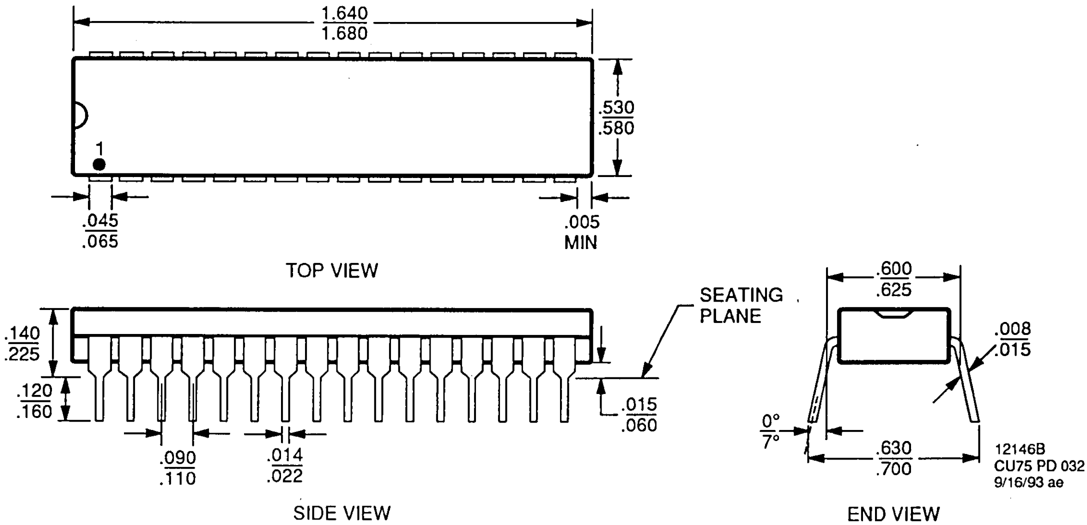
CD 032
32-Pin Ceramic DIP (measured in inches)



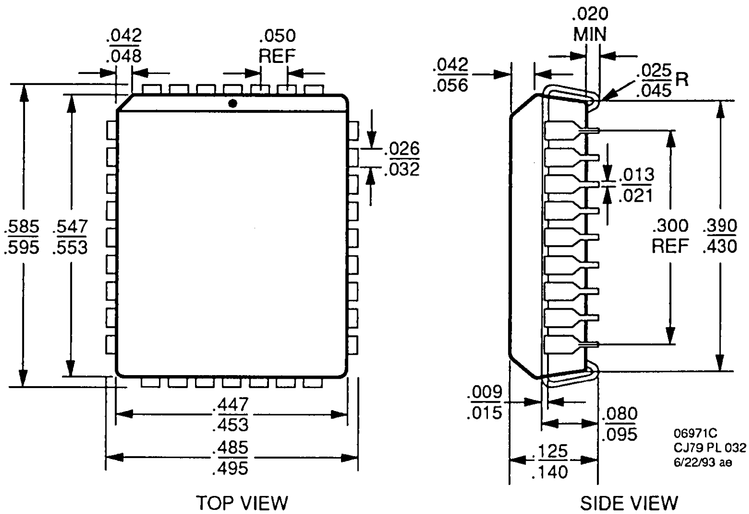
CLR 032
32-Pin Rectangular Ceramic Leadless Chip Carrier (measured in inches)



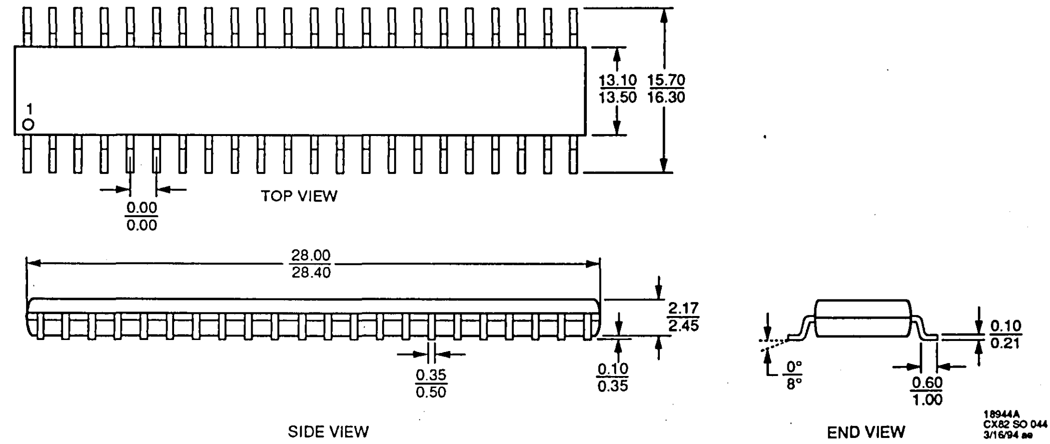
PD 032
32-Pin Plastic DIP (measured in inches)



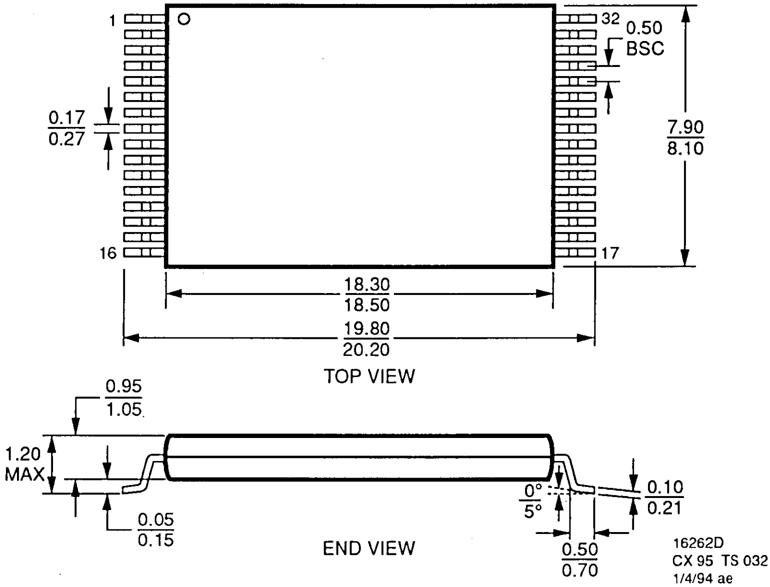
PL 032
32-Pin Plastic Leaded Chip Carrier (measured in inches)



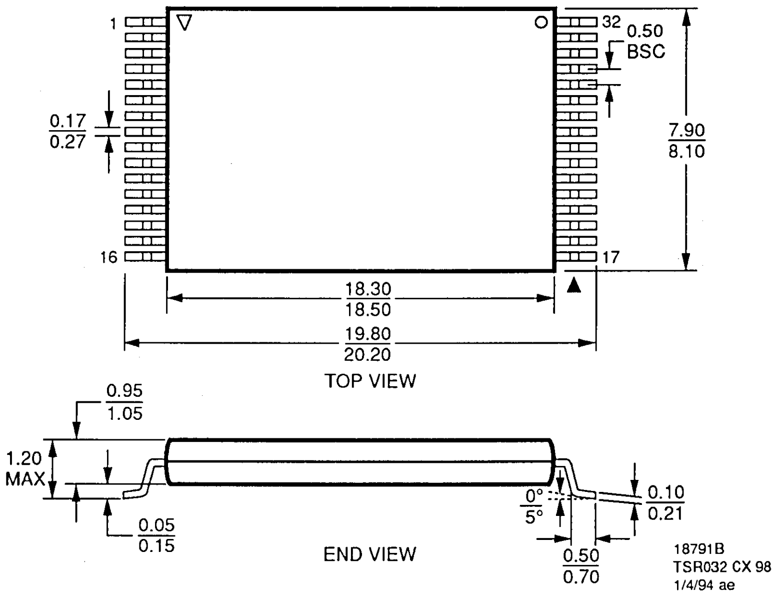
SO 044
44-Pin Small Outline Package (measured in millimeters)



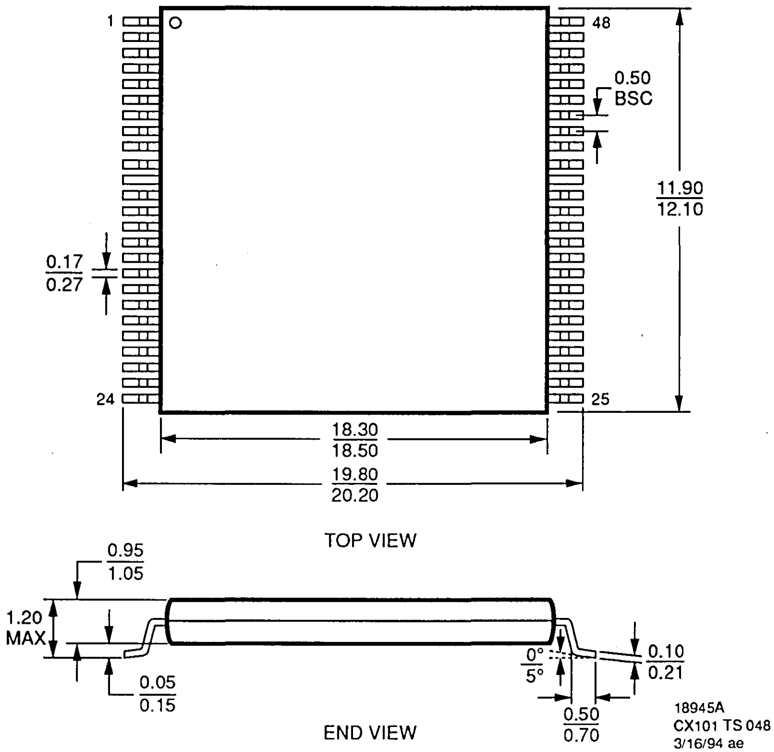
TS 032
32-Pin Standard Thin Small Outline Package (measured in millimeters)



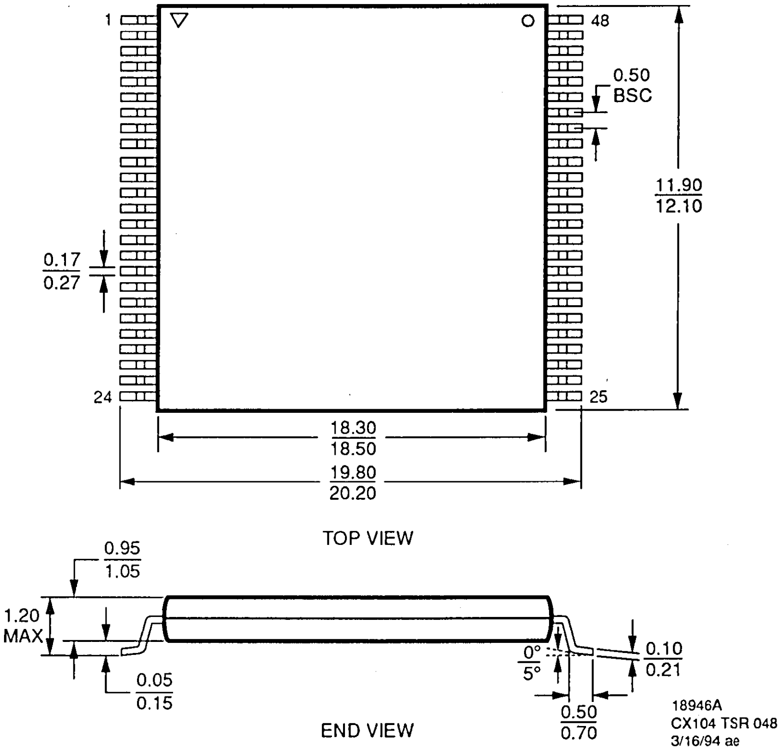
TSR 032
32-Pin Reversed Thin Small Outline Package (measured in millimeters)



TS 048
48-Pin Standard Thin Small Outline Package (measured in millimeters)



TSR 048
48-Pin Reversed Thin Small Outline Package (measured in millimeters)



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