

Disk Control Products Specification Booklet

Advanced Micro Devices

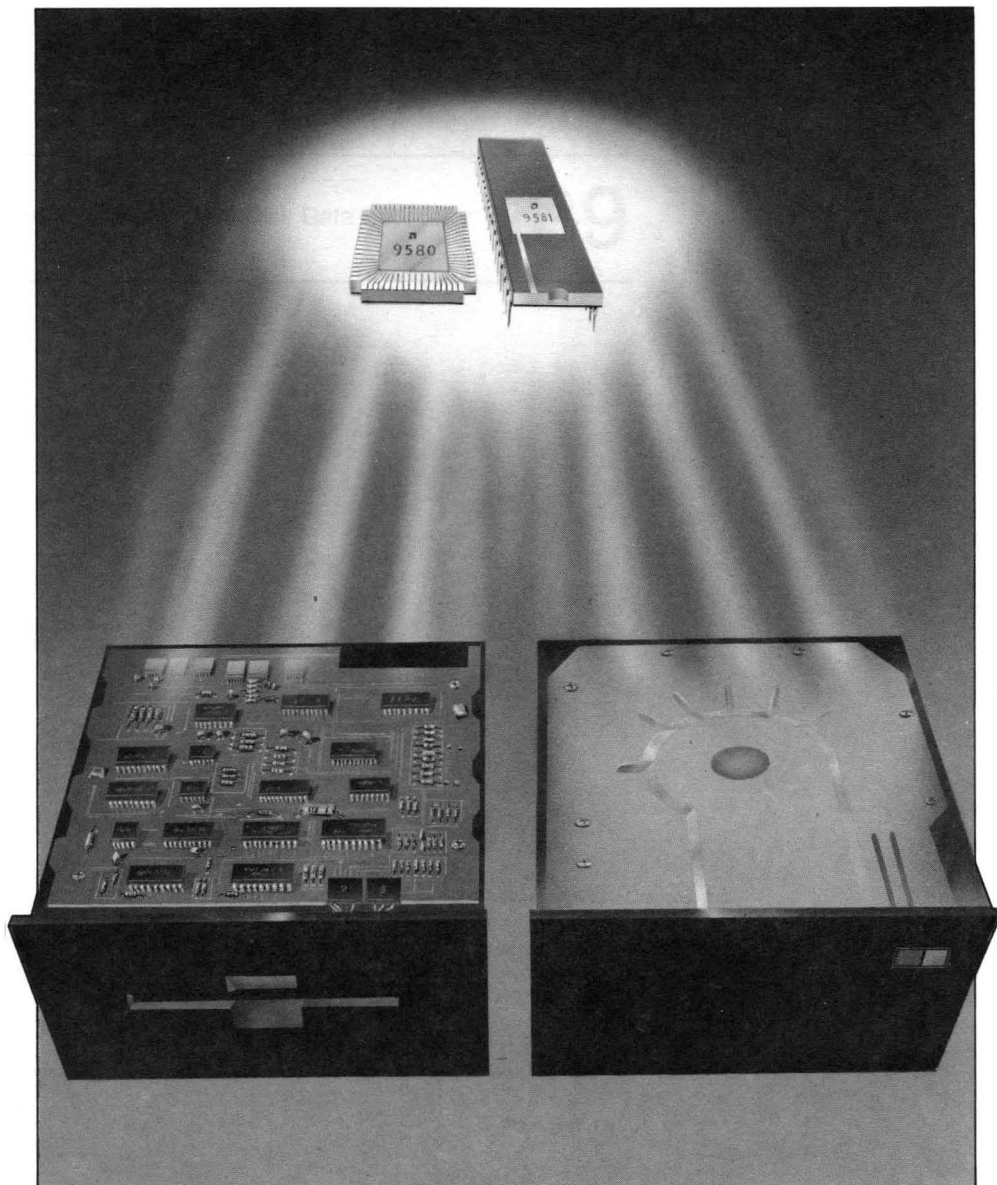




Table of Contents

Am9580 Hard Disk Controller (HDC)

1

Am9581 Floppy/Hard Disk Data Separator

39

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Am9580

Hard Disk Controller (HDC)

ADVANCED INFORMATION



Am9580

Advanced Micro Devices

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DISTINCTIVE CHARACTERISTICS

- Linked list command and data structure
- Controls up to 4 drives, any combination of hard or floppy disk drives
- ST506/412 and user defined disk interface options supported
- Two on-chip sector buffers are programmable for sector sizes of 128, 256, and 512 bytes
- Error checking algorithms supported include
 - CRC/CCITT
 - Single burst Reed-Solomon
 - Double burst Reed-Solomon
 - External ECC (Error Correcting Code)
- On-chip DMA capability supports 32-bit addressing in 8/16-bit systems

GENERAL DESCRIPTION

The Am9580 Hard Disk Controller (HDC) is a single chip solution to the problems encountered in designing Data Formatters and Disk System Controllers. Together with its companion part, the Am9581 Disk Data Separator (DDS), the Am9580 provides all the functions which until now have been found only on sophisticated board-level products.

The Am9580 has been designed with the necessary flexibility to cope with the differing requirements of today's broad marketplace while still retaining the advanced technology and innovative features that tomorrow's market will demand.

The Am9580 supports both Rigid and Flexible Disk Drives and their accompanying Data Formats. The Am9580 can control up to four drives, allowing any mix of Rigid and Flexible drives. As the characteristics of each drive are independently user-programmable, the system designer is provided with the flexibility needed to control any disk drive.

A sophisticated on-chip DMA Controller fetches the commands, writes status information, fetches data to be written on disk and writes data read from disk. The DMA operation is programmable to adjust the bus occupancy, data bus width (8-bit or 16-bit), and wait state insertion. Two sector buffers allow zero sector interleaving to access data on physically contiguous sectors, improving both file access

time and system throughput. The buffers are programmable for sector sizes of 128, 256, and 512 bytes.

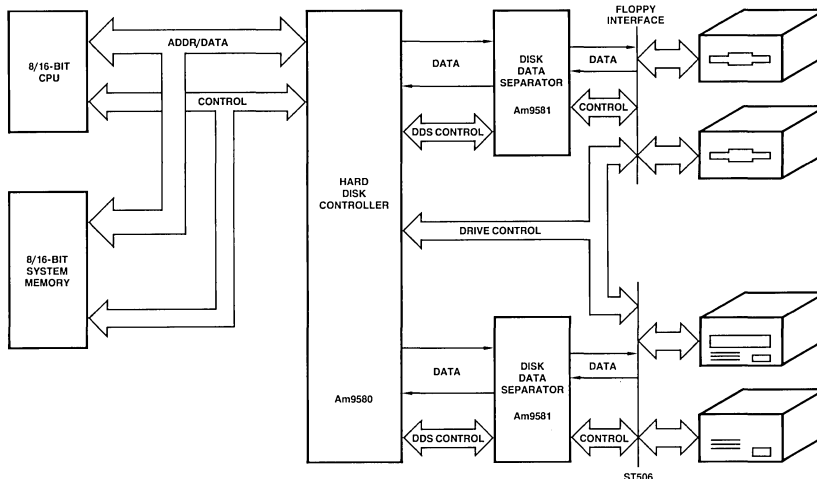
The Am9580 insures data integrity by selecting one error detecting code (CRC-CCITT), or one of two error correcting codes (single and double burst Reed-Solomon). Additionally, the HDC provides handshake signals to control external ECC circuitry to implement any ECC algorithm.

The Am9580 provides signals which are necessary to control external Encode/Decode and Address Mark circuitry such as found on the Am9581. By partitioning the Disk Control System in this way, future developments in the field of Data Encoding can still take advantage of the HDC's advanced Data Formatting and Control capabilities.

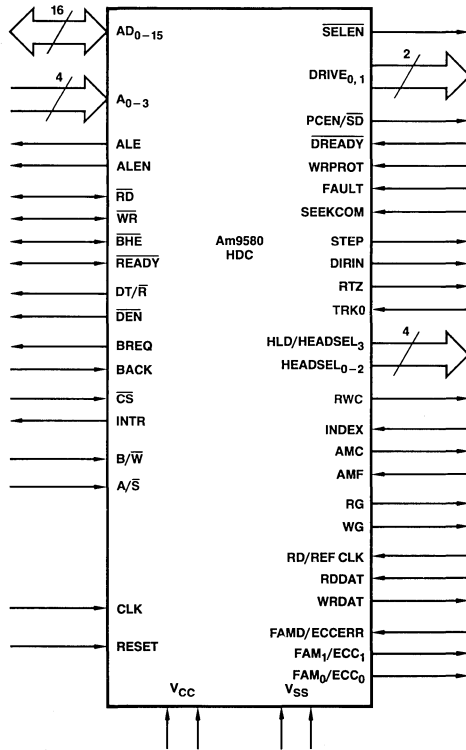
The flexible, user programmable disk interface can be configured to control ST506 or standard Floppy Disk interfaces with only a few buffers required and can easily be adapted to other interface standards.

The Am9580 provides a comprehensive, high level command set for multi-sector disk I/O, marginal data recovery, diagnostics and error recovery. Commands may be linked together to be executed sequentially by the Am9580 without any host intervention. This linked list command structure also simplifies command insertion, deletion, or rearrangement.

Figure 1. Disk Controller System



HDC Logic Symbol



05308A-26

HDC Connection Diagram
(not yet available)

FUNCTIONAL OVERVIEW

HARDWARE ARCHITECTURE

The HDC supports two interfaces as shown in the block diagram in Figure 2; the system interface communicates with the host CPU and system memory, and the disk interface controls the data separator and the disk drives.

System Interface

The HDC is designed for easy interfacing to most 8-bit or 16-bit, multiplexed or demultiplexed, synchronous or asynchronous microprocessor buses. A strap pin programs the system interface for either byte (8-bit) or word (16-bit) mode. In Slave Mode, the host CPU can access the internal registers of the HDC. In Master Mode, the on-chip DMA controller controls the system bus.

DMA Controller

The on-chip DMA controller provides the HDC with the ability to execute complex disk I/O operations without intervention by the host CPU. The DMA controller scans the command chain stored in system memory, updates the Status Result Area when errors occur, and transfers the data between the internal sector buffers and system memory. Data may optionally be stored in noncontiguous memory to support linked-list data storage in word processing systems.

The DMA controller generates 32-bit linear addresses to access system memory of up to 4 GBytes directly. For multiple bus master systems, the DMA transfers can be throttled to dedicate only a certain share of the system bus bandwidth to the HDC. The Mode Register specifies the DMA burst length and dwell time. DMA bursts can be preempted by removing Bus Acknowledge (BACK). The HDC can insert a programmable number of software Wait States into DMA bus cycles. Additionally, hardware Wait States can be added via the **READY** input. The HDC updates the upper address word (A_{16} to A_{31}) when a carry out of the lower 16 bits indicates it is necessary.

User Registers

The Mode Register defines the operation of the DMA controller. The Status/Command Register controls the basic operation of the HDC itself. The Next Block Pointer (NBP) Register links to the first Input/Output Parameter Block (IOPB) of the command chain. The Status Result Pointer Register and the Status Result Length Register define the Status Result Area.

Main Sequencer

The main sequencer translates the high-level system commands into the control signals for the various independent functional sections of the HDC. The power of this 16-bit processor is used to ease the complex data manipulation burden of the system CPU.

Drive Parameter RAMs

The Drive Parameter RAMs store the specification parameters for individual drives that adapt the HDC to any combination of disk recording schemes. The contents can be altered

at any time with a single IOPB. Once loaded these parameters allow disk commands to be independent of the drive format. For example, the write command is the same whether it is for a single-density floppy disk drive or a Winchester hard disk drive.

Error Checking

The HDC features two powerful Reed-Solomon error-correcting codes, as well as the industry-standard error-detection code, CRC-CCITT. It also supports user-definable, external error-correction schemes. These, along with the programmable retry and and correction attempt policy, allow maximum control of data integrity.

Sector Buffers

The HDC transfers data to or from disk without adding time constraints on the system bus bandwidth. The two internal sector buffers can be filled or emptied at any speed without interfering with the data transfer between the sector buffers and the disk. The two internal sector buffers can be toggled for zero sector interleave disk data operations. While one sector buffer is filled with data from disk, the other buffer is emptied by the DMA controller. Physically contiguous sectors on a track can thus be read or written on the fly.

Disk Control Interface

The lines of the Disk Control Interface conform to the ST506 disk drive interface standard. Other drive interface standards can be supported with some external circuitry. The ST506 interface selects one of the four disk drives and one of up to 16 heads. Any combination of floppy disk and hard disk drives can be connected. The Drive Parameter Blocks specify the seek dwell, seek pulse width, and head settle timing.

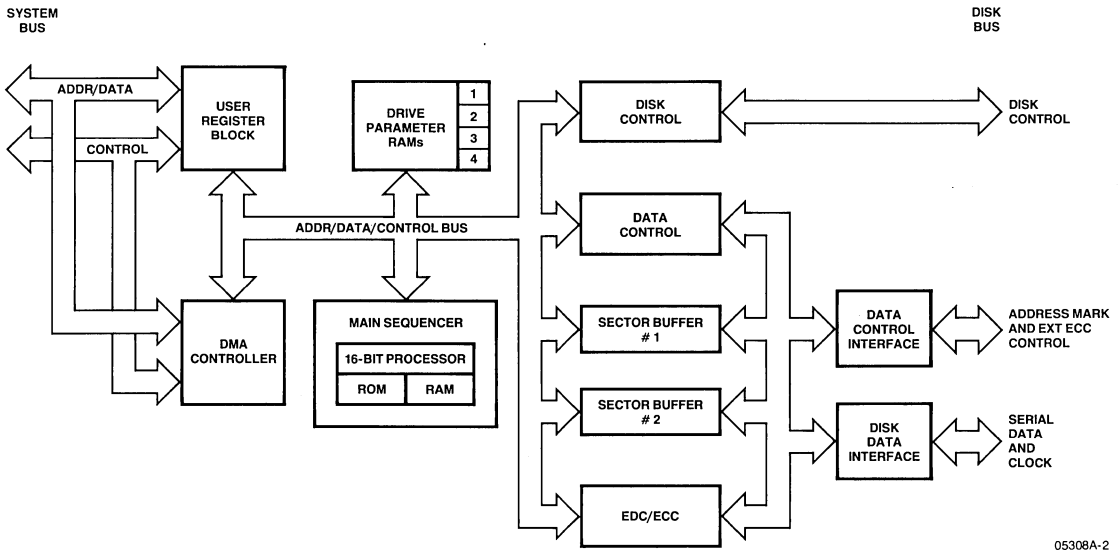
The HDC can perform implied and overlapped seeks. When the implied seek option is selected, the HDC automatically causes the appropriate seeks when issuing a read or write command. If this option is disabled, then the HDC should be issued separate seek commands before executing read or write commands.

When the overlapped seek option is selected, drives can seek in parallel, thus minimizing the seek overhead in multiple disk drive systems. After the HDC has issued a seek command to one drive and while this drive performs the seek, the HDC scans subsequent IOPBs for commands requiring seeks on other drives. If the HDC finds such commands, it issues seek commands to these drives to make them seek in parallel. On receiving a "Seek Complete" from the first drive, the HDC resumes execution of the command chain.

Disk Data Interface

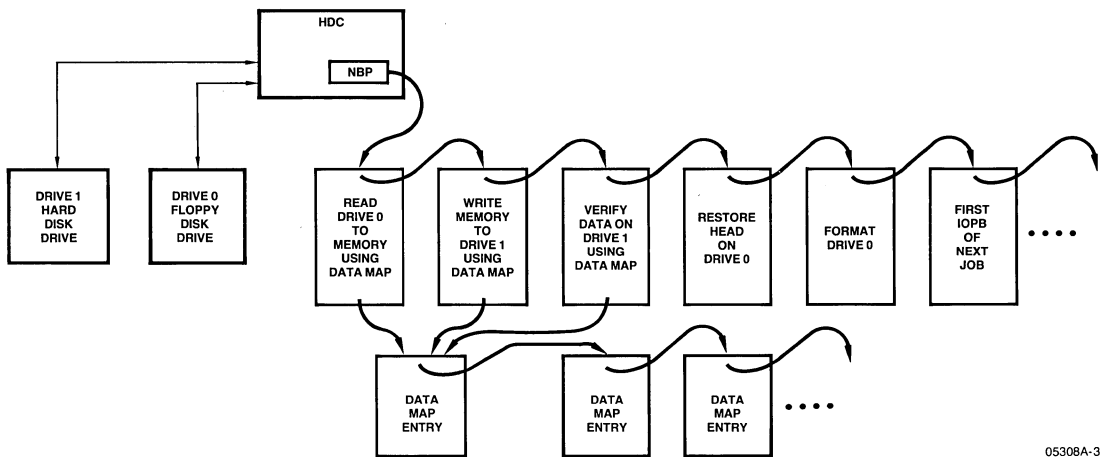
The Disk Data Interface controls the Address Mark handshake with the data separator, controls the optional external ECC logic, and handles the serial data input and output. Operating asynchronously to the other blocks of the device, the Disk Data Interface is driven by the Read/Reference Clock (RD/REF CLK) generated by the data separator. The Disk Data Interface converts the data stored in the sector

Figure 2. HDC Block Diagram



05308A-2

Figure 3. IOPB Linked-List



05308A-3

The IOPB chain in Figure 3 copies the data of a floppy disk to a hard disk, verifies the data, and, when the verification is successful, formats the floppy disk. First it reads the data from the floppy disk into a temporary buffer in system memory. The data-mapping option lets the system use any free memory space. The subsequent write command uses the same data map to transfer data to the hard disk. The verify command ensures that data was written correctly by performing a byte-by-byte comparison of the data on the hard disk with the data in the temporary buffer. Optionally, the chain execution may be stopped in the event of an error in the write or verify command. If there was no problem with the data transfer, the HDC will perform the restore and for-

mat commands. Optionally, the system can be informed that the disk copy has been completed and that the memory space allocated for the temporary buffer of the disk data is free to be reused.

The seek-lookahead mechanism of the HDC will move forward through the IOPB chain to see where it can overlap head seeks. In this example, the HDC will move the head on the hard disk into position for the write command while the read command is still executing. When the HDC starts executing the write command, it will look ahead in the chain and start executing the restore command on the floppy drive to move the head back to track zero. If possible, the HDC will do additional head positioning for commands further down the IOPB chain.

buffer into a serial bit stream for the disk or it de-serializes the incoming bit stream to be loaded into one of the sector buffers. Non-data information, such as the header, pads, gaps, preambles, and postambles, is conditioned according to the parameters stored in the Drive Parameter RAMs to meet the defined recording standard.

SOFTWARE ARCHITECTURE

IOPB Command Structure

The HDC features a high-level data and command structure. The basic unit of a command structure is the Input/Output Parameter Block (IOPB). The host CPU creates IOPBs in system memory to pass control and status information to the HDC. The HDC fetches these IOPBs using its on-chip DMA controller. Each IOPB specifies one disk command and contains all parameters needed to execute it. To start execution of an IOPB, the host CPU loads the address of the first IOPB into the Next Block Pointer Register and issues the command "Start Chain" by programming the Status/Command Register. After the IOPB is executed the HDC reports the status information and waits for further instructions. The host CPU can examine the Status/Command Register for information about the command termination. The CPU can also get status from the Status Result Block in memory if an error occurs.

Optionally, IOPBs may be connected in a linked-list format which the HDC can interpret sequentially. With this structure, a complex list of disk commands can be set up and executed by the HDC without CPU intervention. The CPU is then totally free from any processing for disk control. For example, the host CPU can set up a list of commands to copy an entire floppy disk to a hard disk, verify that the data was copied correctly, and, if so, reformat the floppy disk—all without host CPU intervention.

An IOPB command chain is basically a queue of jobs waiting for execution by the HDC. This offers a pre-defined and efficient structure for the operating system to handle its disk I/O. The ID field of the IOPB allows the operating system to link a particular disk command to the user process that made the disk request. The jobs can thus be placed in the HDC job queue and then forgotten by the operating system unless an error occurs. All the information required to retrace an error is provided by the HDC Status Result Block.

Since the HDC manages the disk job queue, it can look ahead in the queue to overlap some time-consuming operations. Head movement (seeking) can require a major portion of the disk access time. Since the HDC controls up to four drives, it can perform an IOPB operation on one drive while it is executing seeks for future IOPBs on the other drives. This can eliminate the seek-time overhead when those subsequent IOPBs are finally executed.

Data Mapping

Sector data to be transferred to or from the disk may be stored in noncontiguous system memory using the data mapping option. Definable portions of a disk file can be written to or read from separate areas of memory on a byte-by-byte basis. Word processing systems can employ this feature to save text arranged in a linked-list directly on disk and eliminate the time-consuming task of converting the linked-list into a linear list. The Data Map defines the linked-

list data structure. The Data Map option is processed by the HDC while the disk is in operation, so that data maps can be handled without affecting data transfer rate.

Status Result Blocks

When the HDC finds that an IOPB has caused an error, it writes a Status Result Block (SRB). Errors can be caused by invalid command codes, disk read and write errors, and seek or memory time-outs. Since the SRB contains the ID number for the IOPB which caused the error, the operating system can determine which disk I/O job caused the error and report this to the user. Depending upon the type of error and what policy has been selected, the HDC may continue with the IOPB chain automatically or wait for the host processor to tell it whether to start over or continue. The SRBs contain all the specific information required to find the exact location of the error and to make recovery as complete as possible.

Registers

When the IOPB command chain has been set up, the Next Block Pointer Register of the HDC should be set to point to the first IOPB in the chain. Writing a Start Chain command to the Status/Command Register causes the HDC to copy the first IOPB into its internal memory. It starts executing the IOPB after updating the Next Block Pointer to the next command in the IOPB chain. The Status/Command Register also reports HDC error and status codes (such as memory time-outs, IOPB option results, and other information related to the internal operation of the HDC).

The Status Result Pointer points to an area of memory reserved for Status Result Blocks (SRBs). The length of this memory block is defined by the Status Result Length Register, which specifies the number of SRBs. (Each SRB is 10 bytes.) The error-handling scheme of the operating system can manipulate this as needed to coordinate disk use.

The Mode Register controls the HDC's share of the system bus bandwidth to adapt the HDC to the system performance requirements.

REGISTER DESCRIPTION

Four registers control the operation of the HDC. These registers can be accessed directly by the host CPU. The addresses are shown in Figure 4.

MODE REGISTER

Bit assignments of this 16-bit read/write register are shown in Figure 6. This register may be read or written at any time. A hardware or software reset initializes all bits in this register to zero. DMA Burst Length and DMA Dwell Time control the share of the system bus bandwidth allocated to the HDC. DMA Burst Length defines the maximum length of a DMA burst in bytes and DMA Dwell Time specifies the minimum time between DMA bursts that the HDC must stay off the system bus.

Wait Select (WS) defines the number of software Wait States that are inserted into bus transactions. The HDC inserts this number of Wait States and then waits until the READY line is activated (hardware Wait States). If no acknowledge is received within 2^{16} clock periods, a time-out error is generated.

Figure 4. Register Addresses

\overline{CS}	A ₃	A ₂	A ₁	Register Accessed
L	L	L	L	Status/Command Register
L	L	L	H	Mode Register
L	L	H	L	Next Block Pointer (low word)
L	L	H	H	Next Block Pointer (high word)
L	H	L	L	Status Result Pointer (low word)
L	H	L	H	Status Result Pointer (high word)
L	H	H	L	Status Result Length
L	H	H	H	Reserved
H	X	X	X	No Register Accessed

Figure 5. Data Bus Assignment for Byte/Word Transfers

MODE	B/ \overline{W}	B \overline{H} E	A ₀	AD (15 : 8)	AD (7 : 0)
Word Access	L	L	L	HIGH	LOW
	L	H	L	—	LOW
	L	L	H	HIGH	—
Byte Access	H	H	L	—	LOW
	H	H	H	—	HIGH

Figure 6. Mode Register

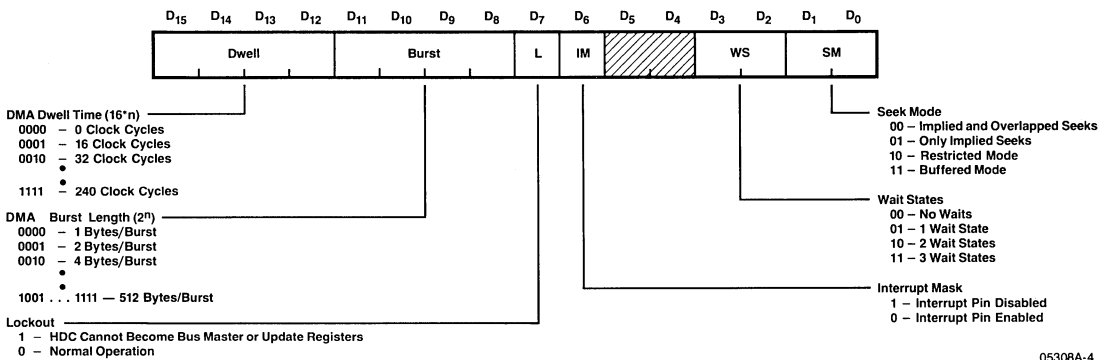
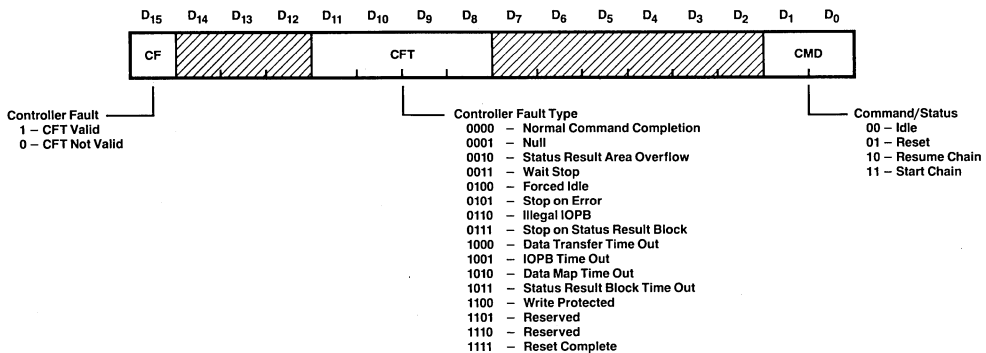


Figure 7. Status/Command Register



The two seek bits control the seek mode. When the Implied Seek option is enabled, the HDC automatically positions the head to the desired track when executing disk commands. This means that explicit seek commands need not precede disk read and write commands. Overlapped seeks are seeks on multiple drives in parallel. In Restricted Mode, seek operations are controlled by external logic. Therefore STEP, DIRIN, and RTZ should not be connected. In Buffered Mode, seek operations and drive selection are handled externally. Therefore, all disk control lines should not be connected. In Buffered Mode the HDC controls only the data transfer (RDDAT, WRDAT, RD/REF CLK and WG), the data separator handshake and ECC operation (AMC, AMF, INDEX, FAM/ECC(1:0), and FAMD/ECCERR).

When the Lock-out bit is set, the HDC does not read or modify internal registers. It also keeps the DMA off the system bus. However, dependent on the time this bit is being set, it may execute further DMA bursts to finish the current sector transfer.

The Interrupt Mask enables and disables the interrupts output pin.

STATUS/COMMAND REGISTER

The host CPU can access the Status/Command Register any time (Figure 7). The execution of some commands modify the content of this register. A hardware or software reset initializes all bits of the Status/Command Register to zero.

Command

When the command field is written by the host CPU, it causes the HDC to enter the programmed state. By reading this field, the host CPU can determine the state of the HDC.

Idle	The HDC is not performing any action. If CF (Controller Fault) is asserted, then CFT (Controller Fault Type) gives the result of the last known action performed. Any command might be written to this command field while the HDC is idle.
Reset	The software reset is immediately executed. On completion of reset, the HDC goes to the idle state. Any access of a register while in the reset state holds READY inactive until the reset is completed, causing the CPU to wait. A software reset is equivalent to a hardware reset.
Resume Chain	The HDC resumes execution of the IOPB chain where it was interrupted due to a Status Result Area overflow. When receiving the Idle command, the HDC completes the current IOPB and then enters the Idle state.
Start	The IOPB chain pointed to by the Next Block Pointer is executed. When receiving the Idle command, the HDC completes the current IOPB and then enters the Idle state.

Controller Fault

When this bit is set, the Controller Fault Type field is valid. The CF-bit is set by the HDC when entering the Idle state and reset when leaving the Idle state.

Controller Fault Type

The Controller Fault Type indicates the status of the HDC upon entering the Idle state. Whenever the Controller Fault Type is updated, the HDC issues an interrupt.

Normal Complete	— Execution of the IOPB chain terminated without fault.
Null NBP	— A Resume or Start Chain command was given with NBP zero.
SRA Overflow	— The HDC filled the Status Result Area (SRA).
Wait Stop	— An IOPB was completed with the option Wait Stop set.
Forced Idle	— An Idle command was given while executing the Resume or Start Chain command.
Stop on Error	— Non-recoverable disk error in conjunction with the SE-bit set caused the HDC to terminate chain execution.
Illegal IOPB	— The HDC attempted to execute an undefined IOPB.
SRB Error	— A Status Result Block (SRB) was written when executing an IOPB with the Stop on SRB (SSRB) option set.
Data Time Out	— Memory Time Out when transferring data.
IOPB Time Out	— Memory Time Out when reading an IOPB.
DM Time Out	— Memory Time Out when reading the Data Map.
SRB Time Out	— Memory Time Out when writing a Status Result Block.
Write Protected	— WRPROT line was asserted when executing a Disk Write command.
Reset	— Hardware or software reset has been executed.

NEXT BLOCK POINTER

The Next Block Pointer Register is a 32-bit register pointing to the IOPB currently being executed. The HDC updates it on IOPB completion.

STATUS RESULT POINTER

The 32-bit Status Result Pointer Register points to the system memory location where the next Status Result Block can be written. This pointer is updated after adding a new Status Result Block to the Status Result Area.

STATUS RESULT LENGTH

The 16-bit Status Result Length Register defines the size of the Status Result Area in terms of the number of Status Result Blocks. Therefore, the maximum size of the Status Result Area is 65536 Status Result Blocks.

The Next Block Pointer, the Status Result Pointer, and the Status Result Length should only be updated while the HDC is in the Idle state.

COMMAND DESCRIPTION

All operations of the HDC result from commands. Commands are set up in system memory in IOPBs (I/O Parameter Blocks) (Figures 8 and 9). The HDC starts interpreting the command list after receiving the "Resume Chain" or "Start Chain" command from the host CPU (see Status/Command Register description). Errors and warnings on command execution are reported by adding Status Result Blocks (SRB) to the Status Result Area.

NORMAL DISK I/O COMMANDS

The HDC supports three normal disk I/O commands: READ, WRITE, and VERIFY. The multi-sector operation is performed on DRIVE starting at the desired TRACK, HEAD and SECTOR. RECORD COUNT defines the number of sectors. The General Select Byte in the Drive Parameter Block specifies whether the track number or the head number is to be incremented on sector overflow. SOURCE/DESTINATION ADDRESS is the starting address of the data block in system memory (DME Low) or the address of the first Data Map Entry (DME High). These commands verify the head position before attempting the data transfer and hence verify seeks implicitly. The Data Mark option allows the DATA MARK parameter to be used instead of F8H. On single-density floppy disks, the Data Mark option also causes the search for a deleted data mark. (See Section "HDC/Data Separator Handshaking.")

READ

READ performs a multi-sector data transfer from disk to system memory.

WRITE

WRITE performs a multi-sector data transfer from system memory to the disk.

VERIFY

VERIFY compares multi-sector data on disk with data stored in system memory. It reports any mismatches or data read errors by updating the Status Result Area.

INITIALIZATION COMMANDS

FORMAT

The HDC formats the number of tracks specified by TRACK COUNT starting at HEAD and TRACK. The head and track number are incremented according to the General Select Byte in the Drive Parameter Block. The sectors are numbered as per the order given in the sector map, which is sequentially loaded from system memory starting at MAP POINTER. The number of sectors per track is specified in the Drive Parameter Block of this DRIVE. The data field of each sector is filled with PATTERN.

RELOCATE TRACK

A relocation vector is written to all data fields of a bad track. The relocation vector consists of the new track number (ALTERNATE TRACK) and the new head number (ALTERNATE HEAD) (i.e., the track's relocated location). Also, the address mark is changed from FE_H to FD_H to mark that this track is relocated. Thus, when the HDC encounters three consecutive sectors with an FD_H data mark, it assumes the track has been relocated. This command is illegal for single-density floppy disk drives.

LOAD DRIVE PARAMETER BLOCK

This command loads the Drive Parameter Block (DPB) for the selected DRIVE into the internal Drive Parameter RAM (see "Drive Parameters").

DUMP DRIVE PARAMETER BLOCK

The Drive Parameter Block for the selected DRIVE is transferred from the internal Drive Parameter RAM to the DESTINATION ADDRESS.

MARGINAL DATA RECOVERY COMMANDS

READ PHYSICAL SECTOR

This command lets the user recover a marginal data field which is unrecoverable by normal disk error recovery procedures. First it seeks to the desired track. If TRACK VERIFY is selected, the HDC reads ID fields until three consecutive sector headers show the right track number. This verifies it is on the right track. Beginning with the next index mark, the HDC starts counting the PHYSICAL SECTOR number of IDs specified by "PHYSICAL SECTOR" to locate the desired sector. It reads the data field while disregarding the ID field. The user can thus possibly recover data where headers and/or data marks have been rendered unreadable. PHYSICAL SECTOR specifies the absolute location of the sector. No retries are performed.

READ ID

READ ID attempts to recover the header ID information of a marginal sector. If LOCATOR DUMP is selected, then the first valid ID read is transferred to the DESTINATION ADDRESS. If LOCATOR DUMP is not selected, then the ID of the absolute sector specified by PHYSICAL SECTOR is transferred to DESTINATION ADDRESS. If this command is successfully executed, it updates the HDC's track position.

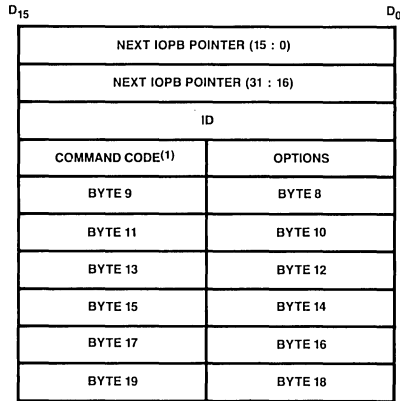
LOAD BUFFER

The data pointed to by the SOURCE ADDRESS is transferred to the internal sector buffer. The number of bytes transferred is determined by the sector size for the selected DRIVE.

DUMP BUFFER

The data in the internal sector buffer is transferred to system memory starting at DESTINATION ADDRESS. The number of bytes transferred is specified by the sector size for the selected DRIVE.

Figure 8. IOPB Structure



(1) Not yet defined.

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Figure 9. IOPB Parameters

Command	Options								Byte 9	Byte 8	Byte 11	Byte 10	Byte 13	Byte 12	Byte 15	Byte 14	Byte 17	Byte 16	Byte 19	Byte 18
	7	6	5	4	3	2	1	0												
Read	W	SE	SSRB		DME	DM			Drive	Track		Head	Sector	Data Mark	Record Count		Destination (15 : 0)		Destination (31 : 16)	
Write	W	SE	SSRB		DME	DM			Drive	Track		Head	Sector	Data Mark	Record Count		Source (15 : 0)		Source (31 : 16)	
Verify	W	SE	SSRB		DME	DM			Drive	Track		Head	Sector	Data Mark	Record Count		Source (15 : 0)		Source (31 : 16)	
Format	W	SE	SSRB					Pattern	Drive	Track		Head			Track Count		Map Pointer (15 : 0)		Map Pointer (31 : 16)	
Relocate Track	W	SE	SSRB						Drive	Track		Head			Alternate Track		Alternate Head			
Load Drive Parameter Block	W	SE	SSRB						Drive								Source (15 : 0)		Source (31 : 16)	
Dump Drive Parameter Block	W	SE	SSRB						Drive								Destination (15 : 0)		Destination (31 : 16)	
Read Physical Sector	W	SE	SSRB		TV				Drive	Track		Head	Physical Sector				Destination (15 : 0)		Destination (31 : 16)	
Read ID	W	SE	SSRB		L				Drive	Track		Head	Physical Sector				Destination (15 : 0)		Destination (31 : 16)	
Load Buffer	W	SE	SSRB		DME				Drive								Source (15 : 0)		Source (31 : 16)	
Dump Buffer	W	SE	SSRB		DME				Drive								Destination (15 : 0)		Destination (31 : 16)	
Load Syndrome	W	SE	SSRB						Drive								Source (15 : 0)		Source (31 : 16)	
Dump Syndrome	W	SE	SSRB						Drive								Destination (15 : 0)		Destination (31 : 16)	
Correct Buffer	W	SE	SSRB		LD				Drive								Destination (15 : 0)		Destination (31 : 16)	
Seek	W	SE	SSRB		TV				Drive	Track		Head								
Restore	W	SE	SSRB		TV				Drive											

LOAD SYNDROME

The Reed-Solomon check bytes are transferred from SOURCE ADDRESS to the internal Syndrome RAM. This command generates an error if the Drive Parameter Block of the selected DRIVE specifies CRC or external ECC error-checking.

DUMP SYNDROME

The Reed-Solomon check bytes are dumped to the DESTINATION ADDRESS.

CORRECT BUFFER

This command uses the contents of the Syndrome RAM to correct the data in the internal sector buffer. It generates an error if the Drive Parameter Block of the selected DRIVE specifies CRC or external ECC error-checking. If the LOCATOR DUMP option is selected, the HDC additionally writes the location and values of errors sequentially to DESTINATION ADDRESS. If the buffer address is greater than the sector size and the error pattern is non-zero, then the error is uncorrectable for that locator. If the error pattern and the buffer address both are zero, then no error was detected by that locator. If the error pattern is zero and the buffer address is greater than the sector size, then the error occurred in the check bytes.

HEAD MOVEMENT COMMANDS

SEEK

The HEAD of the selected DRIVE is moved to the desired TRACK. If TRACK VERIFY is selected, the HDC looks at the first encountered header to determine whether it is on the right track. If the track numbers mismatch, the HDC reports an error. Usually, this command is issued only if implied and overlapped seeks are disabled.

RESTORE

RESTORE moves the heads of the selected DRIVE to track 0. This command synchronizes the HDC and the drives or recovers seek errors. The HDC supports two restore options. It can restore drives by issuing step-out pulses until the drive reaches track 0 and asserts TRK0. Optionally, drives with built-in restore logic may be restored by a pulse on the RTZ (Return To Zero) line. If TRACK VERIFY is selected, the HDC will also scan the header IDs in order to verify that the restore was successful.

OPTION BYTE

One byte in each IOPB contains a set of options applicable to the particular command.

W — WAIT

- 0 — After execution of current IOPB, continue with next IOPB.
- 1 — Stop IOPB execution after terminating current IOPB.

SE — TOP ON ERROR

- 0 — Option disabled.
- 1 — Stop IOPB chain execution if current IOPB causes a Status Result block to be written.

SSRB — STOP ON STATUS RESULT BLOCK

- 0 — Option disabled.
- 1 — Stop IOPB chain execution if current IOPB causes a Status Result block to be written.

DME — DATA MAP ENABLE

- 0 — Data Mapping disabled.
- 1 — Data Mapping enabled. Source/Destination Address links to first Data Map Entry.

DM — DATA MARK

- 0 — Data Mark disabled.
- 1 — Data Mark enabled (see Normal Disk I/O Commands).

TV — TRACK VERIFY

- 0 — Track Verify disabled.
- 1 — Track Verify enabled (see Read Physical Sector and Seek).

L — LOCATOR DUMP

- 0 — Locator Dump disabled.
- 1 — Locator Dump enabled (see Read ID).

DATA MAPPING OPTIONS

The Data Mapping option lets the HDC process data stored in noncontiguous system memory. This option is available to five commands: Read, Write, Verify, Load Buffer, and Dump Buffer. It is enabled by setting the Data Map Enable bit (DME-bit) in the IOPB.

The last two words of the IOPB (Source/Destination Address) link to the first Data Map Entry (Figures 10 and 11). If this pointer is zero, then the Data Map does not exist and the HDC does not transfer data. Data Map Entries are linked together via the Data Map Pointer. The Data Map linked-list is terminated if the Data Map Pointer is set to zero. Each Data Map Entry defines a data buffer in system memory starting at the address defined by Data Source/Destination Address. The size of this buffer is defined by Byte Count. When Byte Count is set to zero, the HDC assumes a size of 2¹⁵ bytes. When the Load Enable (LE-bit) is reset to zero, the HDC masks off a data block with the size specified by Byte Count (Figure 12).

STATUS RESULT BLOCK (SRB)

The host CPU reserves a Status Result Area defined by the 32-bit Status Result Pointer register and the 16-bit Status Result Length Register. Whenever the HDC terminates a command and an error occurred, it adds a Status Result Block (Figures 13 and 14) to the Status Result Area. A Status Result Block carries the same unique ID number of the IOPB where the error occurred.

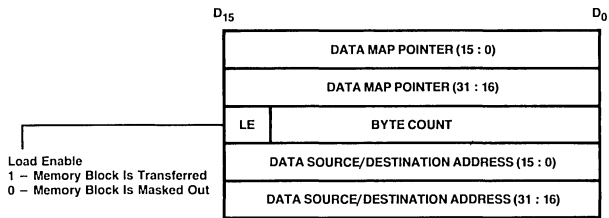
Multi-record Command Terminated

This SRB indicates that a Multi-record command has been terminated due to an error condition at the specified TRACK, HEAD, SECTOR, and RECORD COUNT.

No IDs Found On Track

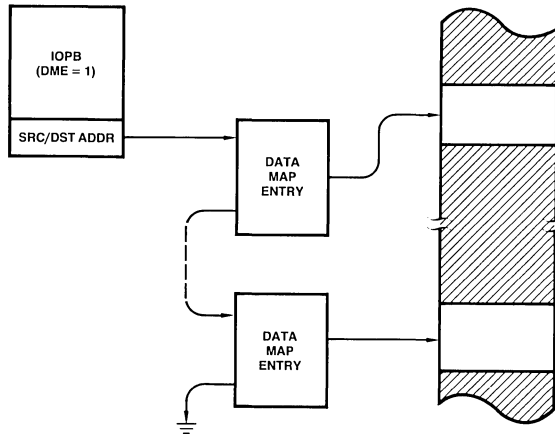
A given Track was searched for an ID and none was found.

Figure 10. Data Map Entry



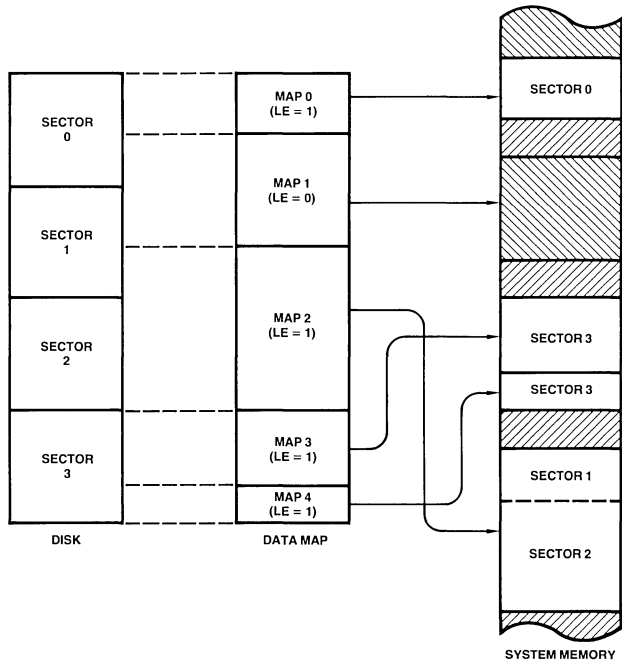
05308A-7

Figure 11. Data Map Entry Linked List



05308A-8

Figure 12. Data Mapping



05308A-9

Figure 13. Layout of Status Result Blocks

D ₁₅		D ₀	
Byte 1	Byte 0	Byte 3	Byte 2
Byte 5	Byte 4	Byte 7	Byte 6
Byte 9	Byte 8		

Figure 14. Status Result Blocks

Status Result Block	Byte 1	Byte 0	Byte 3	Byte 2	Byte 5	Byte 4	Byte 7	Byte 6	Byte 9	Byte 8
Multirecord Command Terminated	ID		Record Count	Code ⁽¹⁾	Track		Head	Sector		
No IDs Found on Track	ID			Code	Track		Head			
Format Error	ID			Code	Track		Head			
Seek Error	ID			Code	Current Track		Desired Track		Current Head	Desired Head
Fatal Seek Error	ID			Code	Current Track		Desired Track		Current Head	Desired Head
Relocated Track	ID			Code	Current Track		New Track		Current Head	New Head
Relocated Track (No Vector)	ID			Code	Track		Head			
Record Not Found	ID			Code	Track		Head	Sector		
Record Not Found (ID Errors)	ID			Code	Track		Head	Sector		
Multirecord Overflow	ID			Code	Track		Head	Sector		
Data Not Recovered	ID			Code	Track		Head	Sector		
Data Not Recovered with Retries	ID		Retry Count	Code	Track		Head	Sector		
Data Not Recovered with ECC	ID		Retry Count	Code	Track		Head	Sector		
Data SYNC Fault	ID			Code	Track		Head	Sector		
Data Mark Error	ID		Data Mark	Code	Track		Head	Sector		
Sector Size Mismatch	ID		Sector Size	Code						
Data Non-Verify	ID			Code	Track		Head	Sector		
Physical Data Recovered with ECC	ID			Code						
ECC Error Not Corrected	ID			Code						
ECC Not Selected	ID			Code						
ECC Error in Data Field	ID			Code						
Data Mark Physical Error	ID		Data Mark	Code						
ID CRC Error	ID			Code						
Fault While Seeking	ID			Code	Track					
Restore Fault	ID		Drive Status	Code	Track					
Fault While Head Select	ID			Code			Head			
Drive Selection Fault	ID		Drive Status	Code						
Drive Status Trap	ID		Drive Status	Code						
Data Timeout	ID			Code	Byte Count		Block Address (15 : 0)		Block Address (31 : 16)	
No Single Density Floppy Relocation	ID			Code						
End of Data Map	ID			Code						

(1) Not yet defined.

Format Error

When reading or writing, it indicates that an Index Pulse occurred when not expected. When formatting, it indicates that the Index Pulse occurred before the format was completed. This means the number of sectors times the sector size is too large for the track.

Seek Error

The HDC has read a valid ID showing that the current TRACK/HEAD differs from the expected TRACK/HEAD.

Fatal Seek Error

After a seek error the HDC has performed a restore and a second seek, but the seek error still persists. The IOPB is aborted.

Relocated Track

A track was read as relocated and the HDC auto-vectored to the new track.

Relocated Track (No Vector)

A track was read as relocated, but the HDC could not find a valid data field to read the vector. The IOPB is aborted.

Record Not Found

No ID was found corresponding to the desired sector number.

Record Not Found (ID Errors)

Sector was not found, but one or more IDs had CRC errors.

Multi-record Overflow

The HDC aborted a Multi-record command because the last sector of a track was read and the programmed Multi-Record Policy prohibits a track/head increment.

Data Not Recovered

The HDC could not recover a sector requested by a read command.

Data Recovered with Retries

Data was recovered using read retries (RETRY COUNT).

Data Recovered with ECC

The Reed-Solomon successfully corrected a read error. Retry Count specifies the number of retries performed before the error was corrected.

Data Sync Fault

The HDC successfully read the ID for the desired sector, but could not find an Address Mark for the data field.

Data Mark Error

The Data Mark read did not correspond to the Data Mark specified by the Drive Parameter Block.

Sector Size Mismatch

Sector Size read from the Header field does not match the Sector Size defined in the Drive Parameter Block (floppy formats only).

Data Non-Verify

The Verify command detected a mismatch between disk and memory data.

Physical Data Recovered with ECC

The Read Physical Sector command had to use ECC to correct the data field.

ECC Error Not Corrected

The data transferred to system memory by Read Physical Sector contained uncorrected errors.

ECC Not Selected

Error correction attempted when ECC was not selected internally.

ECC Error In Data Field

An error was detected in the data field of a sector.

Data Mark Physical Error

The Data Mark read by Read Physical Sector did not correspond to programmed Data Mark.

ID CRC Error

A CRC error was detected when reading the ID field by the Read ID command.

Fault While Seeking

While seeking, the FAULT line was asserted or the SEEKCOM line was not asserted.

Restore Fault

The HDC could not restore the drive.

Fault While Head Select

The HDC could not select the specified head. The FAULT line was asserted or SEEKCOM was not asserted (for floppy disk drives only).

Drive Selection Fault

A fault occurred when selecting a drive. The Drive Status byte latches the levels of the status lines when the fault occurred:

D₉ = DREADY
D₁₀ = FAULT
D₁₁ = SEEKCOM
D₁₂ = WRPROT
D₁₃ = TRK0

Drive Status Trap

An unexpected change in state of one or more drive status lines occurred while the drive was selected. The Drive Status byte latches the status lines. The IOPB is aborted.

Data Time-out

A memory time-out occurred while accessing the system memory. The Block Address defines the starting location of a block of system memory where the time-out occurred. Byte Count defines the length of the block.

No Single-Density Floppy Relocation

A Relocate Track command was attempted on a single-density floppy disk drive.

End Of Data Map

Unexpected end of Data Map encountered.

DISK DATA I/O

SECTOR FORMATS

Data is stored on the disk in sectors. Each sector consists of two fundamental parts: the header and the data field. The sizes of all pads, gaps, preambles, postambles, and data fields are programmable in the Drive Parameter Block. Floppy disk formats also have an Index field at the beginning of each track.

Header

The header contains the Address Mark, the track number, the head number, and the sector number (Figure 16). Two trailing CRC check bytes protect the header. The beginning of the header is marked by an ID Address Mark (IDAM). The single-density floppy format requires a single-byte address mark while the double-density floppy and hard disk formats use a two-byte address mark. The first byte (the only byte for single-density floppy formats) of the address mark is a unique clock/data pattern written and detected by the data separator. Since the unique clock/data pattern is written by the disk data separator, its length and layout are transparent to the HDC. The second byte, which is processed by the HDC, specifies that this is a normal (FE_H) or a relocated (FD_H) track. This byte is not present for single-density floppy formats. A preamble and a postamble compensate for speed and mechanical variations of the disk system. The length of both fields is user-programmable.

Data Field

A Data Mark similar to the header's ID Address Mark marks the beginning of the data field (Figure 17). The single-density floppy format uses a single-byte Data Mark which is different from the Address Mark. The data field can be marked by two types of data marks to specify either a normal data field or a deleted data field. The double-density floppy and the hard disk formats have a two-byte Data Mark consisting of a unique clock/data pattern similar to the Address Mark and a user-programmable Data Mark byte.

The data field has a user-programmable length of 128, 256, or 512 bytes. It is protected by one of three user-selectable data protection algorithms: CRC-CCITT (error detection), Single-Burst or Double-Burst Reed-Solomon (error detection and correction). Optionally, external error processing logic can be interfaced for hard disk format to implement any user-designed algorithm. The check bytes are stored in the ECC field. For external error processing, the user-designed external error processing logic reads and writes the ECC field. The number of ECC bytes appended varies from 2 to 15 bytes for the internal ECC options and 1 to 256 bytes (determined by the drive parameter block) for external ECC.

DATA SEPARATOR INTERFACE SIGNALS

The data lines (RDDAT and WRDAT) transfer the data to and from the disk. The transfer is controlled by five signals: INDEX, AMC, AMF, RG, and WG. The FAM/ECC(1:0) and FAMD/ECCERR lines interface with external hardware to allow user-definable error-detection/correction. For floppy formats, these lines interface with the data separator to allow address/data mark detection and generation.

Header Search Mechanism

The unique clock/data patterns of the address/data marks are written and detected by the data separator only. When the HDC attempts to read a header or to access a data field, it activates Address Mark Control (AMC).

For floppy formats, the FAM/ECC(1:0) outputs differentiate between the various index, address, and data marks defined by the IBM Single- and Double-density Format. Whenever the HDC activates the AMC line to read or write a special mark from a floppy disk, the data separator should use the FAM/ECC(1:0) to determine the unique clock/data pattern to read or write. Additionally, for single-density floppy formats, the FAMD/ECCERR pin indicates that a deleted data address mark should be written or read.

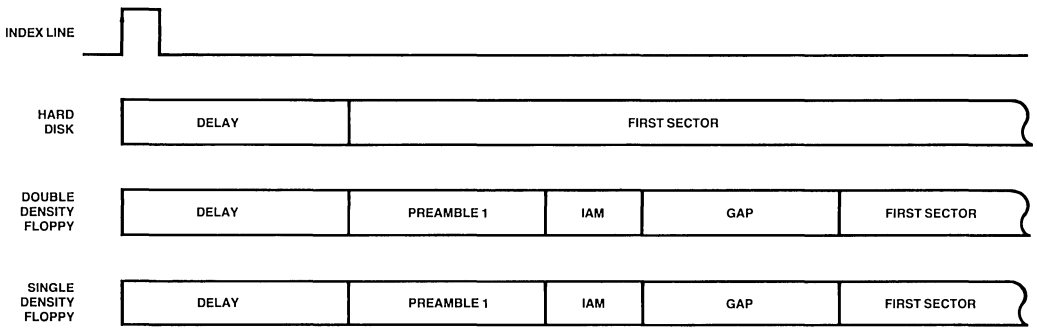
Next, the HDC activates Read Gate (RG) and waits for the data separator acknowledge. The data separator should assert Address Mark Found (AMF) when it detects an address/data mark. The rising edge of AMF indicates that valid data will be on the RDDAT pin on the next rising edge of the RD/REF CLK (see Figure 23). For double-density floppy and hard disk formats, the HDC checks the next eight bits for an FD_H or FE_H . If the check fails, a data address mark was found; the HDC deactivates AMC and RG. After AMF becomes inactive, AMC is reasserted followed by RG and the whole procedure is repeated until a header is found or it is determined that no header can be found (indicated by three index pulses). For single-density floppy formats, the rising edge of AMF indicates that a header address mark has been found.

After finding a valid header address mark, the HDC compares the next 48 bits (6 bytes) of serial data with the track, head, and sector number of the desired sector (and sector size for floppy formats) to determine if the right header has been found. A CRC check ensures the correctness of the header information. If the track or the head numbers recovered from the header do not match the desired track or head number, an error is flagged and the command is aborted. For floppy formats, sector size is also checked against the sector size defined for the current drive. The sector number is checked to see if this is the desired sector.

If the correct sector number was not found, then the process is started all over again until either the desired sector is found or the HDC determines that the sector cannot be found on the current track. If three index pulses are detected (indicating 2+ disk revolutions), the Sector Not Found error is flagged.

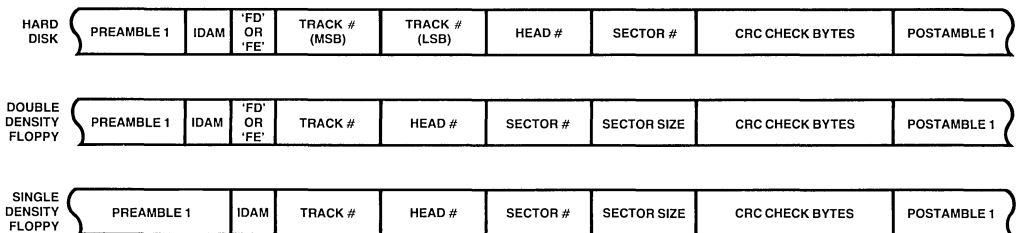
If the correct sector number was found, the search for the data mark begins.

Figure 15. Track Initialization Field



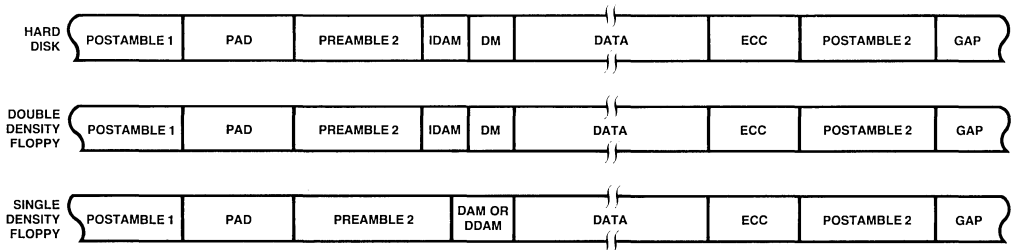
05308A-10

Figure 16. Sector Header Formats



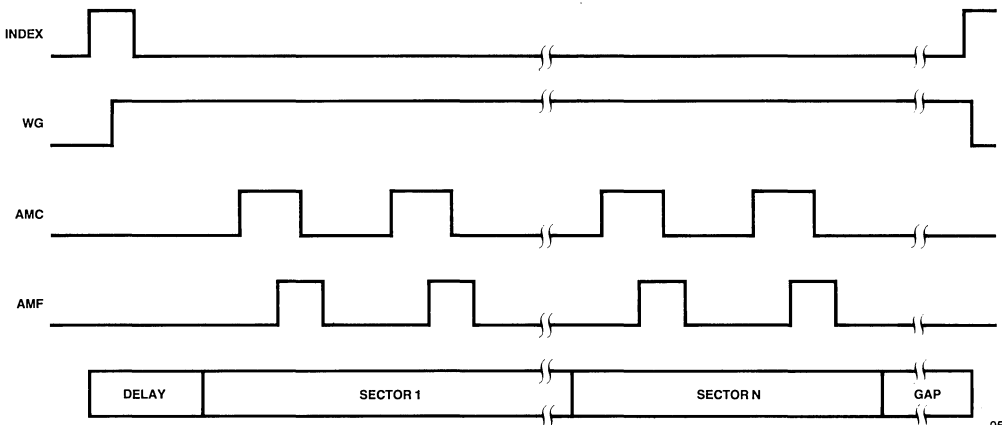
05308A-11

Figure 17. Sector Data Fields Format



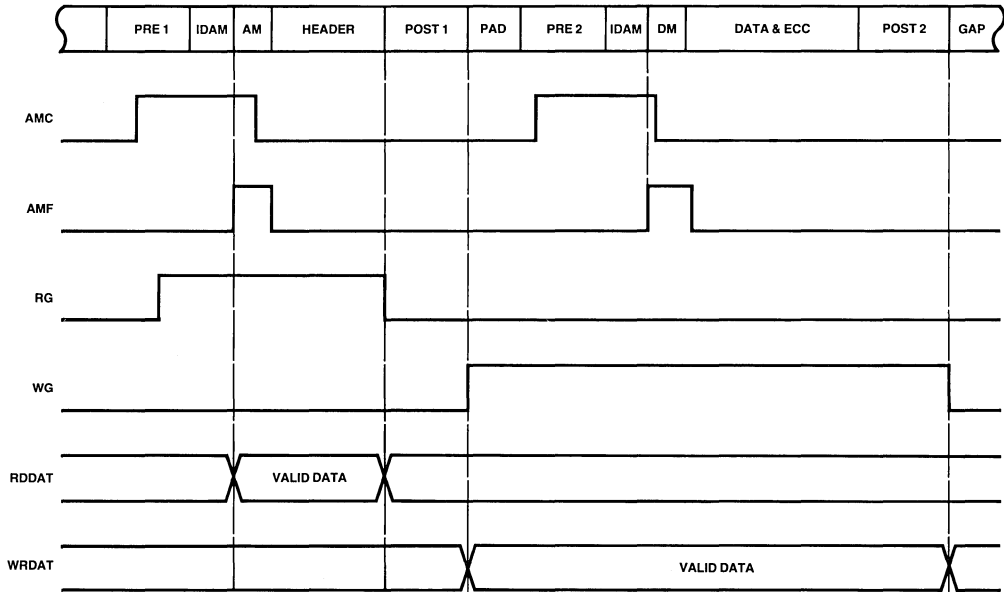
05308A-12

Figure 18. Write Track Sequence



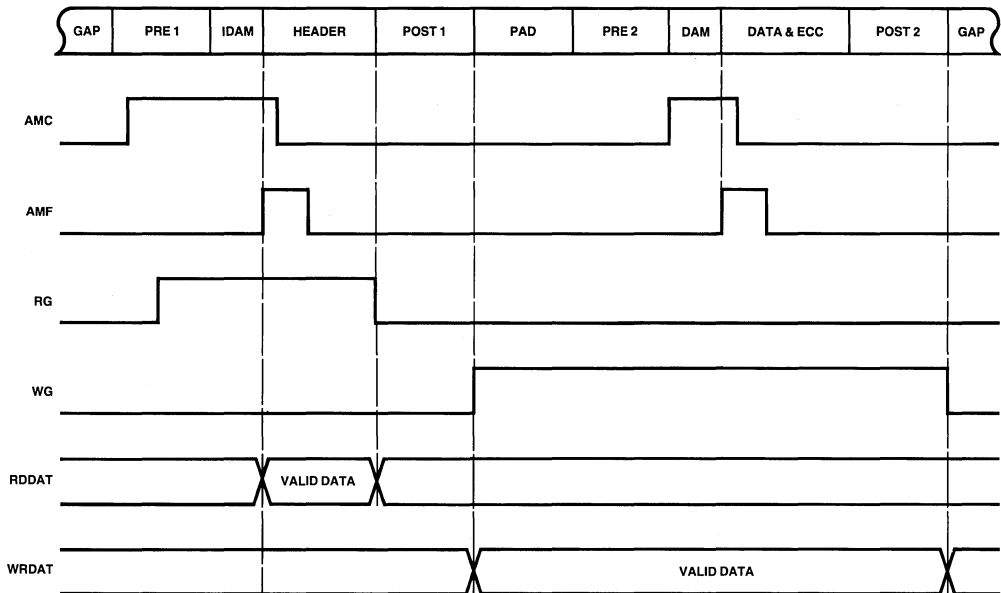
05308A-13

**Figure 19. Write Sector Control Sequence
(For Hard Disk and Double Density Floppies)**



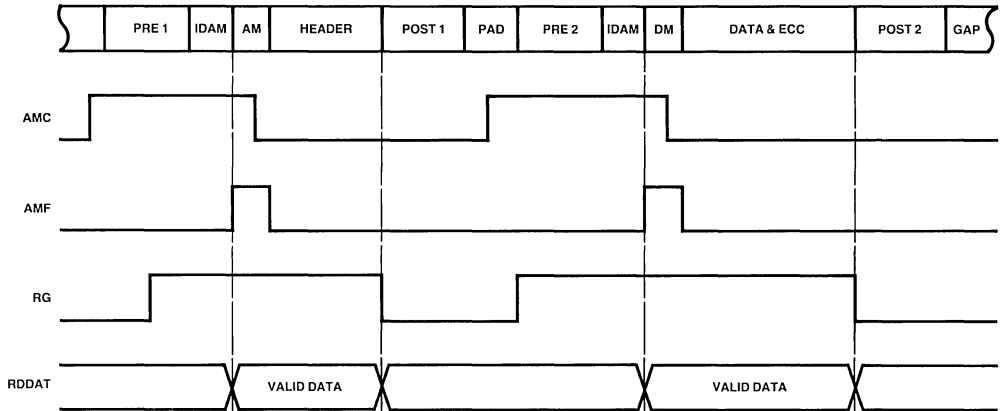
05308A-14

**Figure 20. Write Sector Control Sequence
(For Single Density Floppies)**



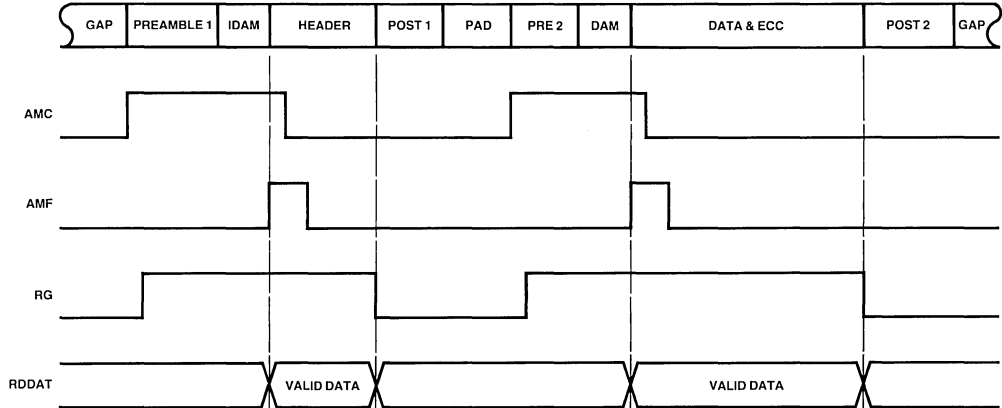
05308A-15

**Figure 21. Read Sector Control Sequence
(For Hard Disks and Double Density Floppies)**



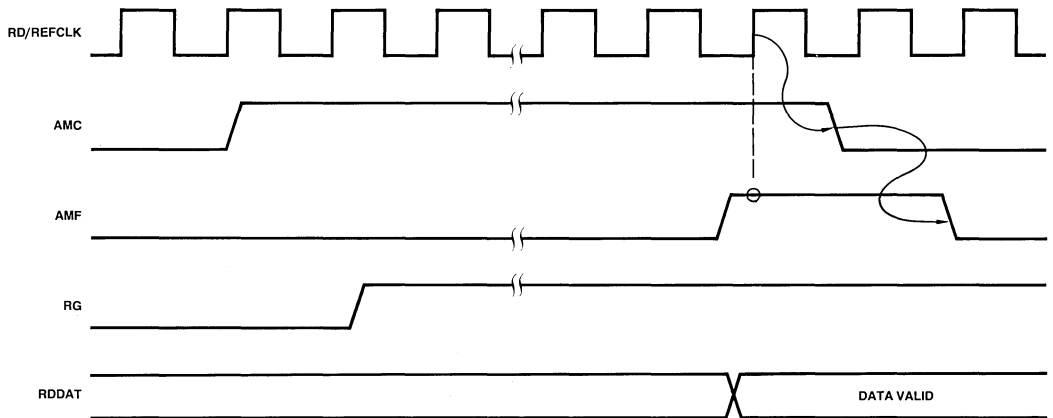
05308A-16

**Figure 22. Read Sector Control Sequence
(For Single Density Floppies)**



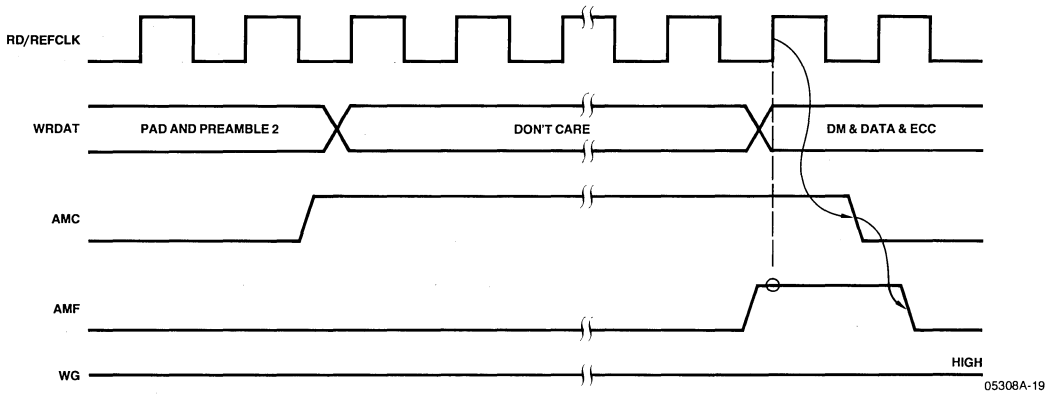
05308A-17

**Figure 23. Address Mark Control/Address Mark Found Handshake
(Read Data)**



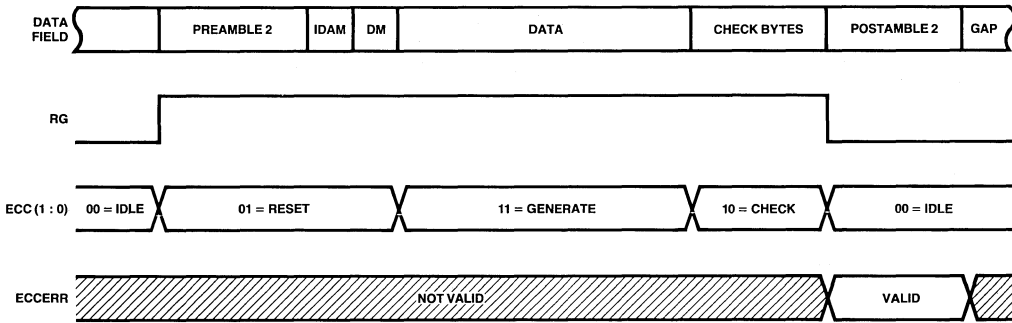
05308A-18

Figure 24. Address Mark Control/Address Mark Found Handshake (Write Data)



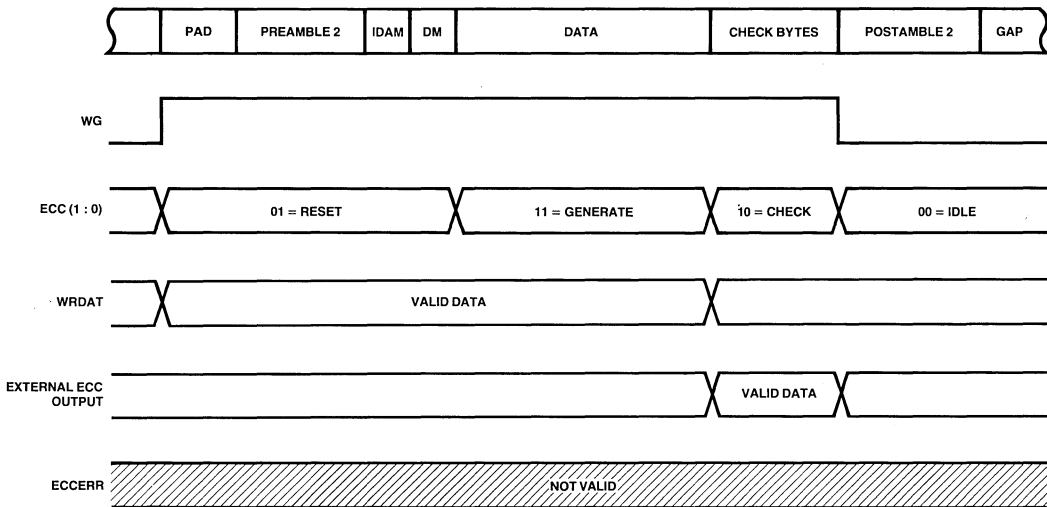
05308A-19

Figure 25. External ECC Handshake (Read Data)



05308A-20

Figure 26. External ECC Handshake (Write Data)



05308A-21

Data Field Read

The HDC uses the same handshake procedure outlined above to search for the data address mark. For double-density floppy and hard disk formats, the HDC compares the byte following the data address mark to the programmed data mark to confirm that the data field has been found. The HDC reads the data field into the sector buffer and the ECC bytes into the error logic. For hard disk formats, the HDC ignores the ECC field if external ECC is selected. The external error processing logic should read the ECC field to verify the integrity of the data field. FAM/ECC(1:0) and FAMD/ECCERR control the external error logic handshake. Immediately after the ECC field has been read, RG is turned off and the sector-read operation is terminated.

Data Field Write

Sector-write commands proceed similarly to sector-reads while searching for the desired sector. After finding the desired sector header, the subsequent data field and ECC field, including pad, preamble2, data address mark and postamble2 is overwritten. The HDC activates Write Gate (WG) at the beginning of the pad. Write Data on WRDAT line is valid with the next rising edge of the clock. First the HDC writes the pad and preamble2 fields. On completion of preamble2, AMC is activated. For floppy formats, FAM/ECC(1:0) indicate to the data separator the data address mark to write. The data separator should assert AMF after writing the last data address mark bit. The HDC resumes data output with the next clock. For double-density floppy and hard disk formats, the HDC writes a user-programmable data mark first. Next the data field is output on the WRDAT line. Depending on the selected ECC mode, either the HDC or the external error logic appends the check bytes to the data field. FAM/ECC(1:0) and FAMD/ECCERR control the external error logic handshake. WG is turned off after the postamble2 field is written. This completes the write-sector sequence.

Format Track

Format Track always writes the entire track. It is the only command that writes the sector header. Beginning with the rising edge of the INDEX pulse, the HDC asserts WG and outputs the pattern for the delay field (Figure 18). Note that disk drives require that the delay field be wider than the INDEX pulse width. For floppy formats, an Index Address Mark (IAM) field follows the delay field. Then the HDC starts writing sectors.

For writing the headers, the HDC uses the track, head and sector size information supplied by the format IOPB. A sector map in the system memory supplies the logical sector number sequence. The first byte of the sector map is written in the sector number field of the first physical sector. The second byte is written in the second physical sector. This process continues until the required number of sectors have been formatted. For multiple track format commands, the sector maps for the tracks to be formatted are organized in a linear list in the system memory. The Map Pointer of format IOPB points to the beginning of this sector map list.

For writing address/data marks, the HDC proceeds as described in the section "Data Field Write". The data field is

filled with the user-supplied pattern byte in the format IOPB. The gap between the end of the last sector and the rising edge of the index pulse is filled by the gap pattern. The length of this gap field depends on the track capacity and the number of sectors/track. It is different from the intersector gap which has a user-definable length. The patterns written for all fields are shown in the table below.

Field	Single-density floppy formats	Double-density floppy and hard disk formats
Delay	FF _H	4E _H
Preamble1	00 _H	00 _H
Postamble1	FF _H	4E _H
Pad	00 _H	00 _H
Preamble2	00 _H	00 _H
Postamble2	FF _H	4E _H
Gap	FF _H	4E _H

DRIVE PARAMETER PROGRAMMING (Figure 27)

The HDC contains one set of Drive Parameter Registers for each drive. The system can only access this register set indirectly by either of the following commands: Load Drive Parameter Block and Dump Drive Parameter Block. The block is set up in contiguous system memory. Byte values in this table, when set to zero, represent the value 256.

General Select Byte (Figure 28)

The EDCP field determines which of the error-checking algorithms the HDC should use to recover marginal data. The Auto Vector Enable bit (AVE) allows the HDC to vector automatically to the new track if a given track is found to be relocated. This bit is ignored for single-density floppy formats. The Multi-Record Policy (MRP) field determines the policy followed for multiple sector transfers. Multi-record commands may require that the HDC select a new track to access subsequent sectors. One option is to increment the head number. If the head number overflows, the HDC resets it to zero and increments the track number. If the track number overflows, it is reset to zero. The second option allows the track number to be incremented first. On overflow, the head number is incremented. The RTZEN bit defines the recalibration mode (move head to track 0). The HDC can either assert the RTZ pin (16 clock cycles active) or issue STEP pulses until TRK0 becomes active. The maximum number of STEP pulses for recalibration is 65535.

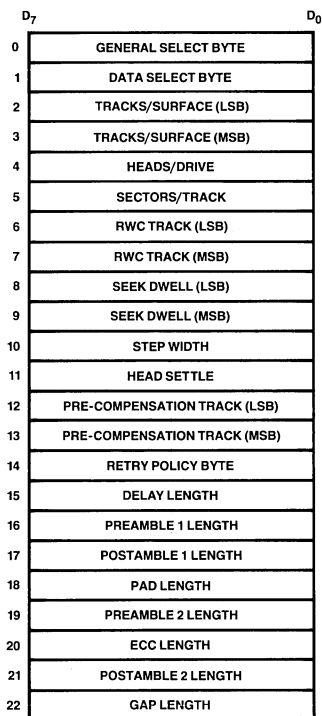
Data Select Byte (Figure 29)

The DSIZE field defines the size of the data field for a particular drive.

Retry Policy Byte (Figure 30)

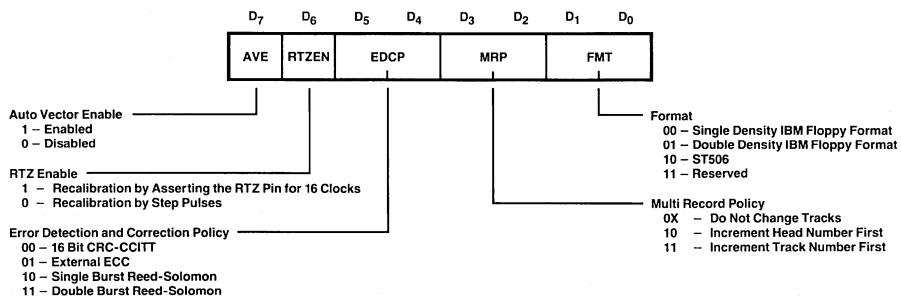
The most significant three bits define the error-checking policy. These bits are ignored if CRC or external ECC is used. If ECC Before Retry is selected, the HDC uses ECC even when retry attempts are disabled. The RE-bit enables the number of retry attempts defined by Retry Count (RC).

Figure 27. Drive Parameter Block



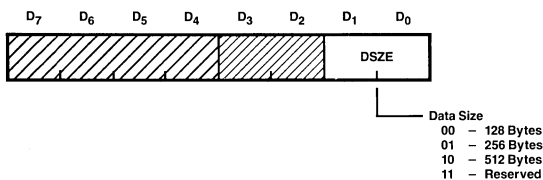
05308A-22

Figure 28. General Select Byte



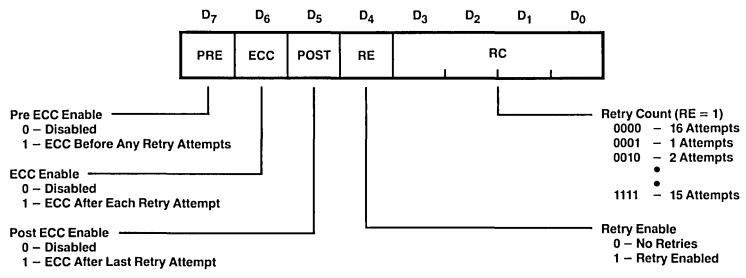
05308A-23

Figure 29. Data Select Byte



05308A-24

Figure 30. Retry Policy Byte



05308A-25

Drive Parameters

Tracks/Surface specifies the number of cylinders (tracks) in the range from 0 to 65536. Head/Drive specifies the number of moving heads (1 to 256). However, only the four least significant bits are output at the head select pins. Sectors/Track defines the number of sectors per track (1 to 256). Heads/Drive and Sectors/Track are only needed for multi-record IOPBs to allow the HDC to determine the new track number. RWC Track specifies the track number where the Reduced Write Current pin should be activated (only for ST506 and floppy formats). If the current track number is greater than RWC Track, the pin (RWC) is activated. Pre-Compensation Track specifies the track where the pre-compensation starts.

Seek Timing

Step Width (8-bit) determines the width of step pulses in increments of 12 clock cycles. Seek Dwell (16-bit) sets the delay between the falling edge and the rising edge of step pulses in increments of 12 clock cycles. Head Settle defines the time to allow the heads of the selected drive to settle, after the head select lines change, in increments of 4 clock cycles.

Sector Format

The sector format parameters specify the sizes of particular sector header and data fields.

DISK DATA PROTECTION

All data stored on disk is protected by error-checking algorithms. The HDC supports four modes:

- 16-bit CRC-CCITT (error detection)
- Single-Burst Reed-Solomon (single-burst correction)
- Double-Burst Reed-Solomon (double-burst correction)
- External ECC

The error-checking scheme for each drive is defined by the EDCP field in the General Select Byte of the Drive Parameter Block. It is possible to use a different ECC for each sector or track provided that the Drive Parameter Block is constantly changed. However, this is not a recommended procedure.

CRC-CCITT

The CRC-CCITT code is a cyclic-based, error-detecting/non-correcting code. It is the industry standard error checking code for magnetic disk systems. CRC-CCITT is mandatory for the protection of the sector ID field, but the data field can be protected by any of the four modes mentioned above. The CRC generator polynomial is:

$$X^{16} + X^{12} + X^5 + 1$$

The guaranteed capabilities of the code are listed below:

- Detects all odd number bit errors
- Detects all single-burst errors of 16 bits or less
- Detects all single, double, and triple bit errors

Single-Burst Reed-Solomon

The HDC supports two error correction codes, Single-Burst Reed-Solomon and Double-Burst Reed-Solomon. Single-Burst Reed-Solomon corrects single-burst errors and detects double-burst and some triple-burst errors. A single burst of errors is defined as any number of bit errors (contiguous or noncontiguous) where the distance between the first and the last bit error does not exceed the burst length given in the table below. The ECC code protects the check bytes as well as the data. The guaranteed performance of the Single-Burst Reed-Solomon code is shown below.

Sector Size (# of bytes)	Detection Capability (# of bits)		Correction Capability (# of bits)		# of Check Bytes
	Single Bursts	Double Bursts	Single Bursts	Double Bursts	
128	33	9	9	0	6
256	33	9	9	0	6
512	57	17	18	0	9

This table shows, for instance, that in a sector of 256 bytes any single burst of errors with a length of up to 33 bits will be detected. Note, that two single bit errors separated by more than 32 bits will count as a double-burst error. Alternatively, any two random single-bursts (double-burst) of up to 9 bits each will be detected also. In this example, this code can correct a single burst of errors up to 9 bits and cannot correct double-burst errors. The table presents the guaranteed capabilities of this code. Under certain circumstances the code is capable of detecting longer bursts or even triple-burst errors.

Double-Burst Reed-Solomon

Double-Burst Reed-Solomon is an enhanced version of Single-Burst Reed-Solomon. This code can detect and correct single- and double-burst errors of the maximum size listed below:

Sector Size (# of bytes)	Detection Capability (# of bits)		Correction Capability (# of bits)		# of Check Bytes
	Single Bursts	Double Bursts	Single Bursts	Double Bursts	
128	49	16	25	9	10
256	49	16	25	9	10
512	81	24	41	17	15

External ECC

The HDC features external ECC to allow schemes other than CRC-CCITT or Reed-Solomon. External ECC can only be used for the protection of data fields. Three lines (ECC < 1:0 > and ECCERR) simplify interfacing the external ECC hardware. ECC < 1:0 > present the status of the HDC to allow the external ECC to run synchronously. The status is coded in Gray code; only one bit changes when going from one state to the next (Figure 26).

In the IDLE state, no data field of a sector is written or read. The external ECC should be inactive.

RESET should reset the external ECC to prepare itself for an ECC process. At the end of the data mark, while reading or writing the last bit, the status lines change into the GENERATE state.

On the next rising edge of the RD/REF CLK, the external ECC must be prepared to receive valid data on either the RDDAT or WTDAT lines (depending on whether RG or WG is asserted). The external ECC must generate the check bytes. When reading or writing the last bit of the data field, the lines change to the CHECK state.

CHECK enables the external ECC either to multiplex the check bytes on WRDAT (WG active) or to compare the generated check bytes with the bytes read from RDDAT (RG active). With the external ECC, a programmable number of check bytes can be added to the data field of a sector (1 to 256 bytes).

On completion of the check byte field, at the last bit of the last check byte, the status lines change back to the IDLE state. On the next rising edge of the RD/REF CLK, the IDLE state will be in effect. During the Postamble2 section following the check bytes, the ECCERR pin will be sampled by the HDC for an "Error Found" signal from the external ECC. If the ECCERR pin remains inactive throughout the Postamble2 field, then the HDC assumes that the data is valid. If the ECCERR line is activated at any time during the Postamble2 field, then the HDC assumes that an error occurred in the data field.

INTERFACING

SYSTEM INTERFACE

For both Slave Mode and Master Mode the system bus interface can be programmed for byte (B/ \bar{W} High) or word (B/ \bar{W} Low) transfers as shown in Figure 5.

Slave Mode

In Slave Mode, the host CPU can access the five internal registers of the HDC. A_0 to A_3 indicate the address of the internal register (Figure 4). In Byte Mode, the High byte is accessed if A_0 is High and the Low byte is accessed if A_0 is Low. In Byte Mode, \bar{BHE} is ignored. The HDC asserts \overline{READY} to indicate that it is ready to complete the access.

Master Mode

The HDC is in Master Mode when it controls the system bus. To request the mastership on the system bus, the HDC asserts Bus Request (BREQ). The bus is granted to the HDC when Bus Acknowledge (BACK) is active. The HDC keeps BREQ asserted until it releases the bus after finishing a DMA burst of programmable length or when the burst is preempted by removing BACK.

A Byte transfer occurs in Word Mode when only one byte remains to be transferred or when the system address is odd. The throttling of DMA transfers on the system bus is controlled by the Mode Register. The HDC inserts a programmable number of software Wait States into the DMA bus cycle. Additionally, it inserts hardware Wait States until the memory asserts \overline{READY} .

Upper Address Latch Enable (ALEN) may latch the upper address word (A_{16} to A_{31}) in an external address latch. The upper address is only updated if a change demands this update.

Interrupts

The HDC interrupts the host CPU when it has completed the initialization procedure executed after a hardware or software reset or when it has completed a command chain. The initialization interrupt cannot be disabled. The interrupt on command chain completion can be enabled or disabled by the Interrupt Mask bit in the Mode Register.

DISK CONTROL INTERFACE

The Disk Control Interface selects drives and heads and controls the head positioning. It is programmable either to provide a floppy disk type of interface or to conform with the ST506 drive interface standard.

Drive Selection

Drives are de-selected when \overline{SELEN} is High. The two bits $DRIVE < 1:0 >$ select one of up to four drives. $DRIVE < 1:0 >$ are valid when \overline{SELEN} is Low. \overline{SELEN} remains Low as long as the drive is selected. The selected drive acknowledges the selection by activating \overline{DREADY} . If \overline{SELEN} is not acknowledged within 2^{16} clocks, then the HDC assumes that the selected drive is not present and generates a time-out error. If \overline{FAULT} is asserted after activating \overline{DREADY} , then the HDC de-selects the drive and generates a fault error.

Head Positioning

Seek operations are performed via the lines STEP, DIRIN, SEEKCOM, RTZ, and TRK0. Normal seeks pulse the STEP line to move the head to the desired track. Restore may pulse the STEP or RTZ line to move the head to track 0. DIRIN specifies the direction in which the head should move on SEEK pulses.

SEEKCOM is asserted by the drive to indicate that the head has moved to the desired track. Once the drive has acknowledged the completion of a seek by activating SEEKCOM, it must keep SEEKCOM active as long as it is selected or until it receives another seek command; otherwise the HDC issues a drive fault error. When executing the restore or seek commands, the drive must acknowledge the first STEP pulse or the RTZ pulse (SEEKCOM pulsed Low) within 2^{16} clocks or the HDC will generate a seek error.

Write Protect

The Write Protect line is sampled just prior to execution of a WRITE or FORMAT command. If the line is High, the command is aborted.

INTERFACE SIGNALS

V_{CC1}, V_{CC2} — +5V Power Supply
 V_{SS1}, V_{SS2} — Ground

SYSTEM INTERFACE LINES

CLK — System Clock (Input)

CLK is a TTL-compatible clock input to time DMA transfers and disk control operations (seeks).

\overline{RD} — Read (Input/Output, Active Low)

Read is a bidirectional, active Low, three-state signal. A Low on this line indicates that the CPU or HDC is performing an I/O or memory read cycle. When the HDC is in Slave Mode, this is an input signal used by the CPU to read the internal registers of the HDC. When the HDC is the bus master, this signal is an output used by the HDC to access data from memory. \overline{RD} and \overline{WR} must not be active simultaneously.

\overline{WR} — Write (Input/Output, Active Low)

Write is a bidirectional, active Low, three-state signal. A Low indicates that the CPU or HDC is performing an I/O or memory write cycle. When the HDC is in Slave Mode, it is an input signal used by the CPU to load the internal registers of the HDC. When the HDC is Bus Master, this signal is an output used by the HDC to write data into system memory. \overline{RD} and \overline{WR} must not be active simultaneously.

ALE — Address Latch Enable (Output, Active High)

The trailing edge of ALE latches the lower address word (A_0 to A_{15}) into the external address latch.

ALEN — Upper Address Latch Enable (Output, Active High)

The trailing edge of ALEN latches the upper address word (A_{16} to A_{31}) into the external address latch. The HDC executes Upper Address latch cycles as necessary to minimize bus occupancy. The address is updated when a new command is executing or whenever the upper address for the current bus cycle differs from the address of the previous bus cycle.

DT/\overline{R} — Data Transmit/Receive (Output, Three-State)

When the HDC is bus master, a High on this output indicates that data is being transmitted from the HDC. A Low on this output indicates that data is being transferred into the HDC. This output is three- stated when the HDC is not in control of the system bus.

DEN — Data Enable (Output, Active Low, Three-State)

When the HDC is bus master, a Low on this output indicates that data is driven on the Address/Data bus or the Address/Data bus is three- stated for receiving data. This output is three-stated when the HDC is not in control of the system bus.

\overline{BHE} — Byte High Enable (Input/Output, Active Low)

\overline{BHE} is a bidirectional, active Low signal to enable data onto the most significant byte of the data bus (AD_{15} – AD_8). \overline{BHE} is Low when data is to be accessed on the high portion of the bus.

\overline{BHE}	A_0	Size
L	L	Whole word
L	H	Upper byte
H	L	Lower byte
H	H	Reserved

When the HDC is a bus master, this pin is an output. It is an input when the HDC is in Slave Mode. \overline{BHE} is disabled and ignored when the HDC is strapped to a byte interface.

$AD < 15:0 >$ — Address/Data Bus (Input/Output, Active High)

The Address/Data Bus is a time-multiplexed, bidirectional, three- state, 16-bit bus used for all system transactions. A logic High on the bus corresponds to a "1" and a logic Low corresponds to a "0". AD_0 is the least significant bit. The presence of an address is defined by ALE or ALEN. When ALE is High, the bus contains the Lower Address bits A_0 to A_{15} . When ALEN is High, the bus contains Upper Address bits A_{16} to A_{31} . The 32-bit address allows the HDC to direct linear addressing of 4 GBytes.

The presence of data is indicated by \overline{RD} and \overline{WR} . When the HDC is in Slave Mode \overline{RD} and \overline{WR} may be asynchronous to the system clock (CLK). In Master Mode the Address/Data Bus is driven synchronously using a four-cycle bus transfer.

A_0 — Address Line 0 (Input, Active High)

This pin selects between the odd byte (High) and the even byte (Low) of the internal registers. It is used only when the HDC is in Slave Mode.

$A < 3:1 >$ — Address Line 1 to 3 (Input, Active High)

When the HDC is in Slave Mode, these lines are the address inputs selecting one of the internal registers. These lines are ignored when the HDC is bus master.

\overline{READY} — Ready (Input/Output, Open Drain, Active Low)

When the HDC is bus master, this is an input to extend the bus cycle for slow memories and peripheral devices. When the HDC is in Slave Mode, this is an output indicating that the HDC is ready to complete the bus transfer. The \overline{READY} input may be synchronous or asynchronous depending on the programming of the A/\overline{S} strap.

BREQ — Bus Request (Output, Active High)

The HDC activates BREQ to request the control of the system bus.

BACK — Bus Acknowledge (Input, Active High)

BACK acknowledges the bus request of the HDC, indicating that the CPU has relinquished the system bus to the HDC. Since BACK is internally synchronized, transitions on BACK do not have to be synchronous with the HDC clock. BACK may be removed at any time to make the HDC release the bus. If the HDC DMA is preempted by removing BACK, the HDC will release BREQ for two clock cycles so that external devices may gain the mastership on the system bus.

INTR — Interrupt Request (Output, Active High)

INTR is activated when the HDC requires service by the CPU. Interrupt Request is reset whenever the status half of the Status/Command Register (SCR) is accessed.

\overline{CS} — Chip Select (Input, Active Low)

The host processor activates \overline{CS} to enable a Slave Mode access, to read or write the internal registers of the HDC. This pin is ignored when the HDC is bus master.

B/\overline{W} — Byte/ \overline{Word} Strap (Input)

This pin selects either a byte (8-bit) or word (16-bit) interface. When a byte interface is selected, only AD<7:0> are used for data transfers and all operations are then byte operations. This pin must be strapped to either V_{CC} or V_{SS} .

V_{CC} = byte interface
 V_{SS} = word interface

A/\overline{S} — Asynchronous/ \overline{S} ynchronous Ready Strap (Input)

This line determines whether the \overline{READY} input is synchronous or asynchronous. When this line is strapped High, the HDC internally synchronizes the \overline{READY} line to the system clock. When the line is strapped Low, the HDC does not synchronize \overline{READY} . It must be synchronized to the system clock externally.

V_{CC} = asynchronous \overline{READY}
 V_{SS} = synchronous \overline{READY}

RESET — Reset (Input, Active High)

When RESET is active all outputs lines are inactive. Three-state outputs are floating. Inputs are ignored. A RESET pulse makes the chip enter the initialization procedure. Upon completion of initialization, an interrupt request will be issued. INTR will go High. If the user attempts to read from or write to the HDC prior to completion of reset, the ready line will remain inactive until the reset is completed, causing the CPU to wait.

DISK INTERFACE LINES

\overline{SELEN} — Select Enable (Output, Active Low)

\overline{SELEN} enables the drive specified by DRIVE<1:0>. When Low, DRIVE<1:0> are valid. When High, no drive is selected. A selected drive should respond with \overline{DREADY} .

DRIVE<1:0> — Drive Address (Output, Active High)

These two lines in conjunction with \overline{SELEN} determine the drive to be selected. The drive numbers are encoded as follows:

DRIVE<1>	DRIVE<0>	Drive Selected
L	L	Drive 0
L	H	Drive 1
H	L	Drive 2
H	H	Drive 3

$\overline{PCEN/S/\overline{D}}$ — Pre-compensation Enable/Single/ \overline{Double} (Output, Active High)

For all drive formats, this line signals when pre-compensation should be used. It enables pre-compensation if High and disables pre-compensation if Low. In addition, for floppy formats it selects either the single or double density recording formats. The falling edge of \overline{SELEN} may be used to latch Single/Double. A latched Low indicates double-density and a latched High single-density.

\overline{DREADY} — Drive Ready (Input, Active Low)

Drive Ready indicates that the currently selected drive is ready to Read, Write, or Seek. It must be asserted within 217 clocks after \overline{SELEN} is asserted by the HDC. Once asserted by the selected drive, any negation of this line causes the current IOPB to be aborted. \overline{DREADY} is ignored while \overline{SELEN} is High.

FAULT — Fault (Input, Active High)

FAULT indicates a fault of the selected drive. Fault must be inactive as long as \overline{DREADY} is active. If it is ever asserted by the selected drive, the current IOPB is aborted and the drive de-selected.

WRPROT — Write Protect (Input, Active High)

WRPROT is sampled after receipt of \overline{DREADY} during any IOPB command which involves a write to the disk. It is ignored during "Read Only"-type commands.

SEEKCOM — Seek Complete (Input, Active High)

SEEKCOM indicates that the drive is on track and that the heads have settled (head settling applies only to floppy disk drives). This line is sampled and verified High before any seek is issued. A High indicates "Seek Complete." It is also used as an indication of head load completion for floppy drives.

STEP — Step (Output, Active High)

The HDC pulses the STEP line to move the head from one track to the next track. The width and spacing of pulses is programmable. This allows easy upgrades to higher performance drives.

DIRIN — Direction In (Output, Active High)

DIRIN indicates the direction the head should move on STEP pulses. When High, the head should move toward higher track numbers (In, or towards the disk spindle). When Low, it should move towards lower track numbers (Out).

RTZ — Return to Zero (Output, Active High)

A pulse on the RTZ output should recalibrate the head to track 0. Optionally, the HDC may recalibrate the drive by issuing STEP pulses until track 0 is reached (TRK0 becomes active). The RTZ pulse has the same width as the STEP pulse. The drive should assert SEEKCOM as an indication of the completion of the requested recalibration.

TRK0 — Track 0 (Input, Active High)

The selected drive should assert TRK0 whenever the head is positioned over track 0.

HLD/HEADSEL <3> — Head Load/Head Select <3> (Output, Active High)

For floppy drives, this line functions as a head load signal. It is active as long as the head should be loaded. SEEKCOM is sampled eight clocks after the assertion of HLD. If Low, the HDC will then wait for it to go High. If High, the HDC assumes that the heads are already loaded. For hard disk drives, this line is the most significant bit of the head number.

HEADSEL <2:0> - Head Select (Output, Active High)

These lines output the lower three bits of the head number. The encoding is standard binary as follows:

RWC — Reduced Write Current (Output, Active High)

When the drive currently selected is configured for a floppy disk or ST506 interface, this line indicates that the head is positioned over an inner track where the Write Current should be reduced.

INDEX — Index (Input, Active High)

INDEX marks each revolution of the disk. The HDC only notes the Low to High transition. INDEX should be valid as long as DREADY is asserted.

AMC — Address Mark Control (Output, Active High)

The HDC asserts AMC in conjunction with RG or WG to command the data separator to write or detect address marks. When RG is asserted, the HDC wants the data separator to search for the next address/data mark. When WG is asserted, the HDC wants the data separator to write an address mark. In both cases, the data separator should acknowledge completion by asserting AMF.

AMF — Address Mark Found (Input, Active High)

The data separator asserts AMF to response to AMC.

RG — Read Gate (Output, Active High)

RG indicates that a disk read is in progress. It commands the Phase Locked Loop (PLL) of the data separator to lock the RD/REF CLK to the serial data from disk. This output changes synchronously with the RD/REF CLK.

WG — Write Gate (Output, Active High)

WG indicates that the HDC is writing to the disk. When WG is asserted disk data is strobed out synchronously with RD/REF CLK.

RD/REF CLK — Read/Reference Clock (Input)

RD/REF CLK is the data clock for sampling read data and strobing out write data. It is assumed valid if the following conditions are met: SELEN = Low, DREADY = Low, SEEKCOM = High, and FAULT = Low. While valid, this clock should be free from any glitches.

RDDAT — Read Data (Input)

RDDAT is the NRZ data input from the disk. The HDC samples RDDAT with the rising edges of RD/REF CLK. Therefore, the data should be set up by the data separator at the falling edge of RD/REF CLK.

WRDAT — Write Data (Output)

WRDAT is the NRZ data output to the disk. Transitions occur on the falling edge of RD/REF CLK.

FAMD/ECCERR — Floppy Address Mark Detect/ECC Error (Input, Active High)

This signal indicates a data read error when external ECC is used. For single-density floppy formats, it indicates detection of a deleted data mark.

FAM <1:0>/ECC <1:0> — Floppy Address Mark/ECC Control (Output, Active High)

These dual-function lines either control external ECC (hard disk format, external ECC enabled) or indicate the type of address/data mark to be used (single- and double-density floppy formats, AMC High).

ECC Control:

00 = Idle	No operation in the external ECC.
01 = Reset	External ECC should reset and prepare itself for an operation.
11 = Generate	Whether reading or writing, the external ECC should strobe data in and generate a check sum.
10 = Check	When reading, this state indicates that the ECC should accept the check sum from the disk. When writing, it should gate the check sum to the disk.

These states always proceed in the Gray code progression shown above: 00-01-11-10-00. The nominal state of the HDC is 00:Idle.

Floppy Address Mark:

Double-Density	00 = Index Address Mark (IAM)
	XX = Data or Header Address Mark (DAM, IDA)
Single Density	00 = Index Address Mark (IAM)
	01 = ID Address Mark (IDAM)
	10 = Data Address Mark (DAM)
	11 = Deleted Data Address Mark (DDAM)

Floppy Address Mark takes precedence over ECC Control.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65 to +150°C
Temperature Ambient Under Bias	-55 to +125°C
Supply Voltage to Ground Potential Continuous	-0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	-0.5V to +V _{CC}
DC Input Voltage	-0.5 to +7.0V

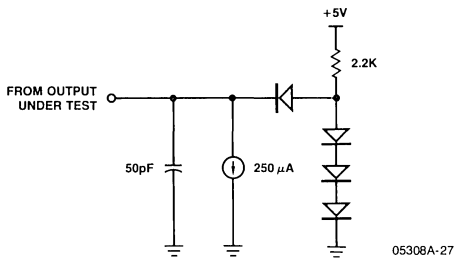
DC CHARACTERISTICS

T_A = 0 to +70°C, V_{CC} = 5V ±5%

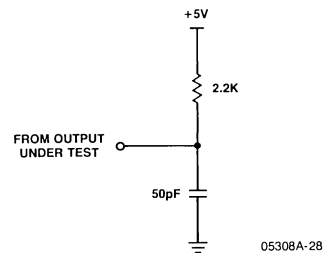
Parameters	Description	Test Conditions	Min	Max	Units
V _{IL}	Input Low Voltage		-0.5	0.8	V
V _{IH}	Input High Voltage		2.0	V _{CC} + 0.5	V
V _{OL}	Output Low Voltage	I _{OL} = 3.2mA		0.4	V
V _{OH}	Output High Voltage	I _{OH} = -250μA	2.4		V
I _I	Input Leakage Current	V _{SS} ≤ V _I ≤ V _{CC}		±10	μA
I _{OZ}	Output Leakage Current	V _{CC} ≤ V _O ≤ V _{SS} + .40		±10	μA
I _{CC}	Supply Current				mA
C _{IN}	Input Capacitance	Unmeasured Pins Returned to Ground. f = 1MHz Over Specified Temperature Range			pF
C _{OUT}	Output Capacitance				pF
C _{I/O}	Bidirectional Capacitance				pF

Standard Test Conditions

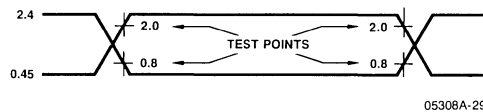
Standard Test Load



Open Drain Test Load

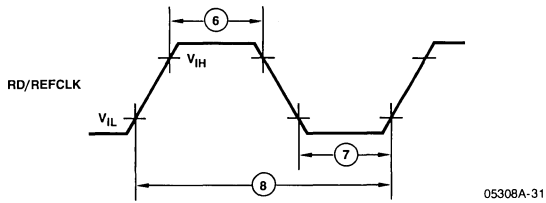
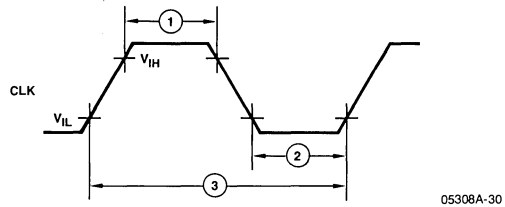


Input Waveform



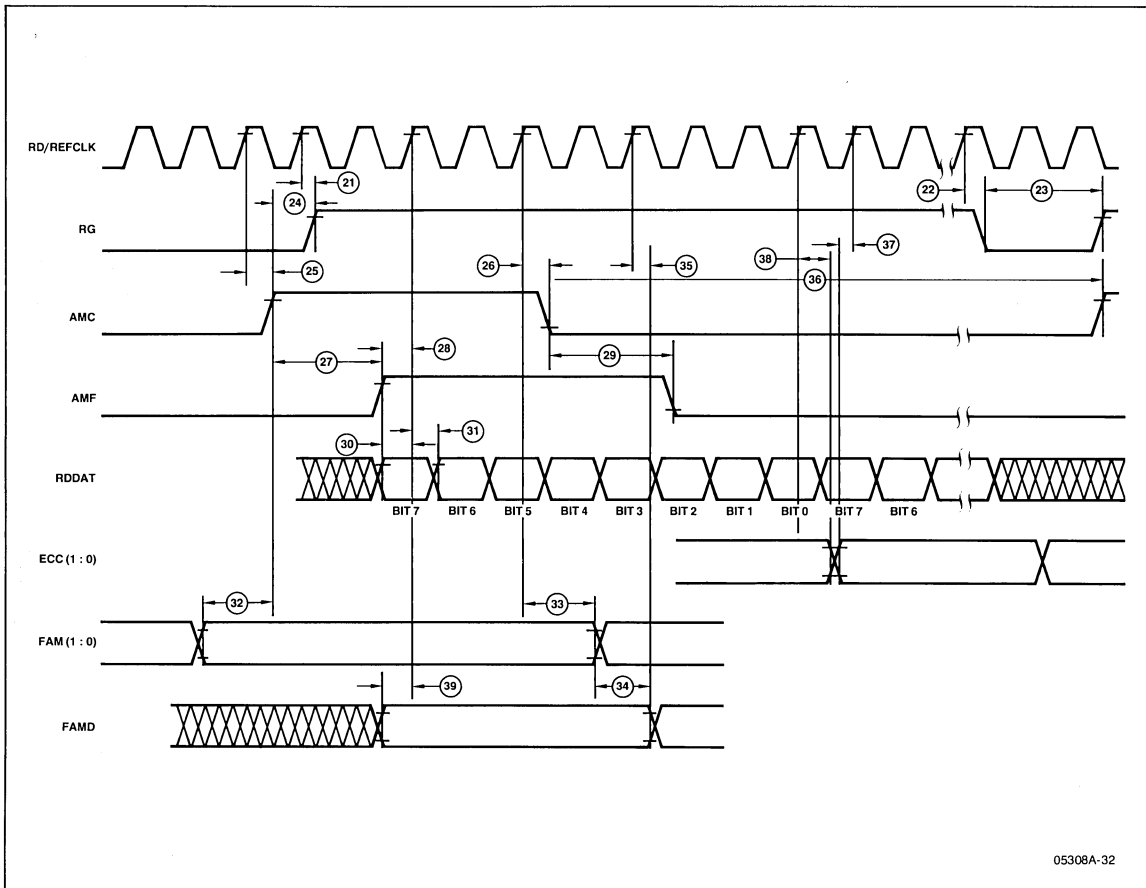
SYSTEM CLOCK AND RD/REFCLK

Number	Parameter	Description	Min	Max
1	t_{CPH}	System Clock High Time		
2	t_{CPL}	System Clock Low Time		
3	t_{CPC}	System Clock Cycle Time		
6	t_{DCPH}	Disk Clock High Time		
7	t_{DCPL}	Disk Clock Low Time		
8	t_{DCPC}	Disk Clock Cycle Time		



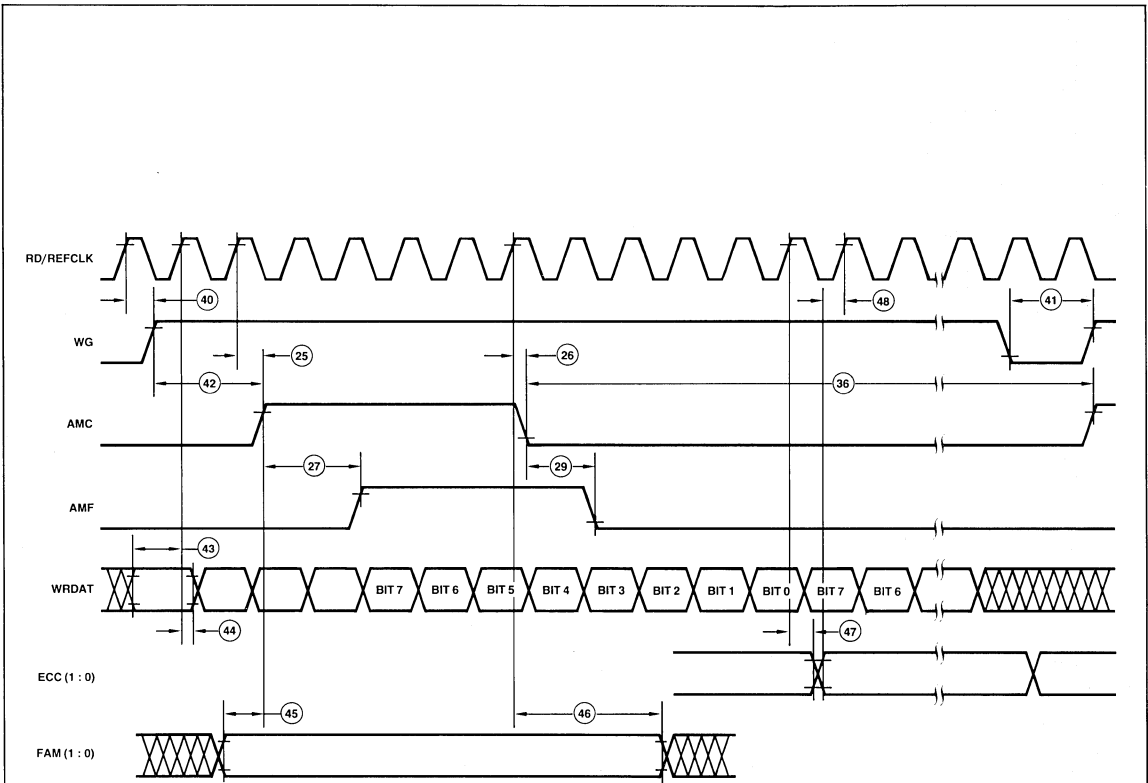
DISK DATA READ

Number	Parameter	Description	Min	Max
21	t_{DRGA}	RD/REFCLK to RG Active		
22	t_{DRGI}	RD/REFCLK to RG Inactive		
23	t_{RGDW}	RG Dwell		
24	t_{AMCRG}	AMC to RG		
25	t_{DAMCA}	RD/REFCLK to AMC Active		
26	t_{DAMCI}	RD/REFCLK to AMC Inactive		
27	t_{AMCAMF}	AMC Active to AMF Active		
28	t_{SUAMF}	AMF Setup to RD/REFCLK		
29	$t_{DAMCAMF}$	AMC Inactive to AMF Inactive		
30	t_{DATSCC}	Data Setup to RD/REFCLK		
31	t_{DATHD}	Data Hold to RD/REFCLK		
32	t_{SUFAM}	FAM (1 : 0) Setup to AMC Active		
33	t_{HDFAM}	FAM (1 : 0) Hold to RD/REFCLK		
34	t_{HDFAMD}	FAM (1 : 0) Change to FAMD Inactive		
35	t_{DFAMD}	RD/REFCLK to FAMD Inactive		
36	t_{AMCDW}	AMC Dwell		
37	t_{SUBCC}	ECC (1 : 0) Change to RD/REFCLK Setup		
38	t_{HDECC}	RD/REFCLK to ECC (1 : 0) Hold		
39	t_{SUFAMD}	FAMD Setup to RD/REFCLK		



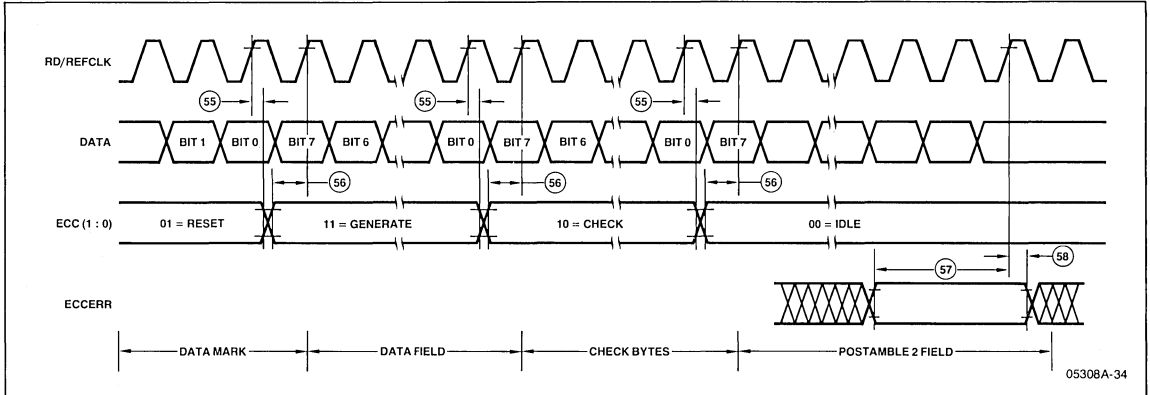
DISK DATA WRITE

Number	Parameter	Description	Min	Max
40	t_{DWG}	RD/REFCLK to WG Active		
41	t_{WGDW}	WG Dwell		
42	t_{DWGAMC}	WG Active to AMC Active		
43	t_{SUWD}	Write Data Setup to RD/REFCLK		
44	t_{HDWD}	Write Data Hold from RD/REFCLK		
45	t_{SUFAM}	FAM (1 : 0) Setup to AMC		
46	t_{HDFAM}	FAM (1 : 0) Hold to AMC Inactive		
47	t_{HDECC}	RD/REFCLK to ECC (0 : 1) Hold		
48	t_{SUBCC}	ECC (1 : 0) Setup to RD/REFCLK		



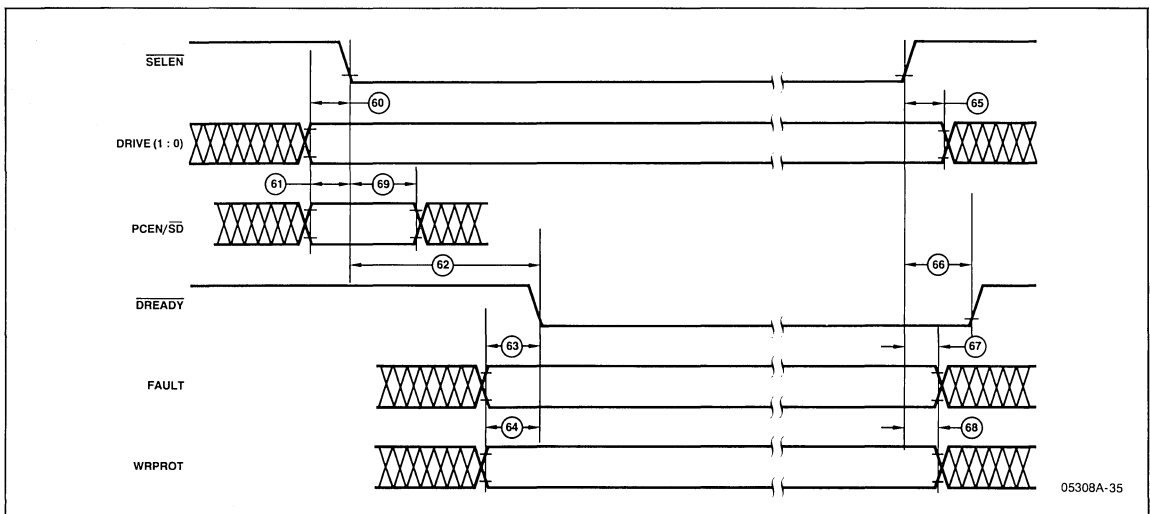
EXTERNAL ECC INTERFACE

Number	Parameter	Description	Min	Max
55	t_{ECCHD}	ECC (1 : 0) Hold to RD/REFCLK		
56	t_{ECCSU}	ECC (1 : 0) Setup to RD/REFCLK		
57	t_{ERRSU}	ERR Setup to Last RD/REFCLK (In Post 2)		
58	t_{ERRHD}	ERR Hold to Last RD/REFCLK (In Post 2)		



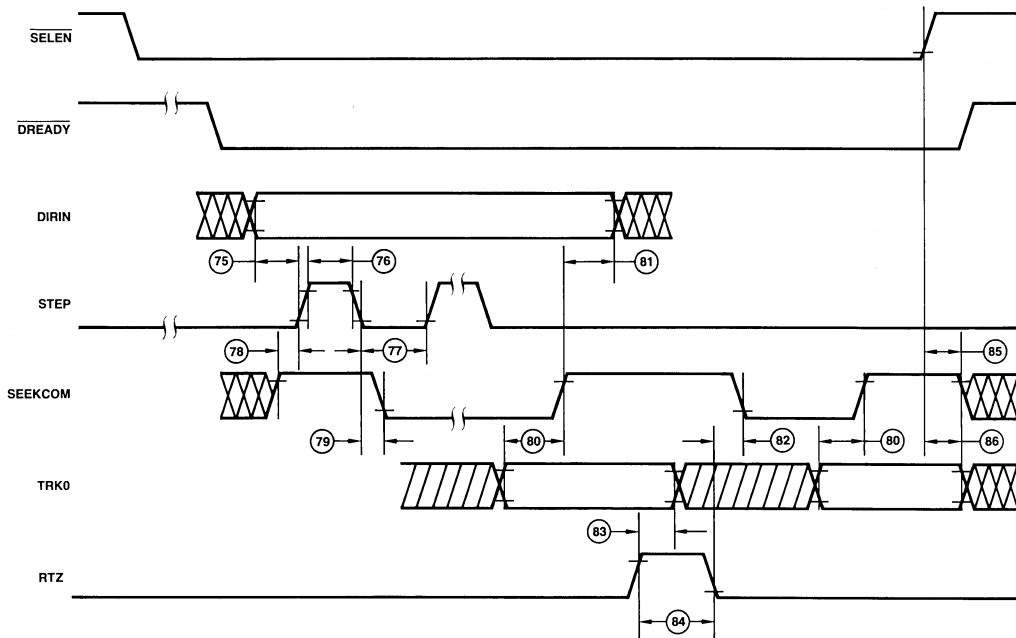
DISK INTERFACE

Number	Parameter	Description	Min	Max
60	t_{DRSU}	DRIVESEL (1 : 0) Setup to \overline{SELEN} Active		
61	t_{PCSU}	PCEN/ \overline{SD} Setup to \overline{SELEN} Active		
62	$t_{SELDRDY}$	\overline{SELEN} Active to \overline{DREADY} Active		
63	t_{FLTSU}	Fault to \overline{DREADY} Setup		
64	t_{WPSU}	WRITEPROT to \overline{DREADY} Setup		
65	t_{DSHD}	\overline{SELEN} Inactive to DRIVESEL (1 : 0) Hold		
66	t_{DRDYHD}	\overline{SELEN} Inactive to \overline{DREADY} Hold		
67	t_{FLTHD}	\overline{SELEN} Inactive to FAULT Hold		
68	t_{WPHD}	\overline{SELEN} Inactive to WRITEPROT Hold		
69	t_{PCHD}	PCEN/ \overline{SD} Hold		



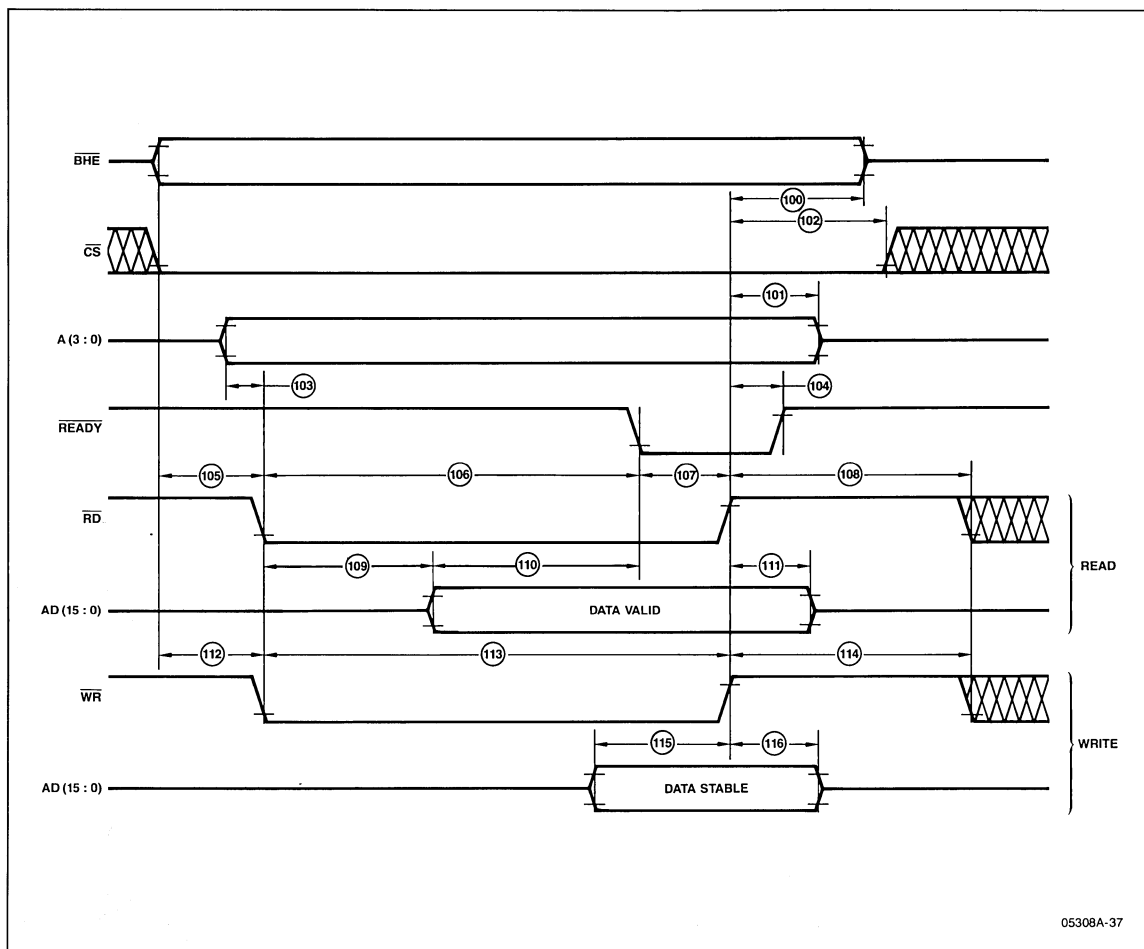
DISK INTERFACE

Number	Parameter	Description	Min	Max
75	t _{DIRSU}	DIRIN Setup		
76	t _{STPWD}	STEP High Width	User Programmable	
77	t _{STLW}	STEP Low Width	User Programmable	
78	t _{SKSU}	SEEKCOM Setup to STEP		
79	t _{STPSK}	STEP Low to SEEKCOM Low		
80	t _{TRKSK}	TRK0 to SEEKCOM Setup		
81	t _{SKDIRI}	SEEKCOM to DIRIN Inactive Hold		
82	t _{RTZSK}	RTZ Low to SEEKCOM Low		
83	t _{RTZTRKI}	RTZ Active to TRK0 Invalid		
84	t _{RTZWD}	RTZ Pulse Width	User Programmable	
85	t _{SELSKI}	SELEN Invalid to SEEKCOM Invalid		
86	t _{SELTRKI}	SELEN Invalid to TRK0 Invalid		

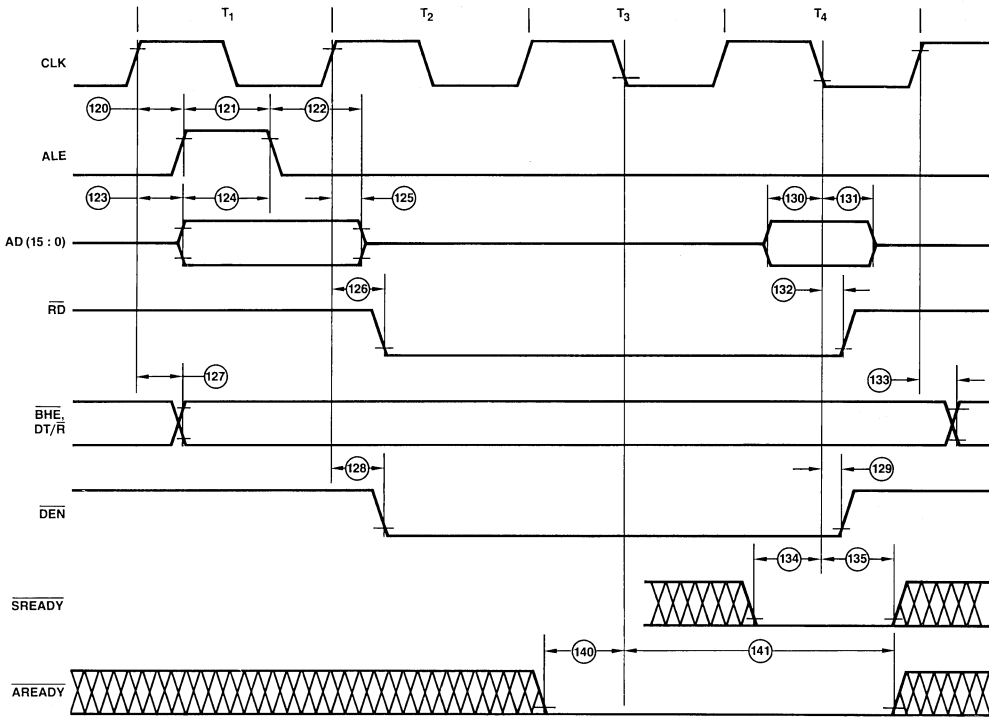


BUS SLAVE READ/WRITE

Number	Parameter	Description	Min	Max
100	t_{HHRW}	\overline{BHE} to \overline{RD} , \overline{WR} Hold		
101	t_{HADD}	Address Hold		
102	t_{HCS}	\overline{CS} Hold Time		
103	t_{SUADD}	Address Setup		
104	t_{NRDY}	\overline{READY} Negate Time		
105	$t_{CSR D}$	\overline{CS} , \overline{BHE} , to \overline{RD} Setup		
106	t_{RRDY}	\overline{READY} Response Time		
107	t_{HSTB}	Strobe Hold		
108	t_{RRCV}	Read Recovery		
109	t_{DATON}	Data Turn On		
110	t_{SUDAT}	Data Setup		
111	t_{DATOFF}	Data Turn-Off		
112	t_{CSWR}	\overline{CS} , \overline{BHE} , to \overline{WR} Setup		
113	t_{STBWR}	\overline{WR} Strobe Width		
114	t_{WRCV}	Write Recovery		
115	t_{SUDATW}	Data Write Setup		
116	t_{HDDATW}	Data Write Hold		

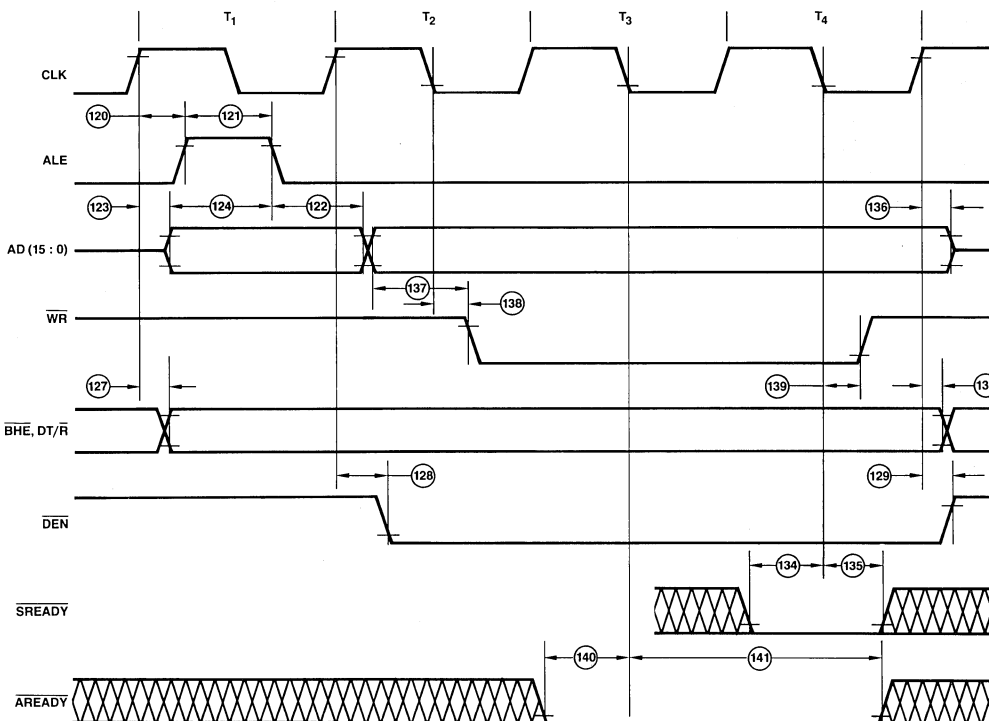


BUS MASTER READ



05308A-38

BUS MASTER WRITE



05308A-39

BUS MASTER READ

Number	Parameter	Description	Min	Max
120	t _{DALE}	CLK to ALE Active		
121	t _{WALE}	ALE Pulse Width		
122	t _{ADDHD}	Address (15 : 0) Hold Time		
123	t _{DADD}	CLK to Address (15 : 0) Valid		
124	t _{SUADD}	Address (15 : 0) Setup		
125	t _{IADD}	CLK to Address (15 : 0) Invalid		
126	t _{DRD}	CLK to \overline{RD} Active		
127	t _{VCNTL}	CLK to \overline{BHE} , $\overline{DT/R}$ Valid		
128	t _{DDEN}	CLK to \overline{DEN} Active		
129	t _{IDEN}	CLK to \overline{DEN} Inactive		
130	t _{SUDAT}	Data In Setup		
131	t _{HDDAT}	Data In Hold		
132	t _{IRD}	CLK to \overline{RD} Negate		
133	t _{ICNTL}	\overline{BHE} , $\overline{DT/R}$ Negate		
134	t _{SURBY}	SREADY Setup		
135	t _{HDRDY}	SREADY Hold		

BUS MASTER WRITE

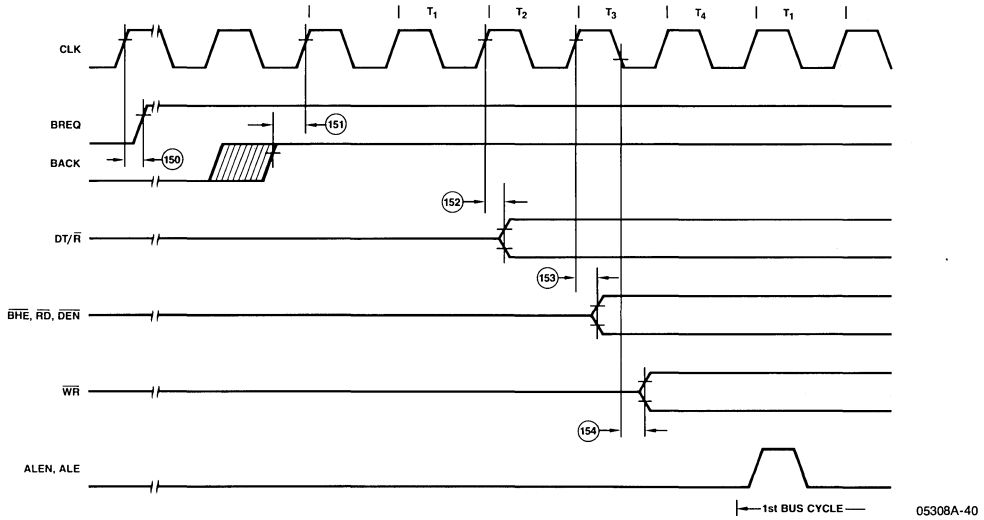
Number	Parameter	Description	Min	Max
136	t _{IDO}	Data Out Invalid		
137	t _{SUDT}	Data Out Setup		
138	t _{DWR}	CLK to \overline{WR} Active		
139	t _{HDWR}	CLK to \overline{WR} Inactive		

\overline{AREADY}

Number	Parameter	Description	Min	Max
140	t _{ARSU}	\overline{AREADY} Setup to CLK Low		
141	t _{ARHD}	\overline{AREADY} Hold to CLK Low		

BUS REQUEST

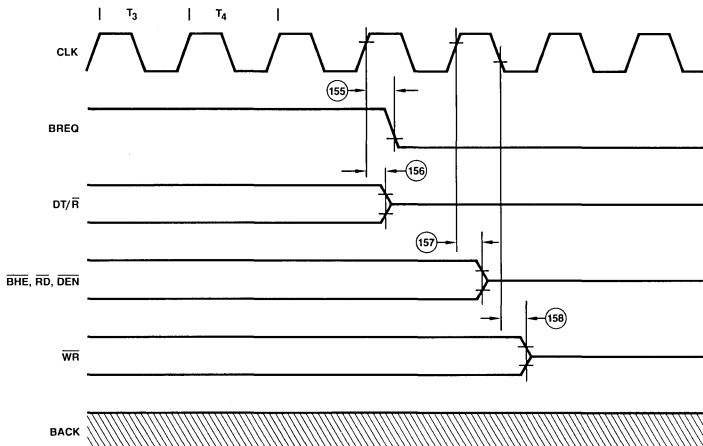
Number	Parameter	Description	Min	Max
150	t_{DBR}	CLK to BREQ Active		
151	t_{DBA}	BACK to CLK Setup		
152	t_{DDTR}	CLK to DT/ \bar{R} Valid		
153	t_{DCNTL}	CLK to \overline{BHE} , \overline{RD} and \overline{DEN} Valid		
154	t_{DWR}	CLK to \overline{WR} Valid		



05308A-40

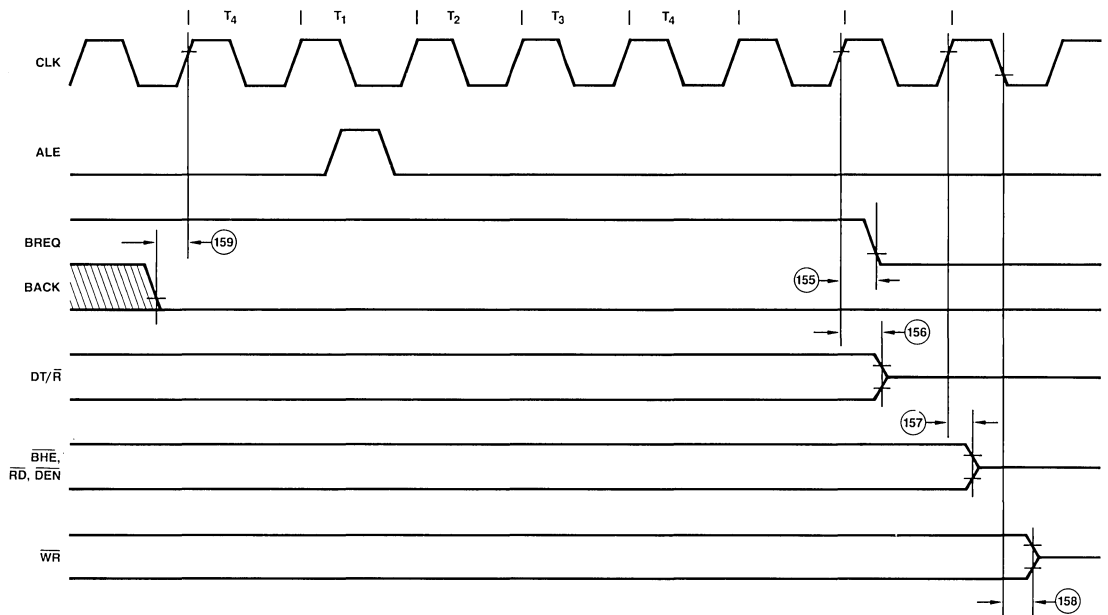
BUS RELEASE

Number	Parameter	Description	Min	Max
155	t_{IBREQ}	CLK to BREQ Inactive		
156	t_{IDTR}	CLK to DT/ \bar{R} Invalid		
157	t_{ICNTL}	CLK to \overline{BHE} , \overline{RD} , and \overline{DEN} Invalid		
158	t_{IWR}	CLK to \overline{WR} Invalid		
159	t_{SBA}	BACK to CLK Setup		



05308A-41

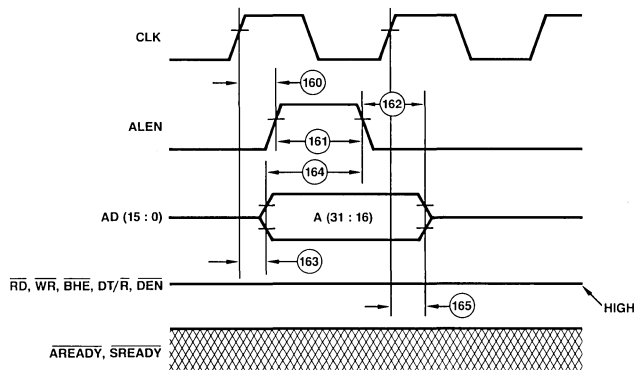
PREEMPTIVE BUS RELEASE



05308A-42

UPPER ADDRESS LATCH

Number	Parameter	Description	Min	Max
160	t_{DALEN}	CLK to ALEN Active		
161	t_{WALEN}	ALEN Pulse Width		
162	t_{DADDH}	AD (15 : 0) Hold Time		
163	t_{DADD}	CLK to AD (15 : 0) Valid		
164	t_{SUADD}	AD (15 : 0) Setup Time		
165	t_{IADD}	CLK to AD (15 : 0) Invalid		



05308A-43



Am9581

Floppy/Hard Disk Data Separator ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- On-chip Phase-Locked-Loop (PLL)
- On-chip MFM/FM Encoder/Decoder
- Supports: 4 to 16Mbits/sec MFM data rates for Hard Disks
125 to 500Kbits/sec Single Density (FM) and 250K to 1Mbit/sec Double Density (MFM) for Floppy Disks
- On-chip Write Pre-compensation
- On-chip Address Mark Generation/Detector
- Provides Clock extracted from the input data for Run-Length-Limited codes

GENERAL DESCRIPTION

The Am9581 Floppy/Hard Disk Data Separator (DDS) is a single-chip solution to several functions associated with reading and writing information to disk drive memory systems. The Am9581 is divided into three sections: read, write, and control.

The read section contains an on-board Phase-Locked-Loop (PLL) to provide a clock signal that tracks the FM/ MFM serial data read off the disk. This data is then fed into the MFM/FM decoder to be converted into NRZ data. Also in this section is the Address Mark Detector for both floppy and hard disks.

The write section contains an encoder to serialize NRZ data and its reference clock into a single bit stream of data (MFM

or FM) to store on the disk. Also in the write section are the Address Mark Generation and the Write Pre-compensation sections. Each sector on a disk contains several Address Marks. These enable the controller to identify sector types, sector numbers and data fields. The Write Pre-compensation section is used to overcome the problem of bit-shifting caused by the method of storage on the media.

The control section handles mainly the drive select and also the head loading logic for floppy disks.

Used in conjunction with the Am9580 Hard Disk Controller (HDC) the chip set provides the total solution for ST-506 and ST-412HP disk interface.

CONNECTION DIAGRAM Top View 48-Pin

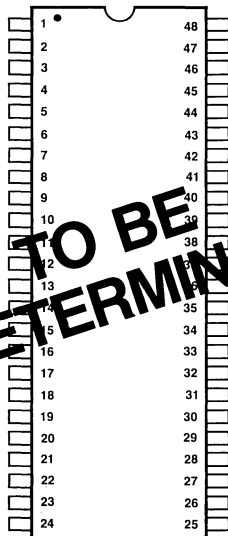
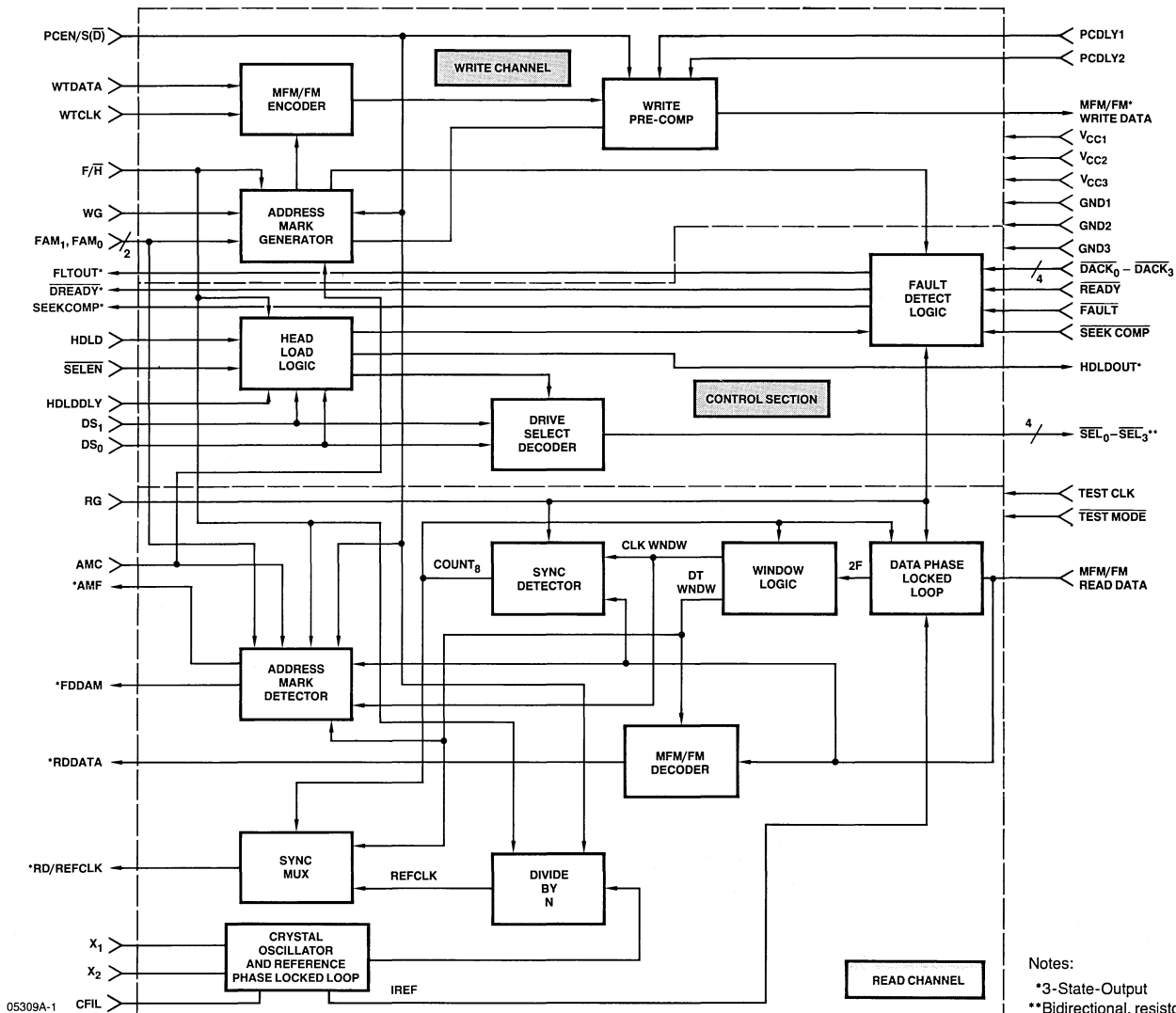


Figure 2. DDS Block Diagram



Notes:
 *3-State-Output
 **Bidirectional, resistor pull up

PIN DESCRIPTION

WRITE SECTION

PCEN/S(\bar{D})	<p>Pre-Compensation Enable/Single (Double) Density (Input)</p> <p>This pin has two functions which are multiplexed. When a drive is selected (\overline{SELEN} going from HIGH to LOW) the logic level on PCEN/S(\bar{D}) is stored internally. A HIGH causes single density operation. A LOW causes double density operation. If the F/\bar{H} pin is LOW, then double density or RLL hard disk operation occurs depending on FAM₀ and FAM₁.</p> <p>During a Write operation a HIGH causes data pre-compensation to take place; otherwise the data is uncompensated. If single density has been selected when \overline{SELEN} goes LOW, then PCEN has no effect and the data is always uncompensated.</p>
PCDLY1 PCDLY2	<p>Pre-Compensation Delay (Inputs)</p> <p>The ratio of resistors (R_{PC1}, R_{PC2}) connected between PCDLY1 and PCDLY2 pins and V_{CC} sets the pre-compensation delay. The range of pre-compensation delay can be set by the user from 1% to 20% of the bit cell time with an accuracy of $\pm 5\%$ of the chosen value or 1ns, whichever is greater using 1% resistors. The minimum precomp delay that can be set is 2ns.</p>
WTDATA	<p>Write Data (Input)</p> <p>NRZ data is applied to this input pin for FM or MFM encoding.</p>
WTCLK	<p>Write Clock (Input)</p> <p>Write Clock is used to synchronize the NRZ write data for magnetic recording. This pin is normally connected to the RD/REFCLK output pin. The user should note that the NRZ input data must meet setup and hold requirements to the write clock. Skew may be compensated by connecting the write clock to the delayed RD/REFCLK.</p>
WG	<p>Write Gate (Input)</p> <p>When HIGH, this line enables the WRITE CHANNEL so that writing data onto the disk is made possible. When both WG and RG (Read Gate) are HIGH, a fault condition is generated causing the FLTOUT line to go to HIGH.</p>
FAM₁, FAM₀	<p>Floppy Address Mark Select Bits (Inputs)</p> <p>These two input bits are used to select the desired Address Mark related to floppies. These bits are further qualified by F/\bar{H} (Floppy/Hard Disk input select bit) and S/\bar{D} inputs. These lines are also used to setup the chip for use with RLL codes as shown in Table 1 (see page 10).</p>
F/\bar{H}	<p>Floppy/Hard Disk Select (Input)</p> <p>When this pin is tied HIGH, the DDS chip is selected for use with single or double density floppies. When tied LOW, the DDS is selected for hard disks. This input line is also used to select the Address Marks for floppies or hard disks. The selection criteria is listed in Table 1.</p>

MFM/FM WRITE DATA	<p>Write Data (Output, 3-State)</p> <p>Encoded output data used for the actual recording process. MFM format is used for most hard disk and double density floppies and FM is used for single density floppies. This line is 3-stated when none of the drives connected to the DDS are selected.</p>
READ SECTION	
RG	<p>Read Gate (Input)</p> <p>A HIGH on this pin enables the READ CHANNEL so that processing of the read back data using the data Phase-Locked-Loop (PLL) can proceed. If both RG and WG are active, a fault condition is generated, causing FLTOUT to go HIGH.</p>
MFM/FM READ DATA	<p>Read Data (Input)</p> <p>The input to this pin is the MFM/FM encoded information read back from the disk. The Data Separator chip separates the clock and the data information from this MFM/FM data and restores it to the original NRZ format.</p>
X₁, X₂	<p>Reference Frequency (Inputs)</p> <p>These two input pins are for connections to an external crystal. An external TTL level clock source can be used instead and tied to the X₁ pin. The frequency of the crystal to be used for various modes of operation is shown in Table 1. The XTAL frequency is divided down internally to produce the necessary 1f and 2f frequencies. (The 2f reference clock is used internally only for FM encoding.)</p>
AMC	<p>Address Mark Control (Input)</p> <p>This control input line is used to generate and write the Address Marks during a WRITE operation (with WG) and detect the Address Marks during a READ operation (with RG).</p>
AMF	<p>Address Mark Found (Output, 3-State)</p> <p>Becomes active in response to an active AMC to indicate that the selected type of Address Marks specified in Table 1 have been found during a read and that an Address Mark of appropriate type has been written during a write. The line is 3-stated when none of the drives connected to the DDS are selected.</p>
FDDAM	<p>Floppy Deleted Data Address Mark (Output, 3-State)</p> <p>For single density floppies, this output pin indicates the detection of a deleted Data Address Mark. During Read operations, this status signal is generated by the Am9581 only when a request is made by the HDC. For MFM hard disks and double density floppies, this pin will always be LOW when the DDS is selected. This pin is 3-stated when none of the drives connected to DDS are selected. In RLL hard disk mode, this pin is used to output 2f clock synchronous with RDDATA.</p>
RDDATA	<p>NRZ Read Data (Output, 3-State)</p> <p>This line contains the binary NRZ data decoded from the MFM/FM READ DATA. In RLL mode, the input data on the MFM/FM READDATA pin is passed directly out to the RDDATA output without any decoding taking place.</p>

RD/REFCLK **Read/Reference Clock (Output, 3-State)**
Read/Reference clock is synchronously multiplexed such that during a READ operation, the clock source is the RDCLK which is derived from the MFM/FM READ DATA bit stream. When not doing a valid READ operation, the clock source is derived from the input to pins X₁ and X₂. The switching from RDCLK to REFCLK is a glitch-free operation. The pin is 3-stated when none of the drives connected to DDS are selected. For RLL hard disks, this pin always outputs REFCLK.

CFIL **Filter Capacitor (Input)**
The filter capacitor for the reference PLL is connected between this pin and ground.

CONTROL SECTION

HDL **Head Load (Input)**
This input pin is applicable to floppies only and is used for controlling the head loading (when HIGH) and unloading (when LOW) mechanism.

HDLDOU **Head Load to Drive (Output, 3-State)**
This is the Head Load signal to the floppy drive. When HDL from the controller chip goes HIGH, HDLDOU goes HIGH immediately. When HDL goes LOW, there is a delay (set by HDLDDLY) before HDLDOU goes LOW. Refer to the timing diagram of Figure 3 for the different cases involving the HDLDOU signal.

HDLDDLY **Head Load Delay (Input)**
A resistor R_X connected between this input pin and V_{CC}, and a capacitor C_X connected between this input pin and ground establish a time delay (selected by user) associated with the unloading of the head in floppies. This time delay is necessary so that a drive may be deselected and selected again without unloading and reloading the head. The user may set the time delay from a minimum of 5ms to a maximum of 500ms with a maximum tolerance of 0.5ms or ±5%, whichever is larger.

SELEN **Select Enable (Input)**
An active LOW signal to this pin enables the drive specified by the drive select bits DS₁, DS₀. The falling edge of SELEN along with the status of the PCEN/S(D) pin determines single or double density operation for floppies.

DS₀, DS₁ **Drive Select (Inputs)**
These two pins specify the selection of up to four drives, as indicated below:

		<u>SEL</u> PIN ACTIVATED
DS ₁	DS ₀	<u>SEL</u> ₀
LOW	LOW	<u>SEL</u> ₁
LOW	HIGH	<u>SEL</u> ₂
HIGH	LOW	<u>SEL</u> ₃
HIGH	HIGH	

SEL₀–SEL₃ **Select_{0–3} (Bidirectional, Resistor Pull Up)**
These four output lines are the decoded DS₁, DS₀ bits used to select up to four drives. When a particular SEL pin is grounded the DDS will not acknowledge a request for this drive from the HDC (all interface lines to the HDC will be tri-stated). In a typical floppy/Winchester disk

drive system with 2 DDS's each attached to 2 drives, the two remaining SEL lines are grounded. In the example on page 17, one DDS interfaces with drives 2 and 3 and has SEL₀ and SEL₁ grounded. Grounding the 2 SEL lines prevents this DDS from acknowledging requests for drives 0 and 1.

DACK₀–DACK₃

Drive Acknowledge (Schmitt Trigger Inputs)
These input pins reflect the response of an individual drive, acknowledging that it has been selected. Therefore these inputs are used with the SEL₀–SEL₃ status to test whether the drive that acknowledged is the one being selected; otherwise, a fault condition will be detected.

READY

Ready (Schmitt Trigger Input)
This input pin indicates that the drive selected is ready to READ, WRITE, or SEEK (access a track).

DREADY

Drive Ready (Output, 3-State)
This status output pin is used to indicate that the selected drive is ready to READ, WRITE or SEEK. When a fault condition is sensed by the F/HDDS this line is set LOW so that the controller can detect the fault by sensing FLTOUT. The line is 3-stated if none of the drives connected to F/HDDS are selected.

FAULT

Fault (Schmitt Trigger Input)
This pin indicates a fault condition when selecting a drive or in the drive itself. An active FAULT is considered only after the Drive Acknowledge bit corresponding to the drive selected is active LOW.

FLTOUT

Fault Out (Output, 3-State)
This output pin is a status output of the fault detection logic. The fault conditions detected are:

1. WG and RG both active.
2. Active FAULT from the selected drive.
3. Unselected drives acknowledging drive selection.
4. More than one drive acknowledge in response to a drive selection.

The pin is 3-stated when none of the drives connected to F/HDDS are selected.

SEEKCOMP

Seek Complete (Schmitt Trigger Input)
This input line indicates that a SEEK operation has successfully been completed and that the head has settled on the desired track. This signal is generated by the drive.

SEEKCOMP

Seek Complete (Output, 3-State)
This status output line is the same as SEEKCOMP for Hard Disk mode. In Floppy mode this output is driven by the Head Load Delay logic (see functional description for details). The line is 3-stated if none of the drives connected to F/HDDS are selected.

GND₁–GND₃

Ground

VCC₁–VCC₃

Power Supply (±5V)

**TEST CLK,
TEST MODE**

(Inputs)
These two lines are used to test the chip logic independent of the PLL.

FUNCTIONAL DESCRIPTION

The Am9581 simplified block diagram shown in Figure 2 is divided into three sections – (1) the CONTROL section, (2) the WRITE section, and (3) the READ section. The WRITE section and the READ sections are independent of each other and under the supervision of the CONTROL section. The functions of each section are described below.

CONTROL SECTION

This section consists of the HEAD LOAD LOGIC, DRIVE SELECT DECODER, and the FAULT DETECT LOGIC. The HEAD LOAD LOGIC is enabled only if the DDS is to be used in floppy disk drives. The HEAD LOAD LOGIC block controls the loading and unloading of the floppy disk drive head as specified in the timing diagram of Figure 3. Each of the three operations is described below.

Normal Operation

The controller selects a drive by asserting $\overline{\text{SELEN}}_{\text{LOW}}$, causing one of the SEL_{0-3} lines to be asserted. Once the drive is selected, the controller can request the DDS to load the head by asserting HDLD. The DDS responds with HDLDOUT going HIGH and asserts SEEKCOMP after a time delay (t_{HDLDDL}) set by the resistor R_X and the capacitor C_X at the HDLDDL pin. This time delay set by the user is to accommodate the settling time associated with the head loading and unloading: t_{HDLDDL} can be calculated as $(1.1 R_X C_X) \pm 5\%$.

To deselect the drive, the controller drives $\overline{\text{SELEN}}_{\text{HIGH}}$ and HDLD LOW. The actual deselection of the drive and the unloading of the head do not occur until after t_{HDLDDL} .

Same Drive Reselected

The selection of the drive and the loading of the head is the same as described in the normal operation. However, if the same drive (DRIVE 0) is deselected and selected again within the time interval defined by t_{HDLDDL} , then the head can remain loaded (HDLDOUT remaining HIGH). In this case, a different track can be accessed while the head remains loaded.

Different Drive Selected

When a drive (DRIVE 0 for example) is deselected and then a different drive (DRIVE 1) is selected during the time interval t_{HDLDDL} , HDLDOUT will remain HIGH. This means that the head of the newly selected drive will be loaded automatically as shown in Figure 3.

Hard disk drives do not have head loading/unloading mechanism since the heads are basically floating when the drive is running. (When a hard disk drive is not running, the heads are in contact with the disk in a specified area called the landing zone.) Each time a different track is to be accessed, a hard disk drive is said to be in SEEK mode. When the desired track is found, the drive issues an active $\overline{\text{SEEKCOMP}}$. This status is indicated to the controller by the Am9581 as an active $\overline{\text{SEEKCOMP}}$.

WRITE SECTION

FM/MFM Encoding

The serial NRZ data pattern is transformed into pulses that occur in a time window specified as the bit cell time. The bit cell time is derived from a very stable reference frequency which can be labeled as the WTCLK. The encoding process takes place during a write operation – i.e., WG is HIGH and RG is LOW. The result of the encoding process is the transformation of the NRZ data and its reference clock into a single bit stream consisting of a CLOCK and/or a DATA pulse for each bit cell depending upon the NRZ value within the bit cell time.

For FM encoding, a CLOCK pulse is always inserted at the beginning of the bit cell. When NRZ data is "1" during the bit cell time, a DATA pulse is inserted in the middle of the bit cell; otherwise no DATA pulse is inserted. Therefore, for FM encoding a CLOCK pulse and a DATA pulse can both be present within the bit cell time (which is $4\mu\text{s}$ for single density floppies running at 250Kbit/sec).

In MFM encoding, when the NRZ data is "1" during the bit cell time, a data pulse is inserted in the middle of the bit cell. If the NRZ data is "0" during the bit cell time, no data pulse is inserted. However, unlike FM, the clock pulses are not automatically inserted at the beginning of each bit cell. The clock pulses are inserted at the beginning of a bit cell if and only if the NRZ data is "0" during the current bit cell as well as the previous bit cell. Otherwise, no clock pulses are written (see Figure 4). Therefore, in MFM, only a CLOCK pulse or a DATA pulse can be present within the bit cell time (which is $2\mu\text{s}$ for a 500Kbit/sec double density floppy and 200ns for a 5Mbit/sec hard disk drive). FM and MFM encoding are shown in Figure 4.

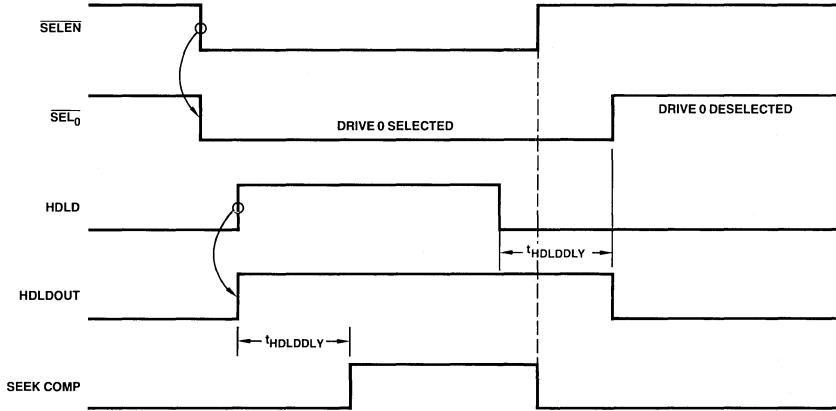
Address Mark Generation

Each sector on the disk contains several Address Marks. These enable the controller to identify sector types, sector numbers, and data fields. So that the Address Marks are unique and always distinguishable from all possible data patterns, the encoding rules (either for FM or MFM) are deliberately violated when an Address Mark is written. This is done by deleting some of the clock bits in the encoded clock/data pattern. When a sector is read back from the disk, these missing clocks are identified, and then the controller is assured that correct synchronization has taken place. The F/HDDS will generate all the standard IBM Address Marks for floppy (IBM format) and Winchester (ST506/SA1000 formats). AMC (ADDRESS MARK CONTROL) is sampled on the rising edge of WTCLK when a WRITE operation is taking place. An Address Mark is then inserted, AMF (ADDRESS MARK FOUND) is brought HIGH in acknowledgement.

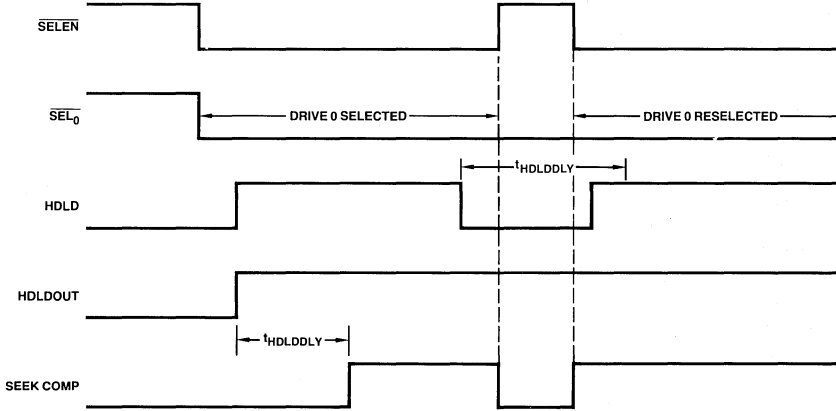
The type of Address Mark generated is dependent on FAM_0 , FAM_1 , and the operating mode, i.e., floppy or hard, and single or double density. The type of Address Mark selected is listed in Table 1.

Figure 3. Floppy Timing Sequence

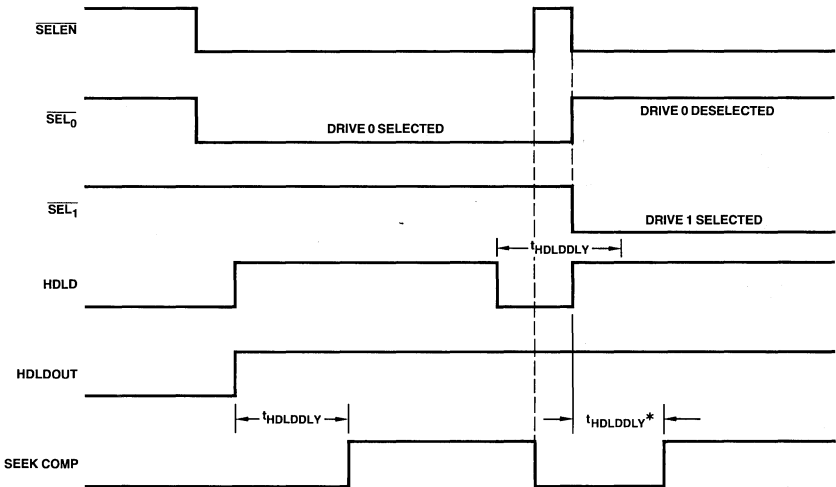
a) Normal Operation



b) Same Drive Reselected



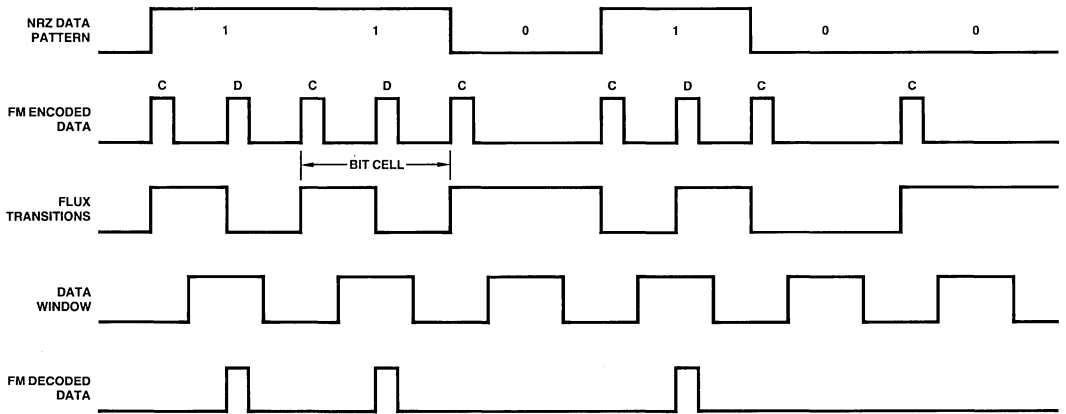
c) Different Drive Selected



*This timeout starts from the falling edge of SELEN or rising edge of HDLD, whichever occurs later.

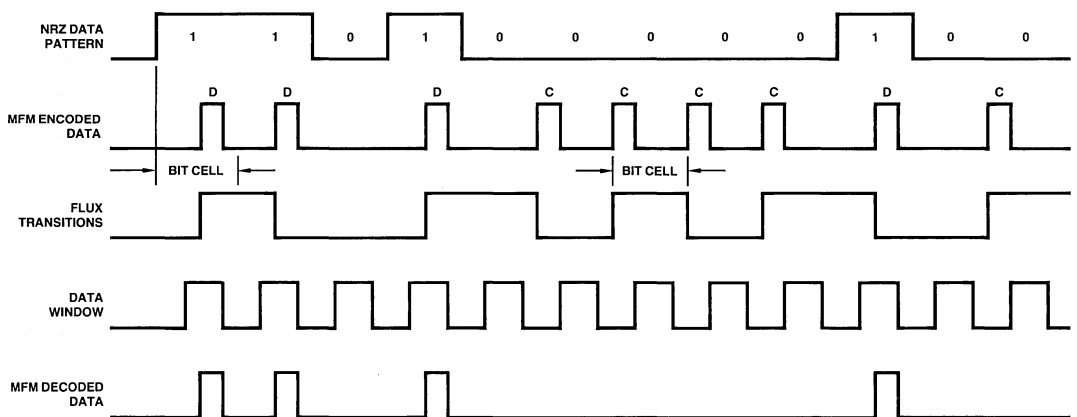
Figure 4. FM vs MFM Encoding – MFM encoding doubles the bit density on the disk by replacing clock bits (C) used in FM encoding with data bits (D). MFM encoding reduces the bit cell by 1/2.

FM ENCODING



05309A-3

MFM ENCODING



05309A-4

The different Address Marks listed below are formed by combinations of the Hexadecimal Data and Clock Patterns.

SINGLE DENSITY FLOPPY

Type	Data Pattern	Clock Pattern	Number of Bytes
IXAM	FC	D7	1
IDAM	FE	C7	1
DAM	FB	C7	1
DDAM	F8	C7	1

DOUBLE DENSITY FLOPPY*

Type	Data Pattern	Clock Pattern	Number of Bytes
IXAM	C2	14	3
DAM and IDAM	A1	0A	3

HARD DISK*

Type	Data Pattern	Clock Pattern	Number of Bytes
DAM and IDAM	A1	0A	1

*Note: The ID Address Marks and Data Address mark for double density floppy and hard disks are normally qualified by an extra byte following the Address Mark. However, these extra bytes are normally encoded (no missing clocks), which the controller can easily detect during a READ operation.

Write Pre-Compensation

Bit shifting is a phenomenon caused by the flux changes stored on the disk interacting with each other. Its effect is to make nearby flux changes move away from each other creating a timing uncertainty which can cause errors when data is read. This phenomenon is much worse on the inside tracks of a disk, because the flux changes are closer together. To overcome this data interaction, the WRITE DATA stream is pre-compensated, i.e., the direction of each bit shift is anticipated and the bit is moved in the other direction by the Am9581 before being written. When PCEN is HIGH, pre-compensation is enabled and each bit will be made either EARLY, NOMINAL, or LATE, depending on its interaction with its neighbors. (In FM mode PCEN has no effect). The amount of time shift between NOMINAL and LATE is set by two external resistors on the PCDLY pins. The pre-compensation is shown in Figure 5.

For RLL codes, NRZ to RLL encoding, write pre-compensation and address mark detection have to be performed by an external circuit.

Read Section

The read section of Am9581 consists of a data Phase-Locked-Loop (PLL), Window Logic, Sync Field Detector, Address Mark Detector, MFM/FM Decoder, Synchronized Multiplexer, crystal controlled oscillator, a reference PLL, and a divide by N counter as shown in Figure 2.

Data Phase-Locked-Loop (PLL)

The main function of the data PLL is to provide a clock signal (shown as 2f in Figure 2) that closely tracks the FM/MFM serial

data read off the disk. The 2f signal is then used by the window logic to generate clock and data windows.

When the chip is in the write mode (WG active), the data PLL is synchronized to the REFCLK derived from the XTAL oscillator and the reference PLL. When the data is read from the disk (RG active), the data PLL is locked to the data stream from the disk.

The Window Logic

The main function of the window logic is to generate clock and data windows using the 2f signal provided by the data PLL. When the Read Gate (RG) is asserted, the window logic assigns clock and data windows arbitrarily.

The Sync Field Detector

The sync field detector looks for the sync field consisting of 8 consecutive pulses in clock windows. When this pattern is detected, the COUNT 8 signal is activated, freezing the window polarity. If the sync pattern is not found, the window logic flips the window polarities so that the sync detector can continue to look for the sync pattern. The apparent sync field ending is seen as a pulse in the data window. This action arms an address mark timeout, i.e., after 8 bit cells (or 24 for double density floppy) an address mark must be found or the state machine is reset back to the lowest level of search — looking for 8 apparent zeros.

Address Mark Detector

The detection of various address marks for floppies and hard disks is performed by this section. The type of address mark to be detected is determined by the signals S/D, F/H, FAM₀ and FAM₁ as shown in Table 1. In response to an active AMC, AMF will be asserted to indicate that the desired address mark has been found during a read or an appropriate address mark has been written during a write. FDDAM is asserted in the FM floppy mode upon detection of a floppy deleted data address mark during a read.

MFM/FM Decoder

The MFM/FM decoder converts the incoming MFM/FM data to NRZ data. If an MFM/FM pulse occurs in a data window, the NRZ data is decoded as a "1." If no pulse occurs in the data window, the NRZ data is decoded as a "0."

SYNC MUX

The SYNC MUX is a synchronized multiplexer that outputs either the REFCLK derived from the XTAL oscillator and the reference PLL or the RDCLK derived from disk data. The multiplexer outputs REFCLK while writing and also while reading until a sync field has been detected. Once the sync is detected, it switches over to RDCLK without any glitches. For RLL hard disks, the output is always REFCLK.

XTAL Oscillator, Reference PLL and Divide by N Counter

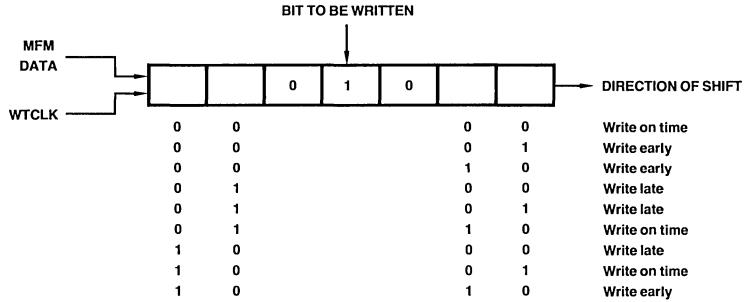
The XTAL oscillator, the reference PLL and the divide by N counter provide REFCLK to the SYNC MUX. This clock is also used in the data PLL to prevent VCO from drifting off from the center of its tuning range while it is not reading data off the disk. The appropriate divide ratio is selected internally as shown in Table 1.

Figure 5.

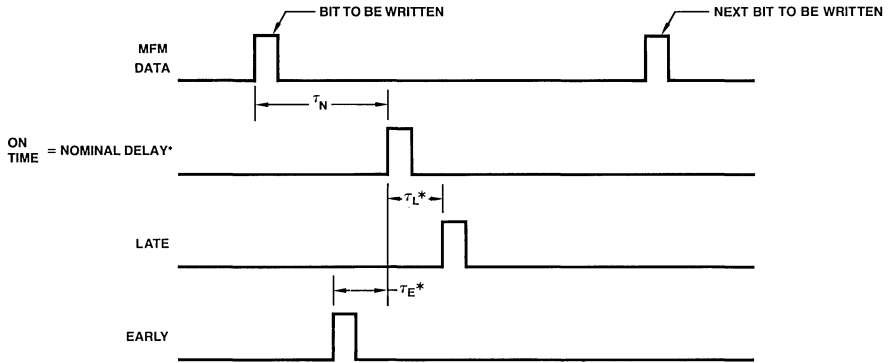
WRITE PRE-COMPENSATION

Pre-compensation is for the MFM case only. FM does not require pre-compensation. The bit to be written is shifted early or

late with respect to a nominal delay. The nominal delay is selected when data is to be written on time. Action to be taken is made by examining a 7-bit register.



05309A-5



05309A-6

* $\tau_L = \tau_E = 1\% - 20\%$ bit cell time
*Nominal delay = τ_N

TABLE 1.

F/H	PCEN/S(D)	FAM ₁	FAM ₀	Address Mark Selected	Mode	XTAL FREQ
1	1	0	0	Index (IXAM)	FM Floppy	
1	1	0	1	ID (IDAM)	FM Floppy	32 x Bit Rate FREQ
1	1	1	0	Data (DAM)	FM Floppy	
1	1	1	1	Deleted Data (DDAM)	FM Floppy	
1	0	0	0	Index (IXAM)	MFM Floppy	16 x Bit Rate FREQ
1	0	1	0	ID or Data	MFM Floppy	
0	X	0	0	Normal A1 Address Mark	MFM Hard Disk	Bit Rate FREQ
0	X	1	1	Any Apparent Address Mark	Dump Clock** - Hard Disk	Bit Rate FREQ
0	X	1	0	None	RLL Hard Disk	Code Rate FREQ*
0	X	0	1	Any Apparent Address Mark	Dump Data - Hard Disk	Bit Rate FREQ
1	0	0	1	Any Apparent Address Mark	Dump Data - Floppy Disk	16 x Bit Rate FREQ
1	0	1	1	Any Apparent Address Mark	Dump Clock - Floppy Disk	16 x Bit Rate FREQ

*Code Rate Frequency = "2F" frequency of PLL.

**Dump is a mode whereby data (or clock) is passed to the HDC on an apparent START of Address Mark (end of apparent SYNC field). This is to enable the recovery of sectors which could not otherwise be read due to corruption of the Address Mark.

DUMP MODE

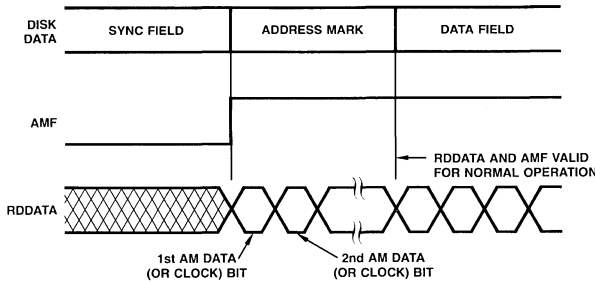


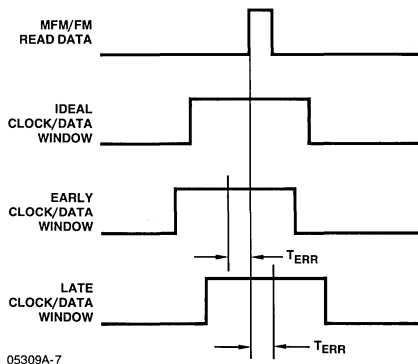
TABLE 2.

DATA PHASE-LOCKED-LOOP SPECIFICATIONS

Supply Voltage	+5V ± 10%
Operating Temperature Range	0 to 70°C (Plastic DIP) -55 to +125°C (Ceramic DIP)
Acquisition Time*	16 x 1/f _D seconds MAX
Capture Range*	± 6% of f _D MIN
Decode Window Error*	± 2.5ns or ± 2% of 1/f _D , MAX whichever larger

*f_D = bit rate frequency

TABLE 3.



05309A-7

DECODE WINDOW ERROR

*Note: f_D = bit rate frequency

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65 to +150°C
Supply Voltage to Ground Potential Continuous	-0.5 to +7.0V
DC Voltage Applied to Outputs for High Output State	-0.5V to +V _{CC}
DC Input Voltage	-0.5 to +7.0V
DC Output Current into Outputs	30mA
DC Input Current	-30 to +5.0mA

Am9581**ELECTRICAL CHARACTERISTICS**

The following conditions apply unless otherwise specified:

COM'L T_A = 0 to +70°C V_{CC} = 5.0V ± 10% (MIN = 4.50V, MAX = 5.50V)

MIL T_C = -55 to +125°C V_{CC} = 5.0V ± 10% (MIN = 4.50V, MAX = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)	Typ		Units	
			Min	Max		
V _{OH}	Output HIGH Voltage	V _{CC} = MIN, V _{IN} = V _{IH} or V _{IL}	I _{OH} = -1mA (Note 6)	2.4		Volts
V _{OL}	Output LOW Voltage	V _{CC} = MIN, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 4mA (Mil), 8mA (Com'l) (Note 6) I _{OL} = 48mA (Note 5)		0.5	Volts
V _{IH}	Input HIGH Level	Guaranteed Input HIGH Voltage for All Inputs		2.0		Volts
V _{IL}	Input LOW Level	Guaranteed Input LOW Voltage for All Inputs			0.8	Volts
V _I	Input Clamp Voltage	V _{CC} = MIN, I _{IN} = -18mA			-1.2	Volts
I _{IL}	Input LOW Current	V _{CC} = MAX, V _{IN} = 0.5V	(Note 7)		-0.4	mA
I _{IH}	Input HIGH Current	V _{CC} = MAX, V _{IN} = 2.4V	(Note 7)		20	μA
I _I	Input HIGH Current	V _{CC} = MAX, V _{IN} = 5.5V			1.0	mA
I _O	Off-State (High-Impedance) Output Current	V _{CC} = MAX	V _O = 0.4V		-50	μA
			V _O = 2.4V		50	
I _{SC}	Output Short Circuit Current (Note 3)	V _{CC} = MAX	(Note 6)	-15	-50	mA
I _{CC}	Power Supply Current (Note 4)	V _{CC} = MAX	0 to +70°C		TBD	mA
			+70°C		TBD	
			-55 to +125°C		TBD	
			+125°C		TBD	

Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

4. All three-state outputs are in the HIGH impedance state.

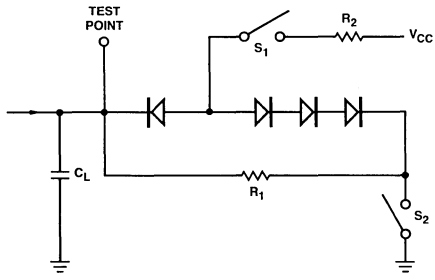
5. SEL₀ - SEL₃ outputs only. These have resistor pullups.

6. All outputs except SEL₀ - SEL₃.

7. All logic inputs. (Does not include X₁, X₂, PCDLY1, PCDLY2, CFIL, HDLDDLY).

AC CHARACTERISTICS

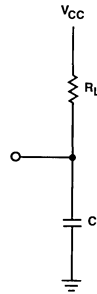
THREE-STATE OUTPUTS



05309A-8

C_L , R_1 , R_2 to be determined.
All diodes IN916 or IN3064.

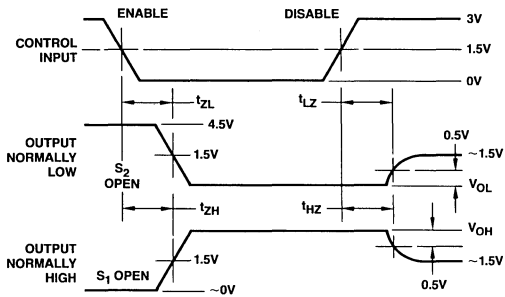
\overline{SEL}_0 - \overline{SEL}_3 OUTPUTS



05309A-9

R_L , C_L to be determined.

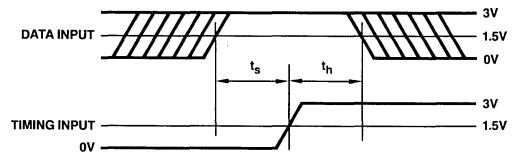
ENABLE AND DISABLE TIMES



05309A-10

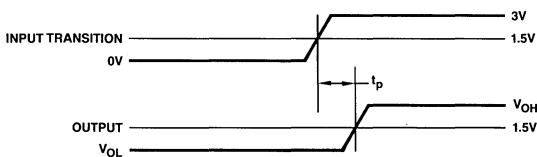
- Notes: 1. Diagram shown for input control Enable-Low and input control Disable-High.
2. S_1 and S_2 of load circuit are closed except where shown.

SETUP AND HOLD TIME MEASUREMENTS



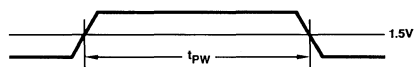
05309A-11

PROPAGATION DELAY MEASUREMENTS



05309A-12

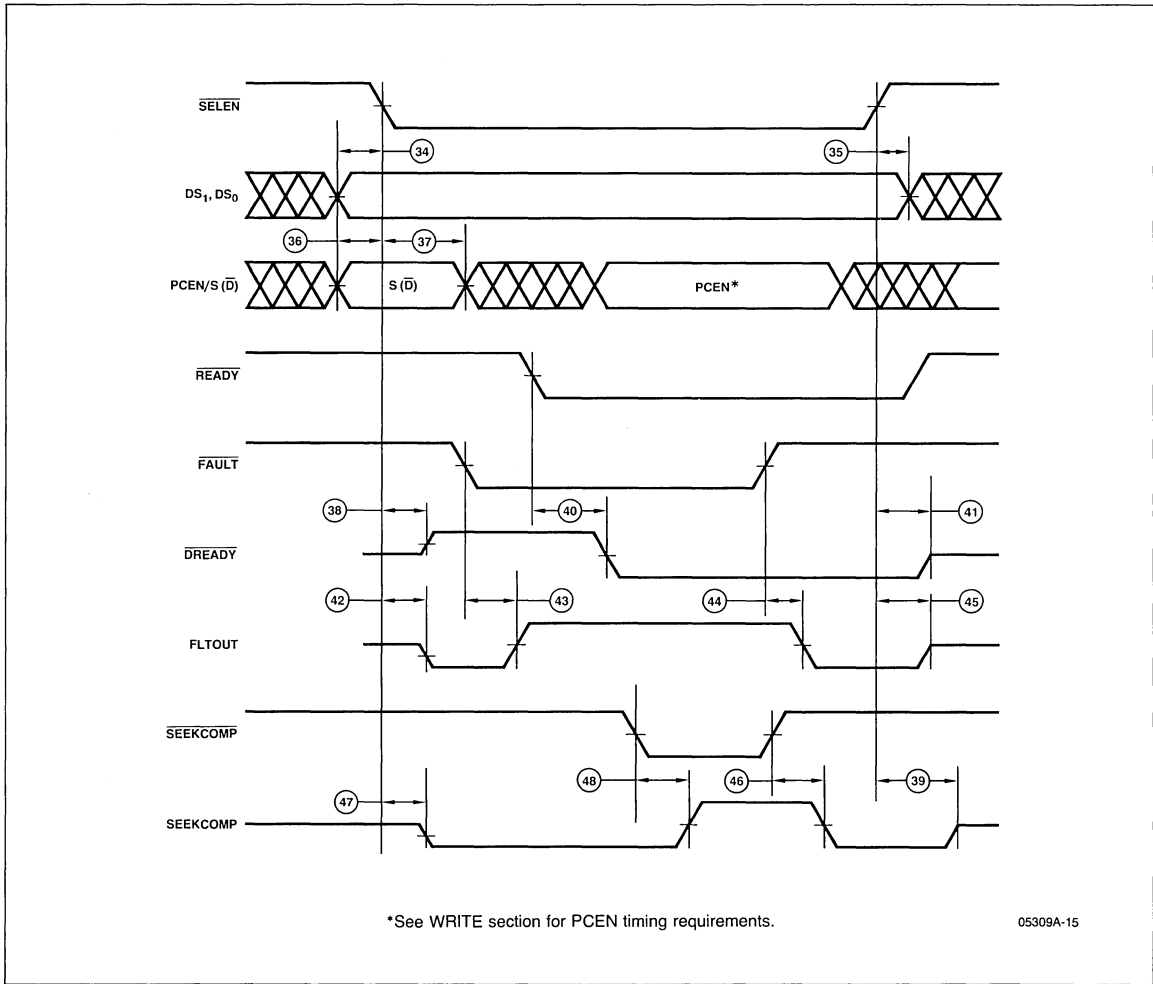
PULSE WIDTH MEASUREMENTS



05309A-13

Am9581 DDS CONTROL SECTION TIMING

No.	Parameter	Description	Min	Typ	Max	Units
34	t_{DSSU}	DS Valid to \overline{SELEN} LOW Setup		20		ns
35	t_{DSH}	\overline{SELEN} HIGH to DS Valid Hold		5		ns
36	$t_{S/DSU}$	S/\overline{D} to \overline{SELEN} LOW Setup		20		ns
37	$t_{S/DH}$	\overline{SELEN} LOW to S/\overline{D} Hold		20		ns
38	t_{SEDR}	\overline{SELEN} LOW to \overline{DREADY} HIGH		50		ns
39	t_{SESCZ}	\overline{SELEN} HIGH to SEEKCOMP High-Z		50		ns
40	t_{DRD}	\overline{READY} LOW to \overline{DREADY} LOW Delay		15		ns
41	t_{SEDRZ}	\overline{SELEN} HIGH to \overline{DREADY} High-Z		50		ns
42	t_{SEFL}	\overline{SELEN} LOW to FLTOUT LOW Delay		50		ns
43	t_{FLFHD}	FAULT LOW to FLTOUT HIGH Delay		10		ns
44	t_{FFD}	FAULT HIGH to FLTOUT LOW Delay		10		ns
45	t_{SEFZ}	\overline{SELEN} HIGH to FLTOUT High-Z		50		ns
46	t_{SCLD}	SEEKCOMP HIGH to SEEKCOMP LOW Delay		10		ns
47	t_{SCD}	\overline{SELEN} LOW to SEEKCOMP LOW		50		ns
48	t_{SCHD}	SEEKCOMP LOW to SEEKCOMP HIGH Delay		10		ns



Am9581 DDS READ/WRITE SECTION TIMING

No.	Name	Description	Min	Typ	Max	Units
READ						
1	t _{RRH}	RD/REFCLK HIGH Time*		0.5T		ns
2	t _{RRL}	RD/REFCLK LOW Time*		0.5T		ns
3	t _{RRC}	RD/REFCLK Cycle Time*		T		ns
4	t _{RGDW}	RG ↓ to RG ↑ DWELL Time*		2T		ns
5	t _{RRAMF}	RD/REFCLK ↑ to AMF ↑ Delay		10		ns
6	t _{AMCAMFL}	AMC ↓ to AMF ↑ Delay		25		ns
7	t _{RRRD}	RD/REFCLK ↑ to Read Data Delay		15		ns
8	t _{FAMSU}	Valid FAM to AMC ↑ Setup		20		ns
9	t _{FAMH}	AMC ↑ to Valid FAM Hold		0		ns
10	t _{FDDAMD}	RD/REFCLK ↑ to Valid FDDAM Delay		15		ns
WRITE						
11	t _{WCH}	WTCLK HIGH Time*		0.5T		ns
12	t _{WCL}	WTCLK LOW Time*		0.5T		ns
13	t _{WCC}	WTCLK Cycle Time*		T		ns
14	t _{RGWGDW}	RG ↓ to WG ↑ DWELL*		2T		ns
15	t _{WGDW}	WG ↓ to WG ↑ DWELL*		2T		ns
16	t _{AMCWC}	AMC ↑ to WTCLK ↑ Setup		20		ns
17	t _{AMCDW}	AMC ↓ to AMC ↑ DWELL*		2T		ns
18	t _{AMFWC}	WTCLK ↑ to AMF Delay		20		ns
19	t _{AMCAMFL}	AMC ↓ to AMF ↓ Delay		25		ns
20	t _{WDSU}	WTDATA to WTCLK ↑ Setup		20		ns
21	t _{WDH}	WTCLK ↑ to WTDATA Hold		0		ns
22	t _{FAMSU}	Valid FAM to AMC ↑ Setup		20		ns
23	t _{FAMH}	AMC ↑ to Valid FAM Hold		0		ns
24	t _{X1D}	X ₁ to RD/REF CLK Delay			TBD	ns
25	t _{WGHWC}	WG ↑ to WTCLK ↑ Setup		20		ns
26	t _{WGLWC}	WG ↓ to WTCLK ↑ Hold		20		ns
27	t _{PCWCSU}	PCEN to WTCLK ↑ Setup		-1T		ns
28**	t _{PCWCH}	PCEN to WTCLK ↑ Hold		6T		ns

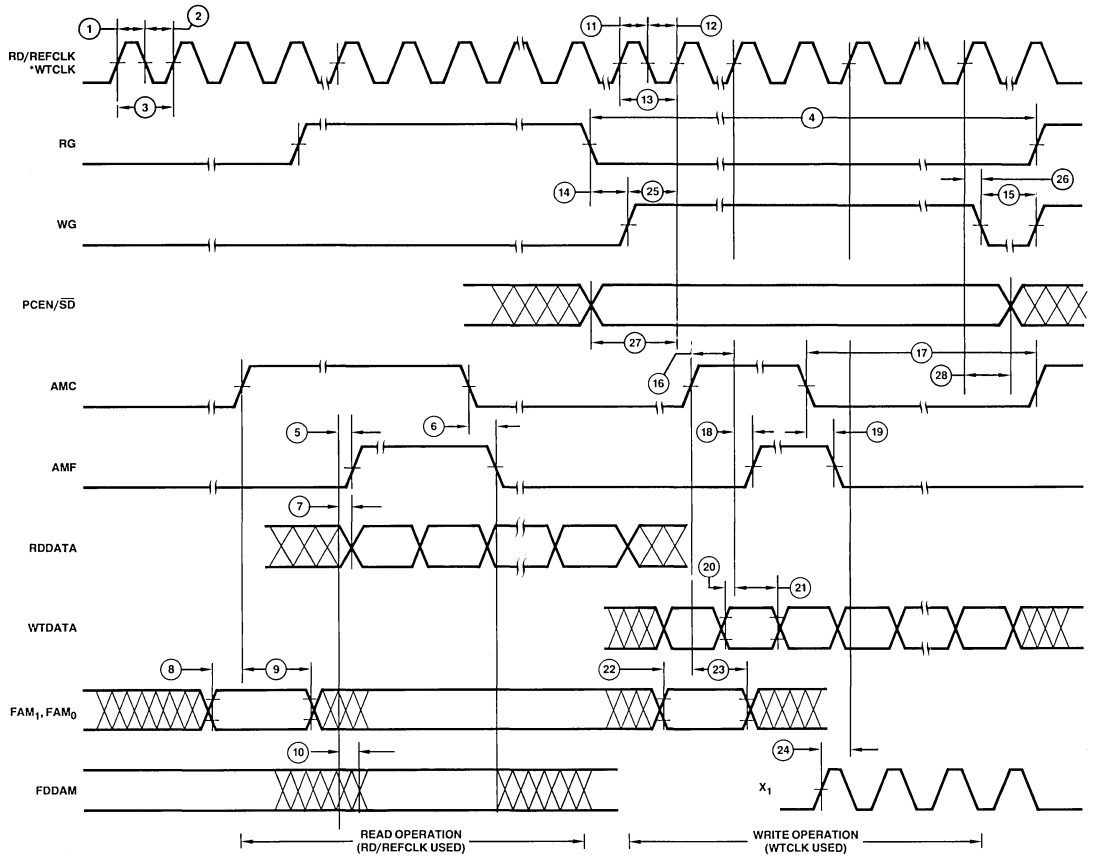
*T = 1/Nominal Data Rate

**If the data pattern remaining in the write pipeline after WG goes LOW does not need precompensation, PCEN can go LOW at the same time as WG.

Am9581 DDS SELECT TIMING

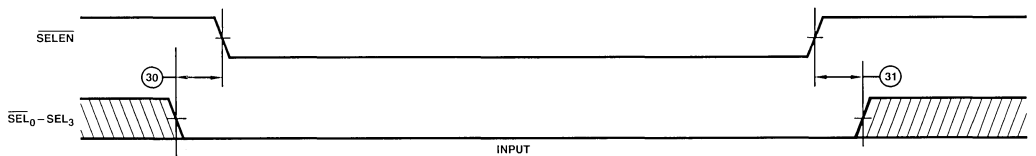
No.	Name	Description	Min	Typ	Max	Units
30	t _{SELSU}	SEL̄ to SELEN ↓ Setup		0		ns
31	t _{SEHH}	SEL̄ ↑ to SELEN ↑ Hold		0		ns
32	t _{SELD}	SELEN ↓ to SEL̄ ↓ Delay		50		ns
33	t _{SEHD}	SELEN ↑ to SEL̄ ↑ Delay		50		ns

Am9581 DDS READ/WRITE SECTION TIMING



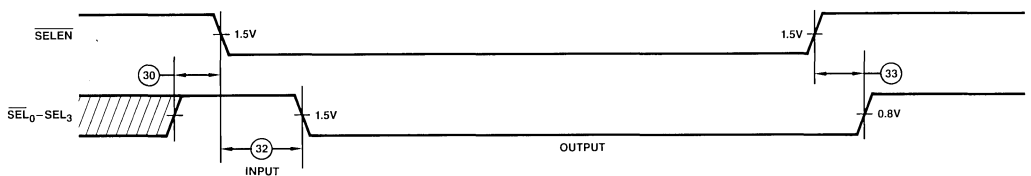
*Note: During write operation, WTCLK is used which could be asynchronous relative to the RD/REFCLK.

DDS NOT SELECTED



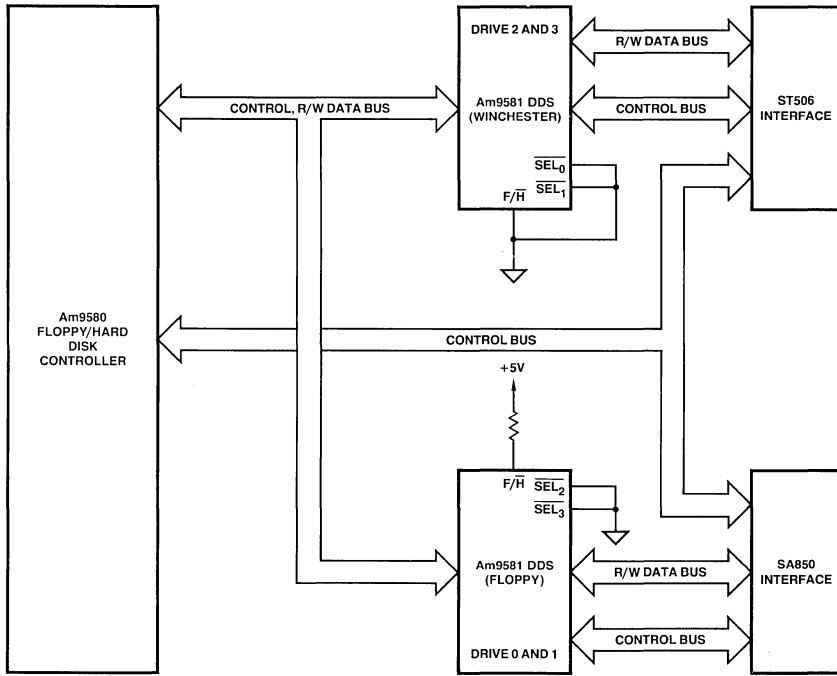
Here a $\overline{\text{SEL}}$ line is used as an input and is held LOW. Whenever the HDC addresses the drive corresponding to this $\overline{\text{SEL}}$ pin, the DDS will tri-state all its output lines on the HDC interface.

DDS SELECTED



Here the DDS causes the $\overline{\text{SEL}}$ output corresponding to the drive selected to go LOW.

TYPICAL FLOPPY/WINCHESTER DISK DRIVE SYSTEM



05309A-16



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