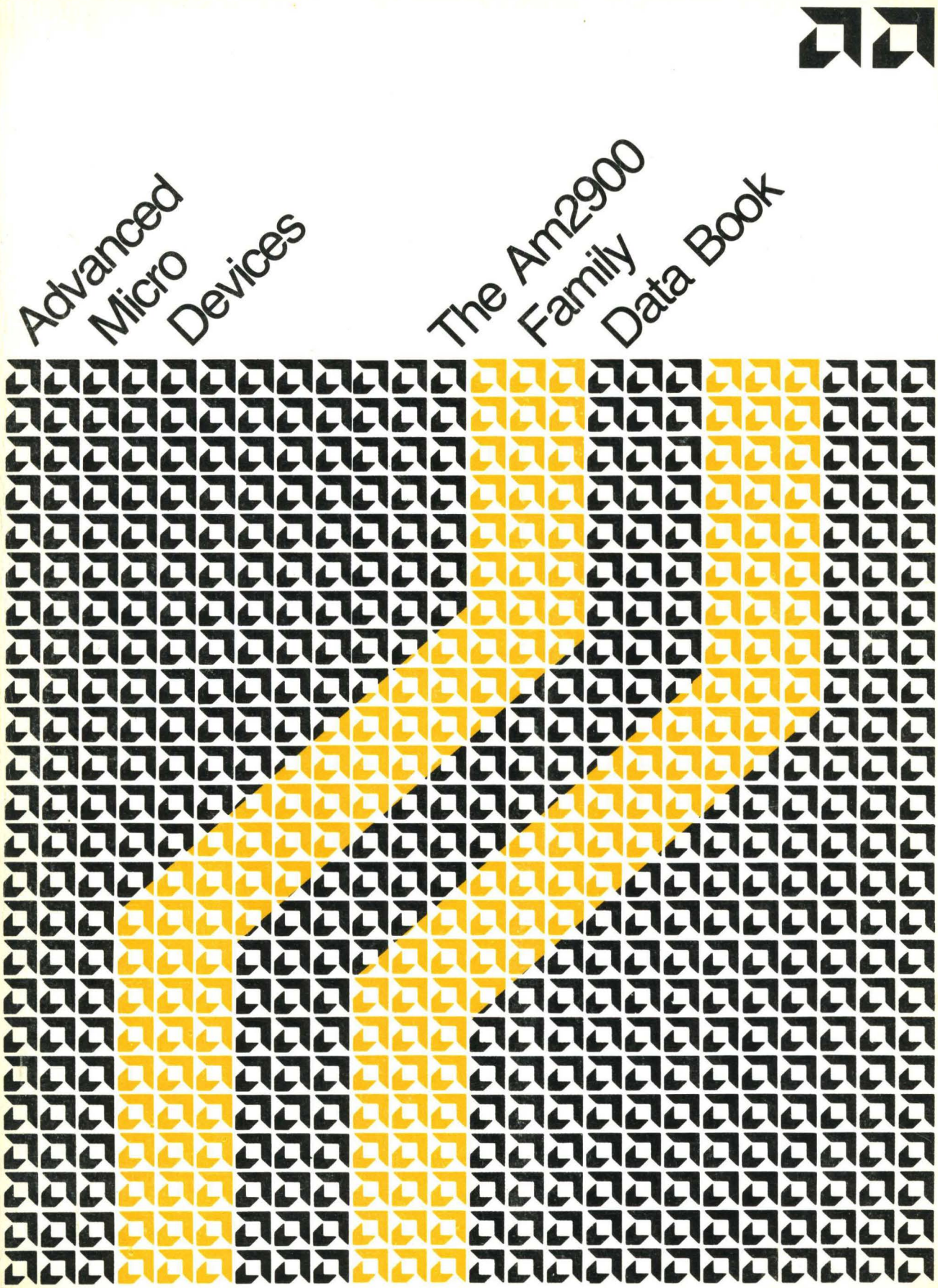
Advanced
Micro
Devices
The Am2900
Family
Data Book

Advanced Micro Devices

The Am2900 Family Data Book With Related Support Circuits

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INTRODUCTION

THREE GENERATIONS OF TTL

Transistor-transistor logic has been the dominant technology for digital circuits since it was developed in the mid-1960's. It has proven itself to be manufacturable in high volume using an extremely reliable process technology. The processes used for TTL have evolved over the years, making components smaller, faster and less expensive. Relative to a TTL gate manufactured in 1966, a gate on a circuit manufactured today occupies 1/5 the area, consumes 1/10 the power, is twice as fast and costs less than 1/100 the price.

The circuits built using TTL technology have gone through two generations; the Am2900 Family represents the beginning of the third. Each generation consists of circuits which are fundamental building blocks of systems – circuits which can be interconnected in many different ways to build many different systems. Only by producing such universal circuits can manufacturing volumes be high enough to generate the rapid cost reductions characteristic of the integrated circuit industry.

The quality which distinguishes one generation from another is the level of integration used, and, because of the level of integration, the philosophy behind the circuit.

If one draws a curve plotting the cost of an individual gate against the number of gates on a chip, Figure 1 results.

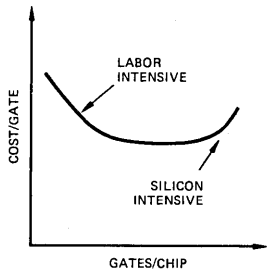


Figure 1. MPR-001

At the left, cost per gate is inversely proportional to the number of gates on the chip. The chip is small enough that it does not represent a significant portion of the cost of the product – it is virtually free. The cost of the product is composed of labor in assembly and test, the cost of processing an order, shipping and fixed overhead. Doubling the number of gates on the chip doesn't materially affect the cost so the cost per gate halves. As the number of gates per chip increases, the die begins to cost more, reversing the downward trend. As die cost dominates, the cost per gate remains relatively flat until the yield of the die begins to decline markedly. The cost per gate then begins to rise again. The lowest cost per gate is achieved at a level of integration corresponding to the flat region. This is the optimum level of integration.

As technology improves, costs are constantly reduced and the optimum level of integration occurs at more and more gates per chip.

The three curves of Figure 2 are the reason for the three generations of TTL. Each generation has consisted of fundamental system building blocks designed to take advantage of the optimum level of integration at the time.

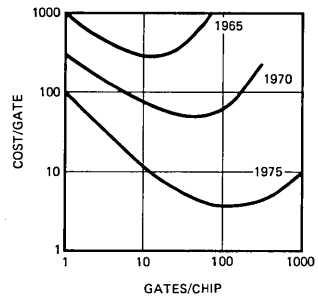


Figure 2. MPR-002

GENERATION I – SSI, 1965

In 1965, the optimum level of integration was three-to-six gates per chip. Users were delighted to buy such chips at $10-20 each. The circuits were useful in many systems. They consisted of gates – the 7400, 7410, 7420 – and, pressing the state of the art, some flip-flops. They were fundamental building blocks.

GENERATION II – MSI, 1970

Beginning around 1968, it became economical to put more gates on a chip and the industry was faced with a problem: How does one put 20 gates on a chip and build a universal building block? Clearly, one answer was to bring the inputs and outputs off chip as had been done before. But that was the wrong answer. The right answer was to redefine fundamental building blocks. The new building blocks fell into seven categories:

- Counters
- Decoders
- Multiplexers
- Operators (adders, comparators)
- Encoders
- Registers
- Latches

All systems could be defined in terms of these seven functions, and integrated circuits could be defined at the 20–50 gate/chip level which performed these functions efficiently. This, of course, is MSI. Over the last six or seven years, more and more circuits of this type have been introduced, utilizing standard gold-doped technology, low-power TTL, high-speed TTL, Schottky TTL, and now low-power Schottky TTL technology. Today, there are over 250 different MSI circuits and new ones appear every month. But in today's technology, many of these circuits are not particularly cost effective. They are too small for today's technology and their costs are labor intensive. (Labor costs do not follow traditional semiconductor pricing patterns.) In 1977, the optimum level of integration for bipolar logic is around 500 gates/chip.

GENERATION III – The Am2900 Family, 1976

At a 500-gate-per-chip level of integration, one does not build counters, decoders, and multiplexers. A new definition of fundamental system functions is needed. Advanced Micro Devices has defined these eight categories:

- Data Manipulation
- Microprogram Control
- Macroprogram Control
- Priority Interrupt
- Direct Memory Access
- I/O Control
- Memory Control
- Front Panel Control

The Am2900 Family consists of circuits designed to perform those functions efficiently. They are fundamental system building blocks; they contain hundreds of gates per chip; they are fast – utilizing Low-Power Schottky TTL technology; they are expandable; they are flexible – useful in emulation; and they are driven under microprogram control.

THE Am2900 FAMILY

The Am2900 Family consists of a series of LSI building blocks designed for use in microprogrammed computers and controllers. Each device is designed to be expandable and sufficiently flexible to be suitable for emulation of many existing machines. It is the wide variety of machine architectures possible with the Am2900 Family which sets it apart from the fixed-instruction microprocessors such as the Am9080A.

While an Am9080A can be used to build a microcomputer with only four or five packages, an Am2900 design will require 30 or 40 or more. The Am9080A design will, therefore, almost always be cheaper. But the Am9080A, or any other fixed-instruction processor, can execute only one instruction set, so it is not really suitable for emulation of another machine.

Moreover, a fixed-instruction processor operates only on words of a single length, usually eight bits. An Am2900 design, on the other hand, can be constructed for any word length which is a multiple of four bits.

Many applications require specialized operations to be performed at relatively high speed. Such functions as multiply and divide and special graphic control operations, can be done in microcode 10-100 times faster than in fixed-instruction MOS processors.

MICROPROGRAMMED ARCHITECTURE

Most small processors today are being designed using a technique called microprogramming. In microprogrammed systems, a large portion of the system's control is performed by a read only memory (usually PROM) rather than large arrays of gates and flip-flops. This technique frequently reduces the package count in the controller and provides a highly ordered structure in the controller, not present when random logic is used. Moreover, microprogramming makes changes in the machines' instruction set very simple to perform – reducing the post-production engineering costs for the system substantially.

The Am2900 Family of Bipolar LSI devices has been designed for use in microprogrammed systems. Each device performs a basic system function and is driven by a set of control lines from a microinstruction.

Figure 3 illustrates a typical system architecture. There are two "sides" to the system. At the left is the control circuitry and on the right is the data manipulation circuitry. The block labeled "2901 array" consists of the ALU, scratchpad registers, data steering logic (all internal to the Am2901's), plus left/right shift control and carry lookahead circuit. Data is processed by moving it from main memory (not shown) into the 2901 registers, performing the required operations on it and returning the result to main memory. Memory addresses may also be generated in the 2901's and sent out to the memory address register (MAR). The four status bits from the 2901's ALU are captured in the status register after each operation.

The logic on the left side is the control section of the computer. This is where the Am2909, 2910, or 2911 is used. The entire system is controlled by a memory, usually PROM, which contains long words called microinstructions. Each microinstruction contains bits to control each of the data manipulation elements in the system. There are, for example, nine bits for the 2901 instruction lines, eight bits for the A and B register addresses, two or three bits to control the shifting multiplexers at the ends of the 2901 array (Figure 19 or 2901 data sheet), and bits to control the register enables on the MAR, instruction register, and various bus transceivers. When the bits in a microinstruction are applied to all the data elements and everything is clocked, then one small operation (such as a data transfer or a register-to-register add) will occur.

A "machine instruction" (such as a minicomputer instruction or a 9080A instruction) is performed by executing several microinstructions in sequence. Each microinstruction therefore contains not only bits to control the data hardware, but also bits to define the location in PROM of the next microinstruction to be executed. The fields are labeled in Figure 3 as I, CC, and BA. The I field controls the sequencer. It indicates where the next address is located – the μPC, the stack, or the direct inputs – and whether the stack is to be pushed or popped.

The CC field contains bits indicating the conditions under which the I field applies. These are compared with the condition codes in the status register and may cause modification to the I field. The comparing and modification occurs in the block labeled "control logic". Frequently this is a PROM or PLA. In the case of the Am2910, it is built into the chip. The BA field is a branch address or the address of a subroutine.

PIPELINING

The address for the microinstructions is generated by the sequencer, starting from a clock edge. The address goes from the sequencer to the ROM and, an access time later, the microinstruction is at the ROM outputs.

A pipeline register is a register placed on the output of the microprogram memory to essentially split the system in two. The pipeline register contains the microinstruction currently being executed ①. (Refer to the circled numbers in Figure 3.) The data manipulation control bits go out to the system elements and a portion of the microinstruction is returned to the sequencer ② to determine the address of the next microinstruction to be executed. That address ③ is sent to the ROM and the next microinstruction ④ sits at the input of the pipeline register. So while the 2901's are executing one instruction, the next instruction is being fetched from ROM. Note that there is no sequential logic in the sequencer between the select lines and the output. This is important because the loop ① to ② to ③ to ④ must occur during a single clock cycle. During the same time, the loop from ① to ⑤ must occur in the 2901's. These two paths are roughly the same (around 200ns worst case for a 16-bit system). The presence of the pipeline register allows the microinstruction fetch to occur in parallel with the data operation rather than serially, allowing the clock frequency to be doubled.

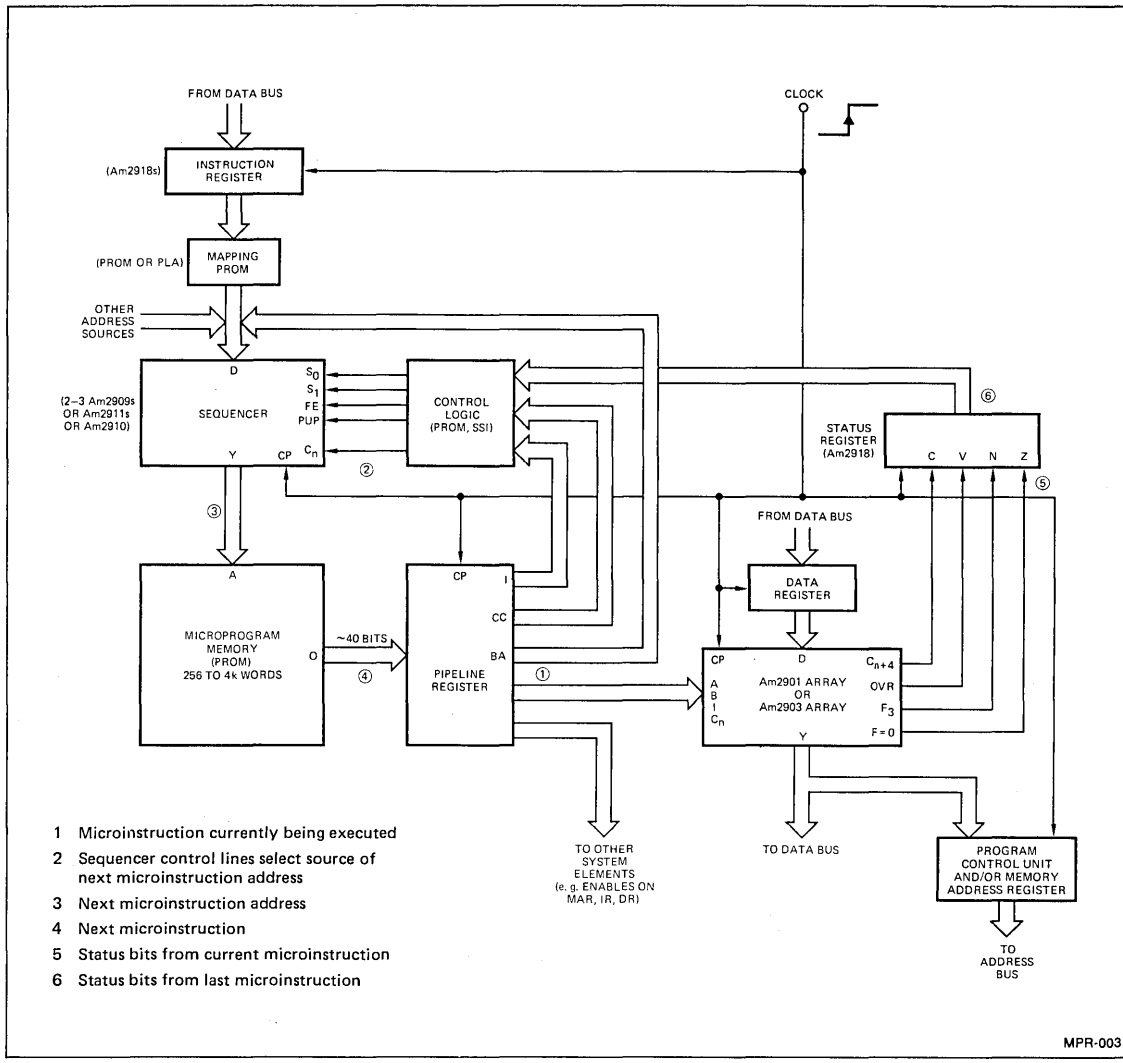
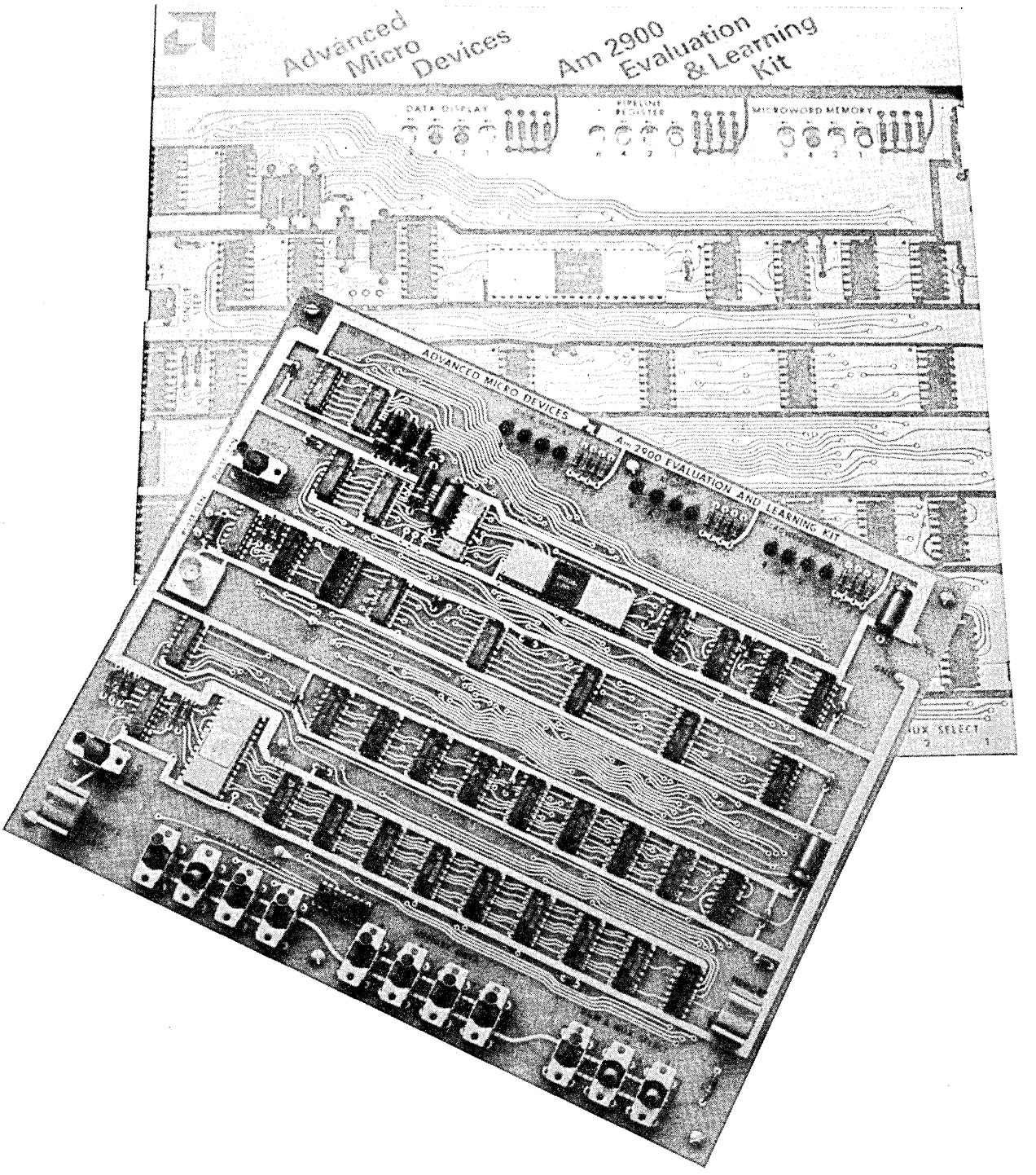


Figure 3.

The system shown in Figure 3 works as follows. A sequence of microinstructions in the PROM is executed to fetch an instruction from main memory. This requires that the program counter, often in a 2901 working register, be sent to the memory address register and incremented. The data returned from memory is loaded into the instruction register. The contents of the instruction register is passed through a PROM or PLA to generate the address of the first microinstruction which must be executed to perform the required function. A branch to this address occurs through the sequencer. Several microinstructions may be executed to fetch data from memory, perform ALU operations, test for overflow, and so forth. Then a branch will be made back to the instruction fetch cycle. At this point, there may be branches to other sections of microcode. For example, the machine might test for an interrupt here and obtain an interrupt service routine address from another mapping ROM rather than start on the next machine instruction. There are obviously many possibilities. Throughout this data book, in application notes, and within data sheets, some suggested techniques will be found.

Additional application notes are in preparation and are planned for publication. Advanced Micro Devices' Applications' staff is available to answer questions and provide technical assistance as well. They may be reached by calling (408) 732-2400, or, outside California (800) 538-8450. Ask for Am2900 Family Applications.


Advanced
Micro
Devices
Am 2900
Evaluation
& Learning
Kit
DATA DISPLAY
PIPELINE REGISTER
MICROWORD MEMORY
ADVANCED MICRO DEVICES
Am 2900 EVALUATION AND LEARNING KIT

THE Am2900 EVALUATION AND LEARNING KIT

Pictured at the left is the Am2900 Evaluation Kit. The system consists of a microprogrammed control unit which controls all the inputs to an Am2901A microprocessor slice. Thirty-two bit microinstructions are entered into a RAM in the control unit using the switch register. Each microinstruction contains bits to control the Am2901A's A and B addresses, instruction, carry in, and data input. Additional bits in the microinstruction control an Am2909 sequencer which generates the addresses for the microprogram memory. Once entered, microinstructions may be executed using a single step clock or using a pulse generator. The LED display provides access to nearly every signal path in the system.

Sixteen "sequence control" instructions are available, including execute, branch conditional, jump-to-subroutine, return, and loop. Because the set of sequence instructions is implemented in a PROM, the user can devise his own set of operations by programming a new PROM.

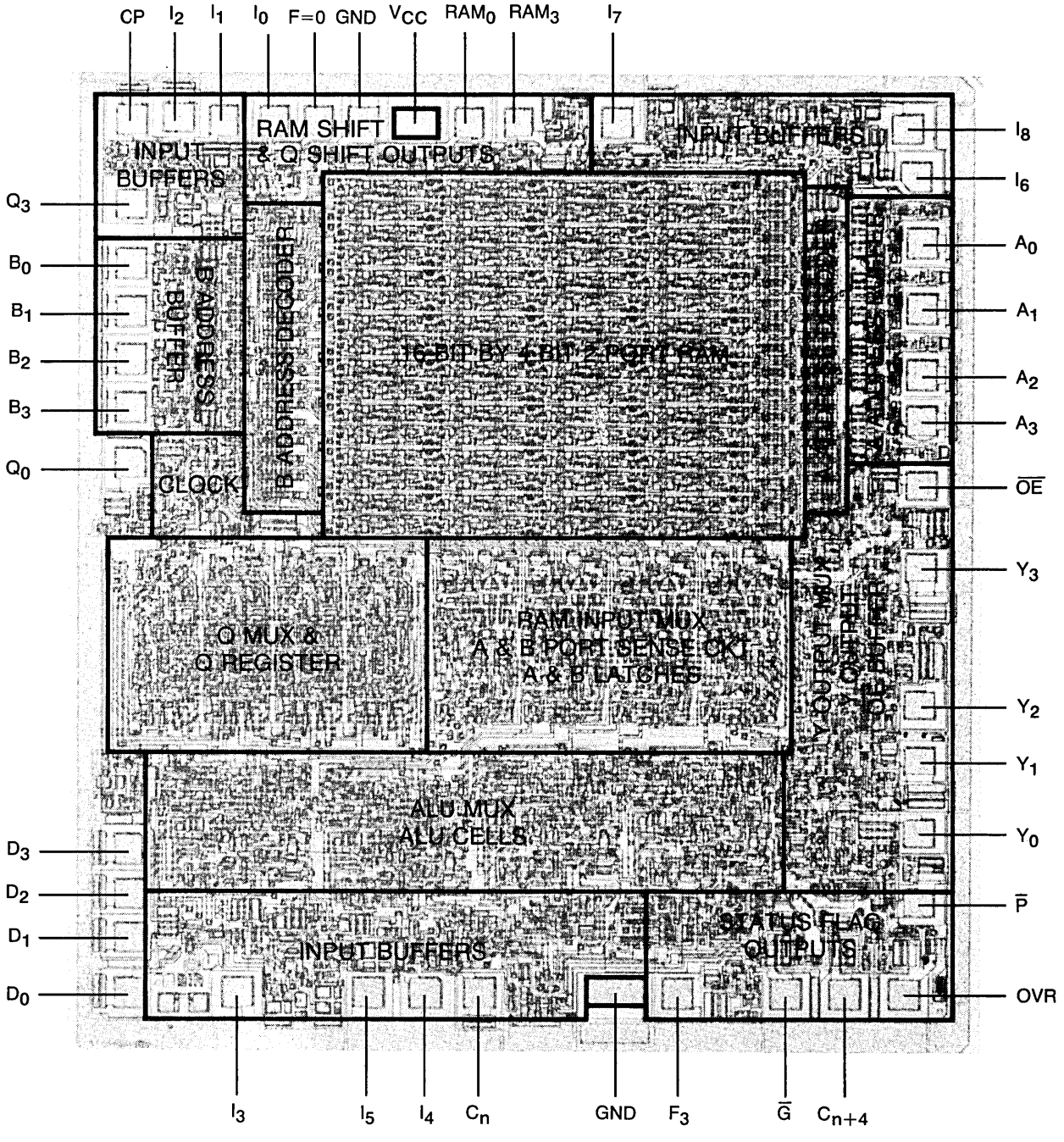
The kit is supplied with 40 IC's, all resistors, capacitors, LED's and switches, the PC board, and a manual containing assembly instructions, theory and a set of exercises. The user need only solder the components in place and attach a 5 V power supply (2.0 ampere rating).

Working with the kit, the user will gain familiarity with a high performance pipelined microprogrammed architecture, and with the operation of the Am2909 and Am2901A. By driving the kit from a pulse generator, the user can observe the operation of the components in real time, executing real instructions.

The part number for this kit is Am2900K1.

Am2901A

Photomicrograph



Am2901A

Four-Bit Bipolar Microprocessor Slice

DISTINCTIVE CHARACTERISTICS

- Two-address architecture –
  Independent simultaneous access to two working registers saves machine cycles.
- Eight-function ALU –
  Performs addition, two subtraction operations, and five logic functions on two source operands.
- Flexible data source selection –
  ALU data is selected from five source ports for a total of 203 source operand pairs for every ALU function.
- Left/right shift independent of ALU –
  Add and shift operations take only one cycle.
- Four status flags –
  Carry, overflow, zero, and negative.
- Expandable –
  Connect any number of Am2901A's together for longer word lengths.
- Microprogrammable –
  Three groups of three bits each for source operand, ALU function, and destination control.

GENERAL DESCRIPTION

The four-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPU's, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the Am2901A will allow efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram below, consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip.

The Am2901A is a pin-for-pin replacement for the Am2901 with increased speed, better output drive and reduced power supply current.

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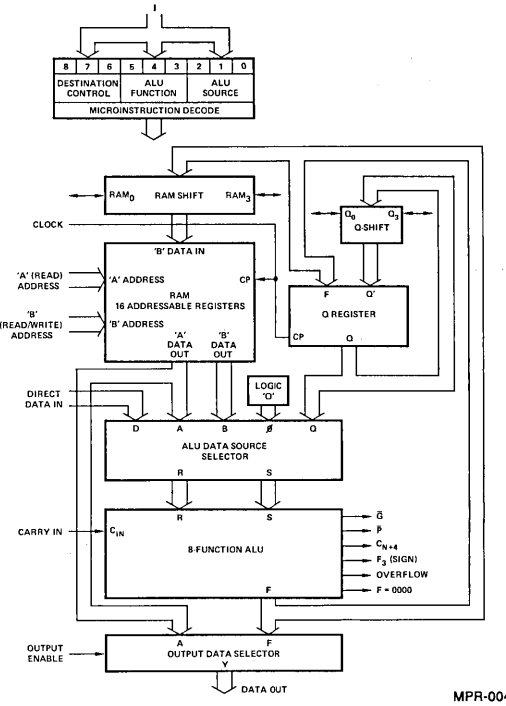
MICROPROCESSOR SLICE BLOCK DIAGRAM



MPR-004

ARCHITECTURE

A detailed block diagram of the bipolar microprogrammable microprocessor structure is shown in Figure 1. The circuit is a four-bit slice cascadable to any number of bits. Therefore, all data paths within the circuit are four bits wide. The two key elements in the Figure 1 block diagram are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Data in any of the 16 words of the Random Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A address field input. Likewise, data in any of the 16 words of the RAM as defined by the B address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A select field and B select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up one bit position, shifted down one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is LOW. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to Figure 1, the ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent that AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely non-redundant source operand pairs for the ALU. The Am2901A microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0, I_1, and I_2 inputs. The definition of I_0, I_1, and I_2 for the eight source operand combinations are as shown in Figure 2. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the four-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high-speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The I_3, I_4, and I_5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Figure 3. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, are outputs of the device for use with a carry-look-ahead-generator such as the Am2902 ('182). A carry-out, C_{n+4}, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out (C_{n+4}) are active HIGH.

The ALU has three other status-oriented outputs. These are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y_3. The F = 0 output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. F = 0 is HIGH when all F outputs are LOW. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is HIGH when overflow exists. That is, when C_{n+3} and C_{n+4} are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6, I_7, and I_8 microinstruction inputs. These combinations are shown in Figure 4.

The four-bit data output field (Y) features three-state outputs and can be directly bus organized. An output control ($\overline{OE}$) is used to enable the three-state outputs. When $\overline{OE}$ is HIGH, the Y outputs are in the high-impedance state.

A two-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6, I_7, and I_8 microinstruction inputs. Refer to Figure 4 for the selected output for each microinstruction code combination.

As was discussed previously, the RAM inputs are driven from a three-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up one position (X2) or shifted down one position (÷2). The shifter has two ports; one is labeled RAM_0 and the other is labeled RAM_3. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer. Thus, in the shift up mode, the RAM_3 buffer is enabled and the RAM_0 multiplexer input is enabled. Likewise, in the shift down mode, the RAM_0 buffer and RAM_3 input are enabled. In the no-shift mode, both buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the I_6, I_7 and I_8 microinstruction inputs as defined in Figure 4.

Similarly, the Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has two ports; one is labeled Q_0 and the other is Q_3. The operation of these two ports is similar to the RAM shifter and is also controlled from I_6, I_7, and I_8 as shown in Figure 4.

The clock input to the Am2901A controls the RAM, the Q register, and the A and B data latches. When enabled, data is clocked into the Q register on the LOW-to-HIGH transition of the clock. When the clock input is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is LOW, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B address field when the clock input is LOW.

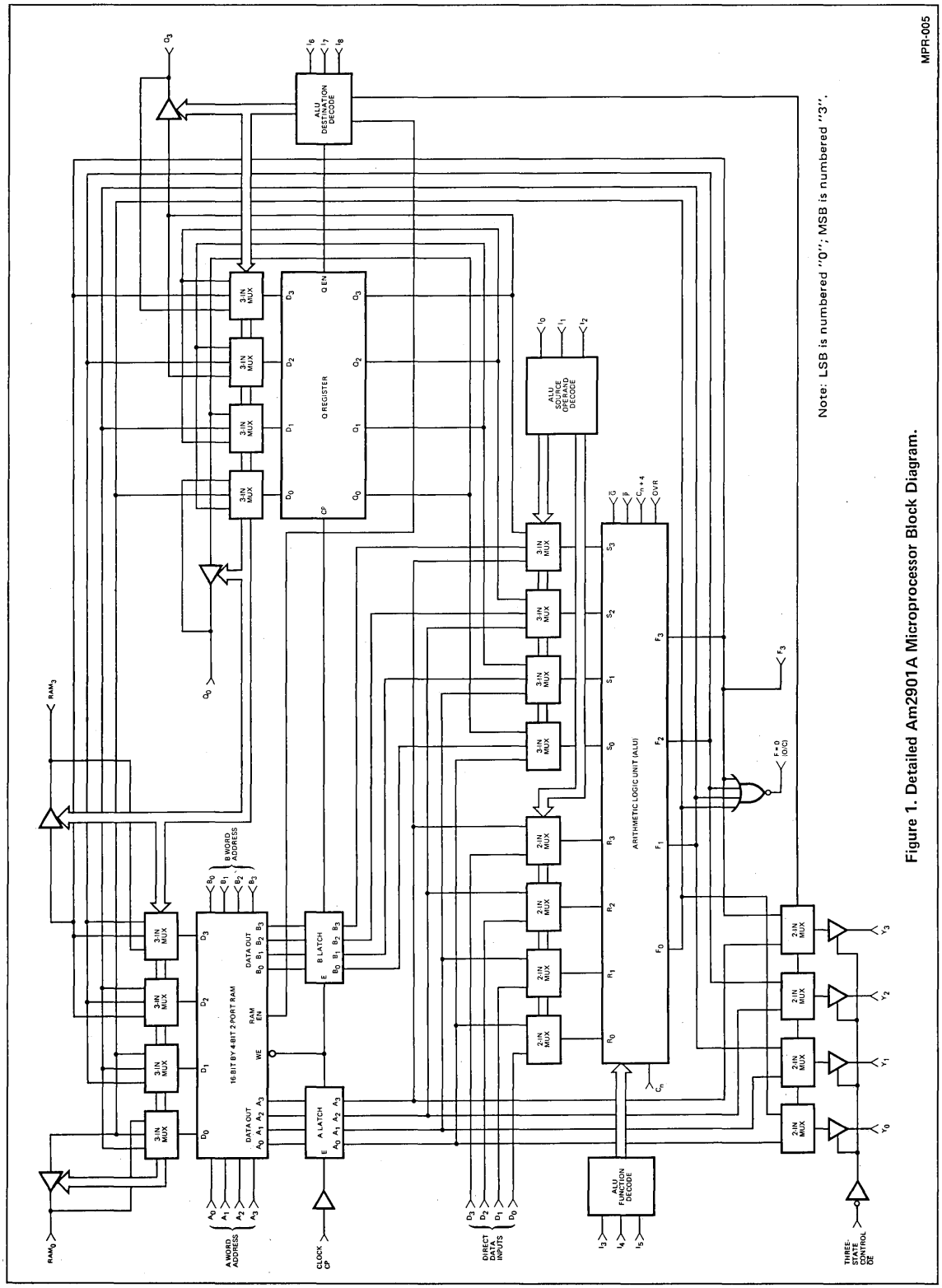


Figure 1. Detailed Am2901A Microprocessor Block Diagram.

Mnemonic	MICRO CODE I_2	I_1	I_0	Octal Code	ALU SOURCE OPERANDS R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

Figure 2. ALU Source Operand Control.

Mnemonic	MICRO CODE I_5	I_4	I_3	Octal Code	ALU Function	SYMBOL
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
EXOR	H	H	L	6	R EX-OR S	R ∀ S
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \forall S}$

Figure 3. ALU Function Control.

Mnemonic	MICRO CODE I_8	I_7	I_6	Octal Code	RAM FUNCTION Shift	Load	Q-REG. FUNCTION Shift	Load	Y OUTPUT	RAM SHIFTER RAM_0	RAM_3	Q SHIFTER Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F → B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F → B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2 → B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F → B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state
B = Register Addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

Figure 4. ALU Destination Control.

OCTAL I_{210}	I_5 I_4 I_3 ALU Function \ ALU Source	0 A, Q	1 A, B	2 0, Q	3 0, B	4 0, A	5 D, A	6 D, Q	7 D, 0
0	C_n = L R Plus S	A+Q	A+B	Q	B	A	D+A	D+Q	D
	C_n = H	A+Q+1	A+B+1	Q+1	B+1	A+1	D+A+1	D+Q+1	D+1
1	C_n = L S Minus R	Q−A−1	B−A−1	Q−1	B−1	A−1	A−D−1	Q−D−1	−D−1
	C_n = H	Q−A	B−A	Q	B	A	A−D	Q−D	−D
2	C_n = L R Minus S	A−Q−1	A−B−1	−Q−1	−B−1	−A−1	D−A−1	D−Q−1	D−1
	C_n = H	A−Q	A−B	−Q	−B	−A	D−A	D−Q	D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ∀ Q	A ∀ B	Q	B	A	D ∀ A	D ∀ Q	D
7	R EX-NOR S	$\overline{A \forall Q}$	$\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; ∀ = EX-OR

Figure 5. Source Operand and ALU Function Matrix.

SOURCE OPERANDS AND ALU FUNCTIONS

There are eight source operand pairs available to the ALU as selected by the I_0, I_1, and I_2 instruction inputs. The ALU can perform eight functions; five logic and three arithmetic. The I_3, I_4, and I_5 instruction inputs control this function selection. The carry input, C_n, also affects the ALU results when in the arithmetic mode. The C_n input has no effect in the logic mode. When I_0 through I_5 and C_n are viewed together, the matrix of Figure 5 results. This matrix fully defines the ALU/source operand function for each state.

The ALU functions can also be examined on a "task" basis, i.e., add, subtract, AND, OR, etc. In the arithmetic mode, the carry will affect the function performed while in the logic mode, the carry will have no bearing on the ALU output. Figure 6 defines the various logic operations that the Am2901A can perform and Figure 7 shows the arithmetic functions of the device. Both carry-in LOW (C_n = 0) and carry-in HIGH (C_n = 1) are defined in these operations.

Octal I_{543}, I_{210}	Group	Function
4 0	AND	A∧Q
4 1		A∧B
4 5		D∧A
4 6		D∧Q
3 0	OR	A∨Q
3 1		A∨B
3 5		D∨A
3 6		D∨Q
6 0	EX-OR	A∀Q
6 1		A∀B
6 5		D∀A
6 6		D∀Q
7 0	EX-NOR	$\overline{A \forall Q}$
7 1		$\overline{A \forall B}$
7 5		$\overline{D \forall A}$
7 6		$\overline{D \forall Q}$
7 2	INVERT	$\overline{Q}$
7 3		$\overline{B}$
7 4		$\overline{A}$
7 7		$\overline{D}$
6 2	PASS	Q
6 3		B
6 4		A
6 7		D
3 2	PASS	Q
3 3		B
3 4		A
3 7		D
4 2	"ZERO"	0
4 3		0
4 4		0
4 7		0
5 0	MASK	$\overline{A}$∧Q
5 1		$\overline{A}$∧B
5 5		$\overline{D}$∧A
5 6		$\overline{D}$∧Q

Figure 6. ALU Logic Mode Functions.

Octal	C_n = 0 (Low)		C_n = 1 (High)	
I_{543}, I_{210}	Group	Function	Group	Function
0 0	ADD	A+Q	ADD plus one	A+Q+1
0 1		A+B		A+B+1
0 5		D+A		D+A+1
0 6		D+Q		D+Q+1
0 2	PASS	Q	Increment	Q+1
0 3		B		B+1
0 4		A		A+1
0 7		D		D+1
1 2	Decrement	Q–1	PASS	Q
1 3		B–1		B
1 4		A–1		A
2 7		D–1		D
2 2	1's Comp.	–Q–1	2's Comp. (Negate)	–Q
2 3		–B–1		–B
2 4		–A–1		–A
1 7		–D–1		–D
1 0	Subtract (1's Comp)	Q–A–1	Subtract (2's Comp)	Q–A
1 1		B–A–1		B–A
1 5		A–D–1		A–D
1 6		Q–D–1		Q–D
2 0		A–Q–1		A–Q
2 1		A–B–1		A–B
2 5		D–A–1		D–A
2 6		D–Q–1		D–Q

Figure 7. ALU Arithmetic Mode Functions.

LOGIC FUNCTIONS FOR G, P, C_{n+4}, AND OVR

The four signals G, P, C_{n+4}, and OVR are designed to indicate carry and overflow conditions when the Am2901A is in the add or subtract mode. The table below indicates the logic equations for these four signals for each of the eight ALU functions. The R and S inputs are the two inputs selected according to Figure 2.

Definitions (+ = OR)

$P_0 = R_0 + S_0$ $\quad G_0 = R_0S_0$

$P_1 = R_1 + S_1$ $\quad G_1 = R_1S_1$

$P_2 = R_2 + S_2$ $\quad G_2 = R_2S_2$

$P_3 = R_3 + S_3$ $\quad G_3 = R_3S_3$

$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$

$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

I_{543}	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \forall C_4$
1	S − R	← Same as R + S equations, but substitute $\overline{R_i}$ for R_i in definitions →			
2	R − S	← Same as R + S equations, but substitute $\overline{S_i}$ for S_i in definitions →			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R}$ ∧ S	LOW	← Same as R ∧ S equations, but substitute $\overline{R_i}$ for R_i in definitions →		
6	R ∀ S	← Same as $R \forall S$, but substitute $\overline{R_i}$ for R_i in definitions →			
7	$\overline{R \forall S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0 (G_0 + C_n)}$	See note

Note: $[\overline{P}_2+\overline{G}_2\overline{P}_1+\overline{G}_2\overline{G}_1\overline{P}_0+\overline{G}_2\overline{G}_1\overline{G}_0C_n] \forall [\overline{P}_3+\overline{G}_3\overline{P}_2+\overline{G}_3\overline{G}_2\overline{P}_1+\overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0+\overline{G}_3\overline{G}_2\overline{G}_1\overline{G}_0C_n]$ + = OR

Figure 8.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2901APC	P-40	C	C-1
AM2901ADC	D-40	C	C-1
AM2901ADC-B	D-40	C	B-1
AM2901ADM	D-40	M	C-3
AM2901ADM-B	D-40	M	B-3
AM2901AFM	F-42	M	C-3
AM2901AFM-B	F-42	M	B-3
AM2901AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2901AXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Figure 9.

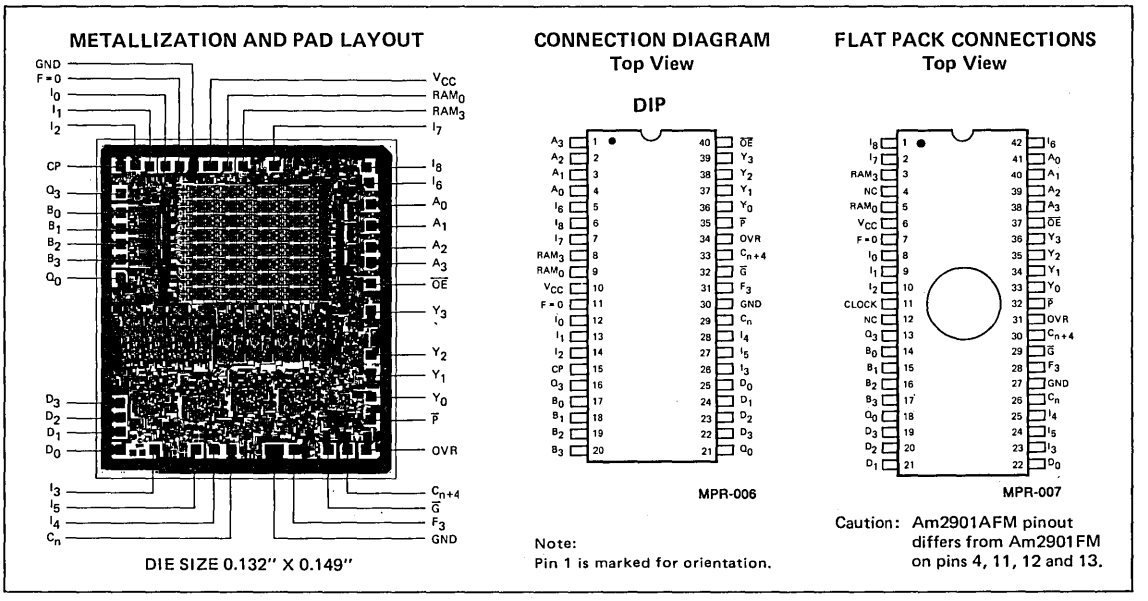


Figure 10.

PIN DEFINITIONS

A_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the A-port.

B_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes LOW.

I_{0-8} The nine instruction control lines to the Am2901A, used to determine what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q-register or the register stack (I_{678}).

Q_3 RAM_3 A shift line at the MSB of the Q register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the Am2901A. When the destination code on I_{678} indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three-state outputs are OFF(high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).

Q_0 RAM_0 Shift lines like Q_3 and RAM_3, but at the LSB of the Q-register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.

D_{0-3} Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the Am2901A. D_0 is the LSB.

Y_{0-3} The four data outputs of the Am2901A. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code I_{678}.

$\overline{OE}$ Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).

$\overline{P}, \overline{G}$ The carry generate and propagate outputs of the Am2901A's ALU. These signals are used with the Am2902 for carry-lookahead.

OVR Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.

F = 0 This is an open collector output which goes HIGH (OFF) if the data on the four ALU outputs F_{0-3} are all LOW. In positive logic, it indicates the result of an ALU operation is zero.

F_3 The most significant ALU output bit.

C_n The carry-in to the Am2901A's ALU.

C_{n+4} The carry-out of the Am2901A's ALU.

CP The clock to the Am2901A. The Q register and register stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which compromises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

OPERATING RANGE

P/N Suffix	Temperature	V_{CC}
PC, DC	T_A = 0°C to +70°C	4.75 V to 5.25 V
DM, FM	T_C = −55°C to +125°C	4.50 V to 5.50 V

STANDARD SCREENING

(Conforms to MIL-STD-883 for Class C Parts)

Step	MIL-STD-883 Method	Conditions	Level PC, DC	Level DM, FM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C 24-hour 150°C	100%	100%
Temperature Cycle	1010	C −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B 10,000 G	100% *	100%
Fine Leak	1014	A 5×10^{-8} atm-cc/sec	100% *	100%
Gross Leak	1014	C2 Fluorocarbon	100% *	100%
Electrical Test Subgroups 1 and 7	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening here for Class B Parts				
Group A Sample Tests	5005	See below for definitions of subgroups		
Subgroup 1			LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 7
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 7

*Not applicable for PC

ADDITIONAL SCREENING FOR CLASS B PARTS

Step	MIL-STD-883 Method	Military (Suffix DMB, FMB) Conditions	Military Level	Commercial (Suffix PCB, DCB) Conditions	Commercial Level
Burn-In	1015	D 125°C, 160 hours min.	100%	C or D 75°C, 48 hours min.	100%
Electrical Test	5004				
Subgroup 1			100%		100%
Subgroup 2			100%		–
Subgroup 3			100%		–
Subgroup 7			100%		100%
Subgroup 9			100%		–
Return to Group A Tests in Standard Screening					

GROUP A SUBGROUPS

(as defined in MIL-STD-883, method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum rated temperature
3	DC	Minimum rated temperature
7	Function	25°C
8	Function	Maximum and minimum rated temperature
9	Switching	25°C
10	Switching	Maximum Rated Temeperature
11	Switching	Minimum Rated Temperature

Am2901A
ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)
(Group A, Subgroups 1, 2, and 3)

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}		I_{OH} = −1.6mA Y_0, Y_1, Y_2, Y_3	2.4			Volts
				I_{OH} = −1.0mA, C_{n+4}	2.4			
				I_{OH} = −800μA, OVR, $\overline{P}$	2.4			
				I_{OH} = −600μA, F_3	2.4			
				I_{OH} = −600μA $RAM_{0,3}$, $Q_{0,3}$	2.4			
				I_{OH} = −1.6mA, $\overline{G}$	2.4			
I_{CEX}	Output Leakage Current for F = 0 Output	V_{CC} = MIN., V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}					250	μA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			$\overline{G}$, F = 0	I_{OL} = 16mA			0.5	
			C_{n+4}	I_{OL} = 10mA			0.5	
			OVR, $\overline{P}$	I_{OL} = 8.0mA			0.5	
			F_3, $RAM_{0,3}$, $Q_{0,3}$	I_{OL} = 6.0mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 7)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 7)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V		Clock, $\overline{OE}$			−0.36	mA
				A_0, A_1, A_2, A_3			−0.36	
				B_0, B_1, B_2, B_3			−0.36	
				D_0, D_1, D_2, D_3			−0.72	
				I_0, I_1, I_2, I_6, I_8			−0.36	
				I_3, I_4, I_5, I_7			−0.72	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			−0.8	
				C_n			−3.6	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		Clock, $\overline{OE}$			20	μA
				A_0, A_1, A_2, A_3			20	
				B_0, B_1, B_2, B_3			20	
				D_0, D_1, D_2, D_3			40	
				I_0, I_1, I_2, I_6, I_8			20	
				I_3, I_4, I_5, I_7			40	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			100	
				C_n			200	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX.		Y_0, Y_1, Y_2, Y_3 V_O = 2.4V			50	μA
				Y_0, Y_1, Y_2, Y_3 V_O = 0.5V			−50	
				$RAM_{0,3}$, $Q_{0,3}$ V_O = 2.4V (Note 4)			100	
				$RAM_{0,3}$, $Q_{0,3}$ V_O = 0.5V (Note 4)			−800	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX. + 0.5V, V_O = 0.5V		$Y_0, Y_1, Y_2, Y_3, \overline{G}$	−30		−85	mA
				C_{n+4}	−30		−85	
				OVR, $\overline{P}$	−30		−85	
				F_3	−30		−85	
				$RAM_{0,3}$, $Q_{0,3}$	−30		−85	
I_{CC}	Power Supply Current (Note 6)	V_{CC} = MAX. (See Fig. 12)	Am2901APC, DC	T_A = 25°C		160	250	mA
				T_A = 0°C to +70°C		160	265	
				T_A = +70°C		160	220	
			Am2901ADM, FM	T_C = −55°C to +125°C		160	280	
				T_C = +125°C		160	190	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I_{678} in a state such that the three-state output is OFF.
5. "MIL" = Am2901AXM, DM, FM. "COM'L" = Am2901AXC, PC, DC.
6. Worst case I_{CC} is at minimum temperature.
7. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

ROOM TEMPERATURE SWITCHING CHARACTERISTICS

(See next page for AC Characteristics over operating range.)

Tables I, II, and III below define the timing characteristics of the Am2901A at 25°C. The tables are divided into three types of parameters; clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

All values are at 25°C and 5.0V. Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level. All outputs fully loaded.

TABLE I

CYCLE TIME AND CLOCK CHARACTERISTICS

TIME	TYPICAL	GUARANTEED
Read-Modify-Write Cycle (time from selection of A, B registers to end of cycle)	55ns	93ns
Maximum Clock Frequency to Shift Q Register (50% duty cycle)	40MHz	20MHz
Minimum Clock LOW Time	30ns	30ns
Minimum Clock HIGH Time	30ns	30ns
Minimum Clock Period	75ns	93ns

TABLE II

COMBINATIONAL PROPAGATION DELAYS (all in ns, C_L = **50pF** (except output disable tests))

From Input \ To Output	TYPICAL 25°C, 5.0V								GUARANTEED 25°C, 5.0V							
	Y	F_3	C_{n+4}	$\overline{G}, \overline{P}$	F=0 R_L= 270	OVR	Shift Outputs		Y	F_3	C_{n+4}	$\overline{G}, \overline{P}$	F=0 R_L= 270	OVR	Shift Outputs	
							RAM_0 RAM_3	Q_0 Q_3							RAM_0 RAM_3	Q_0 Q_3
A, B	45	45	45	40	65	50	60	–	75	75	70	59	85	76	90	–
D (arithmetic mode)	30	30	30	25	45	30	40	–	39	37	41	31	55	45	59	–
D (I = X37) (Note 5)	30	30	–	–	45	–	40	–	36	34	–	–	51	–	53	–
C_n	20	20	10	–	35	20	30	–	27	24	20	–	46	26	45	–
I_{012}	35	35	35	25	50	40	45	–	50	50	46	41	65	57	70	–
I_{345}	35	35	35	25	45	35	45	–	50	50	50	42	65	59	70	–
I_{678}	15	–	–	–	–	–	20	20	26	–	–	–	–	–	26	26
$\overline{OE}$ Enable/Disable	20/20	–	–	–	–	–	–	–	30/33	–	–	–	–	–	–	–
A bypassing ALU (I = 2xx)	30	–	–	–	–	–	–	–	35	–	–	–	–	–	–	–
Clock ↓ (Note 6)	40	40	40	30	55	40	55	20	52	52	52	41	70	57	71	30

TABLE III

SET-UP AND HOLD TIMES (all in ns) (Note 1)

From Input	Notes	TYPICAL 25°C, 5.0V		GUARANTEED 25°C, 5.0V	
		Set-Up Time	Hold Time	Set-Up Time	Hold Time
A, B Source	2, 4 3, 5	40 $t_{pw}L$ + 15	0	93 $t_{pw}L$ + 25	0
B Dest.	2, 4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
D (arithmetic mode)		25	0	70	0
D (I = X37) (Note 5)		25	0	60	0
C_n		15	0	55	0
I_{012}		30	0	64	0
I_{345}		30	0	70	0
I_{678}	4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 25	0
$RAM_{0, 3}$, $Q_{0, 3}$		15	0	20	0

Notes: 1. See next page.
2. If the B address is used as a source operand, allow for the "A, B source" set-up time; if it is used only for the destination address, use the "B dest." set-up time.
3. Where two numbers are shown, both must be met.
4. "$t_{pw}L$" is the clock LOW time.
5. DV0 is the fastest way to load the RAM from the D inputs. This function is obtained with I = 337.
6. Using Q register as source operand in arithmetic mode. Clock is not normally in critical speed path when Q is not a source.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE FOR Am2901A

(See previous page for room temperature characteristics.)

Tables IV, V, and VI below define the timing characteristics of the Am2901A over the operating voltage and temperature range. The tables are divided into three types of parameters; clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level. Input rise and fall times are 1ns/V. All outputs fully loaded.

TABLE IV

CYCLE TIME AND CLOCK CHARACTERISTICS

TIME	COMMERCIAL	MILITARY
Read-Modify-Write Cycle (time from selection of A, B registers to end of cycle)	100ns	110ns
Maximum Clock Frequency to Shift Q Register (50% duty cycle) I = 432 or 632	15MHz	12MHz
Minimum Clock LOW Time	30ns	30ns
Minimum Clock HIGH Time	30ns	30ns
Minimum Clock Period	100ns	110ns

Commercial = Am2901APC, DC, XC T_A = 0°C to +70°C V_{CC} = 4.75 to 5.25V
Military = Am2901ADM, FM, XM T_C = −55°C to +125°C V_{CC} = 4.50 to 5.50V

TABLE V

GUARANTEED COMBINATIONAL PROPAGATION DELAYS (all in ns, C_L = 50pF (except output disable tests))

From Input \ To Output	COMMERCIAL								MILITARY							
	Y	F_3	C_{n+4}	$\overline{G}, \overline{P}$	F=0 R_L= 270	OVR	Shift Outputs		Y	F_3	C_{n+4}	$\overline{G}, \overline{P}$	F=0 R_L= 270	OVR	Shift Outputs	
							RAM_0 RAM_3	Q_0 Q_3							RAM_0 RAM_3	Q_0 Q_3
A, B	80	80	75	65	87	85	95	—	85	85	80	70	97	90	100	—
D (arithmetic mode)	45	45	45	35	57	55	65	—	50	50	50	40	62	60	70	—
D (I = X37) (Note 5)	40	40	—	—	52	—	60	—	45	45	—	—	57	—	65	—
C_n	30	30	20	—	47	30	50	—	35	35	25	—	52	35	55	—
I_{012}	55	55	50	45	67	65	75	—	60	60	55	50	72	70	80	—
I_{345}	55	55	55	50	67	65	75	—	60	60	60	55	72	70	80	—
I_{678}	30	—	—	—	—	—	30	30	35	—	—	—	—	—	35	35
$\overline{OE}$ Enable/Disable	35/25	—	—	—	—	—	—	—	40/25	—	—	—	—	—	—	—
A bypassing ALU (I = 2xx)	45	—	—	—	—	—	—	—	50	—	—	—	—	—	—	—
Clock ↓ (Note 6)	60	60	60	50	72	70	80	30	65	65	65	55	82	75	85	35

TABLE VI

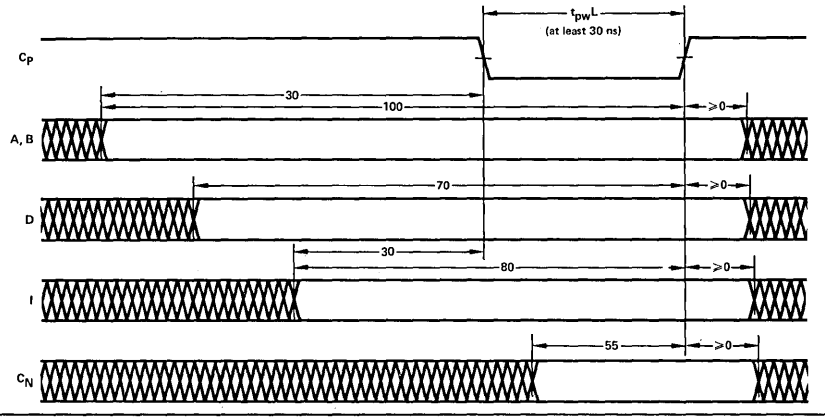
GUARANTEED SET-UP AND HOLD TIMES (all in ns) (Note 1)

From Input	Notes	COMMERCIAL		MILITARY	
		Set-Up Time	Hold Time	Set-Up Time	Hold Time
A, B Source	2, 4 3, 5	100 $t_{pw}L$+30	0	110 $t_{pw}L$+30	0
B Dest.	2, 4	$t_{pw}L$+15	0	$t_{pw}L$+15	0
D (arithmetic mode)		70	0	75	0
D (I = X37) (Note 5)		60	0	65	0
C_n		55	0	60	0
I_{012}		80	0	85	0
I_{345}		80	0	85	0
I_{678}	4	$t_{pw}L$+30	0	$t_{pw}L$+30	0
$RAM_{0, 3}$, $Q_{0, 3}$		25	0	25	0

Notes: 1. See Figure 11. All times relative to clock LOW-to-HIGH transition.
2. If the B address is used as a source operand, allow for the "A, B source" set-up time; if it is used only for the destination address, use the "B dest." set-up time.
3. Where two numbers are shown, both must be met.
4. "$t_{pw}L$" is the clock LOW time.
5. D V 0 is the fastest way to load the RAM from the D inputs. This function is obtained with I = 337.
6. Using Q register as source operand in arithmetic mode. Clock is not normally in critical speed path when Q is not a source.

SET-UP AND HOLD TIMES (minimum cycles from each input)

Set-up and hold times are defined relative to the clock LOW-to-HIGH edge. Inputs must be steady at all times from the set-up time prior to the clock until the hold time after the clock. The set-up times allow sufficient time to perform the correct operation on the correct data so that the correct ALU data can be written into one of the registers.



MPR-008

Figure 11. Minimum Cycle Times from Inputs. Numbers Shown are Minimum Data Stable Times for Am2901ADC, in ns. See Table VI for Detailed Information.

I_{CC} Versus Temperature for Am2901A

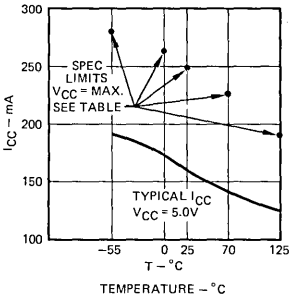
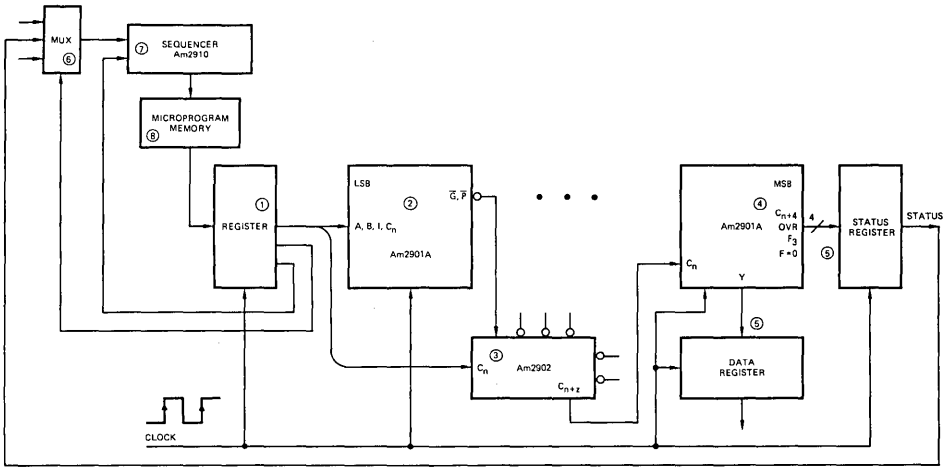


Figure 12.

MPR-009

MINIMUM CYCLE TIME CALCULATIONS FOR 16-BIT SYSTEMS

Speeds used in calculations for parts other than Am2901A are representative for available MSI parts.

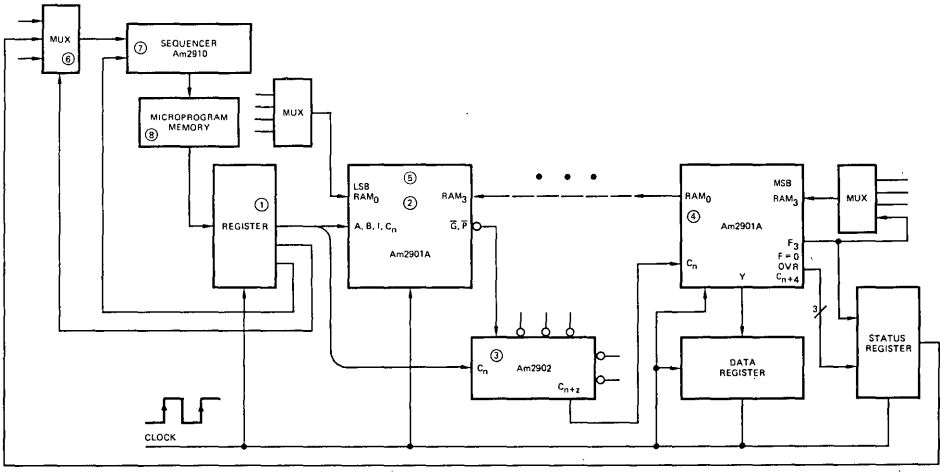


MPR-010

Pipelined System. Add without Simultaneous Shift.

DATA LOOP			CONTROL LOOP		
① Register	Clock to Output	15	① Register	Clock to Output	15
+ ② 2901A	A, B to $\overline{G}$, $\overline{P}$	65	+ ⑥ MUX	Select to Output	20
+ ③ 2902	$\overline{G}_0$, $\overline{P}_0$ to C_{n+z}	10	+ ⑦ 2910	CC to Output	45
+ ④ 2901A	C_n to C_{n+4}, OVR, F_3, F = 0, Y	50	+ ⑧ PROM	Access Time	60
+ ⑤ Register	Set-up Time	5	+ ① Register	Set-up Time	5
		145ns			145ns

Minimum clock period = 145ns



MPR-011

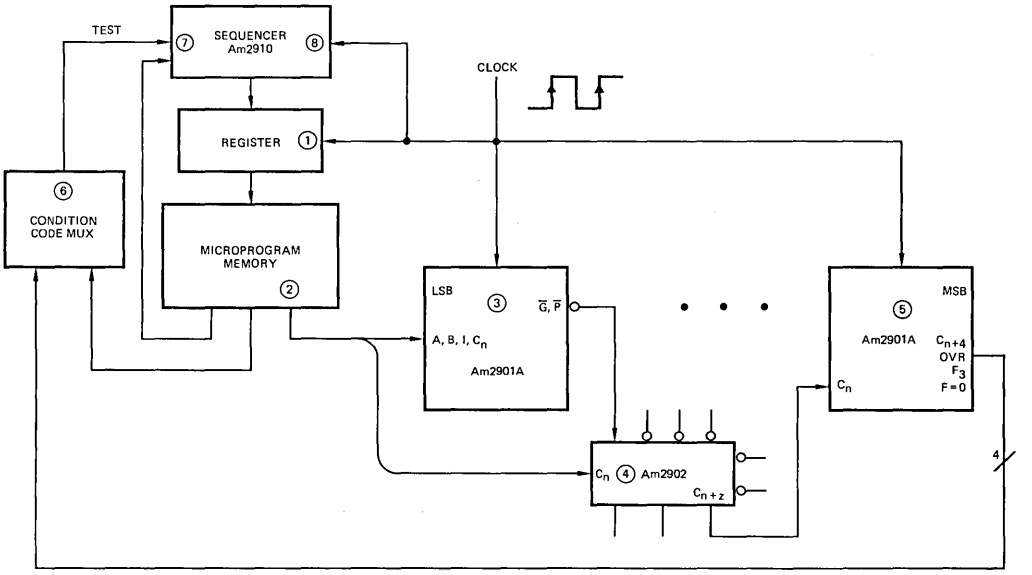
Pipelined System. Simultaneous Add and Shift Down

DATA LOOP			CONTROL LOOP		
① Register	Clock to Output	15	① Register	Clock to Output	15
+ ② 2901A	A, B to $\overline{G}$, $\overline{P}$	65	+ ⑥ MUX	Select to Output	20
+ ③ 2902	$\overline{G}_0\overline{P}_0$ to C_{n+z}	10	+ ⑦ 2910	CC to Output	45
+ ④ 2901A	C_n to RAM_0	50	+ ⑧ PROM	Access Time	60
+ ⑤ 2901A	RAM_3 Set-up Time	25	+ ① Register	Set-up Time	5
		165ns			145ns

Minimum clock period = 165ns

Note: Care is required to define the worst case path at the ends of the array during an add and shift operation. In a shift down (toward LSB), RAM_0 and Q_0 are available after the A, B → RAM, Q delay. In a shift up (toward MSB), Q_3 is available after the A, B → RAM, Q delay. RAM_3, however, is not available until the carry has propagated through the 2902. This is the same as the data loop shown above. If the most significant RAM_3 output were returned through a multiplexer to the RAM_0 or Q_0 input, then this path would be longer than the one shown, but this connection is highly unlikely.

MINIMUM CYCLE TIME CALCULATIONS FOR 16-BIT SYSTEMS (Cont.)

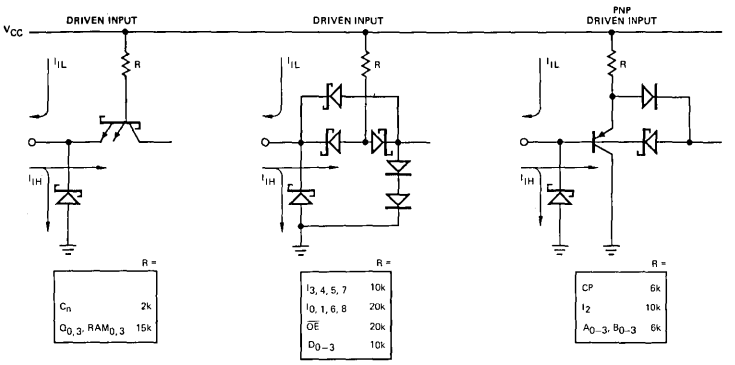


Non-Pipelined Addressed Based Architecture. Instruction Execute and Conditional Branch allowed on Same Cycle (e.g. = subtract and branch if F = 0)

Due to poor speeds, this type of architecture is not recommended. Compare with previous page.

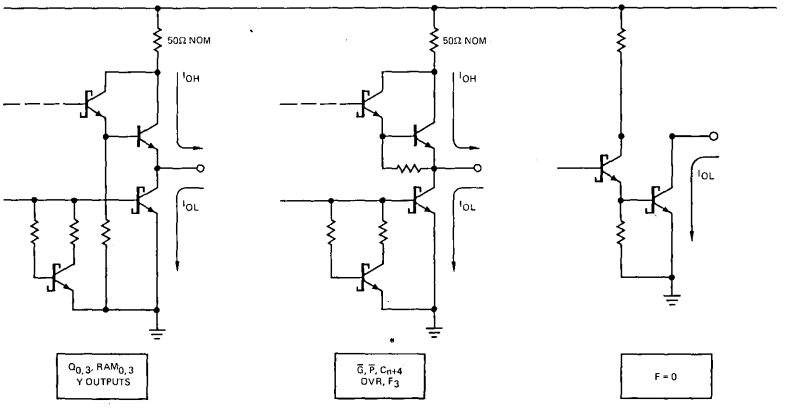
Minimum clock period =	① Register	Clock to output	20
+	② PROM	Access time	60
+	③ 2901A	$\overline{A}$, $\overline{B}$ to $\overline{G}$, $\overline{P}$	65
+	④ 2902	$\overline{G}_0\overline{P}_0$ to C_{n+z}	10
+	⑤ 2901A	C_n to C_{n+4}, OVR, F_3, F = 0	50
+	⑥ MUX	Data in to Data out	15
+	⑦ Am2910	Test to address out	45
+	① Register	Set-up time	5
			265ns

Note: Extra time needed if shift occurs on same cycle.



$C_I \approx 5.0pF$, all inputs.

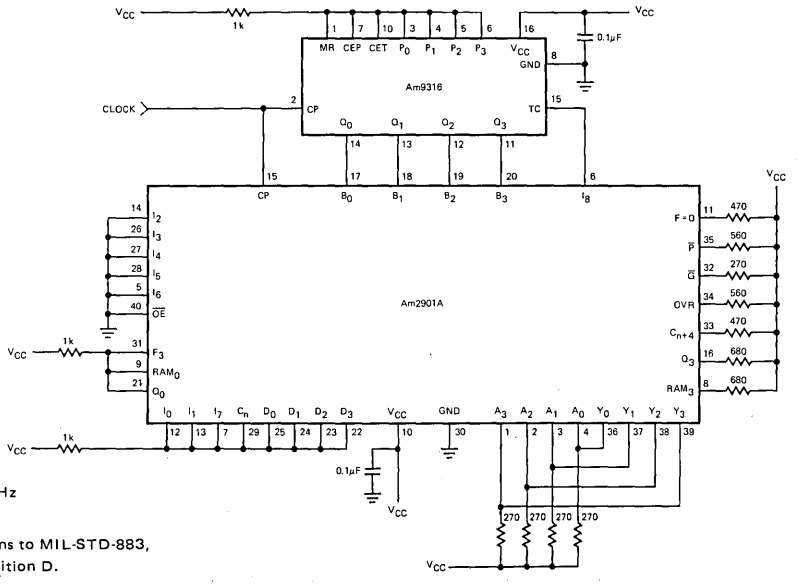
MPR-013



$C_O \approx 5.0pF$, all outputs.

Figure 13. Input/Output Current Interface Conditions.

MPR-014



$V_{CC} = 5.0V$
Frequency = 100KHz
$T_A = 125°C$

This circuit conforms to MIL-STD-883, method 1015, condition D.

Figure 14. Life Test and Burn-in Circuit for Military Class B Parts. (Contact Factory for Commercial Burn-in Conditions)

MPR-015

USING THE Am2901A

BASIC SYSTEM ARCHITECTURE

The Am2901A is designed to be used in microprogrammed systems. Figure 15 illustrates such an architecture. The nine instruction lines, the A and B addresses, and the D data inputs normally will all come from registers clocked at the same time as the Am2901A. The register inputs come from a ROM or PROM – the "microprogram store". This memory contains sequences of microinstructions, typically 28 to 40 bits wide, which apply the proper control signals to the Am2901A's and other circuits to execute the desired operation.

The address lines of the microprogram store are driven from the Am2910 microprogram sequencer. This device has facilities for storing an address, incrementing an address, jumping to any address, and linking subroutines. The Am2910 is controlled by some of the bits coming from the microprogram store. Essentially these bits are the "next instruction" control.

Note that with the microprogram register in-between the microprogram memory store and the Am2901A's, an instruction accessed on one cycle is executed on the next cycle. As one instruction is executed, the next instruction is being read from microprogram memory. In this configuration, system speed is improved because the execution time in the Am2901A's occurs in parallel with the access time of the microprogram store. Without the "pipeline register", these two functions must occur serially.

EXPANSION OF THE Am2901A

The Am2901A is a four-bit CPU slice. Any number of Am2901A's can be interconnected to form CPU's of 12, 16, 24, 36 or more bits, in four-bit increments. Figure 16 illustrates the interconnection of three Am2901A's to form a 12-bit CPU, using ripple carry. Figure 17 illustrates a 16-bit CPU using carry lookahead, and Figure 18 is the general carry lookahead scheme for long words.

With the exception of the carry interconnection, all expansion schemes are the same. Refer to Figure 16. The Q_3 and RAM_3 pins are bidirectional left/right shift lines at the MSB of the device. For all devices except the most significant, these lines are connected to the Q_0 and RAM_0 pins of the adjacent more significant device. These connections allow the Q-registers of all Am2901A's to be shifted left or right as a contiguous n-bit register, and also allow the ALU output data to be shifted left or right as a contiguous n-bit word prior to storage in the RAM. At the LSB and MSB of the CPU, the shift pins should be connected to three-state multiplexers which can be controlled by the microcode to select the appropriate input signals to the shift inputs. (See Figure 19)

The open collector F = 0 outputs of all the Am2901A's are connected together and to a pull-up resistor. This line will go HIGH if and only if the output of the ALU contains all zeroes. Most systems will use this line as the Z (zero) bit of the processor status word.

The overflow and F_3 pins are generally used only at the most significant end of the array, and are meaningful only when two's complement signed arithmetic is used. The overflow pin is the Exclusive-OR of the carry-in and carry-out of the sign bit (MSB). It will go HIGH when the result of an arithmetic

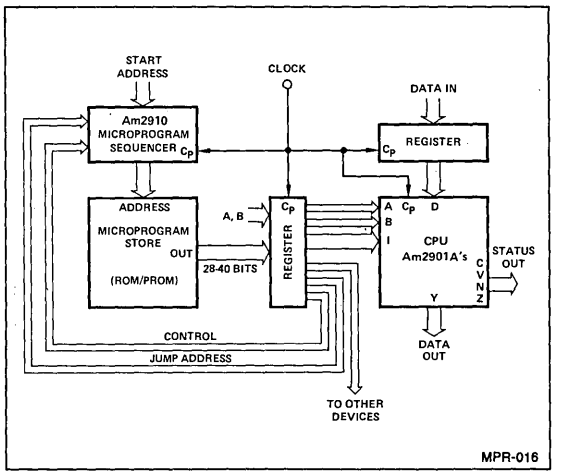


Figure 15. Microprogrammed Architecture Around Am2901A's.

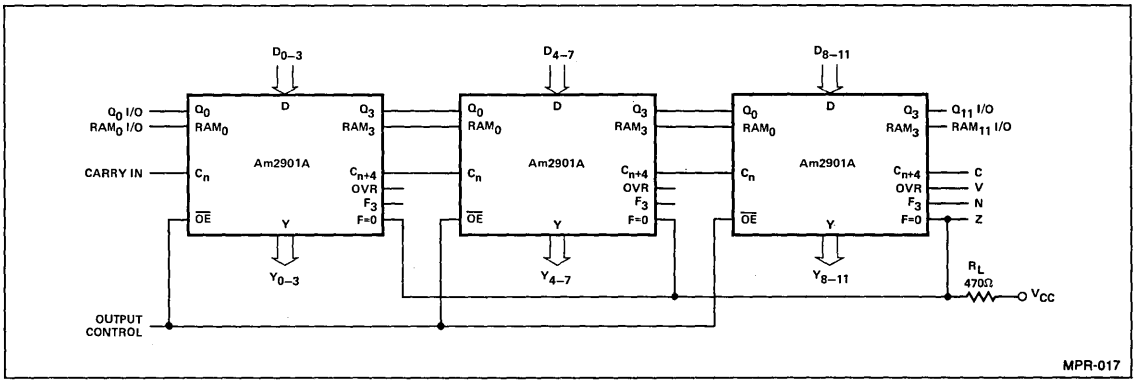


Figure 16. Three Am2901A's used to Construct 12-Bit CPU with Ripple Carry. Corresponding A, B, and I Pins on all Devices are Connected Together.

operation is a number requiring more bits than are available, causing the sign bit to be erroneous. This is the overflow (V) bit of the processor status word. The F_3 pin is the MSB of the ALU output. It is the sign of the result in two's complement notation, and should be used as the Negative (N) bit of the processor status word.

The carry-out from the most significant Am2901A (C_{n+4} pin) is the carry-out from the array, and is used as the carry (C) bit of the processor status word.

Carry interconnections between devices may use either ripple carry or carry lookahead. For ripple carry, the carry-out (C_{n+4}) of each device is connected to the carry-in (C_n) of the next more significant device. Carry lookahead uses the Am2902 lookahead carry generator. The scheme is identical to that used with the 74181/74182. Users unfamiliar with this technique should refer to AMD's application note on Arithmetic Logic Units. Figures 17 and 18 illustrate single and multiple level lookahead.

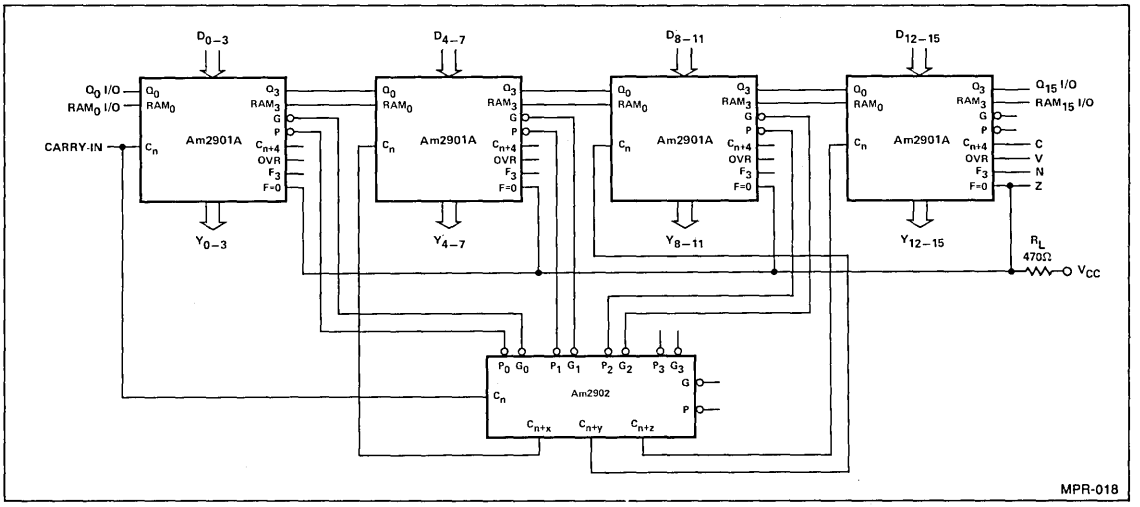


Figure 17. Four Am2901A's in a 16-Bit CPU using the Am2902 for Carry Lookahead.

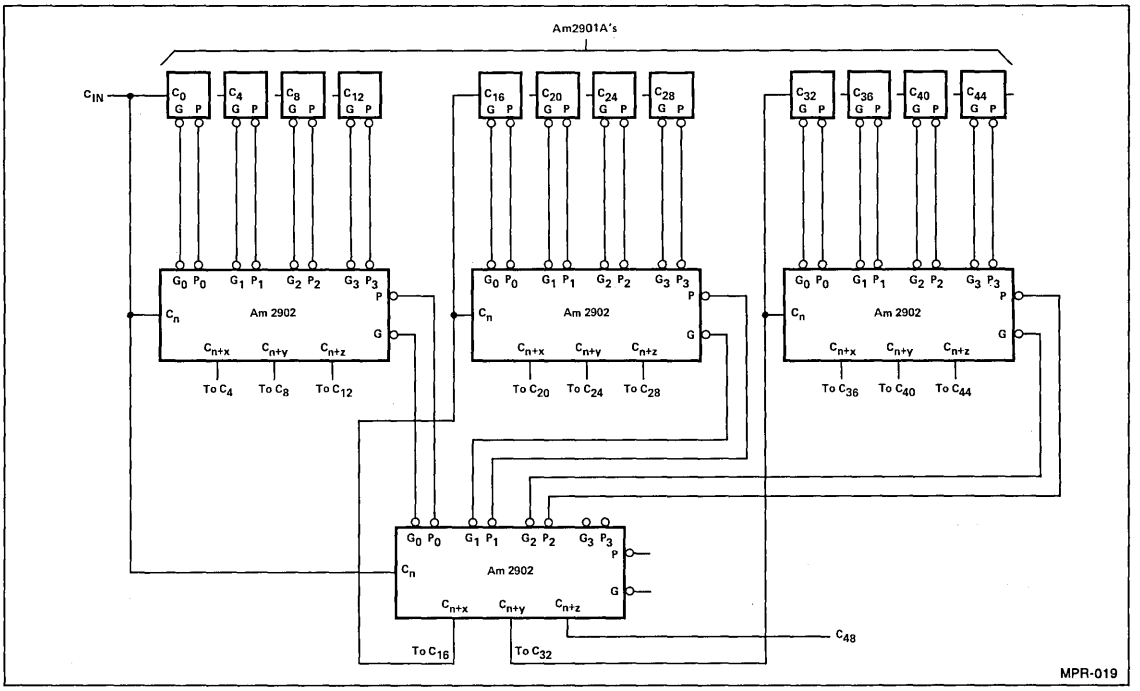


Figure 18. Carry Lookahead Scheme for 48-Bit CPU using 12 Am2901A's. The Carry-Out Flag (C_{48}) Should be Taken from the Lower Am2902 Rather than the Right-Most Am2901A for Higher Speed.

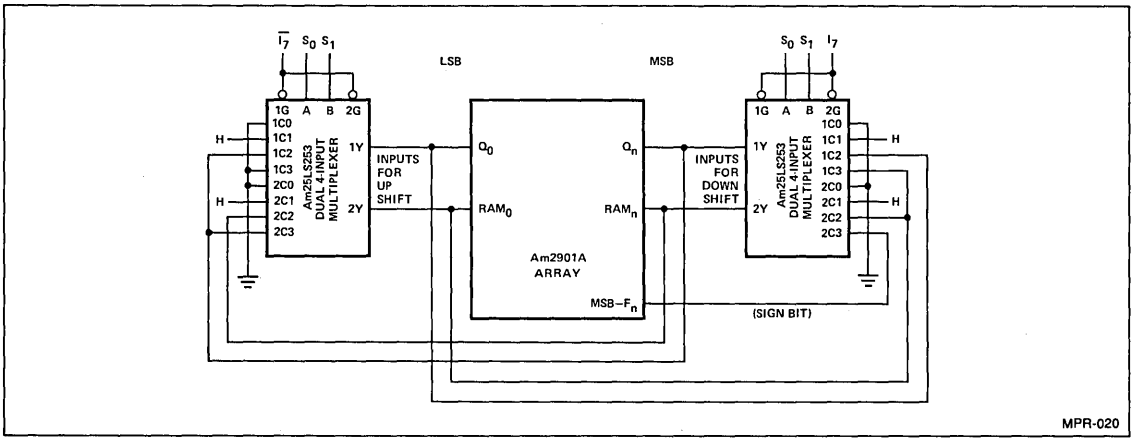


Figure 19. Three-State Multiplexers Used on Shift I/O Lines.

SHIFT I/O LINES AT THE END OF THE ARRAY

The Q-register and RAM left/right shift data transfers occur between devices over bidirectional lines. At the ends of the array, three-state multiplexers are used to select what the new inputs to the registers should be during shifting. The Am2904 includes these multiplexers in a single LSI chip. Figure 19 shows two Am25LS253 dual four-input multiplexers connected to provide four shift modes. Instruction bit I_7 (from the Am2901A) is used to select whether the left-shift multiplexer or the right-shift multiplexer is active. The four shift modes in this example are:

Zero A LOW is shifted into the MSB of the RAM on a down shift. If the Q-register is also shifted, then a LOW is deposited in the Q-register MSB. If the RAM or both registers are shifted up, LOWs are placed in the LSBs.

One Same as zero, but a HIGH level is deposited in the LSB or MSB.

Rotate A single precision rotate. The RAM MSB shifts into the LSB on a right shift and the LSB shifts into the MSB on a left shift. The Q-register, if shifted, will rotate in the same manner.

Arithmetic A double-length Arithmetic Shift if Q is also shifted. On an up shift a zero is loaded into the Q-register LSB and the Q-register MSB is loaded into the RAM LSB. On a down shift, the RAM LSB is loaded into the Q-register MSB and the ALU output MSB (F_n, the sign bit) is loaded into the RAM MSB. (This same bit will also be in the next less significant RAM bit.)

Code			Source of New Data				Shift	Type
I_7	S_1	S_0	Q_0	Q_n	RAM_0	RAM_n		
H	L	L	0	Q_{n-1}	0	F_{n-1}	Up	Zero
H	L	H	1	Q_{n-1}	1	F_{n-1}		One
H	H	L	Q_n	Q_{n-1}	F_n	F_{n-1}		Rotate
H	H	H	0	Q_{n-1}	Q_n	F_{n-1}		Arithmetic
L	L	L	Q_1	0	F_1	0	Down	Zero
L	L	H	Q_1	1	F_1	1		One
L	H	L	Q_1	Q_0	F_1	F_0		Rotate
L	H	H	Q_1	F_0	F_1	$RAM_n = RAM_{n-1} = F_n$		Arithmetic

HARDWARE MULTIPLICATION

Figure 20 illustrates the interconnections for a hardware multiplication using the Am2901A. The system shown uses two devices for 8 x 8 multiplication, but the expansion to more bits is simple — the significant connections are at the LSB and MSB only.

The basic technique used is the "add and shift" algorithm. One clock cycle is required for each bit of the multiplier. On each cycle, the LSB of the multiplier is examined; if it is a "1", then the multiplicand is added to the partial product to generate a new partial product. The partial product is then shifted one place toward the LSB, and the multiplier is also shifted one place toward the LSB. The old LSB of the multiplier is discarded. The cycle is then repeated on the new LSB of the multiplier available at Q_0.

The multiplier is in the Am2901A Q-register. The multiplicand is in one of the registers in the register stack, R_a. The product will be developed in another of the registers in the stack, R_b.

The A address inputs are used to address the multiplicand in R_a, and the B address inputs are used to address the partial product in R_b. On each cycle, R_a is conditionally added to R_b, depending on the LSB of Q as read from the Q_0 output, and both Q and the ALU output are shifted down one place. The instruction lines to the Am2901A on every cycle will be:

I_{876} = 4 (shift register stack input and Q register left)
I_{543} = 0 (Add)
I_{210} = 1 or 3 (select A, B or 0, B as ALU sources)

Figure 20 shows the connections for multiplication. The circled numbers refer to the paragraphs below.

1. The adjacent pins of the Q-register and RAM shifters are connected together so that the Q-registers of both (or all) Am2901A's shift left or right as a unit. Similarly, the entire eight-bit (or more) ALU output can be shifted as a unit prior to storage in the register stack.

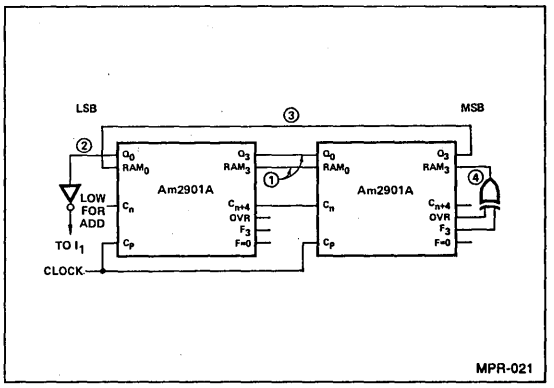


Figure 20. Interconnection for Dedicated Multiplication (8 by 8 Bit) (Corresponding A, B and I Connected Together).

2. The shift output at the LSB of the Q-register determines whether the ALU source operands will be A and B (add multiplicand to partial product) or 0 and B (add nothing to partial product. Instruction bit I_1 can select between A, B or 0, B as the source operands; it can be driven directly from the complement of the LSB of the multiplier.

3. As the new partial product appears at the input to the register stack, it is shifted left by the RAM shifter. The new LSB of the partial product, which is complete and will not be affected by future operations, is available on the RAM_0 pin. This signal is returned to the MSB of the Q-register. On each cycle then, the just-completed LSB of the product is deposited in the MSB of the Q-register; the Q-register fills with the least significant half of the product.

4. As the ALU output is shifted down on each cycle, the sign bit of the new partial product should be inserted in the RAM MSB shift input. The F_3 flag will be the correct sign of the partial product unless overflow has occurred. If overflow occurs during an addition or subtraction, the OVR flag will go HIGH and F_3 is not the sign of the result. The sign of the result must then be the complement of F_3. The correct sign bit to shift into the MSB of the partial product is therefore $F3 \oplus OVR$; that is, F_3 if overflow has not occurred and $\overline{F_3}$ if overflow has occurred. On the last cycle, when the MSB of the multiplier is examined, a conditional subtraction rather than addition should be performed, because the sign bit of the multiplier carries negative rather than positive arithmetic weight.

$$Y = -Y_i 2^i + Y_{i-1} 2^{i-1} + \ldots + Y_0 2^0$$

This scheme will produce a correct two's complement product for all multiplicands and multipliers in two's complement notation.

Figure 21 is a table showing the input states of the Am2901A for each step of a signed, two's complement multiplication. The Am2904 LSI chip conveniently implements the required shift linkages and the EX-OR function for this algorithm.

Initial Register States

R

0	Multiplier
1	Multiplicand
2	X
3	X

Am2901A Microcode

Program 2's Comp. Multiply

Date 8/5/75 By J. S.

Final Register States

R

0	Multiplier
1	Multiplicand
2	LSH Product
3	MSH Product

S, F →	D	Description	Repeat	Pin States (Octal)										Jump	
				A	B	I_{876}	I_{543}	I_{210}	C_n	Q_0	Q_3	RAM_0	RAM_3	To	If
0 ∨ A	Q	Move Multiplier to Q	–	0	X	0	3	4	X	X	X	X	X		
0 ∧ B	B	Clear R_3	–	X	3	2	4	3	X	X	X	X	X		
(O+B)/2 (A+B)/2	B	Cond. Add & Shift	n–1	1	3	4	0	1 or 3 $I_1 = Q_0 LO$	0	–	RAM_0	–	$F_3 \forall OVR$		
(B–O)/2 (B–A)/2	B	Cond. Subt. & Shift	–	1	3	4	1	1 or 3 $I_1 = Q_0 LO$	1	–	RAM_0	–	$F_3 \forall OVR$		
O ∨ Q	B	Move LSH Prod. to R_2	–	X	2	2	3	2	X	X	X	X	X		

X = Don't Care S = Source F = Function D = Destination

Figure 21.

Hardware Division

Division, unlike multiplication, is much more difficult to realize. One of these difficulties can be easily understood by visualizing a 2n-bit Dividend (X) and an n-bit Divisor (Y). The Quotient (Q) can range from 1 bit (when $X \leq Y$) to 2 n bits (when $Y = 1$), discarding the attempt to divide by 0. In most of the divide functions, the Remainder (R) is as important to find as is the Quotient – there is no equivalent to it in multiplication. Division becomes even more complicated when negative numbers are represented in the 2's complement notation. In the "everyday" decimal system, using Sign-and-Magnitude notation, dealing with negative numbers is relatively easy: The sign of the quotient is determined first and then a normal division is performed. Note that in this "normal" division we first "guess" the first digit of the quotient by comparing the most significant part of the dividend to the divisor. Then verify our guess by a multiplication (no "direct" division method is known), and continue to do so for all of the other digits, shifting the divisor to the right one place at a time.

The most straightforward division scheme (for unsigned numbers) is Subsequent Subtraction. The algorithm is as follows: Subtract divisor from dividend and increment a counter (initially reset to zero). Continue to do so as long as the Remainder is positive. When the Remainder becomes negative, cancel the last step; i.e., add back divisor and decrement counter. The counter will contain the Quotient and the Remainder will be correct. The main drawback of this scheme is, of course, the great number of arithmetic operations needed. Again, when dealing with signed numbers, the subtraction should be substituted by addition and vice versa.

A more rapid division can be realized by calculating the Quotient digits instead of counting them. In this algorithm, the divisor is first subtracted from the most significant part of the dividend. If the remainder is positive, the quotient digit is "1", otherwise the subtraction is cancelled (by adding the divisor to the remainder) and the quotient digit will be "0". Now shift the remainder one place to the right (much like you do in a "paper and pencil" division) and repeat until all the quotient digits have been calculated. This algorithm is called "Restoring Division". When signed numbers are involved, inversion of the operations and the quotient digits will be necessary and correction should be performed in some cases. Some time is wasted in the Restoring Division because for every "0" digit in the quotient, two arithmetic operations are needed. This can be saved in the "Non-Restoring Division".

The basis of Non-Restoring Division is the same as in Restoring Division. Consider first unsigned (positive) numbers only. At the beginning, the divisor is subtracted from the most significant part of the dividend. If the result (first remainder) is positive (or zero), the first quotient digit is "1". Otherwise, the quotient digit is "0", but do not restore! Shift divisor one place to the right (or remainder to the left) and add if last quotient digit was "0"; otherwise subtract. Determine quotient digit as before and continue until all quotient digits have been computed. The remainder will be correct if it is non-negative, otherwise correction is needed by a restoring operation (on the remainder only). Extreme care should be taken of the number of bits and the value of the divisor. Assuming the divisor has n bits and the dividend as 2n bits, the above process develops n+1 bits of the quotient. This will not be sufficient if the MSB of the divisor is "0" (which means that the divisor is a small number and more digits are needed in the quotient). Although this condition can be easily detected as overflow will occur in the first subtraction, it can be avoided by aligning the first "1" of the divisor to the MSB of the dividend (by shifting the divisor left until all leading zeros are discarded) before performing the first subtraction. Ample space should be provided for the additional bits of the quotient. Note that leading zeros in the dividend do not disturb the normal operation. The flow chart for unsigned non-restoring division is shown in Figure 22.

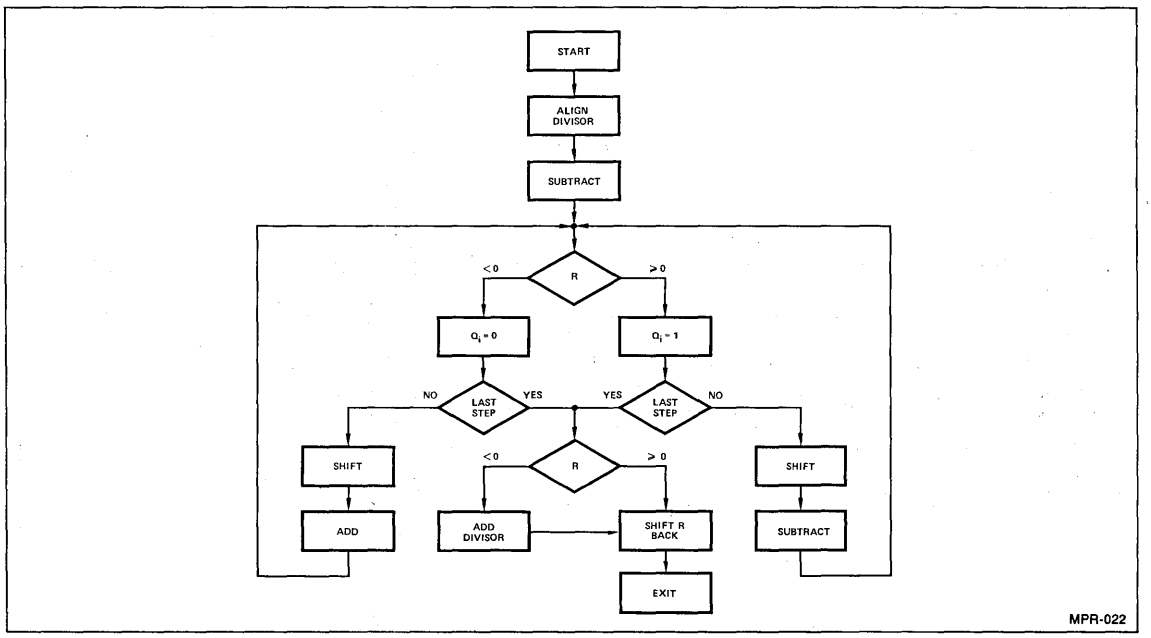


Figure 22. Flowchart for Non-Restoring Division (Unsigned Numbers).

The unsigned division scheme can be applied to signed positive numbers without any change. When negative numbers are encountered, however, changes in the algorithm are necessary. The straightforward method of signed division seems to be "Division in the first quadrant." In that scheme, negative numbers are 2's complemented to obtain positive numbers, remembering the changes done. The division is performed on positive numbers, and finally again 2's complementing occurs wherever necessary. Figure 23 is the flowchart for this algorithm.

Figure 24 is the Interconnection Diagram for both the alignment procedure and the Division Algorithm. It is assumed that the Dividend is in Register R_X (it will be lost during the division and replaced by the Remainder), the Divisor is in Register R_Y. The Quotient will be in the Q register, which should be cleared beforehand.

After checking the signs of the Dividend and Divisor, setting the flags and negating (using 23 or 24 octal as I_5 through I_0 ALU control bits) when necessary, the Divisor should be aligned. This can be done by ORing R_X with 0 (I_{5-0} = 33 octal). The most significant bit is deposited in the Status Register, and can be shifted out by setting $I_8 = I_6$ = HIGH and I_7 to the Exclusive NOR of the previous and present MSB of the Divisor. If these are both "0", I_7 will be HIGH, and an up shift will occur, filling in trailing zeros. When the checked bits are different, I_7 will go LOW, causing a down shift. At the same time the Y output of the Status Register is enabled the leftmost "0" (the sign bit) will be restored.

The first step in the Division routine is a subtract, then shift the R_X and Q registers up. I_{876} will be 6 in octal while I_{210} = 1 in octal and $I_5 = I_4$ = LOW. Pulling the CL bit in the microcode to HIGH, both I_3 and C_n will be HIGH and the ALU is performing a 2's complement subtract. The sign of the Remainder will be latched in the Status Register and the complement of it will be stored in the LSB of the Q register during the shift up operation, which also discards the sign bit of the Remainder.

Now repeating the same operation for all of the other bits of the Remainder with the CL bit in the microcode LOW will leave the control of I_3 to the (complemented) previous sign bit. If it was "0" ($R \geq 0$), I_3 and C_n will be HIGH and the ALU will subtract; if it was 1 ($R < 0$), I_3 and C_n will be LOW and the ALU will ADD, as required. In each up shift, the complement of the present sign bit will be placed at the right of the Quotient, again, as required.

At the end of the division, the sign of the Remainder should be examined and if it is HIGH, the Divisor should be added to it. This can be easily implemented (not depicted on Figure 24) by performing an unconditional ADD (with C_n LOW), letting I_2 LOW, I_0 HIGH and controlling I_1 by the complement of the sign of the Remainder, thus adding to RX either RY (if $R_S = 1$) or zero (if R_S = 0). If an alignment was performed, the remainder should be shifted down the same number of places.

Finally, the Quotient and/or the Remainder should be 2's complemented again according to the flags.

Figure 25 is a table showing the input states of the Am2901A's for each phase of the Alignment and Division.

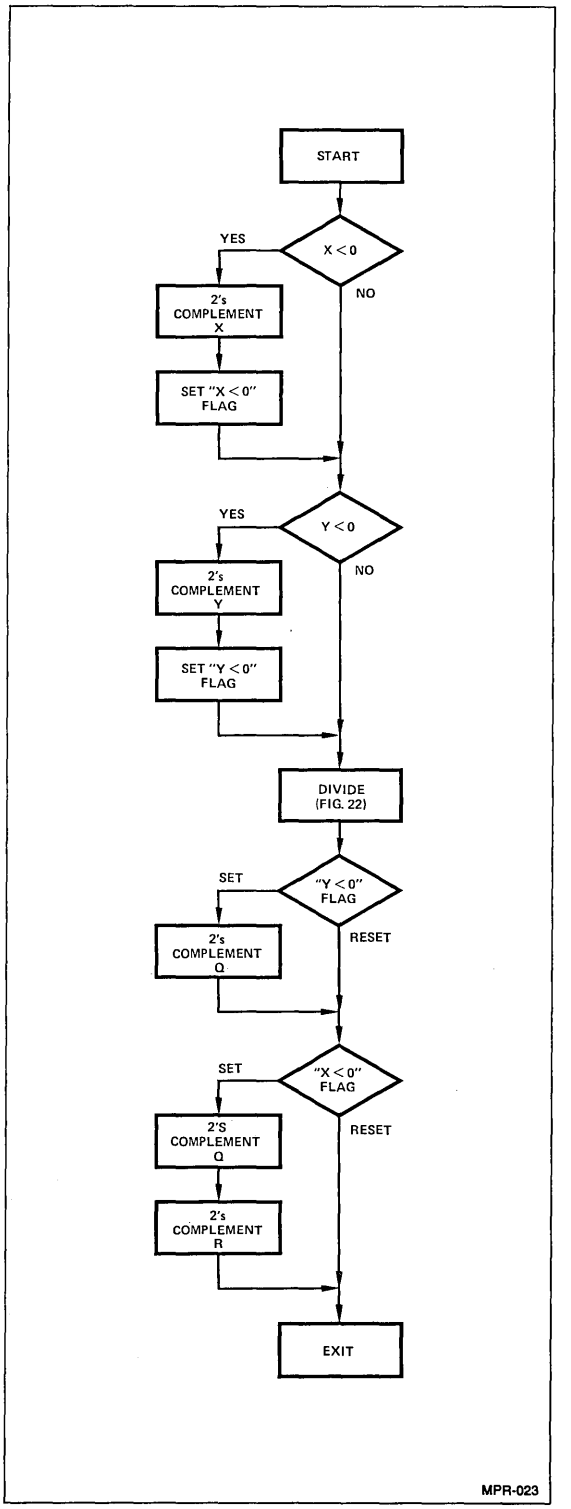


Figure 23. Flowchart for First Quadrant Division with Signed Numbers.

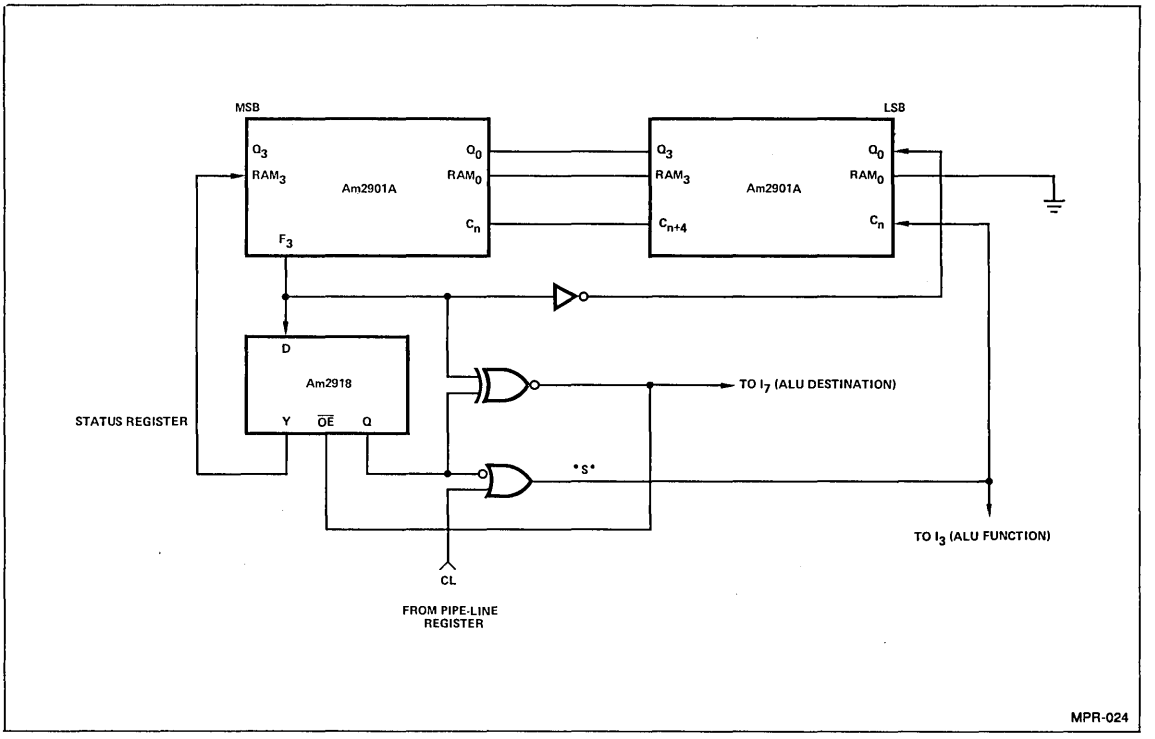


Figure 24. Interconnections for Dedicated Division.

Initial Register Status

R

0	Dividend
1	Divisor
Q	(Cleared)

Am2901A Microcode

Program: 2's Complement Division
Date: 9/24/76 By: M.S.

Final Register Status

R

0	Remainder
1	Divisor
Q	Quotient

					Pin Status (Octal)										Jump	
S, F	D	Description	CL	Repeat	A	B	I_{876}	I_{543}	I_{210}	C_n	Q_0	Q_3	RAM_0	RAM_3	to	if
OVB	B	Align Divisor	X	k	X	1	5/7	3	3	X	X	X	0	X or Sign		
(B−A)*2	B	First Subtract & Shift	1	–	1	0	6	1	1	1	$\overline{F_3}$	X	0	X		
(B±A)*2	B	Loop Subtract/Add & Shift	0	k	1	0	6	1/0	1	1/0	$\overline{F_3}$	X	0	X		
B+A or	B	Correct Remainder	X	–	1	0	3	0	1/3	0	X	X	X	X		
B+0	B	Shift Remainder	1	k	X	1	5	1	3	1	X	X	X	Sign		

k = Number of leading zeros of the Divisor

Figure 25. Am2901 Microcode for Dedicated Division.

EXAMPLES OF SOME OTHER OPERATIONS

1. **Byte Swapping**

   Occasionally the two halves of a 16-bit word must be swapped. D_{0-7} is interchanged with D_{8-15}. The quickest way to perform this operation is to rotate the word in RAM, shifting two bits at a time. Only four shift cycles are required. The same register is selected on both the A and B ports; the two are added together with carry-in connected to carry-out, producing a right shift of one place; then the ALU is shifted right one more place prior to storage.

   Byte Swap of R_0

   $A = B = 0$ $I = 701$ $RAM_0 = RAM_{15}$ $C_{IN} = C_{OUT}$

   Repeat 4 times.

2. **Instruction Fetch Cycle**

   Execution of a macroinstruction generally begins with an instruction fetch cycle. The current contents of the PC (in one of the registers) is the address of the macroinstruction to be fetched, and must be read out to the memory address register. Then the PC is incremented to point to the next macroinstruction. The macroinstruction obtained from memory is then loaded into the microprogram sequencer to cause a jump to the microcode for executing the instruction.

   The PC can be read out and incremented in one cycle by using the Am2901A destination code 2, and addressing the PC with both the A and B addresses. The current value of PC will appear on the Y outputs, and PC+1 will be returned to the register. If the PC is in register 15, then:

   $A = B = 15$, $I = 203$, Carry-in = 1

   The PC will be on the Y outputs via the RAM A-port. On the clock LOW-to-HIGH transition, the program counter is incremented and the value on the Y outputs is loaded into the memory address register. During the following cycle, the memory is read and, on the next clock LOW-to-HIGH transition the instruction from the memory is dropped into the instruction register. The fetch operation requires only two microcycles.

ADDITIONAL READING

For more detailed information on applications of the Am2901A, the following application notes are available from AMD.

Title	Publication Number
A 16-Bit Microprogrammed Computer	AM-PUB 030
An Emulation of the Am9080A	AM-PUB 064
A High Performance Disc Controller	AM-PUB 065

Am2902A

High-Speed Look-Ahead Carry Generator

DISTINCTIVE CHARACTERISTICS

- Provides look-ahead carries across a group of four Am2901A microprocessor ALU's
- Capability of multi-level look-ahead for high-speed arithmetic operation over large word lengths
- Typical carry propagation delay of 4.5 ns
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

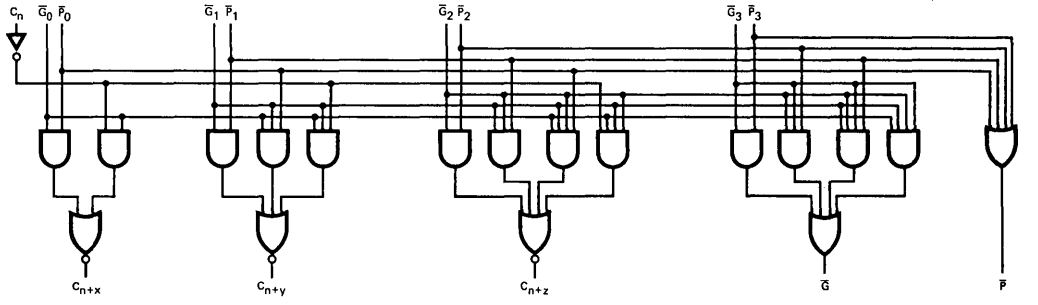
The Am2902A is a high-speed, look-ahead carry generator which accepts up to four pairs of carry propagate and carry generate signals and a carry input and provides anticipated carries across four groups of binary ALU's. The device also has carry propagate and carry generate outputs which may be used for further levels of look-ahead.

The Am2902A is generally used with the Am2901A bipolar microprocessor unit to provide look-ahead over word lengths of more than four bits. The look-ahead carry generator can be used with binary ALU's in an active LOW or active HIGH input operand mode by reinterpreting the carry functions. The connections to and from the ALU to the look-ahead carry generator are identical in both cases.

The logic equations provided at the outputs are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$
$$P = P_3P_2P_1P_0$$

LOGIC DIAGRAM



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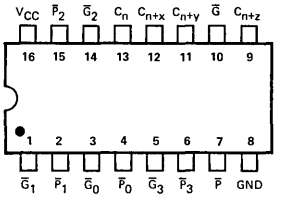
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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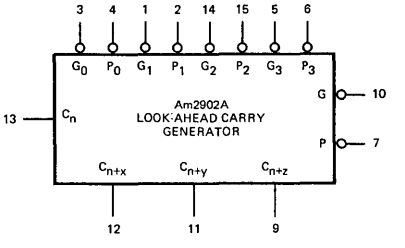
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

MPR-025

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2902AXC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am2902AXM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.50V MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1mA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IH} or V_{IL}				0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.2	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	C_n			−2	mA
			$\overline{P}_3$			−4	
			$\overline{P}_2$			−6	
			$\overline{P}_0, \overline{P}_1, \overline{G}_3$			−8	
			$\overline{G}_0, \overline{G}_2$			−14	
			$\overline{G}_1$			−16	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	C_n			50	µA
			$\overline{P}_3$			100	
			$\overline{P}_2$			150	
			$\overline{P}_0, \overline{P}_1, \overline{G}_3$			200	
			$\overline{G}_0, \overline{G}_2$			350	
			$\overline{G}_1$			400	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit (Note 3)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. All Outputs LOW	MIL		69	99	mA
			COM'L		69	109	
		V_{CC} = MAX. All Ouputs HIGH	MIL		35		mA
			COM'L		35		

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	$\overline{G}_i/\overline{P}_i \rightarrow C_{n+j}$		4.5	7	ns	C_L = 15pF, R_L = 280Ω
t_{PHL}			4.5	7		
t_{PLH}	$\overline{G}_i/\overline{P}_i \rightarrow \overline{G}$		5	7.5	ns	
t_{PHL}			7	10.5		
t_{PLH}	$\overline{P}_i \rightarrow \overline{P}$		4.5	6.5	ns	
t_{PHL}			6.5	10		
t_{PLH}	$C_n \rightarrow C_{n+j}$		6.5	10	ns	
t_{PHL}			7	10.5		

DEFINITION OF FUNCTIONAL TERMS

C_n Carry-in. The carry-in input to the look-ahead generator. Also the carry-in input to the nth Am2901A microprocessor ALU input.

C_{n+j} Carry-out. (j = x, y, z). The carry-out output to be used at the carry-in inputs of the n+1, n+2 and n+3 microprocessor ALU slices.

G_i, P_i Generate and propagate inputs respectively (i = 0, 1, 2, 3). The carry generate and carry propagate inputs from the n, n+1, n+2 and n+3 microprocessor ALU slices.

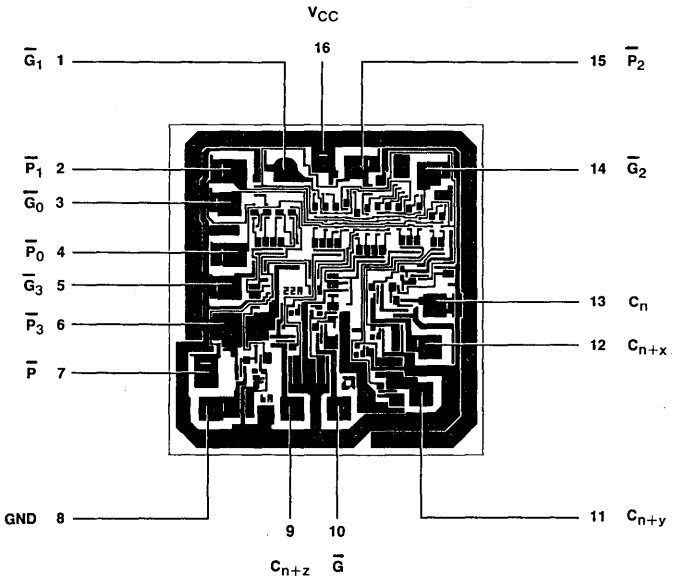
G, P Generate and propagate outputs respectively. The carry generate and carry propagate outputs that can be used with the next higher level of carry look-ahead if used.

TRUTH TABLE

Inputs									Outputs				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	X	X					L		
X	H	H	H	X	X	X					L		
L	H	X	H	X	X	X					L		
X	X	X	L	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	L	X	X	L					H		
H	X	L	L	X	X	L					H		
X	X		X	X	X	X	H	H				H	
X	X		X	X	H	H	H	X				H	
X	H		H	X	H	X	H	X				H	
H	X		H	X	H	X	H	X				H	
X	X		X	X	X	X	L	X				L	
X	X		X	X	L	X	X	L				L	
X	X		L	X	X	L	X	L				L	
X	L		X	L	X	L	X	L				L	
	H	X		X		X		X					H
	X	H		X		X		X					H
	X	X		X		H		X					H
	X	X		X		X		H					H
	X	L		X		L		L					L

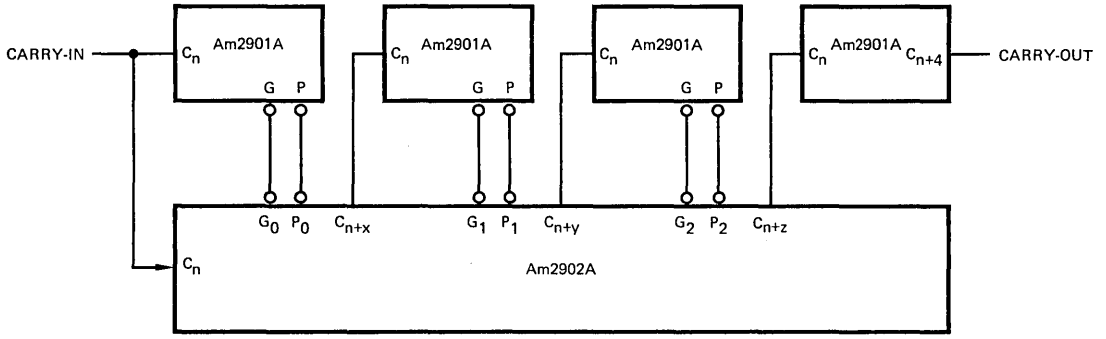
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

Metallization and Pad Layout



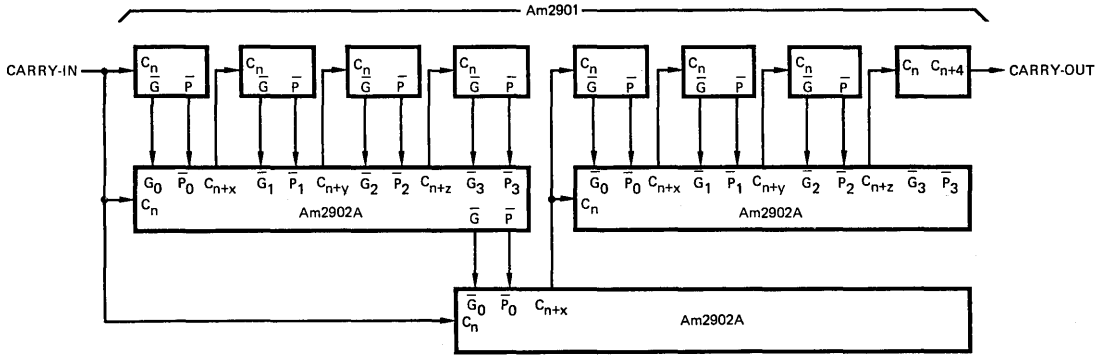
DIE SIZE 0.062" X 0.067"

APPLICATIONS



16-BIT CARRY LOOK-AHEAD CONNECTION.

MPR-028



32-BIT ALU, THREE LEVEL CARRY LOOK-AHEAD.

MPR-029

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2902APC	P-16	C	C-1
AM2902ADC	D-16	C	C-1
AM2902ADC-B	D-16	C	B-1
AM2902ADM	D-16	M	C-3
AM2902ADM-B	D-16	M	B-3
AM2902AFM	F-16	M	C-3
AM2902AFM-B	F-16	M	B-3
Am2902AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
Am2902AXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am2903
The Superslice™

DISTINCTIVE CHARACTERISTICS

- Expandable Register File–
  Like the Am2901A, the Am2903 contains 16 internal working registers arranged in a two-address architecture. But the Am2903 includes the necessary "hooks" to expand the register file externally to any number of registers.
- Built-in Multiplication Logic–
  Performing multiplication with the Am2901A requires a few external gates--these gates are contained on-chip in the Am2903. Three special instructions are used for unsigned multiplication, two's complement multiplication, and the last cycle of a two's complement multiplication.
- Built-in Division Logic–
  The Am2903 contains all logic and interconnects for execution of a non-restoring, multiple-length division with correction of the quotient.
- Built-in Normalization Logic–
  The Am2903 can simultaneously shift the Q Register and count in a working register. Thus, the mantissa and exponent of a floating point number can be developed using a single microcycle per shift. Status flags indicate when the operaton is complete.
- Built-in Parity Generation Circuitry–
  The Am2903 can supply parity across the entire ALU output for use in error detection and CRC code generation.
- Built-in Sign Extension Circuitry–
  To facilitate operation on different length two's complement numbers, the Am2903 provides the capability to extend the sign at any slice boundary.

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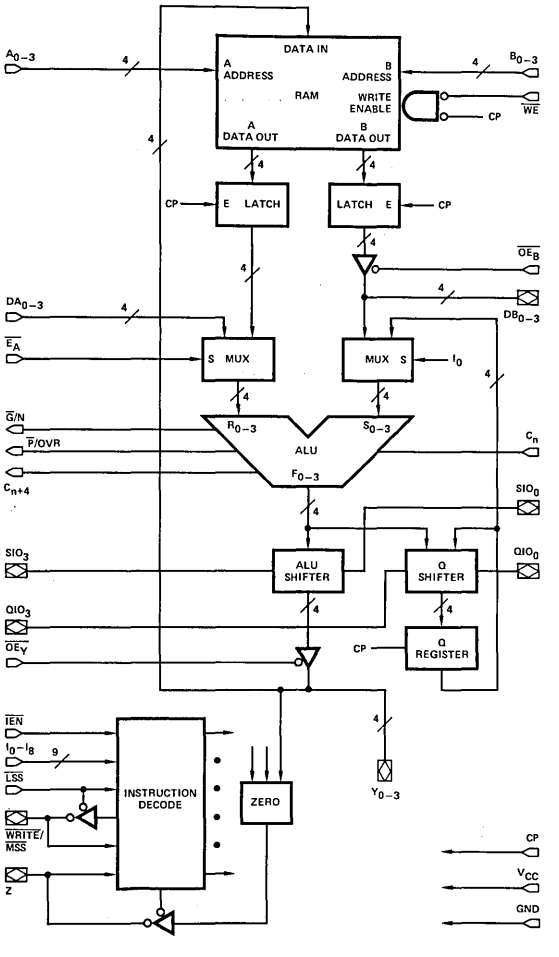
  Memory Expansion 2-50

GENERAL DESCRIPTION

The Am2903 is a four-bit expandable bipolar microprocessor slice. The Am2903 performs all functions performed by the industry standard Am2901A and, in addition, provides a number of significant enhancements that are especially useful in arithmetic-oriented processors. Infinitely expandable memory and three-port, three-address architecture are provided by the Am2903. In addition to its complete arithmetic and logic instruction set, the Am2903 provides a special set of instructions which facilitate the implementation of multiplication, division, normalization, and other previously time-consuming operations. The Am2903 is supplied in a 48 pin dual in-line package.

BLOCK DIAGRAM



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ARCHITECTURE OF THE Am2903

The Am2903 is a high-performance, cascadable, four-bit bipolar microprocessor slice designed for use in CPU's, peripheral controllers, microprogrammable machines, and numerous other applications. The microinstruction flexibility of the Am2903 allows the efficient emulation of almost any digital computing machine. The nine-bit microinstruction selects the ALU sources, function, and destination. The Am2903 is cascadable with full lookahead or ripple carry, has three-state outputs, and provides various ALU status flag outputs. Advanced Low-Power Schottky processing is used to fabricate this 48-pin LSI circuit.

All data paths within the device are four bits wide. As shown in the block diagram, the device consists of a 16-word by 4-bit, two-port RAM with latches on both output ports, a high-performance ALU and shifter, a multi-purpose Q Register with shifter input, and a nine-bit instruction decoder.

Two-Port RAM

Any two RAM words addressed at the A and B address ports can be read simultaneously at the respective RAM A and B output ports. Identical data appear at the two output ports when the same address is applied to both address ports. The latches at the RAM output ports are transparent when the clock input, CP, is HIGH and they hold the RAM output data when CP is LOW. Under control of the $\overline{OE}_B$ three-state output enable, RAM data can be read directly at the Am2903 DB I/O port.

External data at the Am2903 Y I/O port can be written directly into the RAM, or ALU shifter output data can be enabled onto the Y I/O port and entered into the RAM. Data is written into the RAM at the B address when the write enable input, $\overline{WE}$, is LOW and the clock input, CP, is LOW.

Arithmetic Logic Unit

The Am2903 high-performance ALU can perform seven arithmetic and nine logic operations on two 4-bit operands. Multiplexers at the ALU inputs provide the capability to select various pairs of ALU source operands. The $\overline{E}_A$ input selects either the DA external data input or RAM output port A for use as one ALU operand and the $\overline{OE}_B$ and I_0 inputs select RAM output port B, DB external data input, or the Q Register content for use as the second ALU operand. Also, during some ALU operations, zeroes are forced at the ALU operand inputs. Thus, the Am2903 ALU can operate on data from two external sources, from an internal and external source, or from two internal sources. Table I shows all possible pairs of ALU source operands as a function of the $\overline{E}_A$, $\overline{OE}_B$, and I_0 inputs.

When instruction bits I_4, I_3, I_2, I_1, and I_0 are LOW, the Am2903 executes special functions. Table 4 defines these special functions and the operation which the ALU performs for each. When the Am2903 executes instructions other than the nine special functions, the ALU operation is determined by instruction bits I_4, I_3, I_2, and I_1. Table 2 defines the ALU operation as a function of these four instruction bits.

Am2903's may be cascaded in either a ripple carry or lookahead carry fashion. When a number of Am2903's are cascaded, each slice must be programmed to be a most significant slice (MSS), intermediate slice (IS), or least significant slice (LSS) of the array. The carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, signals required for a lookahead carry scheme are generated by the Am2903 and are available as outputs of the least significant and intermediate slices.

The Am2903 also generates a carry-out signal, C_{n+4}, which is generally available as an output of each slice. Both the carry-in, C_n, and carry-out, C_{n+4}, signals are active HIGH. The ALU

TABLE 1. ALU OPERAND SOURCES

$\overline{E}_A$	I_0	$\overline{OE}_B$	ALU Operand R	ALU Operand S
L	L	L	RAM Output A	RAM Output B
L	L	H	RAM Output A	DB_{0-3}
L	H	X	RAM Output A	Q Register
H	L	L	DA_{0-3}	RAM Output B
H	L	H	DA_{0-3}	DB_{0-3}
H	H	X	DA_{0-3}	Q Register

L = LOW H = HIGH X = Don't Care

TABLE 2. ALU FUNCTIONS

I_4	I_3	I_2	I_1	Hex Code	ALU Functions	
L	L	L	L	0	I_0 = L	Special Functions
					I_0 = H	F_i = HIGH
L	L	L	H	1	F = S Minus R Minus 1 Plus C_n	
L	L	H	L	2	F = R Minus S Minus 1 Plus C_n	
L	L	H	H	3	F = R Plus S Plus C_n	
L	H	L	L	4	F = S Plus C_n	
L	H	L	H	5	F = $\overline{S}$ Plus C_n	
L	H	H	L	6	F = R Plus C_n	
L	H	H	H	7	F = $\overline{R}$ Plus C_n	
H	L	L	L	8	F_i = LOW	
H	L	L	H	9	$F_i = \overline{R}_i$ AND S_i	
H	L	H	L	A	$F_i = R_i$ EXCLUSIVE NOR S_i	
H	L	H	H	B	$F_i = R_i$ EXCLUSIVE OR S_i	
H	H	L	L	C	$F_i = R_i$ AND S_i	
H	H	L	H	D	$F_i = R_i$ NOR S_i	
H	H	H	L	E	$F_i = R_i$ NAND S_i	
H	H	H	H	F	$F_i = R_i$ OR S_i	

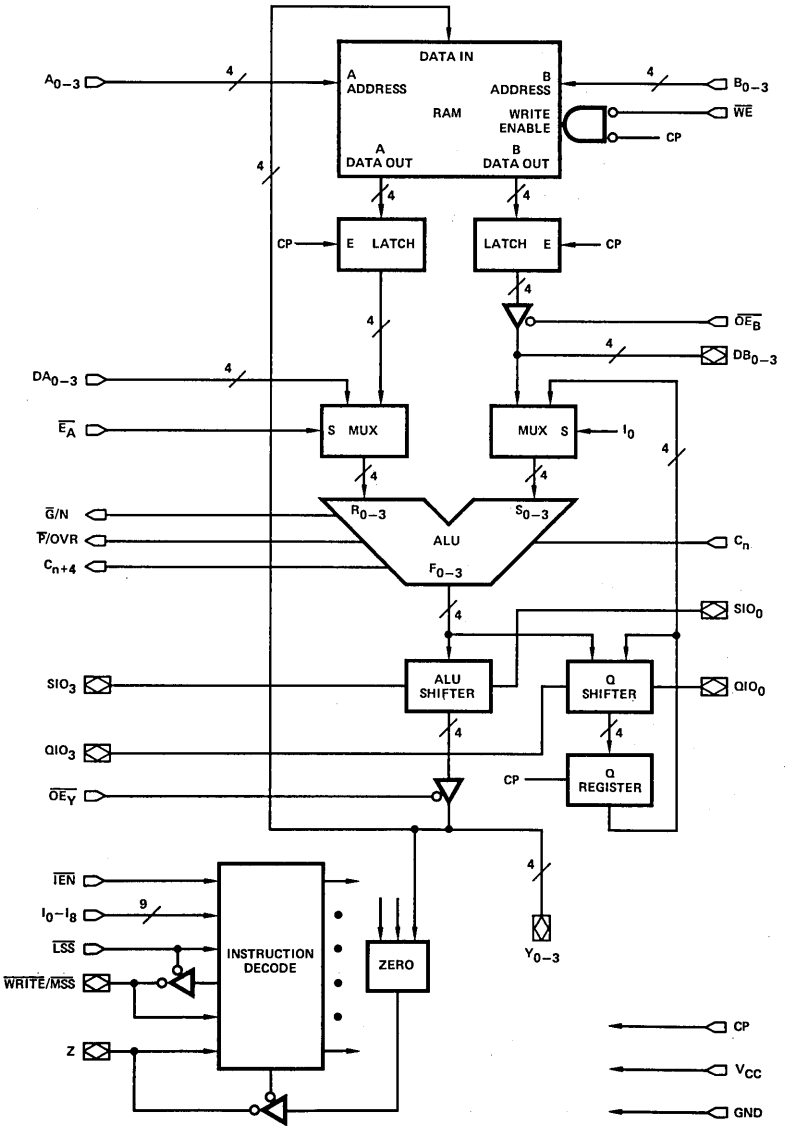
L = LOW H = HIGH i = 0 to 3

generates two other status outputs. These are negative, N, and overflow, OVR. The N output is generally the most significant (sign) bit of the ALU output and can be used to determine positive or negative results. The OVR output indicates that the arithmetic operation being performed exceeds the available two's complement number range. The N and OVR signals are available as outputs of the most significant slice. Thus, the multi-purpose $\overline{G}$/N and $\overline{P}$/OVR outputs indicate $\overline{G}$ and $\overline{P}$ at the least significant and intermediate slices, and sign and overflow at the most significant slice. To some extent, the meaning of the C_{n+4}, $\overline{P}$/OVR, and $\overline{G}$/N signals vary with the ALU function being performed. Refer to Table 5 for an exact definition of these four signals as a function of the Am2903 instruction.

ALU Shifter

Under instruction control, the ALU shifter passes the ALU output (F) non-shifted, shifts it up one bit position (2F), or shifts it down one bit position (F/2). Both arithmetic and logical shift operations are possible. An arithmetic shift operation shifts data around the most significant (sign) bit position of the most significant slice, and a logical shift operation shifts data through this bit position (see Figure A). SIO_0 and SIO_3 are bidirectional serial shift inputs/outputs. During a shift-up operation, SIO_0 is generally a serial shift input and SIO_3 a serial shift output. During a shift-down operation, SIO_3 is generally a serial shift input and SIO_0 a serial shift output.

BLOCK DIAGRAM



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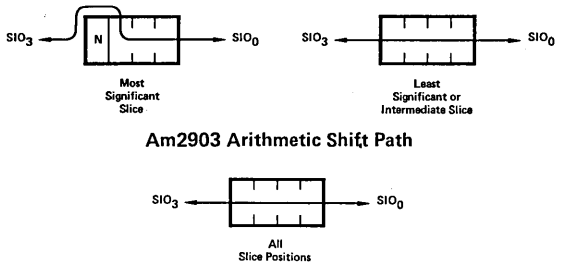


Figure A. MPR-031

To some extent, the meaning of the SIO_0 and SIO_3 signals is instruction dependent. Refer to Tables 3 and 4 for an exact definition of these pins.

The ALU shifter also provides the capability to sign extend at slice boundaries. Under instruction control, the SIO_0 (sign) input can be extended through Y_0, Y_1, Y_2, Y_3 and propagated to the SIO_3 output.

A cascadable, five-bit parity generator/checker is designed into the Am2903 ALU shifter and provides ALU error detection capability. Parity for the F_0, F_1, F_2, F_3 ALU outputs and SIO_3 input is generated and, under instruction control, is made available at the SIO_0 output. Refer to the Am2903 applications section for a more detailed description of the Am2903 sign extension and parity generation/checking capability.

The instruction inputs determine the ALU shifter operation. Table 4 defines the special functions and the operation the ALU shifter performs for each. When the Am2903 executes instructions other than the nine special functions, the ALU shifter operation is determined by instruction bits $I_8I_7I_6I_5$. Table 3 defines the ALU shifter operation as a function of these four bits.

Q Register

The Q Register is an auxiliary four-bit register which is clocked on the LOW-to-HIGH transition of the CP input. It is intended primarily for use in multiplication and division operations; however, it can also be used as an accumulator or holding register for some applications. The ALU output, F, can be loaded into the Q Register, and/or the Q Register can be selected as the source for the ALU S operand. The shifter at the input to the Q Register provides the capability to shift the Q Register contents up one bit position (2Q) or down one bit position (Q/2). Only logical shifts are performed. QIO_0 and QIO_3 are bidirectional shift serial inputs/outputs. During a Q Register shift-up operation, QIO_0 is a serial shift input and QIO_3 is a serial shift output. During a shift-down operation, QIO_3 is a serial shift input and QIO_0 is a serial shift output.

Double-length arithmetic and logical shifting capability is provided by the Am2903. The double-length shift is performed by connecting QIO_3 of the most significant slice to SIO_0 of the least significant slice, and executing an instruction which shifts both the ALU output and the Q Register.

The Q Register and shifter are controlled by the instruction inputs. Table 4 defines the Am2903 special functions and the operations which the Q Register and shifter perform for each. When the Am2903 executes instructions other than the nine special functions, the Q Register and shifter operation is controlled by instruction bits $I_8I_7I_6I_5$. Table 3 defines the Q Register and shifter operation as a function of these four bits.

Output Buffers

The DB and Y ports are bidirectional I/O ports driven by three-state output buffers with external output enable controls. The Y output buffers are enabled when the $\overline{OE}_Y$ input is LOW and are in the high-impedance state when $\overline{OE}_Y$ is HIGH. Likewise, the DB output buffers are enabled when the $\overline{OE}_B$ input is LOW and in the high-impedance state when $\overline{OE}_B$ is HIGH.

The zero, Z, pin is an open collector input/output that can be wire-OR'ed between slices. As an output it can be used as a zero detect status flag and generally indicates that the $Y_{0\text{-}3}$ pins are all LOW, whether they are driven from the Y output buffers or from an external source connected to the $Y_{0\text{-}3}$ pins. To some extent the meaning of this signal varies with the instruction being performed. Refer to Table 5 for an exact definition of this signal as a function of the Am2903 instruction.

TABLE 3. ALU DESTINATION CONTROL FOR I_0 OR I_1 OR I_2 OR I_3 OR I_4 = HIGH, $\overline{IEN}$ = LOW.

						SIO_3		Y_3		Y_2								
I_8	I_7	I_6	I_5	Hex Code	ALU Shifter Function	Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices	Most Sig. Slice	Other Slices	Y_1	Y_0	SIO_0	$\overline{Write}$	Q Reg & Shifter Function	QIO_3	QIO_0
L	L	L	L	0	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	L	H	1	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Hold	Hi-Z	Hi-Z
L	L	H	L	2	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Log. Q/2→Q	Input	Q_0
L	L	H	H	3	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Log. Q/2→Q	Input	Q_0
L	H	L	L	4	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	Hold	Hi-Z	Hi-Z
L	H	L	H	5	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	Log. Q/2→Q	Input	Q_0
L	H	H	L	6	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	F→Q	Hi-Z	Hi-Z
L	H	H	H	7	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	F→Q	Hi-Z	Hi-Z
H	L	L	L	8	Arith. 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	L	H	9	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	L	H	L	A	Arith. 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q→Q	Q_3	Input
H	L	H	H	B	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q→Q	Q_3	Input
H	H	L	L	C	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Hold	Hi-Z	Hi-Z
H	H	L	H	D	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	H	Log. 2Q→Q	Q_3	Input
H	H	H	L	E	SIO_0→Y_0, Y_1, Y_2, Y_3	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	Input	L	Hold	Hi-Z	Hi-Z
H	H	H	H	F	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Hi-Z	L	Hold	Hi-Z	Hi-Z

Parity = $F_3 \forall F_2 \forall F_1 \forall F_0 \forall SIO_3$
$\forall$ = Exclusive OR

L = LOW
H = HIGH

Hi-Z = High Impedance

TABLE 4. SPECIAL FUNCTIONS: $I_0 = I_1 = I_2 = I_3 = I_4$ = LOW, $\overline{IEN}$ = LOW

I_8	I_7	I_6	I_5	Hex Code	Special Function	ALU Function	ALU Shifter Function	SIO_3 Most Sig. Slice	SIO_3 Other Slices	SIO_0	Q Reg & Shifter Function	QIO_3	QIO_0	$\overline{WRITE}$
L	L	L	L	0	Unsigned Multiply	F= S+C_n if Z=L F=R+S+C_n if Z=H	Log. F/2→Y (Note 1)	Hi-Z	Input	F_0	Log. Q/2→Q	Input	Q_0	L
L	L	H	L	2	Two's Complement Multiply	F=S+C_n if Z=L F=R+S+C_n if Z=H	Log. F/2→Y (Note 2)	Hi-Z	Input	F_0	Log. Q/2→Q	Input	Q_0	L
L	H	L	L	4	Increment by One or Two	F=S+1+C_n	F→Y	Input	Input	Parity	Hold	Hi-Z	Hi-Z	L
L	H	L	H	5	Sign/Magnitude-Two's Complement	F=S+C_n if Z=L F=$\overline{S}$+C_n if Z=H	F→Y (Note 3)	Input	Input	Parity	Hold	Hi-Z	Hi-Z	L
L	H	H	L	6	Two's Complement Multiply, Last Cycle	F=S+C_n if Z=L F=S−R−1+C_n if Z=H	Log. F/2→Y (Note 2)	Hi-Z	Input	F_0	Log. Q/2→Q	Input	Q_0	L
H	L	L	L	8	Single Length Normalize	F=S+C_n	F→Y	F_3	F_3	Hi-Z	Log. 2Q→Q	Q_3	Input	L
H	L	H	L	A	Double Length Normalize and First Divide Op.	F=S+C_n	Log 2F→Y	$R_3 \forall F_3$	F_3	Input	Log. 2Q→Q	Q_3	Input	L
H	H	L	L	C	Two's Complement Divide	F=S+R+C_n if Z=L F=S−R−1+C_n if Z=H	Log. 2F→Y	$\overline{R_3 \forall F_3}$	F_3	Input	Log. 2Q→Q	Q_3	Input	L
H	H	H	L	E	Two's Complement Divide, Correction and Remainder	F=S+R+C_n if Z=L F=S−R−1+C_n if Z=H	F→Y	F_3	F_3	Hi-Z	Log. 2Q→Q	Q_3	Input	L

NOTES: 1. At the most significant slice only, the C_{n+4} signal is internally gated to the Y_3 output.
2. At the most significant slice only, $F_3 \forall$ OVR is internally gated to the Y_3 output.
3. At the most significant slice only, $S_3 \forall F_3$ is generated at the Y_3 output.
4. Op codes 1, 3, 7, 9, B, D, and F are reserved for future use.

L = LOW
H = HIGH
X = Don't Care

Hi-Z = High Impedance
$\forall$ = Exclusive OR
Parity = $SIO_3 \forall F_3 \forall F_2 \forall F_1 \forall F_0$

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the nine Instruction inputs, I_{0-8}; the Instruction Enable input, $\overline{IEN}$; the $\overline{LSS}$ input; and the $\overline{WRITE}$/$\overline{MSS}$ input/output.

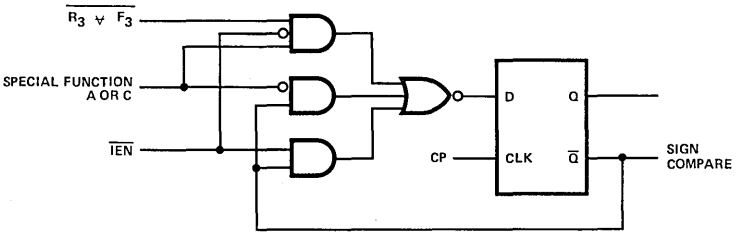
The $\overline{WRITE}$ output is LOW when an instruction which writes data into the RAM is being executed. Refer to Tables 3 and 4 for a definition of the $\overline{WRITE}$ output as a function of the Am2903 instruction inputs.

When $\overline{IEN}$ is HIGH, the $\overline{WRITE}$ output is forced HIGH and the Q Register and Sign Compare Flip-Flop contents are preserved.

When $\overline{IEN}$ is LOW, the $\overline{WRITE}$ output is enabled and the Q Register and Sign Compare Flip-Flop can be written according to the Am2903 instruction. The Sign Compare Flip-Flop is an on-chip flip-flop which is used during an Am2903 divide operation (see Figure B).

Programming the Am2903 Slice Position

Tying the $\overline{LSS}$ input LOW programs the slice to operate as a least significant slice (LSS) and enables the $\overline{WRITE}$ output signal onto the $\overline{WRITE}$/$\overline{MSS}$ bidirectional I/O pin. When $\overline{LSS}$ is tied HIGH, the $\overline{WRITE}$/$\overline{MSS}$ pin becomes an input pin; tying the $\overline{WRITE}$/$\overline{MSS}$ pin HIGH programs the slice to operate as an intermediate slice (IS) and tying it LOW programs the slice to operate as a most significant slice (MSS).



The sign compare signal appears at the Z output of the most significant slice during special functions C, D and E, F. Refer to Table 5.

Figure B. Sign Compare Flip-Flop.

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TABLE 5. Am2903 STATUS OUTPUTS

(Hex) $I_8I_7I_6I_5$	(Hex) $I_4I_3I_2I_1$	I_0	GI (I=0 to 3)	PI (I=0 to 3)	C_{n+4}	$\overline{P}$/OVR Most Sig. Slice	$\overline{P}$/OVR Other Slices	$\overline{G}$/N Most Sig. Slice	$\overline{G}$/N Other Slices	Z Most Sig. Slice	Z Intermediate Slice	Z Least Sig. Slice
X	0	H	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	1	X	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	2	X	$R_i \wedge \overline{S}_i$	$R_i \vee \overline{S}_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	3	X	$R_i \wedge S_i$	$R_i \vee S_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	4	X	0	S_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	5	X	0	$\overline{S}_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	6	X	0	R_i	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	7	X	0	$\overline{R}_i$	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	8	X	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	9	X	$\overline{R}_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	A	X	$R_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	B	X	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	C	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	D	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	E	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	F	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
0	0	L	0 if Z=L $R_i \wedge S_i$ if Z=H	S_i if Z=L $R_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
2	0	L	0 if Z=L $R_i \wedge S_i$ if Z=H	S_i if Z=L $R_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
4	0	L	See Note 1	See Note 2	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
5	0	L	0	S_i if Z=L $\overline{S}_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3 if Z=L $F_3 \forall S_3$ if Z=H	$\overline{G}$	S_3	Input	Input
6	0	L	0 if Z=L $\overline{R}_i \wedge S_i$ if Z=H	S_i if Z=L $\overline{R}_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
8	0	L	0	S_i	See Note 3	$Q_2 \forall Q_1$	$\overline{P}$	Q_3	$\overline{G}$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
A	0	L	0	S_i	See Note 4	$F_2 \forall F_1$	$\overline{P}$	F_3	$\overline{G}$	See Note 5	See Note 5	See Note 5
C	0	L	$R_i \wedge S_i$ if Z=L $\overline{R}_i \wedge S_i$ if Z=H	$R_i \vee S_i$ if Z=L $\overline{R}_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
E	0	L	$R_i \wedge S_i$ if Z=L $\overline{R}_i \wedge S_i$ if Z=H	$R_i \vee S_i$ if Z=L $\overline{R}_i \vee S_i$ if Z=H	$G \vee PC_n$	$C_{n+3} \forall C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input

L = LOW = 0
H = HIGH = 1
$\vee$ = OR
$\wedge$ = AND
$\forall$ = EXCLUSIVE OR
$P = P_3P_2P_1P_0$
$G = G_3 \vee G_2P_3 \vee G_1P_2P_3 \vee G_0P_1P_2P_3$
$C_{n+3} = G_2 \vee G_1P_2 \vee G_0P_1P_2 \vee C_nP_pP_1P_2$

NOTES:
1. If $\overline{LSS}$ is LOW, $G_0 = S_0$ and $G_{1,2,3} = 0$
   If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = 0$
2. If $\overline{LSS}$ is LOW, $P_0 = 1$ and $P_{1,2,3} = S_{1,2,3}$
   If $\overline{LSS}$ is HIGH, $P_i = S_i$
3. At the most significant slice, $C_{n+4} = Q_3 \forall Q_2$
   At other slices, $C_{n+4} = G \vee PC_n$
4. At the most significant slice, $C_{n+4} = F_3 \forall F_2$
   At other slices, $C_{n+4} = G \vee PC_n$
5. $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3\overline{F}_0\overline{F}_1\overline{F}_2\overline{F}_3$

Am2903 SPECIAL FUNCTIONS

The Am2903 provides nine Special Functions which facilitate the implementation of the following operations:

- Single- and Double-Length Normalization
- Two's Complement Division
- Unsigned and Two's Complement Multiplication
- Conversion Between Two's Complement and Sign/Magnitude Representation
- Incrementation by One or Two

Table 4 defines these Special Functions.

The Single-Length and Double-Length Normalization functions can be used to adjust a single-precision or double-precision floating point number in order to bring its mantissa within a specified range.

Three Special Functions which can be used to perform a two's complement, non-restoring divide operation are provided by the Am2903. These functions provide both single- and double-precision divide operations and can be performed in "n" clock cycles, where "n" is the number of bits in the quotient.

The Unsigned Multiply Special Function and the two Two's Complement Multiply Special Functions can be used to multiply two n-bit, unsigned or two's complement numbers, respectively, in n clock cycles. These functions utilize the conditional add and shift algorithm. During the last cycle of the two's complement multiplication, a conditional subtraction, rather than addition, is performed because the sign bit of the multiplier carries negative weight.

The Sign/Magnitude-Two's Complement Special Function can be used to convert number representation systems. A number expressed in Sign/Magnitude representation can be converted to the Two's Complement representation, and vice-versa, in one clock cycle.

The Increment by One or Two Special Function can be used to increment an unsigned or two's complement number by one or two. This is useful in 16-bit word, byte-addressable machines, where the word addresses are multiples of two.

Refer to Am2903 applications section for a more detailed description of these Special Functions.

PIN DEFINITIONS

A_{0-3} Four RAM address inputs which contain the address of the RAM word appearing at the RAM A output port.

B_{0-3} Four RAM address inputs which contain the address of the RAM word appearing at the RAM B output port and into which new data is written when the $\overline{WE}$ input and the CP input are LOW.

$\overline{WE}$ The RAM write enable input. If $\overline{WE}$ is LOW, data at the Y I/O port is written into the RAM when the CP input is LOW. When $\overline{WE}$ is HIGH, writing data into the RAM is inhibited.

DA_{0-3} A four-bit external data input which can be selected as one of the Am2903 ALU operand sources; DA_0 is the least significant bit.

$\overline{EA}$ A control input which, when HIGH, selects DA_{0-3} and, when LOW, selects RAM output A as the ALU R operand.

DB_{0-3} A four-bit external data input/output. Under control of the $\overline{OE_B}$ input, RAM output port B can be directly read on these lines, or input data on these lines can be selected as the ALU S operand.

$\overline{OE_B}$ A control input which, when LOW, enables RAM output B onto the DB_{0-3} lines and, when HIGH, disables the RAM output B tri-state buffers.

C_n The carry-in input to the Am2903 ALU.

I_{0-8} The nine instruction inputs used to select the Am2903 operation to be performed.

$\overline{IEN}$ The instruction enable input which, when LOW, enables the $\overline{WRITE}$ output and allows the Q Register and the Sign Compare flip-flop to be written. When $\overline{IEN}$ is HIGH, the $\overline{WRITE}$ output is forced HIGH and the Q Register and Sign Compare flip-flop are in the hold mode.

C_{n+4} This output generally indicates the carry-out of the Am2903 ALU. Refer to Table 5 for an exact definition of this pin.

$\overline{G}$/N A multi-purpose pin which indicates the carry generate, $\overline{G}$, function at the least significant and intermediate slices, and generally indicates the sign, N, of the ALU result at the most significant slice. Refer to Table 5 for an exact definition of this pin.

$\overline{P}$/OVR A multi-purpose pin which indicates the carry propagate, $\overline{P}$, function at the least significant and intermediate slices, and indicates the conventional two's complement overflow, OVR, signal at the most significant slice. Refer to Table 5 for an exact definition of this pin.

Z An open-collector input/output pin which, when HIGH, generally indicates the Y_{0-3} outputs are all LOW. For some Special Functions, Z is used as an input pin. Refer to Table 5 for an exact definition of this pin.

SIO_0, SIO_3 Bidirectional serial shift inputs/outputs for the ALU shifter. During a shift-up operation, SIO_0 is an input and SIO_3 an output. During a shift-down operation, SIO_3 is an input and SIO_0 is an output. Refer to Tables 3 and 4 for an exact definition of these pins.

QIO_0, QIO_3 Bidirectional serial shift inputs/outputs for the Q shifter which operate like SIO_0 and SIO_3. Refer to Tables 3 and 4 for an exact definition of these pins.

$\overline{LSS}$ An input pin which, when tied LOW, programs the chip to act as the least significant slice (LSS) of an Am2903 array and enables the $\overline{WRITE}$ output onto the $\overline{WRITE}/\overline{MSS}$ pin. When $\overline{LSS}$ is tied HIGH, the chip is programmed to operate as either an intermediate or most significant slice and the $\overline{WRITE}$ output buffer is disabled.

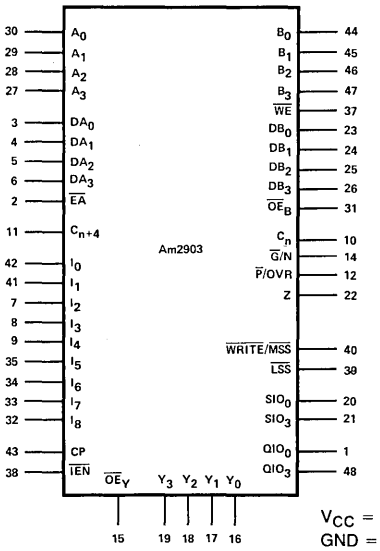
$\overline{WRITE}$/ $\overline{MSS}$ When $\overline{LSS}$ is tied LOW, the $\overline{WRITE}$ output signal appears at this pin; the $\overline{WRITE}$ signal is LOW when an instruction which writes data into the RAM is being executed. When $\overline{LSS}$ is tied HIGH, $\overline{WRITE}/\overline{MSS}$ is an input pin; tying it HIGH programs the chip to operate as an intermediate slice (IS) and tying it LOW programs the chip to operate as the most significant slice (MSS).

Y_{0-3} Four data inputs/outputs of the Am2903. Under control of the $\overline{OE_Y}$ input, the ALU shifter output data can be enabled onto these lines, or these lines can be used as data inputs when external data is written directly into the RAM.

$\overline{OE_Y}$ A control input which, when LOW, enables the ALU shifter output data onto the Y_{0-3} lines and, when HIGH, disables the Y_{0-3} three-state output buffers.

CP The clock input to the Am2903. The Q Register and Sign Compare flip-flop are clocked on the LOW-to-HIGH transition of the CP signal. When enabled by $\overline{WE}$, data is written in the RAM when CP is LOW.

LOGIC SYMBOL



V_{CC} = Pin 36
GND = Pin 13

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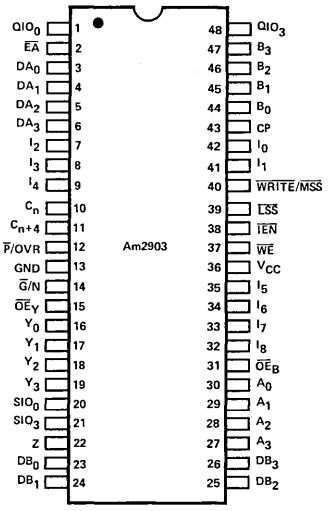
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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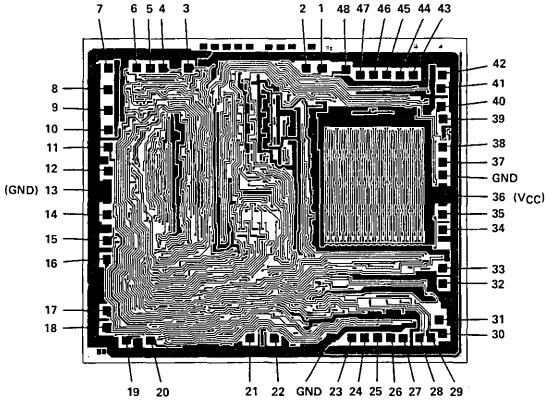
Metallization and Pad Layout



DIE SIZE 0.163" X 0.197"

Note: Pin numbers correspond to DIP package.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2903DC	D-48	C	C-1
AM2903DC-B	D-48	C	B-1
AM2903DM	D-48	M	C-3
AM2903DM-B	D-48	M	B-3
AM2903FM	F-48	M	C-3
AM2903FM-B	F-48	M	B-3

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am2903
OPERATING RANGE

P/N	Range	Temperature	V_{CC}	
Am2903PC, DC	COM'L	T_A = 0°C to +70°C	V_{CC}= 5.0V ±5%	(MIN. = 4.75V, MAX. = 5.25V)
Am2903DM, FM	MIL	T_C = −55°C to +125°C	V_{CC} = 5.0V ±10%	(MIN. = 4.50V, MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6mA Y_0-Y_3, $\overline{G}$/N		2.4			Volts
			I_{OH} = −800µA DB_{0-3}, $\overline{P}$/OVR SIO_0, SIO_3, QIO_0, QIO_3, $\overline{WRITE}$, C_{n+4}		2.4			
I_{CEX}	Output Leakage Current for Z Output (Note 4)	V_{CC} = MIN., V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}					250	µA
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} = or V_{IL}	Y_0, Y_1, Y_2 Y_3, Z	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)				
			DB_0, DB_1, DB_2, DB_3	I_{OL} = 12mA (COM'L)			0.5	
				I_{OL} = 8.0mA (MIL)				
			$\overline{G}$/N	I_{OL} = 18mA			0.5	
			$\overline{P}$/OVR	I_{OL} = 10mA			0.5	
			C_{n+4}, SIO_0 SIO_3, QIO_0 QIO_3, $\overline{WRITE}$	I_{OL} = 8.0mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 6)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 6)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V (Note 4)	C_n				−3.6	mA
			Y_0, Y_1, Y_2, Y_3				−1.08	
			I_0, I_1, I_2, I_3, I_4, DA_0, DA_1, DA_2, DA_3, SIO_0 SIO_3, QIO_0, QIO_3, $\overline{MSS}$, DB_0, DB_1, DB_2, DB_3				−0.72	
			All other inputs				−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V (Note 4)	C_n				120	µA
			Y_0, Y_1, Y_2, Y_3				110	
			I_0-I_4, DA_0-DA_3				40	
			SIO_0, SIO_3, QIO_0, QIO_3, DB_{0-3}, $\overline{MSS}$				90	
			All other inputs				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (HIGH Impedance) Output Current	V_{CC} = MAX., (Note 4)	Y_0-Y_3	V_O = 2.4V			110	µA
				V_O = 0.5V			−1130	
			DB_{0-3}, QIO_0, QIO_0, SIO_0, SIO_3, $\overline{MSS}$/IS	V_O = 2.4V			90	
				V_O = 0.5V			−770	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX + 0.5V V_O = 0.5V			−30		−85	mA
I_{CC}	Power Supply Current (Note 5)	V_{CC} = MAX.	T_A = 25°C			220	335	mA
			COM'L	T_A = 0 to 70°C			350	
				T_A = 70°C			291	
			MIL	T_C = −55 to 125°C			395	
				T_C = 125°C			258	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Y_{0-3}, DB_{0-3}, $SIO_{0,3}$, $QIO_{0,3}$ and WRITE/MSS are three state outputs internally connected to TTL inputs. Z is an open-collector output internally connected to a TTL input. Input characteristics are measured under conditions such that the outputs are in the OFF state.
5. Worst case I_{CC} is at minimum temperature.
6. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

USING THE Am2903

Am2903 APPLICATIONS

The Am2903 is designed to be used in microprogrammed systems. Figure 1 illustrates a recommended architecture. The control and data inputs to the Am2903 normally will all come from registers clocked at the same time as the Am2903. The register inputs come from a ROM or PROM – the "microprogram store". This memory contains sequences of microinstructions which apply the proper control signals to the Am2903's and other circuits to execute the desired operation.

The address lines of the microprogram store are driven from the Am2910 Microprogram Sequencer. This device has facilities for storing an address, incrementing an address, jumping to any address, and linking subroutines. The Am2910 is controlled by some of the bits coming from the microprogram store. Essentially, these bits are the "next instruction" control.

One Level Pipeline Based System

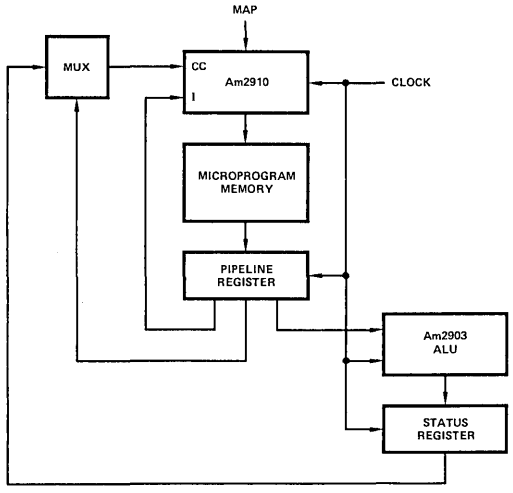


Figure 1. Typical Microprogram Architecture.

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Note that with the microprogram register in between the microprogram memory store and the Am2903's, a microinstruction accessed on one cycle is executed on the next cycle. As one microinstruction is executed, the next microinstruction is being read from microprogram memory. In this configuration, system speed is improved because the execution time in the Am2903's occurs in parallel with the access time of the microprogram store. Without the "pipeline register", these two functions must occur serially.

Expansion of the Am2903

The Am2903 is a four-bit CPU slice. Any number of Am2903's can be interconnected to form CPU's of 8, 16, 32, or more bits, in four-bit increments. Figure 2 illustrates the interconnection of four Am2903's to form a 16-bit CPU, using ripple carry.

With the exception of the carry interconnection, all expansion schemes are the same. The QIO_3 and SIO_3 pins are bidirectional left/right shift lines at the MSB of the device. For all devices except the most significant, these lines are connected to the QIO_0 and SIO_0 pins of the adjacent more significant device. These connections allow the Q Registers of all Am2903's to be shifted left or right as a contiguous n-bit register, and also allow the ALU output data to be shifted left or right as a contiguous n-bit word prior to storage in the RAM. At the LSB and MSB of the CPU, the shift pins should be connected to a shift multiplexer which can be controlled by the microcode to select the appropriate input signals to the shift inputs.

Device 1 has been defined as the least significant slice (LSS) and its $\overline{LSS}$ pin has accordingly been grounded. The Write/Most Significant Slice ($\overline{WRITE}/\overline{MSS}$) pin of device 1 is now defined as being the Write output, which may now be used to drive the write enable ($\overline{WE}$) signal common to the four devices. Devices 2 and 3 are designated as intermediate slices and hence the $\overline{LSS}$ and $\overline{WRITE}/\overline{MSS}$ pins are tied HIGH. Device 4 is designated the most significant slice ($\overline{MSS}$) with the $\overline{LSS}$ pin tied HIGH and the $\overline{WRITE}/\overline{MSS}$ pin held LOW. The open collector, bidirectional Z pins are tied together for detecting zero or for inter-chip communication for some special instruction. The Carry-Out (C_{n+4}) is connected to the Carry-In (C_n) of the next chip in the case of ripple carry. For a faster carry scheme, an Am2902 may be employed (as shown in Figure 3) such that the $\overline{G}$ and $\overline{P}$ outputs of the Am2903 are connected to the appropriate $\overline{G}$ and $\overline{P}$ inputs of the Am2902, while the C_{n+x}, C_{n+y}, and C_{n+z} outputs of the Am2902 are connected to the C_n input of the appropriate Am2903. Note that $\overline{G}$/N and $\overline{P}$/OVR pin functions are device dependent. The most significant slice outputs N and OVR while all other slices output $\overline{G}$ and $\overline{P}$.

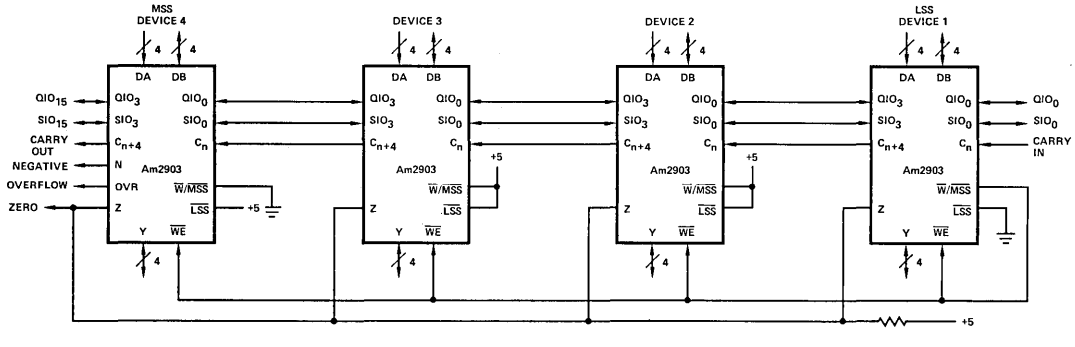

Figure 2. 16-Bit CPU with Ripple Carry.

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The $\overline{IEN}$ pin of the Am2903 allows the option of conditional instruction execution. If $\overline{IEN}$ is LOW, all internal clocking is enabled, allowing the latches, RAM, and Q Register to function. If $\overline{IEN}$ is HIGH, the RAM and Q Register are disabled. The RAM is controlled by $\overline{IEN}$ if $\overline{WE}$ is connected to the $\overline{WRITE}$ output.

It would be appropriate at this point to mention that the Am2903 may be microcoded to work in either two-or three-address architecture modes. The two-address modes allow A+B→B while the three-address mode makes possibleA+B→C. Implementation of a three-address architecture is made possible by varying the timing of $\overline{IEN}$ in relationship to the external clock and changing the B address as shown in Figure 4. This technique is discussed in more detail under Memory Expansion.

Parity

The Am2903 computes parity on a chosen word when the instruction bits I_{5-8} have the values of 4_{16} to 7_{16} as shown in Table 3. The computed parity is the result of the exclusive OR of the individual ALU outputs and SIO_3. Parity output is found on SIO_0. Parity between devices may be cascaded by the interconnection of the SIO_0 and SIO_3 ports of the devices as shown in Figure 3. The equation for the parity output at SIO_0 port of device 1 is given by $SIO_0 = F_{15} \forall F_{14} \forall F_{13} \forall \ldots \forall F_1 \forall F_0 \forall SIO_{15}$.

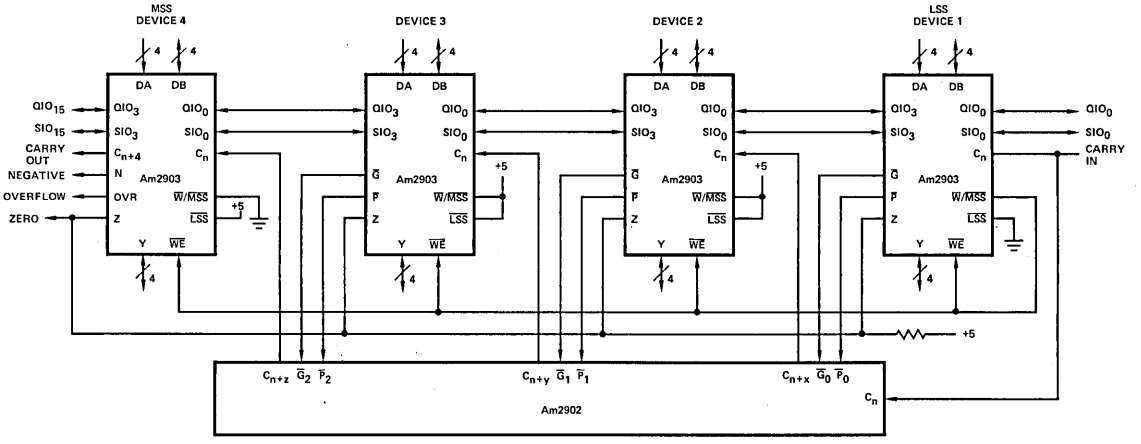

Figure 3. 16-Bit CPU with Carry Look Ahead.

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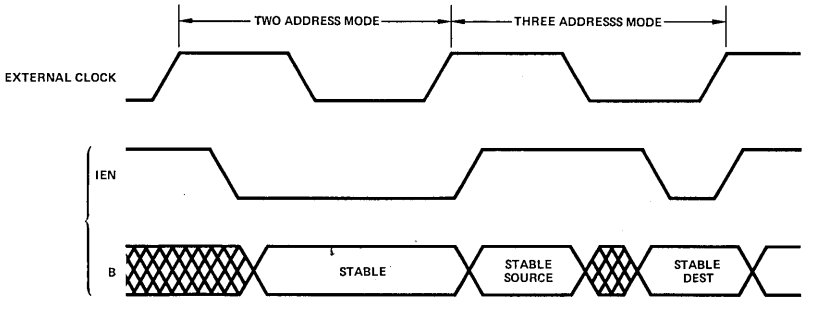


Figure 4. Relationship of $\overline{IEN}$ and Clock During Two Address and Three Address Modes.

MPR-038

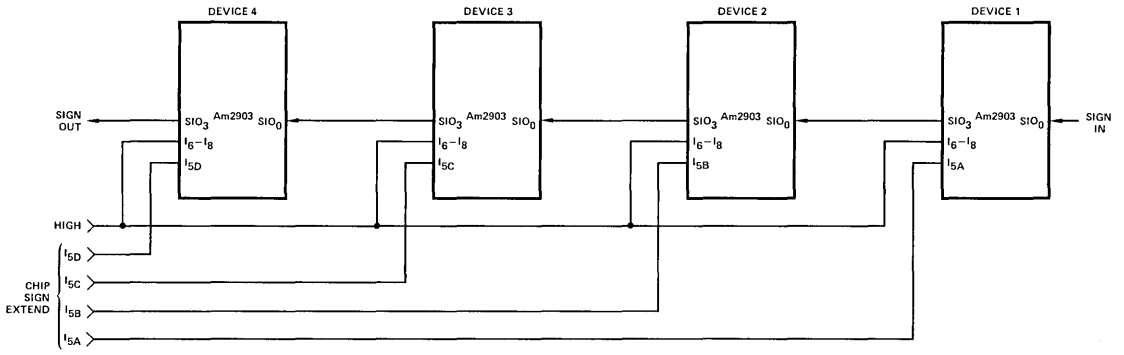


Figure 5. Sign Extend. MPR-039

Sign Extend

Sign extension across any number of Am2903 devices can be done in one microcycle. Referring again to the table of instructions (Table 3), the sign extend instruction (Hex instruction E) on I_{5-8} causes the sign present at the SIO_0 port of a device to be extended across the device and appear at the SIO_3 port and at the Y outputs. If the least significant bit of the instruction (bit I_5) is HIGH, Hex instruction F is present on I_{5-8}, commanding a shifter pass instruction. At this time, F_3 of the ALU is present on the SIO_3 output pin. It is then possible to control the extension of the sign across chip boundaries by controlling the state of I_5 when I_{6-8} are HIGH. Figure 5 outlines the Am2903 in sign extend mode. With I_{6-8} held HIGH, the individual chip sign extend is controlled by $I_{5A\text{-}D}$. If, for example, I_{5A} and I_{5B} are HIGH while I_{5C} and I_{5D} are LOW, the signal present at the boundaries of devices 2 and 3 (F_3 of device 2) will be extended across devices 3 and 4 at the SIO_3 pin of device 4. The output of the four devices will be available at their respective Y data ports. The next positive edge of the clock will load the Y outputs into the address selected by the B port. Hence, the results of the sign extension is stored in the RAM.

SPECIAL FUNCTIONS

When $I_{0-4} = 0$, the Am2903 is in the Special Function mode. In this mode, both the source and destination are controlled by I_{5-8}. The Special Functions are in essence special microinstructions that are used to reduce the number of microcycles needed to execute certain functions in the Am2903.

Normalization, Single- and Double-Length

Normalization is used as a means of referencing a number to a fixed radix point. Normalization strips out all leading sign bits such that the two bits immediately adjacent to the radix point are of opposite polarity.

Normalization is commonly used in such operations as fixed-to-floating point conversion and division. The Am2903 provides for normalization by using the Single-Length and Double-Length Normalize commands. Figure 6a represents the Q Register of a 16-bit processor which contains a positive number. When the Single-Length Normalize command is applied, each positive edge of the clock will cause the bits to shift toward the most significant bit (bit 15) of the Q Register. Zeros are shifted in via the QIO_0 port. When the bits on either side of the radix point (bits 14 and 15) are of opposite value, the number is considered to be normalized as shown in Figure 6b. The event of normalization is externally indicated by a HIGH level on the C_{n+4} pin of the most significant slice (C_{n+4} MSS = Q_3 MSS $\forall$ Q_2 MSS).

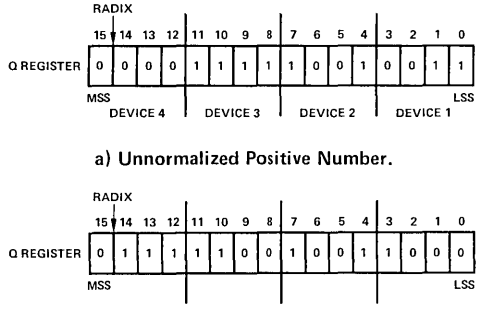


Figure 6. MPR-040

There are also provisions made for a normalization indication via the OVR pin one microcycle before the same indication is available on the C_{n+4} pin (OVR = Q_2 MSS $\forall$ Q_1 MSS). This is for use in applications that require a stage of register buffering of the normalization indication.

Since a number comprised of all zeros is not considered for normalization, the Am2903 indicates when such a condition arises. If the Q Register is zero and the Single-Length Normalization command is given, a HIGH level will be present on the Z line. The sign output, N, indicates the sign of the number stored in the Q register, Q_3 MSS. An unnormalized negative number (Figure 7a) is normalized in the same manner as a positive number. The results of single-length normalization are shown in Figure 7b. The device interconnection for single-length normalization is outlined in Figure 8. During single length normalization, the number of shifts performed to achieve normalization can be counted and stored in one of the working registers. This can be achieved by forcing a HIGH at the C_n input of the least significant slice, since during this special function the ALU performs the function [B] + C_n and the result is stored in B.

Normalizing a double-length word can be done with the Double-Length Normalize command which assumes that a user-selected RAM Register contains the most significant portion of the word to be normalized while the Q Register holds the least significant half (Figure 9). The device interconnection for double-length normalization is shown in Figure 10. The C_{n+4}, OVR, N, and Z outputs of the most significant slice perform the same functions in double-length normalization as they did in single-length normalization except that C_{n+4}, OVR, and N are derived from the output of the ALU of the most significant slice in the case of double-length normalization, instead of the Q Register of the most significant

a) Unnormalized Negative Single Length Number.

b) Normalized Negative Single Length Number.

Figure 7.

MPR-041

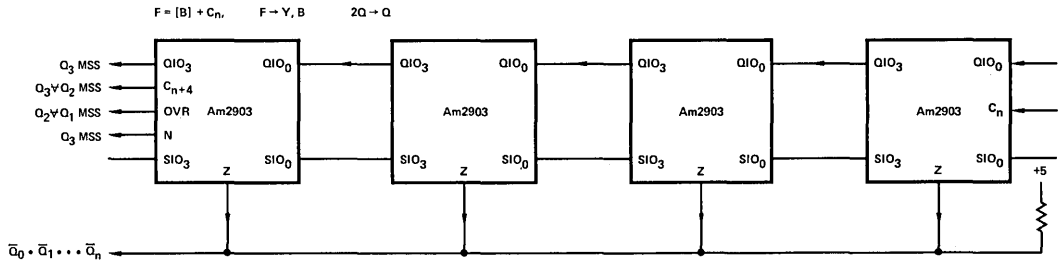


Figure 8. Single Length Normalize.

MPR-042

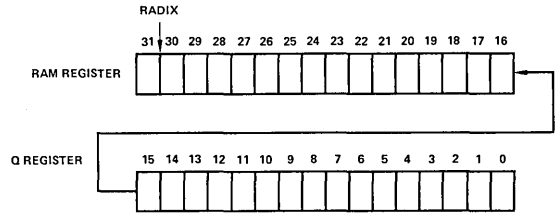


Figure 9. Double Length Word.

MPR-043

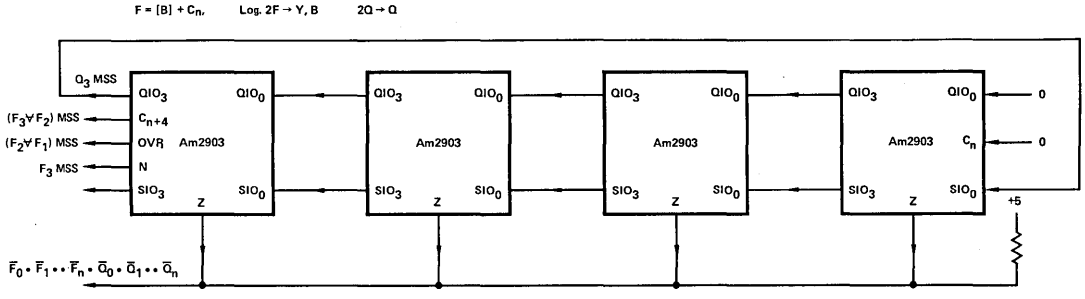


Figure 10. Double Length Normalize.

MPR-044

slice as in single-length normalization. A high-level Z line in double-length normalization reveals that the outputs of the ALU and Q Register are both zero, hence indicating that the double-length word is zero.

When double-length normalization is being performed, shift counting is done either with an extra microcycle or with an external counter.

Sign Magnitude, Two's Complement Conversion

As part of the special instruction set, the Am2903 can convert between two's complement and sign/magnitude representations. Figure 11 illustrates the interconnection needed for sign magnitude/two's complement conversion. The word to be converted is applied to the S input port of the ALU (from the RAM B port or the DB I/O port). The C_n input of device 1 is connected to the Z pin. The sign bit (S_3MSS) is brought out on the Z line and informs the other ALU's if the conversion is being performed on a negative or positive number. If the number to be converted is the most negative number in two's complement [i.e., 100 . . . 00 (-2^n)], an overflow indication will occur. This is because -2^n is one greater than any number that can be represented in sign magnitude notation and hence an attempted conversion to sign magnitude from -2^n will cause an overflow. When minus zero in sign magnitude notation (100 . . . 0) is converted to two's complement notation, the correct result is obtained (0 . . .0).

Increment by One or Two

Incrementation by One or Two is made possible by the Special Function of the same name. This command is quite useful in the case of byte addressable words. Referencing Figure 12, a word may be incremented by one if C_n is LOW or incremented by two if C_n is HIGH.

Unsigned Multiply

This Special Function allows for easy implementation of unsigned multiplication. Figure 13 is the unsigned multiply flow chart. The algorithm requires that initially the RAM word addressed by Address port B be zero, that the multiplier be in the Q Register, and that the multiplicand be in the register addressed by Address port A. The initial conditions for the execution of the algorithm are that: 1) register R_0 be reset to zero; 2) the multiplicand be in R_1; and 3) the multiplier be in R_2. The first operation transfers the multiplier, R_2, to the Q Register. The Unsigned Multiply instruction is then executed 16 times. During the Unsigned Multiply instruction, R_0 is addressed by RAM address port B and the multiplicand is addressed by RAM address port A.

When the unsigned Multiply command is given, the Z pin of device 1 becomes an output while the Z pins of the remaining devices are specified as inputs as shown in Figure 15. The Z output of device 1 is the same state as the least significant bit of the multiplier in the Q Register. The Z output of device 1 informs the ALU's of all the slices, via their Z pins, to add the partial product (referenced by the B address port) to the mul-

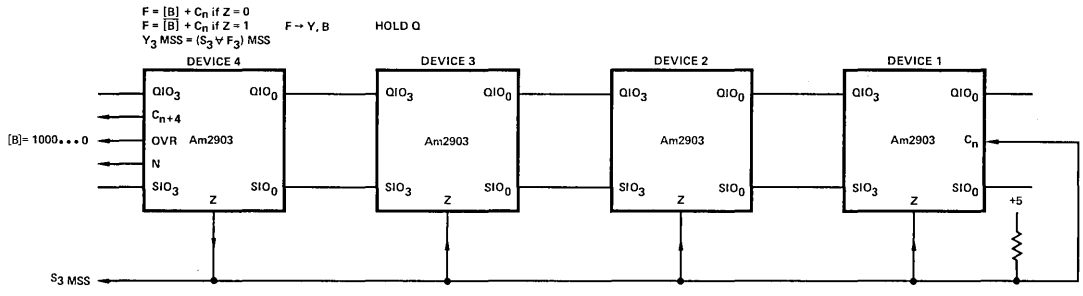


Figure 11. 2's Complement←→Sign/Magnitude.

MPR-045

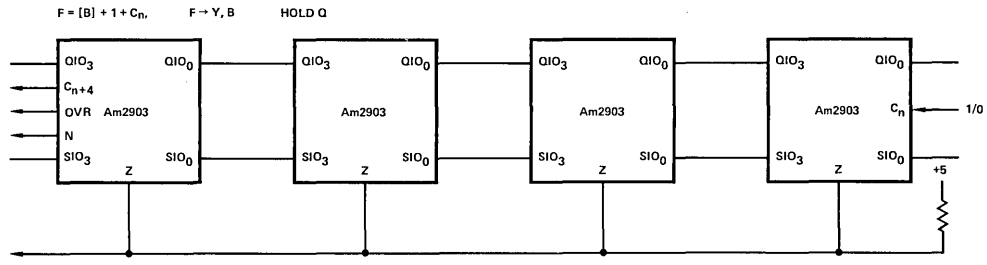


Figure 12. Increment by 2/1.

MPR-046

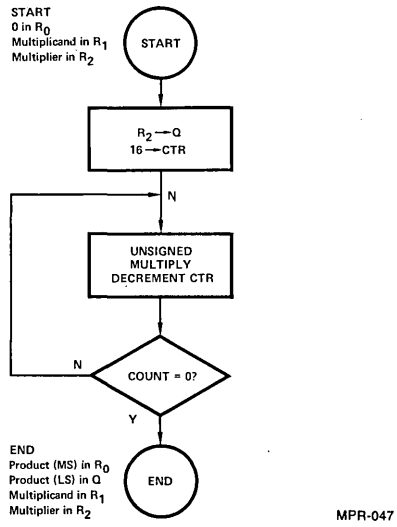


Figure 13. Unsigned 16 X 16 Multiply Flowchart.

tiplicand (referenced by the A address port) if Z = 1. If Z = 0, the output of the ALU is simply the partial product (referenced by the B address port). Since C_n is held LOW, it is not a factor in the computation. Each positive-going edge of the clock will internally shift the ALU outputs toward the least significant bit and simultaneously store the shifted results in the register selected by the B address port, thus becoming the new partial sum. During the down shifting process, the C_{n+4} generated in device 4 is internally shifted into the Y_3 position of device 4. At this time, one bit of the multiplier will down shift out of the QIO_0 ports of each device into the QIO_3 port of the next less significant slice. The partial product is shifted down between chips in a like manner, between the SIO_0 and SIO_3 ports, with SIO_0 of device 1 being connected to QIO_3 of device 4 for purposes of constructing a 32-bit long register to hold the 32-bit product. At the finish of the 16 x 16 multiply, the most significant 16 bits of the product will be found in the register referenced by the B address lines while the least significant 16 bits are stored in the Q Register. Using a typical Computer Control Unit (CCU), as shown in Figure 16, the unsigned multiply operation requires only two lines of microcode, as shown in Figure 17, and is executed in 17 microcycles.

Two's Complement Multiplication

The algorithm for two's complement multiplication is illustrated by Figure 14. The initial conditions for two's complement multiplication are the same as for the unsigned multiply operation. The Two's Complement Multiply Command is applied for 15 clock cycles in the case of a 16 x 16 multiply. During the down shifting process the term N∀OVR generated in device 4 is internally shifted into the Y_3 position of device 4. The data flow shown in Figure 15 is still valid. After 15 cycles, the sign bit of the multiplier is present at the Z output of device 1. At this time, the user must place the Two's Complement Multiply Last cycle command on the instruction lines. The interconnection for this instruction is shown in Figure 18. On the next positive edge of the clock, the Am2903 will adjust the partial product, if the sign of the multiplier is negative, by subtracting out the two's complement representation of the multiplicand. If the sign bit is positive, the partial product is not adjusted. At this point, two's complement multiplication is completed. Using a typical CCU, as shown in Figure 16, the two's complement multiply operation requires only three lines of microcode, as shown in Figure 19, and is executed in 17 microcycles.

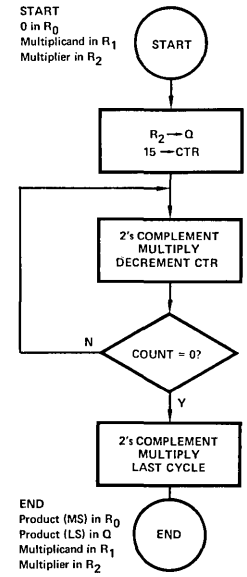
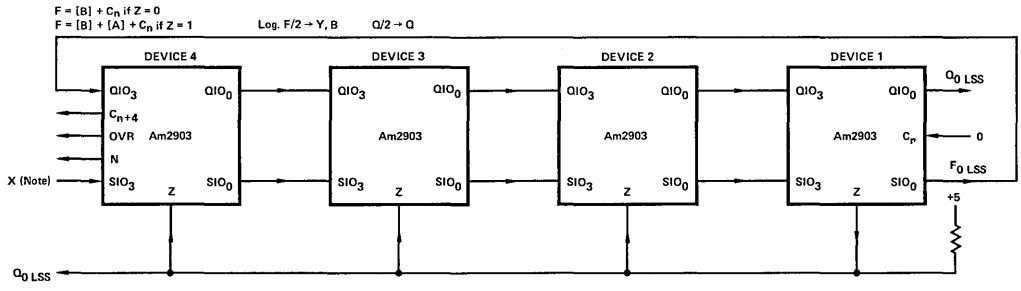


Figure 14. 2's Complement 16 X 16 Multiply.



Note: For unsigned multiply, C_{n+4} MSS is internally shifted into position Y_3 MSS; 2's complement multiply N∀OVR is internally shifted into position Y_3 MSS.

Figure 15. Multiply.

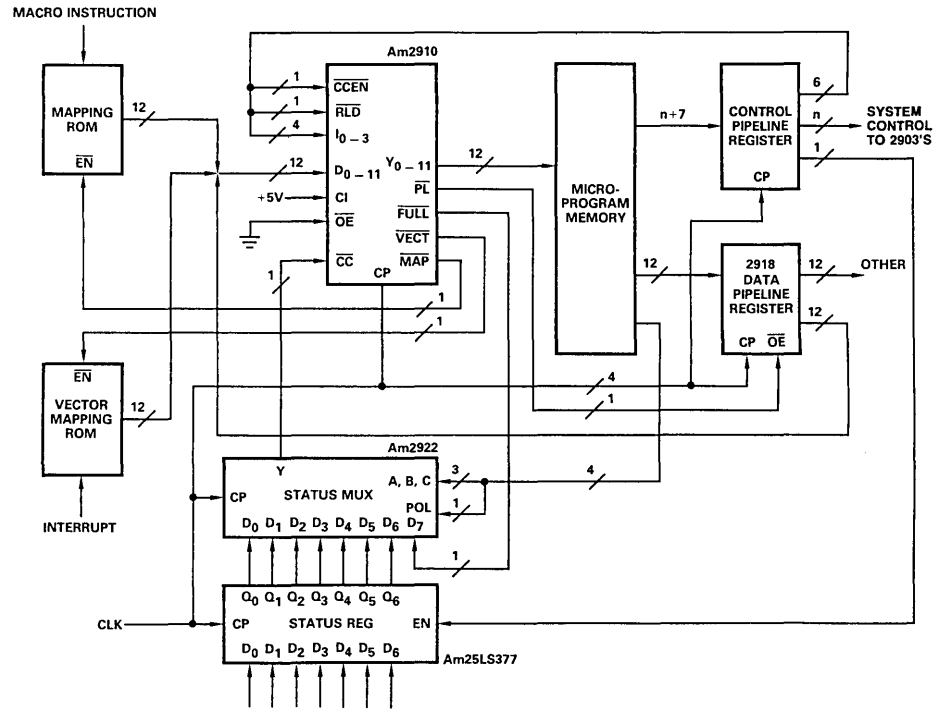
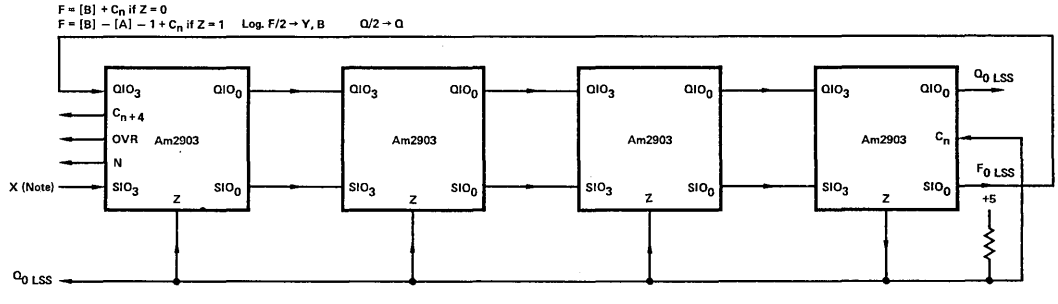


Figure 16. Typical Computer Control Unit (CCU).

MPR-050

Micro Memory Address	Am2910 Inst	Data Pipeline Reg.	I_0	I_4-I_1	I_8-I_5	$\overline{OEB}$	$\overline{OEY}$	A_3-A_0	B_3-B_0	C_n	Comment
n	LDCT	$00F_{16}$	X	6	6	X	X	R_2	X	0	Load Counter & $R_2 \rightarrow Q$
n+1	RPCT	n+1	0	0	0	0	0	R_1	R_0	0	Unsigned Multiply

Figure 17. Micro Code for Unsigned 16 X 16 Multiply.



Note: N ∀ OVR is internally shifted into position Y_3 MSS.

Figure 18. 2's Complement Multiply, Last Cycle.

MPR-051

Memory Address	Am2910 Inst	Data Pipeline Reg.	I_0	I_4-I_1	I_8-I_5	$\overline{OEB}$	$\overline{OEY}$	A_3-A_0	B_3-B_0	C_n	Comment
n	LDCT	$00E_{16}$	X	6	6	X	X	R_2	X	0	Load Counter & $R_2 \rightarrow Q$
n+1	RPCT	n+1	0	0	2	0	0	R_1	R_0	0	2's Complement Multiply
n+2	X	X	0	0	6	0	0	R_1	R_0	Z	2's Complement Multiply (Last Cycle)

Figure 19. Microcode for 2's Complement 16 x 16 Multiply.

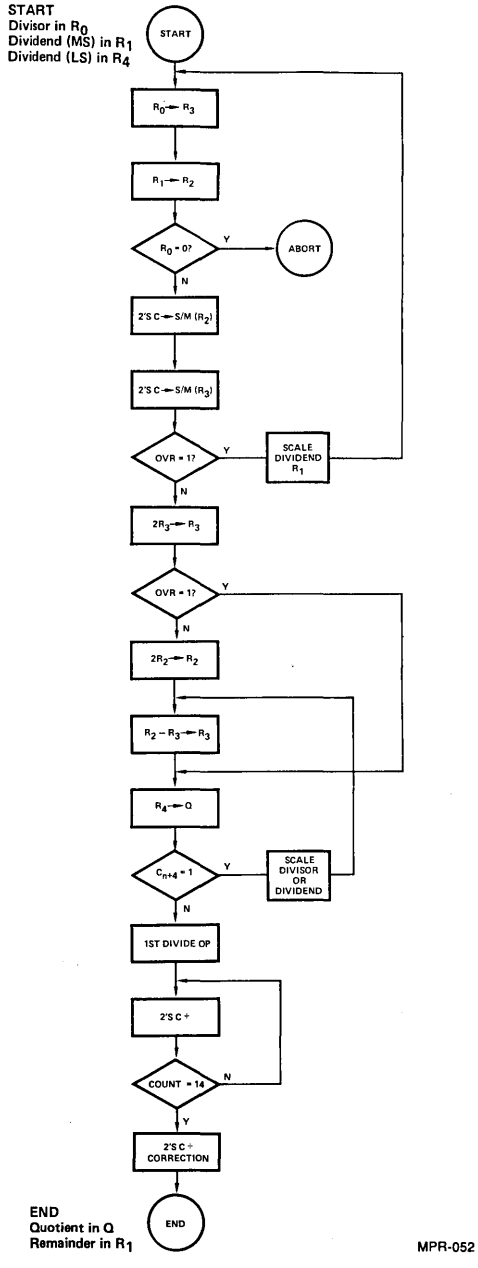


Figure 20. Division Flow Chart – Double Precision Divide.

TWO'S COMPLEMENT DIVISION

The division process is accomplished using a four quadrant non-restoring algorithm which yields an algebraically correct answer such that the divisor times the quotient plus the remainder equals the dividend. The algorithm works for both single precision and multi-precision divide operations. The only condition that needs to be met is that the absolute magnitude of the divisor be greater than the absolute magnitude of the dividend. For multi-precision divide operations the least significant bit of the dividend is truncated. This is necessary if the answer is to be algebraically correct. Bias correction is automatically provided by forcing the least significant bit of the quotient to a one, yet an algebraically correct answer is still maintained. Once the algorithm is completed, the answer may be modified to meet the user's format requirements, such as rounding off or converting the remainder so that its sign is the same as the dividend. These format modifications are accomplished using the standard Am2903 instructions.

The true value of the remainder is equal to the value stored in the working register times 2^{n-1} when n is the number of quotient digits.

The following paragraphs describe a double precision divide operation. The double precision flow chart is based upon the use of the architecture detailed in Figure 16.

Referring to the flow chart outlined in Figure 20, we begin the algorithm with the assumption that the divisor is contained in R_0, while the most significant and least significant halves of the dividend reside in R_1 and R_4 respectively. The first step is to duplicate the divisor by copying the contents of R_0 into R_3. Next the most significant half of the dividend is copied by transferring the contents of R_1 into R_2 while simultaneously checking to ascertain if the divisor (R_0) is zero. If the divisor is zero then division is aborted. If the divisor is not zero, the copy of the most significant half of the dividend in R_2 is converted from its two's complement to its sign magnitude representation. The divisor in R_3 is converted in like manner in the next step, while testing to see if the results of the dividend conversion yielded an indication on the overflow pin of the Am2903. If the output of the overflow pin is a 'one' then the dividend is -2^n and hence is the largest possible number, meaning that it cannot be less than the divisor. What must be done in this case is to scale the dividend by down shifting the upper and lower halves stored in R_1 and R_4 respectively. After scaling, the routine requires that the algorithm be reinitiated at the beginning.

Conversely, if the output of the overflow pin is not a one, the sign magnitude representation of the divisor (R_3) is shifted up in the Am2903, removing the sign while at the same time testing the results of two's complement to sign magnitude conversion of the divisor in the Am2910. If the results of the test indicate that the divisor is -2^n i.e., overflow equals one, then the lower half of the dividend is placed in the Q register

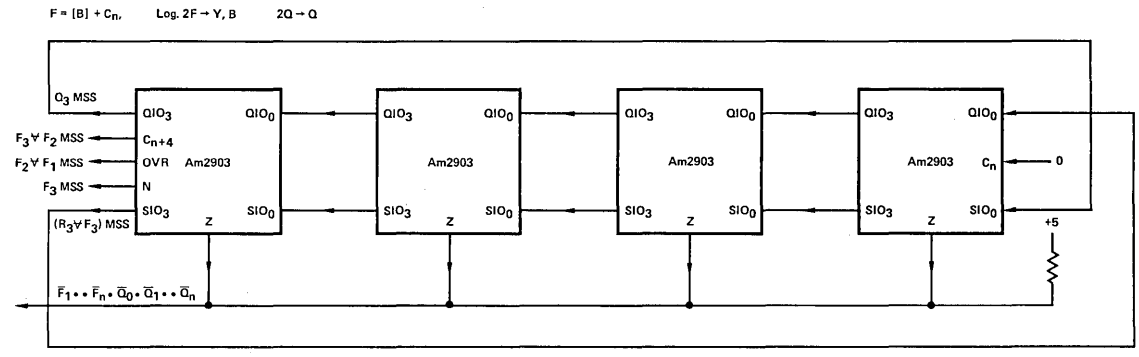


Figure 21. Double Length Normalize/First Divide Operation.

MPR-053

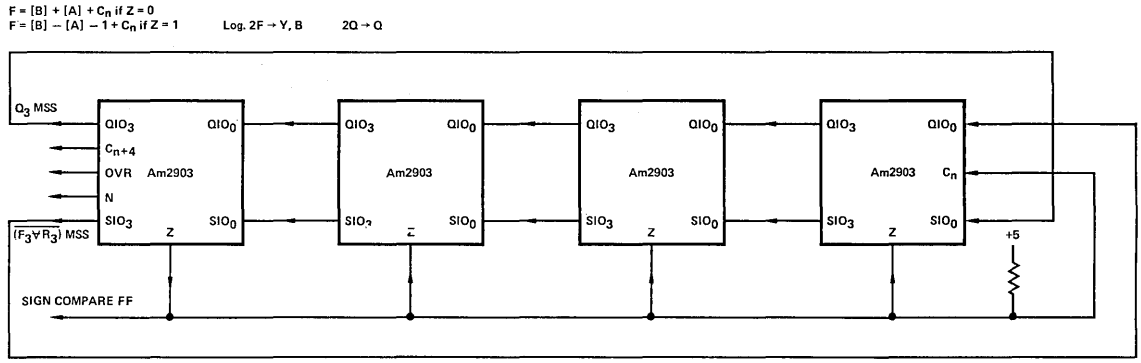


Figure 22. 2's Complement Divide.

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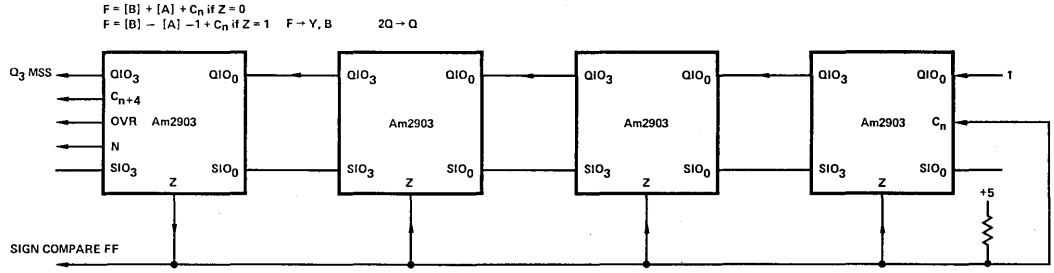

Figure 23. 2's Complement Divide Correction.

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and division may proceed. This is possible because the divisor is now guaranteed to be greater than the dividend. If overflow is not a one then we must proceed by shifting out the sign of the sign magnitude representation of the dividend stored in R_2. At this point we are able to check if the divisor is greater than the dividend by subtracting the absolute value of the divisor (R_3) from the absolute value of the upper half of the dividend (R_2) and storing the results in R_3. Next, the least significant half of the dividend is transferred from R_4 to the Q register while simultaneously testing the carry from the result of the divisor/dividend subtraction. If the carry (C_{n+4}) is one, indicating the divisor is not greater than the dividend then a scaling operation must occur. This involves either shifting up the divisor or shifting down the dividend. If the carry is not one then the divisor is greater than the dividend and division may now begin.

Micro Memory Address	Am2910 Inst.	Data Pipeline Reg.	Am2903 I_0	I_4-I_1	I_8-I_5	$\overline{EA}$	A_3-A_0	B_3-B_0	C_n	Am2922 SEL	POL	Am29LS18 E	Comment
n	CONT	X	0	6	4	0	R_0	R_3	0	X	X	0	$R_0 \rightarrow R_3$
n+1	CJP	Abort	0	6	4	0	R_1	R_2	0	Z	1	X	$R_1 \rightarrow R_2$, if $R_0 = 0$ Abort
n+2	CONT	X	0	0	5	X	X	R_2	0	X	X	0	2's C to S/M (R_2)
n+3	CJP	Scale Dividend	0	0	5	X	X	R_3	0	OVR	1	0	2's C to S/M (R_3), if OVR ≥ 1, scale
n+4	CJP	n+7	0	4	9	X	X	R_2	0	OVR	1	X	Shift out sign of divisor
n+5	CONT	X	0	4	9	X	X	R_3	0	X	X	X	Shift out sign of divisor
n+6	CONT	X	0	2	F	0	R_2	R_3	1	X	X	0	Dividend – Divisor $\rightarrow R_3$
n+7	CJP	Scale Dividend orDivisor	0	6	6	0	R_4	X	0	C_{n+4}	0	X	$R_4 \rightarrow$ Q, if Carry = 1, scale
n+8	PUSH	$00D_{16}$	0	0	A	0	R_0	R_1	0	0	1	X	Loop set up & First Divide Operation
n+9	RFCT	X	0	0	C	0	R_0	R_1	Z	X	X	X	Test Loop Count & 2's C Divide
n+A	CONT	X	0	0	E	0	R_0	R_1	Z	X	X	X	2's C Divide Correction

Figure 24. Microcode for Double Precision Divide.

The first divide operation is used to ascertain the sign bit of the quotient. The two's complement divide instruction is then executed repetitively, fourteen times in the case of a sixteen bit divisor and a thirty-two bit dividend. The final step is the two's complement correction command which adjusts the quotient by allowing the least significant bit of the quotient to be set to one. At the end of the division algorithm the sixteen bit quotient is found in the Q register while the remainder now replaces the most significant half of the dividend in R_1. It should be noted that the remainder must be shifted down fifteen places to represent its true value. The interconnections for these instructions are shown in Figures 21, 22, 23. Using a typical CCU as shown in Figure 16, the double precision divide operation requires only eleven lines of microcode, as shown in Figure 24.

For those applications that require truncation instead of bias correction, the same algorithm as above should be implemented except one additional Two's Complement Divide instruction should be used in lieu of the Two's Complement Divide Correction and Remainder instruction. However, this technique results in an invalid remainder.

It is possible to do multiple-precision divide operations beyond the double precision divide shown above. For example, to do a triple precision divide for a 16-bit CPU, the upper two thirds of the dividend are stored in R_1 and Q as in the case for double precision divide. The lower third of the dividend is stored in a scratch register, R_5. After checking that the magnitude of the divisor is greater than the magnitude of the dividend, using the same tests as defined in Figure 20, the procedure is as follows:

1. Execute a Double Length Normalize/First Divide Operation instruction.
2. Execute the Two's Complement Divide instruction fifteen times.
3. Transfer the contents of Q, the most significant half of the quotient, to R_2.
4. Transfer R_5 to Q.
5. Execute the Two's Complement Divide instruction fifteen times.
6. Execute the Two's Complement Divide Correction and Remainder instruction.

The upper half of the quotient is then in R_2, the lower half of the quotient is in Q and the remainder is in R_1. The flow chart for this is shown in Figure 25. This technique can be expanded for any precision which is required.

Byte Swap

The multi-port architecture of the Am2903 allows for easy implementation of high- and low-order byte swapping. Figure 26 outlines a byte swap implementation utilizing two data ports. Initially, the lower order 8-bit byte is stored in devices 1 and 2, while the high-order byte is in devices 3 and 4. When the user wishes to exchange the two bytes, the register location of the desired word is placed on the B address port. When the byte swap line is brought LOW, the bytes to be swapped will be flowing from the DB ports of the Am2903 through the Am25LS240/244 Three-state Buffers. The outputs of the

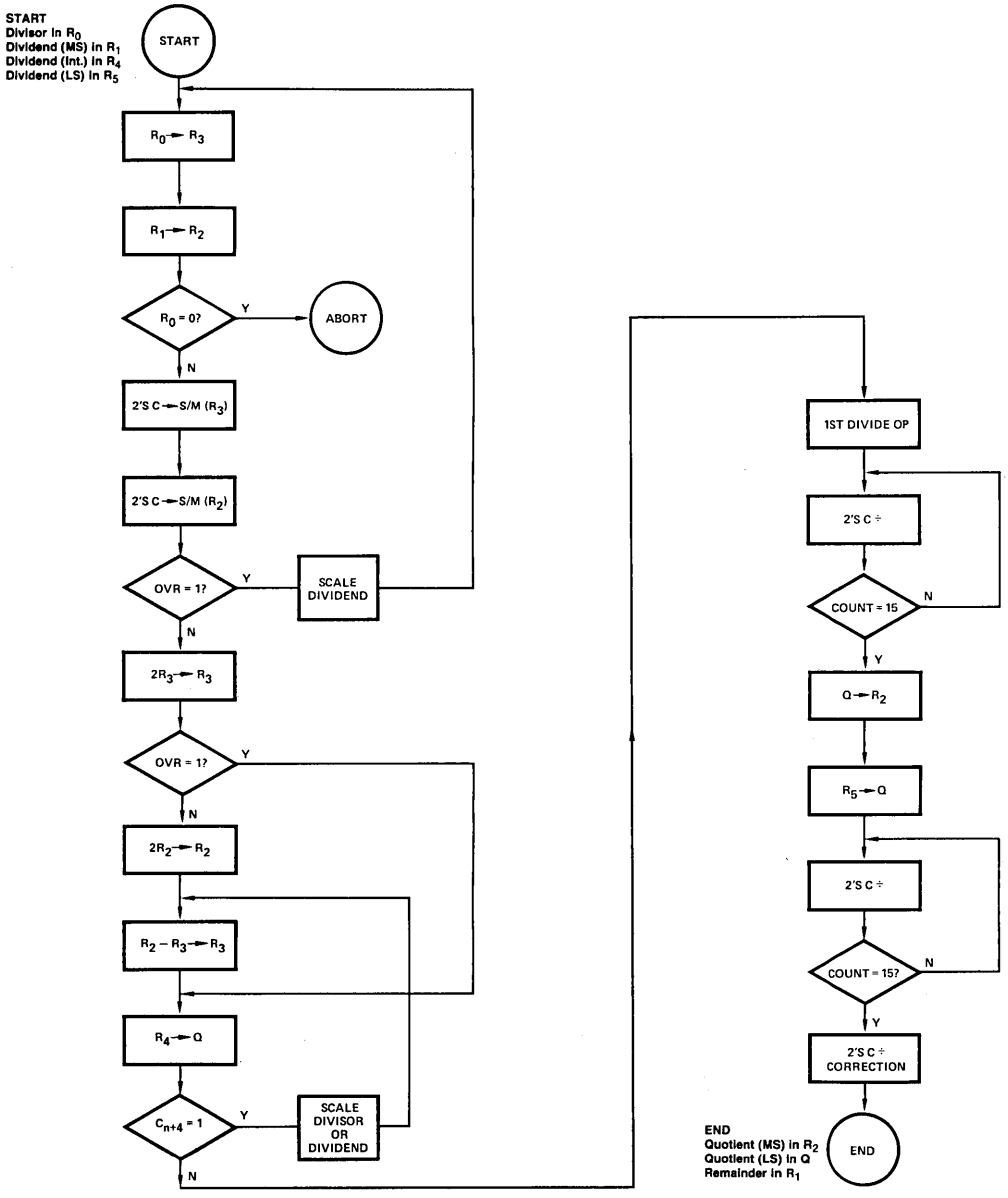

Figure 25. Division Flow Chart — Triple Precision Divide.

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three-state buffers are permuted such that the byte swap is achieved. The resultant permuted data is presented to the DA ports of the Am2903 where it is re-loaded into the memories of the Am2903 on the next positive edge of CP using the source and function commands of F= $\overline{A}$ plus C_n (C_n = 0) for the Am25LS240 or F = A plus C_n (C_n = 0) for the Am25LS244 and the destination command F→Y, B.

A higher speed technique for achieving the byte swap operation is illustrated in Figure 27. Instead of inputting the permuted data via the DA ports, the permuted data is inputted via the Y input/output ports with $\overline{OE}_Y$ held HIGH. This technique bypasses the ALU, thus allowing faster operation. The Am2903 destination command F → Y, B should be used.

Memory Expansion

The Am2903 allows for a theoretically infinite memory expansion. Figure 28 pictures a 4-bit slice of a system which has 48 words of RAM and 16 words of ROM. RAM storage is provided by the Am2903 and the Am29705's. The Am29705 RAM is functionally identical to the Am2903 RAM. The Am29751A is used to store constants and masks and is addressable from address port A only. The system is organized around five data buses. Inter-bus communication may be done through the Am29705's or the Am2903. The memory addressing scheme specifies the data source for the R input of the ALU eminating from the register locations specified by address field A. A_{0-3} addresses 16 memory locations in each chip while address bits A_{4-6} are decoded and used for the output enable for the desired chip. The B address field is used to select the S input of the ALU and the C field is used to specify the register location where the result of the ALU operation is to be stored.

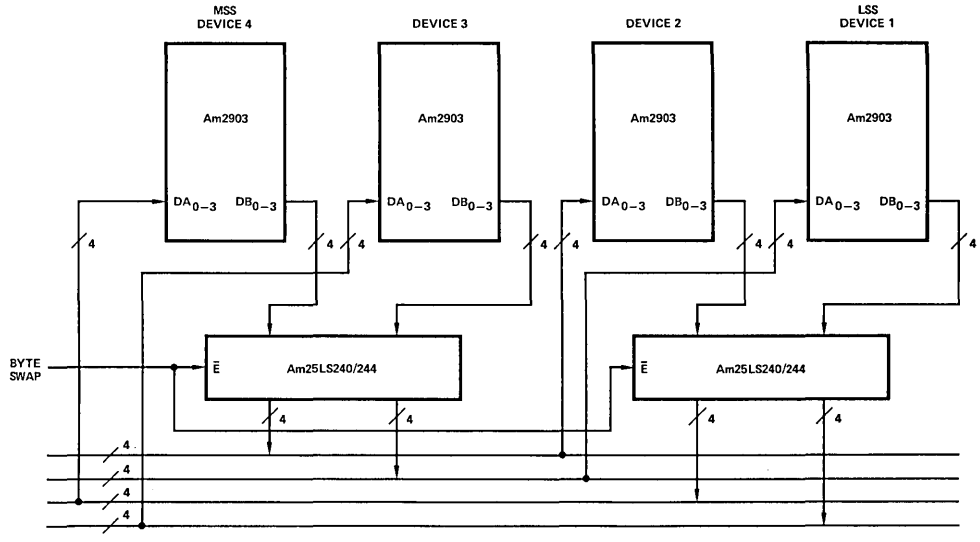

Figure 26. Byte Swap.

MPR-057

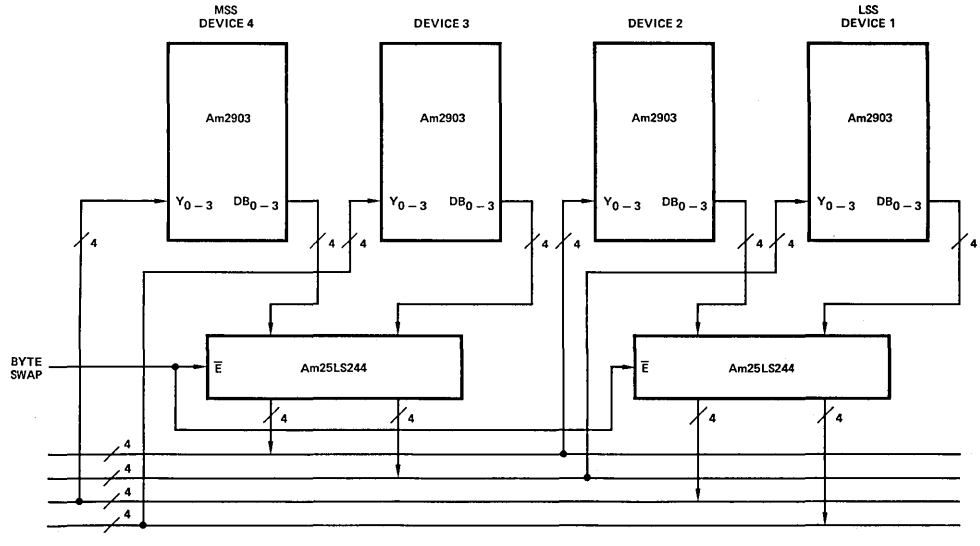

Figure 27. High Speed Byte Swap.

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Bits B_{0-3} are for source register addressing in each chip. Bits B_4 and B_5 are used for chip output enable selection. C_{0-3} access the 16 destination addresses on each chip while bits C_4 and C_5 control the Write Enable of the desired chip. The source and destination register address are multiplexed such that when the clock is HIGH, the source register address is presented to the B address ports of the RAM's. The Instruction Enable ($\overline{IEN}$) is HIGH at this time. The data flows from the Y port or the internal B port as selected by the decoder whose inputs are B_4 and B_5. When the clock goes LOW, the data eminating from the selected Y outputs of the Am29705's and the RAM outputs of the Am2903 are latched and the destination address is now selected for use by the RAM address lines. When the destination address stabilizes on the address lines, the $\overline{IEN}$ pin is brought LOW. The $\overline{WRITE}$ output of the Am2903 will now go LOW, enabling the decoder sourced by address bits C_4 and C_5. The selected decoder line will go LOW, allowing the desired memory location to be written into. To switch between two- and three-address architecture, the user simply makes the source and destination addresses the same; i.e., $B_{0-3} = C_{0-3}$ and $B_{4-5} = C_{4-5}$. For two-address architecture, the MUX is removed from the circuit.

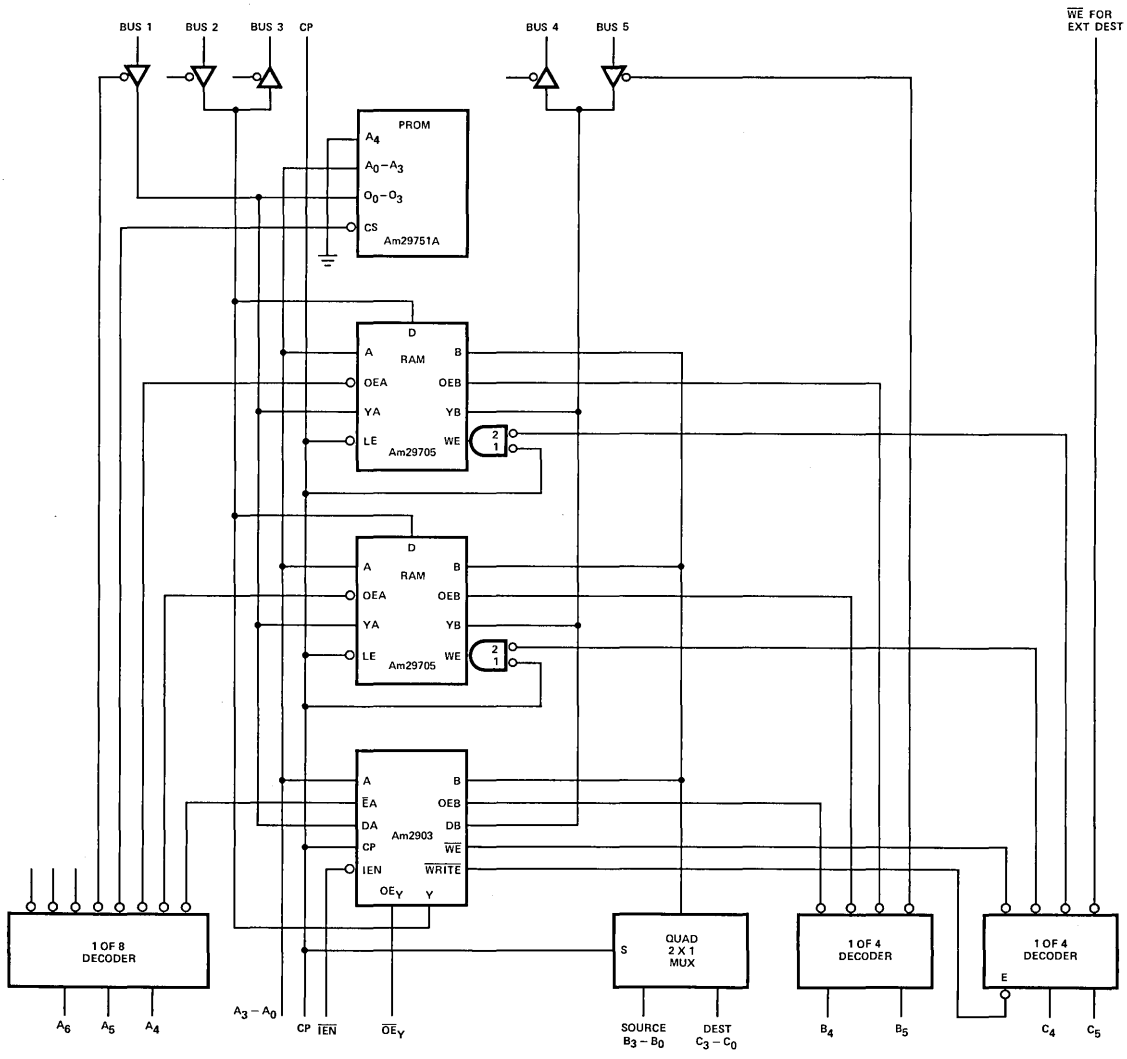


Figure 28. Expanded Memory.

MPR-059

Am2904

Status and Shift Control Unit

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- **Replaces most MSI used around any ALU** including the Am2901A, Am2903 and MSI ALUs.
- **Generates Carry-In to the ALU**
  Carry signal is selectable from 7 different sources.
- **Contains shift linkage multiplexers**
  Connects to shift lines at the ends of a Am2901A or Am2903 array to implement single and double length arithmetic and logical shifts and rotates – 32 different modes in all.
- **Contains two edge-triggered status registers**
  Use for foreground/background registers or as microlevel and machine level status registers. Bit manipulating instructions are provided.
- **Condition Code Multiplexer on chip**
  Single cycle tests for any of 16 different conditions. Tests can be performed on either of the two status registers or directly on the ALU output.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

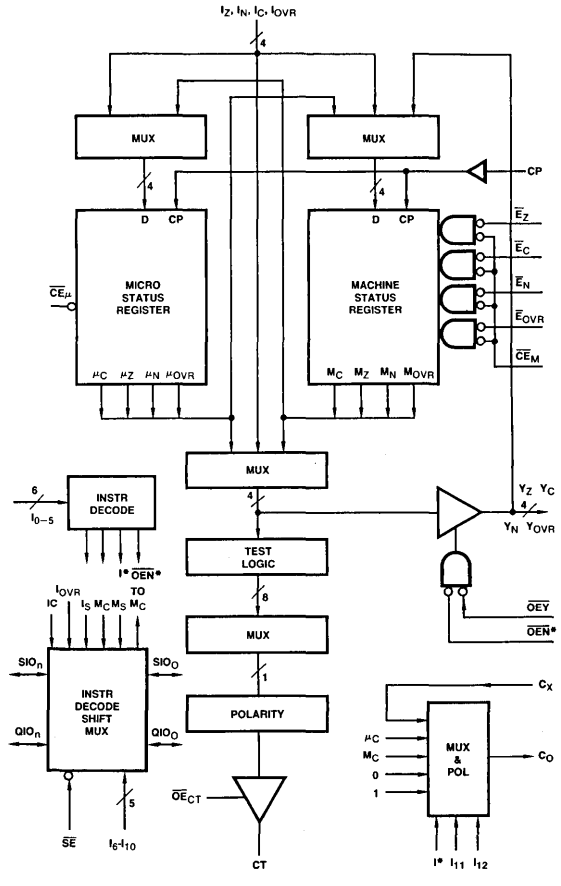
Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2904PC	P-40	C	C-1
AM2904DC	D-40	C	C-1
AM2904DC-B	D-40	C	B-1
AM2904DM	D-40	M	C-3
AM2904DM-B	D-40	M	B-3
AM2904FM	F-42	M	C-3
AM2904FM-B	F-42	M	B-3
AM2904XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2904XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

DESCRIPTION

The Am2904 is designed to perform all the miscellaneous functions which are usually performed in MSI around an ALU. These include the generation of the carry-in signal to the ALU and carry lookahead unit; the interconnection of the data path, auxiliary register, and carry flip-flop during shift operations; and the storage and testing of ALU status flags. These tasks are accomplished in the Am2904 by three nearly independent blocks of logic. The carry-in is generated by a multiplexer. The shift linkages are established by four three-state multiplexers. There are two registers for storing the carry, overflow, zero, and negative status flags. The condition code multiplexer on the Am2904 can look at true or complement of any of the four status bits and certain combinations of status bits from either of the storage registers or directly from the ALU.

BLOCK DIAGRAM



MPR-060

PRODUCT DESCRIPTION

The Am2904 Status and Shift Control Unit provides four functions which are included in all processors. These are: a) Status Register, b) Condition Code Multiplexer, c) Shift Linkages and d) Carry-in Control.

STATUS REGISTER

The Am2904 contains two four-bit registers which can store the status outputs of an ALU: Carry (C), Negative (N), Zero (Z), and Overflow (OVR). They are designated Micro Status Register (μSR) and Machine Status Register (MSR). Each register can be independently controlled.

The μSR can be loaded from the four status inputs (I_C, I_N, I_Z, I_{OVR}) or from the MSR under instruction control (I_{0-5}). The bits in the μSR can also be individually set or reset under instruction control (I_{0-5}). When the $\overline{CE}_\mu$ input is HIGH, the μSR is inhibited from changing, independent of the I_{0-5} inputs.

The MSR can be loaded from the four status inputs (I_C, I_N, I_Z, I_{OVR}), from the μSR and from the four parallel input/output pins (Y_C, Y_N, Y_Z, Y_{OVR}) under instruction control (I_{0-5}). The bits in the MSR can also be individually set, reset or complemented under instruction control (I_{0-5}). The bits in the MSR can be selectively updated by controlling the four bit-enable inputs ($\overline{E}_Z$, $\overline{E}_N$, $\overline{E}_C$, $\overline{E}_{OVR}$) and the $\overline{CE}_M$ input. A LOW on both the $\overline{CE}_M$ input and the bit enable input for a specific bit enables updating that bit. A HIGH on a given bit enable input disables the corresponding bit in the MSR.

The four parallel bidirectional input/output pins (Y_Z, Y_N, Y_C, Y_{OVR}) allow the contents of both the μSR and the MSR to be transferred to the system data bus and also allow both registers to be loaded from the system data bus. This capability is used to save and restore registers during microlevel subroutines and when servicing interrupts.

CONDITION CODE MULTIPLEXER

The Condition Code Multiplexer output, CT, can be selected from 16 different functions which test for arithmetic comparisons such as "greater than", " greater than or equal to", "less than" and "less than or equal to", for both unsigned numbers and two's complement numbers. The Am2904 has the ability to perform these tests on the contents of the μSR, the MSR or the direct status inputs, (I_Z, I_N, I_C, I_{OVR}). The CT output is used as the test ($\overline{CC}$) input of the Am2910.

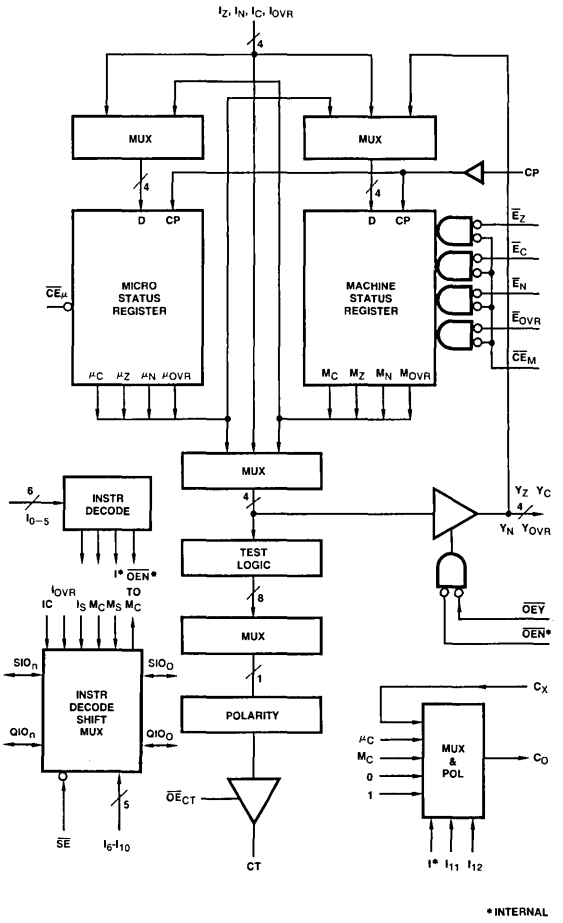
SHIFT LINKAGE MULIPLEXER

The Shift Linkage Multiplexer generates the necessary outputs to perform 32 different shift and rotate functions. Both single length and double length shifts and rotates are provided. Shifts and rotates both with and without carry (M_C) are provided. When the $\overline{SE}$ input is High, the four input/output pins (SIO_0, SIO_n, QIO_0, QIO_n) are disabled. The SIO_0, SIO_n, QIO_0 and QIO_n pins of the Am2904 are intended to be directly connected to the RAM_0, RAM_3, Q_0, and Q_3 pins of the Am2901A or the SIO_0, SIO_3, QIO_0 and QIO_3 pins of the Am2903.

CARRY-IN CONTROL MULTIPLEXER

The Carry-in Control Multiplexer generates the C_0 output which can be selected from 7 functions (0, 1, C_X, μ_C, M_C, $\overline{\mu}_C$, $\overline{M}_C$). These functions allow easy implementation of both single length and double length subtraction with either carry or borrow and single length and double length addition. The C_X input is intended to be connected to the Z output of the Am2903 to facilitate execution of some of the Am2903 special instructions. The C_0 pin is to be connected to the C_n pin of the least significant Am2901A or Am2903 and the C_n pin of the Am2902.

BLOCK DIAGRAM



MPR-060

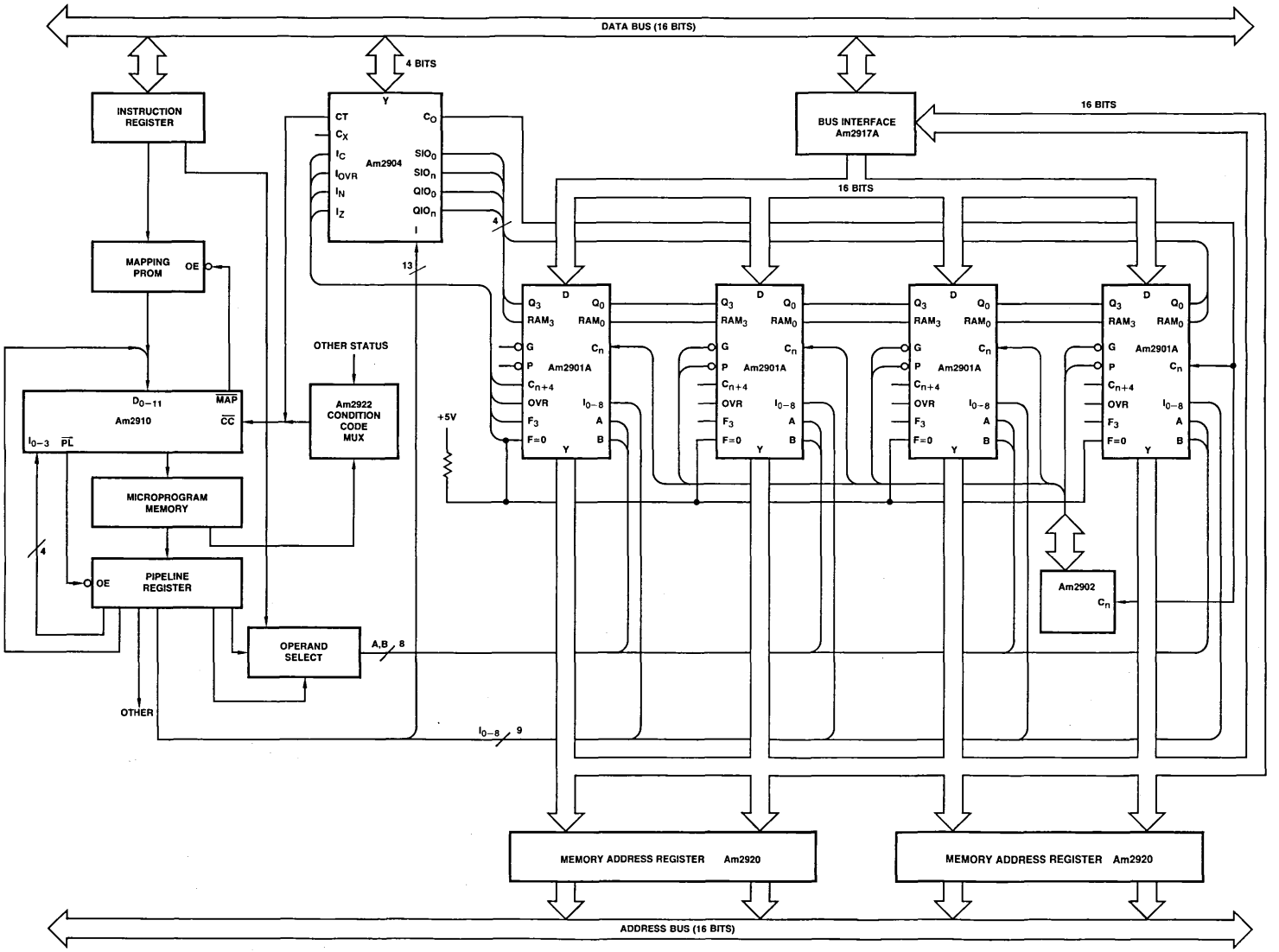


Figure 1. Typical Application of Am2904 with Am2901A.

MPR-061

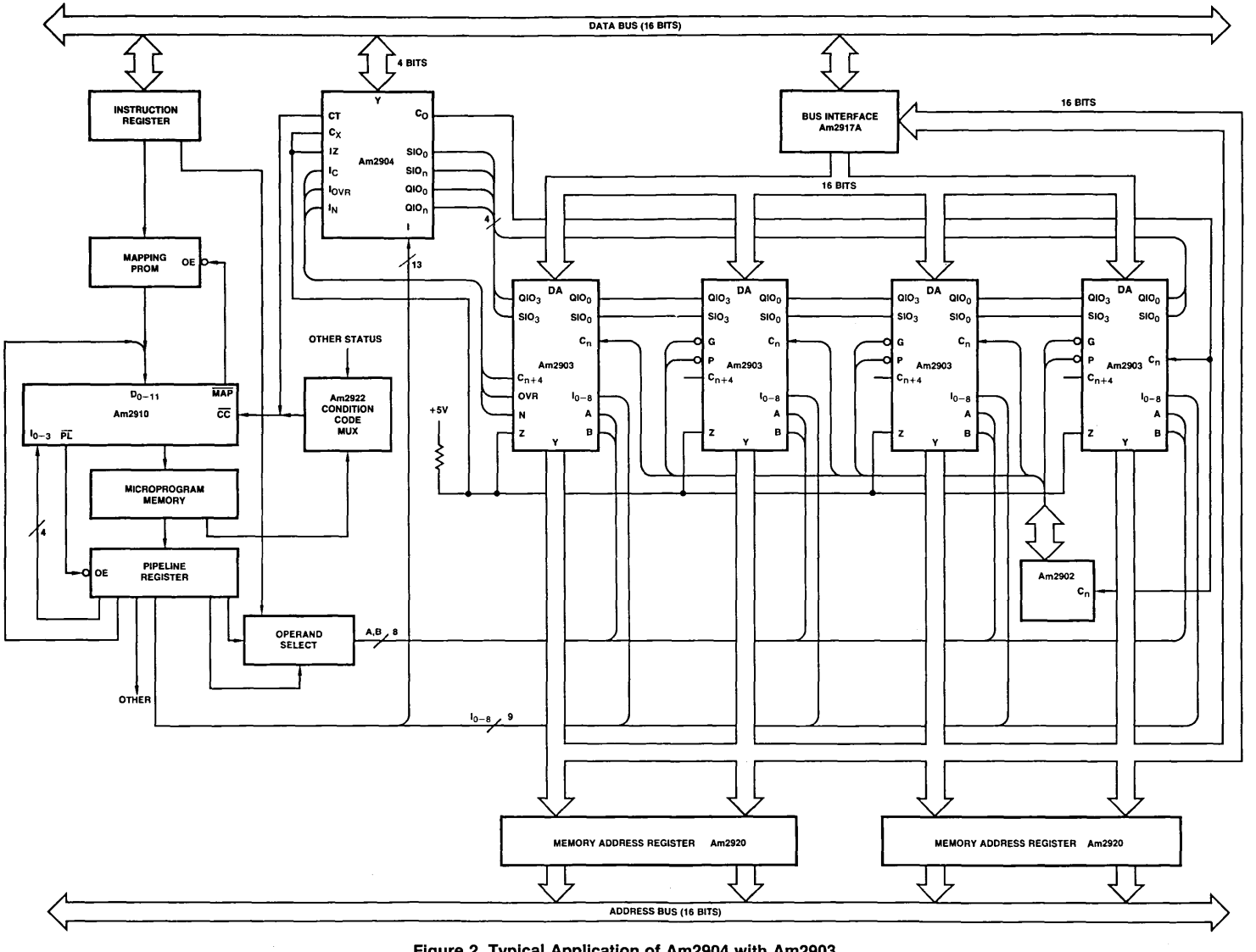


Figure 2. Typical Application of Am2904 with Am2903.

MPR-062

Am2905

Quad Two-Input OC Bus Transceiver With Three-State Receiver

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 100 mA at 0.8V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

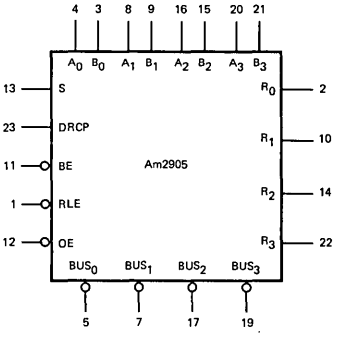
The Am2905 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

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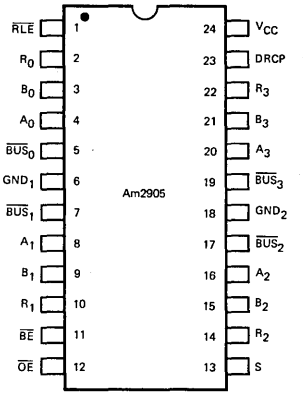
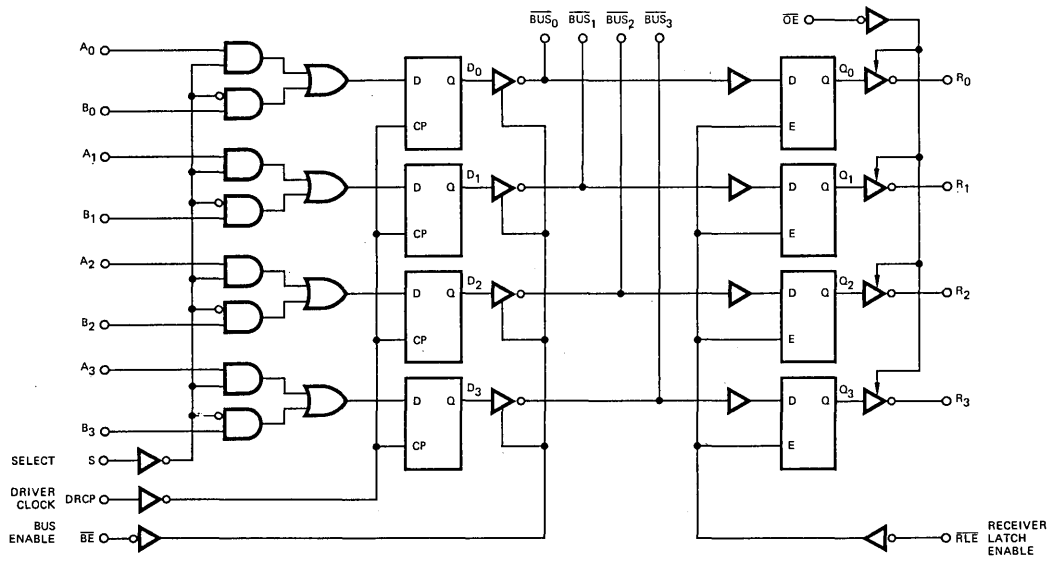
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-064

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	200mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2905XC (COM'L) T_A = 0°C to +70°C V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V
Am2905XM (MIL) T_A = −55°C to +125°C V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2905XC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2905XM MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

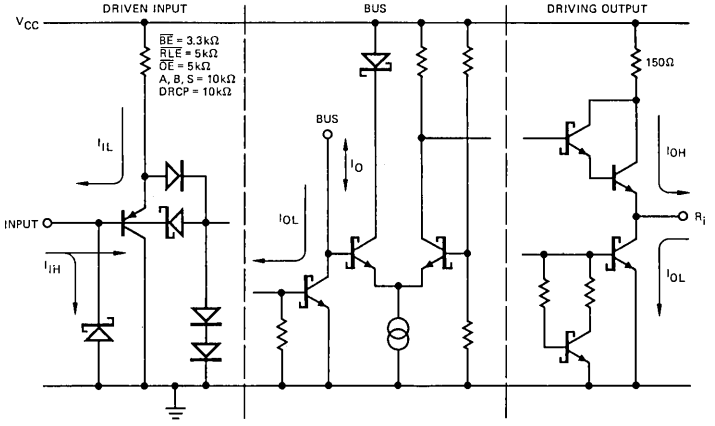
Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	$V_{CC} = V_{IN}$, $V_{IN} = V_{IL}$ or V_{IH}	MIL, $I_{OH} = -1.0$mA		2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6$mA		2.4	3.4		
V_{OL}	Receiver Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4mA			0.27	0.4	Volts
			I_{OL} = 8mA			0.32	0.45	
			I_{OL} = 12mA			0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA					−1.5	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4$V					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7$V					20	µA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 5.5$V					100	µA
I_O	Receiver Off-State Output Current	V_{CC} = MAX.		$V_O = 2.4$V			20	µA
				$V_O = 0.4$V			−20	
I_{SC}	Receiver Output Short Circuit Current	V_{CC} = MAX.			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All inputs = GND				69	105	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2905XM Min.	Am2905XM Typ. (Note 2)	Am2905XM Max.	Am2905XC Min.	Am2905XC Typ. (Note 2)	Am2905XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs (A or B)	C_L = 15pF, R_L = 2.0kΩ	25			23			ns
t_h			8.0			7.0			
t_s	Select Input (S)		33			30			ns
t_h			8.0			7.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enable)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{ZH}	Output Control to Receiver Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Receiver Output			14	28		14	25	ns
t_{LZ}				14	28		14	25	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0$V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

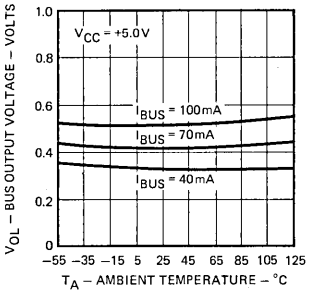


Note: Actual current flow direction shown.

MPR-066

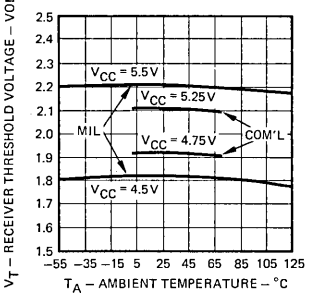
TYPICAL PERFORMANCE CURVES

Bus Output Low Voltage Versus Ambient Temperature



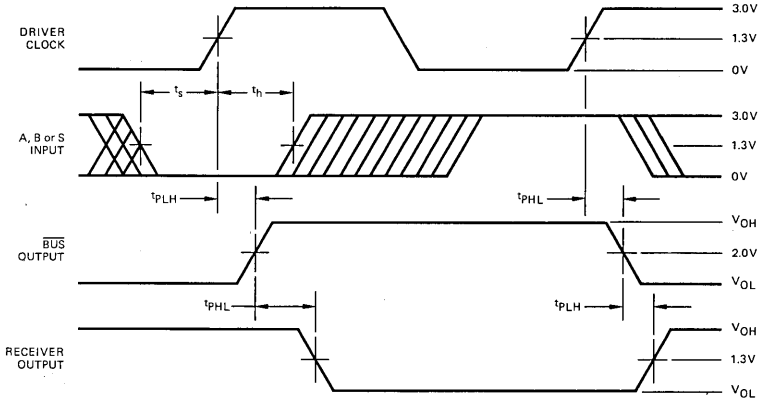
MPR-067

Receiver Threshold Variation Versus Ambient Temperature



MPR-068

SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

MPR-069

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2905PC	P-24	C	C-1
AM2905DC	D-24	C	C-1
AM2905DC-B	D-24	C	B-1
AM2905DM	D-24	M	C-3
AM2905DM-B	D-24	M	B-3
AM2905FM	F-24	M	C-3
AM2905FM-B	F-24	M	B-3
AM2905XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2905XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

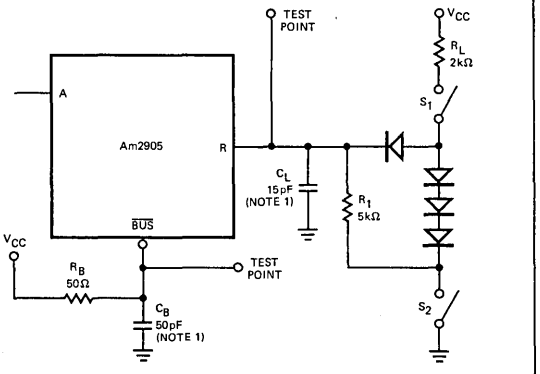
$\overline{BUS}_0$, $\overline{BUS}_1$ $\overline{BUS}_2$, $\overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

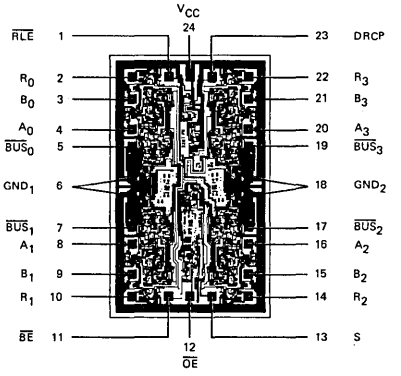
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

LOAD TEST CIRCUIT



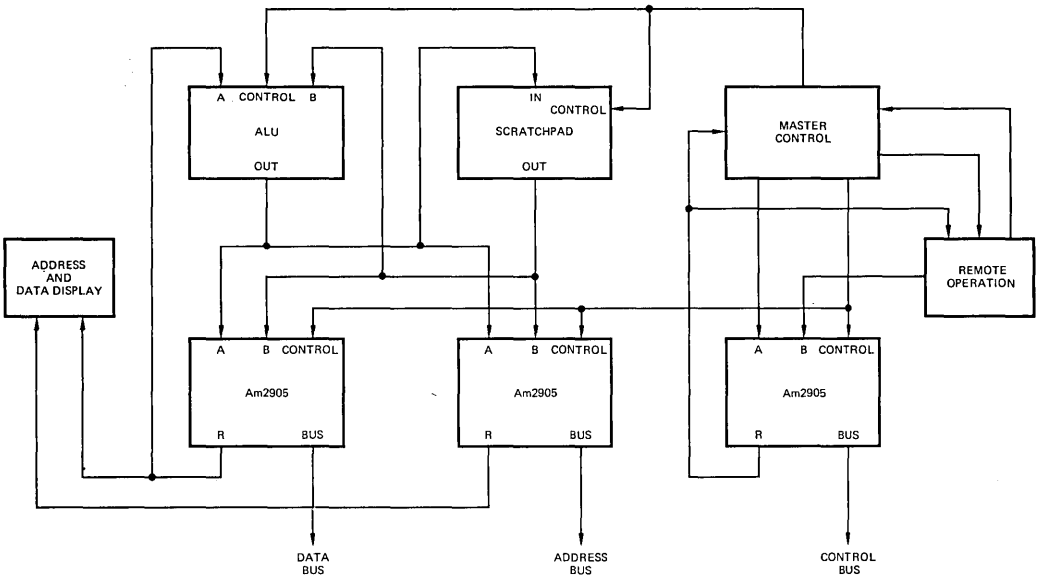
MPR-070

Metallization and Pad Layout



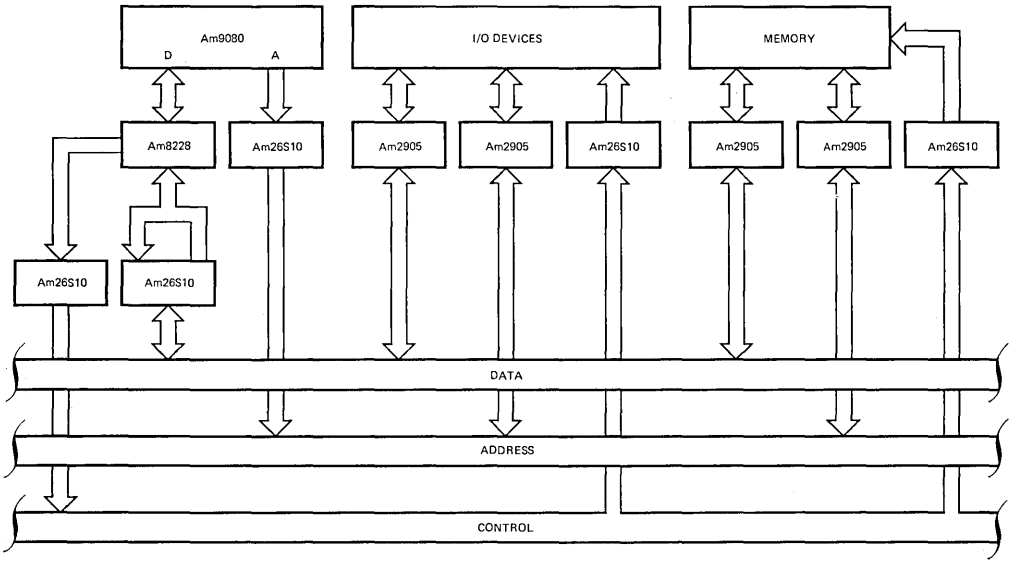
DIE SIZE 0.080" X 0.130"

APPLICATIONS



The Am2905 is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.

MPR-071



Using the Am2905 and Am26S10 in a terminated Bus system for the Am9080 MOS Microprocessor.

MPR-072

Am2906

Quad Two-Input OC Bus Transceiver With Parity

Distinctive Characteristics

- Quad high-speed LSI bus transceiver.
- Open-collector bus driver.
- Two-port input to D-type register on driver.
- Bus driver output can sink 100 mA at 0.8V max.
- Internal odd 4-bit parity checker/generator.
- Receiver has output latch for pipeline operation.
- Receiver outputs sink 12 mA.
- Advanced low-power Schottky processing.
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am2906 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

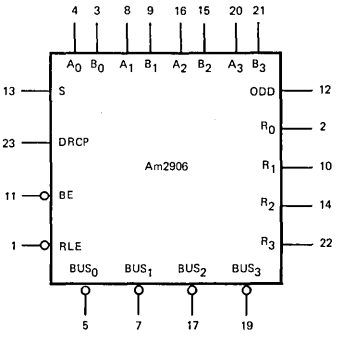
This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

The Am2906 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

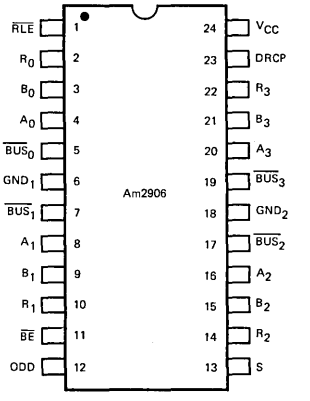
LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

MPR-073

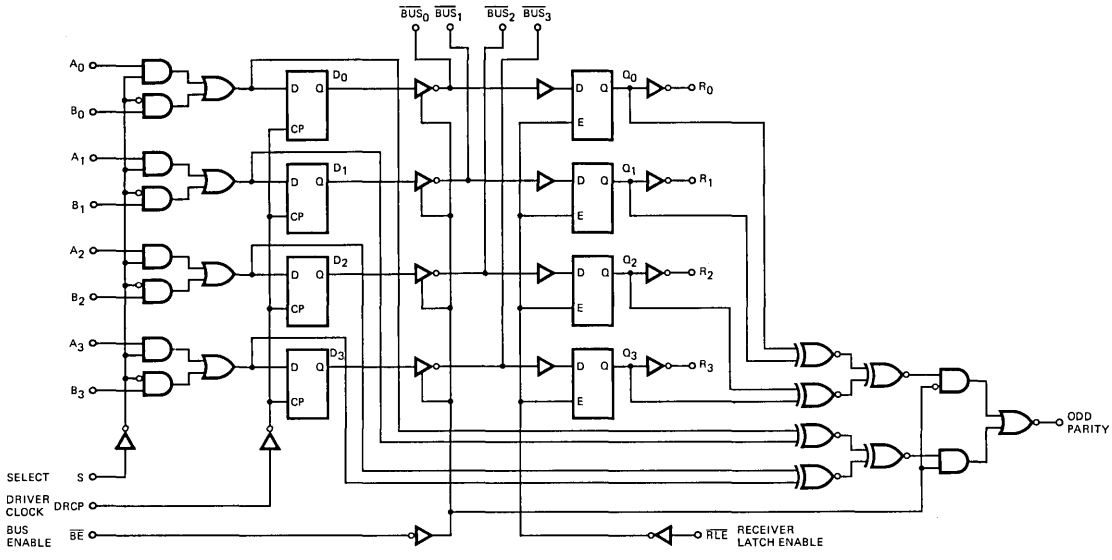
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-074

LOGIC DIAGRAM



MPR-075

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	200mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2906XC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2906XM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage		I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	μA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	μA
V_{TH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2906XC (COM'L)	$T_A = 0°C$ to $+70°C$	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
Am2906XM (MIL)	$T_A = -55°C$ to $+125°C$	V_{CC} MIN. 4.5V	V_{CC} MAX. = 5.5V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

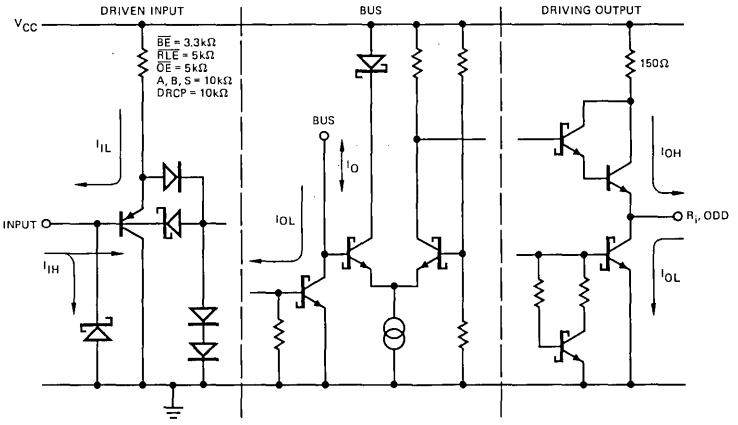
Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL	$I_{OH} = -1mA$	2.4	3.4		Volts
			COM'L	$I_{OH} = -2.6mA$	2.4	3.4		
	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu A$, $V_{IN} = V_{IH}$ or V_{IL}		MIL	2.5	3.4		
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 4mA$			0.27	0.4	Volts
			$I_{OL} = 8mA$			0.32	0.45	
			$I_{OL} = 12mA$			0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18mA$					−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 5.5V$					100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All inputs = GND				72	105	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2906XM Min.	Am2906XM Typ. (Note 2)	Am2906XM Max.	Am2906XC Min.	Am2906XC Typ. (Note 2)	Am2906XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L(BUS) = 50pF, R_L(BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	Data Inputs (A or B)	C_L = 15pF, R_L = 2.0kΩ	25			23			ns
t_h			8.0			7.0			
t_s	Select Inputs (S)		33			30			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

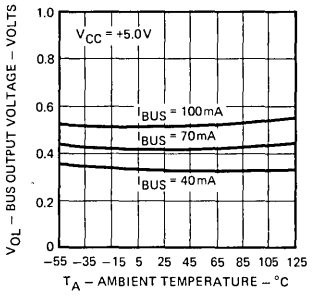


Note: Actual current flow direction shown.

MPR-076

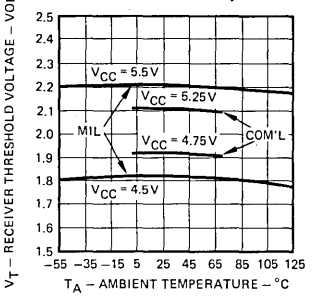
TYPICAL PERFORMANCE CURVES

Bus Output Low Voltage Versus Ambient Temperature



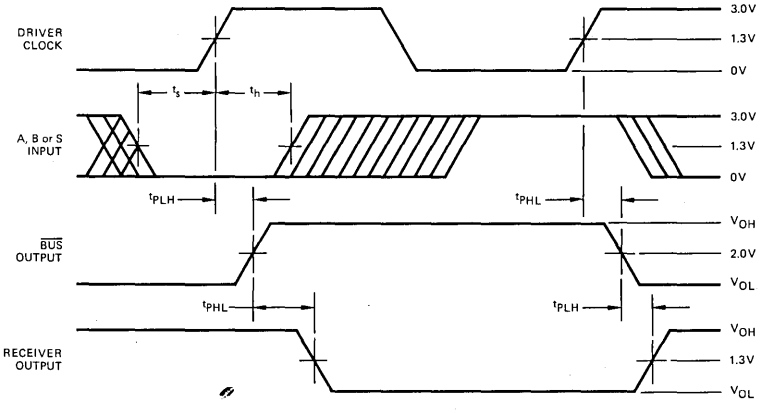
MPR-077

Receiver Threshold Variation Versus Ambient Temperature



MPR-078

SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

MPR-079

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2906PC	P-24	C	C-1
AM2906DC	D-24	C	C-1
AM2906DC-B	D-24	C	B-1
AM2906DM	D-24	M	C-3
AM2906DM-B	D-24	M	B-3
AM2906FM	F-24	M	C-3
AM2906FM-B	F-24	M	B-3
AM2906XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2906XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

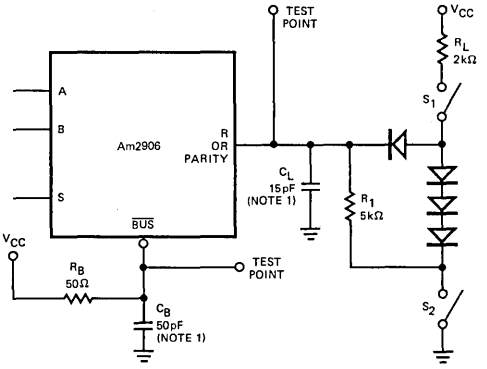
$\overline{BUS}_0, \overline{BUS}_1, \overline{BUS}_2, \overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

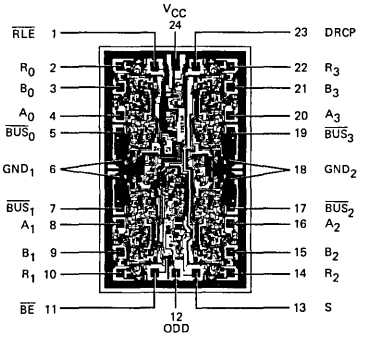
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

LOAD TEST CIRCUIT



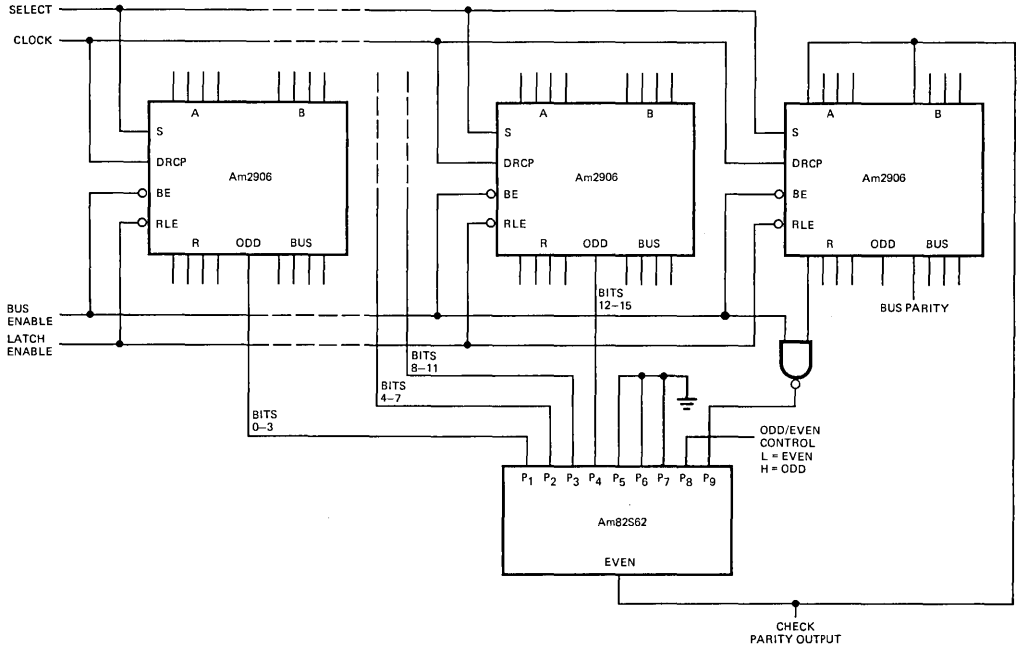
MPR-080

Metallization and Pad Layout



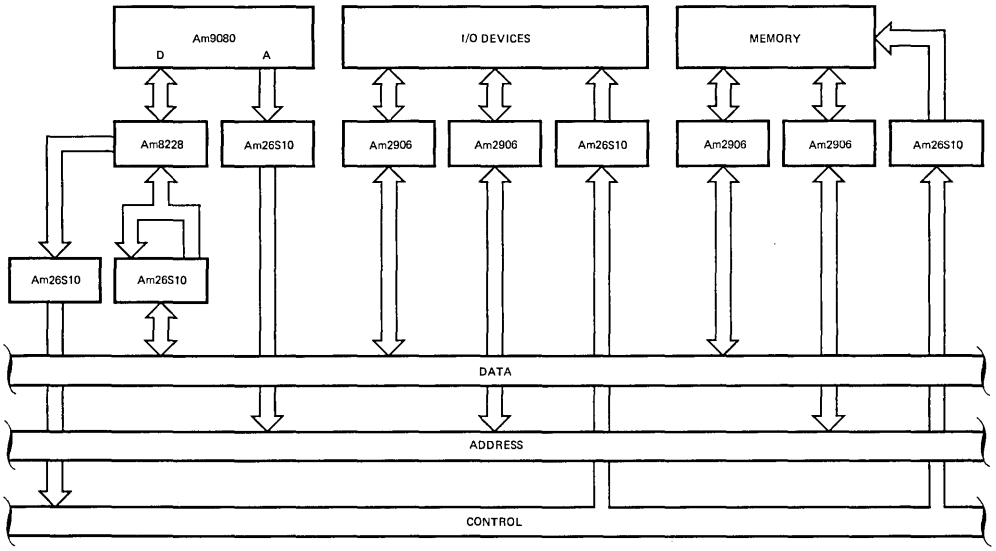
DIE SIZE 0.080" X 0.130"

APPLICATIONS



Generating or checking parity for 16 data bits.

MPR-081



Using the Am2906 and Am26S10 in a terminated Bus system for the Am9080 MOS Microprocessor.

MPR-082

Am2907

Quad Bus Transceiver With Three-State Receiver And Parity

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- D-type register on driver
- Bus driver output can sink 100 mA at 0.8 V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced Low-Power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2907 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

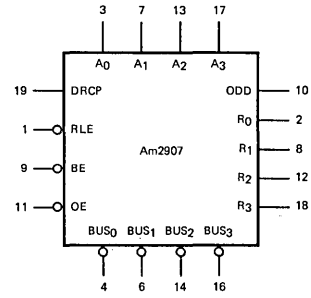
This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8 V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

The Am2907 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

LOGIC SYMBOL

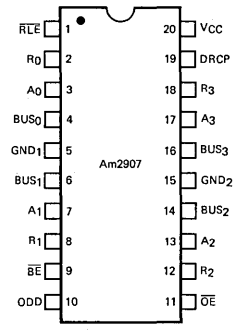


V_{CC} = Pin 20
GND_1 = Pin 5
GND_2 = Pin 15

MPR-083

CONNECTION DIAGRAMS
Top Views

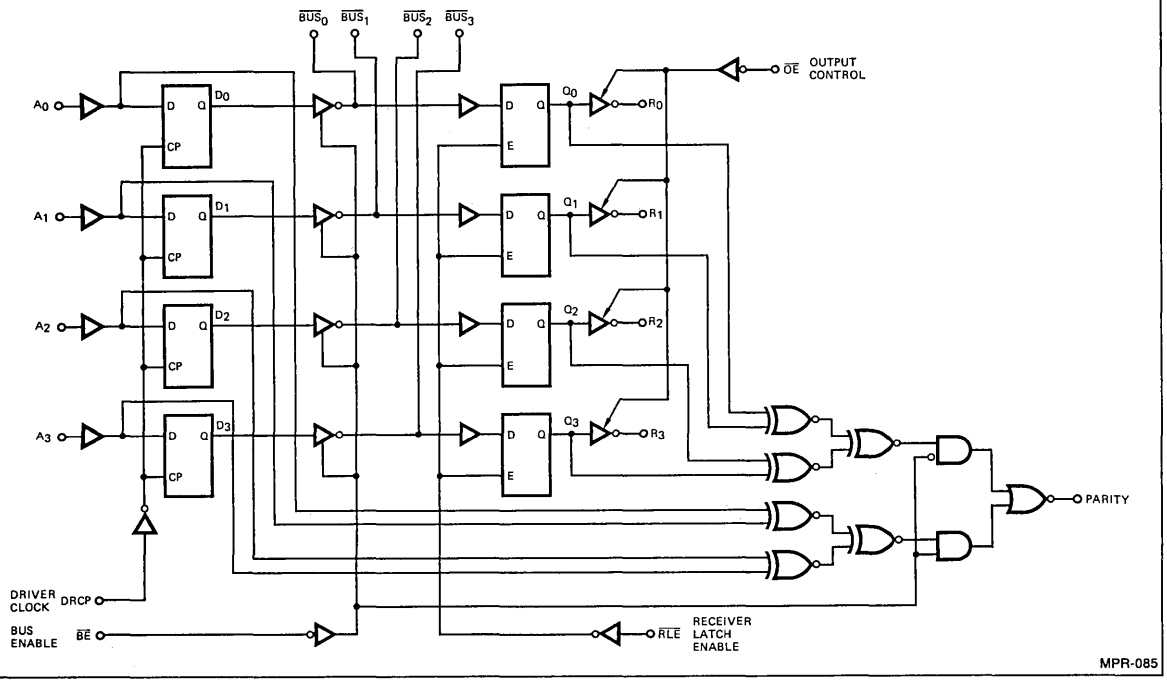
DIP



Note: Pin 1 is marked for orientation.

MPR-084

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	200 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2907XC (COM'L)	T_A = 0°C to +70°C	V_{CC} MIN. = 4.75V	V_{CC} MAX. = 5.25V
Am2907XM (MIL)	T_A = −55°C to +125°C	V_{CC} MIN. = 4.50V	V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 40mA			0.32	0.5	Volts
			I_{OL} = 70mA			0.41	0.7	
			I_{OL} = 100mA			0.55	0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	µA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5V					100	µA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4V		MIL	2.4	2.0		Volts
				COM'L	2.3	2.0		
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4V		MIL		2.0	1.5	Volts
				COM'L		2.0	1.6	

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2907XC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2907XM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

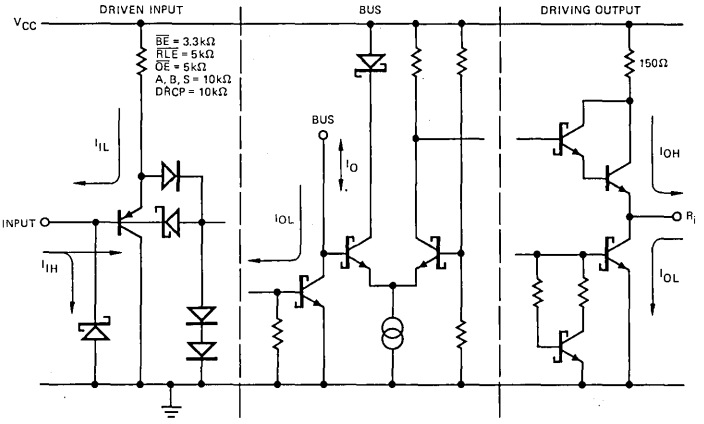
Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN. $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1mA$		2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6mA$		2.4	3.4		
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu A$ $V_{IN} = V_{IH}$ or V_{IL}		MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN. $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4mA			0.27	0.4	Volts
			I_{OL} = 8mA			0.32	0.45	
			I_{OL} = 12mA			0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18mA$					−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4$ V					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7$ V					20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 5.5$ V					100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.			−12		−65	mA
I_{CC}	Power Supply Current	V_{CC} = MAX., All Inputs = GND				75	110	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	$V_O = 2.4$ V				20	μA
			$V_O = 0.4$ V				−20	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2907XM Min.	Am2907XM Typ. (Note 2)	Am2907XM Max.	Am2907XC Min.	Am2907XC Typ. (Note 2)	Am2907XC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF R_L (BUS) = 50Ω		21	40		21	36	ns
t_{PLH}				21	40		21	36	
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{PLH}				13	26		13	23	
t_s	A Data Inputs	C_L = 15pF R_L = 2.0kΩ	25			23			ns
t_h			8.0			7.0			
t_{PW}	Clock Pulse Width (HIGH)		28			25			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	37		18	34	ns
t_{PHL}				18	37		18	34	
t_{PLH}	Latch Enable to Receiver Output			21	37		21	34	ns
t_{PHL}				21	37		21	34	
t_s	Bus to Latch Enable ($\overline{RLE}$)		21			18			ns
t_h			7.0			5.0			
t_{PLH}	A Data to Odd Parity Out (Driver Enabled)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	40		21	36	ns
t_{PHL}				21	40		21	36	
t_{ZH}	Output Control to Output			14	28		14	25	ns
t_{ZL}				14	28		14	25	
t_{HZ}	Output Control to Output	C_L = 5.0pF R_L = 2.0kΩ		14	28		14	25	ns
t_{LZ}				14	28		14	25	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

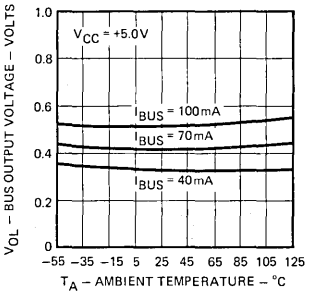


Note: Actual current flow direction shown.

MPR-086

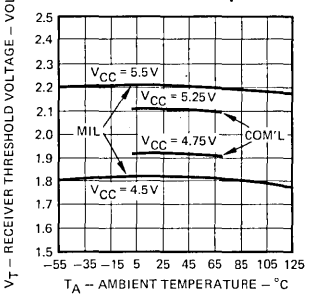
TYPICAL PERFORMANCE CURVES

Bus Output Low Voltage Versus Ambient Temperature



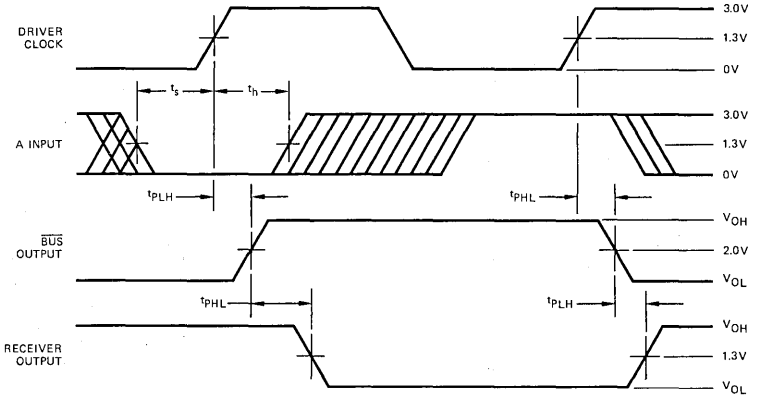
MPR-087

Receiver Threshold Variation Versus Ambient Temperature



MPR-088

SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

MPR-089

TRUTH TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	B_i	R_i	
X	X	H	X	X	X	X	H	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

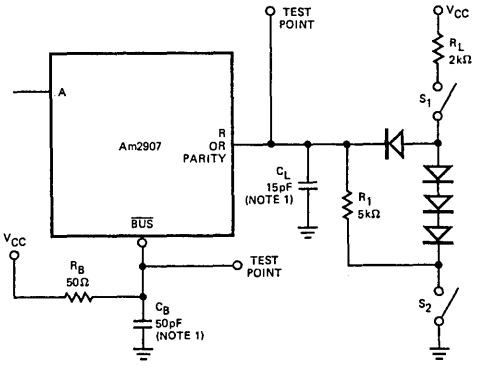
Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2907PC	P-20	C	C-1
AM2907DC	D-20	C	C-1
AM2907DC-B	D-20	C	B-1
AM2907DM	D-20	M	C-3
AM2907DM-B	D-20	M	B-3
AM2907FM	F-20	M	C-3
AM2907FM-B	F-20	M	B-3
AM2907XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2907XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

LOAD TEST CIRCUIT



MPR-090

DEFINITION OF FUNCTIONAL TERMS

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is LOW, the four drivers are in the high impedance state.

BUS_0, BUS_1, BUS_2, BUS_3 The four driver outputs and receiver inputs (data is inverted).

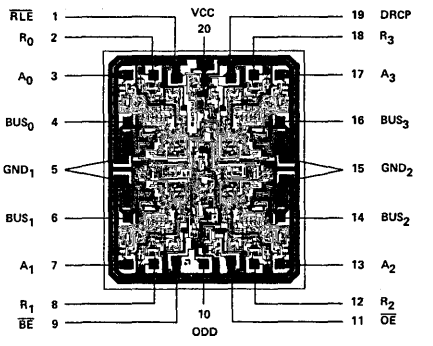
R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

ODD Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

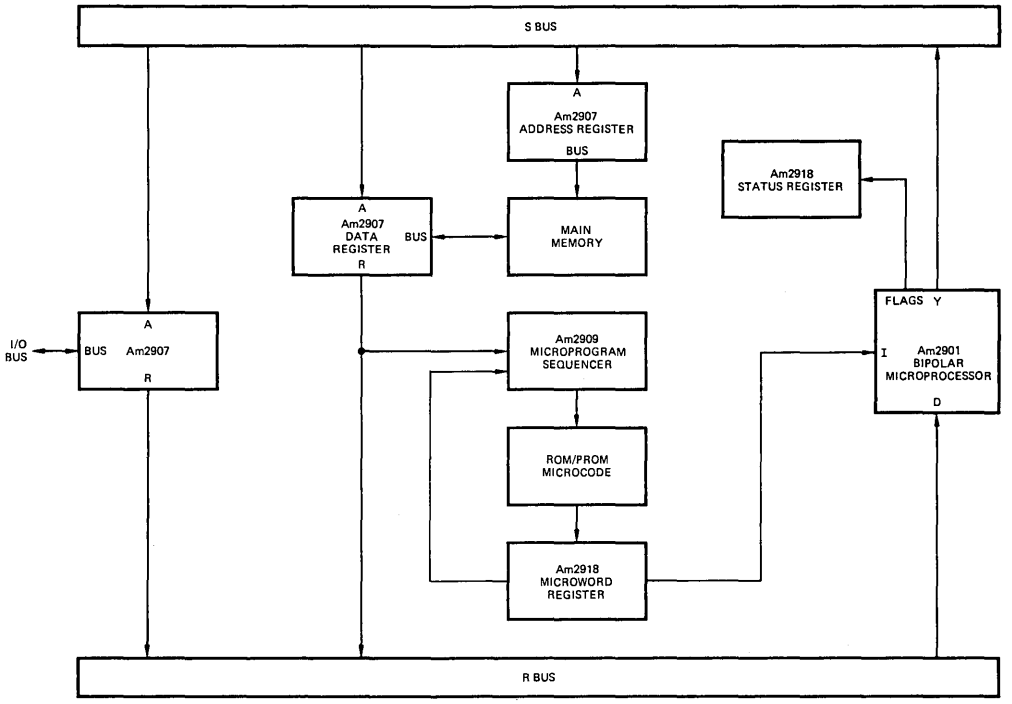
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

Metallization and Pad Layout



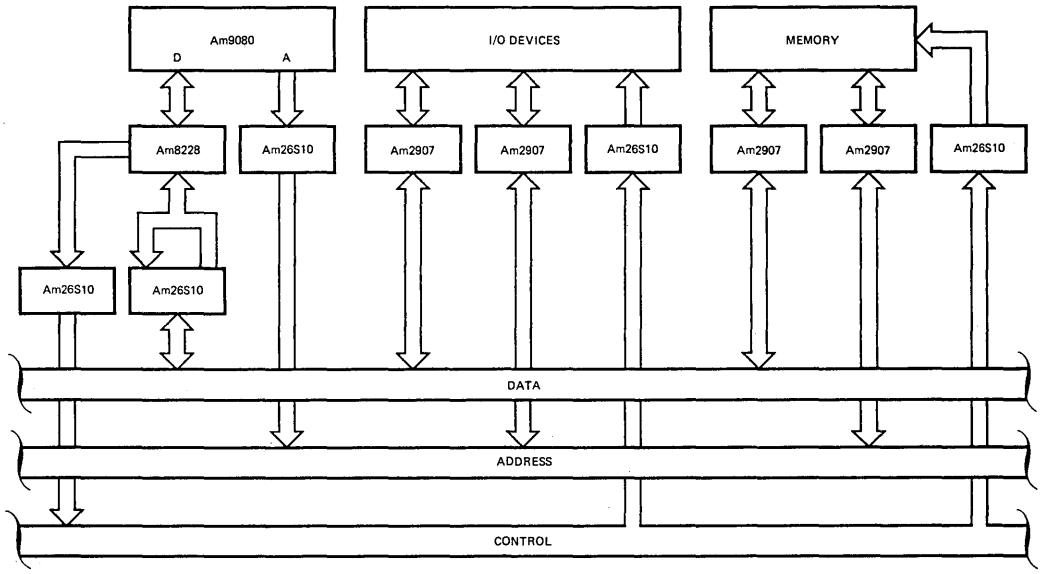
DIE SIZE 0.088" X 0.103"

APPLICATIONS



The Am2907 can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.

MPR-091



Using the Am2907 and Am26S10 in a terminated Bus system for the Am9080 MOS Microprocessor.

MPR-092

Am2909 • Am2911

Microprogram Sequencers

DISTINCTIVE CHARACTERISTICS

- 4-bit slice cascadable to any number of microwords
- Internal address register
- Branch input for N-way branches
- Cascadable 4-bit microprogram counter
- 4 x 4 file with stack pointer and push pop control for nesting microsubroutines.
- Zero input for returning to the zero microcode word
- Individual OR input for each bit for branching to higher microinstructions (Am2909 only).
- Three-state outputs
- All internal registers change state on the LOW-to-HIGH transition of the clock
- Am2909 in 28-pin package
- Am2911 in 20-pin package

GENERAL DESCRIPTION

The Am2909 is a four-bit wide address controller intended for sequencing through a series of microinstructions contained in a ROM or PROM. Two Am2909's may be interconnected to generate an eight-bit address (256 words), and three may be used to generate a twelve-bit address (4K words).

The Am2909 can select an address from any of four sources. They are: 1) a set of external direct inputs (D); 2) external data from the R inputs, stored in an internal register; 3) a four-word deep push/pop stack; or 4) a program counter register (which usually contains the last address plus one). The push/pop stack includes certain control lines so that it can efficiently execute nested subroutine linkages. Each of the four outputs can be OR'ed with an external input for conditional skip or branch instructions, and a separate line forces the outputs to all zeroes. The outputs are three-state.

The Am2911 is an identical circuit to the Am2909, except the four OR inputs are removed and the D and R inputs are tied together. The Am2911 is in a 20-pin, 0.3" centers package.

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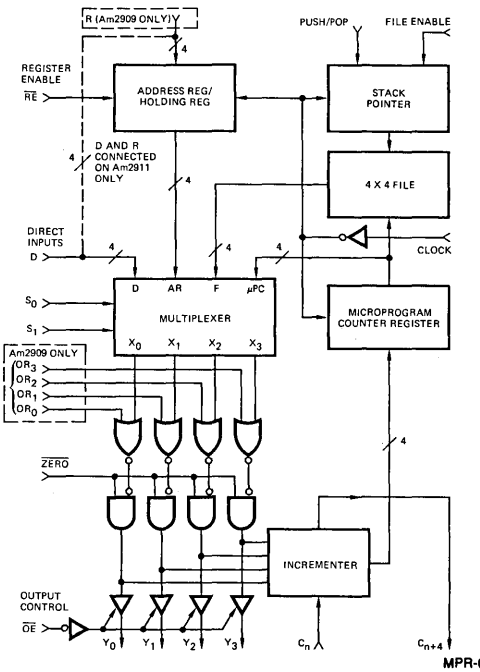
MICROPROGRAM SEQUENCER BLOCK DIAGRAM



ARCHITECTURE OF THE Am2909/Am2911

The Am2909/Am2911 are bipolar microprogram sequencers intended for use in high-speed microprocessor applications. The device is a cascadable 4-bit slice such that two devices allow addressing of up to 256-words of microprogram and three devices allow addressing of up to 4K words of microprogram. A detailed logic diagram is shown in Figure 2.

The device contains a four-input multiplexer that is used to select either the address register, direct inputs, microprogram counter, or file as the source of the next microinstruction address. This multiplexer is controlled by the S_0 and S_1 inputs.

The address register consists of four D-type, edge triggered flip-flops with a common clock enable. When the address register enable is LOW, new data is entered into the register on the clock LOW-to-HIGH transition. The address register is available at the multiplexer as a source for the next microinstruction address. The direct input is a four-bit field of inputs to the multiplexer and can be selected as the next microinstruction address. On the Am2911, the direct inputs are also used as inputs to the register. This allows an N-way branch where N is any word in the microcode.

The Am2909/Am2911 contains a microprogram counter (μPC) that is composed of a 4-bit incrementer followed by a 4-bit register. The incrementer has carry-in (C_n) and carry-out (C_{n+4}) such that cascading to larger word lengths is straightforward. The μPC can be used in either of two ways. When the least significant carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one (Y+1→μPC.) Thus sequential microinstructions can be executed. If this least significant C_n is LOW, the incrementer passes the Y output word unmodified and the microprogram register is loaded with the same Y word on the next clock cycle (Y→μPC). Thus, the same microinstruction can be executed any number of times by using the least significant C_n as the control.

The last source available at the multiplexer input is the 4 x 4 file (stack). The file is used to provide return address linkage when executing microsubroutines. The file contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a push or pop.

The stack pointer operates as an up/down counter with separate push/pop and file enable inputs. When the file enable input is LOW and the push/pop input is HIGH, the PUSH operation is enabled. This causes the stack pointer to increment and the file to be written with the required return linkage — the next microinstruction address following the subroutine jump which initiated the PUSH.

If the file enable input is LOW and the push/pop control is LOW, a POP operation occurs. This implies the usage of the return linkage during this cycle and thus a return from subroutine. The next LOW-to-HIGH clock transition causes the stack pointer to decrement. If the file enable is HIGH, no action is taken by the stack pointer regardless of any other input.

The stack pointer linkage is such that any combination of pushes, pops or stack references can be achieved. One microinstruction subroutines can be performed. Since the stack is 4 words deep, up to four microsubroutines can be nested.

The ZERO input is used to force the four outputs to the binary zero state. When the ZERO input is LOW, all Y outputs are LOW regardless of any other inputs (except $\overline{OE}$). Each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output. This allows jumping to different microinstructions on programmed conditions.

The Am2909/Am2911 feature three-state Y outputs. These can be particularly useful in military designs requiring external Ground Support Equipment (GSE) to provide automatic checkout of the microprocessor. The internal control can be placed in the high-impedance state, and preprogrammed sequences of microinstructions can be executed via external access to the control ROM/PROM.

ORDERING INFORMATION

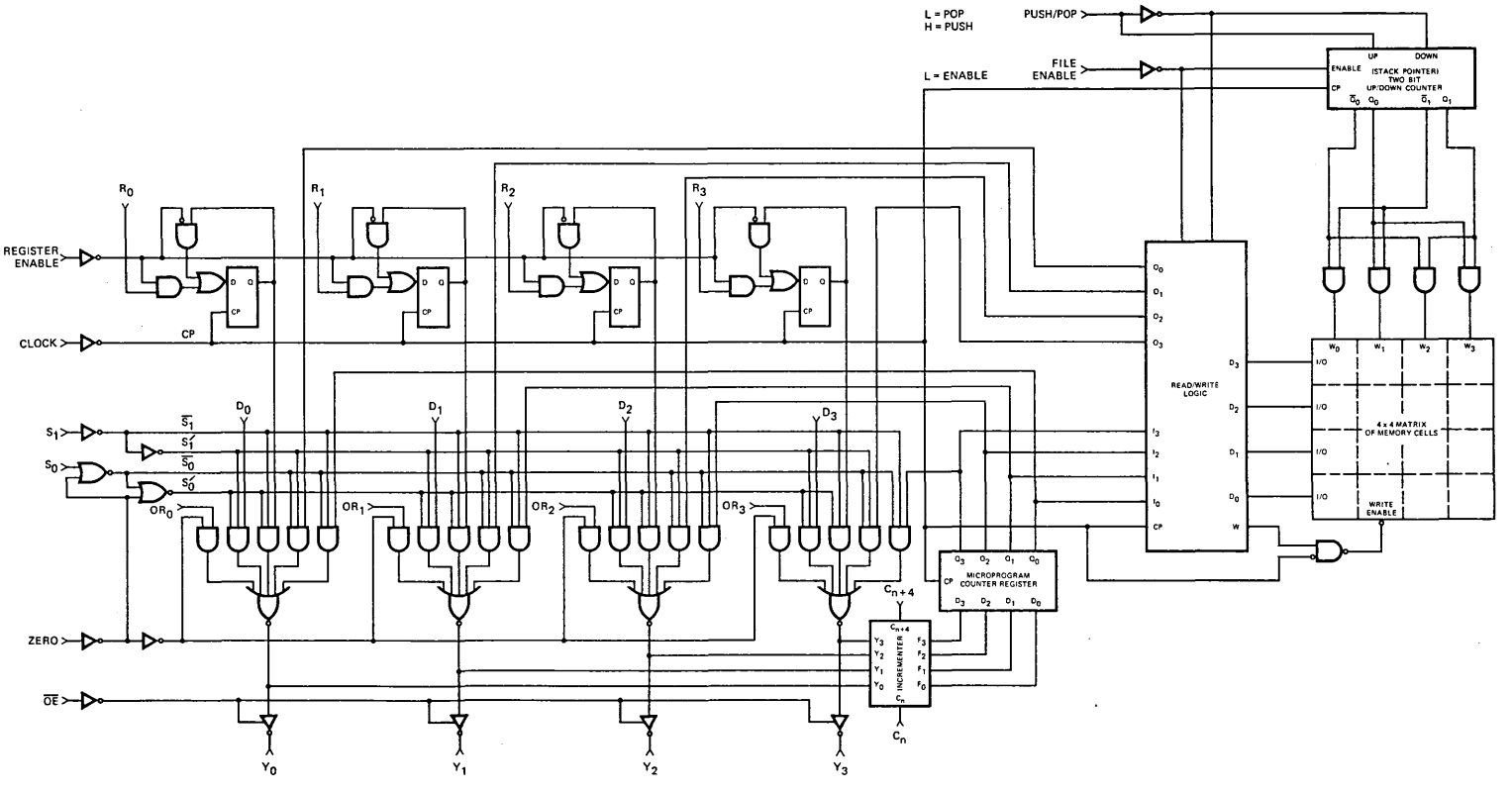
Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2911PC	P-20	C	C-1
AM2911DC	D-20	C	C-1
AM2911DC-B	D-20	C	B-1
AM2911DM	D-20	M	C-3
AM2911DM-B	D-20	M	B-3
AM2911XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2911XM	Dice	M	

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2909PC	P-28	C	C-1
AM2909DC	D-28	C	C-1
AM2909DC-B	D-28	C	B-1
AM2909DM	D-28	M	C-3
AM2909DM-B	D-28	M	B-3
AM2909FM	F-28	M	C-3
AM2909FM-B	F-28	M	B-3
AM2909XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2909XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Figure 1.



Note: R_i and D_i connected together on Am2911 and OR_i removed.

Figure 2. Microprogram Sequencer Block Diagram.

MPR-094

DEFINITION OF TERMS

A set of symbols is used in this data sheet to represent various internal and external registers and signals used with the Am2909. Since its principle application is as a controller for a microprogram store, it is necessary to define some signals associated with the microcode itself. Figure 3 illustrates the basic interconnection of Am2909, memory, and microinstruction register. The definitions here apply to this architecture.

Inputs to Am2909/Am2911

S_1, S_0	Control lines for address source selection
$\overline{FE}$, PUP	Control lines for push/pop stack
$\overline{RE}$	Enable line for internal address register
OR_i	Logic OR inputs on each address output line
$\overline{ZERO}$	Logic AND input on the output lines
$\overline{OE}$	Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high impedance)
C_n	Carry-in to the incrementer
R_i	Inputs to the internal address register
D_i	Direct inputs to the multiplexer
CP	Clock input to the AR and μPC register and Push-Pop stack

Outputs from the Am2909/Am2911

Y_i	Address outputs from Am2909. (Address inputs to control memory.)
C_{n+4}	Carry out from the incrementer

Internal Signals

μPC	Contents of the microprogram counter
REG	Contents of the register
STK0-STK3	Contents of the push/pop stack. By definition, the word in the four-by-four file, addressed by the stack pointer is STK0. Conceptually data is pushed into the stack at STK0; a subsequent push moves STK0 to STK1; a pop implies STK3 → STK2 → STK1 → STK0. Physically, only the stack pointer changes when a push or pop is performed. The data does not move. I/O occurs at STK0.
SP	Contents of the stack pointer

External to the Am2909/Am2911

A	Address to the control memory
I(A)	Instruction in control memory at address A
μWR	Contents of the microword register (at output of control memory). The microword register contains the instruction currently being executed.
T_n	Time period (cycle) n

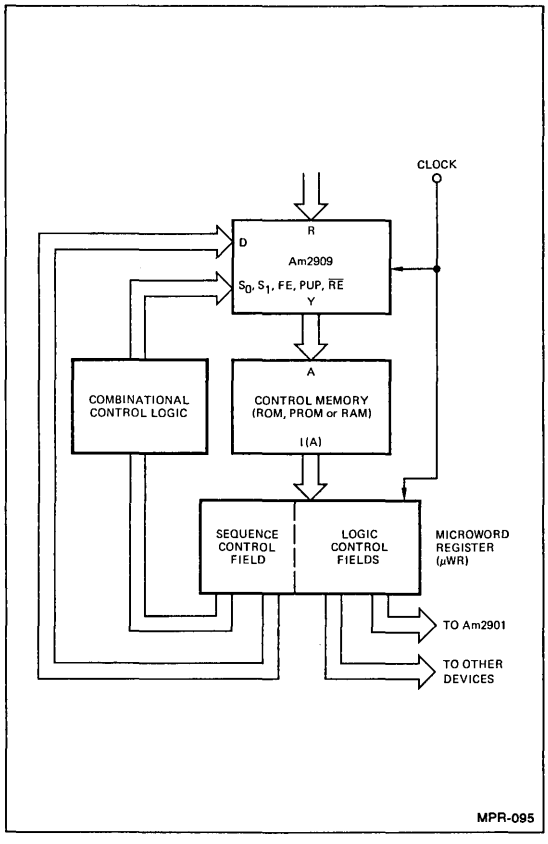


Figure 3. Microprogram Sequencer Control.

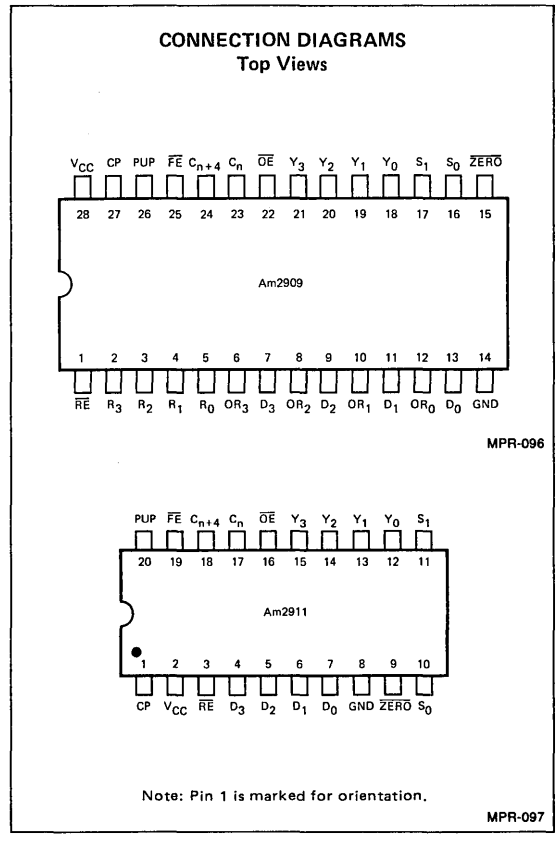


Figure 4.

OPERATION OF THE Am2909/Am2911

Figure 5 lists the select codes for the multiplexer. The two bits applied from the microword register (and additional combinational logic for branching) determine which data source contains the address for the next microinstruction. The contents of the selected source will appear on the Y outputs. Figure 5 also shows the truth table for the output control and for the control of the push/pop stack. Figure 6 shows in detail the effect of S_0, S_1, $\overline{FE}$ and PUP on the Am2909. These four signals define what address appears on the Y outputs and what the state of all the internal registers will be following the clock LOW-to-HIGH edge. In this illustration, the microprogram counter is assumed to contain initially some word J, the address register some word K, and the four words in the push/pop stack contain R_a through R_d.

Address Selection

OCTAL	S_1	S_0	SOURCE FOR Y OUTPUTS	SYMBOL
0	L	L	Microprogram Counter	μPC
1	L	H	Register	REG
2	H	L	Push-Pop stack	STK0
3	H	H	Direct inputs	D_i

Output Control

OR_i	$\overline{ZERO}$	$\overline{OE}$	Y_i
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Z = High Impedance

Synchronous Stack Control

$\overline{FE}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

H = High
L = Low
X = Don't Care

Figure 5.

CYCLE	S_1, S_0, $\overline{FE}$, PUP	μPC	REG	STK0	STK1	STK2	STK3	Y_{OUT}	COMMENT	PRINCIPLE USE
N	0 0 0 0	J	K	Ra	Rb	Rc	Rd	J	Pop Stack	End Loop
N+1	–	J+1	K	Rb	Rc	Rd	Ra	–		
N	0 0 0 1	J	K	Ra	Rb	Rc	Rd	J	Push μPC	Set-up Loop
N+1	–	J+1	K	J	Ra	Rb	Rc	–		
N	0 0 1 X	J	K	Ra	Rb	Rc	Rd	J	Continue	Continue
N+1	–	J+1	K	Ra	Rb	Rc	Rd	–		
N	0 1 0 0	J	K	Ra	Rb	Rc	Rd	K	Pop Stack; Use AR for Address	End Loop
N+1	–	K+1	K	Rb	Rc	Rd	Ra	–		
N	0 1 0 1	J	K	Ra	Rb	Rc	Rd	K	Push μPC; Jump to Address in AR	JSR AR
N+1	–	K+1	K	J	Ra	Rb	Rc	–		
N	0 1 1 X	J	K	Ra	Rb	Rc	Rd	K	Jump to Address in AR	JMP AR
N+1	–	K+1	K	Ra	Rb	Rc	Rd	–		
N	1 0 0 0	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0; Pop Stack	RTS
N+1	–	Ra+1	K	Rb	Rc	Rd	Ra	–		
N	1 0 0 1	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0; Push μPC	
N+1	–	Ra+1	K	J	Ra	Rb	Rc	–		
N	1 0 1 X	J	K	Ra	Rb	Rc	Rd	Ra	Jump to Address in STK0	Stack Ref (Loop)
N+1	–	Ra+1	K	Ra	Rb	Rc	Rd	–		
N	1 1 0 0	J	K	Ra	Rb	Rc	Rd	D	Pop Stack; Jump to Address on D	End Loop
N+1	–	D+1	K	Rb	Rc	Rd	Ra	–		
N	1 1 0 1	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D; Push μPC	JSR D
N+1	–	D+1	K	J	Ra	Rb	Rc	–		
N	1 1 1 X	J	K	Ra	Rb	Rc	Rd	D	Jump to Address on D	JMP D
N+1	–	D+1	K	Ra	Rb	Rc	Rd	–		

X = Don't care, 0 = LOW, 1 = HIGH, Assume C_n = HIGH
Note: STK0 is the location addressed by the stack pointer.

Figure 6. Output and Internal Next-Cycle Register States for Am2909/Am2911.

Figure 7 illustrates the execution of a subroutine using the Am2909. The configuration of Figure 3 is assumed. The instruction being executed at any given time is the one contained in the microword register (μWR). The contents of the μWR also controls (indirectly, perhaps) the four signals S_0, S_1, $\overline{FE}$, and PUP. The starting address of the subroutine is applied to the D inputs of the Am2909 at the appropriate time.

In the columns on the left is the sequence of microinstructions to be executed. At address J+2, the sequence control portion of the microinstruction contains the comand "Jump to subroutine at A". At the time T_2, this instruction is in the μWR, and the Am2909 inputs are set-up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I(A), is accessed and is at the inputs of the μWR. On the next clock transition, I(A) is loaded into the μWR for execution, and the return address J+3 is pushed onto the stack. The return instruction is executed at T_5. Figure 8 is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

CONTROL MEMORY

Execute Cycle	Microprogram	
	Address	Sequencer Instruction
	J−1	–
T_0	J	–
T_1	J+1	–
T_2	J+2	JSR A
T_6	J+3	–
T_7	J+4	–
	–	–
	–	–
	–	–
	–	–
	–	–
T_3	A	I(A)
T_4	A+1	–
T_5	A+2	RTS
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock											
Signals											
Am2909 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	J+4	J+5		
	STK0	–	–	–	J+3	J+3	J+3	–	–		
	STK1	–	–	–	–	–	–	–	–		
	STK2	–	–	–	–	–	–	–	–		
	STK3	–	–	–	–	–	–	–	–		
Am2909 Output	Y	J+1	J+2	A	A+1	A+2	J+3	J+4	J+5		
ROM Output	(Y)	I(J+1)	JSR A	I(A)	I(A+1)	RTS	I(J+3)	I(J+4)	I(J+5)		
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	JSR A	I(A)	I(A+1)	RTS	I(J+3)	I(J+4)		

Figure 7. Subroutine Execution.

C_n = HIGH

CONTROL MEMORY

Execute Cycle	Microprogram	
	Address	Sequencer Instruction
	J−1	–
T_0	J	–
T_1	J+1	–
T_2	J+2	JSR A
T_9	J+3	–
	–	–
	–	–
	–	–
	–	–
T_3	A	–
T_4	A+1	–
T_5	A+2	JSR B
T_7	A+3	–
T_8	A+4	RTS
	–	–
	–	–
	–	–
	–	–
T_6	B	RTS
	–	–
	–	–

Execute Cycle		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
Clock											
Signals											
Am2909 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	μPC	J+1	J+2	J+3	A+1	A+2	A+3	B+1	A+4	A+5	J+4
	STK0	–	–	–	J+3	J+3	J+3	A+3	J+3	J+3	–
	STK1	–	–	–	–	–	–	J+3	–	–	–
	STK2	–	–	–	–	–	–	–	–	–	–
	STK3	–	–	–	–	–	–	–	–	–	–
Am2909 Output	Y	J+1	J+2	A	A+1	A+2	B	A+3	A+4	J+3	J+4
ROM Output	(Y)	I(J+1)	JSR A	I(A)	I(A+1)	JSR B	RTS	I(A+3)	RTS	I(J+3)	I(J+4)
Contents of μWR (Instruction being executed)	μWR	I(J)	I(J+1)	JSR A	I(A)	I(A+1)	JSR B	RTS	I(A+3)	RTS	I(J+3)

Figure 8. Two Nested Subroutines. Routine B is Only One Instruction.

C_n = HIGH

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

OPERATING RANGE

P/N	Ambient Temperature	V_{CC}
Am2909/2911DC, PC	0°C to +70°C	4.75V to 5.25V
Am2909/2911DM, FM	−55°C to +125°C	4.50V to 5.50V

STANDARD SCREENING

(Conforms to MIL-STD-883 for Class C Parts)

Step	MIL-STD-883 Method	Conditions	Level	
			Am2909/Am2911PC, DC	Am2909/Am2911DM, FM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C 24-hour 150°C	100%	100%
Temperature Cycle	1010	C −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B 10,000 G	100% *	100%
Fine Leak	1014	A 5×10^{-8} atm-cc/sec	100% *	100%
Gross Leak	1014	C2 Fluorocarbon	100% *	100%
Electrical Test Subgroups 1 and 7	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening here for Class B Parts				
Group A Sample Tests	5005	See below for definitions of subgroups		
Subgroup 1			LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 7
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 7

*Not applicable for Am2909PC or Am2911PC.

ADDITIONAL SCREENING FOR CLASS B PARTS

Step	MIL-STD-883 Method	Conditions	Level
			Am2909/Am2911DMB, FMB
Burn-In	1015	D 125°C 160 hours min.	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

GROUP A SUBGROUPS

(as defined in MIL-STD-883, method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum rated temperature
3	DC	Minimum rated temperature
7	Function	25°C
8	Function	Maximum and minimum rated temperature
9	Switching	25°C
10	Switching	Maximum Rated Temeperature
11	Switching	Minimum Rated Temperature

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL	I_{OH} = −1.0mA	2.4			Volts
			COM'L	I_{OH} = −2.6mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA (Note 5)				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	C_n				−1.08	mA
			Push/Pop, $\overline{OE}$				−0.72	
			Others (Note 6)				−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	C_n				40	µA
			Push/Pop				40	
			Others (Note 6)				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V	C_n, Push/Pop				0.2	mA
			Others (Note 6)				0.1	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		$Y_0 - Y_3$	−30		−100	mA
				C_{n+4}	−30		−85	
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)				80	130	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX., $\overline{OE}$ = 2.7V	V_{OUT} = 0.4V				−20	µA
I_{OZH}			V_{OUT} = 2.7V				20	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Apply GND to C_n, R_0, R_1, R_2, R_3, OR_0, OR_1, OR_2, OR_3, D_0, D_1, D_2, and D_3. Other inputs open. All outputs open. Measured after a LOW-to-HIGH clock transition.
5. The 12mA guarantee applies only to Y_0, Y_1, Y_2 and Y_3.
6. For the Am2911, D_i and R_i are internally connected. Loading is doubled (to same values as Push/Pop).

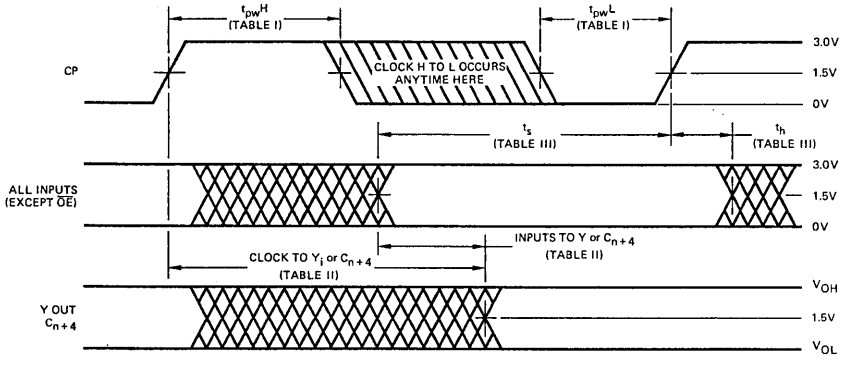


Figure 12. Switching Waveforms. See Tables for Specific Values.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Tables I, II, and III below define the timing characteristics of the Am2909 and Am2911 over the operating voltage and temperature range. The tables are divided into three types of parameters; clock characteristics, combinational delays from inputs to outputs, and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level.

TABLE I
CYCLE TIME AND CLOCK CHARACTERISTICS

TIME	COMMERCIAL	MILITARY
Minimum Clock LOW Time	30	35
Minimum Clock HIGH Time	30	35

TABLE II
MAXIMUM COMBINATIONAL PROPAGATION DELAYS
(all in ns, C_L = 50pF (except output disable tests))

From Input	COMMERCIAL		MILITARY	
	Y	C_{n+4}	Y	C_{n+4}
D_i	17	30	20	32
S_0, S_1	30	48	40	50
OR_i	17	30	20	32
C_n	–	14	–	16
$\overline{ZERO}$	30	48	40	50
$\overline{OE}$ LOW (enable)	25	–	25	–
$\overline{OE}$ HIGH (disable)	25	–	25	–
Clock ↑ S_1S_0 = LH	43	55	50	62
Clock ↑ S_1S_0 = LL	43	55	50	62
Clock ↑ S_1S_0 = HL	80	95	90	102

Operating Range	Part Numbers	Power Supply	Temperature Range
Commercial	Am2909PC, DC Am2911PC, DC	5.0V ± 5%	T_A = 0°C to +70°C
Military	Am2909DM, FM Am2911DM	5.0V ± 10%	T_C = −55°C to +125°C

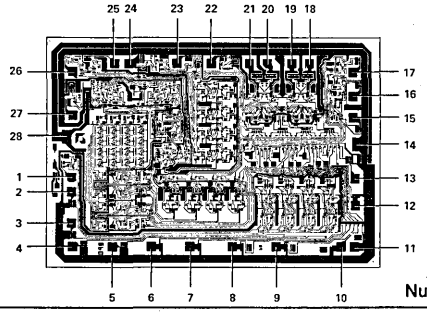
TABLE III
GUARANTEED SET-UP AND HOLD TIMES (all in ns) (Note 1)

From Input	Notes	COMMERCIAL		MILITARY	
		Set-Up Time	Hold Time	Set-Up Time	Hold Time
$\overline{RE}$		22	5	22	5
R_i	2	10	5	12	5
PUSH/POP		26	6	30	7
$\overline{FE}$		26	5	30	5
C_n		28	5	30	5
D_i	2	30	0	35	3
OR_i		30	0	35	3
S_0, S_1		45	0	50	0
$\overline{ZERO}$		45	0	50	0

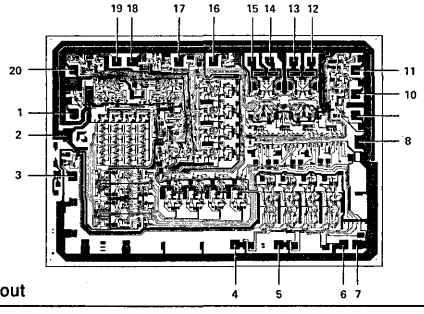
Notes: 1. All times relative to clock LOW-to-HIGH transition.
2. On Am2911, R_i and D_i are internally connected together and labeled D_i. Use R_i set-up and hold times when D inputs are used to load register.

Metallization and Pad Layout

Am2909



Am2911



DIE SIZE 0.110" X 0.160"
Numbers correspond to DIP pin-out

USING THE Am2909 AND Am2911

The Am2909 and Am2911 are four-bit slice sequencers which are cascaded to form a microprogram memory address generator. Both products make available to the user several lines which are used to directly control the internal holding register, multiplexer and stack. By appropriate control of these lines, the user can implement any desired set of sequence control functions; by cascading parts he can generate any desired address length. These two qualities set the Am2909 and Am2911 apart from the Am2910, which is architecturally similar, but is fixed at 12 bits in length and has a fixed set of 16 sequence control instructions. The Am2909 or Am2911 should be selected instead of the Am2910 under the following conditions:

- Address less than 8 bits and not likely to be expanded
- Address longer than 12 bits
- More complex instruction set needed than is available on Am2910

Architecture of the Control Unit

The recommended architecture using the Am2909 or Am2911 is shown in Figure 1. Note that the path from the pipeline register output through the next address logic, multiplexer, and microprogram memory is all combinational. The pipeline register contains the current microinstruction being executed. A portion of that microinstruction consists of a sequence control command such as "continue", "loop", "return-from-subroutine", etc. The bits representing this sequence command are logically combined with bits representing such things as test conditions and system state to generate the required control signals to the Am2909 or Am2911. The block labeled "next address logic" may consist of simple gates, a PROM or a PLA, but it should be all combinational.

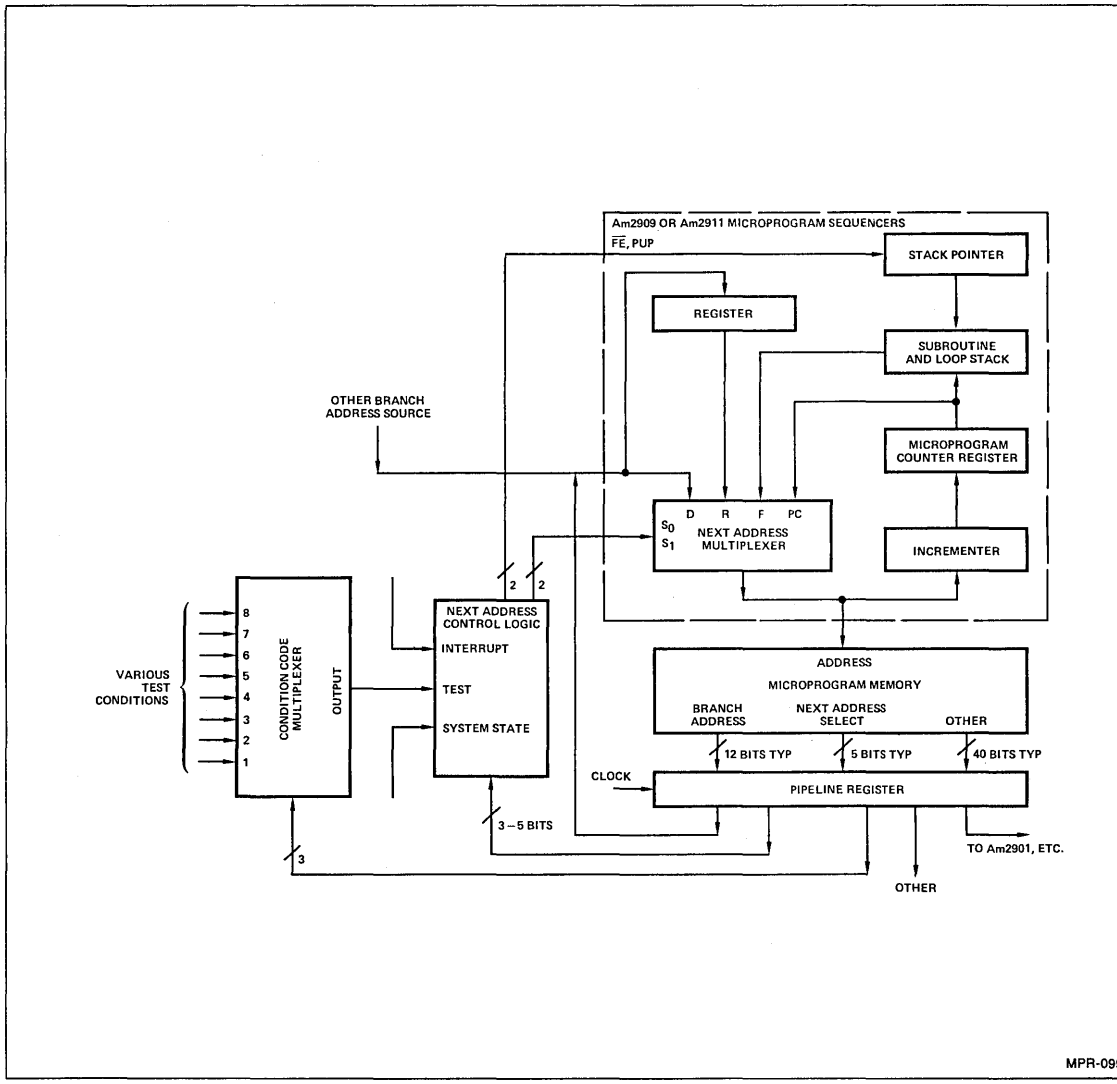


Figure 1. Recommended Computer Control Unit Architecture Using the Am2911 or Am2909.

The Am29811A is a combinational circuit which implements 16 sequence control instructions; it may be used with either an Am2909 or an Am2911. The set of instructions is nearly identical to that implemented internally in the Am2910.

Figure 2 shows the CCU of Figure 1 with the Am29811A in place. The Am29811A, in addition to controlling the Am2911, also controls a loop counter and several branch address sources. The instructions which are implemented by the Am29811A are shown in Figure 3, along with the Am29811A outputs for each instruction. Generating any instruction set consists simply of writing a truth table and designing combinational logic to implement it. For more detailed information refer to "The Microprogramming Handbook".

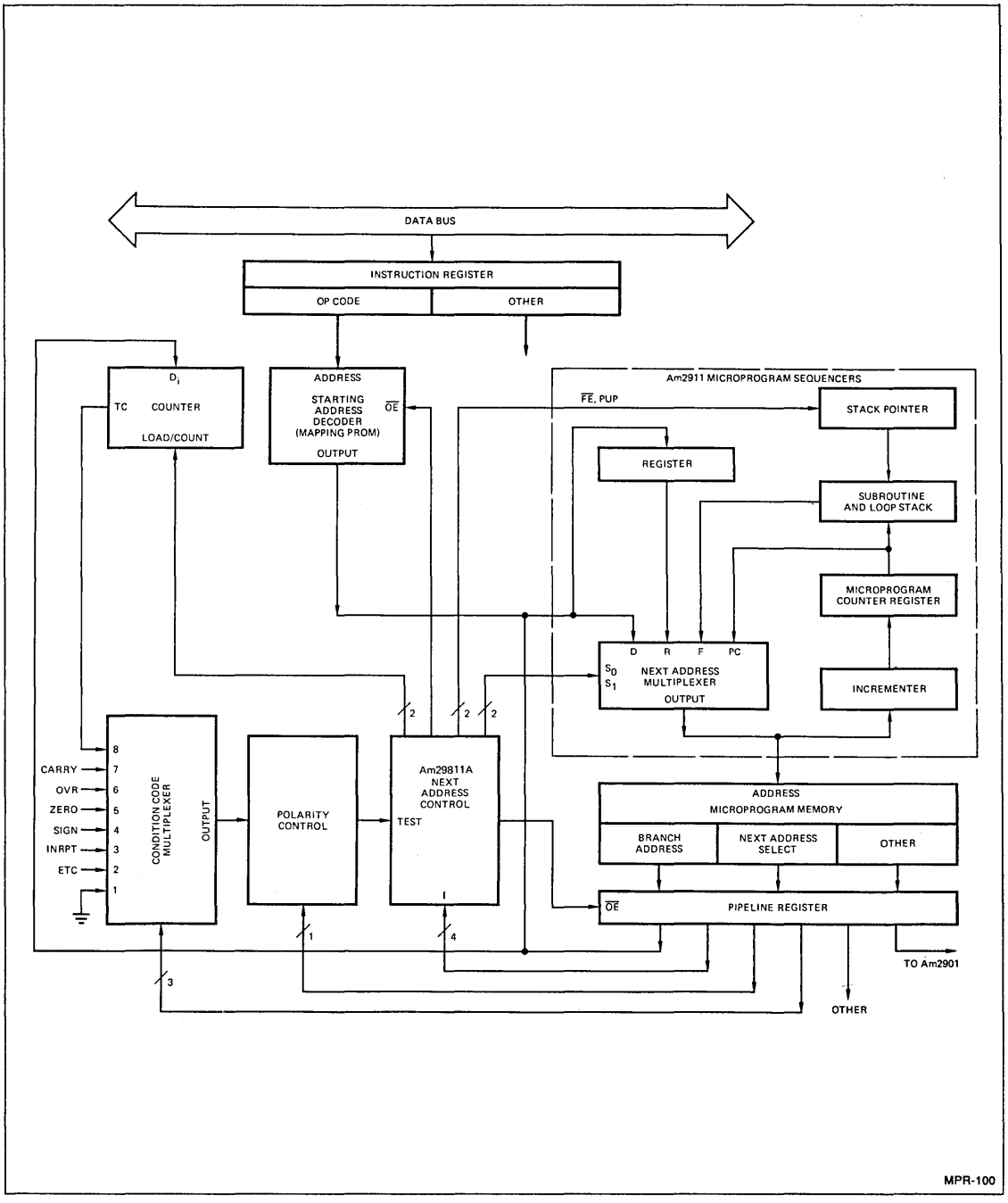


Figure 2. A typical Computer Control Unit Using the Am2911 and Am29811A.

Am29811A FUNCTION TABLE

MNEMONIC	INPUTS			OUTPUTS				
	INSTRUCTION I_3 I_2 I_1 I_0	FUNCTION	TEST INPUT	NEXT ADDR SOURCE	FILE	COUNTER	MAP-E	PL-E
JZ	L L L L	JUMP ZERO	X	D	HOLD	LL*	H	L
CJS	L L L H	COND JSB PL	L	PC	HOLD	HOLD	H	L
			H	D	PUSH	HOLD	H	L
JMAP	L L H L	JUMP MAP	X	D	HOLD	HOLD	L	H
CJP	L L H H	COND JUMP PL	L	PC	HOLD	HOLD	H	L
			H	D	HOLD	HOLD	H	L
PUSH	L H L L	PUSH/COND LD CNTR	L	PC	PUSH	HOLD	H	L
			H	PC	PUSH	LOAD	H	L
JSRP	L H L H	COND JSB R/PL	L	R	PUSH	HOLD	H	L
			H	D	PUSH	HOLD	H	L
CJV	L H H L	COND JUMP VECTOR	L	PC	HOLD	HOLD	H	H
			H	D	HOLD	HOLD	H	H
JRP	L H H H	COND JUMP R/PL	L	R	HOLD	HOLD	H	L
			H	D	HOLD	HOLD	H	L
RFCT	H L L L	REPEAT LOOP, CNTR ≠ 0	L	F	HOLD	DEC	H	L
			H	PC	POP	HOLD	H	L
RPCT	H L L H	REPEAT PL, CNTR ≠ 0	L	D	HOLD	DEC	H	L
			H	PC	HOLD	HOLD	H	L
CRTN	H L H L	COND RTN	L	PC	HOLD	HOLD	H	L
			H	F	POP	HOLD	H	L
CJPP	H L H H	COND JUMP PL & POP	L	PC	HOLD	HOLD	H	L
			H	D	POP	HOLD	H	L
LDCT	H H L L	LOAD CNTR & CONTINUE	X	PC	HOLD	LOAD	H	L
LOOP	H H L H	TEST END LOOP	L	F	HOLD	HOLD	H	L
			H	PC	POP	HOLD	H	L
CONT	H H H L	CONTINUE	X	PC	HOLD	HOLD	H	L
JP	H H H H	JUMP PL	X	D	HOLD	HOLD	H	L

L = LOW
H = HIGH
X = Don't Care

DEC = Decrement
*LL = Special Case

Am29811A TRUTH TABLE

MNEMONIC	FUNCTION	INPUTS					OUTPUTS							
							NEXT ADDR SOURCE		FILE		COUNTER		MAP E	PL E
		I_3	I_2	I_1	I_0	TEST	S_1	S_0	FE	PUP	LOAD	EN		
	PIN NO.	14	13	12	11	10	4	5	3	2	6	7	1	9
JZ	JUMP ZERO	L	L	L	L	L	H	H	H	H	L	L	H	L
		L	L	L	L	H	H	H	H	H	L	L	H	L
CJS	COND JSB PL	L	L	L	H	L	L	L	H	H	H	H	H	L
		L	L	L	H	H	H	H	L	H	H	H	H	L
JMAP	JUMP MAP	L	L	H	L	L	H	H	H	H	H	H	L	H
		L	L	H	L	H	H	H	H	H	H	H	L	H
CJP	COND JUMP PL	L	L	H	H	L	L	L	H	H	H	H	H	L
		L	L	H	H	H	H	H	H	H	H	H	H	L
PUSH	PUSH/COND LD CNTR	L	H	L	L	L	L	L	L	H	H	H	H	L
		L	H	L	L	H	L	L	L	H	L	H	H	L
JSRP	COND JSB R/PL	L	H	L	H	L	L	H	L	H	H	H	H	L
		L	H	L	H	H	H	H	L	H	H	H	H	L
CJV	COND JUMP VECTOR	L	H	H	L	L	L	L	H	H	H	H	H	H
		L	H	H	L	H	H	H	H	H	H	H	H	H
JRP	COND JUMP R/PL	L	H	H	H	L	L	H	H	H	H	H	H	L
		L	H	H	H	H	H	H	H	H	H	H	H	L
RFCT	REPEAT LOOP, CTR ≠ 0	H	L	L	L	L	H	L	H	L	H	L	H	L
		H	L	L	L	H	L	L	L	L	H	H	H	L
RPCT	REPEAT PL, CTR ≠ 0	H	L	L	H	L	H	H	H	H	H	L	H	L
		H	L	L	H	H	L	L	H	H	H	H	H	L
CRTN	COND RTN	H	L	H	L	L	L	L	H	L	H	H	H	L
		H	L	H	L	H	H	L	L	L	H	H	H	L
CJPP	COND JUMP PL & POP	H	L	H	H	L	L	L	H	L	H	H	H	L
		H	L	H	H	H	H	H	L	L	H	H	H	L
LDCT	LD CNTR & CONTINUE	H	H	L	L	L	L	L	H	H	L	H	H	L
		H	H	L	L	H	L	L	H	H	L	H	H	L
LOOP	TEST END LOOP	H	H	L	H	L	H	L	H	L	H	H	H	L
		H	H	L	H	H	L	L	L	L	H	H	H	L
CONT	CONTINUE	H	H	H	L	L	L	L	H	H	H	H	H	L
		H	H	H	L	H	L	L	H	H	H	H	H	L
JP	JUMP PL	H	H	H	H	L	H	H	H	H	H	H	H	L
		H	H	H	H	H	H	H	H	H	H	H	H	L

L = LOW
H = HIGH

Figure 3.

Expansion of the Am2909 or Am2911

Figure 4 shows the interconnection of three Am2911's to form a 12-bit sequencer. Note that the only interconnection between packages, other than the common clock and control lines, is the ripple carry between μPC incrementors. This carry path is not in the critical speed path if the Am2911 Y outputs drive the microprogram memory, because the ripple carry occurs in parallel with the memory access time. If, on the other hand, a micro-address register is placed at the Am2911 output, then the carry may lie in the critical speed path, since the last carry-in must be stable for a set-up time prior to the clock.

Selecting Between the Am2909 and Am2911

The difference between the Am2909 and the Am2911 involves two signals: the data inputs to the holding register and the "OR" inputs. In the Am2909, separate four-bit fields are provided for the holding register and the direct branch inputs to the multiplexer. In the Am2911, these fields are internally tied together. This may affect the design of the branch address system, as shown in Figure 5. Using the Am2909, the register inputs may be connected directly to the microprogram memory; the internal register replaces part of the pipeline register. The direct (D) inputs may be tied to the mapping logic which translates instruction op codes into microprogram addresses. While the same technique might be used with the Am2911, it is more common to connect the Am2911's D inputs to a branch address bus onto which various sources may be enabled. Shown in Figure 5 is a pipeline register and a mapping ROM. Other sources might also be applied to the same bus. The internal register is used only for temporary storage of some previous branch address.

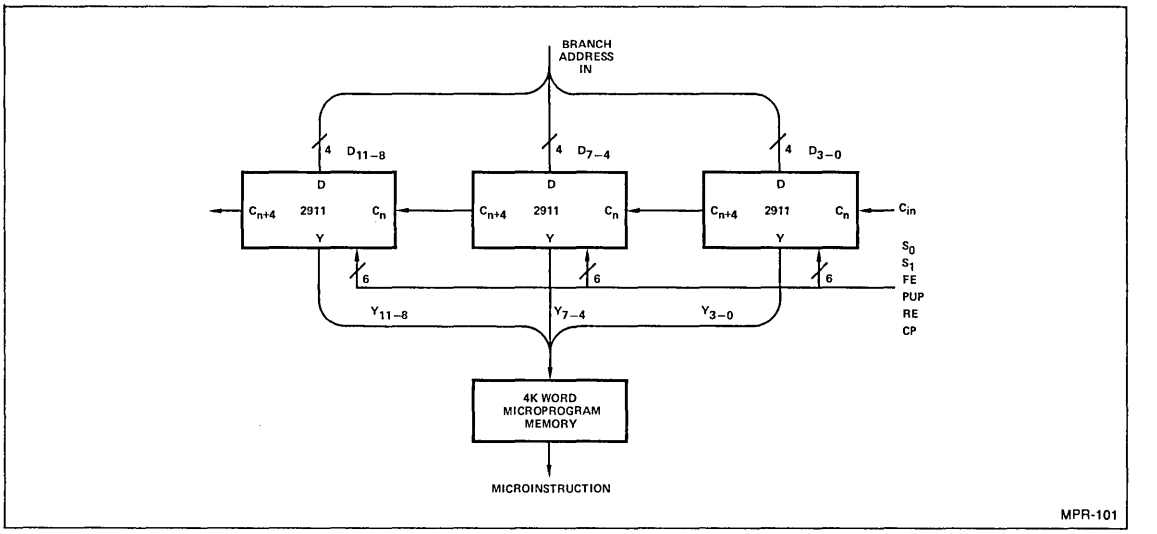


Figure 4. Twelve Bit Sequencer.

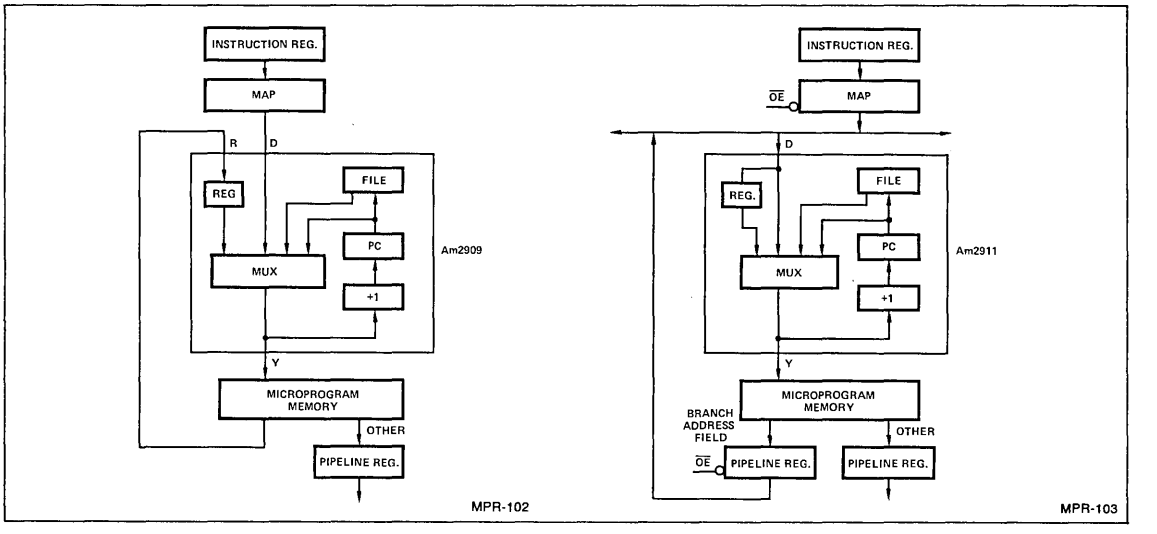


Figure 5. Branch Address Structures.

The second difference between the Am2909 and Am2911 is that the Am2909 has OR inputs available on each address output line. These pins can be used to generate multi-way single-cycle branches by simply tying several test conditions into the OR lines. See Figure 6. Typically, a branch is taken to an address with zeroes in the least significant bits. These bits are replaced with 1's or 0's by test conditions applied to the OR lines. In Figure 6, the states of the two test conditions X and Y result in a branch to 1100, 1101, 1110, or 1111.

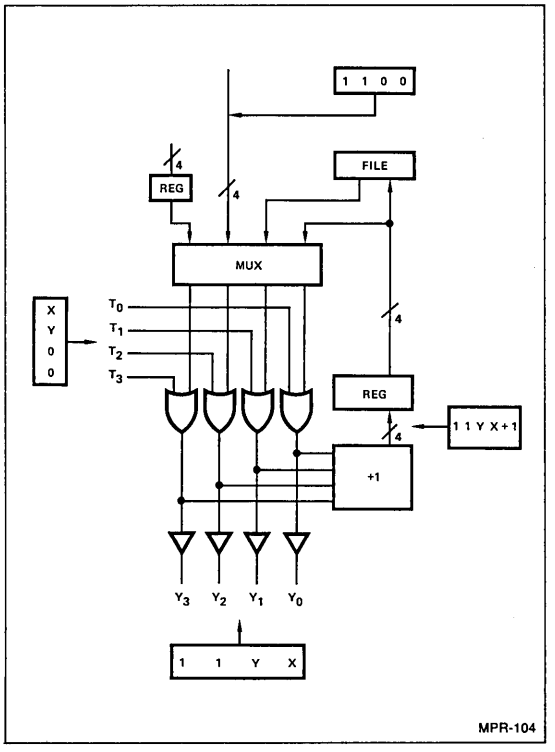


Figure 6. Use of OR Inputs to Obtain 4 - Way Branch.

The Am29803A has been designed to selectively apply any or all of four different test conditions to an Am2909. Figure 7 shows the truth table for this device. A nice trade off between flexibility and board space is achieved by using a single 28-pin Am2909 for the least significant four bits of a sequencer, and using the space-saving 20-pin Am2911's for the remainder of the bits. A detailed logic design for such a system is contained in The Microprogramming Handbook.

How to Perform Some Common Functions with the Am2909 or Am2911

1. CONTINUE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
PC	HOLD	1	0	0	1	X

Contents of PC placed on Y outputs; PC incremented.

2. BRANCH

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	HOLD	1	1	1	1	X

Feed data on D inputs straight through to memory address lines. Increment address and place in PC.

3. JUMP-TO-SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	PUSH	1	1	1	0	1

Sub-routine address fed from D inputs to memory address. Current PC is pushed onto stack, where it is saved for the return.

4. RETURN-FROM-SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
STACK	POP	1	1	0	0	0

The address at the top of the stack is applied to the microprogram memory, and is incremented for PC on the next cycle. The stack is popped to remove the return address.

Am29803A FUNCTION TABLE

	BRANCH ON	I_3	I_2	I_1	I_0	OR_3	OR_2	OR_1	OR_0
NONE	NONE	L	L	L	L	L	L	L	L
Two-Way Branches	T_0	L	L	L	H	L	L	L	T_0
	T_1	L	L	H	L	L	L	L	T_1
	T_2	L	H	L	L	L	L	L	T_2
	T_3	H	L	L	L	L	L	L	T_3
Four-Way Branches	T_1 & T_0	L	L	H	H	L	L	T_1	T_0
	T_2 & T_0	L	H	L	H	L	L	T_2	T_0
	T_3 & T_0	H	L	L	H	L	L	T_3	T_0
	T_2 & T_1	L	H	H	L	L	L	T_2	T_1
	T_3 & T_1	H	L	H	L	L	L	T_3	T_1
	T_3 & T_2	H	H	L	L	L	L	T_3	T_2
Eight-Way Branches	T_2, T_1, T_0	L	H	H	H	L	T_2	T_1	T_0
	T_3, T_1, T_0	H	L	H	H	L	T_3	T_1	T_0
	T_3, T_2, T_0	H	H	L	H	L	T_3	T_2	T_0
	T_3, T_2, T_1,	H	H	H	L	L	T_3	T_2	T_1
Sixteen-Way Branch	T_3, T_2, T_1, T_0	H	H	H	H	T_3	T_2	T_1	T_0

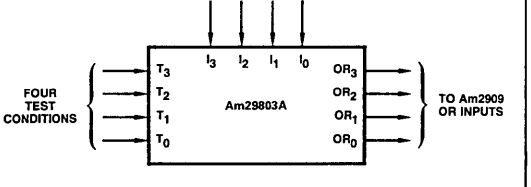


Figure 7.

Am2910
Microprogram Controller

DISTINCTIVE CHARACTERISTICS

- Twelve Bits Wide
  Address up to 4096 words of microcode with one chip. All internal elements are a full 12 bits wide.
- Internal Loop Counter
  Pre-settable 12-bit down-counter for repeating instructions and counting loop iterations.
- Four Address Sources
  Microprogram Address may be selected from microprogram counter, branch address bus, 5-level push/pop stack, or internal holding register.
- Sixteen Powerful Microinstructions
  Executes 16 sequence control instructions, most of which are conditional on external condition input, state of internal loop counter, or both.
- Output Enable Controls for Three Branch Address Sources
  Built-in decoder function to enable external devices onto branch address bus. Eliminates external decoder.
- All Registers Positive Edge-triggered
  Simplifies timing problems. Eliminates long set-up times.
- Fast Control from Condition Input
  Delay from condition code input to address output only 27ns typical.

GENERAL DESCRIPTION

The Am2910 Microprogram controller is an address sequencer intended for controlling the sequence of execution of microinstructions stored in microprogram memory. Besides the capability of sequential access, it provides conditional branching to any microinstruction within its 4096-microword range. A last-in, first-out stack provides microsubroutine return linkage and looping capability; there are five levels of nesting of microsubroutines. Microinstruction loop count control is provided with a count capacity of 4096.

During each microinstruction, the Microprogram controller provides a 12-bit address from one of four sources: 1) the microprogram address register (μPC), which usually contains an address one greater than the previous address; 2) an external (direct) input (D); 3) a register/counter (R) retaining data loaded during a previous microinstruction; or 4) a five-deep last-in, first-out stack (F).

For a detailed discussion of this architectural approach to microprogram control units, refer to "The Microprogramming Handbook", an AMD applications publication.

Am2910 BLOCK DIAGRAM

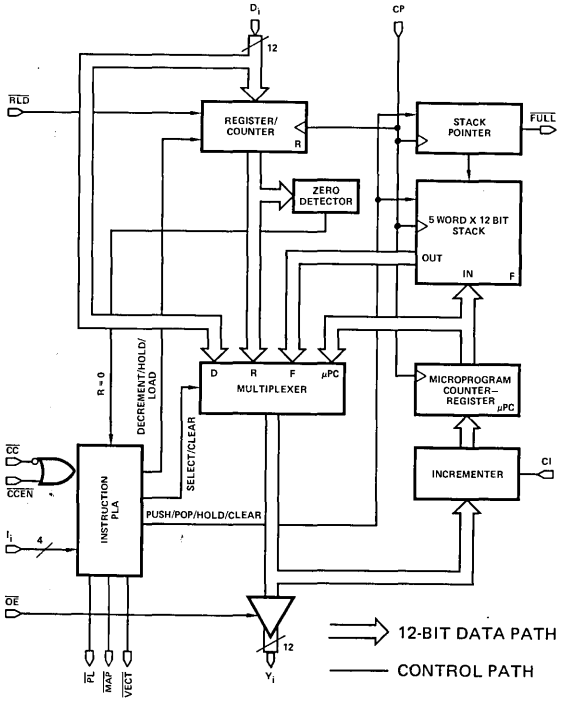


Figure 1.

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ARCHITECTURE OF THE Am2910

The Am2910 is a bipolar microprogram controller intended for use in high-speed microprocessor applications. It allows addressing of up to 4K words of microprogram. A block diagram is shown in Figure 1.

The controller contains a four-input multiplexer that is used to select either the register/counter, direct input, microprogram counter, or stack as the source of the next microinstruction address.

The register/counter consists of 12 D-type, edge-triggered flip-flops, with a common clock enable. When its load control, $\overline{RLD}$, is LOW, new data is loaded on a positive clock transition. A few instructions include load; in most systems, these instructions will be sufficient, simplifying the microcode. The output of the register/counter is available to the multiplexer as a source for the next microinstruction address. The direct input furnishes a source of data for loading the register/counter.

The Am2910 contains a microprogram counter (μPC) that is composed of a 12-bit incrementer followed by a 12-bit register. The μPC can be used in either of two ways: When the carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one ($Y + 1 \rightarrow \mu PC$). Sequential microinstructions are thus executed. When the carry-in is LOW, the incrementer passes the Y output word unmodified so that μPC is reloaded with the same Y word on the next clock cycle ($Y \rightarrow \mu PC$). The same microinstruction is thus executed any number of times.

The third source for the multiplexer is the direct (D) input. This source is used for branching.

The fourth source available at the multiplexer input is a 5-word by 12-bit stack (file). The stack is used to provide return address linkage when executing microsubroutines or loops. The stack contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations (looping) to be performed without a pop.

The stack pointer operates as an up/down counter. During microinstructions 2, 4, and 5, the PUSH operation is performed. This causes the stack pointer to increment and the file to be written with the required return linkage. On the cycle following the PUSH, the return data is at the new location pointed to by the stack pointer.

During five microinstructions, a POP operation may occur. The stack pointer decrements at the next rising clock edge following a POP, effectively removing old information from the top of the stack.

The stack pointer linkage is such that any sequence of pushes, pops, or stack references can be achieved. At RESET (Instruction 0), the depth of nesting becomes zero. For each PUSH, the nesting depth increases by one; for each POP, the depth decreases by one. The depth can grow to five. After a depth of five is reached, $\overline{FULL}$ goes LOW. Any further PUSHes onto a full stack overwrite information at the top of the stack, but leave the stack pointer unchanged. This operation will usually destroy useful information and is normally avoided. A POP from an empty stack may place non-meaningful data on the Y outputs, but is otherwise safe. The stack pointer remains at zero whenever a POP is attempted from a stack already empty.

The register/counter is operated during three microinstructions (8, 9, 15) as a 12-bit down counter, with result = zero available as a microinstruction branch test criterion. This provides efficient iteration of microinstructions. The register/counter is arranged such that if it is preloaded with a number N and then used as a loop termination counter, the sequence will be executed exactly N+1 times. During instruction 15, a three-way branch under combined control of the loop counter and the condition code is available.

The device provides three-state Y outputs. These can be particularly useful in designs requiring automatic checkout of the processor. The microprogram controller outputs can be forced into the high-impedance state, and pre-programmed sequences of microinstructions can be executed via external access to the address lines.

OPERATION

Table I shows the result of each instruction in controlling the multiplexer which determines the Y outputs, and in controlling the three enable signals $\overline{PL}$, $\overline{MAP}$, and $\overline{VECT}$. The effect on the register/counter and the stack after the next positive-going clock edge is also shown. The multiplexer determines which internal source drives the Y outputs. The value loaded into μPC is either identical to the Y output, or else one greater, as determined by CI. For each instruction, one and only one of the three outputs PL, MAP, and VECT is LOW. If these outputs control three-state enables for the primary source of microprogram jumps (usually part of a pipeline register), a PROM which maps the instruction to a microinstruction starting location, and an optional third source (often a vector from a DMA or interrupt source), respectively, the three-state sources can drive the D inputs without further logic.

Several inputs, as shown in Table II, can modify instruction execution. The combination CC HIGH and $\overline{CCEN}$ LOW is used as a test in 10 of the 16 instructions. $\overline{RLD}$, when LOW, causes the D input to be loaded into the register/counter, overriding any HOLD or DEC operation specified in the instruction. $\overline{OE}$, normally LOW, may be forced HIGH to remove the Am2910 Y outputs from a three-state bus.

The stack, a five-word last-in, first-out 12-bit memory, has a pointer which addresses the value presently on the top of the stack. Explicit control of the stack pointer occurs during instruction 0 (RESET), which makes the stack empty by resetting the SP to zero. After a RESET, and whenever else the stack is empty, the contents of the top of stack is undefined until a PUSH occurs. Any POPs performed while the stack is empty put undefined data on the F outputs and leave the stack pointer at zero.

Any time the stack is full (five more PUSHes than POPs have occurred since the stack was last empty), the $\overline{FULL}$ warning output occurs. This signal first appears on the microcycle after a fifth PUSH. No additional PUSH should be attempted onto a full stack; if tried, information within the stack will be overwritten and lost.

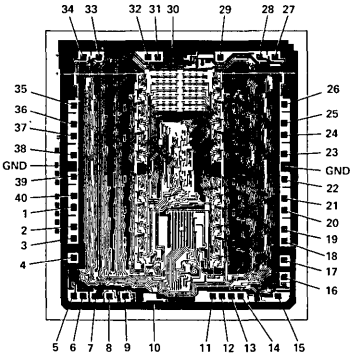
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2910PC	P-40	C	C-1
AM2910DC	D-40	C	C-1
AM2910DC-B	D-40	C	B-1
AM2910DM	D-40	M	C-3
AM2910DM-B	D-40	M	B-3
AM2910FM	F-42	M	C-3
AM2910FM-B	F-42	M	B-3
AM2910XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2910XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

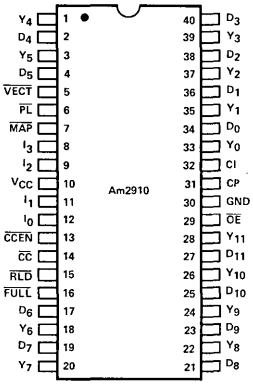
Metallization and Pad Layout



Die Size 0.170" x 0.194"
(Note: Numbers refer to DIP connections)

CONNECTION DIAGRAMS — Top Views

DIP



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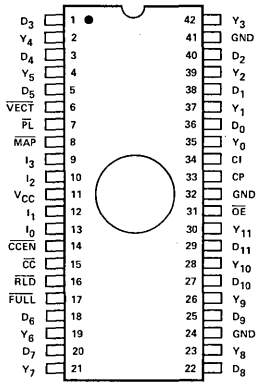
Flat Package



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Pin 1 is marked for orientation. On flat pack all three ground Pins must be connected to ground.

TABLE I. INSTRUCTIONS

HEX I_3-I_0	MNEMONIC	NAME	REG/ CNTR CON-TENTS	FAIL $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH		PASS $\overline{CCEN}$ = HIGH or $\overline{CC}$ = LOW		REG/ CNTR	ENABLE
				Y	STACK	Y	STACK		
0	JZ	JUMP ZERO	X	0	CLEAR	0	CLEAR	HOLD	PL
1	CJS	COND JSB PL	X	PC	HOLD	D	PUSH	HOLD	PL
2	JMAP	JUMP MAP	X	D	HOLD	D	HOLD	HOLD	MAP
3	CJP	COND JUMP PL	X	PC	HOLD	D	HOLD	HOLD	PL
4	PUSH	PUSH/COND LD CNTR	X	PC	PUSH	PC	PUSH	Note 1	PL
5	JSRP	COND JSB R/PL	X	R	PUSH	D	PUSH	HOLD	PL
6	CJV	COND JUMP VECTOR	X	PC	HOLD	D	HOLD	HOLD	VECT
7	JRP	COND JUMP R/PL	X	R	HOLD	D	HOLD	HOLD	PL
8	RFCT	REPEAT LOOP, CNTR ≠ 0	≠0	F	HOLD	F	HOLD	DEC	PL
			=0	PC	POP	PC	POP	HOLD	PL
9	RPCT	REPEAT PL, CNTR ≠ 0	≠0	D	HOLD	D	HOLD	DEC	PL
			=0	PC	HOLD	PC	HOLD	HOLD	PL
A	CRTN	COND RTN	X	PC	HOLD	F	POP	HOLD	PL
B	CJPP	COND JUMP PL & POP	X	PC	HOLD	D	POP	HOLD	PL
C	LDCT	LD CNTR & CONTINUE	X	PC	HOLD	PC	HOLD	LOAD	PL
D	LOOP	TEST END LOOP	X	F	HOLD	PC	POP	HOLD	PL
E	CONT	CONTINUE	X	PC	HOLD	PC	HOLD	HOLD	PL
F	TWB	THREE-WAY BRANCH	≠0	F	HOLD	PC	POP	DEC	PL
			=0	D	POP	PC	POP	HOLD	PL

Note 1: If $\overline{CCEN}$ = LOW and $\overline{CC}$ = HIGH, hold; else load. X = Don't Care

TABLE II. PIN FUNCTIONS

Abbreviation	Name	Function
D_i	Direct Input Bit i	Direct input to register/counter and multiplexer. D_0 is LSB
I_i	Instruction Bit i	Selects one-of-sixteen instructions for the Am2910
$\overline{CC}$	Condition Code	Used as test criterion. Pass test is a LOW on $\overline{CC}$.
$\overline{CCEN}$	Condition Code Enable	Whenever the signal is HIGH, $\overline{CC}$ is ignored and the part operates as though $\overline{CC}$ were true (LOW).
CI	Carry-In	Low order carry input to incrementer for microprogram counter
$\overline{RLD}$	Register Load	When LOW forces loading of register/counter regardless of instruction or condition
$\overline{OE}$	Output Enable	Three-state control of Y_i outputs
CP	Clock Pulse	Triggers all internal state changes at LOW-to-HIGH edge
V_{CC}	+5 Volts	
GND	Ground	
Y_i	Microprogram Address Bit i	Address to microprogram memory. Y_0 is LSB, Y_{11} is MSB
$\overline{FULL}$	Full	Indicates that five items are on the stack
$\overline{PL}$	Pipeline Address Enable	Can select #1 source (usually Pipeline Register) as direct input source
$\overline{MAP}$	Map Address Enable	Can select #2 source (usually Mapping PROM or PLA) as direct input source
$\overline{VECT}$	Vector Address Enable	Can select #3 source (for example, Interrupt Starting Address) as direct input source

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% MIN. = 4.75V MAX. = 5.25V

MIL T_C = −55°C to +125°C V_{CC} = 5.0V ±10% MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −1.6mA V_{IN} = V_{IH} or V_{IL}			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IH} or V_{IL}	Y_{0-11}, I_{OL} = 12mA				0.5	Volts
			$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$, $\overline{FULL}$, I_{OL} = 8mA					
V_{IH}	Input HIGH Level (Note 4)	Guaranteed Input Logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Note 4)	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V		D_{0-11}			−0.87	mA
				CI, $\overline{CCEN}$			−0.54	
				I_{0-3}, $\overline{OE}$, $\overline{RLD}$			−0.72	
				$\overline{CC}$			−1.31	
				CP			−2.14	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		D_{0-11}			80	μA
				CI, $\overline{CCEN}$			30	
				I_{0-3}, $\overline{OE}$, $\overline{RLD}$			40	
				$\overline{CC}$			50	
				CP			100	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX. $\overline{OE}$ = 2.4V		V_{OUT} = 0.5V			−50	μA
I_{OZH}				V_{OUT} = 2.4V			50	
I_{CC}	Power Supply Current	V_{CC} = MAX.		T_A = 25°C		195	320	mA
			Am2910PC, DC	T_A = 0°C to +70°C			344	
				T_A = +70°C			280	
			Am2910DM, FM	T_C = −55°C to +125°C			340	
				T_C = +125°C			227	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be tested in a static-, noise-free environment.

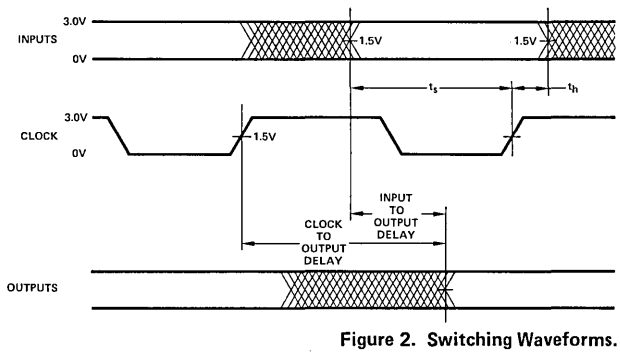

Figure 2. Switching Waveforms.

See Tables A for t_s and t_h for various inputs. See Tables B for combinational delays from clock and other inputs to outputs. See Figure 5 for timing of a typical CCU cycle.

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SWITCHING CHARACTERISTICS

The tables below define the Am2910 switching characteristics. Tables A are set-up and hold times relative to the clock LOW-to-HIGH transition. Tables B are combinational delays. Tables C are clock requirements. All measurements are made at 1.5V with input levels at 0V or 3V. All values are in ns.

TYPICAL ROOM TEMPERATURE CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, C_L = 50pF)

A. Set-up and Hold Times

Input	t_s	t_h
$D_i \rightarrow R$	9	3
$D_i \rightarrow PC$	34	1
I_0-I_3	64	0
$\overline{CC}$	46	0
$\overline{CCEN}$	49	0
CI	26	2
$\overline{RLD}$	18	2

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}	14	–	–
I_0-I_3	40		–
$\overline{CC}$	27	–	–
$\overline{CCEN}$	33	–	–
CP(note) I = 8, 9, 15	66	–	39
CP All other I	37	–	39
$\overline{OE}$	15	–	–

C. Clock Requirements

Minimum Clock LOW Time	23	ns
Minimum Clock HIGH Time	30	ns
Minimum Clock Period, I=8, 9, 15		ns
Minimum Clock Period, I=14		ns

(Clock periods for other instructions are determined by external conditions.)

Note: These instructions are conditional on the counter. Delays from CP to outputs will be longer if the instruction prior to the clock was 4 or 12 or $\overline{RLD}$ was LOW.

GUARANTEED ROOM TEMPERATURE CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0V, C_L = 50pF)

A. Set-up and Hold Times

Input	t_s	t_h
$D_i \rightarrow R$		
$D_i \rightarrow PC$		
I_0-I_3		
$\overline{CC}$		
$\overline{CCEN}$		
CI		
$\overline{RLD}$		

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}			
I_0-I_3			
$\overline{CC}$			
$\overline{CCEN}$			
CP(note) I = 8, 9, 15			
CP All other I			
$\overline{OE}$			

C. Clock Requirements

Minimum Clock LOW Time		ns
Minimum Clock HIGH Time		ns
Minimum Clock Period, I=8, 9, 15		ns
Minimum Clock Period, I=14		ns

(Clock periods for other instructions are determined by external conditions.)

Note: These instructions are conditional on the counter. Delays from CP to outputs will be longer if the instruction prior to the clock was 4 or 12 or $\overline{RLD}$ was LOW.

GUARANTEED CHARACTERISTICS OVER COMMERCIAL OPERATING RANGE
Am2910PC, DC (T_A = 0°C to +70°C, V_{CC} = 4.75V to 5.25V, C_L = 50pF)

A. Set-up and Hold Times

Input	t_s	t_h
$D_i \rightarrow R$		
$D_i \rightarrow PC$		
I_0-I_3		
$\overline{CC}$		
$\overline{CCEN}$		
CI		
$\overline{RLD}$		

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}			
I_0-I_3			
$\overline{CC}$			
$\overline{CCEN}$			
CP(note) I = 8, 9, 15			
CP All other I			
$\overline{OE}$			

C. Clock Requirements

Minimum Clock LOW Time	50	ns
Minimum Clock HIGH Time	30	ns
Minimum Clock Period, I=8, 9, 15		ns
Minimum Clock Period, I=14		ns

(Clock periods for other instructions are determined by external conditions.)

Note: These instructions are conditional on the counter. Delays from CP to outputs will be longer if the instruction prior to the clock was 4 or 12 or $\overline{RLD}$ was LOW.

GUARANTEED CHARACTERISTICS OVER MILITARY OPERATING RANGE
Am2910DM, FM (T_C = –55°C to +125°C, V_{CC} = 4.5V to 5.5V, C_L = 50pF)

A. Set-up and Hold Times

Input	t_s	t_h
$D_i \rightarrow R$		
$D_i \rightarrow PC$		
I_0-I_3		
$\overline{CC}$		
$\overline{CCEN}$		
CI		
$\overline{RLD}$		

B. Combinational Delays

Input	Y	$\overline{PL}$, $\overline{VECT}$, $\overline{MAP}$	$\overline{Full}$
D_0-D_{11}			
I_0-I_3			
$\overline{CC}$			
$\overline{CCEN}$			
CP(note) I = 8, 9, 15			
CP All other I			
$\overline{OE}$			

C. Clock Requirements

Minimum Clock LOW Time		ns
Minimum Clock HIGH Time		ns
Minimum Clock Period, I=8, 9, 15		ns
Minimum Clock Period, I=14		ns

(Clock periods for other instructions are determined by external conditions.)

Note: These instructions are conditional on the counter. Delays from CP to outputs will be longer if the instruction prior to the clock was 4 or 12 or $\overline{RLD}$ was LOW.

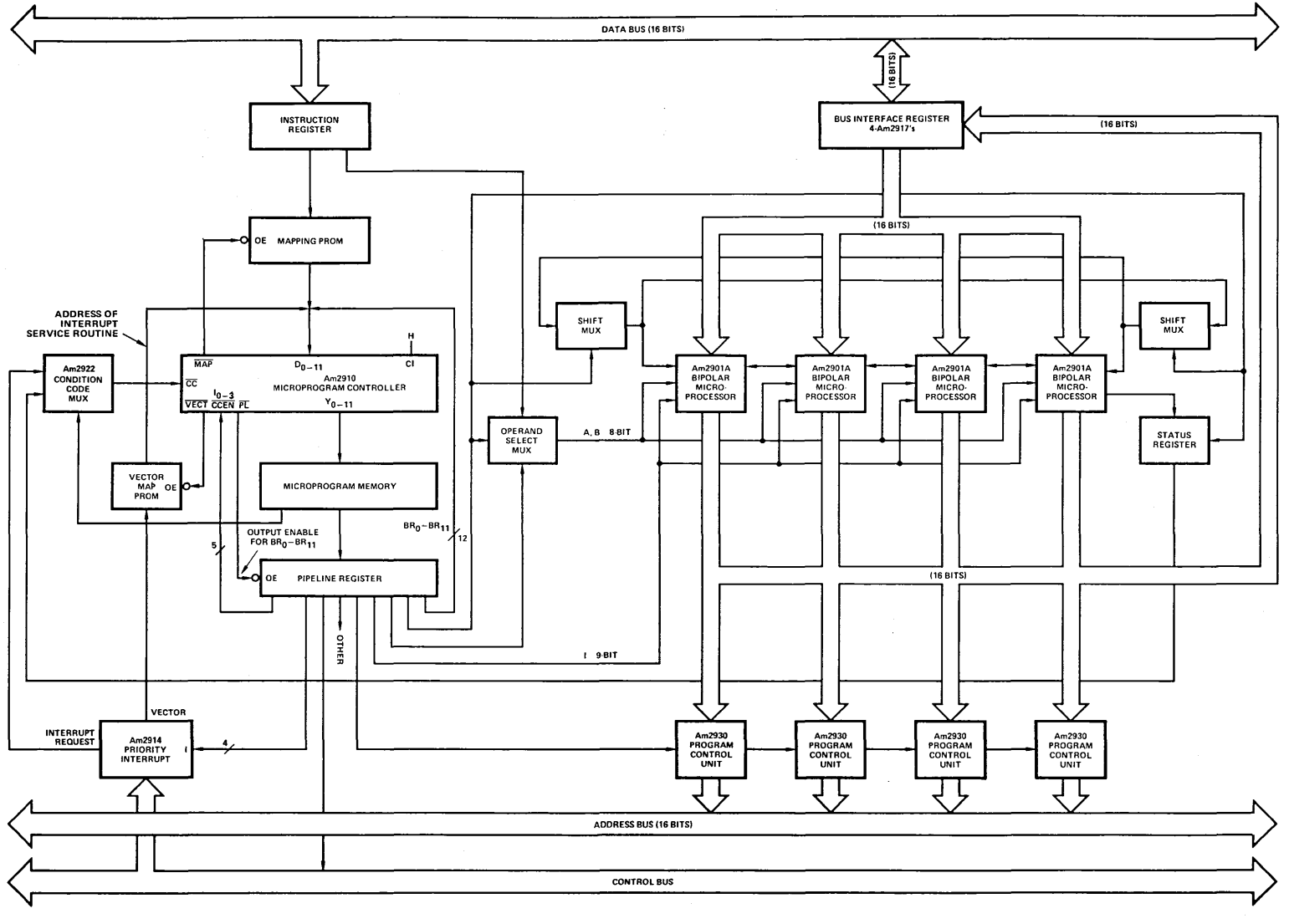

Figure 3. Typical Bipolar Microcomputer Using Am2910.

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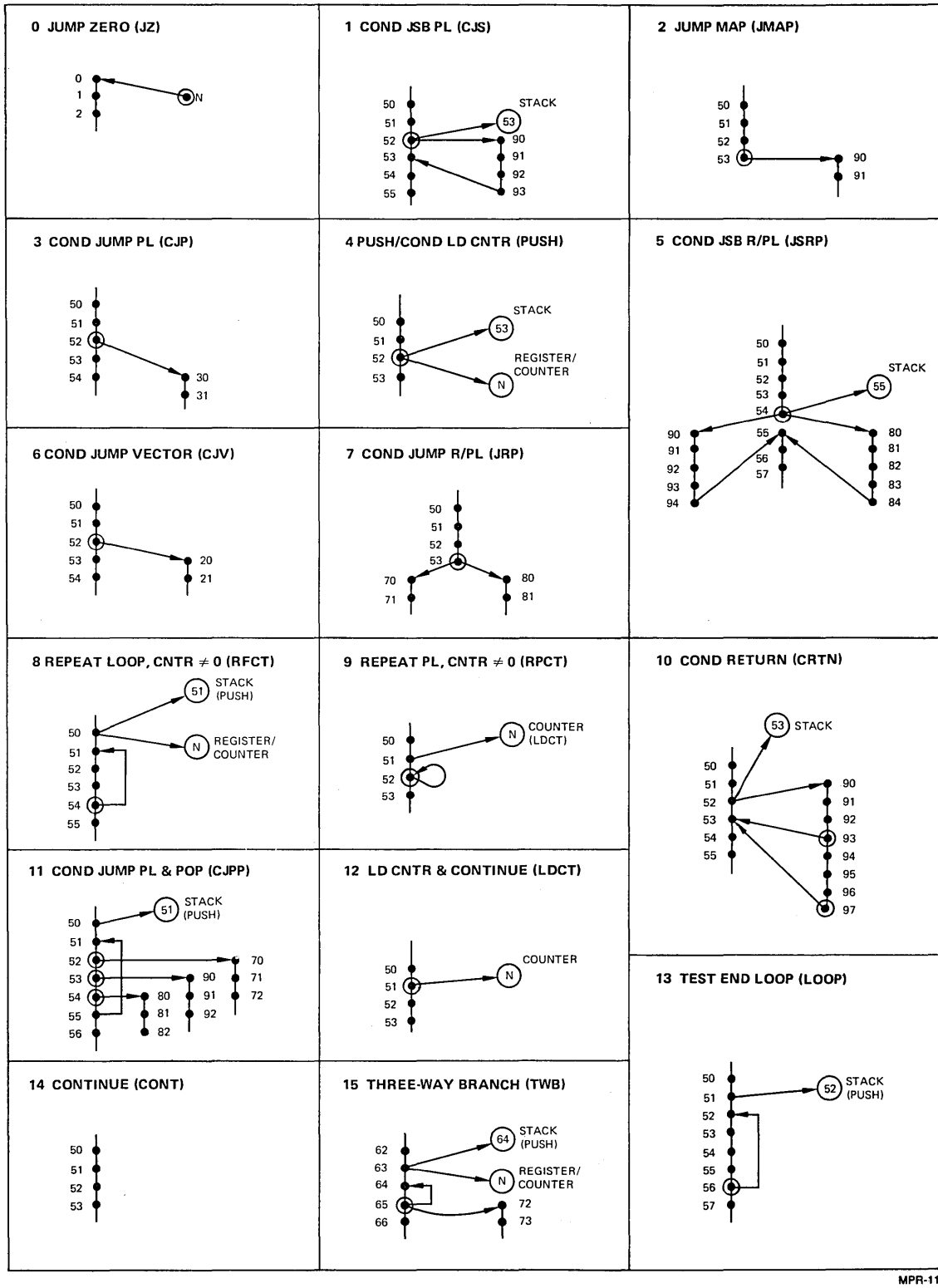


Figure 4. Am2910 Execution Examples.

THE Am2910 INSTRUCTION SET

The Am2910 provides 16 instructions which select the address of the next microinstruction to be executed. Four of the instructions are unconditional – their effect depends only on the instruction. Ten of the instructions have an effect which is partially controlled by an external, data-dependent condition. Three of the instructions have an effect which is partially controlled by the contents of the internal register/counter. The instruction set is shown in Table I. In this discussion it is assumed that C_n is tied HIGH.

In the ten conditional instructions, the result of the data-dependent test is applied to $\overline{CC}$. If the $\overline{CC}$ input is LOW, the test is considered to have been passed, and the action specified in the name occurs; otherwise, the test has failed and an alternate (often simply the execution of the next sequential microinstruction) occurs. Testing of $\overline{CC}$ may be disabled for a specific microinstruction by setting $\overline{CCEN}$ HIGH, which unconditionally forces the action specified in the name; that is, it forces a pass. Other ways of using $\overline{CCEN}$ include (1) tying it HIGH, which is useful if no microinstruction is data-dependent; (2) tying it LOW if data-dependent instructions are never forced unconditionally; or (3) tying it to the source of Am2910 instruction bit I_0, which leaves instructions 4, 6, and 10 as data-dependent but makes others unconditional. All of these tricks save one bit of microcode width.

The effect of three instructions depends on the contents of the register/counter. Unless the counter holds a value of zero, it is decremented; if it does hold zero, it is held and a different microprogram next address is selected. These instructions are useful for executing a microinstruction loop a known number of times. Instruction 15 is affected both by the external condition code and the internal register/counter.

Perhaps the best technique for understanding the Am2910 is to simply take each instruction and review its operation. In order to provide some feel for the actual execution of these instructions, Figure 4 is included and depicts examples of all 16 instructions.

The examples given in Figure 4 should be interpreted in the following manner: The intent is to show microprogram flow as various microprogram memory words are executed. For example, the CONTINUE instruction, instruction number 14, as shown in Figure 4, simply means that the contents of microprogram memory word 50 is executed, then the contents of word 51 is executed. This is followed by the contents of microprogram memory word 52 and the contents of microprogram memory word 53. The microprogram addresses used in the examples were arbitrarily chosen and have no meaning other than to show instruction flow. The exception to this is the first example, JUMP ZERO, which forces the microprogram location counter to address ZERO. Each dot refers to the time that the contents of the microprogram memory word is in the pipeline register. While no special symbology is used for the conditional instructions, the test to follow will explain what the conditional choices are in each example.

It might be appropriate at this time to mention that AMD has a microprogram assembler called AMDASM, which has the capability of using the Am2910 instructions in symbolic representation. AMDASM's Am2910 instruction symbolics (or mnemonics) are given in Figure 4 for each instruction and are also shown in Table I.

Instruction 0, JZ (JUMP and ZERO, or RESET) unconditionally specifies that the address of the next microinstruction is zero. Many designs use this feature for power-up sequences and provide the power-up firmware beginning at microprogram memory word location 0.

Instruction 1 is a CONDITIONAL JUMP-TO-SUBROUTINE via the address provided in the pipeline register. As shown in Figure 4, the machine might have executed words at address 50, 51, and 52. When the contents of address 52 is in the pipeline register, the next address control function is the CONDITIONAL JUMP-TO-SUBROUTINE. Here, if the test is passed, the next instruction executed will be the contents of microprogram memory location 90. If the test has failed, the JUMP-TO-SUBROUTINE will not be executed; the contents of microprogram memory location 53 will be executed instead. Thus, the CONDITIONAL JUMP-TO-SUBROUTINE instruction at location 52 will cause the instruction either in location 90 or in location 53 to be executed next. If the TEST input is such that location 90 is selected, value 53 will be pushed onto the internal stack. This provides the return linkage for the machine when the subroutine beginning at location 90 is completed. In this example, the subroutine was completed at location 93 and a RETURN-FROM-SUBROUTINE would be found at location 93.

Instruction 2 is the JUMP MAP instruction. This is an unconditional instruction which causes the $\overline{MAP}$ output to be enabled so that the next microinstruction location is determined by the address supplied via the mapping PROMs. Normally, the JUMP MAP instruction is used at the end of the instruction fetch sequence for the machine. In the example of Figure 4, microinstructions at locations 50, 51, 52, and 53 might have been the fetch sequence and at its completion at location 53, the jump map function would be contained in the pipeline register. This example shows the mapping PROM outputs to be 90; therefore, an unconditional jump to microprogram memory address 90 is performed.

Instruction 3, CONDITIONAL JUMP PIPELINE, derives its branch address from the pipeline register branch address value (BR_0 – BR_{11} in Figure 2). This instruction provides a technique for branching to various microprogram sequences depending upon the test condition inputs. Quite often, state machines are designed which simply execute tests on various inputs waiting for the condition to come true. When the true condition is reached, the machine then branches and executes a set of microinstructions to perform some function. This usually has the effect of resetting the input being tested until some point in the future. Figure 4 shows the conditional jump via the pipeline register address at location 52. When the contents of microprogram memory word 52 are in the pipeline register, the next address will be either location 53 or location 30 in this example. If the test is passed, the value currently in the pipeline register (3) will be selected. If the test fails, the next address selected will be contained in the microprogram counter which, in this example, is 53.

Instruction 4 is the PUSH/CONDITIONAL LOAD COUNTER instruction and is used primarily for setting up loops in microprogram firmware. In Figure 4, when instruction 52 is in the pipeline register, a PUSH will be made onto the stack and the counter will be loaded based on the condition. When a PUSH occurs, the value pushed is always the next sequential instruction address. In this case, the address is 53. If the test fails, the counter is not loaded; if it is passed, the counter is loaded with the value contained in the pipeline register branch address field. Thus, a single microinstruction can be used to set up a loop to be executed a specific number of times. Instruction 8 will

THE Am2910 INSTRUCTION SET (Cont.)

describe how to use the pushed value and the register/counter for looping.

Instruction 5 is a CONDITIONAL JUMP-TO-SUBROUTINE via the register/counter or the contents of the PIPELINE register. As shown in Figure 4, a PUSH is always performed and one of two subroutines executed. In this example, either the subroutine beginning at address 80 or the subroutine beginning at address 90 will be performed. A return-from-subroutine (instruction number 10) returns the microprogram flow to address 55. In order for this microinstruction control sequence to operate correctly, both the next address fields of instruction 53 and the next address fields of instruction 54 would have to contain the proper value. Let's assume that the branch address fields of instruction 53 contain the value 90 so that it will be in the Am2910 register/counter when the contents of address 54 are in the pipeline register. This requires that the instruction at address 53 load the register/counter. Now, during the execution of instruction 5 (at address 54), if the test failed, the contents of the register (value = 90) will select the address of the next microinstruction. If the test input passes, the pipeline register contents (value = 80) will determine the address of the next microinstruction. Therefore, this instruction provides the ability to select one of two subroutines to be executed based on a test condition.

Instruction 6 is a CONDITIONAL JUMP VECTOR instruction which provides the capability to take the branch address from a third source heretofore not discussed. In order for this instruction to be useful, the Am2910 output, $\overline{VECT}$ is used to control a three-state control input of a register, buffer, or PROM containing the next microprogram address. This instruction provides one technique for performing interrupt type branching at the microprogram level. Since this instruction is conditional, a pass causes the next address to be taken from the vector source, while failure causes the next address to be taken from the microprogram counter. In the example of Figure 4, if the CONDITIONAL JUMP VECTOR instruction is contained at location 52, execution will continue at vector address 20 if the TEST input is HIGH and the microinstruction at address 53 will be executed if the TEST input is LOW.

Instruction 7 is a CONDITIONAL JUMP via the contents of the Am2910 REGISTER/COUNTER or the contents of the PIPELINE register. This instruction is very similar to instruction 5; the conditional jump-to-subroutine via R or PL. The major difference between instruction 5 and instruction 7 is that no push onto the stack is performed with 7. Figure 4 depicts this instruction as a branch to one of two locations depending on the test condition. The example assumes the pipeline register contains the value 70 when the contents of address 52 is being executed. As the contents of address 53 is clocked into the pipeline register, the value 70 is loaded into the register/counter in the Am2910. The value 80 is available when the contents of address 53 is in the pipeline register. Thus, control is transferred to either address 70 or address 80 depending on the test condition.

Instruction 8 is the REPEAT LOOP, COUNTER ≠ ZERO instruction. This microinstruction makes use of the decrementing capability of the register/counter. To be useful, some previous instruction, such as 4, must have loaded a count value into the register/counter. This instruction checks to see whether the register/counter contains a non-zero value. If so, the register/counter is decremented, and the address of the next microinstruction is taken from the top of the stack. If the register counter contains zero, the loop exit condition is occuring; control falls through to the next sequential microinstruction by selecting uPC; the stack is POP'd by decrementing the stack pointer, but the contents of the top of the stack are thrown away.

An example of the REPEAT LOOP, COUNTER ≠ ZERO instruction is shown in Figure 4. In this example, location 50 most likely would contain a PUSH/CONDITIONAL LOAD COUNTER instruction which would have caused address 51 to be PUSHed on the stack and the counter to be loaded with the proper value for looping the desired number of times.

In this example, since the loop test is made at the end of the instructions to be repeated (microaddress 54), the proper value to be loaded by the instructions at address 50 is one less than the desired number of passes through the loop. This method allows a loop to be executed 1 to 4096 times. If it is desired to execute the loop from 0 to 4095 times, the firmware should be written to make the loop exit test immediately after loop entry.

Single-microinstruction loops provide a highly efficient capability for executing a specific microinstruction a fixed number of times. Examples include fixed rotates, byte swap, fixed point multiply, and fixed point divide.

Instruction 9 is the REPEAT PIPELINE REGISTER, COUNTER ≠ ZERO instruction. This instruction is similar to instruction 8 except that the branch address now comes from the pipeline register rather than the file. In some cases, this instruction may be thought of as a one-word file extension; that is, by using this instruction, a loop with the counter can still be performed when subroutines are nested five deep. This instruction's operation is very similar to that of instruction 8. The differences are that on this instruction, a failed test condition causes the source of the next microinstruction address to be the D inputs; and, when the test condition is passed, this instruction does not perform a POP because the stack is not being used.

In the example of Figure 4, the REPEAT PIPELINE, COUNTER ≠ ZERO instruction is instruction 52 and is shown as a single microinstruction loop. The address in the pipeline register would be 52. Instruction 51 in this example could be the LOAD COUNTER AND CONTINUE instruction (number 12). While the example shows a single microinstruction loop, by simply changing the address in a pipeline register, multi-instruction loops can be performed in this manner for a fixed number of times as determined by the counter.

Instruction 10 is the conditional RETURN-FROM-SUBROUTINE instruction. As the name implies, this instruction is used to branch from the subroutine back to the next microinstruction address following the subroutine call. Since this instruction is conditional, the return is performed only if the test is passed. If the test is failed, the next sequential microinstruction is performed. The example in Figure 4 depicts the use of the conditional RETURN-FROM-SUBROUTINE instruction in both the conditional and the unconditional modes. This example first shows a jump-to-subroutine at instruction location 52 where control is transferred to location 90. At location 93, a conditional RETURN-FROM-SUBROUTINE instruction is performed. If the test is passed, the stack is accessed and the program will transfer to the next instruction at address 53. If the test is failed, the next microinstruction at address 94 will be executed. The program will continue to address 97 where the subroutine is complete. To perform an unconditional RETURN-FROM-SUBROUTINE, the conditional RETURN-FROM-SUBROUTINE instruction is executed unconditionally; the microinstruction at address 97 is programmed to force

THE Am2910 INSTRUCTION SET (Cont.)

$\overline{CCEN}$ HIGH, disabling the test and the forced PASS causes an unconditional return.

Instruction 11 is the CONDITIONAL JUMP PIPELINE register address and POP stack instruction. This instruction provides another technique for loop termination and stack maintenance. The example in Figure 4 shows a loop being performed from address 55 back to address 51. The instructions at locations 52, 53, and 54 are all conditional JUMP and POP instructions. At address 52, if the TEST input is passed, a branch will be made to address 70 and the stack will be properly maintained via a POP. Should the test fail, the instruction at location 53 (the next sequential instruction) will be executed. Likewise, at address 53, either the instruction at 90 or 54 will be subsequently executed, respective to the test being passed or failed. The instruction at 54 follows the same rules, going to either 80 or 55. An instruction sequence as described here, using the CONDITIONAL JUMP PIPELINE and POP instruction, is very useful when several inputs are being tested and the microprogram is looping waiting for any of the inputs being tested to occur before proceeding to another sequence of instructions. This provides the powerful jump-table programming technique at the firmware level.

Instruction 12 is the LOAD COUNTER AND CONTINUE instruction, which simply enables the counter to be loaded with the value at its parallel inputs. These inputs are normally connected to the pipeline branch address field which (in the architecture being described here) serves to supply either a branch address or a counter value depending upon the microinstruction being executed. There are altogether three ways of loading the counter — the explicit load by this instruction 12; the conditional load included as part of instruction 4; and the use of the $\overline{RLD}$ input along with any instruction. The use of $\overline{RLD}$ with any instruction overrides any counting or decrementation specified in the instruction, calling for a load instead. Its use provides additional microinstruction power, at the expense of one bit of microinstruction width. This instruction 12 is exactly equivalent to the combination of instruction 14 and $\overline{RLD}$ LOW. Its purpose is to provide a simple capability to load the register/counter in those implementations which do not provide microprogrammed control for $\overline{RLD}$.

Instruction 13 is the TEST END-OF-LOOP instruction, which provides the capability of conditionally exiting a loop at the bottom; that is, this is a conditional instruction that will cause the microprogram to loop, via the file, if the test is failed else to continue to the next sequential instruction. The example in Figure 4 shows the TEST END-OF-LOOP microinstruction at address 56. If the test fails, the microprogram will branch to address 52. Address 52 is on the stack because a PUSH instruction had been executed at address 51. If the test is passed at instruction 56, the loop is terminated and the next sequential microinstruction at address 57 is executed, which also causes the stack to be POP'd; thus, accomplishing the required stack maintenance.

Instruction 14 is the CONTINUE instruction, which simply causes the microprogram counter to increment so that the next sequential microinstruction is executed. This is the simplest microinstruction of all and should be the default instruction which the firmware requests whenever there is nothing better to do.

Instruction 15, THREE-WAY BRANCH, is the most complex. It provides for testing of both a data-dependent condition and the counter during one microinstruction and provides for selecting among one of three microinstruction addresses as the next microinstruction to be performed. Like instruction 8, a previous instruction will have loaded a count into the register/counter while pushing a microbranch address onto the stack. Instruction 15 performs a decrement-and-branch-until-zero function similar to instruction 8. The next address is taken from the top of the stack until the count reaches zero; then the next address comes from the pipeline register. The above action continues as long as the test condition fails. If at any execution of instruction 15 the test condition is passed, no branch is taken; the microprogram counter register furnishes the next address. When the loop is ended, either by the count becoming zero, or by passing the conditional test, the stack is POP'd by decrementing the stack pointer, since interest in the value contained at the top of the stack is then complete.

The application of instruction 15 can enhance performance of a variety of machine-level instructions. For instance, (1) a memory search instruction to be terminated either by finding a desired memory content or by reaching the search limit; (2) variable-field-length arithmetic terminated early upon finding that the content of the portion of the field still unprocessed is all zeroes; (3) key search in a disc controller processing variable length records; (4) normalization of a floating point number.

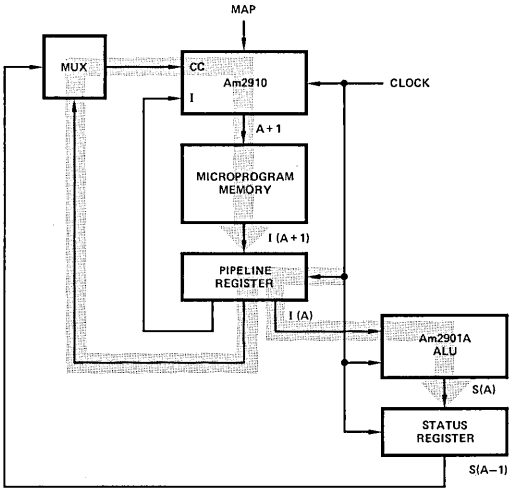
As one example, consider the case of a memory search instruction. As shown in Figure 4, the instruction at microprogram address 63 can be Instruction 4 (PUSH), which will push the value 64 onto the microprogram stack and load the number N, which is one less than the number of memory locations to be searched before giving up. Location 64 contains a microinstruction which fetches the next operand from the memory area to be searched and compares it with the search key. Location 65 contains a microinstruction which tests the result of the comparison and also is a THREE-WAY BRANCH for microprogram control. If no match is found, the test fails and the microprogram goes back to location 64 for the next operand address. When the count becomes zero, the microprogram branches to location 72, which does whatever is necessary if no match is found. If a match occurs on any execution of the THREE-WAY BRANCH at location 65, control falls through to location 66 which handles this case. Whether the instruction ends by finding a match or not, the stack will have been POP'd once, removing the value 64 from the top of the stack.

ARCHITECTURES USING THE Am2910

(Shading shows path(s) which usually limit speed)

Figure 5.

One Level Pipeline Based
(Recommended)



One level pipeline provides better speed than most other architectures. The μProgram Memory and the Am2901A array are in parallel speed paths instead of in series. This is the recommended architecture for Am2900 designs.

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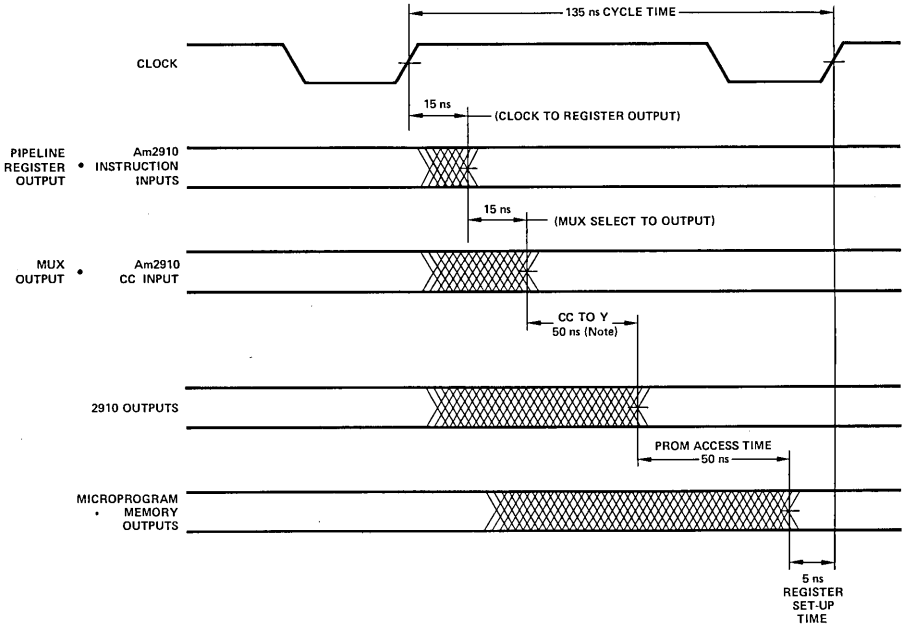

Typical CCU Cycle Timing Waveforms.

This drawing shows the timing relationships in the CCU illustrated above.

(Note: 50 ns figure is an estimate of what worst case delay will be for the $\overline{CC}$ to Y path)

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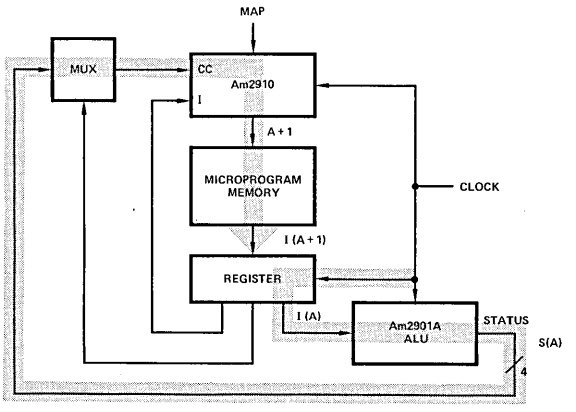
OTHER ARCHITECTURES USING THE Am2910

(Shading shows path(s) which usually limit speed)

Figure 6.

A. Instruction Based



A Register at the Microprogram Memory output contains the microinstruction being executed. The microprogram memory and Am2901A delay are in series. Conditional branches are executed on same cycle as the ALU operation generating the condition.

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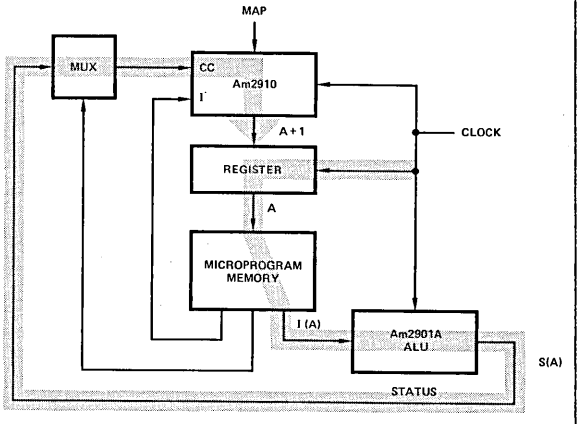
B. Addressed Based



The Register at the Am2910 output contains the address of the microinstruction being executed. The Microprogram Memory and Am2901A are in series in the critical path. This architecture provides about the same speed as the Instruction based architecture, but requires fewer register bits, since only the address (typically 10-12 bits) is stored instead of the instruction (typically 40-60 bits).

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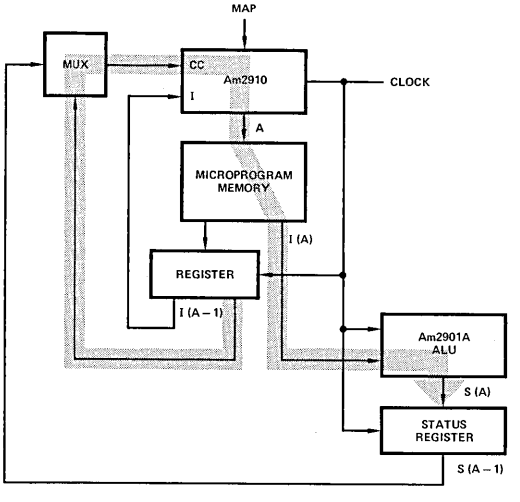
C. Data Based



The Status Register provides conditional Branch control based on results of previous ALU cycle. The Microprogram Memory and Am2901A are in series in the critical paths.

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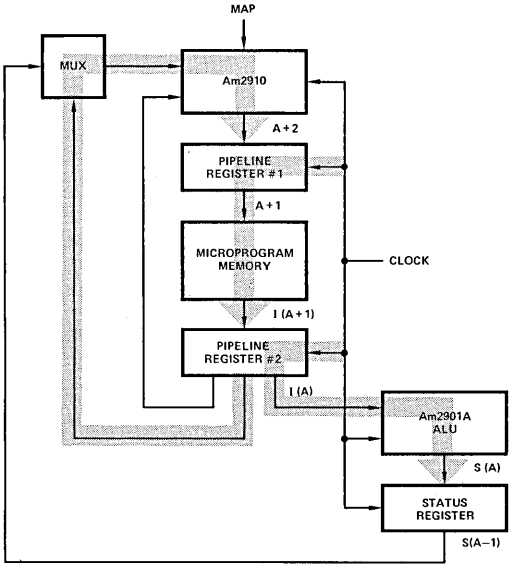
D. Two Level Pipeline Based



Two level pipeline provides highest possible speed. It is more difficult to program because the selection of a microinstruction occurs two instructions ahead of its execution.

MPR-117

Am2913

Priority Interrupt Expander

Distinctive Characteristics

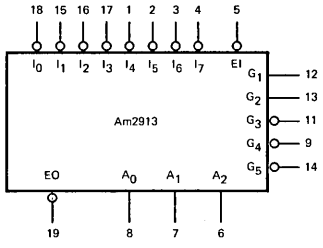
- Encodes eight lines to three-line binary
- Expands use of Am2914
- Cascadable
- Similar in function to Am54LS/74LS/25LS148/2513
- Gated three-state output
- Advanced Low-Power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Low-Power Schottky Priority Interrupt Expander is an extention of the Am2900 series of Bipolar Processor family and is used to expand and prioritize the output of the Am2914 Priority Interrupt circuit. Affording an increase of vectored priority interrupt in groups of eight, this unit accepts active LOW inputs and produces a three-state active HIGH output prioritized from active $\overline{I_7}$ to $\overline{I_0}$. The output is gated by five control signals, three active LOW and two active HIGH. Also provided is a cascade input ($\overline{EI}$) and Enable Output ($\overline{EO}$).

One Am2913 will accept and encode group signal lines from up to 8 Am2914's (64 levels of interrupt). Additional Am2913's may be used to encode more interrupt levels.

LOGIC SYMBOL



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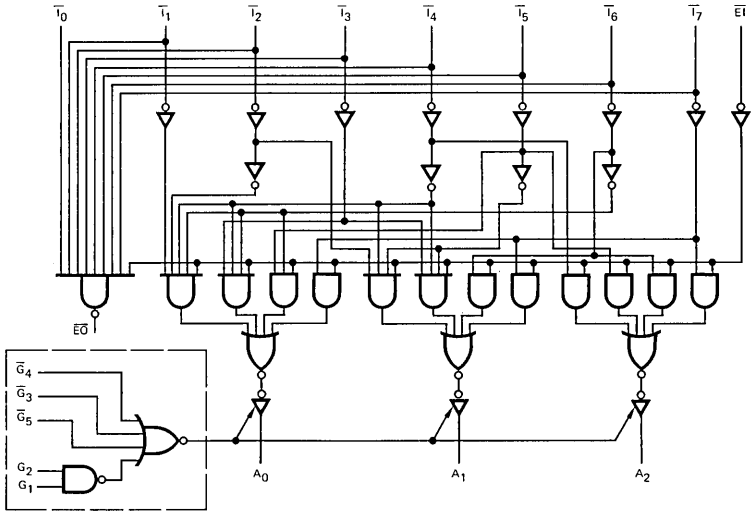
LOGIC DIAGRAM



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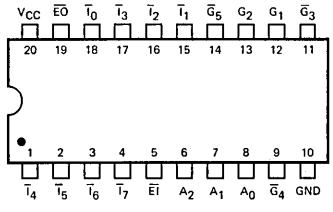
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75V	MAX. = 5.25V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50V	MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$		2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$		2.4	3.2		
			$\overline{EO}$, $I_{OH} = -440\mu A$	MIL	2.5	3.4		
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 12mA (A_n$ Outputs)				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$	$\overline{EI}, G_1, G_2, \overline{G_3}, \overline{G_4}, \overline{G_5}, \overline{I_0}$				0.4	mA
			All others				0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$	$\overline{EI}, G_1, G_2, \overline{G_3}, \overline{G_4}, \overline{G_5}, \overline{I_0}$				20	μA
			All others				40	
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$	$\overline{EI}, G_1, G_2, \overline{G_3}, \overline{G_4}, \overline{G_5}, \overline{I_0}$				0.1	mA
			All others				0.2	
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				15	24	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs and outputs open.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2913PC	P-20	C	C-1
AM2913DC	D-20	C	C-1
AM2913DC-B	D-20	C	B-1
AM2913DM	D-20	M	C-3
AM2913DM-B	D-20	M	B-3
AM2913FM	F-20	M	C-3
AM2913FM-B	F-20	M	B-3
AM2913XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2913XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	$\overline{I_i}$ to A_n (In-phase)		17	25	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			17	25		
t_{PLH}	$\overline{I_i}$ to A_n (Out-phase)		11	17	ns	
t_{PHL}			12	18		
t_{PLH}	$\overline{I_i}$ to $\overline{EO}$		7.0	11	ns	
t_{PHL}			24	36		
t_{PLH}	$\overline{EI}$ to $\overline{EO}$		11	17	ns	
t_{PHL}			23	34		
t_{PLH}	$\overline{EI}$ to A_n		12	18	ns	
t_{PHL}			14	21		
t_{ZH}	G_1 or G_2 to A_n		23	40	ns	
t_{ZL}			20	37		
t_{ZH}	$\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to A_n		20	30	ns	
t_{ZL}			18	27		
t_{HZ}	G_1 or G_2 to A_n		17	27	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			19	28		
t_{HZ}	$\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to A_n		16	24	ns	
t_{LZ}			18	27		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am2913 COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am2913 COM'L Max.	Am2913 MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am2913 MIL Max.	Units	Test Conditions
t_{PLH}	$\overline{I_i}$ to A_n (In-phase)		31		37	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			30		34		
t_{PLH}	$\overline{I_i}$ to A_n (Out-phase)		22		27	ns	
t_{PHL}			22		25		
t_{PLH}	$\overline{I_i}$ to $\overline{EO}$		15		18	ns	
t_{PHL}			48		60		
t_{PLH}	$\overline{EI}$ to $\overline{EO}$		19		21	ns	
t_{PHL}			46		57		
t_{PLH}	$\overline{EI}$ to A_n		22		25	ns	
t_{PHL}			27		32		
t_{ZH}	G_1 or G_2 to A_n		42		49	ns	
t_{ZL}			43		49		
t_{ZH}	$\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to A_n		36		43	ns	
t_{ZL}			35		43		
t_{HZ}	G_1 or G_2 to A_n		34		40	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			34		40		
t_{HZ}	$\overline{G_3}$, $\overline{G_4}$, $\overline{G_5}$ to A_n		30		35	ns	
t_{LZ}			31		35		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

Note: i = 0 to 7
n = 0 to 2

DEFINITIONS OF FUNCTIONAL TERMS

A0, A1, A2	Three-state, active high encoder outputs
$\overline{EI}$	Enable input provided to allow cascaded operation
$\overline{EO}$	Enable output provided to enable the next lower order priority chip
G_1, G_2	Active high three-state output controls
$\overline{G}_3$, $\overline{G}_4$, $\overline{G}_5$	Active low three-state output controls
$\overline{I}_{0\text{-}7}$	Active low encoder inputs

TRUTH TABLE

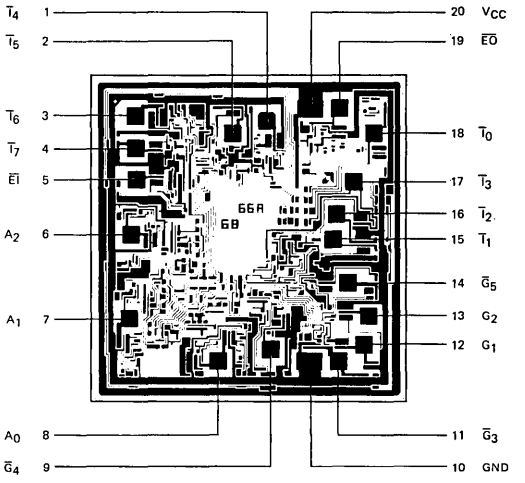
Inputs									Outputs			
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	A_0	A_1	A_2	$\overline{EO}$
H	X	X	X	X	X	X	X	X	L	L	L	H
L	H	H	H	H	H	H	H	H	L	L	L	L
L	X	X	X	X	X	X	X	L	H	H	H	H
L	X	X	X	X	X	X	L	H	L	H	H	H
L	X	X	X	X	X	L	H	H	H	L	H	H
L	X	X	X	X	L	H	H	H	L	L	H	H
L	X	X	X	L	H	H	H	H	H	H	L	H
L	X	X	L	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
For G_1 = H, G_2 = H, G_3 = L, G_4 = L, G_5 = L

G1	G2	$\overline{G3}$	$\overline{G4}$	$\overline{G5}$	A_0	A_1	A_2
H	H	L	L	L	Enabled		
L	X	X	X	X	Z	Z	Z
X	L	X	X	X	Z	Z	Z
X	X	H	X	X	Z	Z	Z
X	X	X	H	X	Z	Z	Z
X	X	X	X	H	Z	Z	Z

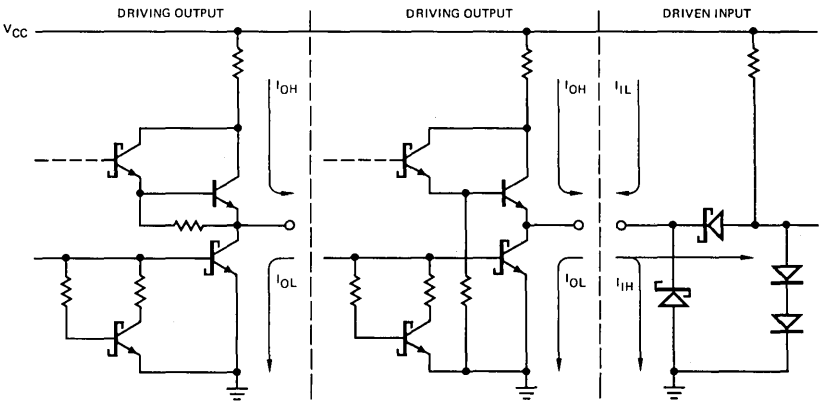
Z = HIGH Impedance

Metallization and Pad Layout



DIE SIZE 0.082" X 0.085"

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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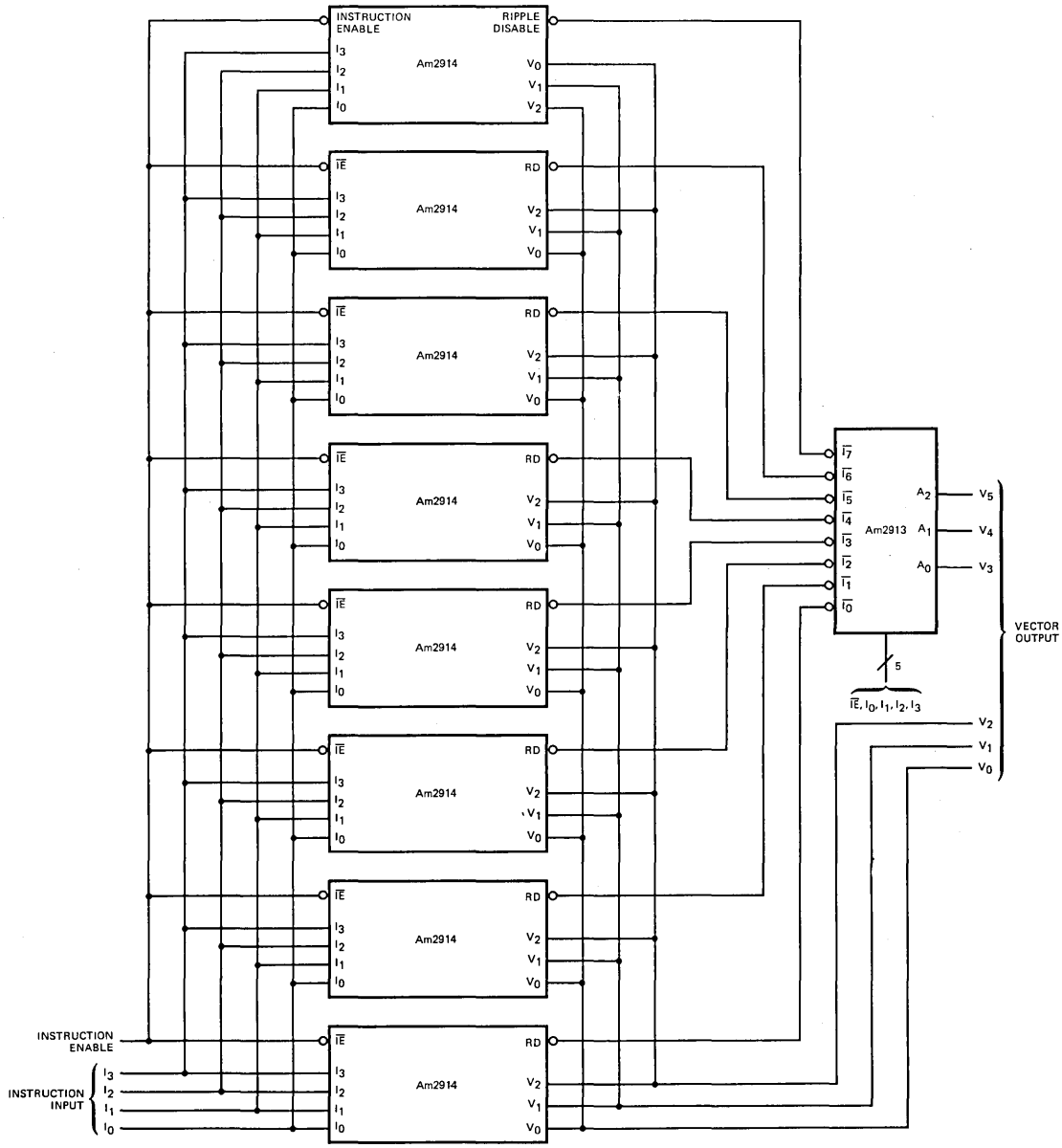
APPLICATION



Shown above is the connection of the instruction lines and vector output lines in a 64-input priority interrupt system. The Am2913 is used to encode the most significant bits associated with the vector output.

MPR-122

Am2914

Vectored Priority Interrupt Controller

DISTINCTIVE CHARACTERISTICS

- Accepts 8 interrupt inputs
  Interrupts may be pulses or levels and are stored internally
- Built-in mask register
  Six different operations can be performed on mask register
- Built-in status register
  Status register holds code for lowest allowed interrupt
- Vectored output
  Output is binary code for highest priority un-masked interrupt
- Expandable
  Any number of Am2914's may be stacked for large interrupt systems
- Microprogrammable
  Executes 16 different microinstructions
  Instruction enable pin aids in vertical microprogramming
- High-speed operation
  Delay from an interrupt clocked into the interrupt register to interrupt request output is typically 60 ns

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AC Characteristics 2-111
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FUNCTIONAL DESCRIPTION

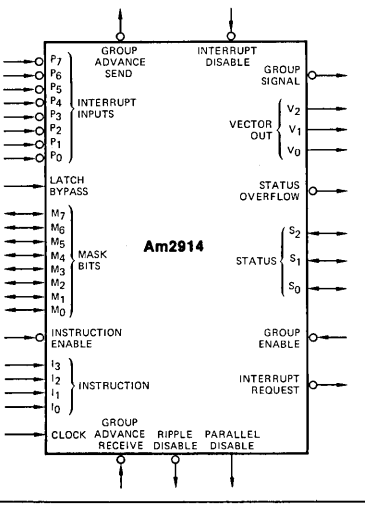
The Am2914 is a high-speed, eight-bit priority interrupt unit that is cascadable to handle any number of priority interrupt request levels. The high-speed of the Am2914 makes it ideal for use in Am2900 family microcomputer designs, but it can also be used with the Am9080A MOS microprocessor.

The Am2914 receives interrupt requests on 8 interrupt input lines (P_0-P_7). A LOW level is a request. An internal latch may be used to catch pulses on these lines, or the latch may be bypassed so the request lines drive the edge-triggered interrupt register directly. An 8-bit mask register is used to mask individual interrupts. Considerable flexibility is provided for controlling the mask register. Requests in the interrupt register are ANDed with the corresponding bits in the mask register and the results are sent to an 8-input priority encoder, which produces a three bit encoded vector representing the highest numbered input which is not masked.

An internal status register is used to point to the lowest priority at which an interrupt will be accepted. The contents of the status register are compared with the output of the priority encoder, and an interrupt request output will occur if the vector is greater than or equal to status. Whenever a vector is read from the Am2914 the status register is automatically updated to point to one level higher than the vector read. (The status register can be loaded externally or read out at any time using the S pins.) Signals are provided for moving the status upward across devices (Group Advance Send and Group Advance Receive) and for inhibiting lower priorities from higher order devices (Ripple Disable, Parallel Disable, and Interrupt Disable). A status overflow output indicates that an interrupt has been read at the highest priority.

The Am2914 is controlled by a 4-bit instruction field I_0-I_3. The command on the instruction lines is executed if IE is LOW and is ignored if IE is HIGH, allowing the 4 I bits to be shared with other devices.

LOGIC SYMBOL



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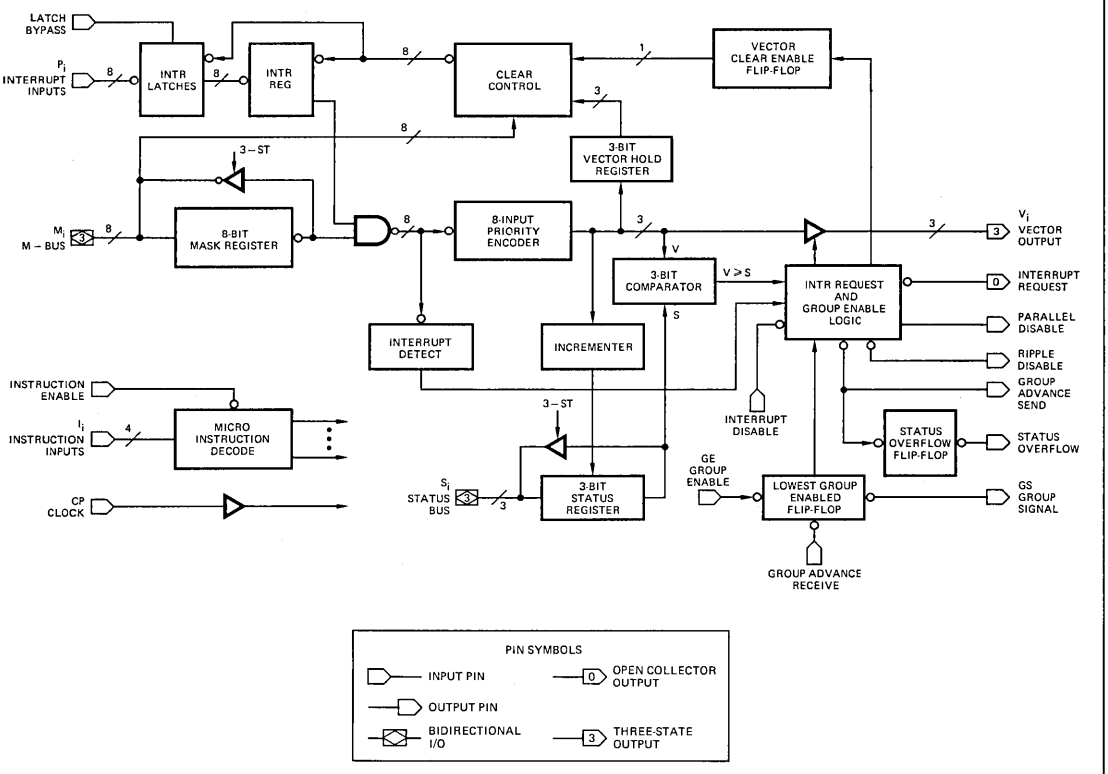
BLOCK DIAGRAM



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BLOCK DIAGRAM DESCRIPTION

The Microinstruction Decode circuitry decodes the Interrupt Microinstructions and generates required control signals for the chip.

The Interrupt Register holds the Interrupt Inputs and is an eight-bit, edge-triggered register which is set on the rising edge of the CP Clock signal.

The Interrupt latches are set/reset-type latches. When the Latch Bypass signal is LOW, the latches are enabled and act as negative pulse catchers on the inputs to the Interrupt Register. When the Latch Bypass signal is HIGH, the Interrupt latches are transparent.

The Mask Register holds the eight mask bits associated with the eight interrupt levels. The register may be loaded from or read to the M Bus. Also, the entire register or individual mask bits may be set or cleared.

The Interrupt Detect circuitry detects the presence of any unmasked Interrupt Input. The eight-input Priority Encoder determines the highest priority, non-masked Interrupt Input and forms a binary coded interrupt vector. Following a Vector Read, the three-bit Vector Hold Register holds the binary coded interrupt vector. This stored vector is used for clearing interrupts.

The three-bit Status Register holds the status bits and may be loaded from or read to the S Bus. During a Vector Read, the Incrementer increments the interrupt vector by one, and the result is clocked into the Status Register. Thus the Status Register always points to the lowest level at which an interrupt will be accepted.

The three-bit Comparator compares the Interrupt Vector with the contents of the Status Register and indicates if the Interrupt Vector is greater than or equal to the contents of the Status Register.

The Lowest Group Enabled Flip-Flop is used when a number of 2914's are cascaded. In a cascaded system, only one Lowest Group Enabled Flip-Flop is LOW at a time. It indicates the eight interrupt group, which contains the lowest priority interrupt level which will be accepted and is used to form the higher order status bits.

The Interrupt Request and Group Enable logic contain various gating to generate the Interrupt Request, Parallel Disable, Ripple Disable, and Group Advance Send signals.

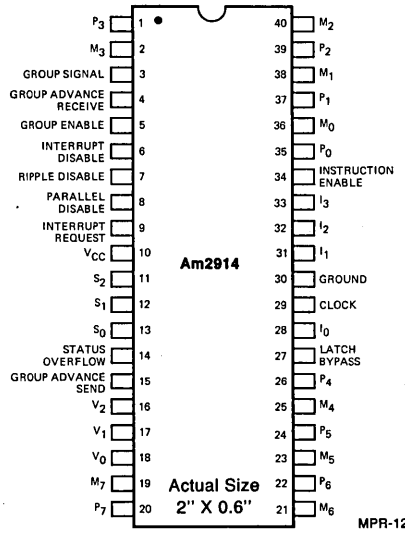
The Status Overflow signal is used to disable all interrupts. It indicates the highest priority interrupt vector has been read and the Status Register has overflowed.

The Clear Control logic generates the eight individual clear signals for the bits in the Interrupt Latches and Register. The Vector Clear Enable Flip-Flop indicates if the last vector read was from this group. When it is set, it enables the Clear Control Logic.

The CP clock signal is used to clock the Interrupt Register, Mask Register, Status Register, Vector Hold Register, and the Lowest Group Enabled, Vector Clear Enable and Status Overflow Flip-Flops, all on the clock LOW-to-HIGH transition.

CONNECTION DIAGRAMS – Top Views

DIP



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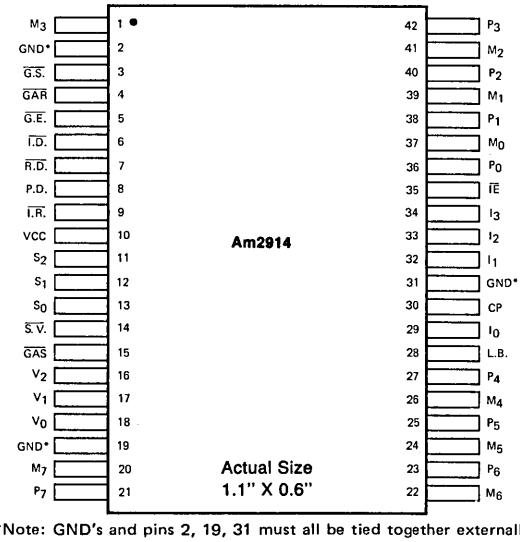
Flat Package



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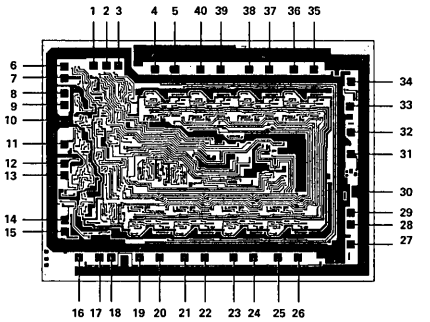
*Note: GND's and pins 2, 19, 31 must all be tied together externally.

Note: Pin 1 is marked for orientation.

Metallization and Pad Layout



DIE SIZE
133 mm X 187 mm

Numbers correspond to DIP pin-out.

TABLE I
MICROINSTRUCTION SET FOR Am2914 PRIORITY INTERRUPT CIRCUIT

Decimal $I_3I_2I_1I_0$	Mnemonic	Instruction
		Mask Register Functions
14	LDM	Load mask register from M bus
7	RDM	Read mask register to M bus
12	CLRM	Clear mask register (enables all priorities)
8	SETM	Set mask register (inhibits all interrupts)
10	BCLRM	Bit clear mask register from M bus
11	BSETM	Bit set mask register from M bus
		Status Register Functions
9	LDSTA	Load status register from S bus and LGE flip-flop from GE input
6	RDSTA	Read status register to S bus
		Interrupt Request Control
15	ENIN	Enable interrupt request
13	DISIN	Disable interrupt request
		Vectored Output
5	RDVC	Read vector output to V outputs, load V+1 into status register, load V into vector hold register and set vector clear enable flip-flop.
		Priority Interrupt Register Clear
1	CLRIN	Clear all interrupts
3	CLRMR	Clear interrupts from mask register data (uses the M bus)
2	CLRMB	Clear interrupts from M bus data
4	CLRVC	Clear the individual interrupt associated with the last vector read
		Master Clear
0	MCLR	Clear all interrupts, clear mask register, clear status register, clear LGE flip-flop, enable interrupt request.

STANDARD SCREENING

(Conforms to MIL-STD-883 for Class C Parts)

Step	MIL-STD-883 Method	Conditions	Level	
			Am2914PC, DC	Am2914DM, FM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C 24-hour 150°C	100%	100%
Temperature Cycle	1010	C −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B 10,000 G	100% *	100%
Fine Leak	1014	A 5×10^{-8} atm-cc/sec	100% *	100%
Gross Leak	1014	C2 Fluorocarbon	100% *	100%
Electrical Test Subgroups 1 and 7	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening here for Class B Parts				
Group A Sample Tests	5005	See below for definitions of subgroups. Maximum accept number is 3		
Subgroup 1			LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 7
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 7

*Not applicable for Am2914PC.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2914PC	P-40	C	C-1
AM2914DC	D-40	C	C-1
AM2914DC-B	D-40	C	B-1
AM2914DM	D-40	M	C-3
AM2914DM-B	D-40	M	B-3
AM2914FM	F-42	M	C-3
AM2914FM-B	F-42	M	B-3
AM2914XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2914XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.

2. C = 0°C to +70°C, M = −55°C to +125°C.

3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	+0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to 5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

P/N	Temperature	V_{CC}
Am2914PC, DC	0°C to +70°C	4.75V to 5.25V
Am2914DM, FM	−55°C to +125°C	4.50V to 5.50V

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

(Group A, Subgroups 1, 2, and 3)

Am2914XC T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (COM'L) MIN. = 4.75V MAX. = 5.25V

Am2914XM T_C = −55°C to +125°C V_{CC} = 5.0V ± 10% (MIL) MIN. = 4.50V MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −1.0mA		2.4			Volts
			COM'L, I_{OH} = −2.6mA		2.4			
I_{CEX}	Output Leakage Current for IR Output	V_{CC} = MIN., V_O = 5.5V					250	µA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA				0.4	Volts
			I_{OL} = 8.0mA				0.45	
			I_{OL} = 12mA				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	$\overline{M}_{0-7}$				−0.15	mA
			$\overline{S}_{0-2}$				−0.1	
			L. B.				−0.4	
			$\overline{I. D.}$				−2.0	
			All Others				−0.8	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V	$\overline{IE}$, $\overline{GE}$, $\overline{GAR}$, $\overline{S}_{0-2}$				40	µA
			$\overline{M}_{0-7}$, $\overline{I. D.}$				60	
			All Others				20	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_O	Off-State Output Current	V_{CC} = MAX.	V_{OUT} = 0.5V	$\overline{M}_{0-7}$			−150	µA
				$\overline{S}_{0-2}$			−100	
				V_{0-2}			−50	
			V_{OUT} = 2.4V	$\overline{M}_{0-7}$			150	
				$\overline{S}_{0-2}$			100	
				V_{0-2}			50	
I_{CC}	Power Supply Current	V_{CC} = 5.0V, 25°C				170	−	mA
		V_{CC} = MAX.	COM'L	0°C			305	
				70°C			250	
			MIL	−55°C			310	
				125°C			200	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−40		−100	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS AT 25°C AND 5.0 VOLTS

Note: Guaranteed limits at 25°C and 5.0V are group A, subgroup 9 tests
All outputs fully loaded. C_L = 50pF. Measurements made at 1.5V with
input levels of 0V and 3.0V. All numbers are in ns.
For interrupt request output, R_L = 470Ω

TABLE I. CLOCK AND INTERRUPT INPUT PULSE WIDTHS (ns)

Time	GUARANTEED
Minimum Clock LOW Time	30
Minimum Clock HIGH Time	30
Minimum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Acceptance (Pulse Mode)	25
Maximum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Rejection (Pulse Mode)	10

TABLE II. COMBINATIONAL PROPAGATION DELAYS (ns)

	TYPICAL						GUARANTEED					
From Input \ To Output	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send
$\overline{IE}$	36	40	40	–	–	30	48	55	55	–	–	47
I_{0123}	36	40	40	–	–	30	48	55	55	–	–	47
Irpt. Disable	–	–	25	35	8	19	–	–	37	42	13	23

R_L = 2.0kΩ, C_L = 15pF

TABLE III. DELAYS FROM CLOCK TO OUTPUTS (ns)

Clock Path	TYPICAL							GUARANTEED						
	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$
Irpt Latches and Register	55	65	37	39	47	–	–	67	82	57	57	66	–	–
Mask Register	55	65	37	39	47	–	–	67	82	57	57	66	–	–
Status Register	45	55	28	31	37	–	–	59	74	57	57	58	–	–
Lowest Group Enabled Flip-Flop	–	–	22	25	–	–	17	–	–	42	45	–	–	32
Irpt Request Enable Flip-Flop	–	40	–	–	–	–	–	–	56	–	–	–	–	–
Status Overflow Flip-Flop	–	–	–	–	–	17	–	–	–	–	–	–	25	–

TABLE IV. SET-UP AND HOLD TIME REQUIREMENTS (ns)

(All relative to clock LOW-to-HIGH transition)

From Input	GUARANTEED	
	Set-up Time	Hold Time
S-Bus	11	8
M-Bus	11	8
$\overline{P_0}$-$\overline{P_7}$	11	6
Latch Bypass	16	0
$\overline{IE}$ I_{0123} (See Note)	46 t_{pwL} + 29	0
$\overline{GE}$	11	11
$\overline{GAR}$	11	11
$\overline{Irpt\ Disable}$	35	0
P_0-P_7 Hold Time Relative to LB	–	16

Note: t_{pwL} is the Clock LOW Time. Both Set-up times must be met.

SWITCHING CHARACTERISTICS OVER OPERATING VOLTAGE AND TEMPERATURE RANGE

(Group A, subgroup 10 and 11 tests and limits)

All outputs fully loaded, C_L = 50pF. Measurements made at 1.5V with input levels of 0V and 3.0V. For Interrupt Request Output, R_L = 470Ω.

TABLE V. CLOCK AND INTERRUPT INPUT PULSE WIDTHS (ns)

Time	Am2914PC, DC, XC T_A = 0°C to +70°C, 5V ± 5%	Am2914DM, FM, XM T_C = –55°C to +125°C, 5V ± 10%
Minimum Clock LOW Time	30	30
Minimum Clock HIGH Time	30	30
Minimum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Acceptance (Pulse Mode)	40	40
Maximum Interrupt Input (P_0-P_7) LOW Time for Guaranteed Rejection (Pulse Mode)	8	8
Minimum Clock Period, $\overline{IE}$ = H on current cycle and previous cycle	50	55
Minimum Clock Period, $\overline{IE}$ = L on current cycle or previous cycle	100	110

TABLE VI. MAXIMUM COMBINATIONAL PROPAGATION DELAYS (ns)

	Am2914PC, DC, XC T_A = 0°C to +70°C, 5V ± 5%						Am2914DM, FM, XM T_C = –55°C to +125°C, 5V ± 10%					
From Input \ To Output	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send	M Bus	S Bus	V_{012}	Irpt Req	Ripple Disable	Group Advance Send
$\overline{IE}$	52	60	60	–	–	56	60	68	68	–	–	62
I_{0123}	52	60	60	–	–	56	60	68	68	–	–	62
Irpt. Disable	–	–	40	52	14	27	–	–	46	60	15	33

R_L = 2.0kΩ, C_L = 15pF

TABLE VII. MAXIMUM DELAYS FROM CLOCK TO OUTPUTS (ns)

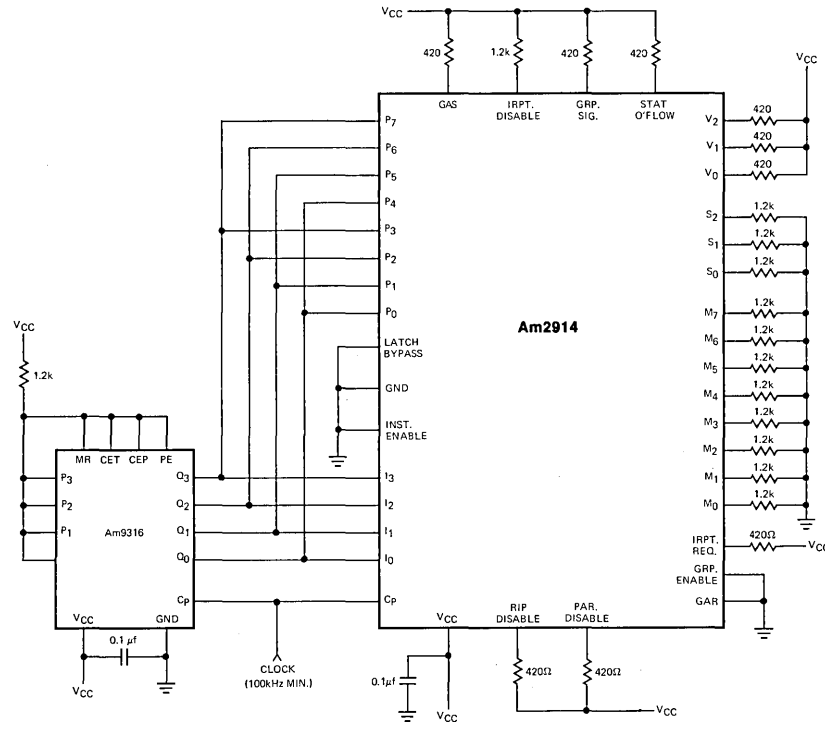
Clock Path	Am2914PC, DC, XC T_A = 0°C to +70°C, 5V ± 5%							Am2914DM, FM, XM T_C = –55°C to +125°C, 5V ± 10%						
	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$	To V_{012}	To Irpt Req	To PD	To $\overline{RD}$	To $\overline{GAS}$	To Status O'flow	To $\overline{GS}$
Irpt Latches and Register	76	97	67	67	80	–	–	82	105	75	75	85	–	–
Mask Register	76	97	67	67	80	–	–	82	105	75	75	85	–	–
Status Register	67	88	63	63	70	–	–	73	96	66	66	76	–	–
Lowest Group Enabled Flip-Flop	–	–	48	52	–	–	38	–	–	54	58	–	–	45
Irpt Request Enable Flip-Flop	–	62	–	–	–	–	–	–	66	–	–	–	–	–
Status Overflow Flip-Flop	–	–	–	–	–	30	–	–	–	–	–	–	35	–

TABLE VIII. SET-UP AND HOLD TIME REQUIREMENTS (ns)

(All relative to clock LOW-to-HIGH transition)

From Input	Am2914PC, DC, XC T_A = 0°C to +70°C, 5V ± 5%		Am2914DM, FM, XM T_C = –55°C to +125°C, 5V ± 10%	
	Set-Up Time	Hold Time	Set-Up Time	Hold Time
S-Bus	15	10	15	10
M-Bus	15	10	15	10
$\overline{P_0}$-$\overline{P_7}$	15	8	15	8
Latch Bypass	20	0	20	0
$\overline{IE}$ I_{0123} (See Note)	55 t_{pwL} + 33	0	55 t_{pwL} + 40	0
$\overline{GE}$	15	13	15	13
$\overline{GAR}$	15	13	15	13
Irpt Disable	42	0	42	0
P_0-P_7 Hold Time Relative to LB	—	20	—	20

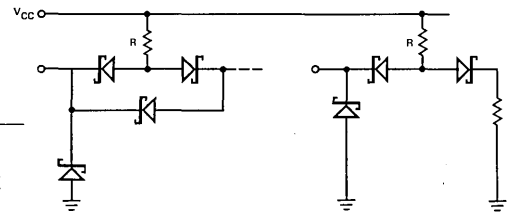
Note: t_{pwL} is the Clock LOW Time. Both Set-up times must be met.



Am2914 Burn-in Circuit

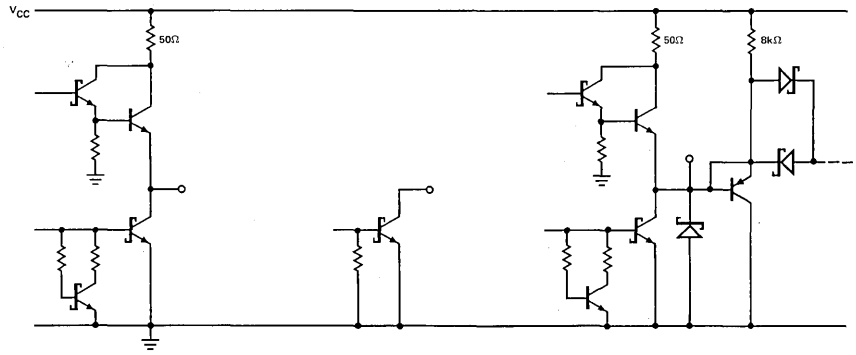
MPR-127

INPUT/OUTPUT CIRCUITS



INPUT	R
I_0-I_3, CP, $\overline{GE}$, $\overline{GAR}$	10K
$\overline{LB}$	20K
$\overline{IE}$	6.7K
$\overline{ID}$	4K

INPUT	R
$\overline{P_7}$-$\overline{P_0}$	10K



OUTPUTS	
V_0-V_3	$\overline{SO}$
$\overline{GAS}$	PD
$\overline{GS}$	$\overline{RD}$

OUTPUT
$\overline{IR}$

OUTPUTS
M_0-M_7
S_0-S_3

MPR-128

A MICROPROGRAMMABLE, BIPOLAR, LSI INTERRUPT STRUCTURE USING THE Am2914

INTRODUCTION

Advanced Micro Devices' introduction of the Am2914 Vectored Priority Interrupt Controller now makes possible the structuring of a microprogrammable bipolar LSI interrupt system. The design engineer may use the Am2914 to simplify his design process, dramatically reduce the system cost, size and package count, and increase the speed, capability and reliability of his interrupt system.

The Am2914 is a modular, low cost, standard LSI component that may be microprogrammed to meet the requirements of specific applications. Today's engineer may utilize the Am2914 microprogrammability to provide functional flexibility and ease of engineering change, while taking advantage of its modularity to provide hardware regularity and future expansion capability.

THE INTERRUPT CONCEPT

In any state machine, a requirement exists for the efficient synchronization and response to asynchronous events such as power failure, machine malfunctions, control panel service requests, external timer signals, supervisory calls, program errors, and input/output device service requests. The merit of such an "asynchronous event handler" may be measured in terms of response time, system throughput, real time overhead, hardware cost and memory space required.

The simplest approach to asynchronous event handling is the poll approach. A status indicator is associated with each possible asynchronous event. The processor tests each indicator in sequence and, in effect, "asks" if service is required. This program-driven method is inefficient for a number of reasons. Much time is consumed polling when no service is required; programs must have frequent test points to poll indicators, and since indicators are polled in sequence, considerable time may elapse before the processor responds to an event. Thus, system throughput is low; real time overhead and response time are high, and a large memory space is required.

The interrupt method is a much more efficient way of servicing asynchronous requests. An asynchronous event requiring service generates an interrupt request signal to the processor. When the processor receives the interrupt request, it may suspend the program it is currently executing, execute an interrupt service routine which services the asynchronous request, then resume the execution of the suspended program. In this system, the execution of the service routine is initiated by an interrupt request; thus, the system is interrupt driven and service routines are executed only when service is requested. Although hardware cost may be higher in this type of system, it is more efficient since system throughput is higher, response time is faster, real time overhead is lower and less memory space is required.

INTERRUPT SYSTEM FUNCTIONAL DEFINITION

A complete and clear functional definition is key to the design of a good interrupt system. The following features are useful.

Multiple Interrupt Request Handling: Since interrupt requests are generated from a number of different sources, the interrupt system's ability to handle interrupt requests from several sources is important.

Interrupt Request Prioritization: Since the processor can service only one interrupt request at a time, it is important that the interrupt system has the ability to prioritize the requests and determine which has the highest priority.

Interrupt Service Routine "Nesting": This feature allows an interrupt service routine for a given priority request to be interrupted in turn, but only by a higher priority interrupt request. The service routine for the higher priority request is executed, then the execution of the interrupted service routine is resumed. If there are "n" interrupt requests, an "n" deep "nest" is possible.

Dynamic Interrupt Enabling/Disabling: The ability to enable/disable all interrupts "on the fly" under microprogram control can be used to prevent interruption of certain processes.

Dynamic Interrupt Request Masking: The ability to selectively inhibit or "mask" individual interrupt requests under microprogram control is useful.

Interrupt Request Vectoring: Many times, a particular interrupt request requires the execution of a unique interrupt service routine. For this reason, the generation of a unique binary coded vector for each interrupt request is very helpful. This vector can be used as a pointer to the start of a unique service routine.

Interrupt Request Priority Threshold: The ability to establish a priority threshold is valuable. In this type of operation, only those interrupt requests which have higher priority than a specified threshold priority are accepted. The threshold priority can be defined by microprogram or can be automatically established by hardware at the interrupt currently being serviced plus one. This automatic threshold prevents multiple interrupts from the same source. Also useful is the ability to read the threshold priority under microprogram control. Thus, the interrupt request being serviced may be determined by the microprogram.

Interrupt Request Clearing Flexibility: Flexibility in the method of clearing interrupt requests allows different modes of interrupt system operation. Of particular value are the abilities to clear the interrupt currently being serviced, clear all interrupts, or clear interrupts via a programmable mask register or bus.

Microprogrammability: Microprogrammability permits the construction of a general purpose or "universal" interrupt structure which can be microprogrammed to meet a specific application's requirements. The universality of the structure allows standardization of the hardware and amortization of the hardware development costs across a much broader user base. The end result is a flexible, low cost interrupt structure.

Hardware Modularity: Modular interrupt system hardware is beneficial in two ways. First, hardware modularity provides expansion capability. Additional modules may be added as the need to service additional requests arises. Secondly, hardware modularity provides a structural regularity which simplifies the system structure and also reduces the number of hardware part numbers.

Fast Interrupt System Response Time: Quick interrupt system response provides more efficient system operation. Fast response reduces real time overhead and increases overall system throughput.

INTERRUPT SYSTEM IMPLEMENTATION USING THE Am2914

The Am2914 provides all of the foregoing features on a single LSI chip. The Am2914 is a high-speed, eight-bit priority interrupt unit that is cascadable to handle any number of priority interrupt request levels. The Am2914's high speed is ideal for use in Am2900 Family microcomputer designs, but it can also be used with the Am9080A MOS microprocessor.

The Am2914 receives interrupt requests on eight Interrupt Input lines (P_0-P_7). A LOW level is a request. An internal latch may be used to catch pulses (HIGH-LOW-HIGH) on these lines, or the latch may be bypassed so that the request lines drive the D-inputs to the edge-triggered Interrupt Register directly. An eight-bit Mask Register is used to mask individual interrupts. Considerable flexibility is provided for controlling the Mask Register. Requests in the Interrupt Register (P_0-P_7) are ANDed with the corresponding bits in the mask register (M_0-M_7) and the results are sent to an eight-input priority encoder, which produces a three-bit encoded vector representing the highest priority input which is not masked.

An internal Status Register is used to point to the lowest priority at which an interrupt will be accepted. The contents of the Status Register are compared with the output of the priority encoder, and an Interrupt Request output will occur if the vector is greater than or equal to the contents of the Status Register. Whenever a vector is read from the Am2914, the Status Register is automatically updated to point to one level higher than the vector read. (The Status Register can be loaded externally or read out at any time using the S-Bus.) Signals are provided for moving the status upward across devices (Group Advance Send and Group Advance Receive) and for inhibiting lower priorities from higher order devices (Ripple Disable, Parallel Disable, and Interrupt Disable). A Status Overflow output indicates that an interrupt has been read at the highest priority.

The Am2914 is controlled by a four-bit microinstruction field I_0-I_3. The microinstruction is executed if $\overline{IE}$ (Instruction Enable) is LOW and is ignored if $\overline{IE}$ is HIGH, allowing the four I bits to be shared with other functions. Sixteen different microinstructions are executed. Figure 2 shows the microinstructions and the microinstruction codes.

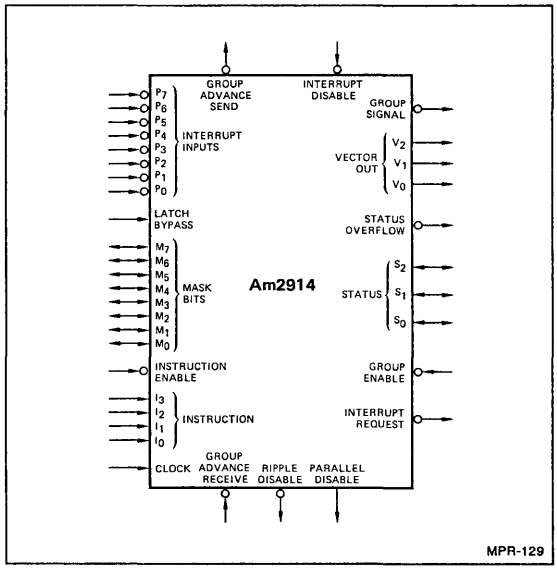


Figure 1. Am2914 Logic Symbol.

MICROINSTRUCTION DESCRIPTION	MICROINSTRUCTION CODE $I_3I_2I_1I_0$
MASTER CLEAR	0000
CLEAR ALL INTERRUPTS	0001
CLEAR INTERRUPTS FROM M-BUS	0010
CLEAR INTERRUPTS FROM MASK REGISTER	0011
CLEAR INTERRUPT, LAST VECTOR READ	0100
READ VECTOR	0101
READ STATUS REGISTER	0110
READ MASK REGISTER	0111
SET MASK REGISTER	1000
LOAD STATUS REGISTER	1001
BIT CLEAR MASK REGISTER	1010
BIT SET MASK REGISTER	1011
CLEAR MASK REGISTER	1100
DISABLE INTERRUPT REQUEST	1101
LOAD MASK REGISTER	1110
ENABLE INTERRUPT REQUEST	1111

Figure 2. Am2914 Microinstruction Set.

In this microinstruction set, the *Master Clear* microinstruction is selected as binary zero so that during a power up sequence, the microinstruction register in the microprogram control unit of the central processor can be cleared to all zeros. Thus, on the next clock cycle, the Am2914 will execute the *Master Clear* function. This includes clearing the Interrupt Latches and Register as well as the Mask Register and Status Register. The LGE flip-flop of the least significant group is set LOW because the Group Advance Receive input is tied LOW. All other Group Advance Receive inputs are tied to Group Advance Send outputs and these are forced HIGH during this instruction. This clear instruction also sets the Interrupt Request Enable flip-flop so that a fully interrupt driven system can be easily initiated from any interrupt.

The *Clear All Interrupts* microinstruction clears the Interrupt Latches and Register.

The *Clear Interrupts from Mask Register* microinstruction clears those Interrupt Latches and Register bits which have corresponding Mask Register bits set equal to one. The M-Bus is used by the Am2914 during the execution of this microinstruction and must be floating.

The *Clear Interrupts from M-Bus* microinstruction clears those Interrupt Latches and Register bits which have corresponding M-Bus bits set equal to one.

The *Clear Interrupt, Last Vector Read* microinstruction clears the Interrupt Latch and Register bit associated with the last vector read.

The *Read Vector* microinstruction is used to read the vector value of the highest priority request causing the interrupt. The vector outputs are three-state drivers that are enabled onto the $V_0V_1V_2$ bus during this instruction. This microinstruction also automatically loads the value "vector plus one" into the Status Register. In addition, this instruction sets the Vector Clear Enable flip-flop and loads the current vector value into the Vector Hold Register so that this value can be used by the *Clear Interrupt, Last Vector Read* microinstruction. This allows the user to read the vector associated with the interrupt, and at some later time clear the Interrupt Latch and Register bit associated with the vector read.

The *Load Status Register* microinstruction loads S-Bus data into the Status Register and also loads the LGE flip-flop from the Group Enable input.

During the *Read Status Register* microinstruction, the Status Register outputs are enabled onto the Status Bus (S_0-S_2). The Status Bus is a three-bit, bi-directional, three-state bus.

The *Load Mask Register* microinstruction loads data from the three-state, bi-directional M-Bus into the Mask Register.

The *Read Mask Register* microinstruction enables the Mask Register outputs onto the bi-directional, three-state M-Bus.

The *Set Mask Register* microinstruction sets all the bits in the Mask Register to one. This results in all interrupts being inhibited.

The entire Mask Register is cleared by the *Clear Mask Register* microinstruction. This enables all interrupts subject to the Interrupt Enable flip-flop and the Status Register.

The *Bit Clear Mask Register* microinstruction may be used to selectively clear individual Mask Register bits. This microinstruction clears those Mask Register bits which have corresponding M-Bus bits equal to one. Mask Register bits with corresponding M-Bus bits equal to zero are not affected.

The *Bit Set Mask Register* microinstruction sets those Mask Register bits which have corresponding M-Bus bits equal to one. Other Mask Register bits are not affected.

All Interrupt Requests may be disabled by execution of the *Disable Interrupt Request* microinstruction. This microinstruction resets an Interrupt Request Enable flip-flop on the chip.

The *Enable Interrupt Request* microinstruction sets the Interrupt Enable flip-flop. Thus, Interrupt Requests are enabled subject to the contents of the Mask and Status Registers.

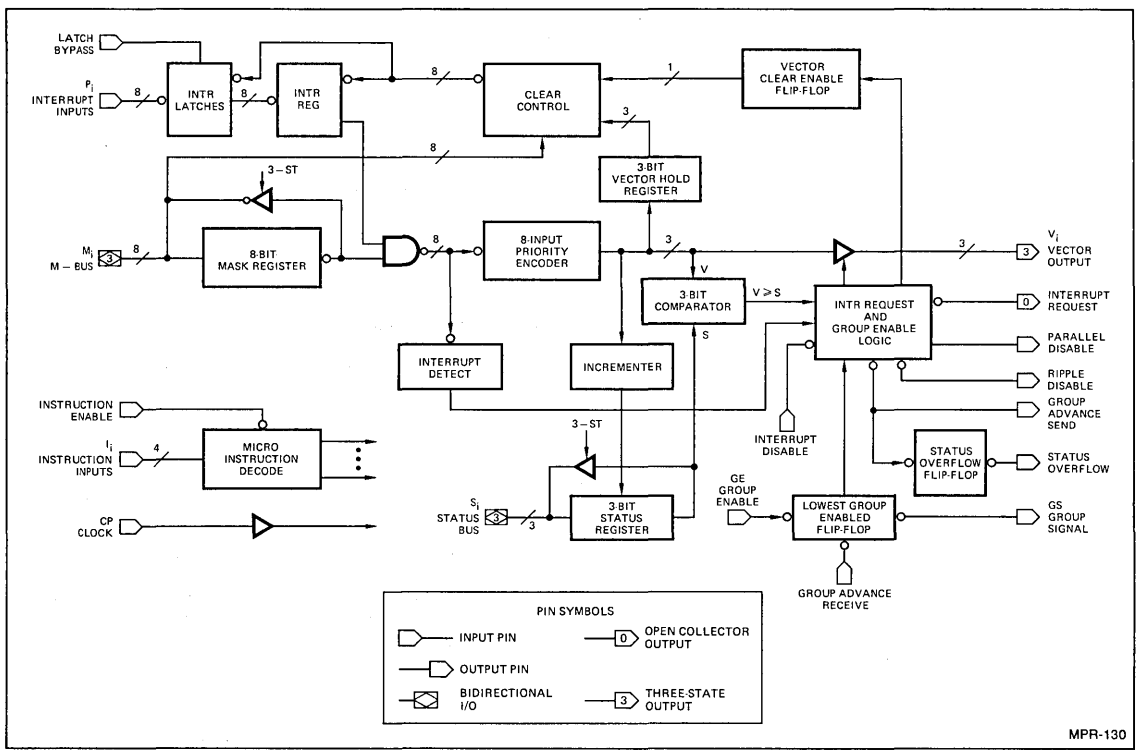


Figure 3. Am2914 Block Diagram.

Am2914 BLOCK DIAGRAM DESCRIPTION

The Am2914 block diagram is shown in Figure 3. The Micro-instruction Decode circuitry decodes the Interrupt Micro-instructions and generates required control signals for the chip.

The Interrupt Register holds the Interrupt Inputs and is an eight-bit, edge-triggered register which is set on the rising edge of the CP Clock signal if the Interrupt Input is LOW.

The Interrupt latches are set/reset latches. When the Latch Bypass signal is LOW, the latches are enabled and act as negative pulse catchers on the inputs to the Interrupt Register. When the Latch Bypass signal is HIGH, the Interrupt latches are transparent.

The Mask Register holds the eight mask bits associated with the eight interrupt levels. The register may be loaded from or read to the M-Bus. Also, the entire register or individual mask bits may be set or cleared.

The Interrupt Detect circuitry detects the presence of any unmasked Interrupt Input. The eight-input Priority Encoder determines the highest priority, non-masked Interrupt Input and forms a binary coded interrupt vector. Following a Vector Read, the three-bit Vector Hold Register holds the binary coded interrupt vector. This stored vector can be used later for clearing interrupts.

The three-bit Status Register holds the status bits and may be loaded from or read to the S-Bus. During a Vector Read, the Incrementer increments the interrupt vector by one, and the result is clocked into the Status Register. Thus, the Status Register points to a level one greater than the vector just read.

The three-bit Comparator compares the Interrupt Vector with the contents of the Status Register and indicates if the Interrupt Vector is greater than or equal to the contents of the Status Register.

The Lowest Group Enabled Flip-Flop is used when a number of Am2914's are cascaded. In a cascaded system, only one Lowest Group Enabled Flip-Flop is LOW at a time. It indicates the eight interrupt group, which contains the lowest priority interrupt level which will be accepted and is used to form the higher order status bits.

The Interrupt Request and Group Enable logic contain various gating to generate the Interrupt Request, Parallel Disable, Ripple Disable, and Group Advance Send signals.

The Status Overflow signal is used to disable all interrupts. It indicates the highest priority interrupt vector has been read and the Status Register has overflowed.

The Clear Control logic generates the eight individual clear signals for the bits in the Interrupt Latches and Register. The Vector Clear Enable Flip-Flop indicates if the last vector read was from this chip. When it is set it enables the Clear Control Logic.

The CP clock signal is used to clock the Interrupt Register, Mask Register, Status Register, Vector Hold Register, and the Lowest Group Enabled, Vector Clear Enable and Status Overflow Flip-Flops, all on the clock LOW-to-HIGH transition.

The Am2914 can be microprogrammed in many different ways. Figure 4 shows an example interrupt sequence. The *Read Vector* microinstruction is necessary in order to read the interrupt priority level. Since vector plus one is automatically loaded into the Status Register when a *Read Vector* microinstruction is executed, the Status Register possibly will overflow and disable all interrupts. For this reason, the Status Register must be reloaded periodically. The other Am2914 microinstructions are optional.

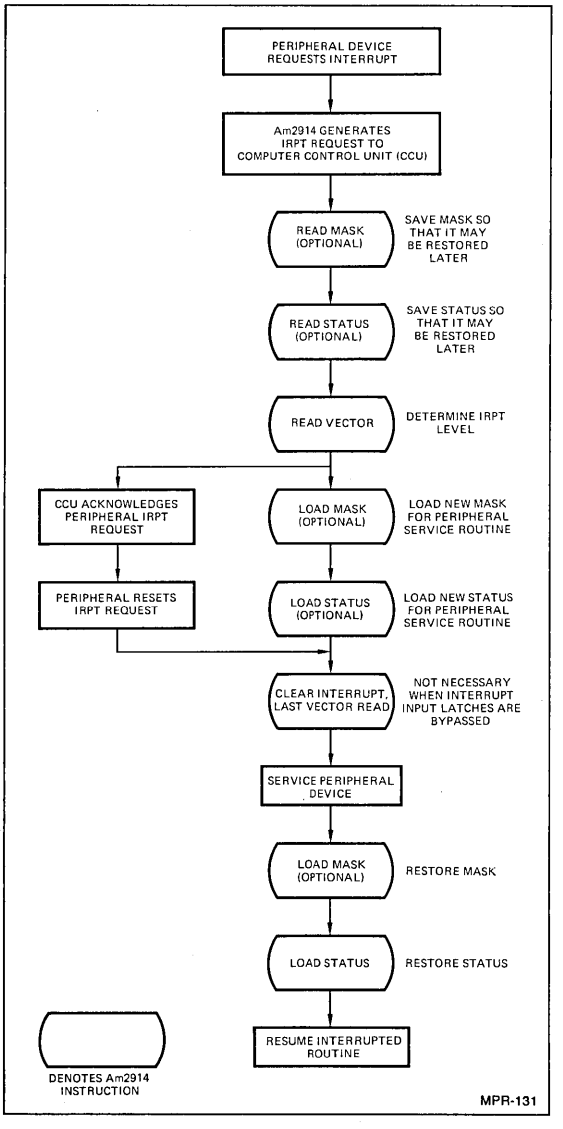


Figure 4. Example Interrupt Sequence.

CASCADING THE Am2914

A number of input/output signals are provided for cascading the Am2914 Vectored Priority Interrupt Encoder. A definition of these I/O signals and their required connections follows:

Group Signal ($\overline{GS}$) – This signal is the output of the Lowest Group Enabled flip-flop and during a Read Status microinstruction is used to generate the high order bits of the Status word.

Group Enable ($\overline{GE}$) – This signal is one of the inputs to the Lowest Group Enable flip-flop and is used to load the flip-flop during the Load Status microinstruction.

Group Advance Send ($\overline{GAS}$) – During a Read Vector microinstruction, this output signal is LOW when the highest priority vector (vector seven) of the group is being read. In a cascaded system Group Advance Send must be tied to the Group Advance Receive input of the next higher group in order to transfer status information.

Group Advance Receive ($\overline{GAR}$) – During a Master Clear or Read Vector microinstruction, this input signal is used with other internal signals to load the Lowest Group Enabled flip-flop. The Group Advance Receive input of the lowest priority group must be tied to ground.

Status Overflow ($\overline{SV}$) – This output signal becomes LOW after the highest priority vector (vector seven) of the group has been read and indicates the Status Register has overflowed. It stays LOW until a Master Clear or Load Status microinstruction is executed. The Status Overflow output of the highest priority group should be connected to the Interrupt Disable input of the same group and serves to disable all interrupts until new status is loaded or the system is master cleared. The Status Overflow outputs of lower priority groups should be left open (see Figure 7).

Interrupt Disable ($\overline{ID}$) – When LOW, this input signal inhibits the Interrupt Request output from the chip and also generates a Ripple Disable output.

Ripple Disable ($\overline{RD}$) – This output signal is used only in the Ripple Cascade Mode (see below). The Ripple Disable output is LOW when the Interrupt Disable input is LOW, the Lowest Group Enabled flip-flop is LOW, or an Interrupt Request is generated in the group. In the ripple cascade mode, the

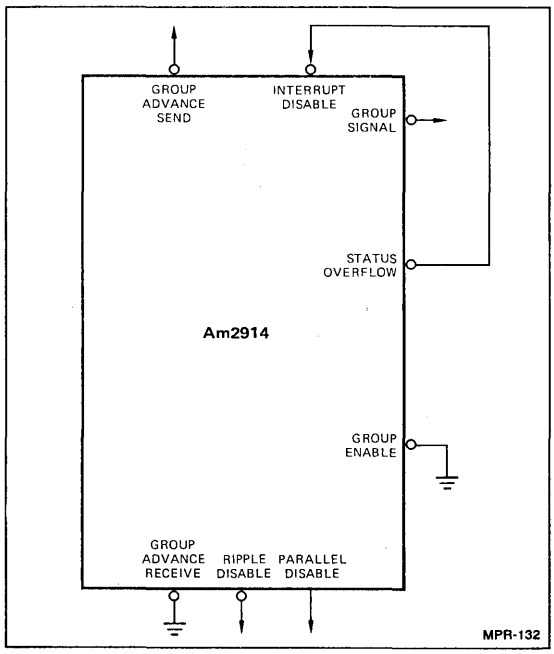


Figure 5. Cascade Lines Connection for Single Chip System.

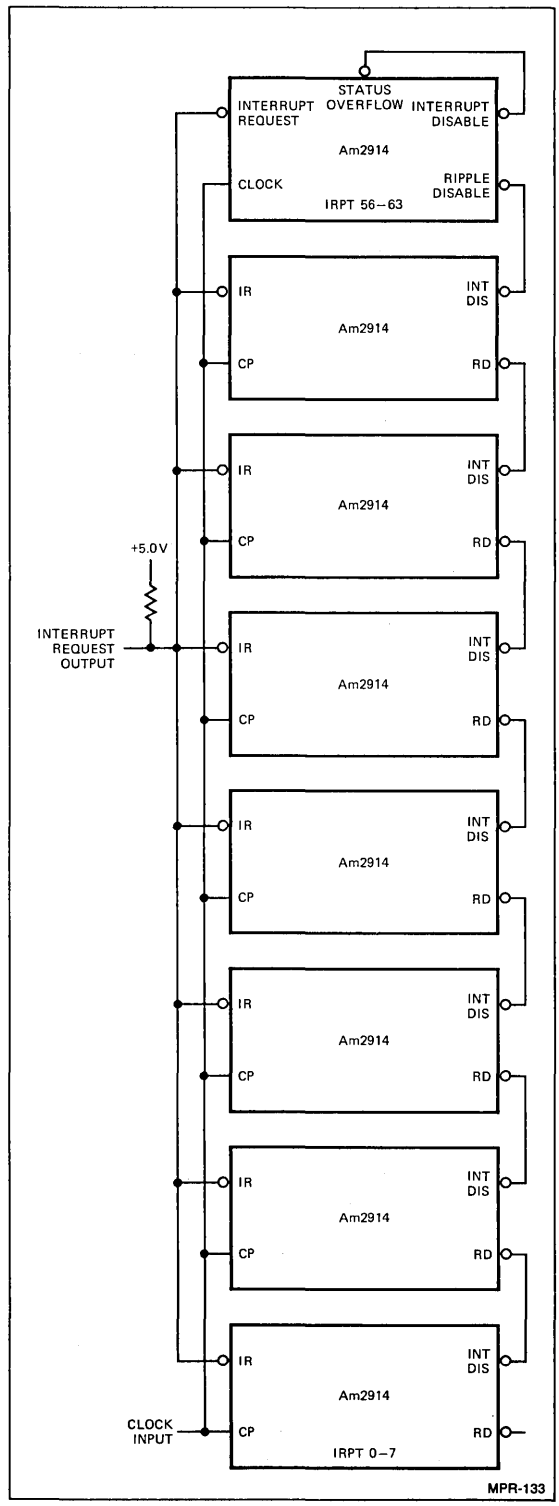


Figure 6. Interrupt Disable Connections for Ripple Cascade Mode.

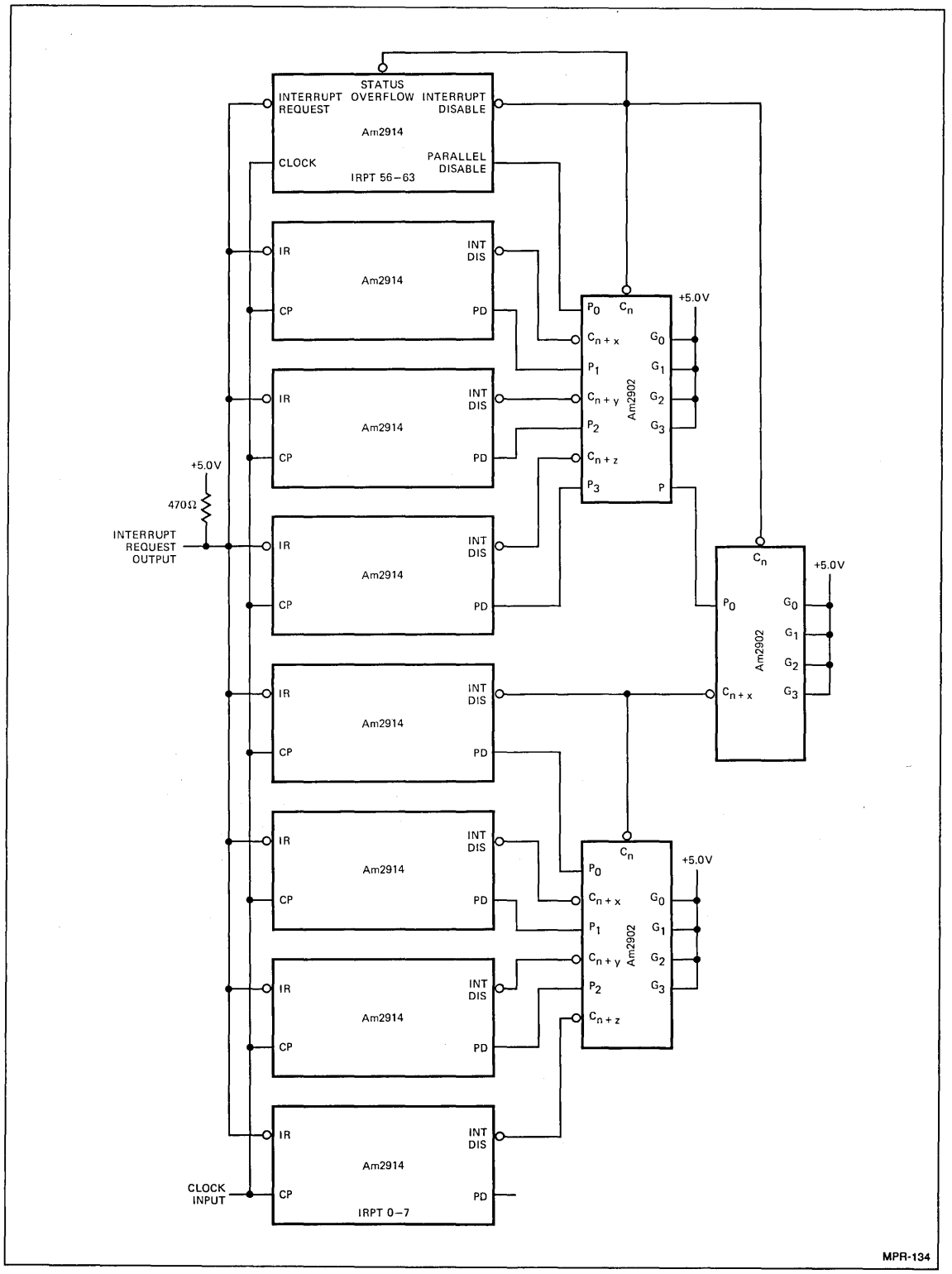


Figure 7. Interrupt Disable Connections for Parallel Cascade Mode.

Ripple Disable output is tied to the Interrupt Disable input of the next lower priority group (see Figure 6).

Parallel Disable (PD) — This output is used only in the parallel cascade mode (see below). It is HIGH when the Lowest Group Enabled flip-flop is LOW or an Interrupt Request is generated in the group. It is not affected by the Interrupt Disable input.

A single Am2914 chip may be used to prioritize and encode up to eight interrupt inputs. Figure 5 shows how the above cascade lines should be connected in such a single chip system.

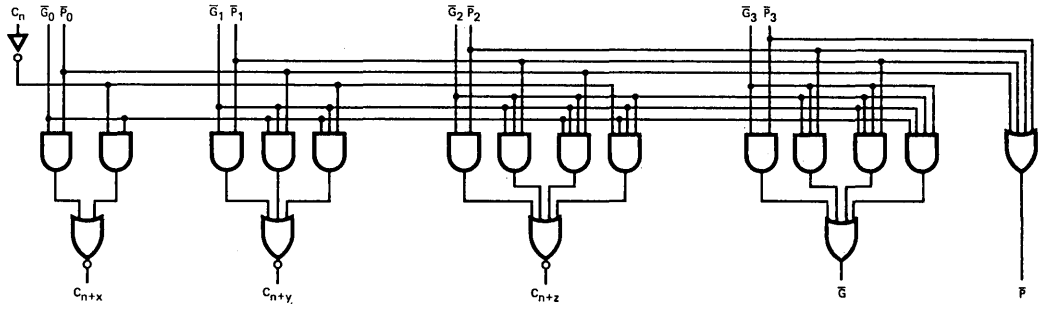
The Group Advance Receive and Group Enable inputs should be connected to ground so that the Lowest Group Enabled flip-flop is forced LOW during a *Master Clear* or *Load Status* microinstruction. Status Overflow should be connected to Interrupt Disable in order to disable interrupts when vector seven is read. The Group Advance Send, Ripple Disable, Group Signal and Parallel Disable pins should be left open.

The Am2914 may be cascaded in either a Ripple Cascade Mode or a Parallel Cascade Mode. In the Ripple Cascade Mode, the Interrupt Disable signal, which disables lower priority interrupts, is allowed to ripple through lower priority groups. Figures 6, 9 and 11 show the cascade connections required for a ripple cascade 64 input interrupt system.

In the parallel cascade mode, a parallel lookahead scheme is employed using the high-speed Am2902 Lookahead Carry Generator. Figures 7, 9 and 10 show the cascade connections required for a parallel cascade 64-input interrupt system. For this application, the Am2902 is used as a lookahead interrupt disable generator. A Parallel Disable output from any group results in the disabling of all lower priority groups in parallel. Figure 8 shows the Am2902 logic diagram and equations.

In Figures 9 and 10, the Am2913 Priority Interrupt Expander is shown forming the high order bits of the vector and status, respectively. The Am2913 is an eight-line to three-line priority encoder with three-state outputs which are enabled by the five output control signals G1, G2, $\overline{G3}$, $\overline{G4}$, and $\overline{G5}$. In Figure 9, the Am2913 is connected so that its outputs are enabled during a Read Vector instruction, and in Figure 10 the Am2913 is connected so that its outputs are enabled during a Read Status instruction. The Am2913 logic diagram and truth table are shown in Figure 11.

The Am25LS138 three-line to eight-line Decoder also is shown in Figure 10. It is used to decode the three high order status bits during a Load Status instruction. The Am25LS138 logic diagram and truth table are shown in Figure 12.



$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$
$$P = P_3P_2P_1P_0$$

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Figure 8. Am2902 Carry Look-Ahead Generator Logic Diagram and Equations.

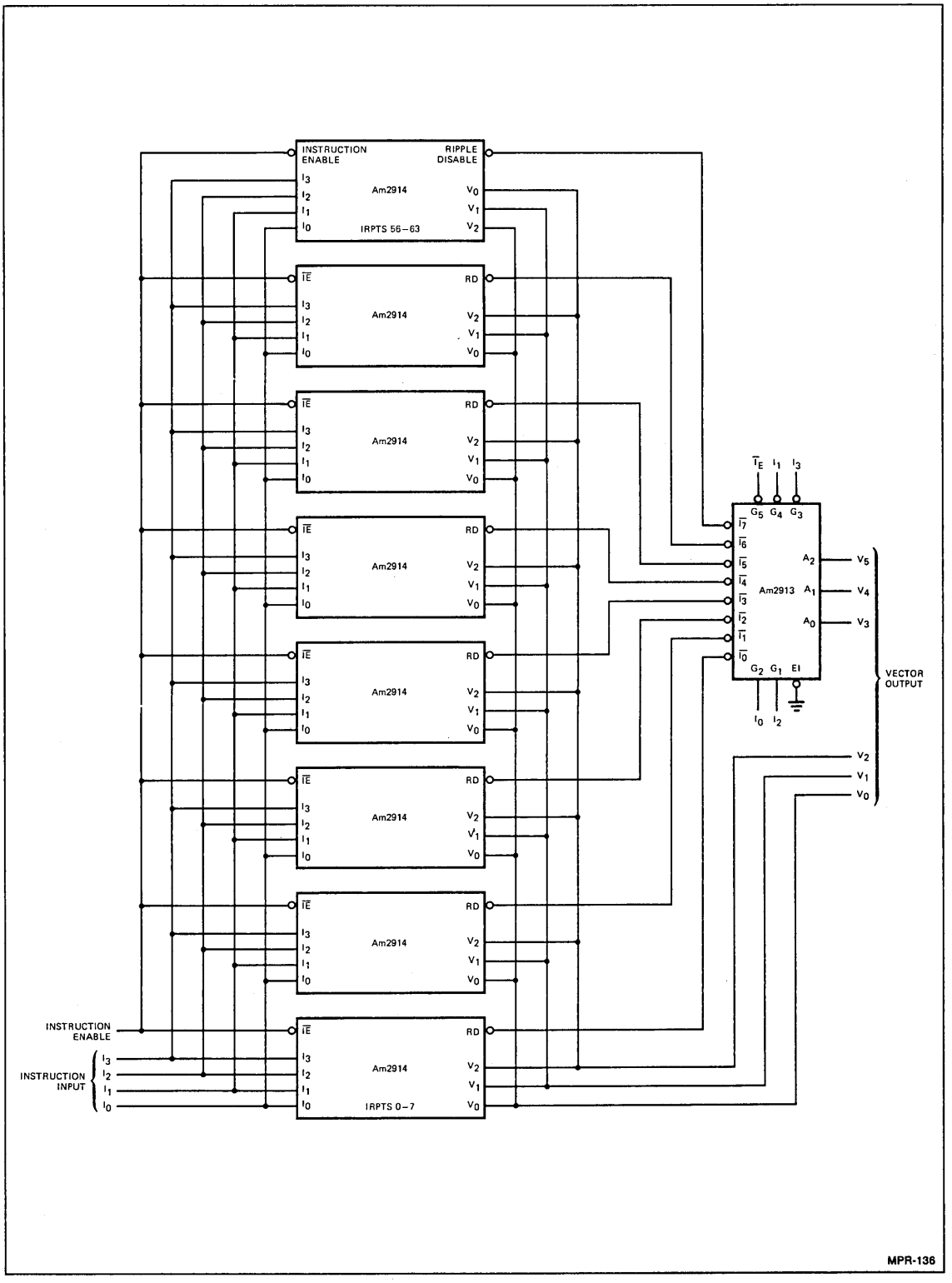


Figure 9. Vector Connections for both the Parallel and Ripple Cascade Modes.

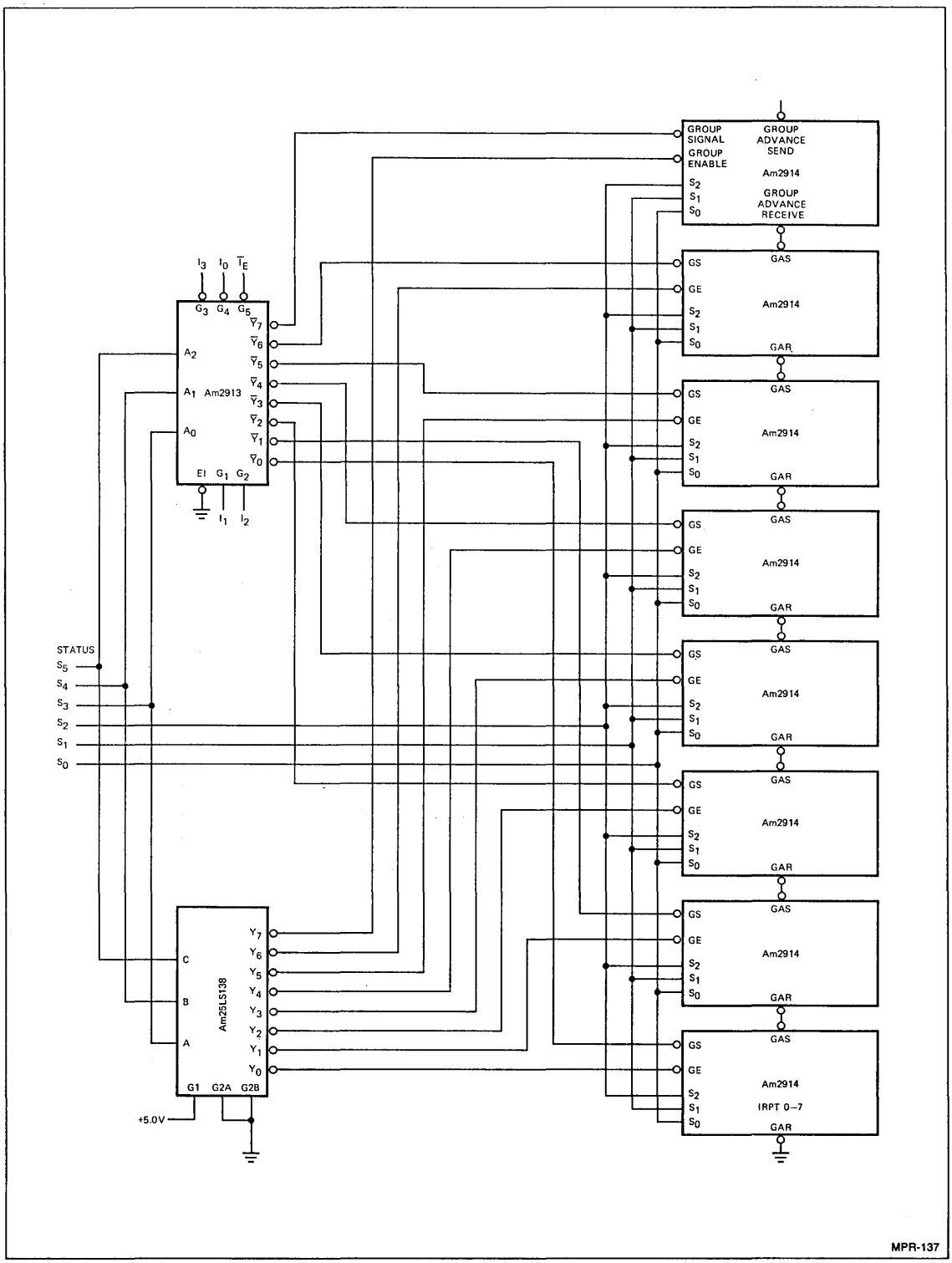
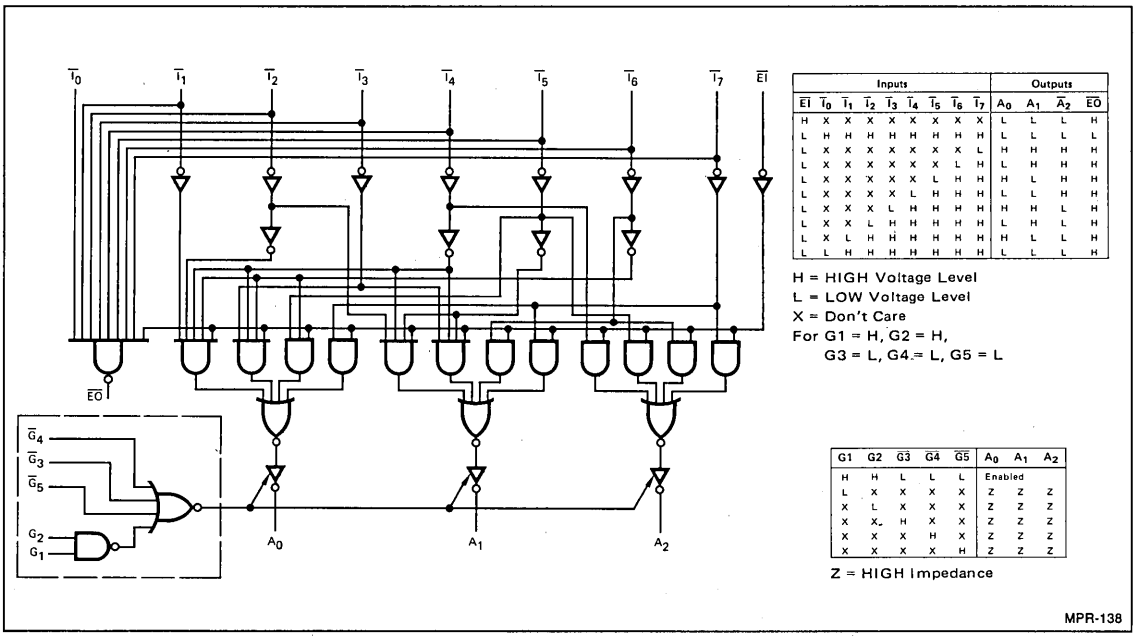


Figure 10. Group Signal, Group Enable, Group Advance Send, Group Advance Receive and Status Connections for Both the Parallel and Ripple Cascade Modes.



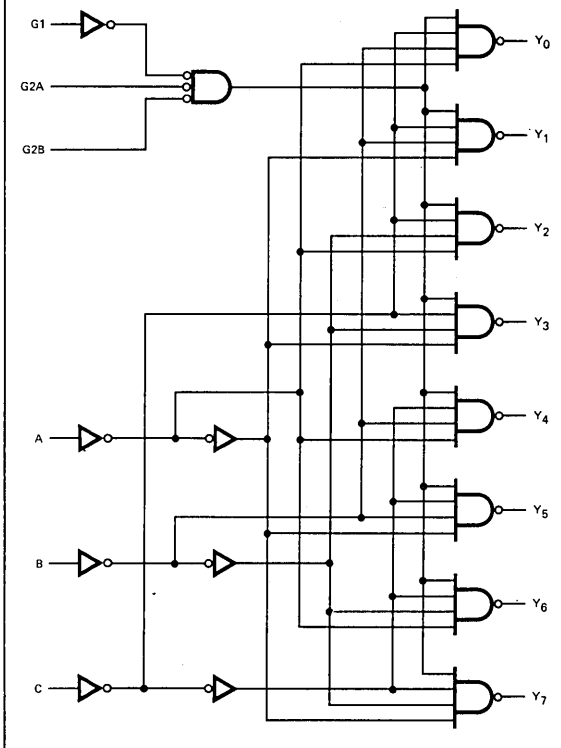
Inputs									Outputs			
$\overline{EI}$	$\overline{I}_0$	$\overline{I}_1$	$\overline{I}_2$	$\overline{I}_3$	$\overline{I}_4$	$\overline{I}_5$	$\overline{I}_6$	$\overline{I}_7$	A_0	A_1	$\overline{A}_2$	$\overline{EO}$
H	X	X	X	X	X	X	X	X	L	L	L	H
L	H	H	H	H	H	H	H	H	L	L	L	L
L	X	X	X	X	X	X	X	L	H	H	H	H
L	X	X	X	X	X	X	L	H	L	H	H	H
L	X	X	X	X	X	L	H	H	H	L	H	H
L	X	X	X	X	L	H	H	H	L	L	H	H
L	X	X	X	L	H	H	H	H	H	H	L	H
L	X	X	L	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	L	L	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
For G1 = H, G2 = H,
G3 = L, G4 = L, G5 = L

G1	G2	$\overline{G3}$	$\overline{G4}$	$\overline{G5}$	A_0	A_1	A_2
H	H	L	L	L	Enabled		
L	X	X	X	X	Z	Z	Z
X	L	X	X	X	Z	Z	Z
X	X	H	X	X	Z	Z	Z
X	X	X	H	X	Z	Z	Z
X	X	X	X	H	Z	Z	Z

Z = HIGH Impedance

Figure 11. Am2913 Priority Interrupt Expander Logic Diagram and Truth Table.



Inputs						Outputs							
Enable			Select										
G1	G2A	G2B	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	H	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = HIGH
L = LOW
X = Don't Care

Figure 12. Am25LS138 3 to 8 Line Decoder Logic Diagram and Truth Table.

EXAMPLE INTERRUPT SYSTEMS DESIGNS FOR AN Am2900 SYSTEM

A classical computer architecture is shown in Figure 13. The Computer Control Unit controls the internal busses and subsystems of the processor, synchronizes internal and external events and grants or denies permission to external systems. The data bus is commonly used by all of the subsystems in the computer. Information, instructions, address operands, data and sometimes control signals are transmitted down the data bus under control of a microprogram. The microprogram selects the source of the data as well as the destination(s) of the data. The Address Bus is typically used to select a word in memory for an internal computer function or to select an input/output port for an external subsystem or peripheral function. The source of the data for the address bus, also selected by microprogram commands, may be the program counter, the memory address register, a direct memory address controller, an interface controller, etc.

The arithmetic/logic unit (ALU) is that portion of the processor that computes. Under control of the microprogram, the ALU performs a number of different arithmetic and logic functions on data in the working registers or from the data bus. The ALU also provides a set of condition codes as a result of the current arithmetic or logic operation. The condition codes, along with other computer status information, are stored in a register for later use by the programmer or computer control unit.

The program counter and the memory address register are the two main sources of memory word and I/O address select data on the address bus. The program counter contains the address of the next instruction or instruction operand that is to be fetched from main memory, and the memory address register contains instruction address operands which are necessary to fetch the data required for the execution of the current instruction.

A subroutine address stack is provided to allow the return address linkage to be handled easily when exiting a subroutine. The address stack is a last-in, first-out stack that is controlled by a jump-to-subroutine, PUSH, or a return-from-subroutine, POP, instruction from the CCU microinstruction word.

The next microprogram address control (NMAC) circuitry controls the generation of microinstruction addresses. Based on microprogram control, interrupt requests, test conditions and commands from a control panel or other processor, the NMAC determines the address of the next microinstruction to be executed.

For a more detailed description of the above portions of the computer, refer to Advanced Micro Devices' Application Note *A Microprogrammed 16 Bit Computer* by James R.W. Clymer.

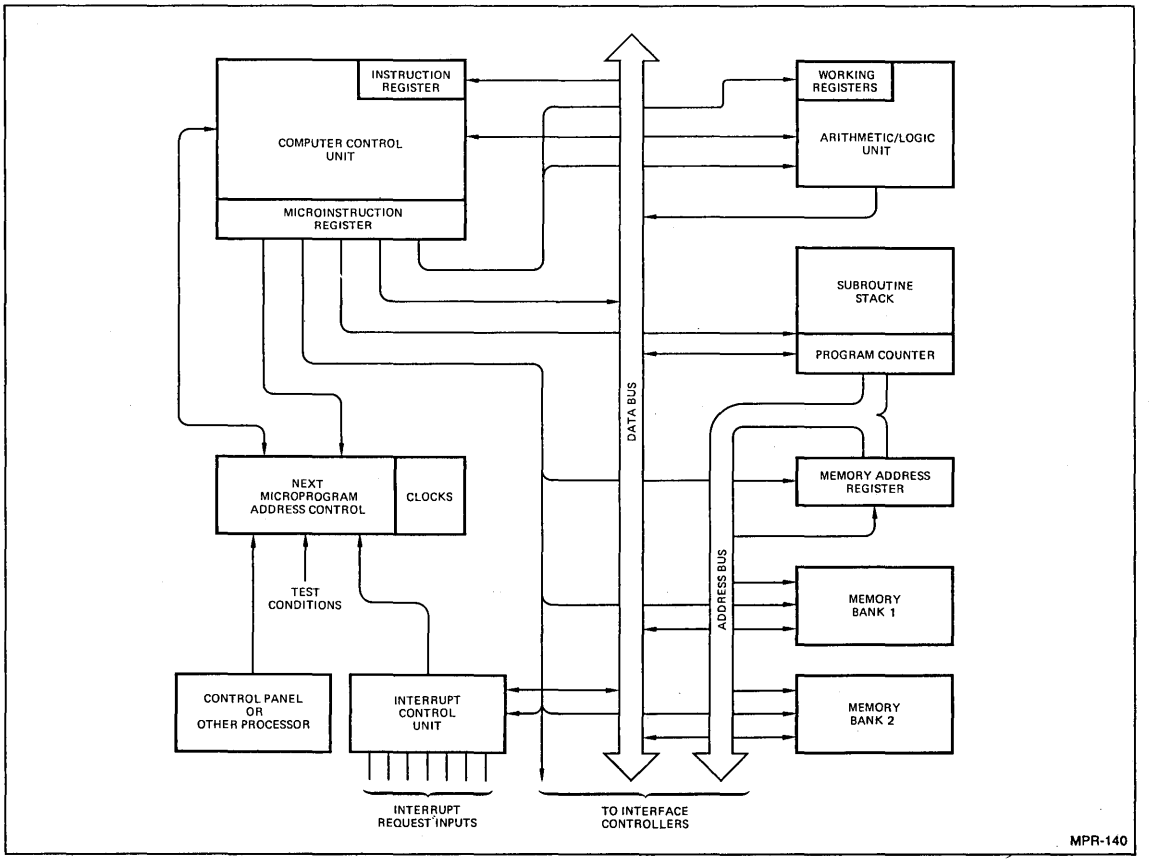


Figure 13. Generalized Computer Architecture.

Figures 14 and 15 show the detailed hardware design of two example interrupt control units (ICU's) for an Am2900 Computer System. Figure 14 shows an eight interrupt level ICU, and Figure 15 shows an ICU which has sixteen levels. In both designs, the Am2914 Instruction inputs and Instruction Enable input are driven by the I_{0-3} field and $\overline{IE}$ bit, respectively, of the Microinstruction Register. Note that Am2914 Instruction inputs are enabled only when the $\overline{IE}$ bit is LOW. Therefore, the I_{0-3} field of the Microinstruction Register may be shared with another functional unit of the computer such as the ALU.

The Latch Bypass input is shown connected to ground so that a LOW-going pulse will be detected at any of the Interrupt Inputs. The Am2914 clock input is driven by the system clock, the same clock used to drive other functional units of the computer.

In both designs, two Am29751 32-word by 8-bit PROMs with three-state outputs are used to map the Am2914 Vector outputs into a 16-bit address vector. The PROM outputs are connected to the data bus so that when an Am2914 Read Vector instruction is executed, the address vector may be gated via the data bus to the Program Counter. At the Program Counter, the address vector may be used as the starting main memory address of a machine instruction interrupt service routine. Figure 16 shows the Computer Control Unit for such a machine program interrupt system.

The address vector also may be gated directly to the "D" inputs of the Am2911 Microprogram Sequencer, and used as the starting PROM address of a microinstruction interrupt service routine. Figure 17 shows the Computer Control Unit for such a microprogram interrupt system. Thus, both the machine program and microprogram can be interrupted and vectored with these designs.

In Figures 15 and 16, the Am2914 Status and Mask inputs/outputs are connected to the data bus in a bi-directional configuration so that the Status and Mask Registers may be loaded from or read to the data bus under Am2914 instruction control. The Am2914 Interrupt Request output, which is open-collector and may be wire-ORed, provides an input to the next microprogram address control circuitry.

For the eight level ICU of Figure 14, the Status Overflow output is connected to the Interrupt Disable input, and the Group Advance Receive and Group Enable inputs are connected to ground, as previously described.

For the 16 interrupt level ICU of Figure 15, the Parallel Disable output of the higher priority group serves as the high order vector bit. An Am2913 Priority Interrupt Expander is gated by the Am2914 instruction lines so that its output is enabled only during a Read Status instruction, and is used to encode the high order bit of the status. An inverter suffices to decode the high order status bit during a Load Status instruction. As described previously for a ripple cascade system, the Group Advance Send output is connected to the Group Advance Receive input of the next higher priority group; the Ripple Disable output is connected to the Interrupt Disable input of the next lower priority group; the Status Overflow output of the highest priority group is connected to the Interrupt Disable input of the same group, and the Group Advance Receive input of the lowest priority group is connected to ground.

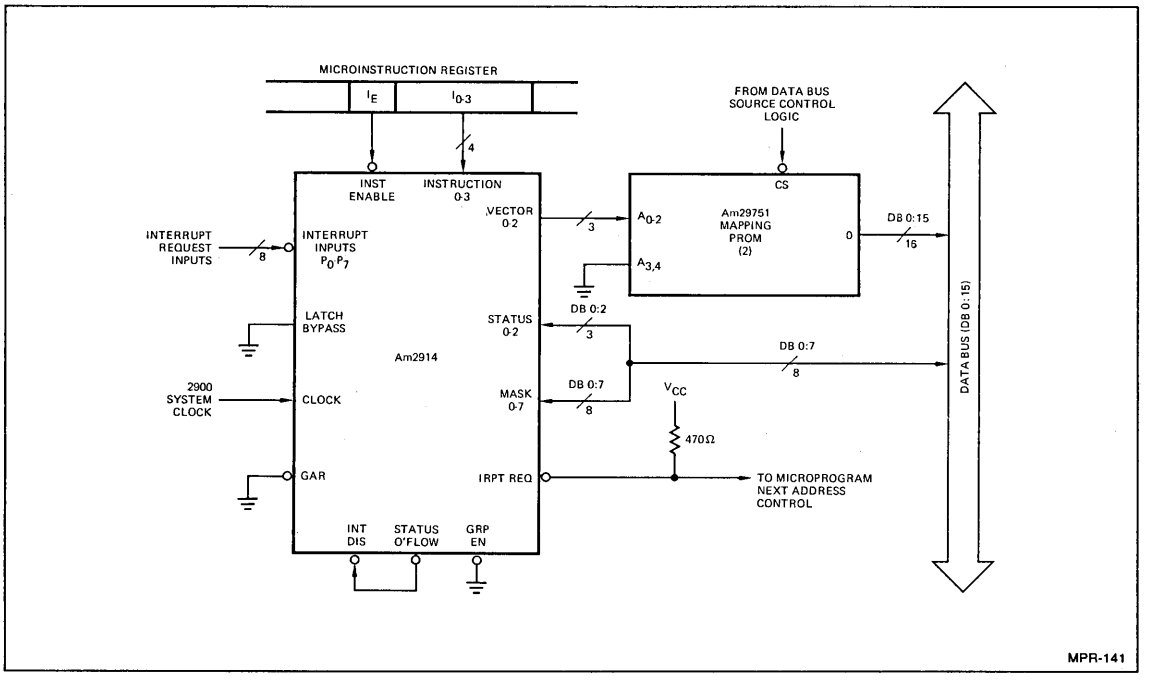


Figure 14. 8 Level Interrupt Control Unit for Am2900 System.

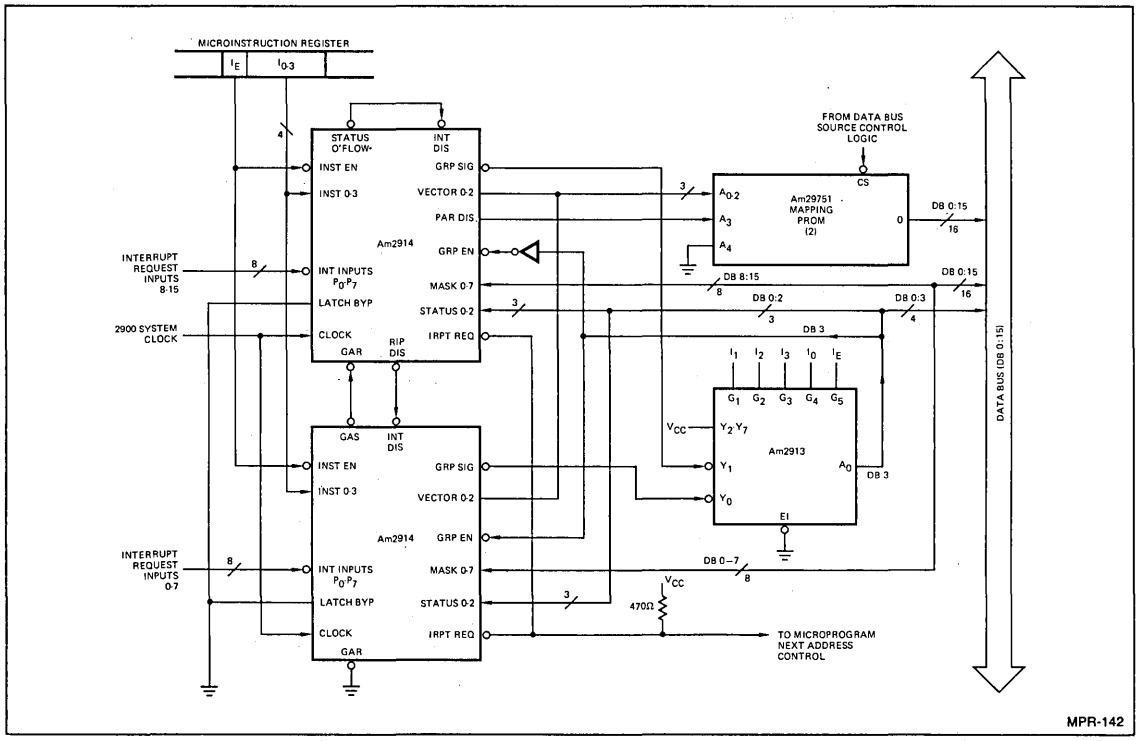


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Figure 15. 16 Level Interrupt Control Unit for Am2900 System.

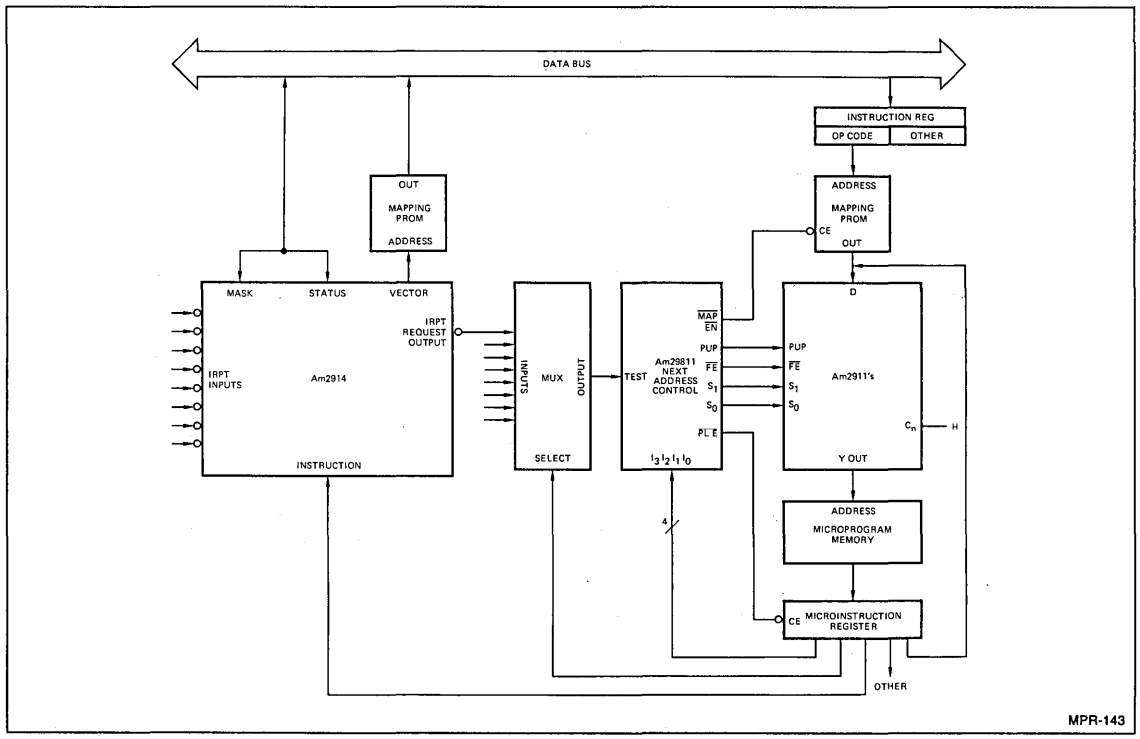

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Figure 16. Computer Control Unit for Machine Program Interrupt System.

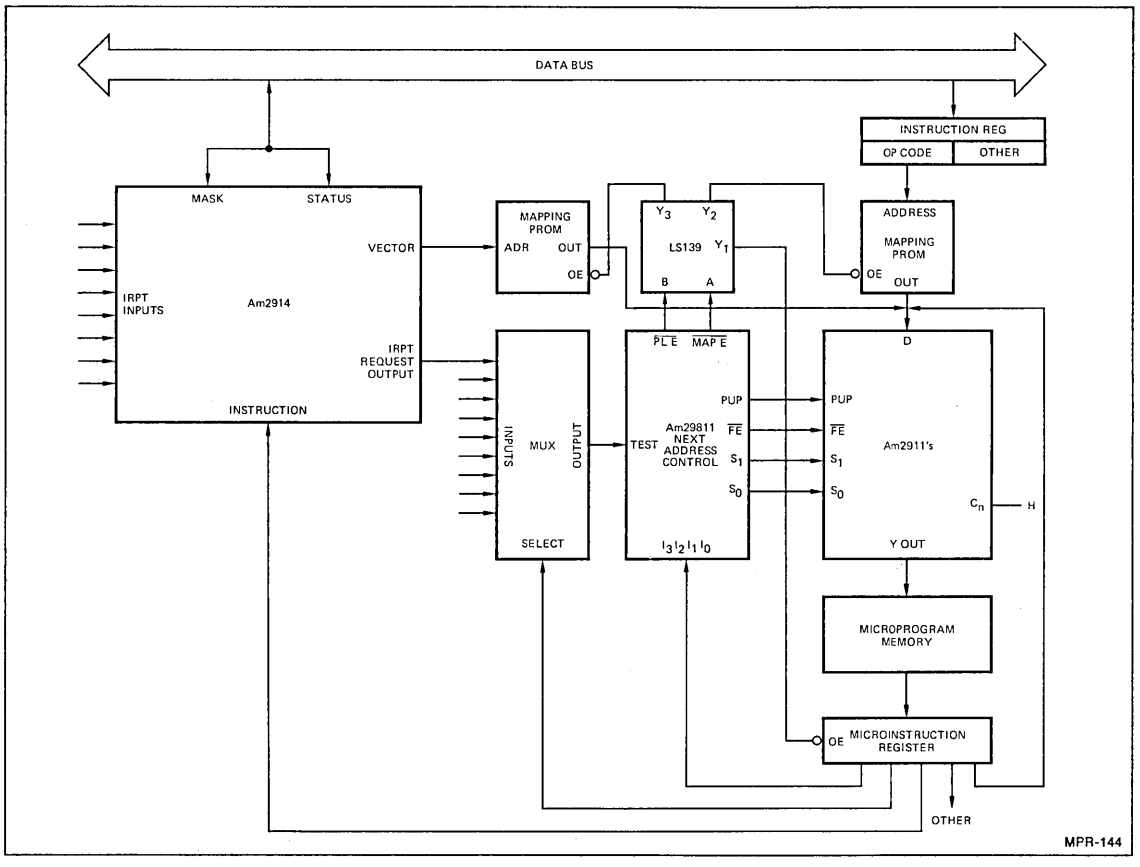

Figure 17. Computer Control Unit for Microprogram Interrupt System.

EXAMPLE INTERRUPT SYSTEM DESIGN FOR AN Am9080A SYSTEM

The Am2914 can be used in an Am9080A system also. Figure 18 shows the detailed hardware design of an eight-level ICU for an Am9080A system. The ICU attaches to the Am8228 data bus and uses any two I/O port addresses, designated X and Y. Three Am8228 control lines, $\overline{INTA}$, $\overline{I/O\ R}$ and $\overline{I/O\ W}$, are used to control the ICU, and the Am8224 ϕ_2 (TTL) output is used as the ICU clock. The ICU provides the INT (interrupt request) input to the Am9080A.

The Am9080A acknowledges an interrupt request with the $\overline{INTA}$ signal which selects the A inputs of the Am25LS09 Instruction Register. The Am25LS09 is a quad, two-input register which is set on the LOW-to-HIGH transition of the clock. The A inputs are wired so that an Am2914 Read Vector instruction is forced at the Am2914 Instruction Inputs. The $\overline{INTA}$ signal also forces the Am2914 Instruction Enable signal LOW and enables the Am25LS241 outputs onto the Am8228 data bus. The Am25LS241 is an eight-bit, three-state bus driver in a 20-pin package. Figure 19 shows a logic diagram of the Am25LS241. Five Am25LS241 inputs are wired HIGH so that, along with the Am2914 Vector outputs, they force an Am9080A Restart instruction onto the Am8228 data bus. The Am9080A then uses the vector to branch to an interrupt service routine.

During the interrupt service routine, the Am2914 is driven by Am9080A software. Figure 20 shows example Am9080A instruction code for Am2914 control and the comments describe the operation of the ICU hardware in detail. The Am2920 Data Out Register buffers data during operations which require the transfer of data from the Am9080A to the Am2914, such as the load mask and load status operations. The Am2920 contains eight "D" type flip-flops. Figure 21 shows the Am2920 logic diagram.

The Am25LS374 Data In Register buffers data during operations which require transfer of data from the Am2914 to the Am9080A, such as the read mask and read status operations. The Am25LS374 contains eight "D" type flip-flops in a 20-pin package. Figure 22 shows the logic diagram for the Am25LS374.

The Am25LS175 "D" type flip-flops are used to synchronize incoming and outgoing control signals with the ϕ_2 clock to meet the Am2914 and Am9080A timing requirements. In this design, the Latch Bypass input is connected to ground so that a negative pulse will be detected at any of the interrupt inputs. As always when a single Am2914 is used, the Status Overflow output is connected to the Interrupt Disable input, and the Group Advance Receive and Group Enable inputs are connected to ground.

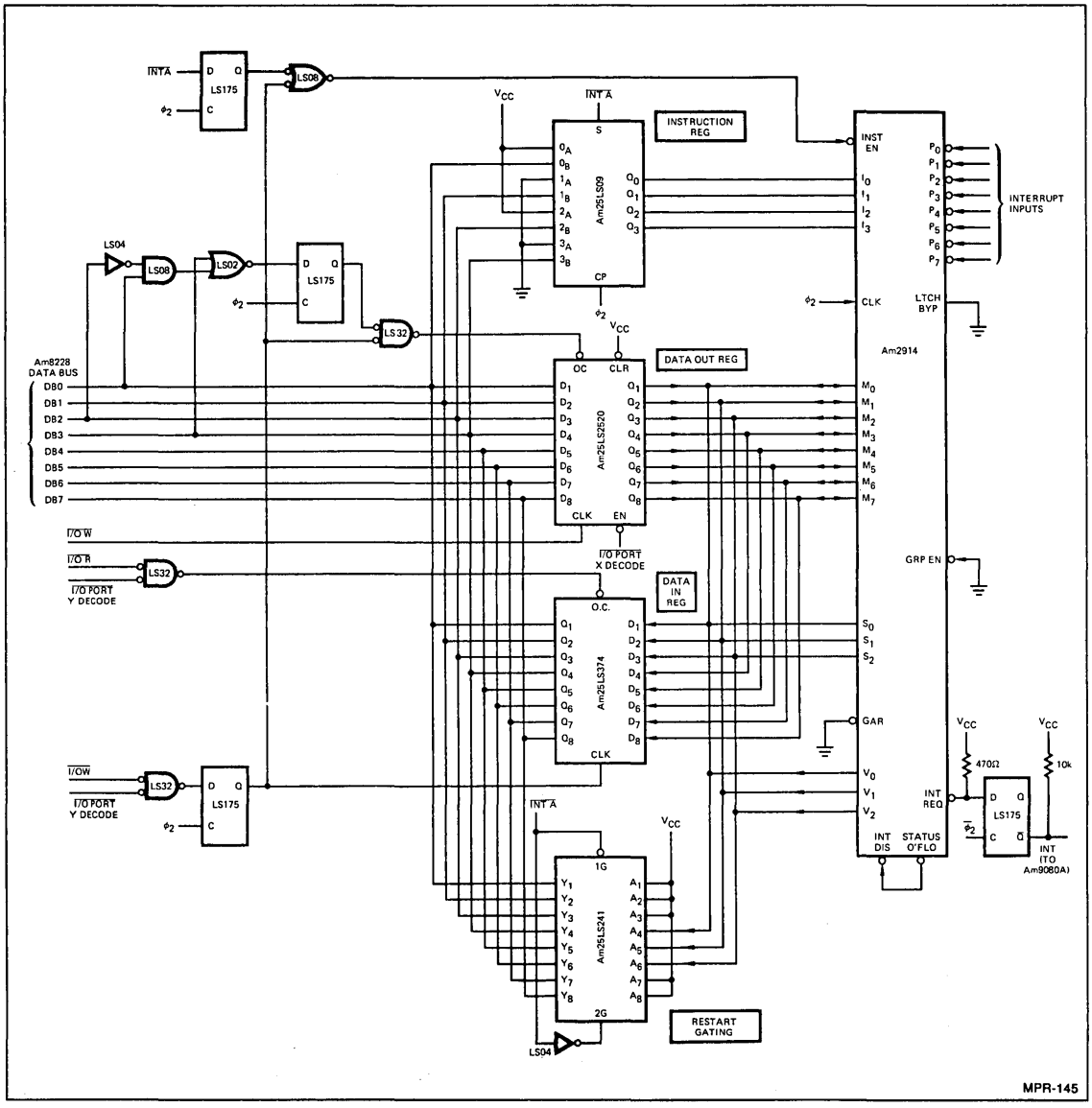

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Figure 18. 8 Level Interrupt Control Unit for Am9080A System.

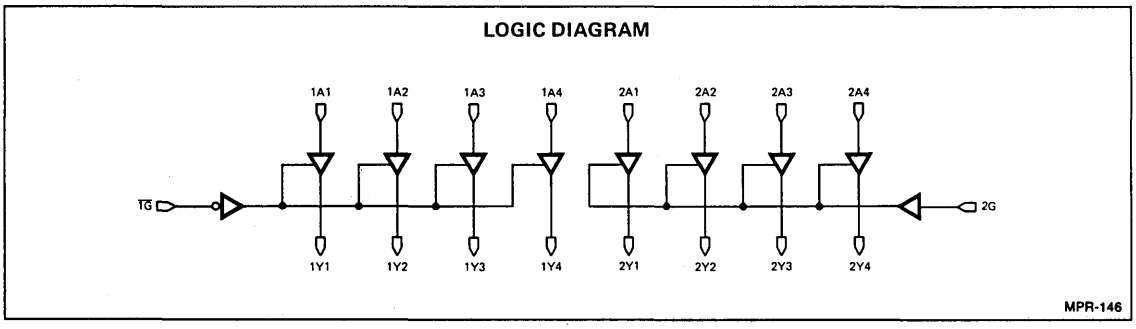

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Figure 19. Am25LS241 Octal Bus Driver with 3-State Outputs, 20 Pin Package.

Am9080A MNEMONIC	Am9080A CODE (HEX)	COMMENTS	
MVI A	3E X0	LOAD IMMEDIATE THE Am2914 MASTER CLEAR INSTRUCTION INTO Am9080A ACCUMULATOR	Am2914 MASTER CLEAR OPERATION
OUT	D3 PORT Y ADR	OUTPUT ACCUMULATOR TO ICU INSTRUCTION REG & ENABLE Am2914 INSTRUCTION	
MVI A	3E MASK PATTERN	LOAD IMMEDIATE THE MASK BIT PATTERN INTO THE Am9080A ACCUMULATOR	Am2914 LOAD MASK OPERATION
OUT	D3 PORT X ADR	OUTPUT ACCUMULATOR TO ICU DATA OUT REG	
MVI A	3E XE	LOAD IMMEDIATE THE Am2914 LOAD MASK INSTRUCTION INTO Am9080A ACCUMULATOR	
OUT	D3 PORT Y ADR	OUTPUT ACCUMULATOR TO ICU INST REG, ENABLE INST., & ENABLE DATA OUT REG OUTPUTS	
MVI A	3E X6	LOAD IMMEDIATE THE Am2914 READ STATUS INSTRUCTION INTO Am9080A ACCUMULATOR	Am2914 READ STATUS OPERATION
OUT	D3 PORT Y ADR	OUTPUT ACCUMULATOR TO ICU INST REG, ENABLE INST., & CLOCK DATA IN REG	
IN	DB PORT Y ADR	ENABLE DATA IN REG ONTO DATA BUS & READ IT INTO THE Am9080A ACCUMULATOR	

Note: Am2914 instruction bits I_0-I_3 must be on data bus bits DB_0-DB_3, respectively.
X = Don't Care.

Figure 20. Example Am9080A Instruction Code for Am2914 Control.

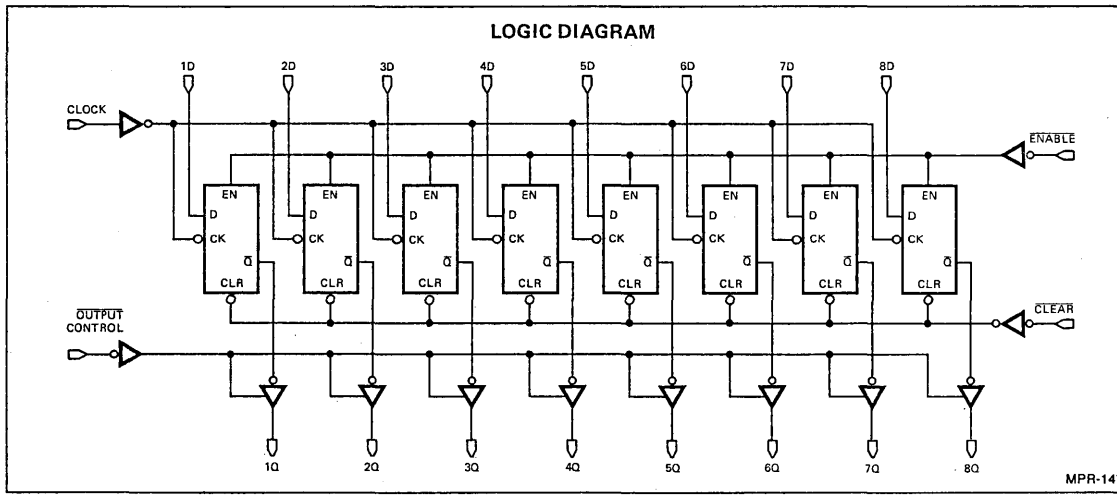


Figure 21. Am2920 Octal D-Type Flip-Flops with 3-State Outputs. Common Clock, Clear, Clock Enable and Output Control, 22 Pin Package.

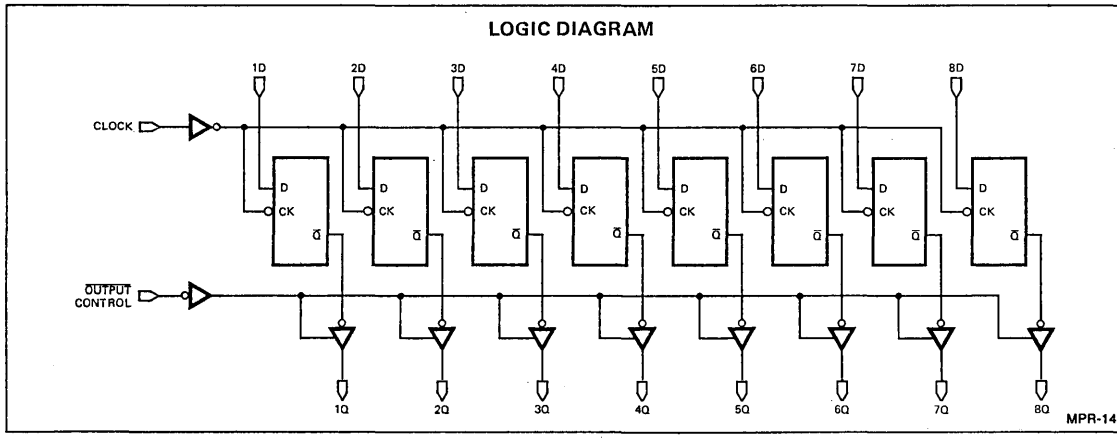


Figure 22. Am25LS374 Octal D-Type Flip-Flops with 3-State Outputs, 20 Pin Package.

Am2914 PRIORITY INTERRUPT ENCODER DETAILED LOGIC DESCRIPTION

INTRODUCTION

A clear understanding of the Am2914 Priority Interrupt controller's operation facilitates its efficient use. With that idea in mind, a detailed logic description of the Am2914 is presented here. A detailed logic diagram and control signal truth table are shown, and significant aspects of the Am2914 design are described verbally.

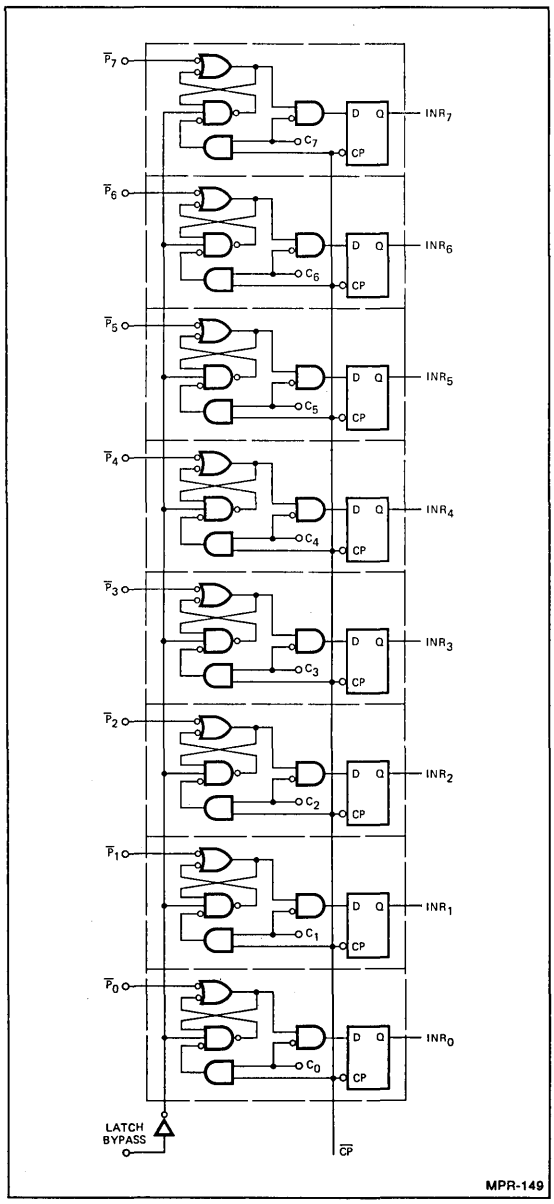


Figure 1. Interrupt Latches and Register.

LOGIC DIAGRAM DESCRIPTION

The Interrupt Latches and Register are shown in Figure 1. The Interrupt latches are set/reset-type latches. When the Latch Bypass signal is LOW, the latches are enabled and act as negative pulse catchers on the inputs to the Interrupt Register. When the Latch Bypass signal is HIGH, the Interrupt latches are transparent. The Interrupt Register holds the Interrupt Inputs and is an eight-bit, edge-triggered register. It is updated on the LOW-to-HIGH transition of the clock pulse (HIGH-to-LOW transition of the $\overline{CP}$ signal) as are all of the flip-flops on the chip.

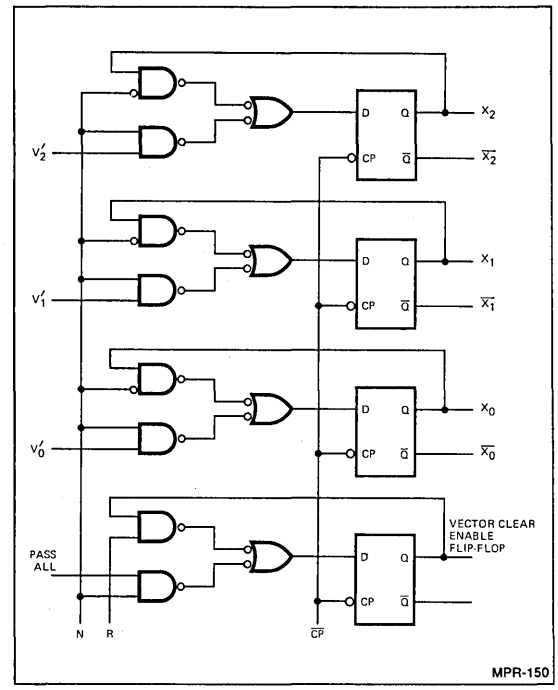


Figure 2. Vector Hold Register

When a Read Vector instruction is executed, the binary coded vector is loaded into the Vector Hold Register of Figure 2. This stored vector can be used later for clearing the interrupt associated with the last vector that was read. The Vector Clear Enable Flip-Flop of Figure 2 is set when a Read Vector instruction is executed and the PASS ALL signal is HIGH. A HIGH PASS ALL signal level indicates that this group is enabled and that an interrupt request in this group was detected and passed priority. The Vector Hold Register and the Vector Clear Enable Flip-Flop are cleared when a Master Clear, Clear All Interrupts, or Clear Interrupt Last Vector Read is executed. Table 1 shows the generation of the "N and R" control signals for each of these operations.

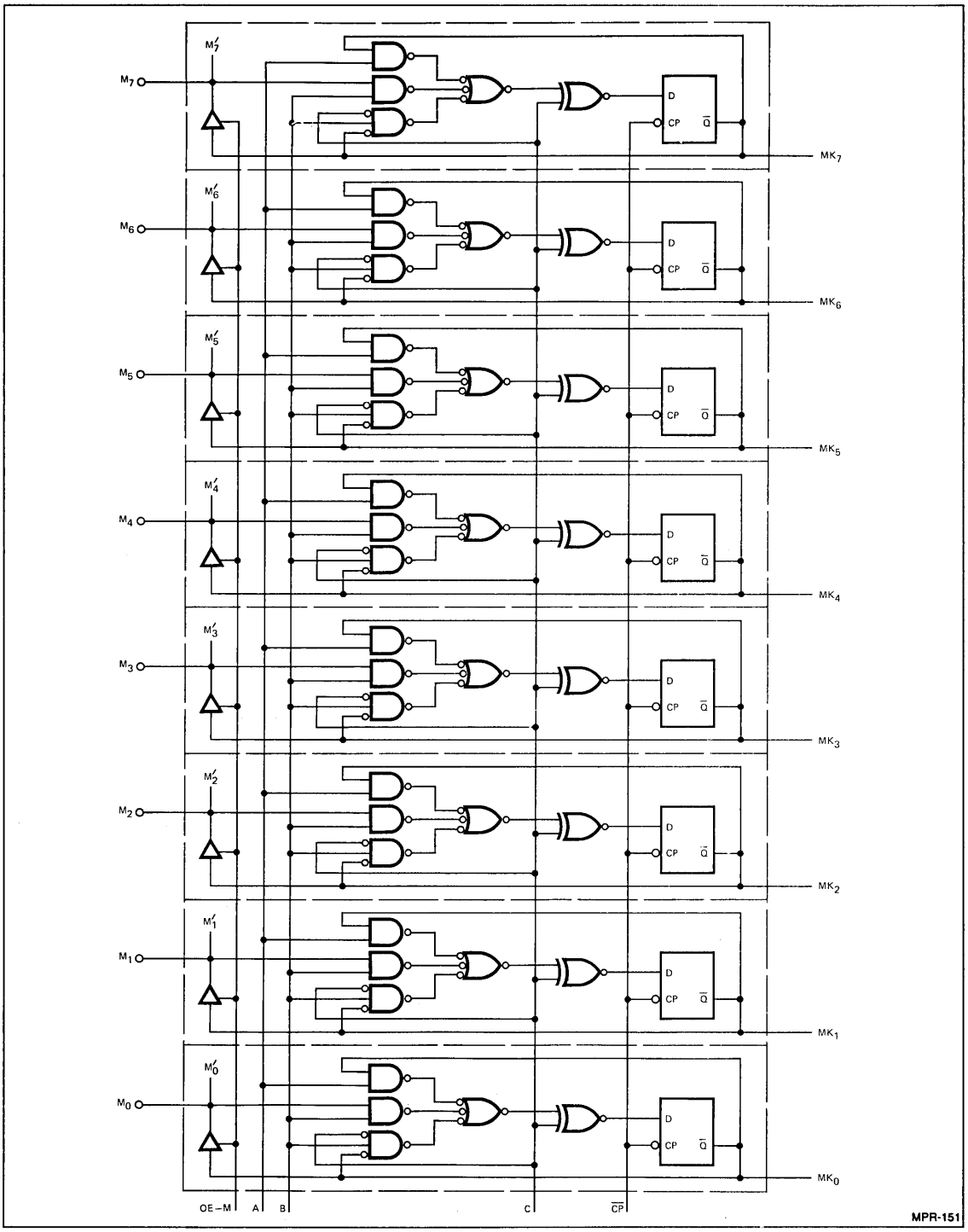


Figure 3. Mask Register.

The Mask Register shown in Figure 3 holds the eight mask bits associated with the eight interrupt levels. The register may be set or cleared, bit set or bit cleared from the "M" bus, or loaded or read to the "M" bus. Table 1 shows the generation of the "A", "B", "C" and "OE-M" control signals for each of these operations.

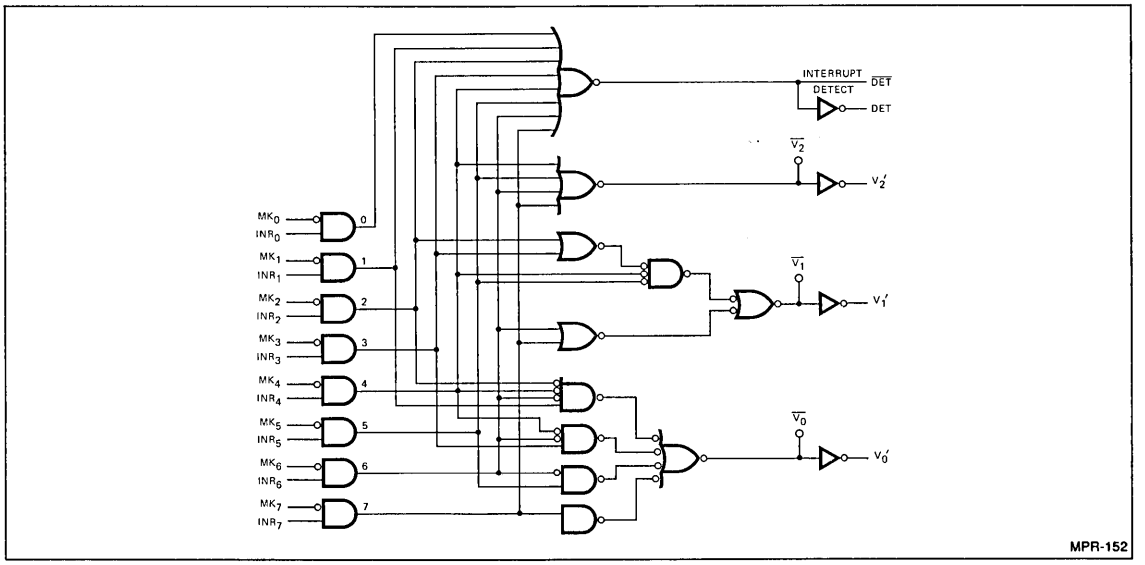


Figure 4. Interrupt Request Detect and Priority Decoder.

The Interrupt Request Detect and Priority Encode circuitry are shown in Figure 4. The Interrupt Detect circuitry detects the presence of any unmasked Interrupt Input. The eight-input Priority Encoder determines the highest priority, non-masked Interrupt Input and forms a binary coded interrupt vector, V_0-V_2.

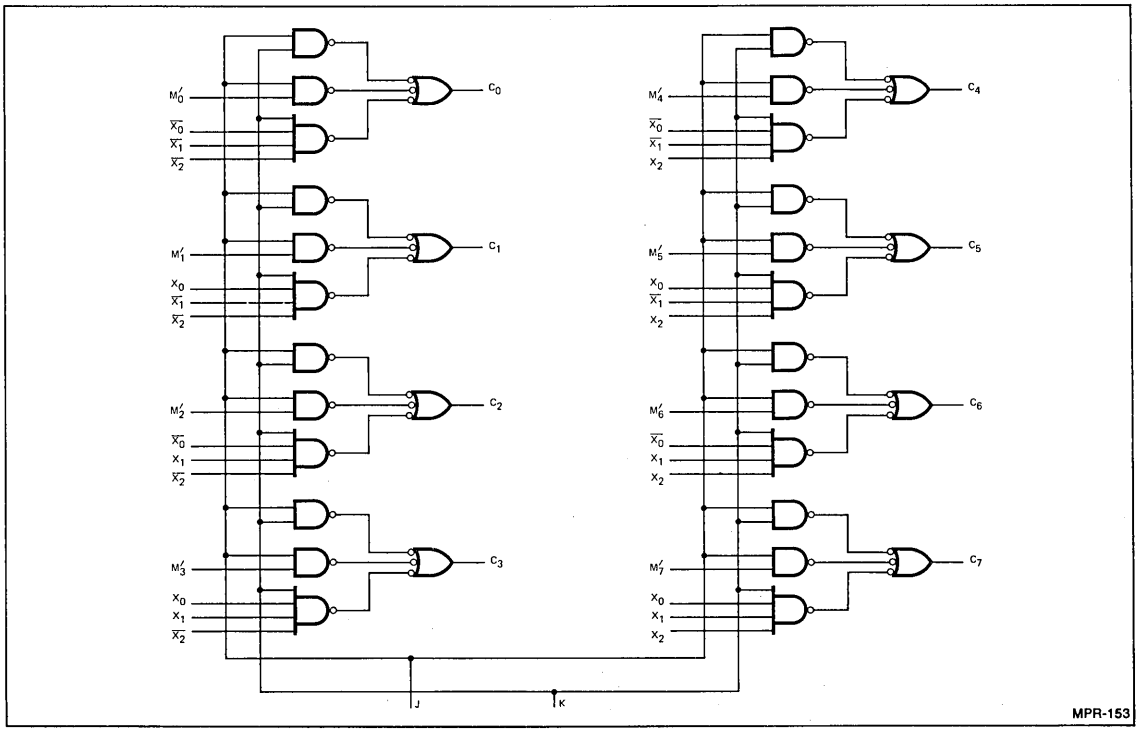


Figure 5. Clear Control.

The Clear Control logic of Figure 5 generates the eight individual clear signals for the eight Interrupt Register bits. Under microinstruction control, all interrupts, interrupts with corresponding mask register bits set, interrupts with corresponding mask bus bits equal to one, or the interrupt associated with the last vector read may be cleared. Table 1 shows the generation of the "J" and "K" control signals for each of these operations.

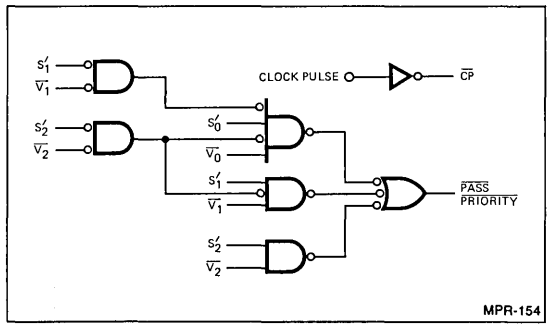


Figure 6. Three-Bit comparator.

The three-bit Comparator of Figure 6 compares the interrupt vector with the contents of the Status Register. A LOW signal level at the PASS PRIORITY output indicates that the interrupt vector is greater than or equal to the contents of the Status Register.

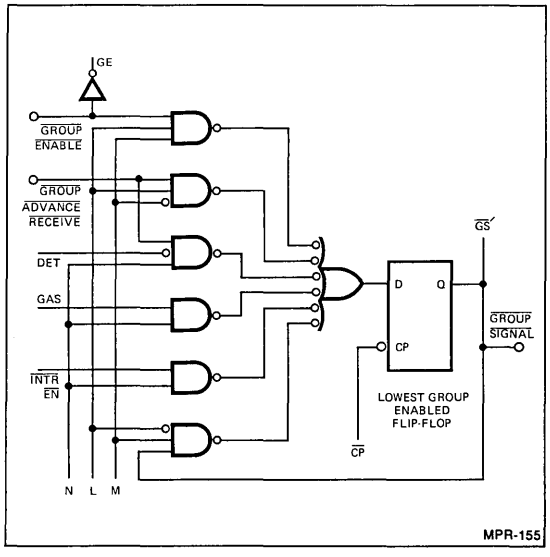


Figure 7. Group Enable Logic.

The Lowest Group Enabled Flip-Flop, Figure.7, is used when a number of Am2914's are cascaded. In a cascaded system, only one Lowest Group Enabled Flip-Flop is LOW at a time. It indicates the group which contains the lowest priority interrupt which will be accepted and is used to form the high order status bits. When a Load Status instruction is executed, the flip-flop is loaded from the GROUP ENABLE input. When a Master Clear instruction is executed, it is loaded from the GROUP ADVANCE RECEIVE input. The flip-flop is set HIGH when a Read Vector instruction is executed if a Group Advance is not received and no interrupt in this group is detected, if a Group Advance is sent from this group, or if interrupts from this group are disabled. For all other instructions, the flip-flop remains the same. Table 1 shows the generation of the "N", "L" and "M" control signals for these operations.

The Status Register holds the status bits and may be loaded from or read to the "S" bus as shown in Figure 8. Note that when a Load Status instruction is executed, status from the "S" bus is loaded into the Status Register only if the GROUP ENABLE input is LOW; if the GROUP ENABLE input is HIGH, the Status Register is cleared. Also note that during a Read Status instruction, the Status Register outputs are enabled onto the "S" bus only if the Lowest Group Enabled Flip-Flop of this group is LOW. When a Read Vector instruction is executed, the incrementer increases the vector by one and the result is loaded into the Status Register. Thus, the Status Register always points to the lowest level at which an interrupt will be accepted. Table 1 shows the generation of the "F", "G" and "OE-S" control signals for Status Register operations.

The Interrupt Request Logic, shown in Figure 9, generates the RIPPLE DISABLE, PARALLEL DISABLE, INTERRUPT REQUEST, GROUP ADVANCE SEND, and STATUS OVERFLOW output signals. The PARALLEL DISABLE signal is generated when the Lowest Group Enabled signal is LOW or an interrupt request in this group is detected and passes priority. The RIPPLE DISABLE signal is generated when the PARALLEL DISABLE signal is generated and also when the INTERRUPT DISABLE input signal is LOW. The INTERRUPT REQUEST output signal is generated when interrupt requests in this group are enabled and a request is detected and passes priority. The GROUP ADVANCE SEND output signal is generated when a vector of value seven is being read. The Status Overflow Flip-Flop is set LOW when a vector of value seven is read and indicates the Status Register has overflowed. The Interrupt Request Enable Flip-Flop is either set or reset by the Enable Request or Disable Request microinstructions respectively, and is used to enable or disable the INTERRUPT REQUEST output. Table 1 shows the generation of control signals "D", "E", "S" and "H".

Note that the vector outputs are enabled only when a Read Vector is being executed. Also note that when a Read Vector instruction is executed, the vector outputs will be disabled after the execution of the instruction since the Status Register is loaded with V+1, and the INTERRUPT REQUEST will no longer be generated.

The Microinstruction Decode circuitry, Figure 10, decodes the Am2914 microinstructions and generates the required internal control signals. Table 1 shows the truth table for these functions and Figure 11 shows the function tables.

Table 1. Am2914 Control Signal Truth Table.

0 = LOW, 1 = HIGH

Microinstruction						Function	Mask Register				Status Register			Group Enable		Clear Control		Irpt Request Enable		Vector Hold Register		Other	
Decimal	$\overline{I_E}$	I_3	I_2	I_1	I_0	Description	A	B	C	OE-M	F	G	$\overline{OE\text{-}S}$	L	M	J	K	D	E	N	R	S	H
0	0	0	0	0	0	Master Clear	0	0	1	0	0	0	1	1	0	1	1	0	1	0	0	1	1
1	0	0	0	0	1	Clear All Interrupts	1	0	1	0	0	1	1	0	1	1	1	1	X	0	0	1	0
2	0	0	0	1	0	Clear Intr Via M Bus	1	0	1	0	0	1	1	0	1	1	0	1	X	0	1	1	0
3	0	0	0	1	1	Clear Intr Via M Reg	1	0	1	1	0	1	1	0	1	1	0	1	X	0	1	1	0
4	0	0	1	0	0	Clear Intr, Last Vector	1	0	1	0	0	1	1	0	1	0	1/0	1	X	0	0	1	0
5	0	0	1	0	1	Read Vector	1	0	1	0	0/1	0	1	0	0	0	0	1	X	1	0	0	1
6	0	0	1	1	0	Read Status Reg	1	0	1	0	0	1	0	0	1	0	0	1	X	0	1	1	0
7	0	0	1	1	1	Read Mask Reg	1	0	1	1	0	1	1	0	1	0	0	1	X	0	1	1	0
8	0	1	0	0	0	Set Mask Reg	0	0	0	0	0	1	1	0	1	0	0	1	X	0	1	1	0
9	0	1	0	0	1	Load Status Reg	1	0	1	0	1	1	1	1	1	0	0	1	X	0	1	1	1
10	0	1	0	1	0	Bit Clear Mask Reg	0	1	0	0	0	1	1	0	1	0	0	1	X	0	1	1	0
11	0	1	0	1	1	Bit Set Mask Reg	1	1	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0
12	0	1	1	0	0	Clear Mask Reg	0	0	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0
13	0	1	1	0	1	Disable Request	1	0	1	0	0	1	1	0	1	0	0	0	0	0	1	1	0
14	0	1	1	1	0	Load Mask Reg	0	1	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0
15	0	1	1	1	1	Enable Request	1	0	1	0	0	1	1	0	1	0	0	0	1	0	1	1	0
X	1	X	X	X	X	Instruction Disable	1	0	1	0	0	1	1	0	1	0	0	1	X	0	1	1	0

Notes: 1. Control line "F" during "READ VECTOR" instruction is 0 when "PASS ALL" is LOW and 1 when "PASS ALL" is HIGH.
2. Control line "K" during "Clear Intr, Last Vector" instruction is 0 when "Vector Clear Enable" is LOW and 1 when "Vector Clear Enable" is HIGH.

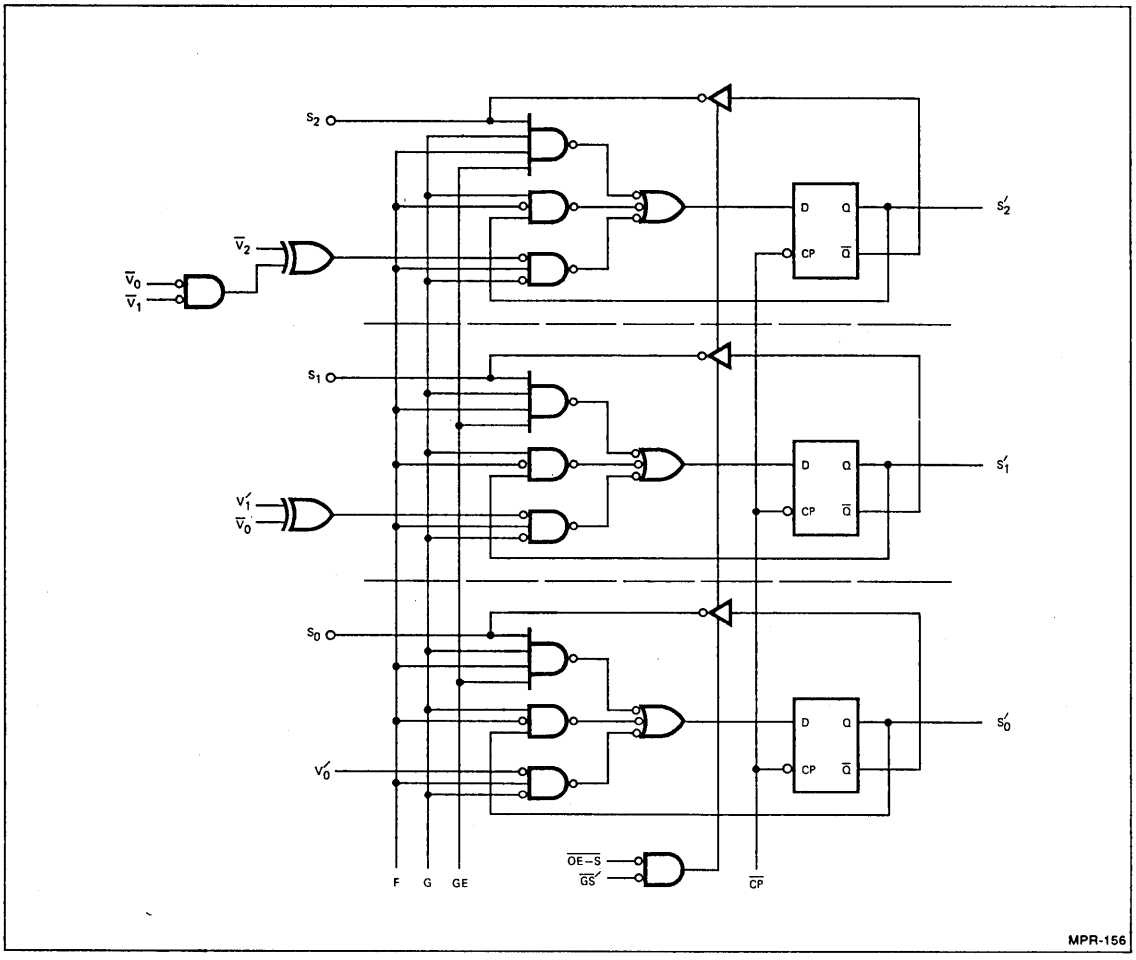


Figure 8. Incrementer and Status Register.

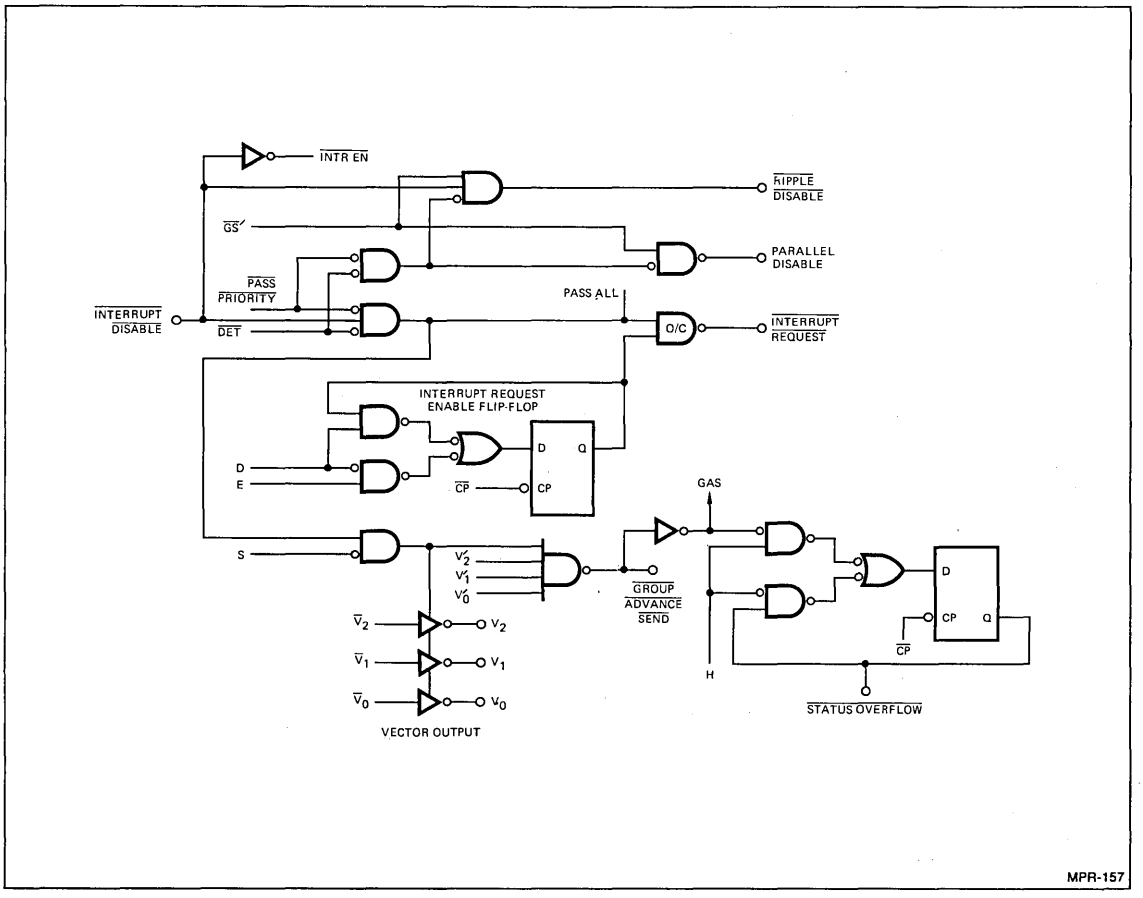


Figure 9. Interrupt Request Logic.

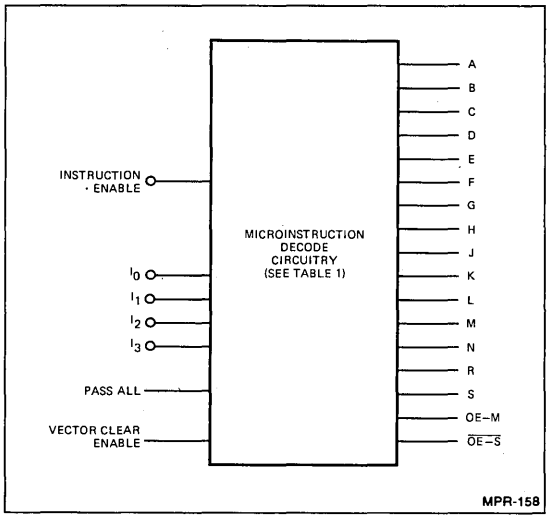


Figure 10.

MASK REGISTER

A	B	C	FUNCTION
0	0	0	SET
0	0	1	CLEAR
0	1	0	BIT CLEAR
0	1	1	LOAD
1	0	1	HOLD
1	1	1	BIT SET

CLEAR CONTROL

J	K	FUNCTION
0	0	NO CLEAR
0	1	CLEAR IRPT, VECTOR
1	0	CLEAR IRPTS VIA M
1	1	CLEAR ALL IRPTS

VECTOR HOLD REGISTER

N	FUNCTION
0	HOLD
1	LOAD

LOWEST GROUP ENABLED FLIP-FLOP

L	M	FUNCTION
0	0	UPDATE
0	1	HOLD
1	0	LOAD VIA GROUP ADVANCE RECEIVE
1	1	LOAD VIA GROUP ENABLE

STATUS REGISTER

F	G	FUNCTION
0	0	CLEAR
0	1	HOLD
1	0	LOAD VECTOR + 1
1	1	LOAD VIA "S" BUS

INTERRUPT REQUEST ENABLE FLIP-FLOP

D	E	FUNCTION
0	0	DISABLE IRPTS
0	1	ENABLE IRPTS
1	X	HOLD

VECTOR CLEAR ENABLE FLIP-FLOP

N	R	FUNCTION
0	0	CLEAR
0	1	HOLD
1	0	LOAD

STATUS OVERFLOW FLIP-FLOP

H	FUNCTION
0	HOLD
1	LOAD

Figure 11. Control Function Tables.

Am2915A

Quad Three-State Bus Transceiver With Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

FUNCTIONAL DESCRIPTION

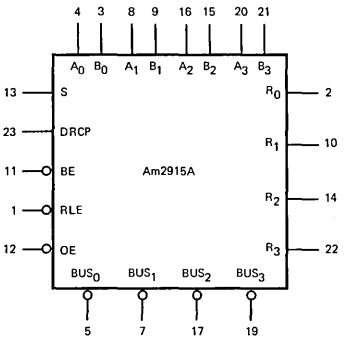
The Am2915A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The V_{OH} and V_{OL} of the bus driver are selected for compatibility with standard and Low-Power Schottky inputs.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and OE LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

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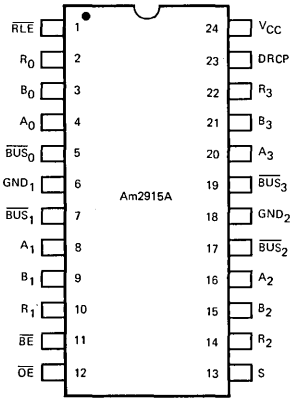
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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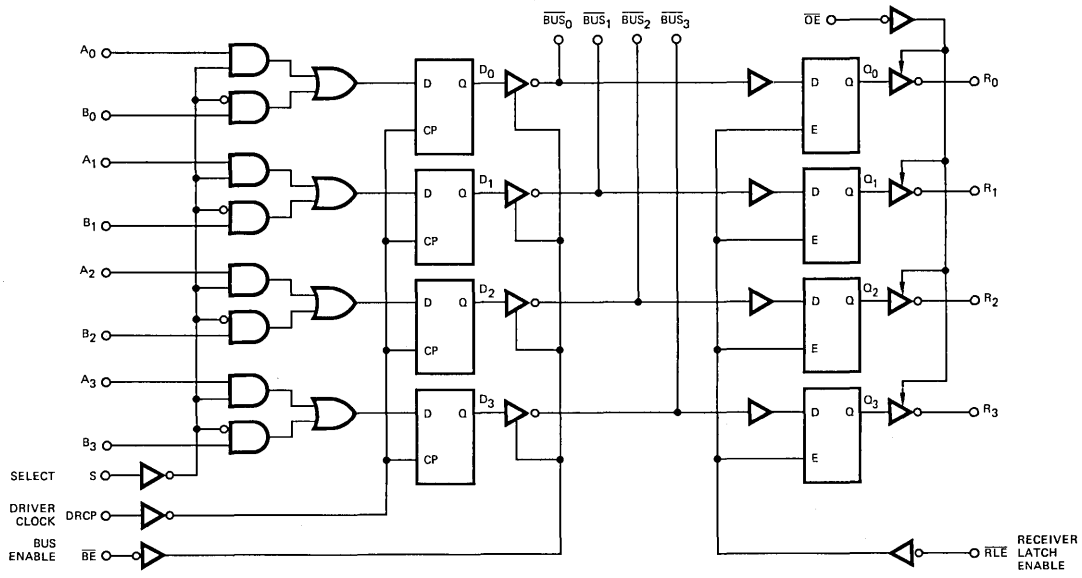
LOGIC DIAGRAM



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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	100mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2915AXC (COM'L) T_A = 0°C to +70°C V_{CC}MIN. = 4.75V V_{CC}MAX. = 5.25V
Am2915AXM (MIL) T_A = −55°C to +125°C V_{CC}MIN. = 4.50V V_{CC}MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4V	V_O = 0.4V			−200	μA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V, V_{CC} = 0V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0V		−50	−120	−225	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2915AXC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75 V V_{CC} MAX. = 5.25 V
Am2915AXM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50 V V_{CC} MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

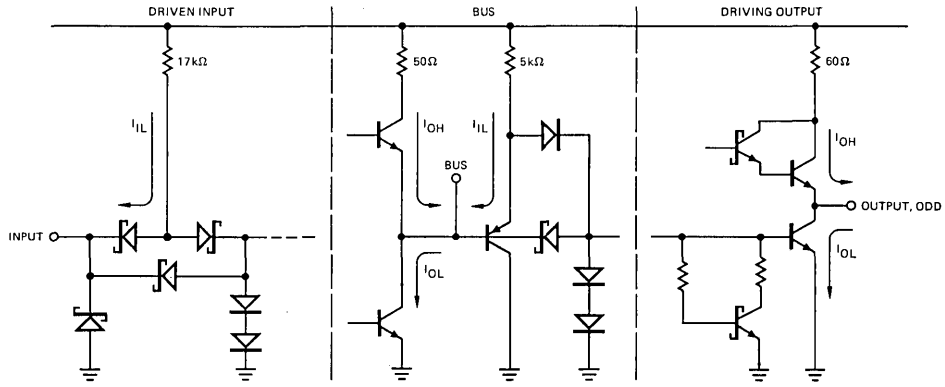
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0$mA	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6$mA	2.4	3.4		
		V_{CC} = 5.0 V, $I_{OH} = -100\mu$A		3.5			
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4.0mA		0.27	0.4	Volts
			I_{OL} = 8.0mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18$mA				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4 V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7 V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 7.0 V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.		−30		−130	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	V_O = 2.4 V			50	μA
			V_O = 0.4 V			−50	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2915AXM Min.	Am2915AXM Typ. (Note 2)	Am2915AXM Max.	Am2915AXC Min.	Am2915AXC Typ. (Note 2)	Am2915AXC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	Data Inputs (A or B)	C_L = 15pF, R_L = 2.0kΩ	15			12			ns
t_h			8.0			6.0			
t_s	Select Input (S)		28			25			ns
t_h			8.0			6.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enable)			18	33		18	30	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			13			ns
t_h			6.0			4.0			
t_{ZH}, t_{ZL}	Output Control to Receiver Output	C_L = 5pF, R_L = 2.0kΩ		14	26		14	23	ns
t_{HZ}, t_{LZ}				14	26		14	23	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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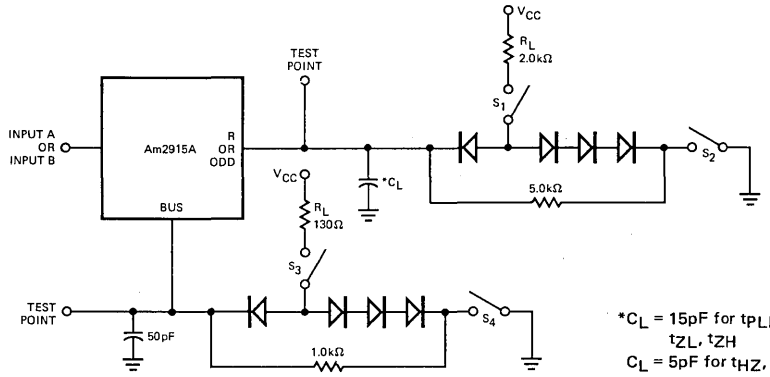
SWITCHING TEST CIRCUIT



*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

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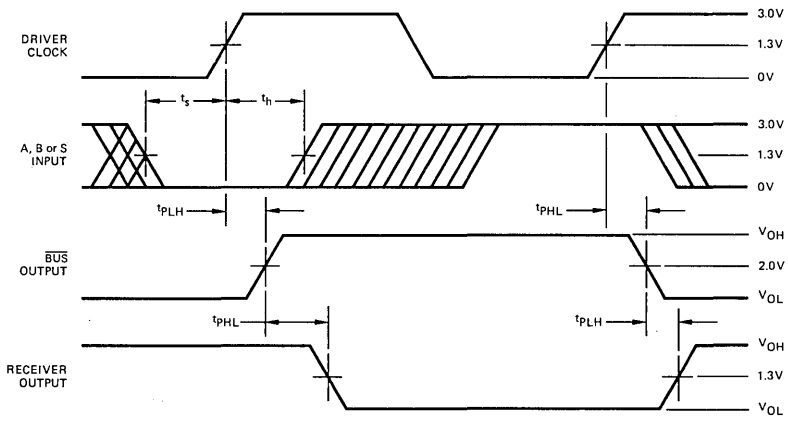
SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

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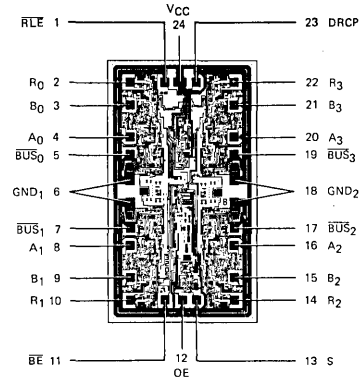
FUNCTIONAL TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

Metallization and Pad Layout



DIE SIZE .074" X .130"

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

$\overline{BUS}_0$, $\overline{BUS}_1$, $\overline{BUS}_2$, $\overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

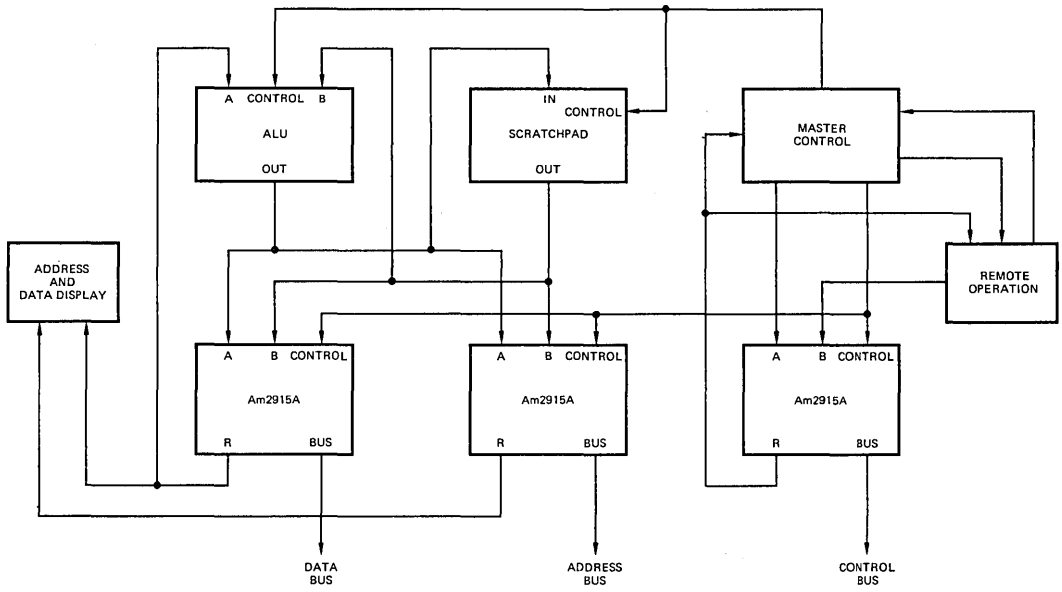
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2915APC	P-24	C	C-1
AM2915ADC	D-24	C	C-1
AM2915ADC-B	D-24	C	B-1
AM2915ADM	D-24	M	C-3
AM2915ADM-B	D-24	M	B-3
AM2915AFM	F-24	M	C-3
AM2915AFM-B	F-24	M	B-3
AM2915AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2915AXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATIONS



The Am2915A is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.

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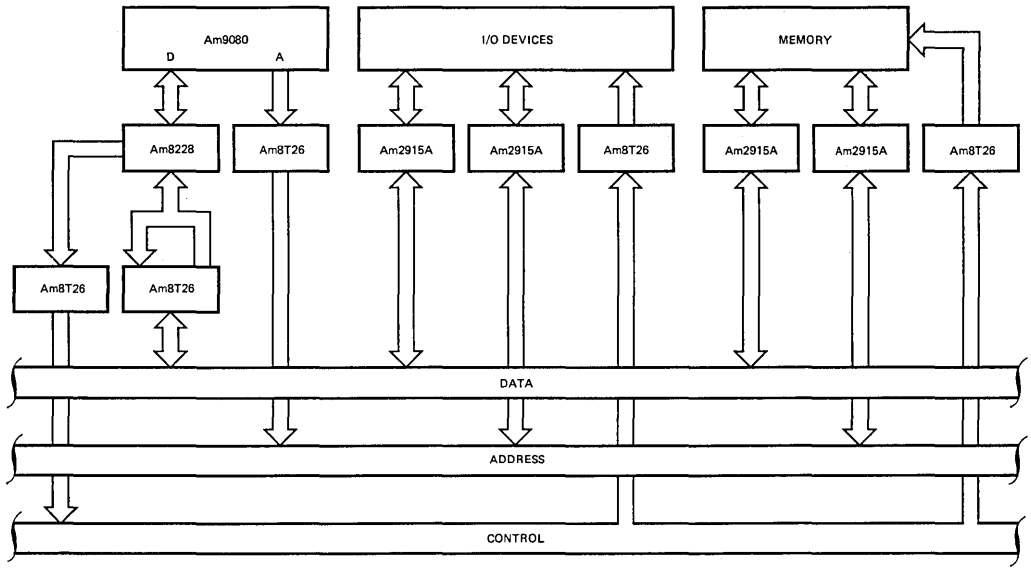


Using the Am2915A and Am8T26 in a terminated Bus system for the Am9080 MOS Microprocessor.

MPR-166

Am2916A

Quad Three-State Bus Transceiver With Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

FUNCTIONAL DESCRIPTION

The Am2916A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

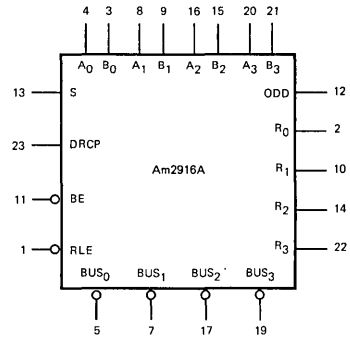
The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data in non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

The Am2916A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

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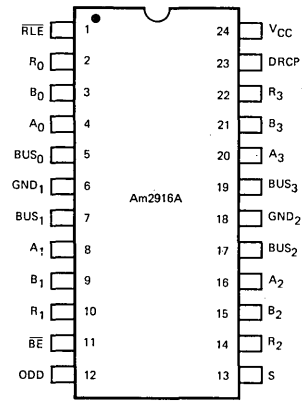
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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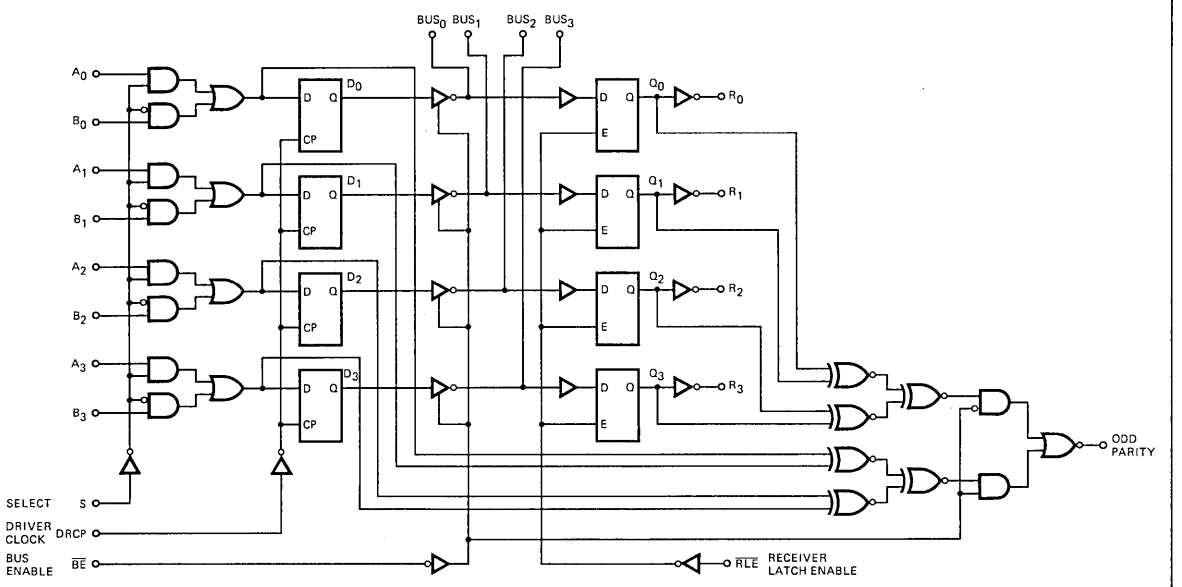
LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	100mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2916AXC (COM'L) T_A = 0°C to +70°C V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2916AXM (MIL) T_A = −55°C to +125°C V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24mA			0.4	Volts
			I_{OL} = 48mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20mA	2.4			Volts
			MIL, I_{OH} = −15mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4V	V_O = 0.4V			−200	μA
			V_O = 2.4V			50	
			V_O = 4.5V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V, V_{CC} = 0V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX., V_O = 0V		−50	−120	−225	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2916AXC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2916AXM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

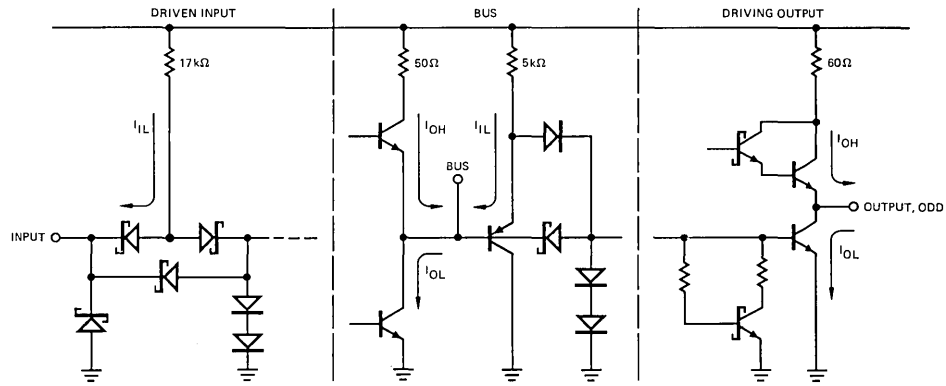
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0mA$	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6mA$	2.4	3.4		
		V_{CC} = 5.0V, $I_{OH} = -100\mu A$		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu A$, $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4.0mA		0.27	0.4	Volts
			I_{OL} = 8.0mA		0.32	0.45	
			I_{OL} = 12mA		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18mA$				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., V_{IN} = 0.4V	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., V_{IN} = 7.0V				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.	RECEIVER	−30		−130	mA
			PARITY	−20		−100	
I_{CC}	Power Supply Current	V_{CC} = MAX., All Inputs = GND			75	110	mA

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2916AXM Min.	Am2916AXM Typ. (Note 2)	Am2916AXM Max.	Am2916AXC Min.	Am2916AXC Typ. (Note 2)	Am2916AXC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus			13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	Data Inputs (A or B)		15			12			ns
t_h			8.0			6.0			
t_s	Select Inputs (S)		28			25			ns
t_h			8.0			6.0			
t_{PW}	Clock Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)	C_L = 15pF, R_L = 2.0kΩ		18	33		18	30	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			13			ns
t_h			6.0			4.0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			32	46		32	42	ns
t_{PHL}				26	40		26	36	
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	32	ns
t_{PHL}				21	36		21	32	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test shoul not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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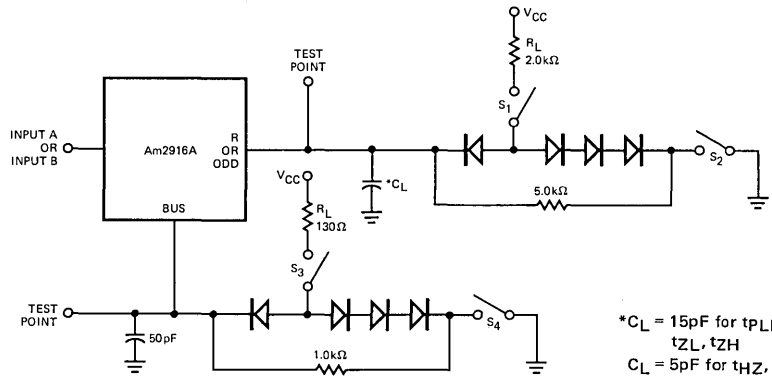
SWITCHING TEST CIRCUIT



*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

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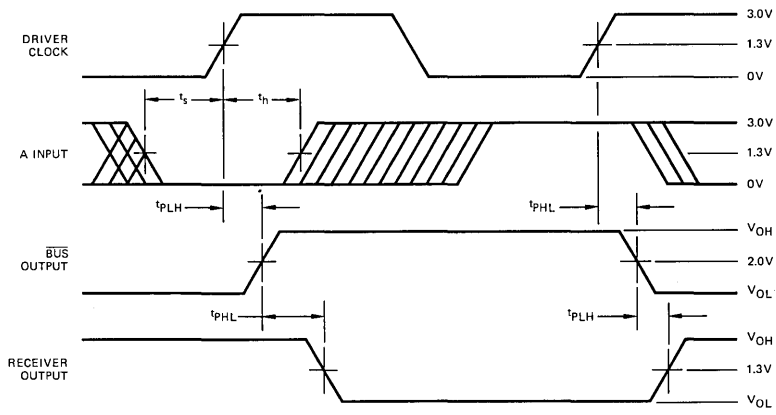
SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the $\overline{BUS}$ to R combinatorial delay.

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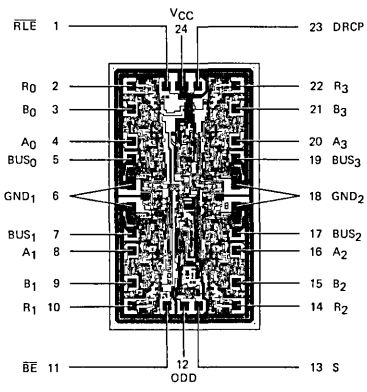
FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	$\overline{BUS}_i$	R_i	
X	X	X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

Metallization and Pad Layout



DIE SIZE .074" X .130"

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is HIGH, the four drivers are in the high impedance state.

$\overline{BUS}_0, \overline{BUS}_1, \overline{BUS}_2, \overline{BUS}_3$ The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

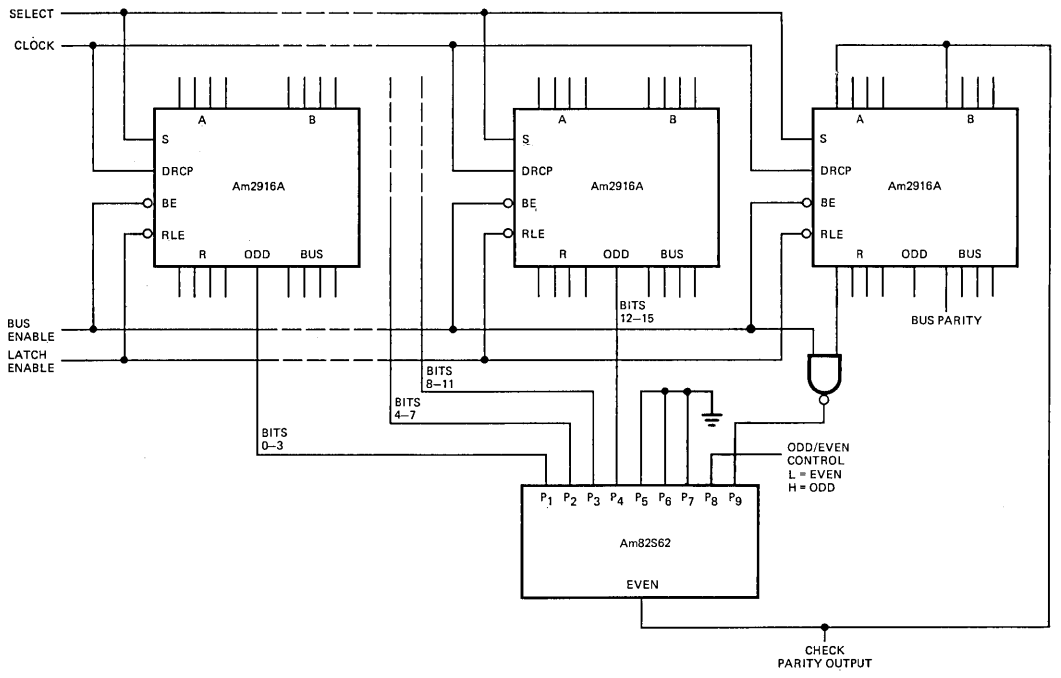
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2916APC	P-24	C	C-1
AM2916ADC	D-24	C	C-1
AM2916ADC-B	D-24	C	B-1
AM2916ADM	D-24	M	C-3
AM2916ADM-B	D-24	M	B-3
AM2916AFM	F-24	M	C-3
AM2916AFM-B	F-24	M	B-3
AM2916AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2916AXM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATIONS



Generating or checking parity for 16 data bits.

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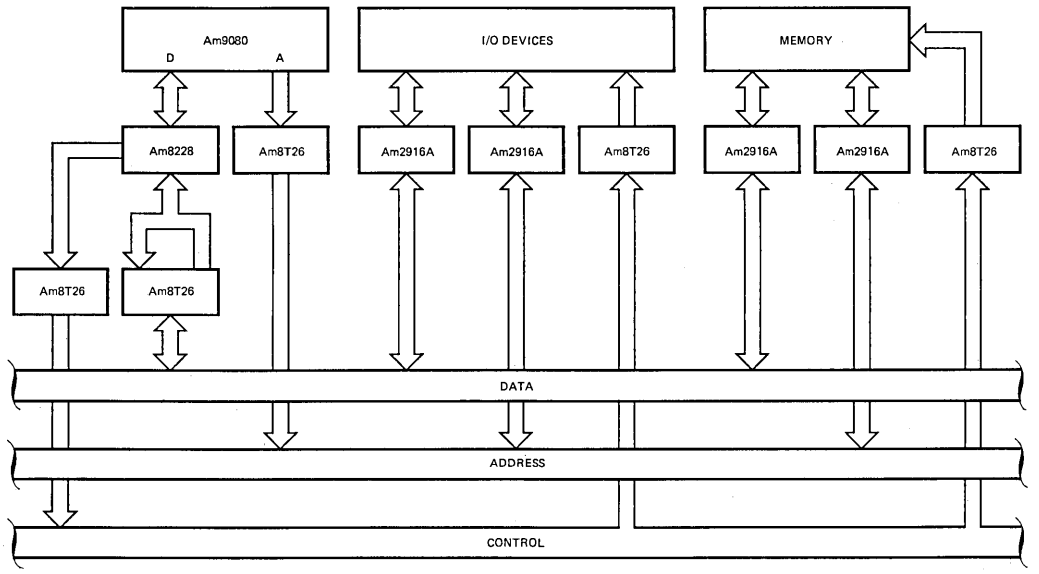


Using the Am2916A and Am8T26 in a terminated Bus system for the Am9080 MOS Microprocessor.

MPR-174

Am2917A

Quad Three-State Bus Transceiver With Interface Logic

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Three-state bus driver
- D-type register on driver
- Bus driver output can sink 48mA at 0.5V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883
- 3.5V minimum output high voltage for direct interface to MOS microprocessors

FUNCTIONAL DESCRIPTION

The Am2917A is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four three-state bus drivers. Each bus driver is internally connected to the input of a receiver. The four receiver outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

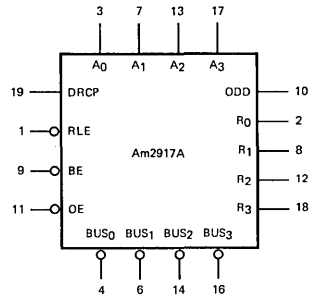
The LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The three-state bus output can sink up to 48mA at 0.5V maximum. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

The Am2917A features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

LOGIC SYMBOL



V_{CC} = Pin 20
GND_1 = Pin 5
GND_2 = Pin 15

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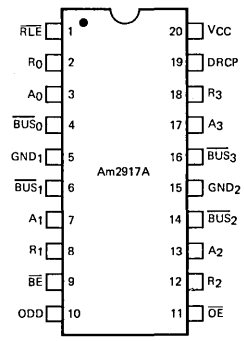
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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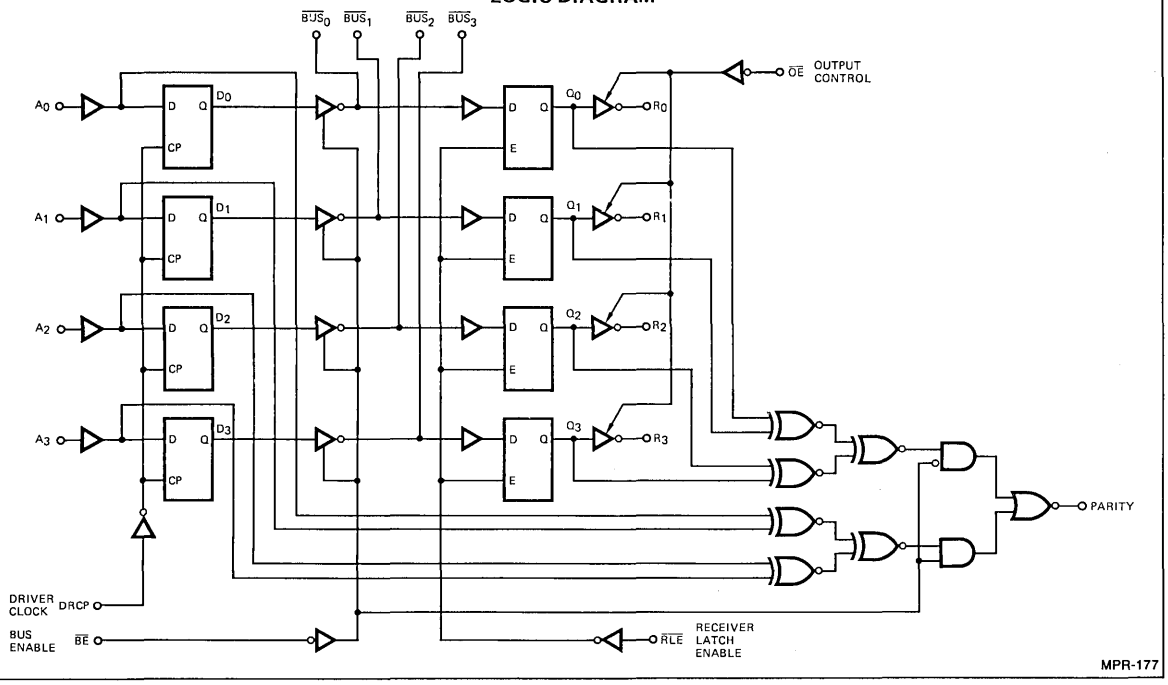
LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	100 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2917AXC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC}MIN. = 4.75 V V_{CC}MAX. = 5.25 V
Am2917AXM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC}MIN. = 4.50 V V_{CC}MAX. = 5.50 V

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ.	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	I_{OL} = 24 mA			0.4	Volts
			I_{OL} = 48 mA			0.5	
V_{OH}	Bus Output HIGH Voltage	V_{CC} = MIN.	COM'L, I_{OH} = −20 mA	2.4			Volts
			MIL, I_{OH} = −15 mA				
I_O	Bus Leakage Current (High Impedance)	V_{CC} = MAX. Bus enable = 2.4 V	V_O = 0.4 V			−200	μA
			V_O = 2.4 V			50	
			V_O = 4.5 V			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5 V V_{CC} = 0 V				100	μA
V_{IH}	Receiver Input HIGH Threshold	Bus enable = 2.4 V		2.0			Volts
V_{IL}	Receiver Input LOW Threshold	Bus enable = 2.4 V	COM'L			0.8	Volts
			MIL			0.7	
I_{SC}	Bus Output Short Circuit Current	V_{CC} = MAX. V_O = 0 V		−50	−120	−225	mA

ELECTRICAL CHARACTERISTICS

The following conditions apply unless otherwise noted:

Am2917AXC (COM'L) $T_A = 0°C$ to $+70°C$ V_{CC} MIN. = 4.75V V_{CC} MAX. = 5.25V
Am2917AXM (MIL) $T_A = -55°C$ to $+125°C$ V_{CC} MIN. = 4.50V V_{CC} MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

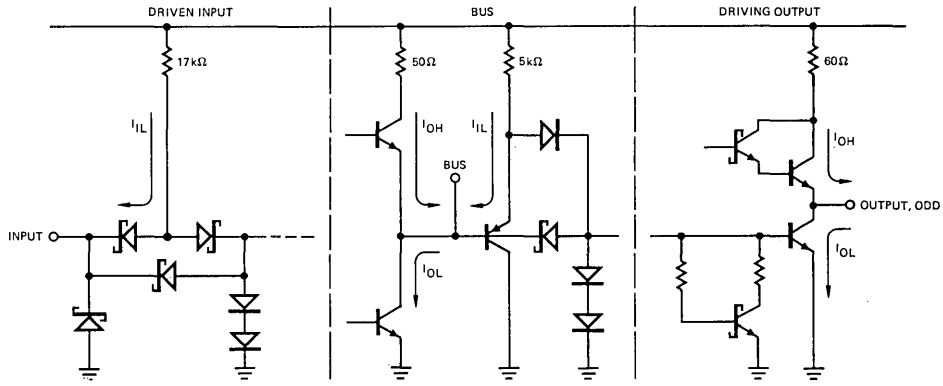
Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1.0mA$	2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6mA$	2.4	3.4		
		$V_{CC} = 5.0V$, $I_{OH} = -100\mu A$		3.5			
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu A$, $V_{IN} = V_{IH}$ or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 4.0mA$		0.27	0.4	Volts
			$I_{OL} = 8.0mA$		0.32	0.45	
			$I_{OL} = 12mA$		0.37	0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18mA$				−1.2	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4V$	$\overline{BE}$, $\overline{RLE}$			−0.72	mA
			All other inputs			−0.36	
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7V$				20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 7.0V$				100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.	RECEIVER	−30		−130	mA
			PARITY	−20		−100	
I_{CC}	Power Supply Current	V_{CC} = MAX.			63	95	mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	$V_O = 2.4V$			50	μA
			$V_O = 0.4V$			−50	

SWITCHING CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Parameters	Description	Test Conditions	Am2917AXM Min.	Am2917AXM Typ. (Note 2)	Am2917AXM Max.	Am2917AXC Min.	Am2917AXC Typ. (Note 2)	Am2917AXC Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L BUS) = 130Ω		21	36		21	32	ns
t_{PLH}				21	36		21	32	
t_{ZH}, t_{ZL}	Bus Enable ($\overline{BE}$) to Bus	$C_L = 15pF$, $R_L = 2.0k\Omega$		13	26		13	23	ns
t_{HZ}, t_{LZ}				13	21		13	18	
t_s	A Data Inputs		15			12			ns
t_h			8.0			6.0			
t_{PW}	Clock Pulse Width (HIGH)		20			17			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			18	33		18	30	ns
t_{PHL}				18	30		18	27	
t_{PLH}	Latch Enable to Receiver Output			21	33		21	30	ns
t_{PHL}				21	30		21	27	
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			13			ns
t_h			6.0			4.0			
t_{PLH}	A Data to Odd Parity Out (Driver Enabled)			32	46		32	42	ns
t_{PHL}				26	40		26	36	
t_{PLH}	Bus to Odd Parity Out (Driver Inhibit)			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			21	36		21	32	ns
t_{PHL}				21	36		21	32	
t_{ZH}, t_{ZL}	Output Control to Output			14	26		14	23	ns
t_{HZ}, t_{LZ}		$C_L = 5pF$, $R_L = 2.0k\Omega$		14	26		14	23	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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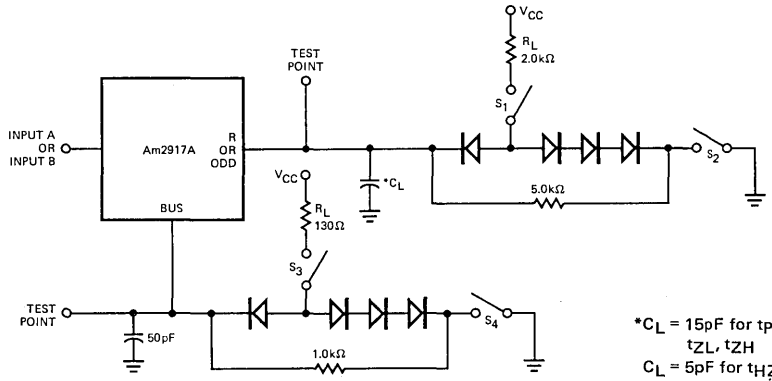
SWITCHING TEST CIRCUIT



*C_L = 15pF for t_{PLH}, t_{PHL}, t_{ZL}, t_{ZH}
C_L = 5pF for t_{HZ}, t_{LZ}

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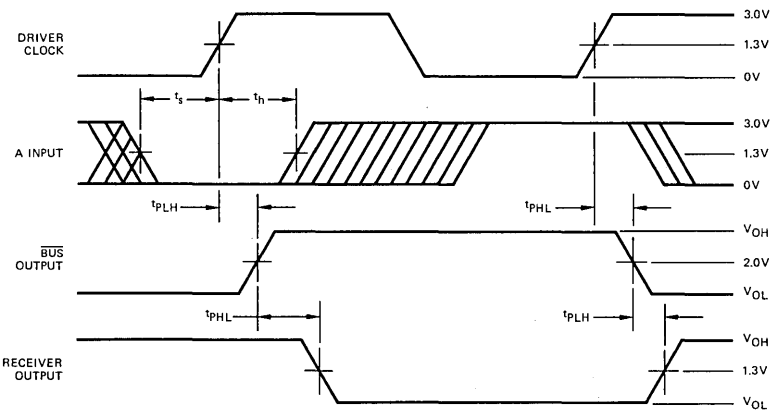
SWITCHING WAVEFORMS



Note: Bus to Receiver output delay is measured by clocking data into the driver register and measuring the BUS to R combinatorial delay.

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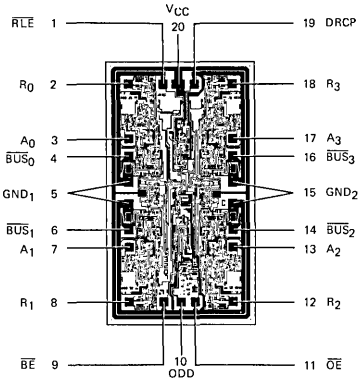
FUNCTION TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	BUS_i	R_i	
X	X	H	X	X	X	X	Z	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH Z = HIGH Impedance X = Don't care i = 0, 1, 2, 3
L = LOW NC = No change ↑ = LOW to HIGH transition

Metallization and Pad Layout



DIE SIZE .074" X .130"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2917APC	P-20	C	C-1
AM2917ADC	D-20	C	C-1
AM2917ADC-B	D-20	C	B-1
AM2917ADM	D-20	M	C-3
AM2917ADM-B	D-20	M	B-3
AM2917AFM	F-20	M	C-3
AM2917AFM-B	F-20	M	B-3
AM2917AXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2917AXM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

DEFINITION OF FUNCTIONAL TERMS

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is LOW, the four drivers are in the high impedance state.

BUS_0, BUS_1, BUS_2, BUS_3 The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

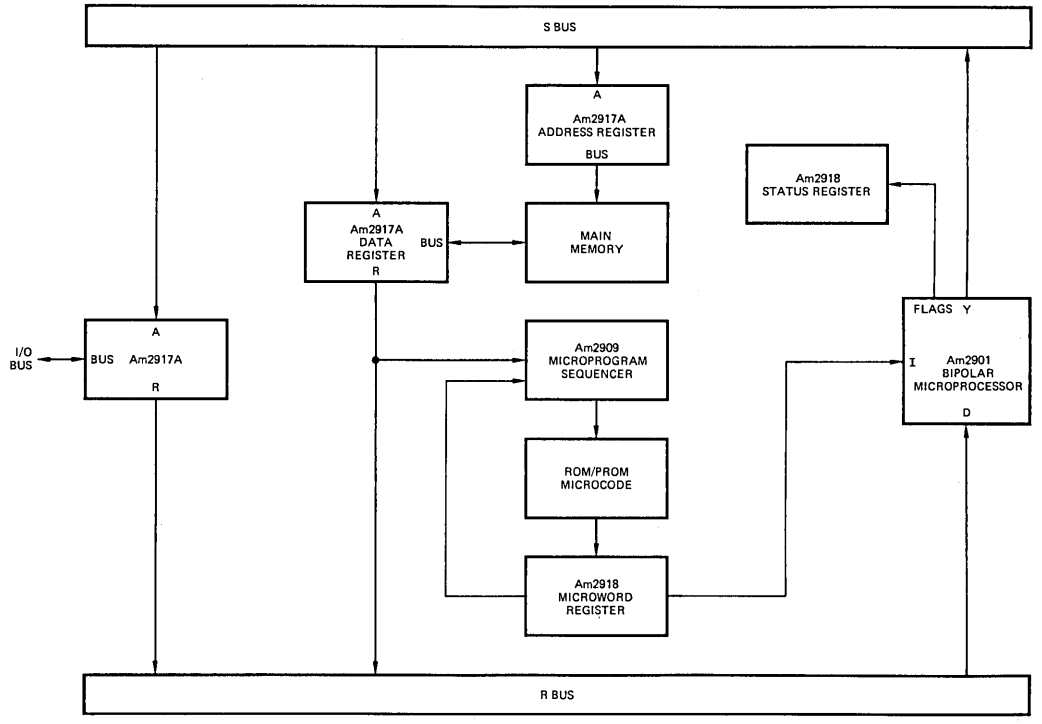
ODD Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	$ODD = A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	$ODD = Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

APPLICATIONS



The Am2917A can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.

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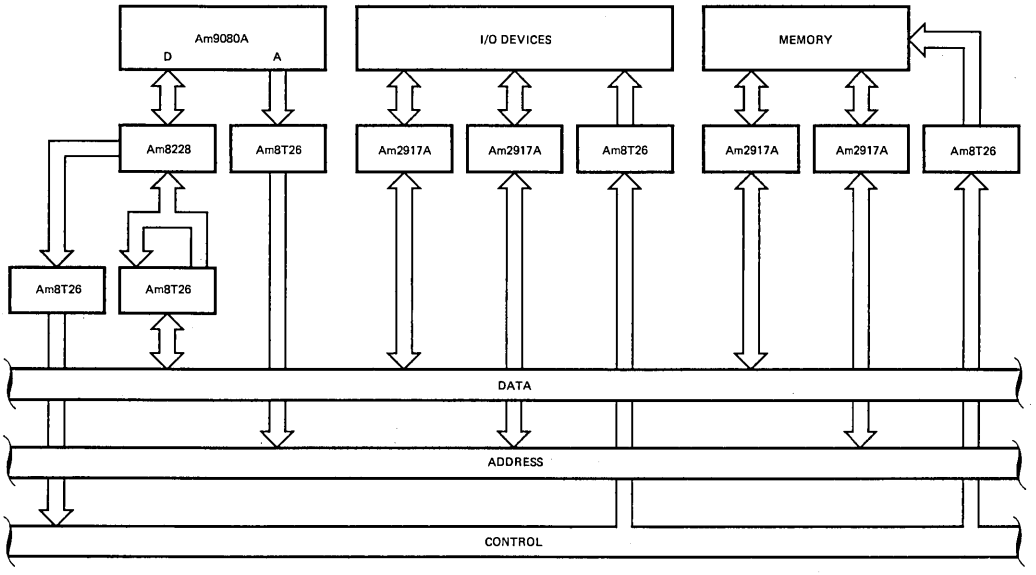

Using the Am2917A and Am8T26 in a terminated Bus system for the Am9080 MOS Microprocessor.

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Am2918

Quad D Register With Standard And Three-State Outputs

Distinctive Characteristics

- Advanced Schottky technology
- Four D-type flip-flops
- Four standard totem-pole outputs
- Four three-state outputs
- 75 MHz clock frequency
- 100% reliability assurance testing in compliance with MIL-STD-883

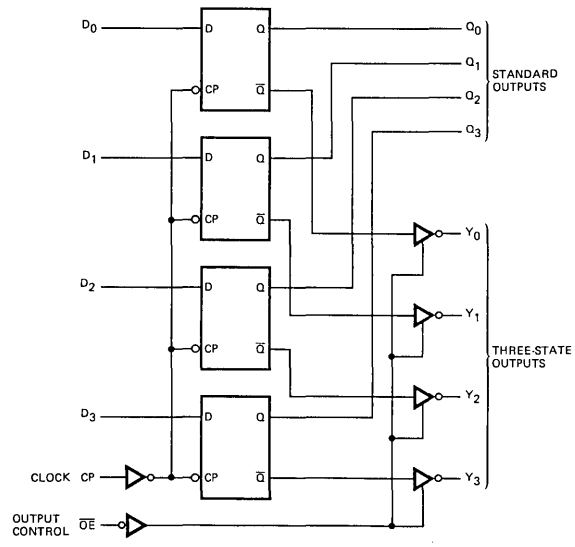
FUNCTIONAL DESCRIPTION

New Schottky circuits such as the Am2918 register provide the design engineer with additional flexibility in system configuration — especially with regard to bus structure, organization and speed. The Am2918 is a quadruple D-type register with four standard totem pole outputs and four three-state bus-type outputs. The 16-pin device also features a buffered common clock (CP) and a buffered common output control ($\overline{OE}$) for the Y outputs. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am2918 register can be used in bipolar microprocessor designs as an address register, status register, instruction register or for various data or microword register applications. Because of the unique design of the three-state output, the device features very short propagation delay from the clock to the Q or Y outputs. Thus, system performance and architectural design can be improved by using the Am2918 register. Other applications of Am2918 register can be found in microprogrammed display systems, communication systems and most general or special purpose digital signal processing equipment.

LOGIC DIAGRAM



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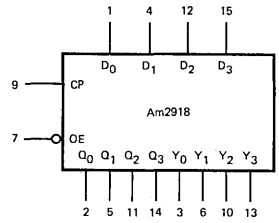
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2918PC	P-16	C	C-1
AM2918DC	D-16	C	C-1
AM2918DC-B	D-16	C	B-1
AM2918DM	D-16	M	C-3
AM2918DM-B	D-16	M	B-3
AM2918FM	F-16	M	C-3
AM2918FM-B	F-16	M	B-3
AM2918XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2918XM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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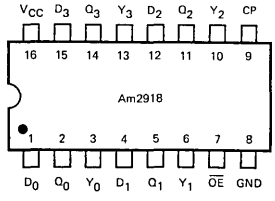
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2918XC	T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am2918XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ± 10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Q	I_{OH} = −1mA MIL	2.5	3.4		Volts
				I_{OH} = −1mA COM'L	2.7	3.4		
			Y	XM, I_{OH} = −2mA	2.4	3.4		
				XC, I_{OH} = −6.5mA	2.4	3.4		
V_{OL}	Output LOW Voltage (Note 6)	V_{CC} = MIN., I_{OL} = 20mA; V_{IN} = V_{IH} or V_{IL}					0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V					−2.0	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					50	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_O	Y Output Off-State Leakage Current	V_{CC} = MAX.		V_O = 2.4V			50	µA
				V_O = 0.4V			−50	
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.			−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)				80	130	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, T_A = 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test shoud not exceed one second.
5. I_{CC} is measured with all inputs at 4.5V and all outputs open.
6. Measured on Q outputs with Y outputs open. Measured on Y outputs with Q outputs open.

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0V, R_L = 280Ω)

Parameters	Description		Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Q Output		C_L = 15pF		6.0	9.0	ns
t_{PHL}					8.5	13	
t_{pw}	Clock Pulse Width	HIGH		7.0			ns
		LOW		9.0			
t_s	Data			5.0			ns
t_h	Data			3.0			ns
t_{PLH}	Clock to Y Output ($\overline{OE}$ LOW)				6.0	9.0	ns
t_{PHL}					8.5	13	
t_{ZH}	Output Control to Output		C_L = 15 pF		12.5	19	ns
t_{ZL}					12	18	
t_{HZ}			C_L = 5.0 pF		4.0	6.0	
t_{LZ}					7.0	10.5	
f_{max}	Maximum Clock Frequency		C_L = 15pF	75	100		MHz

TRUTH TABLE

INPUTS			OUTPUTS		NOTES
$\overline{OE}$	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = LOW
H = HIGH
X = Don't care

NC = No change
↑ = LOW to HIGH transition
Z = High impedance

Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

DEFINITION OF FUNCTIONAL TERMS

D_i The four data inputs to the register.

Q_i The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

Y_i The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.

CP Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

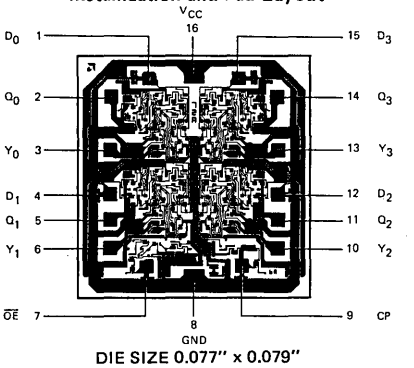
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_0	1	1	–	–
Q_0	2	–	20	10*
Y_0	3	–	40/130	10*
D_1	4	1	–	–
Q_1	5	–	20	10*
Y_1	6	–	40/130	10*
$\overline{OE}$	7	1	–	–
GND	8	–	–	–
CP	9	1	–	–
Y_2	10	–	40/130	10*
Q_2	11	–	20	10*
D_2	12	1	–	–
Y_3	13	–	40/130	10*
Q_3	14	–	20	10*
D_3	15	1	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

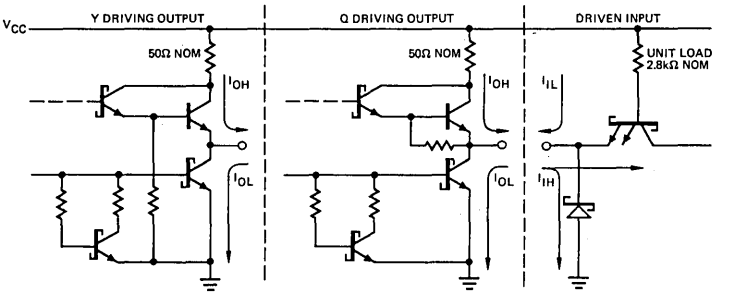
*Fan-out on each Q_i and Y_i output pair should not exceed 15 unit loads (30mA) for i = 0, 1, 2, 3.

Metallization and Pad Layout



DIE SIZE 0.077" x 0.079"

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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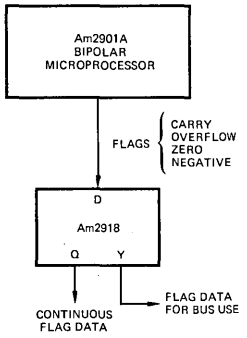
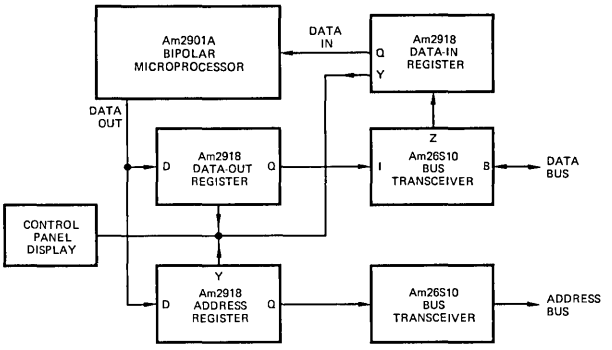
APPLICATIONS



The Am2918 as a 4-Bit status register



The Am2918 used as data-in, data-out and address registers.

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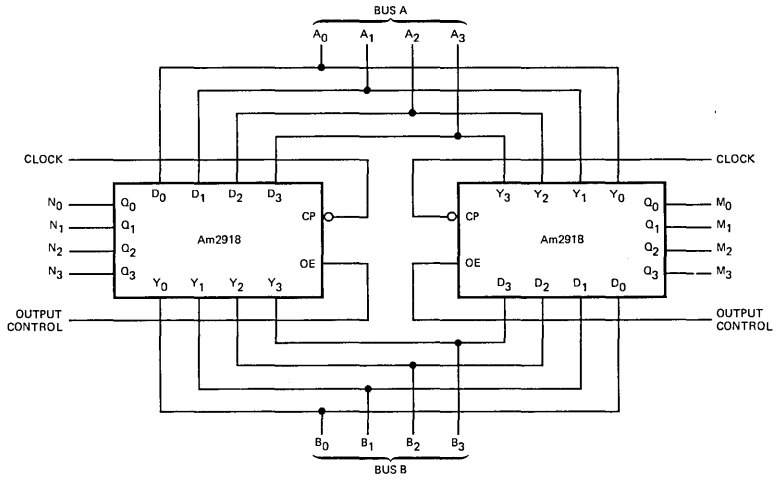

The Am2918 can be connected for bi-directional interface between two buses. The device on the left stores data from the A-bus and drives the A-bus. The device on the right stores data from the B-bus and drives the A-bus. The output control is used to place either or both drivers in the high-impedance state. The contents of each register are available for continuous usage at the N and M ports of the device.

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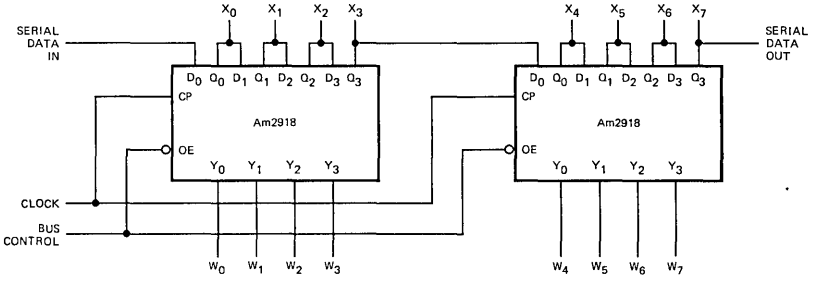


8-Bit serial to parallel converter with three-state output (W) and direct access to the register word (X).

MPR-189

Am29LS18

Quad D Register With Standard And Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Low-power Schottky version of the popular Am2918
- Four standard totem-pole outputs
- Four three-state outputs
- Four D-type flip-flops
- 100% product assurance testing to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am29LS18 consists of four D-type flip-flops with a buffered common clock. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

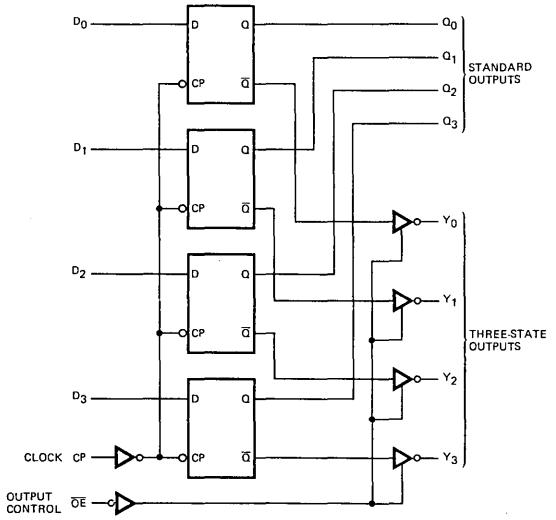
The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" (OE) input is LOW. When the OE input is HIGH, the Y outputs are in the high-impedance state.

The Am29LS18 is a 4-bit, high-speed register intended for use in real-time signal processing systems where the standard outputs are used in a recursive algorithm and the three-state outputs provide access to a data bus to dump the results after a number of iterations.

The device can also be used as an address register or status register in computers or computer peripherals.

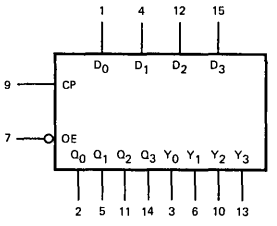
Likewise, the Am29LS18 is also useful in certain display applications where the standard outputs can be decoded to drive LED's (or equivalent) and the three-state outputs are bus organized for occasional interrogation of the data as displayed.

LOGIC DIAGRAM



MPR-190

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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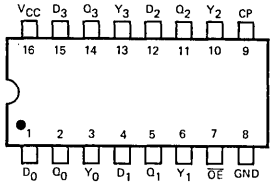
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (MIN. = 4.75V MAX. = 5.25V)
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (MIN. = 4.50V MAX. = 5.50V)

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	Q, $I_{OH} = -660\mu A$	MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
			Y	MIL, $I_{OH} = -1.0mA$	2.4	3.4		
				COM'L, $I_{OH} = 2.6mA$	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 12mA$				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$					0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				17	28	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. I_{CC} is measured with all inputs at 4.5V and all outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to $+V_{CC}$ max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0 V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Q_i			18	27	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				18	27		
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			18	27	ns	
t_{PHL}				18	27		
t_{pw}	Clock Pulse Width	LOW	18			ns	
		HIGH	15				
t_s	Data		15			ns	
t_h	Data		5.0			ns	
t_{ZH}	$\overline{OE}$ to Y_i			7.0	11	ns	
t_{ZL}				8	12		
t_{HZ}	$\overline{OE}$ to Y_i			14	21	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				12	18		
f_{max}	Maximum Clock Frequency (Note 1)		35	50		MHz	

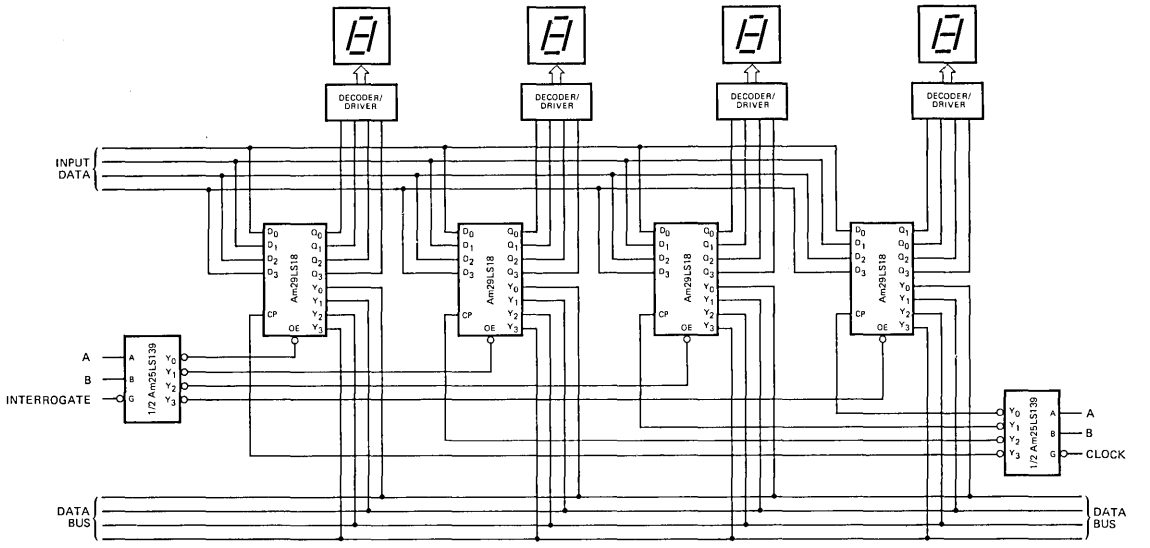
Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am29LS18PC, DC: T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%		Am29LS18DM, FM: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%		Units	Test Conditions
			Min.	Max.	Min.	Max.		
t_{PLH}	Clock to Q_i			38		45	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				38		45		
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			35		40	ns	
t_{PHL}				35		40		
t_{pw}	Clock Pulse Width	LOW	20		20		ns	
		HIGH	20		20			
t_s	Data		15		15		ns	
t_h	Data		5.0		5.0		ns	
t_{ZH}	$\overline{OE}$ to Y_i			15		17	ns	
t_{ZL}				16		17		
t_{HZ}	$\overline{OE}$ to Y_i			27		30	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				24		30		
f_{max}	Maximum Clock Frequency (Note 1)		30				MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

APPLICATIONS



The Am29LS18 used as a display register with bus interrogate capability.

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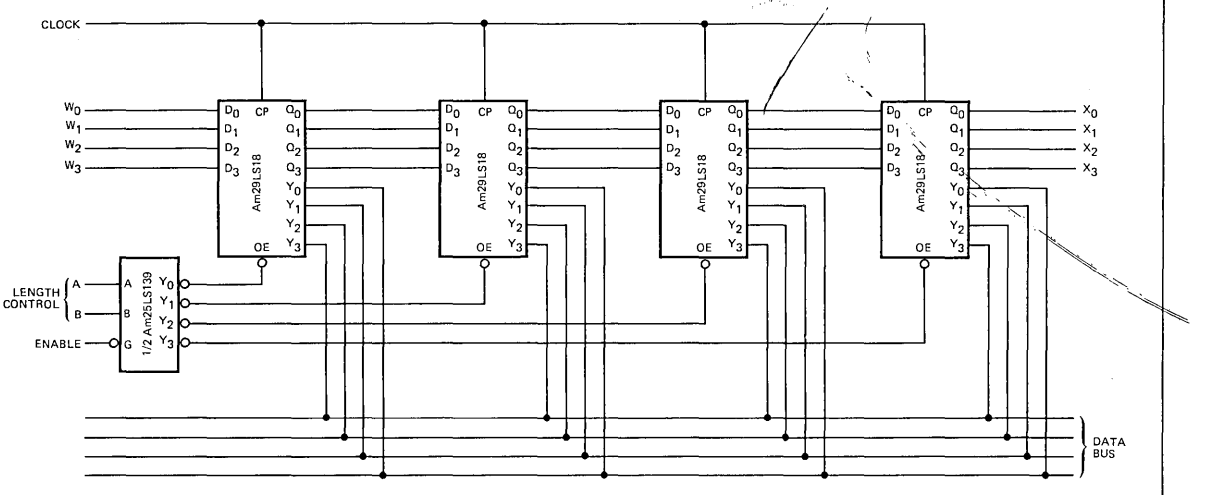
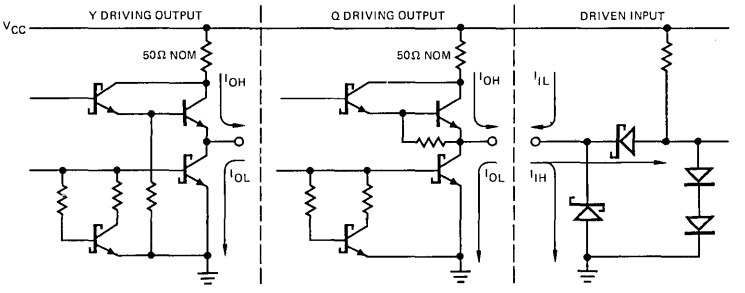


The Am29LS18 as a variable length (1, 2, 3 or 4 word) shift register.

MPR-194

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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DEFINITION OF FUNCTIONAL TERMS

D_i The four data inputs to the register.

Q_i The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

Y_i The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.

CP Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

TRUTH TABLE

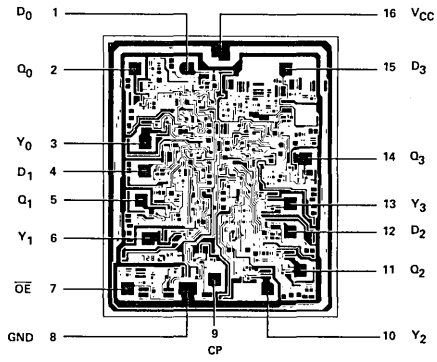
INPUTS			OUTPUTS		NOTES
$\overline{OE}$	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = LOW
H = HIGH
X = Don't care

NC = No change
↑ = LOW to HIGH transition
Z = High impedance

Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

Metallization and Pad Layout



DIE SIZE 0.083" x 0.099"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM29LS18PC	P-16	C	C-1
AM29LS18DC	D-16	C	C-1
AM29LS18DC-B	D-16	C	B-1
AM29LS18DM	D-16	M	C-3
AM29LS18DM-B	D-16	M	B-3
AM29LS18FM	F-16	M	C-3
AM29LS18FM-B	F-16	M	B-3
AM29LS18XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM29LS18XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am2919

Quad Register With Dual Three-State Outputs

DISTINCTIVE CHARACTERISTICS

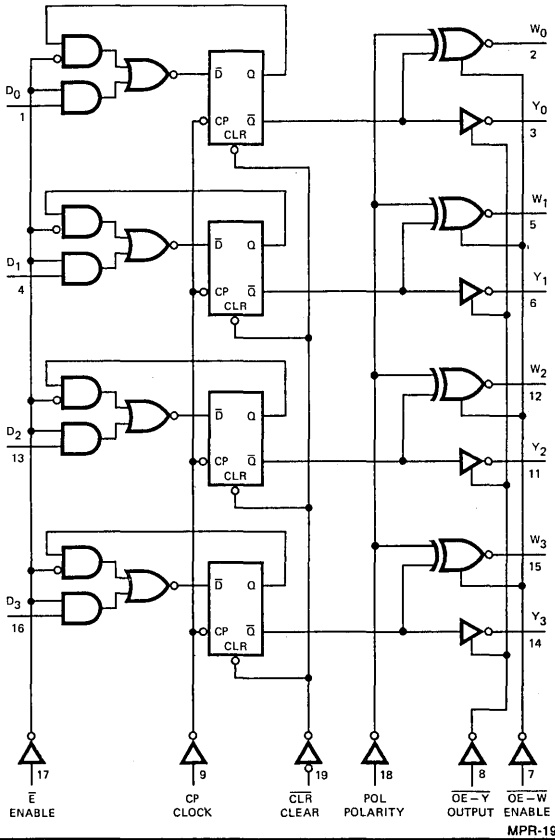
- Two sets of three-state outputs
- Four D-type flip-flops
- Polarity control on one set of outputs
- Buffered common clock enable
- Buffered common asynchronous clear
- Separate buffered common output enable for each set of outputs
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2919 consists of four D-type flip-flops with a buffered common clock enable. Information meeting the set-up and hold time requirements of the D inputs is transferred to the flip-flop outputs on the LOW-to-HIGH transition of the clock. Data on the Q outputs of the flip-flops is enabled at the three-state outputs when the output control ($\overline{OE}$) input is LOW. When the appropriate $\overline{OE}$ input is HIGH, the outputs are in the high impedance state. Two independent sets of outputs—W and Y—are provided such that the register can simultaneously and independently drive two buses. One set of outputs contains a polarity control such that the outputs can either be inverting or non-inverting.

The device also features an active LOW asynchronous clear. When the clear input is LOW, the Q output of the internal flip-flops are forced LOW independent of the other inputs. The Am2919 is packaged in a space-saving (0.3-inch row spacing) 20-pin package.

LOGIC DIAGRAM



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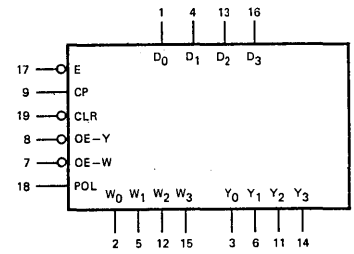
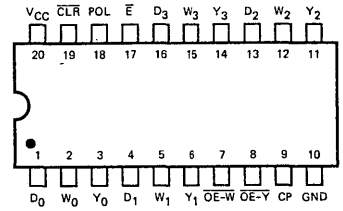
LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

MPR-197

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75 V	MAX. = 5.25 V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$	2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$	2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$			0.4	Volts
			$I_{OL} = 8.0mA$			0.45	
			$I_{OL} = 12mA$			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$				−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$				20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$				0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$			−20	μA
			$V_O = 2.4V$			20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.	MIL		24	36	mA
			COM'L		24	39	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Inputs grounded; outputs open.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

FUNCTION TABLE

FUNCTION	INPUTS							INTERNAL	OUTPUTS	
	CP	D_i	$\overline{E}$	$\overline{CLR}$	POL	$\overline{OE\text{-}W}$	$\overline{OE\text{-}Y}$	Q	W_i	Y_i
Output Three-State Control	X	X	X	X	X	H	L	NC	Z	Enabled
	X	X	X	X	X	L	H	NC	Enabled	Z
	X	X	X	X	X	H	H	NC	Z	Z
	X	X	X	X	X	L	L	NC	Enabled	Enabled
W_i Polarity	X	X	X	X	L	L	L	NC	Inverting	Non-Inverting
	X	X	X	X	H	L	L	NC	Non-Inverting	Non-Inverting
Asynchronous Clear	X	X	X	L	X	X	X	L	–	–
Clock Enable	↑	X	H	H	X	X	X	NC	–	–
	↑	L	L	H	X	X	X	L	–	–
	↑	H	L	H	X	X	X	H	–	–

L = LOW Z = High Impedance X = Don't Care ↑ = LOW-to-HIGH Transition
H = HIGH NC = No Change

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PHL}	Clock to Y_i			22	33	ns	C_L = 15pF R_L = 2.0kΩ
t_{PHL}				20	30		
t_{PLH}	Clock to W_i			24	36	ns	
t_{PHL}	(Either Polarity)			24	36		
t_{PHL}	Clear to Y_i			29	43	ns	
t_{PLH}	Clear to W_i			25	37	ns	
t_{PHL}				30	45		
t_{PLH}	Polarity to W_i			23	34	ns	
t_{PHL}				25	37		
t_{pw}	Clear		18			ns	
t_{pw}	Clock Pulse Width	LOW	15			ns	
		HIGH	18				
t_s	Data		15			ns	
t_h	Data		5			ns	
t_s	Data Enable		20			ns	
t_h	Data Enable		0			ns	
t_s	Set-up Time, Clear Recovery (Inactive) to Clock		20	15		ns	
t_{ZH}	Output Enable to W or Y			11	17	ns	
t_{ZL}				13	20		
t_{HZ}	Output Enable to W or Y			13	20	ns	C_L = 5.0pF R_L = 2.0kΩ
t_{LZ}				11	17		
f_{max}	Maximum Clock Frequency (Note 1)		35	45		MHz	C_L = 15pF R_L = 2.0kΩ

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am2919PC, DC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% Min.	Max.	Am2919DM, FM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% Min.	Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i			39		42	ns	C_L = 50pF R_L = 2.0kΩ
t_{PHL}				39		45		
t_{PLH}	Clock to W_i			41		43	ns	
t_{PHL}	(Either Polarity)			44		48		
t_{PHL}	Clear to Y_i			52		58	ns	
t_{PLH}	Clear to W_i			42		43	ns	
t_{PHL}				51		53		
t_{PLH}	Polarity to W_i			41		45	ns	
t_{PHL}				42		44		
t_{pw}	Clear		20		20		ns	
t_{pw}	Clock	LOW	20		20		ns	
		HIGH	20		20			
t_s	Data		15		15		ns	
t_h	Data		10		10		ns	
t_s	Data Enable		25		25		ns	
t_h	Data Enable		0		0		ns	
t_s	Set-up Time, Clear Recovery (Inactive) to Clock		23		24		ns	
t_{ZH}	Output Enable to W_i or Y_i			24		27	ns	
t_{ZL}				29		35		
t_{HZ}	Output Enable to W_i or Y_i			33		45	ns	C_L = 5.0pF R_L = 2.0kΩ
t_{LZ}				22		26		
f_{max}	Maximum Clock Frequency (Note 1)		30		25		MHz	C_L = 50pF R_L = 2.0kΩ

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

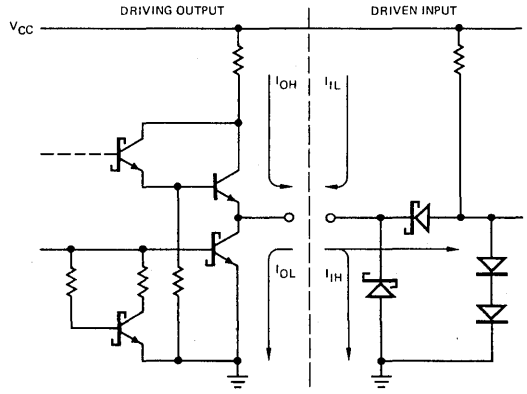
D_i	Any of the four D flip-flop data lines.
$\overline{E}$	Clock Enable. When LOW, the data is entered into the register on the next clock LOW-to-HIGH transition. When HIGH, the data in the register remains unchanged, regardless of the data in.
CP	Clock Pulse. Data is entered into the register on the LOW-to-HIGH transition.
$\overline{OE\text{-}W}$, $\overline{OE\text{-}Y}$	Output Enable. When $\overline{OE}$ is LOW, the register is enable to the output. When HIGH, the output is in the high-impedance state. The $\overline{OE\text{-}W}$ controls the W set of outputs, and $\overline{OE\text{-}Y}$ controls the Y set.
Y_i	Any of the four non-inverting three-state output lines.
W_i	Any of the four three-state outputs with polarity control.
POL	Polarity Control. The W_i outputs will be non-inverting when POL is HIGH, and when it is LOW, the outputs are inverting.
$\overline{CLR}$	Asynchronous Clear. When $\overline{CLR}$ is LOW, the internal Q flip-flops are reset to LOW.

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

Pin No.'s	Input/Output	Input Load	Output HIGH MIL	Output HIGH COM'L	Output LOW MIL	Output LOW COM'L
1	D_0	1.0	–	–	–	–
2	W_0	–	50	130	33	33
3	Y_0	–	50	130	33	33
4	D_1	1.0	–	–	–	–
5	W_1	–	50	130	33	33
6	Y_1	–	50	130	33	33
7	$\overline{OE\text{-}W}$	1.0	–	–	–	–
8	$\overline{OE\text{-}Y}$	1.0	–	–	–	–
9	CP	1.0	–	–	–	–
10	GND	–	–	–	–	–
11	Y_2		50	130	33	33
12	W_2		50	130	33	33
13	D_2	1.0	–	–	–	–
14	Y_3	–	50	130	33	33
15	W_3	–	50	130	33	33
16	D_3	1.0	–	–	–	–
17	$\overline{E}$	1.0	–	–	–	–
18	POL	1.0	–	–	–	–
19	$\overline{CLR}$	1.0	–	–	–	–
20	V_{CC}	–	–	–	–	–

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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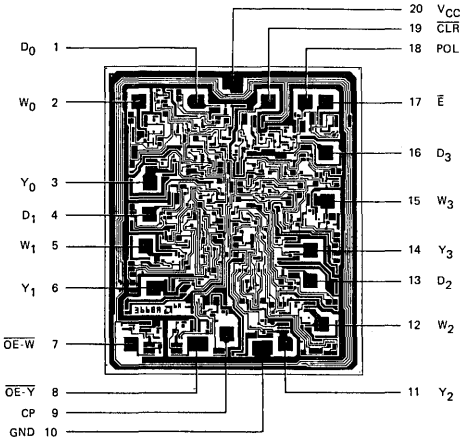
Metallization and Pad Layout



DIE SIZE 0.083" X 0.099"

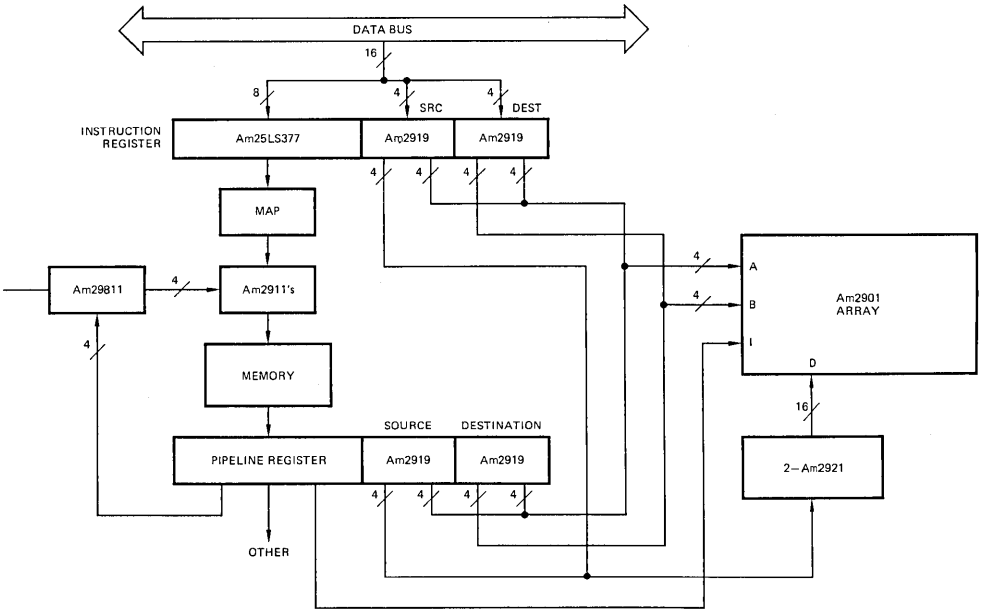
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2919PC	P-20	C	C-1
AM2919DC	D-20	C	C-1
AM2919DC-B	D-20	C	B-1
AM2919DM	D-20	M	C-3
AM2919DM-B	D-20	M	B-3
AM2919FM	F-20	M	C-3
AM2919FM-B	F-20	M	B-3
AM2919XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2919XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATION



The Am2919 provides for easy control of the selection of source and destination register addresses for the Am2901. These controls can emanate from both the instruction register and the pipeline register. The control is accomplished by three-state action at the Am2919 outputs. Four different register outputs can be selected by the B address which is the destination register in the Am2901. Two registers can be selected for the Am2901 A input which is a second RAM source.

The other pair of three-state outputs can be used for function control select as shown with the Am2921. Here, bit set, bit clear, bit toggle and bit test on any of the 16 bits can be performed.

MPR-200

Am2920

Octal D-Type Flip-Flop With Clear, Clock Enable And Three-State Control

DISTINCTIVE CHARACTERISTICS

- Buffered common clock enable input
- Buffered common asynchronous clear input
- Three-state outputs
- 8-bit, high-speed parallel register with positive edge-triggered, D-type flip-flops
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2920 is an 8-bit register built using advanced Low-Power Schottky technology. The register consists of eight D-type flip-flops with a buffered common clock, a buffered common clock enable, a buffered asynchronous clear input, and three-state outputs.

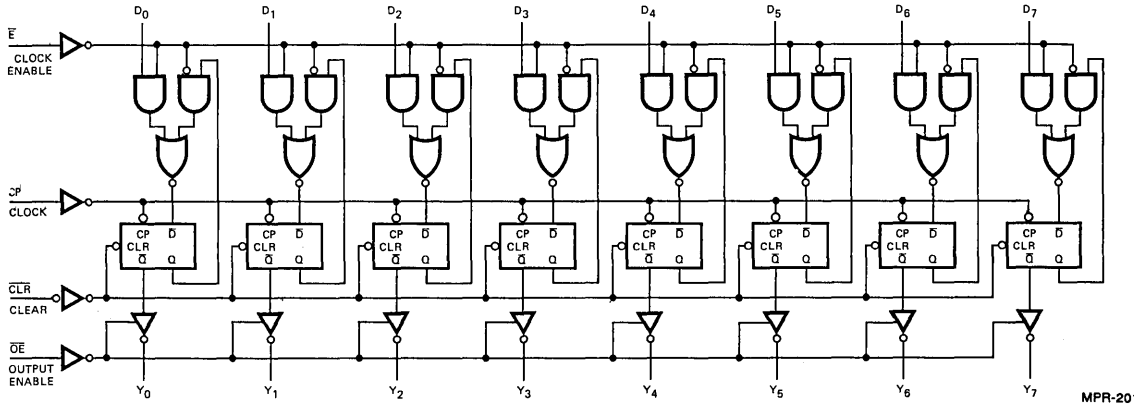
When the clear input is LOW, the internal flip-flops of the register are reset to logic 0 (LOW), independent of all other inputs. When the clear input is HIGH, the register operates in the normal fashion.

When the three-state output enable ($\overline{OE}$) input is LOW, the Y outputs are enabled and appear as normal TTL outputs. When the output enable ($\overline{OE}$) input is HIGH, the Y outputs are in the high impedance (three-state) condition. This does not affect the internal state of the flip-flop Q output.

The clock enable input ($\overline{E}$) is used to selectively load data into the register. When the $\overline{E}$ input is HIGH, the register will retain its current data. When the $\overline{E}$ is LOW, new data is entered into the register on the LOW-to-HIGH transition of the clock input.

This device is packaged in a space-saving (0.4-inch row spacing) 22-pin package.

LOGIC DIAGRAM



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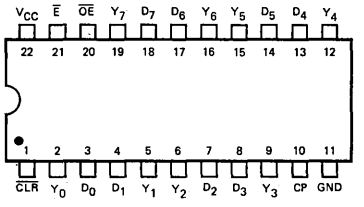
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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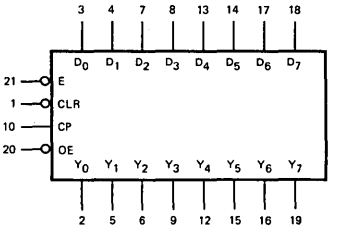
LOGIC SYMBOL



V_{CC} = Pin 22
GND = Pin 11

MPR-203

ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75 V	MAX. = 5.25 V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -1.0mA$		2.4	3.4		Volts
			COM'L, $I_{OH} = -2.6mA$		2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$					0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				24	37	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All outputs open, $\overline{E}$ = GND, Di inputs = CLR = $\overline{OE}$ = 4.5V. Apply momentary ground, then 4.5V to clock input.

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2920PC	P-22	C	C-1
AM2920DC	D-22	C	C-1
AM2920DC-B	D-22	C	B-1
AM2920DM	D-22	M	C-3
AM2920DM-B	D-22	M	B-3
AM2920FM	F-22	M	C-3
AM2920FM-B	F-22	M	B-3
AM2920XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2920XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +7.0V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description		Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			18	27	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}				24	36		
t_{PHL}	Clear to Y			22	35	ns	
t_s	Data (D_i)		10	3		ns	
t_h	Data (D_i)		10	3		ns	
t_s	Enable ($\overline{E}$)	Active	15	10		ns	
		Inactive	20	12			
t_h	Enable ($\overline{E}$)		0	0		ns	
t_s	Clear Recovery (In-Active) to Clock		11	7		ns	
t_{pw}	Clock	HIGH	20	14		ns	
		LOW	25	13			
t_{pw}	Clear		20	13		ns	
t_{ZH}	$\overline{OE}$ to Y_i			9	13	ns	
t_{ZL}				14	21		
t_{HZ}	$\overline{OE}$ to Y_i			20	30	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				24	36		
f_{max}	Maximum Clock Frequency (Note 1)			40		MHz	

Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description		Am2920PC,DC: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5% Min.	Am2920PC,DC Max.	Am2920DM,FM: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10% Min.	Am2920DM,FM Max.	Units	Test Conditions
t_{PLH}	Clock to Y_i ($\overline{OE}$ LOW)			33		39	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}				45		54		
t_{PHL}	Clear to Y			43		51	ns	
t_s	Data (D_i)		12		15		ns	
t_h	Data (D_i)		12		15		ns	
t_s	Enable ($\overline{E}$)	Active	17		20		ns	
		Inactive	20		23			
t_h	Enable ($\overline{E}$)		0		0		ns	
t_s	Clear Recovery (In-Active) to Clock		13		15		ns	
t_{pw}	Clock	HIGH	25		30		ns	
		LOW	30		35			
t_{pw}	Clear		22		25		ns	
t_{ZH}	$\overline{OE}$ to Y_i			19		25	ns	
t_{ZL}				30		39		
t_{HZ}	$\overline{OE}$ to Y_i			35		40	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}				39		42		
f_{max}	Maximum Clock Frequency (Note 1)		25		20		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

D_i The D flip-flop data inputs.

$\overline{CLR}$ When the clear input is LOW, the Q_i outputs are LOW, regardless of the other inputs. When the clear input is HIGH, data can be entered into the register.

CP Clock Pulse for the Register; enters data into the register on the LOW-to-HIGH transition.

Y_i The register three-state outputs.

$\overline{E}$ Clock Enable. When the clock enable is LOW, data on the D_i input is transferred to the Q_i output on the LOW-to-HIGH clock transition. When the clock enable is HIGH, the Q_i outputs do not change state, regardless of the data or clock input transitions.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Y_i outputs are in the high impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

FUNCTION TABLE

	Inputs					Internal	Outputs
Function	$\overline{OE}$	$\overline{CLR}$	$\overline{E}$	D_i	CP	Q_i	Y_i
Hi-Z	H	X	X	X	X	X	Z
Clear	H	L	X	X	X	L	Z
	L	L	X	X	X	L	L
Hold	H	H	H	X	X	NC	Z
	L	H	H	X	X	NC	NC
Load	H	H	L	L	↑	L	Z
	H	H	L	H	↑	H	Z
	L	H	L	L	↑	L	L
	L	H	L	H	↑	H	H

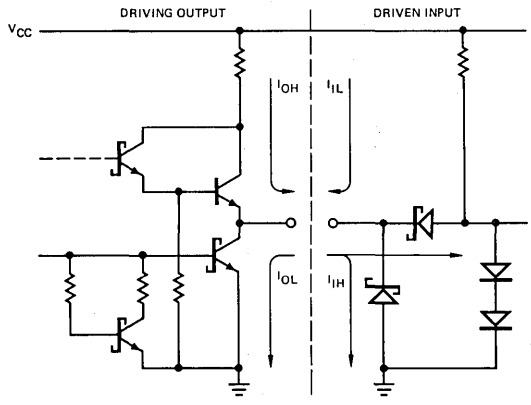
H = HIGH
L = LOW
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition
Z = High Impedance

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

		Am2920				
		Input	Output HIGH		Output LOW	
Pin No.'s	Input/Output	Load	MIL	COM'L	MIL	COM'L
1	$\overline{CLR}$	1	–	–	–	–
2	Y_0	–	50	130	22	22
3	D_0	1	–	–	–	–
4	D_1	1	–	–	–	–
5	Y_1	–	50	130	22	22
6	Y_2	–	50	130	22	22
7	D_2	1	–	–	–	–
8	D_3	1	–	–	–	–
9	Y_3	–	50	130	22	22
10	CP	1	–	–	–	–
11	GND	–	–	–	–	–
12	Y_4	–	50	130	22	22
13	D_4	1	–	–	–	–
14	D_5	1	–	–	–	–
15	Y_5	–	50	130	22	22
16	Y_6	–	50	130	22	22
17	D_6	1	–	–	–	–
18	D_7	1	–	–	–	–
19	Y_7	–	50	130	22	22
20	$\overline{OE}$	1	–	–	–	–
21	$\overline{E}$	1	–	–	–	–
22	V_{CC}	–	–	–	–	–

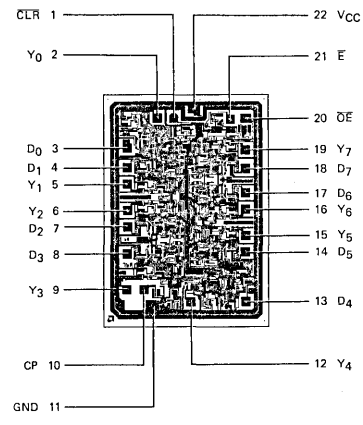
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

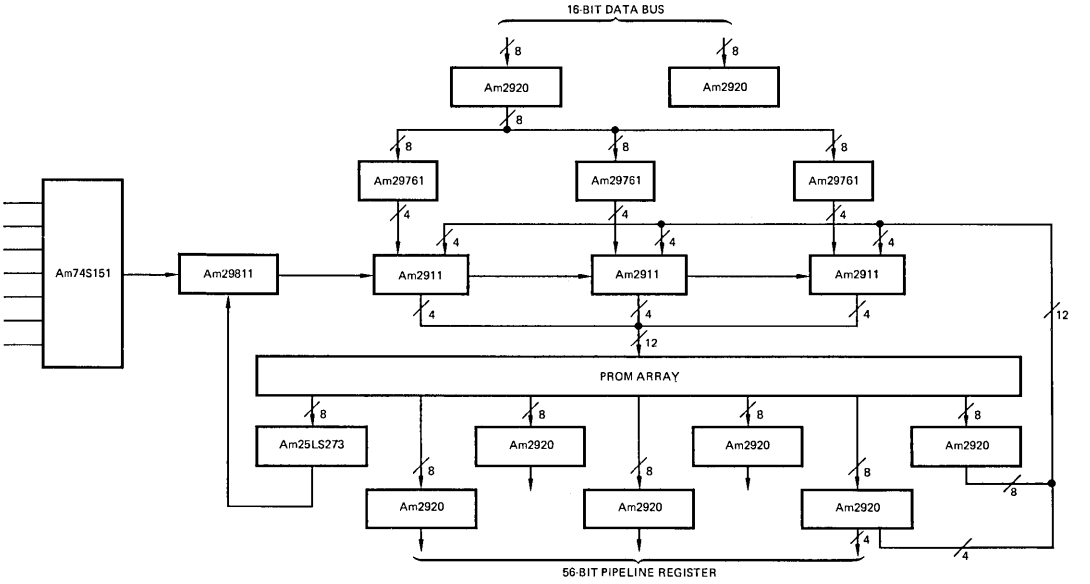
MPR-204

Metallization and Pad Layout



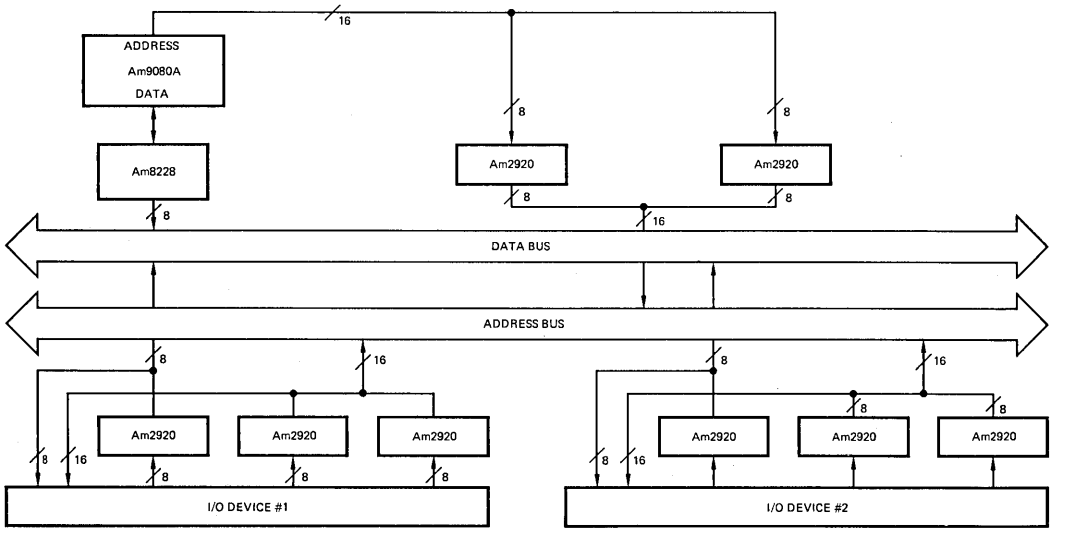
DIE SIZE 0.080" X 0.111"

APPLICATIONS



A typical Computer Control Unit for a microprogrammed machine.

MPR-205



The Am2920 is a useful device in interfacing with the Am9080A system buses.

MPR-206

Am2921

One-of-Eight Decoder
With Three-State Outputs And Polarity Control

DISTINCTIVE CHARACTERISTICS

- Three-state decoder outputs
- Buffered common output polarity control
- Inverting and non-inverting enable inputs
- AC parameters specified over operating temperature and power supply ranges.
- 100% reliability assurance testing in compliance with MIL-STD-883

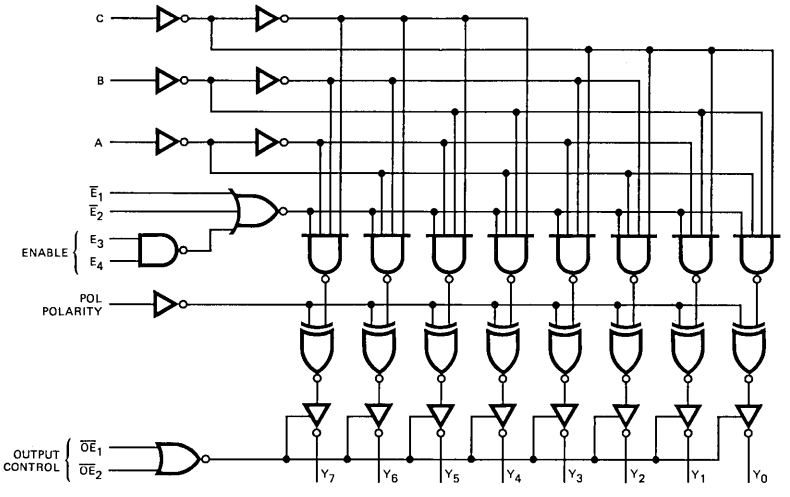
FUNCTIONAL DESCRIPTION

The Am2921 is a three-line to eight-line decoder/demultiplexer fabricated using advanced Low-Power Schottky technology. The decoder has three buffered select inputs—A, B, and C—that are decoded to one-of-eight Y outputs. Two active-HIGH and two active-LOW enables can be used for gating the decoder or can be used with incoming data for demultiplexing applications.

A separate polarity (POL) input can be used to force the function active-HIGH or active-LOW at the output. Two separate active-LOW output enables ($\overline{OE}$) inputs are provided. If either $\overline{OE}$ input is HIGH, the output is in the high impedance (off) state. When the POL input is LOW, the Y outputs are active-HIGH and when the POL input is HIGH, the Y outputs are active-LOW.

The device is packaged in a space saving (0.3-inch row spacing) 20-pin package.

LOGIC DIAGRAM
One-of-Eight Decoder



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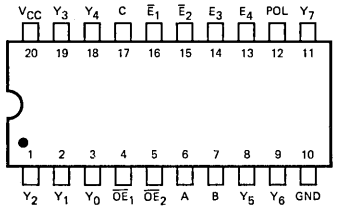
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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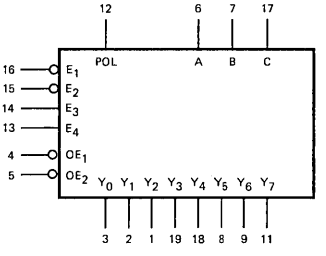
LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$	MIN. = 4.75 V	MAX. = 5.25 V
MIL	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$	MIN. = 4.50 V	MAX. = 5.50 V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = 1.0mA$ (MIL)		2.4	3.4		Volts
			$I_{OH} = -2.6mA$ (COM'L)		2.4	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$				0.4	Volts
			$I_{OL} = 8.0mA$				0.45	
			$I_{OL} = 12mA$				0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$					20	μA
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 7.0V$					0.1	mA
I_O	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$				−20	μA
			$V_O = 2.4V$				20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−15		−85	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.				21	34	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Test conditions: A = B = C = $\overline{E}_1 = \overline{E}_2$ = GND : $E_3 = E_4$ = POL = $\overline{OE}_1 = \overline{OE}_2 = 4.5V$.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5 V to +7.0 V
DC Voltage Applied to Outputs for High Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +7.0 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

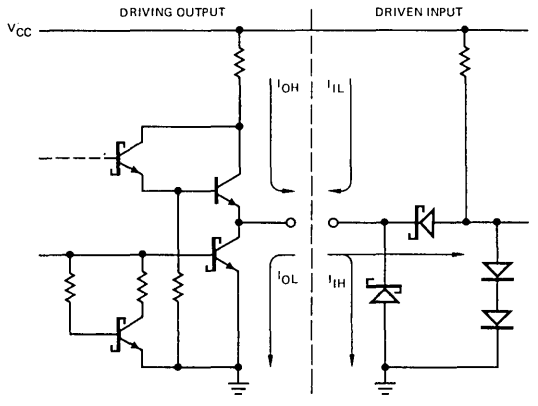
Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	A, B, C to Y_i		20	30	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			15	22		
t_{PLH}	$\overline{E_1}$, $\overline{E_2}$ to Y_i		19	28	ns	
t_{PHL}			20	30		
t_{PLH}	E_3, E_4 to Y_i		21	31	ns	
t_{PHL}			23	34		
t_{PLH}	POL to Y_i		16	24	ns	
t_{PHL}			20	30		
t_{ZH}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		17	25	ns	
t_{ZL}			14	21		
t_{HZ}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		17	25	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			20	30		

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am2921PC, DC: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%		Am2921DM, FM: T_A = −55°C to +125°C, V_{CC} = 5.0V ± 10%		Units	Test Conditions
		Min.	Max.	Min.	Max.		
t_{PLH}	A, B, C to Y_i		36		42	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			29		37		
t_{PLH}	$\overline{E_1}$, $\overline{E_2}$ to Y_i		34		39	ns	
t_{PHL}			38		45		
t_{PLH}	E_3, E_4 to Y_i		38		45	ns	
t_{PHL}			43		52		
t_{PLH}	POL to Y_i		29		34	ns	
t_{PHL}			39		49		
t_{ZH}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		38		45	ns	
t_{ZL}			23		25		
t_{HZ}	$\overline{OE_1}$, $\overline{OE_2}$ to Y_i		29		33	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{LZ}			33		36		

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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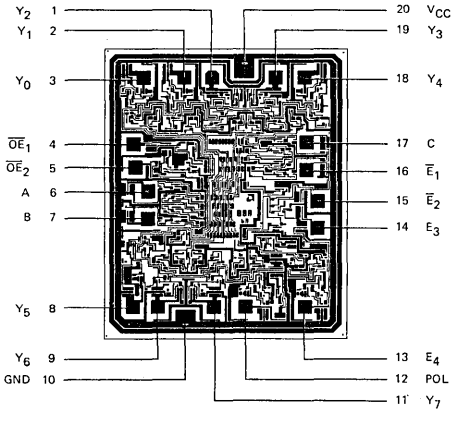
Metallization and Pad Layout



DIE SIZE 0.081" X 0.096"

DEFINITION OF FUNCTIONAL TERMS

A, B, C, D — The three select inputs to the decoder/demultiplexer.

$\overline{E}_1$, $\overline{E}_2$ — The active LOW enable inputs. A HIGH on either the $\overline{E}_1$ or $\overline{E}_2$ input forces all decoded functions to be disabled.

E_3, E_4 — The active HIGH enable inputs. A LOW on either E_3 or E_4 inputs forces all the decoded functions to be inhibited.

POL — Polarity Control. A LOW on the polarity control input forces the output to the active-HIGH state while a HIGH on the polarity control input forces the Y outputs to the active-LOW state.

$\overline{OE}_1$, $\overline{OE}_2$ — Output Enable. When both the $\overline{OE}_1$ and $\overline{OE}_2$ inputs are LOW, the Y outputs are enabled. If either $\overline{OE}_1$ or $\overline{OE}_2$ input is HIGH, the Y outputs are in the high impedance state.

Y_i — The eight outputs for the decoder/demultiplexer.

GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

Pin No.'s	Input/Output	Input Load	Output HIGH MIL	Output HIGH COM'L	Output LOW MIL	Output LOW COM'L
1	Y_2	–	50	130	33	33
2	Y_1	–	50	130	33	33
3	Y_0	–	50	130	33	33
4	$\overline{OE}_1$	1.0	–	–	–	–
5	$\overline{OE}_2$	1.0	–	–	–	–
6	A	1.0	–	–	–	–
7	B	1.0	–	–	–	–
8	Y_5	–	50	130	33	33
9	Y_6	–	50	130	33	33
10	GND	–	–	–	–	–
11	Y_7	–	50	130	33	33
12	POL	1.0	–	–	–	–
13	E_4	1.0	–	–	–	–
14	E_3	1.0	–	–	–	–
15	$\overline{E}_2$	1.0	–	–	–	–
16	$\overline{E}_1$	1.0	–	–	–	–
17	C	1.0	–	–	–	–
18	Y_4	–	50	130	33	33
19	Y_3	–	50	130	33	33
20	V_{CC}	–	–	–	–	–

FUNCTION TABLE

FUNCTION	INPUTS										OUTPUTS							
	$\overline{OE}_1$	$\overline{OE}_2$	$\overline{E}_1$	$\overline{E}_2$	E_3	E_4	POL	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
High Impedance	H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
	X	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	L	H	X	X	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	H	X	X	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	H	X	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	H	X	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	X	L	X	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	X	L	X	H	X	X	X	H	H	H	H	H	H	H	H
	L	L	X	X	X	L	L	X	X	X	L	L	L	L	L	L	L	L
	L	L	X	X	X	L	H	X	X	X	H	H	H	H	H	H	H	H
Active-HIGH Output	L	L	L	L	H	H	L	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	L	H	L	H	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	L	L	L	H	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	H	L	L	L	H	L	L	L	L
	L	L	L	L	H	H	L	H	L	L	L	L	L	L	H	L	L	L
	L	L	L	L	H	H	L	H	L	H	L	L	L	L	L	H	L	L
	L	L	L	L	H	H	L	H	H	L	L	L	L	L	L	L	H	L
	L	L	L	L	H	H	L	H	H	H	L	L	L	L	L	L	L	H
Active-LOW Output	L	L	L	L	H	H	H	L	L	L	L	H	H	H	H	H	H	H
	L	L	L	L	H	H	H	L	L	H	H	L	H	H	H	H	H	H
	L	L	L	L	H	H	H	L	H	L	H	H	L	H	H	H	H	H
	L	L	L	L	H	H	H	L	H	H	H	H	H	L	H	H	H	H
	L	L	L	L	H	H	H	L	H	L	H	H	H	H	L	H	H	H
	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	H	H
	L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	L	H
	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH L = LOW X = Don't Care Z = High Impedance

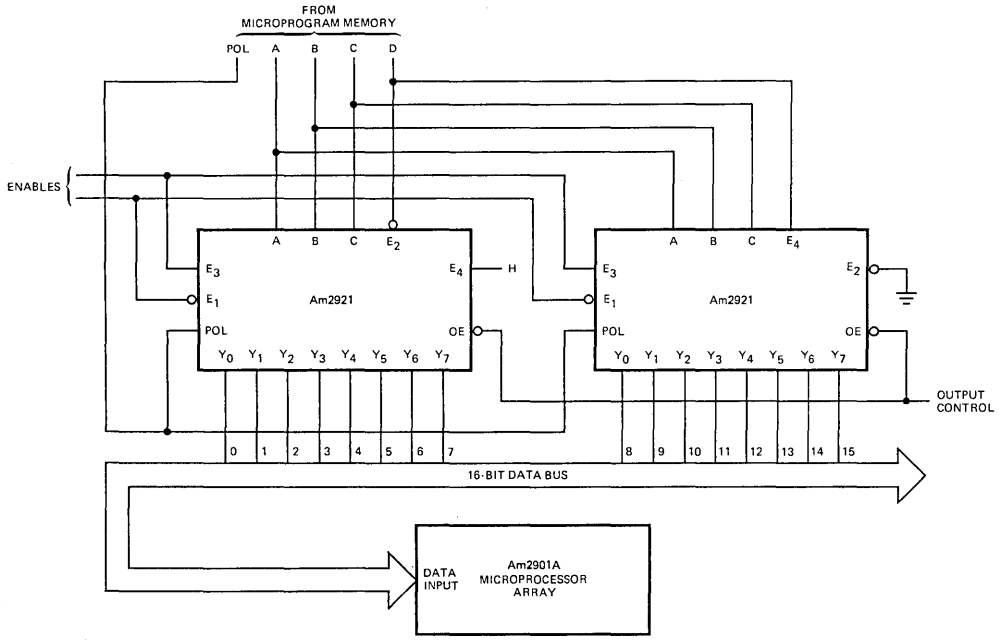
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2921PC	P-20	C	C-1
AM2921DC	D-20	C	C-1
AM2921DC-B	D-20	C	B-1
AM2921DM	D-20	M	C-3
AM2921DM-B	D-20	M	B-3
AM2921FM	F-20	M	C-3
AM2921FM-B	F-20	M	B-3
AM2921XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2921XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATIONS



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Two Am2921's can be used to perform a bit set, bit clear, bit toggle or bit test on any of sixteen bits in a microprocessor system. Examples of the operations performed are as follows:

Microprogram Control					16-Bit Field From Am2921															Am2901A ALU Function	Bit Function Performed On Selected Register
D	C	B	A	POL	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
0	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	OR	BIT SET
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1.	0	0	0	AND	BIT TEST
0	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	AND	BIT CLEAR
1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	EX NOR	BIT TOGGLE
1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	EX OR	BIT TOGGLE

Note: Bit test is performed using F = 0 output of Am2901A.

Am2922

Eight Input Multiplexer With Control Register

DISTINCTIVE CHARACTERISTICS

- High speed eight-input multiplexer
- On-chip Multiplexer Select and Polarity Control Register
- Output polarity control for inverting or non-inverting output
- Common register enable
- Asynchronous register clear
- Three-state output for expansion
- AC parameters specified over operating temperature and power supply ranges.
- 100% product assurance testing to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am2922 is an eight-input Multiplexer with Control Register. The device features high speed from clock to output and is intended for use in high speed computer control units or structured state machine designs.

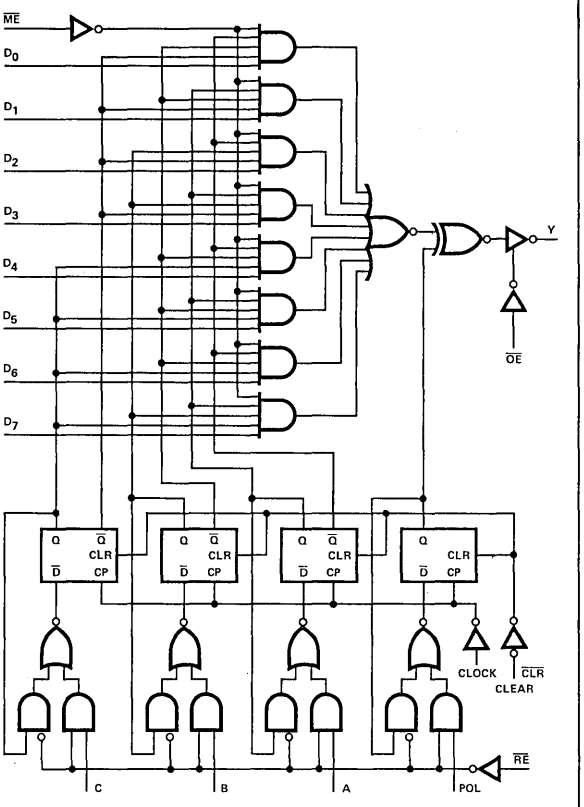
The Am2922 contains an internal register which holds the A, B and C multiplexer select lines as well as the POL (Polarity) control bit. When the Register Enable input ($\overline{RE}$) is LOW, new data is entered into the register on the LOW-to-HIGH, transition of the clock. When $\overline{RE}$ is HIGH, the register retains its current data. An asynchronous clear input ($\overline{CLR}$) is used to reset the register to a logic LOW level.

The A, B and C register outputs select one of eight multiplexer data inputs. A HIGH on the Polarity Control flip-flop output causes a true (non-inverting) multiplexer output, and a LOW causes the output to be inverted. In a computer control unit, this allows testing of either true or complemented flag data at the microprogram sequencer test input.

An active LOW Multiplexer Enable input ($\overline{ME}$) allows the selected multiplexer input to be passed to the output. When $\overline{ME}$ is HIGH, the output is determined only by the Polarity Control bit.

The Am2922 also features a three-state Output Enable control ($\overline{OE}$) for expansion. When $\overline{OE}$ is LOW, the output is enabled. When $\overline{OE}$ is HIGH, the output is in the high impedance state.

LOGIC DIAGRAM



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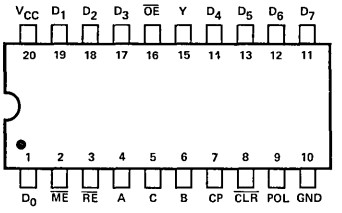
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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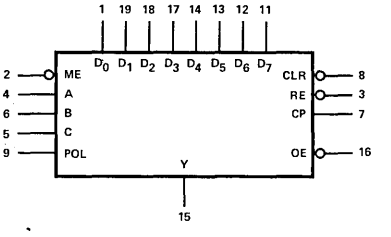
LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

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ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ MIN. = 4.75V MAX. = 5.25V
MIL $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	MIL, $I_{OH} = -2.0mA$	2.4	3.4		Volts
			COM'L, $I_{OH} = -6.5mA$	2.4	3.2		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 4.0mA$			0.4	Volts
			$I_{OL} = 8.0mA$			0.45	
			$I_{OL} = 20mA$			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., $I_{IN} = -18mA$				-1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., $V_{IN} = 0.4V$	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$			-0.72	mA
			D_N, A, B, C, POL, CP, $\overline{CLR}$			-2.0	
I_{IH}	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 2.7V$	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$			40	μA
			D_N, A, B, C, POL, CP, $\overline{CLR}$			50	
I_I	Input HIGH Current	V_{CC} = MAX., $V_{IN} = 5.5V$	$\overline{ME}$, $\overline{OE}$, $\overline{RE}$			0.1	mA
			D_N, A, B, C, POL, CP, $\overline{CLR}$			1.0	
I_{OZ}	Off-State (High-Impedance) Output Current	V_{CC} = MAX.	$V_O = 0.4V$			-50	μA
			$V_O = 2.4V$			50	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		-40		-100	mA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = MAX.			97	148	mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. D_N, A, B, C, POL, $\overline{ME}$ at Gnd. All other inputs and outputs open. Measured after a momentary ground then 4.5V applied to clock input.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential Continuous	-0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	-0.5V to +V_{CC} max.
DC Input Voltage	-0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	-30mA to +5.0mA

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Min.	Typ.	Max.	Units	Test Conditions
t_{PLH}	Clock to Y POL – LOW		21	32	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			19	29		
t_{PLH}	Clock to Y POL – HIGH		16	24	ns	
t_{PHL}			19	29		
t_{PLH}	D_n to Y		10	16	ns	
t_{PHL}			13	19		
t_{PLH}	CLR to Y		22	33	ns	
t_{PHL}			22	33		
t_{PLH}	ME to Y		12	18	ns	
t_{PHL}			12	18		
t_{ZL}	OE to Y		8	14	ns	
t_{ZH}			8	14		
t_{LZ}			10	17	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{HZ}			10	17		
t_s	A, B, C, POL	10			ns	C_L = 15pF, R_L = 2.0kΩ
	CE	15				
t_s	CLR Recovery	5			ns	
t_{pw}	Clock	10			ns	
	Clear (LOW)	10				
t_h	A, B, C, POL, CE	0			ns	

SWITCHING CHARACTERISTICS OVER OPERATING RANGE*

Parameters	Description	Am2922PC, DC T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am2922PC, DC Max.	Am2922DM, FM T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am2922DM, FM Max.	Units	Test Conditions
t_{PLH}	Clock to Y, POL-L		40		47	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			34		38		
t_{PLH}	Clock to Y, POL-H		29		33	ns	
t_{PHL}			35		41		
t_{PLH}	D_N to Y		19		21	ns	
t_{PHL}			22		24		
t_{PLH}	CLR to Y		39		45	ns	
t_{PHL}			39		45		
t_{PLH}	ME to Y		22		26	ns	
t_{PHL}			19		20		
t_{ZL}	OE to Y		19		24	ns	
t_{ZH}			22		29		
t_{LZ}	OE to Y		24		30	ns	C_L = 5.0pF, R_L = 2.0kΩ
t_{HZ}			24		30		
t_s	A, B, C POL	11		12		ns	C_L = 50pF, R_L = 2.0kΩ
	CE	18		20			
t_s	CLR Recovery	6		7		ns	
t_{pw}	Clock	11		12		ns	
	Clear (LOW)	11		12			
t_H	A, B, C, POL, CE	3		3		ns	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

DEFINITION OF FUNCTIONAL TERMS

A, B, C Multiplexer Select Lines. One of eight multiplexer data inputs is selected by the A, B and C register outputs.

POL Polarity Control Bit. A HIGH register output causes a true (non-inverted) output and a LOW causes the output to be inverted.

$\overline{ME}$ Multiplexer Enable. When LOW, it enabled the 8-input multiplexer. When HIGH, the Y output is determined by only the Polarity Control bit.

$\overline{RE}$ Register Enable. When LOW, the Multiplexer Select and Polarity Control Register is enabled for loading. When HIGH, the register holds its current data.

$\overline{CLR}$ Clear. A LOW asynchronously resets the Multiplexer Select and Polarity Control Register.

D_1-D_8 Data Inputs to the 8-input multiplexer.

CP Clock Pulse. When $\overline{RE}$ is LOW, the Multiplexer Select and Polarity Control Register changes state on the LOW-to-HIGH transition of CP.

$\overline{OE}$ Output Enable. When LOW, the output is enabled. When HIGH, the output is in the high impedance state.

Y The chip output.

FUNCTION TABLE

MODE	INPUTS							INTERNAL				INPUTS		OUTPUT
	C	B	A	POL	$\overline{RE}$	$\overline{CLR}$	CP	Q_C	Q_B	Q_A	Q_{POL}	$\overline{ME}$	$\overline{OE}$	Y
Clear	X	X	X	X	X	L	X	L	L	L	L	H	L	H
	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	L	L	$\overline{D}_0$
												X	H	Z
Reg. Disable	X	X	X	X	H	H	X	NC	NC	NC	NC	L	L	D_i/D_i (Note 1)
Select (Multiplex)	L	L	L	L/H	L	H	↑	L	L	L	L/H	L	L	$\overline{D}_0/D_0$
	L	L	H	↓	↓	↓	↓	L	L	H	↓	↓	↓	$\overline{D}_1/D_1$
	L	H	L					L	H	L				$\overline{D}_2/D_2$
	L	H	H					L	H	H				$\overline{D}_3/D_3$
	H	L	L					H	L	L				$\overline{D}_4/D_4$
	H	L	H					H	L	H				$\overline{D}_5/D_5$
	H	H	L					H	H	L				$\overline{D}_6/D_6$
	H	H	H	↓	↓	↓	↓	H	H	H	↓	↓	↓	$\overline{D}_7/D_7$
Multiplexer Disable	X	X	X	X	X	H	X	X	X	X	L	H	L	H
	↓	↓	↓	↓	↓	↓	↓	X	X	X	H	H	L	L
Tri-state Output Disable	↓	↓	↓	↓	↓	↓	↓	X	X	X	X	X	H	Z

NC = No Change
X = Don't Care

Note 1: The output will follow the selected input, D_i, or its complement depending on the state of the POL flip-flop.

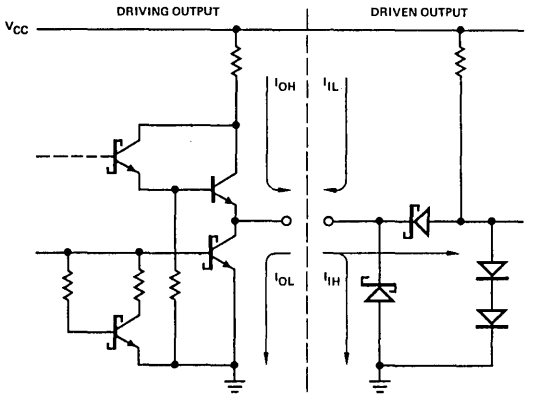
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2922PC	P-20	C	C-1
AM2922DC	D-20	C	C-1
AM2922DC-B	D-20	C	B-1
AM2922DM	D-20	M	C-3
AM2922DM-B	D-20	M	B-3
AM2922FM	F-20	M	C-3
AM2922FM-B	F-20	M	B-3
AM2922XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2922XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

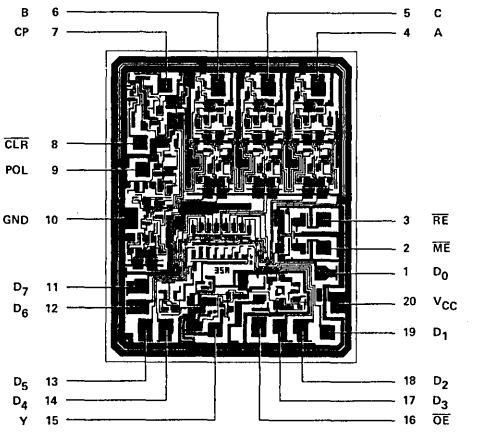
LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

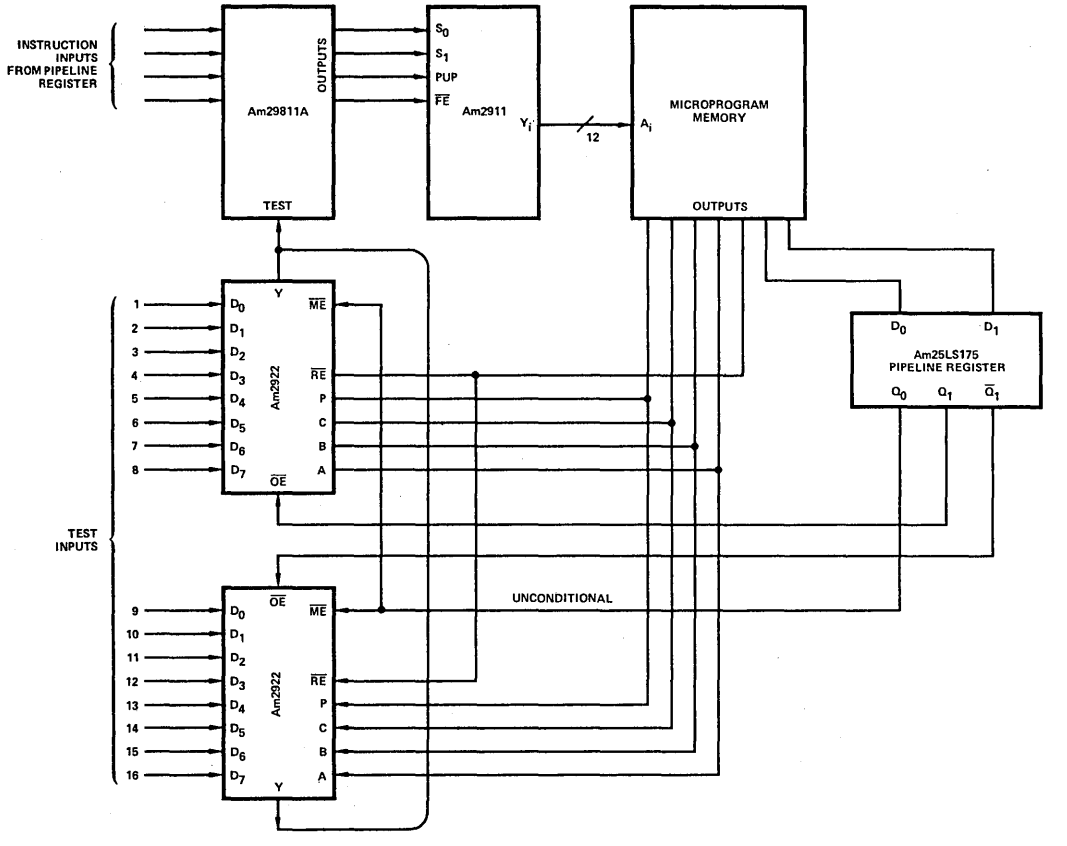
MPR-215

Metallization and Pad Layout



DIE SIZE 0.080" X 0.099"

APPLICATION



A versatile one-of-sixteen Test Select with Polarity Control and Test Select Hold.

MPR-216

Am2925

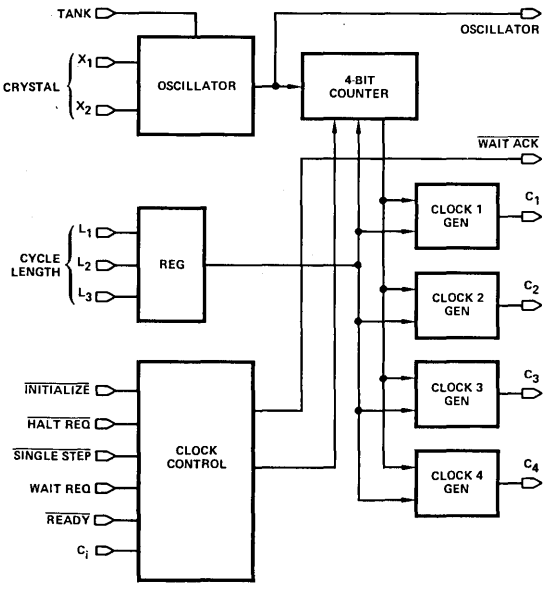
System Clock Generator and Driver

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- Single chip clock generator and driver
- Four different clock output waveforms for Am2900 and other bipolar and MOS systems
- Crystal controlled for stable system operation
- Oscillator to 31MHz – oscillator output for external system timing
- Clock halt, single-step and wait controls
- Variable cycle lengths – 1-of-8 different cycle lengths may be programmed
- 20-Pin package
- 100% product assurance screening to MIL-STD-883 requirements

LOGIC DIAGRAM



MPR-217

FUNCTIONAL DESCRIPTION

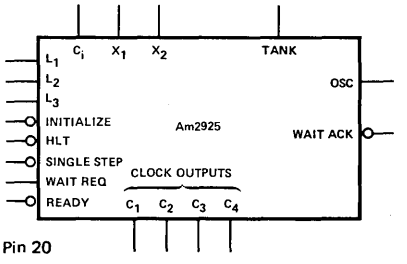
The Am2925 is a single-chip general purpose clock generator/driver. It is controlled by a crystal, selected by the designer, and is microprogrammable to meet a variety of system speed requirements. The Am2925 generates four different clock output waveforms tailored to meet the needs of Am2900 and other bipolar and MOS microprocessor based systems. Also, variable cycle lengths may be generated under microprogram control. One-of-eight different cycle lengths may be microprogrammed using the Cycle Length inputs L1, L2, and L3.

The Am2925 oscillator runs at frequencies up to 31MHz. An input pin is provided for a tank circuit which allows the use of overtone mode crystals. A buffered oscillator output is provided for external system timing.

Clock halt, single-step and wait controls are provided for the Am2925. The HALT REQ input halts the clocks; the clocks resume when the HALT REQ input is deactivated. The SINGLE-STEP input, which operates only when the clocks are halted, generates the clocks for a single cycle. The WAIT REQ input stops the clocks and puts the Am2925 in a "wait" state. In this state, the clocks remain stopped until an asynchronous READY input signal is received. The WAIT ACK output indicates when the Am2925 is in the "wait" state. The WAIT REQ and READY inputs are pulse sensitive and are overridden by the HALT REQ input.

One-of-eight cycle lengths may be microprogrammed using the L1, L2, and L3 inputs. There are four clock output waveforms for each of the eight possible cycle lengths.

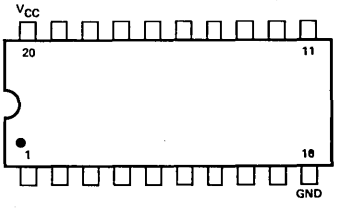
LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

MPR-218

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-219

Am2930

Program Control Unit

DISTINCTIVE CHARACTERISTICS

- Powerful, 4-bit slice address controller for memories
  Useful with both main memory and microprogram memory
  Expandable to generate any address length
- Executes 32 instructions
  Automatic generation of address and update of program counter for fetch cycles, branch cycles, and subroutine call and return
- Contains cascadable full adder
  Twelve different relative address modes are provided, including jump-to-subroutine relative and return-from-subroutine relative
- Built-in condition code input
  Sixteen instructions are dependent on external condition control
- Seventeen-level push/pop stack
  On-chip storage of subroutine return addresses nested up to 17 levels deep
- Separate incrementer for program counter
  A relative address may be computed and PC may be incremented by one on a single cycle

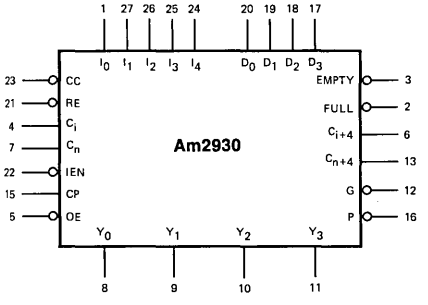
GENERAL DESCRIPTION

The Am2930 is a four-bit wide Program Control Unit intended to perform machine level addressing functions, although the device can also be used as a microprogram sequencer. Four Am2930's may be interconnected to generate a 16-bit address (64K words). The Am2930 contains a program counter, a subroutine stack, an auxiliary register, and a full adder for computing relative addresses.

The Am2930 performs five types of instructions. These are: 1) Unconditional Fetch; 2) Conditional Jump; 3) Conditional Jump-to-Subroutine; 4) Conditional Return-from-Subroutine; and 5) miscellaneous instructions.

There are four sources of data for the adder which generates the Address outputs (Y_0-Y_3). These are: 1) the Program Counter (PC); 2) the Stack (S); 3) the auxiliary Register(R); and 4) the Direct inputs (D). Under control of the Instruction inputs (I_0-I_4), the multiplexers at the adder inputs allow various combinations of these terms to be generated at the three-state Y address outputs. The instruction lines also control the updating of the program counter and the auxiliary register. A condition code input is provided for conditional instructions.

LOGIC SYMBOL



V_{CC} = Pin 28
GND = Pin 14

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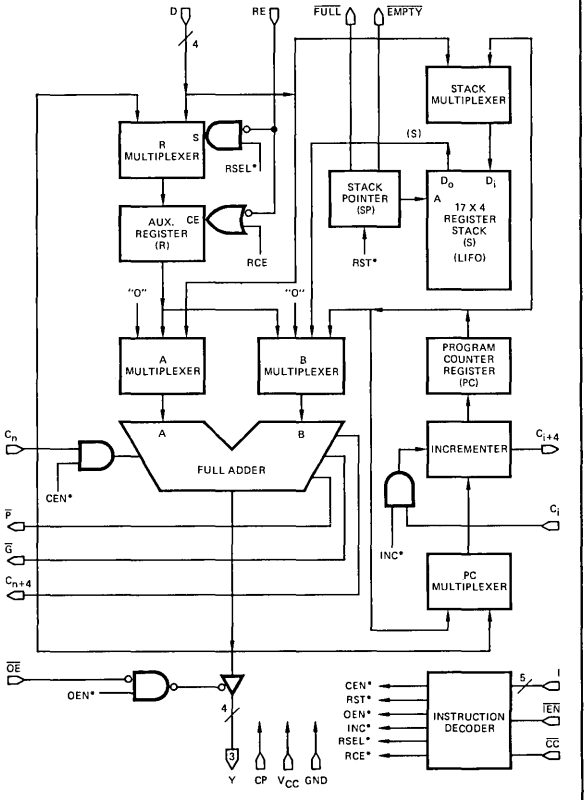
BLOCK DIAGRAM



MPR-221

ARCHITECTURE OF THE Am2930

The Am2930 is a bipolar Program Control Unit intended for use in high-speed microprocessor applications. The device is a cascadable, four-bit slice such that three devices allow addressing of up to 4K words of memory and four devices allow addressing of up to 64K words of memory.

As shown in the Block Diagram, the device consists of the following:

1) A full adder with input multiplexers
2) A Program Counter Register with an incrementer and an input multiplexer
3) A 17 x 4 Last-In, First-Out (LIFO) stack consisting of an input multiplexer, a 17 x 4 RAM, and a Stack Pointer
4) An auxiliary register with an input multiplexer
5) An instruction decoder
6) Four 3-state output buffers on the address outputs

The following paragraphs describe each of these blocks in detail.

Full Adder

The Full Adder is a binary device with full lookahead carry logic for high-speed addition and provision is made for further lookahead by including both carry propagate ($\overline{P}$) and carry generate ($\overline{G}$) outputs. In slower systems, the carry output (C_{n+4}) can be connected to the next higher C_n to provide ripple block arithmetic. The carry input to the adder (C_n) is internally inhibited during those instructions which do not require an addition to be performed. For these instructions, the data is passed directly through the adder, independent of the state of C_n.

The multiplexers at the A and B inputs of the adder are controlled by the Instruction decoder which selects the appropriate adder inputs for the selected instruction.

Program Counter

The program counter consists of a register preceeded by an incrementer. The Program Counter Register (PC) is a four-bit, edge-triggered, D-type register which is loaded from the incrementer output on the LOW-to-HIGH transition of the clock input (CP) at the end of every instruction.

The incrementer utilizes full lookahead logic for high speed. For cascading devices, the carry output of the incrementer (C_{i+4}) is connected to the incrementer carry input (C_i) of the next higher device. The output of the incrementer, which is loaded into the PC, is equal to the incrementer input plus C_i. Therefore, it is possible to control the entire cascaded incrementer from the C_i input of the least significant device; a LOW on the C_i input of the least significant device will simply pass the data from the multiplexer output to the inputs of PC; a HIGH will cause the outputs of the multiplexer to be incremented before they are loaded into PC. During three instructions (unconditional Hold and conditional Hold and Suspend when the $\overline{CC}$ input is LOW), the C_i input is internally inhibited; therefore, data is passed from the multiplexer output to the PC without incrementing. The multiplexer selects the input to the incrementer from either PC or the output of the Full Adder, depending upon the instruction being executed. During the Jump, Jump-to-Subroutine, and Return instructions, the multiplexer chooses the Full Adder outputs as the input to the incrementer if the $\overline{CC}$ input is LOW. The Full Adder output is also selected for the Reset instruction. For all other instructions, the PC is selected as the input to the incrementer.

17 x 4 LIFO Stack

The 17 x 4 LIFO stack consists of a multiplexer, a 17 x 4 RAM, and a Stack Pointer (SP) which address the words in the RAM.

The SP always points to the last word written into the RAM (Top of the Stack). The Top of the Stack (S) is available at the output of the RAM.

Data is pushed onto the Top of the Stack from either D or PC. It is written into memory location SP+1. The SP is incremented on the LOW-to-HIGH clock transition at the end of the cycle so that it still points to the last data written into the RAM.

For a Pop operation, the contents of the RAM are not changed, but the SP is decremented at the end of the cycle so that it then points to the new Top of the Stack.

The SP is an up/down counter which changes state on the LOW-to-HIGH transition of the Clock input. It is internally prevented from incrementing when the stack is full and from decrementing when the Stack is empty. When the Stack is full, the RAM write circuitry is also inhibited.

The active LOW Empty output ($\overline{EMPTY}$) is LOW when the stack is empty (after the Reset instruction and after the last word has been Popped from the stack); the active LOW Full output ($\overline{FULL}$) is LOW either when the stack is full or when the current instruction being executed will fill the stack (during and after the 17th Push).

Auxiliary Register (R)

The Auxiliary Register (R) can be loaded from either the Direct inputs (D) or the output of the Full Adder. It is loaded on the LOW-to-HIGH transition of the clock input (CP) if the Register Enable input ($\overline{RE}$) is LOW or if the Instruction inputs call for it to be loaded. When $\overline{RE}$ is LOW, R is loaded from the D inputs unless the Instruction dictates that R be loaded from the output of the Full Adder.

Instruction Decoder

The Instruction Decoder generates the signals necessary to establish the data paths and to enable the loading of the PC, R, SP, and RAM.

For unconditional instructions, the $\overline{CC}$ input is not utilized; it may be either HIGH or LOW. For conditional instructions, if $\overline{CC}$ is LOW, the condition is met and the conditional operation is performed; if $\overline{CC}$ is HIGH, a Fetch PC is performed.

Output Buffers

The Address outputs (Y_0-Y_3) are three-state drivers which may be disabled either under Instruction control or by a HIGH on the Output Enable input ($\overline{OE}$). Disabling the Y outputs does not affect the execution of instructions inside the Am2930.

Instruction Enable

When HIGH, the Instruction Enable input ($\overline{IEN}$) forces PC and SP into the hold mode and disables the write circuitry to the RAM. The auxiliary register (R) is under control of the $\overline{RE}$ input when $\overline{IEN}$ is HIGH, independent of the state of the Instruction inputs. The $\overline{IEN}$ input does not affect the combinatorial data paths or Y outputs in the Am2930. The data paths are selected by the Instruction and $\overline{CC}$ inputs and are not affected by $\overline{IEN}$.

TABLE I — Am2930 INSTRUCTION SET

Instruction Number	I_4	I_3	I_2	I_1	I_0	$\overline{CC}$	$\overline{IEN}$	Instruction	Y_0-Y_3	Next State (after CP ⎍) (Note 3) PC	R $\overline{RE}$ = L	R $\overline{RE}$ = H	RAM	SP
	X	X	X	X	X	X	H	Instruction Disable	Note 1	—	D	—	—	—
0	L	L	L	L	L	X	L	RESET	"0"	"0"+C_i	D	—	—	Reset
1	L	L	L	L	H	X	L	FETCH PC	PC	PC+C_i	D	—	—	—
2	L	L	L	H	L	X	L	FETCH R	R	PC+C_i	D	—	—	—
3	L	L	L	H	H	X	L	FETCH D	D	PC+C_i	D	—	—	—
4	L	L	H	L	L	X	L	FETCH R+D	R+D+C_n	PC+C_i	D	—	—	—
5	L	L	H	L	H	X	L	FETCH PC+D	PC+D+C_n	PC+C_i	D	—	—	—
6	L	L	H	H	L	X	L	FETCH PC+R	PC+R+C_n	PC+C_i	D	—	—	—
7	L	L	H	H	H	X	L	FETCH S+D	S+D+C_n	PC+C_i	D	—	—	—
8	L	H	L	L	L	X	L	FETCH PC → R	PC	PC+C_i	PC	PC	—	—
9	L	H	L	L	H	X	L	FETCH R+D → R	R+D+C_n	PC+C_i	R+D+C_n	R+D+C_n	—	—
10	L	H	L	H	L	X	L	LOAD R	PC	PC+C_i	D	D	—	—
11	L	H	L	H	H	X	L	PUSH PC	PC	PC+C_i	D	—	PC → Loc SP+1	SP+1
12	L	H	H	L	L	X	L	PUSH D	PC	PC+C_i	D	—	D → Loc SP+1	SP+1
13	L	H	H	L	H	X	L	POP S	S	PC+C_i	D	—	—	SP−1
14	L	H	H	H	L	X	L	POP PC	PC	PC+C_i	D	—	—	SP−1
15	L	H	H	H	H	X	L	HOLD	PC	—	D	—	—	
16-31	H	X	X	X	X	H	L	FAIL COND'L TEST (FETCH PC)	PC	PC+C_i	D	—	—	—
16	H	L	L	L	L	L	L	JUMP R	R	R+C_i	D	—	—	—
17	H	L	L	L	H	L	L	JUMP D	D	D+C_i	D	—	—	—
18	H	L	L	H	L	L	L	JUMP "0"	"0"	"0"+C_i	D	—	—	—
19	H	L	L	H	H	L	L	JUMP R+D	R+D+C_n	R+D+C_n+C_i	D	—	—	—
20	H	L	H	L	L	L	L	JUMP PC+D	PC+D+C_n	PC+D+C_n+C_i	D	—	—	—
21	H	L	H	L	H	L	L	JUMP PC+R	PC+R+C_n	PC+R+C_n+C_i	D	—	—	—
22	H	L	H	H	L	L	L	JSB R	R	R+C_i	D	—	PC → Loc SP+1	SP+1
23	H	L	H	H	H	L	L	JSB D	D	D+C_i	D	—	PC → Loc SP+1	SP+1
24	H	H	L	L	L	L	L	JSB "0"	"0"	"0"+C_i	D	—	PC → Loc SP+1	SP+1
25	H	H	L	L	H	L	L	JSB R+D	R+D+C_n	R+D+C_n+C_i	D	—	PC → Loc SP+1	SP+1
26	H	H	L	H	L	L	L	JSB PC+D	PC+D+C_n	PC+D+C_n+C_i	D	—	PC → Loc SP+1	SP+1
27	H	H	L	H	H	L	L	JSB PC+R	PC+R+C_n	PC+R+C_n+C_i	D	—	PC → Loc SP+1	SP+1
28	H	H	H	L	L	L	L	RETURN S	S	S+C_i	D	—	—	SP−1
29	H	H	H	L	H	L	L	RETURN S+D	S+D+C_n	S+D+C_n+C_i	D	—	—	SP−1
30	H	H	H	H	L	L	L	HOLD	PC	—	D	—	—	—
31	H	H	H	H	H	L	L	SUSPEND	Z (Note 2)	—	D	—	—	—

PC — Program Counter SP — Stack Pointer
R — Auxiliary Register D — Direct Inputs

Notes: 1. When $\overline{IEN}$ is HIGH, the Y_0-Y_3 outputs contain the same data as when $\overline{IEN}$ is LOW, as determined by I_0-I_4 and $\overline{CC}$.
2. Z = High impedance state (outputs "OFF").
3. — = No change

Am2930 INSTRUCTION SET

The Am2930 Instruction set can be divided into five types of instructions. These are:

- Unconditional Fetches
- Conditional Jumps
- Conditional Jumps-to-Subroutine
- Conditional Returns-from-Subroutine
- Miscellaneous Instructions

The following paragraphs describe each of these types in detail.

Unconditional Fetches

As can be seen from Table 1, there are nine unconditional Fetch instructions (Instructions 1-9). Under control of the Instruction inputs, the desired function is placed at the Y outputs. For all Fetch instructions, PC is incremented if C_i of the least significant device is HIGH. For Instructions 1 through 7, the auxiliary register is under control of the RE input. For Instructions 8 and 9, R is loaded with PC and R + D, respectively. The RAM and Stack Pointer are not changed during a Fetch instruction.

Conditional Jumps

There are six conditional Jump instructions (Instructions 16 through 21). Under control of the Instruction inputs, the desired function is placed at the Y outputs. Additionally, the desired function is incremented if C_i of the least significant device is HIGH and loaded into PC. During these instructions, R is controlled by $\overline{RE}$. The RAM and Stack Pointer are not changed during these instructions. The above operations are performed if the $\overline{CC}$ input is LOW; if $\overline{CC}$ is HIGH, a Fetch PC operation is performed.

Conditional Jumps-to-Subroutine

There are six conditional Jump-to-Subroutine instructions (Instructions 22 through 27). Under control of the Instruction inputs, the desired function is placed on the Y outputs. On the rising edge of the clock the data on the Y outputs is incremented and loaded into PC, PC is loaded into the RAM at location SP+1; and SP is incremented.

As with Conditional Jump Instructions, R is controlled by $\overline{RE}$ and whether the Jump-to-Subroutine or Fetch PC is performed depends upon the state of the $\overline{CC}$ input.

Conditional Returns-from-Subroutine

There are two conditional Return-from-Subroutine instructions (Instructions 28 and 29). Under control of the instruction inputs, either S or S+D is placed at the Y outputs. Additionally, the selected function is incremented and loaded into PC and SP is decremented at the end of the cycle (on the rising edge of the clock).

As with the Condition Jump and Jump-to-Subroutine Instructions, R is controlled by $\overline{RE}$ and whether the Return-from-Subroutine or Fetch PC is performed depends upon the state of the $\overline{CC}$ input.

Miscellaneous Instructions

Each of the nine miscellaneous instructions is described individually.

Reset (Instruction 0)

The Reset instruction forces the Y outputs to zero, loads either zero or one into PC, depending upon the C_i input of the least significant device, and resets SP. The RAM is unchanged and R is controlled by $\overline{RE}$.

Load R (Instruction 10)

This instruction loads the data on the D inputs into R. PC is either incremented or held depending upon C_i of the least significant device. The SP and RAM are not changed.

Push PC (Instruction 11)

This instruction is the same as Fetch PC except that PC is loaded into RAM and SP is incremented at the end of the cycle; i.e., the current PC is Pushed onto the stack.

Push D (Instruction 12)

This instruction is the same as Fetch PC except that D is loaded into the RAM and SP is incremented at the end of the cycle; i.e., external data is Pushed onto the stack.

Pop S (Instruction 13)

This instruction places the Top of the Stack (S) at the Y outputs and decrements SP at the end of the cycle. The PC is incremented if the C_i input of the least significant device is HIGH. R is controlled by $\overline{RE}$.

Pop PC (Instruction 14)

This instruction is the same as Fetch PC except SP is decremented at the end of the cycle, causing the data at the top of the stack to be lost.

Hold (Instruction 15)

This instruction places PC at the Y outputs and inhibits any change in PC, SP, and RAM. R is controlled by $\overline{RE}$.

Conditional Hold (Instruction 30)

This instruction is the same as Hold except $\overline{CC}$ must be LOW. If $\overline{CC}$ is HIGH, the Fetch PC instruction is performed.

Suspend (Instruction 31)

The Suspend instruction is the same as th Conditional Hold instruction except the Y outputs are forced into the high-impedance state if $\overline{CC}$ is LOW.

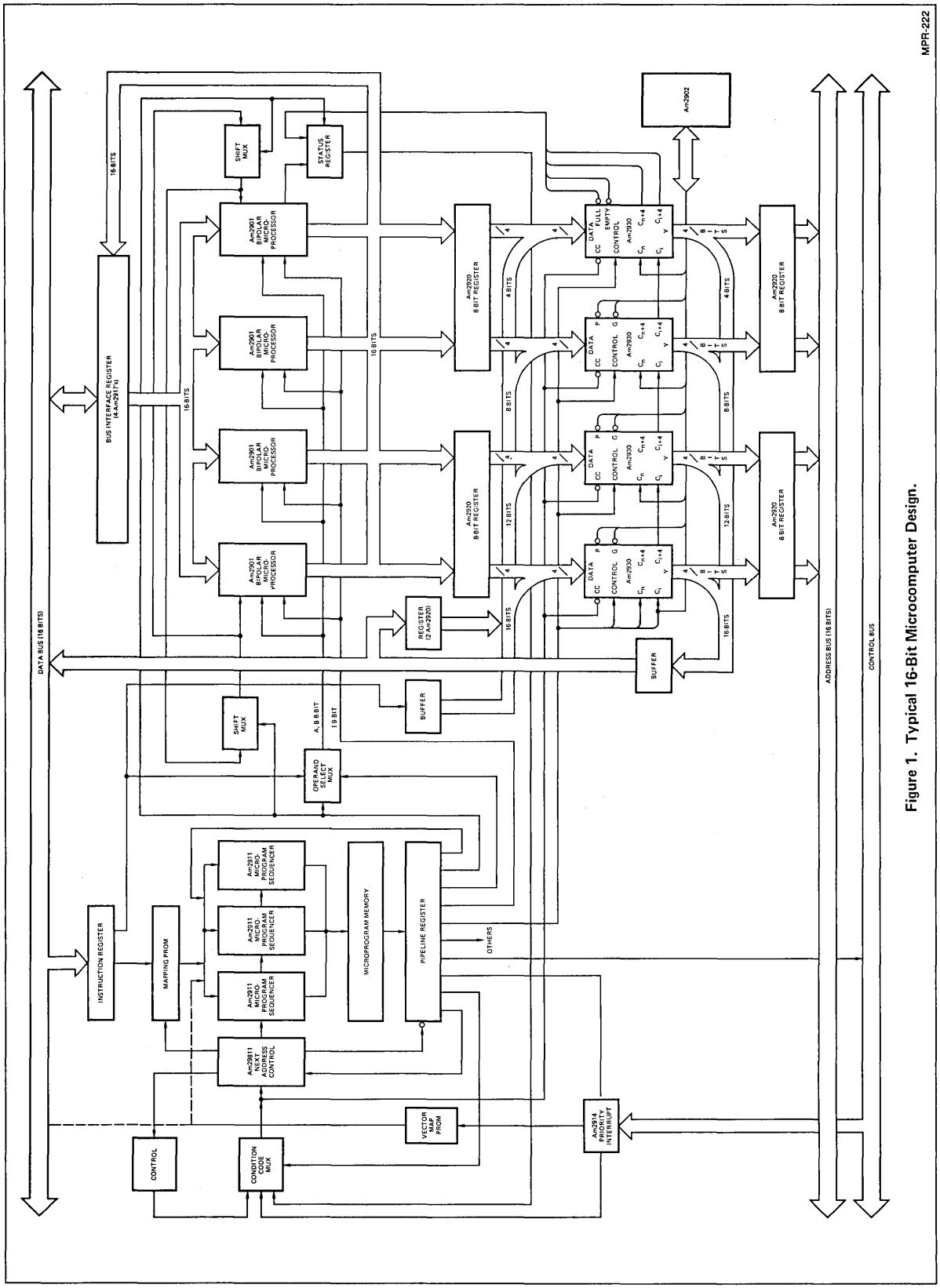


Figure 1. Typical 16-Bit Microcomputer Design.

APPLICATIONS

The Am2930 is shown in a typical 16-bit, 2900 Microcomputer design in Figure 1.

The Direct inputs (D) of the Am2930 are derived from one of three sources: the Instruction Register, the Data Bus via a 16-bit register (two Am2920 8-bit Registers), and the output of the Am2901's via a 16-bit register.

The Address outputs (Y) of the Am2930 are loaded into a 16-bit Memory Address Register (MAR). Although the MAR is shown as part of the CPU, in some applications it may be part of the memory.

An Am2902 High-Speed Lookahead Carry Generator is utilized to provide high-speed relative and indexed addressing. In slower systems, the C_{n+4} output can be wired to the next higher C_n input to provide ripple block arithmetic.

The Condition Code input ($\overline{CC}$) is derived from the same condition code multiplexer which generates the condition code input for the microprogram sequencer.

The control inputs of the Am2930 (I_{0-4}, $\overline{IEN}$, $\overline{RE}$, $\overline{OE}$, and C_i and C_n of the least significant device) are shown originating at the Pipeline Register. Although it is not shown in Figure 1, it is possible to share the Pipeline Register outputs which go to these pins with another device. This can be accomplished if both the Am2930 and the other device do not operate on the same microcycle. Forcing the $\overline{IEN}$ input HIGH inhibits any changes in the Am2930 internal registers, independent of the state of these seven inputs. This allows the Am2930 to be placed in a hold mode while the other device is using the same Pipeline Register outputs as control signals.

PIN DEFINITIONS

I_{0-4} The five Instruction control lines to the Am2930, used to establish data paths and enable internal registers.

$\overline{IEN}$ The Instruction Enable Input, used to enable and disable internal registers. When $\overline{IEN}$ is LOW, all internal registers are under control of the Instruction inputs. When $\overline{IEN}$ is HIGH, all internal registers except R are inhibited from changing state. R is controlled by the $\overline{RE}$ input. The $\overline{IEN}$ input does not affect the combinatorial data paths and the outputs established by the Instruction inputs.

$\overline{CC}$ The Condition Code input determines whether or not a conditional instruction (Instructions 16-31) is performed. If $\overline{CC}$ is LOW, the conditional instruction is executed. If $\overline{CC}$ is HIGH, Fetch PC (Instruction 1) is executed. The $\overline{CC}$ input may be either HIGH or LOW for unconditional instructions (Instructions 0-15).

$\overline{RE}$ The Register Enable input for the Auxiliary Register (R). A LOW on $\overline{RE}$ causes the Auxiliary Register (R) to be loaded from the D inputs unless Instruction 8 or 9 is being executed and $\overline{IEN}$ is LOW.

C_n The carry-in to the Full Adder.

C_{n+4} The carry-out of the Full Adder.

$\overline{P}$, $\overline{G}$ The carry generate and propagate outputs of the Full Adder.

C_i The carry-in to the program counter incrementer.

C_{i+4} The carry-out of the program counter incrementer.

Y_{0-3} The four address outputs of the Am2930. These are three-state output lines. When enabled, they display the outputs of the Full Adder.

$\overline{OE}$ Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high-impedance); when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).

D_{0-3} The four Direct inputs which are used as inputs to the Auxiliary Register, the RAM, and the Full Adder, under instruction control.

$\overline{Empty}$ The Empty output is LOW when the Stack is empty.

$\overline{Full}$ The Full output is LOW when the LIFO stack is full — during and after the 17th push operation.

CP The clock input to the Am2930. All internal registers (R, SP, PC) and the RAM are updated on the LOW-to-HIGH transition of the clock input.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

Part Number	Temperature	V_{CC}
Am2930PC, DC	T_A = 0°C to +70°C	4.75V to 5.25V
Am2930DM, FM	T_C = −55°C to +125°C	4.50V to 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IL} or V_{IH}	Y_0, Y_1, Y_2, Y_3 $\overline{G}$, C_{n+4}, C_{i+4}	I_{OH} = −1.6mA	2.4			Volts
			$\overline{P}$, $\overline{FULL}$, $\overline{EMPTY}$	I_{OH} = −1.2mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN. V_{IN} = V_{IL} or V_{IH}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			$\overline{G}$, C_{n+4} C_{i+4}	I_{OL} = 16mA			0.5	
			$\overline{P}$, $\overline{FULL}$, $\overline{EMPTY}$	I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level (Note 4)				2.0			Volts
V_{IL}	Input LOW Level (Note 4)						0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V	D_{0-3}				−.360	mA
			I_{0-4}, $\overline{RE}$, $\overline{IEN}$, CP, $\overline{OE}$				−.702	
			$\overline{CC}$				−.657	
			C_i				−2.31	
			C_n				−3.25	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V	D_{0-3}				20	μA
			I_{0-4}, $\overline{RE}$, $\overline{IEN}$, CP, $\overline{OE}$				40	
			$\overline{CC}$				50	
			C_i				90	
			C_n				250	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.			−30		−85	mA
I_{OZL}	Output OFF Current	V_{CC} = MAX., $\overline{OE}$ = 2.4V	V_{OUT} = 0.5V				−50	μA
I_{OZH}			V_{OUT} = 2.4V				50	
I_{CC}	Power Supply Current	V_{CC} = 5.0V	T_A = 25°C			118		mA
		V_{CC} = MAX.	T_C = −55°C to +125°C					
			T_C = +125°C					
			T_A = 0°C to +70°C					
			T_A = 70°C					

Notes: 1.For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Durationof the short circuit test should not exceed one second.
4. These input levels provide no guaranteed noise immunity and should only be tested in a static-, noise-free environment.

SWITCHING CHARACTERISTICS (Room Temperature Performance)

Tables I, II, and III define the timing characteristics of the Am2930 at 25°C and 5.0V. The tables divide the parameters into three types: clock characteristics, combinational delays from inputs to outputs, and set-up and hold times relative to the clock pulse. Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level.

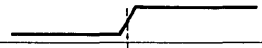
TABLE I
Clock Characteristics

Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns

TABLE II
Combinational Propagation Delays, All in ns.
Outputs fully loaded. C_L = 50pF (except output disable tests)

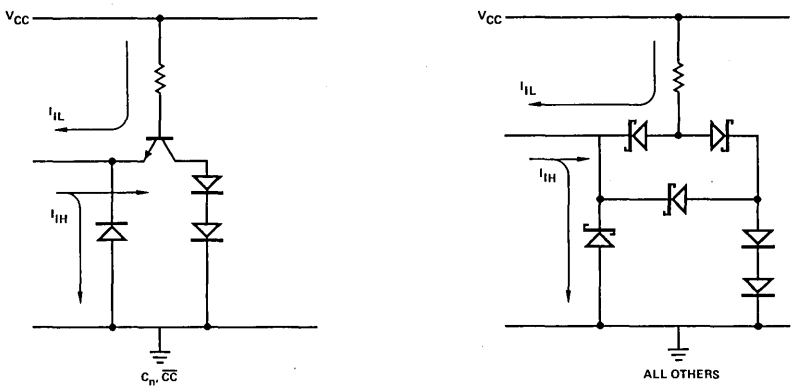
From Input \ To Output	TYPICAL, 5.0V, 25°C							MAXIMUM, 5.0V, 25°C						
	Y	$\overline{G}$, $\overline{P}$	C_{n+4}	C_{i+4} I_4 = L	C_{i+4} I_4 = H	$\overline{Full}$	$\overline{Empty}$	Y	$\overline{G}$, $\overline{P}$	C_{n+4}	C_{i+4} I_4 = L	C_{i+4} I_4 = H	$\overline{Full}$	$\overline{Empty}$
I_{4-0}	60	50	55	60	60	45	–							
$\overline{CC}$	40	35	40	–	60	30	–							
C_n	25	–	18	–	35	–	–							
C_i	–	–	–	12	12	–	–							
CP	48	35	40	40	65	30	30							
D	35	25	30	–	40	–	–							
$\overline{I_{EN}}$	–	–	–	35	40	30								

TABLE III
Set-up and Hold Times. All in ns.
All relative to clock LOW-to-HIGH transition.

Input	CP:  Set-up Time	Hold Time
I_{4-0}	75	0
$\overline{CC}$	60	0
$\overline{I_{EN}}$	65	0
C_n	32	0
C_i	18	0
D → PC	45	0
D → R or Stack	18	3
$\overline{RE}$	18	3

OUTPUT CIRCUIT CURRENT INTERFACE

DRIVEN INPUTS



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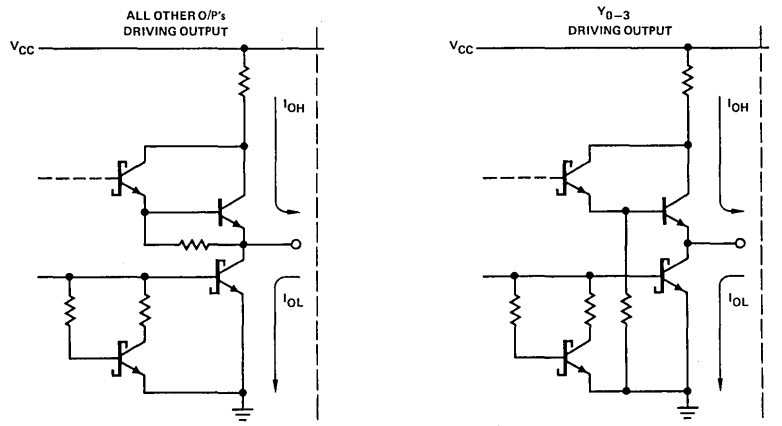
Note; C_i input is connected to both configurations in parallel.

DRIVING OUTPUTS



Note; Actual current flow direction shown.

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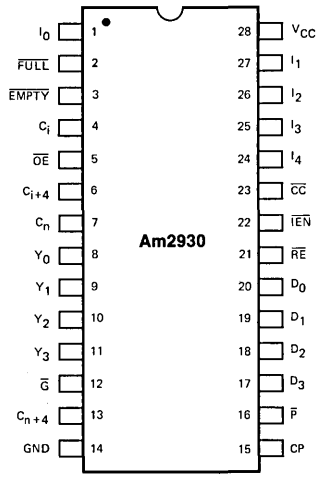
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2930PC	P-28	C	C-1
AM2930DC	D-28	C	C-1
AM2930DC-B	D-28	C	B-1
AM2930DM	D-28	M	C-3
AM2930DM-B	D-28	M	B-3
AM2930FM	F-28	M	C-3
AM2930FM-B	F-28	M	B-3
AM2930XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2930XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am2940

DMA Address Generator

Advance Information

DISTINCTIVE CHARACTERISTICS

- DMA Address Generation
  Generates memory address, word count and DONE signal for DMA transfer operation.
- Expandable Eight-bit Slice
  Any number of Am2940's can be cascaded to form larger memory addresses – three devices address 16 megawords.
- Repeat Data Transfer Capability
  Initial memory address and word count are saved so that the data transfer can be repeated.
- Programmable Control Modes
  Provides four types of DMA transfer control plus memory address increment/decrement.
- High Speed, Bipolar LSI
  Advanced Low-Power Schottky TTL technology provides typical CLOCK to DONE propagation delay of 40ns and 24mA output current sink capability.
- Microprogrammable
  Executes 8 different instructions.

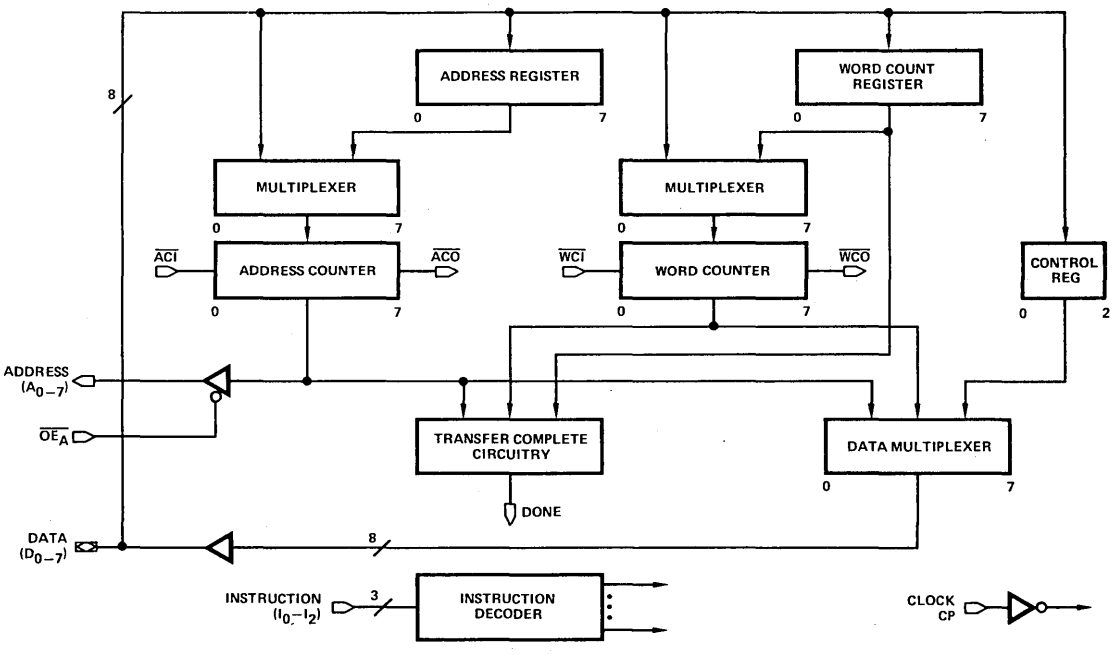
GENERAL DESCRIPTION

The Am2940, a 28-pin member of Advanced Micro Devices Am2900 family of Low-Power Schottky bipolar LSI chips, is a high-speed, cascadable, eight-bit wide Direct Memory Access Address Generator slice. Any number of Am2940's can be cascaded to form larger addresses.

The primary function of the device is to generate sequential memory addresses for use in the sequential transfer of data to or from a memory. It also maintains a data word count and generates a DONE signal when a programmable terminal count has been reached. The device is designed for use in peripheral controllers with DMA capability or in any other system which transfers data to or from sequential locations of a memory.

The Am2940 can be programmed to increment or decrement the memory address in any of four control modes, and executes eight different instructions. The initial address and word count are saved internally by the Am2940 so that they can be restored later in order to repeat the data transfer operation.

BLOCK DIAGRAM



Am2940 DMA Address Generator

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Am2940 ARCHITECTURE

As shown in the Block Diagram, the Am2940 consists of the following:

- A three-bit Control Register.
- An eight-bit Address Counter with input multiplexer.
- An eight-bit Address Register.
- An eight-bit Word Counter with input multiplexer.
- An eight-bit Word Count Register.
- Transfer complete circuitry.
- An eight-bit wide data multiplexer with three-state output buffers.
- Three-state address output buffers with external output enable control.
- An instruction decoder.

Control Register

Under instruction control, the Control Register can be loaded or read from the bidirectional DATA lines D_0-D_7. Control Register bits 0 and 1 determine the Am2940 Control Mode, and bit 2 determines whether the Address Counter increments or decrements. Figure 1 defines the Control Register format.

Address Counter

The Address Counter, which provides the current memory address, is an eight-bit, binary, up/down counter with full look-ahead carry generation. The Address Carry input ($\overline{ACI}$) and Address Carry Output ($\overline{ACO}$) allow cascading to accommodate larger addresses. Under instruction control, the Address Counter can be enabled, disabled, and loaded from the DATA inputs, D_0-D_7, or the Address Register. When enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments/decrements on the LOW to HIGH transition of the CLOCK input, CP. The Address Counter output can be enabled onto the three-state ADDRESS outputs A_0-A_7 under control of the Output Enable input, $\overline{OE}_A$.

Address Register

The eight-bit Address Register saves the initial address so that it can be restored later in order to repeat a transfer operation. When the LOAD ADDRESS instruction is executed, the Address Register and Address Counter are simultaneously loaded from the DATA inputs, D_0-D_7.

Word Counter and Word Count Register

The Word Counter and Word Count Register, which maintain and save a word count, are similar in structure and operation to the Address Counter and Address Register, with the exception that the Word Counter increments in Control Modes 1 and 3, decrements in Control Mode 0, and is disabled in Control Mode 2. The LOAD WORD COUNT instruction simultaneously loads the Word Counter and Word Count Register.

Transfer Complete Circuitry

The Transfer Complete Circuitry is a combinational logic network which detects the completion of the data transfer operation in three Control Modes and generates the DONE output signal. The DONE signal is a open-collector output, which can be dot-anded between chips.

Data Multiplexer

The Data Multiplexer is an eight-bit wide, 3-input multiplexer which allows the Address Counter, Word Counter, and Control Register to be read at the DATA lines, D_0-D_7. The Data Multiplexer and three-state Data output buffers are instruction controlled.

Address Output Buffers

The three-state Address Output Buffers allow the Address Counter output to be enabled onto the ADDRESS lines, A_0-A_7, under external control. When the Output Enable input, $\overline{OE}_A$, is LOW, the Address output buffers are enabled; when $\overline{OE}_A$ is HIGH, the ADDRESS lines are in the high-impedance state. The address and Data Output Buffers can sink 24mA output current over the commercial operating range.

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the INSTRUCTION inputs, I_0-I_2 and Control Register bits 0 and 1.

Clock

The CLOCK input, CP is used to clock the Address Register, Address Counter, Word Count Register, Word Counter, and Control Register, all on the LOW to HIGH transition of the CP signal.

Control Register

CR_2	CR_1	CR_0

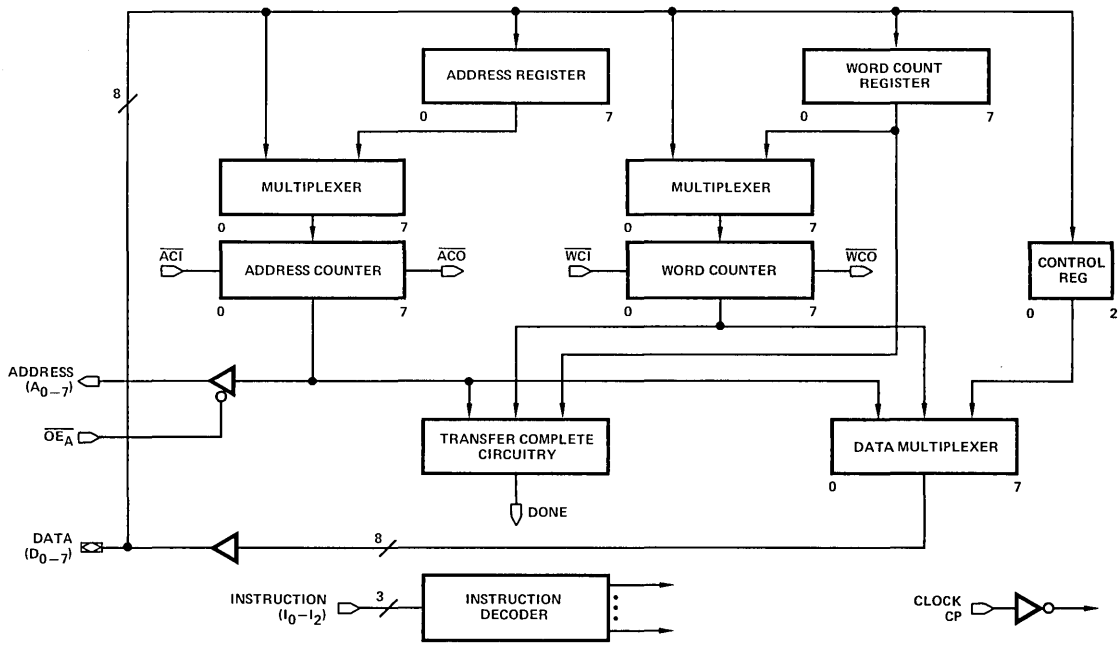
CR_1	CR_0	Control Mode Number	Control Mode Type	Word Counter	Done Output Signal
L	L	0	Word Count Equals One	Decrement	HIGH when Word Counter = 1
L	H	1	Word Count Compare	Increment	HIGH when Word Counter +1 equals Word Count Register
H	L	2	Address Compare	Hold	HIGH when Word Counter = Address Counter
H	H	3	Word Counter Carry out	Increment	Always LOW.

CR_2	Address Counter
L	Increment
H	Decrement

H = HIGH
L = LOW

Figure 1. Control Register Format Definition.

BLOCK DIAGRAM



Am2940 DMA Address Generator

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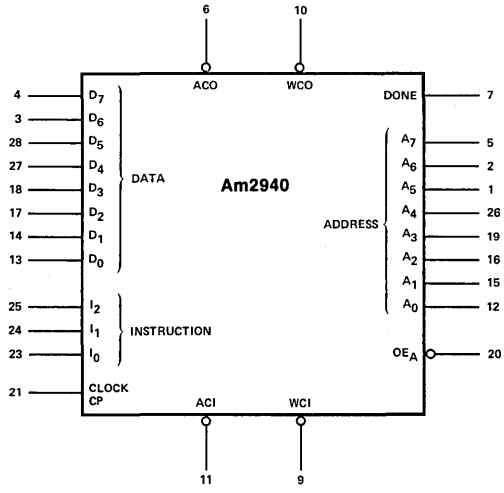
LOGIC SYMBOL



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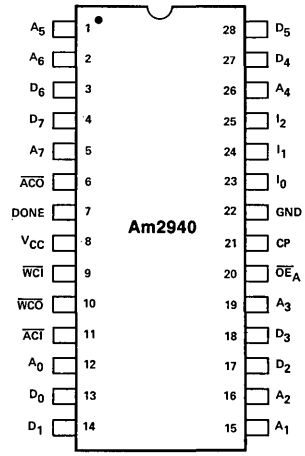
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

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Am2940 CONTROL MODES

Control Mode 0 — Word Count Equals One Mode

In this mode, the number of data words to be transferred is initially loaded into the Word Counter and Word Count Register. When the Word Counter is enabled and the Word Counter Carry-in, $\overline{WCI}$, is LOW, the Word Counter decrements on the LOW to HIGH transition of the CLOCK input, CP. The DONE signal is generated during the last word transfer, i.e. when the Word Counter equals one.

Control Mode 1 — Word Count Compare Mode

Initially, the number of data words to be transferred is loaded into the Word Count Register and the Word Counter is cleared. When the Word Counter is enabled and the $\overline{WCI}$ input is LOW, the Word Counter increments on the LOW to HIGH transition of the CLOCK input, CP. In this mode, the Word Counter always indicates the number of data words that have been transferred. The Transfer Complete Circuitry compares the Word Counter with the Word Count Register and generates the DONE signal during the last word transfer, i.e. when the Word Counter plus one equals the Word Count Register.

Control Mode 2 — Address Compare Mode

In this mode, only an initial and final memory address need be specified. The initial Memory Address is loaded into the Address Register and Address Counter and the final memory address is loaded into the Word Count Register and Word Counter. The Word Counter is always disabled in this mode and serves as a holding register for the final memory address. When the Address Counter is enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments or decrements (depending on Control Register bit 2) on the LOW to HIGH transition of the CLOCK input, CP. The Transfer Complete Circuitry compares the Address Counter with the Word Counter and generates the DONE signal during the last word transfer, i.e. when the Address Counter equals the Word Counter.

Control Mode 3 — Word Counter Carry Out Mode

For this mode of operation, the user can load the Word Count Register and Word Counter with the two's complement of the number of data words to be transferred. When the Word Counter is enabled and the $\overline{WCI}$ input is LOW, the Word Counter increments on the LOW to HIGH transition of the CLOCK input, CP. A Word Counter Carry Out signal, $\overline{WCO}$, indicates the last data word is being transferred. The DONE signal is not required in this mode and, therefore, is always LOW.

Am2940 INSTRUCTIONS

The Am2940 instruction set consists of eight instructions. Six instructions load and read the Address Counter, Word Counter and Control Register, one instruction enables the Address and Word counters, and one instruction reinitializes the Address and Word Counters. The function of the REINITIALIZE COUNTERS, LOAD WORD COUNT, and ENABLE COUNTERS instructions varies with the Control Mode being utilized. Table 1 defines the Am2940 Instructions as a function of Instruction inputs I_0-I_2 and the four Am2940 Control Modes.

The WRITE CONTROL REGISTER instruction writes DATA input D_0-D_2 into the Control Register; DATA inputs D_3-D_7 are "don't care" inputs for this instruction. The READ CONTROL REGISTER instruction gates the Control Register outputs to DATA lines, D_0-D_2. DATA lines D_3-D_7 are in the HIGH state during this instruction.

The Word Counter can be read using the READ WORD COUNTER instruction, which gates the Word Counter outputs to DATA lines D_0-D_7. The LOAD WORD COUNT instruction is Control Mode dependent. In Control Modes 0, 2, and 3, DATA inputs D_0-D_7 are written into both the Word Count Register and Word Counter. In Control Mode 1, DATA inputs D_0-D_7 are written into the Word Count Register and the Word Counter is cleared.

The READ ADDRESS COUNTER instruction gates the Address Counter outputs to DATA lines D_0-D_7, and the LOAD ADDRESS instruction writes DATA inputs D_0-D_7 into both the Address Register and Address Counter.

In Control Modes 0, 1, and 3, the ENABLE COUNTERS instruction enables both the Address and Word Counters; in Control Mode 2, the Address Counter is enabled and the Word Counter holds its contents. When enabled and the carry input is active, the counters increment on the LOW to HIGH transition of the CLOCK input, CP. Thus, with this instruction applied, counting can be controlled by the carry inputs.

The REINITIALIZE COUNTERS instruction also is Control Mode dependent. In Control Modes 0, 2, and 3, the contents of the Address Register and Word Count Register are transferred to the respective Address Counter and Word Counter; in Control Mode 1, the content of the Address Register is transferred to the Address Counter and the Word Counter is cleared. The REINITIALIZE COUNTERS instruction allows a data transfer operation to be repeated without reloading the address and word count from the DATA lines.

TABLE I. Am2940 INSTRUCTIONS

I_2 I_1 I_0	Octal Code	Function	Mnemonic	Control Mode	Word Reg.	Word Counter	Address Reg.	Address Counter	Control Register	Data D_0-D_7
L L L	0	WRITE CONTROL REGISTER	WRCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	D_0-D_2→CR	INPUT
L L H	1	READ CONTROL REGISTER	RDCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	CR→D_0-D_2 (Note 1)
L H L	2	READ WORD COUNTER	RDWC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	WC→D
L H H	3	READ ADDRESS COUNTER	RDAC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	AC→D
H L L	4	REINITIALIZE COUNTERS	REIN	0, 2, 3	HOLD	WCR→WC	HOLD	AR→AC	HOLD	Z
				1	HOLD	ZERO→WC	HOLD	AR→AC	HOLD	Z
H L H	5	LOAD ADDRESS	LDAD	0, 1, 2, 3	HOLD	HOLD	D→AR	D→AC	HOLD	INPUT
H H L	6	LOAD WORD COUNT	LDWC	0, 2, 3	D→WR	D→WC	HOLD	HOLD	HOLD	INPUT
				1	D→WR	ZERO→WC	HOLD	HOLD	HOLD	INPUT
H H H	7	ENABLE COUNTERS	ENCT	0, 1, 3	HOLD	ENABLE COUNT	HOLD	ENABLE COUNT	HOLD	Z
				2	HOLD	HOLD	HOLD	ENABLE COUNT	HOLD	Z

CR = Control Reg.
AR = Address Reg.
AC = Address Counter
WCR = Word Count Reg.
WC = Word Counter
D = Data
L = LOW
H = HIGH
Z = High Impedance

Note 1:
Data Bits D_3-D_7 are high during this instruction.

APPLICATIONS

The Am2940 is designed for use in peripheral controllers with DMA capability or in any other system which transfers data to or from sequential locations of a memory. One or more Am2940's can be used in each peripheral controller of a distributed DMA system to provide the memory address and word count required for DMA operation.

Figure 3 shows a block diagram of an example microprogrammed DMA peripheral controller. The Am2940 Microprogram Sequencer, Microprogram Memory, and the Microinstruction Register form the microprogram control portion of this peripheral controller. The Am2940 generates the memory address and maintains the word count required for DMA operation. An internal three-state bus provides the communication path between the Microinstruction Register, the Am2917 Data Tranceivers, the Am2940, the Am2901A Microprocessor, and the Device Interface Circuitry.

The Am2940 interconnections are shown in detail in Figure 4. Two Am2940's are cascaded to generate a sixteen-bit address. The Am2940 ADDRESS and DATA output current sink capability is 24mA over the commercial operating range. This allows the Am2940's to drive the System Address Bus and Internal Three-State Bus directly, thereby eliminating the need for separate bus drivers. Three-bits in the Microinstruction Register provide the Am2940 Instruction Inputs, I_0-I_2. The microprogram clock is used to clock the Am2940's and, when the ENABLE COUNTERS instruction is applied, address and word counting is controlled by the CNT bit of the Microinstruction Register.

Asynchronous interface control circuitry generates System Bus control signals and enables the Am2940 Address onto the System Address Bus at the appropriate time. The open-collector DONE outputs are dot-anded and used as a test input to the Am2910 Microprogram Sequencer.

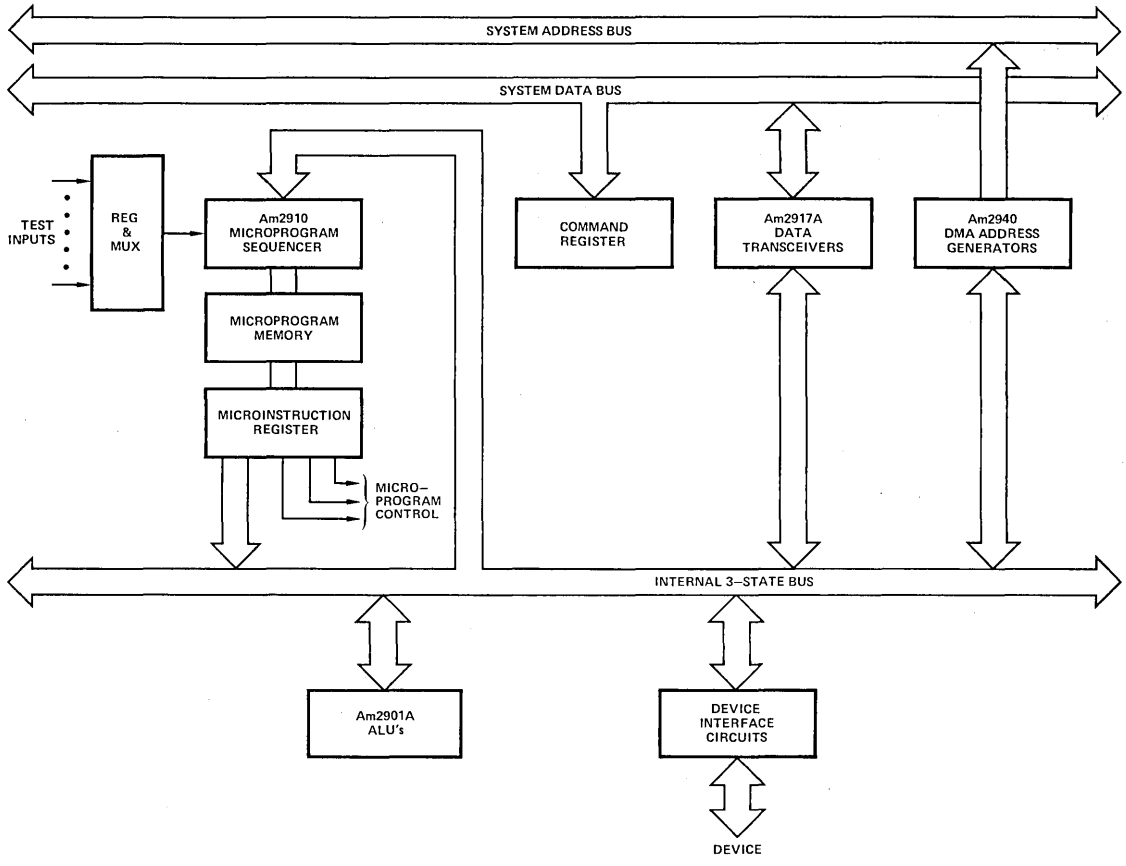

Figure 3. DMA Peripheral Controller Block Diagram.

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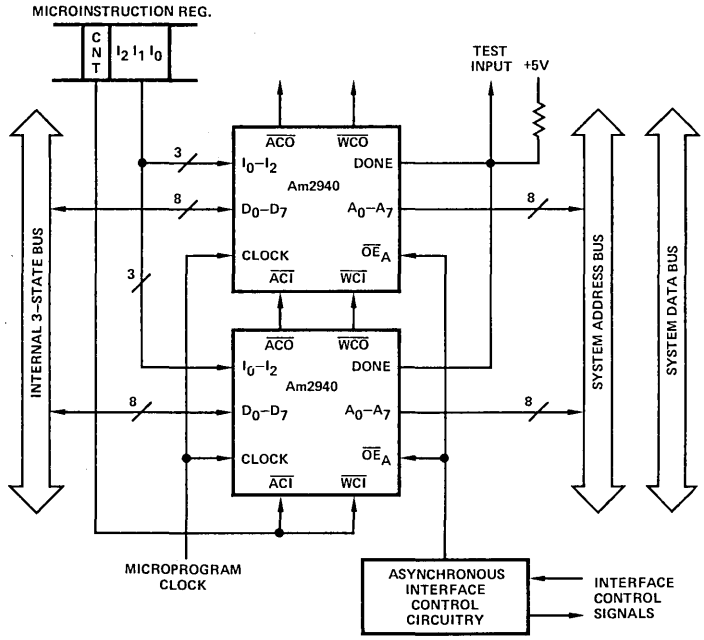

Figure 4. Am2940 Interconnections.

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ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2940PC	P-28	C	C-1
AM2940DC	D-28	C	C-1
AM2940DC-B	D-28	C	B-1
AM2940DM	D-28	M	C-3
AM2940DM-B	D-28	M	B-3
AM2940FM	F-28	M	C-3
AM2940FM-B	F-28	M	B-3
AM2940XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2940XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am2941

Programmable Timer/Counter DMA Address Generator

ADVANCED INFORMATION

DISTINCTIVE CHARACTERISTICS

- 22-pin version of Am2940 –
  Provides multiplexed Address and Data lines plus additional Instruction Input and Instruction Enable pins.
- Can be used as either DMA Address Generator or Programmable Timer Counter.
- Executes 16 instructions –
  Eight DMA instructions plus eight Timer/Counter instructions
- Provides two independent programmable 8-bit up/down counters in a 22-pin package –
  Counters can be cascaded to form single-chip 16-bit up/down counter.
- Reinitialize capability –
  Counters can be reinitialized from on-chip registers.
- Expandable eight-bit slice –
  Any number of Am2941's can be cascaded. Three devices provide a 48 bit counter.
- Programmable control modes –
  Provide four types of control.
- High speed bipolar LSI –
  Advanced Low-Power Schottky TTL technology provides typical count frequency of 25MHz and 24mA output current sink capability.

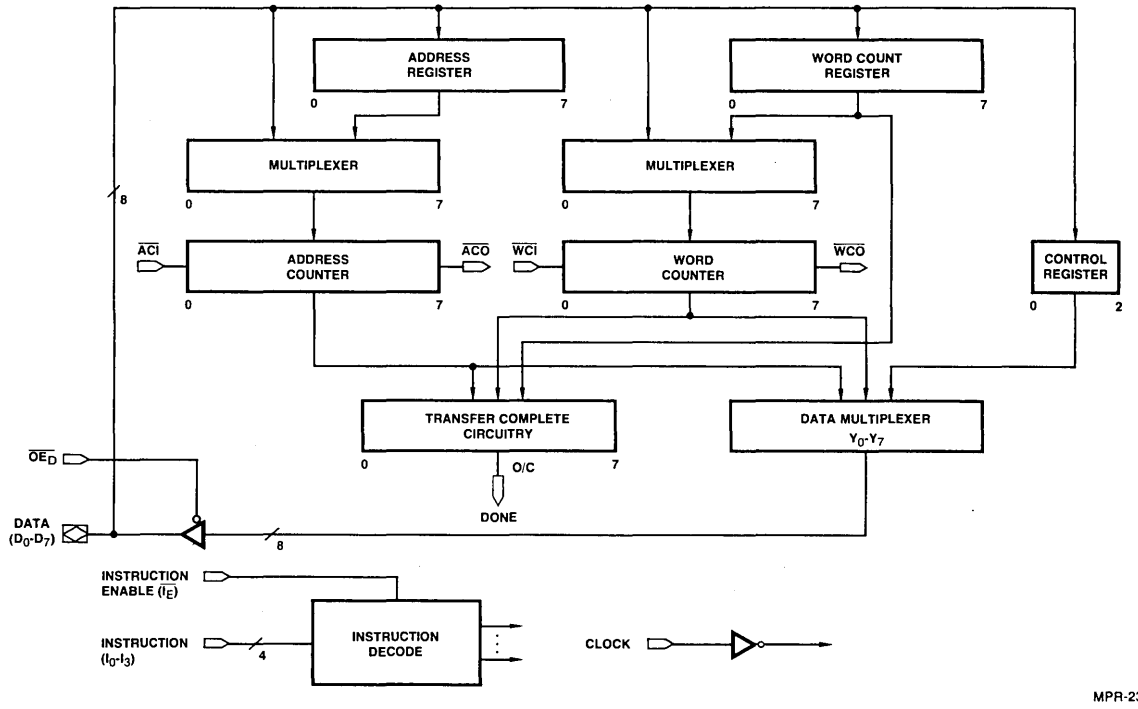
GENERAL DESCRIPTION

The Am2941, a 22-pin version of the Am2940, can be used as a high-speed DMA address Generator or Programmable Timer/Counter. It provides multiplexed Address and Data lines, for use with a common bus, and additional Instruction Input and Instruction Enable pins. The Am2941 executes 16 instructions; eight are the same as the Am2940 instructions, and eight instructions facilitate the use of the Am2941 as a Programmable Timer/Counter. The Instruction Enable input allows the sharing of the Am2941 instruction field with other devices.

When used as a Timer/Counter, the Am2941 provides two independent, programmable, eight-bit, up-down counters in a 22-pin package. The two on-chip counters can be cascaded to form a single chip, 16-bit counter. Also, any number of chips can be cascaded – for example three cascaded Am2941's form a 48-bit timer/counter.

Reinitialization instructions provide the capability to reinitialize the counters from on-chip registers. Am2941 Programmable Control Modes, identical to those of the Am2940, offer four different types of programmable control.

BLOCK DIAGRAM



Am2941 ARCHITECTURE

As shown in the Block Diagram, the Am2941 consists of the following:

- A three-bit Control Register.
- An eight-bit Address Counter with input multiplexer.
- An eight-bit Address Register:
- An eight-bit Word Counter with input mulitplexer.
- An eight-bit Word Count Register.
- Transfer complete circuitry.
- An eight-bit wide data multiplexer with three-state output buffers.
- An instruction decoder.

Control Register

Under instruction control, the Control Register can be loaded or read from the bidirectional DATA lines D_0-D_7. Control Register bits 0 and 1 determine the Am2941 Control Mode, and bit 2 determines whether the Address Counter increments or decrements. Figure 1 defines the Control Register format.

Address Counter

The Address Counter, which provides the current memory address, is an eight-bit, binary, up/down counter with full look-ahead carry generation. The Address Carry input ($\overline{ACI}$) and Address Carry Output ($\overline{ACO}$) allow cascading to accommodate larger addresses. Under instruction control, the Address Counter can be enabled, disabled, and loaded from the DATA inputs, D_0-D_7, or the Address Register. When enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments/decrements on the LOW to HIGH transition of the CLOCK input, CP.

Address Register

The eight-bit Address Register saves the initial address so that it can be restored later in order to repeat a transfer operation. When the LOAD ADDRESS instruction is executed, the Address Register and Address Counter are simultaneously loaded from the DATA inputs, D_0-D_7.

Word Counter and Word Count Register

The Word Counter and Word Count Register, which maintain and save a word count, are similar in structure and operation to the Address Counter and Address Register, with the exception that the Word Counter increments in Control Modes 1 and 3, decrements in Control Mode 0, and is disabled in Control Mode 2. The LOAD WORD COUNT instruction simultaneously loads the Word Counter and Word Count Register.

Transfer Complete Circuitry

The Transfer Complete Circuitry is a combinational logic network which detects the completion of the data transfer operation in three Control Modes and generates the DONE output signal. The DONE signal is a open-collector output, which can be dot-anded between chips.

Data Multiplexer

The Data Multiplexer is an eight-bit wide, three-input multiplexer which allows the Address Counter, Word Counter and Control Register to be read at DATA lines D_0-D_7. The Data Multiplexer output, Y_0-Y_7, is enabled onto DATA lines D_{0-7} if and only if the Output Enable input, OE_D, is LOW. (Refer to Figure 2.)

Instruction Decoder

The Instruction Decoder generates required internal control signals as a function of the INSTRUCTION inputs, I_0-I_3 Control Register bits 0 and 1, and the INSTRUCTION ENABLE input, I_E.

Clock

The CLOCK input, CP is used to clock the Address Register, Address Counter, Word Count Register, Word Counter, and Control Register, all on the LOW to HIGH transition of the CP signal.

Control Register

CR_2	CR_1	CR_0

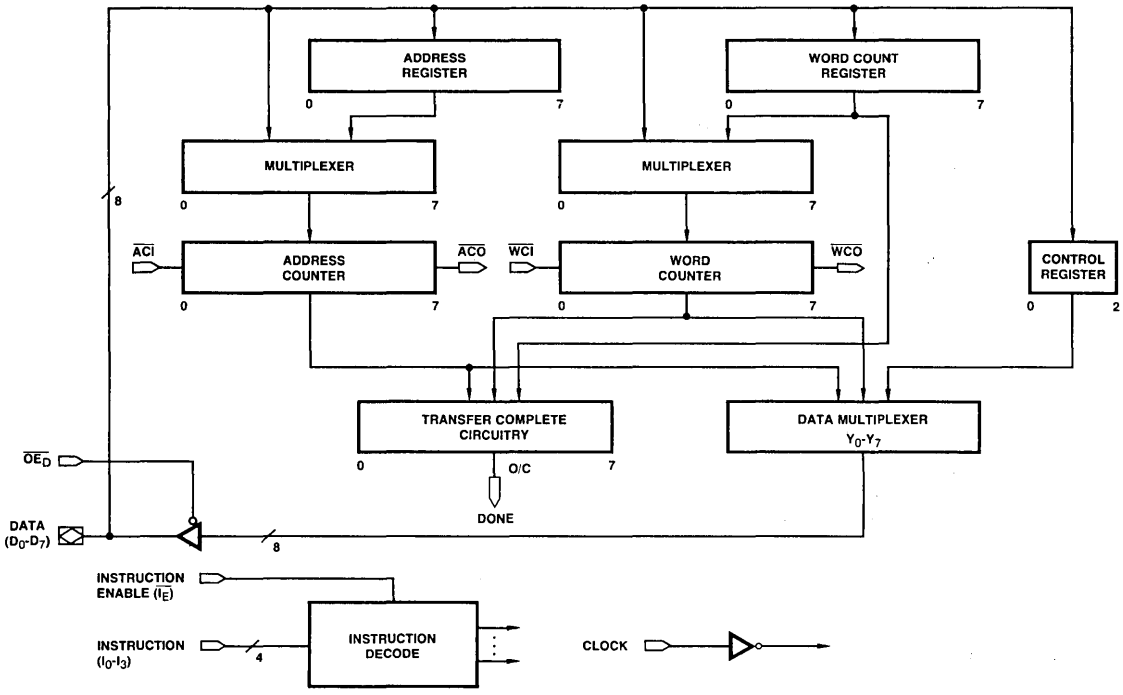
CR_1	CR_0	Control Mode Number	Control Mode Type	Word Counter	Done Output Signal
L	L	0	Word Count Equals One	Decrement	HIGH when Word Counter = 1
L	H	1	Word Count Compare	Increment	HIGH when Word Counter +1 equals Word Count Register
H	L	2	Address Compare	Hold	HIGH when Word Counter = Address Counter
H	H	3	Word Counter Carry out	Increment	Always LOW.

CR_2	Address Counter
L	Increment
H	Decrement

H = HIGH
L = LOW

Figure 1. Control Register Format Definition.

BLOCK DIAGRAM



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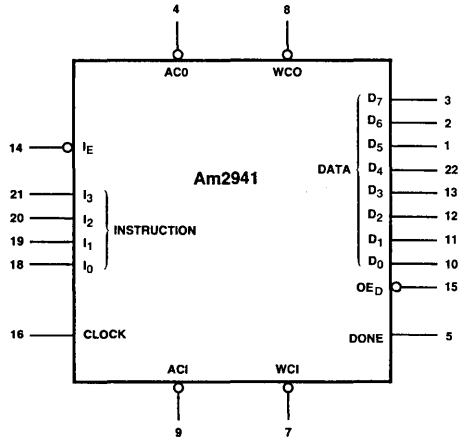
LOGIC SYMBOL



V_{CC} = Pin 6
GND = Pin 17

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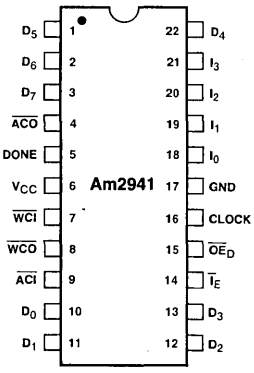
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

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Am2941 CONTROL MODES

Control Mode 0 — Word Count Equals One Mode

In this mode, the number of data words to be transferred is intially loaded into the Word Counter and Word Count Register. When the Word Counter is enabled and the Word Counter Carry-in, $\overline{WCI}$, is LOW, the Word Counter decrements on the LOW to HIGH transition of the CLOCK input, CP. The DONE signal is generated during the last word transfer, i.e. when the Word Counter equals one.

Control Mode 1 — Word Count Compare Mode

Initially, the number of data words to be transferred is loaded into the Word Count Register and the Word Counter is cleared. When the Word Counter is enabled and the $\overline{WCI}$ input is LOW, the Word Counter increments on the LOW to HIGH transition of the CLOCK input, CP. In this mode, the Word Counter always indicates the number of data words that have been transferred. The Transfer Complete Circuitry compares the Word Counter with the Word Count Register and generates the DONE signal during the last word transfer, i.e. when the Word Counter plus one equals the Word Count Register.

Control Mode 2 — Address Compare Mode

In this mode, only an initial and final memory address need to be specified. The initial Memory Address is loaded into the Address Register and Address Counter and the final memory address is loaded into the Word Count Register and Word Counter. The Word Counter is always disabled in this mode and serves as a holding register for the final memory address. When the Address Counter is enabled and the $\overline{ACI}$ input is LOW, the Address Counter increments or decrements (depending on Control Register bit 2) on the LOW to HIGH transition of the CLOCK input, CP. The Transfer Complete Circuitry compares the Address Counter with the Word Counter and generates the DONE signal during the last word transfer, i.e. when the Address Counter equals the Word Counter.

$\overline{OE_D}$	D_0-D_7
L	DATA MULTIPLEXER OUTPUT, Y_0-Y_7
H	HIGH Z

Figure 2. Data Bus Output Enable Function.

Control Mode 3 — Word Counter Carry Out Mode

For this mode of operation, the user can load the Word Count Register and Word Counter with the two's complement of the number of data words to be transferred. When the Word Counter is enabled and the $\overline{WCI}$ input is LOW, the Word Counter increments on the LOW to HIGH transition of the CLOCK input, CP. A Word Counter Carry Out signal, $\overline{WCO}$, indicates the last data word is being transferred. The DONE signal is not required in this mode and, therefore, is always LOW.

Am2941 INSTRUCTIONS

The Am2941 instruction set consists of sixteen instructions. Eight are DMA instructions and are the same as the Am2940 instructions. The remaining eight instructions are designed to facilitate the use of the Am2941 as a Programmable Timer/Counter. Figures 3 and 4 define the Am2941 Instructions.

Instructions 0-7 are DMA instructions. The WRITE CONTROL REGISTER instruction writes DATA input D_0-D_2 into the Control Register; DATA inputs D_3-D_7 are "don't care" inputs for this instruction. The READ CONTROL REGISTER instruction gates the Control Register to Data Mulitplexer outputs Y_0-Y_2. Outputs Y_3-Y_7 are HIGH during this instruction.

The Word Counter can be read using the READ WORD COUNTER instruction, which gates the Word Counter to Data Multiplexer outputs, Y_0-Y_7. The LOAD WORD COUNT instruction is Control Mode dependent. In Control Modes 0, 2, and 3,

$\overline{I_E}$	I_3	I_2	I_1	I_0	HEX CODE		
0	0	0	0	0	0	WRITE CONTROL REGISTER	DMA INSTRUCTIONS
0	0	0	0	1	1	READ CONTROL REGISTER	
0	0	0	1	0	2	READ WORD COUNTER	
0	0	0	1	1	3	READ ADDRESS COUNTER	
0	0	1	0	0	4	REINITIALIZE COUNTERS	
0	0	1	0	1	5	LOAD ADDRESS	
0	0	1	1	0	6	LOAD WORD COUNT	
0	0	1	1	1	7	ENABLE COUNTERS	
1	0	X	X	X	0-7	INSTRUCTION DISABLE	
0	1	0	0	0	8	WRITE CONTROL REGISTER, T/C	TIMER/COUNTER INSTRUCTIONS
0	1	0	0	1	9	REINITIALIZE ADDRESS COUNTER	
0	1	0	1	0	A	READ WORD COUNTER, T/C	
0	1	0	1	1	B	READ ADDRESS COUNTER, T/C	
0	1	1	0	0	C	REINITIALIZE ADDRESS & WORD COUNTERS	
0	1	1	0	1	D	LOAD ADDRESS, T/C	
0	1	1	1	0	E	LOAD WORD COUNT, T/C	
0	1	1	1	1	F	REINITIALIZE WORD COUNTER	
1	1	X	X	X	8-F	INSTRUCTION DISABLE, T/C	

0 = LOW 1 = HIGH X = DON'T CARE

Notes: 1. When I_3 is tied LOW, the Am2941 acts as a DMA circuit: When I_3 is tied HIGH, the Am2941 acts as a Timer/Counter circuit.
2. Am2941 instructions 0 through 7 are the same as Am2940 instructions.

Figure 3. Am2941 Instructions.

DATA inputs D_0-D_7 are written into both the Word Count Register and Word Counter. In Control Mode 1, DATA inputs D_0-D_7 are written into the Word Count Register and the Word Counter is cleared.

The READ ADDRESS COUNTER instruction gates the Address Counter to Data Multiplexer outputs, Y_0-Y_7, and the LOAD ADDRESS instruction writes DATA inputs D_0-D_7 into both the Address Register and Address Counter.

In Control Modes 0, 1, and 3, the ENABLE COUNTERS instruction enables both the Address and Word Counters; in Control Mode 2, the Address Counter is enabled and the Word Counter holds its contents. When enabled and the carry input is active, the counters increment on the LOW to HIGH transition of the CLOCK input, CP. Thus, with this instruction applied, counting can be controlled by the carry inputs.

The REINITIALIZE COUNTERS instruction also is Control Mode dependent. In Control Modes 0, 2, and 3, the contents of the Address Register and Word Count Register are transferred to the respective Address Counter and Word Counter; in Control Mode 1, the content of the Address Register is transferred to the Address Counter and the Word Counter is cleared. The REINITIALIZE COUNTERS instruction allows a data transfer operation to be repeated without reloading the address and word count from the DATA lines.

When $\overline{I_E}$ is HIGH, Instruction inputs, I_0-I_2, are disabled. If I_3 is LOW, the function performed is identical to that of the ENABLE COUNTERS instruction. Thus, counting can be controlled by the carry inputs with the ENABLE COUNTERS instruction applied or with Instruction Inputs I_0-I_2 disabled.

Instructions 8-F facilitate the use of the Am2941 as a Programmable Timer/Counter. They differ from instructions 0-7 in that they provide independent control of the Address Counter, Word Counter and Control Register.

The WRITE CONTROL REGISTER, T/C instruction writes DATA input D_0-D_2 into the Control Register. DATA inputs D_3-D_7 are "don't care" inputs for this instruction. The Address and Word Counters are enabled, and the Control Register contents appear at the Data Multiplexer output.

The REINITIALIZE ADDRESS COUNTER instruction allows the independent reinitialization of the Address Counter. The Word Counter is enabled and the contents of the Address Counter appear at the Data Multiplexer output.

The Word Counter can be read, using the READ WORD COUNTER, T/C instruction. Both counters are enabled when this instruction is executed.

When the READ ADDRESS COUNTER, T/C instruction is executed, both counters are enabled and the address counter contents appear at the Data Multiplexer output.

The REINITIALIZE ADDRESS and WORD COUNTERS instruction provides the capability to reinitialize both counters at the same time. The Address Counter contents appear at the Data Multiplexer output.

DATA inputs D_0-D_7 are loaded into both the Address Register and Counter when the LOAD ADDRESS, T/C instruction is executed. The Word Counter is enabled and its contents appear at the Data Multiplexer output.

The LOAD WORD COUNT, T/C instruction is identical to the LOAD WORD COUNT instruction with the exception that Address Counter is enabled.

The Word Counter can be independently reinitialized using the REINITIALIZE WORD COUNTER instruction. The Address Counter is enabled and the Word Counter contents appear at the Data Multiplexer output.

When the $\overline{I_E}$ input is HIGH, Instruction inputs, I_0-I_2, are disabled. The function performed when I_3 is HIGH is identical to that performed when I_3 is LOW, with the exception that the Word Counter contents appear at the Data Multiplexer output.

$\overline{I_E}$	$I_3I_2I_1I_0$ (Hex)	Function	Mnemonic	Control Mode	Word Reg.	Word Counter	Adr. Reg.	Adr. Counter	Control Reg.	Data Multiplexer Output
L	0	WRITE CONTROL REGISTER	WRCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	$D_{0-2} \rightarrow$ CR	FORCED HIGH
L	1	READ CONTROL REGISTER	RDCR	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	CONTROL REG.
L	2	READ WORD COUNTER	RDWC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	WORD COUNTER
L	3	READ ADDRESS COUNTER	RDAC	0, 1, 2, 3	HOLD	HOLD	HOLD	HOLD	HOLD	ADR. COUNTER
L	4	REINITIALIZE COUNTERS	REIN	0, 2, 3	HOLD	WR → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
				1	HOLD	ZERO → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
L	5	LOAD ADDRESS	LDAD	0, 1, 2, 3	HOLD	HOLD	D → AR	D → AC	HOLD	WORD COUNTER
L	6	LOAD WORD COUNT	LDWC	0, 2, 3	D → WR	D → WC	HOLD	HOLD	HOLD	FORCED HIGH
				1	D → WR	ZERO → WC	HOLD	HOLD	HOLD	FORCED HIGH
L	7	ENABLE COUNTERS	ENCT	0, 1, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	ADR. CNTR.
				2	HOLD	HOLD	HOLD	ENABLE	HOLD	ADR. CNTR.
H	0-7	INSTRUCTION DISABLE	–	0, 1, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	ADR. CNTR.
				2	HOLD	HOLD	HOLD	ENABLE	HOLD	ADR. CNTR.
L	8	WRITE CONTROL REGISTER, T/C	WCRT	0, 1, 2, 3	HOLD	ENABLE	HOLD	ENABLE	$D_{0-2} \rightarrow$ CR	CONTROL REG.
L	9	REINITIALIZE ADR. COUNTER	REAC	0, 1, 2, 3	HOLD	ENABLE	HOLD	AR → AC	HOLD	ADR. COUNTER
L	A	READ WORD COUNTER, TC	RWCT	0, 1, 2, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	WORD COUNTER
L	B	READ ADDRESS COUNTER, T/C	RACT	0, 1, 2, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	ADR. COUNTER
L	C	REINITIALIZE ADDRESS AND WORD COUNTERS	RAWC	0, 2, 3	HOLD	WR → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
				1	HOLD	ZERO → WC	HOLD	AR → AC	HOLD	ADR. CNTR.
L	D	LOAD ADDRESS, T/C	LDAT	0, 1, 2, 3	HOLD	ENABLE	D → AR	D → AC	HOLD	WORD COUNTER
L	E	LOAD WORD COUNT, T/C	LWCT	0, 2, 3	D → WR	D → WC	HOLD	ENABLE	HOLD	FORCED HIGH
				1	D → WR	ZERO → WC	HOLD	ENABLE	HOLD	FORCED HIGH
L	F	REINITIALIZE WORD COUNTER	REWC	0, 2, 3	HOLD	WR → WC	HOLD	ENABLE	HOLD	WD. CNTR.
				1	HOLD	ZERO → WC	HOLD	ENABLE	HOLD	WD. CNTR.
H	8-F	INSTRUCTION DISABLE, T/C	–	0, 1, 3	HOLD	ENABLE	HOLD	ENABLE	HOLD	WD. CNTR.
				2	HOLD	HOLD	HOLD	ENABLE	HOLD	WD. CNTR.

WR = WORD REGISTER
WC = WORD COUNTER
AR = ADDRESS REGISTER
AC = ADDRESS COUNTER
CR = CONTROL REGISTER
D = DATA

Figure 4. Am2941 Function Table

APPLICATIONS

Figure 5 shows an Am2941 used as two independent, programmable eight-bit timer/counters. In this example, an Am2910 Microprogram Sequencer provides an address to Am29775 512 x 8 Registered PROM's. The on-chip PROM output register is used as the Microinstruction Register.

The Am2941 Instruction input, I_3, is tied HIGH to select the eight Timer/Counter instructions. The $\overline{I_E}$, I_0-I_2, and $\overline{OE_D}$ inputs are provided by the microinstruction, and the D_0-D_7 data lines are connected to a common Data Bus. GATE WC and GATE AC are separate enable controls for the respective Word Counter and Address Counter. The DONE, $\overline{ACO}$ and $\overline{WCO}$ output signals indicate that a pre-programmed time or count has been reached.

Figure 6 shows an Am2941 used as a single 16-bit, programmable timer/counter. In this example, the Word Counter carry-out, $\overline{WCO}$, is connected to the Address Counter carry-in, $\overline{ACI}$, to form a single 16-bit counter which is enabled by the GATE signal.

Figure 7 shows two Am2941's cascaded to form a 32-bit programmable timer/counter. The two Word Counters form the low order 16 bits, and the two Address Counters form the high order bits. This allows the timer/counter to be loaded and read 16 bits at a time.

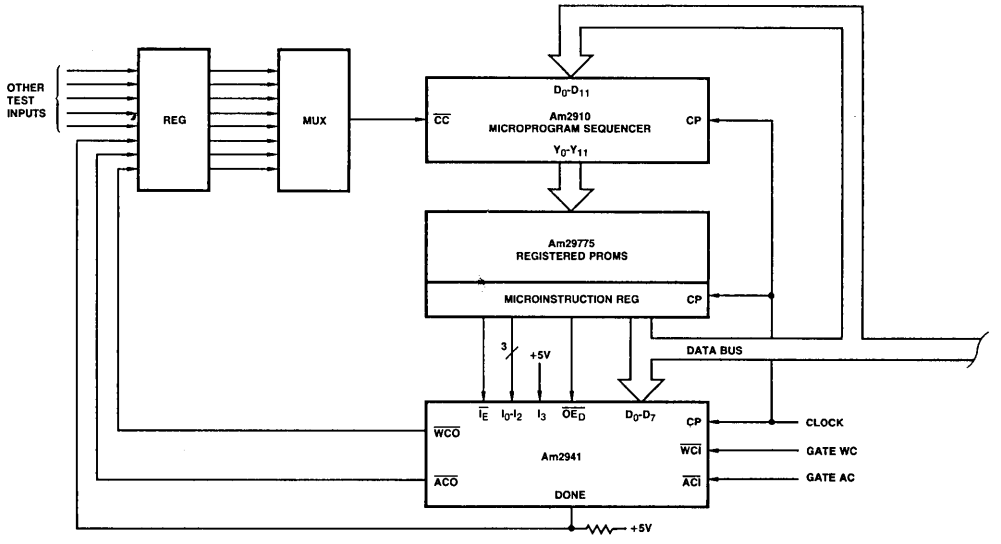

Figure 5. Two 8-Bit Programmable Counters/Timers in a 22-Pin Package

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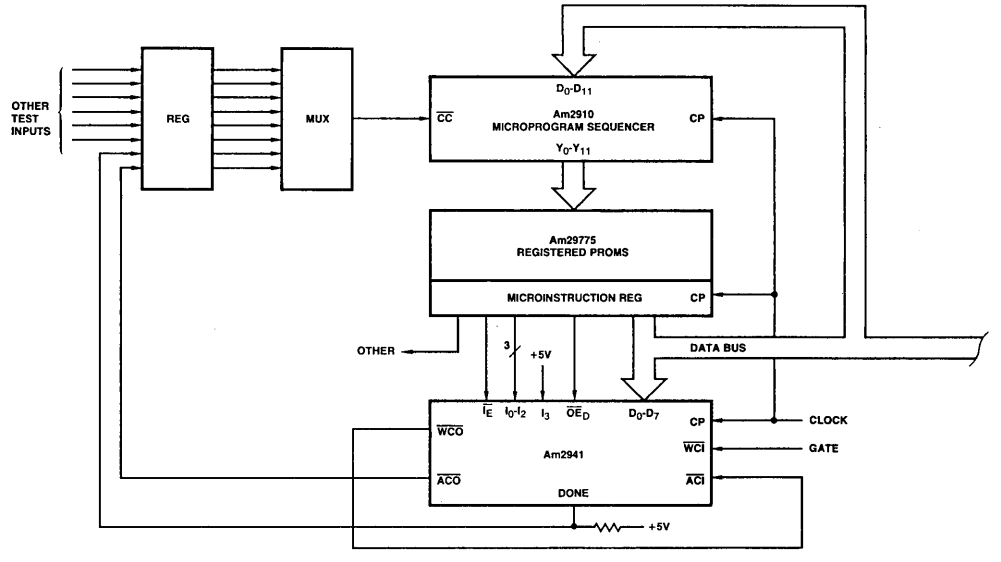


Figure 6. 16-Bit Programmable Counter/Timer Using a Single Am2941

MPR-235

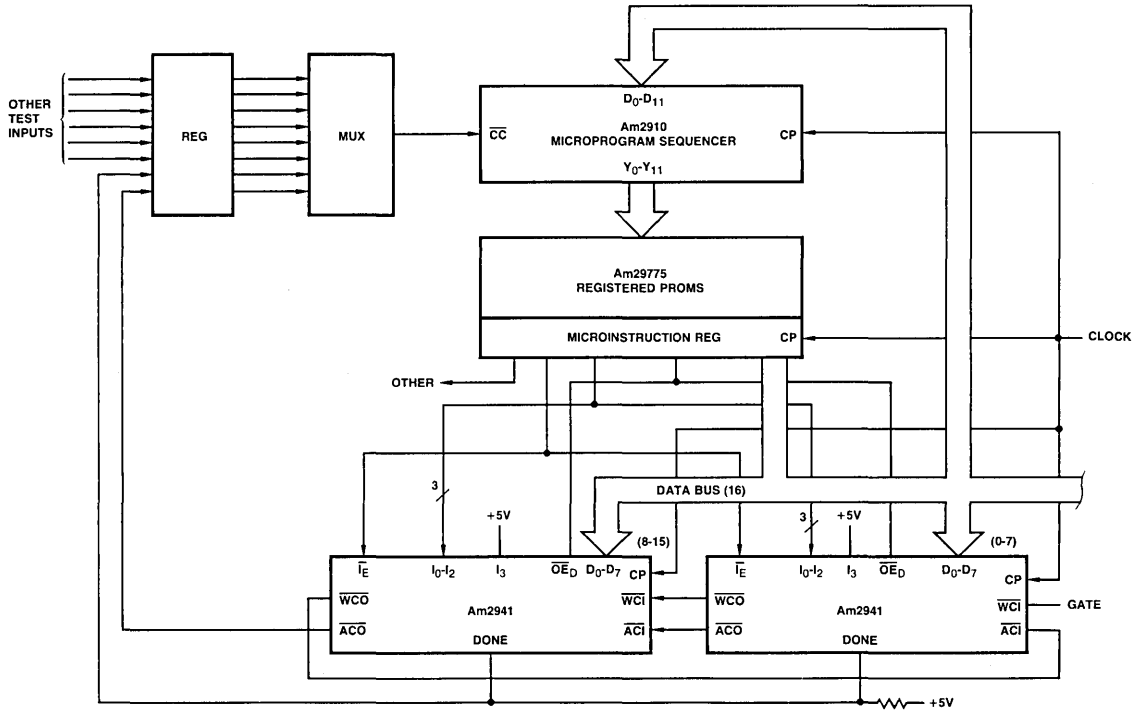


Figure 7. 32-Bit Programmable Counter/Timer Using Two Am2941's

MPR-236

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM2941PC	P-22	C	C-1
AM2941DC	D-22	C	C-1
AM2941DC-B	D-22	C	B-1
AM2941DM	D-22	M	C-3
AM2941DM-B	D-22	M	B-3
AM2941FM	F-22	M	C-3
AM2941FM-B	F-22	M	B-3
AM2941XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2941XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am2950 • Am2951

8-Bit Parallel I/O Port

ADVANCED INFORMATION

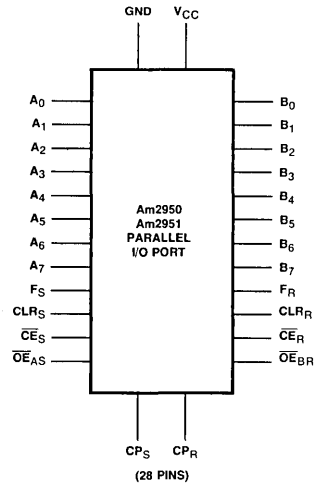
DISTINCTIVE CHARACTERISTICS

- Two Eight-Bit Registers
  Store data moving in either direction between two buses.
- On-Chip Flag Flip-Flops
  Flag sets whenever data is loaded into a register.
- Edge-Sensitive Flag Clear
  Flag Flip-Flops can be reset when data is taken by a transition on the clear line.
- Independent Clocks for each direction
- 24mA output current sink.

FUNCTIONAL DESCRIPTION

The parallel I/O port is designed as an extension of the 2900 Microprocessor bit slice family and will supply the data I/O port requirements with considerable flexibility. The device provides a temporary store for one word in each direction (two registers of eight bits each) that are interconnected to provide a bidirectional buffer for an 8-bit byte. Each register has provision for loading clock (CP_R and CP_S), a clock enable ($\overline{CE}_R$ and $\overline{CE}_S$), a tri-state output enable ($\overline{OE}_{AS}$ and $\overline{OE}_{BR}$). Two flag bits are provided (F_R and F_S); the flags are reset on the Low to High transition of the CLR_R, CLR_S inputs. The flag is set when either register is loaded. Each flag and register has independent control, thus allowing multiple usage of the part in a bidirectional mode. Two versions are available; Am2950 non-inverting data output and the Am2951 inverting data output.

LOGIC SYMBOL



Am2950 Non-Inverting Data
Am2951 Inverting Data

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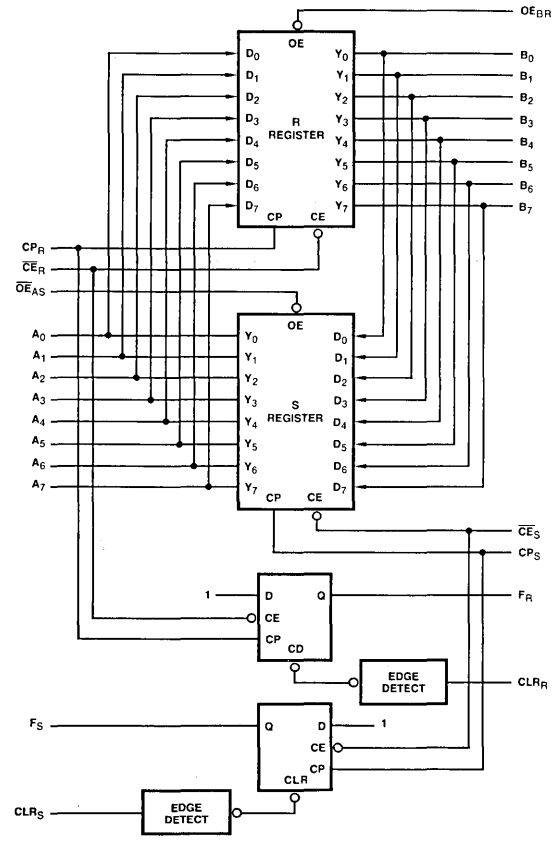
BLOCK DIAGRAM



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Am29700 • Am29701

Non-Inverting Schottky 64-Bit Random Access Memories

DISTINCTIVE CHARACTERISTICS

- Fully decoded 16-word x 4-bit Low-power Schottky RAMs
- Ultra-high speed: Address access time typically 15ns
- Low Power: I_{CC} typically 75mA
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with three-state outputs (Am29701) or with open collector outputs (Am29700)
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically tested and optically inspected die for the assemblers of hybrid products

FUNCTIONAL DESCRIPTION

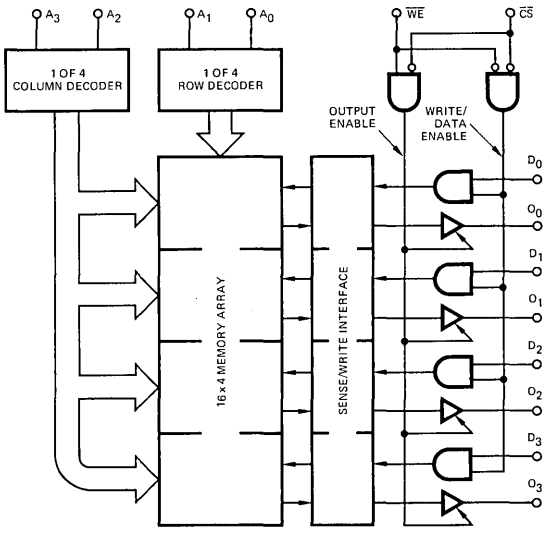
The Am29700 and Am29701 are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs (Am29700) or three-state outputs (Am29701). Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74S138.

An active LOW Write line $\overline{WE}$ controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word and preconditions the output circuitry so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four non-inverting outputs O_0 to O_3.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

LOGIC BLOCK DIAGRAM



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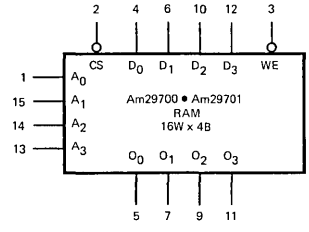
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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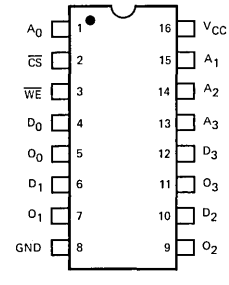
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8)	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	100mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

Part No.	V_{CC}	Ambient Temperature
Commercial Grade Am29700APC, DC Am29701APC, DC	5.0V ±5%	0°C to +75°C
Military Grade Am29700ADM, FM Am29701ADM, FM	5.0V ±10%	−55°C to +125°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	D. C. Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am29701 Only)	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2mA I_{OH} = −2.0mA	COM'L MIL	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA I_{OL} = 20mA			0.350 0.380	0.45 0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.40V	$\overline{WE}$, D_0-D_3, A_0-A_3 $\overline{CS}$			−0.015 −0.030	−0.250 −0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				0.0	10	µA
I_{SC} (Am29701 Only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V			−20	−45	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		COM'L MIL		75 75	100 105	mA
V_C	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−0.850	−1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 2.4V		Am29700/01		0	40	µA
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 0.4V, V_{CC} = MAX.		Am29701	−40	0		µA

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.

FUNCTION TABLE

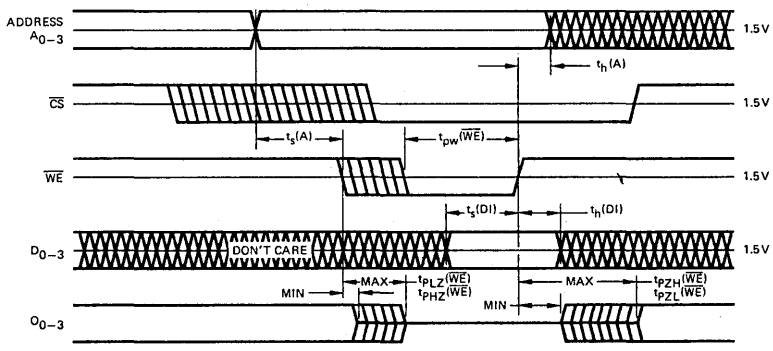
Input		Function	Data Output Status O_{0-3}
$\overline{CE}$	$\overline{WE}$		
Low	Low	Write	Output Disabled
Low	High	Read	Selected Word
High	Don't Care	Deselect	Output and Write Disabled

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

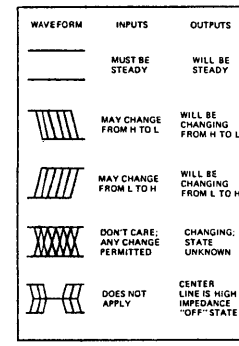
Parameters	Description		A. C. Test Conditions	Typ. (Note 1)	COM'L Min.	COM'L Max.	MIL Min.	MIL Max.	Units
$t_{PLH}(A)$ $t_{PHL}(A)$	Delay from Address to Output	See Fig. 2	Fig. 3 test load (measured to output = 1.5V)	15		25		30	ns
$t_{PZH}(\overline{CS})$ $t_{PZL}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data	See Fig. 2		10		15		20	ns
$t_{PZH}(\overline{WE})$ $t_{PZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery – See Note 2)	See Fig. 1		12		20		25	ns
$t_s(A)$	Set-up Time Address (Prior to Initiation of Write)	See Fig. 1		–6.0	0		0		ns
$t_h(A)$	Hold Time Address (After Termination of Write)	See Fig. 1		–2.5	0		0		ns
$t_s(DI)$	Set-up Time Data Input (Prior to Termination of Write)	See Fig. 1		9.0	20		25		ns
$t_h(DI)$	Hold Time Data Input (After Termination of Write)	See Fig. 1		–4.0	0		0		ns
$t_{pw}(\overline{WE})$	Min. Write Enable Pulse Width to Insure Write	See Fig. 1		10	20		25		ns
$t_{PHZ}(\overline{CS})$ $t_{PLZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (HI-Z)	See Fig. 2		10		15		20	ns
$t_{PLZ}(\overline{WE})$ $t_{PHZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output (HI-Z)	See Fig. 1		12		20		25	ns

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Output is preconditioned to data in during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch)

SWITCHING WAVEFORMS



KEY TO TIMING DIAGRAM



Write Cycle Timing. The cycle is initiated by an address change. After $t_s(A)$ min., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_h(A)$ min. must be allowed before the address may be changed again. The output will be inactive (floating for the Am29701) while the write enable is LOW.

Figure 1.

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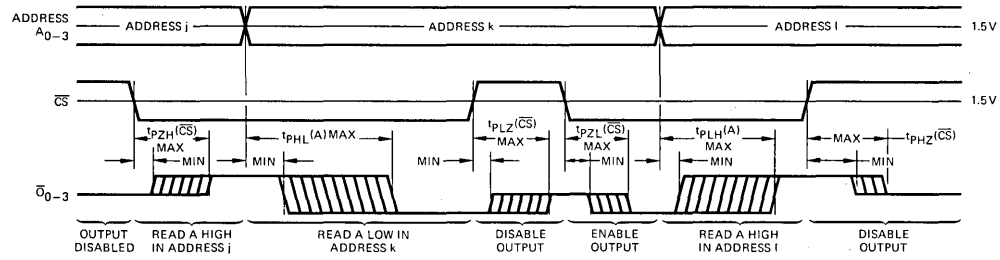
SWITCHING WAVEFORMS (Cont.)



Switching delays from address and chip select inputs to the data output. For the Am29701 disabled output is "OFF", represented by a single center line. For the Am29700, a disabled output is HIGH.

Figure 2.

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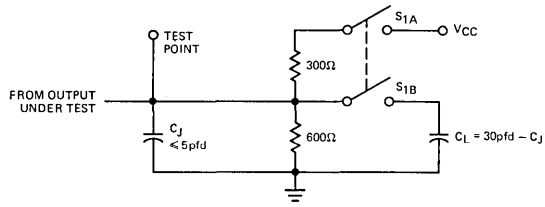
TEST LOAD

Open Collector Am29700

S_1 is closed for all A. C. tests. Note that $t_{PHZ}(\overline{CS})$ and $t_{PHZ}(\overline{WE})$ parameters do not apply to 29700 where disabled output is HIGH.



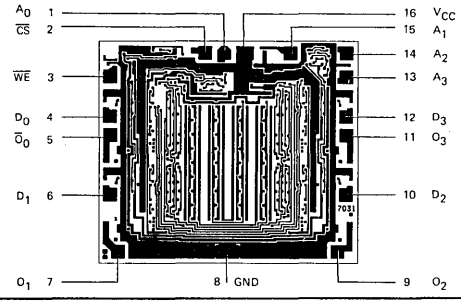
Three-State Am29701

S_1 is closed for all A. C. tests except $t_{PHZ}(\overline{CS})$ and $t_{PHZ}(\overline{WE})$ where S_1 is open and jig capacitance (C_J) is ⩽5pfd.

Figure 3.

MPR-244

Metallization and Pad Layout



DIE SIZE
0.092" X 0.078"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Open Collector Order Number	Three-State Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM29700PC	AM29701PC	P-16	C	C-1
AM29700DC	AM29701DC	D-16	C	C-1
AM29700DC-B	AM29701DC-B	D-16	C	B-1
AM29700DM	AM29701DM	D-16	M	C-3
AM29700DM-B	AM29701DM-B	D-16	M	B-3
AM29700FM	AM29701FM	F-16	M	C-3
AM29700FM-B	AM29701FM-B	F-16	M	B-3
AM29700XC	AM29701XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM29700XM	AM29701XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am29702 • Am29703

Schottky 64-Bit Random Access Memories

DISTINCTIVE CHARACTERISTICS

- Fully decoded 16-word x 4-bit Low-power Schottky RAMs
- Ultra-high speed: Address access time typically 15ns
- Low Power: I_{CC} typically 75mA
- Internal ECL circuitry for optimum speed/power performance over voltage and temperature
- Output preconditioned during write to eliminate write recovery glitch
- Available with three-state outputs (Am29703) or with open collector outputs (Am29702)
- Pin compatible replacements for 3101, 3101A, 74S289, 93403, 7489, 6560 and Am27S02 (use Am29702) for 74S189, 6561, DM8599 and Am27S03, (use Am29703)
- 100% reliability assurance testing in compliance with MIL-STD-883
- Electrically tested and optically inspected die for the assemblers of hybrid products

FUNCTIONAL DESCRIPTION

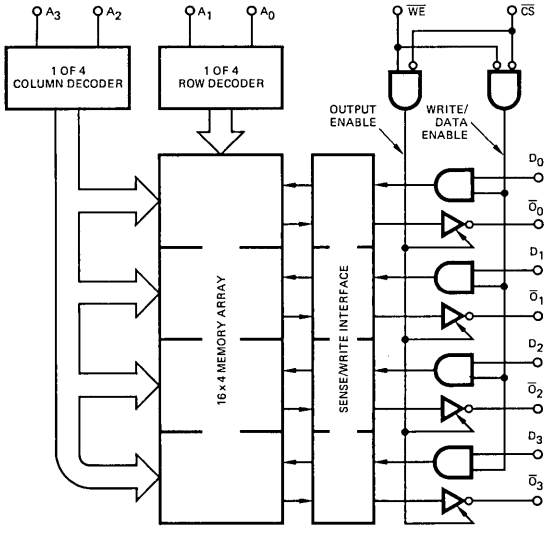
The Am29702 and Am29703 are 64-bit RAMs built using Schottky diode clamped transistors in conjunction with internal ECL circuitry and are ideal for use in scratch pad and high-speed buffer memory applications. Each memory is organized as a fully decoded 16-word memory of 4 bits per word. Easy memory expansion is provided by an active LOW chip select ($\overline{CS}$) input and open collector OR tieable outputs (Am29702) or three-state outputs (Am29703). Chip selection for large memory systems can be controlled by active LOW output decoders such as the Am74S138.

An active LOW Write line $\overline{WE}$ controls the writing/reading operation of the memory. When the chip select and write lines are LOW the information on the four data inputs D_0 to D_3 is written into the addressed memory word and preconditions the output circuitry so that true data is present at the outputs when the write cycle is complete. This preconditioning operation insures minimum write recovery times by eliminating the "write recovery glitch".

Reading is performed with the chip select line LOW and the write line HIGH. The information stored in the addressed word is read out on the four inverting outputs $\overline{O}_0$ to $\overline{O}_3$.

During the writing operation or when the chip select line is HIGH the four outputs of the memory go to an inactive high impedance state.

LOGIC BLOCK DIAGRAM



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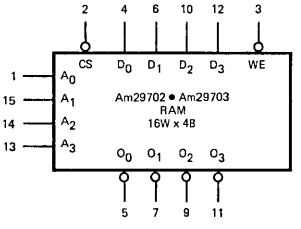
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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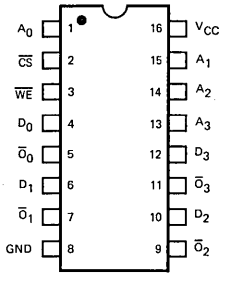
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8)	−0.5V to +7V
DC Voltage Applied to Outputs for High Output State	−0.5V to V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
Output Current, Into Outputs	100mA
DC Input Current	−30mA to +5.0mA

OPERATING RANGE

Part No.	V_{CC}	Ambient Temperature
Commercial Grade Am29702PC, DC Am29703PC, DC	5.0V ±5%	0°C to +75°C
Military Grade Am29702DM, FM Am29703DM, FM	5.0V ±10%	−55°C to +125°C

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	D. C. Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am29703 Only)	Output HIGH Voltage	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL}	I_{OH} = −5.2mA I_{OH} = −2.0mA	COM'L MIL	2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA I_{OL} = 20mA			0.350 0.380	0.45 0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.40V	$\overline{WE}$, D_0-D_3, A_0-A_3 $\overline{CS}$			−0.015 −0.030	−0.1 −0.1	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				0.0	10	μA
I_{SC} (Am29703 Only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V			−20	−45	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		COM'L MIL		75 75	100 105	mA
V_C	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−0.850	−1.2	Volts
I_{CEX}	Output Leakage Current	$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 2.4V		Am29702/03		0	40	μA
		$V_{\overline{CS}}$ = V_{IH} or $V_{\overline{WE}}$ = V_{IL} V_{OUT} = 0.4V, V_{CC} = MAX.		Am29703	−40	0		μA

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.

FUNCTION TABLE

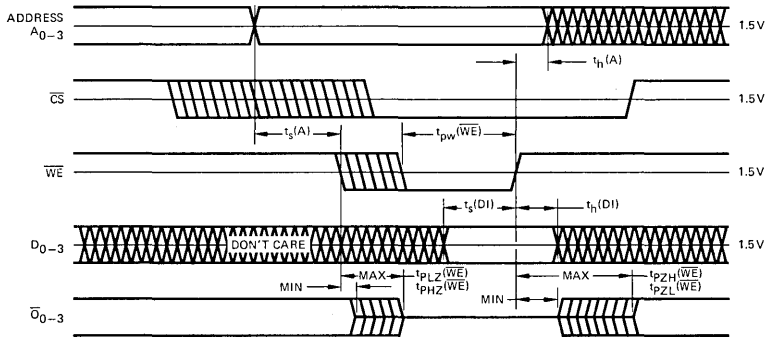
Input		Function	Data Output Status $\overline{O}_{0\text{-}3}$
$\overline{CE}$	$\overline{WE}$		
Low	Low	Write	Output Disabled
Low	High	Read	Selected Word (Inverted)
High	Don't Care	Deselect	Output and Write Disabled

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description		A. C. Test Conditions	Typ. (Note 1)	COM'L Min.	COM'L Max.	MIL Min.	MIL Max.	Units
$t_{PLH}(A)$ $t_{PHL}(A)$	Delay from Address to Output	See Fig. 2	Fig. 3 test load (measured to output = 1.5V)	15		25		30	ns
$t_{PZH}(\overline{CS})$ $t_{PZL}(\overline{CS})$	Delay from Chip Select (LOW) to Active Output and Correct Data	See Fig. 2		10		15		20	ns
$t_{PZH}(\overline{WE})$ $t_{PZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output and Correct Data (Write Recovery – See Note 2)	See Fig. 1		12		20		25	ns
$t_s(A)$	Set-up Time Address (Prior to Initiation of Write)	See Fig. 1		–6.0	0		0		ns
$t_h(A)$	Hold Time Address (After Termination of Write)	See Fig. 1		–2.5	0		0		ns
$t_s(DI)$	Set-up Time Data Input (Prior to Termination of Write)	See Fig. 1		9.0	20		25		ns
$t_h(DI)$	Hold Time Data Input (After Termination of Write)	See Fig. 1		–4.0	0		0		ns
$t_{pw}(\overline{WE})$	Min. Write Enable Pulse Width to Insure Write	See Fig. 1		10	20		25		ns
$t_{PHZ}(\overline{CS})$ $t_{PLZ}(\overline{CS})$	Delay from Chip Select (HIGH) to Inactive Output (HI-Z)	See Fig. 2		10		15		20	ns
$t_{PLZ}(\overline{WE})$ $t_{PHZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output (HI-Z)	See Fig. 1		12		20		25	ns

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Output is preconditioned to data in (inverted) during write to insure correct data is present on all outputs when write is terminated. (No write recovery glitch)

SWITCHING WAVEFORMS



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Write Cycle Timing. The cycle is initiated by an address change. After $t_s(A)$ min., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, $t_h(A)$ min. must be allowed before the address may be changed again. The output will be inactive (floating for the Am29703) while the write enable is LOW.

Figure 1.

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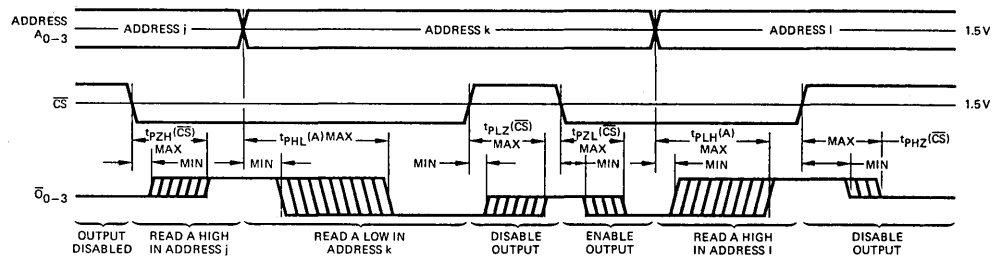
SWITCHING WAVEFORMS (Cont.)



Switching delays from address and chip select inputs to the data output. For the Am29703 disabled output is "OFF", represented by a single center line. For the Am29702, a disabled output is HIGH.

Figure 2.

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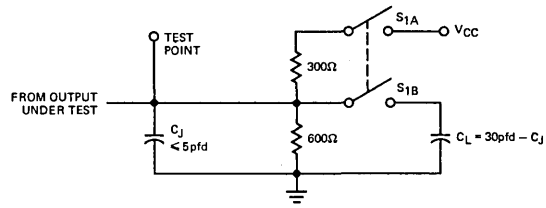
TEST LOAD

Open Collector Am29702

S_1 is closed for all A. C. tests. Note that $t_{PHZ}(\overline{CS})$ and $t_{PHZ}(\overline{WE})$ parameters do not apply to 29702 where disabled output is HIGH.



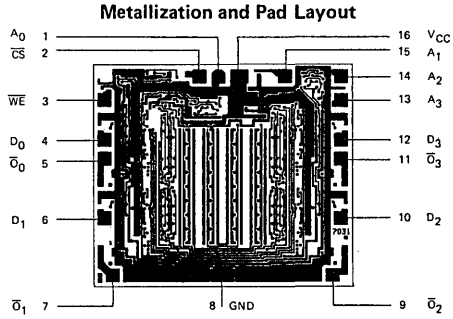
Three-State Am29703

S_1 is closed for all A. C. tests except $t_{PHZ}(\overline{CS})$ and $t_{PHZ}(\overline{WE})$ where S_1 is open and jig capacitance (C_J) is ≤ 5pfd.

Figure 3.

MPR-250

Metallization and Pad Layout



DIE SIZE
0.092" X 0.078"

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Open Collector Order Number	Three-State Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM29702PC	AM29703PC	P-16	C	C-1
AM29702DC	AM29703DC	D-16	C	C-1
AM29702DC-B	AM29703DC-B	D-16	C	B-1
AM29702DM	AM29703DM	D-16	M	C-3
AM29702DM-B	AM29703DM-B	D-16	M	B-3
AM29702FM	AM29703FM	F-16	M	C-3
AM29702FM-B	AM29703FM-B	F-16	M	B-3
AM29702XC	AM29703XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM29702XM	AM29703XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am29704 • Am29705

16-Word By 4-Bit Two-Port RAM

Distinctive Characteristics

- 16-word by 4-bit, 2-port RAM
- Two output ports, each with separate output control
- Separate four-bit latches on each output port
- Data output is non-inverting with respect to data input
- Chip Select and Write Enable inputs for ease in cascading
- Advanced Low-Power Schottky processing
- 100% reliability testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

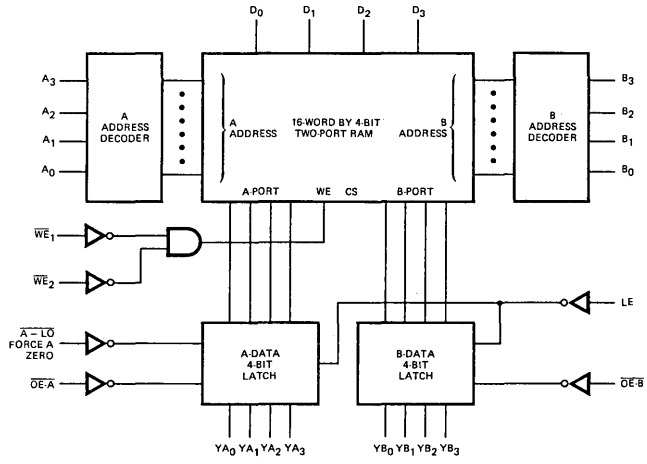
The Am29704 and Am29705 are 16-word by 4-bit, two-port RAM's built using advanced Low-Power Schottky processing. These RAM's feature two separate output ports such that any two 4-bit words can be read from these outputs simultaneously. Each output port has a four-bit latch but a common Latch Enable (LE) input is used to control all eight latches. The device has two Write Enable ($\overline{WE}$) inputs and is designed such that the Write Enable 1 ($\overline{WE}_1$) and Latch Enable (LE) inputs can be wired together to make the operation of the RAM appear edge triggered.

The device has a fully decoded four-bit A-address field to address any of the 16 memory words for the A-output port. Likewise, a four-bit B-address input is used to simultaneously select any of the 16 words for presentation at the B-output port. New incoming data is written into the four-bit RAM word selected by the B-address. The D inputs are used to load new data into the device.

The Am29704 has open-collector outputs and the Am29705 features three-state outputs so that several devices can be cascaded to increase the total number of memory words in the system. The A-output port is in the high-impedance state when the $\overline{OE}$-A input is HIGH. Likewise, the B-output port is in the high-impedance state when the $\overline{OE}$-B input is HIGH. Four devices can be paralleled using only one Am25LS139 decoder for output control.

The Write Enable inputs control the writing of new data into the RAM. When both Write Enable inputs are LOW, new data is written into the word selected by the B-address field. When either Write Enable input is HIGH, no data is written into the RAM.

LOGIC DIAGRAM



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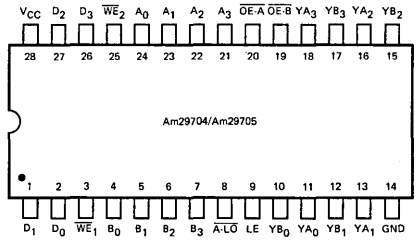
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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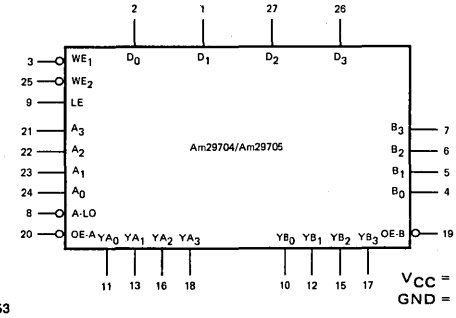
LOGIC SYMBOL



V_{CC} = Pin 28
GND = Pin 14

MPR-253

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am29704XC, Am29705XC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am29704XM, Am29705XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN = 4.50V MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (Am29705 Only)	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	MIL, I_{OH} = −2.0mA	2.4			Volts
			COM'L, I_{OH} = −4.0mA	2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4	Volts
			I_{OL} = 8.0mA			0.45	
			I_{OL} = 12mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	A_i, B_i			−0.25	mA
			$\overline{OE\text{-}A}$, $\overline{OE\text{-}B}$			−0.54	
			Others			−0.36	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				0.1	mA
I_O	Output OFF Current (Am29704 Only)	V_{CC} = MAX., V_{OH} = 5.5V, V_{IN} = V_{IH} or V_{IL}				100	µA
I_O	Off State (High Impedance) Output Current (Am29705 Only)	V_{CC} = MAX., V_{IN} = V_{IH} or V_{IL}	V_O = 2.7V			20	µA
			V_O = 0.4V			−20	
I_{SC}	Output Short Circuit Current (Note 3) (Am29705 Only)	V_{CC} = MAX.		−30		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Worst case I_{CC} is at minimum temperature) (Note 4)	T_A = 25°C		121	195	mA
			T_A = 0°C to +70°C			210	
			T_A = 70°C			170	
			T_C = −55°C to +125°C			210	
			T_C = 125°C			150	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. All inputs grounded except $\overline{OE\text{-}A}$ and $\overline{OE\text{-}B}$ =2.4V.

SWITCHING CHARACTERISTICS

(Input Levels = 0V and 3.0V, Transitions Measured at 1.5V)

Maximum Combinational Delays (in ns) (R_L = 390Ω, C_L = 50pF)

Parameters	From	To	Conditions	T_A = 0°C to +70°C, V_{CC} = 4.75 to 5.25V		T_C = −55°C to +125°C, V_{CC} = 4.5V to 5.5V	
				Am29704	Am29705	Am29704	Am29705
Access Time	A Address Stable or B Address Stable	YA Stable or YB Stable	LE = HIGH	61	53	68	58
	Both $\overline{WE}$ LOW	YB = D or YA = D (If A=B)	LE = HIGH	53	45	58 (Note)	48 (Note)
Turn-on Time	$\overline{OE\text{-}A}$ or $\overline{OE\text{-}B}$ LOW	YA or YB Stable		38	30	40	30
Turn-Off Time	$\overline{OE\text{-}A}$ or $\overline{OE\text{-}B}$ HIGH	YA or YB Off	C_L = 5.0pF	28	20	30	20
Reset Time	$\overline{A\text{-}LO}$ LOW	YA LOW		43	35	45	35
Enable Time	LE HIGH	YA and YB Stable		33	25	38	28
	Data In	YA or YB = D	LE = HIGH, Both $\overline{WE}$ LOW	58	50	60 (Note)	50 (Note)

Note: Transparency not guaranteed below 0°C.

SWITCHING CHARACTERISTICS (Cont.)

(Input Levels = 0V and 3.0V, Transitions Measured at 1.5V)

Minimum Set-up and Hold Times (in ns)

Parameters	From	To	Conditions	$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Max.	$T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Max.
Data Set-up Time	D Stable	Either $\overline{WE}$ HIGH		20	25
Data Hold Time	Either $\overline{WE}$ HIGH	D Changing		3	5
Address Set-up Time	B Stable	Both $\overline{WE}$ LOW		5	5
Address Hold Time	Either $\overline{WE}$ HIGH	B Changing		0	0
Latch Close Before Write Begins	LE LOW	$\overline{WE}_1$ LOW	$\overline{WE}_2$ LOW	0	0
	LE LOW	$\overline{WE}_2$ LOW	$\overline{WE}_1$ LOW	0	0
Address Set-up Before Latch Closes	A or B Stable	LE LOW		45	50

Minimum Pulse Widths

Parameters	Input	Pulse	Conditions	$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$ Max.	$T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$ Max.
Write Pulse Width	$\overline{WE}_1$	HIGH-LOW-HIGH	$\overline{WE}_2$ LOW	25	25
	$\overline{WE}_2$	HIGH-LOW-HIGH	$\overline{WE}_1$ LOW	20	20
A Latch Reset Pulse	$\overline{A\text{-}LO}$	HIGH-LOW-HIGH		20	20
Latch Data Capture	LE	LOW-HIGH-LOW		20	25

FUNCTION TABLES

WRITE CONTROL

$\overline{WE}_1$	$\overline{WE}_2$	Function	RAM Outputs at Latch Inputs A-Port	RAM Outputs at Latch Inputs B-Port
L	L	Write D Into B	A data (A ≠ B)	D input data*
X	H	No write	A data	B data
H	X	No write	A data	B data

H = HIGH
L = LOW
X = Don't care

*Note: Transparency not guaranteed below 0°C.

YA READ

Inputs $\overline{OE-A}$	Inputs $\overline{A-LO}$	Inputs LE	YA Output	Function
H	X	X	Z	High impedance
L	L	X	L	Force YA LOW
L	H	H	A – Port RAM data	Latches transparent
L	H	L	NC	Latches retain data

H = HIGH
L = LOW
X = Don't care
Z = High impedance
NC = No change

YB READ

Inputs $\overline{OE-B}$	Inputs LE	YB Output	Function
H	X	Z	High impedance
L	H	B – Port RAM data	Latches transparent
L	L	NC	Latches retain data

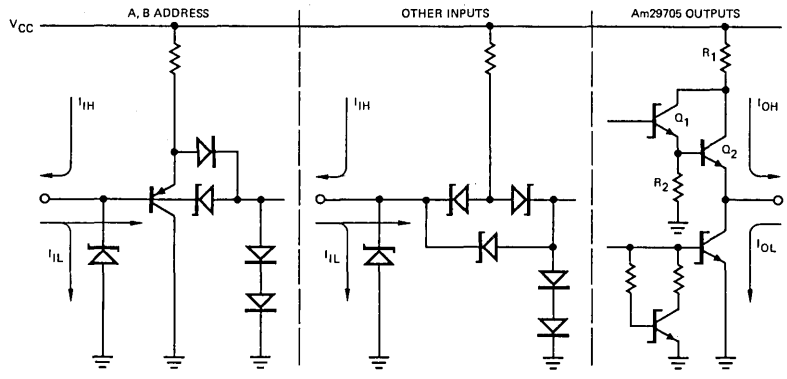
H = HIGH
L = LOW
X = Don't care
Z = High impedance
NC = No change

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_1	1	1	–	–
D_0	2	1	–	–
$\overline{WE}_1$	3	1	–	–
B_0	4	0.55	–	–
B_1	5	0.55	–	–
B_2	6	0.55	–	–
B_3	7	0.55	–	–
$\overline{A-LO}$	8	1	–	–
LE	9	1	–	–
YB_0	10	–	100/200	33
YA_0	11	–	100/200	33
YB_1	12	–	100/200	33
YA_1	13	–	100/200	33
GND	14	–	–	–
YB_2	15	–	100/200	33
YA_2	16	–	100/200	33
YB_3	17	–	100/200	33
YA_3	18	–	100/200	33
$\overline{OE-B}$	19	1	–	–
$\overline{OE-A}$	20	1	–	–
A_3	21	0.55	–	–
A_2	22	0.55	–	–
A_1	23	0.55	–	–
A_0	24	0.55	–	–
$\overline{WE}_2$	25	1	–	–
D_3	26	1	–	–
D_2	27	1	–	–
V_{CC}	28	–	–	–

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

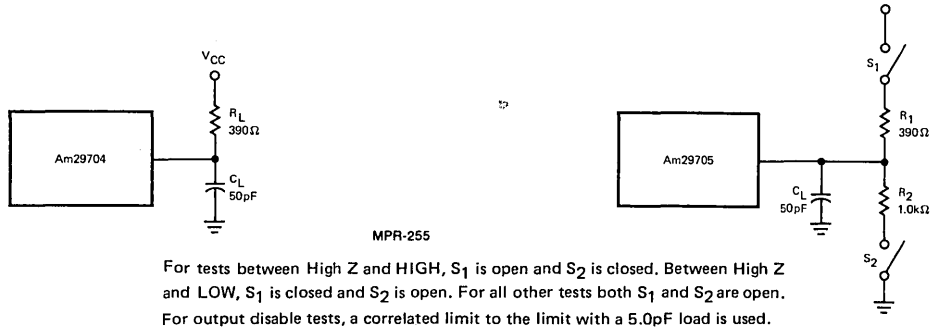
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.
Omit Q_1, Q_2, R_1 and R_2 for Am29704.

MPR-254

LOAD CIRCUITS FOR AC TESTS



MPR-255

For tests between High Z and HIGH, S_1 is open and S_2 is closed. Between High Z and LOW, S_1 is closed and S_2 is open. For all other tests both S_1 and S_2 are open.
For output disable tests, a correlated limit to the limit with a 5.0pF load is used.

MPR-256

DEFINITION OF TERMS

D_0, D_1, D_2, D_3 Data Inputs. New data is written into the RAM through these inputs.

A_0, A_1, A_2, A_3 The A-address Inputs. The four-bit field presented at the A inputs selects one of the 16 memory words for presentation to the A-Data Latch.

B_0, B_1, B_2, B_3 The B-address inputs. The four-bit field presented at the B inputs selects one of the 16 memory words for presentation to the B-Data Latch. The B address field also selects the word into which new data is written.

YA_0, YA_1, YA_2, YA_3 The four A-Data Latch Outputs.

YB_0, YB_1, YB_2, YB_3 The four B-Data Latch Outputs.

$\overline{WE}_1, \overline{WE}_2$ Write Enables. When both Write Enables are LOW, new data is written into the word selected by the B-address field. If either Write Enable input is HIGH, no new data can be written into the memory.

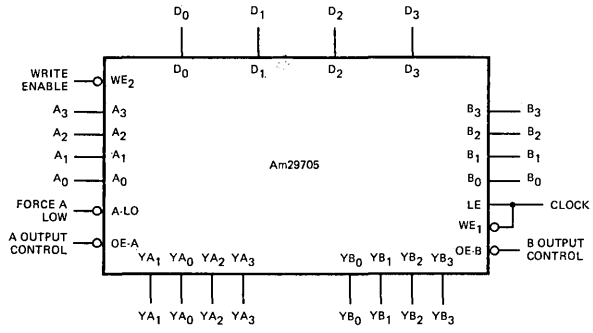
$\overline{OE}$-A A-port Output Enable. When $\overline{OE}$-A is LOW, data in the A-Data Latch is present at the YA_i outputs. If $\overline{OE}$-A is HIGH, the YA_i outputs are in the high-impedance (off) state.

$\overline{OE}$-B B-port Output Enable. When $\overline{OE}$-B is LOW, data in the B-Data Latch is present at the YB_i outputs. When $\overline{OE}$-B is HIGH, the YB_i outputs are in the high-impedance (off) state.

LE Latch Enable. The LE input controls the latches for both the RAM A-output port and RAM B-output port. When the LE input is HIGH, the latches are open (transparent) and data from the RAM, as selected by the A and B address fields, is present at the outputs. When LE is LOW, the latches are closed and they retain the last data read from the RAM independent of the current A and B address field inputs.

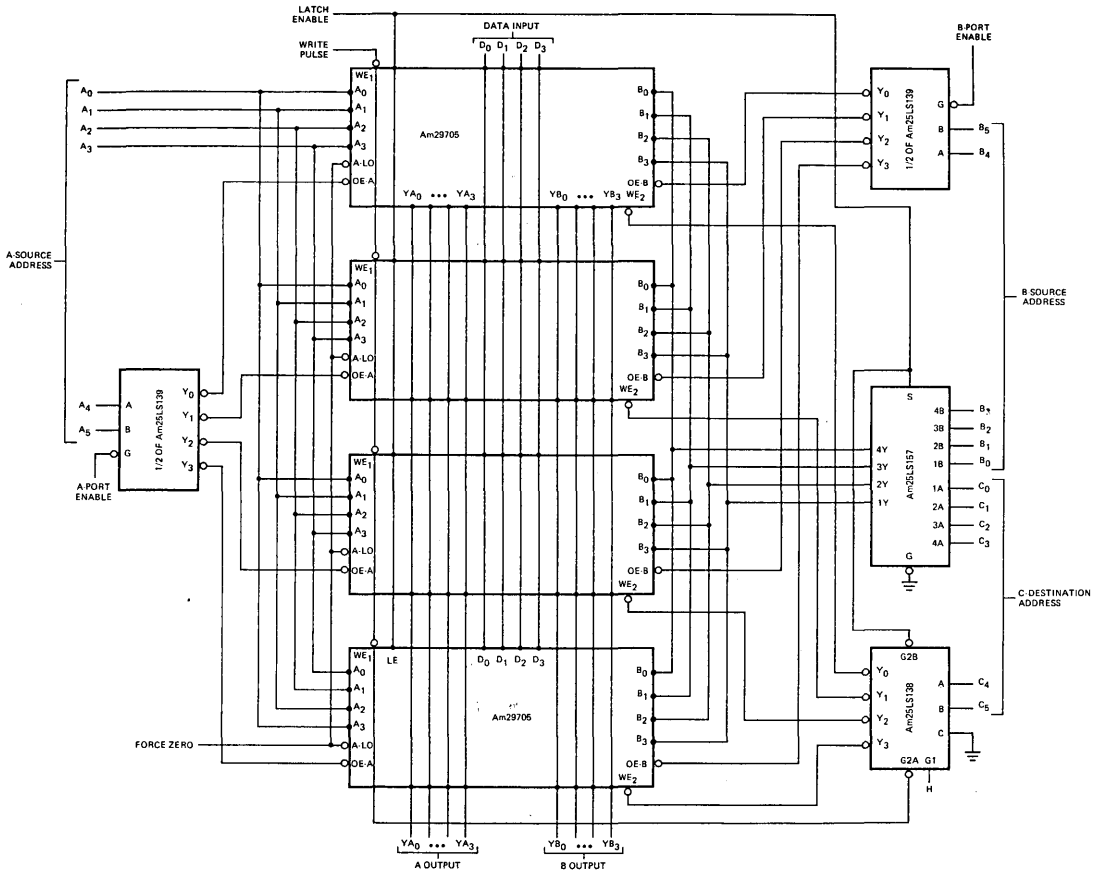
$\overline{A\text{-}LO}$ Force A Zero. This input is used to force the outputs of the A-port latches LOW independent of the Latch Enable input or A-address field select inputs. Thus, the A-output bus can be forced LOW using this control signal. When the $\overline{A\text{-}LO}$ input is HIGH, the A latches operate in their normal fashion. Once the A latches are forced LOW, they remain LOW independent of the $\overline{A\text{-}LO}$ input if the latches are closed.

APPLICATIONS



MPR-257

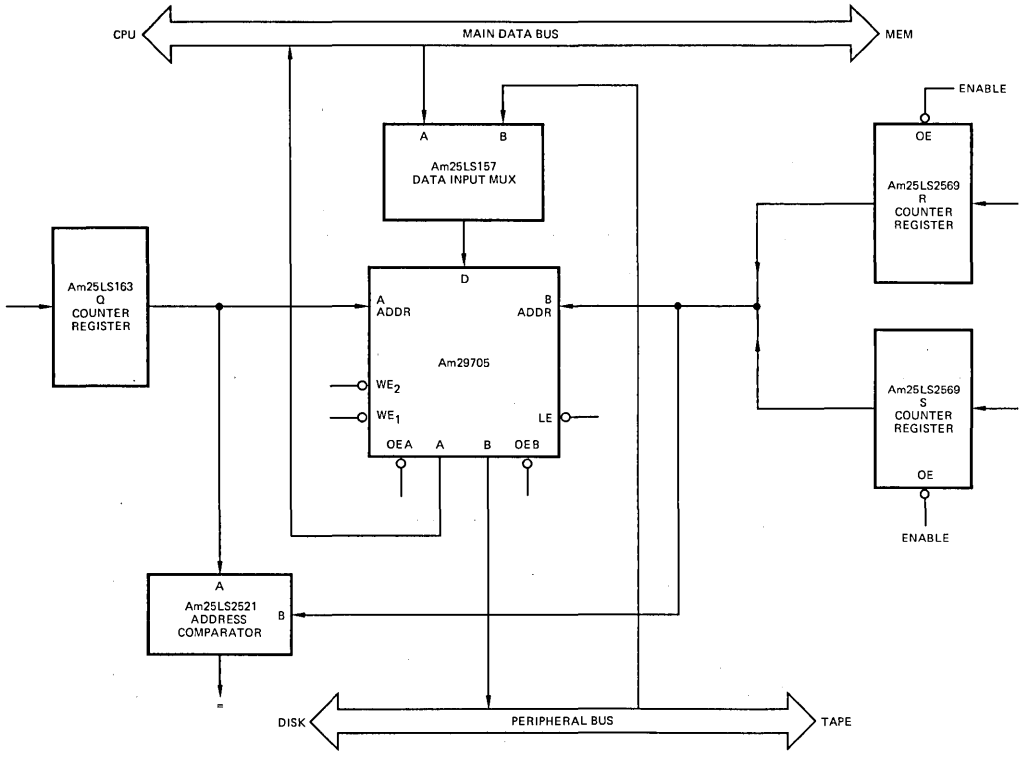
A 16-word by 4-bit two-port RAM with LE and WE_1 connected to make the device appear edge triggered. WE_1 and WE_2 are logically identical but are electrically slightly different. For synchronous operation without possibility of race, WE_1 should be connected to LE.



MPR-258

A 64-word by 4-bit three address memory. Data is read from the A address to the YA outputs and from the B address to the YB outputs while the latch enable is HIGH. When the latch enable goes LOW, the YA and YB data is held in the internal latches, and the RAM B address is switched to the C-destination address lines. A write pulse will then deposit the input data into the location selected by the C address.

APPLICATIONS (Cont'd)



The Am29705 as a two-way interface buffer. Data may be passed between the main data bus and the peripheral data bus under I/O control. The two-port RAM allows data to be written into buffer storage from a peripheral device, using the B address port and the S counter register, while it is being read into main memory, using the A address port and the Q counter register. This simultaneous read/write capability facilitates DMA transfers because the CPU can ignore write requests from the peripheral device. Data output from CPU to the peripheral device is handled by sequential write and read operations. Data is written into buffer storage from the CPU, using the B address port and the R counter register. It is read onto the peripheral device using the B address port and either the R register, for single word transfers, or the S register, for block transfers.

MPR-259

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Open Collector Order Number	Three-State Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM29704PC	AM29705PC	P-28	C	C-1
AM29704DC	AM29705DC	D-28	C	C-1
AM29704DC-B	AM29705DC-B	D-28	C	B-1
AM29704DM	AM29705DM	D-28	M	C-3
AM29704DM-B	AM29705DM-B	D-28	M	B-3
AM29704FM	AM29705FM	F-28	M	C-3
AM29704FM-B	AM29705FM-B	F-28	M	B-3
AM29704XC	AM29705XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM29704XM	AM29705XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am29720 • Am29721

Low-Power Schottky 256-Bit Random Access Memories

DISTINCTIVE CHARACTERISTICS

- Fully decoded 256-bit TTL RAMs.
  Plug-in replacements for 74200, IM5503/5523, 93411/21
  Pin compatible with MM6530/31, 3106/7, 82S06, 74S201
- Open collector (Am29720) and three-state (Am29721)
- High speed operation:
  35ns typical access time
  45ns guaranteed (0°C to +75°C)
  55ns guaranteed (–55°C to +125°C)
- Very low power dissipation
  275mW typical
  70mA maximum I_{CC}
- Full military temperature range performance.
  10% power supply tolerance
- Internal ECL circuitry
  Uniform access times over voltage and temperature variations.
- Tested to GALPAT.
  Functional and switching characteristics are guaranteed for all data and address patterns.

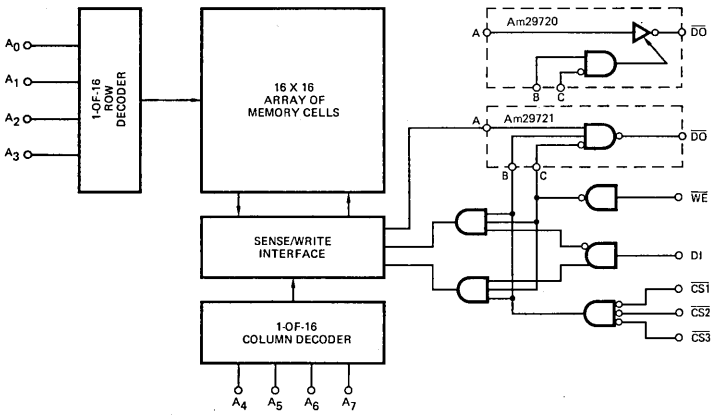
FUNCTIONAL DESCRIPTION

The Am29720 and Am29721 are fully decoded bipolar random access memories for use in high-speed buffer memories and as a replacement for high-speed core memories in digital systems. The memories are organized 256-words by 1-bit with an 8-bit binary address field and separate data in and data output lines. The memories have three active LOW chip select inputs and a three-state output (Am29721) or open-collector output (Am29720). All inputs are buffered to present an input load of only 0.5 TTL unit loads.

Read/write operation is controlled by an active LOW write enable input. When the write enable is LOW and the chip is selected the data on the data input is written into the location specified by the address inputs. During this operation the output floats allowing the data bus to be used by other memories or open-collector logic elements that are tied to the inverting data output. Reading is accomplished by having the chip selected and the write enable input HIGH. Data stored in the location specified by the address inputs is read out and appears on the data output inverted.

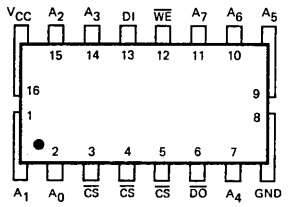
The chip is selected by three active LOW inputs all of which must be LOW in order for the data output to be active during the read operation and for data to be written into or from the memory. These three active LOW chip select inputs permit the Am25LS138 MSI decoders to select memories in either a linear select, two or three dimensional mode of operation when large memory systems are being built. The delay from the chip select to the output is considerably faster than from the address inputs and extra delay can be tolerated in the chip select path without affecting system performance.

LOGIC DIAGRAM



MPR-260

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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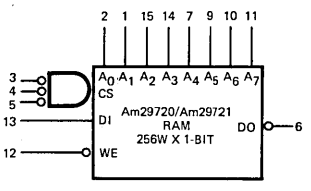
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC} max
DC Input Voltage	−0.5V to +V_{CC}
Output Current, Into Outputs	30mA
DC Input Current	−30mA to +50mA

OPERATING RANGE

Part No.	Ambient Operating Temperature	Power Supply Voltage
Am29720DC, PC Am29721DC, PC	0°C to +75°C	4.75 V to 5.25 V
Am29720DM, FM Am29721DM, FM	−55°C to +125°C	4.50 V to 5.50 V

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage (Am29721 Only)	V_{CC} = MIN., I_{OH} = −2.0 mA (MIL Range) V_{IN} = V_{IH} or V_{IL}, I_{OH} = −2.6 mA (COM'L Range)	2.4	3.1		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16.0 mA, V_{IN} = V_{IH} or V_{IL}		0.3	0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4 V		−0.50	−0.80	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7 V		<1	20	μA
V_{BK}	Input Breakdown Voltage	V_{CC} = MAX., I_{IN} = 100 μA	7.0			V
I_{LK}	Output Leakage Current	V_{CC} = MAX., $\overline{CS}$ = 2.4 V, V_{OUT} = 2.4 V		<1	30	μA
		V_{CC} = MAX., $\overline{CS}$ = 2.4 V, V_{OUT} = 0.4 V		<1	−30	
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0 V	−20	−30	−60	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.		55	70	mA
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18 mA			−1.5	Volts

Note 1. Typical Limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Parameters	Description		T_A = 25°C Typ.	T_A = 0°C to 75°C Min.	T_A = 0°C to 75°C Max.	T_A = −55°C to 125°C Min.	T_A = −55°C to 125°C Max.	Units
t_{PLH}(A) t_{PHL}(A)	Delay from Address to Output	See Fig. 2	35	15	45	10	55	ns
$t_{PZH}(\overline{CS})$ $t_{PZL}(\overline{CS})$	Delay from Chip Select to Active Output and Correct Data	See Fig. 2	15	5	25	5	30	ns
$t_{PHZ}(\overline{CS})$ $t_{PLZ}(\overline{CS})$	Delay from Chip Select to Inactive Output	See Fig. 2	15	5	25	5	30	ns
$t_{rec}(\overline{WE})$	Delay from Write Enable (HIGH) to Correct Output Data	See Fig. 1	25		45		55	ns
$t_{PZH}(\overline{WE})$ $t_{PZL}(\overline{WE})$	Delay from Write Enable (HIGH) to Active Output	See Fig. 1		5		5		ns
$t_{PHZ}(\overline{WE})$ $t_{PLZ}(\overline{WE})$	Delay from Write Enable (LOW) to Inactive Output	See Fig. 1	20		30		40	ns
t_s(A)	Set-up Time Address	See Fig. 1	0	15		20		ns
t_h(A)	Hold Time Address		0	0		10		ns
t_s(DI)	Set-up Time Data Input	See Fig. 1	25	30		40		ns
t_h(DI)	Hold Time Data Input	See Fig. 1	0	0		10		ns
$t_{pw}(\overline{WE})$	Write Enable Pulse Width	See Fig. 1	30	35		50		ns

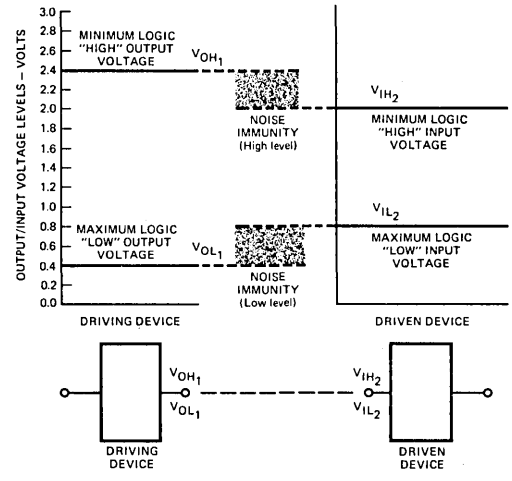
Am29720/Am29721 LOADING RULES (In TTL Unit Loads)

Input/Output	Pin No.s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
A_1	1	0.5	—	—
A_0	2	0.5	—	—
$\overline{CS}$	3	0.5	—	—
$\overline{CS}$	4	0.5	—	—
$\overline{CS}$	5	0.5	—	—
DO	6	—	(Note) 50	10
A_4	7	0.5	—	—
GND	8	—	—	—
A_5	9	0.5	—	—
A_6	10	0.5	—	—
A_7	11	0.5	—	—
$\overline{WE}$	12	0.5	—	—
DI	13	0.5	—	—
A_3	14	0.5	—	—
A_2	15	0.5	—	—
V_{CC}	16	—	—	—

Note: Am2950 has open collector output.

INPUT/OUTPUT INTERFACE CONDITIONS

Voltage Interface Conditions — LOW & HIGH



Note: Refer to Electrical Characteristics for measure currents.

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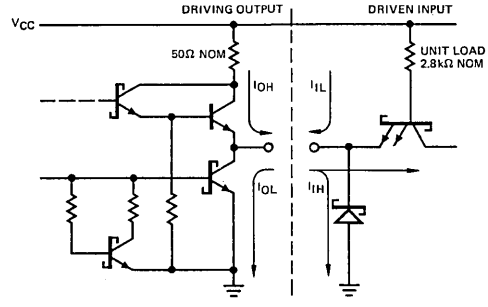
INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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UNIT LOAD DEFINITIONS

SERIES	HIGH Current	HIGH Measure Voltage	LOW Current	LOW Measure Voltage
Am25/26/2700	40μA	2.4V	–1.6mA	0.4V
Am25S/26S/27S	50μA	2.7V	–2.0mA	0.5V
Am25L/26L/27L	20μA	2.4V	–0.4mA	0.3V
Am25LS/26LS/27LS	20μA	2.7V	–0.36mA	0.4V
Am54/74	40μA	2.4V	–1.6mA	0.4V
54H/74H	50μA	2.4V	–2.0mA	0.4V
Am54S/74S	50μA	2.7V	–2.0mA	0.5V
54L/74L (Note 1)	20μA	2.4V	–0.8mA	0.4V
54L/74L (Note 1)	10μA	2.4V	–0.18mA	0.3V
Am54LS/74LS	20μA	2.7V	–0.36mA	0.4V
Am9300	40μA	2.4V	–1.6mA	0.4V
Am93L00	20μA	2.4V	–0.4mA	0.3V
Am93S00	50μA	2.7V	–2.0 mA	0.5 V
Am75/85	40μA	2.4V	–1.6mA	0.4V
Am8200	40μA	4.5V	–1.6mA	0.4V

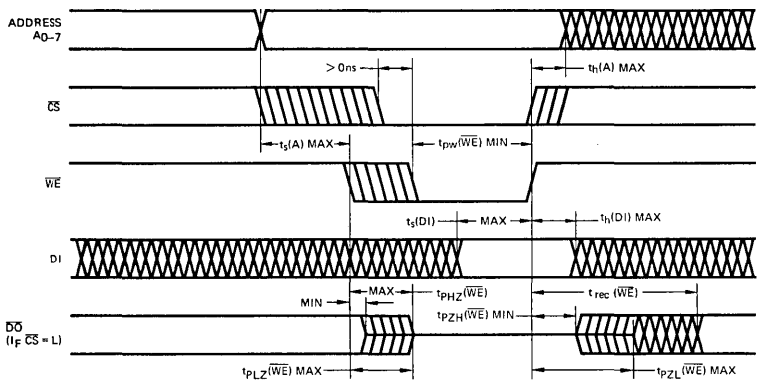
Note: 1. 54L/74L has two different types of standard inputs.

TRUTH TABLE

Inputs $\overline{CS}$	Inputs $\overline{WE}$	Inputs DI	Output $\overline{DO}(t_{n+1})$	Mode
H	X	X	OFF	No Selection
L	L	L	OFF	Write '0'
L	L	H	OFF	Write '1'
L	H	X	$\overline{DI}(t_n)$	Read

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
OFF = Floating output level is determined by external circuitry connected to the output.

SWITCHING WAVEFORMS



KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

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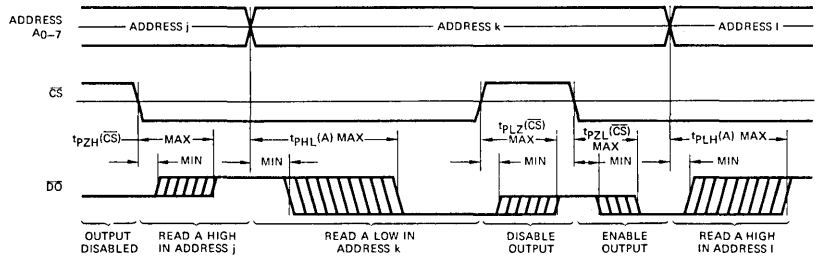
Write Cycle Timing. The cycle is initiated by an address change. After t_s(A) max., the write enable may begin. The chip select must also be LOW for writing. Following the write pulse, t_h(A) max. must be allowed before the address may be changed again. The output will be inactive (floating for the Am29721) while the write enable is LOW. Ordinarily, the chip select should be LOW during the entire write pulse.

Figure 1



Switching delays from address and chip select inputs to the data output. For the Am29721 disabled output is "OFF," represented by a single center line. For the Am29720, a disabled output is HIGH.

Figure 2

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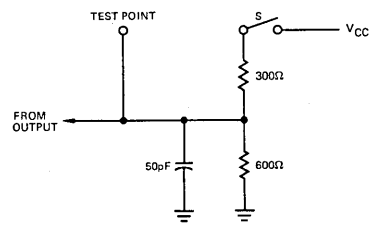
TEST LOAD



Note: All measurements at 1.5V.

S is closed for all tests except for Am29721 tests in which the output switches between an active HIGH level and a HIGH impedance state.

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OUTPUT LOADING RULES

The Am29720 has an open collector output. The outputs of several memories may be tied together and the common line connected through a pull-up resistor to V_{CC}. The common line will go LOW if and only if one of the Am29720 outputs connected to it goes LOW, i.e., is enabled and reading a LOW. The HIGH state is established by the pull-up resistor. The value of the resistor is limited by two equations:

$$R(min) = \frac{V_{CC}\ (max) - 0.4}{16 - i\ (1.6)}$$

i = number of TTL inputs driven

$$R(max) = \frac{V_{CC}\ (min) - 2.4}{0.03n + 0.04i}$$

n = number of outputs connected together

For highest speed, use the minimum R; for lowest power, use the maximum R.

The Am29721 has active circuitry to establish both the HIGH and LOW logic levels and requires no pull-up resistor. Up to 64 Am29721 outputs can be connected together.

DEFINITIONS OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH-signal level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to a LOW signal level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

X Unknown or don't care state

Z OFF, applying to the third high impedance state of the output.

FUNCTIONAL TERMS:

Three State A three state output can exist in three possible states: output LOW sinking current, output HIGH sourcing current, and output floating where the output level is determined by external circuitry connected to the output. This three state output allows AND tying of memory outputs for memory expansion and still keeps the inherent high speed of active pull-up circuitry.

Fully Decoded In a fully decoded memory every possible address combination of logic HIGH's and LOW's uniquely selects a memory word. This form of decoding requires no additional special purpose decoders for system operation and is the most efficient in terms of address inputs required and overall system speed.

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T^2L gate input load.

SWITCHING TERMS: (All switching times are measured at the 1.5 V logic level).

t_{PXH} The delay from a logic level change at an input to a HIGH level on an output.

t_{PXL} The delay from a logic level change at an input to a LOW level on an output.

t_{PXZ} The delay from a logic level change at an input to a high impedance state on a three state output. Measured with a resistor pull-down or pull-up.

t_{PXX}**(A)** The delay from an address input to the memory output.

$t_{PXX}(\overline{CS})$ The delay from a chip select input to the memory output.

$t_{PXZ}(\overline{WE})$ The delay from a HIGH-to-LOW transition on the write enable to a high impedance level on the memory output.

$t_{PZX}(\overline{WE})$ The delay from a LOW-to-HIGH transition on the write enable to an active level on the memory output.

$t_{pw}(\overline{WE})$ The shortest LOW pulse on the write enable input which is guaranteed to cause the memory to write. Pulses shorter than $t_{pw}(\overline{WE})$ min. may or may not cause a write to occur.

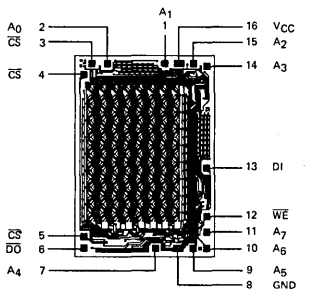
t_s**(A)** The set-up time of the address inputs relative to the HIGH-to-LOW edge of the write pulse. This is the time required for internal address decoding to settle. To avoid writing in spurious addresses, a stable address should be applied to the address inputs at least t_s(A) max. before the write pulse begins.

t_h**(A)** The address hold time. This parameter is similar to t_s(A) but is measured relative to the end of the write pulse rather than the beginning. A stable address should be maintained on the address inputs for t_h(A) max. after the write pulse has ended in order to prevent writing in spurious addresses.

t_s**(DI)** Data set-up time. The time prior to the end of the write pulse during which data must be stable to be correctly written into the memory.

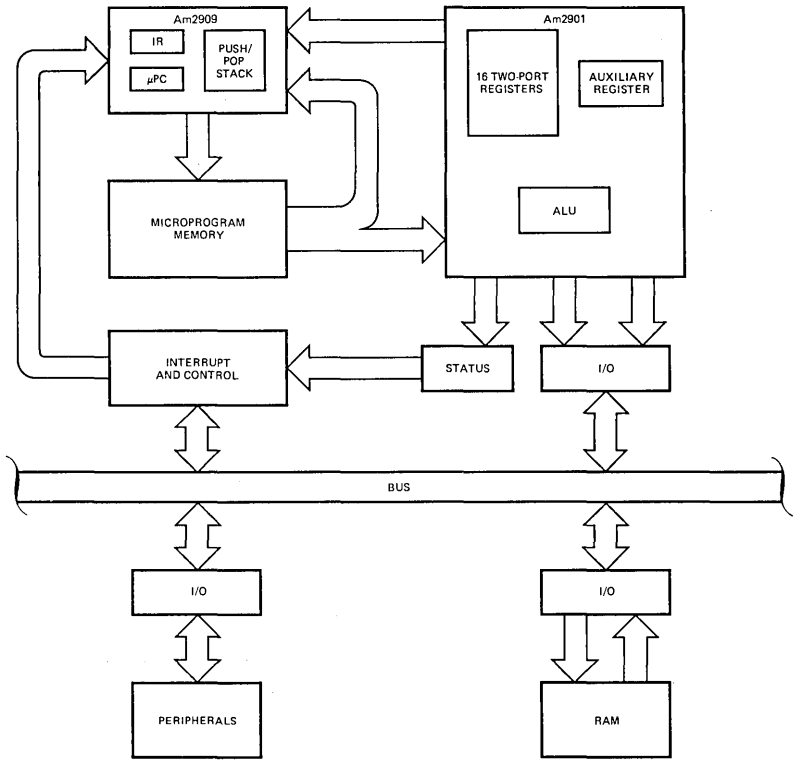
t_h**(DI)** Data hold time. The time following the end of the write pulse during which data must not be changed.

Metallization and Pad Layout



DIE SIZE 84 X 121 Mils

BIPOLAR MICROCOMPUTER ARCHITECTURE



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ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Open Collector Order Number	Three-State Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM29720PC	AM29721PC	P-16	C	C-1
AM29720DC	AM29721DC	D-16	C	C-1
AM29720DC-B	AM29721DC-B	D-16	C	B-1
AM29720DM	AM29721DM	D-16	M	C-3
AM29720DM-B	AM29721DM-B	D-16	M	B-3
AM29720FM	AM29721FM	F-16	M	C-3
AM29720FM-B	AM29721FM-B	F-16	M	B-3
AM29720XC	AM29721XC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM29720XM	AM29721XM	Dice	M	

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am29750A • Am29751A

256-Bit Generic Series Bipolar PROM

PRELIMINARY DATA

DISTINCTIVE CHARACTERISTICS

- High Speed – 40ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

FUNCTIONAL DESCRIPTION

The Am29750A and Am29751A are high speed electrically programmable Schottky read only memories. Organized in the industry standard 32 x 8 configuration, they are available in both open collector Am29750A and three-state Am29751A output versions. After programming, stored information is read on outputs O_0–O_7 by applying unique binary addresses to A_0–A_4 and holding the chip select input, CS, at a logic LOW. If the chip select input goes to a logic HIGH, O_0–O_7 go to the off or high impedance state.

GENERIC SERIES CHARACTERISTICS

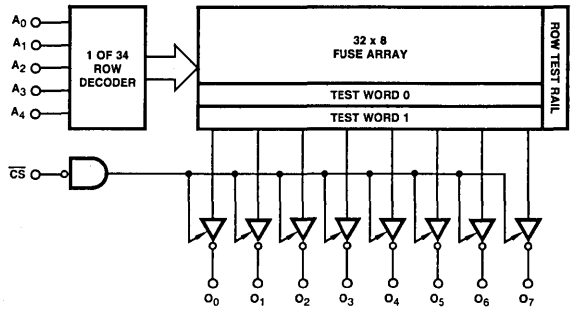
The Am29750A and Am29751A are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

BLOCK DIAGRAM



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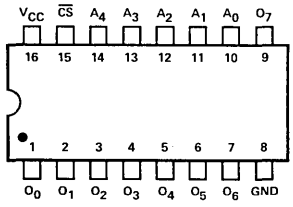
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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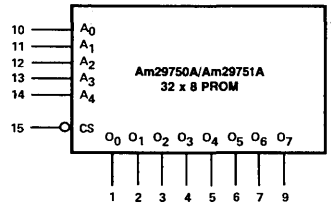
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am29750AXC, Am29751AXC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am29750AXM, Am29751AXM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am29751A only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}					0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V				−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					25	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC} (Am29751A only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)			−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.				90	115	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX. $V_{\overline{CS}}$ = 2.4V	Am29751A only	V_O = 4.5V			40	µA
				V_O = 2.4V			40	
				V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)				4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)				8		pF

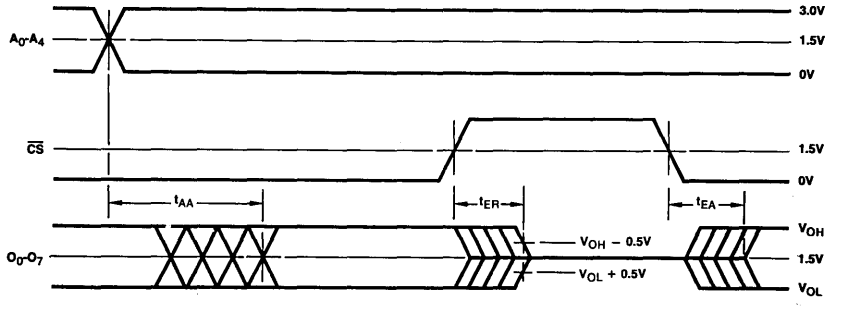
Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but periodically sampled.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE
PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ. 5V 25°C	Max. 5V 25°C	Max. COM'L	Max. MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1–3)	25	35	40	50	ns
t_{EA}	Enable Access Time		15	20	25	30	ns
t_{ER}	Enable Recovery Time		15	20	25	30	ns

Notes: 1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

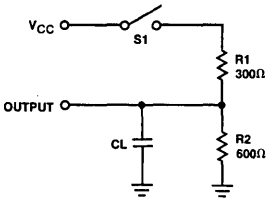
MPR-272

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
▨	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
⋈	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOAD



MPR-273

PROGRAMMING

The Am29750A and Am29751A are manufactured with conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}$ input is at a logic HIGH. Current is gated through the address fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

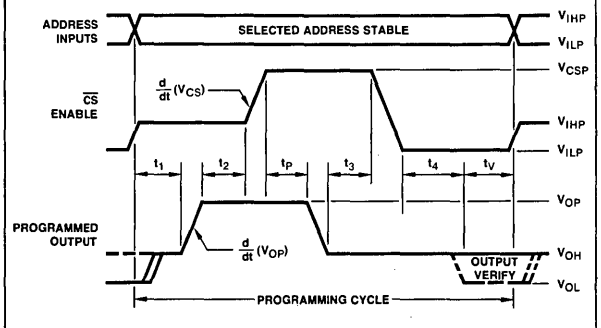
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	CS Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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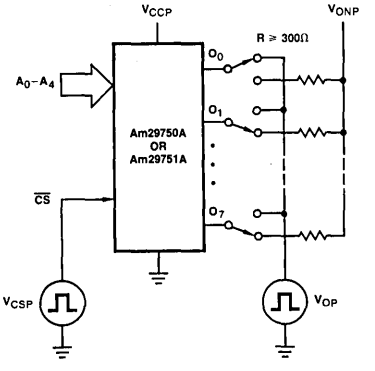
SIMPLIFIED PROGRAMMING DIAGRAM



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PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am29750A • Am29751A ADAPTERS AND CONFIGURATOR	715-1407-1	PA16-2 and 32 x 8 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 32 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output O_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

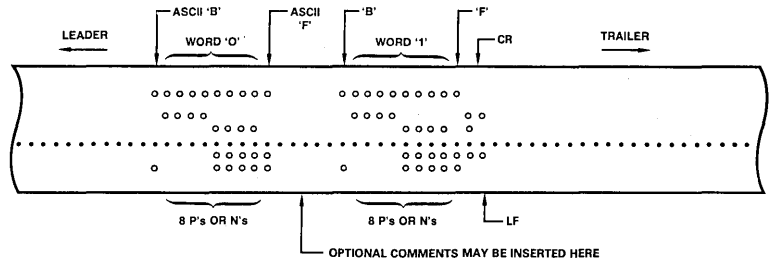
```
ØØØ   BPNPPNNNPF   WORD ZERO (R) (L)
      BPPPPPPNNF   COMMENT FIELD (R) (L)
Ø02   BNNNPPPPNF   ANY (R) (L)
      BNNNNNNNNF   TEXT (R) (L)
Ø04   BPNNNNNNPF   CAN (R) (L)
      BNPPNPPNNF   GO (R) (L)
Ø06   BPNNPPPNNF   HERE (R) (L)
 :    ..........    :
Ø31   BNNNNPPPNF   END (R) (L)

(R) = CARRIAGE RETURN
(L) = LINE FEED
```

RESULTING DEVICE TRUTH TABLE ($\overline{CS}$ = LOW)

A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	H	H	L	H	L	L	H	H	H	L	L
		⋮						⋮				
H	H	H	H	H	L	L	L	L	H	H	H	L

ASCII PAPER TAPE



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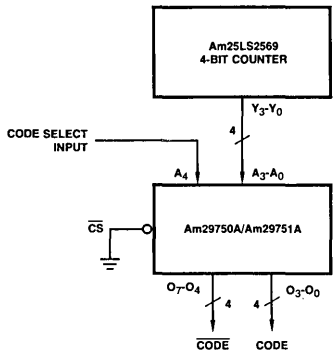
APPLYING THE Am29750A AND Am29751A

The Am29750A and Am29751A PROMs may be used as code converters. Examples include conversion of hexadecimal, octal or BCD to seven segment display drive format. In many code conversion applications an extra PROM address input is available and may be used as a polarity control, blanking control or code selector input. The use of a single Am29750A or Am29751A to convert the outputs of a binary counter to either excess three or gray code format is illustrated below. In this case both codes are generated in true and complemented form simultaneously.



TRUTH TABLE

ADDRESS					COMPLEMENT				TRUE				
A_4	A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	0	0	0	1	1	0	0	0	0	1	1	EXCESS THREE CODE
0	0	0	0	1	1	0	1	1	0	1	0	0	
0	0	0	1	0	1	0	1	0	0	1	0	1	
0	0	0	1	1	1	0	0	1	0	1	1	0	
0	0	1	0	0	1	0	0	0	0	1	1	1	
0	0	1	0	1	0	1	1	1	1	0	0	0	
0	0	1	1	0	0	1	1	0	1	0	0	1	
0	0	1	1	1	0	1	0	1	1	0	1	0	
0	1	0	0	0	0	1	0	0	1	0	1	1	
0	1	0	0	1	0	0	1	1	1	1	0	0	
0	1	0	1	0	X	X	X	X	X	X	X	X	
0	1	0	1	1	X	X	X	X	X	X	X	X	
0	1	1	0	0	X	X	X	X	X	X	X	X	
0	1	1	0	1	X	X	X	X	X	X	X	X	
0	1	1	1	0	X	X	X	X	X	X	X	X	
0	1	1	1	1	X	X	X	X	X	X	X	X	
1	0	0	0	0	1	1	1	1	0	0	0	0	GRAY CODE
1	0	0	0	1	1	1	1	0	0	0	0	1	
1	0	0	1	0	1	1	0	0	0	0	1	1	
1	0	0	1	1	1	1	0	1	0	0	1	0	
1	0	1	0	0	1	0	0	1	0	1	1	0	
1	0	1	0	1	1	0	0	0	0	1	1	1	
1	0	1	1	0	1	0	1	0	0	1	0	1	
1	0	1	1	1	1	0	1	1	0	1	0	0	
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1	1	0	0	1	0	0	1	0	1	1	0	1	
1	1	0	1	0	0	0	0	0	1	1	1	1	
1	1	0	1	1	0	0	0	1	1	1	1	0	
1	1	1	0	0	0	1	0	1	1	0	1	0	
1	1	1	0	1	0	1	0	0	1	0	1	1	
1	1	1	1	0	0	1	1	0	1	0	0	1	
1	1	1	1	1	0	1	1	1	1	0	0	0	

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ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Open Collector Order Number	Three-State Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM29750ADC	AM29751ADC	D-16	C	C-1
AM29750ADC-B	AM29751ADC-B	D-16	C	B-1
AM29750ADM	AM29751ADM	D-16	M	C-3
AM29750ADM-B	AM29751ADM-B	D-16	M	B-3
AM29750AFM	AM29751AFM	F-16	M	C-3
AM29750AFM-B	AM29751AFM-B	F-16	M	B-3

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am29760A • Am29761A

1024 Bit Generic Series Bipolar PROM

PRELIMINARY DATA

DISTINCTIVE CHARACTERISTICS

- High Speed – 45ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

GENERIC SERIES CHARACTERISTICS

The Am29760A and Am29761A are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

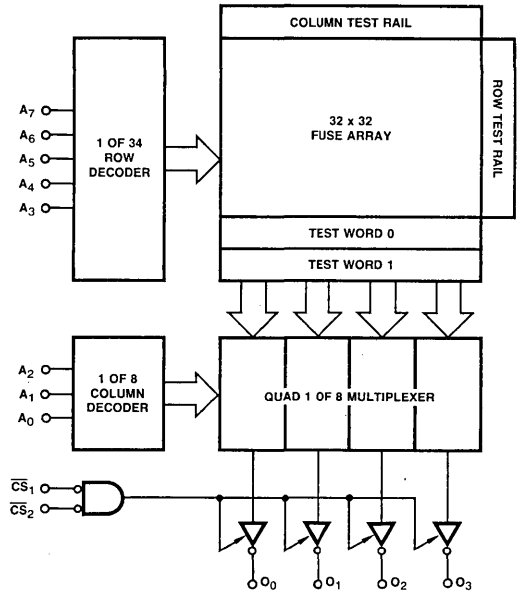
Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliabilty. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

FUNCTIONAL DESCRIPTION

The Am29760A and Am29761A are high speed electrically programmable Schottky read only memories. Organized in the industry standard 256 x 4 configuration, they are available in both open collector Am29760A and three-state Am29761A output versions. After programming, stored information is read on outputs O_0–O_3 by applying unique binary addresses to A_0–A_7 and holding the chip select inputs, $\overline{CS}_1$ and $\overline{CS}_2$, at a logic LOW. If either chip select input goes to a logic HIGH, O_0–O_3 go to the off or high impedance state.

BLOCK DIAGRAM



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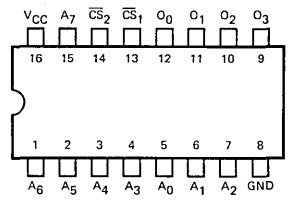
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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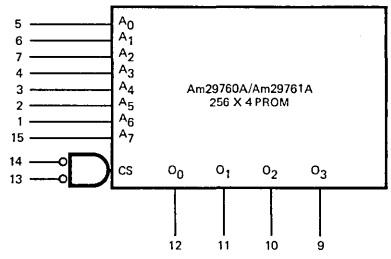
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am29760AXC, Am29761AXC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am29760AXM, Am29761AXM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am27S21 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC} (Am27S21 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		95	130	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS1}}$ = 2.4V; Am29761A only; V_O = 4.5V			40	µA
		V_{CC} = MAX., $V_{\overline{CS1}}$ = 2.4V; Am29761A only; V_O = 2.4V			40	µA
		V_{CC} = MAX., $V_{\overline{CS1}}$ = 2.4V; Am29761A only; V_O = 0.4V			−40	µA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		pF

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C

2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

3. These parameters are not 100% tested, but are periodically sampled.

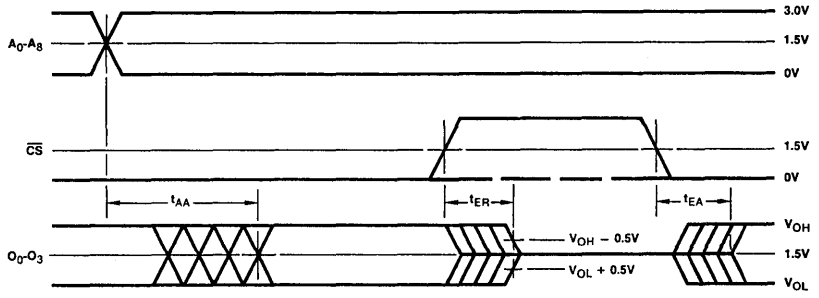
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ. 5V 25°C	Max. 5V 25°C	Max. COM'L	Max. MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1–3)	25	35	45	60	ns
t_{EA}	Enable Access Time		15	18	20	30	ns
t_{ER}	Enable Recovery Time		15	18	20	30	ns

Notes: 1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} – 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



Note: Level on output while either $\overline{CS}$ is HIGH is determined externally.

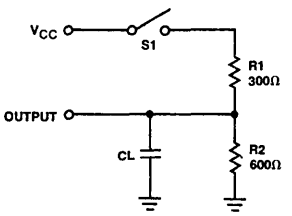
MPR-281

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC TEST LOAD



MPR-282

PROGRAMMING

The Am29760A and Am29761A are manufactured with conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}_1$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

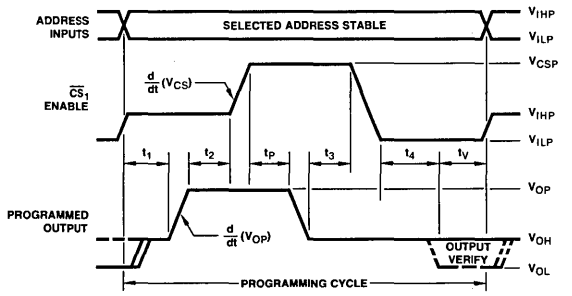
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	$\overline{CS}_1$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of $\overline{CS}_1$, Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes: 1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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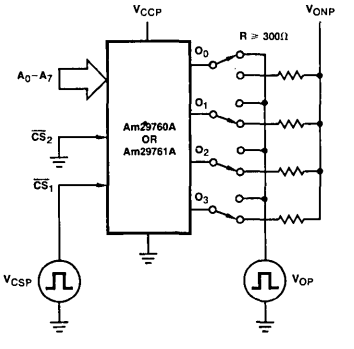
SIMPLIFIED PROGRAMMING DIAGRAM



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PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am29760A • Am29761A ADAPTERS AND CONFIGURATOR	715-1408-1	PA16-1 and 256 x 4 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 256 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of four Ps or Ns, starting with output O_3.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the four Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

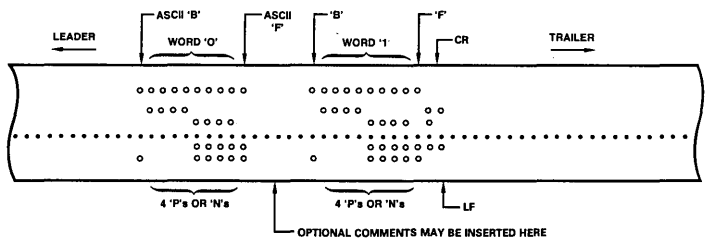
TYPICAL PAPER TAPE FORMAT

```
ØØØ   BNNNPF   WORD ZERO (R) (L)
      BPPNNF   COMMENT FIELD (R) (L)
ØØ2   BPPPNF   ANY (R) (L)
      BNNNNF   TEXT (R) (L)
ØØ4   BNNNPF   CAN (R) (L)
      BPPNNF   GO (R) (L)
ØØ6   BPPNNF   HERE (R) (L)
 .      .       .
 .      .       .
255   BPPPNF   END (R) (L)
```

RESULTING DEVICE TRUTH TABLE ($\overline{CS_1}$ & $\overline{CS_2}$ = LOW)

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_3	O_2	O_1	O_0
L	L	L	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	H	H	H	L	L
L	L	L	L	L	L	H	L	H	H	H	L
L	L	L	L	L	L	H	H	L	L	L	L
L	L	L	L	L	H	L	L	L	L	L	H
L	L	L	L	L	H	L	H	H	H	L	L
L	L	L	L	L	H	H	L	H	H	L	L
				⋮					⋮		
H	H	H	H	H	H	H	H	H	H	H	L

ASCII PAPER TAPE



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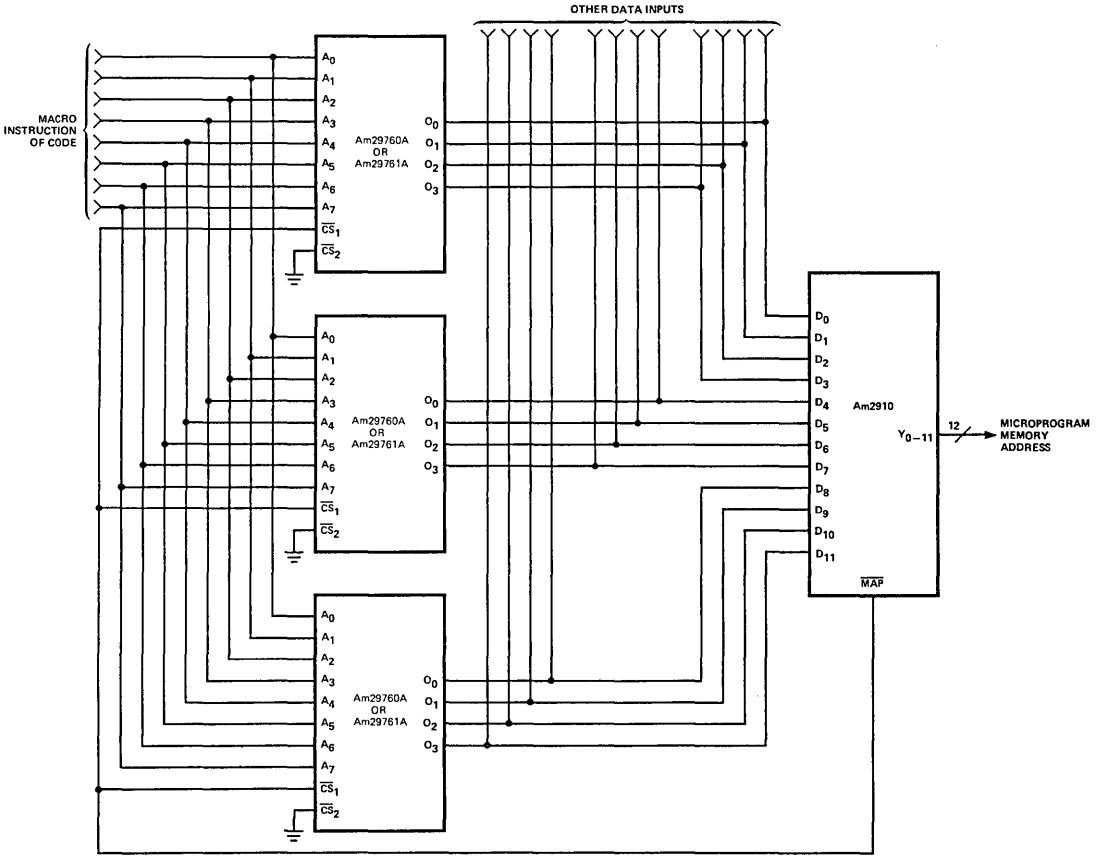
APPLYING THE Am29760A/61A

Typical application of the Am29760A/61A is shown below. The Am29760A/61A's are employed as mapping ROMs in a microprogram computer control unit. The eight-bit macroinstruction from main memory is brought into the A_{0-7} inputs of the mapping ROM array. The instruction is mapped into a 12-bit address space with each PROM output supplying 4 bits. The 12 bits of address are then supplied to the "D" inputs of the Am2910 as a possible next address source for microprogram memory. The $\overline{MAP}$ output of the Am2910 is connected to the $\overline{CS}_1$ input of the Am29760A/61A such that when the $\overline{CS}_1$ input is HIGH, the outputs of the PROMs are either HIGH in the case of the Am29760A or in the three-state mode in the case of the Am29761A. In both cases the $\overline{CS}_2$ input is grounded, thus data from other sources are free to drive the D inputs of the Am2910 when $\overline{MAP}$ is HIGH.



MICROPROGRAMMING INSTRUCTION MAPPING

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ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Open Collector Order Number	Three-State Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM29760ADC	AM29761ADC	D-16	C	C-1
AM29760ADC-B	AM29761ADC-B	D-16	C	B-1
AM29760ADM	AM29761ADM	D-16	M	C-3
AM29760ADM-B	AM29761ADM-B	D-16	M	B-3
AM29760AFM	AM29761AFM	F-16	M	C-3
AM29760AFM-B	AM29761AFM-B	F-16	M	B-3

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am29770 • Am29771

2048-Bit Generic Series Bipolar PROM

PRELIMINARY DATA

DISTINCTIVE CHARACTERISTICS

- High Speed – 50ns max commercial range access time
- Excellent performance over full MIL and commercial ranges
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three-state outputs
- Fast chip select
- Access time tested with N^2 patterns
- Pin for pin replacements for industry standard products
- Common Generic PROM series electrical characteristics and simple programming procedures.

GENERIC SERIES CHARACTERISTICS

The Am29770 and Am29771 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

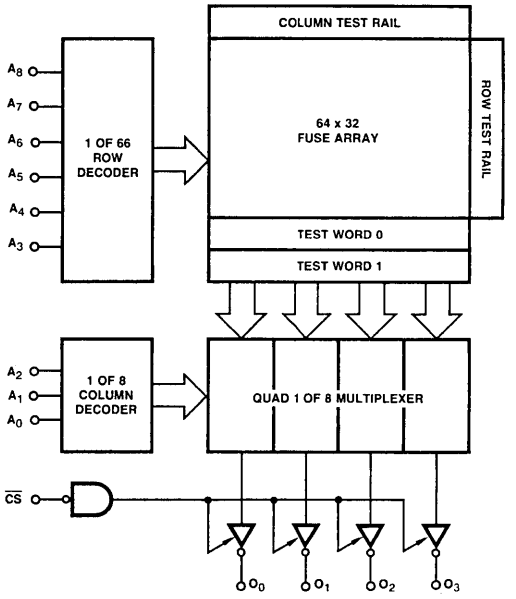
Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

FUNCTIONAL DESCRIPTION

The Am29770 and Am29771 are high speed electrically programmable Schottky read only memories. Organized in the industry standard 512 x 4 configuration, they are available in both open collector Am29770 and three-state Am29771 output versions. After programming, stored information is read on outputs O_0-O_3 by applying unique binary addresses to A_0-A_8 and holding the chip select input, $\overline{CS}$, at a logic LOW. If the chip select input goes to a logic HIGH, O_0-O_3 go to the off or high impedance state.

BLOCK DIAGRAM



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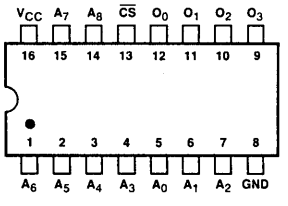
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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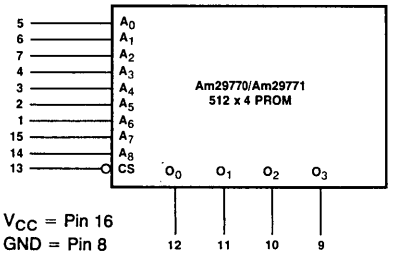
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am29770XC, Am29771XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am29770XM, Am29771XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am29771 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC} (Am29771 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		100	130	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am29771 only; V_O = 4.5V			40	µA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am29771 only; V_O = 2.4V			40	µA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; Am29771 only; V_O = 0.4V			−40	µA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		pF

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

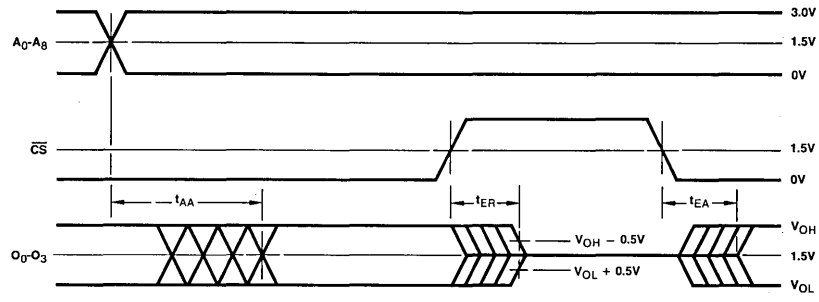
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	Typ. 5V 25°C	Max. 25°C	Max. COM'L	Max. MIL	Units
t_{AA}	Address Access Time	AC Test Load (See Notes 1-3)	30	45	50	60	ns
t_{EA}	Enable Access Time		15	20	25	30	ns
t_{ER}	Enable Recovery Time		15	20	25	30	ns

Notes: 1. t_{AA} is tested with switch S_1 closed and C_L = 30pF.
2. For open collector outputs, t_{EA} and t_{ER} are tested with S_1 closed to the 1.5V output level. C_L = 30pF.
3. For three state outputs, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH} − 0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL} + 0.5V level.

SWITCHING WAVEFORMS



Note: Level on output while $\overline{CS}$ is HIGH is determined externally.

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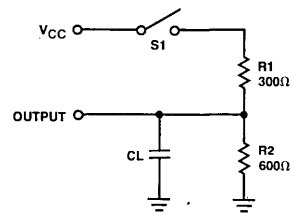
KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS	WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY	▨	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
▨	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L	⋈	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE
▨	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H			

AC TEST LOAD



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PROGRAMMING

The Am29770 and Am29771 are manufactured with conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. To program the device, the fusible links are selectively opened.

The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to one memory output after the $\overline{CS}$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{CS}$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip enabled, and the output level sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{CS}$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

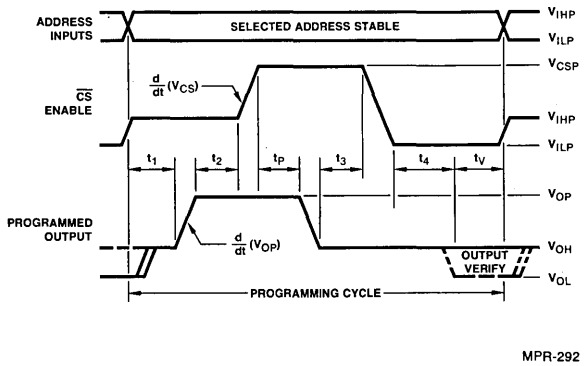
When all programming has been completed, the data content of the memory should be verified by sequentially reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{CSP}	CS Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{CS})/dt$	Rate of CS Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1, t_2, t_3 and t_4 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



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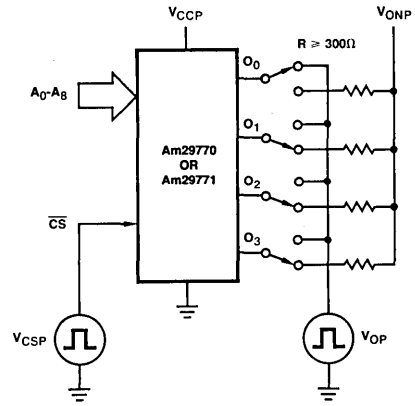
SIMPLIFIED PROGRAMMING DIAGRAM



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PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am29770 • Am29771 ADAPTERS AND CONFIGURATOR	715-1408-2	PA16-1 and 512 x 4 (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 512 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of four Ps or Ns, starting with output O_3.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the four Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

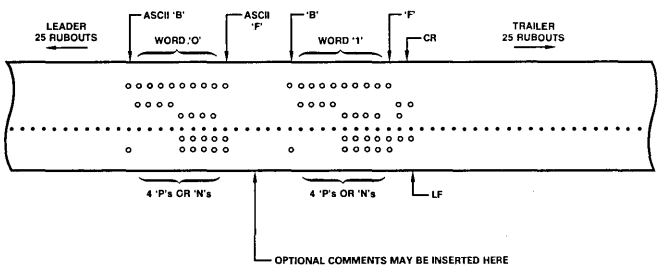
TYPICAL PAPER TAPE FORMAT

```
øøø   BNNNPFF   WORD ZERO (R) (L)
      BPPNNF    COMMENT FIELD (R) (L)
øø2   BPPPNF    ANY (R) (L)
      BNNNNF    TEXT (R) (L)
øø4   BNNNPF    CAN (R) (L)
      BPPNNF    GO (R) (L)
øø6   BPPNNF    HERE (R) (L)
 :     :::::     :
511   BPPPNF    END (R) (L)
```

RESULTING DEVICE TRUTH TABLE ($\overline{CS}$ = LOW)

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_3	O_2	O_1	O_0
L	L	L	L	L	L	L	L	L	L	L	L	H
L	L	L	L	L	L	L	L	H	H	H	L	L
L	L	L	L	L	L	L	H	L	H	H	H	L
L	L	L	L	L	L	L	H	H	L	L	L	L
L	L	L	L	L	L	H	L	L	L	L	L	H
L	L	L	L	L	L	H	L	H	H	H	L	L
L	L	L	L	L	L	H	H	L	H	H	L	L
					⋮							
H	H	H	H	H	H	H	H	H	H	H	H	L

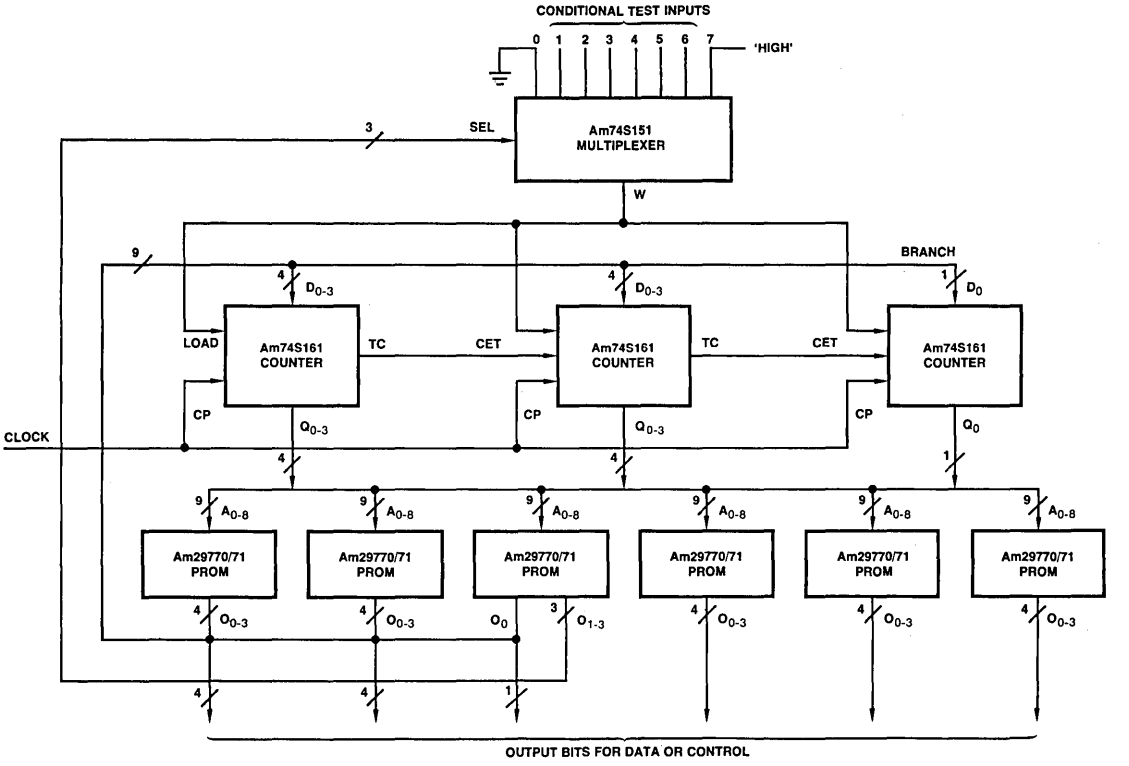
ASCII PAPER TAPE



MPR-294

APPLYING THE Am29770 AND Am29771

The Am29770 and Am29771 can be used with a high speed counter to form a pico-controller for microprogrammed systems. A typical application is illustrated below wherein a multiplexer, under control of one of the PROMs, is continuously sensing the CONDITIONAL TEST INPUTS. When the selected condition occurs, a HIGH signal will result at the multiplexer output causing a predetermined branch address to be loaded into the parallel inputs of the counters on the next clock pulse. The counter then accesses the preprogrammed data or control information sequence from the PROMs.



MPR-295

ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Open Collector Order Number	Three-State Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM29770DC	AM29771DC	D-16	C	C-1
AM29770DC-B	AM29771DC-B	D-16	C	B-1
AM29770DM	AM29771DM	D-16	M	C-3
AM29770DM-B	AM29771DM-B	D-16	M	B-3
AM29770FM	AM29771FM	F-16	M	C-3
AM29770FM-B	AM29771FM-B	F-16	M	B-3

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am29774 • Am29775

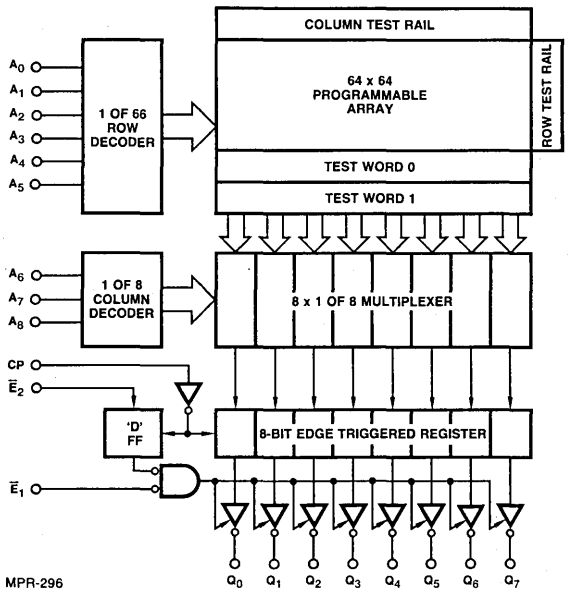
4096-Bit Generic Series Bipolar PROM with Register

PRELIMINARY DATA

DISTINCTIVE CHARACTERISTICS

- On chip edge triggered registers – Ideal for pipelined microprogrammed systems
- Versatile synchronous and asynchronous enables for simplified word expansion
- Predetermined OFF outputs on power-up
- Fast 50ns address setup and 20ns clock to output times
- Excellent performance over the military range
- Performance pretested with N^2 patterns
- Space saving 22 pin package
- Highly reliable, ultra-fast programming Platinum-Silicide fuses
- High programming yield
- Low current PNP inputs
- High current open collector and three state outputs
- Common Generic PROM Series characteristics and programming procedures

BLOCK DIAGRAM



MPR-296

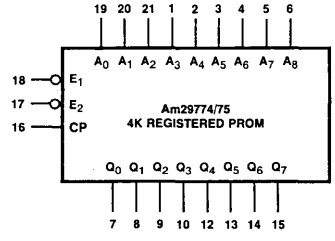
FUNCTIONAL DESCRIPTION

The Am29774 and Am29775 are electrically programmable Schottky TTL read only memories incorporating true D-type, master-slave data registers on chip. These devices feature the versatile 512 word by 8 bit organization and are available in both the open collector Am29774 and three-state Am29775 output versions. Designed to optimize system performance, these devices also substantially reduce the cost of pipelined microprogrammed systems and other designs wherein accessed PROM data is temporarily stored in a register. The Am29774 and Am29775 also offer maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables.

When V_{CC} power is first applied, the synchronous enable ($\overline{E}_2$) flip-flop will be in the set condition causing the outputs, Q_0-Q_7, to be in the OFF or high impedance state, eliminating the need for a register clear input. Reading data is accomplished by first applying the binary word address to the address inputs, A_0-A_8, and a logic LOW to the synchronous output enable, $\overline{E}_2$. During the address setup time, stored data is accessed and loaded into the master flip-flops of the data register. Since the synchronous enable setup time is less than the address setup requirement, additional decoding delays may occur in the enable path without reducing memory performance. Upon the next LOW-to-HIGH transition of the clock, CP, data is transferred to the slave flip-flops which drive the output buffers. Providing the asynchronous enable, $\overline{E}_1$, is also LOW, stored data will appear on the outputs, Q_0-Q_7. If $\overline{E}_2$ is HIGH when the positive clock edge occurs, outputs go to the OFF or high impedance state. The outputs may be disabled at any time by switching $\overline{E}_1$ to a HIGH level. Following the positive clock edge, the address and synchronous enable inputs are free to change; changes do not affect the ouputs until another positive clock edge occurs. This unique feature allows the PROM decoders and sense amplifiers to access the next location while previously addressed data remains stable on the outputs. For less complex applications either enable may be effectively eliminated by tying it to ground.

The on-chip, edge triggered register simplifies system timing since the PROM clock may be derived directly from system clock without introducing dangerous race conditions. Other register timing requirements are similar to those of standard Schottky registers and are easily implemented.

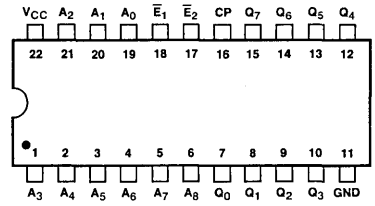
LOGIC SYMBOL



V_{CC} = Pin 22
GND = Pin 11

MPR-297

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-298

GENERIC SERIES CHARACTERISTICS

The Am29974 and Am29775 are members of an Advanced PROM series incorporating common electrical characteristics and programming procedures. All parts in this series are produced with a fusible link at each memory location storing a logic LOW and can be selectively programmed to a logic HIGH by applying appropriate voltages to the circuit.

All parts are fabricated with AMD's fast programming highly reliable Platinum-Silicide Fuse technology. Utilizing easily implemented programming (and common programming personality card sets) these products can be rapidly programmed to any customized pattern. Extra test words are pre-programmed during manufacturing to insure extremely high field programming yields, and produce excellent parametric correlation.

Platinum-Silicide was selected as the fuse link material to achieve a well controlled melt rate resulting in large non-conductive gaps that ensure very stable long term reliability. Extensive operating testing has proven that this low-field, large-gap technology offers the best reliability for fusible link PROMs.

Common design features include active loading of all critical AC paths regulated by a built-in temperature and voltage compensated bias network to provide excellent parametric performance over MIL supply and temperature ranges. Selective feedback techniques have been employed to minimize delays through all critical paths producing the fastest speeds possible from Schottky processed PROMs.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs (Except During Programming)	−0.5V to +V_{CC} max.
DC Voltage Applied to Outputs During Programming	21V
Output Current into Outputs During Programming (Max. Duration of 1 sec.)	200mA
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	AM29774XC, AM29775XC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	AM29774XM, AM29775XM	T_C = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions			Min.	Typ. (Note 1)	Max.	Units
V_{OH} (Am29775 only)	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}			2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}				0.38	0.50	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V				−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC} (Am29775 only)	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)			−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.				125	185	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX. VE_1 = 2.4V		V_O = 4.5V			100	μA
			Am29775 only	V_O = 2.4V			40	
				V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)				8.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)				12		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.

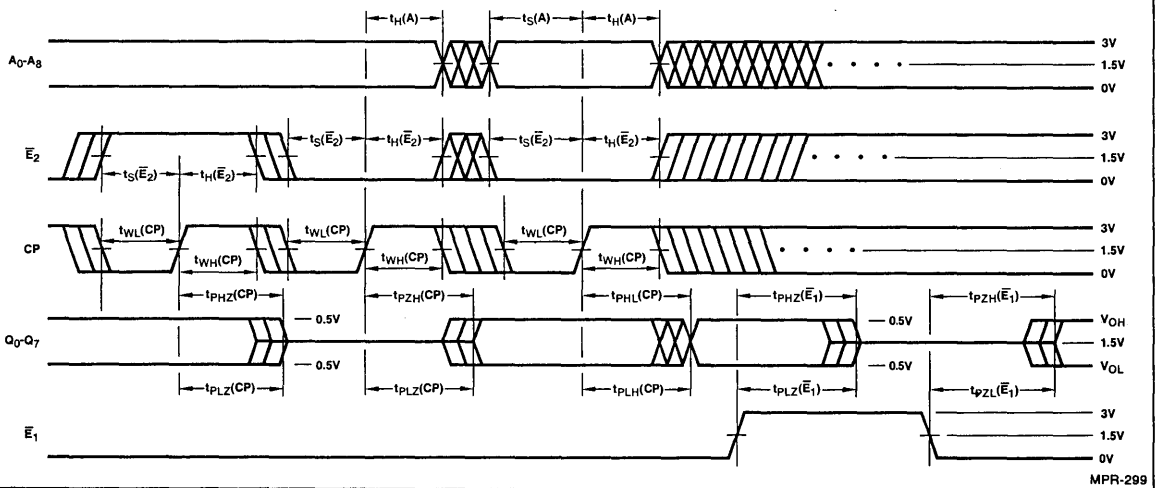
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

PRELIMINARY DATA

Parameter	Description	Test Conditions	T_A= 25°C, V_{CC} = 5.0V Typ.	Min.	Max.	COM'L Min.	COM'L Max.	MIL Min.	MIL Max.	Units
$t_S(A)$	Address to CP (HIGH) Setup Time	C_L = 30pF, S_1 closed. (See AC Test Load below)	40	50						ns
$t_H(A)$	Address to CP (HIGH) Hold Time		−15	0						ns
$t_{PHL}(CP)$ $t_{PLH}(CP)$	Delay from CP (HIGH) to Output (HIGH or LOW)		15		20					ns
$t_{WH}(CP)$ $t_{WL}(CP)$	CP Width (HIGH or LOW)		10	20						ns
$t_S(\overline{E}_2)$	$\overline{E}_2$ to CP (HIGH) Setup Time		10	20						ns
$t_H(\overline{E}_2)$	$\overline{E}_2$ to CP (HIGH) Hold Time		−10	0						ns
$t_{PZL}(CP)$ $t_{PZH}(CP)$	Delay from CP (HIGH) to Active Output (HIGH or LOW) (Note 1)	C_L = 30pF, S_1 closed for t_{PZL} and open for t_{PZH}	15		25					ns
$t_{PZL}(\overline{E}_1)$ $t_{PZH}(\overline{E}_1)$	Delay from $\overline{E}_1$ (LOW) to Active Output (HIGH or LOW) (Note 1)		15		30					ns
$t_{PLZ}(CP)$ $t_{PHZ}(CP)$	Delay from CP (HIGH) to Inactive Output (OFF or high Impedance)(Note 1)	C_L = 5pF (Note 2), S_1 closed for t_{PLZ} and open for t_{PHZ}	15		25					ns
$t_{PLZ}(\overline{E}_1)$ $t_{PHZ}(\overline{E}_1)$	Delay from $\overline{E}_1$ (HIGH) to Inactive Output (OFF or high Impedance)(Note 1)		10		20					ns

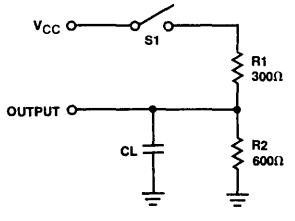
Notes: 1. t_{PHZ} and t_{PZH} apply to the three-state Am29775 only.
2. t_{PHZ} and t_{PLZ} are measured to the V_{OH} − 0.5V and V_{OL} + 0.5V output levels respectively. All other switching parameters are tested from and to the 1.5V threshold levels.
3. Tests are performed with input 10% to 90% rise and fall times of 5ns or less.

SWITCHING WAVEFORMS



MPR-299

AC TEST LOAD



MPR-300

KEY TO TIMING DIAGRAM

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

PROGRAMMING

The Am29774 and Am29775 are manufactured with a conductive Platinum-Silicide link at each bit location. The output of the memory with the link in place is LOW. The fusible links are opened one at a time by passing current through them from a 20 volt supply which is applied to the memory output after the $\overline{E}_1$ input is at a logic HIGH. Current is gated through the addressed fuse by raising the $\overline{E}_1$ input from a logic HIGH to 15 volts. After 50 μsec, the 20 volt supply is removed, the chip is enabled and the CP input is clocked. Each data verification attempt must be preceded by a positive going (LOW-to-HIGH) clock edge to load the array data into the on-chip register. The output level is then sensed to determine if the link has opened. Most links will open within 50 μsec. Occasionally a link will be stronger and require additional programming cycles. The recommended duration of additional programming periods is 5 msec. If a link has not opened after a total elapsed programming time of 400 msec, further programming of the device should not be attempted. Successive links are programmed in the same manner until all desired bit locations have been programmed to the HIGH level.

Typical current into an output during programming will be approximately 140mA until the fuse link is opened, after which the current drops to approximately 40mA. Current into the $\overline{E}_1$ pin when it is raised to 15 volts is typically 1.5mA.

The memories may become hot during programming due to the large currents being passed. Programming cycles should not be continuously applied to one device more than 5 seconds to avoid heat damage. If this programming time is exceeded, all power to the chip including V_{CC} should be removed for a period of 5 seconds after which programming may be resumed.

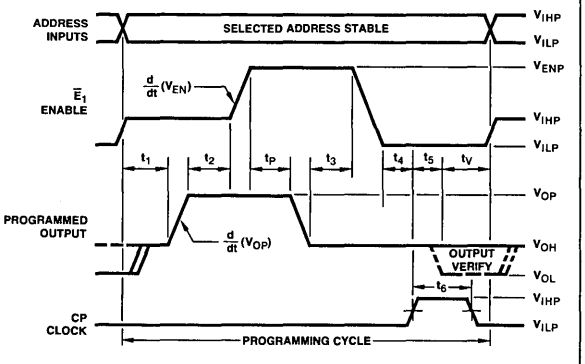
When all programming has been completed, the data content of the memory should be verified by clocking and reading all words. Occasionally this verification will show that an extra undesired link has been fused. Should this occur, immediately check the programming equipment to make sure that all device pins are firmly contacting the programming socket, that the input signal levels exhibit sufficient noise margins, and that the programming voltages are within the specified limits. All of these conditions must be maintained during programming. AMD PROMs are thoroughly tested to minimize unwanted fusing; fusing extra bits is generally related to programming equipment problems.

PROGRAMMING PARAMETERS

Parameter	Description	Min.	Max.	Units
V_{CCP}	V_{CC} During Programming	5.0	5.5	Volts
V_{IHP}	Input HIGH Level During Programming	2.4	5.5	Volts
V_{ILP}	Input LOW Level During Programming	0.0	0.45	Volts
V_{ENP}	$\overline{E}_1$ Voltage During Programming	14.5	15.5	Volts
V_{OP}	Output Voltage During Programming	19.5	20.5	Volts
V_{ONP}	Voltage on Outputs Not to be Programmed	0	V_{CCP}+0.3	Volts
I_{ONP}	Current into Outputs Not to be Programmed		20	mA
$d(V_{OP})/dt$	Rate of Output Voltage Change	20	250	V/μsec
$d(V_{EN})/dt$	Rate of $\overline{E}_1$ Voltage Change	100	1000	V/μsec
t_P	Programming Period – First Attempt	50	100	μsec
	Programming Period – Subsequent Attempts	5.0	15	msec

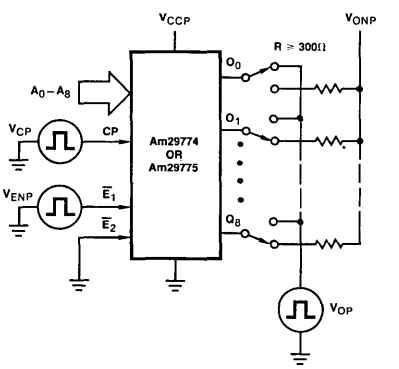
Notes:
1. All delays between edges are specified from completion of the first edge to beginning of the second edge; i.e., not to the midpoints.
2. Delays t_1 through t_6 must be greater than 100 ns; maximum delays of 1 μsec are recommended to minimize heating during programming.
3. During t_V, a user defined period, the output being programmed is switched to the load R and read to determine if additional pulses are required.
4. Outputs not being programmed are connected to V_{ONP} through resistor R which provides output current limiting.

PROGRAMMING WAVEFORMS



MPR-301

SIMPLIFIED PROGRAMMING DIAGRAM



MPR-302

PROGRAMMING EQUIPMENT

Generic programming boards and device adapters are available from the sources listed below. In each case, the programming boards are used in these manufacturer's automatic programmers to program all AMD generic series bipolar PROMs; individual adapters are required for each basic part type in the series.

SOURCE AND LOCATION	Data I/O Corp. P.O. Box 308 Issaquah, Wash. 98027	Pro-Log Corp. 2411 Garden Road Monterey, Ca. 93940
PROGRAMMER MODEL(S)	Model 5, 7 and 9	M900 and M920
AMD GENERIC BIPOLAR PROM PERSONALITY BOARD	909-1286-1	PM9058
Am29774 • Am29775 ADAPTERS AND CONFIGURATOR	715-1412-2	PA22-4 and 512 x 8 w/Register (L)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, however, much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ASCII BPNF

An example of an ASCII tape in the BPNF format is shown below. They can be punched on any Teletype® or on a TWX or Telex machine. The format chosen provides relatively good error detection. Paper tapes must consist of:

1. A leader of at least 25 rubouts.
2. The data patterns for all 512 words, starting with word 0, in the following format:
   a. Any characters, including carriage return and line feed, except "B".
   b. The letter "B", indicating the beginning of the data word.
   c. A sequence of eight Ps or Ns, starting with output Q_7.
   d. The letter "F", indicating the finish of the data word.
   e. Any text, including carriage return and line feed, except the letter "B".
3. A trailer of at least 25 rubouts.

A P is a HIGH logic level = 2.4 volts.
An N is a LOW logic level = 0.4 volts.

A convenient pattern to use for the data words is to prefix the word (or every few words) with the word number, then type the data word, then a comment, then carriage return and line feed as shown below. There must be no characters between the B and the F except for the eight Ps and Ns. If an error is made in a word, the entire word must be cancelled with rubouts back to the letter B, then the word re-typed beginning with the B.

When TWXing your tape, be sure the tape is in even parity. Parity is not necessary if the tape is mailed.

TYPICAL PAPER TAPE FORMAT

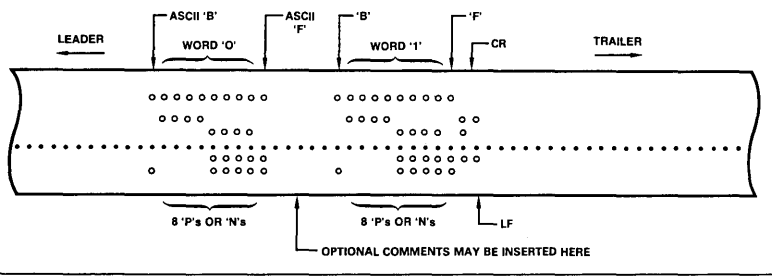
```
øøø   BPNPPNNNPF   WORD ZERO (R) (L)
      BPPPPPPNNF   COMMENT FIELD (R) (L)
øø2   BNNNPPPPNF   ANY (R) (L)
      BNNNNNNNNF   TEXT (R) (L)
øø4   BPNNNNNNPF   CAN (R) (L)
      BNPPNPPNNF   GO (R) (L)
øø6   BPNNPPPNNF   HERE (R) (L)
 :    ..........    :
511   BNNNNPPPNF   END (R) (L)
```

(R) = CARRIAGE RETURN
(L) = LINE FEED

RESULTING DEVICE TRUTH TABLE ($\overline{E}_1$ AND $\overline{E}_2$ LOW)

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
L	L	L	L	L	L	L	L	L	H	L	H	H	L	L	L	H
L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	L
L	L	L	L	L	L	L	H	L	L	L	L	H	H	H	H	L
L	L	L	L	L	L	L	H	H	L	L	L	L	L	L	L	L
L	L	L	L	L	L	H	L	L	H	L	L	L	L	L	L	H
L	L	L	L	L	L	H	L	H	L	H	H	L	H	H	L	L
L	L	L	L	L	L	H	H	L	H	L	L	H	H	H	L	L
				⋮								⋮				
H	H	H	H	H	H	H	H	H	L	L	L	L	H	H	H	L

ASCII PAPER TAPE



MPR-303

APPLYING THE Am29774 AND Am29775 IN BIPOLAR MICROCOMPUTERS

With the advent of the Am2901 and Am2903 4-bit microprocessor slices, the Am2910 bipolar microprogram sequencer and the Am29774/75 registered PROM, the design engineer can upgrade the performance of existing systems or implement new system taking advantage of the latest state-of-the-art technology in Low-Power Schottky integrated circuits. These devices, however, utilize a new concept in machine design not familar to many design engineers. This technique is called microprogramming.

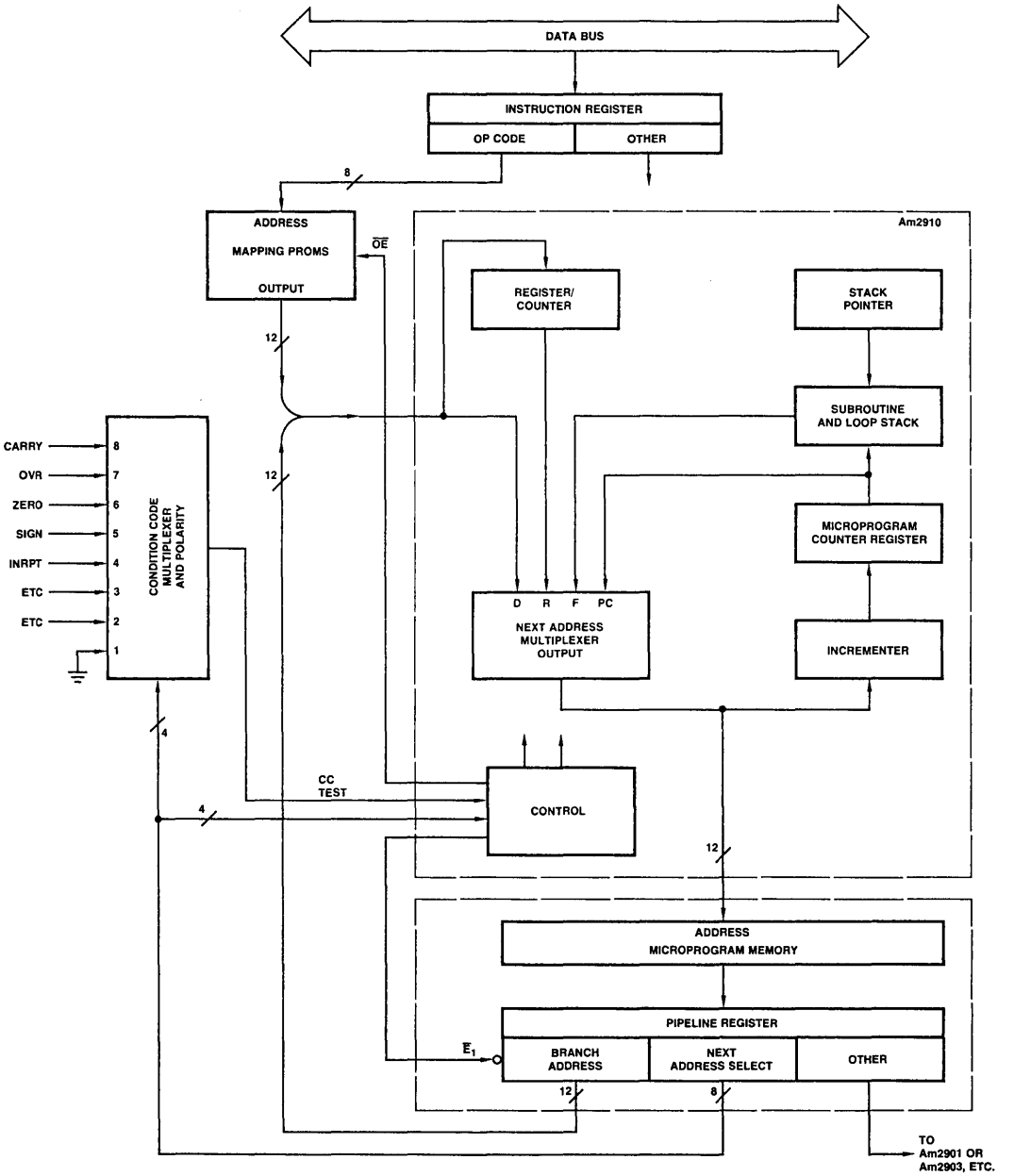


Figure 1. A Typical Computer Control Unit using the Am29774/75.

MPR-304

APPLYING THE Am29774 AND Am29775 IN BIPOLAR MICROCOMPUTERS (Cont.)

Basically, a microprogrammed machine is one in which a coherent sequence of microinstructions is used to execute various commands required by the machine. If the machine is a computer, each sequence of microinstructions can be made to execute a machine instruction. All of the little elemental tasks performed by the machine in executing the machine instruction are called microinstructions. The storage area for these microinstructions is usually called the microprogram memory.

A microinstruction usually has two primary parts. These are: (1) the definition and control of all elemental micro-operations to be carried out and (2) the definition and control of the address of the next microinstruction to be executed.

The definition of the various micro-operations to be carried out usually includes such things as ALU source operand selection, ALU function, ALU destination, carry control, shift control, interrupt control, data-in and data-out control, and so forth. The definition of the next microinstruction function usually includes identifying the source selection of the next microinstruction address and, in some cases, supplying the actual value of that microinstruction address.

Microprogrammed machines are usually distinquished from non-microprogrammed machines in the following manner. Older, non-microprogrammed machines implemented the control function by using combinations of gates and flip-flops connected in a somewhat random fashion in order to generate the required timing and control signals for the machine. Microprogrammed machines, on the other hand, are normally considered highly ordered, particularly with regard to the control function field, and use high speed PROM's for control definition. In its simplest definition, a microprogram control unit consists of the microprogram memory and the structure required to determine the address of the next microinstruction

The microprogram memory control unit block diagram of Figure 1 is easily implemented using the Am2910 and the Am29774/75 registered PROM's. This architecture provides a structured state machine design capable of executing many highly sophisticated next address control instructions. The Am2910 contains a next address multiplexer that provides four different inputs from which the address of the next microinstruction can be selected. These are the direct input (D), the register input (R), the program counter (PC), and the file (F). The starting address decoder (mapping PROM) output and the Am29774/75's pipeline register output are connected together at the D input to the Am2910 and are operated in the three-state mode.

The architecture of Figure 1 shows an instruction register capable of being loaded with a machine instruction word from the data bus. The op code portion of the instruction is decoded using a mapping PROM to arrive at a starting address for the microinstruction sequence required to execute the machine instruction. When the microprogram memory address is to be the first microinstruction of the machine instruction sequence, the Am2910 next address control selects the multiplexer D input and enables the three-state output from the mapping PROM. When the current microinstruction being executed is selecting the next microinstruction address as a JUMP function, the JUMP address will be available at the multiplexer D input. This is accomplished by having the Am2910 select the next address multiplexer D input and also enabling the three-state output of the pipeline register branch address field. The register enable input to the Am2910 can be grounded so that this register will load the value at the Am2910 D input. The value at D is clocked into the Am2910's register (R) at the end of the current microcycle, which makes the D value of this microcycle available as the R value of the next microcyle. Thus, by using the branch address field of two sequential microinstructions, a conditional JUMP-TO-ONE-OF-TWO-SUBROUTINES or a conditional JUMP-TO-ONE-OF-TWO-BRANCH-ADDRESSES can be executed by either selecting the D input or the R input of the next address multiplexer.

When sequencing through continuous microinstructions in the Am29774/75 microprogram memory, the program counter in the Am2910 is used. Here, the control logic simply selects the PC input of the next address multiplexer. In addition, most of these instructions enable the three-state outputs of the Am29774/75 pipeline register associated with the branch address field, which allows the register within the Am2910 to be loaded. The 5 x 12 stack in the Am2910 is used for looping and subroutining in microprogram operations. Up to five levels of subroutines or loops can be nested. Also, loops and subroutines can be intermixed as long as the five word depth of the stack is not exceeded.

The expansion scheme for increasing the depth of Am29774/75's is shown in Figure 2. Note that no speed degradation results when devices are cascaded. This is because the decode of the Am74S139 is in parallel with the PROM access time.

In order to provide an overall view of a typical Am2900 Bipolar Microprocessor, the block diagram of Figure 3 is presented. Here, the computer control unit (CCU) using the Am2910 and Am29774/75 registered PROM's is depicted. In addition, the typical connection scheme for the Am2903 Bipolar Microprocessor slices is shown. The four Am2903 devices in the block diagram form a typical 16-bit architecture. Also shown in Figure 3 is the general connection for the Am2914 Priority Interrupt Controller and the Am2920 as a Memory Address Register.

The block diagram also shows the Am2917 as the bus interface unit. Note that the Am2917 can interface directly with a data bus and the drive levels and receive levels are such that the instruction register can be built using standard Low-Power Schottky devices. This is possible because the receiver threshold on the Am2917 is designed identically to the thresholds on standard power Schottky and the Low-Power Schottky devices.

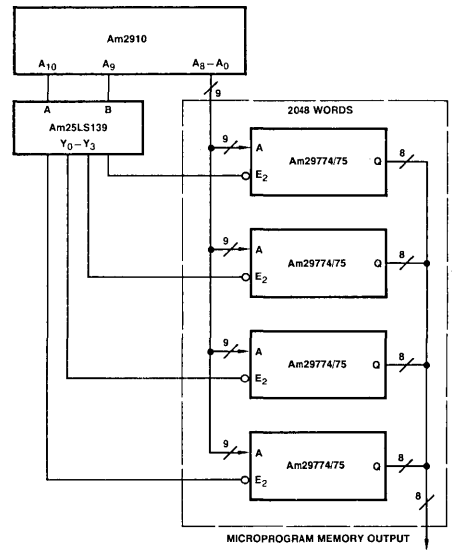


Figure 2. Word Expansion Scheme for the Am29774 and Am29775.

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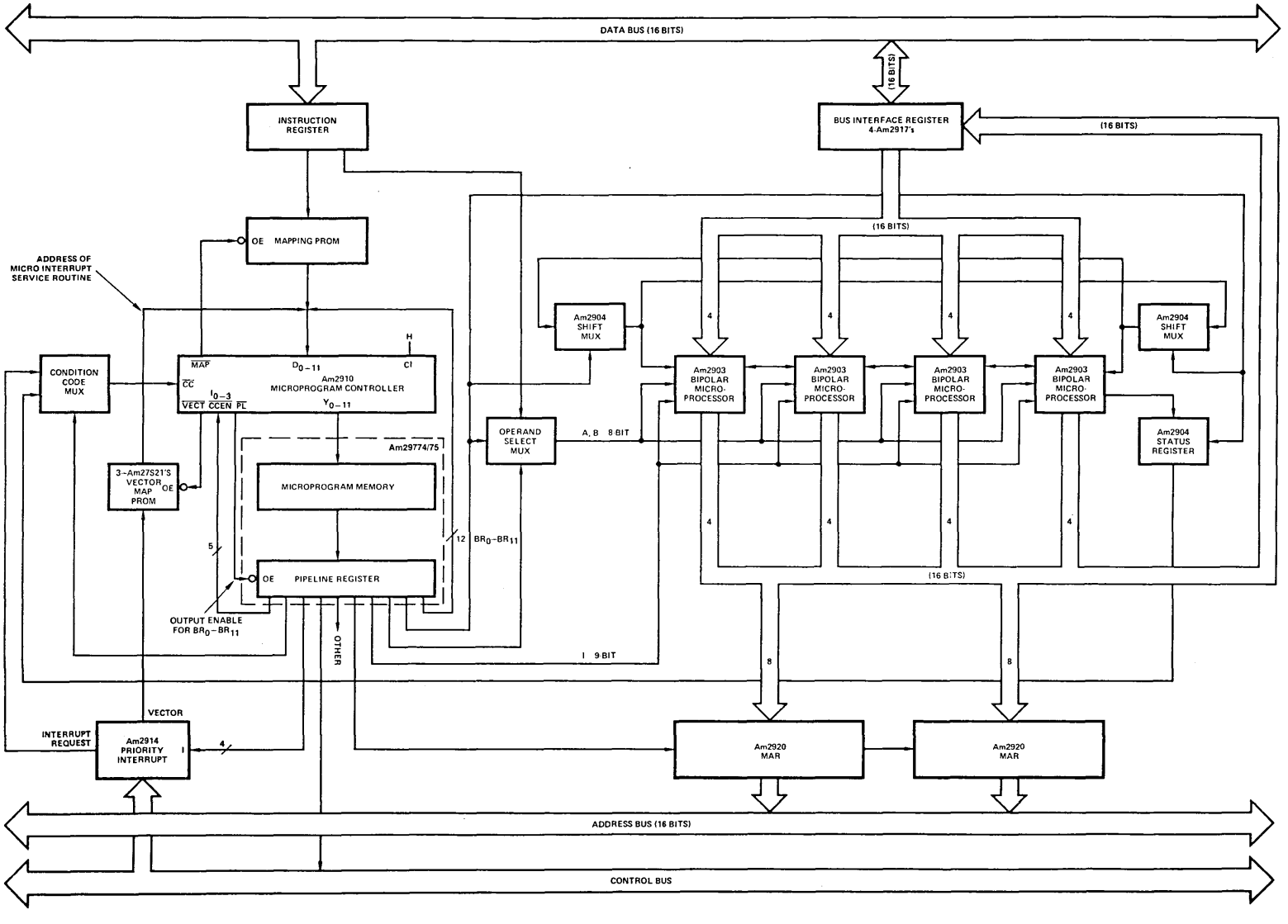

Figure 3. Typical Bipolar Microcomputer using the Am29774/75.

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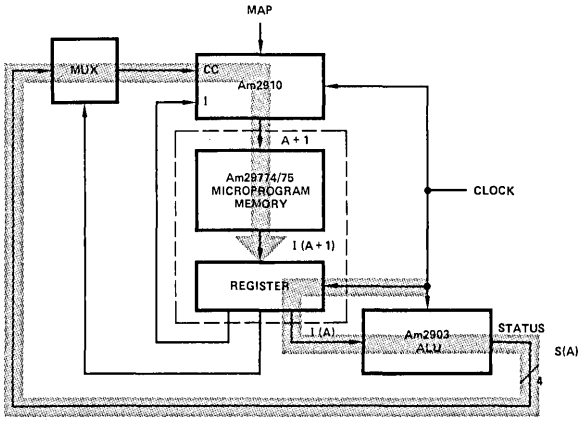
USING THE Am29774/75 IN A PIPELINED ARCHITECTURE



A Register at the Microprogram Memory output contains the microinstruction being executed. The microprogram memory and Am2903 delay are in series. Conditional branches are executed on same cycle as the ALU operation generating the condition.

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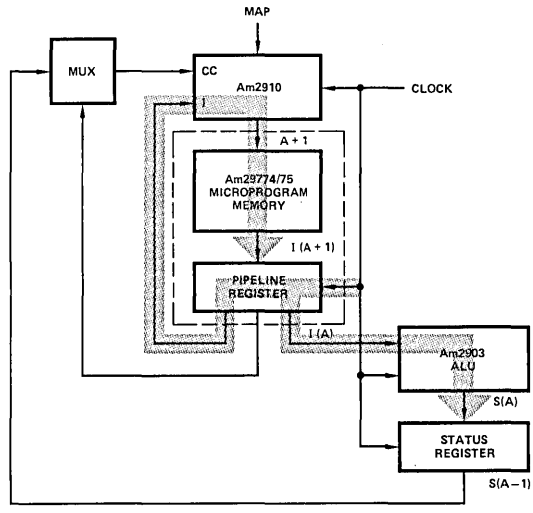

One level pipeline provides better speed than the architecture to the left. The Microprogram Memory and the Am2903 array are in parallel speed paths instead of in series. This is the recommended architecture for Am2900 designs. Note that the Am29774/75 reduces the parts count of the microprogram memory/pipeline by a factor of two.

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ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Open Collector Order Number	Three-State Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM29774DC	AM29775DC	D-22	C	C-1
AM29774DC-B	AM29775DC-B	D-22	C	B-1
AM29774DM	AM29775DM	D-22	M	C-3
AM29774DM-B	AM29775DM-B	D-22	M	B-3
AM29774DM	AM29775FM	F-22	M	C-3
AM29774FM-B	AM29775FM-B	F-22	M	B-3

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

Am29803A
16-Way Branch Control Unit

DISTINCTIVE CHARACTERISTICS

- 16 separate instructions – 2, 4, 8, or 16-way branch in one microprogram execution cycle
- Four individual test inputs
- Four individual outputs for driving the four OR inputs on the Am2909 Microprogram Sequencer
- Provides maximum branch capability in a microprogram control unit using the Am2909
- Advanced Low-Power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

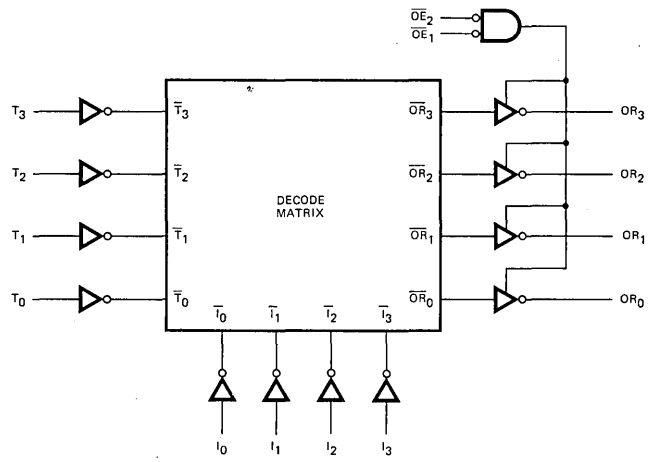
FUNCTIONAL DESCRIPTION

The Am29803A is a Low-Power Schottky processed device that provides 16-way branch control when used in conjunction with the Am2909 Microprogram Sequencer.

The device features 16 instructions that provide all combinations of simultaneous testing of four different inputs. The device has four outputs that are used to drive the four OR inputs of the Am2909 Microprogram Sequencer.

The "zero" instruction inhibits the testing of any of the four test (T) inputs. The remaining 15 instructions are used to test combinations of 1, 2, 3, or 4 of the T inputs simultaneously. If one T input is being tested, the Am29803A will select one of two possible addresses. If two T inputs are being tested, the device will select one of four possible addresses. If three T inputs are being tested, the device will select one of eight possible addresses. If all four T inputs are being tested, the device will select one of sixteen addresses as the field used to drive the OR inputs of the Am2909.

LOGIC DIAGRAM



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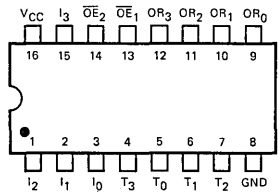
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

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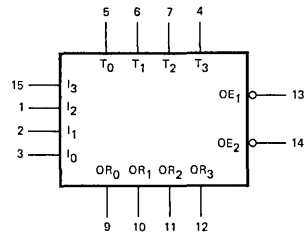
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am29803ADC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am29803ADM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		95	130	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS1}}$ = 2.4V; V_O = 4.5V			40	µA
		V_{CC} = MAX., $V_{\overline{CS1}}$ = 2.4V; V_O = 2.4V			40	µA
		V_{CC} = MAX., $V_{\overline{CS1}}$ = 2.4V; V_O = 0.4V			−40	µA
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		pF

Note 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C

2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

3. These parameters are not 100% tested, but are periodically sampled.

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH} t_{PHL}	I_i to OR_i	C_L = 15pF R_L = 2.0kΩ		25	35	ns
t_{PLH} t_{PHL}	T_i to OR_i			25	35	ns
t_{ZH} t_{ZL}	$\overline{OE}_i$ to OR_i			15	18	ns
t_{HZ} t_{LZ}	$\overline{OE}_i$ to OR_i	C_L = 5.0pF R_L = 2.0kΩ		15	18	ns

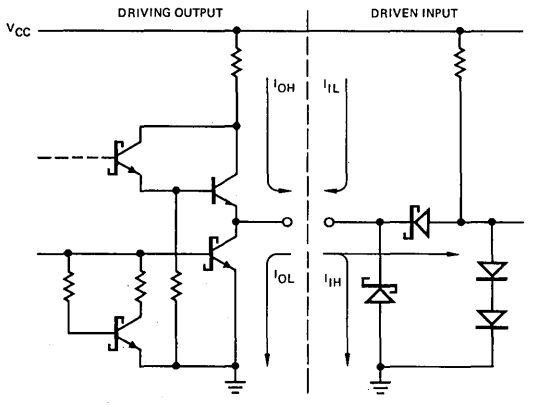
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Parameters	Description	Test Conditions	COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% Min.	COM'L Max.	MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% Min.	MIL Max.	Units
t_{PLH} t_{PHL}	I_i to OR_i	C_L = 15pF R_L = 2.0kΩ		45		60	ns
t_{PLH} t_{PHL}	T_i to OR_i			45		60	ns
t_{ZH} t_{ZL}	$\overline{OE}_i$ to OR_i			30		30	ns
t_{HZ} t_{LZ}	$\overline{OE}_i$ to OR_i			20		20	ns

DEFINITION OF FUNCTIONAL TERMS

I_0, I_1, I_2, I_3	The four instruction inputs to the device
T_0, T_1, T_2, T_3	The four test inputs for the device
OR_0, OR_1, OR_2, OR_3	The four outputs of the device that are connected to the four OR inputs of the Am2909
$\overline{OE}_1, \overline{OE}_2$	Output Enable. When either $\overline{OE}$ input is HIGH, the OR_i outputs are in the high impedance state. When both the $\overline{OE}_1$ and $\overline{OE}_2$ inputs are LOW, the OR outputs are enabled and the selected data will be present.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

Pin No.'s	Input/Output	Input Load	Output HIGH	Output LOW MIL	Output LOW COM'L
1	I_2	0.5	–	–	–
2	I_1	0.5	–	–	–
3	I_0	0.5	–	–	–
4	T_3	0.5	–	–	–
5	T_0	0.5	–	–	–
6	T_1	0.5	–	–	–
7	T_2	0.5	–	–	–
8	GND	–	–	–	–
9	OR_0	–	100	44	44
10	OR_1	–	100	44	44
11	OR_2	–	100	44	44
12	OR_3	–	100	44	44
13	$\overline{OE}_1$	0.5	–	–	–
14	$\overline{OE}_2$	0.5	–	–	–
15	I_3	0.5	–	–	–
16	V_{CC}	–	–	–	–

FUNCTION TABLE

Function	I_3	I_2	I_1	I_0	T_3	T_2	T_1	T_0	OR_3	OR_2	OR_1	OR_0
No Test	L	L	L	L	X	X	X	X	L	L	L	L
Test T_0	L	L	L	H	X	X	X	L	L	L	L	L
					X	X	X	H	L	L	L	H
Test T_1	L	L	H	L	X	X	L	X	L	L	L	L
					X	X	H	X	L	L	L	H
Test T_0 & T_1	L	L	H	H	X	X	L	L	L	L	L	L
					X	X	L	H	L	L	L	H
					X	X	H	L	L	L	H	L
					X	X	H	H	L	L	H	H
Test T_2	L	H	L	L	X	L	X	X	L	L	L	L
					X	H	X	X	L	L	L	H
Test T_0 & T_2	L	H	L	H	X	L	X	L	L	L	L	L
					X	L	X	H	L	L	L	H
					X	H	X	L	L	L	H	L
					X	H	X	H	L	L	H	H
Test T_1 & T_2	L	H	H	L	X	L	L	X	L	L	L	L
					X	L	H	X	L	L	L	H
					X	H	L	X	L	L	H	L
					X	H	H	X	L	L	H	H
Test T_0, T_1 & T_2	L	H	H	H	X	L	L	L	L	L	L	L
					X	L	L	H	L	L	L	H
					X	L	H	L	L	L	H	L
					X	L	H	H	L	L	H	H
					X	H	L	L	L	H	L	L
					X	H	L	H	L	H	L	H
					X	H	H	L	L	H	H	L
					X	H	H	H	L	H	H	H
Test T_3	H	L	L	L	L	X	X	X	L	L	L	L
					H	X	X	X	L	L	L	H
Test T_0 & T_3	H	L	L	H	L	X	X	L	L	L	L	L
					L	X	X	H	L	L	L	H
					H	X	X	L	L	L	H	L
					H	X	X	H	L	L	H	H
Test T_1 & T_3	H	L	H	L	L	X	L	X	L	L	L	L
					L	X	H	X	L	L	L	H
					H	X	L	X	L	L	H	L
					H	X	H	X	L	L	H	H
Test T_0, T_1 & T_3	H	L	H	H	L	X	L	L	L	L	L	L
					L	X	L	H	L	L	L	H
					L	X	H	L	L	L	H	L
					L	X	H	H	L	L	H	H
					H	X	L	L	L	H	L	L
					H	X	L	H	L	H	L	H
					H	X	H	L	L	H	H	L
					H	X	H	H	L	H	H	H
Test T_2 & T_3	H	H	L	L	L	L	X	X	L	L	L	L
					L	H	X	X	L	L	L	H
					H	L	X	X	L	L	H	L
					H	H	X	X	L	L	H	H
Test T_0, T_2 & T_3	H	H	L	H	L	L	X	L	L	L	L	L
					L	L	X	H	L	L	L	H
					L	H	X	L	L	L	H	L
					L	H	X	H	L	L	H	H
					H	L	X	L	L	H	L	L
					H	L	X	H	L	H	L	H
					H	H	X	L	L	H	H	L
					H	H	X	H	L	H	H	H
Test T_1, T_2 & T_3	H	H	H	L	L	L	H	X	L	L	L	L
					L	L	H	X	L	L	L	H
					L	H	L	X	L	L	H	L
					L	H	H	X	L	L	H	H
					H	L	L	X	L	H	L	L
					H	L	H	X	L	H	L	H
					H	H	L	X	L	H	H	L
					H	H	H	X	L	H	H	H
Test T_0, T_1, T_2 & T_3	H	H	H	H	L	L	L	L	L	L	L	L
					L	L	L	H	L	L	L	H
					L	L	H	L	L	L	H	L
					L	L	H	H	L	L	H	H
					L	H	L	L	L	H	L	L
					L	H	L	H	L	H	L	H
					L	H	H	L	L	H	H	L
					L	H	H	H	L	H	H	H
					H	L	L	L	H	L	L	L
					H	L	L	H	H	L	L	H
					H	L	H	L	H	L	H	L
					H	L	H	H	H	L	H	H
					H	H	L	L	H	H	L	L
					H	H	L	H	H	H	L	H
					H	H	H	L	H	H	H	L
					H	H	H	H	H	H	H	H

L = LOW, H = HIGH, X = Don't care

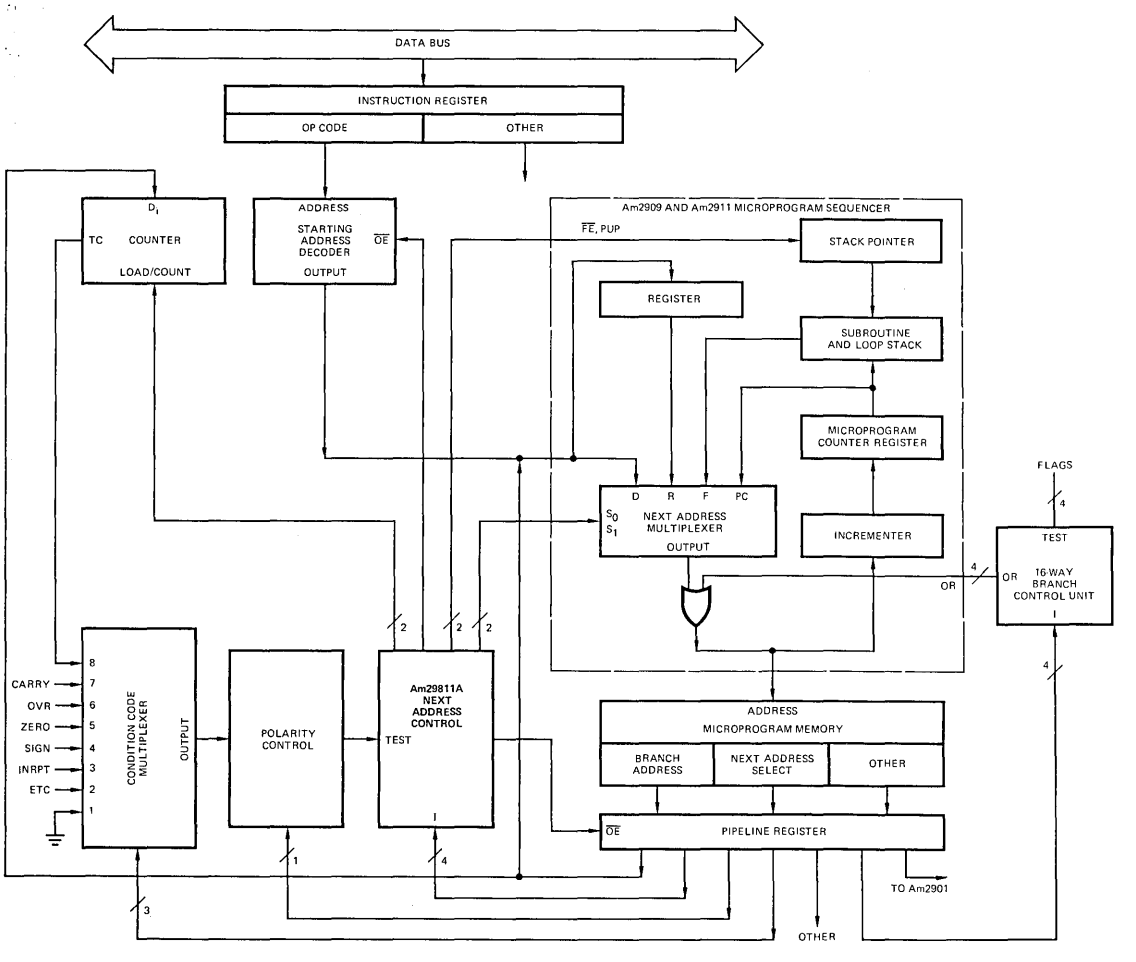
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM29803APC	P-16	C	C-1
AM29803ADC	D-16	C	C-1
AM29803ADC-B	D-16	C	B-1
AM29803ADM	D-16	M	C-3
AM29803ADM-B	D-16	M	B-3
AM29803AFM	F-16	M	C-3
AM29803AFM-B	F-16	M	B-3

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATION



A typical computer control unit using the Am2909, Am2911, Am29803A and Am29811A. Note that the least significant microprogram sequencer is an Am2909 and the more significant sequencers are Am2911's.

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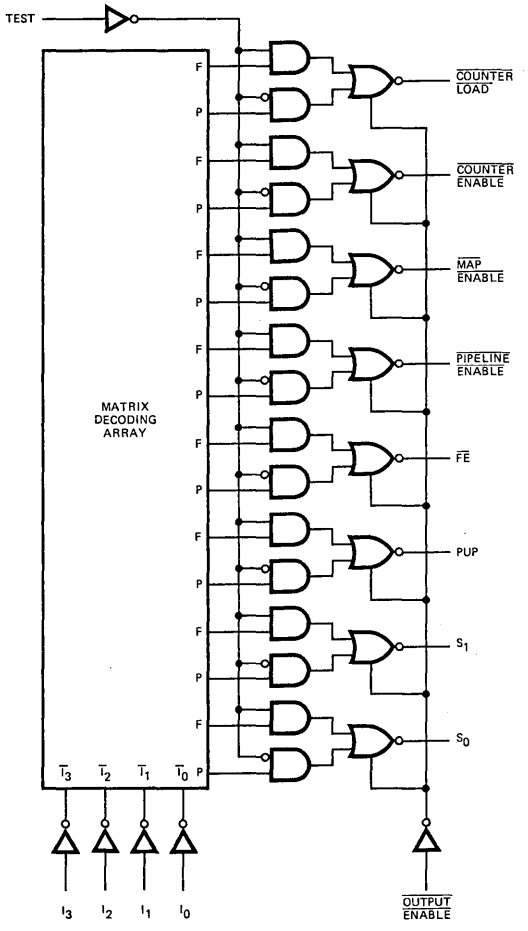
Am29811A

Next Address Control Unit

DISTINCTIVE CHARACTERISTICS

- Next address control unit for the Am2911 Microprogram Sequencer
- 16 next address instructions
- Test input for conditional instructions
- Separate outputs to control the Am2911, an independent event counter, and a mapping PROM/branch address interface
- Advanced Low-Power Schottky technology
- 100% reliability assurance testing in compliance with MIL-STD-883

LOGIC DIAGRAM



P = Pass
F = Fail

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FUNCTIONAL CHARACTERISTICS

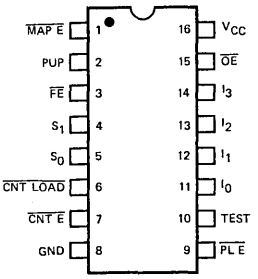
The Am29811A is a Low-Power Schottky device designed specifically for next address control of the Am2911 Microprogram Sequencer. The device contains all outputs required to control a high-performance computer control unit or a structured state machine design using microprogramming techniques.

Sixteen instructions are available by using a four-bit instruction field $I_{0\text{-}3}$. In addition, a test input is available such that conditional instructions can be performed based on a condition code test input.

The full instruction set consists of such functions as conditional jumps, conditional jump-to-subroutine, conditional return-from-subroutine, conditional repeat loops, conditional branch to starting address, and so forth.

One Am29811A can be used to control any number of Am2911 Microprogram Sequencers. The Am2911 Sequencer is a four-bit slice itself. Thus, one Am29811A Next Address Control Unit and three Am2911 Microprogram Sequencers can be used to build the most powerful, state-of-the-art, microprogram sequencer capable of controlling 4k words of microprogram memory.

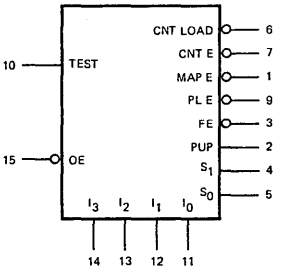
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-315

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

MPR-316

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7.0V
DC Voltage Applied to Outputs	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Input Current	−30mA to +5mA

OPERATING RANGE

COM'L	Am29811ADC	T_A = 0°C to +75°C	V_{CC} = 5.0V ±5%
MIL	Am29811ADM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ. (Note 1)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}	2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.45	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.45V		−0.010	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V			25	μA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V			1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V (Note 2)	−20	−40	−90	mA
I_{CC}	Power Supply Current	All inputs = GND V_{CC} = MAX.		90	115	mA
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA			−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; V_O = 4.5V			40	μA
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; V_O = 2.4V			40	
		V_{CC} = MAX., $V_{\overline{CS}}$ = 2.4V; V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1 MHz (Note 3)		4		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1 MHz (Note 3)		8		

Notes: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but periodically sampled.

SWITCHING CHARACTERISTICS
(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH} t_{PHL}	I_i to Any Output	C_L = 15pF R_L = 2.0kΩ		25	35	ns
t_{PLH} t_{PHL}	Test to Any Output			25	35	ns
t_{ZH} t_{ZL}	$\overline{OE}$ to Any Output			15	20	ns
t_{HZ} t_{LZ}	$\overline{OE}$ to Any Output	C_L = 5.0pF R_L = 2.0kΩ		15	20	ns

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

			COM'L		MIL		
			T_A = 0°C to +70°C V_{CC} = 5.0V ±5%		T_A = −55°C to +125°C V_{CC} = 5.0V ±10%		
Parameters	Description	Test Conditions	Min.	Max.	Min.	Max.	Units
t_{PLH} t_{PHL}	I_i to Any Output	C_L = 15pF R_L = 2.0kΩ		40		50	ns
t_{PLH} t_{PHL}	Test to Any Output			40		50	ns
t_{ZH} t_{ZL}	$\overline{OE}$ to Any Output			25		30	ns
t_{HZ} t_{LZ}	$\overline{OE}$ to Any Output			25		30	ns

DEFINITION OF FUNCTIONAL TERMS

I_0, I_1, I_2, I_3 The four instruction inputs to the Am29811A.

TEST The condition code input to the device. When the test input is LOW, the device assumes the test has failed. When the test input is HIGH, the device assumes the condition code required has been met; the test has passed.

$\overline{\text{Counter Load}}$ This output is used to drive the parallel load input of an Am25LS169 up/down counter.

$\overline{\text{Counter Enable}}$ This output is used to drive the counter enable input of an Am25LS169 up/down counter.

$\overline{\text{Map Enable}}$ This output is used to control the three-state outputs of the mapping PROM or PLA used to provide the initial starting address for each machine instruction.

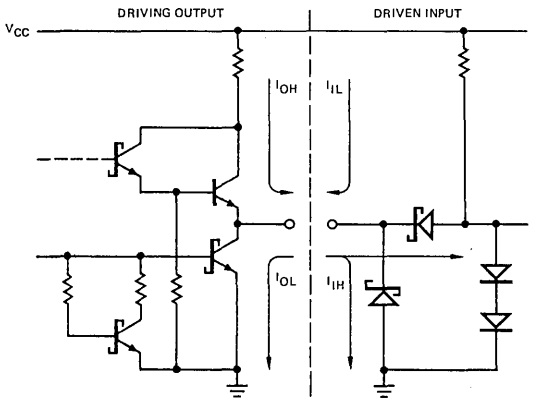
$\overline{\text{Pipeline Enable}}$ This output is used to control the three-state output of the pipeline register (Am2918) containing the branch address for the computer control unit.

$\overline{\text{FE}}$ File Enable This output is used to drive the file enable input of the Am2911. When the file enable output is LOW, a stack operation will take place.

PUP Push/Pop. The PUP output is used to drive the push/pop input of the Am2911 Microprogram Sequencer. When the PUP output is HIGH, a push will take place when the file is enabled. When the PUP output is LOW, a pop will take place when the file is enabled.

S_0, S_1 These two outputs are used to drive the S_0 and S_1 inputs to the Am2911 Microprogram Sequencer. These outputs control whether the direct input, the register, the microprogram counter, or the stack is selected as the source of the next address for the microprogram memory.

LOW-POWER SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

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GUARANTEED LOADING RULES OVER OPERATING RANGE (In Unit Loads)

A Low-Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and –0.36mA measured at 0.4V LOW.

Pin No.'s	Input/Output	Input Load	Output HIGH	Output LOW MIL	Output LOW COM'L
1	$\overline{\text{MAP E}}$	–	100	44	44
2	PUP	–	100	44	44
3	$\overline{\text{FE}}$	–	100	44	44
4	S_1	–	100	44	44
5	S_0	–	100	44	44
6	$\overline{\text{CNT LOAD}}$	–	100	44	44
7	$\overline{\text{CNT E}}$	–	100	44	44
8	GND	–	–	–	–
9	$\overline{\text{PL E}}$	–	100	44	44
10	TEST	0.5	–	–	–
11	I_0	0.5	–	–	–
12	I_1	0.5	–	–	–
13	I_2	0.5	–	–	–
14	I_3	0.5	–	–	–
15	$\overline{\text{OE}}$	–	100	44	44
16	V_{CC}	–	–	–	–

INSTRUCTION TABLE

MNEMONIC	I_3 I_2 I_1 I_0	INSTRUCTION
JZ	L L L L	Jump to Address Zero
CJS	L L L H	Conditional Jump-to-Subroutine with Jump Address in Pipeline Register.
JMAP	L L H L	Jump to Address at Mapping PROM Output.
CJP	L L H H	Conditional Jump to Address in Pipeline Register
PUSH	L H L L	Push Stack and Conditionally Load Counter
JSRP	L H L H	Jump-to-Subroutine with Starting Address Conditionally Selected from Am2911 R-Register or Pipeline Register.
CJV	L H H L	Conditional Jump to Vector Address.
JRP	L H H H	Jump to Address Conditionally Selected from Am2911 R-Register or Pipeline Register.
RFCT	H L L L	Repeat Loop if Counter is not Equal to Zero.
RPCT	H L L H	Repeat Pipeline Address if Counter is not Equal to Zero.
CRTN	H L H L	Conditional Return-from-Subroutine.
CJPP	H L H H	Conditional Jump to Pipeline Address and Pop Stack.
LDCT	H H L L	Load Counter and Continue.
LOOP	H H L H	Test End of Loop.
CONT	H H H L	Continue to Next Address.
JP	H H H H	Jump to Pipeline Register Address.

FUNCTION TABLE

MNEMONIC	INPUTS			OUTPUTS				
	INSTRUCTION I_3 I_2 I_1 I_0	FUNCTION	TEST INPUT	NEXT ADDR SOURCE	FILE	COUNTER	MAP-E	PL-E
JZ	L L L L	JUMP ZERO	X	D	HOLD	L L*	H	L
CJS	L L L H	COND JSB PL	L	PC	HOLD	HOLD	H	L
			H	D	PUSH	HOLD	H	L
JMAP	L L H L	JUMP MAP	X	D	HOLD	HOLD	L	H
CJP	L L H H	COND JUMP PL	L	PC	HOLD	HOLD	H	L
			H	D	HOLD	HOLD	H	L
PUSH	L H L L	PUSH/COND LD CNTR	L	PC	PUSH	HOLD	H	L
			H	PC	PUSH	LOAD	H	L
JSRP	L H L H	COND JSB R/PL	L	R	PUSH	HOLD	H	L
			H	D	PUSH	HOLD	H	L
CJV	L H H L	COND JUMP VECTOR	L	PC	HOLD	HOLD	H	H
			H	D	HOLD	HOLD	H	H
JRP	L H H H	COND JUMP R/PL	L	R	HOLD	HOLD	H	L
			H	D	HOLD	HOLD	H	L
RFCT	H L L L	REPEAT LOOP, CNTR ≠ 0	L	F	HOLD	DEC	H	L
			H	PC	POP	HOLD	H	L
RPCT	H L L H	REPEAT PL, CNTR ≠ 0	L	D	HOLD	DEC	H	L
			H	PC	HOLD	HOLD	H	L
CRTN	H L H L	COND RTN	L	PC	HOLD	HOLD	H	L
			H	F	POP	HOLD	H	L
CJPP	H L H H	COND JUMP PL & POP	L	PC	HOLD	HOLD	H	L
			H	D	POP	HOLD	H	L
LDCT	H H L L	LOAD CNTR & CONTINUE	X	PC	HOLD	LOAD	H	L
LOOP	H H L H	TEST END LOOP	L	F	HOLD	HOLD	H	L
			H	PC	POP	HOLD	H	L
CONT	H H H L	CONTINUE	X	PC	HOLD	HOLD	H	L
JP	H H H H	JUMP PL	X	D	HOLD	HOLD	H	L

L = LOW
H = HIGH
X = Don't Care

DEC = Decrement
*LL = Special Case

TRUTH TABLE

MNEMONIC	FUNCTION	INPUTS					OUTPUTS							
							NEXT ADDR SOURCE		FILE		COUNTER		MAP $\overline{E}$	PL $\overline{E}$
		I_3	I_2	I_1	I_0	TEST	S_1	S_0	$\overline{FE}$	PUP	$\overline{LOAD}$	$\overline{EN}$		
	PIN NO.	14	13	12	11	10	4	5	3	2	6	7	1	9
JZ	JUMP ZERO	L	L	L	L	L	H	H	H	H	L	L	H	L
		L	L	L	L	H	H	H	H	H	L	L	H	L
CJS	COND JSB PL	L	L	L	H	L	L	L	H	H	H	H	H	L
		L	L	L	H	H	H	H	L	H	H	H	H	L
JMAP	JUMP MAP	L	L	H	L	L	H	H	H	H	H	H	L	H
		L	L	H	L	H	H	H	H	H	H	H	L	H
CJP	COND JUMP PL	L	L	H	H	L	L	L	H	H	H	H	H	L
		L	L	H	H	H	H	H	H	H	H	H	H	L
PUSH	PUSH/COND LD CNTR	L	H	L	L	L	L	L	L	H	H	H	H	L
		L	H	L	L	H	L	L	L	H	L	H	H	L
JSRP	COND JSB R/PL	L	H	L	H	L	L	H	L	H	H	H	H	L
		L	H	L	H	H	H	H	L	H	H	H	H	L
CJV	COND JUMP VECTOR	L	H	H	L	L	L	L	H	H	H	H	H	H
		L	H	H	L	H	H	H	H	H	H	H	H	H
JRP	COND JUMP R/PL	L	H	H	H	L	L	H	H	H	H	H	H	L
		L	H	H	H	H	H	H	H	H	H	H	H	L
RFCT	REPEAT LOOP, CTR ≠ 0	H	L	L	L	L	H	L	H	L	H	L	H	L
		H	L	L	L	H	L	L	L	L	H	H	H	L
RPCT	REPEAT PL, CTR ≠ 0	H	L	L	H	L	H	H	H	H	H	L	H	L
		H	L	L	H	H	L	L	H	H	H	H	H	L
CRTN	COND RTN	H	L	H	L	L	L	L	H	L	H	H	H	L
		H	L	H	L	H	H	L	L	L	H	H	H	L
CJPP	COND JUMP PL & POP	H	L	H	H	L	L	L	H	L	H	H	H	L
		H	L	H	H	H	H	H	L	L	H	H	H	L
LDCT	LD CNTR & CONTINUE	H	H	L	L	L	L	L	H	H	L	H	H	L
		H	H	L	L	H	L	L	H	H	L	H	H	L
LOOP	TEST END LOOP	H	H	L	H	L	H	L	H	L	H	H	H	L
		H	H	L	H	H	L	L	L	L	H	H	H	L
CONT	CONTINUE	H	H	H	L	L	L	L	H	H	H	H	H	L
		H	H	H	L	H	L	L	H	H	H	H	H	L
JP	JUMP PL	H	H	H	H	L	H	H	H	H	H	H	H	L
		H	H	H	H	H	H	H	H	H	H	H	H	L

L = LOW
H = HIGH

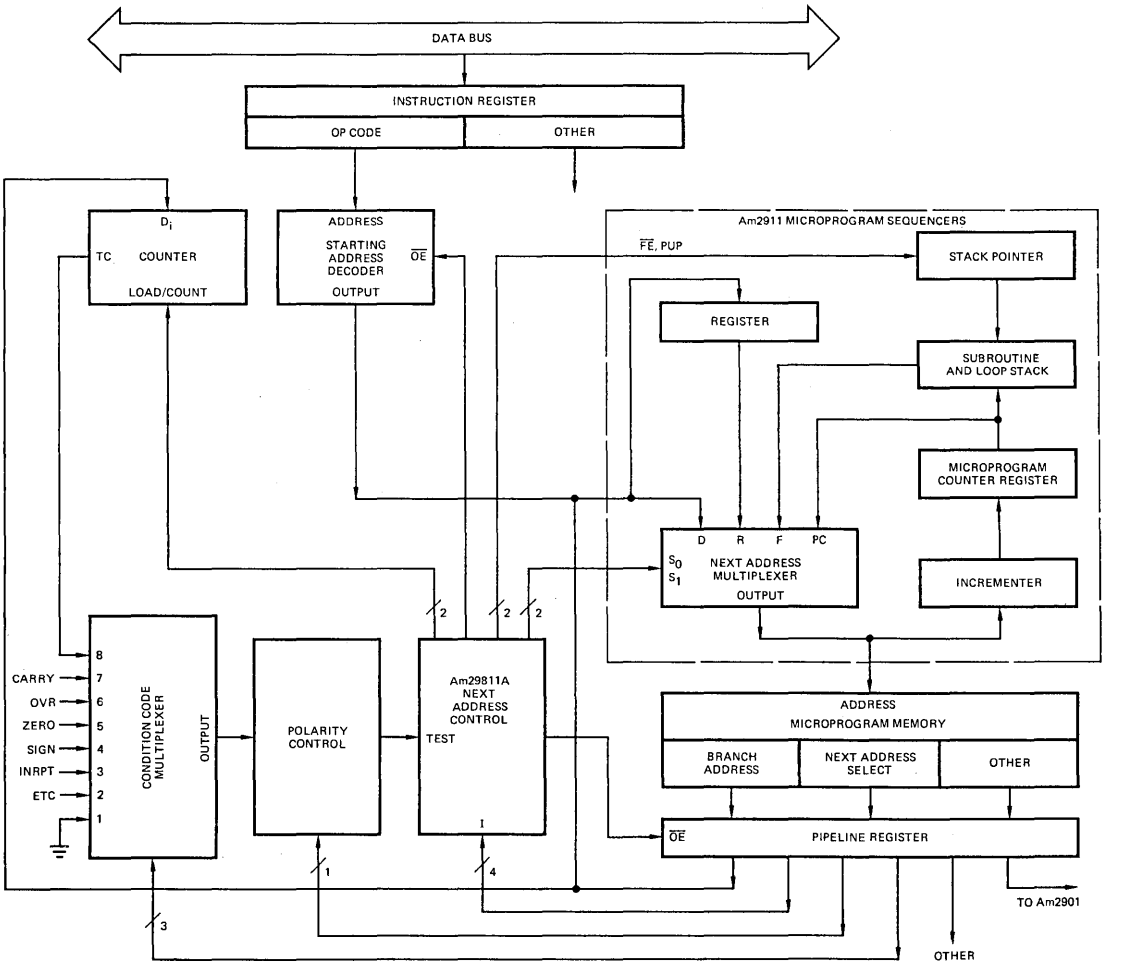
ORDERING INFORMATION

Order the part number according to the table below to obtain the desired package, temperature range, and screening level.

Order Number	Package Type (Note 1)	Temperature Range (Note 2)	Screening Level (Note 3)
AM29811APC	P-16	C	C-1
AM29811ADC	D-16	C	C-1
AM29811ADC-B	D-16	C	B-1
AM29811ADM	D-16	M	C-3
AM29811ADM-B	D-16	M	B-3
AM29811AFM	F-16	M	C-3
AM29811AFM-B	F-16	M	B-3

Notes: 1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0°C to +70°C, M = −55°C to +125°C.
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

APPLICATION



A Typical Computer Control Unit Using the Am2911 and Am29811A.

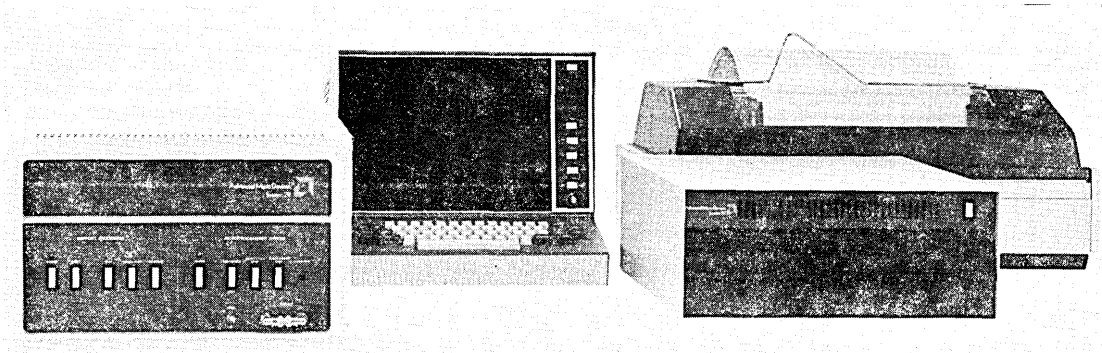
MPR-318

System 29

The Advanced Microprogram Development System

FEATURES

- **The first universal, complete development system for microprogrammed machines.**
  Use to assemble microcode, debug microcode, check out hardware.
- **AMDASM™29 microassembler resident on system.**
  Microprograms can be written, assembled, and loaded into the development hardware all on one system. No transferring from one system to another. No messy paper tape.
- **Software to check out microcode.**
  All the tools needed in a useful development system including single step, trap, edit.
- **Writable Control Store up to 4K words.**
  RAM in System 29 serves as control memory for prototype. Expandable up to 4K words, up to 128 bits each. Access time down to 50ns.
- **Application Cards Available.**
  Pre-built prototype systems reduce design time, get products out sooner.
- **Universal Prototyping cards**
  Use popular SBC-80 form factor and hold parts on 0.3", 0.4", and 0.6" centers.
- **Time proven disk operating system.**
  Complete file management including a context editor.
- **8080 software development tools.**

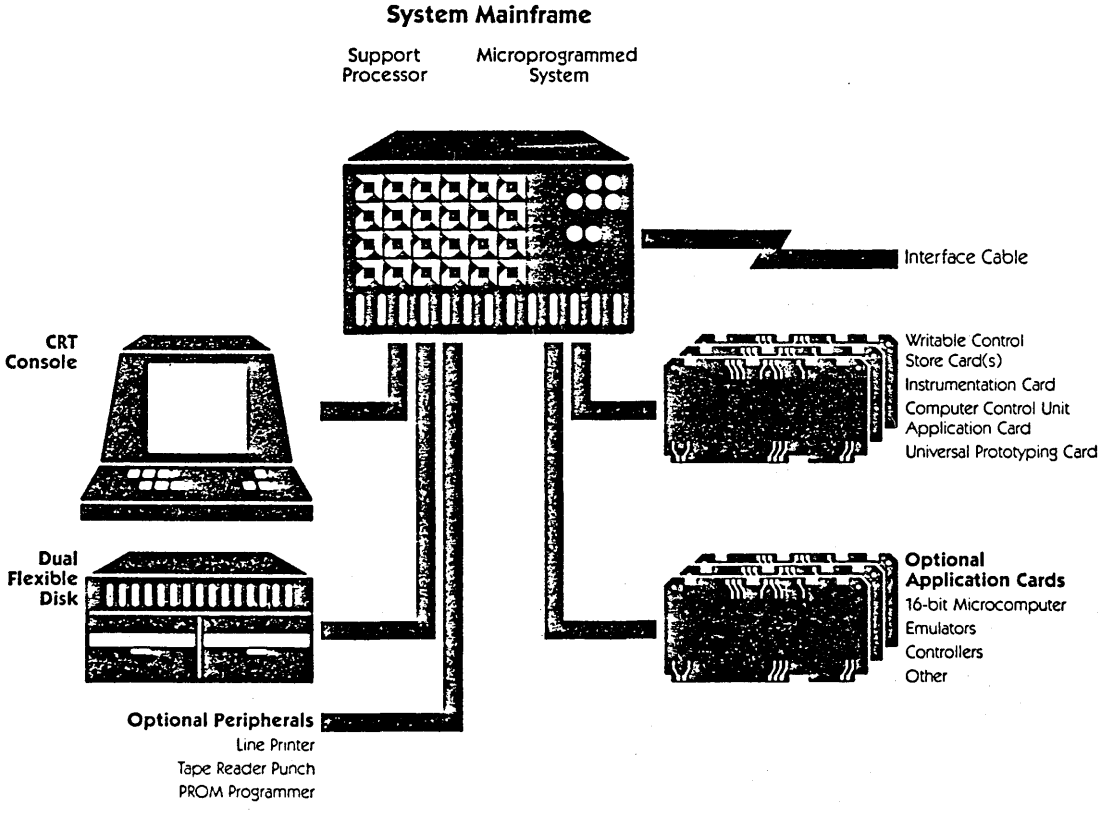


DESCRIPTION:

System 29 is a complete development system. It encompasses all the tools needed, from microcode/firmware definition, assembly, check-out of the hardware and formatting of the microcode, through programming PROM's.

System 29 includes a System Mainframe, CRT Console, and Dual-Drive Flexible Disk. It comes with a comprehensive software package. It is ready to operate in its basic configuration which includes 2K words by 64 bits Writeable Control Store and a Computer Control Unit (CCU) microprogram controller. A number of peripherals (line printer, paper tape reader-punch, PROM programmer) and cards (high-speed Writeable Control Store, trace analyzer, 8080 emulator application card, 16-bit microcomputer application card) enhance its performance even further.

Because it is controlled by an Am9080A, it can also serve as a software development system for the 8080 fixed-instruction-set microprocessors.



SYSTEM DESCRIPTION

BASIC SYSTEM:

A complete working system including;

Equipment

- System Mainframe:
  - Support Processor:
    - Am9080A CPU Card
    - System Memory Card, 32K bytes, expandable to 64K bytes with an additional card
    - 4 Serial Ports (RS232)
    - 1 Parallel Port
    - Power Supply
  - Microprogrammed System:
    - 1 Writeable Control Store Card, 2K x 64 bits. System is pre-wired for 2.
    - 1 Instrumentation Card
    - 1 Computer Control Unit Application Card
    - 5 Open Slots for Additional User Cards
    - 1 Power Supply, +5V, 25A (50A Optional)
- CRT Console
- Dual Drive Flexible Disk
- Universal Prototyping Card
- Outboard Interface Cable
- Blank Diskettes (2)

Software

- AMDOS 29™ Disk Operating System with full set of commands
- Microprogram Generation Software
  - AMDASM 29™ Microprogram Assembler
  - AMSCRM 29™, AMPROM 29™ Post-Processing Programs
- Microprogram Support Software
- Am9080A Software (Assembler, Loader, Dynamic Debugger including disassembler and trace capability)

Documentation (2 sets)

- User Manual
- Software Manual
- Hardware Manual

Services

- User Training (2 Persons)
- Field Applications Support
- Warranty: 1 Year (90 days on System Mainframe Plug-in Cards)

SYSTEM OPTIONS[1]

CARDS[2]

Option No.

0100 *Universal Prototying card,* additional to one included in the basic system.

0105 *Writable Control Store card.* 2K x 64 bits, additional to one included in the basic system. Field updatable.

0106 *High Speed Writable Control Store card,* 1K x 64 bits; system is pre-wired for 2. Field updatable.

PERIPHERALS

0500 *Line Printer,* 220 lines/minute. 132 columns.[3] Field updatable. With stand.

0510 *Paper Tape Reader-Punch*[3]. 300cps read, 75cps punch.

SERVICES

0800 *Training Course.* System 29, for one additional person. Training for 2 persons included in the basic system.

MISCELLANEOUS

0900 *High Speed Extender card,* multilayer (internal ground plane)

0901 *Power Supply,* 50A Module. Field updatable

0902 *Diskettes.* Package of 10 blanks[4].

0903 *System Manual.* One set of manuals, additional to 2 provided with the basic system.[4]

NOTES:

1. SY29XXXX – When coding orders, replace X's with 4 digit option number, leave blank for basic system. Example: SY290500 is code for the Line Printer option
2. Warranty 90 days, parts and labor.
3. Warranty 120 days, parts and labor.
4. Quantity 2 minimum when purchased separately.

SOFTWARE FEATURES

- The convenience of the AMDOS™ 29 Disk Operating System with a full set of file management commands, including an editor.
- Microprogram generation software including the AMDASM™ 29 micro-assembler and the AMSCRM™ 29 and AMPROM™ 29 post-processing programs.
- Microprogram support software to load, save, and debug microcode during the firmware/hardware check-out phase.
- Am9080A software to write special programs to add to the existing software or for separate designs using the Am9080A fixed-instruction-set micro-processor.

HARDWARE FEATURES

- Writable Control Store for microprogram memory and ROM simulation. Its storage capacity can be easily expanded and a high speed option permits real-time testing.
- Microcode check-out functions let the user interact freely with the microcode, i.e., display, modify, move, locate, store, and verify. The user can also single-step through instructions, set trap bits, set comparison values, and force address jumps for easy test and debug of the microcode and its associated hardware. These are combined hardware-software features which are accessible either at the CRT Console or the System Mainframe front panel.
- Universal Prototyping Cards feature high packing density. They accept the user prototype and plug right into System 29.
- The Outboard Interface cable interfaces System 29 to the user design for a form factor that calls for an outboard configuration.
- A number of application cards help the user in his microprogrammed system design.
- Developed microcode can be stored on flexible diskettes, printed out, punched on paper tape or used to drive a PROM programmer.
- Diskette to main memory data transfers are affected by direct memory access (DMA) without I/O port addressing. This results in high-speed data transfers.
- An internal 2.457MHz crystal-controlled clock oscillator is provided. An external connector is available for providing a different clock frequency from a signal generator or an external circuit to meet individual user requirements.

System 29

THE UNIQUE MICROPROCESSOR LAB FOR YOUR MICROPROGRAMMED DESIGNS

By John R. Mick and Robert Schopmeyer

INTRODUCTION

Designing high-speed, microprogrammed processors is a complex task made easier by the availability of powerful LSI building blocks like the Am2900 Family. The design task for microprogrammed machines is usually more difficult than that required for systems based on fixed instruction processors like the Am9080A. Because of the flexibility of the components, a wide variety of architectures are possible for the design of high-performance or special purpose processors. However, it is this flexibility that sometimes tends to complicate the design process because every design is different.

Since each design is different, hardware prototyping and microcode development tend to be an ad hoc process with little of the work expended on one design transferable to the next design. In many cases, the design engineer is forced to "haywire" his engineering model with some type of homebrew PROM simulator. Once the hardware is in place, the design engineer must interface this hardware with the microcode. Usually, the microcode has been written using a microprogram assembler that was modified from the last modification from the last program requiring a modified assembler. To summarize the problem: The microprogrammed microprocessor community does not currently have a good development system designed to meet the diversified requirements for developing microprogrammed systems regardless of their architectures.

"System 29", the Advanced Microprogramming Development System, is Advanced Micro Devices' response to this need. This system will make it easier to design with the Am2900 family by providing the necessary hardware and software to develop microprogrammed systems.

GENERAL DESCRIPTION

System 29 is a complete microprogrammed system development lab which can be used to develop hardware and firmware designs and then used to check out the prototype system.

As shown in Figure 1, System 29 consists of a Support Processor configured and programmed to support a Microprogrammed System. This system provides the design engineer with the following facilities:

- An interactive editing system for building microcode definition and source files
- A microprogram assembler, AMDASM™/29 for assembling microcode
- A prototype check-out work station for debugging microprogrammed hardware designs

TM: Trademark applied for.

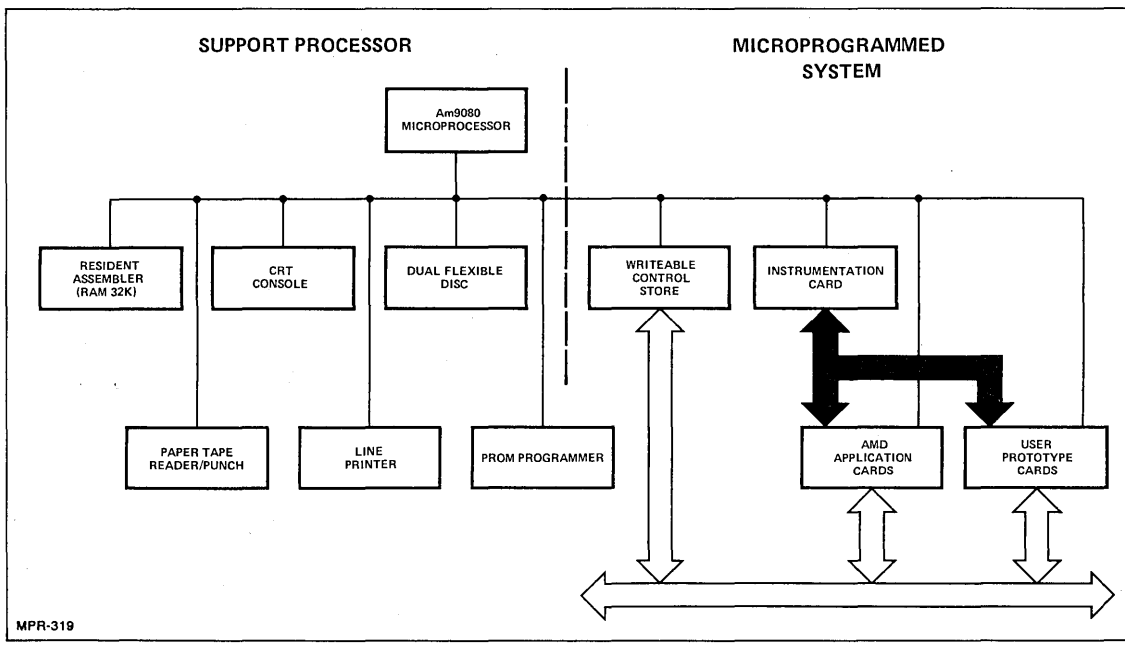


Figure 1. System 29 Architecture.

SYSTEM HARDWARE

System 29 (as shown in detail in Figure 2) is two separate systems in a single package – a Support Processor system and a Microprogrammed System. The Support Processor system is based on the Am9080A MOS Microprocessor and provides the user with an interface to the Microprogrammed System. The Support Processor system consists of:

- The Am9080A Microprocessor to provide system control
- A dual floppy disk to hold all operating software including AMDASM/29
- A memory board consisting of 32K bytes of RAM for use by the Am9080A processor
- A serial interface for communication to a CRT Console.
- Other interfaces: Serial RS-232 communication to a printer and to a high-speed paper tape (for outputting PROM tapes). An interface is also available to a PROM Programmer.
- The Page register for holding the active page number (194 pages of 32k Bytes each can exist in memory space 8000H to FFFFH, the active page is determined by the Page register)

The Microprogrammed System consists of:

- **Writeable Control Store (WCS)** – The WCS is a 2K by 64-bit memory using low-cost 4K Static MOS RAMs (Am9130's 250nsec access). This writeable is intended for users either using slow PROM or for users using fast PROM in their final designs but wanting to verify their microprograms at a reduced system speed. A future WCS will be a 1K by 64-bit, 50ns access memory using fast (30ns access) Bipolar RAMs. This memory is designed for users wanting to simulate as close as possible the operation of fast PROMs in their system. The system will be pre-wired to accept two WCS boards. These boards can be organized to provide microprogram memory space either 128 bits wide by 2K deep or 64 bits wide by 4K deep. This pre-wiring can be modified easily by the user to accomodate additional writeable control store memory boards as necessary.
- **Instrumentation** – This board provides the logic necessary for the Support Processor to directly control the Microprogrammed System and includes clock control and microprogram address trap and branch control. Specifically, the following functions are provided:

  Clock Control – Stop, Single Step, Run, Trap on Breakpoint. Stop, Single Step, Run are under control both from the Support Processor software and the front panel. Trap on Breakpoint is under control only from the Support Processor software. A 12-bit number loaded into a register under software control is compared against the 12-bit address provided to address the writeable control store (or PROM) memory. When there is a match, the Microprogrammed System clock is stopped and an interrupt request is sent to the Support Processor.

  Branch Control – Under software control, a branch address can be forced causing the Microprogrammed System microsequencer to start executing microcode from this location. This feature can be used to provide a starting address or to jump to a diagnostic microroutine when debugging microcode.

  Monitoring – A future addition to the above features is an option to monitor a number of user-defined test points in real time. These test points will be saved in a RAM memory at the Microprogrammed System clock frequency (or some user-selectable fraction or multiple of the Microprogrammed System clock frequency) and when the Microprogrammed System clock is halted the last 256 sets of these test points can be displayed in a user-defined format on the system CRT.

- **Application Cards – The Computer Control Unit (CCU)** is one of the standard designs provided by AMD. It is discussed below in detail.

  Additional AMD designs will be provided in the future across a broad spectrum of applications. They will include, for example, a 16-bit processor which will allow the user to add his own microcode, a disk controller, a microcontroller, and an Am9080 emulation.These designs are intended to serve several functions: The designer with a requirement close to the application aimed at by the particular design can use the AMD design as is or modify it to fit the application. The designer who wants to learn about Am2900 architectures can purchase one of the AMD provided designs and can write and check out his own microprograms (i.e., the fixed-instruction Am2900-based microprocessor allows the user to add instructions by writing additional firmware).

  Universal Prototype Cards – A universal wire wrap card is provided on which to build prototype designs. This board will accommodate 0.3-, 0.4-, 0.6-, 0.7-, and 0.9-inch center I.C. sockets with excellent packing density.

The Computer Control Unit

Figure 3 illustrates the block diagram of the CCU. This unit is intended to illustrate a typical microprogrammed control unit. It is a pipelined microprogram sequencing unit designed to interface directly with System 29's Writeable Control Store. The function of this unit is as follows*.

The microprogram address is generated by Am2909/2911 Sequencers. As can be seen from Figure 3, these sequencers can select this address from several sources (i.e., from D, the external input; from R, and internal register; from the stack; or from the microprogram counter register which holds the last address sent to the microprogram memory incremented by one). The source to be used for the address is determined by the microinstruction which can select any of the above-mentioned inputs/registers as the address unconditionally or can conditionally select between two of these for microprogram branches.Table I defines the resultant address generated by this microprogram sequencer as a function of the microinstruction and the test condition. The condition to be tested using the test multiplexer is also specified by the microinstruction. This CCU uses the Am29811 Instruction Controller to generate the required controls.

In addition to selecting a particular source for the microprogram address, this sequencer can modify this value using the Am29803 16-way Branch Control tied to the "OR" inputs of the Am2909 holding the least significant four address bits. The modified address generated as a function of the microinstruction and the test inputs is listed on Table II.

*The CCU is essentially the same as the CCU described in AMD's Microprogramming Handbook, with a few changes (for one, the Mapping PROM is replaced with a mapping RAM loadable with System 29 software).

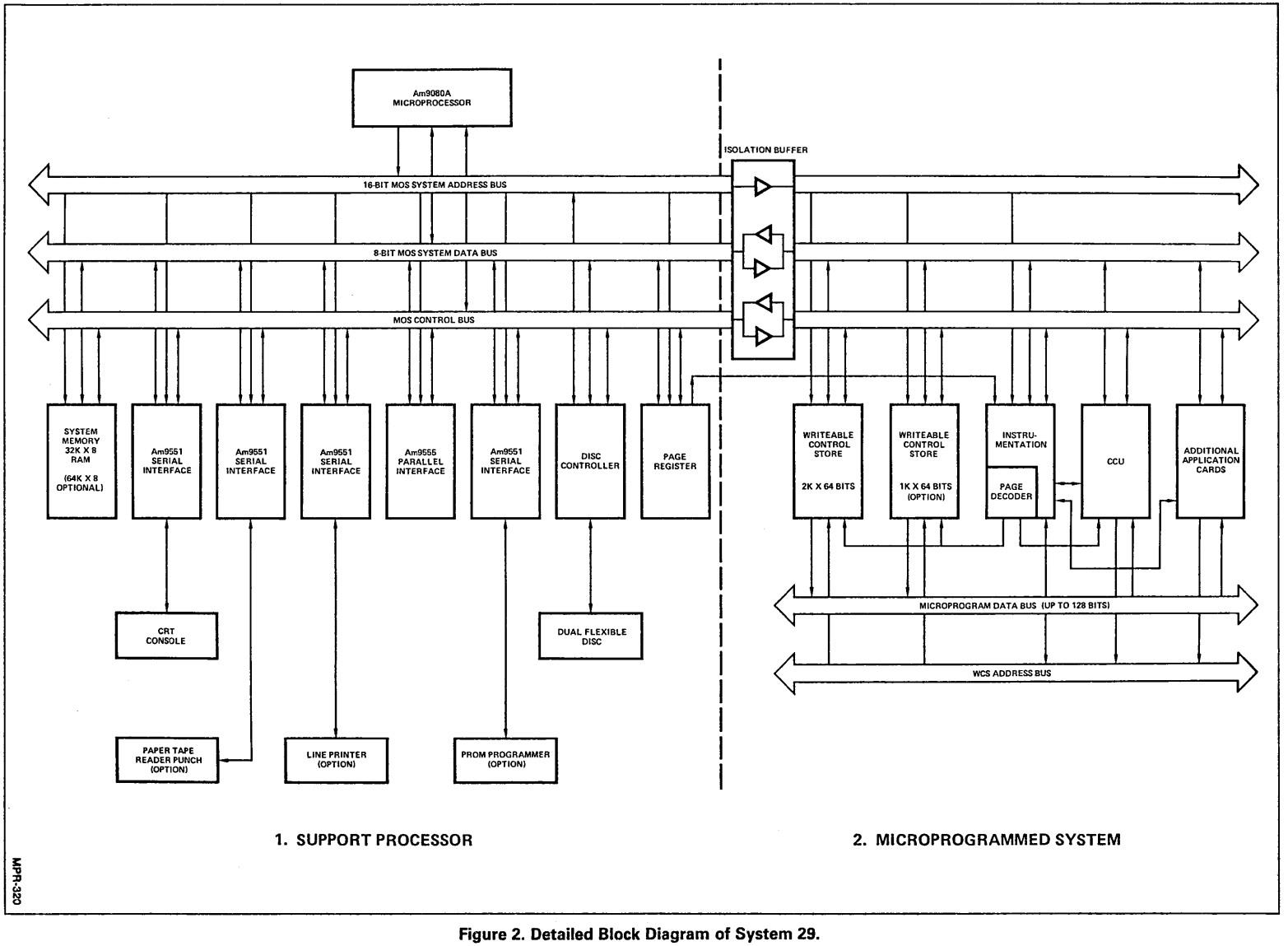


Figure 2. Detailed Block Diagram of System 29.

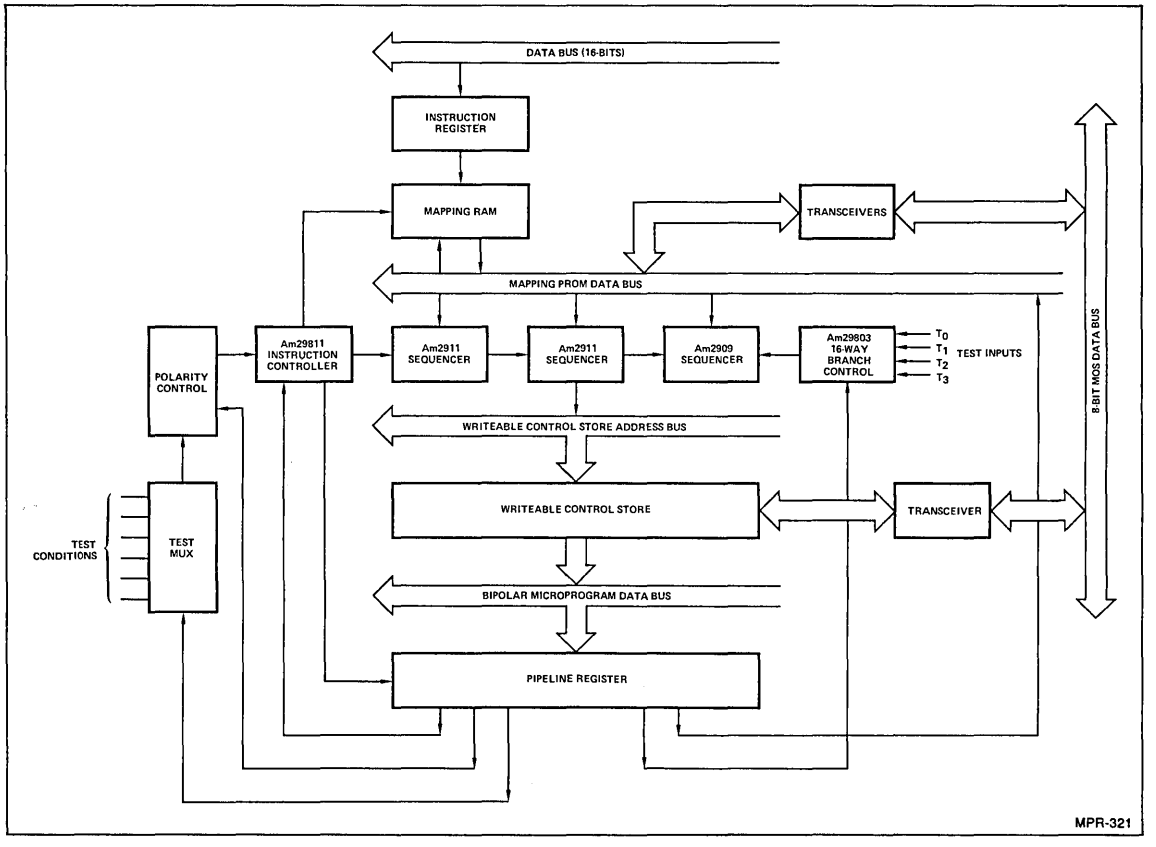


Figure 3. The Computer Control Unit Application Card.

MICROINSTRUCTION		
Mnemonic	Bit Field*	Microinstruction and Resultant Address**
JZ	L L L L	Jump to Address Zero
CJS	L L L H	Conditional Jump-to-Subroutine with Jump Address in Pipeline Register.
JMAP	L L H L	Jump to Address at Mapping PROM Output.
CJP	L L H H	Conditional Jump to Address in Pipeline Register
PUSH	L H L L	Push Stack and Conditionally Load Counter
JSRP	L H L H	Jump-to-Subroutine with Starting Address Conditionally Selected from Am2911 R-Register or Pipeline Register.
CJV	L H H L	Conditional Jump to Vector Address.
JRP	L H H H	Jump to Address Conditionally Selected from Am2911 R-Register or Pipeline Register.
RFCT	H L L L	Repeat Loop if Counter is not Equal to Zero.
RPCT	H L L H	Repeat Pipeline Address if Counter is not Equal to Zero.
CRTN	H L H L	Conditional Return-from-Subroutine.
CJPP	H L H H	Conditional Jump to Pipeline Address and Pop Stack.
LDCT	H H L L	Load Counter and Continue.
LOOP	H H L H	Test End of Loop.
CONT	H H H L	Continue to Next Address.
JP	H H H H	Jump to Pipeline Register Address.

Table 1. Computer Control Unit Instruction Set.

*L = Low, H = High

**Default address: μPC (Microprogram Counter)+1

When the D input to the Am2909/2911 is selected, the mapping RAM can be selected for the next address. This mapping RAM replaces the mapping PROM normally found at this point in the design and provides a means to map a portion of the instruction register (op code) to a starting location in the microprogram. The contents of the mapping RAM can be read or written under control of the System 29 software. This feature provides a convenient means for users to change the macroinstruction decoding of their design by modifying the contents of this RAM.

SYSTEM SOFTWARE

The software system is divided into several distinct parts. These are:

- The basic I/O system
- The disk operating system
- The console command processor
- Transient programs

Basic I/O System and Disk Operating System

Perhaps the most flexible aspect of System 29 is that it comes complete with a full disk operating system designated AMDOS/29. This disk operating system provides rapid access to programs through a comprehensive file management package. The file subsystem supports a named filed structure, allowing dynamic allocation of file space as well as sequential and random file access. This

system provides a number of program entries that allow files to be opened, closed, renamed, read, written onto disk, or searched for by name. Using this file system, a large number of distinct programs can be stored in both source and machine executable form. In addition, the disk operating system provides all operations necessary to access the diskette drives and to interface such standard peripherals as a teletype, CRT, paper tape reader/punch, PROM programmer, and other user-defined peripherals. While it is anticipated that the user will not want to modify the basic disk operating system package, the system can be tailored by the user for any particular microprogrammed hardware environment he may wish to implement by writing additional Am9080 load modules to execute under AMDOS 29.

Console Command

The console command processor reads inputs from the console device and processes these commands to provide listings of the file directory, printing the contents of various files, controlling the operations of various other standard programs supplied with AMDOS/29.

Transient Programs

The transient program area of System Memory holds programs which are loaded from the disk for execution by the system. A number of these transient programs (load modules) are provided along with the basic disk operating system. Typical of these are the programs to perform the following functions.

- **Assemble** – Loads an Am9080A assembler and assembles the specified program from the disk.
- **Status** – Provides statistical information about particular files on the disk.
- **Debugger** – Loads a debug package from the disk and allows the debugging of Am9080A programs.
- **Peripheral Interchange Program** – A program that allows media conversion operations between peripherals.
- **Editor** – Loads and executes a powerful Am9080A text editor program.
- **Batch** – Allows batch processing of various disk operating system commands.

In addition to these programs, a number of powerful microprogram generation aids are available. These include:

- **AMDASM/29™** – A two-pass microprogram assembler used to convert an established set of formats into machine language
- **AMPROM/29™** – A post-processing program that allows the user to output his binary object code in a form which corresponds with his PROM organization
- **AMSCRAM/29™** – A post-processing program that allows the user to reorganize the columns of microcode to be programmed in any PROM
- **AMMAP/29™** – The mapping PROM symbolic data assembler. Used with AMDASM, AMMAP generates microprogram entry point addresses that are loaded into the CCU mapping RAM to decode instructions and generate microprogram starting addresses.
- **Support Programs to the Microprogrammed System**

Once the microcode has been assembled and loaded into the resident Writeable Control Store (or microprogram memory) in System 29, the user will desire the capability to set breakpoints, set trap bits, set comparison values, and so forth, so that he can easily test and debug the microcode and its associated hardware. AMDOS/29 contains a powerful set of programs to allow the setting of traps as well as providing "peeking and poking" in microprogram memory. Examples of these commands are:

Display – Display the contents of memory on the console
Move – Move a block of data to one location from another location in memory
Locate – Locate a particular character sequence in memory
Store – Store hexadecimal data into memory
Verify – Compare two blocks of data in memory
Set – Sets microprogram format table attributes
Jump – Allows transferring control to any WCS memory location
Read – Read hex format paper tape
Write – Write hex format paper tape
Page – Select a particular page as the upper 32K of the Am9080A address space

The display, move, locate, store, read, and write commands will all operate upon any type of available memory; i.e., Support Processor memory or Microprogrammed System support pages (microprogram memory, Mapping PROM, instrumentation pages, etc.). Each of the commands will accept an operand which determines which page to select, should the command address the upper 32K address space.

USING SYSTEM 29

The following illustrates how System 29 is to be used during the development of microcode.

Definition Phase – After the logic design has been completed and the microcode format defined, the designer can start the microassembler definition phase. The definition phase essentially personalizes AMDASM/29 for a particular micro format. System 29 serves as an interactive keyboard terminal using the editor to build these definition files.

Assembler Phase – After the set of definitions has been created, the user can build his microcode source files using the interactive editor. Once the source file is complete, the user can assemble the microprogram using AMDASM/29. This assembly produces a binary representation of the microprogram. The output from the assembly can be listed in several different formats. When the assembly is complete, the binary file is routed to flexible disc storage for post processing.

Check-Out – Once the microcode is assembled and the system fabrication is completed, the next step is to debug the design errors, wiring errors and component failures. During this phase, System 29 serves as a check-out work station. Under control of the user, the binary microcode files can be loaded in the Writeable Control Store. During the actual check-out, System 29 provides these features to the user:

- Inspection and editing of the microcode in the writeable control stores
- Forced branches for microcode starting locations
- Microcode clock control to allow Run, Halt or Single Step of the microprogram
- Breakpoint stop (the breakpoint address or sequence of addresses are loaded from the keyboard)
- Generation and execution of trial sequences of microcode for hardware debug purposes; not necessarily a permanent part of the final machine microcode.

Function	μInstruction I_3	I_2	I_1	I_0	Test Inputs T_3	T_2	T_1	T_0	μProgram Address Least Significant 4 Bits OR_3	OR_2	OR_1	OR_0
No Test	L	L	L	L	X	X	X	X	L	L	L	L
Test T_0	L	L	L	H	X	X	X	L	L	L	L	L
					X	X	X	H	L	L	L	H
Test T_1	L	L	H	L	X	X	L	X	L	L	L	L
					X	X	H	X	L	L	L	H
Test T_0 & T_1	L	L	H	H	X	X	L	L	L	L	L	L
					X	X	L	H	L	L	L	H
					X	X	H	L	L	L	H	L
					X	X	H	H	L	L	H	H
Test T_2	L	H	L	L	X	L	X	X	L	L	L	L
					X	H	X	X	L	L	L	H
Test T_0 & T_2	L	H	L	H	X	L	X	L	L	L	L	L
					X	L	X	H	L	L	L	H
					X	H	X	L	L	L	H	L
					X	H	X	H	L	L	H	H
Test T_1 & T_2	L	H	H	L	X	L	L	X	L	L	L	L
					X	L	H	X	L	L	L	H
					X	H	L	X	L	L	H	L
					X	H	H	X	L	L	H	H
Test T_0, T_1 & T_2	L	H	H	H	X	L	L	L	L	L	L	L
					X	L	L	H	L	L	L	H
					X	L	H	L	L	L	H	L
					X	L	H	H	L	L	H	H
					X	H	L	L	L	H	L	L
					X	H	L	H	L	H	L	H
					X	H	H	L	L	H	H	L
					X	H	H	H	L	H	H	H
Test T_3	H	L	L	L	L	X	X	X	L	L	L	L
					H	X	X	X	L	L	L	H
Test T_0 & T_3	H	L	L	H	L	X	X	L	L	L	L	L
					L	X	X	H	L	L	L	H
					H	X	X	L	L	L	H	L
					H	X	X	H	L	L	H	H
Test T_1 & T_3	H	L	H	L	L	X	L	X	L	L	L	L
					L	X	H	X	L	L	L	H
					H	X	L	X	L	L	H	L
					H	X	H	X	L	L	H	H
Test T_0, T_1 & T_3	H	L	H	H	L	X	L	L	L	L	L	L
					L	X	L	H	L	L	L	H
					L	X	H	L	L	L	H	L
					L	X	H	H	L	L	H	H
					H	X	L	L	L	H	L	L
					H	X	L	H	L	H	L	H
					H	X	H	L	L	H	H	L
					H	X	H	H	L	H	H	H
Test T_2 & T_3	H	H	L	L	L	X	X	X	L	L	L	L
					L	H	X	X	L	L	L	H
					H	L	X	X	L	L	H	L
					H	H	X	X	L	L	H	H
Test T_0, T_2 & T_3	H	H	L	H	L	X	X	L	L	L	L	L
					L	X	X	H	L	L	L	H
					L	H	X	L	L	L	H	L
					L	H	X	H	L	L	H	H
					H	L	X	L	L	H	L	L
					H	L	X	H	L	H	L	H
					H	H	X	L	L	H	H	L
					H	H	X	H	L	H	H	H
Test T_1, T_2 & T_3	H	H	H	L	L	X	L	X	L	L	L	L
					L	X	H	X	L	L	L	H
					L	H	L	X	L	L	H	L
					L	H	H	X	L	L	H	H
					H	L	L	X	L	H	L	L
					H	L	H	X	L	H	L	H
					H	H	L	X	L	H	H	L
					H	H	H	X	L	H	H	H
Test T_0, T_1, T_2 & T_3	H	H	H	H	L	L	L	L	L	L	L	L
					L	L	L	H	L	L	L	H
					L	L	H	L	L	L	H	L
					L	L	H	H	L	L	H	H
					L	H	L	L	L	H	L	L
					L	H	L	H	L	H	L	H
					L	H	H	L	L	H	H	L
					L	H	H	H	L	H	H	H
					H	L	L	L	H	L	L	L
					H	L	L	H	H	L	L	H
					H	L	H	L	H	L	H	L
					H	L	H	H	H	L	H	H
					H	H	L	L	H	H	L	L
					H	H	L	H	H	H	L	H
					H	H	H	L	H	H	H	L
					H	H	H	H	H	H	H	H

L = LOW
H = HIGH
X = Don't care

Table 2. Am29803A Function Table.

The System 29 instrumentation hardware will monitor a number of test points during the sequencing of the microcode and display these test points on the CRT terminal. Examples of these are: the microword, the output of the ALU, the CPU to memory bus, designators, etc. Since the monitoring hardware is under the control of the microprocessor, the output of the monitored points can be displayed in a format convenient for the design engineer.

Post Processing – When microcode check-out has been completed, the utility program AMPROM/29 is available to punch the microcode binary on paper tape in a format appropriate for a given PROM Programmer or the output can be sent to a PROM Programmer directly.

SUMMARY

System 29 is a new development tool that greatly simplifies the prototyping and programming of all microprogrammed systems, regardless of their architectures. System 29 provides, for the first time, a well-defined, easy-to-use interface between hardware design engineers, software design engineers, and firmware design engineers resulting in the world's first complete development system for microprogrammed machines.

Advanced Micro Devices

AMDASM™ Reference Manual

This manual covers AMDASM/80, which runs on the INTEL® MDS System. With the exception of the execution commands it is also applicable to AMDASM/29, which runs on System 29, the AMD development System. Most of the features are also provided on AMDASM/TS, the time-shared version of AMDASM, available on the INFONET division of Computer Science Corporation. Separate manuals are available for the time-shared version and for AMDASM/29.

February, 1978

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CHAPTER I

INTRODUCTION AND PURPOSE

An assembler is a program which "reads" another program written in a symbolic form and produces an output of binary words corresponding to the symbolic input. A microprogram assembler is a special kind of assembler, formally called a "meta-assembler". AMDASM is a meta-assembler.

A meta-assembler differs from an ordinary assembler in that most of the symbols are defined by the user prior to the assembly process itself. In an ordinary assembler, the user may define labels for instructions and symbols for particular data words, but the instructions themselves, including their associated word length and format, are generally already defined by the assembler. This makes perfectly good sense in an ordinary assembler, since the assembler is designed to convert an established set of formats into machine language (ones and zeros) for a particular machine such as the AMD Am9080A.

A microprogram assembler, however, must be far more flexible than a traditional assembler, since it must be useful for many hardware configurations. Each different hardware configuration may require a different format and may require word lengths (microinstructions) over 100 bits.

Moreover, in a microassembler, a format rarely establishes the entire contents of a microinstruction, but rather defines only a few bits of the total word.

These requirements imply that a microprogram assembler must consist of two distinct operations. The first operation is establishment of word length and definition of formats and constants (the Definition File). The second operation is the traditional assembly process (Assembly File) performed on a program that uses the formats and constants from the Definition File. The microprogram assembler, therefore, differs from the traditional assembler in that it may be configured, by the user, to accept any word size, formats and constants the user desires.

The assembler written by Advanced Micro Devices is a very powerful meta-assembler, useful not only with the AMD 2900 family, but with any microprogrammed machine. The assembler operates in two phases, the Definition Phase (PHASE1) and the Assembly Phase (PHASE2).

The Assembly Phase is much like any assembler. It reads a symbolic program, handles most common assembler features such as labeling and setting the address counter, and produces a binary output and various listings and cross-reference tables. The Definition Phase is executed first to set up the table which associates the user's format names and constant names with their corresponding bit patterns.

The Definition Phase lets the user define symbols for formats (format names), symbols for constants (constant names), and the microinstruction word length. In the Definition File the length of the microinstruction is defined first. The word may be any length from 1 to 128 bits. This is adequate for all but the most sophisticated processors.

Each of the user defined symbols has a specific bit pattern associated with it. A format name is used to define all, or part, of one microinstruction. The format definition may consist of:

- Numeric fields, which are defined to contain specific bit patterns.
- Variables, which will be filled in when the format is invoked.
- "Don't care" states.

Once the Definition Phase has been executed, its output may be retained and used by future programs.

A useful feature of the AMD assembler is that "don't care" states are retained until defined, which may not happen until after the assembly process, during a third, or post processing, phase. A listing of the microprogram at the conclusion of assembly shows an 'X' for every undefined bit. This is extremely useful during the development process before the microword length has been optimized by sharing fields.

Following assembly of the user's program, a file is retained which contains the assembled microprogram. This file is then available for post processing to create paper tapes for PROM blowers. The output utility can select columns and rows for a given PROM tape, freeing the user from any restrictions regarding the organization of the microprogram memory, and simplifying the generation of a new tape for each of the many PROMs in the system.

The program to be assembled may be written using any of the features specified during the Definition Phase. In the simplest case, the Assembly Phase source program might be written using just strings of ones and zeros, with the Definition Phase consisting only of the microinstruction word length. At the other extreme, the Assembly Phase source program may refer to multiple format names from the Definition Phase for each microinstruction. Any number of formats may be overlayed to define a single microinstruction, as long as the defined or variable fields of each format fall into the "don't care" fields of the other formats invoked. A user might define, for example, a set of formats specifying sequence control operations, another set for data control, and a third set for memory control.

The AMD assembler has been written to maximize its flexibility and ease of use for hardware designers. Every effort has been made to make the program efficient on the machine and efficient at the human interface, with a minimal knowledge of the host machine's operating system required.

NOTE: Throughout this manual examples often refer to the Am2900 Learning and Evaluation Kit shown in Chapter V.

CHARACTER SET

The following characters are legal in AMDASM source statements:

- The letters of the Alphabet, A through Z. Both upper-and lower-case letters are allowed. Internally, AMDASM treats all letters as though they were upper-case, but the characters are printed exactly as they were input in the source files.
- The digits 0 through 9
- The following special characters:

Character	Meaning
+	Plus sign
–	Minus sign
*	Asterisk
/	Slash
,	Comma
(	Left parenthesis
)	Right parenthesis
&	Ampersand
:	Colon
$	Dollar sign
%	Percent sign
Δ	Blank or space
;	Semicolon
.	Period
(CR)	Carriage return
(HT)	Horizontal tab

DEFINITION OF TERMS

Since there are no standard terms associated with microassemblers, the more common terms used in this manual are listed below:

Term	Definition
Δ	Indicates a **required** blank character.
Name or label	1-8 characters which are assigned a value by the programmer or the assembly process. Labels are used only in the Assembly File.
Constant	A specific pattern of 1-16 bits.
Constant name	A name for a constant.
Field	A group of adjacent bits in a microinstruction.
Format	A model for a microinstruction consisting of fields which contain constants, variables, and "don't cares".
Format name	A name for a format.
Line	An input line of up to 128 characters on a console, teletype, a paper tape reader, or a diskette file.
Modifiers	Symbols (* % : – $) which indicate that the data given for a field is to be modified.
Attribute	A modifier which is permanently associated with a field.
Designator	A symbol (V, X, B#, Q#, D#, or H#) which indicates the type of field or constant: variable (V), "don't care" (X), binary (B#), octal (Q#), decimal (D#), or hexadecimal (H#).
Delimiters	A symbol (: Δ = , /) which indicates the end of a name (: Δ =), the end of a field (,), or the continuation of a statement (/) on another line.
Default values	The value which will be substituted if an explicit value is not specified.
Options	Choices available which indicate the input and output devices to be used, the type of output listing desired, and processing of one or both phases (Definition and Assembly).
{ }	Braces indicate that the enclosed parameter is optional.
(CR)	Carriage Return

DEFINITION PHASE (PHASE1)

The AMDASM Definition Phase includes the following features:

- A name is a packed group of 1 to 8 characters.
- A name may be assigned to a constant value.
- A name may be used to define a format whose fields are given as variables, "don't cares", explicit bit patterns (values), or specific addresses by using appropriate designators.
- Blanks may be used to improve readability.
- Microword length may be 1 to 128 bits.
- Modifiers include inversion, truncation, negation, and designation of a field as an address field to be right-justified (placing a value in a field at the right with leading bits set to zero).
- The ability to set a "page" size via the attribute $. This permits error detection when the Assembly Phase calls for a jump or branch to an address which is on a different "page" of the microcode.

Data from the Definition Phase may be retained for use with subsequent Assembly Phase source programs and/or it may be modified as desired.

ASSEMBLY PHASE (PHASE2)

The Assembly Phase provides for input of the microprogram source statements, conversion of format and constant names to their appropriate bit patterns, substitution of values for variable fields in the format, and generation of listing and binary output. The assembly source program will use references to format names and constant names from the Definition File. It will also contain statements which associate labels with addresses, control assembler operation, and provide program location counter control.

The assembly process provides the user with the following features:

- A microword may be assembled by referring to one or more format names from the Definition File.
- A microword whose format was not specified in the Definition File may be specified by using the built-in free-form format command.
- The programmer may control the program location counter to set the origin and/or to reserve storage.
- The programmer may choose one of four different output listing formats.
- A constant or a variable field may be defined using values and/or expressions.
- Errors are detected and listed. Severe errors cause processing to halt.

Output of the Assembly Phase is an object file which contains the complete microprogram. Post processors can directly convert this object file to any form needed, such as hexadecimal or BNPF punched on paper tape.

IMPLEMENTATION

AMDASM/29 operates on the Advanced Micro Devices' System 29 under the AMDOS/29 Operating System. AMDASM/80 operates on the Intel Intellec® MDS-DOS System under the ISIS-II® operating system.

ASSEMBLER OPERATION

AMDASM is placed into execution by control statements from the console input device.

The Definition File is processed in PHASE1 and if it contains no errors the Assembly Phase begins. PHASE2 Pass 1 assigns values to Assembly File labels and allocates storage. PHASE2 Pass 2 translates the Assembly File source program into object code.

User-selected options determine whether the Definition Phase is to be executed or if a previous execution of that phase has already established the table of formats on a file which will be used by the assembly process.

The AMDOS/29 operating system allocates all necessary input and output resources, such as files, automatically.

CHAPTER II

DEFINITION PHASE (PHASE1)

The Definition Phase allows the user to define the microword length, constants, and formats which he will use to write source programs for his target machine.

DEFINITION FILE

The definitions are input via a sequence of instructions called the Definition File whose content includes the following items:

TITLE (heading to be printed on output listing)
WORD n (defines microinstruction word length)

Printing control statements
Definition statements
Comment statements

END

The control statement WORD must appear as the first statement in the Definition File after the optional TITLE statement. The END statement must be the last statement in the Definition File.

The other statements (shown boxed) may be interspersed throughout the body of the file.

To facilitate readability, blanks may appear in most parts of these statements, although no blanks are permitted between the letters of the control words TITLE, WORD, END, LIST, NOLIST, DEF, EQU, or SUB. An entire blank line may be inserted by entering a semicolon and a carriage return.

TITLE

If the user wishes to have a title printed on his Definition File statements, the first statement input should be TITLE. The general form is:

Form:
TITLEΔ title desired by user

TITLE must:

- Begin on a new line
- Be followed by a blank and a maximum of 60 characters.

WORD

WORD must be the first statement input by the user after the optional TITLE is given. Its general form is:

Form:
WORDΔn

WORDΔ must be followed by a decimal integer value n which indicates the microword size in bits (range 1−128).

WORD must:

- Be followed by at least one blank and 1 to 3 decimal digits.
- Be the first input line (second input line if TITLE was used).
- Begin on a separate line.

If WORD is omitted, assembly will halt as the Definition Phase must know the size of the microword in order to proceed.

END

END indicates the end of the Definition File. If END is omitted an error message will be printed but processing will continue. The general form is:

Form:
END

END must:

- Begin on a new line.
- Be the last statement in the Definition File.
- Be followed by a carriage return.

PRINTING CONTROL STATEMENTS

Printing control statements are used to control printing.

TITLE was listed separately since it must be the first statement input if it is to be printed at the top of the first page of the output. TITLE may be used elsewhere (i.e., interspersed with the statements shown in the box) in which case it causes this new title to printed at that position in the output file.

A description of the other printing control statements, LIST, NOLIST, EJECT and SPACE, follows:

LIST

LIST indicates that the following statements are to be printed whenever printing of the Definition File input is requested. This feature will be most useful when correcting or modifying a Definition File. (AMDASM selects LIST as the default option. NOLIST must be specified if the user does not wish to print his Definition File source statements.) The general form is:

Form:
LIST

LIST must:

- Begin on a new line.
- Be followed by a carriage return.
- Precede the Definition File statements which are to be printed.
- Be interspersed between complete definition statements.

NOLIST

NOLIST turns printing off, and no printing of the Definition File input statements will occur until LIST is encountered. However, *any source statement containing an error will still be listed.*

Form:
NOLIST

NOLIST must:

- Begin on a new line.
- Be followed by a carriage return.
- Precede the Definition File statements which are not to be listed.
- Be interspersed between complete source statements.

SPACE

SPACE indicates that the assembler is to leave n blank lines before printing the next source statement. The general form is:

Form:
SPACEΔ n

SPACE must:

- Begin on a new line.
- Be followed by Δ and a decimal digit indicating the number of succeeding lines to be left blank.
- Be inserted in the Definition File at the point where the spaces are desired.

EJECT

When EJECT is encountered, the assembler generates blank lines on a list device so that any previous lines plus the blank lines equals the specified "page" length (default is 66 lines). It then begins a new "page", headed with the title. On a printer a new page is ejected. The general form is:

Form:
EJECT

EJECT must:

- Begin on a new line.
- Be followed by a carriage return.

DEFINITION STATEMENTS

Definition statements are used to define constants, full microword formats, or partial microword formats. The general form of these statements is:

Form:
name: definition wordΔ field1, field2, . . ., fieldn or constant

DEFINITION WORDS

The definition words and their functions are:

EQU is used to set a name equal to a bit pattern
DEF is used to define a format for a microinstruction
SUB is used to define a format for part of a microinstruction

A complete explanation follows the section defining fields, designators and constants (page 5).

FIELDS

A field is a contiguous group of bits in a microinstruction (such as branch address, next instruction control, etc.). Each field may be one of three types:

- A constant field whose content is a fixed value or a fixed bit pattern, (for example, the next instruction control).
- A variable field whose content will contain different bit patterns in different situations (for example, an address field).
- A don't care field whose content is not used in this format (for example, the address field for a continue instruction).

The type of data in a particular field is indicated by using "designators".

DESIGNATORS

Permissable designators and their meanings are:

Designator	Meaning	Example
B#	A constant or field whose contents will be represented using binary digits (0 and 1). Each digit has an implicit length of one bit.	B#101 (three bits 101).
Q#	A constant or field whose contents will be represented using octal digits (0 through 7). Each digit has an implicit length of three bits.	Q#32 (six bits 011010).
D#	A constant or field whose contents will be represented using decimal digits (0 through 9). For a constant name definition using EQU, the implicit length for decimal numbers is the number of bits needed to represent the number in binary. Thus, D#3 has an implicit length of 2, D#4 has an implicit length of 3. For fields in a format (DEF or SUB), the D# must be preceded by decimal digit(s) giving an explicit length (number of bits) for the field.	D#4 (three bits 100) 3D#6 (three bits 110)
H#	A constant or field whose contents will be represented using hexadecimal digits (0 through 9, A through F). Each digit has an implicit length of four bits.	H#8A (eight bits 10001010)
X	A "don't care" field. X must be preceded by decimal digit(s) giving an explicit length for this field (i.e., the bit length).	4X (4 bit "don't care" field).
V	A variable field. V must be preceded by a decimal digit(s) giving an explicit length for this field (i.e., the bit length). When a designator B#, Q#, D# or H# is given after a V, it becomes a permanent attribute of that field and the assembler assumes that any value specified for that field will be given in digits appropriate to that designator. These permanent designators for variable fields may be overridden when using the format during the Assembly Phase. **If a variable field has no designator given, it defaults to binary.** For example, if all variable fields are given as nVQ# in the Definition Phase, all values for this variable field that are octal may be written during the Assembly Phase by writing only the necessary octal digits. The content of a variable field may be given during the Definition Phase. The V designator may be followed by the B#, Q#, D#, or H# and these may be followed by appropriate digits called the default value for this field. Thus, 6VQ# indicates a 6-bit variable field whose contents will be given in octal. 6VQ#35 indicates that if no value is substituted in the Assembly Phase, this variable field should assume the default value 011101.	6V (six bit variable field).

NOTE: The designators B#, Q#, D#, H# must have no blanks between the letter and the #. The desired value for the field is then given in the appropriate digits as shown in the examples.

FIELD RULES

Each field following a definition word must:

- Contain a maximum of 16 bits unless it is a "don't care" field.
- Be followed by a comma unless it is the last or only field following the definition word.
- Define a constant field using the designators B#, Q#, D#, or H# and the appropriate digits.

or

- Be a variable which gives a bit length and the designator V. If no designator follows the V, the field type defaults to binary.

or

- Be a "don't care" which contains a bit length and the designator X.

or

- Be a constant name or subformat name which has been previously defined.

NAMES

Names may be user-defined constant names, format names, or subformat names.

Names must:

- Be the first element in a statement.
- Begin with an alphabetic character (A-Z) or a period (.).
- Be terminated by a colon (:).
- Contain a maximum of 8 characters not including the colon.
- Not contain any embedded blanks.
- Be followed by EQU, DEF or SUB.
- Contain only alphabetic characters (A-Z), a period (.) or the digits (0 through 9) in positions 2 through 8.

Names may:

- Contain more than 8 characters but will be truncated after the first 8 characters.
- Be preceded by blanks.
- Be followed by blanks after the : and before the EQU, SUB, or DEF.

Examples of proper names are:

NUMBER:
. SHIFT:
REG.3:

Improper names are:

*ADD	(special character used)
SHIFT LEFT:	(embedded blank, more than 8 characters)
3MUXCNTL:	(first character not A through Z or period)

CONSTANTS

Constants are used to associate a name with a value or to define a specified fixed bit pattern.

Constants may be expressed by using designators and the appropriate digits.

For example

Q#62

defines the bit pattern 110010. This type of constant has an implicit bit length of 6 bits (each octal digit represents 3 bits).

If a decimal digit precedes the designator, as for example in

4H#5

the 4 represents the explicit length of the field, and the bit pattern is 0101.

Explicit and implicit lengths are more fully defined later in this chapter.

Constants must be represented in 16 bits (i.e., $2^{16} - 1$ maximum). The permissible forms for constants are:

Form		Permissible Digits	Meaning
	n	0 through 9	Decimal value (default form)
i	B#n	0 or 1	Binary value
i	Q#n	0 through 7	Octal value
i	D#n	0 through 9	Decimal value
i	H#n	0 through 9 or A through F	Hexadecimal value

where i represents optional digits specifying the explicit length.

EXPRESSIONS

Any field may contain an expression. The expression may use designators and/or digits or labels as well as operators.

Operators permitted in expressions are:

Operator	Description
+	Add the value of the left operand to the value of the operand on the right of +
–	Subtract the value of the operand to the right of the minus (–) from the value of the operand on the left
*	Multiply the left operand by the right operand
/	Divide the operand on the left (dividend) by the operand on the right (divisor)

All expressions:

- *Are evaluated from left to right. There is no hierarchy for the operators and no parenthesis for nesting are permitted.*
- Must result in a value which is a positive constant.
- Are calculated using integers; remainders are discarded.

DEFINITION WORDS

The definition words EQU, DEF and SUB are described in detail in this section.

EQU

EQU is used to equate a constant name to a constant value or expression. The general form is:

Form:
name: EQUΔ constant (or expression)

This equates the characters given in the name position to the value of the constant or expression. Only one expression or constant is permitted following the EQU.

The following sets the name R12 equal to the bit pattern 1100:

R12:EQUΔH#C

Future references to the bit pattern 1100 (register 12) may be made by using the name R12.

The default type is decimal if no designator follows the EQU. (R10:EQUΔ10 assumes the bit pattern 1010, implicit length 4 bits).

Each EQU must:

- Begin on a new line.
- Begin with a name:
- The name: must be followed by EQUΔ (blanks between : and EQU are optional).
- Contain a constant, expression or a constant name which represents a bit pattern.
- Define a value which can be represented in 16 bits (2^{16} −1 maximum).

Each EQU may:

- Be followed by a semicolon and comment after the constant or expression.
- Be continued on additional lines by using / (slash) as the first nonblank character in those lines.
- Be used in the Assembly File as well as in the Definition File.

DEF

DEF is used to define a complete microword format establishing the contents of unvarying portions of the microword and establishing the position and length of variable and "don't care" fields. In addition, default values for variable portions of the word may be specified. The general form is:

Form:
name: DEFΔ field1, field2, . . ., fieldn

Each DEF must:

- Begin on a new line
- Be preceded by a name:
- Be followed by one or more blanks, then fields separated by commas.
- Have the sum of the lengths of all fields exactly equal the microword length specified by WORD.
- Begin on a new line
- Specify every bit in the microword in terms of constants, "don't cares", or variables.

A DEF may:

- Contain blanks between name: and DEFΔ.
- Be continued on additional lines by using a / (slash) as the first nonblank character in those lines.
- Be followed by a semicolon and a comment after any full field is defined.
- Contain (in any field) a subformat name or constant name which has been PREVIOUSLY defined.
- Contain a variable, "don't care", constant or expression in any field.
- Contain a variable field which specifies a default value for the field. The default value may be a constant or a "don't care".
- Be overlayed on "don't care" fields with another format to obtain a complete microword during the Assembly Phase. Overlaying on other than "don't care" fields will result in errors, so this feature must be used with care.

SUB

SUB is used to define a subformat which is the format of a portion of the microword. A subformat is the same as a format except that it contains fewer bits than the full microword. The fields may be constants, variables or "don't cares". Its general form is:

Form:
name: SUBΔ field1, field2, . . , fieldn

Each SUB must:

- Be preceded by a name:
- Be followed by one or more blanks, then fields separated by commas.
- Precede the DEF in which it is first referenced.
- Begin on a new line.
- Not be used in the Assembly File.

A SUB may:

- Be less than a microword length in bits.
- Be continued on additional lines by using / (slash) as the first nonblank character in those lines.
- Be followed by a semicolon and a comment after any complete field.
- Contain (for any field) a constant name that was PREVIOUSLY defined, or a constant, expression, variable, or "don't care" specification.

A SUB will be useful when several formats contain identical adjacent fields. In this case, the subformat name may be used in each DEF whenever these fields occur.

EXAMPLES OF EQU, SUB, DEF

An EQU is used to associate a bit pattern with a symbol (constant name); one example is:

```
R2: EQUΔ B#010
```

This defines the name R2 as a 3-bit constant with the bit pattern 010. Whenever the symbol R2 is used, the bit pattern 010 will be substituted.

A SUB might be:

```
SHFTRT:SUBΔ 3V, B#10110, 5X
```

This defines SHFTRT as a subformat with a 3-bit variable field (3V), a 5-bit constant field (B#10110), and a 5-bit "don't care" field (5X) for a total of 13 bits.

A DEF is used to associate bit patterns with a symbol (format name). One example is:

```
ADD: DEFΔ 3V, B#10110, 5X, B#0011, 4X, B#010
```

This defines ADD as a format with a 3-bit variable field (3V), a 5-bit constant field (B#10110), a 5-bit "don't care" field (5X), a 4-bit constant field (B#0011), a 4-bit "don't care" field (4X), and a 3-bit constant field (B#010). This gives a total microword length of 24 bits.

Alternatively, the same format name could be written using the subformat name (SHFTRT) and the constant name (R2) previously defined by writing:

```
ADD: DEFΔ SHFTRT, B#0011, 4X, R2
```

Another example of an EQU is:

```
TWOK: EQUΔ 2048
```

This assigns the bit pattern 100000000000 and a length of 12 bits to the name TWOK. The 2048 is assumed to be decimal and the length is taken from the rightmost bit through the leftmost bit in which a 1 appears.

Thus,

```
EIGHT: EQUΔ 8
```

yields the bit pattern 1000 with a length of 4

Alternatively, by using different designators, the constant

```
TWOK: EQUΔ 2048
```

could be written:

```
TWOK: EQUΔ B#100000000000
TWOK: EQUΔ Q#4000
TWOK: EQUΔ H#800
```

All of these yield the bit pattern 100000000000 and a length of 12.

FIELD LENGTHS

Each field may be given an explicit or implicit length. An explicit length is indicated for a field by using decimal digit(s) before the designator. The maximum length is 16 bits except for don't care fields whose maximum length is the microword size.

Thus,

```
3B#101
```

indicates a field with an explicit length of 3 bits.

Decimal, variable or "don't care" designators **require** an explicit length before the designator D#, V or X.

"Don't care" or variable fields **require** an explicit length since they do not, necessarily, initially contain a definite bit pattern.

Decimal **fields** in a format or subformat require an explicit length since there is no direct correlation between the number of decimal digits given and the number of binary bits desired for this field.

Example	Description
4V	Defines a variable field with the explicit length of 4 bits.
5D#16	Defines a constant field with the explicit length of 5 bits and the bit pattern 10000.
R3:EQUΔ5	Defines a constant using the default type decimal, value 5. The implicit bit length is 3.

CONSTANT LENGTHS

A constant may have an implicit or an explicit length. An explicit length is given by placing the bit length (in decimal digits) before the designator. Thus,

```
B:EQUΔ4D#8
```

has an explicit length of 4 and the bit pattern 1000.

If an explicit length is not given, the constant is assigned an implicit length determined by the designator used.

Table 2-1
Implicit Length Attributes of Constants

Constant	Implicit Length	Binary Value	Description
AB:EQUΔB#1000	4	1000	Each binary digit yields an implicit length of 1 bit per digit.
BB:EQUΔQ#10	6	001 000	Each octal digit yields an implicit length of 3 bits per digit.
CB:EQUΔH#10	8	0001 0000	Each hexadecimal digit yields an implicit length of 4 bits per digit
DB:EQUΔ12	4	1100	The 12 is assumed to be decimal, and the implicit length is counted from the rightmost bit through the leftmost 1.
EB:EQUΔ4	3	100	Same as above. Implicit length 3.

CONTINUATION

Any statement may be continued on additional lines by placing a / (slash) as the first nonblank character in those lines.

A continuation must:

- Have a slash as the first nonblank character in its line.
- Preferably be indicated after a complete field (including the comma) has been given on the preceding line.
- Never occur between the designators B, D, Q, or H, and the # sign.

Examples are:

```
SHFTRT: SUBΔ 3V, B#10110,
/5X

ADD: DEFΔ 3V, B#10110, 5X,
/B#0011, 4X, B#010
```

COMMENT STATEMENTS

A comment statement is used to provide information about program variables or program flow. The general form is:

Form:
; comment text

A comment may be a full or a partial line. All data from the semicolon to the end of the input line is ignored by the assembler.

Comments must:

- Begin with a semicolon.
- Be placed after a complete field if used within a DEF or SUB, in which case subsequent fields for that DEF or SUB must begin on a new line with a / (slash) indicating that they are a continuation of this DEF or SUB.

For example:

```
1. SHFTRT: SUBΔ 3V, ; this is a shift right subformat
2. / B# 10110, 5X; which is continued on a second line
3. ; the ADD given below is a complete microword format
4. ADD: DEFΔ SHFTRT, B#0011, 4X, R2
5. ; total number of bits for SHFTRT is 13
6. ; the bit pattern for SHFTRT will be substituted
7. ; in the ADD given above
```

Statements 3, 5, 6, and 7 are full comment lines. Statements 1 and 2 are statements to be processed but all characters after the 'semicolon' will be treated as comments. The SUB begun in statement 1 is continued in statement 2 where '/' indicates continuation.

MODIFIERS AND ATTRIBUTES

Modifiers are placed after a constant or after the designator V. When placed after a constant they alter only the value given. When used after a V, the modifiers are called attributes of that field and are permanently associated with the field. Attributes will modify any default value given with the variable field in the Definition File and they will modify any value substituted for this variable field when the format name is used in the Assembly File.

Permitted modifiers and their actions are:

Modifier	Action Performed on Constants or Default Values
*	Inversion (one's complement)
–	Negate the number (two's complement)
:	Truncate on the left to make the value given fit into the number of explicit bits for this field.
%	This field is to be considered an address field. Any value given is to be right-justified in the field and any bits remaining on the left are to be filled with zeros.
$	The field is treated as an address within a "paged" memory organization. This attribute permits substitution in this regard and initiates out-of-bounds page checking logic. Used only with variable fields as an attribute (may not follow a default value).

Examples of correct use of modifiers with constants:

Example	Description
D#5*	Yields bit pattern 010 (101 (5) is inverted).
B#0101–	Yields bit pattern 1011 (0101 is two's complemented).
6Q#357:	Yields bit pattern 101 111 (the left bits 011 (3) are truncated).
12H#A5%	Yields bit pattern 0000 1010 0101 (the A5 is right justified in a 12 bit field).

Examples of incorrect fields due to ommision of modifiers:

Example	Description
4B#101	Explicit length is 4 bits, only 3 bits follow the B# but no % sign (indicating right justification) is given.
5Q#34	Explicit length is 5 bits but the 34 generates 6 bits and no : has been given to indicate that the leftmost bit is to be truncated.

Modifiers must:

- Appear after the value of a constant (i.e., 12H#4C% or 5Q#37:).
- Appear after the V but before the (optional) default value for a variable field (12V%Q#46), if they are to be permanent attributes of the field. The % and the Q# become permanent attributes of this variable field and are also modifiers of the default value. To modify only the default value, modifiers must follow the value (12VQ#46%).
- Not appear with "don't cares" (e.g., 3X% is illegal).

The modifiers * and – may not both be used for the same field.

A more detailed description and examples are given in Chapter III.

MODIFIER PRECEDENCE

Modifiers or attributes may appear in any order but will always be processed in the following order:

Modifier	Description
* or–	Inversion or negation
%	Right justification
:	Truncation
$	Paged addressing

DESIGNATORS AS ATTRIBUTES

Variable fields may use the B#, Q#, D# and H# as attributes. Once given, B#, Q#, D# and H# are permanently associated with that variable field unless overridden. If a variable field has no radix base specified, it will **default to binary.**

If the user always wants to input assembly variables in octal, each variable field in the Definition Phase should be written as nVQ#. Then, in the Assembly Phase the value for this field may be given as, 27, and the program will assume that these are octal digits. If, in the Assembly File, octal is not desired, the field in the Assembly File program could be written as B#010111, or H#27, etc., to override the octal attribute.

If a variable field is defined with a default value (4VH#C), the designator (H#) becomes an attribute of that field.

The attribute H#, if given with a variable field in the Definition File, may need to be repeated in the Assembly File. This is necessary since the program can not distinguish hexadecimal values which begin with A through F from names, which may also begin with the letters A through F.

$ ATTRIBUTE

The $ attribute may be used only with variable fields to indicate paged addressing.

When the $ is given with a variable field, the % and : attributes are automatically set for that field.

The $ will indicate that this is a field whose remaining upper (leftmost) bits are to be truncated and compared with the corresponding bits of the current Program Counter.

If the truncated bits do not agree with the corresponding bits of the PC, an error occurs.

The desired length of the "page" is determined by the number of bits given as the width of this variable field.

Thus, if a "page" is to be 256 words deep, the variable field would be defined as 8V$. Any value substituted for this field will be truncated on the left and the remaining eight right-hand bits will be substituted into the field. If the truncated left bits do not agree with the corresponding bits of the current program counter value, the substitution would attempt to produce a jump to another page; thus an error message is generated.

"DON'T CARES"

A "don't care" is used to indicate the bits (a field) whose state (bit pattern) is irrelevant in this microword instruction.

The general form is:

Form:
nX

where

n is the number of bits (in decimal), and X indicates "don't care".

"Don't cares":

- Are printed as an X in the Assembly Phase output.
- May be assigned the value 0 or 1 during the post processing phase.
- Are the only fields which may be greater than 16 bits in length.
- Are the only fields in a format which may be overlayed (or'ed) with another format which contains a constant in the same field.

VARIABLES

Variables are used to define microword fields whose contents need not be assigned until assembly time. A variable field may be assigned a default value in the Definition File. The general forms are:

Form:
nV
nV attributes
nV attributes default-value
nV attributes default-value modifiers
nV default-value modifiers

A variable field must:

- Be preceded by an explicit length (n) which gives (in decimal) the bit length of the field. (n ≤ 16)
- Contain a V after the length.
- End with a comma (,) if another field follows it.
- Contain a % after the V if an expression or the program counter is to be used as a substitute for this field in the Assembly File.

A variable field may:

- Contain attributes (immediately after the V), such as inversion (*), which will always invert any value given for this field.
- Contain a designator given with or without a default value which will automatically determine the default type for this field.
- Contain a default value given in binary indicated by (B#), octal (Q#), hexadecimal (H#), or decimal (D#) followed by the desired digits.
- Contain modifiers after the default value. These modify **only** the default value and are not permanently associated with this variable field.
- Contain a default value given as X (indicating "don't care") if the user wishes to overlay this field during the Assembly Phase.
- Contain **either** a default value of "don't care" **or** an explicit default value (bit pattern) but not both.

Examples of the correct use of variable fields with a default value of "don't care" are:

3VX
3V*X
3V$X
3V*$X

EXAMPLES OF VARIABLE FIELDS

Field Content	Meaning
3V	A 3-bit field. The content is variable and will be supplied when this format name is used in the Assembly File. The field type defaults to binary.
3VQ#	A 3-bit field whose content is variable. The content will be supplied when the format name is used during the Assembly File. The content may then be given as one octal digit without using the designator Q#. If the content is to be given in binary, decimal, etc., then the designator B# or D# would be placed before the digit(s) given in the Assembly File.
3V*%	A 3-bit field whose content is variable. Any value given for this field within the Assembly File will automatically be inverted and right-justified. Since no designator is given, the field defaults to binary. If the content is to be given in octal, etc. in the Assembly File, the appropriate designator (Q#, H#, D#) must precede the digit(s).
3VQ#5	A 3-bit field whose content is variable. If no value is specified for this field in the Assembly File, it will assume the default value (specified as Q#5) bit pattern 101.
3VQ#5*	Is the same as above but the 5 is inverted to yield the bit pattern 010. Values *substituted* for this field during the Assembly File are not automatically inverted.
3V*Q#5	Yields the same pattern as 3VQ#5*but, in addition, any value substituted during the Assembly File for this field will also be automatically inverted since the * follows the V rather than the 5.
3V*Q#5*	Yields a 3-bit variable field with a default value of 5, inverted, then inverted again by the * following the V. The resulting bit pattern is 101. Any value substituted for this field in the Assembly File will be inverted.

To summarize, attributes placed immediately after the V are permanently attached to this field and will operate on any default value given with the field as well as any value substituted for the field in the Assembly File.

Modifiers placed after a default value apply only to the default value.

Examples of incorrect variable fields are:

Field Content	Description
3VH#7	The H#7 yields 4 bits. No : was given to indicate that the left bit should be truncated to fit the 3-bit field.
3:VH#7	The : is in an incorrect position. It should be 3V:H#7 or 3VH#7: (depending on whether the truncation is a permanent field attribute or a modifier of the default value H#7).

In short, attributes must be placed immediately after the V. Modifiers must be placed immediately after the digits given for the default value.

DEFINITION FILE RESERVED WORDS

The following words are used during the assembly phase as assembler control statements and may not be used as format names or constant names in the Definition File :

ALIGN	EQU	NOLIST	SPACE
EJECT	FF	ORG	TITLE
END	LIST	RES	

SAMPLE DEFINITIONS

Some possible ways of defining a few of the fields and formats for the Am2900 Learning and Evaluation Kit (see Figure 5-2) are:

```
R2:EQUΔH#2  }
R11:EQUΔH#B } Registers

CONT:DEFΔ4X, B#0010,24X          } Next instruction
BREGFEQ0:DEFΔ4VH#,4D#12,24X      } control
```

Registers 2 and 11 are defined as 4 bits, with the assigned values 2 (0010) and 11 (1011), respectively.

CONT (continue) defines only the four bits (shown as 27-24 in Figure 5-2) with the pattern 0010. All other bits are left as don't cares.

BREGFEQ0 (Branch Register if F = 0) defines the four bits (bit numbers 31-28 in Figure 5-2) as a variable field, to be given a value during the Assembly Phase using hexadecimal digits. The next four bits (bit numbers 27-24 in Figure 5-2) are given the constant pattern 1100 (value 12). All other bits are don't cares.

NUMBER OF PERMITTED EQUs, DEFs, AND SUBs

There is no fixed maximum number of EQUs, DEFs or SUBs because AMDASM stores all data dynamically. The user of a 32K-byte system has available, in PHASE1, approximately 10K bytes for variable storage; PHASE2 has approximately 8K bytes.

PHASE1 allocates:
- 12 bytes for each EQU
- 12 bytes for each format or subformat name
- 4 bytes for each field in a DEF or SUB

PHASE2 allocates:
- 12 bytes for each format name, constant name and label
- 4 bytes for each format field

HORIZONTAL TABS

A horizontal tab may be entered for readability as the user inputs his source files. The assembler places the character following the horizontal tab at the next tab position. Tab stops begin with position 1, and occur every eight positions thereafter as follows: position 1, 9, 17, 25, etc. Thus if data is input at character position 5, a tab will place the next character input at position 9. However, if data is input at character position 17, a tab will place the next character at position 25.

Horizontal tabs may be used in both the Definition and Assembly Files.

CHAPTER III

ASSEMBLY PHASE (PHASE2)

The Assembly Phase reads in the source program statements, assigns values to labels and constants, then translates the source program's **executable** statements into a binary format. The Definition Phase output (a table of format and constant names and their associated bit patterns) is used for this translation.

The user must input his source program statements in the order corresponding to the desired order of his executable statements. The user may allocate blocks of storage, control printing, and set the program counter via nonexecutable assembler control instructions which are interspersed with, and do not affect the order of, his executable statements.

The object code is input via a sequence of instructions called the Assembly File whose content includes the following:

TITLE (heading to be printed on the output listing)

Printing control words Program counter control words Constant definition word Executable statements Comments

END

The optional TITLE statement is usually input first so that the desired title appears on the first output page.

The other statements (shown boxed) may be interspersed throughout the body of the file. However, the executable statements must be input in the order that corresponds to the desired sequence of the object (micro) code.

The END statement must be the last statement in the Assembly File.

The permissible Assembly Phase statements are:

TITLE LIST NOLIST SPACE EJECT	Printing control words
ORG RES ALIGN	Program counter control words
EQU	Constant definition word
FF	Free form definition word to establish a microword content

References to format names from the Definition Phase

Comments — Used for documentation and program flow.

END — End of the Assembly File.

None of the control words (LIST, ORG, etc.) or format names may contain blanks.

ASSEMBLY FILE STATEMENTS

Each statement contains an optional label followed by a statement type. Some statement types must be followed by an argument which may be a constant, a constant name, or an expression.

The general form of all Assembly File statements except comments is:

Form:

{ label: / name: } { control word / format name / definition word } { Δarguments }

CONTINUATION

Any statement may be continued on additional lines by placing a / (slash) as the first nonblank character in those lines.

LABELS OR NAMES

Labels or names are packed groups of letters and/or symbols which have an associated value.

Labels are permissible with executable statements and names are required with the definition word EQU.

Form:

---

name: definition word

or

label: format name

A name or label's value is determined by the statement type which follows it. Thus,

name: EQUΔn

equates the symbol "name" with the value given for "n",

while

label: format name Δ VFS, VFS . . .

equates label to the current value of the program counter, so that reference may be made to this location in the microcode by using this label.

A label or name must:

- Begin with an alphabetic character (A through Z) or period (.).
- End with a colon.
- Contain no more than 8 characters, exclusive of the colon. (Excess characters are truncated on the right.)
- Contain no imbedded blanks.
- Each be unique. If duplicates are given, the value given at the first occurrence is used and a warning message is issued for each duplicate.

A label or name may:

- Precede an EQU, RES, ORG, FF, or an executable instruction
- Be used as a variable field substitute (VFS)
- Be used as a field in an FF statement
- Not be a reserved word
- Contain only the letters A-Z, numerals 0-9 or a period (.) in positions 2 through 8.

When a name is defined by an EQU, the definition (source statement) must precede the use of the name as a field or a constant. If the statement

AM2909:DEFΔJSR,28X

is given, it must be physically located in the source program **after** the statement

JSR:EQUΔH#5

A good general rule is to place all EQUs at the beginning of the Assembly File program.

ENTRY POINT SYMBOLS

When a label is followed by a double colon (::) it is called an Entry Point. Entry Points are used when generating Mapping PROMs to easily obtain the program (location) counter value associated with certain points in the microcode.

Entry Points are indicated in the assembly source file as

label: : format name Δ VFS, . . .

Except for the double colon, Entry Points are subject to all the rules applicable to labels.

A list of the Entry Points (symbols and values) may be obtained when AMDASM is executed by requesting the MAP option (see Chapter 4, page 20).

STATEMENT TYPES

The Assembly File uses six general types of statements. These are listed below with their permissible control words:

- Printing control statements (LIST, NOLIST, SPACE, EJECT, TITLE)
- Program counter control statements (RES, ORG, ALIGN)
- Constant definition statement (EQU).
- Executable instruction statements (format names from the Definition Phase, FF).
- Comment Statements (;).
- END Statement

PRINTING CONTROL STATEMENTS

TITLE

All data input on the line with TITLE will be printed at the top of each page of output. A maximum of 60 characters may be input for a title. When a new TITLEΔ is encountered the list device ejects blank lines to complete the present page and succeeding "pages" will contain this title. A "page" is not necessarily a physical page since the user may specify the length (number of lines) of a "page". The general form is:

Form:	
TITLE Δ	alphanumeric data to be printed at the top of the page

LIST

LIST indicates that the following statements are to be printed whenever printing of the Assembly File input is requested. This feature will be most useful when correcting or modifying an Assembly File. (AMDASM automatically prints the source statements unless NOLIST is specified by the user.) The general form is:

Form:
LIST

LIST must:

- Begin on a new line.
- Be followed by a carriage return.
- Precede the Assembly File statements which are to be printed.
- Be interspersed between **complete** assembly statements.

NOLIST

NOLIST turns off the printing of assembly source statements. Printing of the Assembly File input will be suppressed until LIST is again encountered. Any source statement containing an error will still be printed. The general form is:

Form:
NOLIST

NOLIST must:

- Begin on a new line.
- Be followed by a carriage return.
- Precede the Assembly File statements which are not to be listed.
- Be interspersed between complete assembly statements.

SPACE

SPACE indicates that the assembler is to leave n blank lines before printing the next source statement. The general form is:

Form:
SPACEΔ n

SPACE must:

- Begin on a new line.
- Be followed by Δ and a decimal digit indicating the number of succeeding lines to be left blank.
- Be inserted in the Assembly File at the point where the spaces are desired.

EJECT

When EJECT is encountered, the assembler generates blank lines on a list device so that any previous lines plus the blank lines equals the specified "page" length (default is 66 lines). It then begins a new "page", headed with the title. On a printer a new page is ejected. The general form is:

Form:
EJECT

EJECT must:

- Begin on a new line.
- Be followed by a carriage return.

PROGRAM COUNTER CONTROL STATEMENTS

ORG

ORG is used to set a new program counter (PC) origin. The next assembled microword will be located at the new origin. The general form is:

Form:
ORGΔ n

ORG must:

- Be followed by at least one blank and n.
- Have n specified using decimal digits unless one of the designators B#, Q# or H# precedes the digits given.
- Be used only for setting the program counter forward.
- Be greater than or equal to the current value of the program counter.

ORG may:

- Contain an expression instead of n.
- Be used an unlimited number of times in the Assembly File.

If no ORG is specified the assembler uses an initial PC of 0.

RES

RES is used to reserve n words of memory. This increments the program counter by n. The reserved words will automatically be filled with "don't cares" by the assembler. The general form is:

Form:
RESΔ n

RES must:

- Be followed by at least one blank and n.
- Have n specified using decimal digits unless one of the designators B#, Q# or H# precedes the digits given.

RES may:

- Contain an expression instead of n.
- Be used an unlimited number of times in the Assembly File.

ALIGN

ALIGN is used to set the program counter to the next value which is an integral multiple of the value n. It is used to align the program counter to a specific boundary such that the next microinstruction will be assembled at an address which is, for example, the next integral multiple of 2, 4, 8 or 16. The general form is:

Form:
ALIGNΔ n

ALIGN must:

- Be followed by at least one blank and n
- Have n specified using decimal digits unless one of the designators B#, Q#, H# precedes the digits given.

ALIGN may:

- Contain an expression instead of n.
- Be used an unlimited number of times in the Assembly File.

CONSTANT DEFINITION STATEMENT

EQU

EQU is used to equate a constant name to a constant value or expression. The general form is:

Form:
name: EQUΔ constant (or expression)

This equates the characters given in the name position to the value of the constant or expression. Only one expression or constant is permitted following the EQU.

Each EQU must:

- Begin on a new line.
- Begin with a name:
- The name: must be followed by EQUΔ (blanks between : and EQU are optional).
- Contain a constant or expression which represents the bit pattern for one field.
- Define a value which can be represented in 16 bits ($2^{16}-1$ maximum).

Each EQU may:

- Be followed by a semicolon and comment after the constant or expression.
- Be continued on additional lines by using / (slash) as the first non-blank character in these lines.
- Be used in the Assembly File even if defined in the Definition File.
- Be equated to the current value of the program counter by using $ as the designator. The $ may be part of an expression.

Examples of EQUs:

ADD:EQUΔQ#0

defines a 3-bit field whose bit pattern is 000.

This could be an ALU function of ADD for the Learning Kit.

PUSH:EQUΔH#9

defines a 4-bit field, bit pattern 1001 which might represent the next microinstruction control field in the Learning Kit.

EXECUTABLE STATEMENTS

Executable statements form the body of the Assembly Phase Program. When assembled (with appropriate substitution of parameters) they form the binary output code of the Assembly Phase. They must be input in an order which corresponds to the desired order of the object code.

EXECUTABLE STATEMENTS USING FORMAT NAMES

Most executable instructions will refer to the format names established by the Definition Phase. Their general form is:

Form:

{label:}format nameΔVFS,VFS

(VFS = Variable Field Substitution)

These formats may be referenced singly (with appropriate VFSs) or they may be combined (overlayed) with other formats (and their appropriate VFSs). All cases result in the formation of a single, complete microword.

Executable Instruction Statements must:

- Begin on a new line.
- Contain a format name from the Definition Phase.
- Substitute a constant name, a label, a constant, or an expression for each variable field and these must be separated by commas. If a default value was given in the Definition Phase and is to be used, the VFS may be omitted.

Executable Instruction Statements may:

- Contain a single format name or may contain an unlimited number of format names to be overlayed.
- Contain the current value of the program counter as the value for a field if $ is the VFS used for that field. The $ may be part of an expression ($ + n) given for a VFS.
- Be preceded by a label: or a label::

FREE FORMAT STATEMENT FF

Executable statements whose instruction formats were not defined in the Definition Phase may be defined in the Assembly Phase by using the built-in free format command FF. The general form is:

Form:

{ label: } FFΔ field1, field2, . . ., fieldn

An Assembly File may contain an unlimited number of FFs.

Each FF must:

- Begin on a new line.
- Contain a / (slash) as the first nonblank character if continued on another line.
- Have fields separated by commas.
- Have an explicit length "n" given for "don't care" fields (nX) or for fields defined using decimal (nD#m).
- Not contain a variable field.
- Not contain a constant name for a field unless that constant has been **previously** defined in the Assembly or Definition File.
- Not be overlayed with another format name.

Each FF may:

- Be preceded by a label : or label ::
- Contain an expression for any field but the expression must be enclosed in parenthesis and must be preceded by the field length "n", for example:

  FFΔ5X,10($-5),B#101

- Contain a value for an expression which is to be automatically right justified in a field. However, if the number of bits which represent the value is larger than the field length, an error is generated unless the truncation follows the) for this expression
- Contain a field whose value is the current value of the program counter by using $ for that field (or an expression containing $ may be used).

For example, if the constants

```
WORDΔ  48
AZ:    EQUΔB#01
RB:    EQUΔQ#10
```

were defined in the Definition File, then the Assembly File could contain the following statements:

```
C: EQUΔ H#C
XTRA: FFΔ 12H#3%, AZ, 18X, C, B#10111,
/1X, RB
```

The microinstruction (binary output) for this FF is:

```
000000000011  01  XXXXXXXXXXXXXXXXXX
   12H#3%     AZ          18X
    1100     10111     X    001000
      C     B#10111    1X     RB
```

which will be printed in the following format:

```
000000000011101XX XXXXXXXXXXXXXXXX 110010111X001000
```

OVERLAYING FORMATS

When formats are overlayed (combined) to form a microword, the general form is:

Form:

{label:}format nameΔVFS,VFS, &format nameΔVFS,VFS . .

(VFS = Variable Field Substitution) (& = overlay)

Formats may be overlayed (combined) with other formats provided that:

- Each bit of format name (#2) that contains a one or zero, must have that bit specified as a "don't care" in the format name (#1) to be overlayed. Subsequent overlays must be on the "don't care" fields remaining after the overlay of all preceding formats.
- Each format is a full microword in length.

Microword instructions defined using the built-in free format (FF) may **not** be overlayed.

For example, if the Definition File contains:

```
ADD: DEFΔ 5X, 8H#A2, 3X
REG1: DEFΔ B#00001, 11X
CARRY: DEFΔ 15X, B#1
```

Then in the Assembly Phase

```
ADRGCY:  ADD & REG1 & CARRY
```

yields

```
00001  10100010  XX1
```

COMMENT STATEMENTS

Comment statements are nonexecutable statements which are used to provide information about the program variables or the program flow. A comment may be a full line or may follow, for example, a constant definition statement. All characters from the semicolon to the end of the input line are not processed and serve merely as a documentation aid. The general form is:

Form:
; comment text desired

END

END indicates that the Assembly File is complete and should be processed. The general form is:

Form:
END

END must:

- Begin on a new line.
- Be the last statement in the Assembly File.
- Be followed by a carriage return.

ARGUMENTS

An Argument follows some types of statements as shown in the executable instruction section.

Permissible Arguments are:

Constants
Expressions
Constant names
Labels

The statements

LIST
NOLIST
END
EJECT

require no Arguments.

Executable instructions which contain format names from the Definition File need Arguments only if there were no default values given for variable fields. Arguments which are to be substituted in variable fields are called Variable Field Substitutes (VFS).

All other statements types **require** Arguments.

CONSTANTS

Constants are used as Arguments for the commands EQU, ALIGN, RES, SPACE, ORG or as variable field substitutes (VFSs).

Note that in the Assembly File the $ is used to indicate the substitution of the program counter value for the content of a constant or field. The following table lists the designators which may be used to define constants:

Designator	Meaning
B#	A constant or field whose content will be represented using binary digits (0 and 1).
Q#	A constant or field whose content will be represented using octal digits (0 through 7).
D#	A constant or field whose content will be represented using decimal digits (0 through 9). A D# **must** be preceded by decimal digit(s) giving an explicit length (number of bits) when representing a field in an FF statement.
H#	A constant or field whose content will be represented using hexadecimal digits (0 through 9, A through F).
$	Use the current program counter as the value for this field or constant.

CONSTANT LENGTHS

Constant lengths were discussed in detail in Chapter I. However, the length associated with the use of the $ is a special case.

When the $ is detected in the evaluation of a constant field or expression, the current program counter value is substituted in place of the $.

If the PC = 59 at the instruction preceding:

NEXTLOC: EQUΔ$+5

then NEXTLOC is equated to 64.

If the $ is substituted for a field, the length of the PC is calculated by counting the bits from the right to the leftmost significant one bit. The PC length most probably will not agree with the defined (explicit) field length.

Thus, when defining fields in a format in the Definition Phase or in an FF statement, the fields which are to have $ substituted in them should include the % and/or the : attributes. For example, the field definition

4V%:

will permit any PC value to be substituted into it but

4V

will accept only PC values between 0000_2 and 1111_2.

CONSTANT MODIFIERS

Constants may have modifiers following their given value. They must appear after the constant digits where they may be in any order but will be **processed in the following order:**

Modifier	Description
* or –	Inversion or negation
%	Right justification
:	Left truncation
$	Paging

A constant may not be modified by both inversion and negation.

If a constant, including modifiers, is given as a VFS, any attributes (permanent modifiers) given for that field in the Definition File will also modify the value of the constant given.

If, for example the Definition File contains:

A: DEFΔ 5X, 3V*, 2X, 5V%H#, B#10101
field#1 field#2

and the Assembly File is written:

TEST: AΔ011,9

the binary value 011 is inverted and substituted for field #1, while the 9 (hex) is equated to binary 1001 and right justified for field#2 resulting in the microinstruction

XXXXX 100 XX 01001 10101

If the Assembly File statement is written

TEST2: AΔ001*, 3*

the binary value 001 is inverted by the current *, then inverted again by the attribute in the Definition File for field#1. Field#2 hex 3 (binary 0011) is inverted to 1100 and right justified in field#2.

The complete microinstruction is:

XXXXX 001 XX 01100 10101

EXPRESSIONS

Expressions may be used when the programmer wishes to have a value calculated as an argument or as a field substitution. An expression assumes the form:

Form:
Symbol operator symbol operator . . .

All expressions:

- Are evaluated using integer arithmetic and remainders are discarded
- Must result in a positive value which can be represented in 16 bits ($2^{16}-1$ maximum).
- Use only the operators, + addition, − subtraction, * multiplication, /division, which are described in Chapter II, page 5.
- Are evaluated in strict left to right sequence. There is no hierarchy for the operators and no parenthesis for nesting are permitted.
- May contain the $ as a symbol to indicate that the current value of the program counter is to be substituted.
- Are terminated by a comma or the end of the line except when used as a field in FF where they are enclosed by parenthesis.
- May be continued on the next line by making the first nonblank character a slash (/). A continuation involving a division would thus require a double slash (//).
- May contain constants, constant names or labels.

For example, if SBB is a format name, and the first variable field is to contain the value 3, it might be written as:

SBBΔ1 + 2

which is the same as SBBΔ3 (1 and 2 are expression symbols, + is an expression operator). The expression

JMPΔ$ − 5

yields the current value of the program counter minus 5 as the VFS for the first variable field in the format name JMP. ($ and 5 are expression symbols, − is an expression operator). The expression

EIGHT: EQUΔ 2*2*2

means EIGHT = 8 (2's are the expression symbols, *'s are the operators).

EXAMPLES OF CORRECT CONSTANT USAGE

```
QREG:EQUΔQ#0
      .
      .
      .
AQ:EQUΔQREG
DQ:EQUΔ4+8/6 (value = 2)
AB:EQUΔQREG+1
AM2901:DEFΔ4V%D#,5X,AQ,3V,17X
```

} Definition File

```
EXOR:EQUΔQREG+6
BEGIN:AM2901Δ$+2,EXOR
      AM2901Δ$−1,AB
```

} Assembly File

VARIABLE FIELD SUBSTITUTES (VFS)

When a format is defined in the Definition File some of its fields may be designated as variable fields. If these fields are not given a default value during their definition or if one wishes to override the default value, a substitution must be made for these field(s) in the Assembly File source statements. These substitutes are called Variable Field Substitutes, VFS.

REQUIRED SUBSTITUTIONS

If the variable field(s) are not given default values in the Definition File, values for these fields **must** be provided in the Assembly File source statements. If omitted, an error message will be provided, and processing of that statement ends.

SUBSTITUTION SEPARATORS

Each VFS (whether required or optional) represents a single field and must be separated from other VFSs by a comma. Trailing commas may be omitted but the assembler uses the commas to indicate which fields are to be given substitute values (i.e., VFSs are positional and position is determined by the number of commas), so leading or intermediate commas must be given.

For example if the Definition File contains:

A: DEFΔ 5X, 3V*B#110, 2X, 5V%H#, B#10101

field #1 field#2

Then if the Assembly File is written as

TEST3: AΔ,4

field#1 will assume the default value 001 (from 3V*B#110) while field#2 will be equated to 0100 and right justified in the 5-bit field so that field#2 is 00100.

The complete microinstruction will be

XXXXX 001 XX 00100 10101

If the comma were omitted and

TEST4: AΔ4

were written, the assembler would try to use 4 as the VFS for field#1. Two errors are present. The 4 is not a binary number as required for field #1, and no value is indicated for field #2. Field #2 had no explicit default value, and no VFS is given which is an error. The indicated error would be "illegal character," since the 4 is assumed to go with field #1 which requires binary digits.

If, however, the user wishes to input field#1 as an octal 4 and field#2 as zero, he could write:

TEST5: AΔQ#4,0

which yields the microinstruction

XXXXX 011 XX 00000 10101

octal 4 inverted — hex 0 right-justified

In short, when forming the microword definition, if a leading or intermediate variable field is to assume a default value but a trailing field requires a VFS, each field to be skipped must be represented by a comma.

This is best explained by an example. Assume a format ADE with three variable fields, each having a default value of zero specified in the Definition File:

ADE: DEFΔ 3VB#000, 3VB#000, 3VB#000

The following example illustrates fields which assume their default values and fields which are given override or substitute values.

Instruction	Resultant Microword Definition	Meaning
TEST6: ADEΔ,,010 or TEST7: ADEΔ,,Q#2	000 000 010 000 000 010	Fields 1 and 2 assume their default values, field 3 contains 010.
TEST8:ADEΔQ#4,,B#101	100 000 101	Field 2 assumes its default value, field 1 is 100, field 3 is 101.
TEST9: ADEΔ011	011 000 000	Fields 2 and 3 assume their default values, field 1 is 011.

If the variable field substitutions contain modifiers, using the Definition File statement:

ADE: DEFΔ 3VB#000, 3VB#000, 3VB#000

the Assembly File statements for the previous example could be written:

Instruction	Resultant Microword Definition	Meaning
TEST10:ADEΔ,,101*	000 000 010	Fields 1 and 2 assume their default values. Field 3 is 101 inverted.
TEST11:ADEΔH#4:	100 000 000	Field 1 is hex 4 (binary) 0100) truncated to 100. Fields 2 and 3 assume their default values.

The variable fields may contain attributes in the Definition File such as:

ADE: DEFΔ 3V:H#0 ,3V*B#000, 3V%B#000

The Assembly File Statements written below now generate:

Instruction	Resultant Microword Definition	Meaning
TEST12:ADEΔ,,01*	000 111 010	Field 1 assumes its default value 000. Field 2 assumes its default value 111. (000 inverted). Field 3 is inverted to 10 then right justified to be 010.
TEST13:ADEΔ9, Q#3*,1	001 011 001	Field 1 is hex 9 truncated to 001. Field 2 is octal 3 inverted to 100, then inverted by field#2 attribute (*) to 011. Field 3 is binary 1 right justified to 001.

FITTING VARIABLE SUBSTITUTES TO VARIABLE FIELDS

Any value given as a Variable Field Substitute (VFS) must contain exactly the number of bits specified (in the Definition File) for the total length of the variable field unless the modifiers % (right justification), : (truncation), or $ (paged addressing) are given.

These modifiers may be supplied as attributes with the original field definition (Definition File) or they may be supplied with the field substitution value in the Assembly File.

PAGED AND RELATIVE ADDRESSING

$ is used in two ways in the Assembly File:

a) To indicate that the current value of the program counter is the value to be substituted into this field. This is called relative addressing.
b) As an attribute to indicate that the value substituted for this field must be on the same memory "page" as the microword into which it is substituted. This is called paged addressing.

For relative addressing, the $ alone or as part of an expression is used as a VFS.

For paged addressing, the $ may be given as an attribute of this variable field in the Definition File, or the $ may immediately follow the VFS in the Assembly File source statement.

For example, if the Definition File contains

```
JSR:DEFΔ8X,8V$, H# 27, 12VH#
JSB:DEFΔ8V%D#, 8X, 8Q#013:, 12X
```

the Assembly File could be written

```
Line#
  1    JSR Δ  BEGIN,0BC
  2    JSB Δ  MULT$+5
  3    JSR Δ  MULT, BEGIN$
  4    JSB Δ  H#37
  5    JSB Δ  $+5
                •
                •
                •
       BEGIN:  ADD
                •
                •
                •
       MULT:   MPY
```

Lines 1-3 are examples of $ used for paged addressing. In Line 1, the value of the program counter (where BEGIN: appears) is substituted into the first variable field of the format JSR. This value is truncated on the left, if necessary, to fit into this 8-bit field, and any truncated left bits must be identical to the corresponding bits of the program counter associated with Line 1.

The same type of substitution, truncation, etc. occurs for Lines 2 and 3.

Note that:

- The JSB on line 2 needs a $ after MULT if paged addressing is desired since no $ was given with that variable field in the Definition File.
- For expressions such as line 5, the constant (5) is added to the value of the label (MULT) **before** the check is made to ensure that the value substituted is still on the correct "page".
- The JSR on line 1 needs no $ with the BEGIN since that variable field contained a $ in the Definition File.
- The JSR on line 3 requires a $ after BEGIN since the second variable field did not contain a $ in the Definition File.
- On line 2 a label with a $ may be part of an expression.

Line 5 is an example of relative addressing. The current value of the program counter plus 5 will be substituted for the variable field.

Note that:

- There is no connection between the $ used for paged addressing – as an attribute for a variable field – and the $ used as a variable field substitute to indicate use of the current value of the program counter (relative addressing).

HEXADECIMAL ATTRIBUTE

The designator H#, if given with a variable field in the Definition File, is a permanent attribute but may need to be repeated in the Assembly File. This is necessary since the program cannot distinguish a hexadecimal value which begins with an A through F from a label or format name.

Thus, if the Definition File contains

```
AM2901:DEFΔ8V%H#,Q#0,21X
```

and the Assembly File statement contains

```
AM2901Δ3A
```

it is clear to the program that the digits 3A are to be substituted into the variable field. (A label or name cannot begin with a numeral).

However, the statement:

```
AM2901ΔAB
```

does not clearly indicate whether the constant name AB is meant, or the value of the hexadecimal digits AB is meant. If the programmer wishes the hex value AB, he must write:

```
AM2901ΔH#AB
```

The statement AM2901ΔAB will substitute the value of the constant named AB in the first variable field. If there is no constant named AB, an error will be generated.

ASSEMBLER SYMBOL TABLE

The symbol table contains a list of all the symbols (constant names) defined by EQUs and all labels in the Assembly File. The symbol table also includes all the constant names and their associated values defined using EQUs in the Definition File.

For each symbol, the table lists the label and the program counter value of the statement where the label is defined, or if the symbol is a constant name (defined by EQU), it is followed by the value of the constant.

A symbol table is useful when errors occur due to misspelling or the omission of the colon after a label.

A sample symbol table is:

```
SYMBOLS
  A     0001
  S     0023
  X     0000
```

Printing of the Symbol Table is optional and is described in the SYMBOL and NOSYMBOL section of Table 4-1.

ASSEMBLER ENTRY POINT TABLE

The entry point table contains a list of all the entry point symbols (labels followed by ::) and their associated program counters. These values are useful for mapping PROMs.

Printing of the entry point table is optional and is described in the MAP and NOMAP section of Table 4-1.

ASSEMBLY FILE – RESERVED WORDS

The following are reserved words used by the assembler program during the Assembly Phase. These words MAY NOT BE USED AS LABELS in the Assembly File statements:

ALIGN	NOLIST
EJECT	ORG
END	RES
FF	SPACE
LIST	TITLE

Format names or constant names from the Definition File.

CHAPTER IV

AMDASM/80 EXECUTION

After the user has created his Definition File and Assembly File using the MDS Text Editor, he is ready to execute AMDASM/80. After the ISIS© operating system has issued a user prompt (i.e., a "–" character) the microassembler is executed by entering the command:

–AMDASMΔ PHASEn(filename) Δ { options }

PHASE1 (filename) specifies execution of the Definition Phase using (filename) for the definition source file.

PHASE2 (filename) specifies execution of the Assembly Phase using (filename) as the assembly source file.

PHASE1 (filename) PHASE2 (filename) specifies execution of both the Definition and Assembly Phases.

Thus

–AMDASMΔ PHASE1(:F1:DEFN) specifies execution of only the Definition Phase using the file (on drive 1) called DEFN.

or

–AMDASMΔ PHASE1(:F1:DEFN) PHASE2(:F1:ASMSRC)

specifies execution of the Definition and Assembly Phases using the files (on drive 1) DEFN as the definition source file and ASMSRC as the assembly source file.

Either PHASE1or PHASE2 or both **must** be specified following AMDASMΔ. P1 and P2 are the alternate options used for PHASE1 and PHASE2, respectively.

The user then enters the desired options. Options and their default values are shown in Table 4-1. The full option may be typed (OBJECT) but only the alternate option (O) need be typed.

Table 4-1 AMDASM/80 Options

OPTION	ALTERNATE OPTION	DEFAULT	MEANING
DEF (filename)	D	(AMDASM.DEF)	Specifies the name of the file where output of the Definition Phase is to be stored. When only PHASE2 is executed, this specifies the input file which contains the processed definitions. If no DEF (filename) is given, the default name AMDASM.DEF will be used.
LIST (filename)	L	(AMDASM.LST)	Specifies where the Definition and Assembly output is to go. (:LP:) for the filename causes the output to be listed on the line printer. If no LIST (filename) is given, the output goes to the file with the default name (AMDASM.LST)
NOLIST	NL		Suppresses listing of assembly source code.
OBJECT (filename)	O	(AMDASM.OBJ)	Specifies that the microcode (object code) is to be output on a file with the name (filename). If not given, the microcode is placed on a file with the default name AMDASM.OBJ.
NOOBJECT	NO		Suppresses placement of the microcode onto a file. If block format printing is requested, the object code printing is also suppressed.
INTER	IL	BLOCK	Specifies inter-leaved listing format.
BLOCK	BL		Specifies blocked listing format
SRCONLY	SO		Specifies source-only listing format
OBJONLY	OB		Specifies object-only listing format
WIDTH (n)	W	n=72	Specifies width n, (a decimal number) in characters of listing device.
LINES (n)	LN	n=66	Specifies number n, (a decimal number) of lines per page. If not specified, default is 66 lines (11 inches).
MAP	M	MAP	Specifies listing of entry point symbols (i.e., label symbols designated as entry points by double colons "::")
NOMAP	NM		Suppresses listing of entry point symbols If not specified, defaults to MAP
HEX	H	HEX	Specifies listing of location counter in hexadecimal format
OCTAL	Q		Specifies listing of location counter in octal format. If not specified defaults to HEX.
SYMBOL	S	SYMBOL	Specifies listing of constant names and labels and their associated values.
NOSYMBOL	NS		Supresses listing of Symbol table. If not specified, defaults to SYMBOL.

In the option table (Table 4-1), **filename** must be an ISIS filename of the form:

:device:name.ext

where: :device: is optional and is :F0:, :F1:, :F2:, or :F3: to indicate the drive on which the diskette is mounted. If omitted, :F0: is assumed.

name is from 1 to 6 uppercase letters or digits and is required.

.ext is a period followed by 1 to 3 uppercase letters or digits and is optional.

Options need to be separated by at least one blank character from other options in the command. If an option ends with), the blank space is not needed.

Whenever a user does not specify an option in his execution command AMDASM will use the default given in the preceding table.

The command language for executing AMDASM is best illustrated with examples:

–AMDASMΔP1(DEFN.SRC)P2(MUCODE.SRC)

specifies execution of both PHASE 1 and PHASE 2 using DEFN.SRC as the input file for PHASE 1 and MUCODE.SRC for PHASE 2. Defaults are selected for all other options.

–AMDASMΔPHASE1 (DEFN.SRC) DEF (AM9080.DEF)

specifies execution of PHASE 1 with DEFN.SRC as the input source file and AM9080.DEF as the definition table output file.

–AMDASMΔPHASE2 (MUCODE.SRC) DEF(AM9080.DEF) INTERΔNOSYMBOL

specifies execution of PHASE 2 with MUCODE.SRC as the input source file and AM9080.DEF as the definition table input file, interleaved listing format, a list of entry point symbols, and no symbol table listing.

The interleaved format prints a line of source code followed by a line of object code.

The block format prints all lines of source code, then all lines of object code.

The source-only format prints only the source code.

The object-only format prints only the object code.

CHAPTER V

SAMPLE OF AMDASM PROCESSING

The capabilities of AMDASM/80 can be demonstrated by microprogramming one of the exercises from the Am2900 Learning and Evaluation Kit. This kit provides a simple but complete example of a microprogrammed system.

The architecture of the kit is shown in Figure 5-1. The dashed lines outline the two LSI components, the Am2909 microprogram sequencer and the Am2901 four-bit slice microprocessor. Each microinstruction in the microprogram memory consists of 32 bits divided into fields to control the sequencer, branch address, shift multiplexers, and all the inputs to the Am2901. The fields and their functions are defined in Figure 5-2.

The first step in using AMDASM/80 is the creation of a set of definitions which reflect the hardware on which the microprogram will run. The statements in Figure 5-3 completely define, mnemonically, the fields in the kit. That is, they implement exactly the fields and their functions for the microprocessor architecture defined in Figure 5-1, and so may be used in writing all microprograms that are to operate in this architecture. Figure 5-4 shows a flow chart of the program to be written. Figure 5-5 is the AMDASM output in Block format.

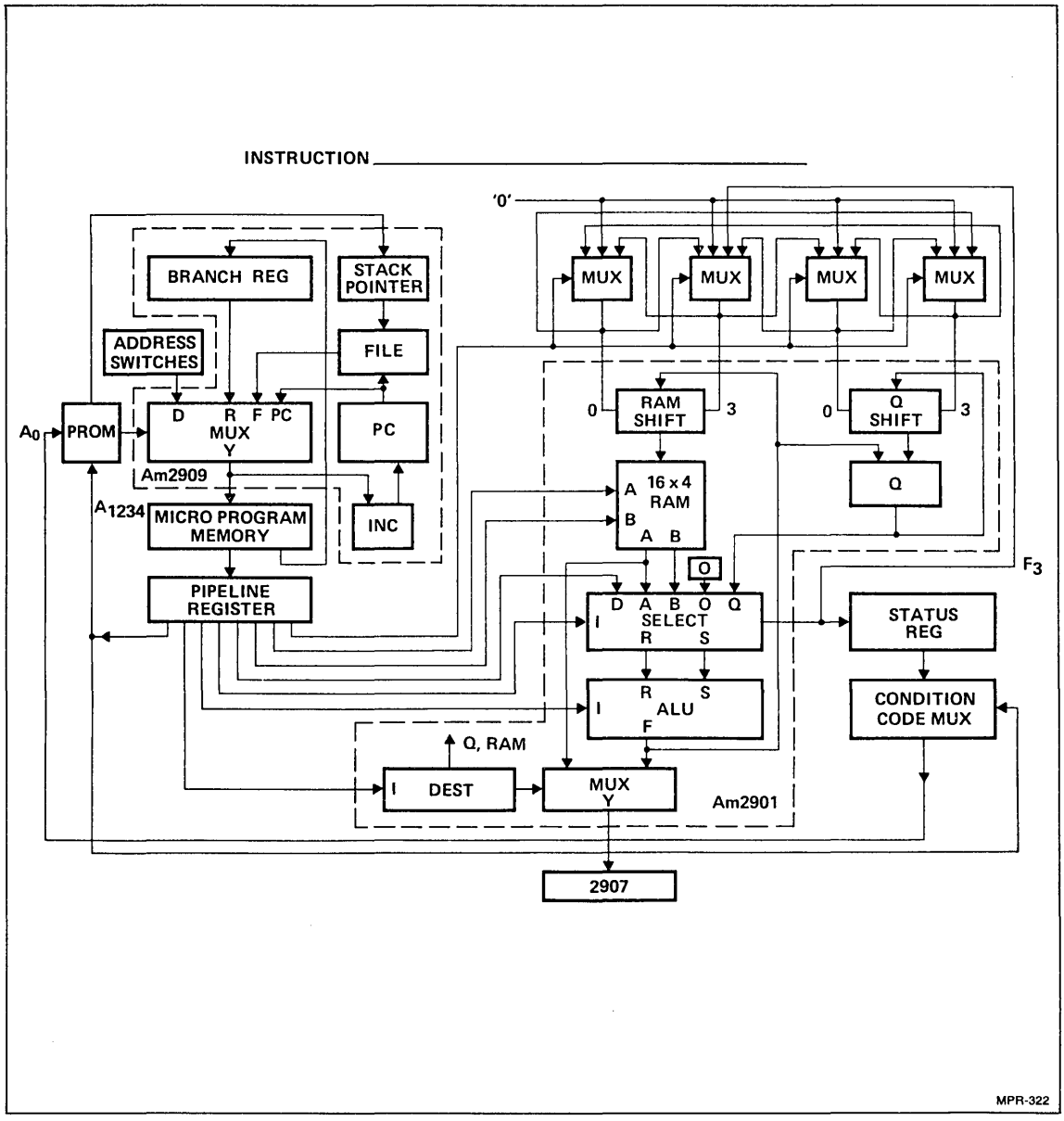


Figure 5-1. Am2900 Learning and Evaluation Kit Architecture

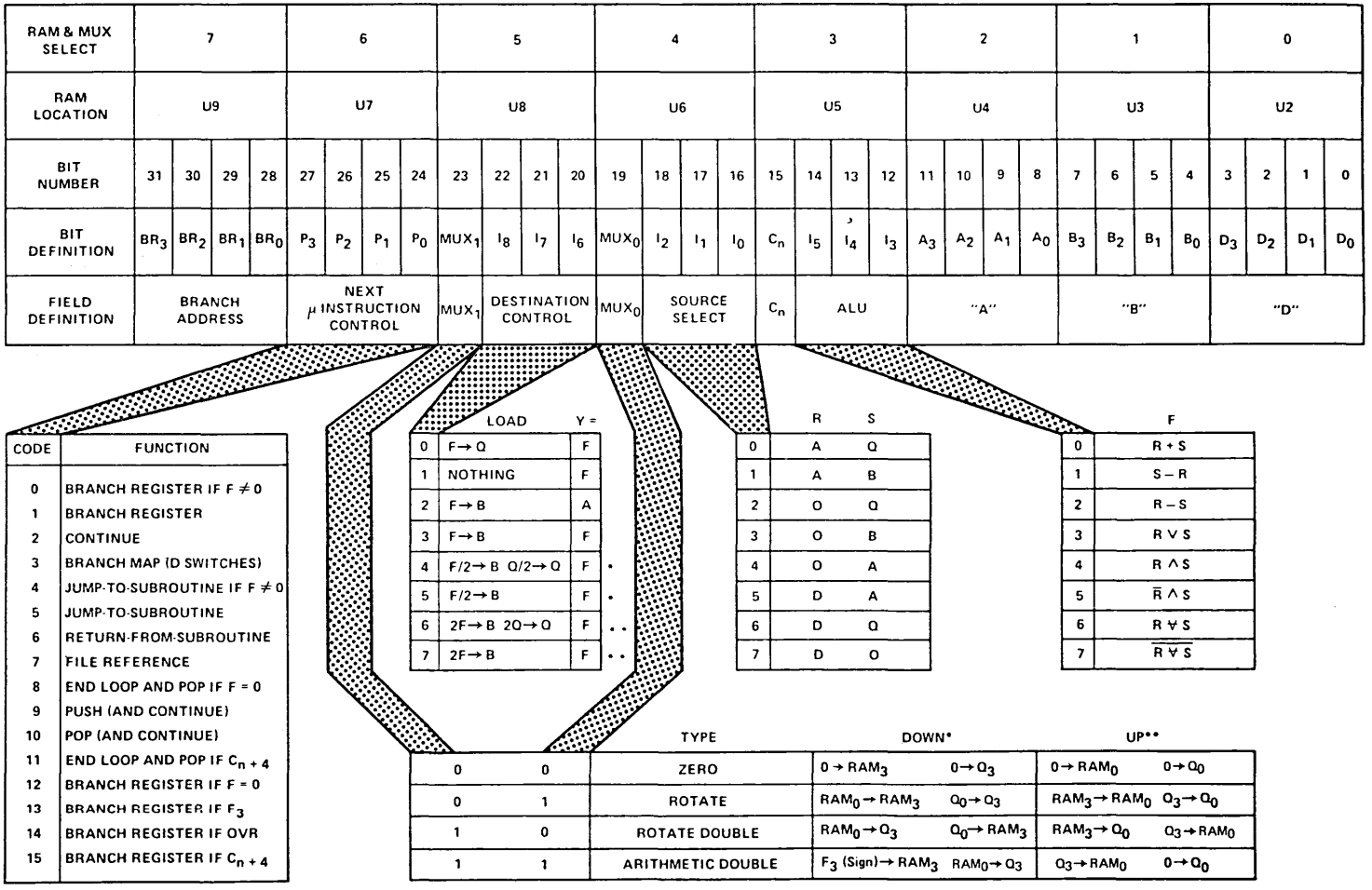


Figure 5-2. Example of Fields and Functions

```
TITLE AM2900 KIT DEFINITIONS

;
WORD 32
;
;REGISTER DEFINITIONS
;
R0:  EQU H#0
R1:  EQU H#1
R2:  EQU H#2
R3:  EQU H#3
R4:  EQU H#4
R5:  EQU H#5
R6:  EQU H#6
R7:  EQU H#7
R8:  EQU H#8
R9:  EQU H#9
R10: EQU H#A
R11: EQU H#B
R12: EQU H#C
R13: EQU H#D
R14: EQU H#E
R15: EQU H#F
;
;AM2901 SOURCE OPERANDS (R S)
;
AQ: EQU Q#0
AB: EQU Q#1
ZQ: EQU Q#2
ZB: EQU Q#3
ZA: EQU Q#4
DA: EQU Q#5
DQ: EQU Q#6
DZ: EQU Q#7
;
;AM2901 ALU FUNCTIONS (R FUNCTION S)
;
ADD:   EQU Q#0
SUBR:  EQU Q#1
SUBS:  EQU Q#2
OR:    EQU Q#3
AND:   EQU Q#4
NOTRS: EQU Q#5
EXOR:  EQU Q#6
EXNOR: EQU Q#7
;
;AM2901 DESTINATION CONTROL
;
QREG:  EQU Q#0
NOP:   EQU Q#1
RAMA:  EQU Q#2
RAMF:  EQU Q#3
RAMQD: EQU Q#4
RAMD:  EQU Q#5
RAMQU: EQU Q#6
RAMU:  EQU Q#7
;
;SHIFT MATRIX CONTROL
;
SHIFT:   DEF 8X,B#0,3X,B#0,19X
ROTATE:  DEF 8X,B#0,3X,B#1,19X
DBLROT:  DEF 8X,B#1,3X,B#0,19X
ARITH:   DEF 8X,B#1,3X,B#1,19X
;
;NEXT MICROINSTRUCTION ADDRESS SELECT
;
BRFNO:     EQU H#0 ;BRANCH REGISTER IF F NOT EQUAL TO ZERO
BR:        EQU H#1 ;BRANCH REGISTER
CONT:      EQU H#2 ;CONTINUE
BM:        EQU H#3 ;BRANCH MAP
JSRFNO:    EQU H#4 ;JUMP-TO-SUBROUTINE IF F NOT EQUAL TO ZERO
JSR:       EQU H#5 ;JUMP-TO-SUBROUTINE
RTS:       EQU H#6 ;RETURN FROM SUBROUTINE
STKREF:    EQU H#7 ;FILE REFERENCE
LOOPFNO:   EQU H#8 ;END LOOP AND POP IF F=0
PUSH:      EQU H#9 ;PUSH AND CONTINUE
POP:       EQU H#A ;POP AND CONTINUE
LOOPCOUT:  EQU H#B ;END LOOP AND POP IF CN+4
BRFEQ0:    EQU H#C ;BRANCH REGISTER IF F=0
BRF3:      EQU H#D ;BRANCH REGISTER IF F3
BROVR:     EQU H#E ;BRANCH REGISTER IF OVR
BRCOUT:    EQU H#F ;BRANCH REGISTER IF CN+4
;
;OTHER STUFF
;
CN0:  EQU B#0
CN1:  EQU B#1
LOW:  EQU B#0
HIGH: EQU B#1
ZERO: EQU B#0
ONE:  EQU B#1
;
AM2901: DEF 9X,3VQ#1,1X,3VX,1VX,3VX,4VX,4VX,4X
AM2909: DEF 4VX,4VH#2,24X
DIN:    DEF 28X,4VH#
;
END
```

"R0" to "R15" are set to hex 0 to F using the "equate" statement. The "H#" designator means the numbers following are in hex, and each digit represents 4 bits.

ALU Source operands are assigned octal values using the "equate". The "Q#" designates octal, 3 bits, per digit.

The 8 ALU functions of the AM2901 are given names.

Defines the two separated bits which control the left-right shift multiplexers. The "x's" are "don't-care" bits in between the defined bits.

Definitions for the sequence control instructions used in the second field of the microinstruction.

Format definitions are made for the ALU fields, the sequence control fields, and the data input. Formats contain don't cares (x) and variables (v). Each variable can have a default value. For example, in AM2909, the second four-bit variable defaults to hex 2, and the first four-bit variable defaults to x.

Figure 5-3. Definition File

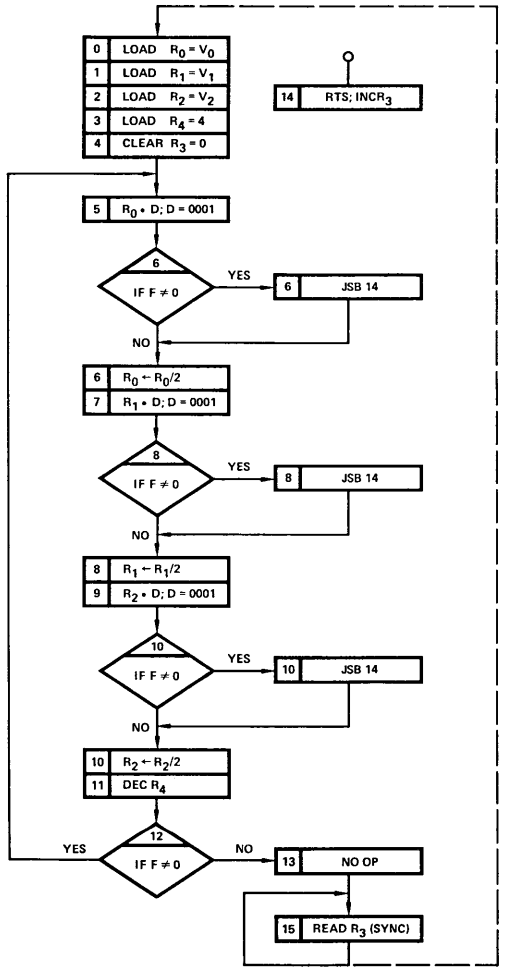


Figure 5-4. Flow Chart of Example

```
0000      AM2909 & AM2901   RAMF, DZ,,OR,,R0 & DIN H#F
0001      AM2909 & AM2901   RAMF, DZ,,OR,,R1 & DIN 9
0002      AM2909 & AM2901   RAMF, DZ,,OR,,R2 & DIN 0
0003      AM2909 & AM2901   RAMF, DZ,,OR,,R4 & DIN 4
0004      AM2909 & AM2901   RAMF, ZB,,AND,,R3
0005 A5:  AM2909 & AM2901    ,DA,,AND,R0,R0 & DIN 1
0006      AM2909 A14,JSRFN0 & AM2901  RAMD, ZB,,OR,,R0
0007      AM2909 & AM2901   ,DA,,AND,R1,R1 & DIN 1
0008      AM2909 A14,JSRFN0 & AM2901  RAMD, ZB,,OR,,R1
0009      AM2909 & AM2901   ,DA,,AND,R2,R2  & DIN 1
000A      AM2909 A14,JSRFN0 & AM2901  RAMD, ZB,,OR,,R2
000B      AM2909 & AM2901  RAMF, ZB, CN0,SUBR,,R4
000C      AM2909 A5,BRFN0 & AM2901
000D      AM2909 A15,BR & AM2901
000E A14: AM2909 ,RTS & AM2901  RAMF, ZB,CN1,ADD,,R3
000F A15: AM2909 A15,BR & AM2901   ,ZB,,OR,,R3
     END

0000 XXXX0010X011X111 X011XXXX00001111
0001 XXXX0010X011X111 X011XXXX00011001
0002 XXXX0010X011X111 X011XXXX00100000
0003 XXXX0010X011X111 X011XXXX01000100
0004 XXXX0010X011X011 X100XXXX0011XXXX
0005 XXXX0010X001X101 X100000000000001
0006 11100100X101X011 X011XXXX0000XXXX
0007 XXXX0010X001X101 X100000100010001
0008 11100100X101X011 X011XXXX0001XXXX
0009 XXXX0010X001X101 X100001000100001
000A 11100100X101X011 X011XXXX0010XXXX
000B XXXX0010X011X011 0001XXXX0100XXXX
000C 01010000X001XXXX XXXXXXXXXXXXXXXX
000D 11110001X001XXXX XXXXXXXXXXXXXXXX
000E XXXX0110X011X011 1000XXXX0011XXXX
000F 11110001X001X011 X011XXXX0011XXXX
```

Figure 5-5. Assembly Output in Block Format

CHAPTER VI

AMPROM/80 POST PROCESSING

When a user has completed an AMDASM assembly, he may wish to output his binary object code in a form which corresponds with his PROMs' organization and/or he may wish to punch the object code from his program onto paper tapes to be used as input to a PROM burner.

In order to understand post processing one must know how the PROMs are organized in the computer memory space.

PROM ORGANIZATION

If AMDASM/80 has been executed using the command

-AMDASMΔP1(DEF)P2(ASM)O(PRMOUT)L(:LP:)

AMDASM generates binary object code for the executable statements in the file named ASM.

This binary object code is output to a file called PRMOUT.

For our example we shall assume that the microword is 48 bits wide and the number of executable statements is 1024.

This gives us a matrix 48 wide by 1024 deep as shown in Figure 6-1.

Bit No.	1 2 3 4 • 48
Executable Instruction Number	1
	2
	3
	4
	•
	•
	•
	1024

Figure 6-1. Bit Matrix

After PROM width and depth are specified, the Bit Matrix is subdivided to yield a PROM Map where each PROM is n bits wide by m bits deep. If we assume that the program origin is zero for our example, the actual PROM MAP printed might appear as shown in Figure 6-2.

	PC	C1	C2	C3	C4	C5	C6	C7	
R1	0000	1	2	3	4	5	6	7	PROM No.
R2	0100	8	9	10	11	12	13	14	
R3	0300	15	16	17	18	19	20	21	
R4	0380	22	23	24	25	26	27	28	

where

PC represents the initial program counter value for that PROM row. The PC value is given in hexadecimal.

Figure 6-2. Sample PROM MAP.

For the example, PROMs shall be organized as shown in Figure 6-3.

Each executable instruction naturally has a program counter associated with it by virtue of its position in the program and/or the origin(s) that were set during the assembly execution.

This breakup of the matrix is now called a PROM map which has associated with it, not only the PROMs shown, but rows and columns as shown in Figure 6-3. Thus, we may now refer to PROM 19 by using the digits 19, or by referencing R3 for Row 3 and C5 for Column 5.

As shown in Figure 6-4, all PROMs in Row 1 are 256 (instructions) deep, but PROMs 1, 3, 5, and 6 are only 4 bits wide, while PROMs 2 and 7 are 8 bits wide and PROM 4 is 16 bits wide.

In Row 2, all PROMs are 512 (instructions) deep and PROMs 8, 10, 12 and 13 are 4 bits wide, PROMs 9 and 14 are 8 bits wide and PROM 11 is 16 bits wide.

Rows 3 and 4 are each 128 (instructions) deep; PROMs 15, 22, 17, 24, 19, 26, 20, and 27 are 4 bits wide; PROMs 16, 23, 21, and 28 are 8 bits wide; and PROMs 18 and 25 are 16 bits wide.

If the user requests printing (or punching) of PROM #1 he will obtain data that is 4 by 256.

If the user requests printing of Row 3, he will obtain data (i.e., the contents of PROMs 15 through 21) in the following form:

4 X 128, 8 X 128, 4 X 128, 16 X 128, 4 X 128, 4 X 128, 8 X 128

If the user requests printing of Column 4 he will obtain data (i.e., the contents of PROMs 4, 11, 18, and 25) that is:

16 X 256, 16 X 512, 16 X 128, 16 X 128

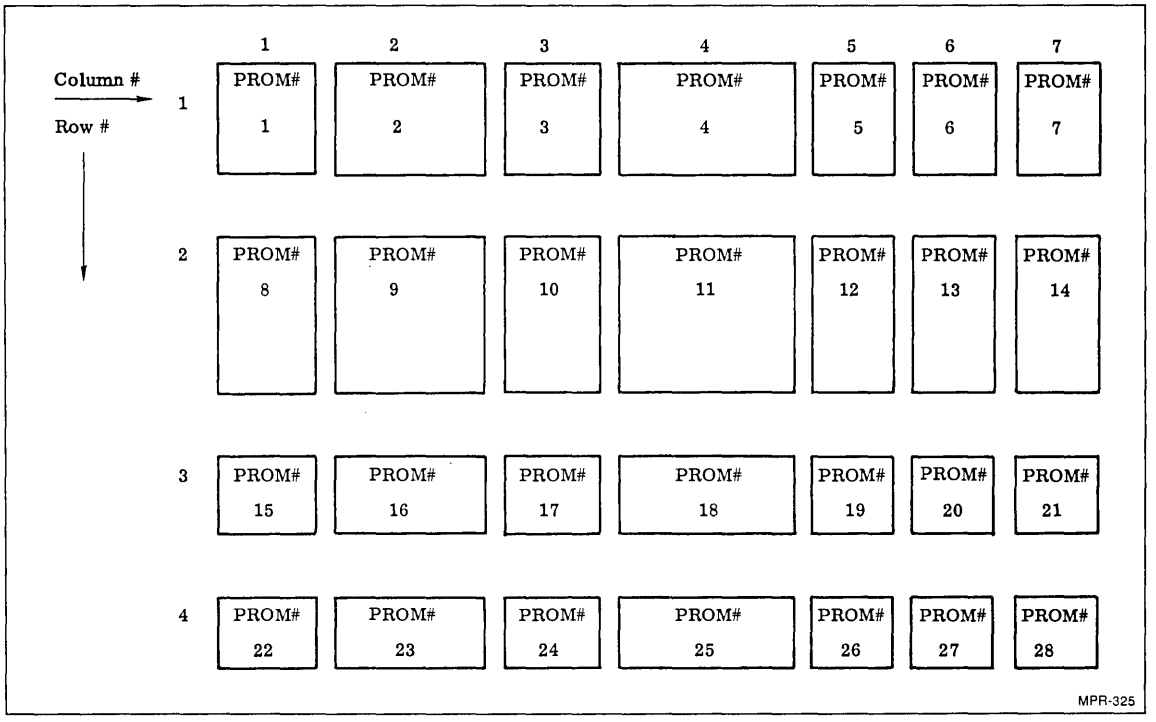


Figure 6-3. PROM MAP

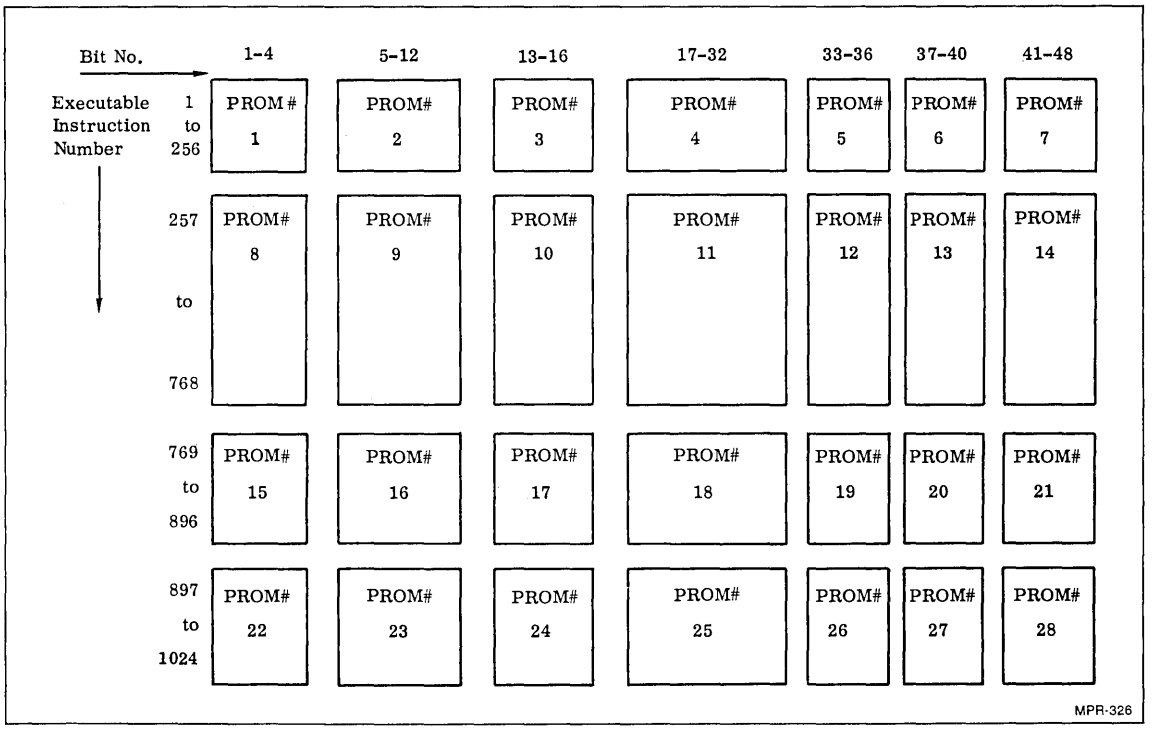


Figure 6-4. Organization of PROMs

POST PROCESSING FEATURES

AMPROM/80 allows the user to specify:

- The depth (number of instructions) and width (bits of the microword) for each PROM.
- Listing or suppression of listing of the PROM MAP.
- The PROMs to be punched or not punched on paper tape in BNPF or hexadecimal format.
- Listing or suppression of listing of PROM contents.
- Listing of the PROM contents by PROM rows **or** PROM columns **or** by PROM number.
- Optional automatic inversion of all bits except the "don't care" bits.
- Specification of "don't care" bits to be 0 or 1.

EXECUTION OF AMPROM

To execute AMPROM the general form of the command is:

−AMPROM {Δoption}

To illustrate execution of AMPROM, the command

−AMPROMΔ PUNCH (:HP:)Δ LIST (:LP:) HEX

specifies the PROM MAP is to be printed, the content of the PROMs is to be printed, and the content of the PROMs is to be punched in hexadecimal.

However,

−AMPROMΔ NOLISTΔ NOMAPΔ PUNCH (:HP:)

specifies that the content of PROMs is to be punched with no listing of the PROM MAP or PROM content.

Both examples assume the AMPROM input (AMDASM output) is on the default file named AMDASM.OBJ.

Note that each option specified is preceded by a space, the options may be given in any order, and the full option name or the alternate name may be used.

Table 6-1
AMPROM/80 Options

OPTION	ABBREVIATED OPTION	DEFAULT	MEANING
MAP	M	MAP	Print the PROM map.
NOMAP	NM		Suppress printing the PROM map. If NOMAP is not specified, the program automatically prints the PROM map.
HEX	H	HEX	Punch the PROM output in hexadecimal format.
BNPF	B		Punch the PROM output in BNPF format. If BNPF is not specified the output is automatically punched in hexadecimal
INVERT	I	No Inversion	If INVERT is specified, all ones are inverted to zeros, and zeros to ones, except for bits specified as "don't cares". If INVERT is not specified there is no modification of the binary object code.
OBJECT (filename)	O	(AMDASM.OBJ)	Specifies the name of the file on which the AMDASM object code is located. If not specified, a default file named AMDASM.OBJ is assumed.
PUNCH (filename)	P	(AMPROM.OUT)	Specifies the name of the file or device where punch data is to be output. If not specified the output goes to the file with the default name AMPROM.OUT.
NOPUNCH	NP		Suppresses punching the PROM contents. If not specified, defaults to PUNCH.
LIST (filename)	L	(AMPROM.LST)	Specifies the name of the output file or device where the AMPROM output listing is to be placed. If not specified, the output automatically goes to the default file named AMPROM.LST.
NOLIST	NL		Specifies that the output is not to be listed. This would be used when only punching of the output is desired. If not specified the program defaults to LIST using the default filename AMPROM.LST.

AMPROM FILENAMES

As part of –AMPROMΔ {options} the user may need to specify filename information. Whether filename information is needed will depend on whether or not he specified a filename for the binary output when AMDASM was executed [OBJECT (filename)] and whether the user wishes to receive his output at a printer, console or punched on paper tape.

Possible options are shown in Table 6-1.

The OBJECT (filename), PUNCH (filename) and LIST (filename) must each be preceded by a blank and may be specified in any order. The filename may be any ISIS© device.

If, for example, the user executed AMDASM with the command:

–AMDASMΔPHASE1 (DEF) PHASE2 (ASM) OBJECT (PRMOUT)

the binary object code is stored on a file called PRMOUT.

In this case when executing AMPROM, PRMOUT must be given as the input filename.

–AMPROMΔ OBJECT (PRMOUT)

and since no LIST or PUNCH is specified, all output will be to the default filenames.

If the user executes AMDASM with the command

–AMDASMΔ PHASE1 (DEF) PHASE2 (ASM)

the binary object code is output to the **default file** called AMDASM.OBJ.

AMPROM assumes the binary object code is stored on a file named AMDASM.OBJ if no input filename is given (i.e., the AMPROM input default filename is AMDASM.OBJ). Thus, in this example, the command

–AMPROM

will cause AMPROM to be executed and specifies (by default) that the binary object code is to be input from a file named AMDASM.OBJ.

The command

–AMPROMΔNOLISTΔPUNCH (PRMPNC) OBJECT (PRMDAT)

specifies that listing of the PROM content is to be suppressed, the output for punching a paper tape is to be written on a file called PRMPNC, and the input (binary object code) for execution of AMPROM is to be from a file called PRMDAT.

This assumes the AMDASM output was stored on a file called PRMDAT.

Note that the options may be given in any order desired by the user.

REQUIRED AMPROM INPUT

Once AMPROM has begun execution the user will be acting interactively with the console. He will receive messages from the console and will be expected to input responses followed by a carriage return. The terminal will print the requested output or a message requesting additional input. When execution is complete, control returns to ISIS©.

A sample of the console messages is given below. For this example, underlined letters are used to illustrate the user's input. Following the example is a table of the substitutes which may be used for these letters.

To begin execution the user has input –AMPROM. The terminal responds by printing:

DON'T CARES? Z

For example,

DON'T CARES? 1

ENTER PROM WIDTH(S) W

For example

ENTER PROM WIDTHS 4*8, 4

ENTER PROM DEPTH(S): D

For example,

ENTER PROM DEPTHS 128

If a MAP listing at the output device is requested the PROM map is output here. Then the console prints

WHICH PROMS DO YOU WISH TO PRINT? Q

For example,

WHICH PROMS DO YOU WISH TO PRINT? 5-7

If printing of the PROM content was specified, the PROM content is printed here. These same PROMs will be punched unless NOPUNCH was specified. The punch device should be turned on before keying in the PROMs to be printed and punched.

When paper tape punching is completed, control is returned to ISIS©.

INPUT SUBSTITUTES

When the terminal requests information the substitutes permitted are shown in Table 6-2.

Table 6-2.
AMPROM Input Substitutes

Console Prompt	Substitutes	Meaning
DON'T CARES?	0 or 1	The value specified here is assigned to all "don't care" bits in the PROM(s). Any value except 0 or 1 is an error and the prompt is repeated.
ENTER PROM WIDTHS	n	n is a decimal integer and each PROM is n bits wide. If the microword size is 60 and n is given as 8, 8 PROMs will be generated. The first seven will contain actual microword information but the 8th PROM will contain microword information in its leftmost 4 bits and "don't cares" in the 4 right-hand bits. (i.e., if the microword width is not an even multiple of n, it is padded on the right with "don't cares").
	l•b	l is a decimal integer indicating a number of PROMs. b is a decimal integer indicating the number of bits wide each of these PROMs should be Thus, 3 • 4 means there are 3 PROMs each 4 bits wide.
	Combinations of n and l•b	For the PROM MAP (Figure 6-4), the user would write 4, 8, 4, 16, 2•4, 8. Any combination of n and l•b is permissible if separated by commas and if the total number of bits is greater than or equal to the microword width.
ENTER PROM DEPTHS	r	r is a decimal integer and each PROM is r instructions deep (long). If the binary object code is not an even multiple of r, AMPROM fills the final PROM locations with "don't cares".
	t•d	t is a decimal integer indicating a number of PROMs. d is a decimal integer indicating how many words deep each of these PROMs is to be. Thus 2 • 512 indicates there are 2 PROMs each 512 bits deep.
	Combinations of r and t•d	For the PROM MAP in Figure 6-4, the user would write 256, 512, 2•128. Any combination of r and t•d is permissible if separated by commas.
WHICH PROMS DO YOU WISH TO PRINT***	Y	Y is a decimal integer which is a PROM number. 5 means list the contents of PROM #5.
	Y_1-Y_n	Y_1 is a decimal integer specifying the number of the first PROM to be listed. Y_n is a decimal integer specifying the last PROM to be listed. Thus, 2-5 specifies listing of PROMs 2, 3, 4 and 5.
	Combinations of Y and Y_1-Y_n	3, 5-7, 9 means print (and punch) PROMs 3, 5, 6, 7 and 9. All combinations of Y and Y_1-Y_n are acceptable if separated by commas.
	Cs	C means column and s is a decimal integer which specifies the PROM column desired. C4 means print all PROMs in column 4.
	Cs_1-s_n	Print columns s_1, through s_n. C1-6 indicates print PROM columns 1 through 6.
	Combinations of Cs, s_1-s_n	C5, 7-9, 11 means print columns 5, 7, 8, 9, 11. C3-6, 10 means print columns 3, 4, 5, 6, 10 (i.e., C is only given once, then the s and/or s_1-s_n separated by commas).
	Rs	R means row and s is a decimal integer which specifies the row desired. R1 means print all PROMs in row 1.
	Rs_1-s_n	List the contents of PROM rows s_1, through s_n. R2-6 means print all PROMs in rows 2 through row 6.
	Combinations of Rs, s_1-s_n	The same as columns. The R is given once, followed by the row numbers separated by commas. R1, 4-6, 11-13 prints rows 1, 4, 5, 6, 11, 12, 13.
	N	The letter N is typed if the user wishes to indicate none of the PROM contents are to be listed
	A	The letter A when typed means all PROMs are to be printed.

***The same PROMs are printed and/or punched. Thus, all values for printing apply for punching also.

BNPF PAPER TAPE OPTION

When BNPF is specified as an option, the tape is punched in the BNPF format. B is punched as the first character, then a P (for a one) or an N (for a zero) is punched for each bit in the width of this PROM, then an F is punched as the last character for this row of PROM data. This continues until all rows (the depth) of the PROM are punched.

Before the first BNPF for each PROM is punched, the program punches identification on the tape which consists of:

- 32 Rubouts
- 4 ASCII characters which are the PROM number
- 32 NULs to be used as the leader when loading the PROM burner tape reader

After the PROM data is punched, 40 NULS are punched to facilitate tape handling.

For example, if PROM#5 is 4 bits wide by 128 bits deep, and begins at origin zero, the paper tape will appear as shown in Table 6-3.

Table 6-3
BNPF Paper Tape Contents

Tape Contents	Content Explanation
$Rubout_1$	
•	
•	32 Rubouts
•	
$Rubout_{32}$	
Characters 0005	PROM number
NUL_1	
•	
•	32 NULs
•	
NUL_{32}	
Character B	
Character N or P	BPNF format for one
Character N or P	row of this 4-bit wide
Character N or P	PROM
Character N or P	
Character F	
Space	*See Note
Character B	
Character N or P	Repeated 127 times
•	
•	
•	
NUL_1	
•	
•	40 trailing NULs
•	
NUL_{40}	

*Note: Carriage return/line feed for possible listings is inserted after 8 words for PROMs 4 or less bits wide, after 4 words for widths of 16 or less bits, and after one word for widths greater than 16.

HEXADECIMAL PAPER TAPE OPTION

When punching is desired, and HEX is specified or assumed by default, the PROM contents are punched in the DATA I/O hexadecimal format.

The same initial data (32 Rubouts, PROM number and 32 NULs) is punched as is punched for the BNPF format, followed by the PROM contents in hexadecimal.

For PROMs 4 or less bits wide, one hexadecimal character and a space is punched. For PROMs greater than 4 bits wide, two hexadecimal characters and a space are punched. Thus two characters, space, two characters, space would be punched for either 2 rows of an 8-bit PROM, or for 1 row of a 16-bit wide PROM.

Thus if PROM #7 (16 bits x 128 words) is punched, the output will be:

Table 6-4
Hexadecimal Paper Tape Contents

Tape Contents	Content Explanation
$Rubout_1$	
•	
•	32 Rubouts
•	
$Rubout_{32}$	
Characters 0007	PROM Number
NUL_1	
•	
•	32 NULs
•	
NUL_{32}	
SOH	Start of Header
Character	
Character	
Blank	Contents of
Character	PROM Row 1
Character	(4 HEX digits)
Blank	
Character	
Character	Repeated 127 Times
•	*See Note
•	
•	
ETX	End of Text
NUL_1	
•	
•	40 NULs
•	
NUL_{40}	

*Note: A carriage return/line feed for possible listings is inserted after 16 groups of hexadecimal characters.

EXAMPLE OF AMPROM

Figure 6-5 is an example of AMPROM/80 for the AMD 2900 Learning & Evaluation Kit.

```
CONSOLE INPUT
DON'T CARES?Ø
ENTER PROM WIDTH?8
ENTER PROM DEPTH?16
WHICH PROMS DO YOU WISH TO PRINT?3-4

AMPROM OUTPUT

AMD AMPROM UTILITY
AM29ØØ KIT EXERCISE 1ØB
PROM MAP
     PC    C1    C2    C3    C4
R1  ØØØØ    1     2     3     4
PROM CONTENTS
PC   ADD P 3      P 4
ØØØØ ØØØ ØØ11ØØØØ ØØØØ1111
ØØØ1 ØØ1 ØØ11ØØØØ ØØØ11ØØ1
ØØØ2 ØØ2 ØØ11ØØØØ ØØ1ØØØØØ
ØØØ3 ØØ3 ØØ11ØØØØ Ø1ØØØ1ØØ
ØØØ4 ØØ4 Ø1ØØØØØØ ØØ11ØØØØ
ØØØ5 ØØ5 Ø1ØØØØØØ ØØØØØØØ1
ØØØ6 ØØ6 ØØ11ØØØØ ØØØØØØØØ
ØØØ7 ØØ7 Ø1ØØØØØ1 ØØØ1ØØØ1
ØØØ8 ØØ8 ØØ11ØØØØ ØØØ1ØØØØ
ØØØ9 ØØ9 Ø1ØØØØ1Ø ØØ1ØØØØ1
ØØØA ØØA ØØ11ØØØØ ØØ1ØØØØØ
ØØØB ØØB ØØØ1ØØØØ Ø1ØØØØØØ
ØØØC ØØC ØØØØØØØØ ØØØØØØØØ
ØØØD ØØD ØØØØØØØØ ØØØØØØØØ
ØØØE ØØE 1ØØØØØØØ ØØ11ØØØØ
ØØØF ØØF ØØ11ØØØØ ØØ11ØØØØ

PUNCH OUTPUT

  3
BNNPPNNNNF BNNPPNNNNF BNNPPNNNNF BNNPPNNNNF
BNPNNNNNNF BNPNNNNNNF BNNPPNNNNF BNPNNNNNPF
BNNPPNNNNF BNPNNNNNPF BNNPPNNNNF BNNNPNNNNF
BNNNNNNNNF BNNNNNNNNF BPNNNNNNNF BNNPPNNNNF
  4
BNNNNPPPPF BNNNPPNNPF BNNPNNNNNF BNPNNNPNNF
BNNPPNNNNF BNNNNNNNPF BNNNNNNNNF BNNNPNNNPF
BNNNPNNNNF BNNPNNNNPF BNNPNNNNNF BNPNNNNNNF
BNNNNNNNNF BNNNNNNNNF BNNPPNNNNF BNNPPNNNNF
```

Figure 6-5. AMPROM/80 Output for AMD 2900 Learning Kit.

CHAPTER VII

ERROR MESSAGES AND INTERPRETATIONS

AMDASM ERRORS

Each source file input statement is processed until a single error is detected. One missing comma between fields, for example, would result in incorrect processing of the remainder of the statement.

Thus, the assembler stops when an error is encountered, records the error and the statement which caused it, and proceeds to process subsequent source input statements.

AMDASM and AMPROM error messages will have the form

*** ERROR n {y}

where n is the error number and y, if present, contains the illegal character or symbol. Fatal error messages appear on the console output device as well as on the assembly list file.

Error messages will sometimes seem inappropriate for the statement being processed. This occurs because the assembler is unable to determine the programmer's intent. This is often the result of a missing comma (,), semicolon (;), blank (Δ) or colon (:).

Errors where n is ≥ 100 halt execution.

It is recommended that the user read the entire error message section.

ERROR 1 ILLEGAL CHARACTER

The character which cannot be interpreted is printed and the line in which it occurs is also printed. This message may be generated by:

- Striking the wrong console key.
- A missing comma or semicolon (B#101Q#7 is not interpretable).
- A wrong number base used (B#3 or Q#8 cannot be interpreted).

ERROR 2 UNDEFINED SYMBOL

This message will most often occur when:

- Something is misspelled.

  HERE: EQUΔ100
  GO.TO: DEFΔ HEER (the assembler cannot find HEER)

- The # is missing after a B, Q, D, or H.
- The space is missing after definition words DEF, EQU, SUB, WORD, TITLE, RES, ORG, ALIGN, FF, SPACE
- A symbol is referenced before it is defined by a SUB or an EQU.
- A VFS for a hexadecimal field begins with the letters A through F and the H# designator does not precede the letter.

ERROR 3 UNDEFINED FORMAT

The format name given is misspelled or was not defined in the Definition Phase or the required blank was not supplied after the format name.

ERROR 4 DUPLICATE FORMAT

The name given before a format (DEF) has already been used as a name. If names contain more than 8 characters, the first 8 must be unique. Check for misspelled names.

ERROR 5 DUPLICATE LABEL

This label has been used more than once as a constant name or a label. If the label is more than 8 characters, the first 8 must be unique.

ERROR 6 DUPLICATE SUBDEFINE

The name given preceding a subformat (SUB) has already been used as a name. If names contain more than 8 characters, the first 8 must be unique. Check for misspelled names.

ERROR 7 FORMAT FIELD OVERFLOW

The user is permitted a maximum of 128 fields per format name (DEF). This number has been exceeded. The format must be revised and fields must be combined.

ERROR 8 SUBDEFINE FIELD OVERFLOW

The user is permitted a maximum of 128 fields per subformat name (SUB). This number has been exceeded. Revise the subformat and combine fields or use two subformats for this bit pattern.

ERROR 9 UNDEFINED DIRECTIVE

No name: was found and the characters given are not TITLE, WORD, LIST, NOLIST, END, ORG, RES, SPACE, or ALIGN.

Check for a missing colon after a name, or misspelling, or blanks in TITLE, WORD, etc.

ERROR 10 ILLEGAL MICROWORD LENGTH

Each time DEF or FF is encountered, the assembler checks to see if the sum of the bits for all fields for this format name **exactly** equals the microword length.

Thus, the user is assured that each DEF or FF contains an exact number of bits. If the number of bits in this format does not **exactly** equal the number of bits given with WORD, the interpretation of the faulty DEF or FF is bypassed and the assembler attempts interpretation of the next source statement.

ERROR 11 ILLEGAL FIELD LENGTH

No field, except a "don't care" field, may be more than 16 bits in length. The value calculated for this field cannot be represented in 16 bits.

ERROR 12 DON'T CARE FIELD TOO LONG.

The explicit length given for a "don't care" field exceeds the microword length specified by WORD. Improper digits may have been assumed for the explicit length due to a missing comma or designator.

ERROR 13 ARITHMETIC OPERATION ON FIXED FIELD.

If a field is defined as a variable field in the Definition File, an expression cannot be used as a VFS in the Assembly File unless the field contained the % attribute in its definition.

ERROR 14 ATTRIBUTE ERROR

Both the negative (−) sign and inversion (*) have been assigned to a single variable or constant. This is not permitted. 4V−* or 4B#1011*− are meaningless.

ERROR 15 (Not used)

ERROR 16 MISSING END STATEMENT

The Definition or Assembly File is missing the END statement.

ERROR 17 ILLEGAL SYMBOL

A character other than A through Z, digits 0 through 9, or period was used in a name, or a comma may be missing between fields.

ERROR 18 OVERLAY ERROR

This message is given when two formats are overlayed and both of them contain constants for the same bit position. If the assembler is run using each of the formats in the overlay statement as a separate format, and the output is printed in block form, the erroneous bits are easily detected.

For example if the Definition File statements are:

A: DEFΔ4X,B#1011
B: DEFΔB#01111,3X

and the Assembly File statement is

A & B

the overlay error message occurs.

Rerun the Assembly File with source statements given as

A
B

and block output requested which generates

XXXX [1] 011
0111 [1] XXX

It can easily be seen that bits [1] are causing the overlay error. The improper DEF can then be corrected and the overlay A & B can be used in the Assembly File statement.

ERROR 19 NO DEFAULT VALUE

A format name was defined with a variable field in the Definition File. Since no default value was given in the definition, a variable field substitute **must** be supplied for this field when the format name is used in the Assembly File. Check for missing commas.

ERROR 20 FIELD LENGTH CONFLICT

The calculated or implicit field length for the constant or expression given after the designator does not have the same number of bits as the explicit field length. Check for a missing % or :, or a comma missing after the previous field.

This message may be output when commas are left out. For example,

8H#A39Q#274

is missing the comma between 3 and 9. Thus the program assumes A39 is to be substituted into the 8-bit hexadecimal field.

Similarly,

8H#A3, 9Q27, 4

will generate this error message since the comma between the 7 and the 4 is misplaced.

ERROR 21 $ SPECIFIED FOR NON-ADDRESS FIELD

In order to use the value of the program counter (indicated with a $) as a VFS, that field must contain the % attribute.

ERROR 22 (Not used)

ERROR 23 MISSING DESIGNATOR

A field has been encountered which contains only decimal numbers. This is not permitted for a field in a DEF, SUB or FF. Decimal numbers must be input as, n D# digits, where n is the explicit length of the field and digits are the decimal integers which generate the desired bit pattern or field value.

ERROR 24 SPACE DIRECTIVE ERROR

The value input following SPACE is interpreted as less than zero or greater than the number of lines given per page.

ERROR 25 ORG SET TO LESS THAN CURRENT PC

When ORG is encountered, the value given is compared with the current program (location) counter. If ORG is less than the program counter, the value given with ORG is ignored.

ERROR 26 NO FORMAT NAME AFTER &

When a line ends with an & and no continuation (/) is given at the beginning of the next line, this error is generated. A format name is missing after the &, or a / is missing on the continuation line.

ERROR 27 (Not used)

ERROR 28 ADDRESS NOT IN CURRENT PAGE

When the user gives a label or a label$ as a VFS or has defined his variable field with the $ attribute, this message will be generated if the left bits to be truncated do not match the corresponding bits of the current program counter.

ERROR 29 LENGTH REQUIRED FOR $ MODIFIER

Paged addressing (use of the $ as a modifier) requires the field length before the symbol in FF statements. Thus, 6SYMBOL$ is correct but SYMBOL$ is incorrect.

ERROR 30 ILLEGAL FIELD LENGTH IN FF STMT.

A field is greater than 16 bits in a FF statement. Only "don't care" fields may be larger than 16 bits.

ERROR 31 (Not used)

ERROR 32 NO EXPLICIT LENGTH BEFORE (

An expression in a FF statement must be enclosed in (). The explicit field length must precede the (.

AMDASM ERRORS WHICH HALT EXECUTION

Error messages with n ≥ 100 cause execution to stop. They are listed below:

ERROR 100 COMMAND OPTION SYNTAX ERROR

The input command contains an error. Check for correct spelling of filenames and options, spaces between options, and correct drive specification with filenames.

ERROR 101 DEF TABLE OVERFLOW

ERROR 102 SUB TABLE OVERFLOW

ERROR 103 EQU TABLE OVERFLOW

ERROR 106 FIELD TABLE OVERFLOW

Errors 101, 102, 103 and 106 occur when the amount of memory available has been exceeded.

ERROR 104 INCORRECT OR MISSING WORD SIZE

Either the WORD n command is not given as the first command (or the first command after TITLE) or the value given for n is < 1 or > 128.

ERROR 105 UNEXPECTED END OF FILE

The user has given an incorrect file name or the source file is not correct. AMDASM has encountered an end of file when it was still expecting data.

AMPROM ERRORS

ERROR 1 DON'T CARE DEFINITION ERROR

A value other than zero or one was input as the value for "don't care" bits. The user has input an incorrect character.

ERROR 2 WIDTH INPUT SYNTAX ERROR

The PROM width specified using n and/or l*b has been stated incorrectly. Check for missing commas or asterisks.

ERROR 3 WIDTH EXCEEDS MICROWORD SIZE

The width given for all of the PROMs totals to so many bits that at least one additional PROM width is being specified. For example, if the microword width is 60 and PROM width is specified as 9*8, an error will be generated as there are 12 (72-60) extra bits specified which is greater than the 8-bit width of each PROM. Program execution stops. However, 8*8 will not generate an error since the extra 4 bits (64-60) will fit within one 8-bit wide PROM.

ERROR 4 TOO MANY PROM COLUMNS

The user is limited to 32 columns in his PROM MAP. When a number of columns greater than 32 is specified this error occurs.

ERROR 5 DEPTH INPUT SYNTAX ERROR

The data (r and/or t*d) specifying the PROM depths has been input incorrectly. Check for missing commas or asterisks.

ERROR 6 WARNING DEPTH EXCEEDS MAXIMUM PC

The depth specified by the user will require at least one additional PROM filled with "don't cares".

Thus, if the object code depth is 120 words and the user specifies 3*64 for t*d, the extra 72 words are flagged as an error. However, if the user specified 2*64 (or 128) the extra 8 words would simply be filled with "don't cares". This is issued as a warning message. The additional PROM is filled with "don't cares" and the program continues executing.

ERROR 7 TOO MANY PROM ROWS

A PROM MAP may contain a maximum of 64 rows. This provides for 64K of storage if the user has chosen 1K PROMs. A PROM MAP with more than 64 rows is not permitted.

ERROR 8 ILLEGAL VALUE FOR ROWS OR COLUMNS

The user has input something other than a decimal integer Y or Rs or Cs or the letters N or A.

The user may have forgotten the – between Y_1 and Y_n or Cs_1 and s_n, etc.

ERROR 9 ILLEGAL PROM NO., ROW, OR COLUMN DESIGNATION

The user has requested a PROM number or a PROM row or column using a decimal value greater than any of the PROM numbers, PROM row numbers, or PROM column numbers.

ERROR 10 UNEXPECTED END OF FILE ON INPUT FILE.

This error only occurs when input to AMPROM is from a file (i.e., the user is not inputting the data interactively). A line giving the "don't care" value, the PROM width or the PROM depth, or the printing information has been omitted.

ERROR 100 COMMAND OPTION SYNTAX ERROR

This error occurs due to illegal command options or illegal syntax.

Execution halts and the correct command must be entered.

Check for misspelling, missing blanks or =, or incorrect drive specifications.

NOTE: Errors 1, 2 and 5 are indicated on the console and the previous data request is repeated. In order to end this loop, the user must input correct data or abort. For AMPROM/29 enter Control-C. For AMPROM/80 push interrupt 1.

APPENDIX A
ERRORS

AMDASM ERRORS

ERROR 1 ILLEGAL CHARACTER
ERROR 2 UNDEFINED SYMBOL
ERROR 3 UNDEFINED FORMAT
ERROR 4 DUPLICATE FORMAT
ERROR 5 DUPLICATE LABEL
ERROR 6 DUPLICATE SUBDEFINE
ERROR 7 FORMAT FIELD OVERFLOW
ERROR 8 SUBDEFINE FIELD OVERFLOW
ERROR 9 UNDEFINED DIRECTIVE
ERROR 10 ILLEGAL MICROWORD LENGTH
ERROR 11 ILLEGAL FIELD LENGTH
ERROR 12 DON'T CARE FIELD TOO LONG
ERROR 13 ARITHMETIC OPERATION ON FIXED FIELD
ERROR 14 ATTRIBUTE ERROR
ERROR 15 (Not used)
ERROR 16 MISSING END STATEMENT
ERROR 17 ILLEGAL SYMBOL
ERROR 18 OVERLAY ERROR
ERROR 19 NO DEFAULT VALUE
ERROR 20 FIELD LENGTH CONFLICT
ERROR 21 $ SPECIFIED FOR NON-ADDRESS FIELD
ERROR 22 (Not used)
ERROR 23 MISSING DESIGNATORS
ERROR 24 SPACE DIRECTIVE ERROR
ERROR 25 ORG SET TO LESS THAN CURRENT PC
ERROR 26 NO FORMAT NAME AFTER &
ERROR 27 (Not used)
ERROR 28 ADDRESS NOT IN CURRENT PAGE
ERROR 29 LENGTH REQUIRED FOR $ MODIFIER
ERROR 30 ILLEGAL FIELD LENGTH IN FF STMT
ERROR 31 (Not used)
ERROR 32 NO EXPLICIT LENGTH BEFORE (

AMDASM ERRORS WHICH HALT EXECUTION

ERROR 100 COMMAND OPTION SYNTAX ERROR
ERROR 101 DEF TABLE OVERFLOW
ERROR 102 SUB TABLE OVERFLOW
ERROR 103 EQU TABLE OVERFLOW
ERROR 104 INCORRECT OR MISSING WORD SIZE
ERROR 105 UNEXPECTED END OF FILE
ERROR 106 FIELD TABLE OVERFLOW

AMPROM ERRORS

ERROR 1 DON'T CARE DEFINITION ERROR
ERROR 2 WIDTH INPUT SYNTAX ERROR
ERROR 3 WIDTH EXCEEDS MICROWORD SIZE
ERROR 4 TOO MANY PROM COLUMNS
ERROR 5 DEPTH INPUT SYNTAX ERROR
ERROR 6 WARNING DEPTH EXCEEDS MAXIMUM PC
ERROR 7 TOO MANY PROM ROWS
ERROR 8 ILLEGAL VALUE FOR ROWS OR COLUMNS
ERROR 9 ILLEGAL PROM NO., ROW, OR COLUMN DESIGNATION
ERROR 10 UNEXPECTED END OF FILE ON INPUT FILE
ERROR 100 COMMAND OPTION SYNTAX ERROR

ADVANCED MICRO DEVICES
SCHOTTKY AND LOW-POWER SCHOTTKY MSI

Advanced Micro Devices offers a complete line of Schottky and Low-Power Schottky MSI products. On the following pages are a selector guide for these products and brief data on several of the most useful parts. For complete data refer to our Schottky and Low-Power Schottky Data Book.

Advanced Micro Devices offers two LS Logic families.

- Am25LS – High Performance
- Am54/74LS – Standard Performance

Similar elements of both families are described on the same data sheet. Key parameters are compared below.

All Advanced Micro Devices' products are manufactured to the quality assurance requirements of MIL-STD-883, Level C. According to Handbook 217B published by the Rome Air Development Center, the Air Force's principal authority on component reliability, Level C integrated circuits are up to ten times more reliable than normal industry commercial parts.

Even if you don't need the performance features of Am25LS, you can buy our versions of 54/74LS devices with the assurance that they are manufactured to the stringent quality standards of MIL-STD-883.

10X MORE RELI

50mV MOF NOISE MAR

Am25LS IMPROVED PERFORMANCE

- Noise Margin
  At I_{OL} = 8mA, Am25LS guarantees V_{OL} = 0.45V compared to 0.50V for 54/74LS.
- Fan Out
  Over the military temperature range, Am25LS is specified at I_{OL} = 8mA, for a F.O. of 22 (8mA/0.36mA). 54LS is guaranteed at I_{OL} = 4mA only, for F.O. = 11 (4mA/0.36mA).
- I_{SC} (Max.)
  Am25LS has I_{SC} upper limit controlled to 85mA (Max.).
- Speed
  In this example, Am25LS164 has worst case clock to output delay specified at up to 45% faster and f_{MAX} at more than 40% faster than 54/74LS164: Most Am25LS devices offer similar improvements.

TWICE TH FAN-OUT

REDUCED SUPP CURRENT SPIKI

FASTER

SWITCHING SPEED SPECIFIED AT TEMPERATURE AND POWER SUPPLY EXTREMES

The switching speeds of all new Am25LS devices are now being specified at:

- Full 50pF load
- Over the operating temperature range
  - Military –55°C to +125°C
  - Commercial 0°C to +70°C
- Over the operating power supply range
  - Military 5.0V ± 10%
  - Commercial 5.0V ± 5%

MORE FULLY SPECIFIED

PRICE

Most Am25LS device list prices are the same or less than the equivalent 54/74LS standard performance device.

Am25LS164 • Am54LS/74LS164

8-Bit Serial-In, Parallel-Out Shift Register

DISTINCTIVE CHARACTERISTICS

- Gated serial inputs
- Asynchronous clear
- Am25LS devices offer the following improvements over Am54/74LS
  - Higher speed
  - 50mV lower V_{OL} at I_{OL} = 8mA
  - Twice the fan-out over military range
  - 440µA source current at HIGH output
- 100% product assurance testing to MIL-STD-883 requirements

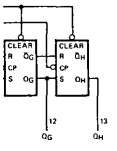
FUNCTIONAL DESCRIPTION

The Am25LS164 and Am54LS/74LS164 are eight-bit, serial in/parallel out shift registers built using advanced Low-Power Schottky processing. A gated input provides enable/disable control over incoming data such that the data can be entered or logic zeros can be entered into the register.

An asynchronous clear input can be used to simultaneously clear the eight flip-flops in the device. When the clear input is LOW, all internal flip-flops are forced LOW independent of the clock input. An incoming data bit is entered into the Q_a flip-flop and the data in all internal flip-flops is shifted right on the LOW-to-HIGH transition of the clock input.

The Am54LS/74LS164 is a standard performance version of the Am25LS164. See appropriate electrical characteristic tables for detailed Am25LS improvements.

LOGIC DIAGRAM



ELECTRICAL CHARACTERISTICS

The Following Conditions Apply Unless Otherwise Specified:

COM'L T_A = 0°C to +70°C V_{CC} = 5.0V ±5% MIN. = 4.75V MAX. = 5.25V

MIL T_A = −55°C to +125°C V_{CC} = 5.0V ±10% MIN. = 4.50V MAX. = 5.50V

DC CHARACTERISTICS OVER OPERATING RANGE

Am25LS164

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −440µA, V_{IN} = V_{IH} or V_{IL}	MIL	2.5	3.4		Volts
			COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA		0.25	0.4	Volts
			I_{OL} = 8.0mA		0.35	0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	Clock, Clear			−0.36	mA
			A, B			−0.4	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V				20	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 7.0V				0.1	mA
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.		−15		−85	mA
I_{CC}	Power Supply Current (Note 4)						

Notes: 1. For conditions shown as MIN. or MAX
2. Typical limits are at V_{CC} = 5.0V, 25°C
3. Not more than one output should be sh
4. Measured with outputs open, serial inp

Am54LS/74LS164

MAX. = 5.25V
MAX. = 5.50V

ditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
−400µA	MIL	2.5	3.4		Volts
	COM'L	2.7	3.4		
All, I_{OH} = 4.0mA			0.25	0.4	Volts
74LS only, I_{OL} = 8.0mA			0.35	0.5	
ical HIGH		2.0			Volts
				0.7	Volts
				0.8	
				−1.5	Volts
				−0.4	mA
				20	µA
				0.1	mA
				−100	mA
				27	mA

cable device type.

SWITCHING CHARACTERISTICS

(T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Am25LS Min.	Am25LS Typ.	Am25LS Max.	Am54LS/74LS Min.	Am54LS/74LS Typ.	Am54LS/74LS Max.	Units	Test Conditions
t_{PLH}	Clock to Output		14	20		17	27	ns	C_L = 15pF, R_L = 2.0kΩ
t_{PHL}			17	22		21	32	ns	
t_{PHL}	Clear to Output		19	29		24	36	ns	
t_{pw}	Clock or Clear	17			20			ns	
t_s	Data	10			15			ns	
t_h	Data	5.0			5.0			ns	
t_s	Clear Recovery Time	20			–	–		ns	
f_{max}	Maximum Clock Frequency	35	42		25	36		MHz	

Am25LS ONLY SWITCHING CHARACTERISTICS OVER OPERATING RANGES*

Parameters	Description	Am25LS COM'L T_A = 0°C to +70°C, V_{CC} = 5.0V ±5% Min.	Am25LS COM'L Max.	Am25LS MIL T_A = −55°C to +125°C, V_{CC} = 5.0V ±10% Min.	Am25LS MIL Max.	Units	Test Conditions
t_{PLH}	Clock to Output		26		30	ns	C_L = 50pF, R_L = 2.0kΩ
t_{PHL}			30		35		
t_{PHL}	Clear to Output		37		42	ns	
t_{pw}	Clock or Clear	22		25		ns	
t_s	Data	13		15		ns	
t_h	Data	5		5		ns	
t_s	Clear Recovery Time	25		30		ns	
f_{max}	Maximum Clock Frequency	25		20		MHz	

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

SCHOTTKY AND LOW-POWER SCHOTTKY FUNCTIONAL SELECTOR GUIDE

This guide divides the AMD Low-Power Schottky and Schottky TTL Product Line by function into three basic performance categories indicated by the examples below.

1. High-Performance, Low-Power Schottky Ex. 25LS174 Six Bit Register. f_{max} = 40MHz (Min.)
2. Standard Low-Power Schottky Ex. 74LS174 Six Bit Register. f_{max} = 30MHz (Min.)
3. High-Speed Schottky Ex. 74S174 Six Bit Register. f_{max} = 75MHz (Min.)

DESCRIPTION	HIGH-PERFORMANCE LOW-POWER SCHOTTKY	STANDARD LOW-POWER SCHOTTKY	HIGH-SPEED SCHOTTKY
DECADE (BCD) COUNTERS			
Asynchronous Clear	25LS160	54/74LS160	54/74S160/93S10
Synchronous Clear	25LS162	54/74LS162	
Up-Down, Synchronous Preset	25LS168	54/74LS168	
Up-Down, Asynchronous Preset, Single Clock	25LS190	54/74LS190	
Up-Down, Asynchronous Preset, Dual Clock	25LS192	54/74LS192	
Up-Down, Synchronous Preset, Three-State	*25LS2568		
BINARY HEXADECIMAL COUNTERS			
Asynchronous Clear	25LS161	54/74LS161	54/74S161/93S16
Synchronous Clear	25LS163	54/74LS163	
Up-Down, Synchronous Preset	25LS169	54/74LS169	
Up-Down, Asynchronous Preset, Single Clock	25LS191	54/74LS191	
Up-Down, Asynchronous Preset, Dual Clock	25LS193	54/74LS193	
Up-Down, Synchronous Preset, Three-State	*25LS2569		
DECODER/DEMULTIPLEXERS			
One-of-Ten Decoder/Demultiplexer, Polarity Control	25LS2537		
One-of-Eight Decoder/Demultiplexer	25LS138	54/74LS138	54/74S138
One-of-Eight Decoder/Demultiplexer with Control Storage	25LS2536		
Dual One-of-Four Decoder/Demultiplexer	25LS139	54/74LS139	54/74S139/93S21
One-of-Eight Decoder/Demultiplexer, Polarity Control	25LS2538		
Dual One-of-Four Decoder/Demultiplexer, Polarity Control	25LS2539		
MULTIPLEXERS			
Eight-Input Multiplexer	25LS151	54/74LS151	54/74S151
Eight-Input Multiplexer with Control Storage	25LS2535		
Three-State Eight-Input Multiplexer	25LS251	54/74LS251	54/74S251
Dual Four-Input Multiplexer	25LS153	54/74LS153	54/74S153
Three-State Dual Four-Input Multiplexer	25LS253	54/74LS253	54/74S253
Quad Two-Input Multiplexer; Non-Inverting	25LS157	54/74LS157	54/74S157/93S22
Three-State Quad Two-Input Multiplexer; Non-Inverting	25LS257	54/74LS257	54/74S257
Quad Two-Input Multiplexer; Inverting	25LS158	54/74LS158	54/74S158
Three-State Quad Two-Input Multiplexer; Inverting	25LS258	54/74LS258	54/74S258
MONOSTABLE (ONE-SHOT)			
Dual Retriggerable, Resettable Monostable Multivibrator			26S02
OPERATORS (ALU, MULTIPLIER, PRIORITY ENCODER, etc.)			
Four by Two Two's Complement Multiplier			25S05
Four-Bit, Four-Way Shifter			*25S10/54/74S350
Four-Bit ALU/Function Generator	25LS181	54/74LS181	54/74S181
Four-Bit ALU/Function Generator	25LS2517		
Four-Bit ALU/Function Generator	25LS381	54/74LS381	
Four-Bit Parallel Accumulator	25LS281	54/74LS281	
Priority Encoder, Eight Line to Three Line	25LS148	54/74LS148	
Four-Bit Serial Adder/Subtractor	*25LS15		
Priority Encoder, Three State	25LS2513		
Eight by One Serial/Parallel Two's Complement Multiplier	*25LS14		
Eight-Bit by Eight-Bit Multiplier/Accumulator	*25LS2516		
Eight-Bit Comparator	25LS2521		
Eight-Bit Registered Comparator	25LS2524		
System Clock Generator and Driver	25LS2525		

*Data Sheet on following pages.

FUNCTIONAL SELECTOR GUIDE (Cont.)

DESCRIPTION	HIGH-PERFORMANCE LOW-POWER SCHOTTKY	STANDARD LOW-POWER SCHOTTKY	HIGH-SPEED SCHOTTKY
PARITY CHECKER/GENERATORS			
Nine-Input Parity Checker/Generator			82S62
Twelve-Input Parity Checker/Generator			93S48
REGISTERS			
Four-Bit Register with Common Clock Enable	25LS08	54/74LS379	*25S08/54/74S379
Four-Bit Register with Two-Input Multiplexers on Inputs	25LS09	54/74LS399	*25S09/54/74S399
Four-Bit Register with Standard and Three-State Outputs	25LS2518		25S18/54/74S388
Four-Bit, Two-Output Three-State Register	25LS2519		
Four-Bit Register with Common Clear	25LS175	54/74LS175	54/74S175
Four-Bit Register; Shift Right, Left or Parallel Load	25LS194A	54/74LS194A	54/74S194
Four-Bit Register; Shift Right or Parallel Load	25LS195A	54/74LS195A	54/74S195
Six-Bit Register with Common Clock Enable	25LS07	54/74LS378	*25S07/54/74S378
Six-Bit Register with Common Clear	25LS174	54/74LS174	54/74S174
Eight-Bit, Serial-In, Parallel-Out Register	25LS164	54/74LS164	
Eight-Bit Shift/Storage Register; Synchronous Clear	25LS23		
Eight-Bit Shift/Storage Register; Asynchronous Clear	25LS299	54/74LS299	
Eight-Bit Shift-Storage Register with Sign Extend	*25LS22		
Octal D-Type Register, Common Clear	25LS273	54/74LS273	
Octal Transparent Latch (Three State)	25LS373	54/74LS373	*54/74S373
Octal D-Type Register (Three State)	25LS374	54/74LS374	*54/74S374
Octal D-Type Register, Common Enable	25LS377	54/74LS377	
Four-Bit by Four-Bit Register File(O.C.)	25LS170	54/74LS170	
Four-Bit by Four-Bit Register File (Three State)	25LS670	54/74LS670	
Octal D-Type Register, Common Enable and Clear, Three-State	25LS2520		
BUS TRANSCEIVERS/DRIVERS			
Quad Bus Transceiver, Inverting, (100mA)			26S10
Quad Bus Transceiver, Non-Inverting (100mA)			26S11
Quad Bus Transceiver, Inverting	25LS242	54/74LS242	*54/74S242
Quad Bus Transceiver, Non-Inverting	25LS243	54/74LS243	*54/74S243
Quad Open-Collector Bus Transceiver			26S12/12A
Quad Three-State Bus Transceiver (Inverting)			8T26/8T26A
Quad Three-State Bus Transceiver (Non-Inverting)			8T28
Quad Two I/P Transceiver with Three-State Receiver (O.C.)	2905		
Quad Two I/P Transceiver with Parity (O.C.)	2906		
Quad Two I/P Transceiver with Parity (O.C.)	2907		
Quad Two I/P Transceiver with Three-State Receiver (Three-State)	2915A		
Quad Two I/P Transceiver with Parity (Three-State)	2916A		
Quad Two I/P Transceiver with Parity (Three-State)	2917A		
Octal Bus Driver, Inverting	25LS240	54/74LS240	*54/74S240
Octal Bus Driver, Non-Inverting (Complementary G, G inputs)	25LS241	54/74LS241	*54/74S241
Octal Bus Driver, Non-Inverting	25LS244	54/74LS244	*54/74S244
Octal Bidirectional Bus Transceiver	8304		

*Data Sheet on following pages.

Am25LS14

8-Bit Serial/Parallel Two's Complement Multiplier

DISTINCTIVE CHARACTERISTICS

- Two's complement multiplication without correction
- Magnitude only multiplication
- Cascadable for any number of bits
- 8-bit parallel multiplicand data input
- 25MHz minimum clock frequency
- Second sourced by T.I. as the SN54LS/74LS384
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

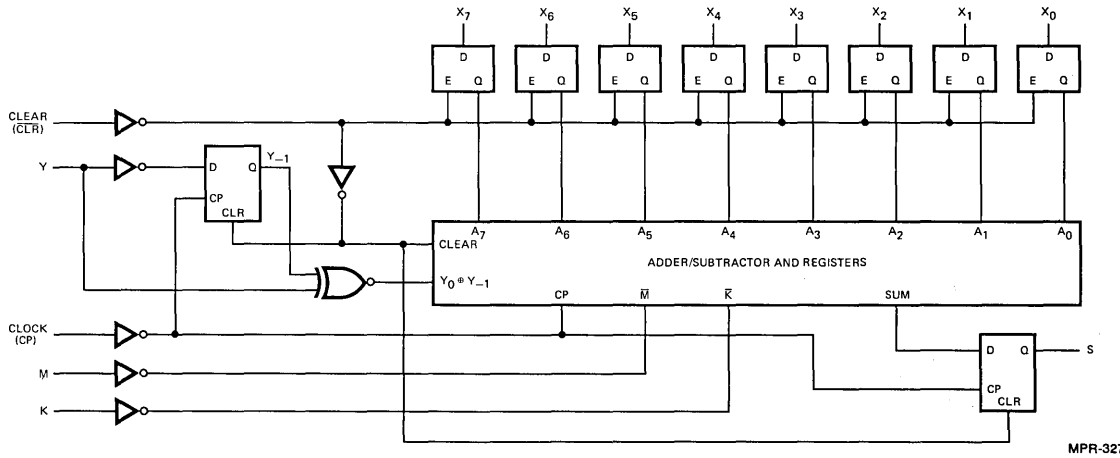
The Am25LS14 is an 8-bit by 1-bit sequential logic element that performs digital multiplication of two numbers represented in two's complement form to produce a two's complement product without correction by using Booth's algorithm internally. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. The X latches are controlled via the clear input. When the clear input is LOW, all internal flip-flops are cleared and the X latches are opened to accept new multiplicand data. When the clear input is HIGH, the latches are closed and are insensitive to X input changes.

The multiplier word data is passed by the Y input in a serial bit stream — least significant bit first. The product is clocked out the S output least significant bit first.

The multiplication of an m-bit multiplicand by an n-bit multiplier results in an m + n bit product. The Am25LS14 must be clocked for m + n clock cycles to produce this two's complement product. Likewise, the n-bit multiplier (Y-input) sign bit data must be extended for the remaining m-bits to complete the multiplication cycle.

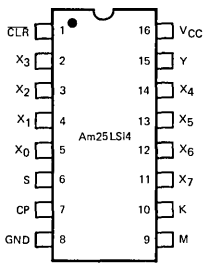
The device also contains a K input so that devices can be cascaded for longer length X words. The sum (S) output of one device is connected to the K input of the succeeding device when cascading. Likewise, a mode input (M) is used to indicate which device contains the most significant bit. The mode input is wired HIGH or LOW depending on the position of the 8-bit slice in the total X word length.

LOGIC DIAGRAM



MPR-327

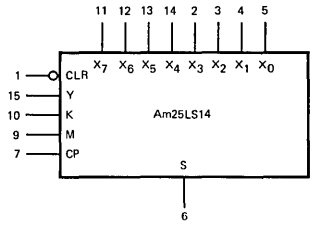
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-328

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

MPR-329

Am25LS15

Quad Serial Adder/Subtractor

DISTINCTIVE CHARACTERISTICS

- Four independent adder/subtractors
- Use with two's complement arithmetic
- Magnitude only addition/subtraction
- Second sourced by T.I. as Am54LS/74LS385
- 100% product assurance screening to MIL-STD-883 requirements

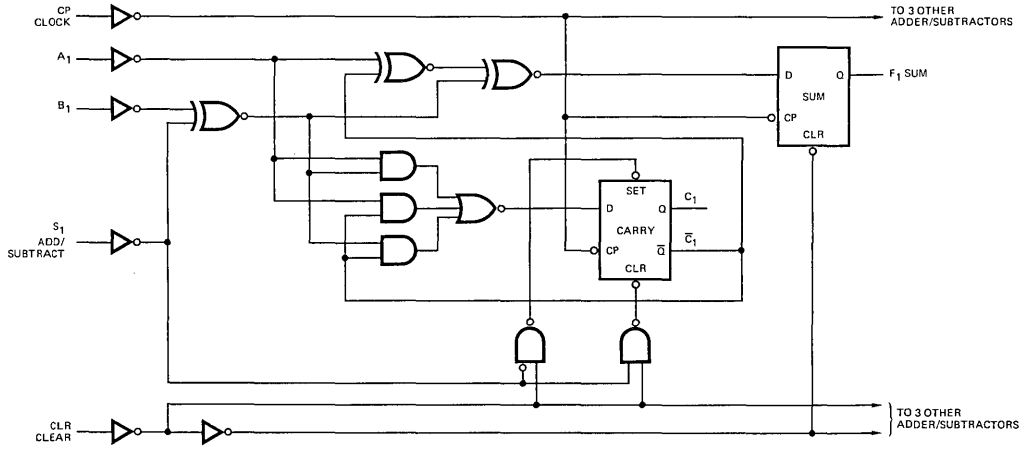
FUNCTIONAL DESCRIPTION

The Am25LS15 is a serial two's complement adder/subtractor designed for use in association with the Am25LS14 serial/parallel two's complement multiplier. This device can also be used for magnitude only or one's complement addition or subtraction.

Four independent adder/subtractors are provided with common clock and clear inputs. The add function is A plus B and the subtract function is A minus B. The clear function sets the internal carry function to logic zero in the add mode and to logic one in subtract mode. This least significant carry is self propagating in the subtract mode as long as zeroes are applied to the A and B inputs at the LSB's. All internal flip-flops change state on the LOW-to-HIGH clock transition.

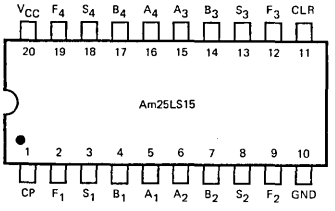
The Am25LS15 is particularly useful for recursive or non-recursive digital filtering or butterfly networks in Fast Fourier Transforms.

LOGIC DIAGRAM
(One of Four Similar Functions)



MPR-330

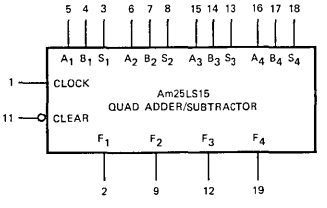
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-331

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

MPR-332

Am25LS22

8-Bit Serial/Parallel Register With Sign Extend

DISTINCTIVE CHARACTERISTICS

- Three-state outputs with multiplexed input
- Multiplexed serial data input
- Sign extend function
- Second sourced by T.I. as Am54LS/74LS322
- 100% product assurance screening to MIL-STD-883 requirements

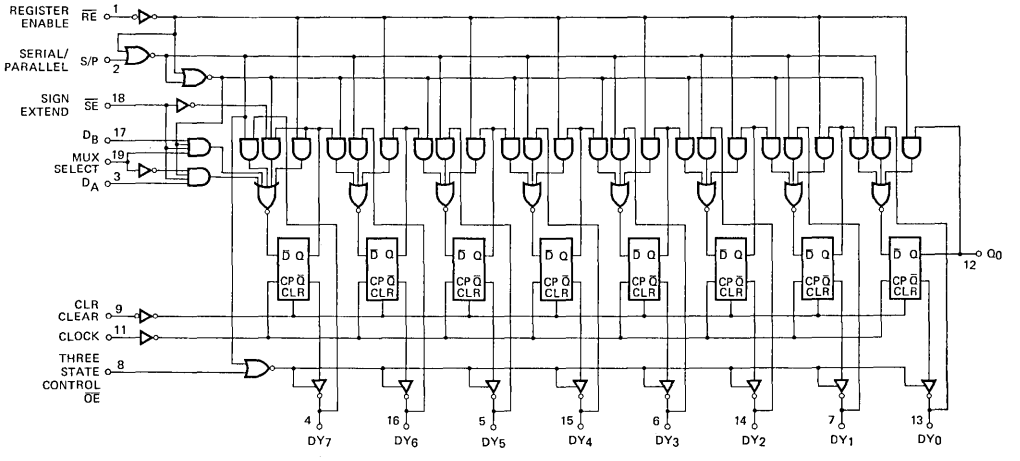
FUNCTIONAL DESCRIPTION

The Am25LS22 is an eight-bit serial/parallel register built using advanced Low-Power Schottky processing. The device features an eight-bit parallel multiplexed input/output port to provide improved bit density in a 20-pin package. Data may also be loaded into the device in a serial manner from either input D_A or D_B. A serial output, Q_0, is also provided.

The Am25LS22 is specifically designed for operation with the Am25LS14 serial/parallel two's complement multiplier and provides the sign extend function required for this device.

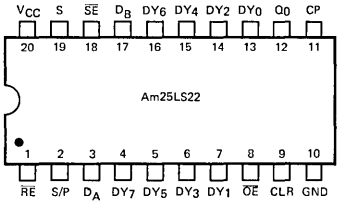
When the Register Enable ($\overline{RE}$) input is HIGH, the register will retain its current contents. Synchronous parallel loading is accomplished by applying a LOW to $\overline{RE}$ and applying a LOW to the Serial/Parallel (S/P) input. This places the three-state outputs in the high-impedance state independent of $\overline{OE}$ and allows data that is applied on the input/output lines (DY_i) to be clocked into the register. When the S/P input is HIGH, the device will shift right. The Sign Extend ($\overline{SE}$) input is used to repeat the sign in the Q_7 flip-flop. This occurs whenever $\overline{SE}$ is LOW when the SHIFT mode is selected. When $\overline{SE}$ is high, the serial two-input multiplexer is enabled. Thus, either D_A or D_B can be selected to load data serially. The register changes state on the LOW-to-HIGH transition of the clock. A clear input (CLR) is used to asynchronously reset all flip-flops when a LOW is applied.

LOGIC DIAGRAM



MPR-333

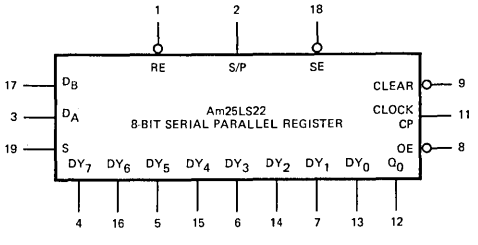
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-334

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

MPR-335

Am25LS2516

Eight-Bit By Eight-Bit Serial/Parallel Multiplier with Accumulator

DISTINCTIVE CHARACTERISTICS

- Two's complement, two-bit lookahead carry-save arithmetic
- Microprogrammable — four-bit instruction code for load, multiply, and read operations
- Cascadable, two devices perform full 16-bit multiplication without additional hardware
- Eight-bit byte parallel, bidirectional, bussed I/O
- On-chip registers and double length accumulator
- Overflow indicator
- Three-state shared bus input/output lines
- High-speed architecture provides clock rates of 20MHz (Typ)
- 100% product assurance screening to MIL-STD-883 requirements

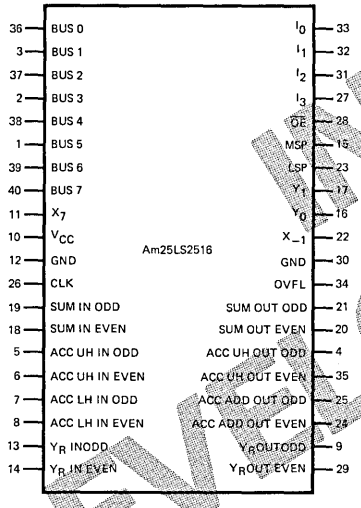
FUNCTIONAL DESCRIPTION

The Am25LS2516 is an eight-bit by eight-bit multiplier and accumulator employing serial/parallel, two's complement, carry-save arithmetic to deliver a 16-bit product in eight clock cycles. The device is fully cascadable for use in high-speed, real-time, digital signal processing applications.

The device includes an eight-bit X Register prior to the X latch providing X hold for chain or overlapping calculations. The X and Y registers are loaded by clocking prior to the beginning of a multiply cycle, the data supplied by the bidirectional bus or the accumulator register. The double length, 16-bit output is multiplexed onto the eight-bit bus; either the upper or lower halves of the result can be read at any one time.

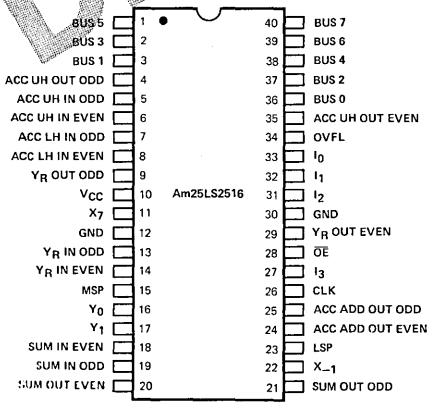
The accumulator and the Y register are both organized as dual-rank shift registers, allowing them to shift two bits at a time. The serial inputs and outputs of the Y register, the low and high order halves of the accumulator and the two-bit serial accumulator adder output, both serially and in parallel, are all available at external pins to provide cascadability.

LOGIC SYMBOL



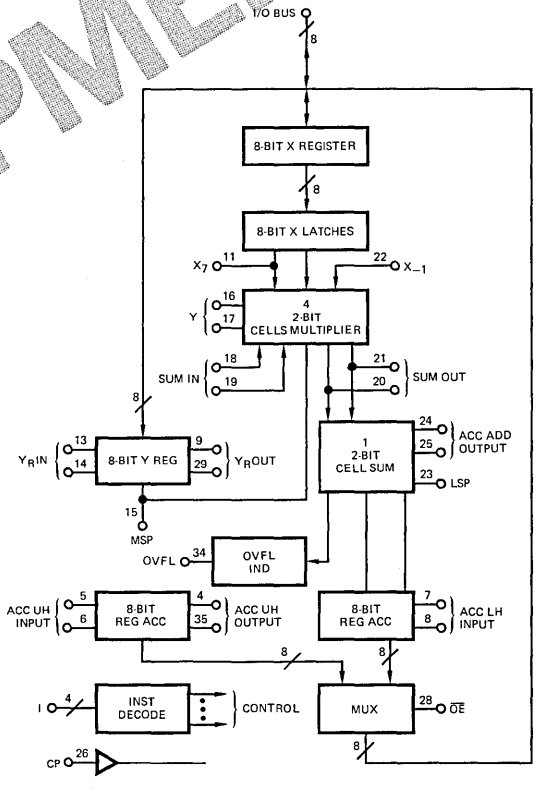
MPR-336

CONNECTION DIAGRAM



MPR-337

LOGIC DIAGRAM



MPR-338

Am25LS2568 • Am25LS2569

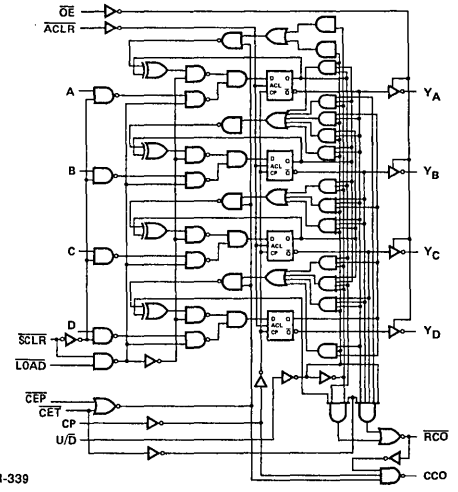
Four-Bit Up/Down Counters With Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- 4-bit synchronous counter, synchronously programmable
- Both synchronous and asynchronous clear inputs
- Three-state counter outputs interface directly with bus organized systems
- Internal look-ahead carry logic and two count enable lines for high speed cascaded operation
- Ripple carry output for cascading
- Clock carry output for convenient modulo configuration
- Fully buffered outputs
- Second sourced as the 54LS/74LS568 and LS569
- Advanced low-power Schottky technology
- 100% product assurance screening to MIL-STD-883 requirements

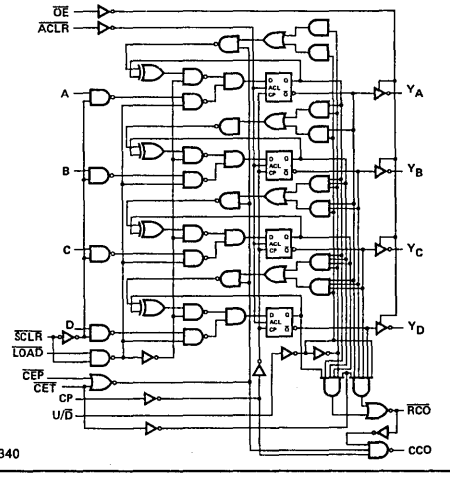
LOGIC DIAGRAMS

Am25LS2568



MPR-339

Am25LS2569



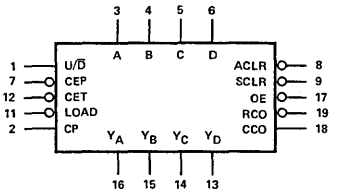
MPR-340

FUNCTIONAL DESCRIPTION

The Am25LS2568 and Am25LS2569 are programmable up/down BCD and Binary counters respectively with three-state outputs for bus organized systems. All functions except output enable ($\overline{OE}$) and asynchronous clear ($\overline{ACLR}$) occur on the positive edge of the clock input (CP).

With the $\overline{LOAD}$ input LOW, the outputs will be programmed by the parallel data inputs (A, B, C, D) on the next clock edge. Counting is enabled only when $\overline{CEP}$ and $\overline{CET}$ are LOW and LOAD is HIGH. The up-down input (U/$\overline{D}$) controls the direction of count, HIGH counts up and LOW counts down. Internal look-ahead carry logic and an active LOW ripple carry output ($\overline{RCO}$) allows for high-speed counting and cascading. During up-count, the $\overline{RCO}$ is LOW at binary 9 for the LS2568 (binary 15 for the LS2569) and upon down-count, it is LOW at binary 0. Normal cascaded operations requires only the $\overline{RCO}$ to be connected to the succeeding block at $\overline{CET}$. When counting, the clocked carry output (CCO) provides a HIGH-LOW-HIGH pulse for a duration equal to the LOW time of the clock pulse and only when $\overline{RCO}$ is LOW. Two active LOW reset lines are available, synchronous clear ($\overline{SCLR}$) and a master reset asynchronous clear ($\overline{ACLR}$). The output control ($\overline{OE}$) input forces the counter output into the high impedance state when HIGH and when LOW, the counter outputs are enabled.

LOGIC SYMBOL

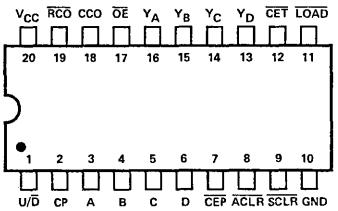


V_{CC} = Pin 20
GND = Pin 10

MPR-341

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

MPR-342

Am25S07•Am25S08

Hex/Quad Parallel D Registers With Register Enable

Distinctive Characteristics

- 4-bit and 6-bit high-speed parallel registers
- Common clock and common enable
- Positive edge triggered D flip-flops
- 100% reliability assurance testing in compliance with MIL-STD-883.

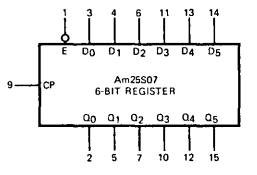
FUNCTIONAL DESCRIPTION

The Am25S07 is a 6-bit, high-speed Schottky register with a buffered common register enable. The Am25S08 is a 4-bit register with a buffered common register enable. The devices are similiar to the Am54S/74S174 and Am54S/74S175 but feature the common register enable rather than common clear.

Both registers will find application in digital systems where information is associated with a logic gating signal. When the enable is LOW, data on the D inputs is stored in the register on the positive going edge of the clock pulse. When the enable is HIGH, the register will not change state regardless of the clock or data input transitions.

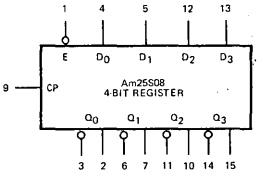
LOGIC SYMBOLS

Am25S07



MPR-343

Am25S08

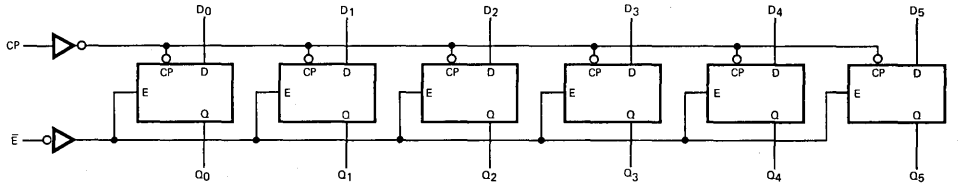


MPR-344

V_{CC} = Pin 16
GND = Pin 8

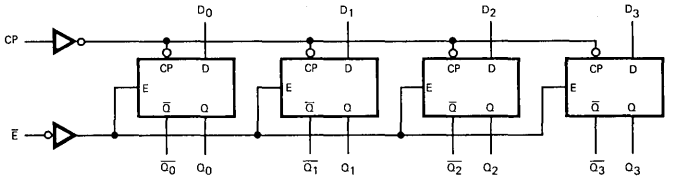
LOGIC DIAGRAMS

Am25S07



MPR-345

Am25S08

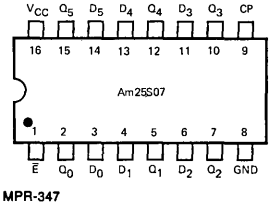


MPR-346

Low-Power Schottky versions of these devices available also. Order Am25LS07 and Am25LS08.

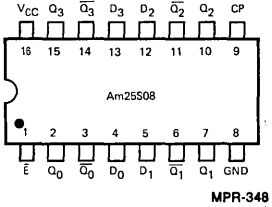
CONNECTION DIAGRAMS
Top Views

Am25S07



MPR-347

Am25S08



MPR-348

Note: Pin 1 is marked for orientation.

Am25S09

Quad Two-Input, High-Speed Register

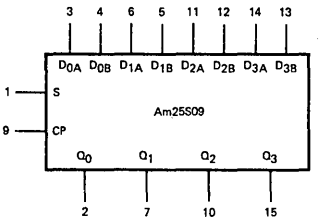
Distinctive Characteristics

- Four-bit register accepts data from one of two 4-bit input fields.
- Edge triggered clock action
- High-speed Schottky technology.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

FUNCTIONAL DESCRIPTION

The Am25S09 is a dual port high-speed, four-bit register using advanced Schottky technology to reduce the effect of transistor storage time. The register consists of four D flip-flops with a buffered common clock, and a two-input multiplexer at the input of each flip-flop. A common select line, S, controls the four multiplexers. Data on the four inputs selected by the S line is stored in the four flip-flops at the clock LOW-to-HIGH transition. When the S input is LOW, the D_{iA} input data will be stored in the register. When the S input is HIGH, the D_{iB} input data will be stored in the register.

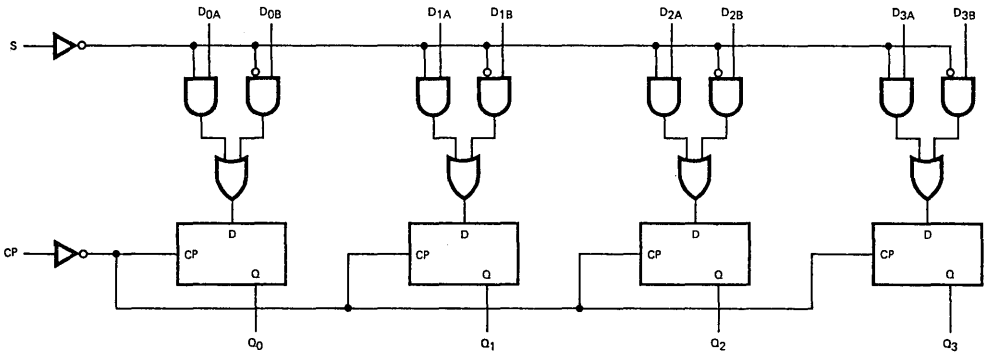
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

MPR-349

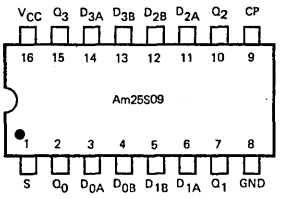
LOGIC DIAGRAM



MPR-350

Low-Power Schottky version of this part available also. Order part number Am25LS09.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

MPR-351

Am25S10

Four-Bit Shifter With Three-State Outputs

Distinctive Characteristics

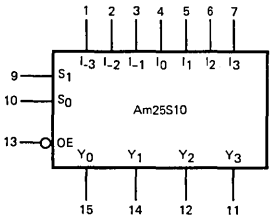
- Shifts 4-bits of data to 0, 1, 2 or 3 places under control of two select lines.
- Three-state outputs for bus organized systems.
- 6.5 ns typical data propagation delay
- Alternate source is 54S/74S350
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am25S10 is a combinatorial logic circuit that accepts a four-bit data word and shifts the word 0, 1, 2 or 3 places. The number of places to be shifted is determined by a two-bit select field S_0 and S_1. An active-LOW enable controls the three-state outputs. This feature allows expansion of shifting over a larger number of places with one delay.

By suitable interconnection, the Am25S10 can be used to shift any number of bits any number of places up or down. Shifting can be logical, with logic zeroes pulled in at either or both ends of the shifting field; arithmetic, where the sign bit is repeated during a shift down; or end around, where the data word forms a continuous loop.

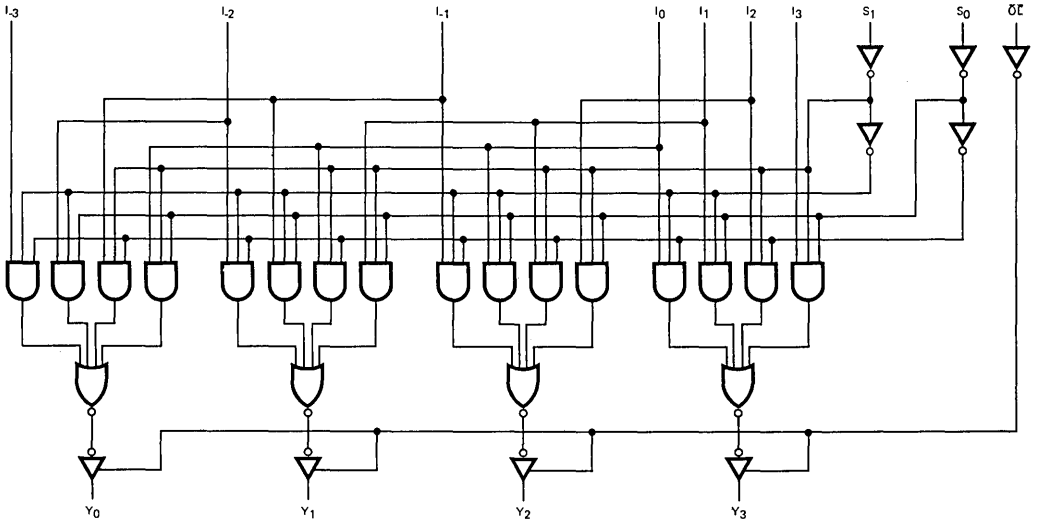
LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

MPR-352

LOGIC DIAGRAM

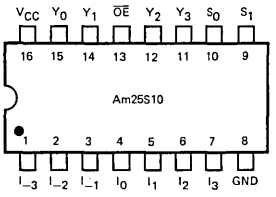


MPR-353

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM25S10PC
Hermetic DIP	0°C to +70°C	AM25S10DC
Dice	0°C to +70°C	AM25S10XC
Hermetic DIP	−55°C to +125°C	AM25S10DM
Hermetic Flat Pak	−55°C to +125°C	AM25S10FM
Dice	−55°C to +125°C	AM25S10XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation

MPR-354

Am54S/74S240 • Am54S/74S241
Am54S/74S242 • Am54S/74S243
Am54S/74S244

Octal Buffers/Line Drivers/Line Receivers With Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Three-state outputs drive bus lines directly
- Advanced Schottky processing
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- V_{OL} of 0.55V at 64mA for Am74S; 48mA for Am54S
- Data-to-output propagation delay times:
  Inverting – 7.0ns MAX
  Non-inverting – 9.0ns MAX
- Enable-to-output – 15.0ns MAX
- 100% reliability assurance testing in compliance with MIL-STD-883
- 20 pin hermetic and molded DIP packages for Am54S/74S240, Am54S/74S241, and Am54S/74S244

FUNCTIONAL DESCRIPTION

These buffers/line drivers, used as memory-address drivers, clock drivers, and bus oriented transmitters/receivers, provide improved PC board density. The outputs of the commercial temperature range versions have 64mA sink and 15mA source capability, which can be used to drive terminated lines down to 133Ω. The outputs of the military temperature range versions have 48mA sink and 12mA source current capability.

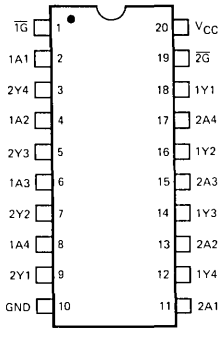
Featuring 0.2V minimum guaranteed hysteresis at each low-current PNP data input, they provide improved noise rejection and high-fan-out outputs to restore Schottky TTL levels completely.

The Am54S/74S240, Am54S/74S241 and Am54S/74S244 have four buffers which are enabled from one common line, and the other four buffers are enabled from another common line. The Am54S/74S240 is inverting, while the Am54S/74S241 and Am54S/74S244 present true data at the outputs.

The Am54S/74S242 and Am54S/74S243 have the two 4-line data paths connected input-to-output on both sides to form an asynchronous transceiver/buffer with complementing enable inputs. The Am54S/74S242 is inverting, while the Am54S/74S243 presents non-inverting data at the outputs.

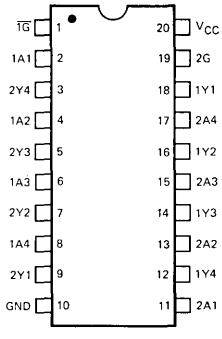
CONNECTION DIAGRAMS
Top Views

Am54S/74S240



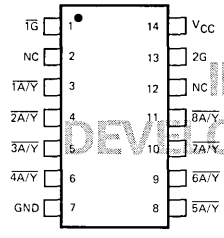
MPR-355

Am54S/74S241



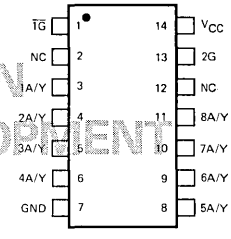
MPR-356

Am54S/74S242



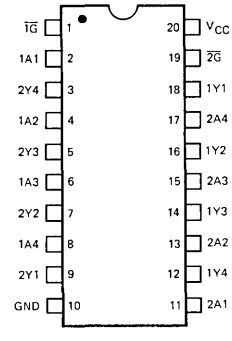
MPR-357

Am54S/74S243



MPR-358

Am54S/74S244



MPR-359

Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number Am54S/74S240	Am54S/74S241	Am54S/74S242	Am54S/74S243	Am54S/74S244
Hermetic	−55°C to +125°C	SN54S240J	SN54S241J	SN54S242J	SN54S243J	SN54S244J
Dice	−55°C to +125°C	AM54S240X	AM54S241X	AM54S242X	AM54S243X	AM54S244X
Hermetic	0°C to +70°C	SN74S240J	SN74S241J	SN74S242J	SN74S243J	SN74S244J
Molded	0°C to +70°C	SN74S240N	SN74S241N			SN74S244N
Dice	0°C to +70°C	AM74S240X	AM74S241X	AM74S242X	AM74S243X	AM74S244X

Low-Power Schottky versions of these parts available also.

Am54S/74S373

Octal Latch With Three-State Outputs

DISTINCTIVE CHARACTERISTICS

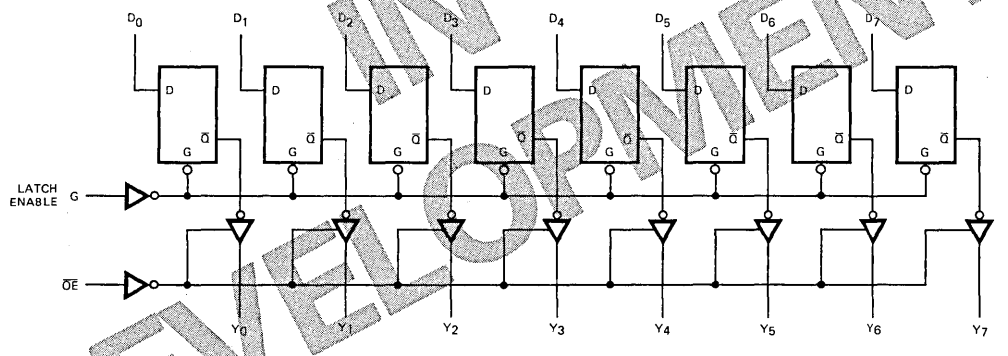
- 8 latches in a single package
- Three-state outputs interface directly with bus organized systems
- Hysteresis on latch enable input for improved noise margin
- High speed – Clock to output 12ns typical
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

The Am54S/74S373 is an octal latch with three-state outputs for bus organized system applications. The latching flip-flops appear to be transparent to the data (data changes asynchronously) when latch enable, G, is HIGH. When G is LOW, the data that meets the set-up times is latched. Data appears on the bus when the output enable, $\overline{OE}$, is LOW. When $\overline{OE}$ is HIGH the bus output is in the high-impedance state.

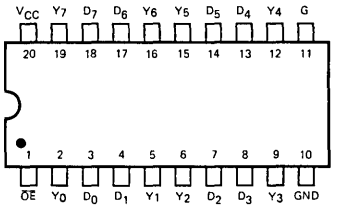
Note: Higher sink current and inverting versions are also in development.

LOGIC DIAGRAM



MPR-360

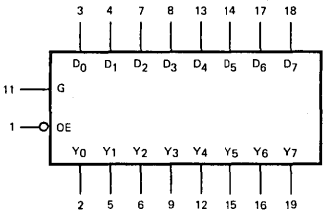
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-361

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

MPR-362

Am54S/74S374

8-Bit Register with Three-State Outputs

DISTINCTIVE CHARACTERISTICS

- Eight-bit, high speed parallel registers
- Positive, edge-triggered, D-type flip-flops
- Buffered common clock and buffered common three-state control
- High speed – Clock to output 11ns typical
- 100% product assurance screening to MIL-STD-883 requirements

FUNCTIONAL DESCRIPTION

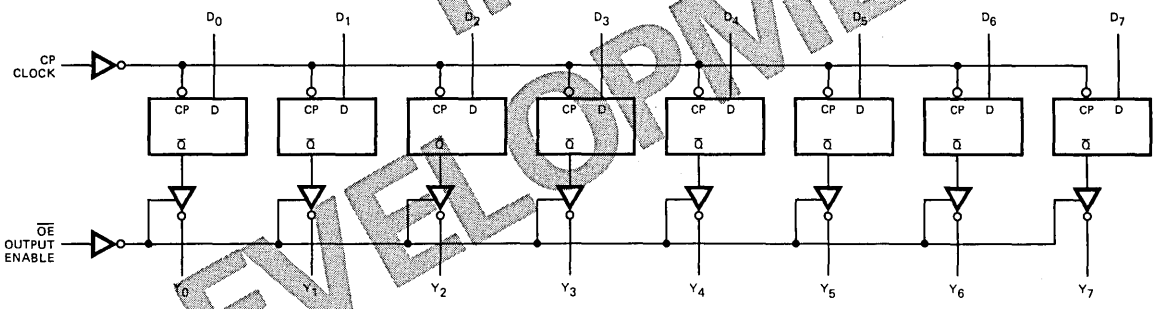
The Am54S/74S374 is an eight-bit register built using high speed Schottky technology. This register consists of eight D-type flip-flops with a buffered common clock and a buffered three-state output control. When the output enable ($\overline{OE}$) input is LOW, the eight outputs are enabled. When the $\overline{OE}$ input is HIGH, the outputs are in the three-state condition.

Input data meeting the set-up and hold time requirements of the D inputs is transferred to the Y outputs on the LOW-to-HIGH transition of the clock input.

The device is packaged in a space-saving (0.3-inch row spacing) 20-pin package.

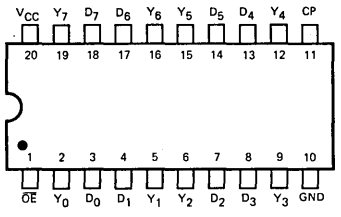
Note: Higher sink current and inverting versions are also in development.

LOGIC DIAGRAM



MPR-363

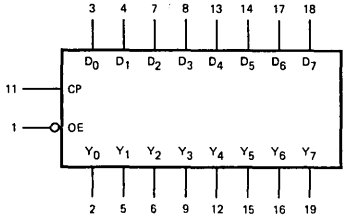
CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MPR-364

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

MPR-365

ADVANCED MOS/LSI

Advanced Micro Devices is an industry leader in the production of high-technology MOS products. The company's n-channel, silicon-gate MOS process is ideally suited for the dense, high-speed memory and microprocessor products required by today's systems.

Although most of the MOS products are oriented toward the Am9080A 8-bit MOS microprocessor, the static RAM's are ideal for use with the Am2900 family. The access times of these devices are often well matched to 2900 system microcycle times and provide significant cost benefits over bipolar memories of the same density.

Of particular interest to users of the Am2900 family are the Am9130 and Am9140 4096-bit RAM's. These devices are organized as 4K x 1 and as 1K x 4 and are available with access times to 200ns.

Complete data on these devices is included in the following pages, along with our 16K dynamic RAM, the Am9016. The selection guide on the next few pages lists other Advanced MOS products which may be of interest. Most of these products are available for full military temperature range operation. For complete data on our MOS products, see our MOS/LSI Data Book.

MOS MEMORY SELECTION GUIDE

STATIC R/W RANDOM-ACCESS MEMORIES

Part Number	Organization	Maximum Access Time (ns)	Temp. Range	Supply Voltage	Outputs	Data I/O Configuration	Package Pins	Operating Power Max. (mW)	Standby Power Max. (mW)
Am9101A	256 × 4	500	C, M	+5	3-State	Separate	22	290	46
Am91L01A	256 × 4	500	C, M	+5	3-State	Separate	22	173	37
Am9101B	256 × 4	400	C, M	+5	3-State	Separate	22	290	46
Am91L01B	256 × 4	400	C, M	+5	3-State	Separate	22	173	37
Am9101C	256 × 4	300	C, M	+5	3-State	Separate	22	315	46
Am91L01C	256 × 4	300	C, M	+5	3-State	Separate	22	189	37
Am9101D	256 × 4	250	C	+5	3-State	Separate	22	315	46
Am9102	1024 × 1	650	C, M	+5	3-State	Separate	16	263	42
Am91L02	1024 × 1	650	C, M	+5	3-State	Separate	16	158	35
Am9102A	1024 × 1	500	C, M	+5	3-State	Separate	16	263	42
Am91L02A	1024 × 1	500	C, M	+5	3-State	Separate	16	158	35
Am9102B	1024 × 1	400	C, M	+5	3-State	Separate	16	263	42
Am91L02B	1024 × 1	400	C, M	+5	3-State	Separate	16	158	35
Am9102C	1024 × 1	300	C, M	+5	3-State	Separate	16	290	42
Am91L02C	1024 × 1	300	C, M	+5	3-State	Separate	16	173	35
Am9102D	1024 × 1	250	C	+5	3-State	Separate	16	290	42
Am9111A	256 × 4	500	C, M	+5	3-State	Bussed	18	290	46
Am91L11A	256 × 4	500	C, M	+5	3-State	Bussed	18	173	37
Am9111B	256 × 4	400	C, M	+5	3-State	Bussed	18	290	46
Am91L11B	256 × 4	400	C, M	+5	3-State	Bussed	18	173	37
Am9111C	256 × 4	300	C, M	+5	3-State	Bussed	18	315	46
Am91L11C	256 × 4	300	C, M	+5	3-State	Bussed	18	189	37
Am9111D	256 × 4	250	C	+5	3-State	Bussed	18	315	46
Am9112A	256 × 4	500	C, M	+5	3-State	Bussed	16	290	46
Am91L12A	256 × 4	500	C, M	+5	3-State	Bussed	16	173	37
Am9112B	256 × 4	400	C, M	+5	3-State	Bussed	16	290	46
Am91L12B	256 × 4	400	C, M	+5	3-State	Bussed	16	173	37
Am9112C	256 × 4	300	C, M	+5	3-State	Bussed	16	315	46
Am91L12C	256 × 4	300	C, M	+5	3-State	Bussed	16	189	37
Am9112D	256 × 4	250	C	+5	3-State	Bussed	16	315	46
Am9114B	1024 x 1	450	C, M	+5	3-State	Bussed	18	500	–
Am9114C	1024 x 1	300	C, M	+5	3-State	Bussed	18	500	–
Am9114E	1024 x 1	200	C	+5	3-State	Bussed	18	500	–
Am9130A	1024 × 4	500	C, M	+5	3-State	Bussed	22	578	84
Am9130B	1024 × 4	400	C, M	+5	3-State	Bussed	22	578	84
Am9130C	1024 × 4	300	C, M	+5	3-State	Bussed	22	578	84
Am9130D	1024 × 4	250	C	+5	3-State	Bussed	22	578	84
Am9130E	1024 × 4	200	C	+5	3-State	Bussed	22	578	84
Am91L30A	1024 × 4	500	C, M	+5	3-State	Bussed	22	367	72
Am91L30B	1024 × 4	400	C, M	+5	3-State	Bussed	22	367	72
Am91L30C	1024 × 4	300	C, M	+5	3-State	Bussed	22	367	72
Am91L30D	1024 × 4	250	C	+5	3-State	Bussed	22	367	72
Am9131A	1024 × 4	500	C, M	+5	3-State	Bussed	22	578	84
Am9131B	1024 × 4	400	C, M	+5	3-State	Bussed	22	578	84
Am9131C	1024 × 4	300	C, M	+5	3-State	Bussed	22	578	84
Am9131D	1024 × 4	250	C	+5	3-State	Bussed	22	578	84
Am9131E	1024 × 4	200	C	+5	3-State	Bussed	22	578	84
Am91L31A	1024 × 4	500	C, M	+5	3-State	Bussed	22	367	72
Am91L31B	1024 × 4	400	C, M	+5	3-State	Bussed	22	367	72
Am91L31C	1024 × 4	300	C, M	+5	3-State	Bussed	22	367	72
Am91L31D	1024 × 4	250	C	+5	3-State	Bussed	22	367	72
Am9140A	4096 × 1	500	C, M	+5	3-State	Separate	22	578	84
Am9140B	4096 × 1	400	C, M	+5	3-State	Separate	22	578	84
Am9140C	4096 × 1	300	C, M	+5	3-State	Separate	22	578	84
Am9140D	4096 × 1	250	C	+5	3-State	Separate	22	578	84
Am9140E	4096 × 1	200	C	+5	3-State	Separate	22	578	84
Am91L40A	4096 × 1	500	C, M	+5	3-State	Separate	22	367	72
Am91L40B	4096 × 1	400	C, M	+5	3-State	Separate	22	367	72
Am91L40C	4096 × 1	300	C, M	+5	3-State	Separate	22	367	72
Am91L40D	4096 × 1	250	C	+5	3-State	Separate	22	367	72
Am9141A	4096 × 1	500	C, M	+5	3-State	Separate	22	578	84
Am9141B	4096 × 1	400	C, M	+5	3-State	Separate	22	578	84
Am9141C	4096 × 1	300	C, M	+5	3-State	Separate	22	578	84
Am9141D	4096 × 1	250	C	+5	3-State	Separate	22	578	84
Am9141E	4096 × 1	200	C	+5	3-State	Separate	22	578	84
Am91L41A	4096 × 1	500	C, M	+5	3-State	Separate	22	367	72
Am91L41B	4096 × 1	400	C, M	+5	3-State	Separate	22	367	72
Am91L41C	4096 × 1	300	C, M	+5	3-State	Separate	22	367	72
Am91L41D	4096 × 1	250	C	+5	3-State	Separate	22	367	72

MOS MEMORY SELECTION GUIDE

DYNAMIC R/W RANDOM-ACCESS MEMORIES

Part Number	Organization	Maximum Access Time (ns)	Temp. Range	Supply Voltages	Operating Power (mW)	Outputs	Data I/O Configuration	Package Pins	Refresh Time (ns)	Standby Power-Max. (mW)
Am9050C	4096 × 1	300	C	−5, +12	750	Open Drain	Bussed	18	2.0	3.0
Am9050D	4096 × 1	250	C	−5, +12	750	Open Drain	Bussed	18	2.0	3.0
Am9050E	4096 × 1	200	C	−5, +12	750	Open Drain	Bussed	18	2.0	3.0
Am9060C	4096 × 1	300	C	±5, +12	750	3-State	Separate	22	2.0	3.0
Am9060D	4096 × 1	250	C	±5, +12	750	3-State	Separate	22	2.0	3.0
Am9060E	4096 × 1	200	C	±5, +12	750	3-State	Separate	22	2.0	3.0
Am9016C	16384 x 1	300	C	±5, +12	480	3-State	Separate	16	2.0	20.0
Am9016D	16384 x 1	250	C	±5, +12	480	3-State	Separate	16	2.0	20.0
Am9016E	16384 x 1	200	C	±5, +12	480	3-State	Separate	16	2.0	20.0

READ-ONLY MEMORIES

Part Number	Organization	Access Time (ns)	Temp. Range	Supply Voltages	Operating Power-Max. (mW)	Outputs
C8316A	2048 × 8	850	C	+5	514	3-State
C8316E	2048 × 8	450	C	+5	499	3-State
Am9208B	1024 × 8	400	C, M	+5, +12	620	3-State
Am9208C	1024 × 8	300	C, M	+5, +12	620	3-State
Am9208D	1024 × 8	250	C	+5, +12	700	3-State
Am9214	512 × 8	500	C, M	+5	263	3-State
Am9216B	2048 × 8	400	C, M	+5, +12	660	3-State
Am9216C	2048 × 8	300	C	+5, +12	700	3-State
Am9217A	2048 × 8	550	C, M	+5	367	3-State
Am9217B	2048 × 8	450	C, M	+5	367	3-State
Am9218B	2048 × 8	450	C, M	+5	367	3-State
Am9218C	2048 × 8	350	C	+5	367	3-State
Am9232	4096 x 8	350	C, M	+5	500	3-State

ERASABLE PROGRAMMABLE READ-ONLY MEMORY

Part Number	Organization	Access Time (nsec)	Temp. Range	Supply Voltages	Operating Power-Max. (mW)	Outputs
Am1702A	256 × 8	1.0μs	C, E	−9V, +5V	676	3-State
Am2708	1024 × 8	450	C	+5V, +12V, −5V	800	3-State

Am9016

16,384 x 1 Dynamic R/W Random Access Memory

DISTINCTIVE CHARACTERISTICS

- High density 16k x 1 organization
- Direct replacement for MK4116
- Worst-case refresh intervals at 70°C — 2ms for Am9016, 4ms for Am90R16
- Low maximum power dissipation — 462mW active, 20mW standby
- High speed operation — 200ns access, 375ns cycle
- ±10% tolerance on standard +12, +5, −5 voltages
- TTL compatible interface signals
- Three-state output
- RAS only, RMW and Page mode clocking options
- 128 cycle refreshing
- Unlatched data output
- Standard 16-pin, .3 inch wide dual in-line package
- Double poly N-channel silicon gate MOS technology
- 100% MIL-STD-883 reliability assurance testing

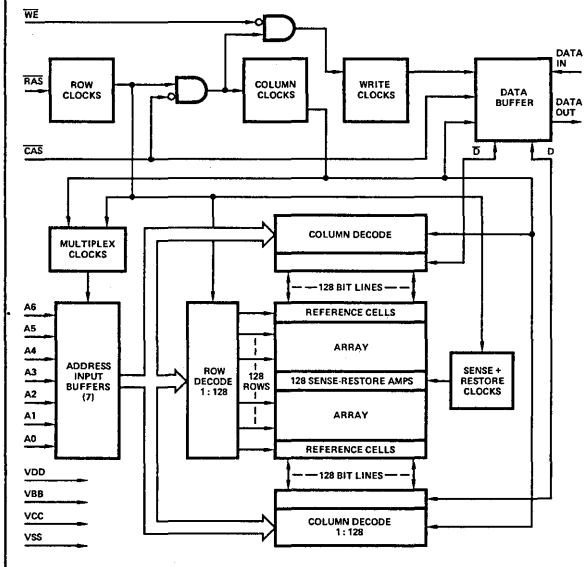
GENERAL DESCRIPTION

The Am9016 is a high speed, 16k-bit, dynamic, read/write random access memory. It is organized as 16,384 words by 1 bit per word and is packaged in a standard 16-pin DIP. The basic memory element is a single transistor cell that stores charge on a small capacitor. This mechanism requires periodic refreshing of the memory cells to maintain stored information.

All input signals, including the two clocks, are TTL compatible. The Row Address Strobe ($\overline{RAS}$) loads the row address and the Column Address Strobe ($\overline{CAS}$) loads the column address. The row and column address signals share 7 input lines. Active cycles are initiated when $\overline{RAS}$ goes low, and standby mode is entered when $\overline{RAS}$ goes high. In addition to normal read and write cycles, other types of operations are available to improve versatility, performance, and power dissipation.

The three-state output buffer turns on when the column access time has elapsed and turns off after $\overline{CAS}$ goes high. Input and output data are the same polarity.

BLOCK DIAGRAM



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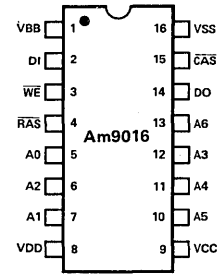
CONNECTION DIAGRAM



Top View

Pin 1 is marked for orientation.

A0 – A6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
DI	DATA IN
DO	DATA OUT
$\overline{RAS}$	ROW ADDRESS STROBE
VDD	POWER (+12V)
VCC	POWER (+5V)
VSS	GROUND
VBB	POWER (−5V)
$\overline{WE}$	WRITE ENABLE

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ORDERING INFORMATION

Ambient Temperature	Package Type	Refresh Interval	Access Time		
			300ns	250ns	200ns
$0°C \leq T_A \leq +70°C$	Hermetic DIP	2msec	AM9016CDC	AM9016DDC	AM9016EDC
		4msec	AM90R16CDC	AM90R16DDC	AM90R16EDC

MAXIMUM RATINGS above which useful life may be impaired

Storage Temperature	−55°C to +150°
Ambient Temperature under Bias	0°C to +70°
Input Signal Voltages with Respect to VBB	−0.5V to +20
VDD and VCC Supply Voltages with Respect to VBB	−0.5V to +20
Power Dissipation	1.0
Short Circuit Output Current	50m

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulation o static charge. It is suggested nevertheless, that conventional precautions be observed during storage, handling, and use in order to avoi exposure to excessive voltages.

OPERATING RANGE

Ambient Temperature	VDD	VCC	VSS	VBB
$0°C \leq T_A \leq +70°C$	+12V ±10%	+5V ±10%	0	−5.0V ±10%

ELECTRICAL CHARACTERISTICS over operating range (Notes 1, 11)

Parameters	Description		Test Conditions		Am9016X Am90R16X Min.	Typ.	Max.	Units
VOH	Output HIGH Voltage		IOH = −5.0mA		2.4		VCC	Volts
VOL	Output LOW Voltage		IOL = 4.2mA		VSS		0.40	Volts
VIH	Input HIGH Voltage for Address, Data In				2.4		7.0	Volts
VIHC	Input HIGH Voltage for $\overline{CAS}$, $\overline{RAS}$, $\overline{WE}$				2.7		7.0	Volts
VIL	Input LOW Voltage				−1.0		0.80	Volts
IIX	Input Load Current		VSS ≤ VI ≤ VCC		−10		10	µA
IOZ	Output Leakage Current		VSS ≤ VO ≤ VCC, Output OFF		−10		10	µA
ICC	VCC Supply Current		Output OFF (Note 4)		−10		10	µA
IBB	VBB Supply Current, Average		Standby, $\overline{RAS} \geq$ VIHC				100	µA
			Operating, Minimum Cycle Time				200	
IDD	VDD Supply Current, Average	Operating	$\overline{RAS}$ Cycling, $\overline{CAS}$ Cycling, Minimum Cycle Times	Am9016C			35	mA
				Am9016D			35	
				Am9016E			35	
		Page Mode	$\overline{RAS} \leq$ VIL, $\overline{CAS}$ Cycling, Minimum Cycle Times	Am9016C			27	
				Am9016D			27	
				Am9016E			27	
		$\overline{RAS}$ – Only Refresh	$\overline{RAS}$ Cycling, $\overline{CAS} \geq$ VIHC, Minimum Cycle Times	Am9016C			27	
				Am9016D			27	
				Am9016E			27	
		Standby	$\overline{RAS} \geq$ VIHC				1.5	
CI	Input Capacitance	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Inputs at 0V, f = 1MHz, Nominal Supply Voltages				10	pF
		Address, Data In					5.0	
CO	Output Capacitance		Output OFF				7.0	

SWITCHING CHARACTERISTICS over operating range (Notes 2, 3, 5, 10)

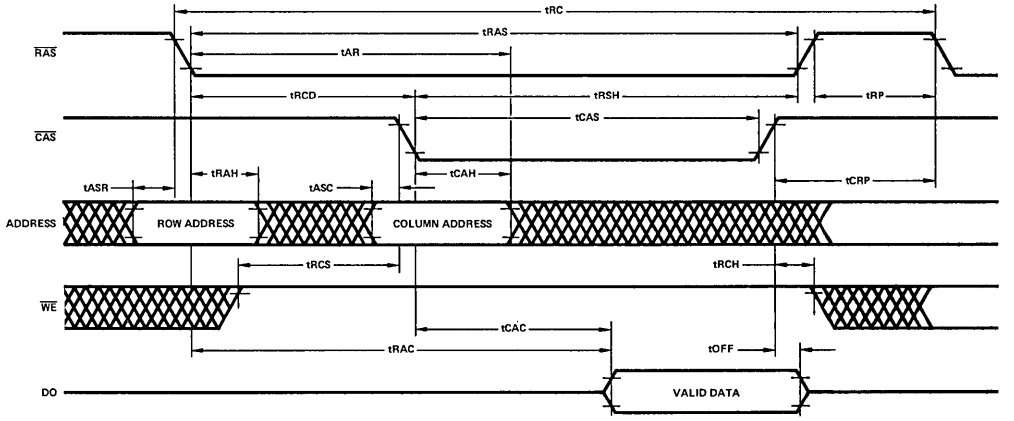
Parameters	Description		Renamed Parameter	Am9016C Min.	Am9016C Max.	Am9016D Min.	Am9016D Max.	Am9016E Min.	Am9016E Max.	Units
tAR	$\overline{RAS}$ LOW to Column Address Hold Time		TRELAX (C)	200		160		120		ns
tASC	Column Address Set-up Time		TAVCEL	−10		−10		−10		ns
tASR	Row Address Set-up Time		TAVREL	0		0		0		ns
tCAC	Access Time from $\overline{CAS}$ (Note 6)		TCELQV		185		165		135	ns
tCAH	$\overline{CAS}$ LOW to Column Address Hold Time		TCELAX	85		75		55		ns
tCAS	$\overline{CAS}$ Pulse Width		TCELCEH	185	10,000	165	10,000	135	10,000	ns
tCP	Page Mode $\overline{CAS}$ Precharge Time		TCEHCEL	100		100		80		ns
tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		TCEHREL	−20		−20		−20		ns
tCWD	$\overline{CAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9)		TCELWL	145		125		95		ns
tCWL	$\overline{WE}$ LOW to $\overline{CAS}$ HIGH Set-up Time		TWLCEH	100		100		80		ns
tDH	$\overline{CAS}$ LOW or $\overline{WE}$ LOW to Data In Valid Hold Time (Note 7)		TCELDX or TWLDX	85		75		55		ns
tDHR	$\overline{RAS}$ LOW to Data In Valid Hold Time		TRELDX	200		160		120		ns
tDS	Data In Stable to $\overline{CAS}$ LOW or $\overline{WE}$ LOW Set-up Time (Note 7)		TDVCEL or TDVWL	0		0		0		ns
tOFF	$\overline{CAS}$ HIGH to Output OFF Delay		TCEHQZ	0	60	0	60	0	50	ns
tPC	Page Mode Cycle Time		TCELCEL (P)	295		275		225		ns
tRAC	Access Time from $\overline{RAS}$ (Note 6)		TRELQV		300		250		200	ns
tRAH	$\overline{RAS}$ LOW to Row Address Hold Time		TRELAX (R)	45		35		25		ns
tRAS	$\overline{RAS}$ Pulse Width		TRELREH	300	10,000	250	10,000	200	10,000	ns
tRC	Random Read or Write Cycle Time		TRELREL	460		410		375		ns
tRCD	$\overline{RAS}$ LOW to $\overline{CAS}$ LOW Delay (Note 6)		TRELCEL	35	115	35	85	25	65	ns
tRCH	Read Hold Time		TCEHWX	0		0		0		ns
tRCS	Read Set-up Time		TWHCEL	0		0		0		ns
tREF	Refresh Interval	Am90R16			4		4		4	ms
		Am9016			2		2		2	
tRP	$\overline{RAS}$ Precharge Time		TREHREL	150		150		120		ns
tRSH	$\overline{CAS}$ LOW to $\overline{RAS}$ HIGH Delay		TCELREH	185		165		135		ns
tRWC	Read/Write Cycle Time		TRELREL (R/W)	525		515		375		ns
tRWD	$\overline{RAS}$ LOW to $\overline{WE}$ LOW Delay (Note 9)		TRELWL	260		210		160		ns
tRWL	$\overline{WE}$ LOW to $\overline{RAS}$ HIGH Set-up Time		TWLREH	100		100		80		ns
tT	Transition Time			3	50	3	50	3	50	ns
tWCH	Write Hold Time		TCELWH	85		75		55		ns
tWCR	$\overline{RAS}$ LOW to Write Hold Time		TRELWH	200		160		120		ns
tWCS	$\overline{WE}$ LOW to $\overline{CAS}$ LOW Set-up Time (Note 9)		TWLCEL	−20		−20		−20		ns
tWP	Write Pulse Width		TWLWH	85		75		55		ns

NOTES

1. Typical values are for $T_A = 25°C$, nominal supply voltages and nominal processing parameters.
2. Signal transition times are assumed to be 5ns. Transition times are measured between specified high and low logic levels.
3. Timing reference levels for both input and output signals are the specified worst-case logic levels.
4. VCC is used in the output buffer only. ICC will therefore depend only on leakage current and output loading. When the output is ON and at a logic high level, VCC is connected to the Data Out pin through an equivalent resistance of approximately 135Ω. In standby mode VCC may be reduced to zero without affecting stored data or refresh operations.
5. Output loading is two standard TTL loads plus 100pF capacitance.
6. Both $\overline{RAS}$ and $\overline{CAS}$ must be low to read data. Access timing will depend on the relative positions of their falling edges. When tRCD is less than the maximum value shown, access time depends on $\overline{RAS}$ and tRAC governs. When tRCD is more than the maximum value shown access time depends on $\overline{CAS}$ and tCAC governs. The maximum value listed for tRCD is shown for reference purposes only and does not restrict operation of the part.
7. Timing reference points for data input setup and hold times will depend on what type of write cycle is being performed and will be the later falling edge of $\overline{CAS}$ or $\overline{WE}$.
8. At least two initialization cycles that exercise both $\overline{RAS}$ and $\overline{CAS}$ should be performed after power-up and before valid operations are begun.
9. The tWCS, tRWD and tCWD parameters are shown for reference purposes only and do not restrict the operating flexibility of the part. When the falling edge of $\overline{WE}$ follows the falling edge of $\overline{CAS}$ by at most tWCS, the data output buffer will remain off for the whole cycle and an "early write" cycle is defined. When the falling edge of $\overline{WE}$ follows the falling edges of $\overline{RAS}$ and $\overline{CAS}$ by at least tRWD and tCWD respectively, the Data Out from the addressed cell will be valid at the access time and a "read/write" cycle is defined. The falling edge of $\overline{WE}$ may also occur at intermediate positions, but the condition and validity of the Data Out signal will not be known.
10. Switching characteristics are listed in alphabetical order.
11. All voltages referenced to VSS.

SWITCHING WAVEFORMS

READ CYCLE



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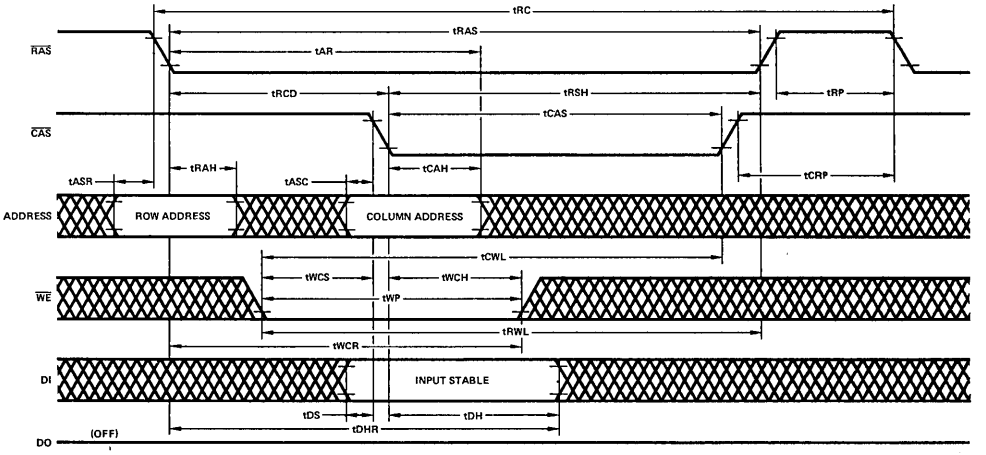
WRITE CYCLE (EARLY WRITE)



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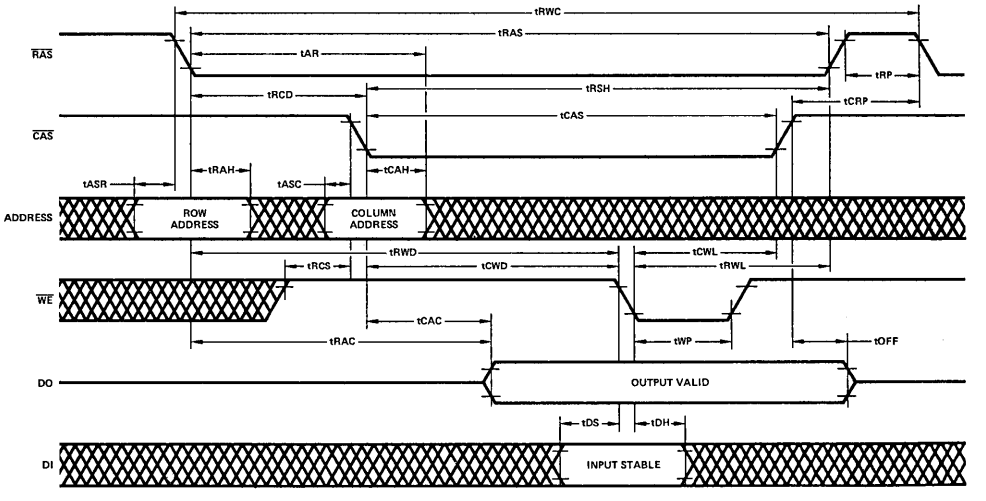
READ-WRITE/READ-MODIFY-WRITE CYCLE



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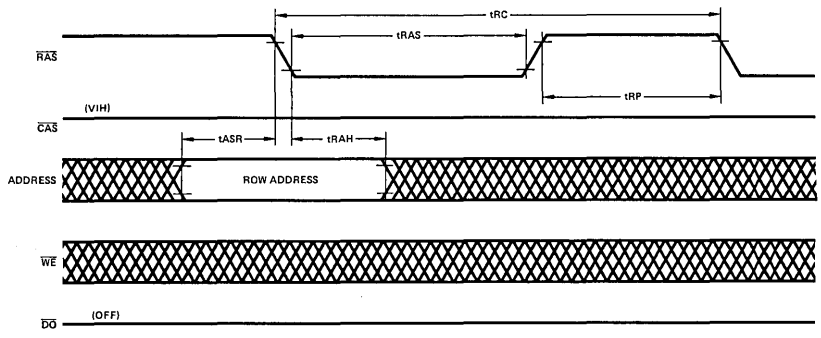
SWITCHING WAVEFORMS (Cont.)

$\overline{RAS}$ ONLY REFRESH CYCLE



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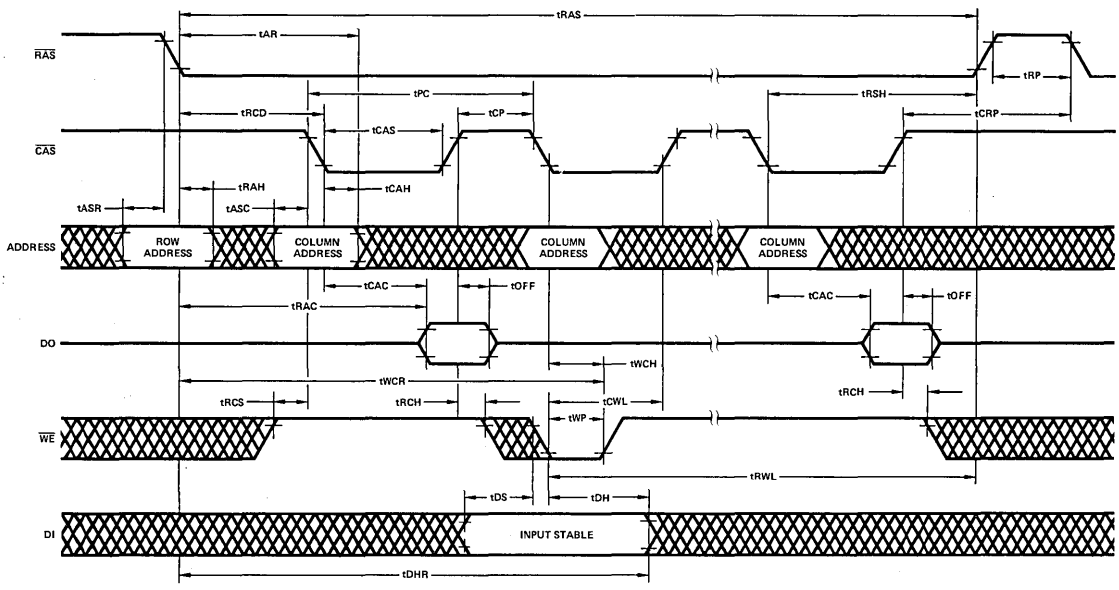
PAGE MODE CYCLE



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APPLICATION INFORMATION

The Am9016 electrical connections are such that if power is applied with the device installed upside down it will be permanently damaged. Precautions should be taken to avoid this mishap.

OPERATING CYCLES

Random read operations from any location hold the $\overline{WE}$ line high and follow this sequence of events:

1) The row address is applied to the address inputs and $\overline{RAS}$ is switched low.
2) After the row address hold time has elapsed, the column address is applied to the address inputs and $\overline{CAS}$ is switched low.
3) Following the access time, the output will turn on and valid read data will be present. The data will remain valid as long as $\overline{CAS}$ is low.
4) $\overline{CAS}$ and $\overline{RAS}$ are then switched high to end the operation. A new cycle cannot begin until the precharge period has elapsed.

Random write operations follow the same sequence of events, except that the $\overline{WE}$ line is low for some portion of the cycle. If the data to be written is available early in the cycle, it will usually be convenient to simply have $\overline{WE}$ low for the whole write operation.

Sequential Read and Write operations at the same location can be designed to save time because re-addressing is not necessary. A read/write cycle holds $\overline{WE}$ high until a valid read is established and then strobes new data in with the falling edge of $\overline{WE}$.

After the power is first applied to the device, the internal circuit requires execution of at least two initialization cycles which exercise both $\overline{RAS}$ and $\overline{CAS}$ before valid memory accesses are begun.

The Am9016 draws most of its power as transients that occur as a result of address strobe switching. Thus, power dissipation for a given part will be a function of strobe duty cycles. The Am9016E may be operated at a maximum cycle rate of 375ns in an ambient environment of +70°C. Memory read or memory write cycles may also be reduced from 375ns to as low as 330ns when the ambient temperature is maintained at +70°C. Figure 1 shows cycle time versus ambient temperature relationship.

Maximum Ambient Temperature Versus Cycle Rate

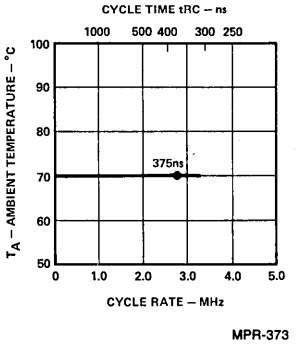


Figure 1.

ADDRESSING

14 address bits are required to select one location out of the 16,384 cells in the memory. Two groups of 7 bits each are multiplexed onto the 7 address lines and latched into the internal address registers. Two negative-going external clocks are used to control the multiplexing. The Row Address Strobe ($\overline{RAS}$) enters the row address bits and the Column Address Strobe ($\overline{CAS}$) enters the column address bits.

When $\overline{RAS}$ is inactive, the memory enters its low power standby mode. Once the row address has been latched, it need not be changed for successive operations within the same row, allowing high-speed page-mode operations.

Page-mode operations first establish the row address and then maintain $\overline{RAS}$ low while $\overline{CAS}$ is repetitively cycled and designated operations are performed. Any column address within the selected row may be accessed in any sequence. The maximum time that $\overline{RAS}$ can remain low is the factor limiting the number of page-mode operations that can be performed.

Multiplexed addressing does not introduce extra delays in the access path. By inserting the row address first and the column address second, the memory takes advantage of the fact that the delay path through the memory is shorter for column addresses. The column address does not propagate through the cell matrix as the row address does and it can therefore arrive somewhat later than the row address without impacting the access time.

REFRESH

The Am9016 is a dynamic memory and each cell must be refreshed at least once every refresh interval in order to maintain the cell contents. Any operation that accesses a row serves to refresh all 128 cells in the row. Thus the refresh requirement is met by accessing all 128 rows at least once every refresh interval. This may be accomplished, in some applications, in the course of performing normal operations. Alternatively, special refresh operations may be initiated. These special operations could be simply additional conventional accesses or they could be "$\overline{RAS}$-only" cycles. Since only the rows need to be addressed, $\overline{CAS}$ may be held high while $\overline{RAS}$ is cycled and the appropriate row addresses are input. Power required for refreshing is minimized and simplified control circuitry will often be possible.

DATA INPUT/OUTPUT

Data is written into a selected cell by the combination of $\overline{WE}$ and $\overline{CAS}$ while $\overline{RAS}$ is low. The later negative transition of $\overline{WE}$ or $\overline{CAS}$ strobes the data into the internal register. In a write cycle, if the $\overline{WE}$ input is brought low prior to $\overline{CAS}$, the data is strobed by $\overline{CAS}$, and the set-up and hold times are referenced to $\overline{CAS}$. If the cycle is a read/write cycle then the data set-up and hold times are referenced to the negative edge of $\overline{WE}$.

In the read cycle the data is read by maintaining $\overline{WE}$ in the high state throughout the portion of the memory cycle in which $\overline{CAS}$ is low. The selected valid data will appear at the output within the specified access time.

DATA OUTPUT CONTROL

Any time $\overline{CAS}$ is high the data output will be off. The output contains either one or zero during read cycle after the access time has elapsed. Data remains valid from the access time until $\overline{CAS}$ is returned to the high state. The output data is the same polarity as the input data.

APPLICATION INFORMATION (Cont.)

The user can control the output state during write operations by controlling the placement of the $\overline{WE}$ signal. In the "early write" cycle (see note 9) the output is at a high impedance state throughout the entire cycle.

POWER CONSIDERATIONS

$\overline{RAS}$ and/or $\overline{CAS}$ can be decoded and used as a chip select signal for the Am9016 but overall system power is minimized if $\overline{RAS}$ is used for this purpose. The devices which do not receive $\overline{RAS}$ will be in low power standby mode regardless of the state of $\overline{CAS}$.

Figure 2 shows the change in IDD supply current as a function of operating cycle rate.

At all times the Absolute Maximum Rating Conditions must be observed. During power supply sequencing VBB should never be more positive than VSS when power is applied to VDD.

Maximum IDD Versus Cycle Rate

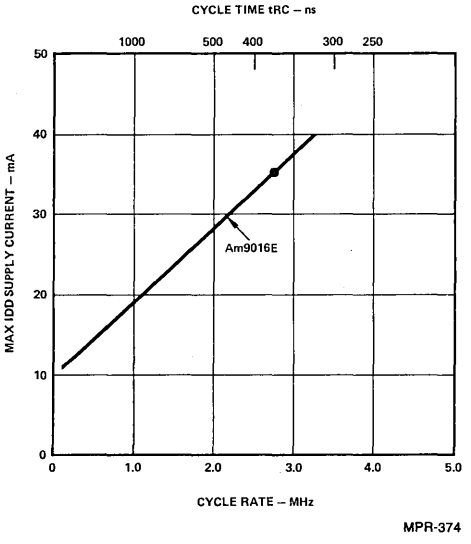
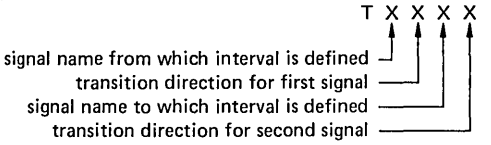


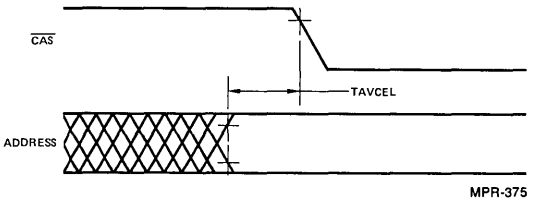
Figure 2.

PARAMETER ABBREVIATIONS

The Switching Characteristics table includes an extra column of parameter abbreviations. They illustrate a new type of specification nomenclature designed to help clarify signal symbols and make data sheet information more consistent.

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors that specify two signal points arranged in a 'from-to' sequence that define a timing interval. The descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:



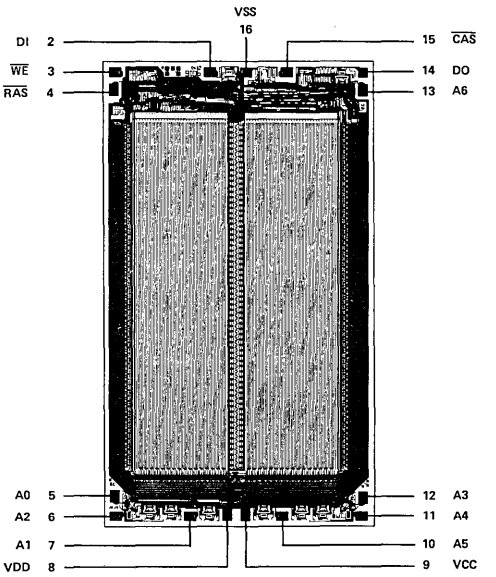


The drawing shows a column address setup time defined as TAVCEL, Address Valid to Column Enable Low time.

The signal definitions used in this data sheet are:
A = Address
D = Data In
Q = Data Out
W = Write Enable
RE = Row Address Strobe
CE = Column Address Strobe

The transition definitions used in this data sheet are:
H = transition to high
L = transition to low
V = transition to valid
X = transition to invalid or don't care
Z = transition to off (high impedance)

Metallization and Pad Layout



DIE SIZE 0.136" X 0.233"

Am9130 • Am91L30

1024 x 4 Static R/W Random Access Memories

DISTINCTIVE CHARACTERISTICS

- 1k X 4 organization
- Fully static data storage — no refreshing
- Single +5V power supply
- High-speed — access times down to 200ns max.
- Low operating power
  - 578mW max., 9130
  - 368mW max., 91L30
- Interface logic levels identical to TTL
- High noise immunity — 400mV worst-case
- High output drive — two standard TTL loads
- DC power-down mode — reduces power by >80%
- Single phase, low voltage, low capacitance clock
- Static clock may be stopped in either state
- Data register on-chip
- Address register on-chip
- Steady power drain — no large surges
- Unique Memory Status signal
  - improves performance
  - self clocking operation
- Full MIL temperature range available
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

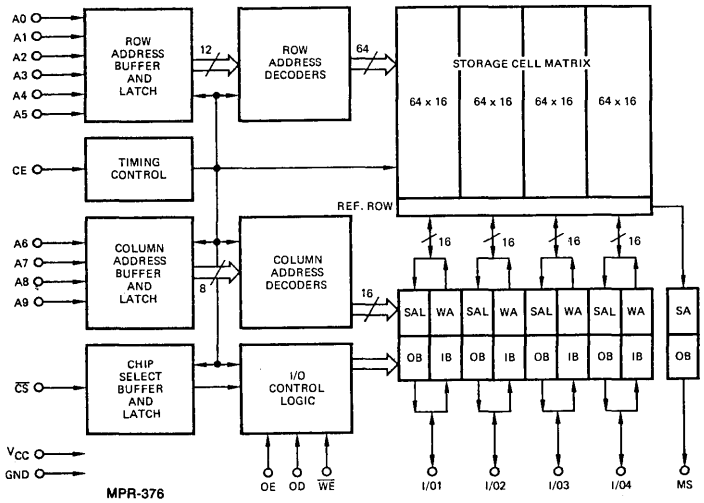
The Am9130 and Am91L30 products are high performance, adaptive, low-power, 4k-bit, static, read/write random access memories. They are implemented as 1024 words by 4 bits per word. Only a single +5V power supply is required for normal operation. A DC power-down mode reduces power while retaining data with a supply voltage as low as 1.5V.

All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive two full TTL loads or more than eight low-power Schottky loads.

Operational cycles are initiated when the Chip Enable clock goes HIGH. When the read or write is complete, Chip Enable goes LOW to preset the memory for the next cycle. Address and Chip Select signals are latched on-chip to simplify system timing. Output data is also latched and is available until the next operating cycle. The $\overline{WE}$ signal is HIGH for all read operations and is LOW during the Chip Enable time to perform a write. Data In and Data Out signals share common I/O pins.

Memory Status is an output signal that indicates when data is actually valid and when the preset interval is complete. It can be used to generate the CE input and to improve the memory performance.

BLOCK DIAGRAM



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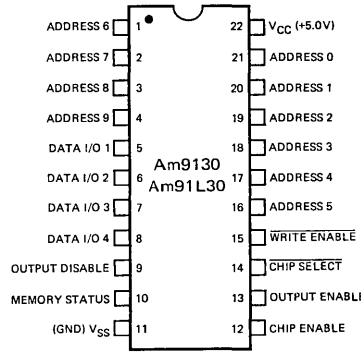
CONNECTION DIAGRAM



Top View

Pin 1 is marked for orientation.

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ORDERING INFORMATION

Package Type	Ambient Temperature	Power Type	Access Time				
			500ns	400ns	300ns	250ns	200ns
Hermetic DIP	$0°C \leq T_A \leq +70°C$	STD	Am9130ADC	Am9130BDC	Am9130CDC	Am9130DDC	Am9130EDC
		LOW	Am91L30ADC	Am91L30BDC	Am91L30CDC	Am91L30DDC	
	$-55°C \leq T_A \leq +125°C$	STD	Am9130ADM	Am9130BDM	Am9130CDM		
		LOW	Am91L30ADM	Am91L30BDM	Am91L30CDM		

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} with Respect to V_{SS}	−0.5V to +7.0V
All Signal Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	1.25W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE		POWER-DOWN RANGE			
V_{CC}	V_{SS}	V_{CC}	V_{SS}	Ambient Temperature	Part Number
$4.75V \leq V_{CC} \leq 5.25V$	0V	$1.5V \leq V_{CC} \leq 5.25V$	0V	$0°C \leq T_A \leq +70°C$	AM91X30XDC
$4.50V \leq V_{CC} \leq 5.50V$	0V	$1.5V \leq V_{CC} \leq 5.50V$	0V	$-55°C \leq T_A \leq +125°C$	AM91X30XDM

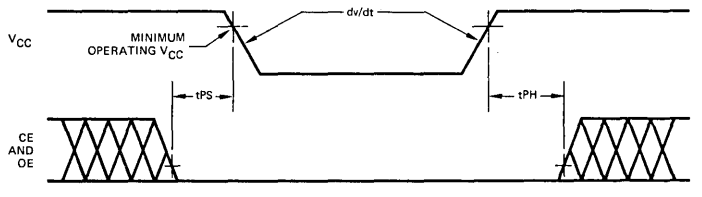
ELECTRICAL CHARACTERISTICS over operating range (Note 1)

Parameters	Description	Test Conditions		Am9130 Min.	Am9130 Typ.	Am9130 Max.	Am91L30 Min.	Am91L30 Typ.	Am91L30 Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -200\mu A$	$V_{CC} = 4.75V$	2.4			2.4			Volts
			$V_{CC} = 4.5V$	2.2			2.2			
V_{OL}	Output LOW Voltage	$I_{OL} = 3.2mA$				0.4			0.4	Volts
V_{IH}	Input HIGH Voltage			2.0		V_{CC}	2.0		V_{CC}	Volts
V_{IL}	Input LOW Voltage			−0.5		0.8	−0.5		0.8	Volts
I_{LI}	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{CC}$				10			10	μA
I_{LO}	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{CC}$, Output disabled				10			10	μA
I_{CC}	V_{CC} Supply Current	Max. V_{CC}, Output disabled	$T_A = 25°C$		50	100		40	65	mA
			$T_A = 0°C$			110			70	
			$T_A = -55°C$			125			80	
C_{IA}	Input Capacitance (Address)	Test frequency = 1MHz, $T_A = 25°C$, All pins at 0V			3.0	6.0		3.0	6.0	pF
C_{OUT}	Output Capacitance				4.0	7.0		4.0	7.0	pF
C_{IC}	Input Capacitance (Control)				6.0	9.0		6.0	9.0	pF
$C_{I/O}$	I/O Capacitance				6.0	9.0		6.0	9.0	pF

POWER DOWN CHARACTERISTICS

Parameter	Description	Test Conditions		Am9130 Min.	Am9130 Typ.	Am9130 Max.	Am91L30 Min.	Am91L30 Typ.	Am91L30 Max.	Unit
dv/dt	V_{CC} Rate of Change					3.0			3.0	V/μs
tPS	Power Down Set-Up Time			tEL			tEL			ns
tPH	Power Up Hold Time			tEL			tEL			ns
I_{PD}	I_{CC} in Standby (Note 2)	$V_{CC} = 2.0V$	$T_A = 25°C$		36	72		28	55	mA
			$T_A = 0°C$			78			60	mA
			$T_A = -55°$			89			68	mA
		$V_{CC} = 1.5V$	$T_A = 25°C$		20	52		16	45	mA
			$T_A = 0°C$			56			48	mA
			$T_A = -55°C$			64			55	mA

POWER DOWN WAVEFORM



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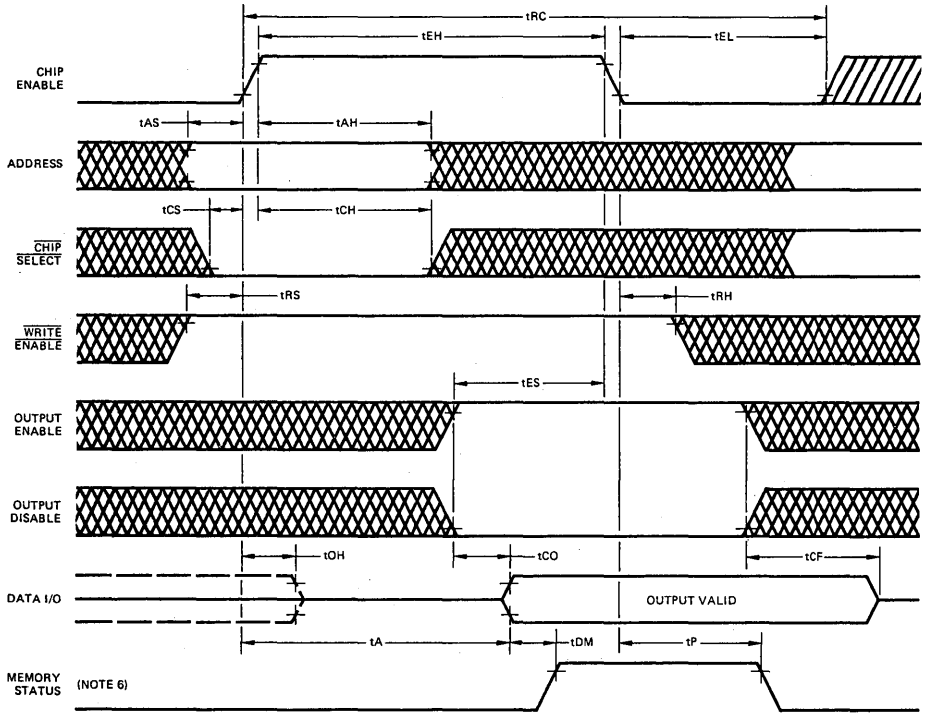
SWITCHING CHARACTERISTICS over operating range

READ CYCLE (Notes 7, 8, 9)

Parameter	Description	Am9130A Am91L30A Min.	Max.	Am9130B Am91L30B Min.	Max.	Am9130C Am91L30C Min.	Max.	Am9130D Am91L30D Min.	Max.	Am9130E Min.	Max.	Unit
tRC	Read Cycle Time (Note 5)	770		620		470		395		320		ns
tA	Access Time (Note 3) (CE to Output Valid Delay)		500		400		300		250		200	ns
tEH	Chip Enable HIGH Time (Note 14)	500		400		300		250		200		ns
tEL	Chip Enable LOW Time (Note 14)	250		200		150		125		100		ns
tCH	Chip Enable to Chip Select Hold Time	200		170		150		130		120		ns
tAH	Chip Enable to Address Hold Time	200		170		150		130		120		ns
tCS	Chip Select to CE Set-Up Time (Note 4)	–5		–5		–5		–5		–5		ns
tAS	Address to Chip Enable Set-Up Time	0		0		0		0		0		ns
tRS	Read to Chip Enable Set-Up Time	0		0		0		0		0		ns
tRH	Chip Enable to Read Hold Time	0		0		0		0		0		ns
tOH	Chip Enable to Output OFF Delay (Note 3)	0		0		0		0		0		ns
tCF	OE or OD to Output OFF Delay (Note 11)		200		165		135		115		100	ns
tCO	OE or OD to Output ON Delay (Note 11)		220		185		150		125		110	ns
tES	Output Enable to CE LOW Set-Up Time (Note 12)	90		75		60		55		50		ns
tDM	Data Out to Memory Status Delay	0		0		0		0		0		ns
tP	Internal Preset Interval (Note 14)		tEL		tEL		tEL		tEL		tEL	ns

SWITCHING WAVEFORMS

READ CYCLE



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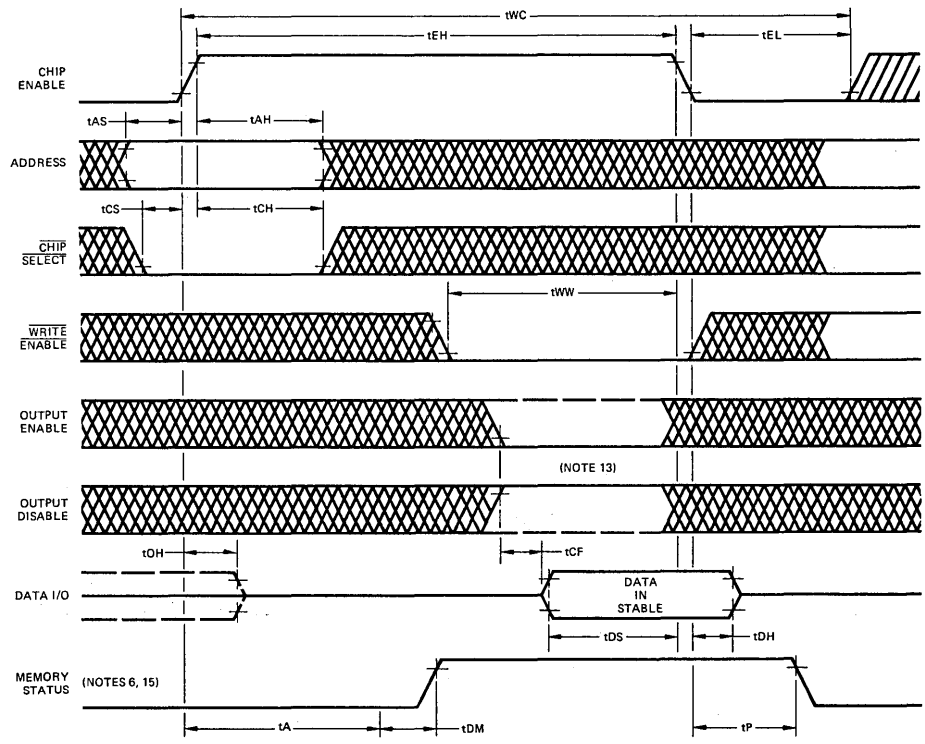
SWITCHING CHARACTERISTICS over operating range

WRITE CYCLE (Notes 7, 8, 9)

Parameter	Description	Am9130A / Am91L30A Min.	Am9130A / Am91L30A Max.	Am9130B / Am91L30B Min.	Am9130B / Am91L30B Max.	Am9130C / Am91L30C Min.	Am9130C / Am91L30C Max.	Am9130D / Am91L30D Min.	Am9130D / Am91L30D Max.	Am9130E Min.	Am9130E Max.	Unit
tWC	Write Cycle Time (Note 5)	770		620		470		395		320		ns
tA	Access Time (CE to Output ON Delay)		500		400		300		250		200	ns
tEH	Chip Enable HIGH Time (Notes 14, 15)	500		400		300		250		200		ns
tEL	Chip Enable LOW Time (Notes 14, 15)	250		200		150		125		100		ns
tAS	Address to Chip Enable Set-Up Time	0		0		0		0		0		ns
tAH	Chip Enable to Address Hold Time	200		170		150		130		120		ns
tCS	Chip Select to CE Set-Up Time (Note 4)	–5		–5		–5		–5		– 5		ns
tCH	Chip Enable to Chip Select Hold Time	200		170		150		130		120		ns
tWW	Write Pulse Width (Note 10)	200		165		135		115		100		ns
tDS	Data Input Set-Up Time (Note 10)	200		165		135		115		100		ns
tDH	Data Input Hold Time (Note 10)	0		0		0		0		0		ns
tDM	Data Out to Memory Status Delay	0		0		0		0		0		ns
tP	Internal Preset Interval		tEL		tEL		tEL		tEL		tEL	ns

SWITCHING WAVEFORMS

WRITE CYCLE



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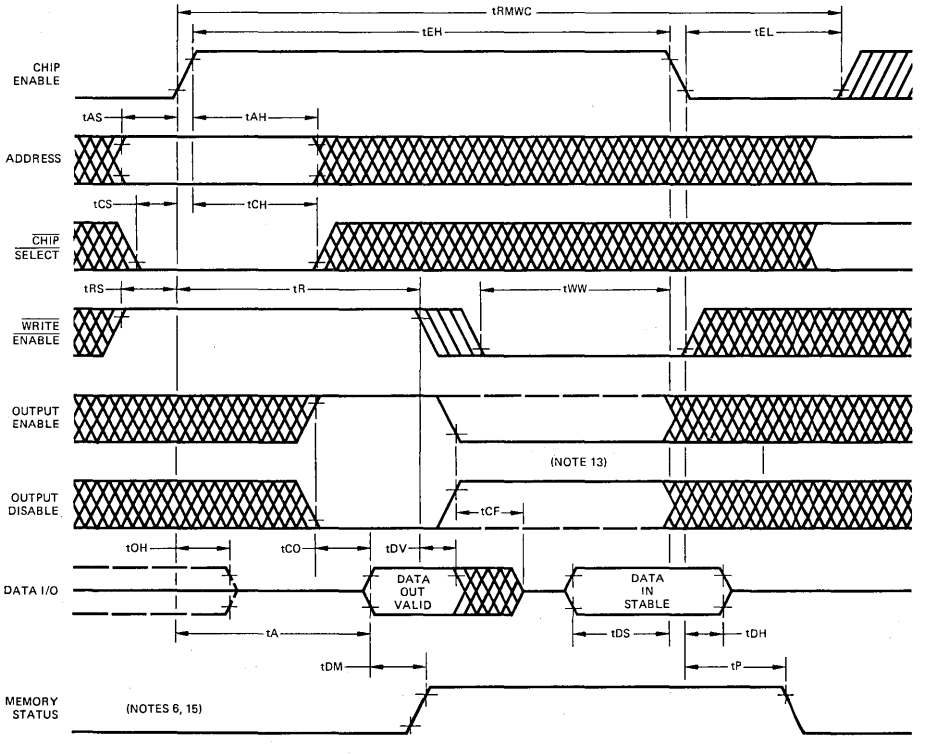
SWITCHING CHARACTERISTICS over operating range

READ/MODIFY/WRITE CYCLE (Notes 7, 8, 9)

Parameter	Description	Am9130A / Am91L30A Min.	Am9130A / Am91L30A Max.	Am9130B / Am91L30B Min.	Am9130B / Am91L30B Max.	Am9130C / Am91L30C Min.	Am9130C / Am91L30C Max.	Am9130D / Am91L30D Min.	Am9130D / Am91L30D Max.	Am9130E Min.	Am9130E Max.	Unit
tRMWC	R/M/W Cycle Time (Notes 5, 16)	1170		950		740		625		520		ns
tA	Access Time (CE to Output Valid Delay)		500		400		300		250		200	ns
tEH	Chip Enable HIGH Time (Notes 14, 15)	900		730		570		480		400		ns
tEL	Chip Enable LOW Time (Notes 14, 15)	250		200		150		125		100		ns
tCH	Chip Enable to Chip Select Hold Time	200		170		150		130		120		ns
tAH	Chip Enable to Address Hold Time	200		170		150		130		120		ns
tCS	Chip Select to CE Set-Up Time (Note 4)	–5		–5		–5		–5		–5		ns
tAS	Address to Chip Enable Set-Up Time	0		0		0		0		0		ns
tRS	Read to Chip Enable Set-Up Time	0		0		0		0		0		ns
tOH	Chip Enable to Output OFF Delay	0		0		0		0		0		ns
tDH	Data Input Hold Time (Note 10)	0		0		0		0		0		ns
tDS	Data Input Set-Up Time (Note 10)	200		165		135		115		100		ns
tWW	Write Pulse Width (Note 10)	200		165		135		115		100		ns
tCF	OE or OD to Output OFF Delay (Note 11)		200		165		135		115		100	ns
tCO	OE or OD to Output ON Delay (Note 11)		220		185		150		125		110	ns
tDV	Data Valid after Write Delay	10		10		10		10		10		ns
tR	Read Mode Hold Time	tA		tA		tA		tA		tA		ns
tDM	Data Out to Memory Status Delay	0		0		0		0		0		ns
tP	Internal Preset Interval		tEL		tEL		tEL		tEL		tEL	ns

SWITCHING CHARACTERISTICS
READ/MODIFY/WRITE CYCLE



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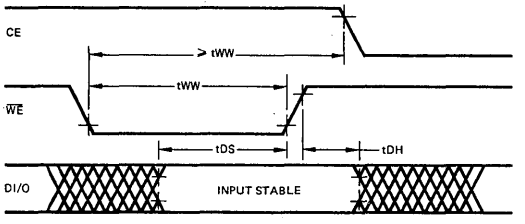
NOTES:

1. Typical operating supply current values are specified for nominal processing parameters, nominal supply voltage and the specific ambient temperature shown.
2. Typical power-down supply current values are specified for nominal processing parameters, the specific supply voltage shown and the specific ambient temperature shown.
3. At any operating temperature the minimum access time, tA(min.), will be greater than the maximum CE to output OFF delay, tOH(max.).
4. The negative value shown indicates that the Chip Select input may become valid as late as 5ns following the start of the Chip Enable rising edge.
5. The worst-case cycle times are the sum of CE rise time, tEH, CE fall time and tEL. The cycle time values shown include the worst-case tEH and tEL requirements and assume CE transition times of 10ns.
6. The Memory Status signal is a two-state output and is not affected by the Output Disable or Output Enable signals. If the output data buffers are turned off, Memory Status will continue to reflect the internal status of the memory.
7. Output loading is assumed to be one standard TTL gate plus 50pF of capacitance.
8. Timing reference levels for both input and output signals are 0.8V and 2.0V.
9. CE and $\overline{WE}$ transition times are assumed to be $\leqslant$10ns.
10. The internal write time of the memory is defined by the overlap of CE high and $\overline{WE}$ low. Both signals must be present on a selected chip to initiate a write. Either signal can terminate a write. The tWW, tDS and tDH specifications should all be referenced to the end of the write time. The Write Cycle timing diagram shows termination by the falling edge of CE. If termination is defined by bringing $\overline{WE}$ high while CE is high, the following timing applies:



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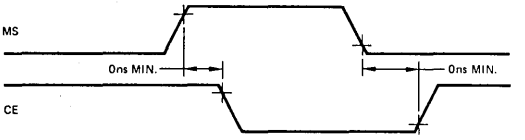
11. The output data buffer can be ON and output data valid only when Output Enable is high and Output Disable is low. OE and OD perform the same function with opposite control polarity.
12. The output data buffer should be enabled before the falling edge of CE in order to read output information. When the output is disabled and CE is low, the output data register is cleared.
13. Input and output data are the same polarity.
14. The Chip Enable waveform requirements may be defined by the Memory Status output waveform. For a read cycle, the basic CE requirement is that tEH $\geqslant$ tA and tEL $\geqslant$ tP:



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15. The Memory Status output functions as if all operations are read cycles. If a write cycle begins with $\overline{WE}$ low and Data In stable at the time CE goes high, the rising edge of MS may be used as an indication that the write is complete and CE may be brought low. In a cycle where $\overline{WE}$ goes low at some point within the CE high time, the rising edge of MS should be ignored as an indication of write status. The falling edge of MS is always valid independent of the type of operation being performed.
16. For the R/M/W cycle, tEH (min.) is defined as tR (min.) +tCF (max.) + tDS (min.). This provides a conservative design with no I/O overlap and assumes that tCF begins at the end of the tR time. Other designs with somewhat shorter R/M/W cycles are possible.

FUNCTION DESCRIPTION

Block Diagram

The block diagram for the Am9130 shows the interface connections along with the general signal flow. There are ten address lines (A0 through A9) that are used to specify one of 1024 locations, with each location containing 4 bits. The Chip Select signal acts as a high order address. The Chip Enable clock latches the addresses into the address registers and controls the sequence of internal activities.

The row address signals (A0 through A5) and their inversions are distributed to the 64 row address decoders where one of the rows is selected. The 64 cells on the selected row are then connected to their respective bit line columns. Meanwhile, the column address signals (A6 through A9) are decoded and used to select 4 of 64 columns for the sense amplifiers. Thus a single cell is connected to each output path.

During read operations, the sensed data is latched into the output register and is available for the balance of the operating cycle. During write operations, the write amplifier is turned on and drives the input data onto the sense lines, up the column

bit lines and into the selected cell. Read and write data are the same polarity.

The data buffer is three-state and unselected chips have their outputs turned off so that several may be wire-ored together. The Output Enable and Output Disable signals provide asynchronous controls for turning off the output buffers.

Within the storage matrix there is an extra row of simulated cells. This reference row is selected on every operating cycle in addition to the addressed row and provides internal timing signals that control the data flow through the memory. The Memory Status output signal is derived from the reference row and uses the same designs for its sense and buffer circuits as used by the data bits.

Chip Enable

The Chip Enable input is a control clock that coordinates all internal activities. The rising edge of CE begins each cycle and strobes the Address and Chip Select signals into the on-chip register. Internal timing signals are derived from CE and from transitions of the address latches and the reference cells.

When the actual access time of the part has been reached (or a write operation is complete), CE may be switched low if desired. The worst-case time as specified in the data sheet may be used to determine the access. Alternatively, the access or write-complete time indicated by the rising edge of the Memory Status output signal may be used.

When CE goes low, the internal preset operation begins. The memory is ready for a new cycle only after the preset is complete. The worst-case CE low time specified in the data sheet may be used to determine the preset interval. Alternatively, the actual preset time is indicated as complete when Memory Status goes low.

There are no restrictions on the maximum times that CE may remain in either state so the clock may be extended or stopped whenever convenient. After power-on and before beginning a valid operation, the clock should be brought low to initially preset the memory.

Address and Chip Select

The Address inputs are latched into the on-chip address register by the rising edge of CE. Addresses must be held stable for the specified minimum time following the rising edge of CE in order to be properly loaded into the register. Following the address hold time, the address inputs are ignored by the memory until the next cycle is initiated.

The Chip Select input acts as a high order address for use when the system word capacity is larger than that of an individual chip. It allows the Address lines to be wired in parallel to all chips with the CS lines then used to select one active row of chips at a time. Unselected chips have their output buffers off so that selected chips wired to the same data lines can dominate the output bus. Only selected chips can perform write operations.

CS is latched in the same way that Addresses are. Once a memory is selected or deselected, it will remain that way until a new cycle with new select information begins.

Write Enable

The Write Enable line controls the read or write condition of the devices. When the CE clock is low, the WE signal may be in any state without affecting the memory. WE does not affect the status of the output buffer.

To execute a read cycle, WE is held high while CE is high. To perform a write operation, the WE line is switched low while CE is high. Only a narrow write pulse width is required to successfully write into a cell. In many cases, however, it will be convenient to leave the WE line low during the whole cycle.

A write cycle can take place only when three conditions are met: The chip is selected, CE is high, and WE is low. This means that if either CE goes low or WE goes high, the writing is terminated.

Data In and Data Out

The requirements for incoming data during a write operation show a minimum set-up time with respect to the termination of the write. Termination occurs when either WE goes high or CE goes low. If incoming data changes during a write operation, the information finally written in the cell will be that stable data preceeding the termination by the set-up time. Since the data being written during a write cycle is impressed on the sense amplifier inputs, the output data will be the same as the input once the write is established.

During a read cycle, once all of the addressing is complete and the cell information has propagated through the sense amplifier, it enters the output data register. The read information can also flow through to the output if the buffer is enabled. As long as CE is high, the addressing remains valid and the output data will be stable. When CE goes low to begin the internal preset operation, the output information is latched into the data register. It will remain latched and stable as long as CE is low. If the output is disabled when CE is low, the output data register is cleared. At the start of every cycle when CE goes high, the output data latch is cleared in preparation for new information to come from the sense amplifier, and the output buffer is turned off.

OE and OD are designed to provide asynchronous control of the output buffer independent of the synchronous Chip Select control. The OE and OD control lines perform the same internal function except that one is inverted from the other. If either OE is low or OD is high, the output buffer will turn off. If the CS input is latched low and OE is high and OD is low, then the output buffer can turn on when data is available.

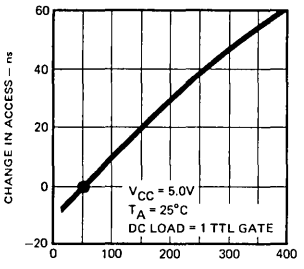
Memory Status

The Memory Status output is derived from the actual performance of the reference row of cells. Since the reference row is always doing a read operation, the MS output will appear in every operating cycle, whether a read or write is being performed. MS uses the same output circuitry as used in the data path. The result is that Memory Status tracks very closely the true operating performance of the memory.

The rising edge of MS indicates when output data is valid and tracks changes in access time with changing operating conditions. The rising edge also specifies the end of the time that CE must be held high for a read. CE may be high as long as desired, but may safely go low any time after MS goes high. The falling edge of MS occurs after CE goes low and the internal preset period is complete. It indicates that CE may go high to begin a new cycle. See the Am9130/40 Application Note for details.

CHARACTERISTICS

Access Change Versus Capacitive Load



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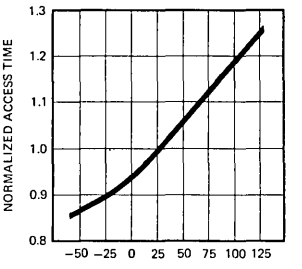
Access Time Versus Ambient Temperature



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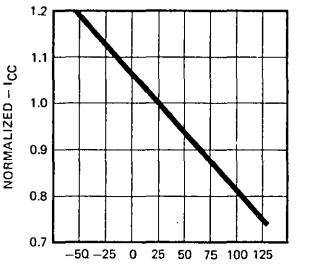
Supply Current Versus Ambient Temperature



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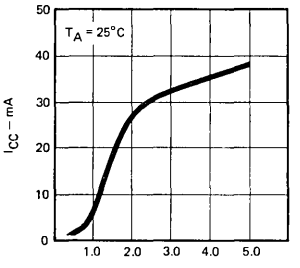
Typical I_{CC} Versus V_{CC}



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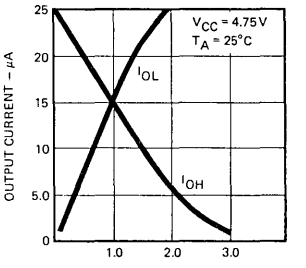
Typical Output Currents Versus Output Voltage



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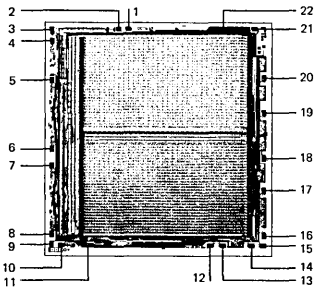
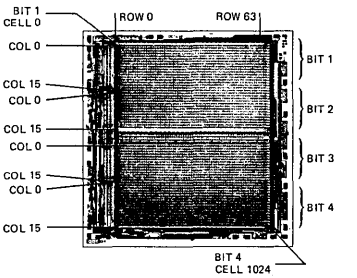
Metallization and Pad Layout



DIE SIZE 0.192" X 0.197"

Bit Map



For bit mapping purposes:
Row address LSB = A5, MSB = A0
Column address LSB = A6, MSB = A9

Am9140 • Am91L40

4096 x 1 Static R/W Random Access Memories

DISTINCTIVE CHARACTERISTICS

- 4k X 1 organization
- Fully static data storage — no refreshing
- Single +5V power supply
- High-speed — access times down to 200ns max.
- Low operating power
  - 578mW max., 9140
  - 368mW max., 91L40
- Interface logic levels identical to TTL
- High noise immunity — 400mV worst-case
- High output drive — two standard TTL loads
- DC power-down mode — reduces power by >80%
- Single phase, low voltage, low capacitance clock
- Static clock may be stopped in either state
- Data register on-chip
- Address register on-chip
- Steady power drain — no large surges
- Unique Memory Status signal
  - improves performance
  - self-clocking operation
- Full MIL temperature range available
- 100% MIL-STD-883 reliability assurance testing

GENERAL DESCRIPTION

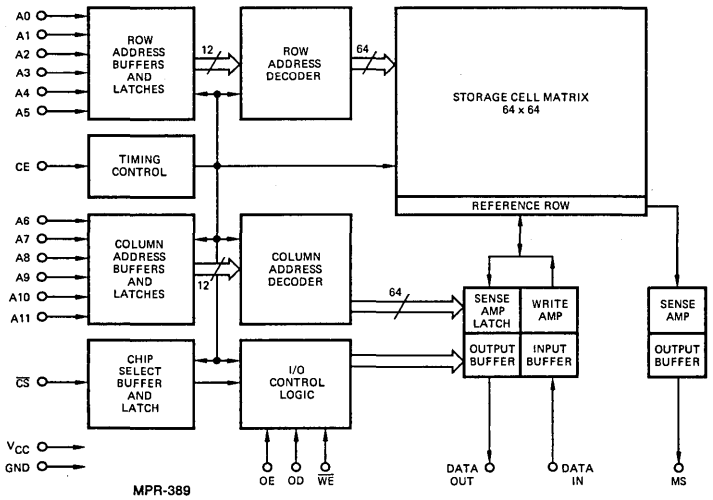
The Am9140 and Am91L40 products are high performance, adaptive, low-power, 4k-bit, static, read/write random access memories. They are implemented as 4096 words by 1 bit per word. Only a single +5V power supply is required for normal operation. A DC power down mode reduces power while retaining data with a supply voltage as low as 1.5V.

All interface signal levels are identical to TTL specifications, providing good noise immunity and simplified system design. All inputs are purely capacitive MOS loads. The outputs will drive two full TTL loads or more than eight low-power Schottky loads.

Operational cycles are initiated when the Chip Enable clock goes HIGH. When the read or write is complete, Chip Enable goes LOW to preset the memory for the next cycle. Address and Chip Select signals are latched on-chip to simplify system timing. Output data is also latched and is available until the next operating cycle. The $\overline{WE}$ signal is HIGH for all read operations and is LOW during the Chip Enable time to perform a write.

Memory Status is an output signal that indicates when data is actually valid and when the preset interval is complete. It can be used to generate the CE input and to improve the memory performance.

BLOCK DIAGRAM



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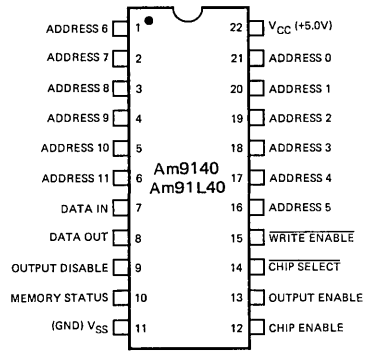
CONNECTION DIAGRAM



Top View

Pin 1 is marked for orientation.

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ORDERING INFORMATION

Package Type	Ambient Temperature	Power Type	Access Time 500ns	400ns	300ns	250ns	200ns
Hermetic DIP	$0°C \leq T_A \leq +70°C$	STD	Am9140ADC	Am9140BDC	Am9140CDC	Am9140DDC	Am9140EDC
		LOW	Am91L40ADC	Am91L40BDC	Am91L40CDC	Am91L40DDC	
	$-55°C \leq T_A \leq +125°C$	STD	Am9140ADM	Am9140BDM	Am9140CDM		
		LOW	Am91L40ADM	Am91L40BDM	Am91L40CDM		

MAXIMUM RATINGS above which the useful life may be impaired

Storage Temperature	−65°C to +150°C
Ambient Temperature Under Bias	−55°C to +125°C
V_{CC} with Respect to V_{SS}	−0.5V to +7.0V
All Signal Voltages with Respect to V_{SS}	−0.5V to +7.0V
Power Dissipation	1.25W

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of static charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

OPERATING RANGE		POWER DOWN RANGE			
V_{CC}	V_{SS}	V_{CC}	V_{SS}	Ambient Temperature	Part Number
$4.75V \leq V_{CC} \leq 5.25V$	0V	$1.5V \leq V_{CC} \leq 5.25V$	0V	$0°C \leq T_A \leq +70°C$	AM91X40XDC
$4.50V \leq V_{CC} \leq 5.50V$	0V	$1.5V \leq V_{CC} \leq 5.50V$	0V	$-55°C \leq T_A \leq +125°C$	AM91X40XDM

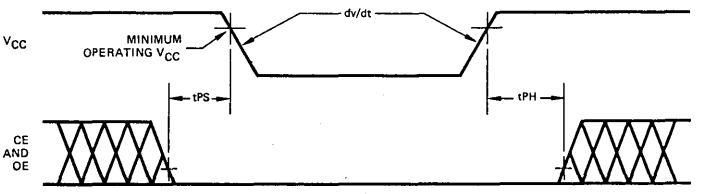
ELECTRICAL CHARACTERISTICS over operating range (Note 1)

Parameters	Description	Test Conditions		Am9140 Min.	Am9140 Typ.	Am9140 Max.	Am91L40 Min.	Am91L40 Typ.	Am91L40 Max.	Units
V_{OH}	Output HIGH Voltage	$I_{OH} = -200\mu A$	$V_{CC} = 4.75V$	2.4			2.4			Volts
			$V_{CC} = 4.5V$	2.2			2.2			
V_{OL}	Output LOW Voltage	$I_{OL} = 3.2mA$				0.4			0.4	Volts
V_{IH}	Input HIGH Voltage			2.0		V_{CC}	2.0		V_{CC}	Volts
V_{IL}	Input LOW Voltage			−0.5		0.8	−0.5		0.8	Volts
I_{LI}	Input Load Current	$V_{SS} \leq V_{IN} \leq V_{CC}$				10			10	µA
I_{LO}	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{CC}$, Output disabled				10			10	µA
I_{CC}	V_{CC} Supply Current	Max. V_{CC} Output disabled	$T_A = 25°C$		50	100		40	65	mA
			$T_A = 0°C$			110			70	
			$T_A = -55°C$			125			80	
C_{IA}	Input Capacitance (Address)	Test frequency = 1MHz $T_A = 25°C$ All pins at 0V			3.0	6.0		3.0	6.0	pF
C_{OUT}	Output Capacitance				4.0	7.0		4.0	7.0	pF
C_{IC}	Input Capacitance (Control)				6.0	9.0		6.0	9.0	pF

POWER DOWN CHARACTERISTICS

Parameter	Description	Test Conditions		Am9140 Min.	Am9140 Typ.	Am9140 Max.	Am91L40 Min.	Am91L40 Typ.	Am91L40 Max.	Unit
dv/dt	V_{CC} Rate of Change					3.0			3.0	V/µs
tPS	Power Down Set-Up Time			tEL			tEL			ns
tPH	Power Up Hold Time			tEL			tEL			ns
I_{PD}	I_{CC} in Standby (Note 2)	$V_{CC} = 2.0V$	$T_A = 25°C$		36	72		28	55	mA
			$T_A = 0°C$			78			60	mA
			$T_A = -55°$			89			68	mA
		$V_{CC} = 1.5V$	$T_A = 25°C$		20	52		16	45	mA
			$T_A = 0°C$			56			48	mA
			$T_A = -55°C$			64			55	mA

POWER DOWN WAVEFORM



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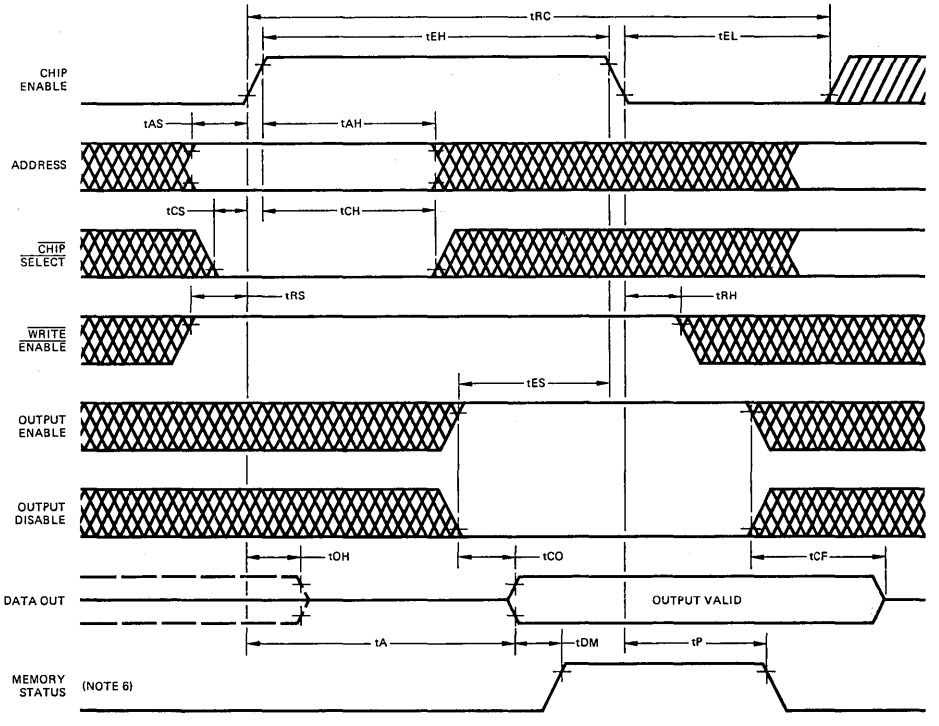
SWITCHING CHARACTERISTICS over operating range

READ CYCLE (Notes 7, 8, 9)

Parameter	Description	Am9140A / Am91L40A Min.	Am9140A / Am91L40A Max.	Am9140B / Am91L40B Min.	Am9140B / Am91L40B Max.	Am9140C / Am91L40C Min.	Am9140C / Am91L40C Max.	Am9140D / Am91L40D Min.	Am9140D / Am91L40D Max.	Am9140E Min.	Am9140E Max.	Unit
tRC	Read Cycle Time (Note 5)	770		620		470		395		320		ns
tA	Access Time (Note 3) (CE to Output Valid Delay)		500		400		300		250		200	ns
tEH	Chip Enable HIGH Time (Note 14)	500		400		300		250		200		ns
tEL	Chip Enable LOW Time (Note 14)	250		200		150		125		100		ns
tCH	Chip Enable to Chip Select Hold Time	200		170		150		130		120		ns
tAH	Chip Enable to Address Hold Time	200		170		150		130		120		ns
tCS	Chip Select to CE Set-Up Time (Note 4)	–5		–5		–5		–5		–5		ns
tAS	Address to Chip Enable Set-Up Time	0		0		0		0		0		ns
tRS	Read to Chip Enable Set-Up Time	0		0		0		0		0		ns
tRH	Chip Enable to Read Hold Time	0		0		0		0		0		ns
tOH	Chip Enable to Output OFF Delay (Note 3)	0		0		0		0		0		ns
tCF	OE or OD to Output OFF Delay (Note 11)		200		165		135		115		100	ns
tCO	OE or OD to Output ON Delay (Note 11)		220		185		150		125		110	ns
tES	Output Enable to CE LOW Set-Up Time (Note 12)	90		75		60		55		50		ns
tDM	Data Out to Memory Status Delay	0		0		0		0		0		ns
tP	Internal Preset Interval (Note 14)		tEL		tEL		tEL		tEL		tEL	ns

SWITCHING WAVEFORMS

READ CYCLE



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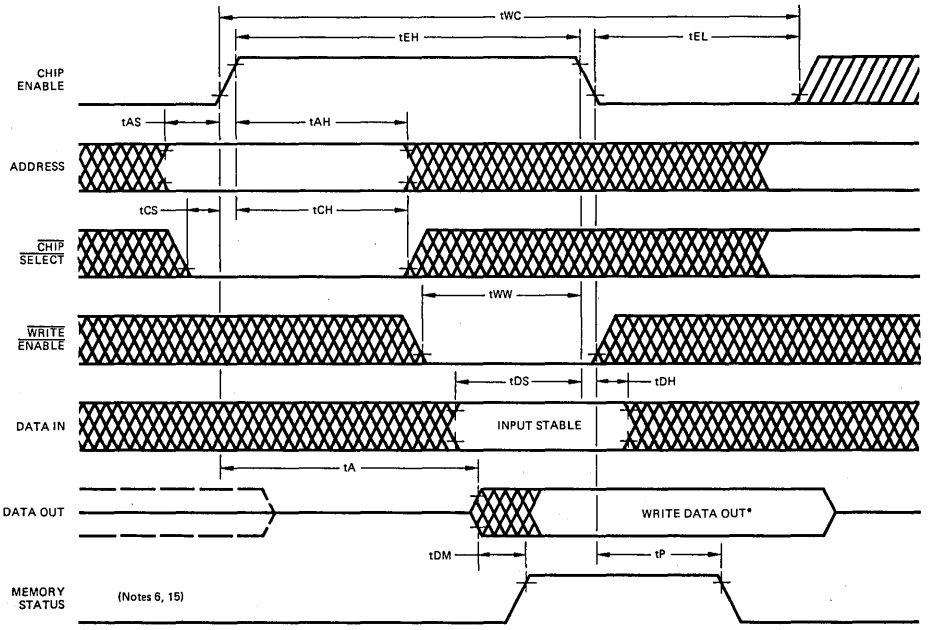
SWITCHING CHARACTERISTICS over operating range

WRITE CYCLE (Notes 7, 8, 9)

Parameter	Description	Am9140A / Am91L40A Min.	Am9140A / Am91L40A Max.	Am9140B / Am91L40B Min.	Am9140B / Am91L40B Max.	Am9140C / Am91L40C Min.	Am9140C / Am91L40C Max.	Am9140D / Am91L40D Min.	Am9140D / Am91L40D Max.	Am9140E Min.	Am9140E Max.	Unit
tWC	Write Cycle Time (Note 5)	770		620		470		395		320		ns
tA	Access Time (CE to Output ON Delay)		500		400		300		250		200	ns
tEH	Chip Enable HIGH Time (Notes 14, 15)	500		400		300		250		200		ns
tEL	Chip Enable LOW Time (Notes 14, 15)	250		200		150		125		100		ns
tAS	Address to Chip Enable Set-Up Time	0		0		0		0		0		ns
tAH	Chip Enable to Address Hold Time	200		170		150		130		120		ns
tCS	Chip Select to CE Set-Up Time (Note 4)	–5		–5		–5		–5		– 5		ns
tCH	Chip Enable to Chip Select Hold Time	200		170		150		130		120		ns
tWW	Write Pulse Width (Note 10)	200		165		135		115		100		ns
tDS	Data Input Set-Up Time (Note 10)	200		165		135		115		100		ns
tDH	Data Input Hold Time (Note 10)	0		0		0		0		0		ns
tDM	Data Out to Memory Status Delay	0		0		0		0		0		ns
tP	Internal Preset Interval		tEL		tEL		tEL		tEL		tEL	ns

SWITCHING WAVEFORMS

WRITE CYCLE



*Assumes output is enabled.

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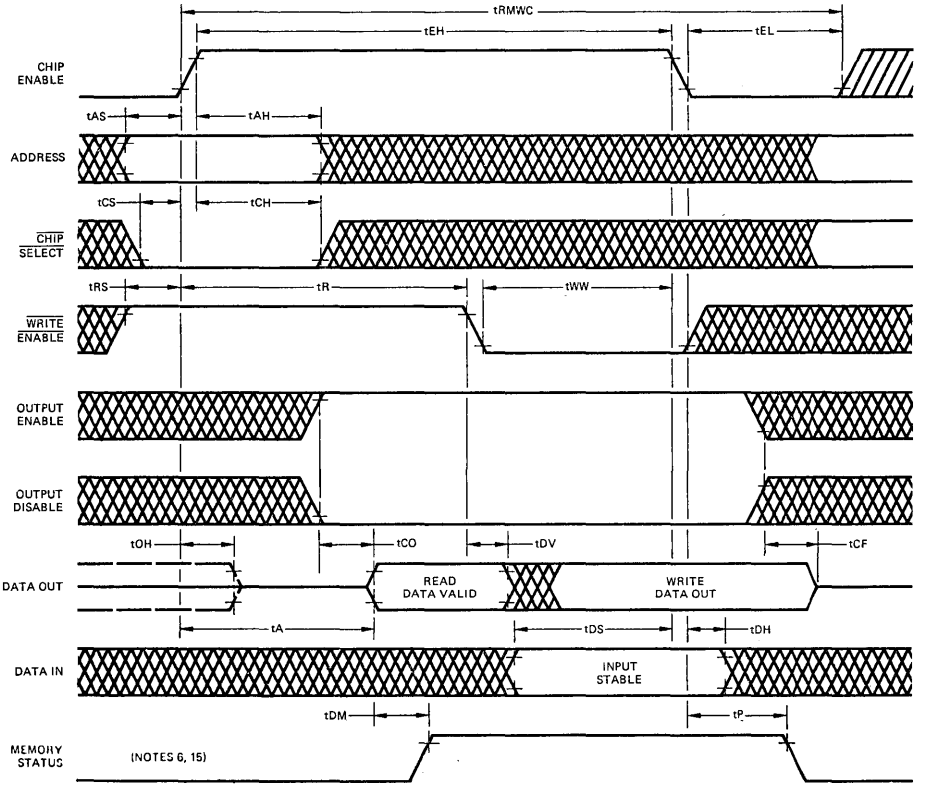
SWITCHING CHARACTERISTICS over operating range

READ/MODIFY/WRITE CYCLE (Notes 7, 8, 9)

Parameter	Description	Am9140A / Am91L40A Min.	Am9140A / Am91L40A Max.	Am9140B / Am91L40B Min.	Am9140B / Am91L40B Max.	Am9140C / Am91L40C Min.	Am9140C / Am91L40C Max.	Am9140D / Am91L40D Min.	Am9140D / Am91L40D Max.	Am9140E Min.	Am9140E Max.	Unit
tRMWC	R/M/W Cycle Time (Notes 5, 16)	970		785		605		510		420		ns
tA	Access Time (CE to Output Valid Delay)		500		400		300		250		200	ns
tEH	Chip Enable HIGH Time (Notes 14, 15)	700		565		435		365		300		ns
tEL	Chip Enable LOW Time (Notes 14, 15)	250		200		150		125		100		ns
tCH	Chip Enable to Chip Select Hold Time	200		170		150		130		120		ns
tAH	Chip Enable to Address Hold Time	200		170		150		130		120		ns
tCS	Chip Select to CE Set-Up Time (Note 4)	–5		–5		–5		–5		–5		ns
tAS	Address to Chip Enable Set-Up Time	0		0		0		0		0		ns
tRS	Read to Chip Enable Set-Up Time	0		0		0		0		0		ns
tOH	Chip Enable to Output OFF Delay	0		0		0		0		0		ns
tDH	Data Input Hold Time (Note 10)	0		0		0		0		0		ns
tDS	Data Input Set-Up Time (Note 10)	200		165		135		115		100		ns
tWW	Write Pulse Width (Note 10)	200		165		135		115		100		ns
tCF	OE or OD to Output OFF Delay (Note 11)		200		165		135		115		100	ns
tCO	OE or OD to Output ON Delay (Note 11)		220		185		150		125		110	ns
tDV	Data Valid after Write Delay	10		10		10		10		10		ns
tR	Read Mode Hold Time	tA		tA		tA		tA		tA		ns
tDM	Data Out to Memory Status Delay	0		0		0		0		0		ns
tP	Internal Preset Interval		tEL		tEL		tEL		tEL		tEL	ns

SWITCHING WAVEFORMS

READ/MODIFY/WRITE CYCLE



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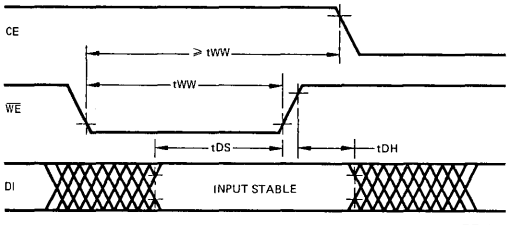
NOTES:

1. Typical operating supply current values are specified for nominal processing parameters, nominal supply voltage and the specific ambient temperature shown.
2. Typical power-down supply current values are specified for nominal processing parameters, the specific supply voltage shown and the specific ambient temperature shown.
3. At any operating temperature the minimum access time, tA(min.), will be greater than the maximum CE to output OFF delay, tOH(max.).
4. The negative value shown indicates that the Chip Select input may become valid as late as 5.0ns following the start of the Chip Enable rising edge.
5. The worst-case cycle times are the sum of CE rise time, tEH, CE fall time and tEL. The cycle time values shown include the worst-case tEH and tEL requirements and assume CE transition times of 10ns.
6. The Memory Status signal is a two-state output and is not affected by the Output Disable or Output Enable signals. If the output data buffers are turned off, Memory Status will continue to reflect the internal status of the memory.
7. Output loading is assumed to be one standard TTL gate plus 50pF of capacitance.
8. Timing reference levels for both input and output signals are 0.8V and 2.0V.
9. CE and $\overline{WE}$ transition times are assumed to be $\leqslant$10ns.
10. The internal write time of the memory is defined by the overlap of CE high and $\overline{WE}$ low. Both signals must be present on a selected chip to initiate a write. Either signal can terminate a write. The tWW, tDS and tDH specifications should all be referenced to the end of the write time. The Write Cycle timing diagram shows termination by the falling edge of CE. If termination is defined by bringing $\overline{WE}$ high while CE is high, the following timing applies:



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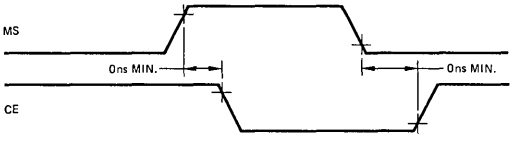
11. The output data buffer can be ON and output data valid only when Output Enable is high and Output Disable is low. OE and OD perform the same function with opposite control polarity.
12. The output data buffer should be enabled before the falling edge of CE in order to read output information. When the output is disabled and CE is low, the output data register is cleared.
13. Input and output data are the same polarity.
14. The Chip Enable waveform requirements may be defined by the Memory Status output waveform. For a read cycle, the basic CE requirement is that tEH $\geqslant$ tA and tEL $\geqslant$ tP:



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15. The Memory Status output functions as if all operations are read cycles. If a write cycle begins with $\overline{WE}$ low and Data In stable at the time CE goes high, the rising edge of MS may be used as an indication that the write is complete and CE may be brought low. In a cycle where $\overline{WE}$ goes low at some point within the CE high time, the rising edge of MS should be ignored as an indication of write status. The falling edge of MS is always valid independent of the type of operation being performed.
16. For the R/M/W cycle, tEH (min.) is defined as tR (min.) + tWW. Note 5 defines tRMWC but it may also be viewed as tRC + tWW. Modify times are assumed to be zero. For systems with Data In and Data Out tied together R/M/W timing should make allowance for tCF time so that no bus conflict occurs (see Am9130 data sheet for timing approach).

FUNCTIONAL DESCRIPTION

Block Diagram

The block diagram for the Am9140 shows the interface connections along with the general signal flow. There are twelve address lines (A0 through A11) that are used to specify one of 4096 locations, with each location containing one bit. The Chip Select signal acts as a high order address. The Chip Enable clock latches the addresses into the address registers and controls the sequence of internal activities.

The row address signals (A0 through A5) and their inversions are distributed to the 64 row address decoders where one of the rows is selected. The 64 cells on the selected row are then connected to their respective bit line columns. Meanwhile, the column address signals (A6 through A11) are decoded and used to select one of 64 columns for the sense amplifier. Thus a single cell is connected into the output path.

During read operations, the sensed data is latched into the output register and is available for the balance of the operating cycle. During write operations, the write amplifier is turned on and drives the input data onto the sense lines, up the column

bit lines and into the selected cell. Read and write data are the same polarity.

The data buffer is three-state and unselected chips have their outputs turned off so that several may be wire-ored together. The Output Enable and Output Disable signals provide asynchronous controls for turning off the output buffers.

Within the storage matrix there is an extra row of simulated cells. This reference row is selected on every operating cycle in addition to the addressed row and provides internal timing signals that control the data flow through the memory. The Memory Status output signal is derived from the reference row and uses the same designs for its sense and buffer circuits as used by the data bits.

Chip Enable

The Chip Enable input is a control clock that coordinates all internal activities. The rising edge of CE begins each cycle and strobes the Address and Chip Select signals into the on-chip register. Internal timing signals are derived from CE and from transitions of the address latches and the reference cells.

When the actual access time of the part has been reached (or a write operation is complete), CE may be switched low if desired. The worst-case time as specified in the data sheet may be used to determine the access. Alternatively, the access or write-complete time indicated by the rising edge of the Memory Status output signal may be used.

When CE goes low, the internal preset operation begins. The memory is ready for a new cycle only after the preset is complete. The worst-case CE low time specified in the data sheet may be used to determine the preset interval. Alternatively, the actual preset time is indicated as complete when Memory Status goes low.

There are no restrictions on the maximum times that CE may remain in either state so the clock may be extended or stopped whenever convenient. After power-on and before beginning a valid operation, the clock should be brought low to initially preset the memory.

Address and Chip Select

The Address inputs are latched into the on-chip address register by the rising edge of CE. Addresses must be held stable for the specified minimum time following the rising edge of CE in order to be properly loaded into the register. Following the address hold time, the address inputs are ignored by the memory until the next cycle is initiated.

The Chip Select input acts as a high order address for use when the system word capacity is larger than that of an individual chip. It allows the Address lines to be wired in parallel to all chips with the CS lines then used to select one active row of chips at a time. Unselected chips have their output buffers off so that selected chips wired to the same data lines can dominate the output bus. Only selected chips can perform write operations.

CS is latched in the same way that Addresses are. Once a memory is selected or deselected, it will remain that way until a new cycle with new select information begins.

Write Enable

The Write Enable line controls the read or write condition of the devices. When the CE clock is low, the WE signal may be in any state without affecting the memory. WE does not affect the status of the output buffer.

To execute a read cycle, WE is held high while CE is high. To perform a write operation, the WE line is switched low while CE is high. Only a narrow write pulse width is required to successfully write into a cell. In many cases, however, it will be convenient to leave the WE line low during the whole cycle.

A write cycle can take place only when three conditions are met: The chip is selected, CE is high, and WE is low. This means that if either CE goes low or WE goes high, the writing is terminated.

Data In and Data Out

The requirements for incoming data during a write operation show a minimum set-up time with respect to the termination of the write. Termination occurs when either WE goes high or CE goes low. If incoming data changes during a write operation, the information finally written in the cell will be that stable data preceeding the termination by the set-up time. Since the data being written during a write cycle is impressed on the sense amplifier inputs, the output data will be the same as the input once the write is established.

During a read cycle, once all of the addressing is complete and the cell information has propagated through the sense amplifier, it enters the output data register. The read information can also flow through to the output if the buffer is enabled. As long as CE is high, the addressing remains valid and the output data will be stable. When CE goes low to begin the internal preset operation, the output information is latched into the data register. It will remain latched and stable as long as CE is low. If the output is disabled when CE is low, the output data register is cleared. At the start of every cycle when CE goes high, the output data latch is cleared in preparation for new information to come from the sense amplifier, and the output buffer is turned off.

OE and OD are designed to provide asynchronous control of the output buffer independent of the synchronous Chip Select control. The OE and OD control lines perform the same internal function except that one is inverted from the other. If either OE is low or OD is high, the output buffer will turn off. If the CS input is latched low and OE is high and OD is low, then the output buffer can turn on when data is available.

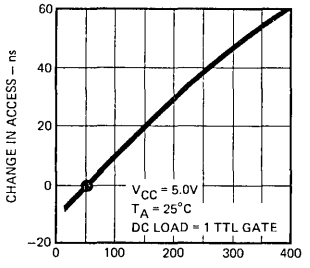
Memory Status

The Memory Status output is derived from the actual performance of the reference row of cells. Since the reference row is always doing a read operation, the MS output will appear in every operating cycle, whether a read or write is being performed. MS uses the same output circuitry as used in the data path. The result is that Memory Status tracks very closely the true operating performance of the memory.

The rising edge of MS indicates when output data is valid and tracks changes in access time with changing operating conditions. The rising edge also specifies the end of the time that CE must be held high for a read. CE may be high as long as desired, but may safely go low any time after MS goes high. The falling edge of MS occurs after CE goes low and the internal preset period is complete. It indicates that CE may go high to begin a new cycle. See the Am9130/40 Application Note for details.

CHARACTERISTICS

Access Change Versus Capacitive Load



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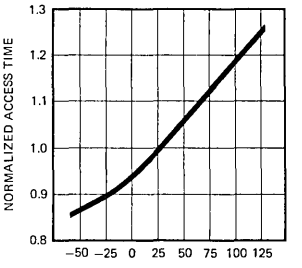
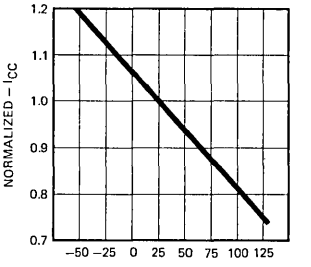
Access Time Versus Ambient Temperature



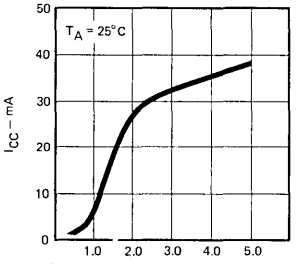
MPR-398

Supply Current Versus Ambient Temperature



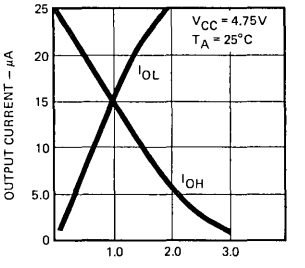
MPR-399

Typical I_{CC} Versus V_{CC}



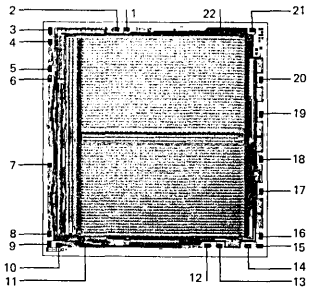
MPR-400

Typical Output Currents Versus Output Voltage



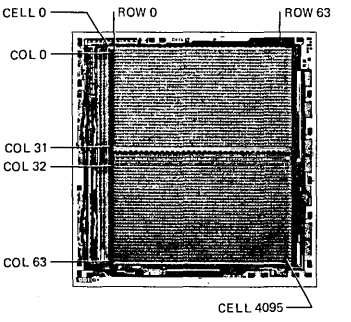
MPR-401

Metallization and Pad Layout



DIE SIZE 0.192" X 0.197"

Bit Map

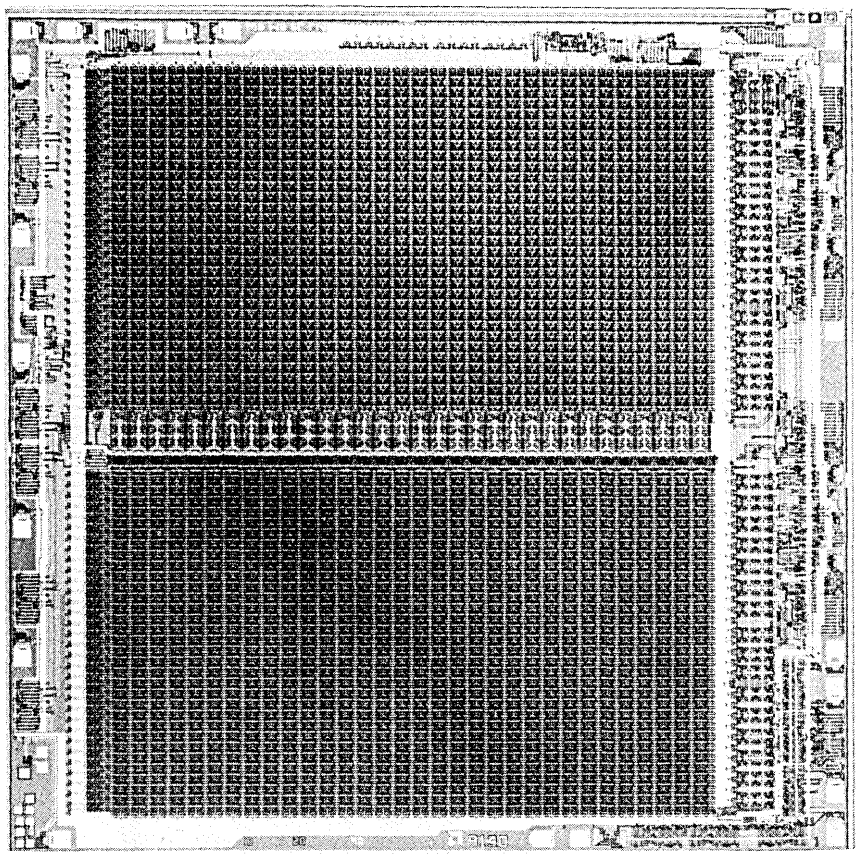


For bit mapping purposes:
Row address LSB = A5, MSB = A0
Column address LSB = A6, MSB = A11

Am9130/Am9140

DESIGNING WITH SELF-CLOCKING, ADAPTIVE 4K STATIC R/W RANDOM ACCESS MEMORIES

By Joseph H. Kroeger



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GENERAL CHARACTERISTICS

Introduction

The Am9130 and Am9140 products from Advanced Micro Devices are 4K-bit, static, self-clocking, adaptive, read/write random access memories. Both types of devices use only a single +5 volt power supply, yet offer high speed performance and low power dissipations. Figure 1 lists the appropriate part numbers for the combinations of variables available at press time. As product enhancement proceeds, it is anticipated that higher speed parts and wider ranges of low-power and military temperature parts will be available. Plastic DIP packages will also become an option. The latest factory data sheets show all available variations of parts.

The Am9130 is organized as 1024 words by 4 bits per word; the Am9140 is organized as 4096 words by 1 bit per word. Parts are available in both commercial and military temperature ranges. Although the standard power parts offer quite low per-bit power dissipation, there is also a family of low-power parts available. As usual at AMD, all parts are 100% reliability assurance tested to the requirements of MIL-STD-883.

Figure 2 shows the pin assignments for the two memories. The package for both parts is a standard 22-pin dual in-line. Both memory configurations are manufactured from the same basic chip and use only specialized metal interconnect layers to define the structural differences. This approach allows several manufacturing efficiencies to be realized and permits each part to benefit from the combined volume of both parts.

The Am9130 and Am9140 memories are implemented with AMD's LINOX N-channel silicon gate MOS technology. The processing and design rules are exactly the same as those used for some time to produce the popular Am9102 line of 1K static R/W memories. LINOX features physically flat structures, triple ion-implantation, and low capacitance, high-speed devices. The new 4K memories are very dense with more than 27,500 active transistors in an area of less than 37,800 mil^2. The chip measures 192 x 197 mils with 58% of the area devoted to the 4096 storage cells.

ORGANIZATION	AMBIENT TEMPERATURE	POWER	ACCESS TIME			
			500ns	400ns	300ns	200ns
1024 x 4	$0°C \leq T_A \leq 70°C$	STANDARD	AM9130ADC	AM9130BDC	AM9130CDC	AM9130EDC
		LOW	AM91L30ADC	AM91L30BDC	AM91L30CDC	
	$-55°C \leq T_A \leq 125°C$	STANDARD	AM9130ADM	AM9130BDM	AM9130CDM	
		LOW	AM91L30ADM	AM91L30BDM		
4096 x 1	$0°C \leq T_A \leq 70°C$	STANDARD	AM9140ADC	AM9140BDC	AM9140CDC	AM9140EDC
		LOW	AM91L40ADC	AM91L40BDC	AM91L40CDC	
	$-55°C \leq T_A \leq +125°C$	STANDARD	AM9140ADM	AM9140BDM	AM9140CDM	
		LOW	AM91L40ADM	AM91L40BDM		

Figure 1. Part Number Matrix.

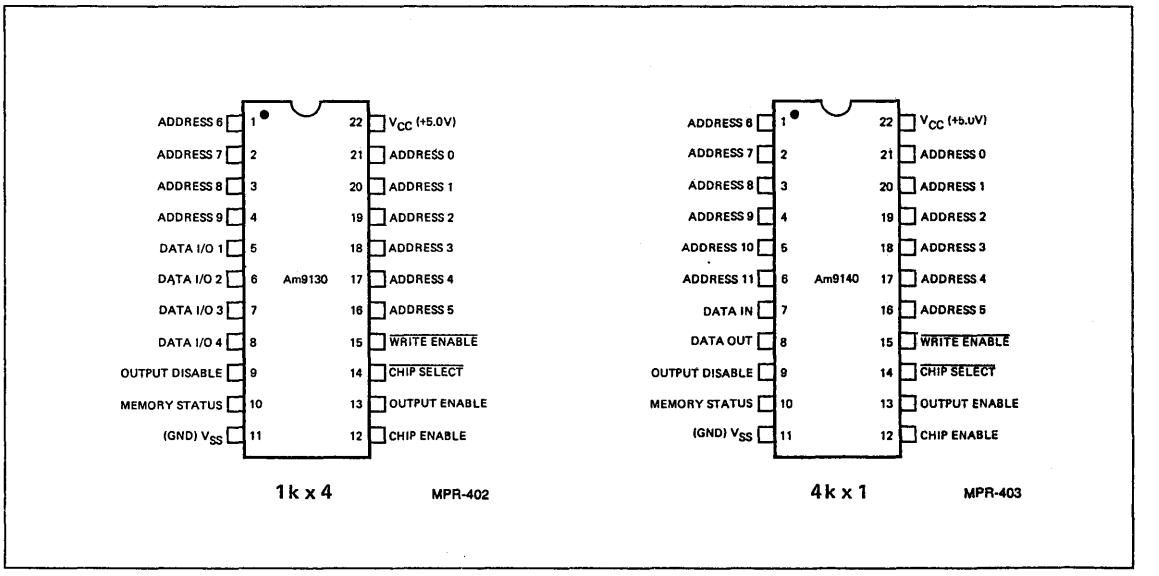


Figure 2. Pin Assignments.

Design Philosophy

Read/write random access memories are customarily divided into two categories based on the storage mechanism used in the memory cells. **Dynamic** memories use dynamic cells that store information in the form of charge on small capacitors. **Static** memories use static cells that store information in the form of latched currents flowing through transistors. Dynamic memories must be periodically refreshed in order to maintain the stored information. Static memories maintain the stored data without refreshing as long as power is applied. (Both types are volatile – that is, stored information is lost when power is removed.)

The basic storage mechanisms of the cells contribute significantly to the characteristics of the overall memory, but an important contribution is also made by the access method used with a particular cell. Dynamic storage has conventionally been used with dynamic decoding and control circuitry. Similarly, static storage has traditionally used static support circuitry. But those associations are not necessary. Other combinations are possible and provide different overall specifications. One example is provided by Advanced Micro Devices' 4K dynamic memories, the Am9050 and Am9060. They use static circuitry on some input signals in order to significantly improve several timing characteristics. There also exist several types of read-only memories that use dynamic decoding for improved performance.

The Am9130 and Am9140 memories take advantage of a new combination that provides static storage together with a novel type of clocked access method. The storage cells use a conventional, fully static design. The decoding and sensing circuits use a clocked static approach that has no dynamic nodes. The clocked circuitry allows the addition of several new features, increases speed and decreases power dissipation relative to an analogous non-clocked design. At the same time, the usual disadvantages of a clock have been either eliminated or minimized in these new memories.

This philosophy, combined with Advanced N-channel MOS technology, has produced these new combinations of features, including:

- Fully static storage
- Fast access and cycle times
- Low operating power dissipation
- Self-clocking mode of operation
- Single phase, low voltage, low capacitance clock
- Static clock that may be stopped in either state
- Address register on-chip
- Output data register on-chip
- Single +5 volt power supply requirement
- Interface logic levels identical to TTL
- High output drive capability
- Nearly constant power drain; no large current surges
- DC standby mode for reduced power consumption
- Operation over full military temperature range

Interface Considerations

In common with other AMD static R/W RAM's, all of the input and output signals for the Am9130 and Am9140 memories are specified with logic levels identical to those of standard TTL circuits. The worst-case input high and low levels are 2.0V and 0.8V, respectively; the worst-case output high and low levels are 2.4V and 0.4V, respectively. Thus, with TTL interfacing, the normal worst-case noise immunity of at least 400mV is maintained.

All inputs include protection networks designed to prevent damaging accumulations of static charge. During normal operation, the protection circuitry is inactive and may be modeled as a simple series RC. See Figure 3. The first functionally active connection for every input is the gate of an MOS transistor. No active sources or drains are connected to the inputs so that no transient or steady-state currents are impressed on the driving signals other than the simple charging or discharging of the input capacitance, plus the accumulated leakage associated with the protection network and the input gate. Input capacitances are usually around 5pF and leakage currents are usually less than 1μA.

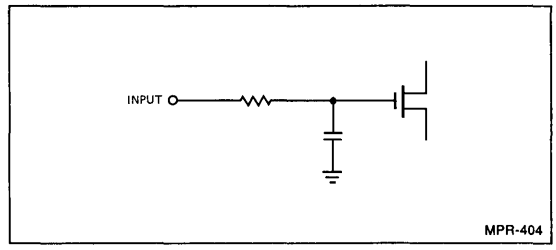


Figure 3. Equivalent Input Circuit.

The output buffers can source at least 200μA worst-case and can sink at least 3.2mA worst-case, while still maintaining TTL output logic levels. Thus, the memories can drive two standard TTL loads or nine standard Low-Power Schottky TTL loads. This unusually high output drive capability allows not only improved fan-out, but also better capacitive drive and noise immunity.

Delays in the output circuits show little variation with changes in the DC loads being driven. Changes with capacitive loading are shown by the curve in Figure 4. Access times are specified for a total load of one TTL gate plus 50pF of capacitance.

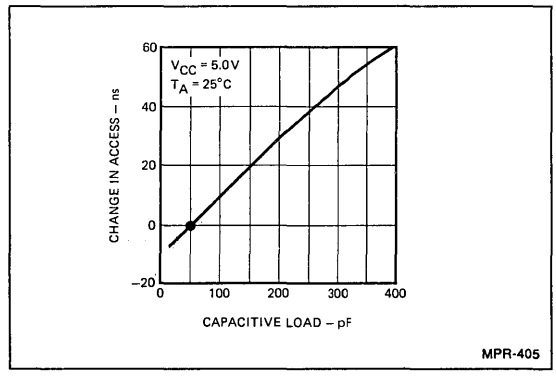


Figure 4. Access Change Versus Load.

Power Supply

The Am9140 and Am9130 memories require only a single supply voltage. They perform their normal operations at a V_{CC} of +5 volts. The commercial temperature range parts have a voltage tolerance of ±5%; the military temperature range tolerance is ±10%. The worst-case current drains are specified in the data sheets at the high side of the voltage tolerance and the low end of the temperature range. In addition, the current

specifications take into account the worst-case distribution of processing parameters that may be encountered during the manufacturing life of the product.

The current drain for these parts is relatively quite constant over their various operating cycles. Since the basic storage mechanism involves latched currents in each cell, there is a necessary cumulative current flowing at all times, even when the memory is not being actively accessed. The average currents specified are largely independent of the CE input state, or the condition of any of the input signals. At the falling edge of the CE clock, there is a brief current surge of an additional 4 to 8mA that occurs as the decoders are being preset.

Dynamic memories usually have quite different current characteristics. Their average power dissipation is proportional to their operating frequency, so that average current drain decreases significantly when they are cycling slowly or doing refresh operations only. There are very large peak currents associated with every cycle in a dynamic memory, no matter how frequently or infrequently the cycles occur. Power supplies and power distribution systems must be capable of handling these peak demands.

Power vs. speed characteristics for the Am9130 and Am9140 4K statics are flat horizontal lines. See Figure 5. A representative 4K dynamic has a rising line as shown. The dynamic dissipation becomes higher than the regular-power static parts out near the high end of the speed range. The cross-over occurs much earlier for the low-power statics.

The power-down mode is entered by simply bringing both CE and OE low and then ramping V_{CC} down as low as 1.5V. Power dissipation will fall by more than 80%. Normal cycles may resume when V_{CC} has been returned to its operating range. See specification sheets for further details.

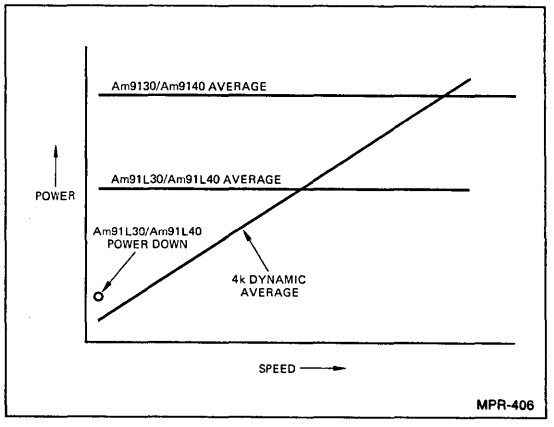


Figure 5. Power Versus Speed Comparisons.

INTERFACE SIGNALS

Signal Flow

Figure 6 is the block diagram for the Am9130 version and shows the interface connections along with the general signal flow. There are ten address lines (A0 through A9) that are used to specify one of 1024 locations, with each location containing four bits. The Chip Select signal acts as a high order address for multiple chip memory configurations. The Chip Enable clock latches the addresses into the address registers and controls the sequences of internal activities.

The row address signals (A0 through A5) and their inversions are distributed to the 64 row address decoders where one of the rows is selected. The 64 cells on the selected row are then connected to their respective bit line columns. Meanwhile, the column address signals (A6 through A9) have been decoded and used to select one of 16 columns for each of the four sense amplifiers. The end result is that one cell is connected to one sense amplifier.

During read operations, the sensed data is latched into the output register and is available for the balance of the operating cycle. During write operations, the write amplifier is turned on and drives the input data onto the sense lines, up the column bit lines and into the selected cells. Input and output data signals share common interface pins.

The output buffers use a three-state design that simplifies external interfacing. Unselected chips have the outputs turned off so that several chips may be wire-ored together easily. The Output Enable and Output Disable signals provide fully asynchronous controls for turning off the output buffers when desired.

Within the storage matrix, there is an extra row of simulated cells. This reference row is selected on every operating cycle in addition to the addressed row and provides internal timing signals that help control the data flow through the part. The Memory Status output signal is derived from the reference row and uses the same designs for its sense and buffer circuits as used by the data bits. Memory Status specifies when output data is available and simplifies generation of Chip Enable.

Figure 7 is the block diagram for the Am9140 version. The basic operation and signal flows are similar to the Am9130. There are two additional address lines (A10, A11), allowing selection of one of 4096 locations. Each location contains one bit so only one set of data I/O circuits are needed. Input and output data signals use separate interface pins.

Chip Enable

The Chip Enable input is a control clock that coordinates all internal activities. All active memory functions are initiated when CE goes high. At the completion of the active operation, CE goes low to preset the memory for the next cycle. There are no restrictions on the maximum times that CE may remain in either state so the clock may be extended or stopped whenever convenient. After power-up and before beginning a valid operation, the clock should be brought low to initially preset the memory.

Figure 8 illustrates a basic operating cycle for either of the memories. The rising edge of CE begins each cycle and strobes the Address and Chip Select signals into the on-chip register. Internal timing signals are derived from CE and from transitions of the address latches and the reference cells. Various control functions are activated by these timing signals as the addresses and data flow through the memory.

When the actual access time of the part has been reached (or a write operation is complete), CE may be switched low if desired. The worst-case time as specified in the data sheet may be used to determine the access. Alternatively, the access or write complete time indicated by the rising edge of the Memory Status output signal may be used. (See the Memory Status section of this Note.) It is perfectly acceptable to leave the CE clock high following the access time; some system operating modes will find it convenient to do so. A Read/Modify/Write cycle, for example, will keep CE high after the access until the modify and write portions of the cycle are finished.

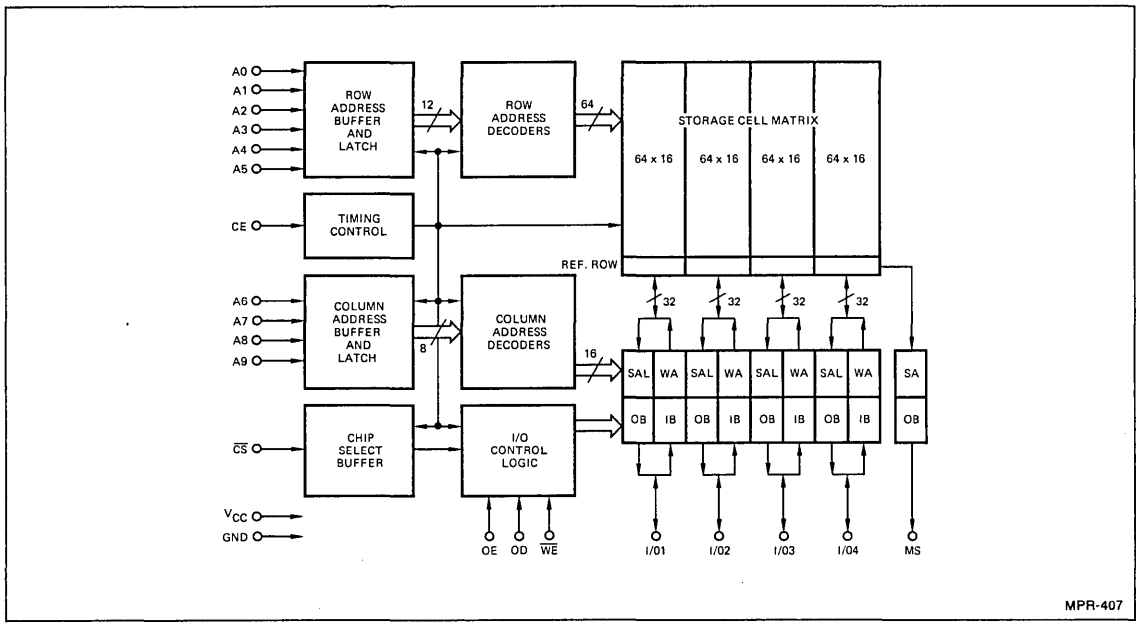


Figure 6. Am9130 Block Diagram.

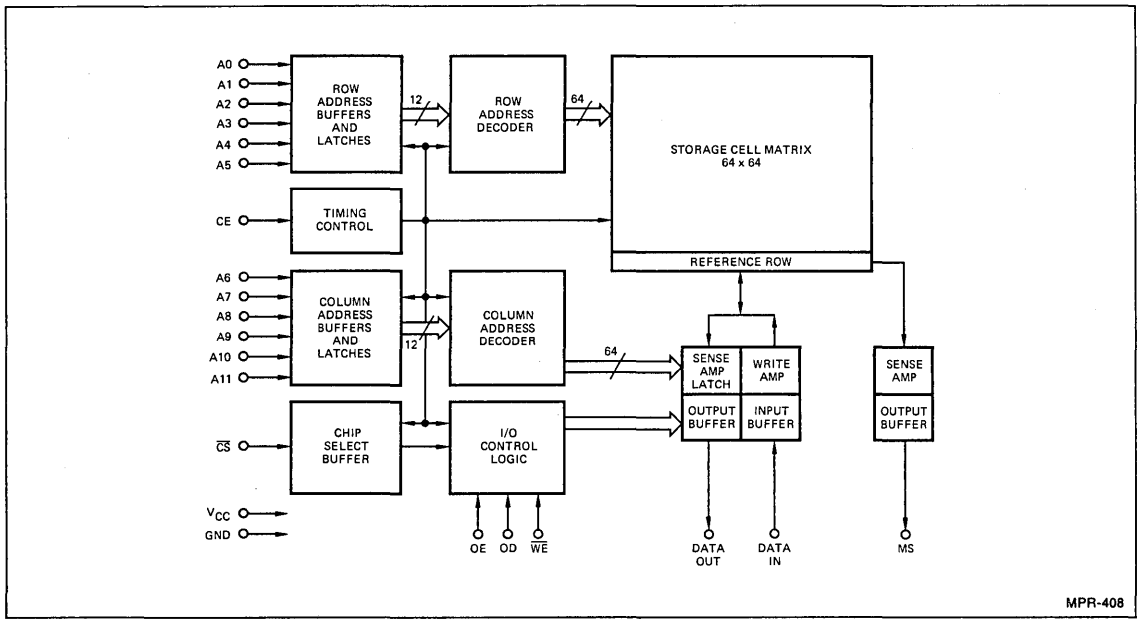


Figure 7. Am9140 Block Diagram.

When CE does go low, the internal preset operation begins. The memory is ready for a new cycle only after the preset is complete. The worst-case CE low time specified in the data sheet may be used to determine the preset interval. Alternatively, the actual preset time is indicated as complete as soon as Memory Status goes low. CE may remain low as long as desired.

Address and Chip Select

The Address inputs are binary coded lines that specify the word location to be accessed within the memory. The Am9130 has 1024 word locations, any one of which may be selected by a ten-bit binary address (2^{10} = 1024). The Am9140 has 4096 locations and so uses a 12-bit address (2^{12} = 4096).

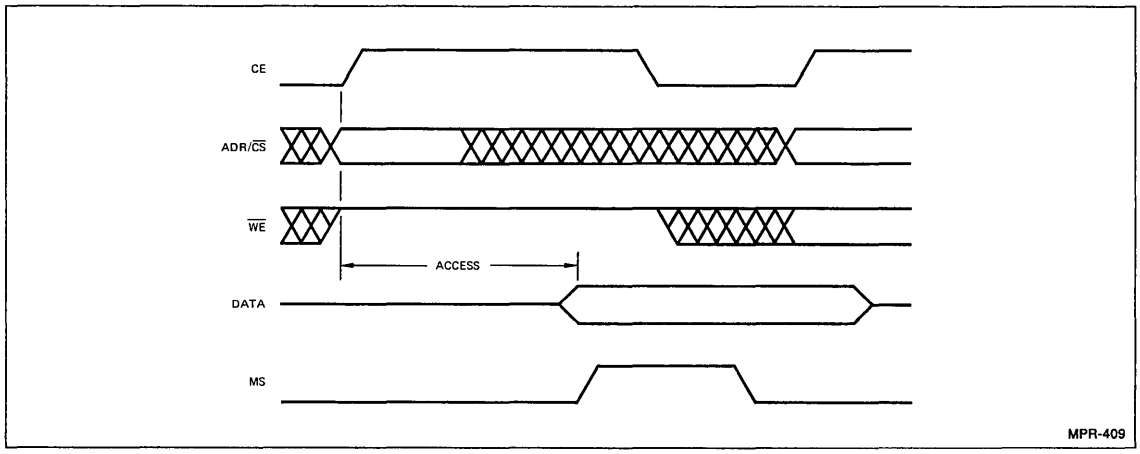


Figure 8. Basic Operating Cycle.

The Address input signals are latched into an on-chip address register by the rising edge of CE. They are allowed to become stable at the same time that the clock goes high: The address set-up time is zero. They must be held stable for the specified minimum time following the CE rising edge in order to be properly loaded into the register. Once the address hold time has been observed, the address inputs are ignored by the memory until the next cycle is initiated.

The Chip Select input acts as a high order address for use when the memory system word capacity is larger than the word capacity of an individual chip. When multiple chips are stacked up, the Address lines may be wired in parallel to all chips and the CS lines used to individually select one active chip, or row of chips, at a time. Chip Select controls the operation of both the output buffers and the write amplifiers. Unselected chips have their output buffers off so that selected chips wired to the same data lines can dominate the output bus. Only selected chips can perform write operations so the Write Enable control signal and the input data lines may be wired in parallel to several chips.

CS is latched into the on-chip register in the same way that Addresses are. This means that once a memory is selected or deselected, it will remain that way until a new cycle with new select information begins. The OE and OD lines provide asynchronous control over the output buffer when that function is necessary on a selected chip.

Chip Select is an active low function – that is, the input signal must be low at the rising edge of CE in order to select the chip. Most CS signals are derived from high order addresses. In small systems, a simple NAND gate can provide the necessary logic. In larger systems, a binary decoder (such as the Am25LS138) works well. In either case, the outputs are active low and thus directly match the input polarity of the Chip Select.

Write Enable

The Write Enable line controls the read or write status of the devices. When the CE clock is low, the WE signal may be any value without affecting the memory. This allows the line to be indeterminant while the using system is deciding what the next cycle will be. WE does not affect the status of the output buffer.

To execute a read cycle, WE is held high while CE is high. To perform a write operation, the WE line is switched low during the cycle. The data sheet for the memories shows the minimum write pulse width required to successfully complete the writing of information into a cell. In many cases, however, it will be convenient to leave the WE line low during the whole cycle so that no intra-cycle timing is necessary for a write operation. The memories are designed so that WE may remain low continuously as long as successive write cycles are being executed.

A write cycle can take place only when three conditions are met: The chip is selected, CE is high, and WE is low. This means that if either CE goes low or WE goes high, the writing is terminated. Thus, the full minimum write pulse width must appear within the CE high time to perform a successful write.

If WE is low when CE goes high to initiate a new cycle, the write amplifier is enabled and the write data propagates onto the data lines internally. However, no columns or rows are selected until after the address for the new cycle is decoded, so actual writing into the cell is delayed by the decoding time following CE. This delay means that the minimum write pulse width cannot apply when WE goes low very early in the cycle.

Data In and Data Out

The specification sheet requirements for incoming data during a write operation show a minimum set-up time with respect to the termination of the write. Termination occurs when either WE goes high or CE goes low. Input data may arrive earlier than the set-up time, where convenient. If incoming data changes during a write operation, the information finally written in the cell will be that stable data preceeding the termination by the set-up time. The data input hold time with respect to the termination of write is zero. If the Am9140 is used with the Data In and Data Out lines remaining separate, the input data may occupy the bus at all times, if desired. The valid written data is then determined by the timing of WE.

If the Am9140 is used with the Data In and Data Out tied together, or if the Am9130 is used, care should be taken to avoid conflict between incoming and outgoing data on the shared lines. It is important to note that when WE is low, it does **not** turn off the output buffers; the potential conflict must be resolved in other ways. One convenient method is

to tie the Output Enable line to the WE line. Then, whenever WE goes low to write, it also turns off the output buffer. After a delay long enough for the output to reach its high impedance state, the input data can be introduced without conflict. The time that WE is low should be long enough to cover the output turn-off delay as well as the input data set-up time.

Since the data being written during a write cycle is impressed on the sense amplifier inputs, the output data will be the same as the input once the write is established. The conflicts occur with old output data that remains from a previous cycle or with new data that may be accessed before the write is established. If the write (and the associated input data) can be initiated while the output buffers are turned off, the conflict is eliminated; even if the outputs turn on, the output data will match the input data.

During a read cycle, once all of the addressing is complete and the cell information has propagated through the sense amplifier, it enters an output data register. The read information can also flow through to the output if the buffer is enabled. As long as CE is high, the addressing remains valid and the output data will be stable. When CE goes low to begin the internal preset operation, the output information is latched into the data register. It will remain latched and stable as long as CE is low.

At the start of every cycle when CE goes high, the output data latch is cleared in preparation for new information to come from the sense amplifier, and the output buffer is turned off. This is done so that in multiple chip systems with the outputs bussed together, old data from one chip will not interfere with new data being accessed on another.

Output Enable and Output Disable

The OE and OD control lines perform the same internal function except that one is inverted from the other. If either OE is low or OD is high, the output buffer will turn off. If the CS input is latched low and OE is high and OD is low, then the output buffer can turn on when data is available.

OE and OD are designed to provide asynchronous control of the output buffer independent of the Chip Select control. This capability makes it easy to tie together the Data In and Data Out lines on the Am9140 where bussed operation is desired, and simplifies operation of the Am9130 which has the Data I/O signals internally tied.

OD and OE will often be used to resolve contention on data busses, but there are other convenient uses as well. The nature of these memories is such that it is easy to individually clock each row in a memory system and to achieve an interleaved mode of operation that effectively shortens the average cycle time. In such designs, the output buffers must be controlled to prevent overlap of read information from two rows that are tied together but clocked at different times.

Memory Status

Memory Status is a new, unique output signal that offers several important features for the memory system designer. It indicates when data is valid at the outputs, when CE may be brought low, and when preset is complete so that a new cycle may begin. The Memory Status signal may be completely ignored without affecting the operation of the memory. On the other hand, it has several implications that make it a potentially interesting and useful signal.

A major function of the MS concept is to indicate actual performance of the memory rather than worst-case performance. Thus, the access time indicated by Memory Status will always be better than the worst-case specification as long as the conditions and assumptions on which the worst-case numbers are predicated are better. Further, real operating results change with changing conditions and Memory Status follows those changes. Thus, for example, as temperature decreases, access time also decreases and MS tracks the change in access exactly.

There are many different ways to use the Memory Status signal and several are illustrated in this Note. Basically it offers improved performance and self-timed operation, along with other related implications.

INTERNAL CIRCUITRY

Address Register

The circuitry for the address register is shown in Figure 9. Inverters K and L isolate the register from the input pin and convert the TTL input levels to the wider logic swings used internally. M inverts the address so that both A and $\overline{A}$ propagate to the inputs of the register.

Transistors 1, 3 5, and 7 are depletion devices. Transistor pairs 1, 2 and 3, 4 form two inverters that are cross-coupled to provide the basic latch. Transistor pairs 5, 6 and 7, 8 are used to enter information into the latch. If point A goes high, then 5 and 6 turn on and 7 and 8 turn off, forcing the latch to one polarity. Notice that the circuit would work without transistors 5 or 7. They are added to minimize the propagation delay through the register.

When transistors 9 and 10 are turned on, 5, 6, 7 and 8 are turned off and the latch is isolated from the input signal. When transistors 11 and 12 are turned on, the outputs from the register are held low and the following address decoders are in their preset state.

The timing for the address register operation is shown in Figure 10. ϕB and ϕC are simply delayed inversions of CE. ϕA is derived from the outputs of the slowest bit position in the address register. During the preset state of the memory when the CE clock is low, both ϕB and ϕC are high and ϕA is low. In that condition, transistors 9, 10, 11 and 12 are all turned on and no signals can travel into or out of the register.

When CE goes high to start a cycle, ϕB goes low after a brief delay. This turns off 9 and 10 and opens a window that allows the address information at the input to proceed into the latch. The path that generates ϕB is slightly longer than the path that the address follows to the register. This is done so that the address setup time relative to CE can be specified as zero.

Next, ϕC also goes low, permitting the latch to set and the register outputs to travel on to the decoders. The delay from ϕB to ϕC prevents any address spiking from disturbing the decoding circuits.

During the preset time, both X5 and $\overline{X5}$ are held low, keeping ϕA low. After the active cycle starts, either X5 or $\overline{X5}$ will make a transition high, depending on the state of the Address 5 input. Thus, ϕA will go high in every memory cycle. When it does, transistors 9 and 10 will turn on again, closing the window into the latch. This prevents any changes in external address information from affecting the stored address. Notice that ϕA is dependent on the presence of address information and only occurs after the address has reached the register outputs.

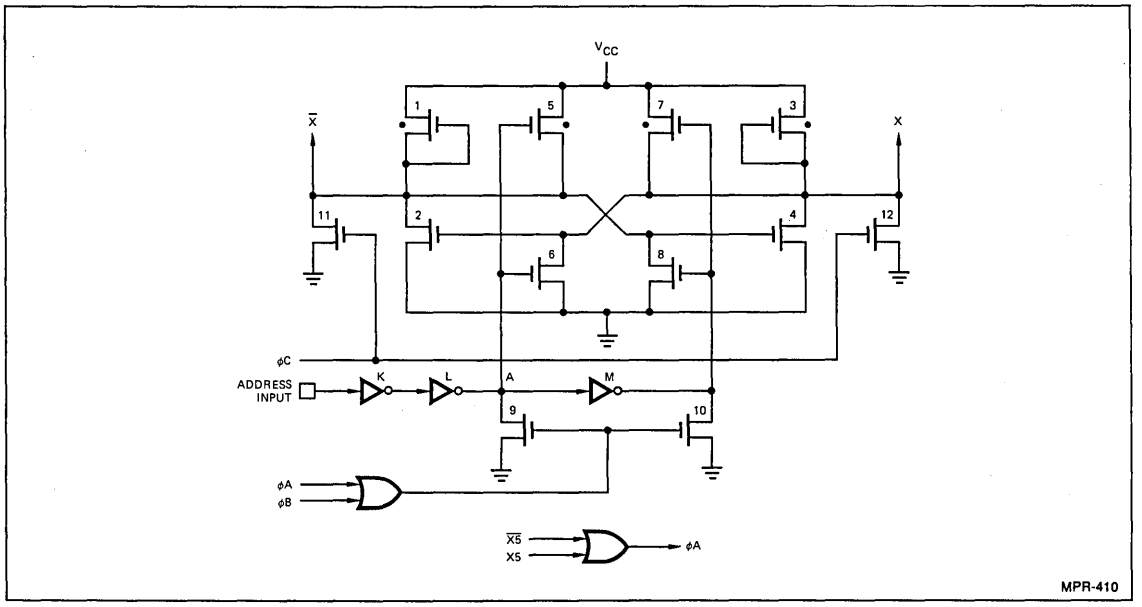


Figure 9. Input Latch Circuit.

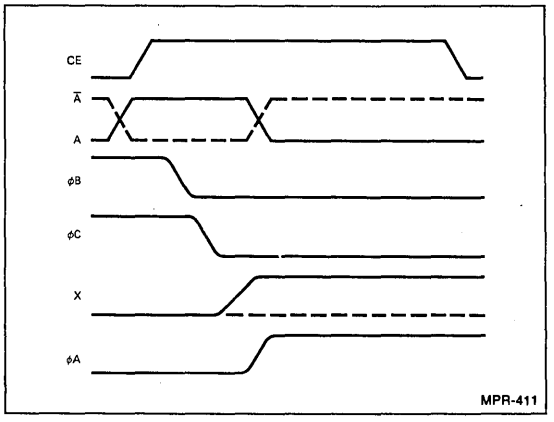


Figure 10. Input Latch Timing.

Address Decoding

There are 64 of the row decoder circuits shown in Figure 11. The decoding is done by a simple six-input gate that is selectively wired to the outputs from the six low order bits of the address register. Each has a unique combination of X and $\overline{X}$ signals on its inputs ($2^6 = 64$). Only one decoder will have all of its inputs low during the decoding. The other 63 gates have at least one input high, thus keeping the decoder output low and the row driver, T, off. The single selected gate allows its row driver to turn on.

ϕA, which is derived from the transitions of the X5 signals, is buffered and used as ϕDEC, the decoder clock. When ϕDEC goes high, it passes through the selected row driver and brings the associated row select line high. All the other row select lines remain low. During the preset time when CE is low, all of the decoders have all of their inputs held low by ϕC, thus enabling all of the row drivers. To keep all the rows unselected, ϕDEC is low during the preset time and keeps all the select lines low.

There is a simple latch connected to each of the 64 select lines. It holds its select line low and prevents it from floating when the row driver is turned off. An active (high) row select line flips and holds the latch in addition to driving the 64 cells in the row.

Memory Cell

The storage cells that are the heart of the memories use a conventional static design with six transistors. See Figure 12. Transistor pairs 1, 5 and 2, 6 are connected as simple inverters that are cross-coupled to form a bistable latch. Either transistor 1 or 2 is turned on and defines the data state of the cell. Transistors 5 and 6 are depletion-mode devices that act as pull-ups and maintain the state of the latch as long as power is applied.

The access devices permit the cell to be attached to its bit lines. When the cell's row select line is low, 3 and 4 are off and the cell is isolated from all other circuitry. When the select line is high, 3 and 4 are on and the cell is connected to the bit lines. If a read operation is in progress, the cell then pulls one of the bit lines low. If a write operation is being performed, the bit lines are driven by the data to be written and the cell is forced into the desired state.

Bit and Data Lines

Figure 13 shows the bit line column and data line organization. A total of 64 cells — one from each row — are connected to one bit line pair to form a column of cells. Columns are connected in parallel through the column select transistors to form the data lines. The data lines feed into a sense amplifier or are fed from the write amplifier. For the Am9140, all 64 columns are connected to one pair of data lines and one set

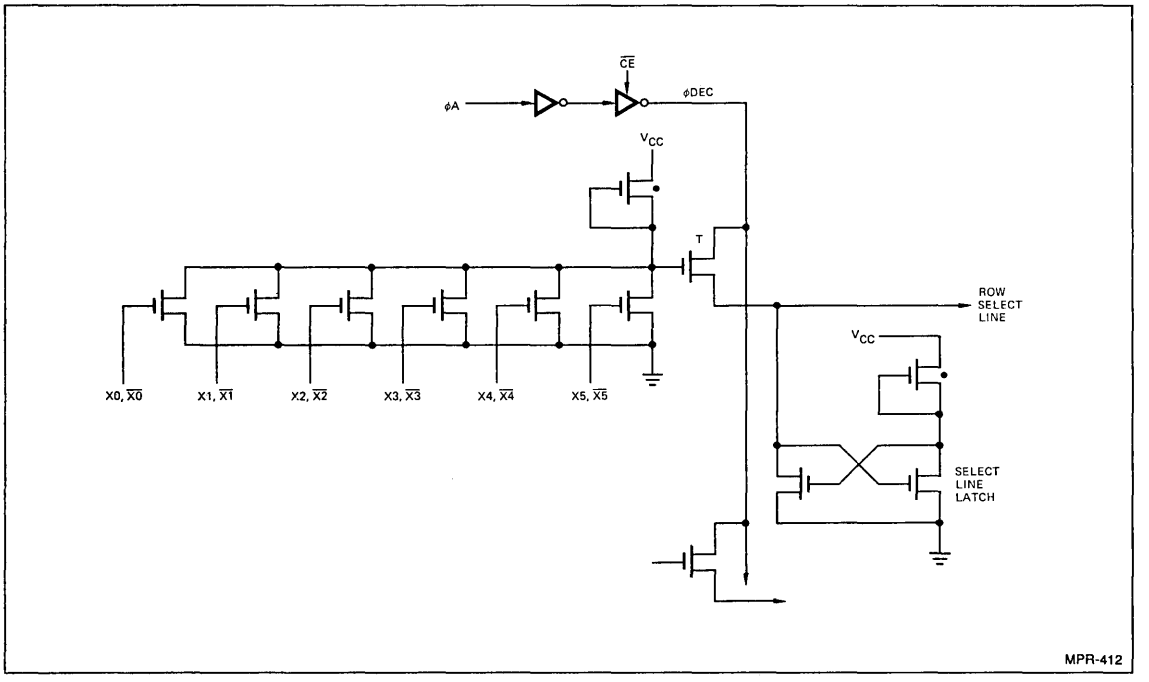


Figure 11. Row Decoder Circuit.

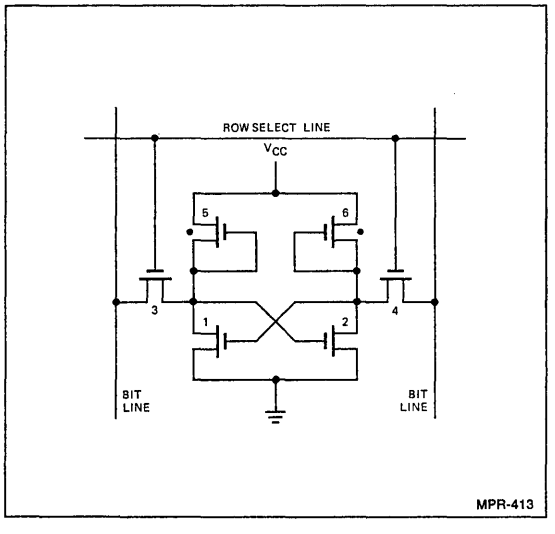


Figure 12. Cell Circuit.

of I/O circuits. For the Am9130, there are four pairs of data lines with four sets of I/O circuits and 16 columns are connected to each pair of data lines.

In addition to the storage cells, each column contains the reference row transistors and two other circuits labeled in the figure as EQ and BLL. The EQ circuit is active only during the preset time when CE is low. It is used to balance and equalize the bit lines and bring them to a voltage level somewhat below V_{CC}. The same EQ circuit is also used with the data lines.

The BLL circuit is a Bit Line Latch that is inactive during preset and is used during the active portion of the cycle to help the selected cell discharge the capacitive load presented by the bit and data lines. It is controlled by ϕL, a timing signal derived from the reference row.

The row driver, T, for the reference row is always enabled and the reference row is therefore selected by ϕDEC on every cycle. The two reference transistors in each column are the same as the access devices in each cell that are driven by the other row select lines. When the reference row select signal has propagated all the way to the end of the row, it is buffered and used to generate ϕL. When ϕL is true, the BLL is enabled and follows the state of the bit lines as set by the selected cell in that column.

The column decoders work much the same way as the row decoders, except that they are not turned on and off by a decode clock. During an active cycle, only one column is connected to one pair of data lines.

Sense Amplifier

A unique feedback amplifier detects the state of the data lines to provide read data for the output. The circuit in Figure 14 shows a simple differential amplifier (transistors 2, 3, 4, 5) with a pedestal voltage established by transistor 1. The output from the differential stage is fed back to influence the pedestal via transistors 6, 7 and 8. Notice that differential signals are balanced out and eliminated from the feedback loop. But supply voltage, temperature and process variations cause common mode shifts that are compensated for.

The output of the differential stage also goes to a latch circuit that squares and buffers the amplified signal. The latch simply follows the data that flows into it and feeds information to the output data register.

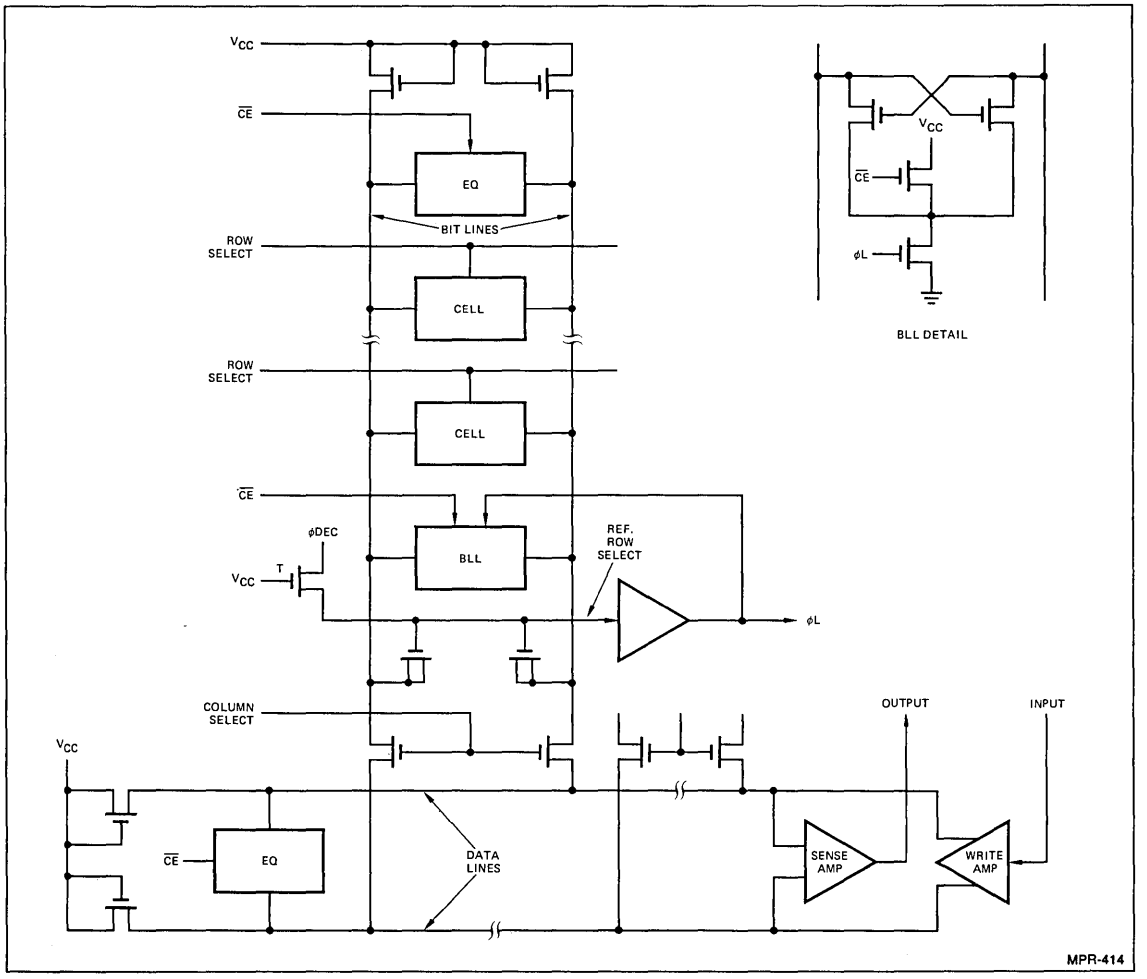


Figure 13. Bit and Data Line Organization.

Data I/O Stages

The output stage shown in Figure 15 includes the output data register plus the output control logic plus the output buffer. Information from the sense amplifier can flow into and through the register and on to the output pin at the access time. As long as the CE clock is high, the cell addressing will be valid and the sense amplifier and output can remain stable. When CE goes low, the register inputs are isolated from the sensed data and the output can stay valid until CE next goes high.

There are several signals that can turn off the output buffer. Only when they are all simultaneously in the necessary state will the output turn on. When CE goes high, the output will turn off until the access time arrives as indicated by ϕL. When $\overline{CS}$ is latched high, the output will be off. When OE is low the outputs will be off. When OD is high the outputs will be off.

The write amplifier control logic only allows a write to take place on a selected chip with the CE high and the Write Enable low. Note that the WE line does not affect the output buffer. On the Am9130, the data input and output signals are tied together and share common interface pins.

Memory Status Circuit

The Memory Status output is derived from the internal ϕL timing signal that is in turn derived from the true performance of the reference row. MS uses the same output buffer, control logic, register and sense amplifier circuitry as used in the data path. Even where a control gating function is absent, the circuitry is included but disabled. At the input to the MS sense circuit, a pseudo data line pair is created that is directly analogous to the storage cell data lines, including the EQ and column select devices. The result is that Memory Status tracks the output data very closely under all operating conditions.

Since the final output circuits are the same for both MS and Data, they respond identically to variations in loading. If the data output is heavily loaded, then similar equivalent loading should be used on the Memory Status output in order to maintain their responses relative to each other.

The MS output is always enabled and never enters a three-state off mode. Even on an unselected chip, the MS signal continues to reflect the status of the memory.

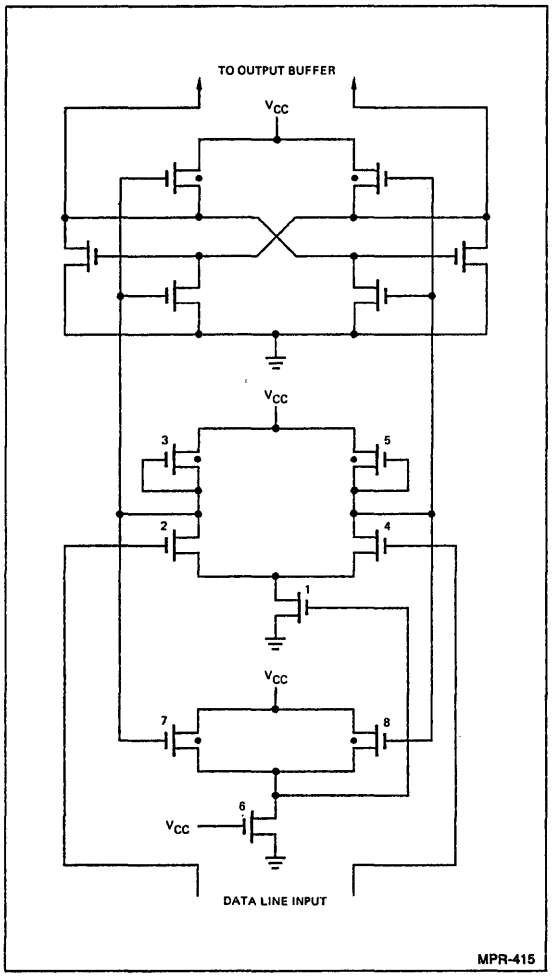


Figure 14. Sense Amplifier Circuit.

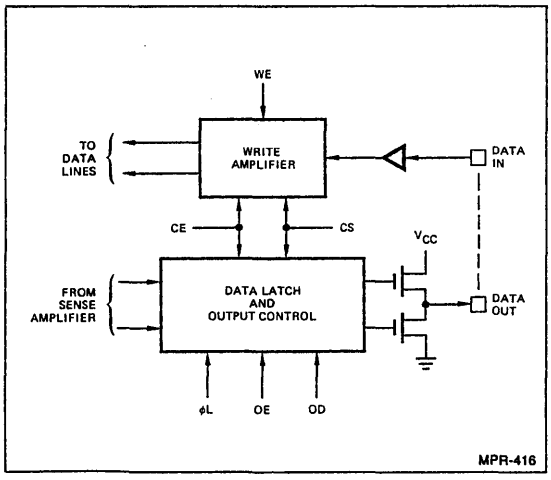


Figure 15. Data I/O Stages.

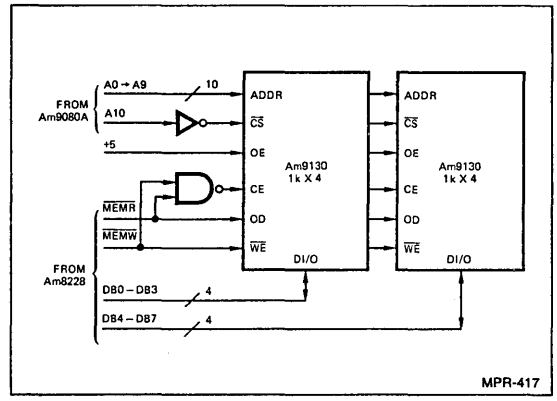


Figure 16. 1k x 8 R/W Memory for Am9080A.

SYSTEM DESIGNS

Interface Timing

The specification sheets for the Am9130 and Am9140 show the various input requirements and output responses for the memories. In each case, the parameters shown are worst-case in order to fully describe the operational limits of the parts. But many system situations allow the timings to be greatly simplified. For example, in small memories that are only one chip deep, the Chip Select signal may not be required and $\overline{CS}$ may be tied low. Similarly, in many instances OD may be tied low or OE may be tied high or both.

In some circumstances, it may be quite convenient to leave the addresses stable longer than the parts require. The falling edge of CE might be used by the associated system to initiate the derivation of a new address and the decision about reading or writing the next cycle. Those signals can then stay stable until the following decision time.

It will quite often be easy to leave the Write Enable line low during all of the CE high time of a write cycle. This eliminates some intra-cycle timing of the write pulse. The WE line may be any value as long as CE is low. Similarly, it will also be easy to have the Data In information available during the time that WE is low — indeed, WE will often be useful as the control line for gating the incoming data on and off.

Many times CE can be easily and directly derived from other signals in the using system. Figure 16 shows an example of a small memory for a microprocessor. Two Am9130 parts form a 1K x 8 memory for an Am9080A. The processor supplies the Addresses and the chip select signals. The Am8228 System Controller associated with the processor supplies the $\overline{MEMR}$ and $\overline{MEMW}$ control lines as well as a buffered data bus. A10 is inverted and used for the Chip Select signal, placing the addressing range in the second 1K of system memory. For larger systems or different configurations, other select logic may be required.

The Controller can request a Memory Read or a Memory Write operation. The NAND gate shown generates a CE when either request is made. When $\overline{MEMR}$ is high, the output buffers are turned off via the OD control. When $\overline{MEMR}$ is true the memory output will be connected to the data bus. When $\overline{MEMW}$ is low, a write operation is performed at the specified address. There is always sufficient time between operation requests for the memory to be fully preset.

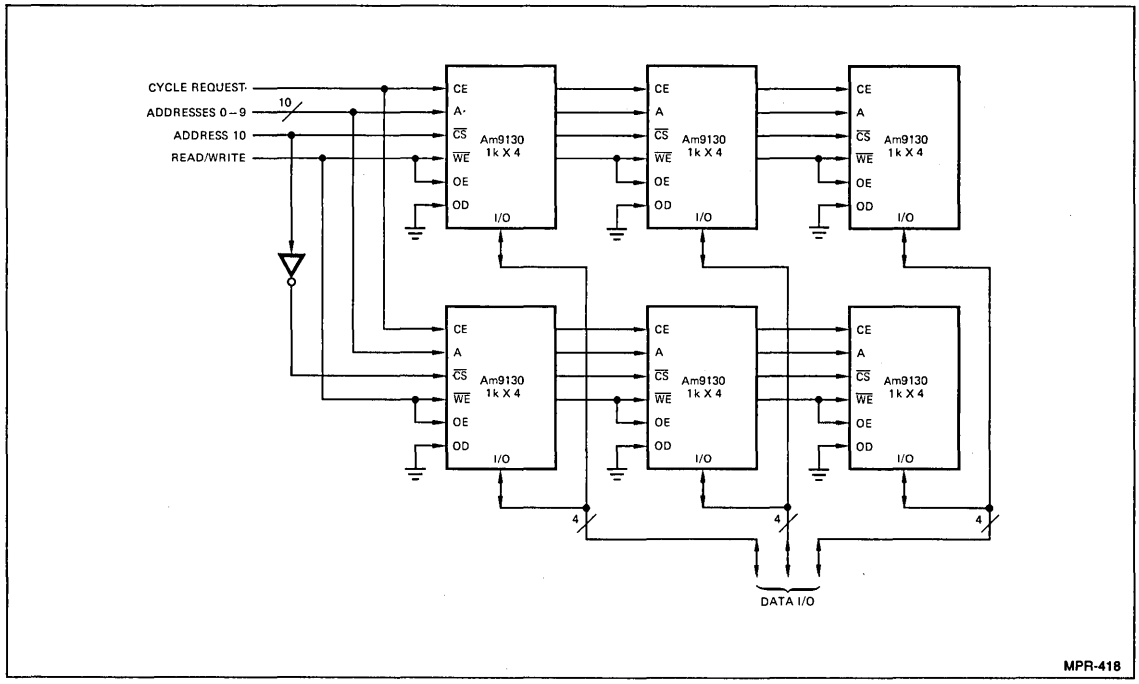


Figure 17. 2k x 12 Memory System.

Small Memory Arrays

As an illustration of a conventional approach for operating multiple chips, Figure 17 shows a convenient way to connect six Am9130 chips to make a 2K x 12 memory. The Chip Enable clock is wired in parallel to all six chips, as are the ten Address lines and the R/W control line. Output Disable is tied to ground, allowing Output Enable to provide asynchronous external control of the output buffer status. OE is tied to Write Enable so that the R/W line turns off the output buffers when it goes low during a write cycle.

Address 10 and its inversion are used to select one of the two rows of chips for each operating cycle. As long as A10 is low, the upper row will respond to the clock and will communicate on the data bus while the lower row is deselected and can neither read nor write. When A10 is high the row roles are reversed.

The Data I/O lines have corresponding bits tied together in vertical columns. The control logic is arranged so that only one of the output buffers at a time will drive an I/O line, and only one chip at a time will write from an I/O line.

The type of memory illustrated is easily expanded to many different capacities. An 8K x 16, for example, could be implemented with 32 Am9140 chips (16 in each row), using the same control line configuration, plus two more address lines.

Driving and buffering limitations for both the inputs and the outputs will be dictated by a) accumulated leakage currents and b) accumulated capacitance. On an address line, for example, many chips may be driven in parallel from a standard TTL output. As the number of chips goes up, the leakage currents in the MOS memory gradually become a significant load for the TTL output especially in the high logic level state. Similarly, many parallel inputs will present a capacitive load that will degrade the rise and fall characteristics of the signal. Added buffering will usually only be necessary when the transition times begin to cause the overall system delays to be excessive.

As the capacity of systems like the one in Figure 17 grows, decoding of the Chip Select information gradually involves a little more logic. If the memory was 3K x 12, for example, it might be implemented with three rows of Am9130 chips. Select information is then needed to assure that only one of the rows at most is active at a time. A one-of-three decoder is easy to implement from two address lines with simple gates as shown in Figure 18. As the number of rows to be selected grows, however, both the wiring and the gate count tend to get much more complex.

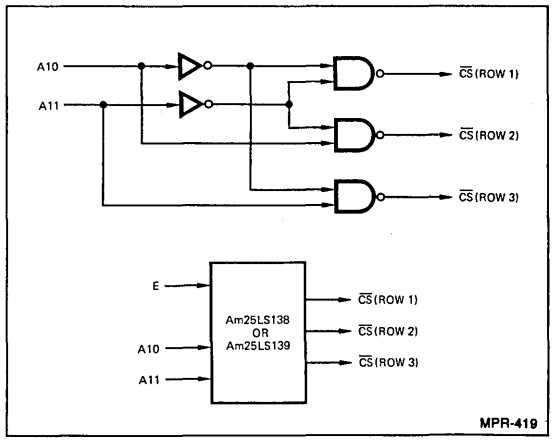


Figure 18. Chip Select Decoding.

Another approach (also shown in the Figure 18) takes advantage of MSI binary decoders like the Am25LS138 or Am25LS139. Both offer package count advantages, especially as the system gets bigger, and control logic is included that permits deselection of all rows. This can be handy for power-down situations and some other circumstances. Notice that the output polarity is such that the decoders interface directly with the memory chips.

The Am9140 can be converted to a common I/O instead of a separate I/O device simply by wiring together the Data In and the Data Out lines. When that is done, the same precautions suggested for the Am9130 concerning bus contention should be observed. Conversion of the Am9130 from common to separate I/O is only slightly more complex. The Am2915 (or Am2905) is a quad three-state bus transceiver. When connected as illustrated in Figure 19, it serves to create the bus needed by the Am9130 from separate input and output data. It even includes convenient registers on both sides. For a circuit without the registers and other control features of the Am2915, try the Am8T26. Both are four bits wide and so match up nicely with a column of Am9130 chips operating in parallel.

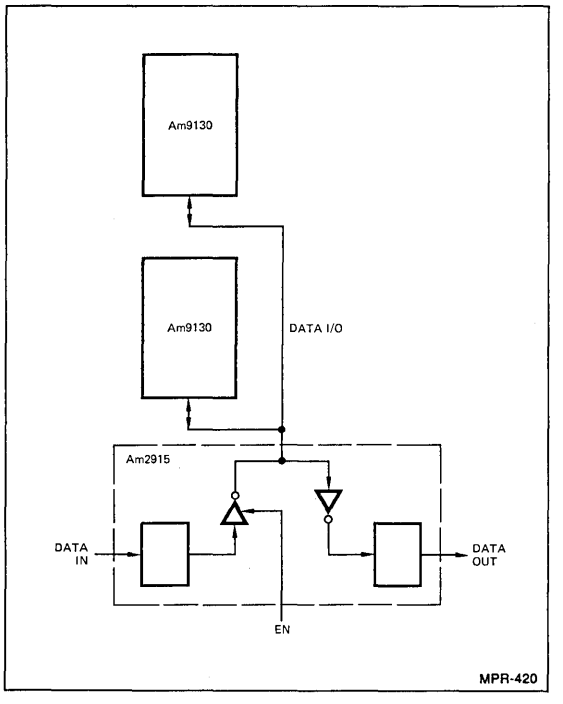


Figure 19.

Memory Status Timing

Figure 20 shows the timing information conveyed by the MS output. The rising edge indicates that output data is valid and makes a convenient strobe for output to the rest of the system. See Figure 20a. When several chips are being used in parallel, the Memory Status signal from the slowest chip should be the strobe in order to assure that all the data bits are available and valid. There is a brief nominal delay from the worst-case output data to the rising edge of MS. That time is always greater then zero under similar loading conditions for the two signals.

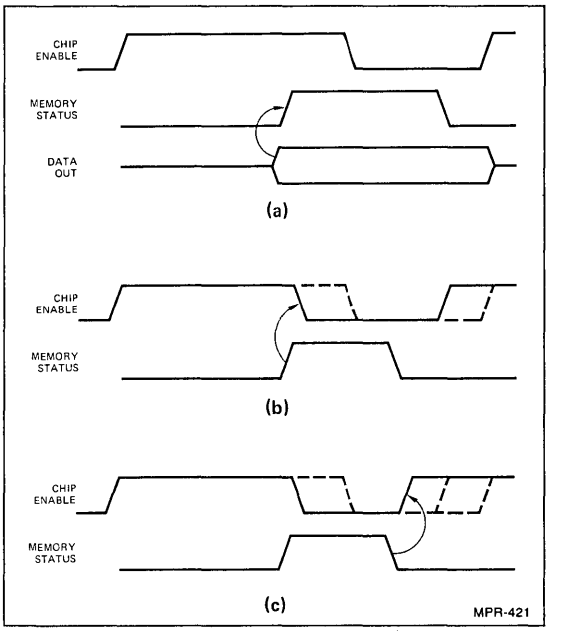


Figure 20. Memory Status Information.

The front edge of MS also specifies the end of the time that CE must be held high for that operation. See Figure 20b. Though CE may be high as long as desired, it may safely go low any time after MS goes high. MS will stay high until the internal preset operation is complete. Thus, it will not go low until some time after CE goes low and the total time that MS is high depends not only on the actual operating conditions of the memory, but also the delay from MS high to CE low.

The falling edge of MS specifies that the memory is ready for a new operation to be initiated. See Figure 20c. When several chips are operated in parallel, the latest falling edge will indicate the earliest time that their CE should go high. The chip with the longest access time will also be the chip with the longest preset time. The picture in Figure 21 shows an MS waveform during a simple read cycle.

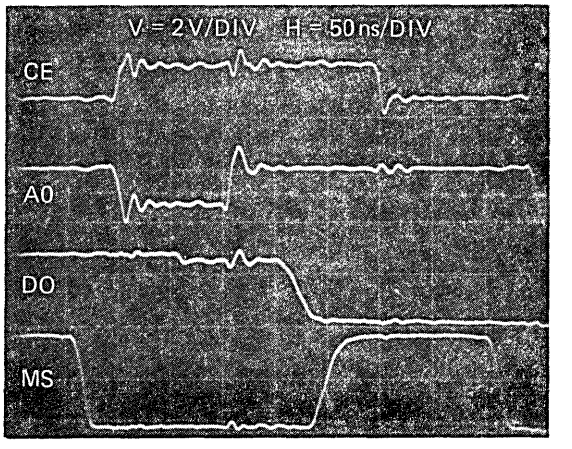


Figure 21. Read Cycle Waveforms.

Memory Status is derived from the selection of the row of reference cells and the reference row is always doing a read operation. Thus, the MS output will appear in every operating cycle, whether a read or a write is being performed. If the Write Enable line is low at the start of the cycle, and if the input data are present at the same time, MS may be considered a valid indication that the write is complete and CE may be switched low. However, if WE is not low or input data are not present until sometime later in the cycle, then the worst-case write timing requirements as shown in the specification sheet must be observed, independent of indications from the rising edge of MS. The falling edge of MS will be fully valid in any type of cycle.

Since the requirements for the two transitions of the Chip Enable clock can be fully specified by the transitions of the Memory Status output, these memories can be effectively self-clocking. The MS output may be inverted and then used as the CE input as shown in Figure 22. Not only will the memory run properly, but it will run at its best frequency for any given set of operating conditions and it will change that frequency as the conditions change. There are many potential capabilities implied by the Memory Status concept, including: adaptive self-timed memories, true asynchronous operations, elimination of support circuit skews, temperature compensation, new memory architectures, improved speed/power ratio, etc.

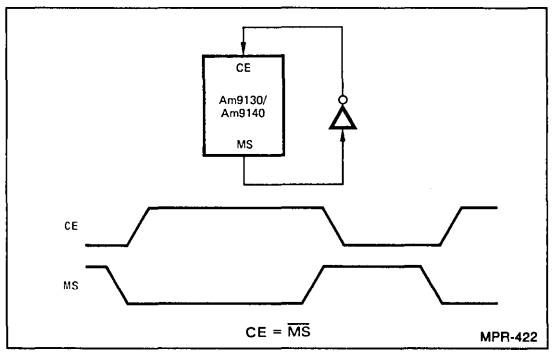


Figure 22. The Self-Clocking Memory.

Memory Status Coordination

Figure 23 shows logic for combining multiple Memory Status signals. Gate A is used to detect when **both** MS outputs are high indicating that output data is available. Similarly, gate B detects that **both** MS outputs are low, indicating that the preset period is complete for both chips. The system associated with the memory can use this information to coordinate the flow and the generation of the CE clock. Essentially, this logic allows the slowest chip to govern the overall memory speed. The inputs to the coordinating logic can of course be expanded to handle as many chips as desired.

To combine these two pieces of status information, a simple cross-coupled latch can be added as shown in Figure 24. Since there are times when neither condition is true, the latch serves to maintain the previous status indication until a new state is valid. The result is a System Status signal that specifies for the system the same information that each MS signal specifies for an individual chip.

The clock may be derived independently for synchronization with the using system. Alternatively, the System Status signal may be inverted and used for the CE clock as indicated by the dotted line. The timing for this arrangement is shown in Figure 25. The memory will free-run at its best speed and the System Status will provide a synchronizing signal for use by the rest of the system.

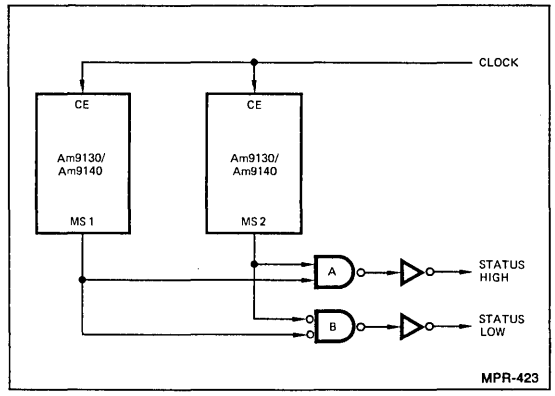


Figure 23. Status Coordination Logic.

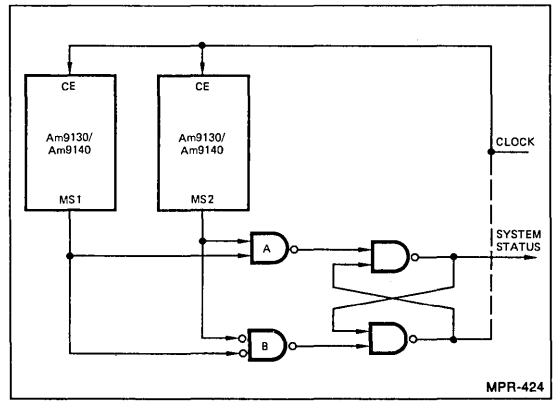


Figure 24. Clock Generation Logic.

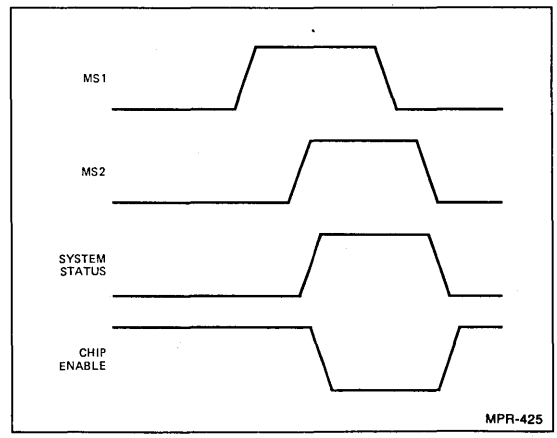


Figure 25. Status Timing.

Handshaking Control

For systems that cannot be memory-driven, some means of controlling the clocking is needed. To permit the memory to single-step, a gate can be inserted in the dotted line of Figure 24 with a control line to turn the clock on or off. A more versatile and more asynchronous approach is illustrated in Figure 26. An additional latch is added to generate the clock so that the status information is derived independent of the clock control.

When the Cycle Request input is low, the memory will preset and prepare for an active cycle. When all is ready, Status Acknowledge will go low. When CR goes high, the memory will execute a cycle and will acknowledge conditions of access by bringing SA high. CR and SA then form a simple asynchronous handshaking pair for memory control. Notice that CR may go high at any time to start a cycle. If the chips are ready (SA low), the clock will proceed, but if preset is not complete (SA high) the memory will wait before initiating the requested cycle.

The timing for CR is quite simple. It should be held high until SA goes low. If SA is already low, a narrow CR pulse will suffice. Thus, a brief Cycle Request will cause the memory to execute one complete cycle and stop. If CR is held high, the memory will access (SA goes high) and then will leave the clock high until CR goes low. This allows Read/Modify/Write operations to be performed quite easily.

Advanced Micro Devices has designed a Low-Power Schottky support circuit for use with these memories. It integrates all of the logic for coordinating several Memory Status signals and for controlling the CE clock. It uses the same basic approach as shown here. Please contact the factory for details.

Interleaved Operation

With the clock derived locally within the memory from the MS signals, and with the clocking logic integrated on a single chip, it becomes convenient to individually clock each row of a memory system. An example configuration is shown in Figure 27, with each support logic block being similar to the circuitry previously discussed. Each row is clocked only when it is addressed by the Chip Select signal (A0 or $\overline{A0}$). Unselected rows wait in their preset state until they are selected and clocked. The Cycle Request input is steered to the selected row by added logic. The Status Acknowledge outputs are three-state and only the SA for the selected row is turned on. The selected row will proceed when its preset is complete. When the data from the requested operation is available, the Status Acknowledge output goes high. The using system can then request another operation immediately once a new address is ready.

Independent clocking of each row adds little support circuit complexity while providing increased overall performance in two ways. First, the speed of each access is limited only by the slowest device in the selected row rather than the slowest device in the whole array. Secondly, successive operations in different rows will be faster because the wait for preset is eliminated; one row will preset while another is being accessed. Notice that the low order bit is used as the Chip Select address. In many systems, this will improve the distribution of alternate accesses for sequential information by mapping even addresses in one row and odd addresses in the other.

In any event, no matter where the operation is addressed or when it is requested, the memory will respond in the best possible time. The Cycle Request and Status Acknowledge signals form a true asynchronous handshaking pair. All of the variations in performance caused by the timing of the request, the row addressing patterns, the speeds of the individual chips and the memory operating conditions are automatically reflected in the response of the Acknowledge signal. An interesting challenge will be to design using systems that can take advantage of this unusual capability.

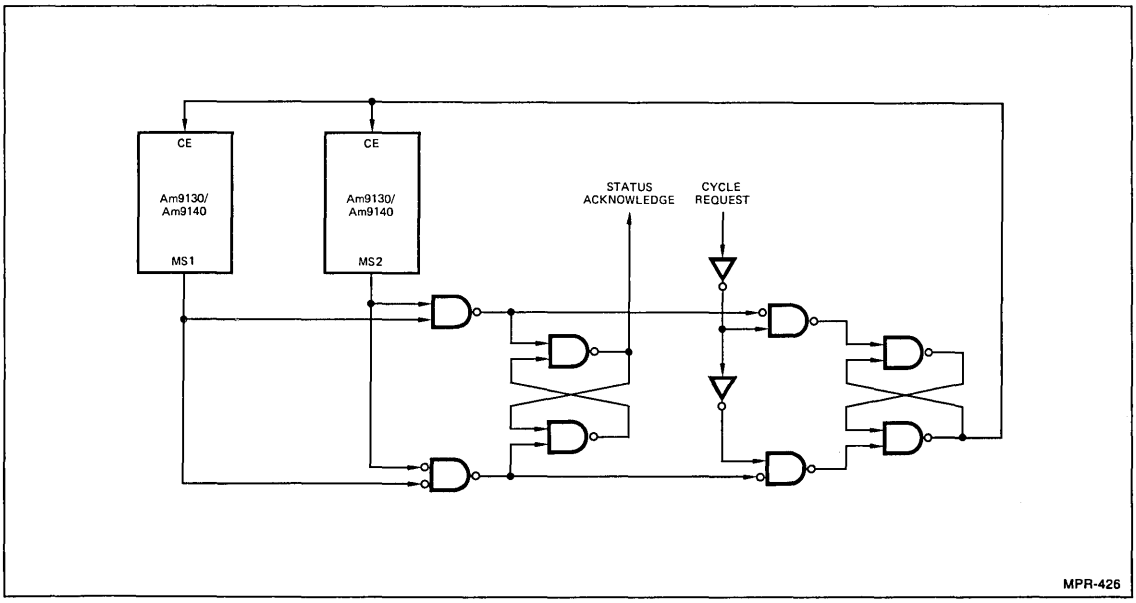


Figure 26. Handshaking Control.

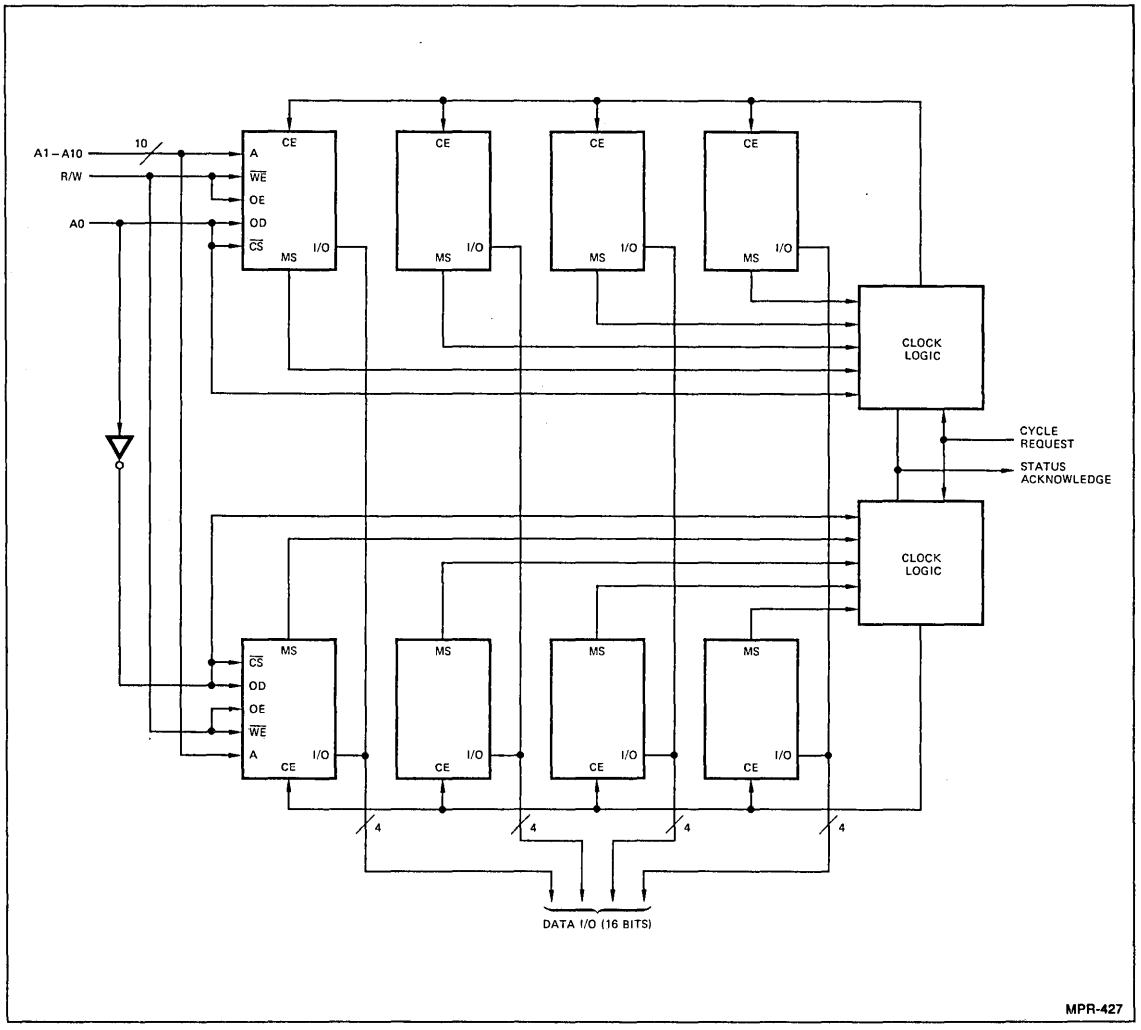


Figure 27. 2k x 16 Interleaved Memory System.

Am2900 Family Applications Literature

The Microprogramming Handbook	A 44-page book providing examples of the design of microprogram control systems and an explanation of the techniques used in programming these machines. Order AM-PUB029 Price $5.00
A 16-Bit Microprogrammed Computer	The complete design of a 16-Bit Minicomputer covering specification, management, architecture, and detailed design of the ALU, Memory, DMA channel, interrupt system, and control unit. 48 pages. Order AM-PUB030 Price $5.00
A High Performance Disc Controller	This book covers the detailed design of a controller. Specifically it is an interface between a Pertec disc and a DEC PDP-11® minicomputer. Most controllers will be architecturally similar. Includes schematics and microcode. Order AM-PUB065 Price $5.00
An Emulation of the Am9080A	This book describes a 2900 based system which executes instructions of the Am9080A MOS microprocessor. It operates about 4 times faster than the Am9080A and leaves space for user defined instructions in addition to the standard instruction set. Order AM-PUB064 Price $5.00
Microprogram Design with the Am2900 Family	A discussion of the "instruction-cracking" problem in microprogrammed machines. Discusses ways to translate op codes into microprogram addresses and control lines. Order AM-PUB069 Free
The Microprogramming Card	This pocket sized card gives the block diagrams, pin-outs, and instruction sets for most Am2900 products. Also includes AMDASM summary. Order AM-PUB068 Free

Advanced Micro Devices Commitment to Excellence

Product Assurance Programs for Military and Commercial Integrated Circuits

Am-PUBO66

APPENDIX A

A COMMITMENT TO EXCELLENCE

Advanced Micro Devices was conceived on the premise that there was a place in the semiconductor community for a manufacturer dedicated to excellence.

In product assurance procedures, Advanced Micro Devices is unique. Only Advanced Micro Devices processes all integrated circuits, commercial as well as military, to the demanding requirements of MIL-STD-883. The Rome Air Development Center (RADC), which is the Air Force's principal authority on component reliability, has issued MIL-HDBK-217B which indicates that parts processed to Military Standard 883, Level C (Advanced Micro Devices' standard processing) yield a product nearly ten times better in failure rates than the industry commercial average.

Our Sunnyvale facility has been certified by the Defense Electronics Supply Center (DESC) to produce parts to JAN Class B and C under Military Specification MIL-M-38510. The National Aeronautics and Space Administration (NASA) has certified this production line for the manufacture of Class A products for programs requiring the highest levels of reliability. Advanced Micro Devices is the only integrated circuit company formed within the last ten years to achieve such line certification.

This brochure outlines Advanced Micro Devices' standard programs for Class B, C and A devices for military and commercial operating range applications. These will cover the majority of system requirements today. Alternative screening flows for specific user needs can be performed on request. Check with your local sales office for further information.

ADVANCED MICRO DEVICES' STANDARD PRODUCTS ARE MANUFACTURED TO MIL-STD-883 REQUIREMENTS

Advanced Micro Devices' product assurance programs are based on two key documents.

MIL-M-38510 – General Specification for Microcircuits

MIL-STD-883 – Test Methods and Procedures for Microelectronics

The screening charts in this brochure show that every integrated circuit shipped by Advanced Micro Devices receives the critical screening procedures defined in MIL-STD-883, Method 5004 for Class C product. This includes molded plastic devices.

In addition, documentation, design, processing and assembly workmanship guidelines are patterned after MIL-M-38510 specifications.

Commercial and industrial users receive the quality and reliability benefits of this aerospace-type screening and documentation at no additional cost.

STANDARD PRODUCT TESTING CATEGORIES

Advanced Micro Devices offers integrated circuits to four standard testing categories.

1. Commercial operating range product (typically 0°C to 70°C)
2. Commercial product with 100% temperature testing
3. Military operating range product (typically −55°C to +125°C)
4. JAN qualified product

Categories 1, 2 and 3 are available on most Advanced Micro Devices circuits. Category 4 is offered on a more limited line. Check with your local sales office for details.

STANDARD PRODUCT ASSURANCE CATEGORIES

Devices produced to the above testing categories are available to the three standard classes of product assurance defined by MIL-STD-883. As a minimum, every device shipped by Advanced Micro Devices meets the screening requirements of Class C.

Class C – For commercial and ground-based military systems where replacement can be accomplished without difficulty.

According to MIL-HDBK-217B, this assures relative failure rates 9.4 times better than that of regular industry commercial product.

Class B – For flight applications and commercial systems where maintenance is difficult or expensive and where reliablity is vital.

Devices are upgraded from Class C to Class B by burn-in screening and additional testing.

According to MIL-HDBK-217B, Class B failure rate is improved 30 times over regular industry commercial product. Advanced Micro Devices Class B processing conforms to MIL-STD-883 requirements. MIL-HDBK-217B indicates that this may provide failure rates as much as two times better than some other manufacturers' "equivalent" or "pseudo" Class B programs.

Class S – For space applications where replacement is extremely difficult or impossible and reliability is imperative.

Class S screening includes x-ray and other special inspections tailored to the specific requirements of the user.

The 100% screening and quality conformance testing performed within these Advanced Micro Devices programs is shown in TABLES I, II and III. A full description of the process flow is provided in Product Assurance Document 15-010, available on request.

CLASS C SCREENING FLOW
FOR COMMERCIAL SYSTEMS AND GROUND BASED MILITARY SYSTEMS

TABLE I
CLASS C
INTEGRATED CIRCUITS

Screening Procedure per MIL-STD-883 Method 5004, Class C		COMMERCIAL OPERATING RANGE		MILITARY OPERATING RANGE	
		HERMETIC AND MOLDED PACKAGES		HERMETIC PACKAGE ONLY	
Screen	Test Method	C1 Commercial Product	C2 Commercial Product With 100% Temperature Testing	C3 Military Product	C4 Jan Qualified Product
VISUAL AND MECHANICAL					
Internal visual	2010, Condition B	100%	100%	100%	100%
High temperature storage	1008, Condition C, 24 hours	100%	100%	100%	100%
Temperature cycle	1010, Condition C	100%	100%	100%	100%
Constant acceleration	2001	100% (1)	100% (1)	100%	100%
Hermeticity, Fine and Gross	1014	100% (1)	100% (1)	100%	100%
FINAL ELECTRICAL TESTS		AMD Data Sheet	AMD Data Sheet	AMD Data Sheet	38510 Slash Sheet
Static (dc)	a) At 25°C, and power supply extremes	100%	100%	100%	100%
	b) At temperature and power supply extremes	(2)	100% (3)	–	–
Functional	a) At 25°C, and power supply extremes	100%	100%	100%	100%
	b) At temperature and power supply extremes	(2)	100% (3)	–	–
Switching (ac) or Dynamic	At 25°C, nominal power supply	(2)	(2)	–	–
QUALITY CONFORMANCE	5005, Group A (See Table II)	Sample	Sample	Sample	Sample
Sample Tests	Group B	–	–	–	Sample
	Group C	–	–	–	Sample
	Group D	–	–	–	Sample
EXTERNAL VISUAL	2009 (Note 5)	100%	100%	100%	100%

TABLE II
GROUP A QUALITY CONFORMANCE LEVELS

Advanced Micro Devices employs the military-recommended LTPD sampling system to assure quality. MIL-STD-883, Method 5005, TABLE I, Group A, subgroups 1 through 9 as appropriate to the device family are performed on every lot. Quality levels defined for Class B product are applied by Advanced Micro Devices to both Class B and Class C orders.

	LTPD	INITIAL SAMPLE SIZE
Subgroup 1 – Static tests at 25°C	5	45
Subgroup 2 – Static tests at maximum rated operating temperature	7	32
Subgroup 3 – Static tests at minimum rated operating temperature	7	32
Subgroup 4 – Dynamic tests at 25°C – LINEAR devices	5	45
Subgroup 5 – Dynamic tests at maximum rated operating temperature – LINEAR devices	7	32
Subgroup 6 – Dynamic tests at minimum rated operating temperature – LINEAR devices	7	32
Subgroup 7 – Functional tests at 25°C	5	45
Subgroup 8 – Functional tests at maximum and minimum rated operating temperatures	10	22
Subgroup 9 – Switching tests at 25°C – DIGITAL devices	7	32
Subgroup 10 – Switching tests at maximum rated operating temperatures – DIGITAL devices	*	
Subgroup 11 – Switching tests at minimum rated operating temperatures – DIGITAL devices	*	

*These subgroups, where applicable, are usually performed during initial characterization only for all except JAN Qualified product.

CLASS B SCREENING FLOW
FOR HIGH RELIABILITY COMMERCIAL AND MILITARY SYSTEMS

TABLE III
CLASS B
INTEGRATED CIRCUITS
(Class C plus burn in screening and additional testing.)

Screening Procedure per MIL-STD-883 Method 5004, Class B		COMMERCIAL OPERATING RANGE		MILITARY OPERATING RANGE	
		HERMETIC AND MOLDED PACKAGES		HERMETIC PACKAGE ONLY	
Screen	Test Method	B1 Commercial Product	B2 Commercial Product With 100% Temperature Testing	B3 Military Product	B4 Jan Qualified Product
VISUAL AND MECHANICAL					
Internal visual	2010, Condition B	100%	100%	100%	100%
High temperature storage	1008, Condition C, 24 hours	100%	100%	100%	100%
Temperature cycle	1010, Condition C	100%	100%	100%	100%
Constant acceleration	2001	100% (1)	100% (1)	100%	100%
Hermeticity, Fine and Gross	1014	100% (1)	100% (1)	100%	100%
BURN IN					
Interim (pre burn in) electricals	Per applicable device specification	100%	100%	100%	100%
Burn in	1015, 160 hours at 125°C or equivalent.	100%	100%	100%	100%
FINAL ELECTRICAL TESTS		AMD Data Sheet	AMD Data Sheet	AMD Data Sheet	38510 Slash Sheet
Static (dc)	a) At 25°C, and power supply extremes	100%	100%	100%	100%
	b) At temperature and power supply extremes	(2)	100% (3)	100%	100%
Functional	a) At 25°C, and power supply extremes	100%	100%	100%	100%
	b) At temperature and power supply extremes	(2)	100% (3)	100%	100%
Switching (ac) or Dynamic	At 25°C, nominal power supply	(2)	(2)	100%	100%
QUALITY CONFORMANCE	5005, Group A (See Table II)	Sample	Sample	Sample	Sample
Sample Tests	Group B	–	–	(4)	Sample
	Group C	–	–	(4)	Sample
	Group D	–	–	(4)	Sample
EXTERNAL VISUAL	2009 (Note 5)	100%	100%	100%	100%

Notes: 1. Not applicable to molded packages.
2. All MOS RAMs and many other MOS devices receive a.c. testing and 100% d.c. screening at high temperature and power supply extremes as standard. Other products sampled at Group A (Table III).
3. Tested at high temperature, 100°C, only on commercial range product. Note that this is a full d.c. check of all parameters in addition to the simple "hot-rail" functional sequence performed on most other commercial programs.
4. Available to special order.
5. Without optical aid for commercial devices.

CLASS S
FOR AEROSPACE SYSTEMS. (FORMERLY CLASS A)

Advanced Micro Devices offers a Class S program based on screening defined in MIL-STD-883, Method 5004.

This program together with other high reliability screening options, such as SEM and x-ray, is described as Option A in Advanced Micro Devices' Extended Processing Options Document 00-003. Contact your local Advanced Micro Devices sales office for more information.

STANDARD PRODUCT
SCREENING SUMMARY AND ORDERING INFORMATION

1. COMMERCIAL PRODUCT

- Screened per MIL-STD-883, Method 5004.
- Electrically tested per AMD Data Sheet.
- Supplied in hermetic and molded packages.
- Quality conformance testing, Method 5005, Group A, performed to levels specified for Class B on both Class C and Class B options.

Class C (Flow C1)

- Order standard AMD part number.
- Marked same as order number.

  Example: Am2901ADC

Class B (Flow B1)

- Burn in performed in AMD circuit condition.
- Order standard AMD part number, add suffix B (or /883B for 1, 2 and 300 Series Linear devices).
- Marked same as order number.

  Example: Am2901ADC-B

2. COMMERCIAL PRODUCT WITH 100% TEMPERATURE TESTING

- Identical to standard commercial operating range product with the addition of 100% dc and functional testing at 100°C and power supply extremes.

Class C (Flow C2)

- Order standard AMD part number, add suffix T.
- Marked same as order number.

  Example: Am2901ADC-T

Class B (Flow B2)

- Burn in performed in AMD circuit condition.
- Order standard AMD part number, add suffix TB.
- Marked same as order number.

  Example: Am2901ADC-TB

3. MILITARY PRODUCT

- Screened per MIL-STD-883, Method 5004.
- Electrically tested per AMD Data Sheet.
- Supplied in hermetic package only.
- Quality conformance testing, Method 5005, Group A, performed to levels specified for Class B on both Class B and Class C options.

Class C (Flow C3)

- Order standard AMD part number.
- Marked same as order number.

  Example: Am2901ADM

Class B (Flow B3)

- Burn in performed in AMD circuit condition.
- AC at 25°C, dc and functional testing at 25°C as well as temperature and power supply extremes performed on 100% of every lot.
- Quality conformance testing, Method 5005, Groups B, C and D available to special order.
- Order standard AMD part number, add suffix B.
- Marked same as order number.

  Example: Am2901ADM-B

4. JAN QUALIFIED PRODUCT

- Screened per MIL-STD-883, Method 5004.
- Electrically tested to JAN detail specification (slash sheet).
- Manufactured in Defense Logistics Agency certified facility.
- Quality conformance testing, Method 5005, Groups A, B, C and D performed as standard and must be completed prior to shipment.
- It is a product for which AMD has gained QPL listing.*

Class C (Flow C4)

- Order per military document.
- Marked per military document.

  Example: JM38510/44001CQB

Class B (Flow B4)

- Burn in performed in circuit condition approved for JAN devices.
- Order per military document.
- Marked per military document.

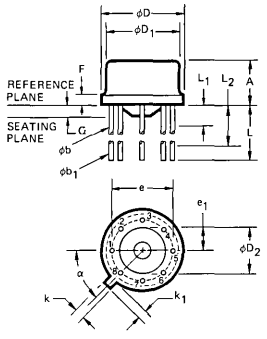
  Example: JM38510/44001BRC

*In certain cases where JAN Qualified product is specified but is not available, Advanced Micro Devices can provide devices to the electrical limits and burn-in criteria of the slash sheet. This class of product has been called JAN Equivalent and marked M38510/ by some manufacturers. This identification is no longer permitted by DESC. Check with your local sales office for availability of specific device types.

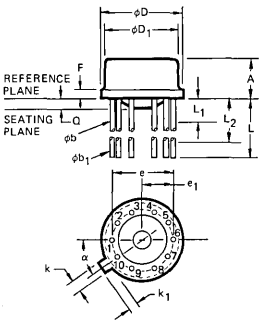
PACKAGE OUTLINES

METAL CAN PACKAGES

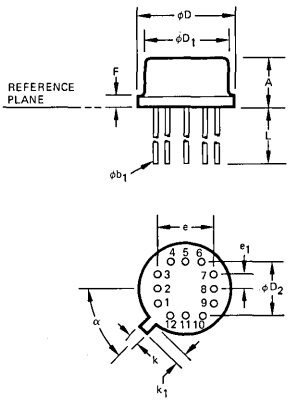
H-8-1



H-10-1



G-12-1



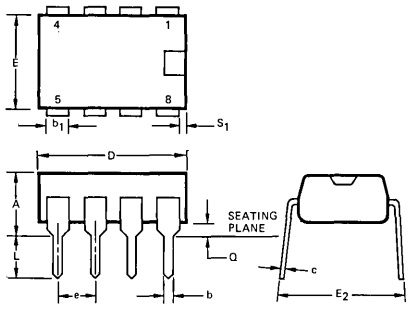
AMD Pkg.	H-8-1		H-10-1		G-12-1	
Common Name	TO-99 Metal Can		TO-100 Metal Can		TO-8 Metal Can	
38510 Appendix C	A-1		A-2		–	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.
A	.165	.185	.165	.185	.155	.180
e	.185	.215	.215	.245	.390	.410
e_1	.090	.110	.105	.125	.090	.110
F	.013	.033	.013	.033	.020	.030
k	.027	.034	.027	.034	.024	.034
k_1	.027	.045	.027	.045	.024	.038
L	.500	.570	.500	.610	.500	.600
L_1		.050		.050		
L_2	.250		.250			
α	45° BSC		36° BSC		45°	
ϕb	.016	.019	.016	.019		
ϕb_1	.016	.021	.016	.021	.016	.021
ϕD	.350	.370	.350	.370	.590	.610
ϕD_1	.305	.335	.305	.335	.540	.560
ϕD_2	.120	.160	.120	.160	.390	.410
Q	.015	.045	.015	.045		

Notes: 1. Standard lead finish is bright acid tin plate or gold plate.
2. ϕb applies between L_1 and L_2. ϕb_1 applies between L_1 and 0.500" beyond reference plane.

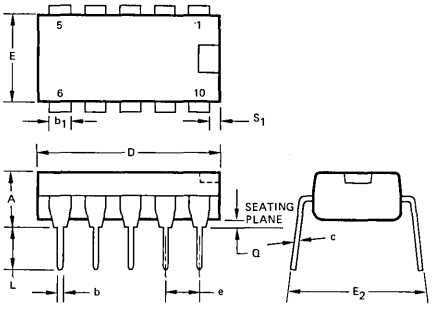
PACKAGE OUTLINES (Cont.)

MOLDED DUAL IN-LINE PACKAGES

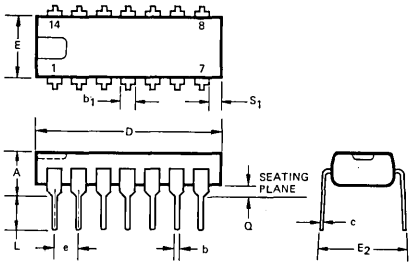
P-8-1



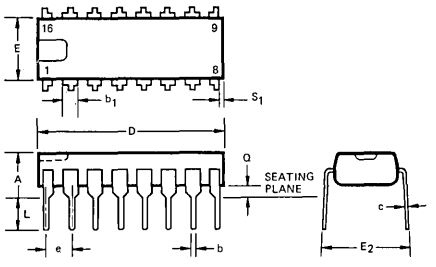
P-10-1



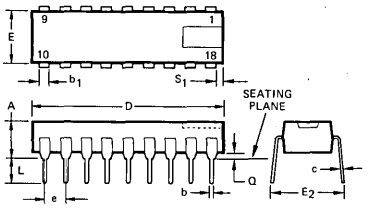
P-14-1



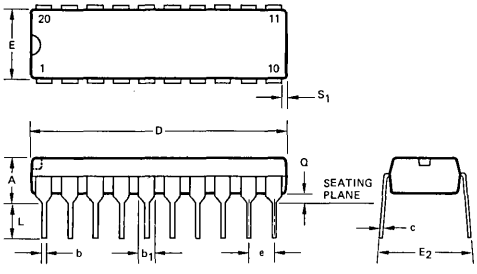
P-16-1



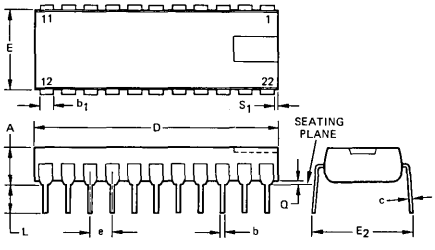
P-18-1



P-20-1



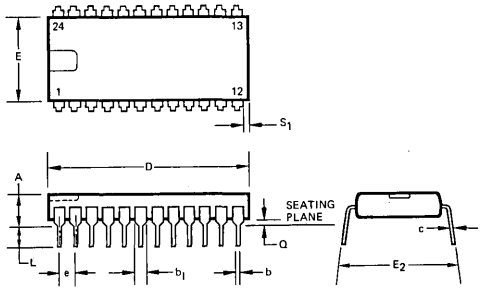
P-22-1



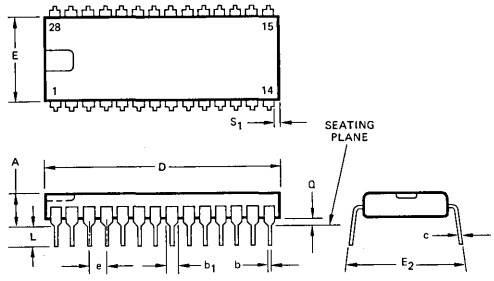
PACKAGE OUTLINES (Cont.)

MOLDED DUAL IN-LINE PACKAGES (Cont.)

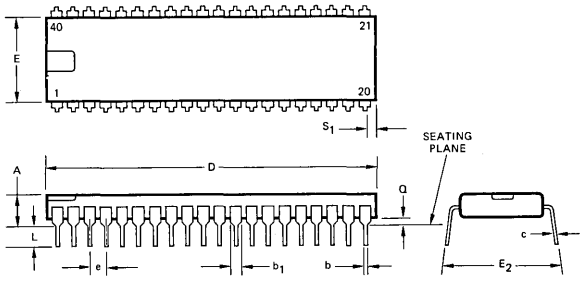
P-24-1



P-28-1



P-40-1



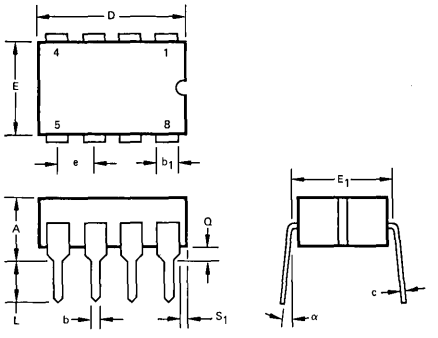
AMD Pkg.	P-8-1		P-10-1		P-14-1		P-16-1		P-18-1		P-20-1		P-22-1		P-24-1		P-28-1		P-40-1	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.150	.200	.150	.200	.150	.200	.150	.200	.150	.200	.150	.200	.150	.200	.170	.215	.150	.200	.150	.200
b	.015	.022	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020	.015	.020
b_1	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065	.055	.065
c	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011	.009	.011
D	.375	.395	.505	.550	.745	.775	.745	.775	.895	.925	1.010	1.050	1.080	1.120	1.240	1.270	1.450	1.480	2.050	2.080
E	.240	.260	.240	.260	.240	.260	.240	.260	.240	.260	.250	.290	.330	.370	.515	.540	.530	.550	.530	.550
E_2	.310	.385	.310	.385	.310	.385	.310	.385	.310	.385	.310	.385	.410	.480	.585	.700	.585	.700	.585	.700
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.125	.150	.125	.150	.125	.150	.125	.150	.125	.150	.125	.150	.125	.160	.125	.160	.125	.160	.125	.160
Q	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060	.015	.060
S_1	.010	.030	.040	.070	.040	.065	.010	.040	.030	.040	.025	.055	.015	.045	.035	.065	.040	.070	.040	.070

Notes: 1. Standard lead finish is tin plate or solder dip.
2. Dimension E_2 is an outside measurement.

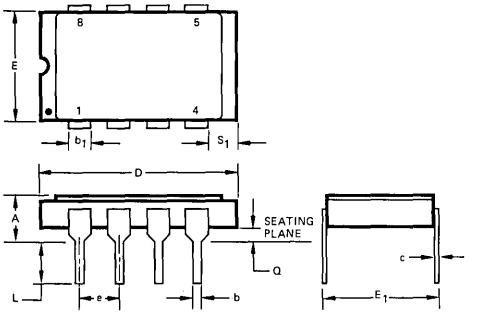
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES

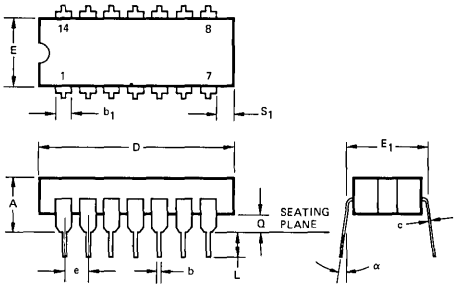
D-8-1



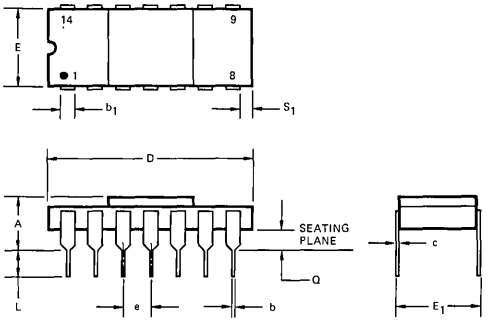
D-8-2



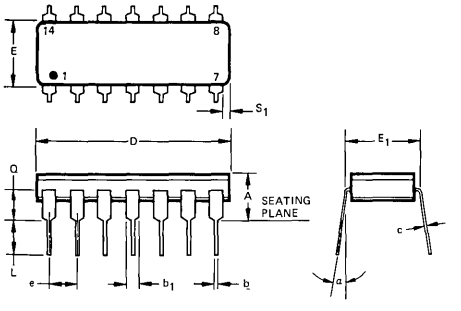
D-14-1



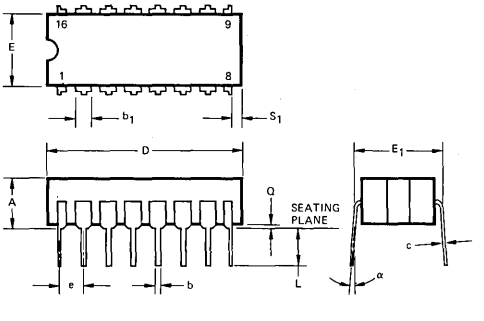
D-14-2



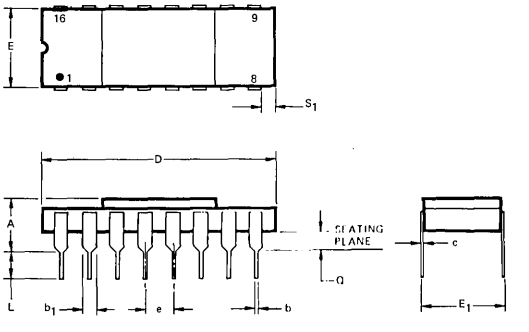
D-14-3



D-16-1



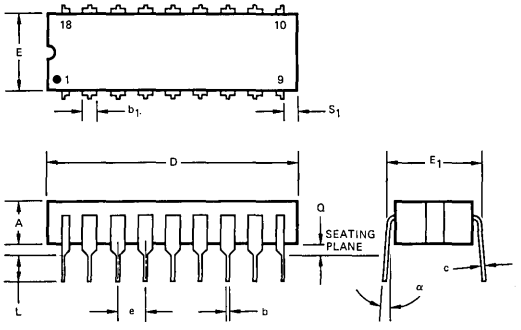
D-16-2



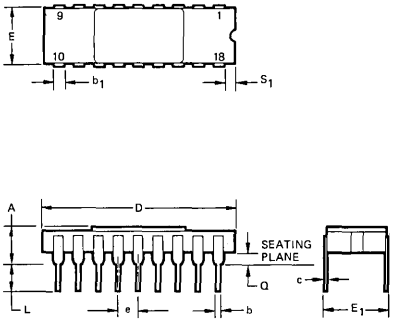
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

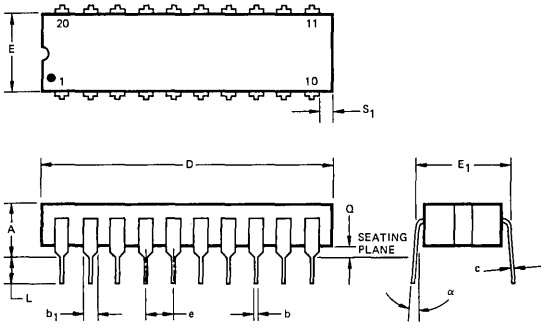
D-18-1



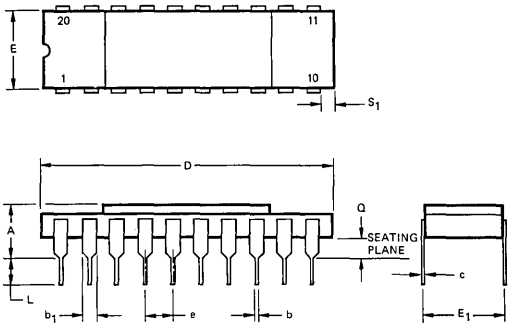
D-18-2



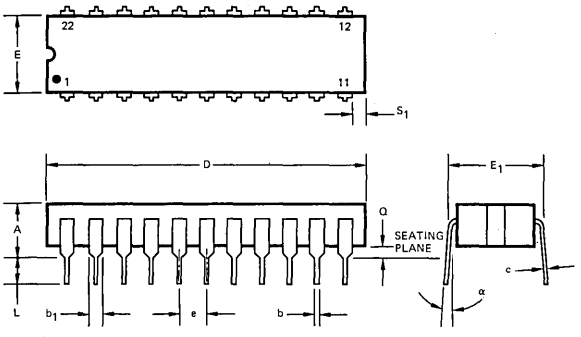
D-20-1



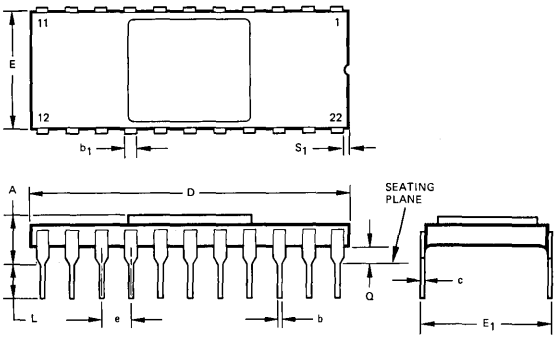
D-20-2



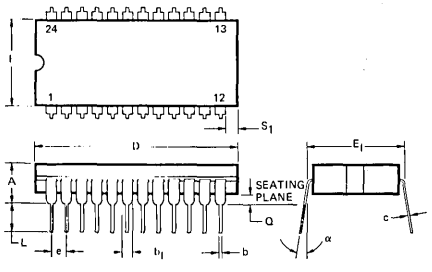
D-22-1



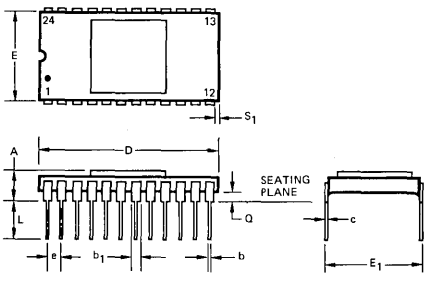
D-22-2



D-24-1 and D-24-4



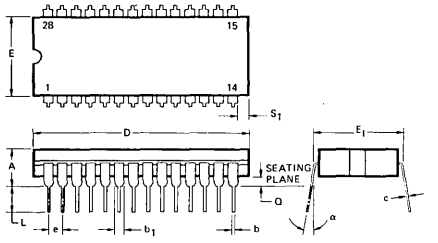
D-24-2



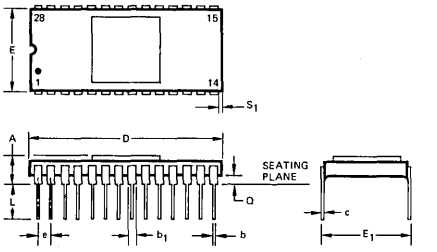
PACKAGE OUTLINES (Cont.)

HERMETIC DUAL IN-LINE PACKAGES (Cont.)

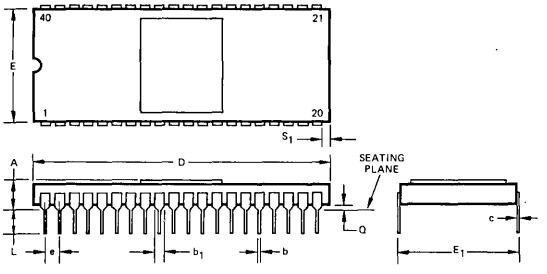
D-28-1



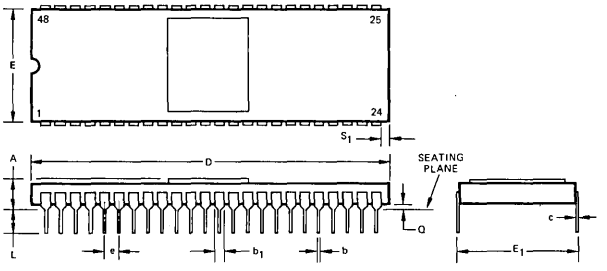
D-28-2



D-40-2



D-48-2



AMD Pkg.	D-8-1		D-8-2		D-14-1		D-14-2		D-14-3 (Note 2)		D-16-1		D-16-2		D-18-1		D-18-2		D-20-1	
Common Name	CERDIP		SIDE-BRAZED		CERDIP		SIDE-BRAZED		METAL DIP		CERDIP		SIDE-BRAZED		CERDIP		SIDE-BRAZED		CERDIP	
38510 Appendix C	–		–		D-1(1)		D-1(3)		D-1(1)		D-2(1)		D-2(3)		–		–		–	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.130	.200	.100	.200	.130	.200	.100	.200	.100	.200	.130	.200	.100	.200	.130	.200	.100	.200	.140	.220
b	.016	.020	.015	.022	.016	.020	.015	.022	.015	.023	.016	.020	.015	.022	.016	.020	.015	.022	.016	.020
b_1	.050	.070	.040	.065	.050	.070	.040	.065	.030	.070	.050	.070	.040	.065	.050	.070	.040	.065	.050	.070
c	.009	.011	.008	.013	.009	.011	.008	.013	.008	.011	.009	.011	.008	.013	.009	.011	.008	.013	.009	.011
D	.370	.400	.500	.540	.745	.785	.690	.730	.660	.785	.745	.785	.780	.820	.870	.920	.850	.930	.935	.970
E	.240	.285	.260	.310	.240	.285	.260	.310	.230	.265	.240	.310	.260	.310	.280	.310	.260	.310	.245	.285
E_1	.300	.320	.290	.320	.290	.320	.290	.320	.290	.310	.290	.320	.290	.320	.290	.320	.290	.320	.290	.320
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.125	.150	.125	.160	.125	.150	.125	.160	.100	.150	.125	.150	.125	.160	.125	.150	.125	.160	.125	.150
Q	.015	.060	.020	.060	.015	.060	.020	.060	.020	.080	.015	.060	.020	.060	.015	.060	.020	.060	.015	.060
S_1	.004		.005		.010		.005		.020		.005		.005		.005		.005		.005	
α	3°	13°			3°	13°			3°	13°	3°	13°			3°	13°			3°	13°
Standard Lead Finish	b		b or c		b		b or c		c		b		b or c		b		b or c		b	

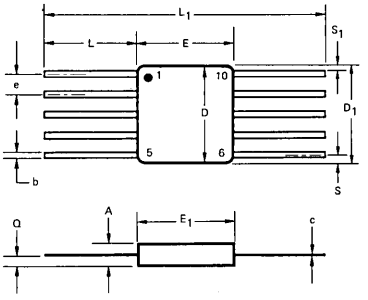
AMD Pkg.	D-20-2		D-22-1		D-22-2		D-24-1		D-24-2		D-24-4		D-28-1		D-28-2		D-40-2		D-48-2	
Common Name	SIDE-BRAZED		CERDIP		SIDE-BRAZED		CERDIP		SIDE-BRAZED		CERVIEW		CERDIP		SIDE-BRAZED		SIDE-BRAZED		SIDE-BRAZED	
38510 Appendix C	–		–		–		D-3(1)		D-3(3)		–		–		–		–		–	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.100	.200	.140	.220	.100	.200	.150	.225	.100	.200	.150	.225	.150	.225	.100	.200	.100	.200	.100	.200
b	.015	.022	.016	.020	.015	.022	.016	.020	.015	.022	.016	.020	.016	.020	.015	.022	.015	.022	.015	.022
b_1	.040	.065	.045	.065	.030	.060	.045	.065	.030	.060	.045	.065	.045	.065	.030	.060	.030	.060	.030	.060
c	.008	.013	.009	.011	.008	.013	.009	.011	.008	.013	.009	.011	.009	.012	.008	.013	.008	.013	.008	.013
D	.950	1.010	1.045	1.110	1.050	1.110	1.230	1.285	1.170	1.200	1.235	1.280	1.440	1.490	1.380	1.420	1.960	2.040	2.370	2.430
E	.260	.310	.360	.405	.360	.410	.510	.545	.550	.610	.510	.550	.510	.545	.560	.600	.550	.610	.570	.610
E_1	.290	.320	.390	.420	.390	.420	.600	.620	.590	.620	.600	.630	.600	.620	.590	.620	.590	.620	.590	.620
e	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110	.090	.110
L	.125	.160	.125	.150	.125	.160	.120	.150	.120	.160	.120	.150	.125	.150	.120	.160	.120	.160	.125	.160
Q	.020	.060	.015	.060	.020	.060	.015	.060	.020	.060	.015	.060	.015	.060	.020	.060	.020	.060	.020	.060
S_1	.005		.005		.005		.010		.005		.010		.010		.005		.005		.005	
α			3°	13°			3°	13°			3°	13°	3°	13°						
Standard Lead Finish	b or c		b		b or c		b		b or c				b		b		b or c		b or c	

Notes: 1. Load finish b is tin plate. Finish c is gold plate.
2. Used only for LM108/LM108A.
3. Dimensions E and D allow for off-center lid, meniscus and glass overrun.

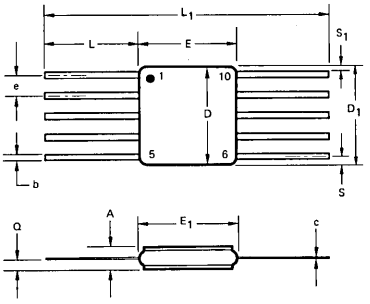
PACKAGE OUTLINES (Cont.)

FLAT PACKAGES

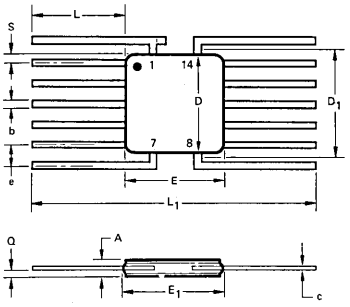
F-10-1



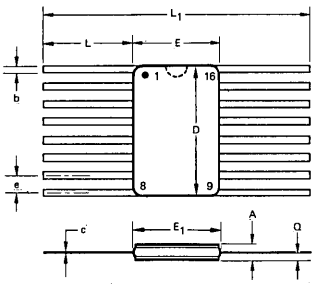
F-10-2



F-14-1 and F-14-2

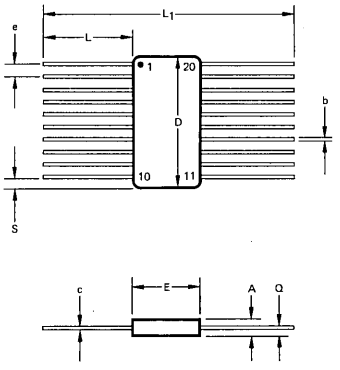


F-16-1 and F-16-2

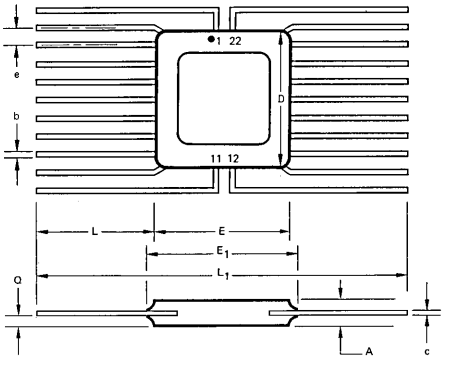


Note: Notch is pin 1 index on cerpack.

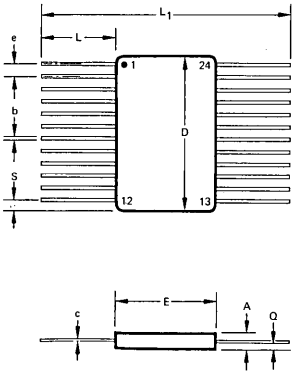
F-20-1



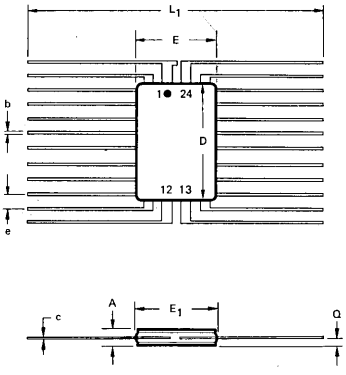
F-22-1



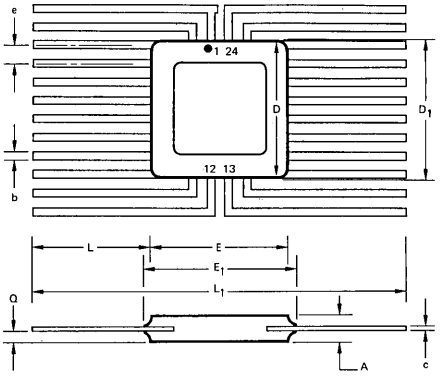
F-24-1



F-24-2



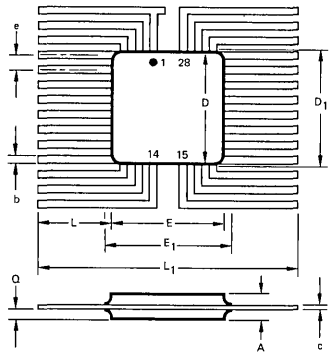
F-24-3



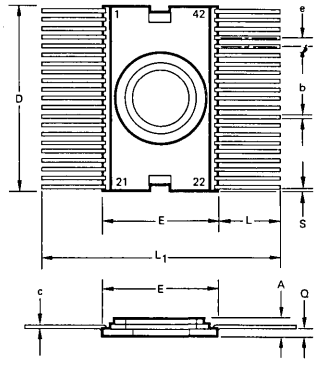
PACKAGE OUTLINES (Cont.)

FLAT PACKAGES (Cont.)

F-28-1



F-42-1



AMD Pkg.	F-10-1		F-10-2		F-14-1		F-14-2		F-16-1		F-16-2		F-20-1		F-22-1	
Common NAME	CERPACK		METAL FLAT PAK		CERPACK		METAL FLAT PAK		CERPACK		METAL FLAT PAK		CERPACK		METAL FLAT PAK	
38510 Appendix C	F-4		F-4		.F-1		F-1		F-5		–		–		–	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.045	.080	.045	.080	.045	.080	.045	.085	.045	.085	.045	.085	.045	.085	.045	.090
b	.015	.019	.012	.019	.015	.019	.012	.019	.015	.019	.015	.019	.015	.019	.015	.019
c	.004	.006	.003	.006	.004	.006	.003	.006	.004	.006	.003	.006	.004	.006	.003	.006
D	.230	.255	.235	.275	.230	.255	.230	.270	.370	.425	.370	.400	.490	.520	.380	.420
D_1				.275				.280				.410				.440
E	.240	.260	.240	.260	.240	.260	.240	.260	.245	.285	.245	.285	.245	.285	.380	.420
E_1		.275		.280		.275		.280		.290		.305		.290		.440
e	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055
L	.300	.370	.300	.370	.300	.370	.300	.370	.300	.370	.300	.370	.300	.370	.250	.320
L_1	.920	.980	.920	.980	.920	.980	.920	.980	.920	.980	.920	.980	.920	.980	.920	.980
Q	.010	.040	.010	.040	.010	.040	.010	.040	.020	.040	.010	.040	.020	.040	.010	.040
S_1	.005		.005		.005		.005		.005		.005		.005			
Standard Lead Finish	b		c		b		c		b		c		b		c	

AMD Pkg.	F-24-1		F-24-2		F-24-3		F-28-1		F-42-1	
Common Name	CERPACK		METAL FLAT PAK		METAL FLAT PAK		METAL FLAT PAK		CERAMIC FLAT PAK	
38510 Appendix C	F-6		F-8		–		–		–	
Parameters	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
A	.050	.090	.045	.090	.045	.090	.045	.080	.070	.115
b	.015	.019	.015	.019	.015	.019	.015	.019	.017	.023
c	.004	.006	.003	.006	.003	.006	.003	.006	.006	.012
D	.580	.620	.360	.410	.380	.420	.360	.410	1.030	1.090
D_1				.420		.440		.410		1.090
E	.360	.385	.245	.285	.380	.420	.360	.410	.620	.660
E_1		.410		.305		.440		.410		.660
e	.045	.055	.045	.055	.045	.055	.045	.055	.045	.055
L	.265	.320	.300	.370	.250	.320	.270	.320	.320	.370
L_1	.920	.980	.920	.980	.920	.980	.955	1.000	1.300	1.370
Q	.020	.040	.010	.040	.010	.040	.010	.040	.020	.060
S_1	.005		.005		0		0		.005	
Standard Lead Finish	b		c		c		c		c	

Notes: 1. Lead finish b is tin plate. Finish c is gold plate.
2. Dimensions E_1 and D_1 allow for off-center lid, meniscus, and glass overrun.

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