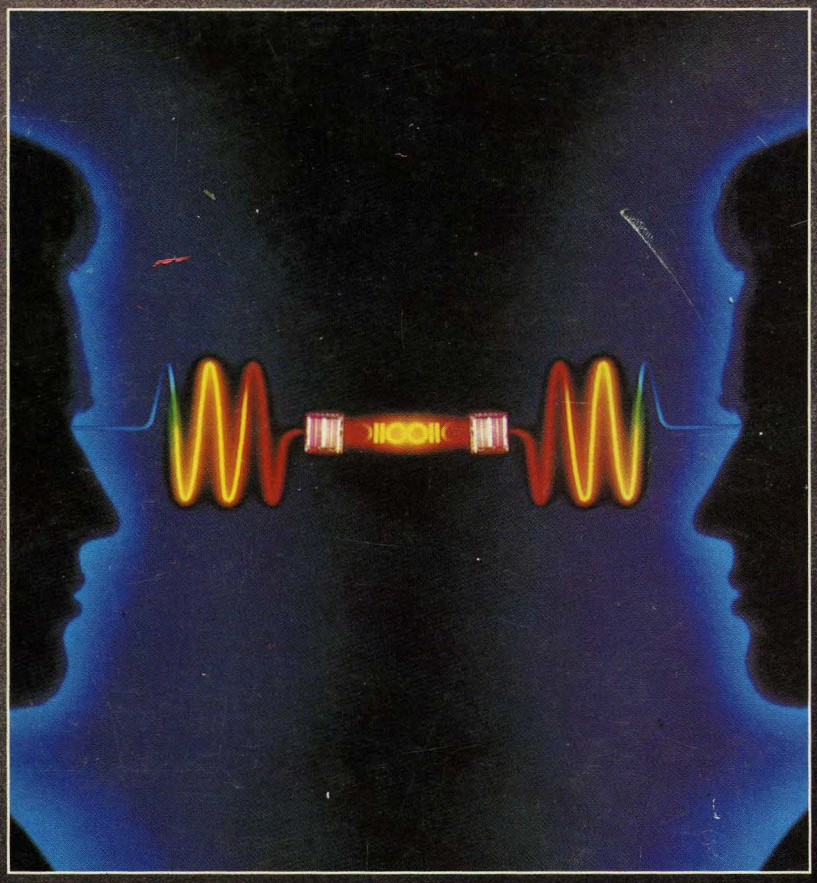

Data Acquisition

HARRIS
SEMICONDUCTOR

HARRIS SEMICONDUCTOR

THE NEW HARRIS SEMICONDUCTOR

In December 1988, Harris Semiconductor acquired the General Electric Solid State division, thereby adding former GE, RCA, and Intersil devices to the Harris Semiconductor line.

This Data Acquisition databook represents the full line of Harris Semiconductor Data Acquisition products for commercial applications and supersedes previously published Data Acquisition databooks under the Harris, GE, RCA or Intersil names. For a complete listing of all Harris Semiconductor products, please refer to the Product Selection Guide (SPG-201R; ordering information below).

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Melbourne, FL 32901
(407) 724-3739
FAX 407-724-3937

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2-4-1 Nishi-Shinjuku
Shinjuku-Ku, Tokyo 163 Japan
TEL: 81-3-3345-8911

Printed in U.S.A., 8/1991

Harris Semiconductor products are sold by description only. All specifications in this product guide are applicable only to packaged products; specifications for die are available upon request. Harris reserves the right to make changes in circuit design, specifications and other information at any time without prior notice. Accordingly, the reader is cautioned to verify that information in this publication is current before placing orders. Reference to products of other manufacturers are solely for convenience of comparison and do not imply total equivalency of design, performance, or otherwise.

HARRIS
SEMICONDUCTOR

DATA ACQUISITION

TABLE OF CONTENTS

DATA ACQUISITION PRODUCT TECHNICAL ASSISTANCE

For technical assistance on the Harris products listed in this databook, please contact Field Applications Engineering staff available at one of the following Harris Sales Offices:

UNITED STATES

CALIFORNIA	Costa Mesa	714-433-0600
	San Jose	408-922-0977
	Woodland Hills	818-992-0686
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ILLINOIS	Schaumburg	708-240-3480
MASSACHUSETTS	Burlington	617-221-1850
NEW JERSEY	Mt. Laurel	609-727-1909
	Rahway	201-381-4210
TEXAS	Dallas	214-733-0800

INTERNATIONAL

FRANCE	Paris	33-1-346-54046
GERMANY	Munich	49-8-963-8130
ITALY	Milano	39-2-262-22141
JAPAN	Tokyo	81-3-345-8911
KOREA	Seoul	82-2-551-0931
U.K.	Camberley	44-2-766-86886

For literature requests, please contact Harris Telemarketing at 407-724-3739.

DATA ACQUISITION 1

GENERAL INFORMATION

Alphanumeric Product Index

Alphanumeric Product Index (Continued)

Alphanumeric Product Index (Continued)

Alphanumeric Product Index (Continued)

Alphanumeric Product Index (Continued)

Alphanumeric Product Index (Continued)

Product Index by Family

A/D CONVERTERS DISPLAY

A/D CONVERTERS INTEGRATING

A/D SUCCESSIVE APPROXIMATION

A/D CONVERTERS FLASH

Product Index by Family (Continued)

D/A CONVERTERS

ANALOG SWITCHES

Product Index by Family (Continued)

ANALOG SWITCHES (Continued)

Product Index by Family (Continued)

ANALOG SWITCHES (Continued)

1

MULTIPLEXERS

Product Index by Family (Continued)

MULTIPLEXERS (Continued)

DISPLAY DRIVERS

REAL-TIME CLOCK

Product Index by Family (Continued)

Harris Semiconductor Data Acquisition

Obsolete Parts and Not Recommended for New Design Parts

OBSOLETE PRODUCT	SUGGESTED REPLACEMENT
HI-DAC87V/883	AD7545SQ/883
ICM7218E	ICM7228A,B,C,D
ICM7225	
ICM7233	
IH5040	HI5040 or IH5140*
IH5041	HI5041 or IH5141*
IH5042	HI5042 or IH5142*
IH5044	HI5044 or IH5144*
IH5045	HI5045 or IH5145*
IH5046	HI5046*
IH5047	HI5047*
IH5148	HI5048*
IH5149	HI5049*
IH5150	HI5050*
IH6116	DG506A*
IH6216	DG507A*
IH9108	
IM4702	HD-4702*
IM6402	HD-6402*

NOT RECOMMENDED FOR NEW DESIGN	SUGGESTED REPLACEMENT
ICM7218A,B,C,D	ICM7228A,B,C,D
ICL7112	ICL7115*
HI-7159	HI-7159A*
HI-562A	HI-565A
HI-DAC16B/16C	ICL7121
ICL7107CDL	ICL7107CPL*
ICL7107CJL	ICL7107CPL*
ICL7126CDL	ICL7126CPL*
ICL7135CJI	ICL7135CPI*
ICL7136CDL	ICL7136CPL*
ICL7136CJL	ICL7136CPL*
ICL7137CDL	ICL7137CPL*
ICM7231BFIJL	ICM7231BFIPL*
ICM7231BFIM44	ICM7231BFIPL
ICM7232BFIJL	ICM7231BFIPL*
ICM7232CRIJL	ICM7232CRIPL*
ICM7232CRIM44	ICM7232CRIPL
ICM7232BFIM44	ICM7232BFIPL
ICM7217AIJI	ICM7217AIPI
ICM7217CIJI	ICM7217CIPI
ICL7139CM44	ICL7139CPL
ICL7116RCPL	ICL7116CPL
ICL7117RCPL	ICL7117CPL
ICL7137RCPL	ICL7137CPL

Note: * Pin for Pin Compatible

Die Availability

Most of the products listed in this catalog are available in Die or Wafer form. Please consult your local sales office or representative for specific information.

Application Note Abstracts

AN#	TITLE	ABSTRACTS
AO01	**Glossary of Data Conversion Terms**	This glossary defines the most often used terms in the field of data conversion technology.
AO02	**Principles of Data Acquisition and Conversion**	Presents theory, converter coding, topologies, and specifications.
AO04	**IH5009 Low Cost Analog Switch Series**	Compares the members of the IH5009 "virtual ground" analog switches and provides suggested applications.
AO16	**Selecting A/D Converters**	Describes the differences between integrating converters and successive approximation converters. Includes a checklist for decision making, and a note on multiplexed data systems.
AO17	**The Integrating A/D Converter**	Provides an explanation of integrating A/D converters, together with a detailed error analysis.
AO18	**Do's and Dont's of Applying A/D Converters**	An analysis of proper design techniques using D/A converters.
AO19	**4½-Digit Panel Meter Demonstration/Instrumentation Boards**	Describes two typical PC board layouts using the 8052A/7103A 4½-digit A/D pair. Includes schematics, parts layout, list of materials, etc. Also see AO28.
AO20	**A Cookbook Approach to High-Speed Data Acquisition and Microprocessor Interfacing**	Uses the building block approach to design a complete 12 volt system. Explains the significance of each component and demonstrates methods for microprocessor interfacing, including the use of control signals.
AO23	**Low Cost Digital Panel Meter Designs**	Provides a detailed explanation of the 7106 and 7107 3½-digit panel meter IC's, and describes two of the evaluation kits available from Harris.
AO28	**Building an Autoranging DMM with the ICL71C03A/8052A A/D Converter Pair**	This companion application note to AO19 explains the use of the 8052A/7103A converter pair to build a ±4½-digit autoranging digital multimeter. Included are schematics, circuit descriptions, tips and hints, etc.
AO30	**ICL7104; a Binary Output A/D Converter for μProcessors**	Describes in detail the operation of the 7104. Includes in digital interfacing, handshake mode, buffer gain, auto-zero, and external zero. Appendix includes detailed discussion of auto-zero loop residual errors in dual slope A/D conversion.
AO32	**Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7107/7109 Family**	Explains in detail the operation of the ICL7106/7107/7109 family of A/D converters.
AO42	**Interpretation of Data Converter Accuracy Specifications**	Cognizance of accuracy factors involved when interfacing data converters into system applications permits designers to meet overall error budget constraints. Transfer functions; quantization noise; offset, gain, and linearity errors; and temperature effects must be interpreted to satisfy specification requirements.
AO46	**Building a Battery Operated Autoranging DVM with the ICL7106**	Explains principles of autoranging, problems, and solutions. Includes clock circuits, power supply requirements, design hints, schematics, etc.
AO47	**Games People Play with Harris's A/D Converters**	Describes 25 different integrating A/D converter applications. Input circuits, conversion modifications, display and microprocessor interfaces are shown in detail.
AO48	**Know Your Converter Codes**	When you work with A/D and D/A converters, there are many input and output codes to choose from.
AO49	**Applying the ICL7109 A/D Converter**	The operation and application of the ICL7109 12-bit integrating A/D converter is presented.
AO52	**Tips for Using Single-Chip 3½-Digit A/D Converters**	Answers frequently asked questions regarding the operation of 3½-digit single-chip A/D converters. Included are sections on power supplies, displays, timing, and component selection.
AO54	**Display Driver Family Combines Convenience of Use with Microprocessor Interfaceability**	Compares and describes the various display drivers. Includes design examples for 7 segment, alphanumeric, and bargraph systems.

Application Note Abstracts (Continued)

AN#	TITLE	ABSTRACTS
AO57	**Graphs Give Aperture Time Required for A/D Conversion**	It is important for the designer to know what aperture time is required to keep the system error to a tolerable value in terms of the resolution of his A/D converter.
AO59	**Digital Panel Meter Experiments for the Hobbyist**	Explains how the ICL7106/7107 can be used to make fundamental measurements of voltage, current, and resistance.
KB11	**3¾-Digit Autoranging Multimeter — ICL7139EV/Kit**	Detailed description of internal device circuitry and its intended operation, assembly instructions, block diagrams, current, voltage, resistance measurements, electrical characteristics. An excellent means of checking the characteristics and evaluating the performance of the ICL7139.
RO09	**Reduce CMOS-Multiplexer Troubles through Proper Device Solutions**	Addresses the issue of error sources, specifically output leakage and over-voltage protection circuitry. Discusses multiplexer selection alternatives.
RO23	**Interface a Real-Time Clock Chip to the IBM PC or Apple II**	Discusses crystal selection, oscillator circuitry, battery backup scheme and PC board layout and how these affect the accuracy and stability of the Real-Time Clock.
520	**CMOS Analog Multiplexers and Switches; Application Considerations**	Switch selection criteria, datasheet definitions, care and feeding of multiplexers and switches, digital interface, practical multiplexer applications alternative to CMOS switches and multiplexers.
521	**Getting the Most Out of CMOS Devices for Analog Switching Jobs**	CMOS versus bipolar device performances, over voltage and channel interaction conditions, JI technology and latch-up, floating-body JI technology, foolproof CMOS analog multiplexer, other DI benefits.
522	**Digital-to-Analog Converter Terminology**	Explains DAC terminology, Resolution Gain Error, Offset Error, Linearity Error, Differential Linearity Error, Drift, Settling Time, etc.
524	**Digital-to-Analog Converter High-Speed A/D Applications**	Use of High-Speed DAC's in tracking, servo, and successive approximation Analog-to-Digital Converters. Design ideas for Data Acquisition Systems.
531	**Analog Switch Applications in A/D Data Conversion Systems**	System configurations, analog switch types, CMOS switch selection guidelines, alternate uses of CMOS switches.
532	**Common Questions Concerning CMOS Analog Switches**	Power supply considerations, input overvoltage protection, single supply operation, various questions about Harris D.I. switches.
534	**Additional Information on the HI-300 Series Switch**	"ON" resistance, leakage currents, switching speeds, power supply requirements, internal switch operation, charge injection, power supplies conditions, and protective circuitry.
535	**Design Considerations for a Data Acquisition System (DAS)**	A collection of guidelines for the design of a Data Acquisition System. Includes signal conditioning, transducers, single-ended vs. differential signal paths, low level signals, filters, Programmable Gain Amplifiers, sampling rate, and computer interfacing.
539	**A Monolithic 16-Bit D/A Converter**	Detailed description of the HI-DAC16 D/A Converter, chip photo and schematic, plus applications and interface considerations.
543	**New High-Speed Switch Offers Sub-50ns Switching Times**	Application enhancement using the HI-201HS, high-speed multiplexers, high-speed sample and hold, analog switch and op amp circuitry, integrator with start/reset, low pass filter with select break frequency, amplifier with programmable gain, future applications.
557	**Recommended Test Procedures for Analog Switches**	Description of analog switch test methods employed at Harris Semiconductor.
559	**HI-222 Video/HF Switch Optimizes Key Parameters**	Presents video performance characteristics such as differential gain and phase, off-isolation, crosstalk. Also covers reduced supply operation, charge injection, and PC board layout techniques.

Competitive Cross Reference Chart

Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement
AD562	HI-562A	
AD562A	HI-562A	
AD563		HI-565A
AD565A	HI-565A	
AD571		CA3310, HI-7151/52
AD573		CA3310, HI-7151/52
AD574A	HI-574A	
AD589	ICL8069	
AD590	AD590	
AD674A	HI-674A	
AD679		ICL7115
AD5240		HI-674A, HI-774
AD7501		HI-508
AD7506	DG506A	
AD7506	HI-506	
AD7507	HI-507	
AD7507	DG507A	
AD7511		HI-201
AD7512		HI-5043
AD7520	AD7520	
AD7521	AD7521	
AD7523	AD7523	
AD7530	AD7530	
AD7531	AD7531	
AD7533	AD7533	
AD7534		ICL7134
AD7535		ICL7134
AD7536		ICL7134
AD7538		ICL7134
AD7541	AD7541	
AD7545	AD7545	
AD7579		CA3310, HI-7151/52
AD7580		CA3310, HI-7151/52
ADADC80		HI-574A, HI-674A
ADADC84-85		HI-674A, HI-774
ADC0802	ADC0802	
ADC0803	ADC0803	
ADC0804	ADC0804	
ADC1080/1280		HI-574A
ADC1080/1280		HI-674A
ADC1210/11		HI-574A
ADC550		HI-574A
ADC574A	HI-574A	
ADC581		HI-574A
ADC674A	HI-674A	
ADC774	HI-774	
ADC80		HI-674A
ADC84/85		HI-674A
ADC8412		HI-674A
ADC85C12		HI-674A

Competitive Cross Reference Chart (Continued)

Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement
ADC8712		HI-674A
ADC9012		HI-674A
ADC910		HI-7151/52
ADCHX12B		HI-574A, HI-674A
ADCL12B2		HI-574A
ADCL12B2		HI-674A
ADCM12B2		HI-674A
ADCMA12B2B		HI-674A
ADCMA12B2B		HI-574A
ADCMAI13B2A		HI-574A
ADDAC71/72		HI-DAC16, ICL7121
ADDAC80V	HI-DAC80V	
ADDAC85V	HI-DAC85V	
ADDAC87V	HI-DAC87V	
ADG201	DG201A	
ADG201HS	HI-201HS	
ADG202	DG202	
ADG211	DG211	
ADG212	DG212	
ADG506A	DG506A	
ADG507A	DG507A	
ADG508A	DG508A	
ADG509A	DG509A	
ADG526	DG526	
ADG527	DG527	
ADG528	DG528	
ADG529	DG529	
AM6012		HI-562A
CA3304	CA3304	
CA3306	CA3306	
CA3338	CA3338	
DA700/701		HI-DAC16, ICL7121
DA702/703		HI-DAC16, ICL7121
DAC1020	AD7520	
DAC1021	AD7520	
DAC1022	AD7520	
DAC1220	AD7521	
DAC1221	AD7521	
DAC1222	AD7521	
DAC1265	HI-565A	
DAC3281016		HI-DAC16, ICL7121
DAC346C		HI-DAC80V
DAC347LP-12		HI-DAC87
DAC372		HI-DAC80
DAC562	HI-562A	
DAC70		HI-DAC16, ICL7121
DAC71/72		HI-DAC16, ICL7121
DAC7541	AD7541	
DAC7545	AD7545	
DAC80	HI-DAC80V	
DAC85	HI-DAC85V	
DAC87	HI-DAC87V	
DACHR16B		HI-DAC16

Competitive Cross Reference Chart (Continued)

Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement
DG180	DG180	
DG181	DG181	
DG182	DG182	
DG183	DG183	
DG184	DG184	
DG185	DG185	
DG186	DG186	
DG187	DG187	
DG188	DG188	
DG189	DG189	
DG190	DG190	
DG191	DG191	
DG200A	DG200	
DG201A	DG201A	
DG202	DG202	
DG211	DG211	
DG212	DG212	
DG271	HI-201HS	
DG300A	DG300A	
DG301A	DG301A	
DG302A	DG302A	
DG303A	DG303A	
DG304A	HI-304	
DG305A	HI-305	
DG306A	HI-306	
DG307A	HI-307	
DG308A	DG308A	
DG309	DG309	
DG381A	HI-381	
DG384A	HI-384	
DG387A	HI-387	
DG390	HI-390	
DG5040	HI-5040	
DG5041	HI-5041	
DG5041	HI-5042	
DG5043	IH5043/HI-5043	
DG5044	HI-5044	
DG5045	HI-5045	
DG506A	DG506A	
DG507A	DG507A	
DG508A	DG508A	
DG509A	DG509A	
DG5140	IH5140	
DG5141	IH5141	
DG5142	IH5142	
DG5143	IH5143	
DG5144	IH5144	
DG5145	IH5145	

Competitive Cross Reference Chart (Continued)

Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement
DG526	DG526	
DG527	DG527	
DG528	DG528	
DG529	DG529	
HI-506A	HI-506A	
HI-507A	HI-507A	
HI-508A	HI-508A	
HI-509A	HI-509A	
HS5200		HI-674A
HS574	HI-574A	
HS574	HI-674A	
HS7541	AD7541	
HS7545	AD7545	
HSDA387	HI-DAC87V	
ICL7106	ICL7106	
ICL7107	ICL7107	
ICL7109	ICL7109	
ICL7112	ICL7112	
ICL7115	ICL7115	
ICL7116	ICL7116	
ICL7117	ICL7117	
ICL7121	ICL7121	
ICL7126	ICL7126	
ICL7129	ICL7129	
ICL7134	ICL7134	
ICL7135	ICL7135	
ICL7136	ICL7136	
ICL7137	ICL7137	
ICL7139	ICL7139	
ICL7149	ICL7149	
ICL7182	ICL7182	
ICL8069	ICL8069	
ICM7170	ICM7170	
ICM7207	ICM7207	
ICM7208	ICM7208	
ICM7209	ICM7209	
ICM7210	ICM7210	
ICM7211	ICM7211	
ICM7212	ICM7212	
ICM7213	ICM7213	
ICM7217	ICM7217	
ICM7218	ICM7218, ICM7228	
ICM7224	ICM7224	
ICM7226	ICM7226	
ICM7228	ICM7228	
ICM7231	ICM7231	
ICM7243	ICM7243	
ICM7249	ICM7249	
LF11201	DG201	
LF13201	DG201A	
LF13508	DG508A	
LF13509	DG509A	
LM113	ICL8069	
LT1081	ICL232	

Competitive Cross Reference Chart (Continued)

Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement
MAX130	ICL7106	
MAX131	ICL7136	
MAX136	ICL7116	
MAX173	HI-7152	
MAX177	HI-7151	
MAX232	ICL232	
MAX358	IH5108	
MAX359	IH5208	
MC3412	HI-565A	
MP5010	ICL8069	
MP574A	HI-574, HI-674A	
MP7520	AD7520	
MP7521	AD7521	
MP7523	AD7523	
MP7533	AD7533	
MP7541	AD7541	
MP7545	AD7545	
MP7621	AD7541	
MP7682	CA3306	
MP7684	HI-5700	
MP7684A	HI-5700	
MPC800KG	HI-516-5	
MPC801KG	HI-518-2	
MPC801SG	HI-518-1	
MUX-08	HI-508	
MUX-16	HI-506	
MUX-24	HI-509	
MUX-28	HI-507	
MUX-88	HI-508	
MX151		HI-7152
MX565A	HI-565A	
MX574A	HI-574A	
MX674A	HI-674A	
MX774	HI-774	
MX7520	AD7520	
MX7521	AD7521	
MX7523	AD7523	
MX7530	AD7530	
MX7533	AD7533	
MX7534		ICL7134
MX7535		ICL7134
MX7536		ICL7134
MX7541	AD7541	
MX7545	AD7545	
PM562	HI-562A	
PM7533	AD7533	
PM7541	AD7541	
PM7545	AD7545	
TL185	HI-5045	
TL188	HI-5042	
TL191	IH5043/HI-5043	
TLC7135	ICL7135	
TS8308		CA3318
TSC04	ICL8069	
TSC232	ICL232	

Competitive Cross Reference Chart (Continued)

Part Number	Harris Pin-for-Pin Replacement	Harris Closest Replacement
TSC7106	ICL7106	
TSC7107	ICL7107	
TSC7109	ICL7109	
TSC7116	ICL7116	
TSC7117	ICL7117	
TSC7126	ICL7126	
TSC7129	ICL7129	
TSC7135	ICL7135	
TSC7136	ICL7136	
TSC7137	ICL7137	
TSC7211	ICM7211	
TSC7212	ICM7212	
TSC805		ICL7149
TSC810	ICL7116	
TSC815		ICL7149
TSC825		ICL7182
TSC9491	ICL8069	

DATA ACQUISITION 2

A/D CONVERTERS DISPLAY

HARRIS SEMICONDUCTOR

Data Conversion Circuits

CA3162, CA3162A

A/D Converter for 3-Digit Display

Features:

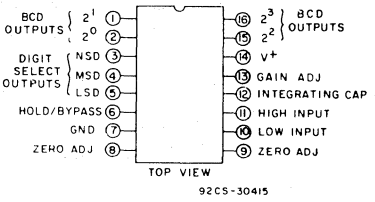
- *Dual-slope A/D conversion*
- *Multiplexed BCD display*
- *Ultra-stable internal band-gap voltage reference*
- *Capable of reading 99 mV below ground with single supply*
- *Differential input*
- *Internal timing - no external clock required*
- *Choice of low-speed (4-Hz) or high-speed (96-Hz) conversion rate*
- *"Hold" inhibits conversion but maintains delay*
- *Overrange indication - "EEE" for reading greater than +999 mV, "-" for reading more negative than -99 mV when used with CA3161E BCD-to-Seven Segment Decoder/Driver*
- *Extended temperature range version available*

The CA3162E and CA3162AE are I^2L monolithic A/D converters that provide a 3-digit multiplexed BCD output. They are used with the CA3161E BCD-to-Seven-Segment Decoder/Driver* and a minimum of external parts to implement a complete 3-digit display. The CA3162AE is identical to the CA3162E except for an extended operating temperature range.

The CA3162 is supplied in a 16-lead dual-in-line plastic package (E suffix). The CA3162 is also available in chip form (H suffix).

* The CA3161E is described in RCA data bulletin File No. 1079.

TERMINAL ASSIGNMENT
CA3162E



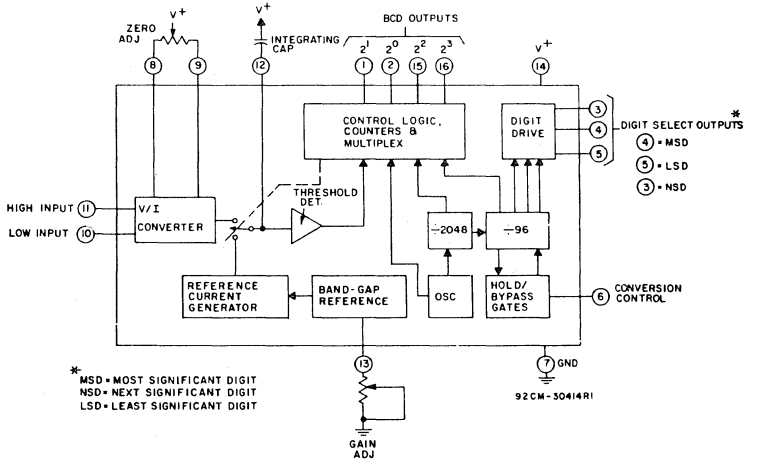


Fig. 1 - Functional block diagram of the CA3162E.

File Number **1080**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (between terminals 7 and 14) ..... +7 V
INPUT VOLTAGE (terminal 10 or 11 to ground) ..... ±15 V
DEVICE DISSIPATION:
Up to T_A = +55°C ..... 750 mW
Above T_A = +55°C ..... Derate Linearly at 7.9 mW/°C
AMBIENT TEMPERATURE RANGE:
Operating, CA3162E ..... 0 to +75°C
Operating, CA3162AE ..... -40 to +85°C
Storage ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V + = 5 V, Zero pot centered, gain pot = 2.4 kΩ unless otherwise stated

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Operating Supply Voltage Range V +	—	4.5	5	5.5	V
Supply Current, I+	100 kΩ to V+ on terms. 3, 4, 5	—	—	17	mA
Input Impedance, Z_I	—	—	100	—	MΩ
Input Bias Current, I_{IB}	Terms. 10 and 11	—	-80	—	nA
Unadjusted Zero Offset	V_{11} -V_{10} = 0 V, read decoded output	-12	—	+12	mV
Unadjusted Gain	V_{11} -V_{10} = 900 mV, read decoded output	846	—	954	mV
Linearity	See Notes 1 and 2	-1	—	+1	Count
Conversion Rate:					
Slow Mode	Term. 6 = open or gnd	—	4	—	Hz
Fast Mode	Term. 6 = 5 V	—	96	—	Hz
Conversion Control Voltage (Hold Mode) at Terminal 6	—	0.8	1.2	1.6	V
Common-Mode Input Voltage Range, V_{ICR}	See Note 3, 4	-0.2	—	+0.2	V
BCD Sink Current at terms. 1, 2, 15, 16	$V_{BCD} \geq$ 0.5 V, at logic zero state	0.4	1.6	—	mA
Digit Select Sink Current at terms. 3, 4, 5	$V_{Digit\ Select}$ = 4 V at logic zero state	1.6	2.5	—	mA
Zero Temperature Coefficient	V_I = 0 V, zero pot centered	—	10	—	μV/°V
Gain Temperature Coefficient	V_I = 900 mV, gain pot = 2.4 KΩ	—	0.005	—	%/°C

Notes:

1. Apply zero volts across V_{11} to V_{10}. Adjust zero potentiometer to give 000 mV reading. Apply 900 mV to input and adjust gain potentiometer to give 900 mV reading.
2. Linearity is measured as a difference from a straight line drawn through zero and positive full scale. Limits do not include ± 0.5 count bit digitizing error.
3. For applications where negative terminal 10 is not operated at terminal 7 potential, a return path of not more than 100 kΩ resistance must be provided for input bias currents.
4. The common-mode input voltage above ground cannot exceed + 0.2 V if the full input signal range of 999 mV is required at terminal 11. That is, terminal 11 may not operate higher than 1.2 V positive with respect to ground or 0.2 V negative with respect to ground. If the maximum input signal is less than 999 mV, the common-mode input voltage may be raised accordingly.

CA3162, CA3162A

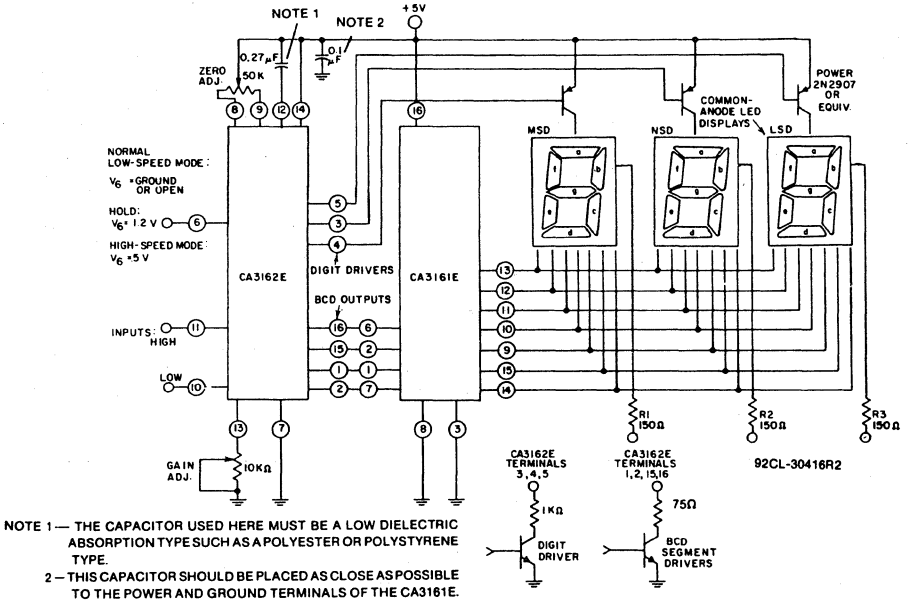
Circuit Description

The functional block diagram of the CA3162E is shown in Fig. 1. The heart of the system is the V/I converter and reference-current generator. The V/I converter converts the input voltage applied between terminals 10 and 11 to a current that charges the integrating capacitor on terminal 12 for a predetermined time interval. At the end of the charging interval, the V/I converter is disconnected from the integrating capacitor, and a band-gap reference constant-current source of opposite polarity is connected. The number of clock counts that elapse before the charge is restored to its original value is a direct measure of the signal induced current. The restoration is sensed by the comparator, which in turn latches the counter. The count is then multiplexed to the BCD outputs.

The timing for the CA3162E is supplied by a 786-Hz ring oscillator, and the input at terminal 6 determines the sampling rate. A 5-V input provides a high-speed sampling rate (96 Hz), and grounding or floating terminal 6 provides a low-speed (4 Hz) sampling rate. When terminal 6 is fixed at + 1.2 V (by placing a 12 K resistor between terminal 6 and the + 5-V supply) a "hold" feature is available. While the CA3162E is in the hold mode, sampling continues at 4 Hz but the display data are latched to the last reading prior to the application of the 1.2 V. Removal of the 1.2 V restores continuous display changes. Note, however, that the sampling rate remains at 4 Hz.

Fig. 3 shows the timing of sampling and digit select pulses for the high-speed mode. Note that the basic A/D conversion process requires approximately 5 ms in both modes.

The "EEE" or "---" displays indicate that the range of the system has been exceeded in the positive or negative direction, respectively. Negative voltages to -99 mV are displayed with the minus sign in the MSD. The BCD code is 1010 for a negative overrange (---) and 1011 for a positive overrange (EEE).



NOTE 1 — THE CAPACITOR USED HERE MUST BE A LOW DIELECTRIC ABSORPTION TYPE SUCH AS A POLYESTER OR POLYSTYRENE TYPE.
2 — THIS CAPACITOR SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE POWER AND GROUND TERMINALS OF THE CA3161E.

Fig. 2 - Basic digital readout system using the CA3162E and the CA3161E.

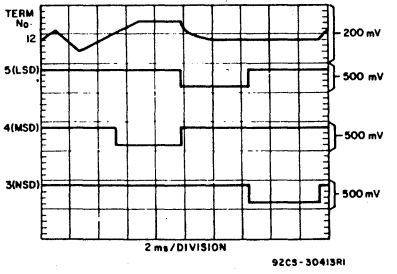


Fig. 3 - High speed mode timing diagram.

CA3162E Liquid Crystal Display (LCD) Application

Fig. 4 shows the CA3162E in a typical LCD application. LCD's may be used in favor of LED displays in applications requiring lower power dissipation, such as battery-operated equipment, or when visibility in high-ambient-light conditions is desired.

Multiplexing of LCD digits is not practical, since LCD's must be driven by an ac signal and the average voltage across each segment is zero. Three CD4056B liquid-crystal decoder/drivers are therefore used. Each CD4056B contains an input latch so that the BCD data for each digit may be latched into the decoder using the inverted digit-select outputs of the CA3162E as strobes.

The capacitors on the outputs of inverters G3 and G4 filter out the decode spikes on the MSD and NSD signals. The capacitors and pull-up resistors connected to the MSD, NSD and LSD outputs are there to shorten the digit drive signal thereby providing proper timing for the CD4056B latches.

Inverters G1 and G2 are used as an astable multivibrator to provide the ac drive to the LCD backplane. Inverters G3, G4, and G5 are the digit-select inverters and require pull-up resistors to interface the open-collector outputs of the CA3162E to CMOS logic. The BCD outputs of the CA3162E may be connected directly to the corresponding CD4056B inputs (using pull-up resistors). In this arrangement, the CD4056B decodes the negative sign (-) as an "L" and the positive overload indicator (E) as an "H".

The circuit as shown in Fig. 4, using G7, G8 and G9, will decode the negative sign (-) as a negative sign (-), and the positive overload indicator (E) as "H".

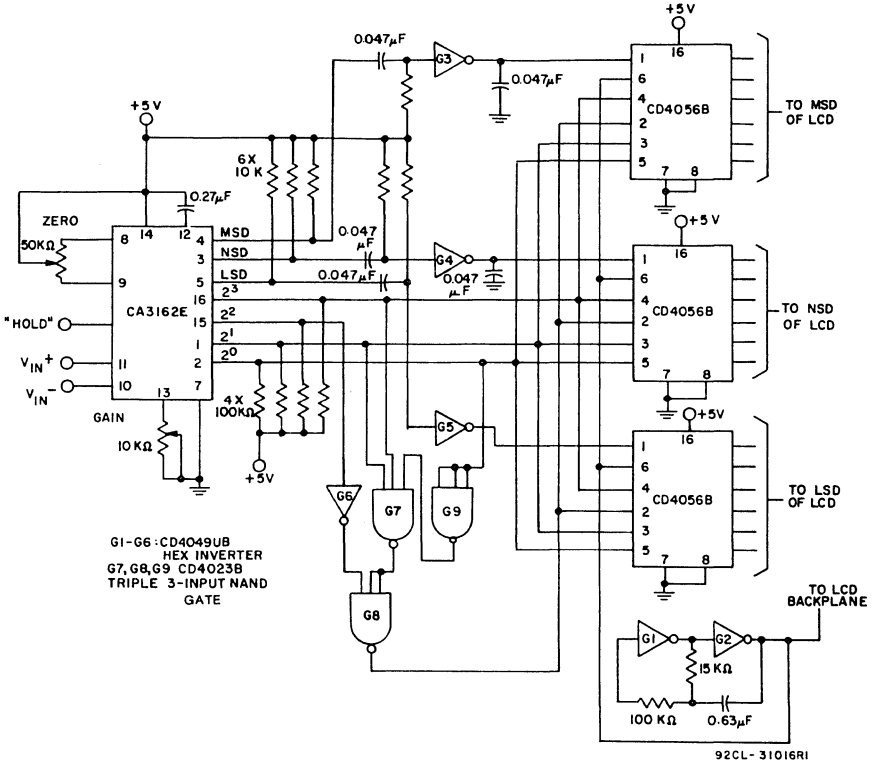


Fig. 4 - Typical LCD application.

CA3162, CA3162A

CA3162E Common-Cathode, LED Display Application

Fig. 5 shows the CA3162E connected to a CD4511B decode/driver to operate a common-cathode LED display. Unlike the CA3161E, the CD4511B remains blank for all BCD codes greater than nine. After 999 mV the display blanks rather than displaying EEE, as with the CA3161E. When displaying negative voltage, the first digit remains blank instead of (-), and during a negative or positive overrange the display blanks.

The additional logic shown within the dotted area of Fig. 5 restores the negative sign (-), allowing the display of negative numbers as low as -99 mV. Negative overrange is indicated by a negative sign (-) in the MSD position. The rest of the display is blanked. During a positive overrange, only segment b of the MSD is displayed. One inverter from the CD4049B is used to operate the decimal points. By connecting the inverter input to either the MSD or NSD line either DP1 or DP2 will be displayed. Fig. 7 shows the P.C. board and component placement.

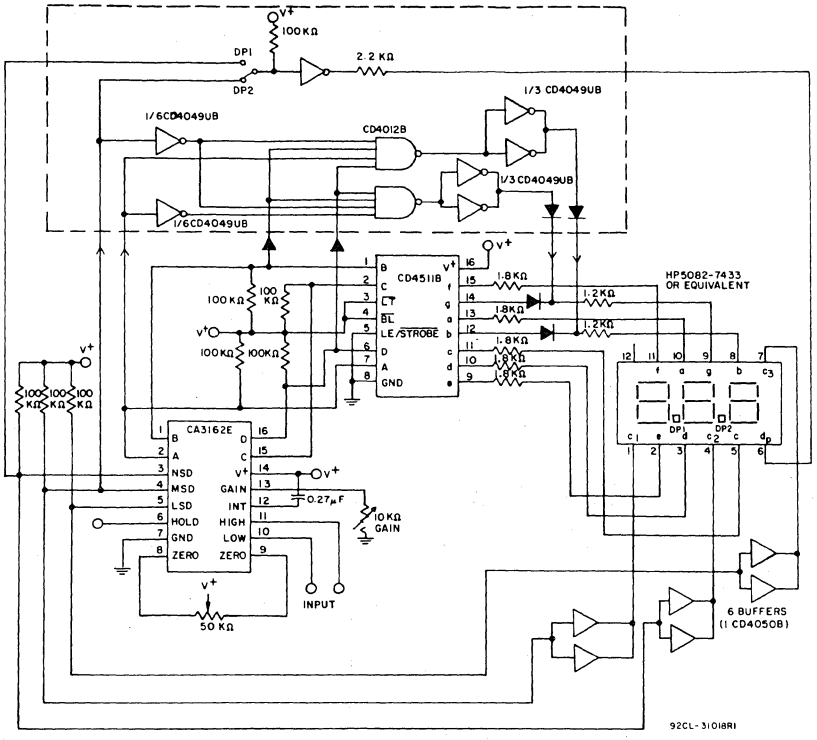
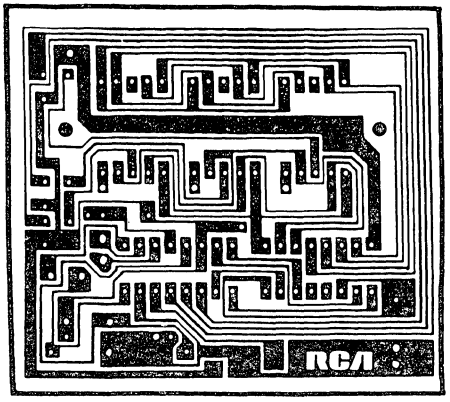
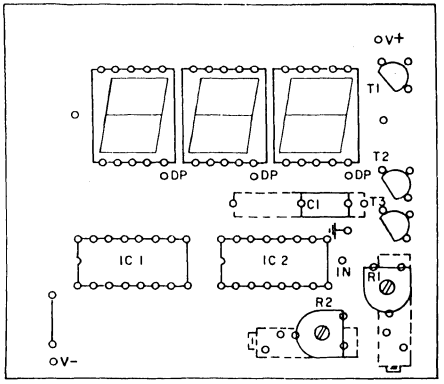


Fig. 5 - Typical common-cathode LED application.

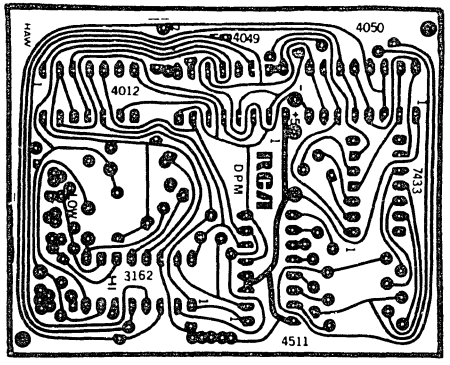


92CS-32692

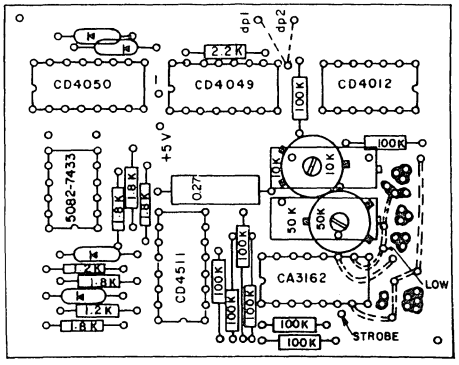


92CS-32693

Fig. 6 - P.C. board template (actual size ± 3%) and component layout guide for circuit shown in Fig. 2.*



92CS-32691

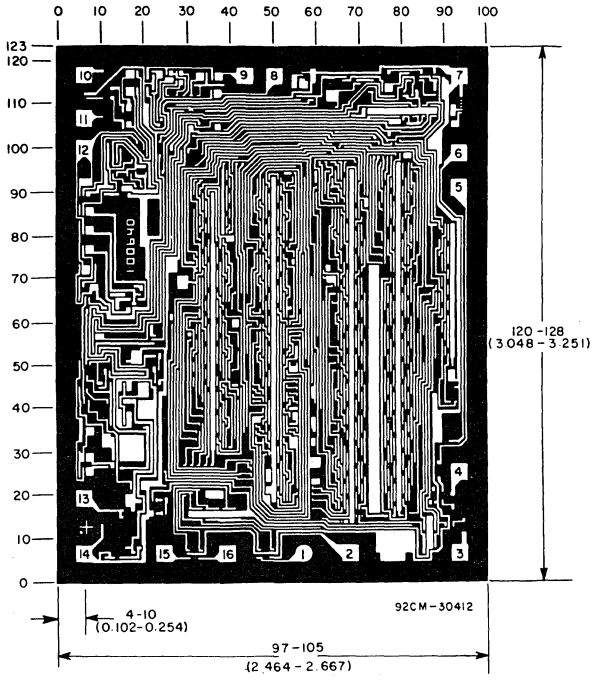


92CS-32694

Fig. 7 - P.C. board template (actual size ± 3%) and component layout guide for circuit shown in Fig. 5.

**P.C. board courtesy ETS. Velleman P.V.B.A., St. Amandsberg, Belgium*

CA3162, CA3162A



Dimensions and pad layout for CA3162H chip.

The photographs and dimensions of each Linear chip represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

ORDERING INFORMATION

Part Number	Temperature Range	Package
CA3162E	0°C to + 70°C	16-Pin Plastic Dip
CA3162AE	−40°C to + 85°C	16-Pin Plastic Dip

HARRIS SEMICONDUCTOR

ICL8052/ICL71C03
ICL8068/ICL71C03
Precision 4½ Digit A/D Converter

GENERAL DESCRIPTION

The ICL8052 or ICL8068/ICL71C03 chip pairs with their multiplexed BCD output and digit drivers are ideally suited for the visual display DVM/DPM market. The outstanding 4½ digit accuracy, 200.00 mV to 2.0000V full scale capability, auto-zero and auto-polarity combine with true ratiometric operation, almost ideal differential linearity and time-proven dual slope conversion. Use of these chip pairs eliminates clock feedthrough problems, and avoids the critical board layout usually required to minimize charge injection.

When only 2000 counts of resolution are required the 71C03 can be wired for 3½ digits and give up to 30 readings/second making it ideally suited for a wide variety of applications.

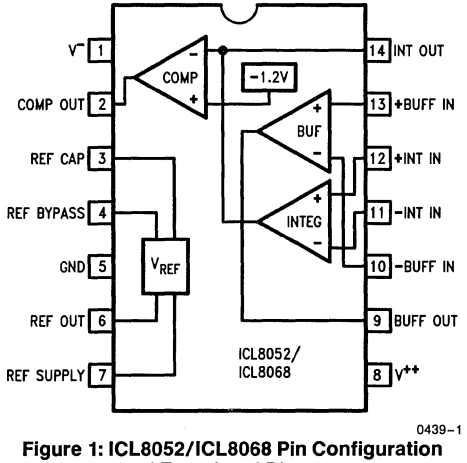
The ICL71C03 is an improved CMOS plug-in replacement for the ICL7103 and should be used in all new designs.

ORDERING INFORMATION

Part Number	Temp. Range	Package
ICL8052CPD	0°C to +70°C	14-Pin Plastic DIP
ICL8052CDD	0°C to +70°C	14-Pin Ceramic DIP
ICL8052CJD	0°C to +70°C	14-Pin CERDIP
ICL8052ACPD	0°C to +70°C	14-Pin Plastic DIP
ICL8052ACDD	0°C to +70°C	14-Pin Ceramic DIP
ICL8052ACJD	0°C to +70°C	14-Pin CERDIP
ICL8068CDD	0°C to +70°C	14-Pin Ceramic DIP
ICL8068ACDD	0°C to +70°C	14-Pin Ceramic DIP
ICL8068ACJD	0°C to +70°C	14-Pin CERDIP
ICL71C03CPI	0°C to +70°C	28-Pin Plastic DIP
ICL71C03ACPI	0°C to +70°C	28-Pin Plastic DIP

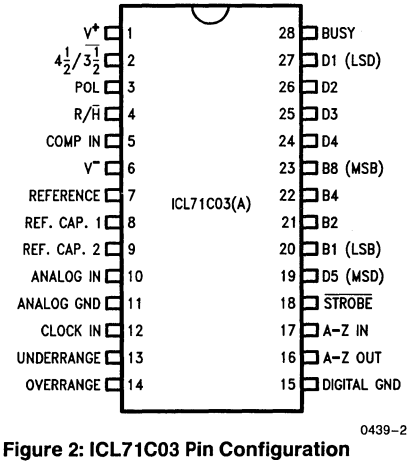
FEATURES

- **Typically Less Than 2 μV p-p Noise (200.00 mV Full Scale, ICL8068)**
- **Accuracy Guaranteed to ±1 Count over Entire ±20,000 Counts (2.0000V Full Scale)**
- **Guaranteed Zero Reading for 0V Input**
- **True Polarity at Zero Count for Precise Null Detection**
- **Single Reference Voltage Required**
- **Over-range and Under-Range Signals Available for Auto-Ranging Capability**
- **All Outputs TTL Compatible**
- **Medium Quality Reference (40 ppm typical) on Board**
- **Blinking Display Gives Visual Indication of Overrange**
- **Six Auxillary Inputs/Outputs Are Available for Interfacing to UARTs, Microprocessors or Other Complex Circuitry**
- **5 pA Input Current Typical (8052A)**



0439-1

Figure 1: ICL8052/ICL8068 Pin Configuration and Functional Diagram



0439-2

Figure 2: ICL71C03 Pin Configuration

NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL71C03, ICL8068/ICL71C03

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 500 mW
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10 Sec.) ..... 300°C

8052, 8068

Supply Voltage ..... ±18V
Differential Input Voltage
(8068) ..... ±30V
(8052) ..... ±6V
Input Voltage (Note 2) ..... ±15V
Output Short Circuit Duration,
All Outputs (Note 3) ..... Indefinite
Operating Temperature ..... 0°C to +70°C

71C03

Power Supply Voltage (GND to V^+) 6.5V
Negative Supply Voltage (GND to V^-) ..... −17V
Analog Input Voltage (Note 4) ..... V^+ to V^-
Digital Input Voltage
(Note 5) ..... (GND − 0.3V) to (V^+ + 0.3V)

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Units
I_{INL} I_{INH}	Clock In, Run/$\overline{Hold}$, 4½/$\overline{3½}$	V_{IN} = 0 V_{IN} = +5V		0.2 0.1	0.6 10	mA μA
I_{INL} I_{INH}	Comp. In Current	V_{IN} = 0 V_{IN} = +5V		0.1 0.1	10 10	μA μA
V_{INTH}	Threshold Voltage			2.5		V
V_{OL}	All Outputs	I_{OL} = 1.6 mA		0.25	0.40	V
V_{OH}	B_1, B_2, B_4, B_8 D_1, D_2, D_3, D_4, D_5	I_{OH} = −1 mA	2.4	4.2		V
V_{OH}	Busy, $\overline{Strobe}$, Over-range, Under-range Polarity	I_{OH} = −10 μA	4.9	4.99		V
$r_{DS(on)}$	Switches 1, 3, 4, 5, 6			400		Ω
$r_{DS(on)}$	Switch 2			1200		Ω
$I_{D(off)}$	Switch Leakage (All)			2		pA
V^+	+5V Supply Range		+4	+5	+6	V
V^-	−15V Supply Range		−5	−15	−18	V
I^+	+5V Supply Current	fclk = 0		1.1	3.0	mA
I^-	−15V Supply Current	fclk = 0		0.8	3.0	mA
C_{PD}	Power Dissipation Capacitance	vs. Clock Freq		40		pF
	Clock Freq. (Note 6)		DC	2000	1200	kHz

NOTES 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10 mW/°C.

2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

4: Input voltages may exceed the supply voltages provided the input current is limited to ±100 μA.

5: Connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latchup. For this reason it is recommended that the power supply to the 71C03 be established before any inputs from sources not on that supply are applied.

6: This specification relates to the clock frequency range over which the ICL71C03(A) will correctly perform its various functions. See the "Max Clock Frequency" section under COMPONENT VALUE SELECTION for limitations on the clock frequency range in a system.

NOTE: All typical values have been characterized but are not tested.

ICL8068 ELECTRICAL CHARACTERISTICS

(V_{SUPPLY} = ±15V, T_A = 25°C unless otherwise specified)

Symbol	Characteristics	Test Conditions	8068			8068A			Units
			Min	Typ	Max	Min	Typ	Max	
EACH OPERATIONAL AMPLIFIER									
V_{OS}	Input Offset Voltage	V_{CM} = 0V		20	65		20	65	mV
I_{IN}	Input Current (either input) (Note 1)	V_{CM} = 0V		175	250		80	150	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
	Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V_{CM} = ±2V		110			110		dB
A_V	Large Signal Voltage Gain	R_L = 50 kΩ	20,000			20,000			V/V
SR	Slew Rate			6			6		V/μs
GBW	Unity Gain Bandwidth			2			2		MHz
I_{SC}	Output Short-Circuit Current			5			5		mA
COMPARATOR AMPLIFIER									
A_{VOL}	Small-Signal Voltage Gain	R_L = 30 kΩ			4000				V/V
$+V_O$	Positive Output Voltage Swing		+12	+13		+12	+13		V
$-V_O$	Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
VOLTAGE REFERENCE									
V_O	Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
R_O	Output Resistance			5			5		Ω
TC	Temperature Coefficient			50			40		ppm/°C
V_{SUPPLY}	Supply Voltage ($V^{++} - V^{-}$)		±10		±16	±10		±16	V
I_{SUPPLY}	Supply Current Total				14		8	14	mA

ICL8052 ELECTRICAL CHARACTERISTICS

(V_{SUPPLY} = ±15V, T_A = 25°C unless otherwise specified)

Symbol	Characteristics	Test Conditions	8052			8052A			Units
			Min	Typ	Max	Min	Typ	Max	
EACH OPERATIONAL AMPLIFIER									
V_{OS}	Input Offset Voltage	V_{CM} = 0V		20	75		20	75	mV
I_{IN}	Input Current (either input) (Note 1)	V_{CM} = 0V		5	50		2	10	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
	Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V_{CM} = ±2V		110			110		dB
A_V	Large Signal Voltage Gain	R_L = 50 kΩ	20,000			20,000			V/V
SR	Slew Rate			6			6		V/μs
GBW	Unity Gain Bandwidth			1			1		MHz
I_{SC}	Output Short-Circuit Current			20			20		mA

NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL71C03, ICL8068/ICL71C03

ICL8052 ELECTRICAL CHARACTERISTICS

(V_{SUPPLY} = ±15V, T_A = 25°C unless otherwise specified) (Continued)

Symbol	Characteristics	Test Conditions	8052			8052A			Units
			Min	Typ	Max	Min	Typ	Max	
COMPARATOR AMPLIFIER									
A_{VOL}	Small-Signal Voltage Gain	R_L = 30 kΩ		4000					V/V
$+V_O$	Positive Output Voltage Swing		+12	+13		+12	+13		V
$-V_O$	Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
VOLTAGE REFERENCE									
V_O	Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
R_O	Output Resistance			5			5		Ω
TC	Temperature Coefficient			50			40		ppm/°C
V_{SUPPLY}	Supply Voltage ($V^{++} - V^-$)		±10		±16	±10		±16	V
I_{SUPPLY}	Supply Current Total			6	12		6	12	mA

NOTES 1: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + R_{\theta JA}Pd$ where $R_{\theta JA}$ is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

2: This is the only component that causes error in dual-slope converter.

SYSTEM ELECTRICAL CHARACTERISTICS: 8068/71C03

(V^{++} = +15V, V^+ = +5V, V^- = −15V, T_A = 25°C, Clock Frequency Set for 3 Reading/Sec.)

Characteristics	Conditions	8068/71C03(1)			8068A/71C03A(2)			Units
		Min	Typ	Max	Min	Typ	Max	
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.00 mV	−000.0	±000.0	+000.0	−000.00	±000.00	+000.00	Digital Reading
Ratiometric Reading (Note 3)	$V_{IN} = V_{REF}$ Full Scale = 2.000V	+0.999	+1.000	+1.001	+0.9999	+1.0000	+1.0001	Digital Reading
Linearity Over ± Full Scale (Error of Reading from Best Straight Line)	$-2V \le V_{IN} \le +2V$		0.2	1		0.5	1	COUNTS
Differential Linearity (Difference between Worse Case Step of Adjacent Counts and Ideal Step)	$-2V \le V_{IN} \le +2V$		0.01			0.01		COUNTS
Rollover Error (Difference in Reading for Equal Positive & Negative Voltage Near Full Scale)	$-V_{IN} \equiv +V_{IN} \approx 2V$		0.2	1		0.5	1	COUNTS
Noise (P-P Value Not Exceeded 95% of Time)	V_{IN} = 0V Full Scale = 200.0 mV		3			2		μV
Leakage Current at Input	V_{IN} = 0V		200	300		100	200	pA
Zero Reading Drift	V_{IN} = 0V $0 \le T_A \le 50°C$ (Note 4)		1	5		0.5	2	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = +2V $0 \le T_A \le 50°C$ (Note 4) (Ext. Ref. 0 ppm/°C)		3	15		2	5	ppm/°C

NOTE: All typical values have been characterized but are not tested.

SYSTEM ELECTRICAL CHARACTERISTICS: 8052/71C03

(V^{++} = +15V, V^{+} = +5V, V^{-} = −15V, T_A = 25°C, Clock Frequency Set for 3 Reading/Sec.)

Characteristics	Conditions	8068/71C03(1)			8068A/71C03A(2)			Units
		Min	Typ	Max	Min	Typ	Max	
Zero Input Reading	V_{IN} = 0.0V Full Scale = 2.000V	−0.000	±0.000	+0.000	−0.0000	±0.0000	+0.0000	Digital Reading
Ratiometric Reading (Note 3)	$V_{IN} = V_{REF}$ Full Scale = 2.000V	+0.999	+1.000	+1.001	+0.9999	+1.0000	+1.0001	Digital Reading
Linearity Over ± Full Scale (Error of Reading from Best Straight Line)	$-2V \le V_{IN} \le +2V$		0.2	1		0.5	1	COUNTS
Differential Linearity (Difference between Worse Case Step of Adjacent Counts and Ideal Step)	$-2V \le V_{IN} \le +2V$		0.01			0.01		COUNTS
Rollover Error Difference in Reading for Equal Positive & Negative Voltage Near Full Scale)	$-V_{IN} \equiv +V_{IN} \approx 2V$		0.2	1		0.5	1	COUNTS
Noise (P–P Value not Exceeded 95% of Time)	V_{IN} = 0V Full Scale = 200.0 mV Full Scale = 2.000V		20 50			 30		μV
Leakage Current at Input	V_{IN} = 0V		5	30		3	10	pA
Zero Reading Drift	V_{IN} = 0V $0 \le T_A \le 70°C$		1	5		0.5	2	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = +2V $0 \le T_A \le 70°C$ (Ext. Ref. 0 ppm/°C)		3	15		2	5	ppm/°C

NOTES 1: Tested in 3½ digit (2,000 count) circuit shown in Figure 7, clock frequency 12 kHz. Pin 2 71C03 connected to GND.

2: Tested in 4½ digit (20,000 count) circuit shown in Figure 7, clock frequency 120 kHz. Pin 2 71C03A open.

3: Tested with a low dielectric absorption integrating capacitor. See Component Selection Section.

4: The temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the 8068.

NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL71C03, ICL8068/ICL71C03

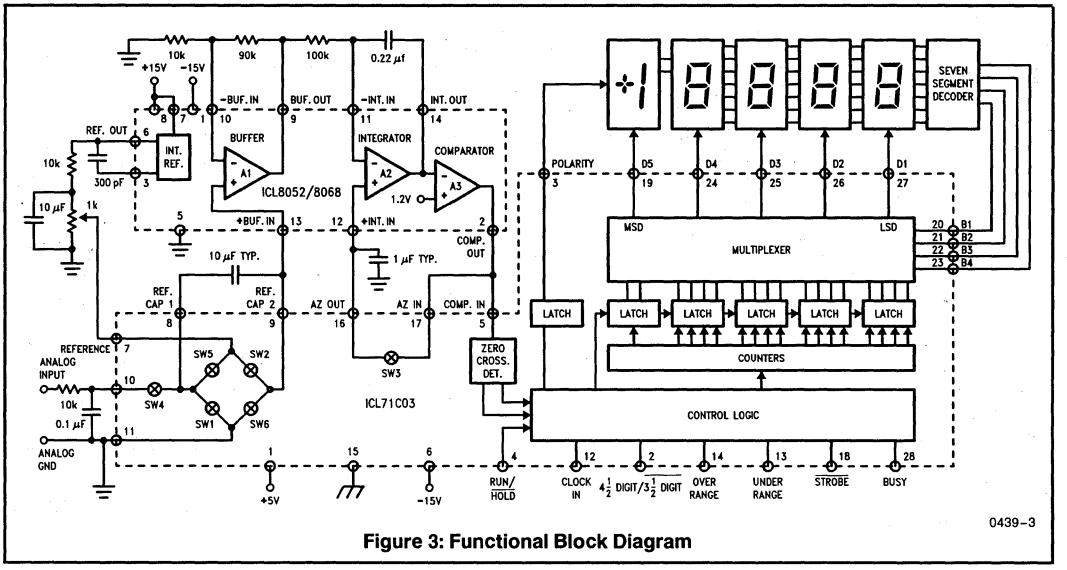


Figure 3: Functional Block Diagram

DETAILED DESCRIPTION

Analog Section

Figure 4 shows the equivalent Circuit of the Analog Section of both the ICL71C03/8052 and the ICL71C03/8068 in the 3 different phases of operation. If the RUN/$\overline{\text{HOLD}}$ pin is left open or tied to V^+, the system will perform conversions at a rate determined by the clock frequency: 40,002 at 4½ digit and 4002 at 3½ digit clock periods per cycle (see Figure 5 for details of conversion timing.

1. AUTO-ZERO PHASE I (Figure 4A)

During Auto-Zero, the input of the buffer is connected to V_{REF} through switch 2, and switch 3 closes a loop around the integrator and comparator, the purpose of which is to charge the auto-zero capacitor until the integrator output does not change with time. Also, switches 1 and 2 recharge the reference capacitor to V_{REF}.

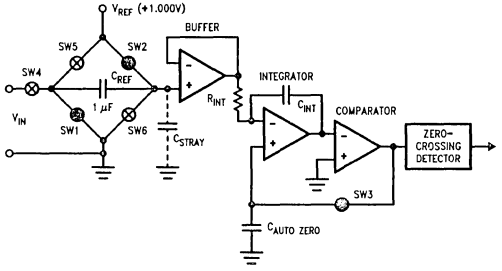
2. INPUT INTEGRATE PHASE II (Figure 4B)

During Input Integrate the auto-zero loop is opened and the ANALOG INPUT is connected to the BUFFER INPUT through switch 4 and C_{REF}. If the input signal is zero, the buffer, integrator and comparator will see the same voltage that existed in the previous state (Auto-Zero). Thus, the integrator output will not change but will remain stationary during the entire Input Integrate cycle. If V_{IN} is not equal to zero, an unbalanced condition exists compared to the Auto-Zero phase, and the integrator will generate a ramp whose slope is proportional to V_{IN}. At the end of this phase, the sign of the ramp is latched into the polarity F/F.

3. DEINTEGRATE PHASE II (Figures 4C and 4D)

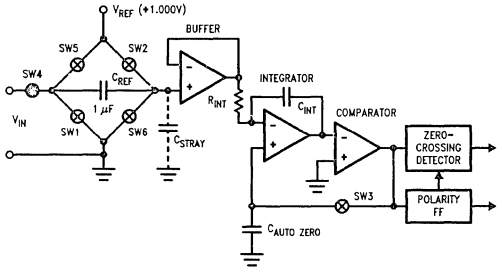
During the Deintegrate phase, the switch drive logic uses the output of the polarity F/F in determining whether to close switch 6 or 5. If the input signal is positive, switch 6 is closed and a voltage which is V_{REF} more negative than during Auto-Zero is impressed on the BUFFER INPUT. Negative Inputs will cause $+2(V_{REF})$ to be applied to the BUFFER INPUT via switch 5. Thus, the reference capacitor generates the equivalent of a (+) or (−) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to the zero-crossing point established in Phase I. The time, or number of counts, required to do this is proportional to the input voltage. Since the Deintegrate phase can be twice as long as the Input Integrate phase, the input voltage required to give a full scale reading is 2 V_{REF}.

NOTE: All typical values have been characterized but are not tested.



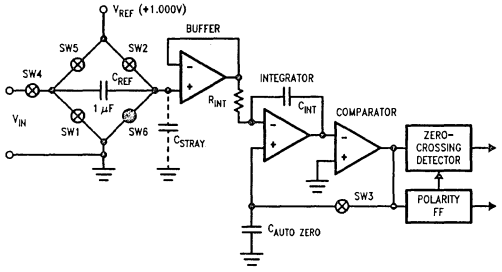
0439-4

Figure 4A: Phase I Auto-Zero



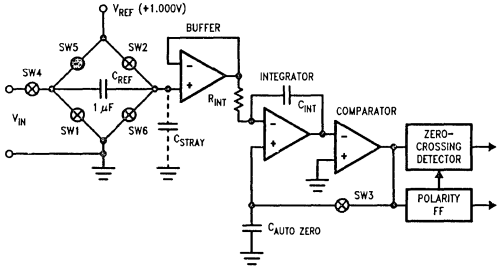
0439-6

Figure 4B: Phase II Integrate Input



0439-5

Figure 4C: Phase III + Deintegrate



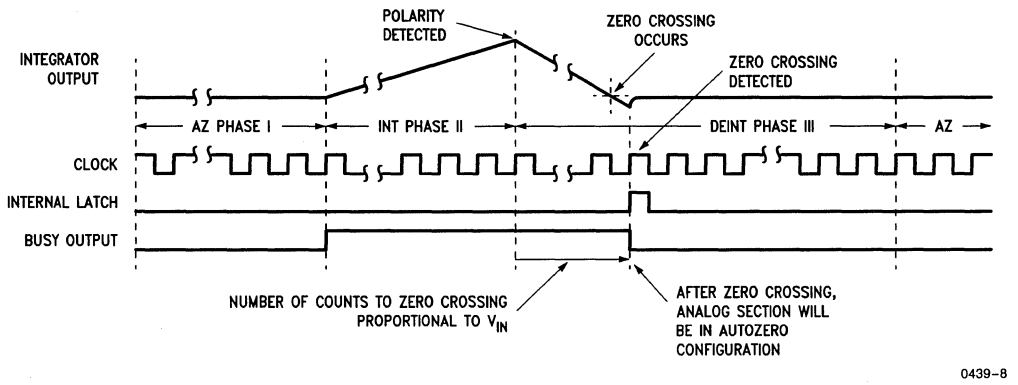
0439-7

Figure 4D: Phase III − Deintegrate

Figure 4: Analog Section of Either ICL8052 or ICL8068 with ICL71C03

NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL71C03, ICL8068/ICL71C03



COUNTS			
	Phase I	**Phase II**	**Phase III**
4½ Digit	10,001	10,000	20,001
3½ Digit	1,001	1,000	2,001

Figure 5: Conversion Timing

Zero-Crossing Flip-Flop

Figure 6 shows the problem that the zero-crossing F/F is designed to solve.

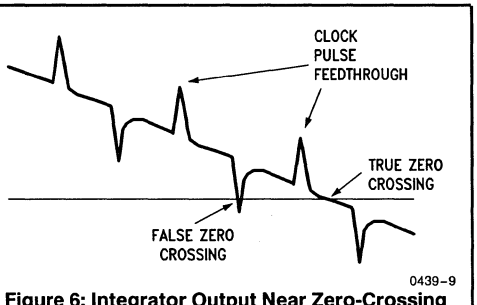


Figure 6: Integrator Output Near Zero-Crossing

The integrator output is approaching the zero-crossing point where the count will be latched and the reading displayed. For a 20,000 count instrument, the ramp is changing approximately 0.50 mV per clock pulse (10V max integrator output divided by 20,000 counts). The clock pulse feedthrough superimposed upon this ramp would have to be less than 100 μV peak to avoid causing significant errors.

The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore the counter is disabled for one clock pulse at the beginning of phase 3. This one count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one count delay at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2, so that true ratiometric readings result.

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

Digital Section

The 71C03 includes several pins which allow it to operate conveniently in more sophisticated systems. These include:

1. 4½/3½ (Pin 2). When high (or open) the internal counter operates as a full 4½ decade counter, with a complete measurement cycle requiring 40,002 counts. When held low, the least significant decade is cleared and the clock is fed directly into the next decade. A measurement cycle now requires only 4,002 clock pulses. All 5 digit drivers are active in either case, with each digit lasting 200 counts with Pin 2 high (4½ digit) and 20 counts for Pin 2 low (3½ digit).

2. RUN/HOLD (Pin 4). When high (or open) the A/D will free-run with equally spaced measurement cycles every 40,002/4,002 clock pulses. If taken low, the converter will continue the full measurement cycle that it is doing and then hold this reading as long as Pin 4 is held low. A short positive pulse (greater than 300 ns) will now initiate a new measurement cycle beginning with up to 10,001/1,001 counts of auto zero. Of course if the pulse occurs before the full measurement cycle (40,002/4,002 counts) is completed, it will not be recognized and the converter will simply complete the measurement it is doing. An external indication that a full measurement cycle has been completed is that the first STROBE pulse (see below) will occur 101/11 counts after the end of this cycle. Thus, if RUN/HOLD is low and has been low for at least 101/11 counts, the converter is holding and ready to start a new measurement when pulsed high.

3. STROBE (Pin 18). This is a negative-going output pulse that aids in transferring the BCD data to external latches, UARTs or microprocessors. There are 5 negative-going STROBE pulses that occur in the center of each of the digit drive pulses and occur once and only once for each measurement cycle starting 101/11 pulses after the end of the full measurement cycle. Digit 5 (MSD) goes high at the end of the measurement cycle and stays on for 201/21 counts. In the center of this digit pulse (to avoid race conditions between changing BCD and digit drives) the first STROBE pulse goes negative for ½ clock pulse width. Similary, after Digit 5, Digit 4 goes high (for 200/20 clock pulses) and 100/10 pulses later the STROBE goes negative for the second time. This continues through Digit 1 (LSD) when the fifth and last STROBE pulse is sent. The digit drive will continue to scan (unless the previous signal was over-range) but no additional STROBE pulses will be sent until a new measurement is available.

4. BUSY (Pin 28). BUSY goes high at the beginning of signal integrate and stays high until the first clock pulse after zero-crossing (or after end of measurement in the case of an OVER-RANGE). The internal latches are enabled (i.e., loaded) during the first clock pulse after BUSY and are latched at the end of this clock pulse. The circuit automatically reverts to auto-zero when not BUSY so it may also be considered an A–Z signal. A very simple means for transmitting the data down a single wire pair from a remote location would be to AND BUSY with clock and subtract 10,001/1,001 counts from the number of pulses received—as mentioned previously there is one "NO-count" pulse in each Reference Integrate cycle.

5. OVER-RANGE (Pin 4). This pin goes positive when the input signal exceeds the range (20,000/2,000) of the converter. The output F–F is set at the end of BUSY and is reset to zero at the beginning of Reference Integrate in the next measurement cycle.

6. UNDER-RANGE (Pin 13). This pin goes positive when the reading is 9% of range or less. The output F–F is set at the end of BUSY (if the new reading is 1800/180 or less) and is reset at the beginning of Signal Integrate of the next reading.

7. POLARITY (Pin 3). This pin is positive for a positive input signal. It is valid even for a zero reading. In other words, +0000 means the signal is positive but less than the least significant bit. The converter can be used as a null detector by forcing equal (+) and (−) readings. The null at this point should be less than 0.1 LSB. This output becomes valid at the beginning of Reference Integrate and remains correct until it is revalidated for the next measurement.

8. Digit Drives (Pins 19, 24, 25, 26 and 27). Each digit drive is a positive-going signal which lasts for 200/20 clock pulses. The scan sequence is D_5 (MSD), D_4, D_3, D_2 and D_1 (LSD). All five digits are scanned even when operating in the 3½ digit mode, and this scan is continuous unless an OVER-RANGE occurs. Then all Digit drives are blanked from the end of the STROBE sequence until the beginning of Reference Integrate, at which time D_5 will start the scan again. This gives a blinking display as a visual indication of OVER-RANGE.

9. BCD (Pins 20, 21, 22 and 23). The Binary coded decimal bit B_8, B_4, B_2 and B_1 are positive logic signals that go on simultaneously with the Digit driver.

NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL71C03, ICL8068/ICL71C03

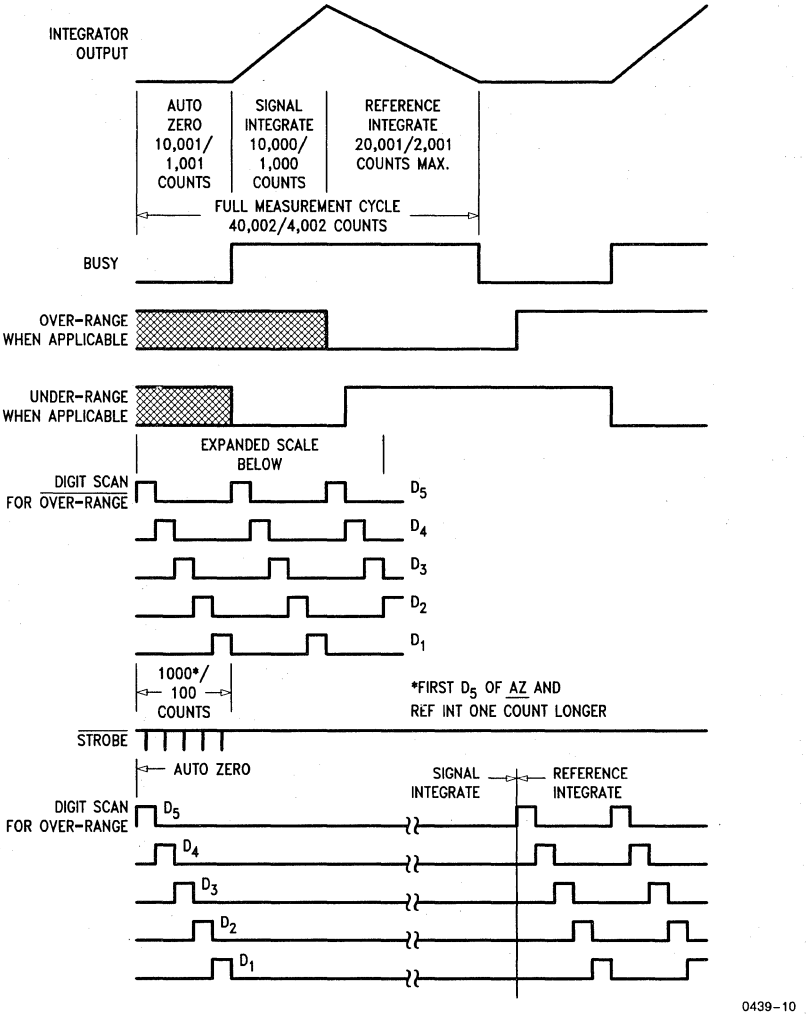


Figure 7: Timing Diagram for Outputs

NOTE: All typical values have been characterized but are not tested.

COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. This current should be small compared to the output short circuit current such that thermal effects are kept to a minimum and linearity is not affected. Values of 5 μA to 40 μA give good results with a nominal of 20 μA. The exact value may be chosen by

$$R_{INT} = \frac{\text{Full Scale Voltage}}{20\ \mu A}$$

***NOTE:** If gain is used in the buffer amplifier then—

$$R_{INT} = \frac{\text{(Buffer Gain) (Full Scale Voltage)}}{20\ \mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor is selected to give 9V swing for full scale inputs. This is a compromise between possibly saturating the integrator (at +14V) due to tolerance build-up between the resistor, capacitor and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. In general, the value of C_{INT} is given by

$$C_{INT} = \frac{\left[\frac{10{,}000\ (4\frac{1}{2}\ \text{Digit})}{1000\ (3\frac{1}{2}\ \text{Digit})} \times \text{Clock Period}\right] \times (20\ \mu A)}{\text{Integrator Output Voltage Swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale 1.0000, and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may be used in less critical applications.

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system, with a larger value capacitor giving less noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

When gain is used in the buffer amplifier the reference capacitor should be substantially larger than the auto-zero capacitor. As a rule of thumb, the reference capacitor should be approximately the gain times the value of the auto-zero capacitor. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that an external high quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

Buffer Gain

At the end of the auto-zero interval, the instantaneous noise voltage on the auto-zero capacitor is stored and subtracted from the input voltage while adding to the reference voltage during the next cycle. The result of this is that the noise voltage is effectively somewhat greater than the input noise voltage of the buffer itself during integration. By introducing some voltage gain into the buffer, the effect of the auto-zero noise (referred to the input) can be reduced to the level of the inherent buffer noise. This generally occurs with a buffer gain of between 3 and 10. Further increase in buffer gain merely increases the total offset to be handled by the auto-zero loop, and reduces the available buffer and integrator swings, without improving the noise performance of the system. The circuit recommended for doing this with the ICL8068/ICL71C03 is shown in Figure 8.

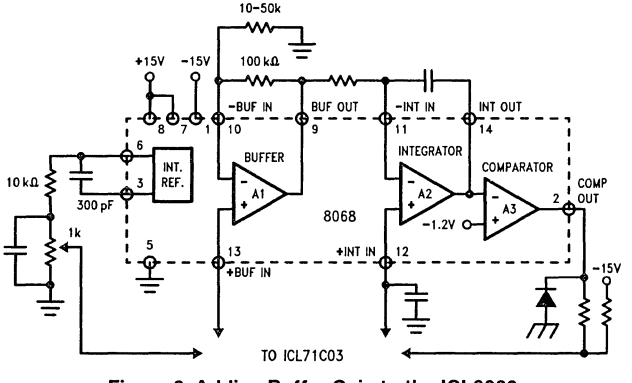


Figure 8: Adding Buffer Gain to the ICL8068

NOTE: All typical values have been characterized but are not tested.

ICL8052 vs ICL8068

The ICL8052 offers significantly lower input leakage currents than the ICL8068, and may be found preferable in systems with high input impedances. However, the ICL8068 has substantially lower noise voltage, and is the device of choice for systems where noise is a limiting factor, particularly in low signal level conditions.

Max Clock Frequency

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit is no exception, even though it is entirely NPN with an open-loop gain-bandwidth product of 300 MHz. The comparator output follows the integrator ramp with a 3 μs delay, and at a clock frequency of 160 kHz (6 μs period) half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50 μV input, 1 to 2 with 150 μV, 2 to 3 at 250 μV etc. This transition at midpoint is considered desirable by most users. However, if the clock frequency is increased appreciably above 160 kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, clock rates of up to approximately 1 MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

The minimum clock frequency is established by leakage on the auto-zero and reference caps. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 300 kHz, 200 kHz, 150 kHz, 120 kHz, 100 kHz, 40 kHz, 33⅓ kHz, etc. should be selected. For 50 Hz rejection, oscillator frequencies of 250 kHz, 166⅔ kHz, 125 kHz, 100 kHz, etc. would be suitable. Note that 100 kHz (2.5 readings/second) will reject both 50 Hz and 60 Hz.

The clock used should be free from significant phase or frequency jitter. A simple two-gate oscillator and one based on a CMOS 7555 timer are shown in the Applications section. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

APPLICATIONS

Specific Circuits Using the 8068/71C03 8052/71C03

Figure 9 shows the complete circuit for a ±4½ digit (±200.0 mV full scale) A/D converter with LED readout using the internal reference of the 8068/52. If an external reference is used, the reference supply (pin 7) should be connected to ground and the 300 pF reference cap deleted. The circuit also shows a typical RC input filter. Depending on the application, the time-constant of this filter can be made faster, slower, or the filter deleted completely. The ½ digit LED is driven from the 7 segment decoder, with a zero reading blanked by connecting a D5 signal to RBI input of the decoder.

A voltage translation network is connected between the comparator output of the 8068/52 and the auto-zero input of the 71C03. The purpose of this network is to assure that, during auto-zero, the output of the comparator is at or near the threshold of the 71C03 logic (+2.5V) while the auto-zero capacitor is being charged to V_{REF} (+100.0 mV for a 200.0 mV instrument). Otherwise, even with zero volts in, some reference integrate period would be required to drive the comparator output to the threshold level. This would show up as an equivalent offset error. Once the divider network has been selected, the unit-to-unit variation should contribute less than a tenth of a count error. A second feature is the back-to-back diodes, used to lower the noise. In the normal operating mode they offer a high impedance and long integrating time constant to any noise pulses charging the auto-zero cap. At startup or recovery from an overload, their impedance is low to large signals so that the cap can be charged up in one auto-zero cycle. The buffer gain does not have to be set precisely at 10 since the gain is used in both the integrate and deintegrate phase. For scale factors other than 200.00 mV the gain of the buffer should be changed to give a ±2V buffer output. For 2.0000V full scale this means unity gain and for 20,000 mV (1 μV resolution) a gain of 100 is necessary. Not all 8068As can operate properly at a gain of 100 since their offset should be less than 10 mV in order to accommodate the auto-zero circuitry. However, for devices selected with less than 10 mV offset, the noise performance is reasonable with approximately 1.5 μV near full scale. On all scales less than 200.00 mV, the voltage translation network should be made adjustable as an offset trim.

NOTE: All typical values have been characterized but are not tested.

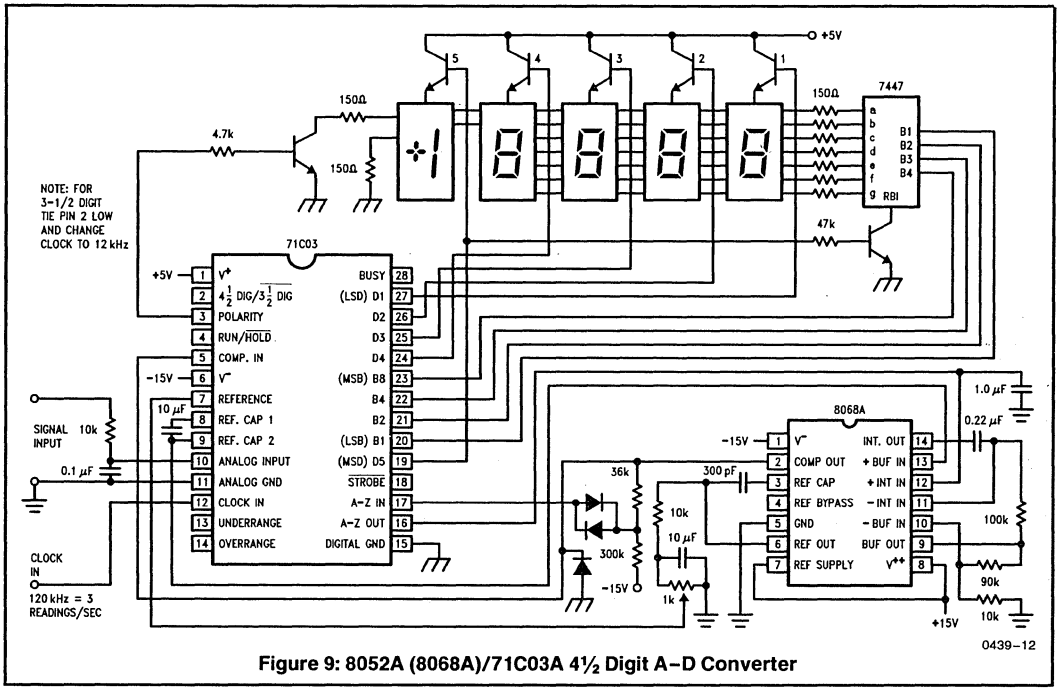


Figure 9: 8052A (8068A)/71C03A 4½ Digit A-D Converter

The auto-zero cap should be 1 μF for all scales and the reference capacitor should be 1 μF times the gain of the buffer amplifier. At this value if the input leakages of the 8052/8068 are equal, the droop effects will cancel giving zero offset. This is especially important at high temperature. Some typical component values are shown in the table below. For 3½ digit conversion use 12 kHz clock.

$V^{++} = +15V$, $V^{+} = 5V$, $V^{-} = -15V$

Clock Freq. = 120 kHz (4½ Digit) or 12 kHz (3½ Digit)

Specification	Valve			Units
Full Scale V_{IN}	20	200	2000	mV
Buffer Gain $\frac{(RB1 + RB2)}{RB2}$	100*	10	1	V/V
R_{INT}	100	100	100	kΩ
C_{INT}	0.22	0.22	0.22	μF
C_{AZ}	1.0	1.0	1.0	μF
C_{REF}	10	10	1.0	μF
V_{REF}	10	100	1000	mV
Resolution (4½ Digit)	1	10	100	μV

*Note comment on offset limitations above. Buffer gain does not improve ICL8052 noise performance adequately.

NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL71C03, ICL8068/ICL71C03

A suitable circuit for driving a plasma-type display is shown in Figure 10. The high voltage anode driver buffer is made by Dionics. The 3 AND gates and caps driving "BI" are needed for interdigit blanking of multiple-digit display elements, and can be omitted if not needed. The 2K and 3K resistors set the current levels in the display. A similar arrangement can be used with "Nixie"® tubes.

Nixie® is a registered trademark of Burroughs Corporation.

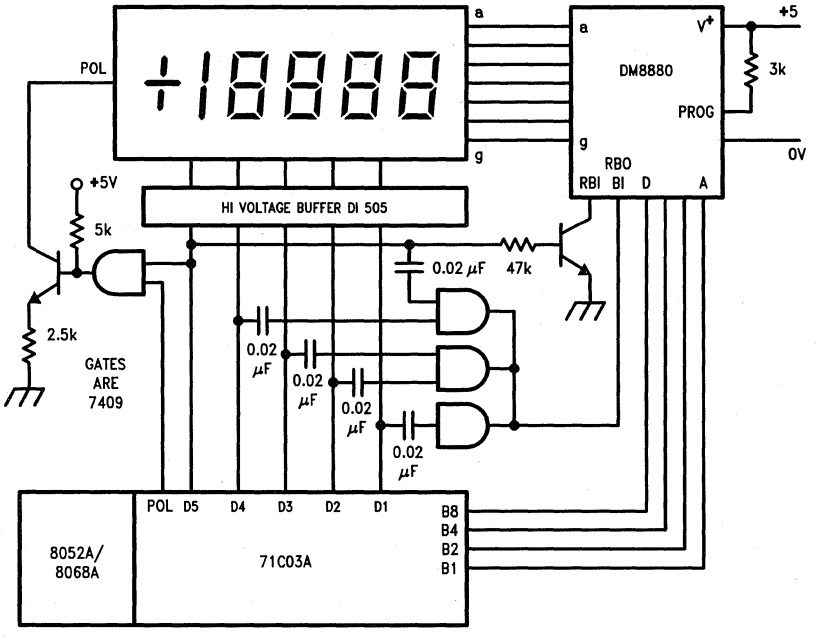


Figure 10: ICL8052-8068/71C03A Plasma Display Circuit

NOTE: All typical values have been characterized but are not tested.

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of 8068 or 8052/71C03A circuits, especially in high sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line. Both of the above circuits have considerable current flowing in the digital ground returns from drivers, etc. A recommended connection sequence for the ground lines is shown in Figure 11.

Other Circuits for Display Applications

Popular LCD displays can be interfaced to the Output of the ICL71C03 with suitable display drivers, such as the ICM7211A as shown in Figure 12. A standard CMOS 4000 series LCD driver circuit is used for displaying the ½ digit, the polarity, and the "overrange" flag. A similar circuit can be used with the ICM7212A LED driver. Of course, another full driver circuit could be ganged to the one shown if required. This would be useful if additional annunciators were needed.

Figure 12 shows the complete circuit for a 4½ digit (±2.000V) A/D, again using the internal reference of the 8052A/8068A.

Figure 13 shows a more complicated circuit for driving LCD displays. Here the data is latched into the ICM7211 by the $\overline{\text{STROBE}}$ signal and "Overrange" is indicated by blanking the 4 digits. A clock oscillator circuit using the ICM7555 CMOS timer is shown. Some other suitable clock circuits are suggested in Figures 14 and 15. The 2-gate circuit should use CMOS gates to maintain good power supply rejection.

A problem sometimes encountered with the 8052/68/71C03 A/D is that of gross over-voltage applied to the input. Voltage in excess of ±2.000V may cause the integrator output to saturate. When this occurs, the integrator can no longer source (or sink) the current required to hold the summing junction (Pin 11) at the voltage stored on the auto zero capacitor. As a result, the voltage across the integrator capacitor decreases sufficiently to give a false voltage reading. This problem can also show up as large-signal instability on overrange conditions. A simple solution to this problem is to use junction FET transistors across the integrator capacitor to source (or sink) current into the summing junction and prevent the integrator amplifier from saturating, as shown in Figure 16.

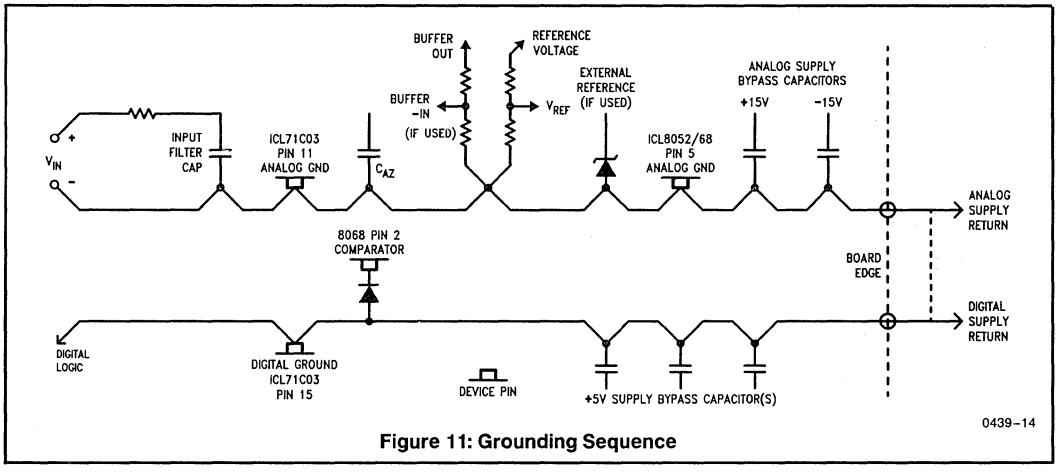


Figure 11: Grounding Sequence

NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL71C03, ICL8068/ICL71C03

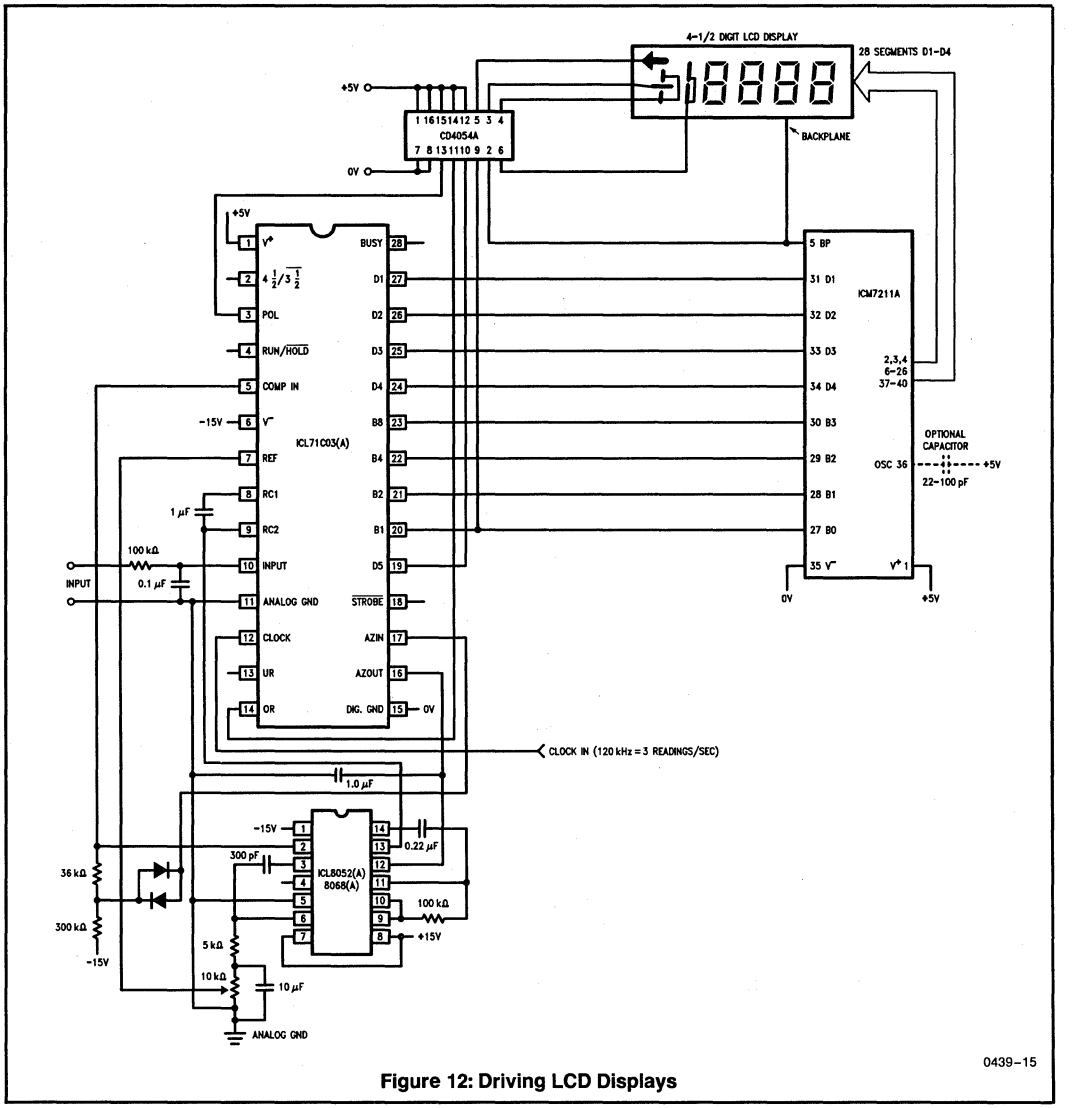


Figure 12: Driving LCD Displays

NOTE: All typical values have been characterized but are not tested.

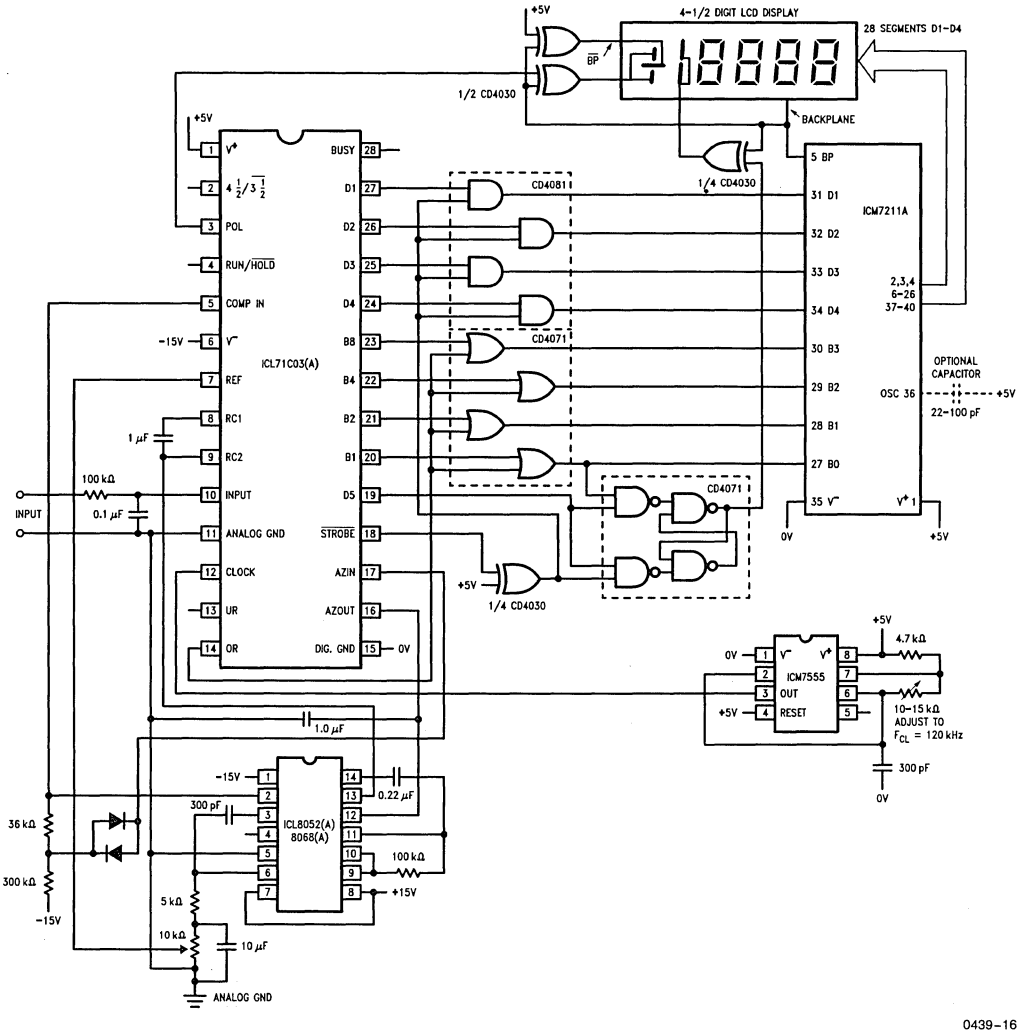


Figure 13: 4½ Digit LCD DPM with Digit Blanking on Overrange

NOTE: All typical values have been characterized but are not tested.

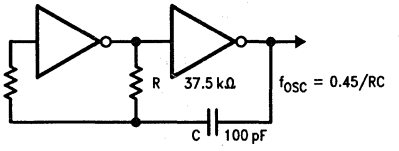


Figure 14: CMOS Oscillator

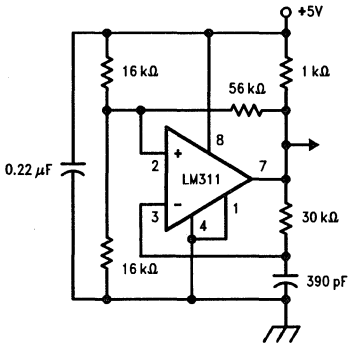


Figure 15: LM311 Oscillator

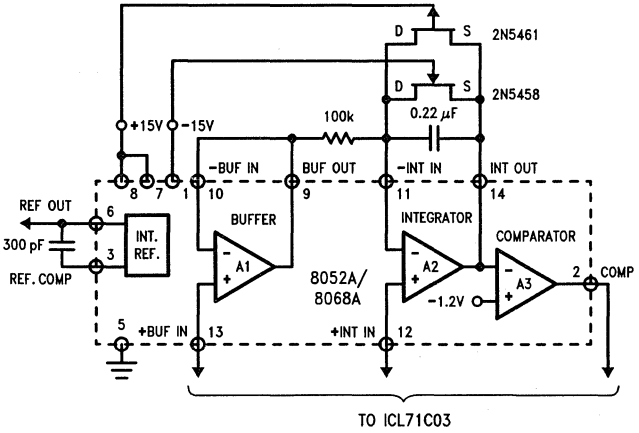


Figure 16: Gross Overvoltage Protection Circuit

INTERFACING WITH UARTS AND MICROPROCESSORS

Figure 17 shows a very simple interface between a free-running 8068/8052/71C03A and a UART. The five $\overline{\text{STROBE}}$ pulses start the transmission of the five data words. The digit 5 word is 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. Also the polarity is transmitted indirectly by using it to drive the Even Parity Enable Pin (EPE). It EPE of the receiver is held low, a parity flag at the receiver can be decoded as a positive signal, no flag as negative. A complex arrangement is shown in Figure 16. Here the UART can instruct the A/D to begin a measurement sequence by a word on RRI. The Busy signal resets the Data Ready Reset (DRR). Again $\overline{\text{STROBE}}$ starts the transmit sequence. A quad 2 input multiplexer is used to superimpose polarity, over-range, and under-range onto the D_5 word since in this instance it is known that $B_2 = B_4 = B_8 = 0$.

For correct operation it is important that the UART clock be fast enough that each word is transmitted before the next $\overline{\text{STROBE}}$ pulse arrives. Parity is locked into the UART at load time but does not change in this connection during an output stream.

Circuits to interface the 71C03(A) directly with three popular microprocessors are shown in Figures 19, 20 and 21. The main differences in the circuits are that the IM6100 with its 12 bit word capability can accept polarity, over-range, under-range, 4 bits of BCD and 5 digits simultaneously where the 8080/8048 and the MC6800 groups with 8 bit words need to have polarity, over-range and under-range multiplexed onto the Digit 5 word—as in the UART circuits. In each case the microprocessor can instruct the A/D when to begin a measurement and when to hold this measurement.

NOTE: All typical values have been characterized but are not tested.

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar

A017 "The Integrating A/D Converters," by Lee Evans

A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood

A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort

A028 "Building an Auto-Ranging DMM Using the 8052A/7103A A/D Converter Pair," by Larry Goff

R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976

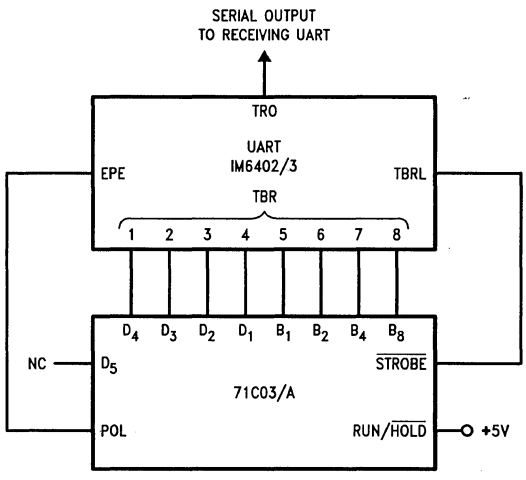


Figure 17: Simple 71C03/71C03A to UART Interface

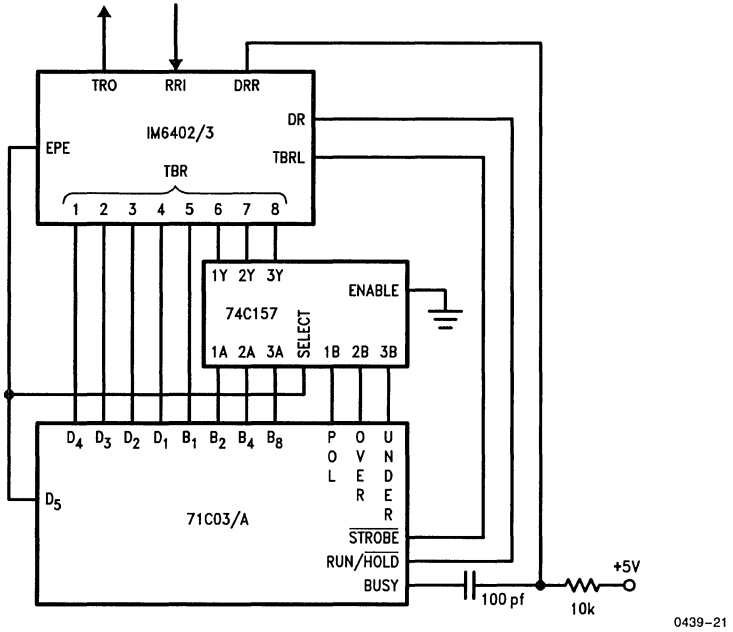


Figure 18: Complex 71C03/7103A to UART Interface

NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL71C03, ICL8068/ICL71C03

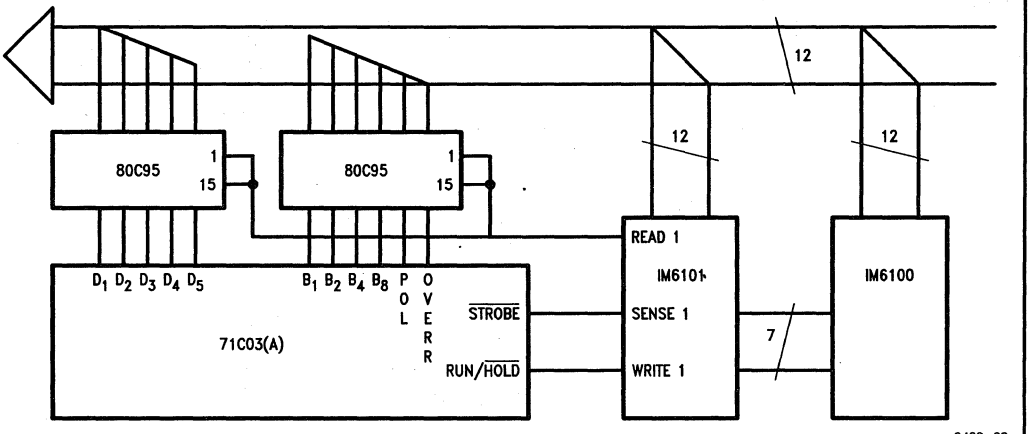


Figure 19: IM6100 to 71C03/71C03A Interface

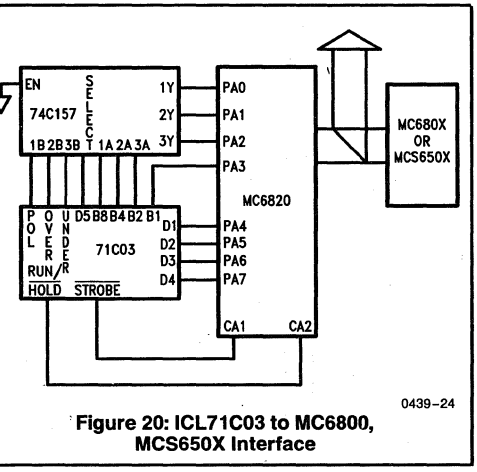


Figure 20: ICL71C03 to MC6800, MCS650X Interface

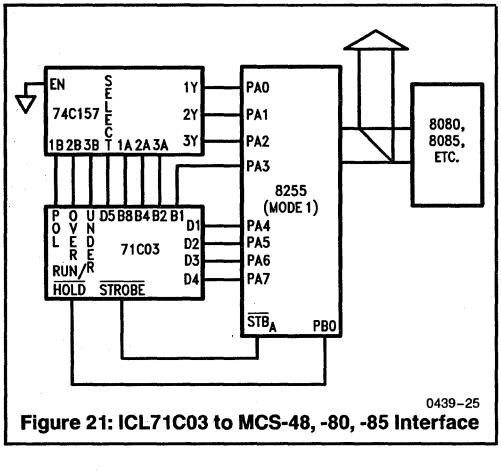


Figure 21: ICL71C03 to MCS-48, -80, -85 Interface

NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL71C03, ICL8068/ICL71C03

ICL71C03 with ICL8052/8068 INTEGRATING A/D CONVERTER EQUATIONS

The ICL71C03 does not have an internal crystal or RC oscillator. It has a clock input only.

Integration Period

$$t_{INT} = \frac{10{,}000}{f_{CLOCK}} \text{ (4½ Digit)}$$

$$t_{INT} = \frac{1{,}000}{f_{CLOCK}} \text{ (3½ Digit)}$$

Integration Clock Period

$$t_{CLOCK} = 1/f_{CLOCK}$$

60 Hz/50 Hz Rejection Criterion

$$t_{INT}/t_{60\ Hz} \text{ or } t_{INT}/t_{50\ Hz} = \text{Integer}$$

Optimum Integration Current

$$I_{INT} = 20.0\ \mu A$$

Full Scale Analog Input Voltage

$$V_{INFS} \text{ Typ.} = 200\ mV \text{ to } 2.0V = 2\ V_{REF}$$

Integrate Resistor

$$R_{INT} = \frac{\text{(Buffer Gain)} \times V_{INFS}}{I_{INT}}$$

Integrate Capacitor

$$C_{INT} = \frac{(t_{INT})\,(I_{INT})}{V_{INT}}$$

Integrator Output Voltage

$$V_{INT} = \frac{(t_{INT})\,(I_{INT})}{C_{INT}}$$

V_{INT} **Typically = 9.0V**

Display Count

$$\text{Count} = 10{,}000 \times \frac{V_{IN}}{V_{REF}} \text{ (4½ Digit)}$$

$$\text{Count} = 1{,}000 \times \frac{V_{IN}}{V_{REF}} \text{ (3½ Digit)}$$

NOTE: The 4½ digit mode's LSD will be output as a zero in the 3½ digit mode.

Output Type:

4 Nibbles BCD with Polarity and Overrange

Power Supply: ±15.0V, +5.0V

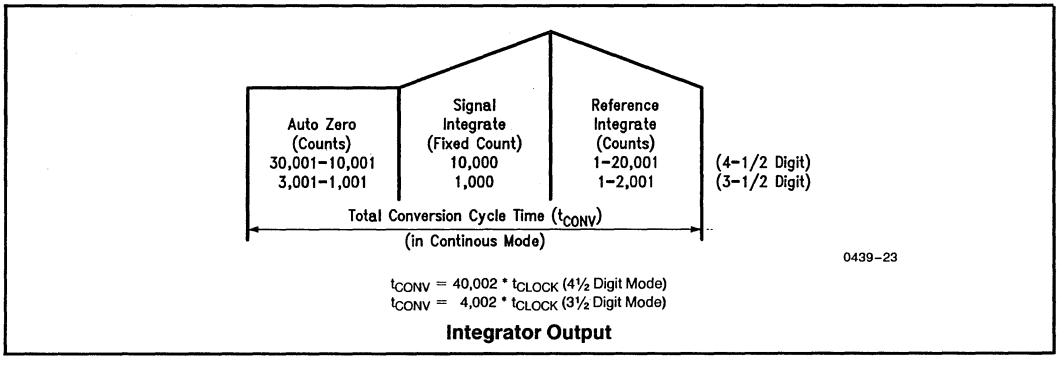
$V^{++} = +15.0V$
$V^{-} = -15.0V$
$V^{+} = +5.0V$

Auto Zero Capacitor Values

$0.01\ \mu F < C_{AZ} < 1.0\ \mu F$

Reference Capacitor Value

$C_{REF} = \text{(Buffer Gain)} \times C_{AZ}$



Integrator Output

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICL7106/ICL7107
3½-Digit LCD/LED Single-Chip A/D Converter

GENERAL DESCRIPTION

The Harris ICL7106 and 7107 are high performance, low power 3½-digit A/D converters containing all the necessary active devices on a single CMOS I.C. Included are seven-segment decoders, display drivers, a reference, and a clock. The 7106 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7107 will directly drive an instrument-size light emitting diode (LED) display.

The 7106 and 7107 bring together an unprecedented combination of high accuracy, versatility, and true economy. It features auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10 pA max., and rollover error of less than one count. True differential inputs and reference are useful in all systems, but give the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. Finally, the true economy of single power supply operation (7106), enables a high performance panel meter to be built with the addition of only 10 passive components and a display.

FEATURES

- **Guaranteed Zero Reading for 0 Volts Input on All Scales**
- **True Polarity at Zero for Precise Null Detection**
- **1pA Typical Input Current**
- **True Differential Input and Reference**
- **Direct Display Drive — No External Components Required — LCD ICL7106**
  — LED ICL7107
- **Low Noise - Less Than 15μV p-p**
- **On-Chip Clock and Reference**
- **Low Power Dissipation - Typically Less Than 10mW**
- **No Additional Active Circuits Required**
- **New Small Outline Surface Mount Package Available**

ORDERING INFORMATION

Part Number	Temperature Range	Package	Display Type
ICL7106CPL	0°C to +70°C	40-Pin Plastic DIP	Direct Drive LCD
ICL7106RCPL	0°C to +70°C	40-Pin Plastic DIP (Note 1)	Direct Drive LCD
ICL7106CM44	0°C to +70°C	44-Pin Surface Mount	Direct Drive LCD
ICL7107CPL	0°C to +70°C	40-Pin Plastic DIP	Common Anode LED
ICL7107RCPL	0°C to +70°C	40-Pin Plastic DIP (Note 1)	Common Anode LED
ICL7107CM44	0°C to +70°C	44-Pin Surface Mount	Common Anode LED

NOTE 1: "R" indicates device with reversed leads.

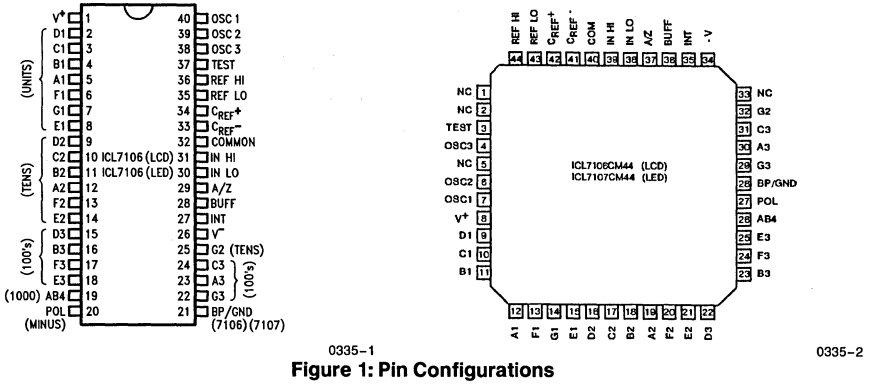


Figure 1: Pin Configurations

301650-004

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
- ICL7106, V^+ to V^- 15V
- ICL7107, V^+ to GND ..... +6V
- ICL7107, V^- to GND ..... −9V

Analog Input Voltage (either input)(Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input
- ICL7106 ..... TEST to V^+
- ICL7107 ..... GND to V^+

Power Dissipation (Note 2)
- Ceramic Package 1000mW
- Plastic Package-DIP 800mW
- Plastic Package-SOIC 600mW

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTES 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

ELECTRICAL CHARACTERISTICS (Note 3)

Characteristics	Test Conditions	Min	Typ	Max	Unit
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative inputs near Full Scale)	$-V_{IN} = +V_{IN} \cong$ 200.0mV	−1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200.0mV or full scale = 2.000V (Note 6)	−1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current Input	V_{IN} = 0 (Note 6)		1	10	pA
Zero Reading Drift	V_{IN} = 0 0° < T_A < 70°C (Note 6)		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° < T_A < 70°C (Ext. Ref. Oppm/°C) (Note 6)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7107)	V_{IN} = 0		0.8	1.8	mA
V^- Supply Current (7107 only)			0.6	1.8	mA
Analog Common Voltage (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With respect to Pos. Supply)	25kΩ between Common & Pos. Supply		80		ppm/°C

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Note 3) (Continued)

Characteristics	Test Conditions	Min	Typ	Max	Unit
7106 ONLY Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
7107 ONLY Segment Sinking Current (Except Pin 19 & 20)	V^+ = 5.0V Segment voltage = 3V	5	8.0		mA
(Pin 19 only)		10	16		mA
(Pin 20 only)		4	7		

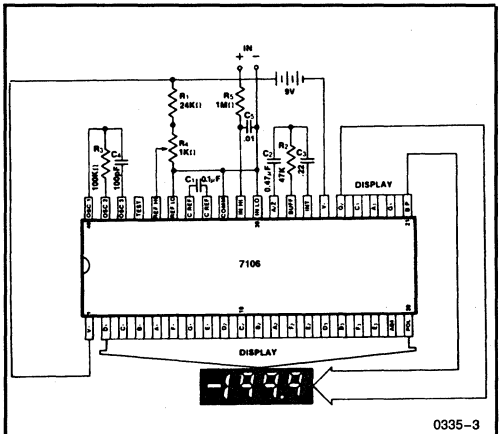
NOTES 3: Unless otherwise noted, specifications apply to both the 7106 and 7107 at T_A = 25°C, f_{clock} = 48kHz. 7106 is tested in the circuit of Figure 2. 7107 is tested in the circuit of Figure 3.

4: Refer to "Differential Input" discussion.

5: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

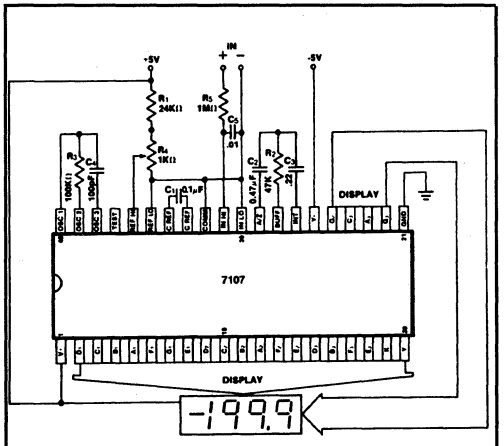
6: Not tested, guaranteed by design.

TEST CIRCUITS



0335-3

Figure 2: ICL7106 Test Circuit and Typical Application With Liquid Crystal Display Components Selected for 200mV Full Scale



0335-4

Figure 3: ICL7107 Test Circuit and Typical Application With LED Display Components Selected for 200mV Full Scale

NOTE: All typical values have been characterized but are not tested.

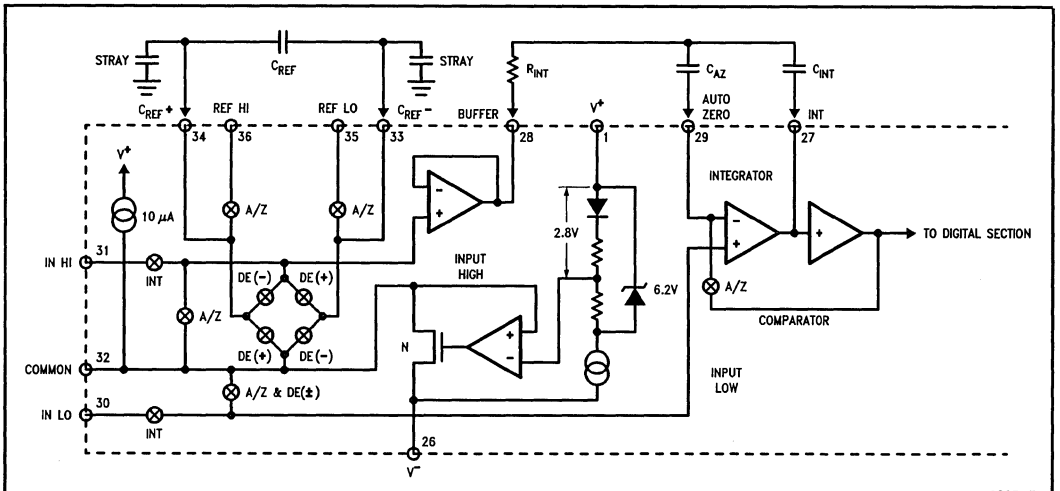


Figure 4: Analog Section of 7106/7107

DETAILED DESCRIPTION

Analog Section

Figure 4 shows the Analog Section for the ICL7106 and 7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A/Z), (2) signal integrate (INT) and (3) de-integrate (DE).

Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A/Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range: up to one volt from either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is $1000\left(\frac{V_{IN}}{V_{REF}}\right)$.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range, the system has a CMRR of 86 dB typical. However, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3 volts of either supply without loss of linearity. See Application Note A032 for a discussion of the effects of stray capacitance.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for positive or negative input voltage will give a roll-over error. However, by selecting the reference capacitor such that it is

NOTE: All typical values have been characterized but are not tested.

large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count worst case. (See Component Value Selection.)

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (7106) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (0.001%/V), low output impedance (≅15Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. With the 7107, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25 μV to 80μVp-p. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111(8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overrange condition. This is because overrange is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overrange and a nonoverrange count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7106, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Figure 5.

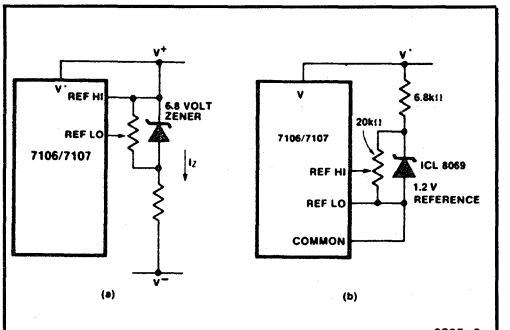


Figure 5: Using an External Reference

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently tied to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink approximately 30mA of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

TEST

The TEST pin serves two functions. On the 7106 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 6 and 7 show such an application. No more than a 1mA load should be applied.

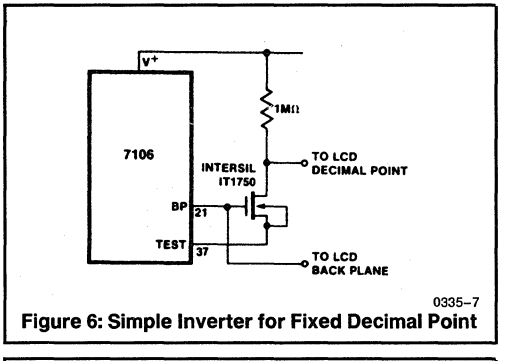


Figure 6: Simple Inverter for Fixed Decimal Point

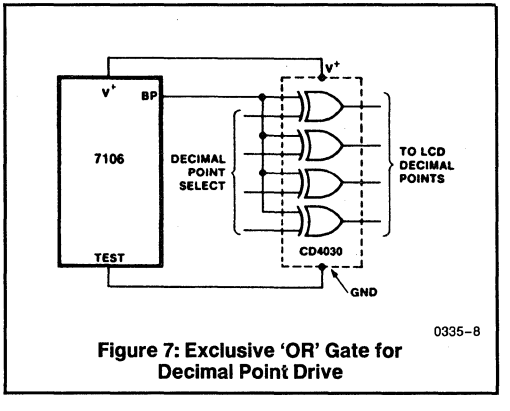


Figure 7: Exclusive 'OR' Gate for Decimal Point Drive

NOTE: All typical values have been characterized but are not tested.

DISPLAY FONT

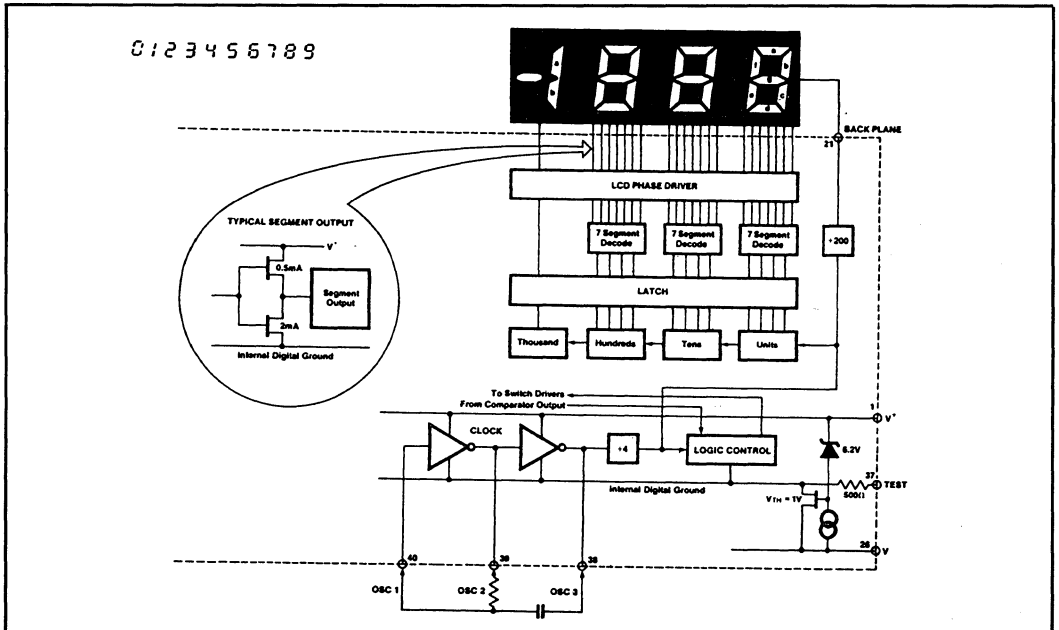


Figure 8: Digital Section 7106

0335-9

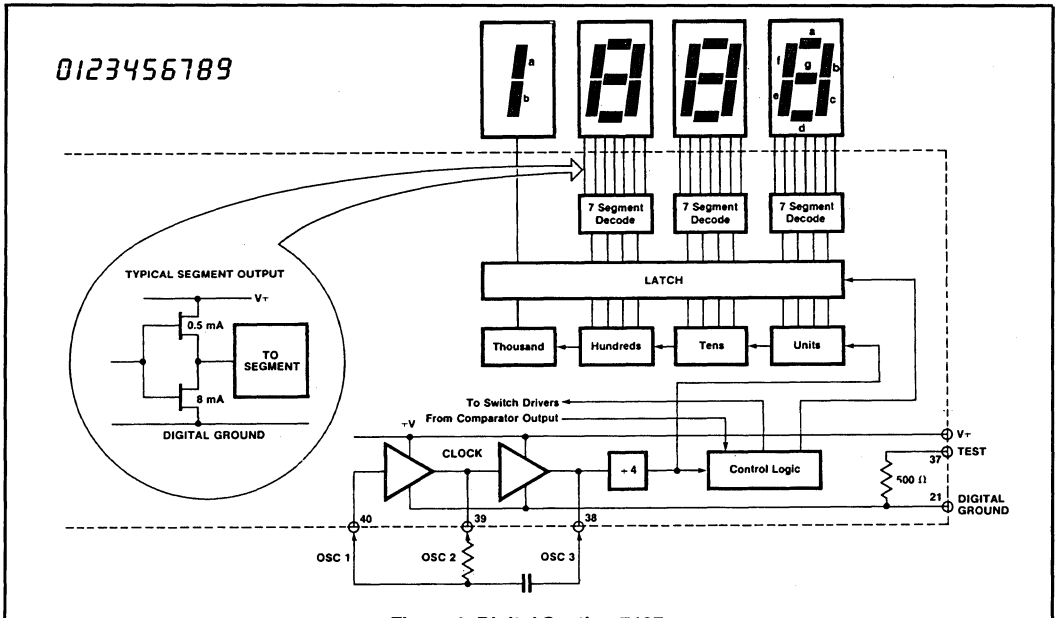


Figure 9: Digital Section 7107

0335-10

NOTE: All typical values have been characterized but are not tested.

The second function is a "lamp test". When TEST is pulled high (to V+) all segments will be turned on and the display should read — 1888. The TEST pin will sink about 10mA under these conditions.

Caution: on the 7106, in the lamp test mode, the segments have a constant DC voltage (no square-wave) and may burn the LCD display if left in this mode for several minutes.

DIGITAL SECTION

Figures 8 and 9 show the digital section for the 7106 and 7107, respectively. In the 7106, an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

Figure 9 is the Digital Section of the 7107. It is identical to the 7106 except that the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8 mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

In both devices, the polarity indication is "on" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

System Timing

Figure 10 shows the clocking arrangement used in the 7106 and 7107. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 counts (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33⅓kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 66⅔ kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

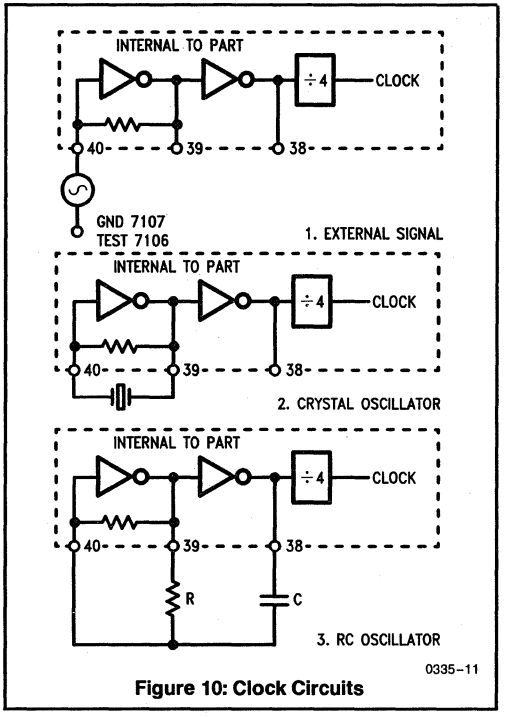


Figure 10: Clock Circuits

COMPONENT VALUE SELECTION

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 4μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 470kΩ is near optimum and similarly a 47kΩ for a 200.0 mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the 7106 or the 7107, when the analog COMMON is used as a reference, a nominal ±2 volt full scale integrator swing is fine. For the 7107 with ±5 volt supplies and analog COMMON tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.22μF and 0.10μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

NOTE: All typical values have been characterized but are not tested.

An additional requirement of the integrating capacitor is that it must have a low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.47μF capacitor is recommended. On the 2 volt scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0μF will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

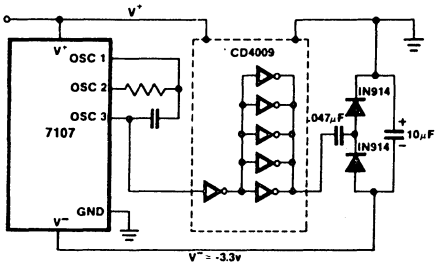
For all ranges of frequency a 100kΩ resistor is recommended and the capacitor is selected from the equation $f=\frac{0.45}{RC}$. For 48kHz clock (3 readings/second), C=100pF.

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN}=2V_{REF}$. Thus, for the 200.0mV and 2.000 volt scale, Vref should equal 100.0 mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select $V_{REF}=0.341V$. Suitable values for integrating resistor and capacitor would be 120kΩ and 0.22μF. This makes the system slightly quieter and also avoids a divider network on the input. The 7107 with ±5V supplies can accept input signals up to ±4V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN}\neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

7107 Power Supplies

The 7107 is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 11 shows this application. See ICL7660 data sheet for an alternative.



0335-12

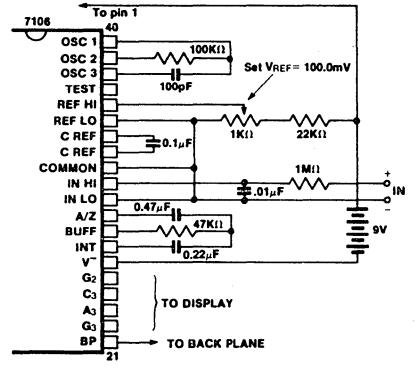
Figure 11: Generating Negative Supply from +5V

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts.
3. An external reference is used.

TYPICAL APPLICATIONS

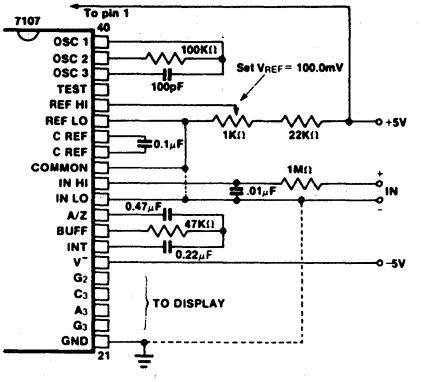
The 7106 and 7107 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.



0335-13

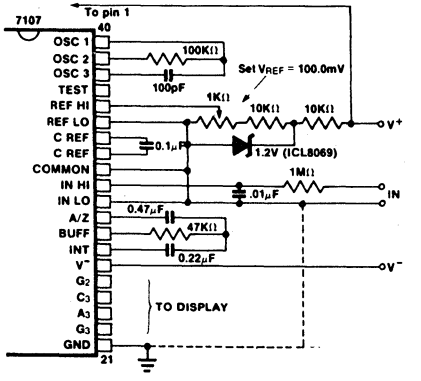
Figure 12: 7106 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second, floating supply voltage (9V battery).

NOTE: All typical values have been characterized but are not tested.



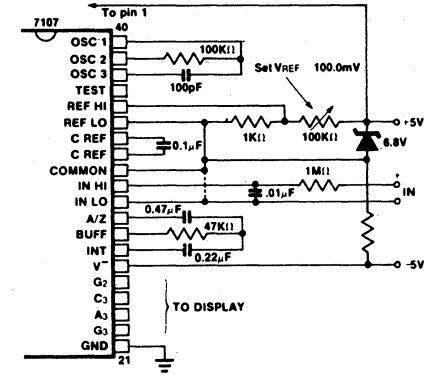
0335-14

Figure 13: 7107 using the internal reference. Values shown are for 200.0mV full scale, 3 readings per second. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)



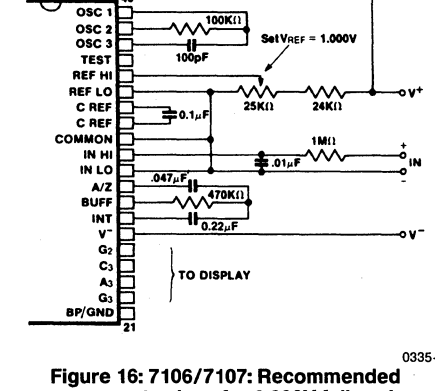
0335-15

Figure 14: 7107 with an external band-gap reference (1.2V type). IN LO is tied to COMMON, thus establishing the correct common mode voltage. If COMMON is not shorted to GND, the input voltage may float with respect to the power supply and COMMON acts as a pre-regulator for the reference. If COMMON is shorted to GND, the input is single ended (referred to supply ground) and the pre-regulator is over-ridden.



0335-16

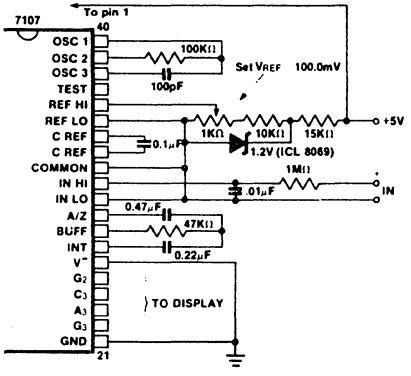
Figure 15: 7107 with Zener diode reference. Since low T.C. zeners have breakdown voltages ~ 6.8V, diode must be placed across the total supply (10V). As in the case of Figure 15, IN LO may be tied to either COMMON or GND.



0335-17

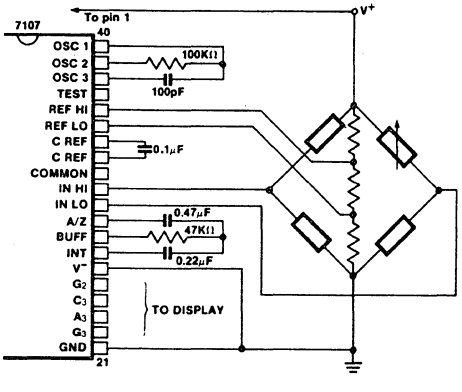
Figure 16: 7106/7107: Recommended component values for 2.000V full scale.

NOTE: All typical values have been characterized but are not tested.



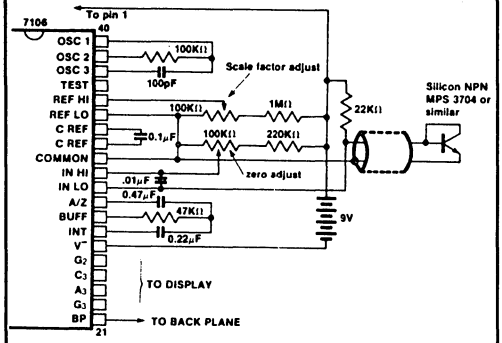
0335-18

Figure 17: 7107 operated from single +5V supply. An external reference must be used in this application, since the voltage between V+ and V− is insufficient for correct operation of the internal reference.



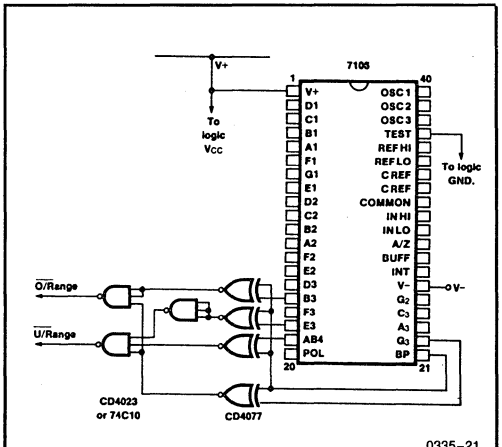
0335-19

Figure 18: 7107 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.



0335-20

Figure 19: 7106 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.



0335-21

Figure 20: Circuit for developing Underrange and Overrange signals from 7106 outputs.

NOTE: All typical values have been characterized but are not tested.

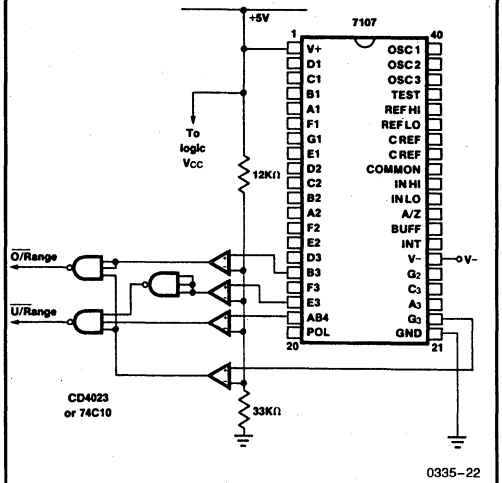


Figure 21: Circuit for developing Underrange and Overrange signals from 7107 outputs. The LM339 is required to ensure logic compatibility with heavy display loading.

APPLICATION NOTES

A016 "Selecting A/D Converters", by David Fullagar.

A017 "The Integrating A/D Converter", By Lee Evans.

A018 "Do's and Don'ts of Applying A/D Converters", by Peter Bradshaw and Skip Osgood.

A023 "Low Cost Digital Panel Meter Designs", by David Fullagar and Michael Dufort.

A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7/9 Family", by Peter Bradshaw.

A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106", by Larry Goff.

A052 "Tips for Using Single-Chip 3½-Digit A/D Converters", by Dan Watson.

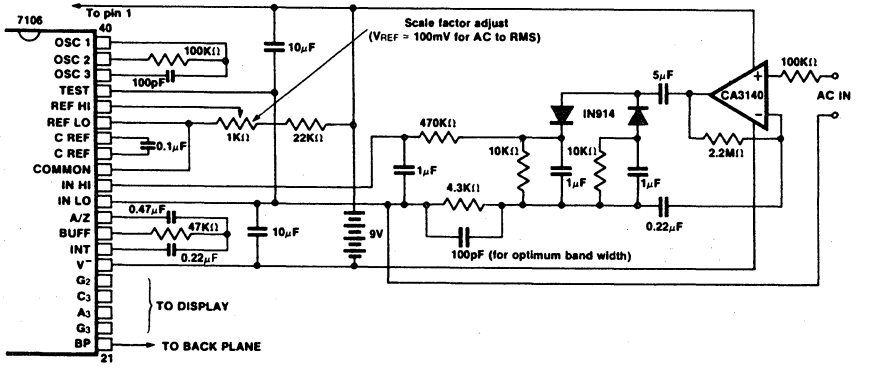
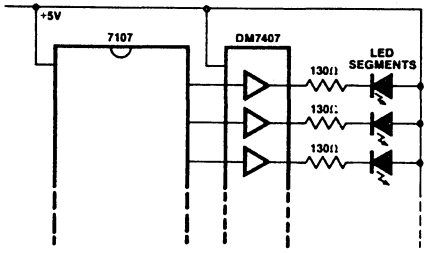


Figure 22: AC to DC Converter with 7106. TEST is used as a common mode reference level to ensure compatibility with most op-amps.

NOTE: All typical values have been characterized but are not tested.



0335-24

Figure 23: Display Buffering for increased drive current. Requires four DM7407 Hex Buffers. Each buffer is capable of sinking 40 mA.

NOTE: All typical values have been characterized but are not tested.

ICL7106/07 INTEGRATING A/D CONVERTER EQUATIONS

Oscillator Frequency
$f_{OSC} = 0.45/RC$
$C_{OSC} > 50pF$; $R_{OSC} > 50K\Omega$
f_{OSC} typ. = 48KHz

Oscillator Period
$t_{OSC} = RC/0.45$

Integration Clock Frequency
$f_{CLOCK} = f_{OSC}/4$

Integration Period
$t_{INT} = 1000 \times (4/f_{OSC})$

60/50 Hz Rejection Criterion
t_{INT}/t_{60Hz} or t_{INT}/t_{50Hz} = Integer

Optimum Integration Current
$I_{INT} = 4.0\mu A$

Full Scale Analog Input Voltage
V_{INFS} Typically = 200mV or 2.0V

Integrate Resistor

$$R_{INT} = \frac{V_{INFS}}{I_{INT}}$$

Integrate Capacitor

$$C_{INT} = \frac{(t_{INT})(I_{INT})}{V_{INT}}$$

Integrator Output Voltage Swing

$$V_{INT} = \frac{(t_{INT})(I_{INT})}{C_{INT}}$$

V_{INT} Maximum Swing:
$(V^- + 0.5V) < V_{INT} < (V^+ - 0.5V)$
V_{INT} typically = 2.0V

Display Count

$$COUNT = 1000 \times \frac{V_{IN}}{V_{REF}}$$

Conversion cycle
$t_{CYC} = t_{CLOCK} \times 4000$
$t_{CYC} = t_{OSC} \times 16{,}000$
when f_{OSC} = 48KHz; t_{CYC} = 333mS

Common Mode Input Voltage
$(V^- + 1.0V) < V_{IN} < (V^+ - 0.5V)$

Auto Zero Capacitor
$0.01\mu F < C_{AZ} < 1.0\ \mu F$

Reference Capacitor
$0.1\mu F < C_{REF} < 1.0\ \mu F$

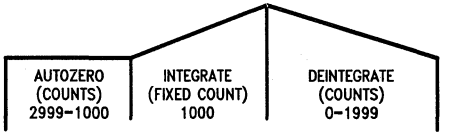
V_{COM}
Biased between V^+ and V^-.
$V_{COM} \cong V^+ - 2.8V$
Regulation lost when V^+ to $V^- < \cong 6.4V$.
If V_{COM} is externally pulled down to $(V^+$ to $V^-)/2$, the V_{COM} circuit will turn off.

ICL7106 Power Supply: Single 9V
$V^+ - V^- = 9V$
Digital supply is generated internally
$V_{GND} \cong V^+ - 4.5V$

ICL7106 Display: LCD
Type: Direct drive with digital logic supply amplitude.

ICL7107 Power Supply: Dual ±5.0V
$V^+ = +5.0V$ to GND
$V^- = -5.0V$ to GND
Digital Logic and LED driver supply
V^+ to GND

ICL7107 Display: LED
Type: Non-Multiplexed Common Anode



Total Conversion Time = 4000 * t_{CLOCK} = 16,000 * t_{OSC}

0335–26

Figure 24

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICL7116/7117
3½-Digit LCD/LED Single-Chip A/D Converter with Display Hold

GENERAL DESCRIPTION

The Harris ICL7116 and 7117 are high performance, low power 3-½ digit A/D converters. All the necessary active devices are contained on a single CMOS I.C., including seven segment decoders, display drivers, reference, and a clock. The 7116 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7117 will directly drive an instrument-size common anode light emitting diode (LED) display.

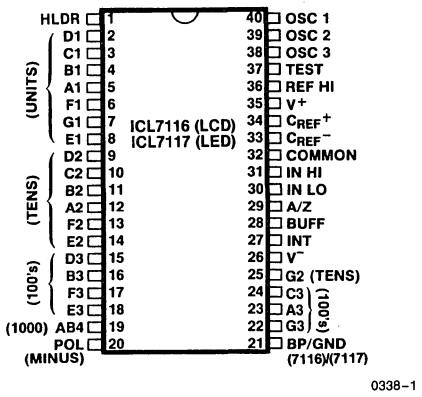
The 7116 and 7117 have almost all of the features of the 7106 and 7107 with the addition of a HoLD Reading input. With this input, it is possible to make a measurement and then retain the value on the display indefinitely. To make room for this feature the reference input has been referenced to Common rather than being fully differential. These circuits retain the accuracy, versatility, and true economy of the 7106 and 7107. They feature auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA maximum, and roll over error of less than one count. The versatility of true differential input is of particular advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally, the true economy of single power supply operation (7116) enables a high performance panel meter to be built with the addition of only eleven passive components and a display.

FEATURES

- **HoLD Reading Input Allows Indefinite Display Hold**
- **Guaranteed Zero Reading for 0 Volts Input**
- **True Polarity at Zero for Precise Null Detection**
- **1pA Input Current Typical**
- **True Differential Input**
- **Direct Display Drive — No External Components Required — LCD ICL7116**
  — LED ICL7117
- **Low Noise — Less Than 15μV pk-pk Typical**
- **On-Chip Clock and Reference**
- **Low Power Dissipation — Typically Less Than 10mW**
- **No Additional Active Circuits Required**
- **New Small Outline Surface Mount Package Available**

ORDERING INFORMATION

Part Number	Temperature Range	Package	Display Type
ICL7116CPL	0°C to +70°C	40 Pin Plastic DIP	LCD
ICL7116CM44	0°C to +70°C	44 Pin Surface Mount	LCD
ICL7117CPL	0°C to +70°C	40 Pin Plastic DIP	LED



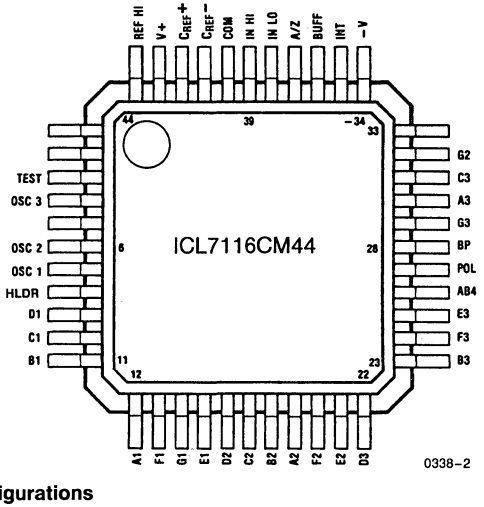


Figure 1: Pin Configurations

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

ICL7116

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
HLDR, Clock Input ..... Test to V^+
Power Dissipation (Note 2)
  Ceramic Package 1000mW
  Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

ICL7117

Supply Voltage V^+ ..... +6V
  V^- ..... −9V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
HLDR, Clock Input ..... Gnd to V^+
Power Dissipation (Note 2)
  Ceramic Package 1000mW
  Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS (Note 3)

Parameter	Test Conditions	Min	Typ	Max	Unit
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$\lvert V_{IN} \rvert \cong$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200mV or Full Scale = 2.000V (Note 7)	−1	±0.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V, Full Scale = 200.0mV		50		μV/V
Noise (Pk — Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V (Note 7)		1	10	pA
Zero Reading Drift	V_{IN} = 0 0°C < T_A < 70°C (Note 7)		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0°C < T_A < 70°C (Ext. Ref. 0ppm/°C) (Note 7)		1	5	ppm/°C
V^+ Supply Current (Does not include LED current for 7117)	V_{IN} = 0		0.8	1.8	mA
V^- Supply Current (7117 only)			0.6	1.8	mA
Analog Common Voltage (With respect to pos. supply)	25kΩ between COMMON & pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to pos. Supply)	25kΩ between COMMON & pos. Supply		80		ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70		kΩ
V_{IL}, Pin 1 (7116 only)				TEST + 1.5	V

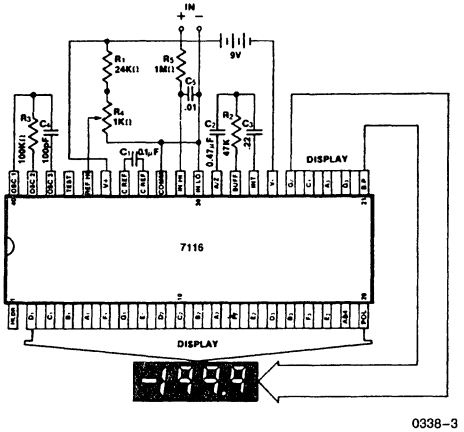
NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Note 3) (Continued)

Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}, Pin 1 (7117 only)				GND+1.5	V
V_{IH}, Pin 1 (Both)		V+−1.5			V
7116 ONLY Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage (Note 5)	V+−V−=9V	4 4	5 5	6 6	V
7117 ONLY Segment Sinking Current (Except Pin 19 and 20) (Pin 19 only) (Pin 20 only)	V+=5.0V Segment Voltage=3V	 5 10 4	 8.0 16 7		 mA

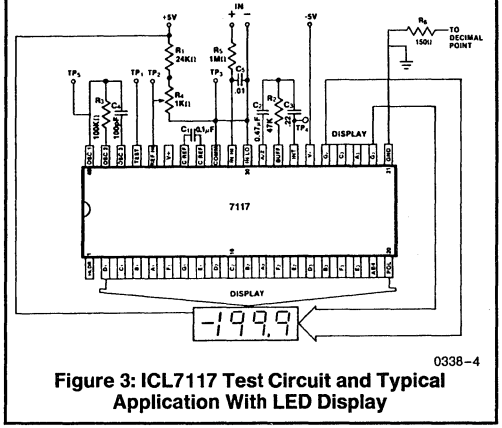
NOTES: 3. Unless otherwise noted, specifications apply to both the 7116 and 7117 at T_A=25°C, f_{clock}=48kHz. 7116 is tested in the circuit of Figure 2. 7117 is tested in the circuit of Figure 3.
4. Refer to "Differential Input" discussion.
5. Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
6. The 7116 logic input has an internal pull-down resistor connected from HLDR, pin 1, to TEST, pin 37. The 7117 logic input has an internal pull-down resistor connected from HLDR, pin 1 to GROUND, pin 21.
7. Not tested, guaranteed by design.

TEST CIRCUITS



0338-3

Figure 2: ICL7116 Test Circuit and Typical Application With Liquid Crystal Display



0338-4

Figure 3: ICL7117 Test Circuit and Typical Application With LED Display

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

Analog Section

Figure 4 shows the Analog Section for the ICL7116 and 7117. Each measurement cycle is divided into three phases. They are (1) auto-zero (A/Z), (2) signal integrate (INT) and (3) de-integrate (DE).

Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is $1000\left(\frac{Vin}{Vref}\right)$.

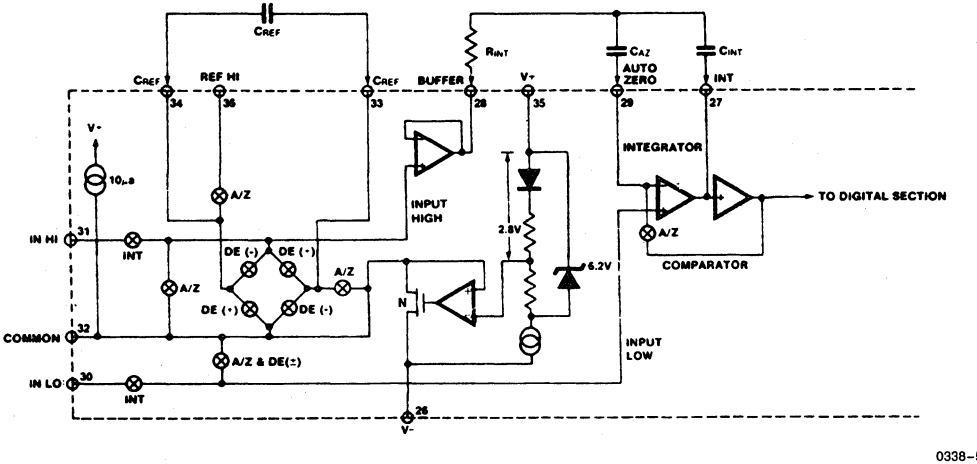


Figure 4: Analog Section of 7116/7117

NOTE: All typical values have been characterized but are not tested.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of typically 86dB. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3 volts of either supply without loss of linearity. See Application Note A032 for a discussion of the effects of stray capacitance.

Reference

The reference input must be generated as a positive voltage with respect to COMMON. Note that current flowing in the COMMON pins' internal resistance causes a slight shift in the effective reference voltage, disturbing ratiometric readings at low reference inputs. If possible, do not let this current vary.

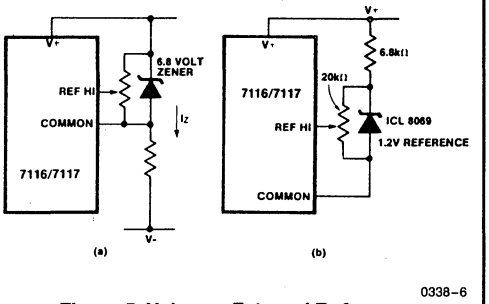
Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (7116) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 volts less than the positive supply. This is selected to provide proper operation with a minimum end-of-life battery voltage of about 6V. However, analog COMMON does have some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (.001%/V), low output impedance ($\cong 15\Omega$), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. With the 7117, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25μV to 80μVpk-pk. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a nonoverload count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7116, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Figure 5.

Analog COMMON is also the voltage that input low returns to during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter.



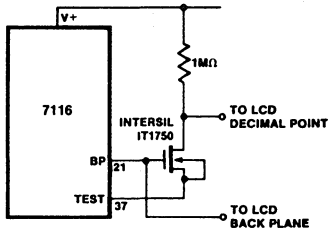
0338-6

Figure 5: Using an External Reference

Within the IC, analog COMMON is tied to an N channel FET that can sink 30mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

TEST

The TEST pin serves two functions. On the 7116 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 6 and 7 show such an application. No more than a 1mA load should be applied.



0338-7

Figure 6: Simple Inverter for Fixed Decimal Point

NOTE: All typical values have been characterized but are not tested.

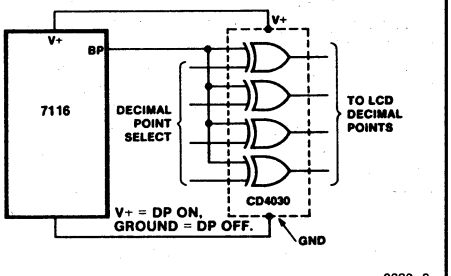


Figure 7: Exclusive 'OR' Gate for Decimal Point Drive

The second function is a "lamp test". When TEST is pulled to high (to V^+) all segments will be turned on and the display should read − 1888. **[Caution: on the 7116, in the lamp test mode, the segments have a constant DC voltage (no square-wave) and will burn the LCD display if left in this mode for several minutes.]**

DIGITAL SECTION

Figures 8 and 9 show the digital section for the 7116 and 7117, respectively. In the 7116, an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

Figure 9 is the Digital Section of the 7117. It is identical to that of the 7116 except the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

In both devices the polarity indicator is ON for negative analog inputs. This can be reversed by simply reversing IN LO and IN HI.

HOLD Reading Input

The HLDR input will prevent the latch from being updated when this input is at a logic "1". The chip will continue to make A/D conversions, however, the results will not be updated to the internal latches until this input goes low. This input can be left open or connected to TEST (7116) or GROUND (7117) to continuously update the display. This input is CMOS compatible, and has a 70kΩ typical resistance to either TEST (7116) or GROUND (7117).

NOTE: All typical values have been characterized but are not tested.

DISPLAY FONT

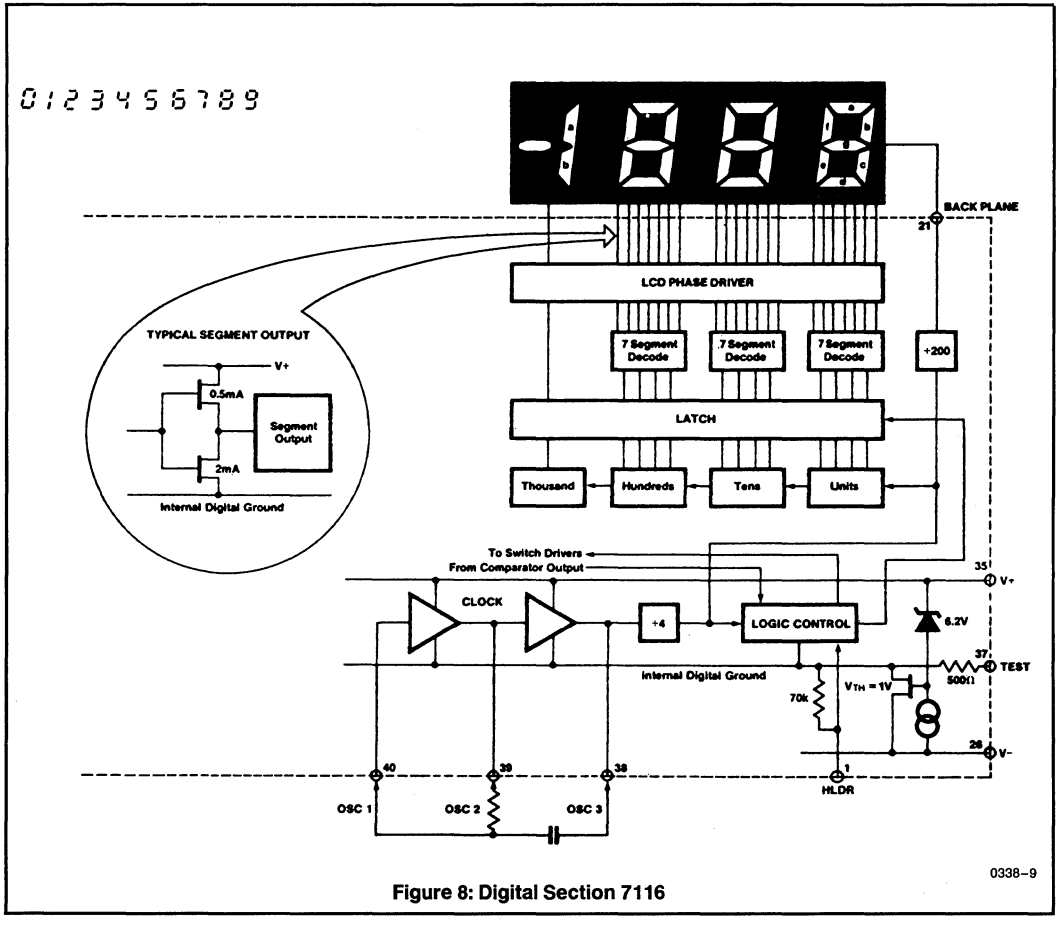


Figure 8: Digital Section 7116

NOTE: All typical values have been characterized but are not tested.

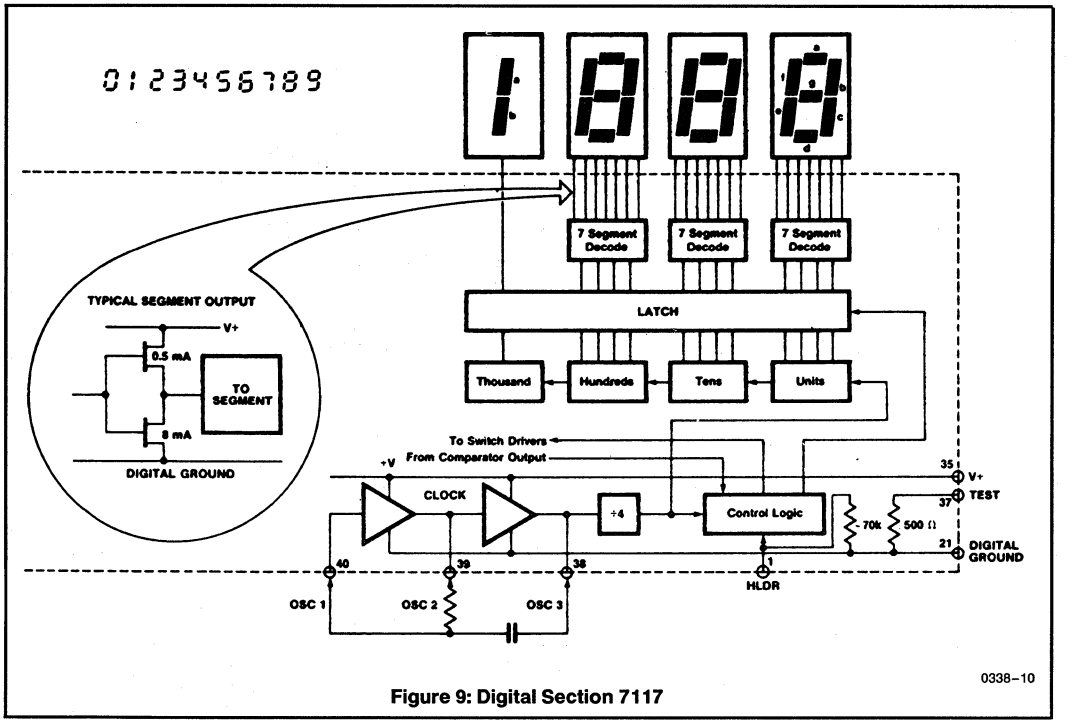


Figure 9: Digital Section 7117

System Timing

Figure 10 shows the clocking arrangement used in the 7116 and 7117. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33⅓kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 66⅔kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

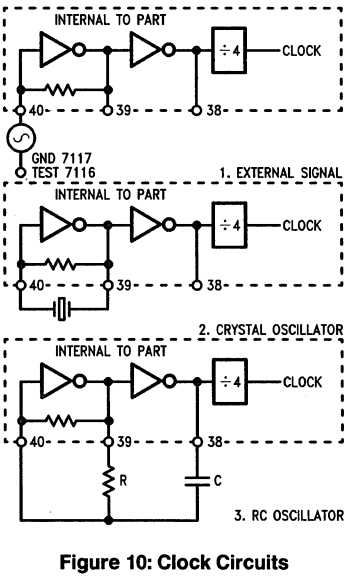


Figure 10: Clock Circuits

NOTE: All typical values have been characterized but are not tested.

COMPONENT VALUE SELECTION

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volts full scale, 470kΩ is near optimum and similarly a 47kΩ resistor is optimum for a 200.0mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the 7116 or the 7117, when the analog COMMON is used as a reference, a nominal ±2 volt full scale integrator swing is fine. For the 7117 with ±5 volt supplies and analog common tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48kHz clock), nominal values for C_{INT} are 0.22μF and 0.10μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.47μF capacitor is recommended. On the 2 volt scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. If rollover errors occur a larger value, up to 1.0μF may be required.

Oscillator Components

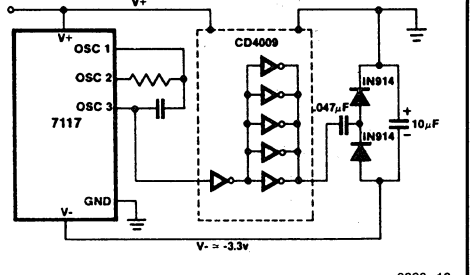
For all ranges of frequency a 100kΩ resistor is recommended and the capacitor is selected from the equation $f \cong \frac{0.45}{RC}$. For 48kHz clock (3 readings/second), C=100pF.

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN}=2V_{REF}$. Thus, for the 200.0mV and 2.000 volt scale, V_{REF} should equal 100.0mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select $V_{REF}=0.341V$. Suitable values for integrating resistor and capacitor would be 120kΩ and 0.22μF. This makes the system slightly quieter and also avoids a divider network on the input. The 7117 with ±5 volts supplies can accept input signals up to ±4 volts. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN}\neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

7117 Power Supplies

The 7117 is designed to work from ±5 volt supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 11 shows this application. See ICL7660 data sheet for an alternative.



0338-12

Figure 11: Generating Negative Supply from +5v

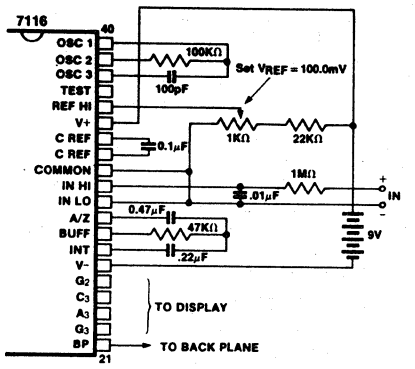
In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts in magnitude.
3. An external reference is used.

TYPICAL APPLICATIONS

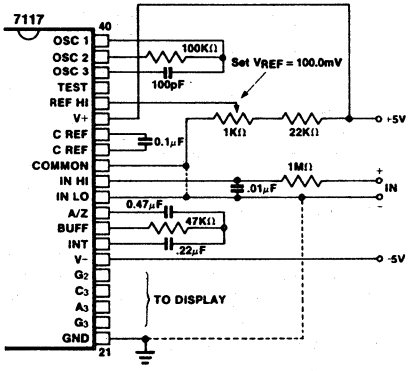
The 7116 and 7117 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

NOTE: All typical values have been characterized but are not tested.



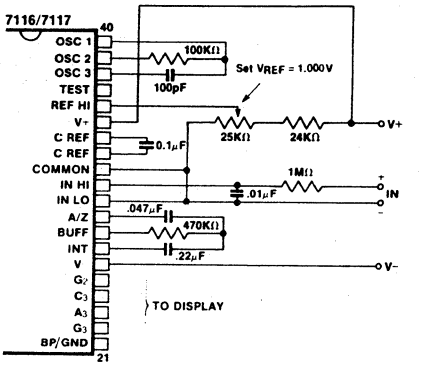
0338-13

Figure 12: 7116 using the internal reference. Values shown are for 200.0mV full scale, 3 readings per second, floating supply voltage (9V battery).



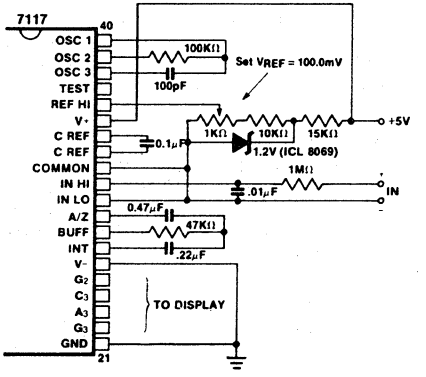
0338-14

Figure 13: 7117 using the internal reference. Values shown are for 200.0mV full scale, 3 readings per second. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog Common.)



0338-15

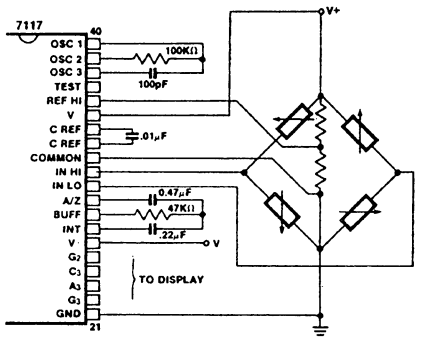
Figure 14: 7116/7117: Recommended component values for 2.000V full scale.



0338-16

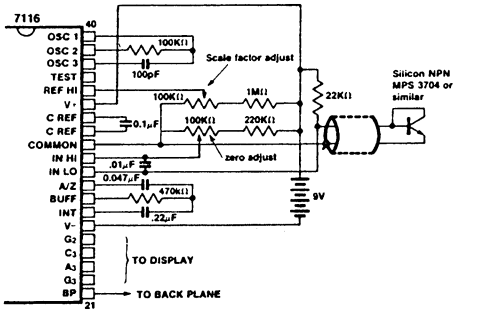
Figure 15: 7117 operated from single +5V supply. An external reference must be used in this application, since the voltage between V+ and V− is insufficient for correct operation of the internal reference.

NOTE: All typical values have been characterized but are not tested.



0338-17

Figure 16: 7117 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.



0338-18

Figure 17: 7116 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar.

A017 "The Integrating A/D Converter," by Lee Evans.

A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.

A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.

A032 "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.

A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.

A047 "Games People Play with Harris' A/D Converters," edited by Peter Bradshaw.

A052 "Tips for Using Single-Chip 3½-Digit A/D Converters," by Dan Watson.

NOTE: All typical values have been characterized but are not tested.

ICL7116/17
INTEGRATING A/D CONVERTER
EQUATIONS

Oscillator Frequency

$f_{OSC} = 0.45/RC$

$C_{OSC} \geq 50$ pF; $R_{OSC} > 50$ kΩ

f_{OSC} typ. = 48 kHz

Oscillator Period

$t_{OSC} = RC/0.45$

Integration Clock Frequency

$f_{CLOCK} = f_{OSC}/4$

Integration Period

$t_{INT} = 1000 \times (4/f_{OSC})$

60/50 Hz Rejection Criterion

$t_{INT}/t_{60\ Hz}$ or $t_{INT}/t_{50\ Hz}$ = Integer

Optimum Integration Current

$I_{INT} = 4.0\ \mu A$

Full Scale Analog Input Voltage

V_{INFS} typically = 200 mV or 2.0V

Integrate Resistor

$$R_{INT} = \frac{(V_{INFS})}{I_{INT}}$$

Integrate Capacitor

$$C_{INT} = \frac{(t_{INT})(I_{INT})}{V_{INT}}$$

Integrator Output Voltage Swing

$$V_{INT} = \frac{(t_{INT})(I_{INT})}{C_{INT}}$$

V_{INT} Maximum Swing:

$(V^- + 0.5V) < V_{INT} < (V^+ - 0.5V)$

V_{INT} typically = 2.0V

Display Count

$$COUNT = 1000 \times \frac{V_{IN}}{V_{REF}}$$

Conversion Cycle

$t_{CYC} = t_{CLOCK} \times 4{,}000$

$t_{CYC} = t_{OSC} \times 16{,}000$

when f_{OSC} = 48 kHz, t_{CYC} = 333 ms

Common Mode Input Voltage

$(V^- + 1.0V) < V_{IN} < (V^+ - 0.5V)$

Auto Zero Capacitor

$0.01\ \mu F < C_{AZ} < 1.0\ \mu F$

Reference Capacitor

$0.1\ \mu F < C_{REF} < 1.0\ \mu F$

V_{COM}

Biased between V^+ and V^-.

$V_{COM} \cong V^+ - 2.8V$

Regulation lost when V^+ to $V^- < \cong 6.4V$.

If V_{COM} is externally pulled down to (V^+ to V^-)/2, the V_{COM} circuit will turn off.

ICL7116 Power Supply: Single 9V

$V^+ - V^- = 9V$

Digital supply is generated internally

$V_{GND} \cong V^+ - 4.5V$

ICL7116 Display: LCD

Type: Direct drive with digital logic supply amplitude.

ICL7117 Power Supply: Dual ±5.0V

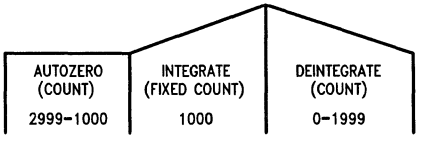
$V^+ = +5.0V$ to GND

$V^- = -5.0V$ to GND

Digital Logic and LED driver supply: V^+ to GND.

ICL7117 Display: LED

Type: Non-Multiplexed Common Anode



0338-19

Total Conversion Time = 4000 * t_{CLOCK} = 16,000 * t_{OSC}

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICL7126
3½-Digit Low-Power Single-Chip A/D Converter

GENERAL DESCRIPTION

The Harris ICL7126 is a high performance, very low power 3½-digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven segment decoders, display drivers, reference, and clock. The 7126 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive. The supply current is 100μA, ideally suited for 9V battery operation.

The 7126 brings together an unprecedented combination of high accuracy, versatility, and true economy. It features auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation allows a high performance panel meter to be built with the addition of only 10 passive components and a display.

The ICL7126 can be used as a plug-in replacement for the ICL7106 in a wide variety of applications, changing only the passive components.

FEATURES

- **8,000 Hours Typical 9 Volt Battery Life**
- **Guaranteed Zero Reading for 0 Volts Input On All Scales**
- **True Polarity at Zero for Precise Null Detection**
- **1pA Typical Input Current**
- **True Differential Input and Reference**
- **Direct LCD Display Drive — No External Components Required**
- **Pin Compatible With The ICL7106**
- **Low Noise — Less Than 15μVp-p**
- **On-Chip Clock and Reference**
- **Low Power Dissipation Guaranteed Less Than 1mW**
- **No Additional Active Circuits Required**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7126CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7126RCPL	0°C to +70°C	40-Pin Plastic DIP*
ICL7126CDL	0°C to +70°C	40-Pin Ceramic DIP
ICL7126CJL	0°C to +70°C	40-Pin CERDIP

* "R" indicates device with reversed leads.

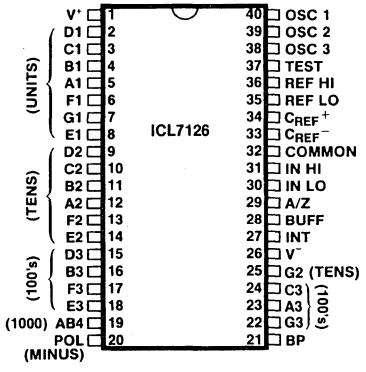


Figure 1: Pin Configuration

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (Either Input) (Note 1) .... V^+ to V^-
Reference Input Voltage (Either Input) ..... V^+ to V^-
Clock Input ..... TEST to V^+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

NOTE 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS (Note 3)

Characteristics	Test Conditions	Min	Typ	Max	Unit
Zero Input Reading	V_{IN} = 0.0V Full Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$ V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	$\lvert -V_{IN} \rvert = +V_{IN} \cong$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	−1	±0.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		50		μV/V
Noise (Pk - Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0 0°C < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0°C < T_A < 70°C (Ext. Ref. 0 ppm/°C)		1	5	ppm/°C
Supply Current (Does not include COMMON current)	V_{IN} = 0 (Note 6)		70	100	μA
Analog COMMON Voltage (With respect to pos. supply)	250kΩ between Common & pos. Supply	2.4	2.8	3.2	V

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Note 3) (Continued)

CHARACTERISTICS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Temp. Coeff. of Analog COMMON (with respect to pos. Supply)	250kΩ between Common & pos. Supply		150		ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to V^- = 9V	4	5	6	V
Power Dissipation Capacitance	vs. Clock Freq.		40		pF

NOTES: 3. Unless otherwise noted, specifications apply at T_A = 25°C, f_{clock} = 16kHz and are tested in the circuit of Figure 4.
4. Refer to "Differential Input" discussion.
5. Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
6. During auto zero phase, current is 10-20μA higher. 48kHz oscillator, Figure 5, increases current by 8μA (typ).
7. Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

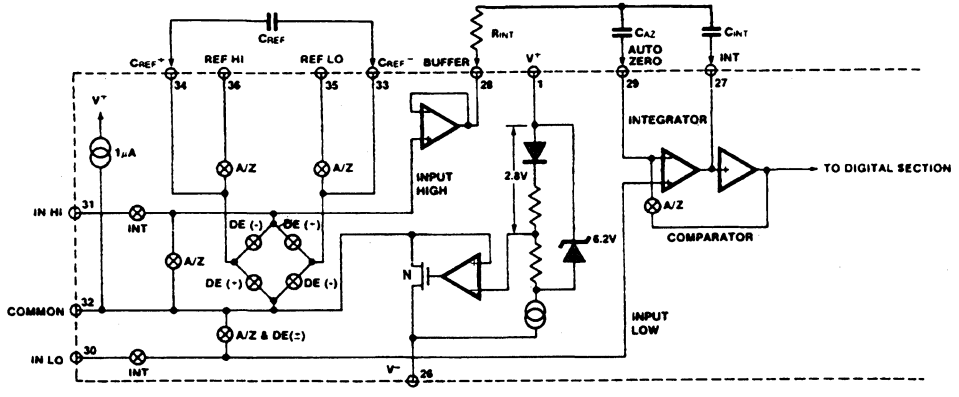
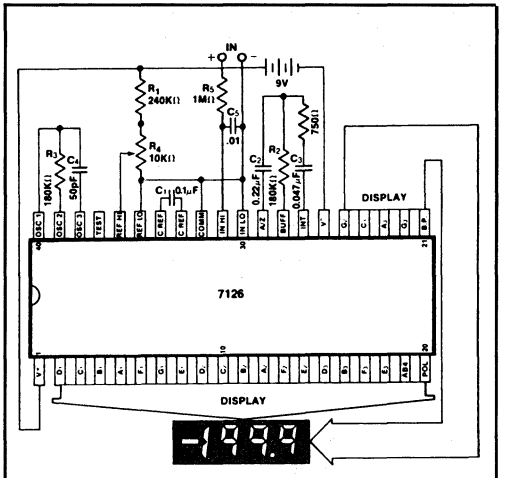


Figure 2: Analog Section of 7126

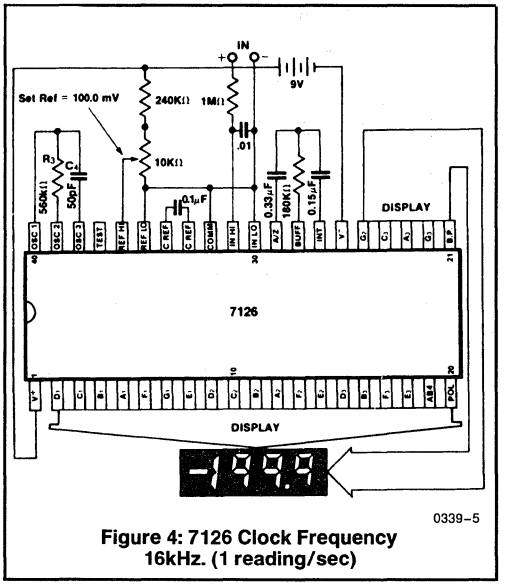
NOTE: All typical values have been characterized but are not tested.

TEST CIRCUITS



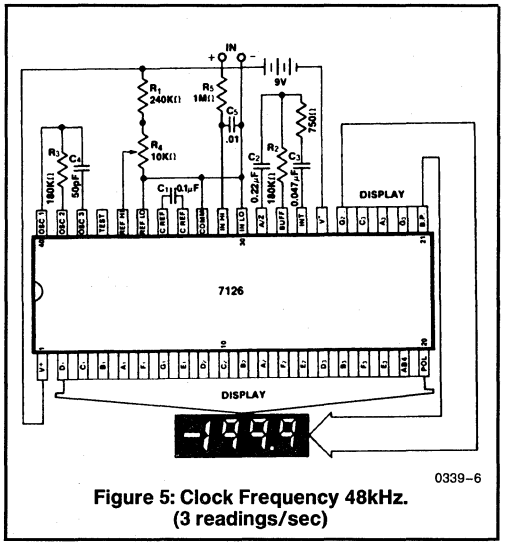
0339-4

Figure 3: ICL7126 with Liquid Crystal Display



0339-5

Figure 4: 7126 Clock Frequency 16kHz. (1 reading/sec)



0339-6

Figure 5: Clock Frequency 48kHz. (3 readings/sec)

DETAILED DESCRIPTION

Analog Section

Figure 2 shows the Functional Diagram of the Analog Section for the ICL7126. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less then 10μV.

Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one Volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and in-

NOTE: All typical values have been characterized but are not tested.

put high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is $1000\left(\frac{V_{IN}}{V_{REF}}\right)$.

Differential Input

The input can accept differential voltages anywhere within the common mode rante of the input amplifier; or specifically from 0.5 Volts below the positive supply to 1.0 Volt above the negative supply. In this range the system has a CMRR of 86 db typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 Volts of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition. (See Component Value Selection.)

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8 Volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (<7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance (≅15Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2 to 8°C, typical for instruments, can give a scale factor error of a count or more. Also the common voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (<7V). These problems are eliminated if an external reference is used, as shown in Figure 6.

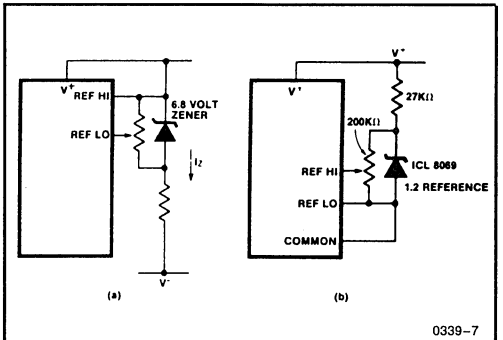


Figure 6: Using an External Reference

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink 3mA or more of current to hold the voltage 2.8 Volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 1μA of source current, so COMMON may easily be tied to a more negative voltage thus over-riding the internal reference.

TEST

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 7 and 8 show such an application. No more than a 1mA load should be applied.

The second function is a "lamp test." When TEST is pulled high (to V+) all segments will be turned on and the display should read — 1888. The TEST pin will sink about 10mA under these conditions.

Caution: In the lamp test mode, the segments have a constant D-C voltage (no square-wave) and may burn the LCD display if left in this mode for extended periods.

NOTE: All typical values have been characterized but are not tested.

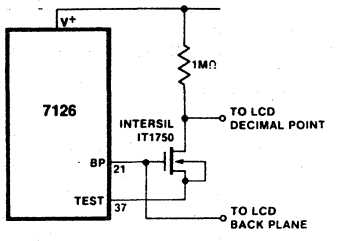


Figure 7: Simple Inverter for Fixed Decimal Point

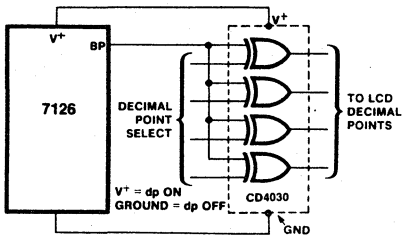


Figure 8: Exclusive 'OR' Gate for Decimal Point Drive

DISPLAY FONT

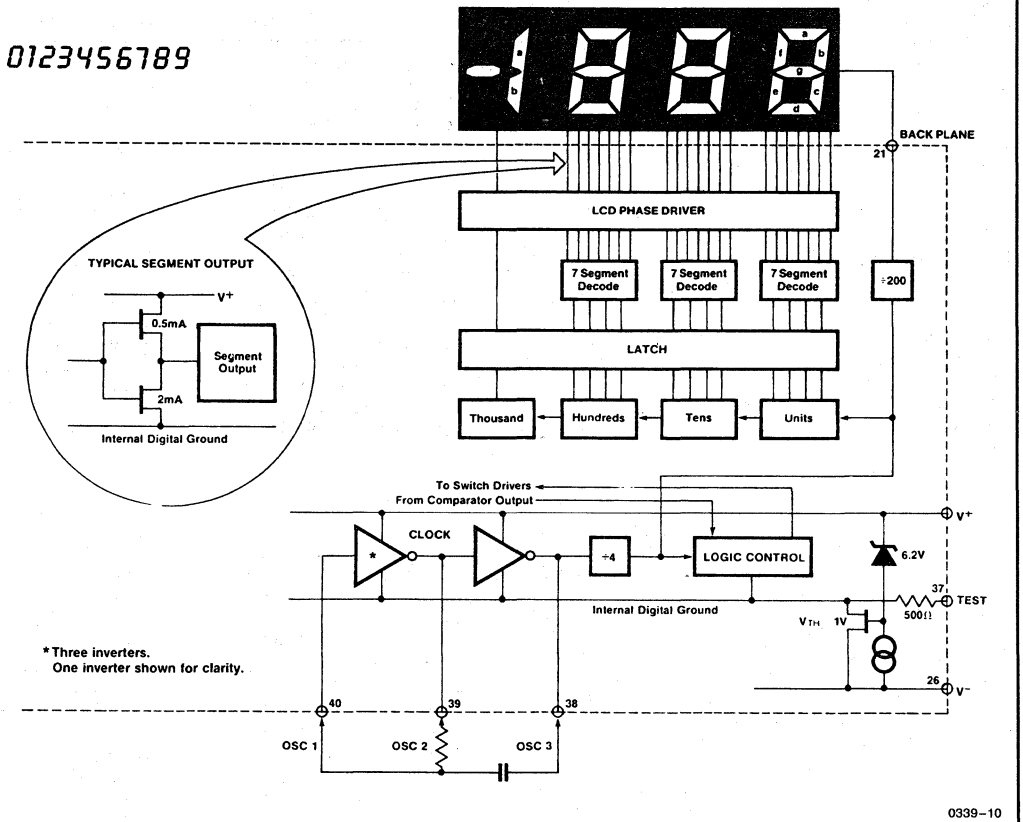


Figure 9: Digital Section

NOTE: All typical values have been characterized but are not tested.

DIGITAL SECTION

Figure 9 shows the digital section for the 7126. An internal digital ground is generated from a 6 Volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 Volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

System Timing

Figure 10 shows the clocking arrangement used in the 7126. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

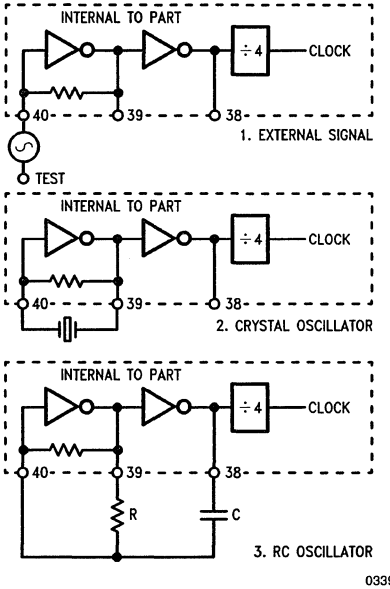


Figure 10: Clock Circuits

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33-⅓kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66-⅔kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

COMPONENT VALUE SELECTION

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6μA of quiescent current. They can supply ~1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 Volt full scale, 1.8mΩ is near optimum and similarly 180kΩ for a 200.0mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 Volt from either supply). When the analog COMMON is used as a reference, a nominal ±2 Volt full scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.047μF, for 1/sec (16kHz) 0.15μF. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

At three readings/sec., a 750Ω resistor should be placed in series with the integrating capacitor, to compensate for comparator delay. See App. Note A017 for a description of the need and effects of this resistor.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full scale where noise is very important, a 0.32μF capacitor is recommended. On the 2 Volt scale, a 0.033μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e., the REF LO pin is not analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0μF will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation $f \sim \frac{0.45}{RC}$. For 48kHz clock (3 readings/second), R = 180kΩ.

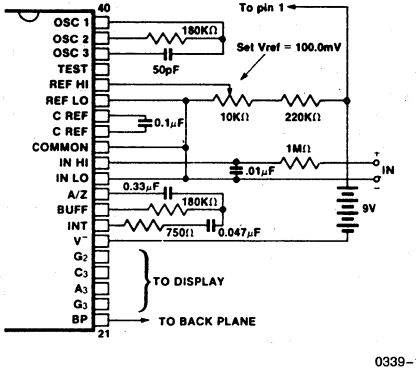
NOTE: All typical values have been characterized but are not tested.

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200.0mV and 2.000 Volt scale, V_{REF} should equal 100.0mV and 1.000 Volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select $V_{REF} = 0.341V$. A suitable value for integrating resistor would be 330kΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighting systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

TYPICAL APPLICATIONS

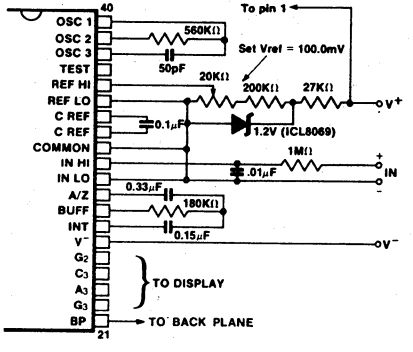
The 7126 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.



0339-12

Figure 11: 7126 using the internal reference.

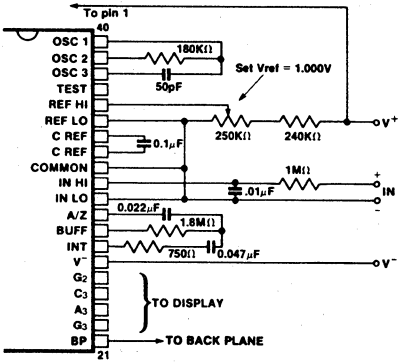
Values shown are for 200.0mV full scale, 3 readings per second, floating supply voltage (9V battery).



0339-13

Figure 12: 7126 with an external band-gap reference (1.2V type).

IN LO is tied to COMMON, thus establishing the correct common mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading per second.

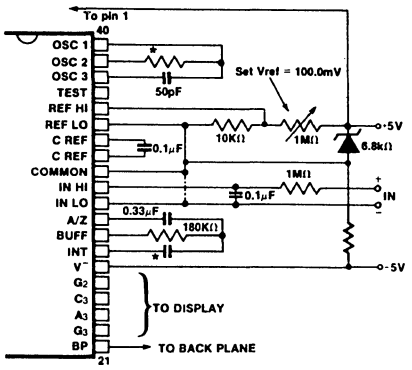


0339-14

Figure 13: Recommended component values for 2.000V full scale, 3 readings per second.

For 1 reading per second, delete 750Ω resistor, change C_{INT}, R_{OSC} to values of Figure 12.

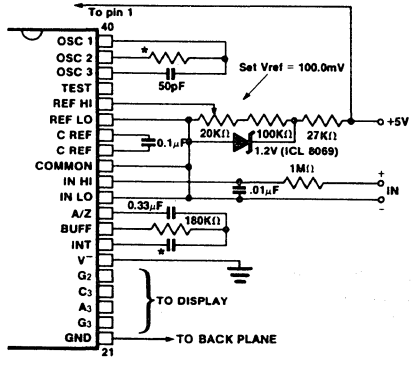
NOTE: All typical values have been characterized but are not tested.



0339-15

Figure 14: 7126 with Zener diode reference.

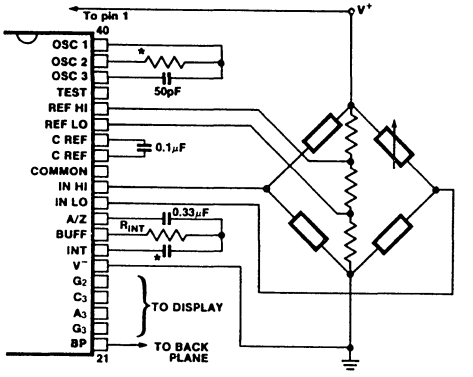
Since low T.C. zeners have breakdown voltages ~6.8V, diode must be placed across the total supply (10V). As in the case of Figure 13, IN LO may be tied to COMMON.



0339-16

Figure 15: 7126 operated from single +5V supply.

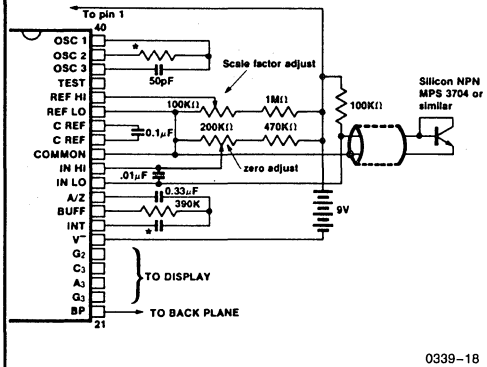
An external reference must be used in this application, since the voltage between V+ and V− is insufficient for correct operation of the internal reference.



0339-17

Figure 16: 7126 measuring ratiometric values of Quad Load Cell.

The resistor values within the bridge are determined by the desired sensitivity.



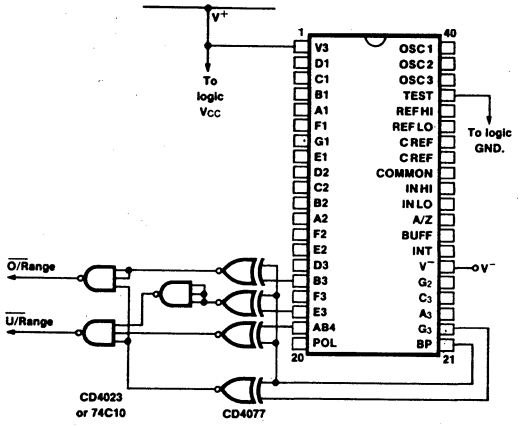
0339-18

Figure 17: 7126 used as a digital centigrade thermometer.

A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

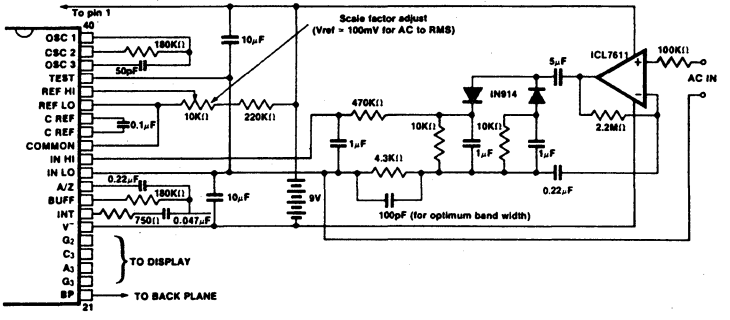
*Values depend on clock frequency. See Figures 11, 12, 13.

NOTE: All typical values have been characterized but are not tested.



0339-19

Figure 18: Circuit for developing Underrange and Overrange signals from 7126 outputs.



0339-20

Figure 19: AC to DC Converter with 7126. Test is used as a common mode reference level to ensure compatibility with most op-amps.

NOTE: All typical values have been characterized but are not tested.

APPLICATION NOTES

A016 "Selecting A/D Converters", by David Fullagar.

A017 "The Integrating A/D Converter", by Lee Evans.

A018 "Do's and Don'ts of Applying A/D Converters", by Peter Bradshaw and Skip Osgood.

A023 "Low Cost Digital Panel Meter Designs", by David Fullagar and Michael Dufort.

A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7/9 Family", by Peter Bradshaw.

A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106", by Larry Goff.

A052 "Tips for Using Single-Chip 3½-Digit A/D Converters", by Dan Watson.

7126 EVALUATION KIT

After purchasing a sample of the 7126, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application.

To facilitate evaluation of this unique circuit, Harris is offering a kit which contains all the necessary components to build a 3½-digit panel meter. With the ICL7126EV/KIT and the small number of additional components required, an engineer or technician can have the system "up and running" in about half an hour. The kit contains a circuit board, a display (LCD), passive components, and miscellaneous hardware.

NOTE: All typical values have been characterized but are not tested.

ICL7126
INTEGRATING A/D CONVERTER EQUATIONS

Oscillator Frequency

$f_{OSC} = 0.45/RC$

$C_{OSC} > 50$ pF; $R_{OSC} > 50$ kΩ

f_{OSC} typ. = 48 kHz

Oscillator Period

$t_{OSC} = RC/0.45$

Integration Clock Frequency

$f_{CLOCK} = f_{OSC}/4$

Integration Period

$t_{INT} = 1000 \times (4/f_{OSC})$

60/50 Hz Rejection Criterion

t_{INT}/t_{60} Hz or t_{INT}/t_{50} Hz = Integer

Optimum Integration Current

$I_{INT} = 1.0\ \mu A$

Full Scale Analog Input Voltage

V_{INFS} Typically = 200 mV or 2.0V

Integrate Resistor

$$R_{INT} = \frac{V_{INFS}}{I_{INT}}$$

Integrate Capacitor

$$C_{INT} = \frac{(t_{INT})(I_{INT})}{V_{INT}}$$

Integrator Output Voltage Swing

$$V_{INT} = \frac{(t_{INT})(I_{INT})}{C_{INT}}$$

V_{INT} Maximum Swing:

$(V^- + 0.5V) < V_{INT} < (V^+ - 0.5V)$

V_{INT} typically = 2.0V

Display Count

$$COUNT = 1000 \times \frac{V_{IN}}{V_{REF}}$$

Conversion Cycle

$t_{CYC} = t_{CLOCK} \times 4000$

$t_{CYC} = t_{OSC} \times 16{,}000$

when f_{OSC} = 48 kHz; t_{CYC} = 333 ms

Common Mode Input Voltage

$(V^- + 1.0V) < V_{IN} < (V^+ - 0.5V)$

Auto Zero Capacitor

$0.01\ \mu F < C_{AZ} < 1.0\ \mu F$

Reference Capacitor

$0.1\ \mu F < C_{REF} < 1.0\ \mu F$

V_{COM}

Biased between V^+ and V^-.

$V_{COM} \cong V^+ - 2.8V$

Regulation lost when V^+ to $V^- < \cong 6.4V$.

If V_{COM} is externally pulled down to $(V^+$ to $V^-)/2$, the V_{COM} circuit will turn off.

Power Supply: Single 9V

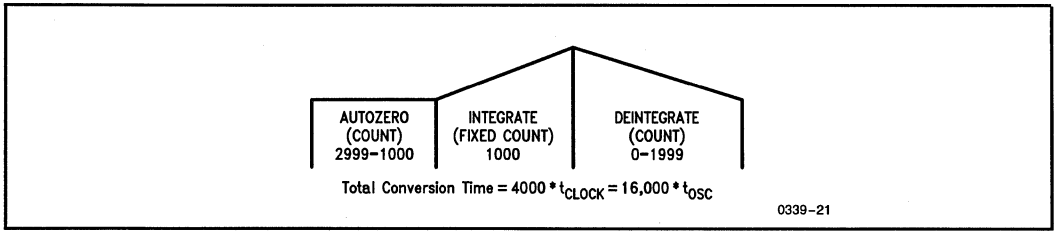
$V^+ - V^- = 9V$

Digital supply is generated internally

$V_{GND} \cong V^+ - 4.5V$

Display: LCD

Type: Direct drive with digital logic supply amplitude.



NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICL7129
4½ Digit LCD Single-Chip A/D Converter

GENERAL DESCRIPTION

The Harris ICL7129 is a very high-performance 4½-digit analog-to-digital converter that directly drives a multiplexed liquid crystal display. This single-chip CMOS integrated circuit requires only a few passive components and a reference to operate. It is ideal for high-resolution hand-held digital multimeter applications.

The performance of the ICL7129 has not been equaled before in a single-chip A/D converter. The successive integration technique used in the ICL7129 results in accuracy better than 0.005% of full-scale and resolution down to 10μV/count.

The ICL7129, drawing only 1mA from a 9V battery, is well suited for battery powered instruments. Provision has been made for the detection and indication of a "LOW/BATTERY" condition. Autoranging instruments can be made with the ICL7129 which provides overrange and underrange outputs and 10:1 range changing input. The ICL7129 instantly checks for continuity, giving both a visual indication and a logic level output which can enable an external audible transducer. These features and the high performance of the ICL7129 make it an extremely versatile and accurate instrument-on-a-chip.

FEATURES

- **±19,999 Count A/D Converter Accurate to ±4 Count**
- **10μV Resolution On 200mV Scale**
- **110dB CMRR**
- **Direct LCD Display Drive**
- **True Differential Input and Reference**
- **Low Power Consumption**
- **Decimal Point Drive Outputs**
- **Overrange and Underrange Outputs**
- **Low Battery Detection and Indication**
- **10:1 Range Change Input**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7129CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7129RCPL	0°C to +70°C	40-Pin Plastic DIP*
ICL7129CM44	0°C to +70°C	44-Pin Surface Mount

* "R" indicates device with reversed leads.

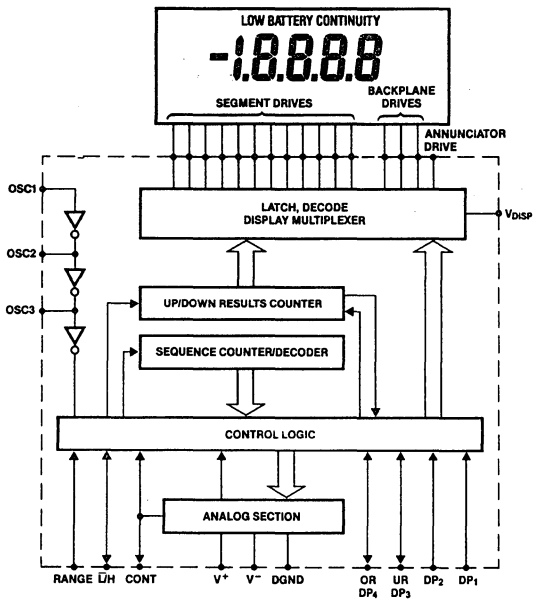


Figure 1: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages (V^+ to V^-) 15V
Reference Voltage (REF HI or REF LO) ..... V^+ to V^-
Input Voltage (Note 1)
(IN HI or IN LO) ..... V^+ to V^-
V_{DISP} ..... DGND −0.3V to V^+
Digital Input Pins
1, 2, 19, 20, 21, 22, 27,
37, 38, 39, 40 ..... DGND to V^+

Power Dissipation (Note 2)
Plastic package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages provided that input current is limited to ±400μA. Currents above this value may result in invalid display readings but will not destroy the device if limited to ±1mA.

Note 2: Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

V^- to V^+ = 9V, V_{REF} = 1.00V. T_A = +25°C, f_{CLK} = 120kHz, unless otherwise noted.

Characteristics	Test Conditions	Min	Typ	Max	Unit
Zero Input Reading	V_{IN} = 0V 200mV Scale	−0000	0000	+0000	Counts
Zero Reading Drift	V_{IN} = 0V 0°C < T_A < +70°C		±0.5		μV/°C
Ratiometric Reading	V_{IN} = V_{REF} = 1000mV RANGE = 2V	9996	9999	10000	Counts
Range Change Accuracy	V_{IN} = 0.10000V on Low Range ≈ V_{IN} = 1.0000V on High Range	0.9999	1.0000	1.0001	Ratio
Rollover Error	$-V_{IN}$ = $+V_{IN}$ = 199mV		1.5	3.0	Counts
Linearity Error	200mV Scale		1.0		
Input Common-Mode Rejection Ratio	V_{CM} = 1.0V, V_{IN} = 0V 200mV Scale		110		dB
Input Common-Mode Voltage Range	V_{IN} = 0V 200mV Scale		(V^-) +1.5 (V^+) −1.0		V
Noise (p-p Value not Exceeding 95% of Time)	V_{IN} = 0V 200mV Scale		14		μV
Input Leakage Current	V_{IN} = 0V, Pin 32, 33		1	10	pA
Scale Factor Tempco	V_{IN} = 199mV 0°C < T_A < +70°C External V_{REF} = 0ppm/°C		2	7	ppm/°C
COMMON Voltage	V^+ to Pin 28	2.8	3.2	3.5	V
COMMON Sink Current	ΔCommon = +0.1V		0.6		mA
COMMON Source Current	ΔCommon = −0.1V		10		μA
DGND Voltage	V^+ to Pin 36 V^+ to V^- = 9V	4.5	5.3	5.8	V
DGND Sink Current	ΔDGND = +0.5V		1.2		mA
Supply Voltage Range	V^+ to V^- (Note 1)	6	9	12	V

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

V^- to $V^+ = 9V$, $V_{REF} = 1.00V$. $T_A = +25°C$, $f_{CLK} = 120kHz$, unless otherwise noted. (Continued)

Characteristics	Test Conditions	Min	Typ	Max	Unit
Supply Current Excluding COMMON Current	V^+ to $V^- = 9V$		1.0	1.5	mA
Clock Frequency	(Note 1)		120	360	kHz
V_{DISP} Resistance	V_{DISP} to V^+		50		kΩ
Low Battery Flag Activation Voltage	V^+ to V^-	6.3	7.2	7.7	V
CONTINUITY Comparator Threshold Voltages	V_{OUT} Pin 27 = HI V_{OUT} Pin 27 = LO	100	200 200	400	mV
Pull-Down Current	Pins 37, 38, 39		2	10	μA
"Weak Output" Current Sink/Source	Pin 20, 21 Sink/Source		3/3		μA
	Pin 27 Sink/Source		3/9		
Pin 22 Source Current Pin 22 Sink Current			40 3		μA

NOTES: 1. Device functionality is guaranteed at the stated Min/Max limits. However, accuracy can degrade under these conditions.

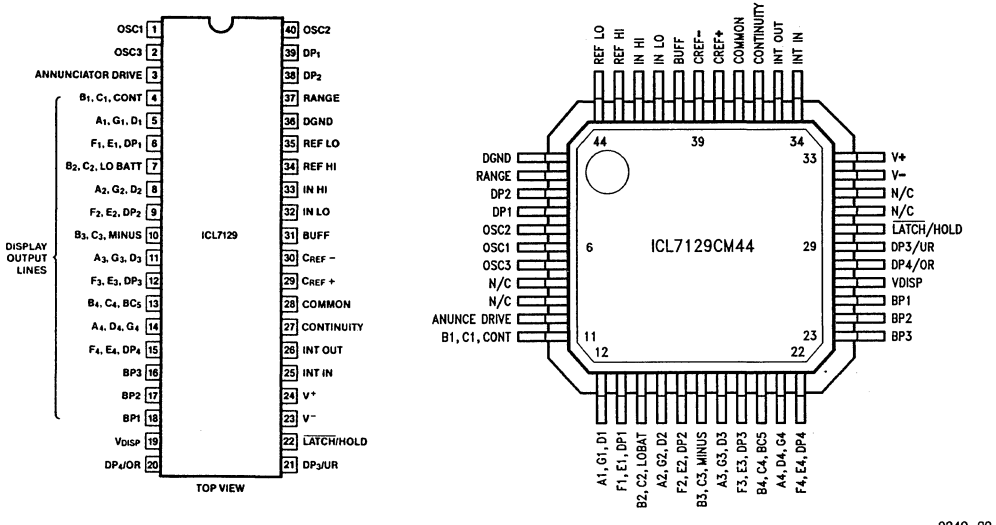


Figure 2: Pin Configurations

NOTE: All typical values have been characterized but are not tested.

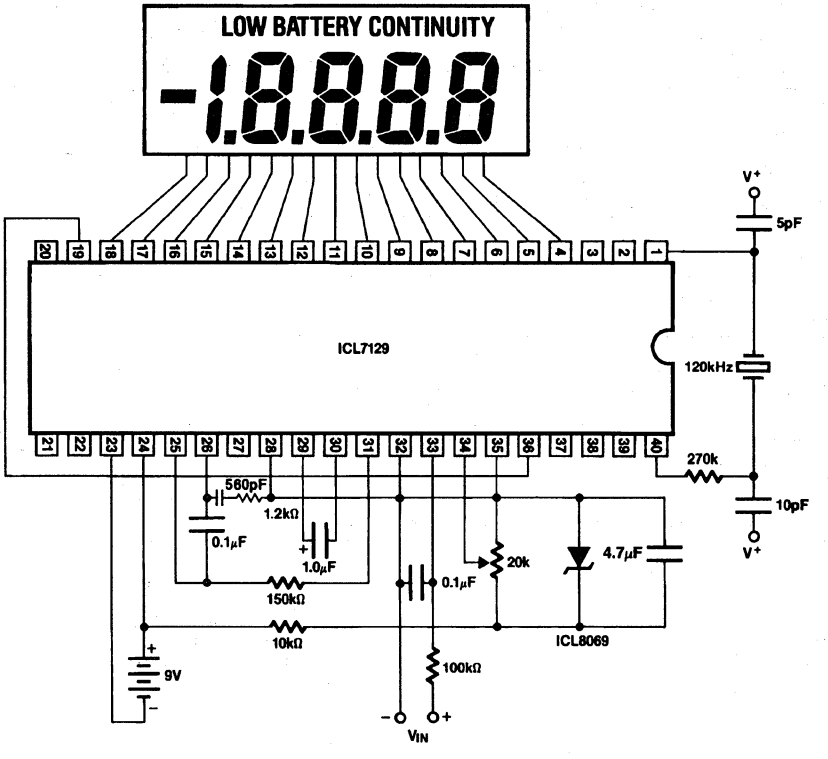


Figure 3: Typical Application

NOTE: All typical values have been characterized but are not tested.

Table 1. Pin Descriptions

Pin	Name	Function
1	OSC1	Input to first clock inverter.
2	OSC3	Output of second clock inverter.
3	ANNUNCIATOR DRIVE	Backplane squarewave output for driving annunciators.
4	B_1, C_1, CONT	Output to display segments.
5	A_1, G_1, D_1	Output to display segments.
6	F_1, E_1, DP_1	Output to display segments.
7	B_2, C_2, LO BATT	Output to display segments.
8	A_2, G_2, D_2	Output to display segments.
9	F_2, E_2, DP_2	Output to display segments.
10	B_3, C_3, MINUS	Output to display segments.
11	A_3, G_3, D_3	Output to display segments.
12	F_3, E_3, DP_3	Output to display segments.
13	B_4, C_4, BC_5	Output to display segments.
14	A_4, D_4, G_4	Output to display segments.
15	F_4, E_4, DP_4	Output to display segments.
16	BP3	Backplane #3 output to display.
17	BP2	Backplane #2 output to display.
18	BP1	Backplane #1 output to display.
19	V_{DISP}	Negative rail for display drivers.
20	DP_4/OR	INPUT: When HI, turns on most significant decimal point. OUTPUT: Pulled HI when result count exceeds ±19,999.
21	DP_3/UR	INPUT: Second most significant decimal point on when HI. OUTPUT: Pulled HI when result count is less than ±1,000.
22	$\overline{\text{LATCH}}$/HOLD	INPUT: When floating, A/D converter operates in the free-run mode. When pulled HI, the last displayed reading is held. When pulled LO, the result counter contents are shown incrementing during the de-integrate phase of cycle. OUTPUT: Negative going edge occurs when the data latches are updated. Can be used for converter status signal.
23	V^-	Negative power supply terminal.
24	V^+	Positive power supply terminal, and positive rail for display drivers.
25	INT IN	Input to integrator amplifier.
26	INT OUT	Output of integrator amplifier.
27	CONTINUITY	INPUT: When LO, continuity flag on the display is off. When HI, continuity flag is on. OUTPUT: HI when voltage between inputs is less than +200mV. LO when voltage between inputs is more than +200mV.
28	COMMON	Sets common-mode voltage of 3.2V below V^+ for DE, 10X, etc. Can be used as pre-regulator for external reference.
29	C_{REF}^+	Positive side of external reference capacitor.
30	C_{REF}^-	Negative side of external reference capacitor.
31	BUFFER	Output of buffer amplifier.
32	IN LO	Negative input voltage terminal.
33	IN HI	Positive input voltage terminal.
34	REF HI	Positive reference voltage input terminal.
35	REF LO	Negative reference voltage input terminal.
36	DGND	Ground reference for digital section.
37	RANGE	3μA pull-down for 200mV scale. Pulled HIGH externally for 2V scale.
38	DP_2	Internal 3μA pull-down. When HI, decimal point 2 will be on.
39	DP_1	Internal 3μA pull-down. When HI, decimal point 1 will be on.
40	OSC2	Output of first clock inverter. Input of second clock inverter.

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

Harris' ICL7129 is a uniquely designed single-chip A/D converter. It features a new "successive integration" technique to achieve 10μV resolution on a 200mV full-scale range. To achieve this resolution a 10:1 improvement in noise performance over previous monolithic CMOS A/D converters was accomplished. Previous integrating converters used an external capacitor to store an offset correction voltage. This technique worked well but greatly increased the equivalent noise bandwidth of the converter. The ICL7129 removes this source of error (noise) by not using an auto-zero capacitor. Offsets are cancelled using digital techniques instead. Savings in external parts cost are realized as well as improved noise performance and elimination of a source of electromagnetic and electrostatic pick-up.

The overall functional diagram of the ICL7129 is shown in Figure 1. The heart of this A/D converter is the sequence counter/decoder which drives the control logic and keeps track of the many separate phases required for each conversion cycle. The sequence counter is constantly running and is a separate counter from the up/down results counter which is activated only when the integrator is de-integrating. At the end of a conversion the data remaining in the results counter is latched, decoded and multiplexed to the liquid crystal display.

The analog section block diagram shown in Figure 4 includes all of the analog switches used to configure the voltage sources and amplifiers in the different phases of the cycle. The input and reference switching schemes are very similar to those in other less accurate integrating A/D converters. There are 5 basic configurations used in the full conversion cycle. Figure 5 illustrates a typical waveform on the integrator output. INT, INT_1, and INT_2 all refer to the signal integrate phase where the input voltage is applied to the integrator amplifier via the buffer amplifier. In this phase, the integrator ramps over a fixed period of time in a direction opposite to the polarity of the input voltage.

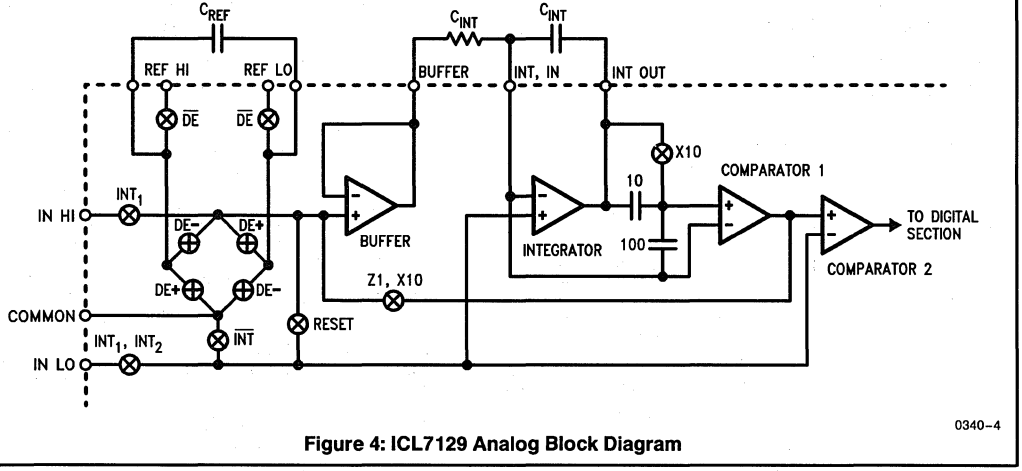


Figure 4: ICL7129 Analog Block Diagram

NOTE: All typical values have been characterized but are not tested.

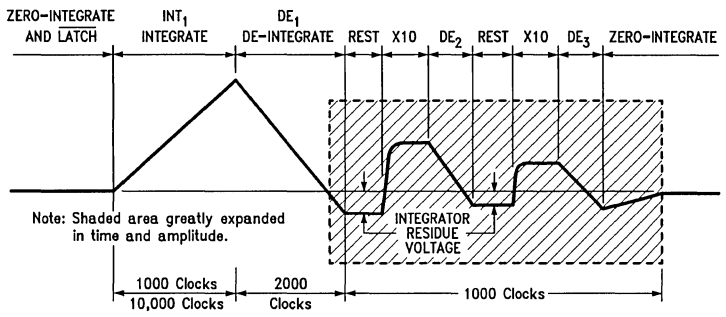


Figure 5: Integrator Waveform for Negative Input Voltage Showing Successive Integration Phases and Residue Voltage

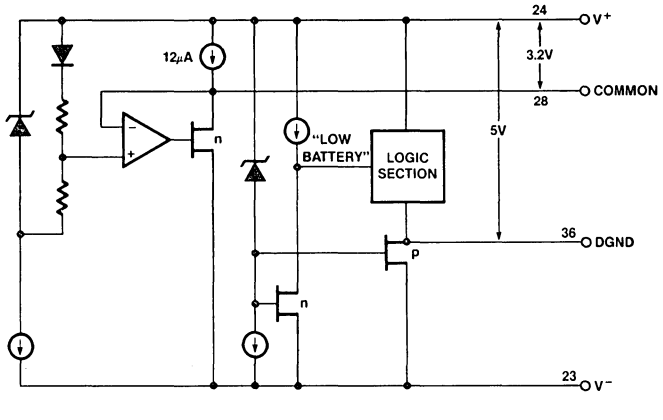


Figure 6: Biasing Structure for COMMON and DGND

DE_1, DE_2, and DE_3 are the de-integrate phases where the reference capacitor is switched in series with the buffer amplifier and the integrator ramps back down to the level it started from before integrating. However, since the de-integrate phase can terminate only at a clock pulse transition, there is always a small overshoot of the integrator past the starting point. The ICL7129 amplifies this overshoot by 10 and DE_2 begins. Similarly DE_2's overshoot is amplified by 10 and DE_3 begins. At the end of DE_3 the results counter holds a number with 5½ digits of resolution. This was obtained by feeding counts into the results counter at the 3½ digit level during DE_1, into the 4½ digit level during DE_2 and the 5½ digit level for DE_3. The effects of offset in the buffer, integrator, and comparator can now be cancelled by repeating this entire sequence with the inputs shorted and subtracting the results from the original reading. For this phase INT_2 switch is closed to give the same common-mode voltage as the measurement cycle. This assures excellent CMRR. At the end of the cycle the data in the up/down results counter is accurate to 0.02% of full-scale and is sent to the display driver for decoding and multiplexing.

COMMON, DGND, AND "LOW BATTERY"

The COMMON and DGND (Digital GrouND) outputs of the ICL7129 are generated from internal zener diodes (Figure 6). COMMON is included primarily to set the common-mode voltage for battery operation or for any system where the input signals float with respect to the power supplies. It also functions as a pre-regulator for an external precision reference voltage source. The voltage between DGND and V^+ is the supply voltage for the logic section of the ICL7129 including the display multiplexer and drivers. Both COMMON and DGND are capable of sinking current from external loads, but caution should be taken to ensure that these outputs are not overloaded. Figure 7 shows the connection of external logic circuitry to the ICL7129. This connection will work providing that the supply current requirements of the logic do not exceed the current sink capability of the DGND pin. If more supply current is required, the buffer in Figure 8 can be used to keep the loading on DGND to a minimum. COMMON can source approximately 12μA while DGND has no source capability.

NOTE: All typical values have been characterized but are not tested.

The "LOW BATTERY" annunciator of the display is turned on when the voltage between V^+ and V^- drops below 7.2V typically. The exact point at which this occurs is determined by the 6.3V zener diode and the threshold voltage of the n-channel transistor connected to the V^- rail in Figure 6. As the supply voltage decreases, the n-channel transistor connected to the V-rail eventually turns off and the "LOW BATTERY" input to the logic section is pulled HIGH, turning on the "LOW BATTERY" annunciator.

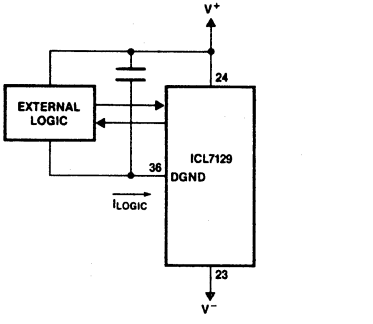


Figure 7: DGND Sink Current

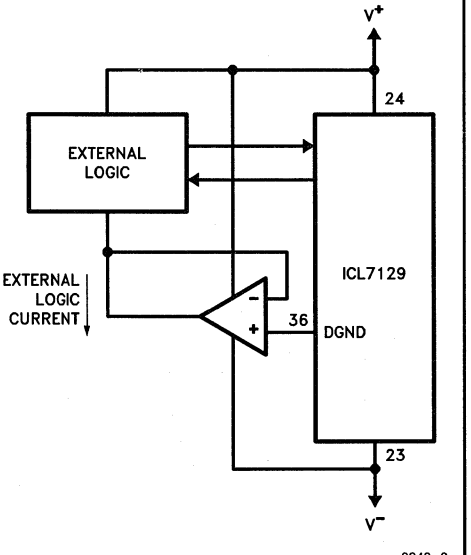


Figure 8: Buffered DGND

I/O PORTS

Four pins of the ICL7129 can be used as either inputs or outputs. The specific pin numbers and functions are described in the Pin Description table (Table 1). If the output function of the pin is not desired in an application it can easily be overridden by connecting the pin to V^+ (HI) or DGND (LO). This connection will not damage the device because the output impedance of these pins is quite high. A simplified schematic of these input/output pins is shown in Figure 9. Since there is approximately 500kΩ in series with the output driver, the pin (when used as an output) can only drive very light loads such as 4000 series, 74CXX type CMOS logic, or other high input impedance devices. The output drive capability of these four pins is limited to 3μA, nominally, and the input switching threshold is typically DGND+2V.

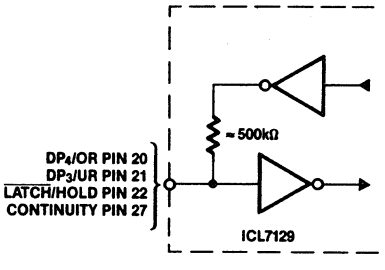


Figure 9: "Weak Output"

LATCH/HOLD, OVERRANGE, AND UNDERRANGE TIMING

The LATCH/HOLD output (pin 22) will be pulled low during the last 100 clock cycles of each full conversion cycle. During this time the final data from the ICL7129 counter is latched and transferred to the display decoder and multiplexer. The conversion cycle and LATCH/HOLD timing are directly related to the clock frequency. A full conversion cycle takes 30,000 clock cycles which is equivalent to 60,000 oscillator cycles. OverRange (OR pin 20) and UnderRange (UR pin 21) outputs are latched on the falling edge of LATCH/HOLD and remain in that state until the end of the next conversion cycle. In addition, digits 1 through 4 are blanked during overrange. All three of these pins are "weak outputs" and can be overridden with external drivers or pull-up resistors to enable their input functions as described in the Pin Description table.

INSTANT CONTINUITY

A comparator with a built-in 200mV offset is connected directly between INPUT HI and INPUT LO of the ICL7129 (Figure 10). The CONTINUITY output (pin 27) will be pulled high whenever the voltage between the analog inputs is less than 200mV. This will also turn on the "CONTINUITY" annunciator on the display. The CONTINUITY output may be used to enable an external alarm or buzzer, thereby giving the ICL7129 an audible continuity checking capability.

NOTE: All typical values have been characterized but are not tested.

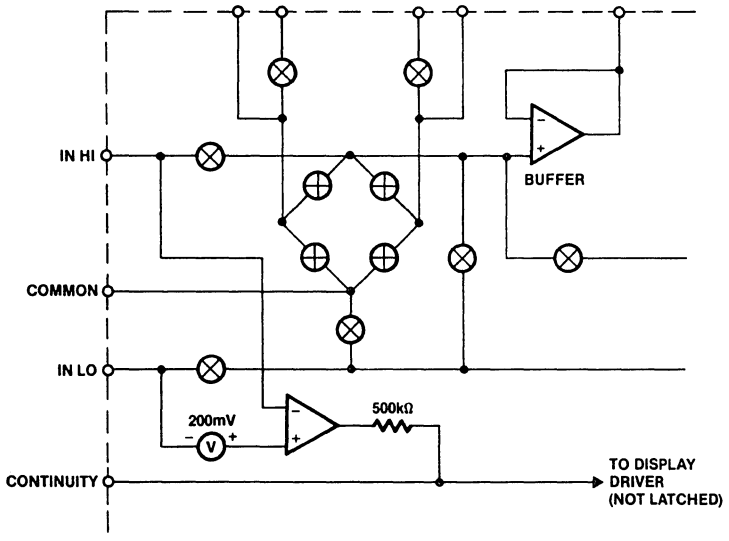


Figure 10: "Instant Continuity" Comparator and Output Structure

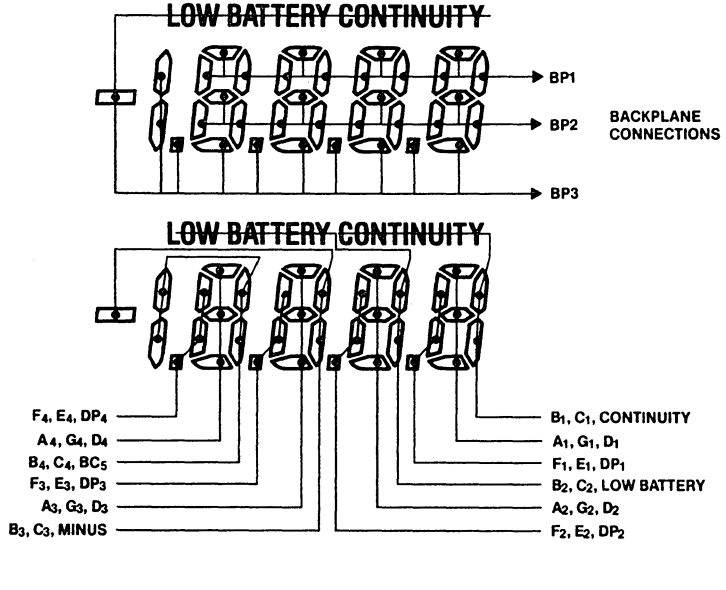
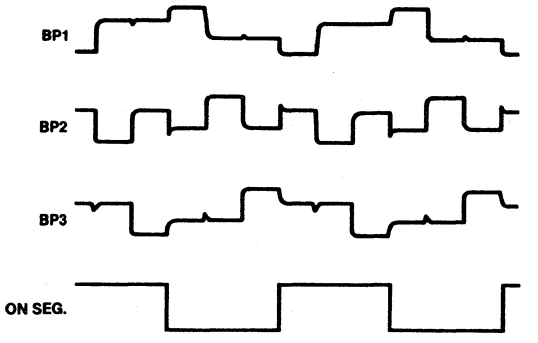


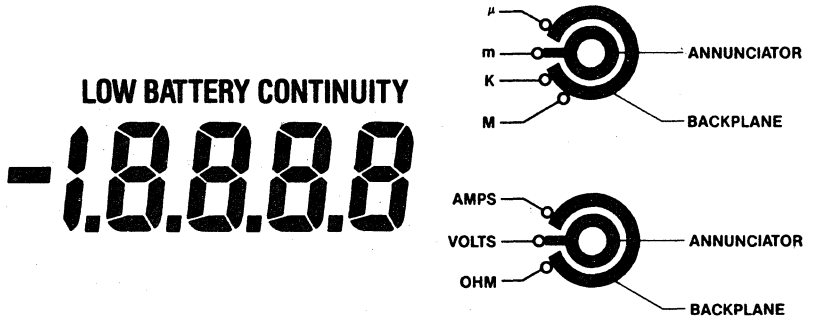
Figure 11: Triplexed Liquid Crystal Display Layout for ICL7129

NOTE: All typical values have been characterized but are not tested.



0340-12

Figure 12: Typical Backplane and Annunciator Drive Waveforms



0340-13

Figure 13: Multimeter Example Showing Use of Annunciator Drive Output

Since the CONTINUITY output is one of the four "weak outputs" of the ICL7129, the "continuity" annunciator on the display can be driven by an external source if desired. The continuity function can be overridden with a pull-down resistor connected between CONTINUITY pin and DGND (pin 36).

DISPLAY CONFIGURATION

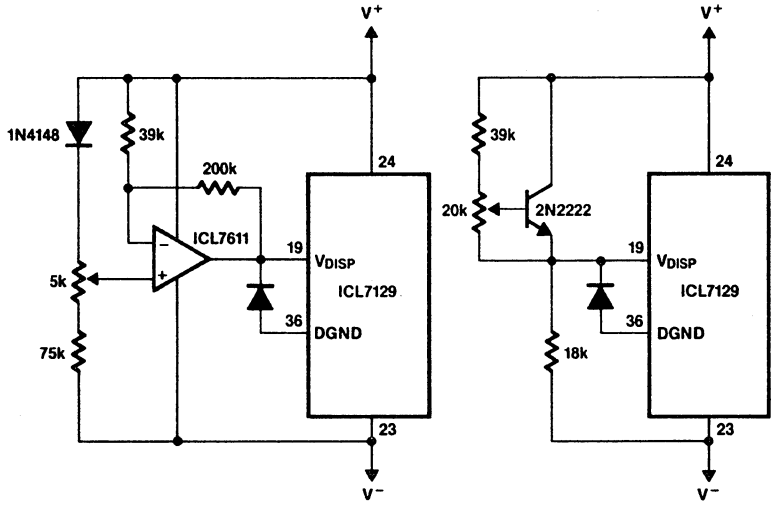
The ICL7129 is designed to drive a triplexed liquid crystal display. This type of display has three backplanes and is driven in a multiplexed format similar to the ICM7231 display driver family. The specific display format is shown in Figure 11. Notice that the polarity sign, decimal points, "LOW BATTERY", and "CONTINUITY" annunciators are directly driven by the ICL7129. The individual segments and annunciators are addressed in a manner similar to row-column addressing. Each backplane (row) is connected to one-third of the total number of segments. BP1 has all F, A, and B segments of the four least significant digits. BP2 has all of the C, E, and G segments. BP3 has all D segments, decimal points, and annunciators. The segment lines (columns) are connected in groups of three bringing all segments of the display out on just 12 lines.

ANNUNCIATOR DRIVE

A special display driver output is provided on the ICL7129 which is intended to drive various kinds of annunciators on custom multiplexed liquid crystal displays. The ANNUNCIATOR DRIVE output (pin 3) is a squarewave signal running at the backplane frequency, approximately 100Hz. This signal swings from V_{DISP} to V^+ and is in sync with the three backplane outputs BP1, BP2, and BP3. Figure 12 shows these four outputs on the same time and voltage scales.

Any annunciator associated with any of the three backplanes can be turned on simply by connecting it to the ANNUNCIATOR DRIVE pin. To turn an annunciator off connect it to its backplane. An example of a display and annunciator drive scheme is shown in Figure 13.

NOTE: All typical values have been characterized but are not tested.



0340-14

Figure 14: Two Methods for Temperature Compensating the Liquid Crystal Display

DISPLAY TEMPERATURE COMPENSATION

For most applications an adequate display can be obtained by connecting V_{DISP} (pin 19) to DGND (pin 36). In applications where a wide temperature range is encountered, the voltage drive levels for some triplexed liquid crystal displays may need to vary with temperature in order to maintain good display contrast and viewing angle. The amount of temperature compensation will depend upon the type of liquid crystal used. Display manufacturers can supply the temperature compensation requirements for their displays. Figure 14 shows two circuits that can be adjusted to give a temperature compensation of $\approx +10mV/°C$ between V^+ and V_{DISP}. The diode between DGND and V_{DISP} should have a low turn-on voltage to assure that no forward current is injected into the chip if V_{DISP} is more negative than DGND.

COMPONENT SELECTION

There are only three passive components around the ICL7129 that need special consideration in selection. They are the reference capacitor, integrator resistor, and integrator capacitor. There is **no** auto-zero capacitor like that found in earlier integrating A/D converter designs.

The integrating resistor is selected to be high enough to assure good current linearity from the buffer amplifier and integrator and low enough that PC board leakage is not a problem. A value of 150kΩ should be optimum for most applications. The integrator capacitor is selected to give an optimum integrator swing at full-scale. A large integrator swing will reduce the effect of noise sources in the comparator but will affect rollover error if the swing gets too close to the positive rail ($\approx 0.7V$). This gives an optimum swing of $\approx 2.5V$ at full-scale. For a 150kΩ integrating resistor and 2 conversions per second the value is 0.10μF. For different conversion rates, the value will change in inverse proportion. A second requirement for good linearity is that the capacitor have low dielectric absorption. Polypropylene caps give good performance at a reasonable price. Finally the foil side of the cap should be connected to the integrator output to shield against pick-up.

The only requirement for the reference cap is that it be low leakage. In order to reduce the effects of stray capacitance, a 1.0μF value is recommended.

CLOCK OSCILLATOR

The ICL7129 achieves its digital range changing by integrating the input signal for 1000 clock pulses (2,000 oscillator cycles) on the 2V scale and 10,000 clock pulses on the 200mV scale. To achieve complete rejection of 60Hz on both scales, an oscillator frequency of 120kHz is required, giving two conversions per second.

In low resolution applications, where the converter uses only 3½ digits and 100μV resolution, an R-C type oscillator is adequate. In this application a C of 51pF is recommended and the resistor value selected from $f_{OSC} = 0.45/RC$. However, when the converter is used to its full potential (4½ digits and 10μV resolution) a crystal oscillator is recom-

NOTE: All typical values have been characterized but are not tested.

mended to prevent the noise from increasing as the input signal is increased due to frequency jitter of the R-C oscillator. Both R-C and crystal oscillator circuits are shown in Figure 15.

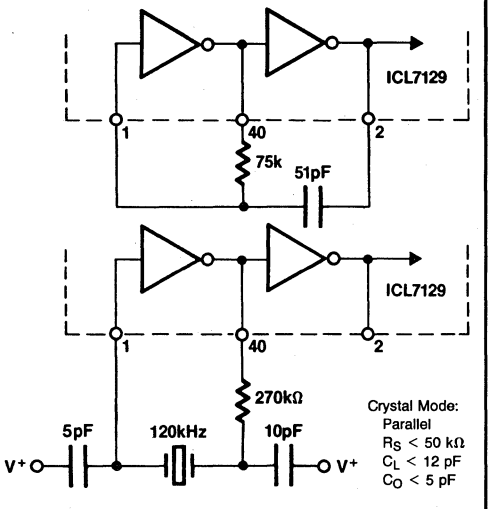


Figure 15: RC and Crystal Oscillator Circuits

POWERING THE ICL7129

The ICL7129 may be operated as a battery powered hand-held instrument or integrated into larger systems that have more sophisticated power supplies. Figures 16, 17, and 18 show various powering modes that may be used with the ICL7129.

The standard supply connection using a 9V battery is shown in Figure 3.

The power connection for systems with +5V and −5V supplies available is shown in Figure 16. Notice that measurements are with respect to ground. COMMON is also tied to INLO to remove any common-mode voltage swing on the integrator amplifier inputs.

It is important to notice that in Figure 16, digital ground of the ICL7129 (DGND pin 36) is **not** directly connected to power supply ground. DGND is set internally to approximately 5V less than the V+ terminal and is not intended to be used as a power input pin. It may be used as the ground reference for external logic, as shown in Figure 7 and 8. In Figure 7, DGND is used as the negative supply rail for external logic provided that the supply current for the external logic does not cause excessive loading on DGND. The DGND output can be buffered as shown in Figure 8. Here, the logic supply current is shunted away from the ICL7129 keeping the load on DGND low. This treatment of the DGND output is necessary to insure compatibility when the external logic is used to interface directly with the logic inputs and outputs of the ICL7129.

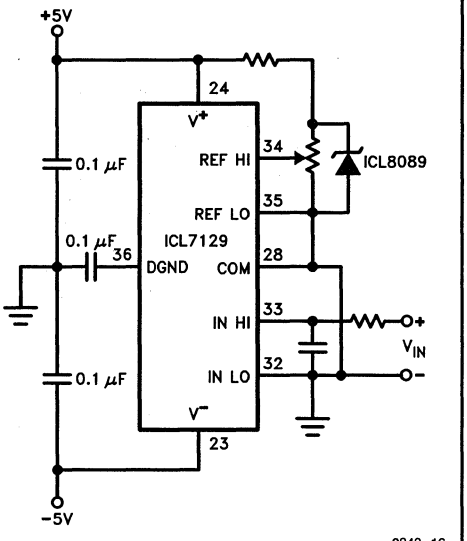


Figure 16: Powering the ICL7129 from +5V and −5V Power Supplies

When a battery voltage between 3.8V and 7V is desired for operation, a voltage doubling circuit should be used to bring the voltage on the ICL7129 up to a level within the power supply voltage range. This operating mode is shown in Figure 17.

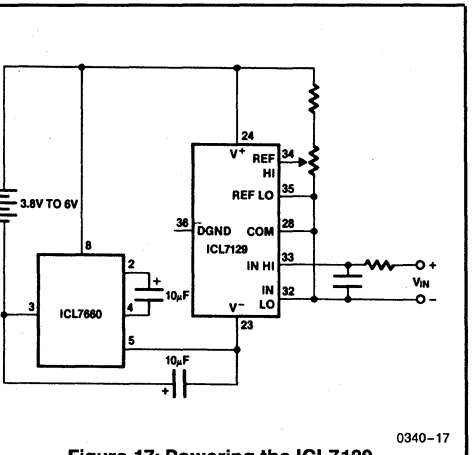


Figure 17: Powering the ICL7129 from a 3.8V to 6V Battery

NOTE: All typical values have been characterized but are not tested.

Again measurements are made with respect to COMMON since the entire system is floating. Voltage doubling is accomplished by using an ICL7660 CMOS voltage converter and two inexpensive electrolytic capacitors. The same principle applies in Figure 18 where the ICL7129 is being used in a system with only a single +5V power supply. Here measurements are made with respect to power supply ground.

A single polarity power supply can be used to power the ICL7129 in applications where battery operation is not appropriate or convenient **only** if the power supply is **isolated** from system ground. Measurements must be made with respect to COMMON or some other voltage within its input common-mode range.

VOLTAGE REFERENCES

The COMMON output of the ICL7129 has a temperature coefficient of ±80ppm/°C typically. This voltage is only suitable as a reference voltage for applications where ambient temperature variations are expected to be minimal. When the ICL7129 is used in most environments, other voltage references should be considered. The diagram in Figures 3 and 18 show the ICL8069 1.2V band-gap voltage source used as the reference for the ICL7129, and the COMMON output as its pre-regulator. The reference voltage for the ICL7129 is set to 1.000V for both 2V and 200mV full-scale operation.

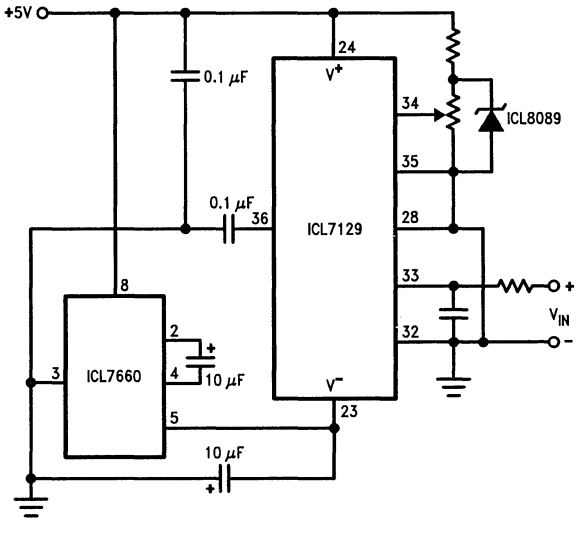


Figure 18: Powering the ICL7129 from a Single Polarity Power Supply

NOTE: All typical values have been characterized but are not tested.

ICL7129
MULTIPLE INTEGRATION A/D CONVERTER EQUATIONS

Oscillator Frequency

$f_{OSC} = 0.45/RC$

$C_{OSC} > 50$ pF; $R_{OSC} > 50$ kΩ

f_{OSC} typ. = 120 kHz

OR

$f_{OSC} = 120$ kHz Crystal (Recommended)

Oscillator Period

$t_{OSC} = 1/f_{OSC}$

Integration Clock Period

$t_{CLOCK} = 2*t_{OSC}$

Integration Period

$t_{INT(2V)} = 1000*t_{CLOCK}$ (Range = 1)

$t_{INT(200\ mV)} = 10{,}000*t_{CLOCK}$ (Range = 0)

60/50 Hz Rejection Criterion

$t_{INT}/t_{60\ Hz}$ or $t_{INT}/t_{50\ Hz}$ = Integer

Optimum Integration Current

$I_{INT} = 13\ \mu A$

Full Scale Analog Input Voltage

V_{INFS} Typically = 200 mV or 2.0V

Integrate Resistor

$R_{INT} = V_{INFS}/I_{INT}$

R_{INT} Typ. = 150 kΩ

Integrate Capacitor

$$C_{INT} = \frac{(t_{INT})(I_{INT})}{V_{INT}}$$

Integrator Output Voltage Swing

$$V_{INT} = \frac{(t_{INT})(I_{INT})}{C_{INT}}$$

V_{INT} Maximum Swing:

$(V^- + 0.5V) < V_{INT} < (V^+ - 0.7V)$

Display Count

$$\text{COUNT} = 10{,}000 \times \frac{V_{IN}}{V_{REF}} \text{ (Range = 1)}$$
(2.0V Range)

$$\text{COUNT} = 10{,}000 \times \frac{V_{IN} \times 10}{V_{REF}} \text{ (Range = 0)}$$
(200 mV Range)

Minimum V_{REF}: 500 mV

Common Mode Input Voltage

$(V^- + 1.0V) < V_{IN} < (V^+ - 0.5V)$

Auto Zero Capacitor: C_{AZ} not used

Reference Capacitor: 0.1 μF < C_{REF} < 1.0 μF

V_{COM}

Biased Between V^+ and V^-.

$V_{COM} \cong V^+ - 2.9V$

Regulation lost when V^+ to $V^- <\cong 6.4V$.

If V_{COM} is externally pulled down to $(V^+$ to $V^-)/2$, the V_{COM} circuit will turn off.

Power Supply: Single 9V

$V^+ - V^- = 9V$

Digital supply is generated internally

$V_{GND} \cong V^+ - 4.5V$

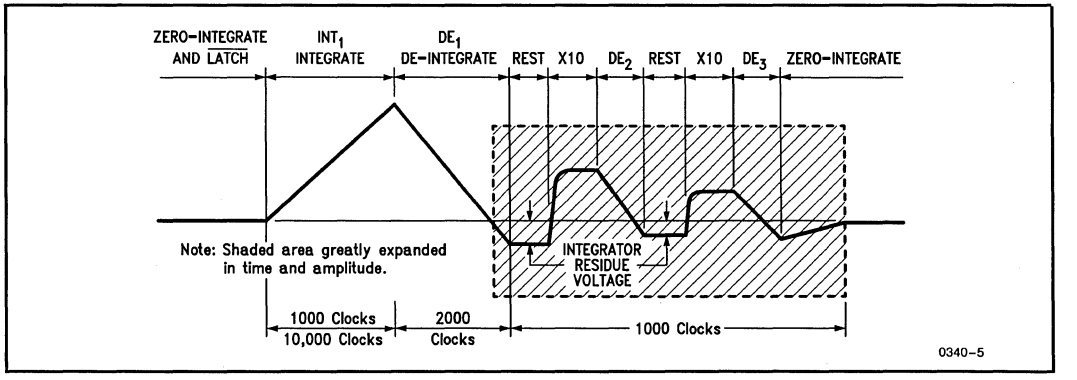
Display: Triplexed LCD

Continuity Output On If

V_{INHI} to $V_{INLO} < 200$ mV

Conversion Cycle (In Both Ranges)

$t_{CYC} = t_{CLOCK} \times 30{,}000$



NOTE: All typical values have been characterized but are not tested.

ICL7136
3½-Digit LCD Low Power A/D Converter

GENERAL DESCRIPTION

The Harris ICL7136 is a high performance, very low power 3½-digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven-segment decoders, display drivers, reference, and clock. The 7136 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive. The supply current is under 100μA, ideally suited for 9V battery operation.

The 7136 brings together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy, like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation allows a high performance panel meter to be built with the addition of only 7 passive components and a display.

The ICL7136 is an improved version of the ICL7126, eliminating the overrange hangover and hysteresis effects, and should be used in its place in all applications. It can also be used as a plug-in replacement for the ICL7106 in a wide variety of applications, changing only the passive components.

FEATURES

- **First-Reading Recovery From Overrange Gives Immediate "OHMS" Measurement**
- **Guaranteed Zero Reading for 0V Input**
- **True Polarity at Zero for Precise Null Detection**
- **1pA Typical Input Current**
- **True Differential Input and Reference**
- **Direct LCD Display Drive — No External Components Required**
- **Pin Compatible With The ICL7106, ICL7126**
- **Low Noise — 15μVp-p Without Hysteresis or Overrange Hangover**
- **On-Chip Clock and Reference**
- **Low Power Dissipation, Guaranteed Less Than 1mW — Gives 8,000 Hours Typical 9V Battery Life**
- **No Additional Active Circuits Required**

2

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7136CPL	0°C to +70°C	40 Pin Plastic DIP
ICL7136RCPL	0°C to +70°C	40 Pin Plastic DIP (Note 1)
ICL7136CM44	0°C to +70°C	44 Pin Surface Mount (Note 2)

NOTES 1. "R" indicates device with reversed leads.
2. Add "T" to part number to specify tape and reel packaging.

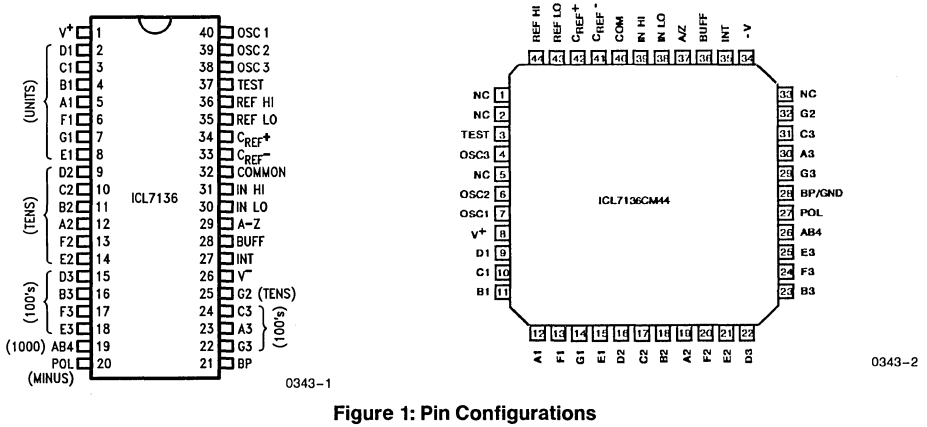


Figure 1: Pin Configurations

301668-004

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input)(Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... TEST to V^+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTES 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

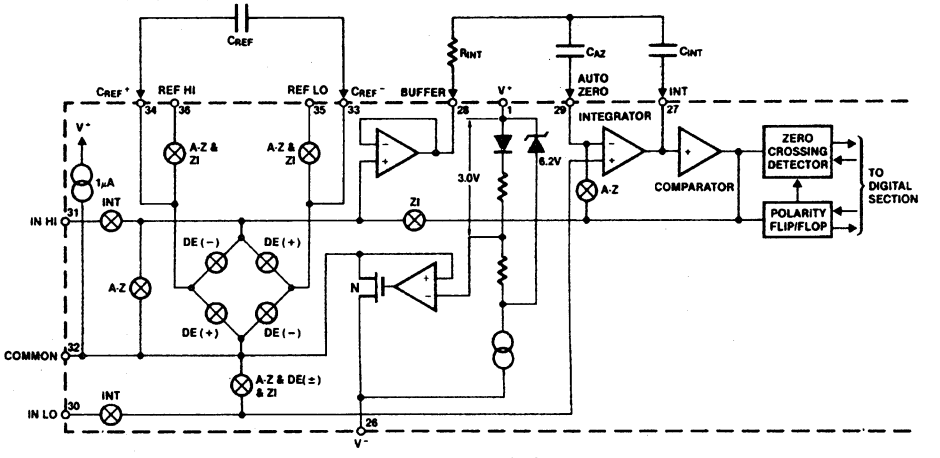


Figure 2: Functional Diagram 0343-3

ELECTRICAL CHARACTERISTICS (Notes 3, 7)

Parameter	Test Conditions	Min	Typ	Max	Units
Zero Input Reading	V_{IN} = 0.0V Full-Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN} = +V_{IN} \cong$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-scale = 200mV or Full-Scale = 2.000V	−1	±0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full-Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V, Full Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA

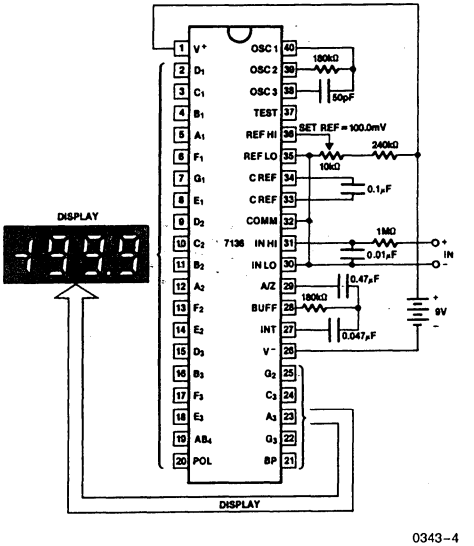
NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Notes 3, 7) (Continued)

Parameter	Test Conditions	Min	Typ	Max	Unit
Zero Reading Drift	$V_{IN}=0V$, $0°C<T_A<+70°C$		0.2	1	μV/°C
Scale Factor Temperature Coefficient	$V_{IN}=199.0mV$, $0°C<T_A<+70°C$ (Ext. Ref. Oppm/°C)		1	5	ppm/°C
Supply Current (Does not include COMMON current)	$V_{IN}=0V$ (Note 6)		70	100	μA
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250kΩ between Common and Positive Supply		150		ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V^+ to $V^-=9V$	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V^+ to $V^-=9V$	4	5	6	V
Power Dissipation Capacitance	vs Clock Frequency		40		pF

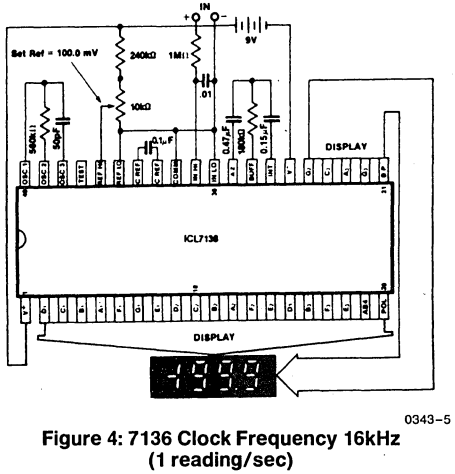
NOTES: 3. Unless otherwise noted, specifications apply at $T_A=25°C$, $f_{clock}=16kHz$ and are tested in the circuit of Figure 4.
4. Refer to "Differential Input" discussion.
5. Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
6. 48kHz oscillator, Figure 5, increases current by 20μA (typ).
7. Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

TEST CIRCUITS



0343-4

Figure 3: ICL7136 with Liquid Crystal Display



0343-5

Figure 4: 7136 Clock Frequency 16kHz (1 reading/sec)

NOTE: All typical values have been characterized but are not tested.

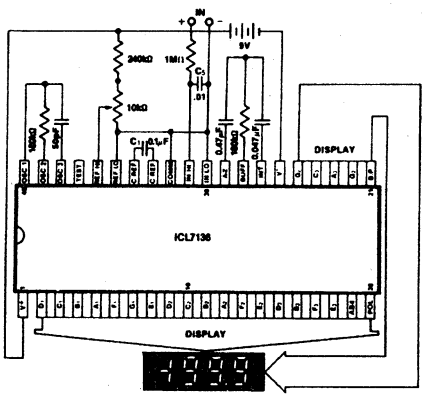


Figure 5: Clock Frequency 48kHz (3 readings/sec)

DETAILED DESCRIPTION (Analog Section)

Figure 2 shows the Functional Diagram of the Analog Section for the ICL7136. Each measurement cycle is divided into four phases. They are 1) auto-zero (A-Z), 2) signal integrate (INT), 3) de-integrate (DE) and 4) zero integrator (ZI).

AUTO-ZERO PHASE

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ}, to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

SIGNAL INTEGRATE PHASE

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common-mode range; within 1V of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

DE-INTEGRATE PHASE

The next phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically, the digital reading displayed is 1000 (V_{IN}/V_{REF}).

ZERO INTEGRATOR PHASE

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Finally, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal conditions, this phase lasts for between 11 to 140 clock pulses, but after a "heavy" overrange conversion, it is extended to 740 clock pulses.

Differential Input

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 0.5V below the positive supply to 1.0V above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage caused by the reference capacitance losing or gaining charge to stray capacity on its nodes. If there is a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Values Selection).

Analog Common

This pin is included primarily to set the common-mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 3.0V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance ($\cong$35Ω), and a temperature coefficient typically less than 150ppm/°C.

NOTE: All typical values have been characterized but are not tested.

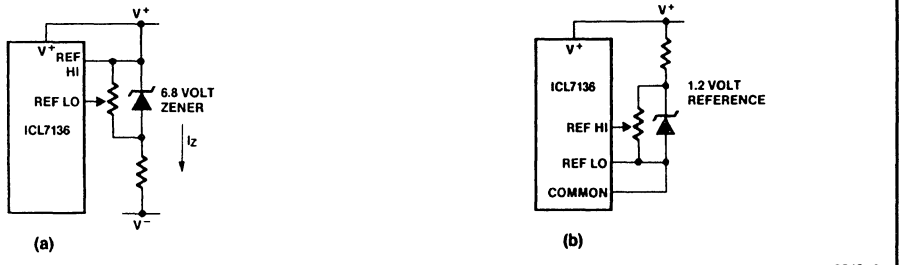


Figure 6: Using an External Reference

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2°C to 8°C, typical for instruments, can give a scale factor error of a count or more. Also, the COMMON voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (<7V). These problems are eliminated if an external reference is used, as shown in Figure 6.

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If the reference can be conveniently referred to analog COMMON, it should be since this removes the common-mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET which can sink 3mA or more of current to hold the voltage 3.0V below the positive supply (when a load is trying to pull the common line positive). However, there is only 1μA of source current, so COMMON may easily be tied to a more negative voltage, thus overriding the internal reference.

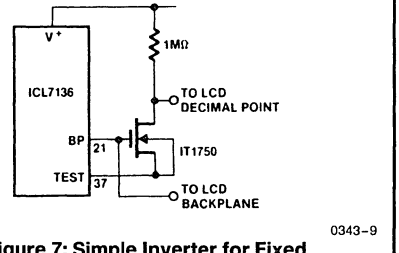


Figure 7: Simple Inverter for Fixed Decimal Point

TEST

The TEST pin serves two functions. It is coupled to the internally generated digital supply through a 500Ω resistor. Thus, it can be used as the negative supply for external segment drivers such as for decimal points or any other presentation the user may want to include on the LCD display. Figures 7 and 8 show such an application. No more than a 1mA load should be applied.

The second function is a "lamp test." When TEST is pulled high (to V+) all segments will be turned on and the display should read −1888. The TEST pin will sink about 10mA under these conditions.

Caution: In the lamp test mode, the segments have a constant DC voltage (no square-wave). This may burn the LCD display if maintained for extended periods.

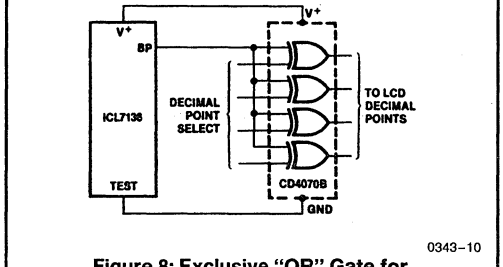


Figure 8: Exclusive "OR" Gate for Decimal Point Drive

DETAILED DESCRIPTION (Digital Section)

Figure 9 shows the digital section for the 7136. An internal digital ground is generated from a 6V Zener diode and a large P channel source follower. This supply is made stiff to absorb the relatively large capacitive currents when the backplane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square-wave with a nominal amplitude of 5V. The segments are driven at the same frequency and

NOTE: All typical values have been characterized but are not tested.

DISPLAY FONT

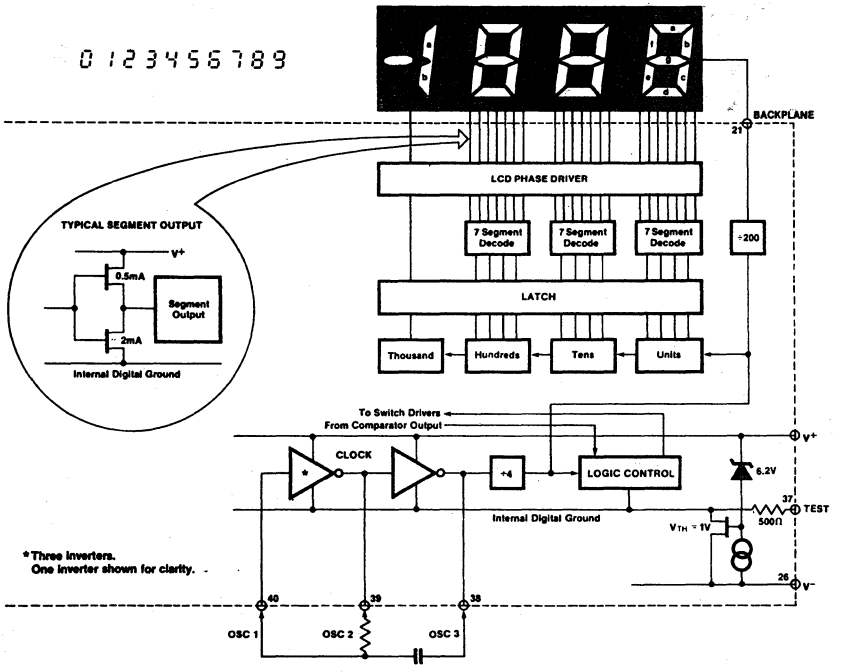


Figure 9: Digital Section

amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

System Timing

Figure 10 shows the clock oscillator provided in the 7136. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the

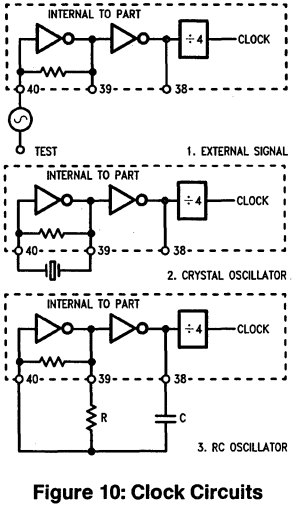


Figure 10: Clock Circuits

NOTE: All typical values have been characterized but are not tested.

four convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 counts to 2000 counts), zero integrator (11 counts to 140 counts*) and auto-zero (910 counts to 2900 counts). For signals less than full-scale, auto-zero gets the unused portion of reference de-integrate and zero integrator. This makes a complete measure cycle of 4000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of the 60Hz period. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33⅓kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66⅔kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz). See also A052.

COMPONENT VALUE SELECTION

(See also A052)

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6μA of quiescent current. They can supply ~1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full-scale, 1.8MΩ is near optimum, and similarly 180kΩ for a 200.0mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3V from either supply). When the analog COMMON is used as a reference, a nominal ±2V full-scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.047μF, for 1 reading/second (16kHz) 0.15μF. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full-scale where noise is very important, a 0.47μF capacitor is recommended. The ZI phase allows a large auto-zero capacitor to be used without causing the hysteresis or overrange hangover problems that can occur with the ICL7126 or ICL7106 (see A032).

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common-mode voltage exists (i.e., the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally, 1.0μF will hold the roll-over error to 0.5 count in this instance.

*After an overranged conversion of more than 2060 counts, the zero integrator phase will last 740 counts, and auto-zero will last 260 counts.

Oscillator Components

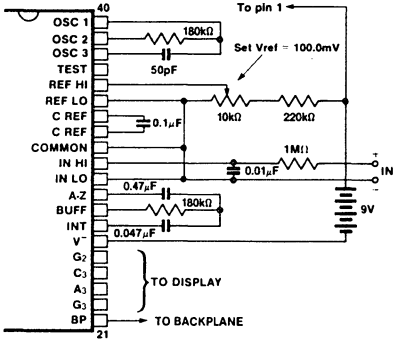
For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation f~0.45/RC. For 48kHz clock (3 readings/second), R=180kΩ, for 16kHz, R=560kΩ.

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is $V_{IN}=2V_{REF}$. Thus, for the 200.0mV and 2.000V scale, V_{REF} should equal 100.0mV and 1.000V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and select $V_{REF}=0.341V$. A suitable value for the integrating resistor would be 330kΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN}\neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

TYPICAL APPLICATIONS

The 7136 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

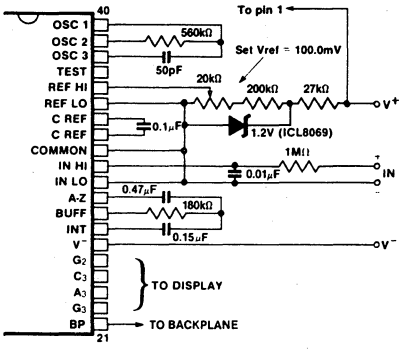


0343-13

Figure 11: 7136 Using the Internal Reference

Values shown are for 200.0mV full-scale, 3 readings/sec, floating supply voltage (9V battery).

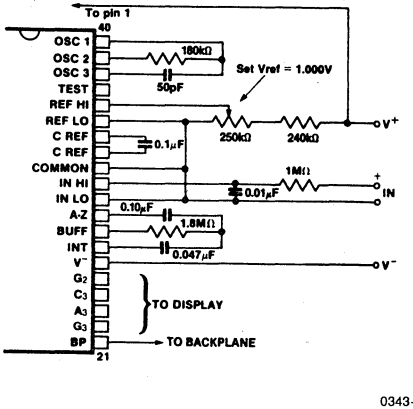
NOTE: All typical values have been characterized but are not tested.



0343-14

Figure 12: 7136 with an External Band-Gap Reference (1.2V Type)

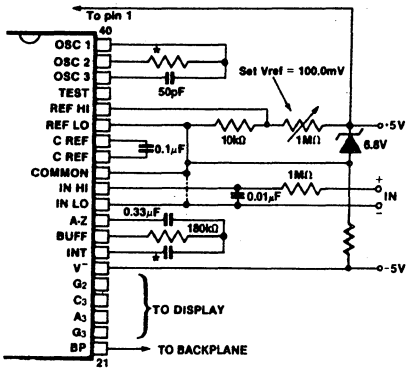
IN LO is tied to COMMON, thus establishing the correct common-mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading/sec.



0343-15

Figure 13: Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec

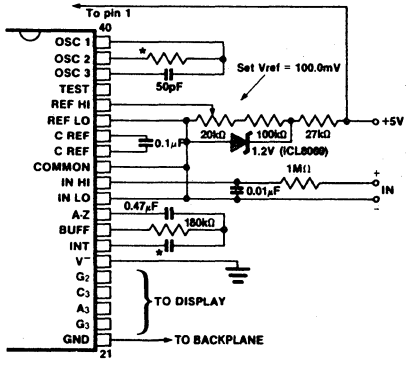
For 1 reading/sec, change C_{INT}, R_{OSC} to values of Figure 12.



0343-16

Figure 14: 7136 with Zener Diode Reference

Since low TC zeners have breakdown voltages ~6.8V, diode must be placed across the total supply (10V). As in the case of Figure 13, IN LO may be tied to COMMON.



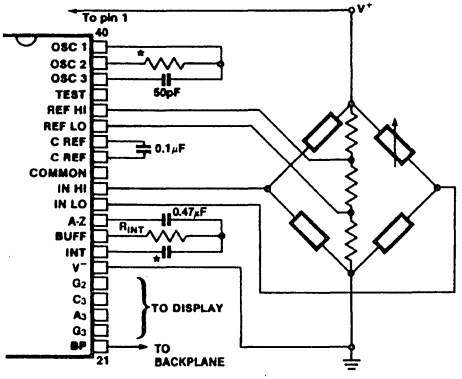
0343-17

Figure 15: 7136 Operated from Single +5V Supply

An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.

*Values depend on clock frequency. See Figures 11, 12, 13.

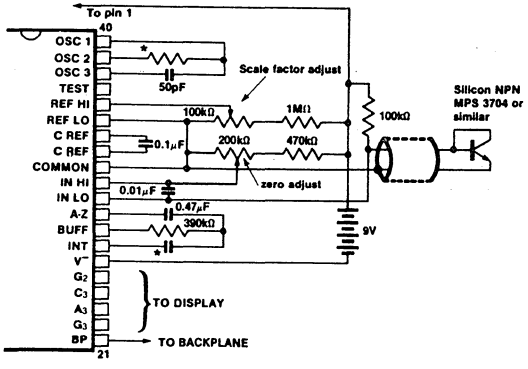
NOTE: All typical values have been characterized but are not tested.



0343-18

Figure 16: 7136 Measuring Ratiometric Values of Quad Load Cell

The resistor values within the bridge are determined by the desired sensitivity.

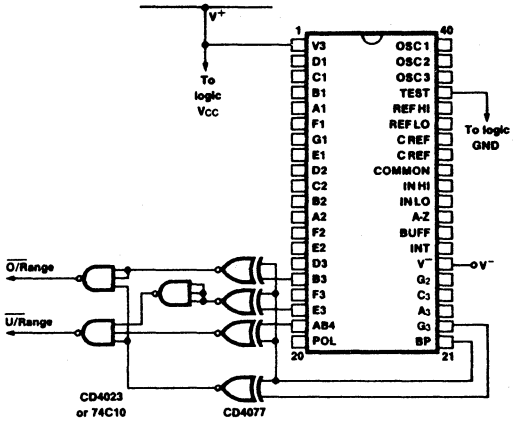


0343-19

Figure 17: 7136 used as a Digital Centigrade Thermometer

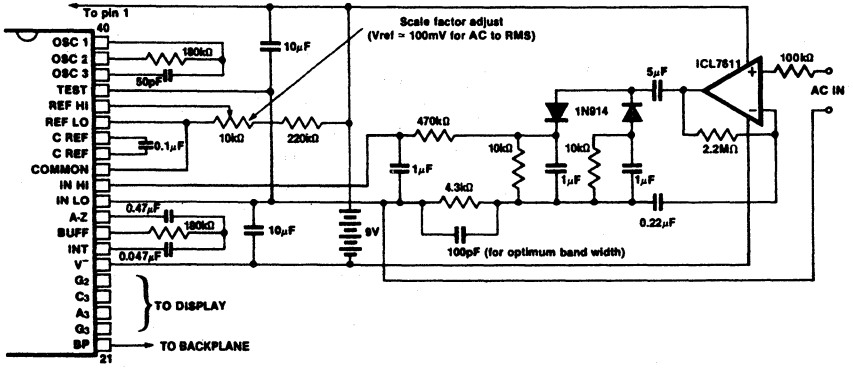
A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading. See ICL807¾ and AD590 data sheets for alternative circuits.

NOTE: All typical values have been characterized but are not tested.



0343-20

Figure 18: Circuit for Developing Underrange and Overrange Signals from 7136 Outputs



0343-21

Figure 19: AC to DC Converter with 7136

Test is used as a common-mode reference level to ensure compatibility with most op amps.

NOTE: All typical values have been characterized but are not tested.

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar.

A017 "The Integrating A/D Converter," by Lee Evans.

A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.

A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.

A032 "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.

A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.

A047 "Games People Play with Harris' A/D Converters," edited by Peter Bradshaw.

A052 "Tips for Using Single-Chip 3½-Digit A/D Converters," by Dan Watson.

NOTE: All typical values have been characterized but are not tested.

ICL7136
INTEGRATING A/D CONVERTER EQUATIONS

Oscillator Frequency

$f_{OSC} = 0.45/RC$

$C_{OSC} > 50$ pF; $R_{OSC} > 50$ kΩ

f_{OSC} typically = 48 kHz

Oscillator Period

$t_{OSC} = RC/0.45$

Integration Clock Frequency

$f_{CLOCK} = f_{OSC}/4$

Integration Period

$t_{INT} = 1000 \times (4/f_{OSC})$

60/50 Hz Rejection Criterion

$t_{INT}/t_{60\ Hz}$ or $t_{INT}/t_{50\ Hz}$ = Integer

Optimum Integration Current

$I_{INT} = 1.0\ \mu A$

Full Scale Analog Input Voltage

V_{INFS} typically = 200 mV or 2.0V

Integrate Resistor

$$R_{INT} = \frac{V_{INFS}}{I_{INT}}$$

Integrate Capacitor

$$C_{INT} = \frac{(t_{INT})(I_{INT})}{V_{INT}}$$

Integrator Output Voltage Swing

$$V_{INT} = \frac{(t_{INT})(I_{INT})}{C_{INT}}$$

V_{INT} Maximum Swing:

$(V^- + 0.5V) < V_{INT} < (V^+ - 0.5V)$

V_{INT} typically = 2.0V

Display Count

$$COUNT = 1000 \times \frac{V_{IN}}{V_{REF}}$$

Conversion Cycle

$t_{CYC} = t_{CLOCK} \times 4{,}000$

$t_{CYC} = t_{OSC} \times 16{,}000$

when f_{OSC} = 48 kHz; t_{CYC} = 333 ms

Common Mode Input Voltage

$(V^- + 1.0V) < V_{IN} < (V^+ - 0.5V)$

Auto Zero Capacitor

$0.01\ \mu F < C_{AZ} < 1.0\ \mu F$

Reference Capacitor

$0.1\ \mu F < C_{REF} < 1.0\ \mu F$

V_{COM}

Biased between V^+ and V^-.

$V_{COM} \cong V^+ - 2.8V$

Regulation lost when V^+ to $V^- \leq \cong 6.4V$.

If V_{COM} is externally pulled down to $(V^+$ to $V^-)/2$, the V_{COM} circuit will turn off.

Power Supply: Single 9V

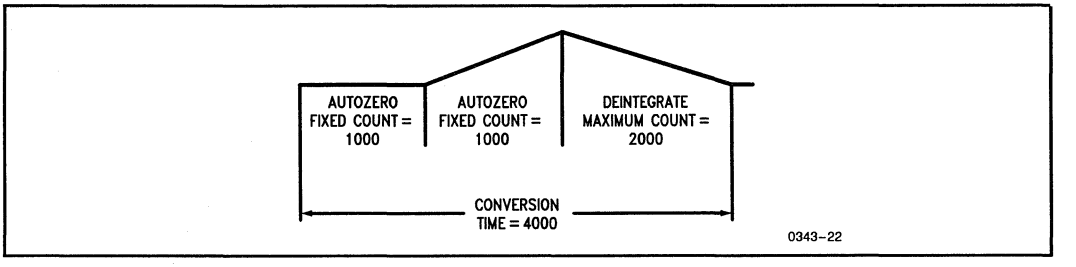
$V^+ - V^- = 9V$

Digital supply is generated internally

$V_{GND} \cong V^+ - 4.5V$

Display: LCD

Type: Direct drive with digital logic supply amplitude.



NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICL7137
3½-Digit LED Low Power Single-Chip A/D Converter

GENERAL DESCRIPTION

The Harris ICL7137 is a high performance, very low power 3½-digit A/D converter. All the necessary active devices are contained on a single CMOS IC, including seven-segment decoders, display drivers, reference, and clock. The 7137 is designed to interface with a light emitting diode (LED) display. The supply current (exclusive of display) is under 200μA, ideally suited for battery operation.

The 7137 brings together an unprecedented combination of high accuracy, versatility, and true economy. The device features auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of the ICL7137 allows a high performance panel meter to be built with the addition of only 10 passive components and a display.

The ICL7137 is an improved version of the ICL7107, eliminating the overrange hangover and hysteresis effects, and should be used in its place in all applications, changing only the passive component values.

FEATURES

- **First-Reading Recovery From Overrange allows Immediate "OHMS" Measurement**
- **Guaranteed Zero Reading for 0V Input**
- **True Polarity at Zero for Precise Null Detection**
- **1pA Typical Input Current**
- **True Differential Input and Reference**
- **Direct LED Display Drive — No External Components Required**
- **Pin Compatible With The ICL7107**
- **Low Noise — 15μVp-p Without Hysteresis or Overrange Hangover**
- **On-Chip Clock and Reference**
- **Improved Rejection of Voltage On COMMON Pin**
- **No Additional Active Circuits Required**

2

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7137CPL	0°C to +70°C	40 Pin Plastic DIP

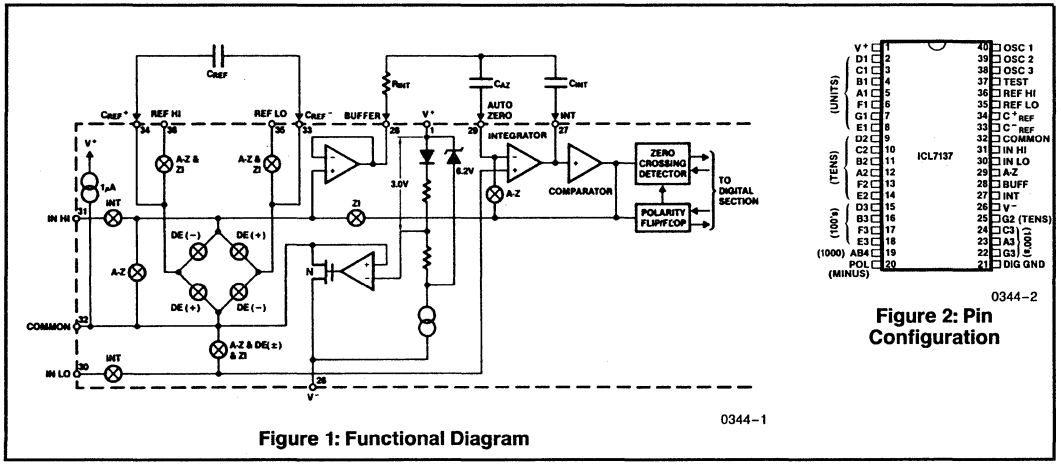


Figure 1: Functional Diagram

Figure 2: Pin Configuration

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V^+ ..... +6V
V^- ..... −9V
Analog Input Voltage (either input)(Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... GND to V^+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

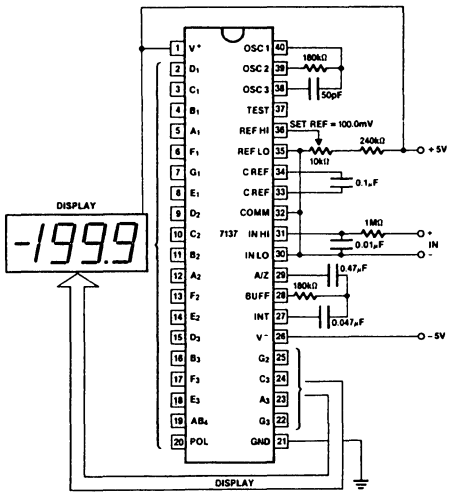
NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS (Note 3)

Parameter	Test Conditions	Min	Typ	Max	Unit
Zero Input Reading	V_{IN} = 0.0V Full-Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	998	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN} = +V_{IN} \cong$ 200.0mV	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-scale = 200mV or Full-Scale = 2.000V	−1	±0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	V_{CM} = ±1V, V_{IN} = 0V Full-Scale = 200.0mV		30		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V, Full-Scale = 200.0mV		15		μV
Leakage Current @ Input	V_{IN} = 0V		1	10	pA
Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV, 0°C < T_A < +70°C (Ext. Ref. Oppm/°C)		1	5	ppm/°C
V^+ Supply Current (Does not Include LED current)	V_{IN} = 0V (Note 5)		70	200	μA
V^- Supply current			40		
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250kΩ between Common and Positive Supply		150		ppm/°C
Segment Sinking Current (Except Pins 19 & 20) (Pin 19 only) (Pin 20 only)	V^+ = 5.0V Segment Voltage = 3V	5 10 4	8.0 16 7		mA
Power Dissipation Capacitance	vs. Clock Frequency		40		pF

NOTES: 3. Unless otherwise noted, specifications apply at T_A = 25°C, f_{clock} = 16kHz and are tested in the circuit of Figure 4.
4. Refer to "Differential Input" discussion.
5. 48kHz oscillator, Figure 5, increases current by 35μA (typ).
6. Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

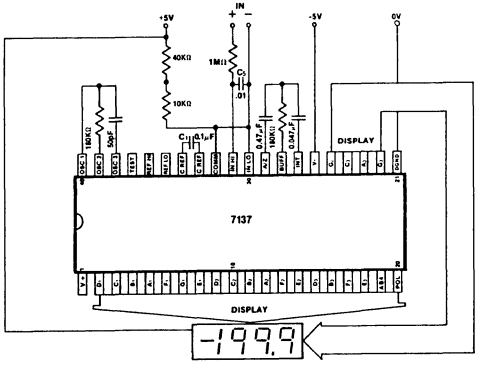
NOTE: All typical values have been characterized but are not tested.



0344-3

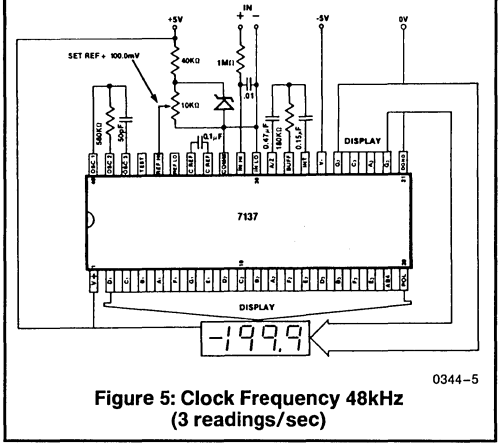
Figure 3: ICL7137 with LED Display

TEST CIRCUITS



0344-4

Figure 4: 7137 Clock Frequency 16kHz (1 reading/sec)



0344-5

Figure 5: Clock Frequency 48kHz (3 readings/sec)

DETAILED DESCRIPTION (Analog Section)

Figure 1 shows the Functional Diagram of the Analog Section for the ICL7137. Each measurement cycle is divided into four phases. They are 1) auto-zero (A-Z), 2) signal integrate (INT), 3) de-integrate (DE) and 4) zero-integrator (ZI).

AUTO-ZERO PHASE

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor, C_{AZ}, to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

SIGNAL INTEGRATE PHASE

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common-mode range; within 1V of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

NOTE: All typical values have been characterized but are not tested.

DE-INTEGRATE PHASE

The next phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically; the digital reading displayed is $1000(V_{IN}/V_{REF})$.

ZERO INTEGRATOR PHASE

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Finally, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal conditions, this phase lasts for between 11 to 140 clock pulses, but after a "heavy" overrange conversion, it is extended to 740 clock pulses.

Differential Input

The input can accept differential voltages anywhere within the common-mode range of the input amplifier; or specifically from 0.5V below the positive supply to 1.0V above the negative supply. In this range the system has a CMRR of 90dB typical. However, since the integrator also swings with the common-mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common-mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage caused by the reference capacitance losing or gaining charge to stray capacity on its nodes. If there is a large common-mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Value Selection).

Analog Common

This pin is included primarily to set the common-mode voltage for battery operation or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 3.0V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (0.001%/%), low output impedance(≅35Ω), and a temperature coefficient typically less than 150ppm/°C.

The limitations of the on-chip reference should also be recognized, however. The reference temperature coefficient (TC) can cause some degradation in performance. Temperature changes of 2°C to 8°C, typical for instruments, can give a scale factor error of a count or more. Also, the COMMON voltage will have a poor voltage coefficient when the total supply voltage is less than that which will cause the zener to regulate (<7V). These problems are eliminated if an external reference is used, as shown in Figure 6.

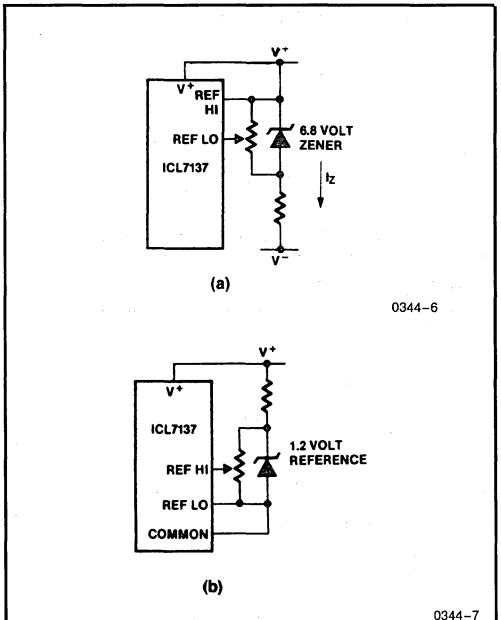


Figure 6: Using an External Reference

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If the reference can be conveniently referred to analog COMMON, it should be since this removes the common-mode voltage from the reference system.

NOTE: All typical values have been characterized but are not tested.

Within the IC, analog COMMON is tied to an N channel FET which can sink 100μA or more of current to hold the voltage 3.0V below the positive supply (when a load is trying to pull the common line positive). However, there is only 1μA of source current, so COMMON may easily be tied to a more negative voltage, thus overriding the internal reference.

TEST

The TEST pin is coupled to the internal digital supply through a 500Ω resistor, and functions as a "lamp test." When TEST is pulled high (to V+) all segments will be turned on and the display should read — 1888. The TEST pin will sink about 10mA under these conditions.

DISPLAY FONT

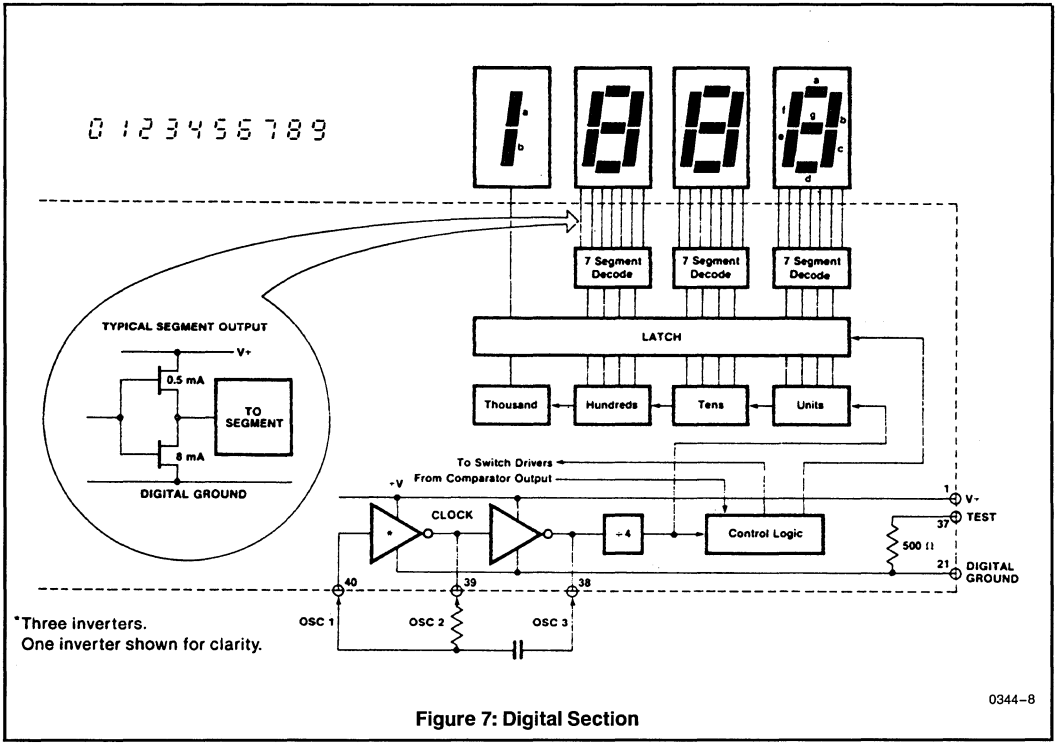


Figure 7: Digital Section

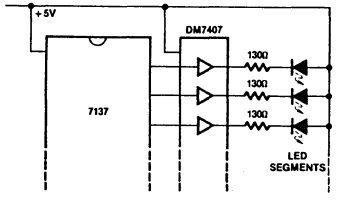


Figure 8: Display Buffering for Increased Drive Current

DETAILED DESCRIPTION (Digital Section)

Figure 7 shows the digital section for the 7137. The segments are driven at 8mA, suitable for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA. The polarity indication is "ON" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

Figure 8 shows a method of increasing the output drive current, using four DM7407 Hex Buffers. Each buffer is capable of sinking 40mA.

NOTE: All typical values have been characterized but are not tested.

System Timing

Figure 9 shows the clock oscillator provided in the 7137. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An RC oscillator using all three pins.

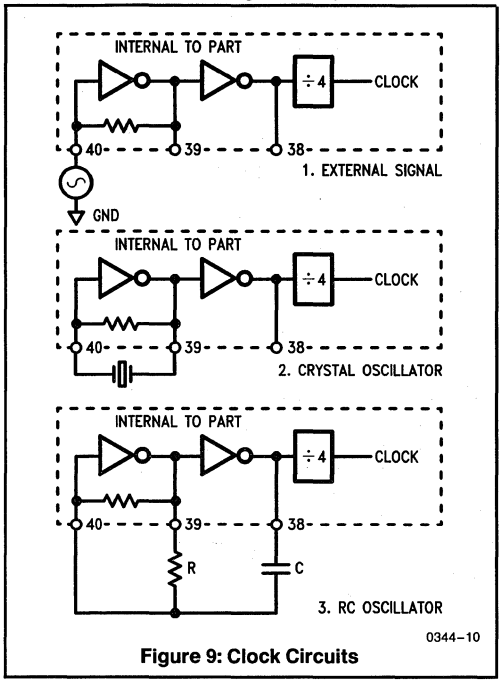


Figure 9: Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the four convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 counts to 2000 counts), zero integrator (11 counts to 140 counts*) and auto-zero (910 counts to 2900 counts). For signals less than full-scale, auto-zero gets the unused portion of reference de-integrate and zero integrator. This makes a complete measure cycle of 4000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of the 60Hz period. Oscillator frequencies of 60kHz, 48kHz, 40kHz, 33⅓kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 66⅔kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz.) See also A052.

*After an overranged conversion of more than 2060 counts, the zero integrator phase will last 740 counts, and auto-zero will last 260 counts.

COMPONENT VALUE SELECTION

(See Application Note A052)

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 6μA of quiescent current. They can supply ~1μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full-scale, 1.8MΩ is near optimum, and similarly 180kΩ for a 200.0mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3V from either supply). When the analog COMMON is used as a reference, a nominal ±2V full-scale integrator swing is fine. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.047μF, for 1 reading/second (16kHz) 0.15μF. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

The integrating capacitor should have low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full-scale where noise is very important, a 0.47μF capacitor is recommended. The ZI phase allows a large auto-zero capacitor to be used without causing the hysteresis or overrange hangover problems that can occur with the ICL7107 or ICL7117 (See Application Note A032).

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common-mode voltage exists (i.e., the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally, 1.0μF will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

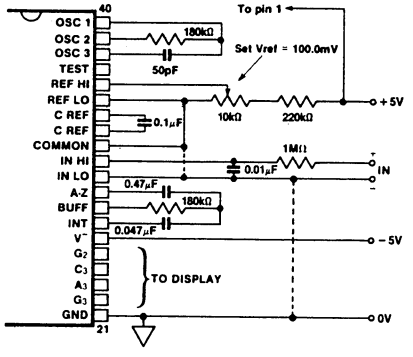
For all ranges of frequency a 50pF capacitor is recommended and the resistor is selected from the approximate equation $f \cong 0.45/RC$. For 48kHz clock (3 readings/second), R=180kΩ, while for 16kHz (1 reading/sec), R=560kΩ.

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN}=2V_{REF}$. Thus, for the 200.0mV and 2,000V scale, V_{REF} should equal 100.0mV and 1.000V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down

NOTE: All typical values have been characterized but are not tested.

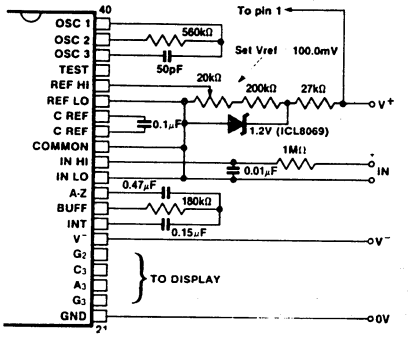
to 200.0mV, the designer should use the input voltage directly and select $V_{REF} = 0.341V$. A suitable value for the integrating resistor would be 330kΩ. This makes the system slightly quieter and also avoids the necessity of a divider network on the input. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.



0344-11

Figure 10: 7137 Using the Internal Reference.

Values shown are for 200.0mV full-scale, 3 readings/sec. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)



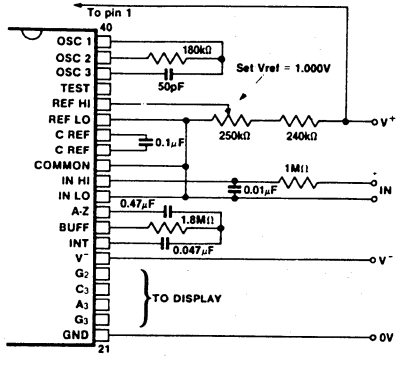
0344-12

Figure 11: 7137 with an External Band-Gap Reference (1.2V Type).

IN LO is tied to COMMON, thus establishing the correct common-mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading/sec.

TYPICAL APPLICATIONS

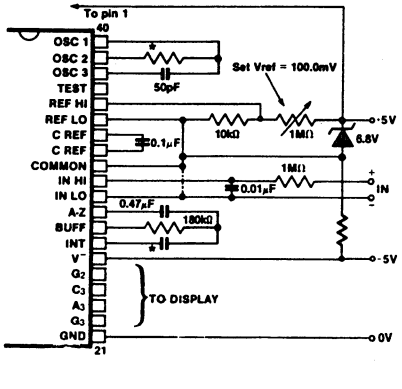
The 7137 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.



0344-13

Figure 12: Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec.

For 1 reading/sec, change C_{INT}, R_{OSC} to values of Figure 11.

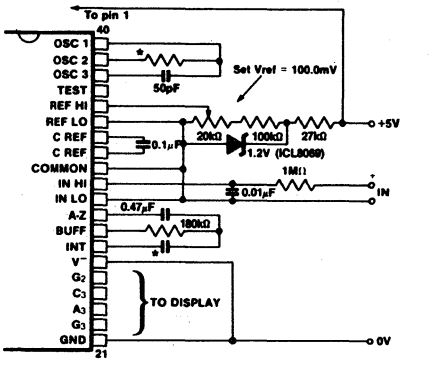


0344-14

Figure 13: 7137 with Zener Diode Reference.

Since low TC zeners have breakdown voltages ~ 6.8V, diode must be placed across the total supply (10V). As in the case of Figure 11, IN LO may be tied to COMMON.

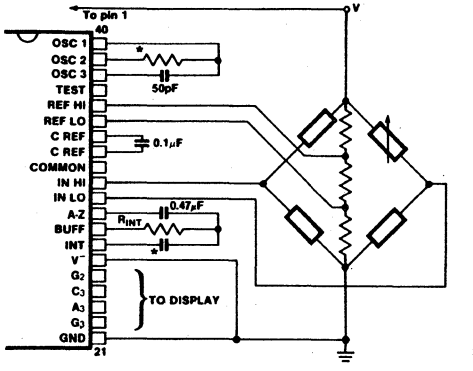
NOTE: All typical values have been characterized but are not tested.



0344-15

Figure 14: 7137 Operated from Single +5V Supply.

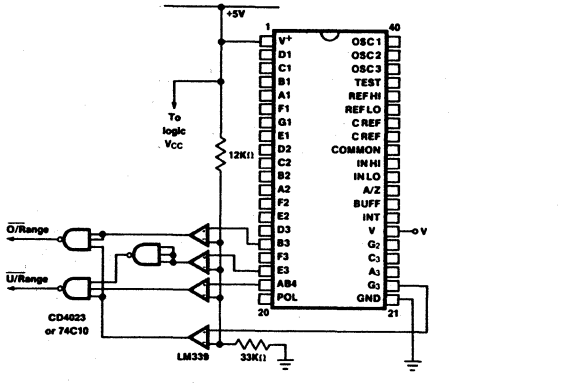
An external reference must be used in this application, since the voltage between V^+ and V^- is insufficient for correct operation of the internal reference.



0344-16

Figure 15: Measuring Ratiometric Values of Quad Load Cell.

The resistor values within the bridge are determined by the desired sensitivity.



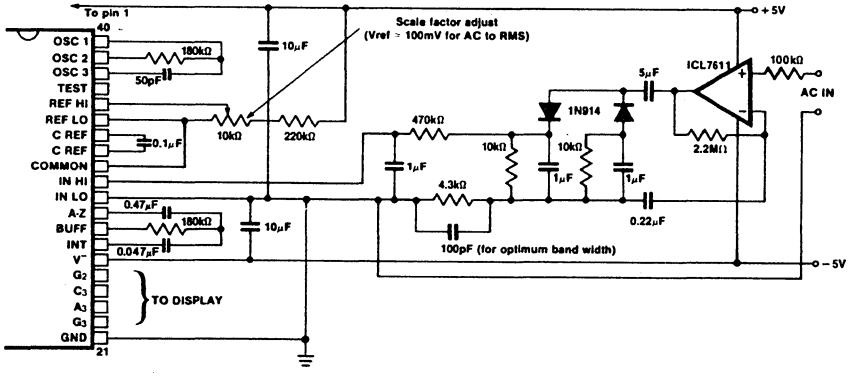
0344-17

Figure 16: Circuit for developing Underrange and Overrange signals from outputs.

The LM339 is required to ensure logic compatibility with heavy display loading.

*Values depend on clock frequency. See Figures 10, 11, and 12.

NOTE: All typical values have been characterized but are not tested.



0344-18

Figure 17: AC to DC Converter with 7137

APPLICATION NOTES

A016 "Selecting A/D converters," by David Fullagar.

A017 "The Integrating A/D Converter," by Lee Evans.

A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.

A023 "Low Cost Digital Panel Meter Designs," by David Fullagar and Michael Dufort.

A032 "Understanding the Auto-Zero and Common-Mode Behavior of the ICL7106/7/9 Family," by Peter Bradshaw.

A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106," by Larry Goff.

A047 "Games People Play with Harris' A/D Converters" edited by Peter Bradshaw.

A052 "Tips for Using Single-Chip 3½-Digit A/D Converters," by Dan Watson.

NOTE: All typical values have been characterized but are not tested.

ICL7137
INTEGRATING A/D CONVERTER EQUATIONS

Oscillator Frequency

$f_{OSC} = 0.45/RC$

$C_{OSC} > 50$ pF; $R_{OSC} > 50$ kΩ

f_{OSC} typ. = 48 kHz

Oscillator Period

$t_{OSC} = RC/0.45$

Integration Clock Frequency

$f_{CLOCK} = f_{OSC}/4$

Integration Period

$t_{INT} = 1000 \times (4/f_{OSC})$

60/50 Hz Rejection Criterion

$t_{INT}/t_{60\ Hz}$ or $t_{INT}/t_{50\ Hz}$ = Integer

Optimum Integration Current

$I_{INT} = 1.0\ \mu A$

Full Scale Analog Input Voltage

V_{INFS} typically = 200 mV or 2.0V

Integrate Resistor

$$R_{INT} = \frac{V_{INFS}}{I_{INT}}$$

Integrate Capacitor

$$C_{INT} = \frac{(t_{INT})(I_{INT})}{V_{INT}}$$

Integrator Output Voltage Swing

$$V_{INT} = \frac{(t_{INT})(I_{INT})}{C_{INT}}$$

V_{INT} Maximum Swing:

$(V^- + 0.5V) < V_{INT} < (V^+ - 0.5V)$

V_{INT} typically = 2.0V

Display Count

$$COUNT = 1000 \times \frac{V_{IN}}{V_{REF}}$$

Conversion Cycle

$t_{CYC} = t_{CLOCK} \times 4000$

$t_{CYC} = t_{OSC} \times 16{,}000$

when f_{OSC} = 48 kHz, t_{CYC} = 333 ms

Common Mode Input Voltage

$(V^- + 1.0V) < V_{IN} < (V^+ - 0.5V)$

Auto Zero Capacitor

$0.01\ \mu F < C_{AZ} < 1.0\ \mu F$

Reference Capacitor

$0.1\ \mu F < C_{REF} < 1.0\ \mu F$

V_{COM}

Biased between V^+ and V^-

$V_{COM} \cong V^+ - 2.8V$

Regulation lost when V^+ to V^- $< \cong$ 6.4V.

If V_{COM} is externally pulled down to (V^+ to V^-)/2, the V_{COM} circuit will turn off.

Power Supply: Dual ±5.0V

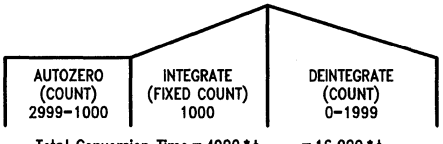
$V^+ = +5.0V$ to GND

$V^- = -5.0V$ to GND

Digital Logic and LED driver supply V^+ to GND

Display: LED

Type: Non-Multiplexed Common Anode



Total Conversion Time = 4000 * t_{CLOCK} = 16,000 * t_{OSC}

0344-19

Figure 18

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICL7139
3¾-Digit Autoranging Multimeter

GENERAL DESCRIPTION

The Harris ICL7139 is a high performance, low power, auto-ranging digital multimeter IC. Unlike other autoranging multimeter ICs, the ICL7139 always displays the result of a conversion on the correct range. There is no "range hunting" noticeable in the display. The unit will autorange between the four different ranges. A manual switch is used to select the 2 high group ranges. DC current ranges are 4 mA and 40 mA in the low current group, 400 mA and 4A in the high current group. Resistance measurements are made on 4 ranges, which are divided into two groups. The low resistance ranges are 4/40 kilohms. High resistance ranges are 0.4/4 megohms. Resolution on the lowest range is 1 ohm.

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7139CPL	0°C to +70°C	40 Pin Plastic DIP

FEATURES

- **13 Ranges:**
  - **4 DC Voltage—400 mV, 4V, 40V, 400V**
  - **1 AC Voltage—400V**
  - **4 DC Current—4 mA, 40 mA, 400 mA, 4A**
  - **4 Resistance—4 KΩ, 40 KΩ, 400 KΩ, 4 MΩ**
- **Autoranging—First Reading is Always on Correct Range**
- **On-Chip Duplex LCD Display Drive Including Three Decimal Points and 11 Annunciators**
- **No Additional Active Components Required**
- **Low Power Dissipation—Less than 20 mW—1000 Hour Typical Battery Life**
- **Average Responding Converter for Sinewave Inputs**
- **Display Hold Input**
- **Continuity Output Drives Piezoelectric Beeper**
- **Low Battery Annunciator with On-Chip Detection**
- **Guaranteed Zero Reading for 0 Volts Input on All Ranges**

2

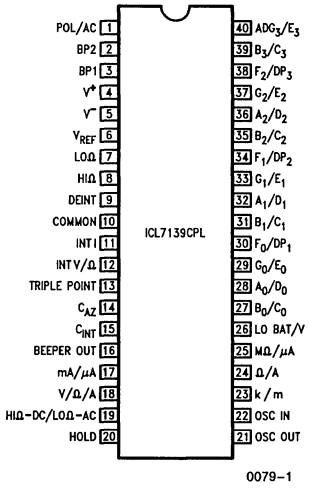


Figure 1: Pin Configuration

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Reference Input Voltage (V_{REF} to COM) 3V
Analog Input Current ..... 100 μA
(IN + Current or IN + Voltage)
Clock Input Swing ..... V^+ to $V^+ - 3$
Power Dissipation (Plastic Package) ..... 800 mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +130°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

$V^+ = +9.0V$, $T_A = +25°C$, V_{REF} adjusted for −3.700 reading on DC volts, test circuit as shown in Figure 3. Crystal = 120 kHz.

Parameter	Test Conditions	Min	Typ	Max	Units
Zero Input Reading	V_{IN} or I_{IN} or R_{IN} = 0.00	−00.0		+00.0	V, I, Ω
Linearity (Best Straight Line) (Note 6)	(Note 1)	−1		+1	Counts
Accuracy DC V, 400 Volt Range Only	(Note 1)			±1	% of RDG ± 1
Accuracy DC V, 400 Volt Range Excluded	(Note 1)			±0.30	% of RDG ± 1
Accuracy Ohms, 4K and 400K Range	(Note 1)			±0.75	% of RDG ± 8
Accuracy Ohms, 40K and 4 Meg Range	(Note 1)			±1	% of RDG ± 9
Accuracy DC I, Unadjusted for FS	(Note 1)			±0.75	% of RDG ± 1
Accuracy DC I, Adjusted for FS	(Note 1)		±0.2		% of RDG ± 1
Accuracy AC V (Note 5)	@60 Hz		±2		% of RDG
Open Circuit Voltage for Ohms Measurements	$R_{UNKNOWN}$ = Infinity		V_{REF}		V
Noise (Note 2, 95% of Time)	V_{IN} = 0, DC Volts		0.1		LSB
Noise (Note 2, 95% of Time)	V_{IN} = 0, AC Volts		4		LSB
Supply Current	V_{IN} = 0, DC Voltage Range		1.5	2.4	mA
Analog Common (with Respect to V^+)	I_{COMMON} < 10 μA	2.7	2.9	3.1	V
Temperature Coefficient of Analog Common	I_{COMMON} < 10 μA, Temp = 0–70°C		−100		ppm/°C
Output Impedance of Analog Common	I_{COMMON} < 100 μA		1	10	Ω
Backplane/Segment Drive Voltage	Average DC < 50 mV	2.8	3.0	3.2	V
Backplane/Segment Display Frequency			75		Hz
Switch Input Current (Note 3)	V_{IN} = V^+ to V^-	−50		+50	μA
Switch Input Levels (High Trip Point)		$V^+ - 0.5$		V^+	V
Switch Input Levels (Mid Trip Point)		$V^- + 3$		$V^+ - 2.5$	V
Switch Input Levels (Low Trip Point)		V^-		$V^- + 0.5$	V
Beeper Output Drive (Rise or Fall Time)	C_{LOAD} = 10 nF		25	100	μs
Beeper Output Frequency			2		kHz
Continuity Detect	Range = Low Ohms, V_{REF} = 1.00V		1.5		kΩ
Power Supply Functional Operation	V^+ to V^-	7	9	11	V
Low Battery Detect (Note 4)	V^+ to V^-	6.5	7	7.5	V

NOTE 1: Accuracy is defined as the worst case deviation from ideal input value including: offset, linearity, and rollover error.
2: Noise is defined as the width of the uncertainty window (where the display will flicker) between two adjacent codes.
3: Applies to pins 17–20.
4: Analog Common falls out of regulation when the Low Battery Detect is asserted, however the ICL7139 will continue to operate correctly with a supply voltage above 7 volts and below 11 volts.
5: For 50 Hz use a 100 kHz crystal.
6: Guaranteed by design, not tested.

RDG = Reading

NOTE: All typical values have been characterized but are not tested.

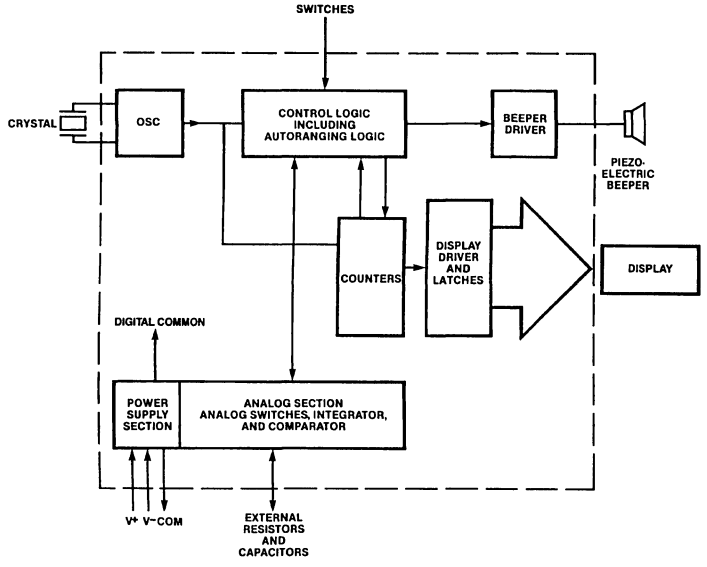


Figure 2: Functional Diagram

3¾-Digit Autoranging DMM Using Harris' ICL7139

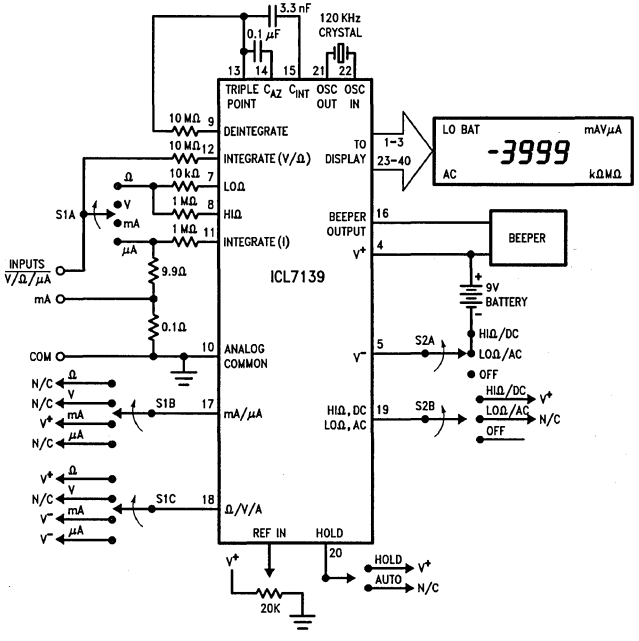


Figure 3: ICL7139 Test Circuit

NOTE: All typical values have been characterized but are not tested.

Table 1: Pin Numbers and Function

I/O	Pin Number	Pin Function
O	1	Segment Driver POL/AC
O	2	Backplane 2
O	3	Backplane 1
I	4	V^+
I	5	V^-
I	6	Reference Input
O	7	Lo Ohms
O	8	Hi Ohms
I/O	9	Deintegrate
I/O	10	Analog Common
I	11	Int I
I	12	Int V/Ohms
I	13	Triple Point
I	14	Auto Zero Capacitor (C_{AZ})
I	15	Integrate Capacitor (C_{INT})
O	16	Beeper Output
I	17	mA/μA
I	18	Ohms/V/A
I	19	Hi Ohms DC/Lo Ohms AC
I	20	Hold
O	21	Oscillator Out
I	22	Oscillator In
O	23	Segement DRIVER k/m
O	24	Segment Driver Ohms/A
O	25	Segment Driver M Ohms/μA
O	26	Segment Driver Lo Bat/V
O	27	Segment Driver B_0/C_0
O	28	Segment Driver A_0/D_0
O	29	Segment Driver G_0/E_0
O	30	Segment Driver F_0/DP_1
O	31	Segment Driver B_1/C_1
O	32	Segment Driver A_1/D_1
O	33	Segment Driver G_1/E_1
O	34	Segment Driver F_1/DP_1
O	35	Segment Driver B_2/C_2
O	36	Segment Driver A_2/D_2
O	37	Segment Driver G_2/E_2
O	38	Segment Driver F_2/DP_3
O	39	Segment Driver B_3/C_3
O	40	Segment Driver ADG_3/E_3

NOTE: For segment drivers, segments are listed as (segment for backplane 1)/(segment for backplane 2). Example: pin 27; segment B_0 is on backplane 1, segment C_0 is on backplane 2.

DETAILED DESCRIPTION

General

Figure 2 is a simplified block diagram of the ICL7139. The digital section includes all control logic, counters, and display drivers. The digital section is powered by V^+ and Digital Common, which is about 3V below V^+. The oscillator is also in the digital section. Normally 120 kHz for rejection of 60 Hz AC interference and 100 kHz for rejection of 50 Hz AC, the oscillator output is divided by two to generate the internal master clock. The analog section contains the integrator, comparator, reference section, analog buffers, and several analog switches which are controlled by the digital logic. The analog section is powered from V^+ and V^-.

DC VOLTAGE MEASUREMENT

Autozero

Only those portions of the analog section which are used during DC voltage measurements are shown in Figure 5. As shown in the timing diagram (Figure 6), each measurement starts with an autozero (AZ) phase. During this phase, the integrator and comparator are configured as unity gain buffers and their non-inverting inputs are connected to Common. The output of the integrator, which is equal to its offset, is stored on C_{AZ}—the autozero capacitor. Similarly, the offset of the comparator in stored in C_{INT}. The autozero cycle equals 1000 clock cycles which is one 60 Hz line cycle with a 120 kHz oscillator or one 50 Hz line cycle with a 100 kHz crystal.

Range 1 Integrate

The ICL7139 performs a full autorange search for each reading, beginning with range 1. During the range 1 integrate period, internal switches connect the INT V/Ohm terminal to the Triple Point (Pin 13). The input signal is integrated for 10 clock cycles, which are gated out over a period of 1000 clock cycles to ensure good normal mode rejection of AC line interference.

Range 1 Deintegrate

At the beginning of the deintegrate cycle, the polarity of the voltage on the integrator capacitor (C_{INT}) is checked, and either the $DEINT^+$ or $DEINT^-$ is asserted. The integrator capacitor C_{INT} is then discharged with a current equal to V_{REF}/R_{DEINT}. The comparator monitors the voltage on C_{INT}. When the voltage on C_{INT} is reduced to zero (actually to the V_{OS} of the comparator), the comparator output switches, and the current count is latched. If the C_{INT} voltage zero-crossing does not occur before 4000 counts have elapsed, the overload flag is set. "OL" (overload) is then displayed on the LCD. If the latched result is between 360 and 3999, the count is transferred to the output latches and is displayed. When the count is less than 360, an underrange has occurred, and the ICL7139 then switches to range 2—the 40V scale.

Range 2

The range 2 measurement begins with an autozero cycle similar to the one that preceded range 1 integration. Range 2 cycle length however, is one AC line cycle, minus 360 clock cycles. When performing the range 2 cycle, the signal is integrated for 100 clock cycles, distributed throughout

NOTE: All typical values have been characterized but are not tested.

one line cycle. This is done to maintain good normal mode rejection. Range 2 sensitivity is ten times greater than range 1 (100 vs. 10 clock cycle integration) and the full scale voltage of range 2 is 40V. The range 2 deintegrate cycle is identical to the range 1 deintegrate cycle, with the result being displayed only for readings greater than 360 counts. If the reading is below 360 counts, the ICL7139 again asserts the internal underrange signal and proceeds to range 3.

Range 3

The range 3 or 4V full scale measurement is identical to the range 2 measurement, except that the input signal is integrated during the full 1000 clock cycles (one line frequency cycle). The result is displayed if the reading is greater than 360 counts. Underrange is asserted, and a range 4 measurement is performed if the result is below 360 counts.

Range 4

This measurement is similar to the range 1, 2 and 3 measurements, except that the integration period is 10,000 clock cycles (10 line cycles) long. The result of this measurement is transferred to the output latches and displayed even if the reading is less than 360.

Autozero

After finding the first range for which the reading is above 360 counts, the display is updated and an autozero cycle is entered. The length of the autozero cycle is variable which results in a fixed measurement period of 24,000 clock cycles (24 line cycles).

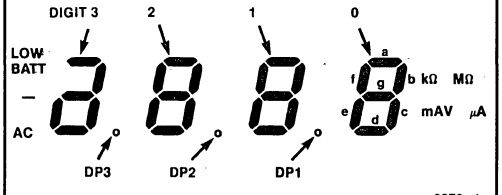


Figure 4: Display Segment Nomenclature

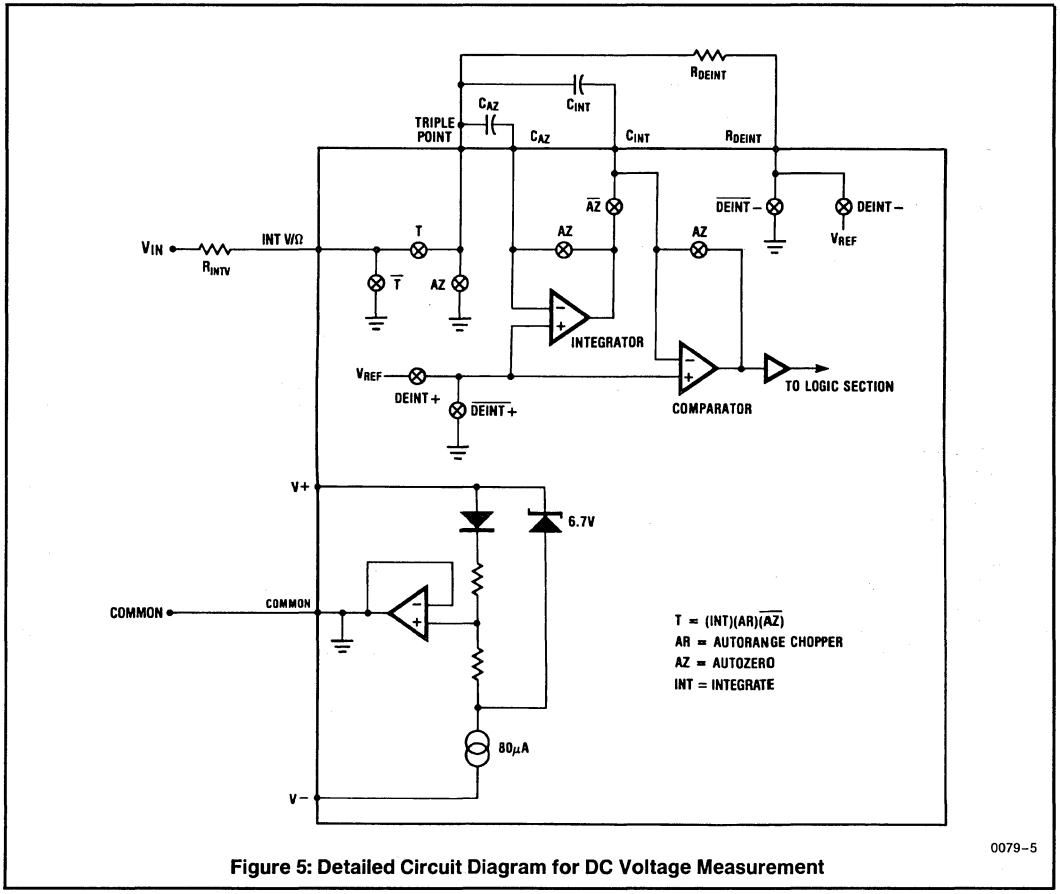


Figure 5: Detailed Circuit Diagram for DC Voltage Measurement

NOTE: All typical values have been characterized but are not tested.

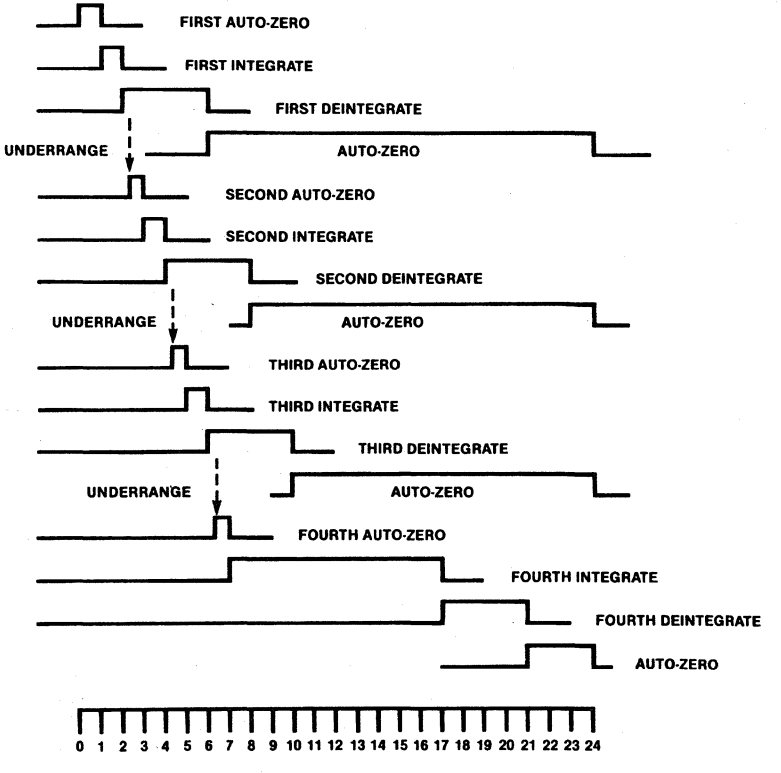


Figure 6: Timing Diagram for DC Voltage Measurement

DC CURRENT

Figure 7 shows a simplified block diagram of the analog section of the ICL7139 during DC current measurement. The DC current measurements are very similar to DC voltage measurements except: 1) The input voltage is developed by passing the input current through a 0.1 ohm (HI current ranges), or 9.9 ohm (LOW current ranges) current sensing resistor; 2) Only those ranges with 1000 and 10,000 clock cycles of integration are used; 3) The $R_{INT\ I}$ resistor is 1 megohm, rather than the 10 megohm value used for the $R_{INT\ V}$ resistor.

By using the lower value integration resistor, and only the 2 most sensitive ranges, the voltage drop across the current sensing resistor is 40 mV maximum on the 4 mA and 400 mA ranges; 400 mV maximum on the 40 mA and 4A scales. With some increase in noise, these "burden" voltages can be reduced by lowering the value of both the current sense resistors and the $R_{INT\ I}$ resistor proportionally. The DC current measurement timing diagram is similar to the DC voltage measurement timing diagram, except in the DC current timing diagram, the first and second integrate and deintegrate phases are skipped.

NOTE: All typical values have been characterized but are not tested.

AC VOLTAGE MEASUREMENT

As shown in Figure 8, the AC input voltage is applied directly to the ICL7139 input resistor. No separate AC to DC conversion circuitry is needed. The AC measurement cycle is begun by disconnecting the integrator capacitor and using the integrator as an autozeroed comparator to detect the positive-going zero crossing. Once synchronized to the AC input, the autozero loop is closed and a normal integrate/deintegrate cycle begins. The ICL7139 resynchronizes itself to the AC input prior to every reading. Because diode D4 is in series with the integrator capacitor, only positive current from the integrator flows into the integrator capacitor, C_{INT}. Since the voltage on C_{INT} is proportional to the half-wave rectified average AC input voltage, a conversion factor must be applied to convert the reading to RMS. This conversion factor is $\pi/2\sqrt{2} = 1.1107$, and the system clock is manipulated to perform the RMS conversion. As a result the deintegrate and autozero cycle times are reduced by 10%.

Ratiometric Ohms Measurement

The ratiometric ohms measurement is performed by first integrating the voltage across an unknown resistor, Rx, then effectively deintegrating the voltage across a known resistor (R_{KNOWN1} or R_{KNOWN2} of Figure 9). The shunting effect of R_{INTV} does not affect the reading because it cancels exactly between integration and deintegration. Like the current measurements, the ohm measurements are split into two sets of ranges. LO ohms measurements use a 10 kilohm reference resistor, and the full scale ranges are 4 and 40 kilohms. HI ohms measurements use a 1 megohm reference resistor, and the full scale ranges are 0.4 and 4 megohms. The measurement phases and timing are the same as the measurement phases and timing for DC current except: 1) During the integrate phases the input voltage is the voltage across the unknown resistor Rx, and; 2) During the deintegrate phases, the input voltage is the voltage across the reference resistor R_{KNOWN1} or R_{KNOWN2}.

Continuity Indication

When the ICL7139 is in the LO ohms measurement mode, the continuity circuit of Figure 10 will be active. When the voltage across Rx is less than approximately 100 mV, the beeper output will be on. When R_{KNOWN} is 10 kilohms, the beeper output will be on when Rx is less than 1 kilohm.

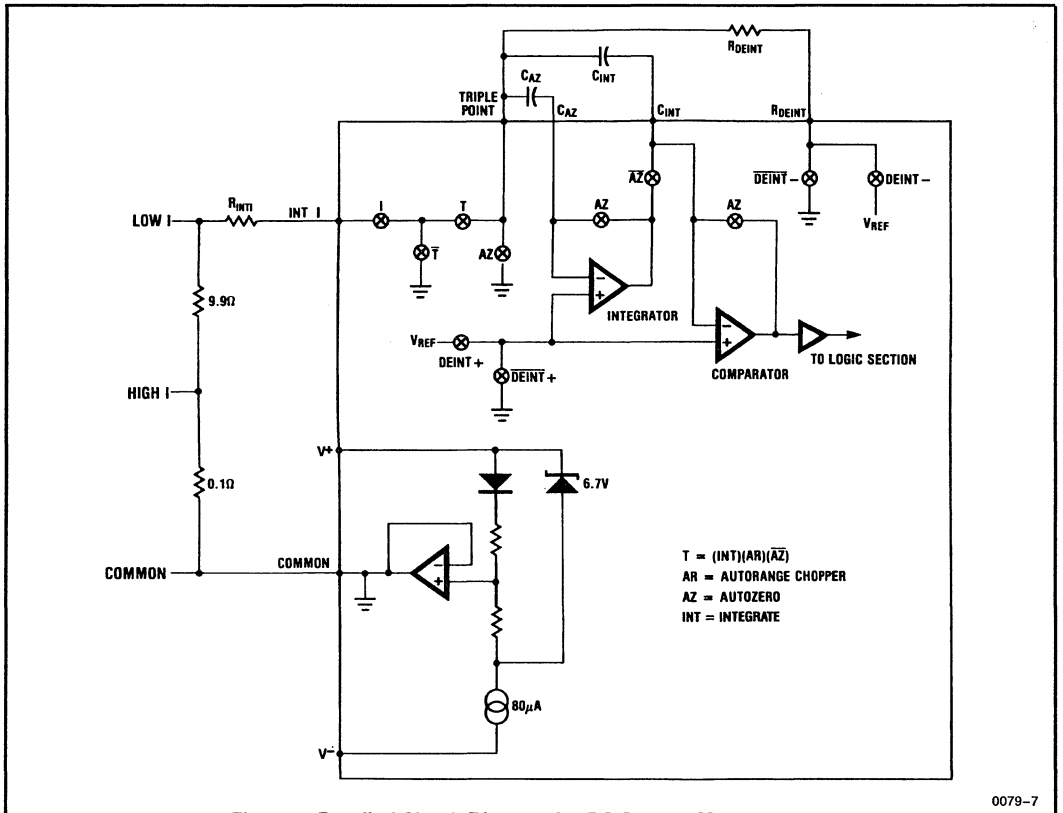


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Figure 7: Detailed Circuit Diagram for DC Current Measurement

NOTE: All typical values have been characterized but are not tested.

Common Voltage

The analog and digital common voltages of the ICL7139 are generated by an on-chip resistor/zener/diode combination, shown in Figure 11. The resistor values are chosen so the coefficient of the diode voltage cancels the positive temperature coefficient of the zener voltage. This voltage is then buffered to provide the analog common and the digital common voltages. The nominal voltage between V^+ and analog common is 3V. The analog common buffer can sink about 20 mA, or source 0.01 mA, with an output impedance of 10 ohms. A pullup resistor to V^+ may be used if more sourcing capability is desired. Analog common may be used to generate the reference voltage, if desired.

Oscillator

The ICL7139 uses a parallel resonant-type crystal in a Pierce oscillator configuration, as shown in Figure 12, and requires no other external components. The crystal eliminates the need to trim the oscillator frequency. An external signal may be capacitively coupled in OSC IN, with a signal level between 0.5 and 3V pk-pk. Because the OSC OUT pin is not designed to drive large external loads, loading on this pin should not exceed a single CMOS input. The oscillator frequency is internally divided by two to generate the ICL7139 clock. The frequency should be 120 kHz to reject 60 Hz AC signals, and 100 kHz to reject 50 Hz signals.

Display Drivers

Figure 13 shows typical LCD Drive waveforms, RMS ON, and RMS OFF voltage calculations. Duplex multiplexing is used to minimize the number of connections between the ICL7139 and the LCD. The LCD has two separate backplanes. Each drive line can drive two individual segments, one referenced to each backplane. The ICL7139 drives 3¾ 7-segment digits, 3 decimal points, and 11 annunciators. Annunciators are used to indicate polarity, low battery condition, and the range in use. Peak drive voltage across the display is approximately 3V. An LCD with approximately 1.4V RMS threshold voltage should be used. The third voltage level needed for duplex drive waveforms is generated through an on-chip resistor string. The DC component of the drive waveforms is guaranteed to be less than 50 mV.

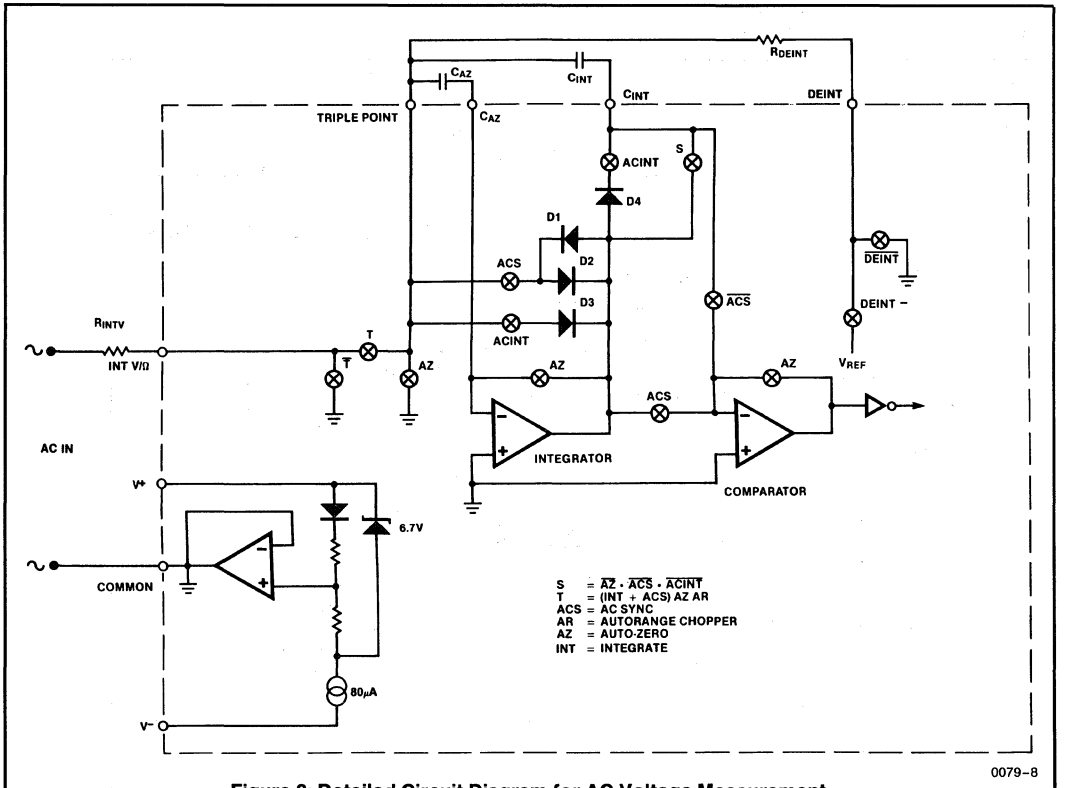

Figure 8: Detailed Circuit Diagram for AC Voltage Measurement

NOTE: All typical values have been characterized but are not tested.

Ternary Input

The Ohms/Volts/Amps logic input is a ternary, or 3-level input. This input is internally tied to the common voltage through a high-value resistor, and will go to the middle, or "Volts" state, when not externally connected. When connected to V−, approximately 5 μA of current flows out of the input. In this case, the logic level is the "Amps", or low state. When connected to V+, about 5 μA of current flows into the input. Here, the logic level is the "Ohms", or high state. For other pins, see Table 2.

Table 2: Ternary Inputs Connections

Pin Number	V+	OPEN or COM	V−
17	mA	μA	Test
18	Ohms	Volts	Amps
19	HiΩ/DC	LoΩ/AC	Test
20	Hold	Auto	Test

COMPONENT SELECTION

For optimum performance while maintaining the low-cost advantages of the ICL7139, care must be taken when selecting external components. This section reviews specifications and performance effects of various external components.

Integrator Capacitor, C_{INT}

As with all dual-slope integrating convertors, the integration capacitor must have low dielectric absorption to reduce linearity errors. Polypropylene capacitors add undetectable errors at a reasonable cost, while polystyrene and polycarbonate may be used in less critical applications. The ICL7139 is designed to use a 3.3 nF (0.0033 μF) C_{INT} with an oscillator frequency of 120 kHz and an R_{INTV} of 10 megohms. With a 100 kHz oscillator frequency (for 50 Hz line frequency rejection), C_{INT} and R_{INTV} affects the voltage swing of the integrator. Voltage swing should be as high as possible without saturating the integrator. Saturation occurs when the integrator output is within 1V of either V+ or V−. Integrator voltage swing should be about ±2V when using standard component values. For different R_{INTV} and oscillator frequencies the value of C_{INT} can be calculated from:

$$C_{INT} = \frac{(\text{Integrate Time}) \times (\text{Integrate Current})}{(\text{Desired Integrator Swing})}$$

$$= \frac{(10{,}000 \times 2 \times \text{Oscillator Period}) \times 0.4\text{V}/R_{INTV}}{(2\text{V})}$$

Integrator Resistors

The normal values of the $R_{INT\ V}$ and $R_{INT\ I}$ resistors are 10 megohms and 1 megohm respectively. Though their absolute values are not critical, unless the value of the current sensing resistors are trimmed, their ratio should be 10:1, within 0.05%. Some carbon composition resistors have a large voltage coefficient which will cause linearity errors on the 400V scale. Also, some carbon composition resistors are very noisy. The class "A" output of the integrator begins to have nonlinearities if required to sink more than 70 μA (the sourcing limit is much higher). Because $R_{INT\ V}$ drives a virtual ground point, the input impedance of the meter is equal to $R_{INT\ V}$.

Deintegration Resistor, R_{DEINT}

Unlike most dual-slope A/D converters, the ICL7139 uses different resistors for integration and deintegration. R_{DEINT} should normally be the same value as R_{INTV}, and have the same temperature coefficient. Slight errors in matching may be corrected by trimming the reference voltage.

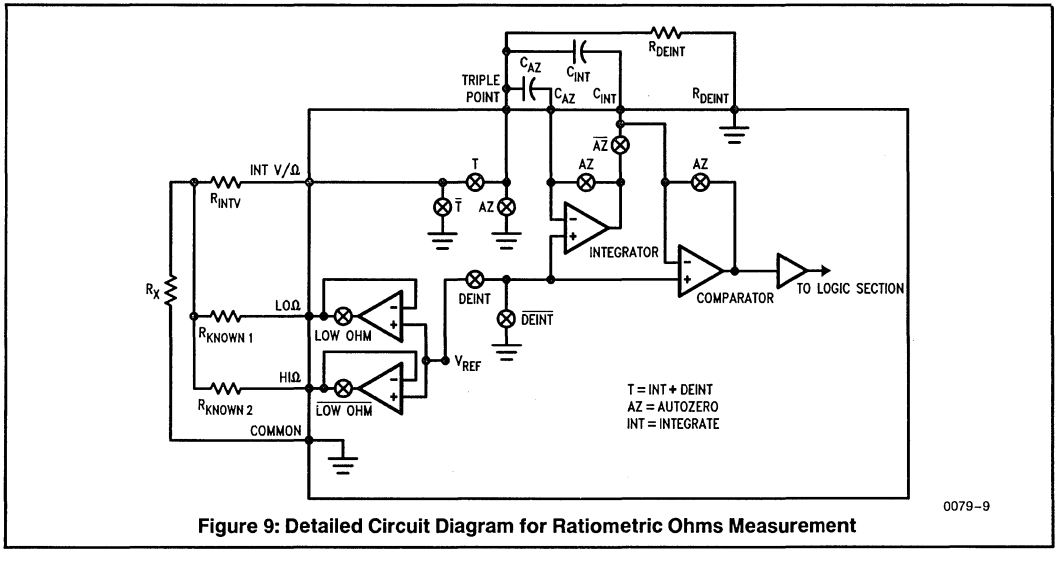

Figure 9: Detailed Circuit Diagram for Ratiometric Ohms Measurement

NOTE: All typical values have been characterized but are not tested.

Autozero Capacitor, C_{AZ}

The C_{AZ} is charged to the integrator's offset voltage during the autozero phases, and subtracts that voltage from the input signal during the integrate phases. The integrator thus appears to have zero offset voltage. Minimum C_{AZ} value is determined by: 1) Circuit leakages; 2) C_{AZ} self-discharge; 3) Charge injection from the internal autozero switches. To avoid errors, the C_{AZ} voltage change should be less than $1/_{10}$ of a count during the 10,000 count clock cycle integration period for the 400 mV range. These requirements set a lower limit of 0.047 μF for C_{AZ} but 0.1 μF is the preferred value. The upper limit on the value of C_{AZ} is set by the time constant of the autozero loop, and the 1 line cycle time period allotted to autozero. C_{AZ} may be several 10s of microfarads before approaching this limit.

The ideal C_{AZ} is a low leakage polypropylene or Teflon capacitor. Other film capacitors such as polyester, polystyrene, and polycarbonate introduce negligible errors. If a few seconds of settling time upon power-up is acceptable, the C_{AZ} may be a ceramic capacitor, provided it does not have excessive leakage.

Ohms Measurement Resistors

Because the ICL7139 uses a ratiometric ohms measurement technique, the accuracy of ohms reading is primarily determined by the absolute accuracy of the R_{KNOWN1} and R_{KNOWN2}. These should normally be 10 kilohms and 1 megohm, with an absolute accuracy of at least 0.5%.

Current Sensing Resistors

The 0.1 ohm and 9.9 ohm current sensing resistors convert the measured current to a voltage, which is then measured using $R_{INT\ I}$. The two resistors must be closely matched, and the ratio between $R_{INT\ I}$ and these two resistors must be accurate—normally 0.5%. The 0.1 ohm resistor must be capable of handling the full scale current of 4 amps, which requires it to dissipate 1.6 watts.

Continuity Beeper

The Continuity Beeper output is designed to drive a piezoelectric transducer at 2 kHz (using a 120 kHz crystal), with a voltage output swing of V^+ to V^-. The beeper output off state is at the V^+ rail. When crystals with different frequencies are used, the frequency needed to drive the transducer can be calculated by dividing the crystal frequency by 60.

Display

The ICL7139 uses a custom, duplexed drive display with range, polarity, and low battery annunciators. With a 3 volt peak display voltage, the RMS ON voltage will be 2.37V minimum; RMS OFF voltage will be 1.06V maximum. Because the display voltage is not adjustable, the display should have a 10% ON threshold of about 1.4V. Most display manufacturers supply a graph that shows contrast versus RMS drive voltage. This graph can be used to determine what the contrast ratio will be when driven by the ICL7139. Most display thresholds decrease with increasing temperature. The threshold at the maximum operating temperature should be checked to ensure that the "off" segments will not be turned "on" at high temperatures.

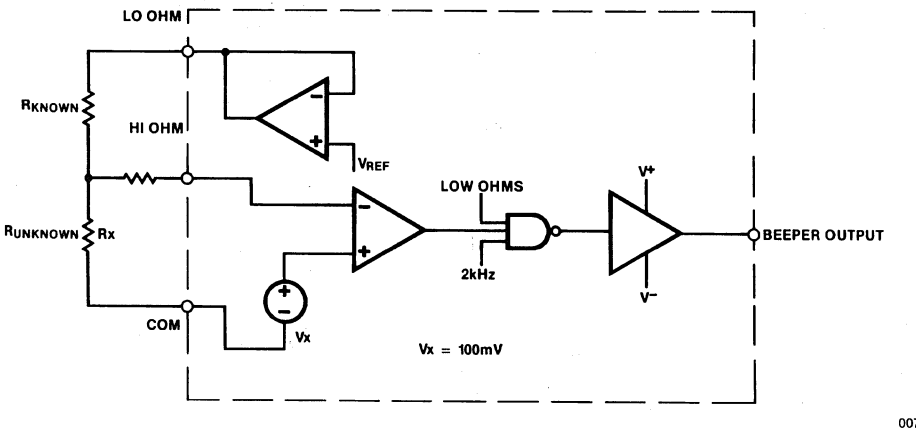

Figure 10: Continuity Beeper Drive Circuit

NOTE 1: The ICL7139 contains a comparator that is enabled on the lowest ohms range. It trips at approximately 1.5 kΩ and enables the beeper driver to oscillate (between V^- and V^+) at 2 kHz. The beeper driver is capable of driving a piezo-electric transducer. The beeper output response is independent of the state of the conversion; therefore appears instantaneous to the user. Some applications may require a 150 pF capacitor between pin 4 and pin 8 to insure a sharp on/off continuity detection.

NOTE: All typical values have been characterized but are not tested.

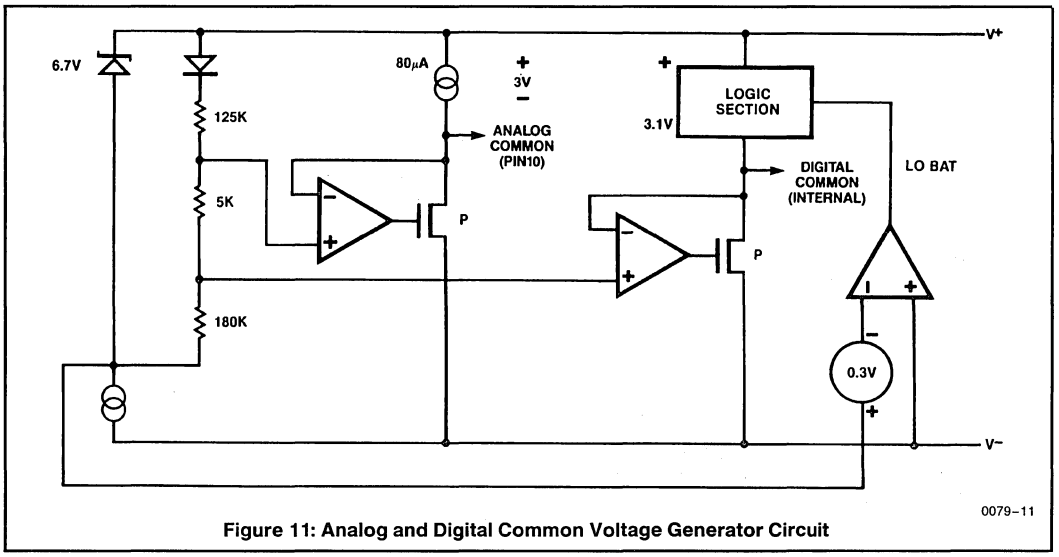

Figure 11: Analog and Digital Common Voltage Generator Circuit

Crystal

The ICL7139 is designed to use a parallel resonant 120 kHz or 100 kHz crystal with no additional external components. The R_S parameter should be less than 25 kilohms to ensure oscillation. Initial frequency tolerance of the crystal can be a relatively loose 0.05%.

Switches

Because the logic input draws only about 5 μA, switches driving these inputs should be rated for low current, or "dry" operations. The switches on the external inputs must be able to reliably switch low currents, and be able to handle voltages in excess of 400V AC.

Reference Voltage Source

A voltage divider connected to V^+ and Common is the simplest source of reference voltage. While minimizing external component count, this approach will provide the same voltage tempco as the ICL7139 Common—about 100 PPM/°C. To improve the tempco, an ICL8069 bandgap reference may be used (see Figure 14). The reference voltage source output impedance must be $\leq R_{DEINT}/4000$.

Applications, Examples, and Hints

A complete autoranging 3¾ digit multimeter is shown in Figure 15. The following sections discuss the functions of specific components and various options.

Meter Protection

The ICL7139 and its external circuitry should be protected against accidental application of 110/220V AC line voltages on the ohms and current ranges. Without the necessary precautions, both the 7139 and its external components could be damaged under such fault conditions. For the current ranges, fast-blow fuses should be used between S5A in Figure 15 and the 0.1 ohm and 9.9 ohm shunt resistors. For the ohms ranges, no additional protection circuitry is required. However, the 10 kilohm resistor connected to pin 7 must be able to dissipate 1.2W or 4.8W for short periods of time during accidental application of 110V or 220V AC line voltages respectively.

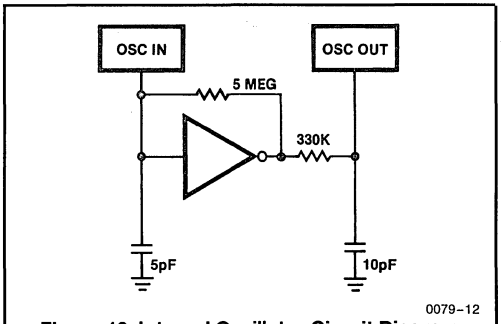

Figure 12: Internal Oscillator Circuit Diagram

NOTE: All typical values have been characterized but are not tested.

Printed Circuit Board Layout Considerations

Particular attention must be paid to rollover performance, leakages, and guarding when designing the PCB for a ICL7139-based multimeter.

Rollover Performance, Leakages, and Guarding

Because the ICL7139 system measures very low currents, it is essential that the PCB have low leakage. Boards should be properly cleaned after soldering. Areas of particular importance are: 1) The INT V/Ω and INT I Pins; 2) The Triple Point; 3) The R_{DEINT} and the C_{AZ} pins.

The conversion scheme used by the ICL7139 changes the common mode voltage on the integrator and the capacitors C_{AZ} and C_{INT} during a positive deintegrate cycle. Stray capacitance to ground is charged when this occurs, removing some of the charge on C_{INT} and causing rollover error. Rollover error increases about 1 count for each picofarad of capacitance between C_{AZ} or the Triple Point and ground, and is seen as a zero offset for positive voltages. Rollover error is not seen as gain error.

The rollover error causes the width of the +0 count to be larger than normal. The ICL7139 will thus read zero until several hundred microvolts are applied in the positive direction. The ICL7139 will read −1 when approximately −100 μV is applied.

The rollover error can be minimized by guarding the Triple Point and C_{AZ} nodes with a trace connected to the C_{INT} pin, which is driven by the output of the integrator. Guarding these nodes with the output of the integrator reduces the stray capacitance to ground, which minimizes the charge error on C_{INT} and C_{AZ}. If possible, the guarding should be used on both sides of the PC board.

Stray Pickup

While the ICL7139 has excellent rejection of line frequency noise and pickup in the DC ranges, any stray coupling will affect the AC reading. Generally, the analog circuitry should be as close as possible to the ICL7139. The analog circuitry should be removed or shielded from any 120V AC power inputs, and any AC sources such as LCD drive waveforms. Keeping the analog circuit section close to the ICL7139 will also help keep the area free of any loops, thus reducing magnetically coupled interference coming from power transformers, or other sources.

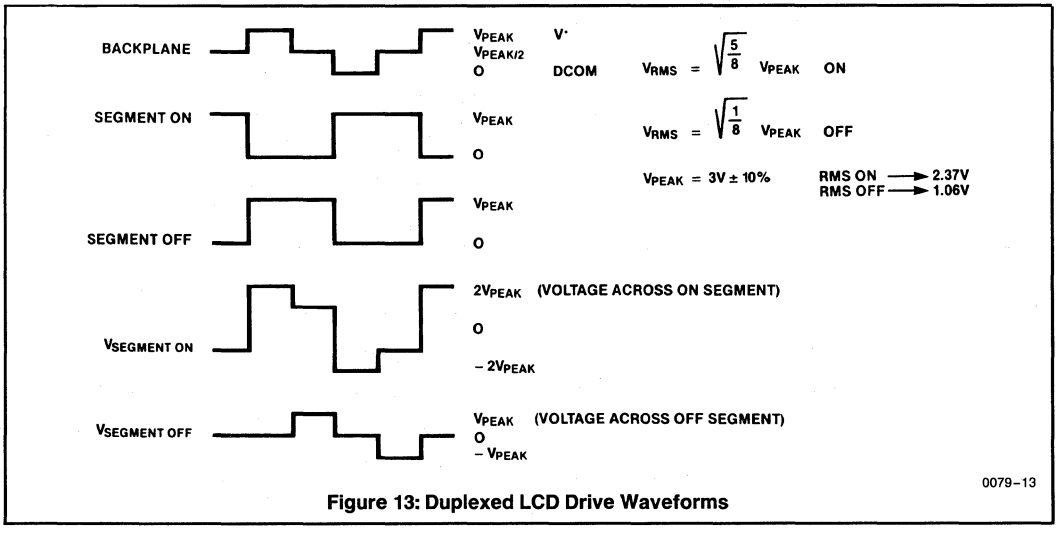

Figure 13: Duplexed LCD Drive Waveforms

NOTE: All typical values have been characterized but are not tested.

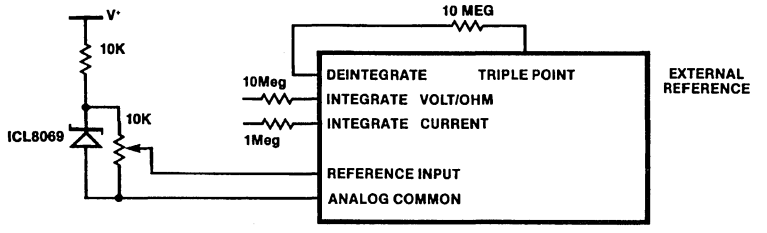

Figure 14: External Voltage Reference Connection to ICL7139

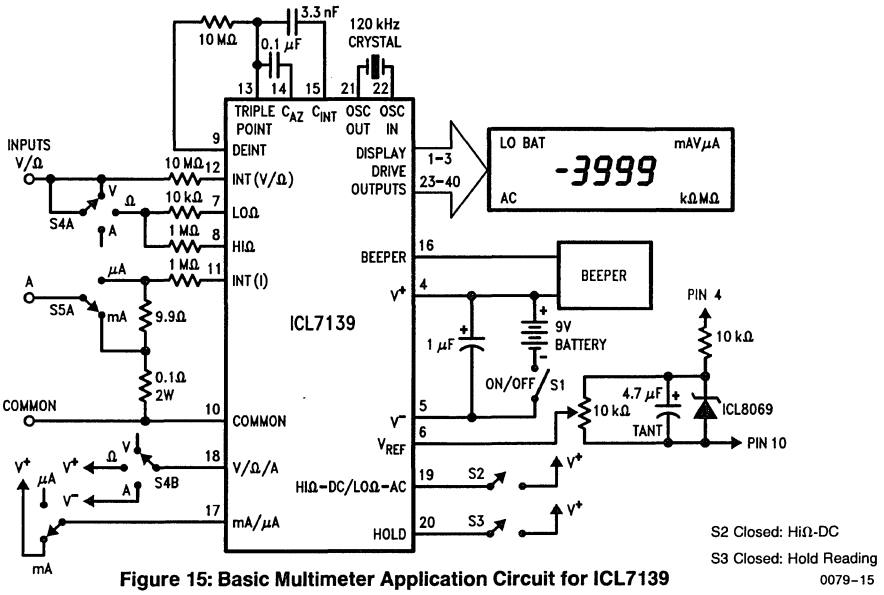

Figure 15: Basic Multimeter Application Circuit for ICL7139

NOTE 1: Crystal is a Statek or SaRonix CX-IV type.
2: Multimeter protection components have not been shown.
3: Display is from LXD, part number 38D8R02H (or equivalent).
4: Beeper is from muRata, part number PKM24-4A0 (or equivalent).

NOTE: All typical values have been characterized but are not tested.

ICL7139

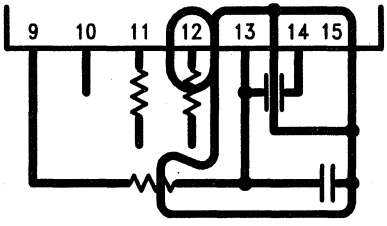

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Figure 16: PC Board Layout

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICL7149
Low Cost 3¾-Digit Autoranging Multimeter

GENERAL DESCRIPTION

The Harris ICL7149 is a high performance, low power, autoranging digital multimeter IC. Unlike other autoranging multimeter ICs, the ICL7149 always displays the result of a conversion on the correct range. There is no "range hunting" noticeable in the display. The unit will autorange between the four different ranges in the DC voltage, DC current and resistance measurement modes. A manual switch is used to select the 2 high group ranges. DC current ranges are 4 mA and 40 mA in the low current group, 400 mA and 4A in the high current group. Resistance measurements are made on 4 ranges, which are divided into two groups. The low resistance ranges are 4/40 kilohms. High resistance ranges are 0.4/4 megohms. Resolution on the lowest range is 1 ohm.

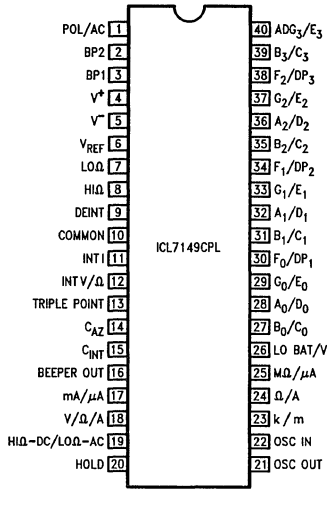
ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL7149CPL	0°C to +70°C	40 Pin Plastic DIP
ICL7149CM44	0°C to +70°C	44 Pin Surface Mount

FEATURES

- **18 Ranges:**
  - **4 DC Voltage—400 mV, 4V, 40V, 400V**
  - **2 AC Voltage—with Optional AC Circuit**
  - **4 DC Current—4 mA, 40 mA, 400 mA, 4A**
  - **4 AC Current with Optional AC Circuit**
  - **4 Resistance—4 kΩ, 40 kΩ, 400 kΩ, 4 MΩ**
- **Autoranging—First Reading is Always on Correct Range**
- **On-Chip Duplex LCD Display Drive Including Three Decimal Points and 11 Annunciators**
- **Low Power Dissipation—Less than 20 mW—1000 Hour Typical Battery Life**
- **Display Hold Input**
- **Continuity Output Drives Piezoelectric Beeper**
- **Low Battery Annunciator with On-Chip Detection**
- **Guaranteed Zero Reading for 0 Volts Input on All Ranges**

2



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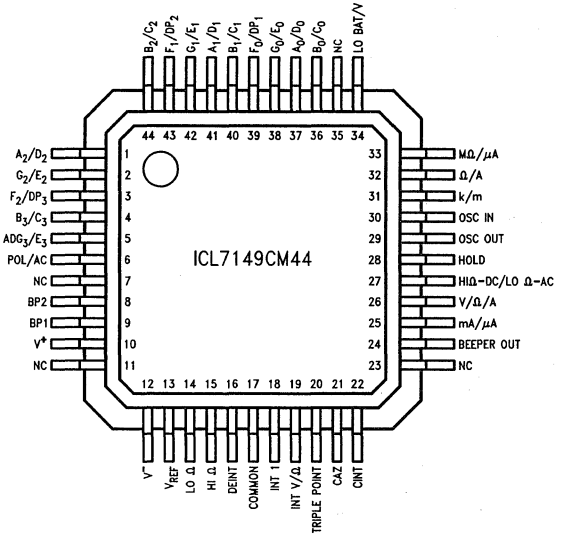

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Figure 1: Pin Configurations

301672-003

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ to V^-) 15V
Reference Input Voltage (V_{REF} to COM) 3V
Analog Input Current ..... 100 μA
(IN+ Current or IN+ Voltage)
Clock Input Swing ..... V^+ to $V^+ - 3$
Power Dissipation (Plastic Package) ..... 800 mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +130°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

$V^+ = +9.0V$, $T_A = +25°C$, V_{REF} adjusted for −3.700 reading on DC volts, test circuit as shown in Figure 3. Crystal Frequency = 120 kHz.

Parameter	Test Conditions	Min	Typ	Max	Units
Zero Input Reading	V_{IN} or I_{IN} or R_{IN} = 0.00	−00.0		+00.0	V, I, Ω
Linearity (Best Straight Line) (Note 5)	(Note 1)	−1		+1	Counts
Accuracy DC V, 400 Volt Range Only	(Note 1)			±1	% of RDG ± 1
Accuracy DC V, 400 Volt Range Excluded	(Note 1)			±0.30	% of RDG ± 1
Accuracy Ohms, 4K and 400K Range	(Note 1)			±0.75	% of RDG ± 8
Accuracy Ohms, 40K and 4Meg Range	(Note 1)			±1	% of RDG ± 9
Accuracy DC I, Unadjusted for FS	(Note 1)			±0.75	% of RDG ± 1
Accuracy DC I, Adjusted for FS	(Note 1)		±0.2		% of RDG ± 1
Open Circuit Voltage for Ohms Measurements	$R_{UNKNOWN}$ = Infinity		V_{REF}		V
Noise (Note 2, 95% of Time)	V_{IN} = 0, DC Volts		0.1		LSB
Supply Current	V_{IN} = 0, DC Voltage Range		1.5	2.4	mA
Analog Common (with Respect to V^+)	I_{COMMON} < 10 μA	2.7	2.9	3.1	V
Temperature Coefficient of Analog Common	I_{COMMON} < 10 μA, Temp = 0°C–70°C		−100		ppm/°C
Output Impedance of Analog Common	I_{COMMON} < 100 μA		1	10	Ω
Backplane/Segment Drive Voltage	Average DC < 50 mV	2.8	3.0	3.2	V
Backplane/Segment Display Frequency			75		Hz
Switch Input Current (Note 3)	V_{IN} = V^+ to V^-	−50		+50	μA
Switch Input Levels (High Trip Point)		$V^+ - 0.5$		V^+	V
Switch Input Levels (Mid Trip Point)		$V^- + 3$		$V^+ - 2.5$	V
Switch Input Levels (Low Trip Point)		V^-		$V^- + 0.5$	V
Beeper Output Drive (Rise or Fall Time)	C_{LOAD} = 10 nF		25	100	μs
Beeper Output Frequency			2		kHz
Continuity Detect	Range = Low Ohms, V_{REF} = 1.00V		1.5		kΩ
Power Supply Functional Operation	V^+ to V^-	7	9	11	V
Low Battery Detect (Note 4)	V^+ to V^-	6.5	7	7.5	V

NOTE 1: Accuracy is defined as the worst case deviation from the ideal input value including: offset, linearity and rollover error.

2: Noise is defined as the width of the uncertainty window (where the display will flicker) between two adjacent codes.

3: Applies to pins 17–20.

4: Analog Common falls out of regulation when the Low Battery Detect is asserted, however the ICL7149 will continue to operate correctly with a supply voltage above 7 volts and below 11 volts.

5: Guaranteed by design, not tested.

RDG = Reading

NOTE: All typical values have been characterized but are not tested.

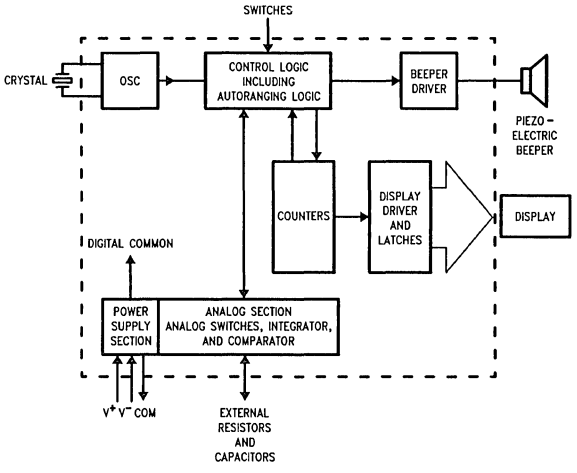

Figure 2: Functional Diagram

3¾-Digit Autoranging DMM Using Harris' ICL7149

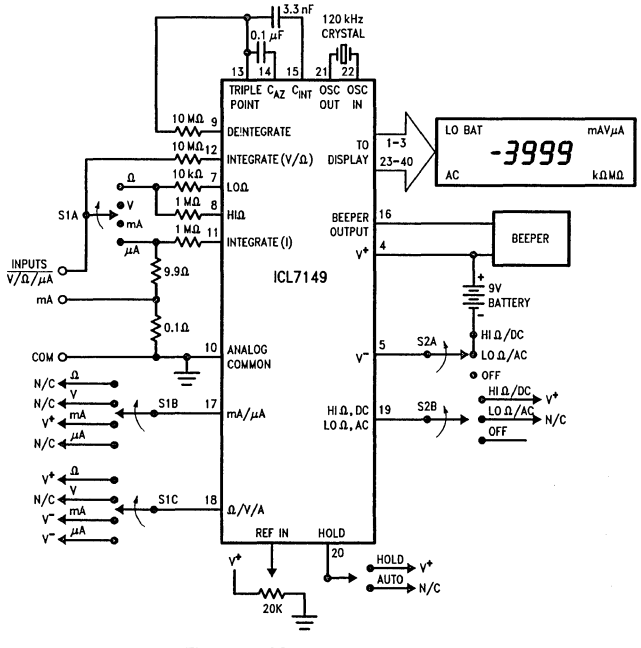

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Figure 3: ICL7149 Test Circuit

NOTE: All typical values have been characterized but are not tested.

Table 1: Pin Numbers and Functions

I/O	Pin Number	Pin Function
O	1	Segment Driver, POL/AC
O	2	Backplane 2
O	3	Backplane 1
I	4	V^+
I	5	V^-
I	6	Reference Input
O	7	Lo Ohms
O	8	Hi Ohms
I/O	9	Deintegrate
I/O	10	Analog Common
I	11	Int I
I	12	Int V/Ohms
I	13	Triple Point
I	14	Auto Zero Capacitor (C_{AZ})
I	15	Integrate Capacitor (C_{INT})
O	16	Beeper Output
I	17	mA/μA
I	18	Ohms/V/A
I	19	Hi Ohms-DC/Lo Ohms-AC
I	20	Hold
O	21	Oscillator Out
I	22	Oscillator In
O	23	Segment Driver k/m
O	24	Segment Driver Ohms/A
O	25	Segment Driver M Ohms/μA
O	26	Segment Driver Lo Bat/V
O	27	Segment Driver B_0/C_0
O	28	Segment Driver A_0/D_0
O	29	Segment Driver G_0/E_0
O	30	Segment Driver F_0/DP_1
O	31	Segment Driver B_1/C_1
O	32	Segment Driver A_1/D_1
O	33	Segment Driver G_1/E_1
O	34	Segment Driver F_1/DP_1
O	35	Segment Driver B_2/C_2
O	36	Segment Driver A_2/D_2
O	37	Segment Driver G_2/E_2
O	38	Segment Driver F_2/DP_3
O	39	Segment Driver B_3/C_3
O	40	Segment Driver ADG_3/E_3

NOTE: For segment drivers, segments are listed as (segment for backplane 1)/(segment for backplane 2). Example: pin 27; segment B0 is on backplane 1, segment C0 is on backplane 2.

DETAILED DESCRIPTION

General

Figure 2 is a simplified block diagram of the ICL7149. The digital section includes all control logic, counters, and display drivers. The digital section is powered by V^+ and Digital Common, which is about 3V below V^+. The oscillator is also in the digital section. Normally 120 kHz for rejection of 60 Hz AC interference and 100 kHz for rejection of 50 Hz AC, the oscillator output is divided by two to generate the internal master clock. The analog section contains the integrator, comparator, reference section, analog buffers, and several analog switches which are controlled by the digital logic. The analog section is powered from V^+ and V^-.

DC VOLTAGE MEASUREMENT

Autozero

Only those portions of the analog section which are used during DC voltage measurements are shown in Figure 5. As shown in the timing diagram (Figure 6), each measurement starts with an autozero (AZ) phase. During this phase, the integrator and comparator are configured as unity gain buffers and their non-inverting inputs are connected to Common. The output of the integrator, which is equal to its offset, is stored on C_{AZ}, the autozero capacitor. Similarly, the offset of the comparator is stored in C_{INT}. The autozero cycle equals 1000 clock cycles, which is one 60 Hz line cycle with a 120 kHz crystal, or one 50 Hz line cycle with a 100 kHz crystal.

Range 1 Integrate

The ICL7149 performs a full autorange search for each reading, beginning with range 1. During the range 1 integrate period, internal switches connect the INT V/Ohm terminal to the Triple Point (Pin 13). The input signal is integrated for 10 clock cycles, which are gated out over a period of 1000 clock cycles to ensure good normal mode rejection of AC line interference.

Range 1 Deintegrate

At the beginning of the deintegrate cycle, the polarity of the voltage on the integrator capacitor (C_{INT}) is checked, and either the $DEINT^+$ or $DEINT^-$ is asserted. The integrator capacitor C_{INT} is then discharged with a current equal to V_{REF}/R_{DEINT}. The comparator monitors the voltage on C_{INT}. When the voltage on C_{INT} is reduced to zero (actually to the V_{OS} of the comparator), the comparator output switches, and the current count is latched. If the C_{INT} voltage zero-crossing does not occur before 4000 counts have elapsed, the overload flag is set. "OL" (overload) is then displayed on the LCD. If the latched result is between 360 and 3999, the count is transferred to the output latches and is displayed. When the count is less than 360, an underrange has occurred, and the ICL7149 then switches to range 2—the 40V scale.

NOTE: All typical values have been characterized but are not tested.

Range 2

The range 2 measurement begins with an autozero cycle similar to the one that preceded range 1 integration. range 2 cycle length however, is one AC line cycle, minus 360 clock cycles. When performing the range 2 cycle, the signal is integrated for 100 clock cycles, distributed throughout one line cycle. This is done to maintain good normal mode rejection. Range 2 sensitivity is ten times greater than range 1 (100 vs 10 clock cycle integration) and the full scale voltage of range 2 is 40V. The range 2 deintegrate cycle is identical to the range 1 deintegrate cycle, with the result being displayed only for readings greater than 360 counts. If the reading is below 360 counts, the ICL7149 again asserts the internal underrange signal and proceeds to range 3.

Range 3

The range 3 or 4V full scale measurement is identical to the range 2 measurement, except that the input signal is integrated during the full 1000 clock cycles (one line frequency cycle). The result is displayed if the reading is greater than 360 counts. Underrange is asserted, and a range 4 measurement is performed if the result is below 360 counts.

Range 4

This measurement is similar to the range 1, 2 and 3 measurements, except that the integration period is 10,000 clock cycles (10 line cycles) long. The result of this measurement is transferred to the output latches and displayed even if the reading is less than 360.

Autozero

After finding the first range for which the reading is above 360 counts, the display is updated and an autozero cycle is entered. The length of the autozero cycle is variable which results in a fixed measurement period of 24,000 clock cycles (24 line cycles).

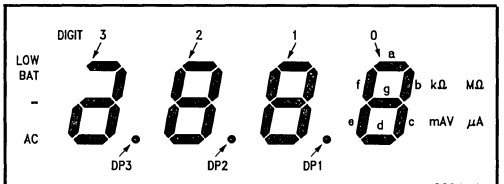

Figure 4: Display Segment Nomenclature

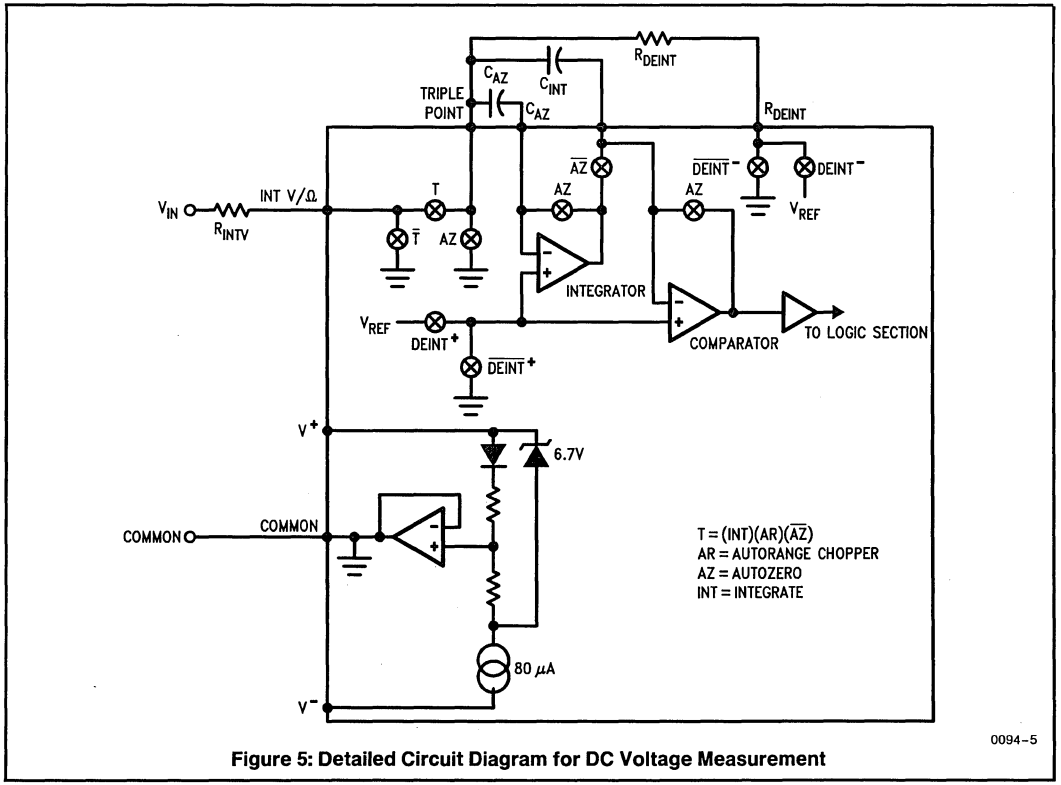

Figure 5: Detailed Circuit Diagram for DC Voltage Measurement

NOTE: All typical values have been characterized but are not tested.

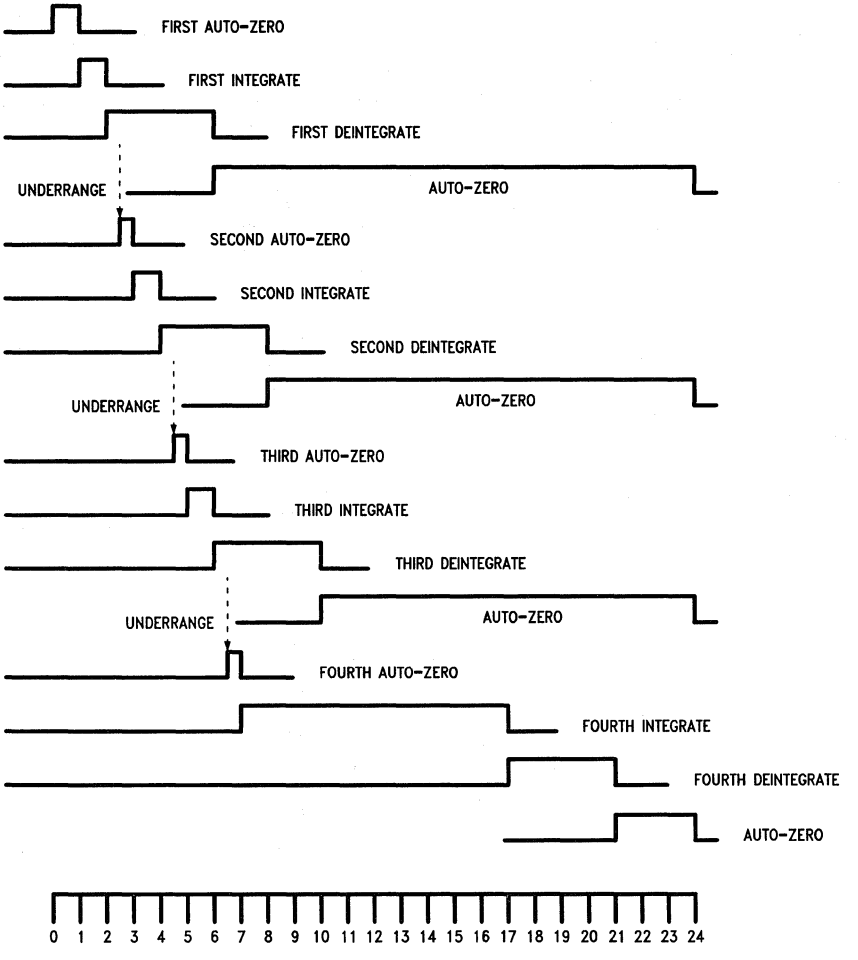

Figure 6: Timing Diagram for DC Voltage Measurement

DC CURRENT

Figure 7 shows a simplified block diagram of the analog section of the ICL7149 during DC current measurement. The DC current measurements are very similar to DC voltage measurements except: 1) The input voltage is developed by passing the input current through a 0.1 ohm (HI current ranges), or 9.9 ohm (LOW current ranges) current sensing resistor; 2) Only those ranges with 1000 and 10,000 clock cycles of integration are used; 3) The $R_{INT\ I}$ resistor is 1 megohm, rather than the 10 megohm value used for the $R_{INT\ V}$ resistor.

By using the lower value integration resistor, and only the 2 most sensitive ranges, the voltage drop across the current sensing resistor is 40 mV maximum on the 4 mA and 400 mA ranges; 400 mV maximum on the 40 mA and 4A scales. With some increase in noise, these "burden" voltages can be reduced by lowering the value of both the current sense resistors and the $R_{INT\ I}$ resistor proportionally. The DC current measurement timing diagram is similar to the DC voltage measurement timing diagram, except in the DC current timing diagram, the first and second integrate and deintegrate phases are skipped.

NOTE: All typical values have been characterized but are not tested.

AC VOLTAGE MEASUREMENT

The ICL7149 is designed to be used with an optional AC to DC voltage converter circuit. It will autorange through two voltage ranges (400V and 40V), and the AC annunciator is enabled as with the ICL7139. A typical averaging AC to DC converter is shown in Figure 8, while an RMS to DC converter is shown in Figure 9. AC current can also be measured with some simple modifications to either of the two circuits in Figures 8 and 9.

Ratiometric Ohms Measurement

The ratiometric ohms measurement is performed by first integrating the voltage across an unknown resistor, Rx, then effectively deintegrating the voltage across a known resistors (R_{KNOWN1} or R_{KNOWN2} of Figure 10). The shunting effect of R_{INTV} does not affect the reading because it cancels exactly between integration and deintegration. Like the current measurements, the ohm measurements are split into two sets of two ranges. LO ohms measurements use a 10 kilohm reference resistor, and the full scale ranges are 4 and 40 kilohms. HI ohms measurements use a 1 megohm reference resistor, and the full scale ranges are 0.4 and 4 megohms. The measurement phases and timing are the same as the measurement phases and timing for DC current except: 1) During the integrate phases the input voltage is the voltage across the unknown resistor Rx, and; 2) During the deintegrate phases, the input voltage is the voltage across the reference resistor R_{KNOWN1} or R_{KNOWN2}.

Continuity Indication

When the ICL7149 is in the LO ohms measurement mode, the continuity circuit of Figure 11 will be active. When the voltage across Rx is less than approximately 100 mV, the beeper output will be on. When R_{KNOWN} is 10 kilohms, the beeper output will be on when Rx is less than 1 kilohm.

Common Voltage

The analog and digital common voltages of the ICL7149 are generated by an on-chip resistor/zener/diode combination, shown in Figure 12. The resistor values are chosen so the coefficient of the diode voltage cancels the positive temperature coefficient of the zener voltage. This voltage is then buffered to provide the analog common and the digital common voltages. The nominal voltage between V^+ and analog common is 3V. The analog common buffer can sink about 20 mA, or source 0.01 mA, with an output impedance of 10 ohms. A pullup resistor to V^+ may be used if more sourcing capability is desired. Analog common may be used to generate the reference voltage, if desired.

Oscillator

The ICL7149 uses a parallel resonant-type crystal in a Pierce oscillator configuration, as shown in Figure 13, and requires no other external components. The crystal eliminates the need to trim the oscillator frequency. An external signal may be capacitively coupled to OSC IN, with a signal level between 0.5V and 3V pk-pk. Because the OSC OUT pin is not designed to drive large external loads, loading on this pin should not exceed a single CMOS input. The oscillator frequency is internally divided by two to generate the ICL7149 clock. The frequency should be 120 kHz to reject 60 Hz AC signals, and 100 kHz to reject 50 Hz signals.

Display Drivers

Figure 14 shows typical LCD Drive waveforms, RMS ON, and RMS OFF voltage calculations. Duplex multiplexing is used to minimize the number of connections between the ICL7149 and the LCD. The LCD has two separate backplanes. Each drive line can drive two individual segments, one referenced to each backplane. The ICL7149 drives 3¾ 7-segment digits, 3 decimal points, and 11 annunciators. Annunciators are used to indicate polarity, low battery condition, and the range in use. Peak drive voltage across the display is approximately 3V. An LCD with approximately 1.4V RMS threshold voltage should be used. The third voltage level needed for duplex drive waveforms is generated through an on-chip resistor string and the DC component of the drive waveforms is guaranteed to be less than 50 mV.

Ternary Input

The Ohms/Volts/Amps logic input is a ternary, or 3-level input. This input is internally tied to the common voltage through a high-value resistor, and will go to the middle, or "Volts" state, when not externally connected. When connected to V^-, approximately 5 μA of current flows out of the input. In this case, the logic level is the "Amps", or low state. When connected to V^+, about 5 μA of current flows into the input. Here, the logic level is the "Ohms", or high state. For other pins, see Table 2.

Table 2: Ternary Inputs Connections

Pin Number	V^+	OPEN or COM	V^-
17	mA	μA	Test
18	Ohms	Volts	Amps
19	HiΩ/DC	LoΩ/AC	Test
20	Hold	Auto	Test

NOTE: All typical values have been characterized but are not tested.

COMPONENT SELECTION

For optimum performance while maintaining the low-cost advantages of the ICL7149, care must be taken when selecting external components. This section reviews specifications and performance effects of various external components.

Integrator Capacitor, C_{INT}

As with all dual-slope integrating convertors, the integration capacitor must have low dielectric absorption to reduce linearity errors. Polypropylene capacitors add undetectable errors at a reasonable cost, while polystyrene and polycarbonate may be used in less critical applications. The ICL7149 is designed to use a 3.3 nF (0.0033 μF) C_{INT} with an oscillator frequency of 120 kHz and an R_{INTV} of 10 megohms. With a 100 kHz oscillator frequency (for 50 Hz line frequency rejection), both C_{INT} and R_{INTV} affect the voltage swing of the integrator. Voltage swing should be as high as possible without saturating the integrator, which occurs when the integrator output is within 1V of either V^+ or V^-. Integrator voltage swing should be about $\pm 2V$ when using standard component values. For different R_{INTV} and oscillator frequencies the value of C_{INT} can be calculated from:

$$C_{INT} = \frac{\text{(Integrate Time)} \times \text{(Integrate Current)}}{\text{(Desired Integrator Swing)}}$$

$$= \frac{(10{,}000 \times 2 \times \text{Oscillator Period}) \times 0.4V/R_{INTV}}{(2V)}$$

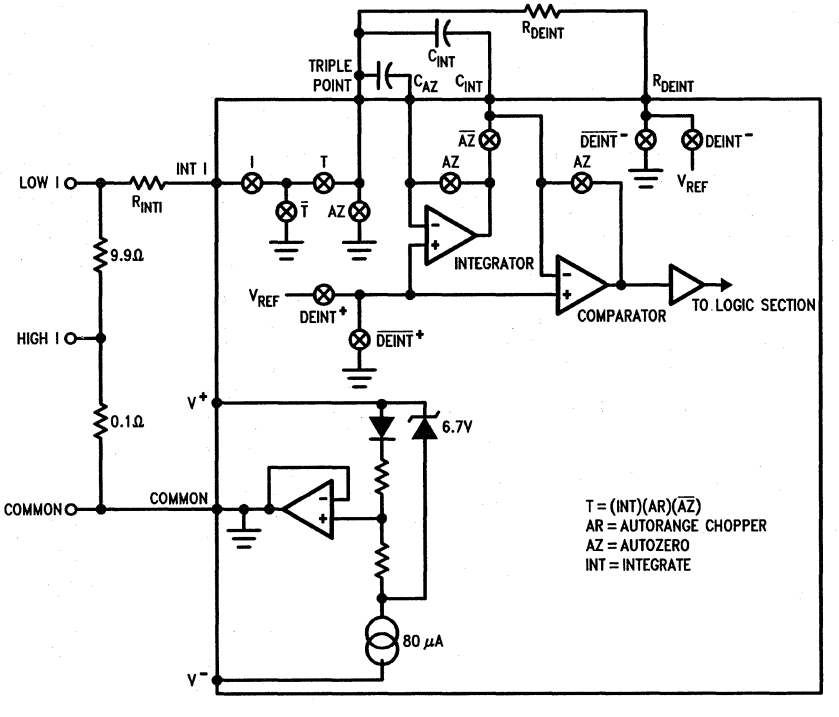

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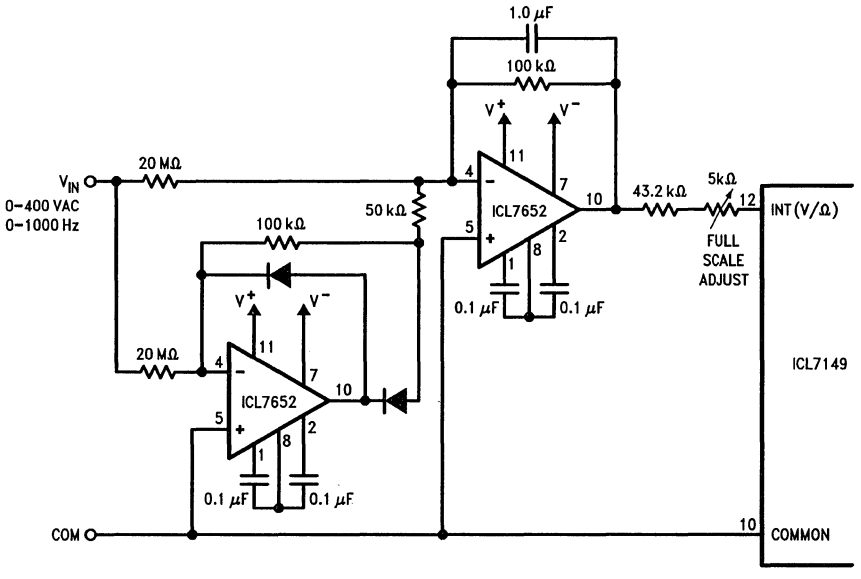
Figure 7: Detailed Circuit Diagram for DC Current Measurement

NOTE: All typical values have been characterized but are not tested.



NOTE: Diodes are low-leakage ID100.

Figure 8: AC Voltage Measurement Using Optional Averaging Circuit

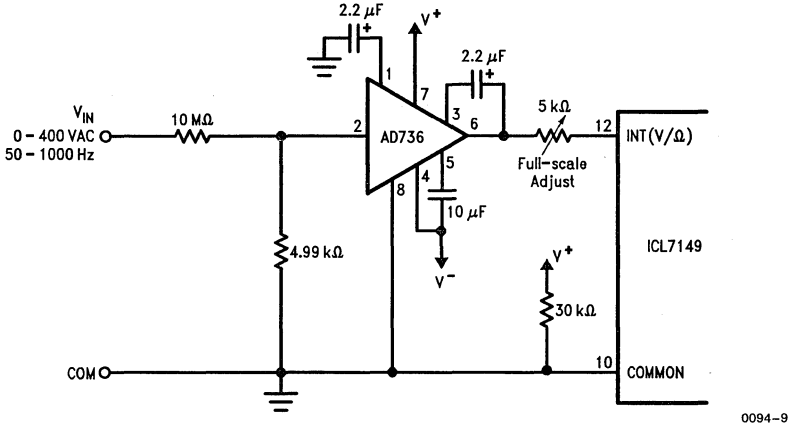


Figure 9: AC Voltage Measurement Using Optional RMS Converter Circuit

NOTE: All typical values have been characterized but are not tested.

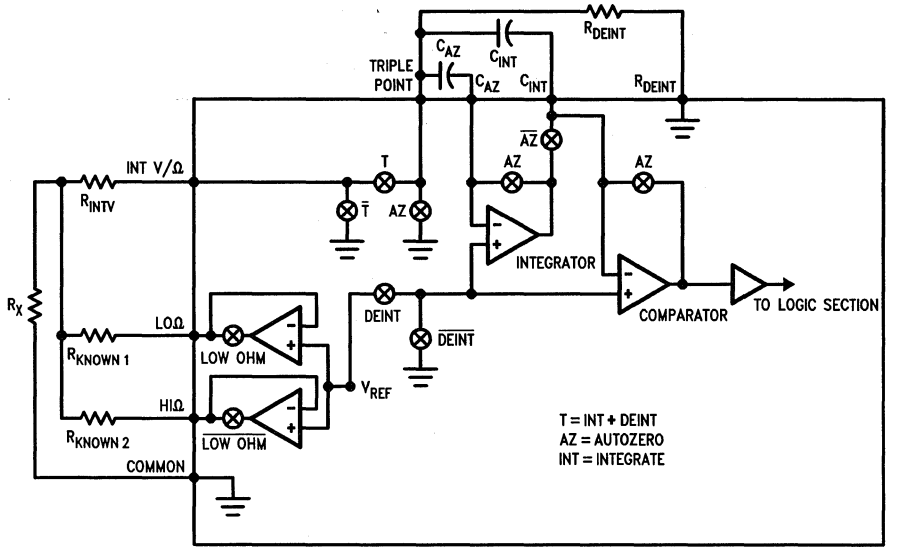


Figure 10: Detailed Circuit Diagram for Ratiometric Ohms Measurement

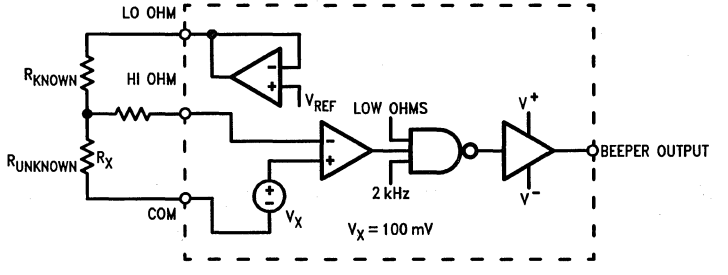


Figure 11: Continuity Beeper Drive Circuit

NOTE: The ICL7139 contains a comparator that is enabled on the lowest ohms range. It trips at approximately 1.5 kΩ and enables the beeper driver to oscillate (between V^- and V^+) at 2 kHz. The beeper driver is capable of driving a piezo-electric transducer. The beeper output response is independent of the state of the conversion; therefore appears instantaneous to the user. Some applications may require a 150 pF capacitor between pin 4 and pin 8 to insure a sharp on/off continuity detection.

NOTE: All typical values have been characterized but are not tested.

Integrator Resistors

The normal values of the $R_{INT\ V}$ and $R_{INT\ I}$ resistors are 10 megohms and 1 megohm respectively. Though their absolute values are not critical, unless the value of the current sensing resistors are trimmed, their ratio should be 10:1, within 0.05%. Some carbon composition resistors have a large voltage coefficient which will cause linearity errors on the 400V scale. Also, some carbon composition resistors are very noisy. The class "A" output of the integrator begins to have nonlinearities if required to sink more than 70 μA (the sourcing limit is much higher). Because $R_{INT\ V}$ drives a virtual ground point, the input impedance of the meter is equal to $R_{INT\ V}$.

Deintegration Resistor, R_{DEINT}

Unlike most dual-slope A/D converters, the ICL7149 uses different resistors for integration and deintegration. R_{DEINT} should normally be the same value as R_{INTV}, and have the same temperature coefficient. Slight errors in matching may be corrected by trimming the reference voltage.

Autozero Capacitor, C_{AZ}

The C_{AZ} is charged to the integrator's offset voltage during the autozero phases, and subtracts that voltage from the input signal during the integrate phases. The integrator thus appears to have zero offset voltage. Minimum C_{AZ} value is determined by: 1) Circuit leakages; 2) C_{AZ} self-discharge; 3) Charge injection from the internal autozero switches. To avoid errors, the C_{AZ} voltage change should be less than $1/_{10}$ of a count during the 10,000 count clock cycle integration period for the 400 mV range. These requirements set a lower limit of 0.047 μF for C_{AZ} but 0.1 μF is the preferred value. The upper limit on the value of C_{AZ} is set by the time constant of the autozero loop, and the line cycle time period allotted to autozero. C_{AZ} may be several 10s of microfarads before approaching this limit.

The ideal C_{AZ} is a low leakage polypropylene or Teflon capacitor. Other film capacitors such as polyester, polystyrene, and polycarbonate introduce negligible errors. If a few seconds of settling time upon power-up is acceptable, the C_{AZ} may be a ceramic capacitor, provided it does not have excessive leakage.

Ohms Measurement Resistors

Because the ICL7149 uses a ratiometric ohms measurement technique, the accuracy of ohms reading is primarily determined by the absolute accuracy of the R_{KNOWN1} and R_{KNOWN2}. These should normally be 10 kilohms and 1 megohm, with an absolute accuracy of at least 0.5%.

Current Sensing Resistors

The 0.1 ohm and 9.9 ohm current sensing resistors convert the measured current to a voltage, which is then measured using $R_{INT\ I}$. The two resistors must be closely matched, and the ratio between $R_{INT\ I}$ and these two resistors must be accurate—normally 0.5%. The 0.1 ohm resistor must be capable of handling the full scale current of 4 amps, which requires it to dissipate 1.6 watts.

Continuity Beeper

The Continuity Beeper output is designed to drive a piezoelectric transducer at 2 kHz (using a 120 kHz crystal), with a voltage output swing of V^+ to V^-. The beeper output off state is at the V^+ rail. When crystals with different frequencies are used, the frequency needed to drive the transducer can be calculated by dividing the crystal frequency by 60.

Display

The ICL7149 uses a custom, duplexed drive display with range, polarity, and low battery annunciators. With a 3 volt peak display voltage, the RMS ON voltage will be 2.37V minimum; RMS OFF voltage will be 1.06V maximum. Because the display voltage is not adjustable, the display should have a 10% ON threshold of about 1.4V. Most

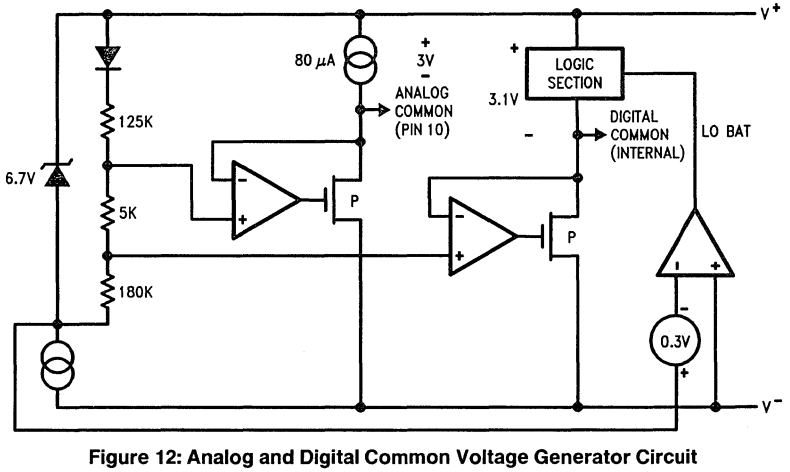


Figure 12: Analog and Digital Common Voltage Generator Circuit

NOTE: All typical values have been characterized but are not tested.

display manufacturers supply a graph that shows contrast versus RMS drive voltage. This graph can be used to determine what the contrast ratio will be when driven by the ICL7149. Most display thresholds decrease with increasing temperature, and the threshold at the maximum operating temperature should be checked to ensure that the "off" segments will not be turned "on" at high temperatures.

Crystal

The ICL7149 is designed to use a parallel resonant 120 kHz or 100 kHz crystal with no additional external components. The R_S parameter should be less than 25 kilohms to ensure oscillation. Initial frequency tolerance of the crystal can be a relatively loose 0.05%

Switches

Because the logic input draws only about 5 μA, switches driving these inputs should be rated for low current, or "dry" operations. The switches on the external inputs must be able to reliably switch low currents, and be able to handle voltages in excess of 400V AC.

Reference Voltage Source

A voltage divider connected to V^+ and Common is the simplest source of reference voltage. While minimizing external component count, this approach will provide the same voltage tempco as the ICL7149 Common—about 100 PPM/°C. To improve the tempco, an ICL8069 bandgap reference may be used (see Figure 15). The reference voltage source output impedance must be $\leq R_{DEINT}/4000$.

Applications, Examples, and Hints

A complete autoranging 3¾ digit multimeter is shown in Figure 16. The following sections discuss the functions of specific components and various options.

Meter Protection

The ICL7149 and its external circuitry should be protected against accidental application of 110/220V AC line voltages on the ohms and current ranges. Without the necessary precautions, both the 7149 and its external components could be damaged under such fault conditions. For the current ranges, fast-blow fuses should be used between S5A in Figure 16 and the 0.1 ohm and 9.9 ohm shunt resistors. For the ohms ranges, no additional protection circuitry is required. However, the 10 kilohm resistor connected to pin 7 must be able to dissipate 1.2W or 4.8W for short periods of time during accidental application of 110V or 220V AC line voltages respectively.

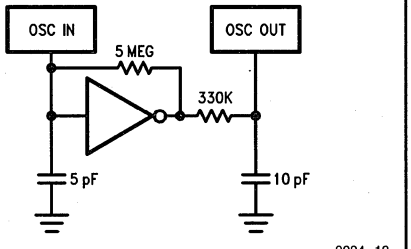


Figure 13: Internal Oscillator Circuit Diagram

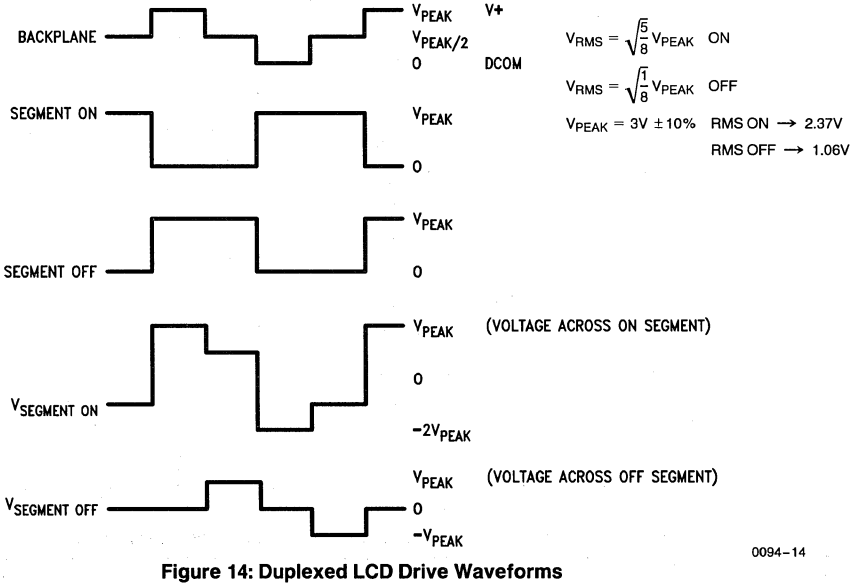


Figure 14: Duplexed LCD Drive Waveforms

NOTE: All typical values have been characterized but are not tested.

Printed Circuit Board Layout Considerations

Particular attention must be paid to rollover performance, leakages, and guarding when designing the PCB for a ICL7149-based multimeter.

Rollover Performance, Leakages, and Guarding

Because the ICL7139 system measures very low currents, it is essential that the PCB have low leakage. Boards should be properly cleaned after soldering. Areas of particular importance are: 1) The INT V/Ω and INT I Pins; 2) The Triple Point; 3) The R_{DEINT} and the C_{AZ} pins.

The conversion scheme used by the ICL7139 changes the common mode voltage on the integrator and the capacitors C_{AZ} and C_{INT} during a positive deintegrate cycle. Stray capacitance to ground is charged when this occurs, removing some of the charge on C_{INT} and causing rollover error. Rollover error increases about 1 count for each picofarad of capacitance between C_{AZ} or the Triple Point and ground, and is seen as a zero offset for positive voltages. Rollover error is not seen as gain error.

The rollover error causes the width of the +0 count to be larger than normal. The ICL7139 will thus read zero until several hundred microvolts are applied in the positive direction. The ICL7139 will read −1 when approximately −100 μV are applied.

The rollover error can be minimized by guarding the Triple Point and C_{AZ} nodes with a trace connected to the C_{INT} pin, which is driven by the output of the integrator. Guarding these nodes with the output of the integrator reduces the stray capacitance to ground, which minimizes the charge error on C_{INT} and C_{AZ}. If possible, the guarding should be used on both sides of the PC board.

Stray Pickup

While the ICL7149 has excellent rejection of line frequency noise and pickup in the DC ranges, any stray coupling will affect the AC reading. Generally, the analog circuitry should be as close as possible to the ICL7149. The analog circuitry should be removed or shielded from any 120V AC power inputs, and any AC sources such as LCD drive waveforms. Keeping the analog circuit section close to the ICL7149 will also help keep the area free of any loops, thus reducing magnetically coupled interference coming from power transformers, or other sources.

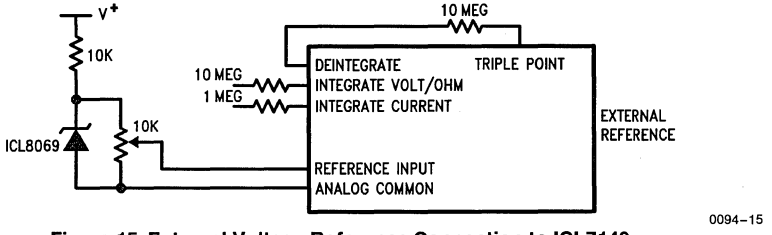


Figure 15: External Voltage Reference Connection to ICL7149

NOTE: All typical values have been characterized but are not tested.

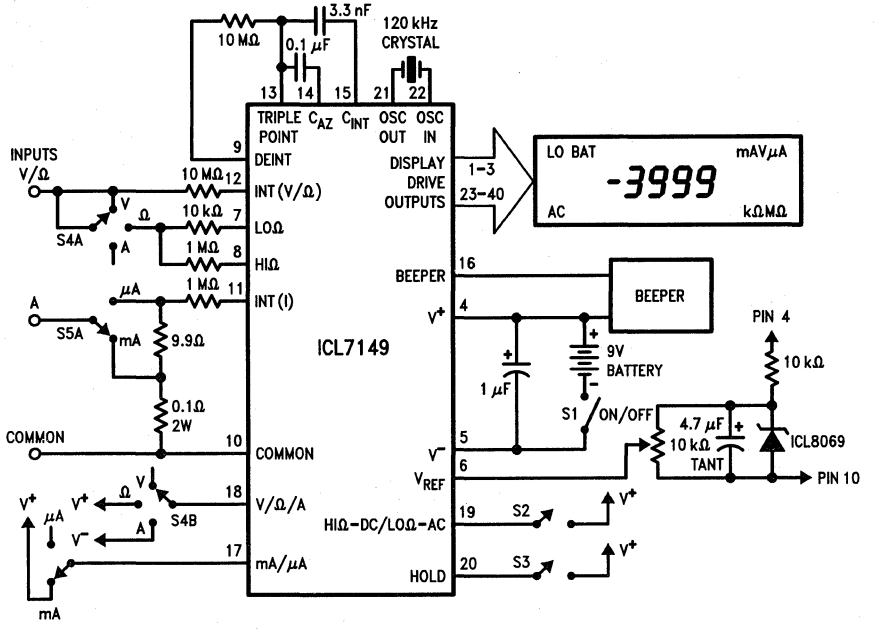


Figure 16: Basic Multimeter Application Circuit for ICL7149

NOTE 1: Crystal is a Statek CX-1V type.

2: Multimeter protection components have not been shown.

3: Display is from LXD, part number 38D8R02H or equivalent.

4: Beeper is from muRata, part number PKM24-4A0 or equivalent.

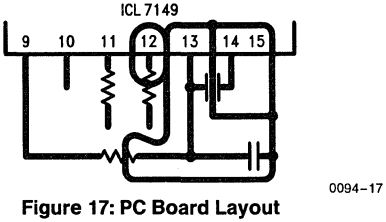


Figure 17: PC Board Layout

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICL7182
101 Segment LCD Bargraph A/D Converter

GENERAL DESCRIPTION

The Harris ICL7182 is a complete analog-to-digital converter (ADC) that directly drives a multiplexed liquid crystal display (LCD). Included are a charge-balanced ADC, a 2.56V bandgap reference, display decode and driver, and a 50 kHz oscillator. Only a display and three passive components are required for a complete analog bargraph.

The fully differential analog and reference inputs may be operated anywhere between and including the supply rails. This allows sensing either ground-referenced signals or bridge configurations. Linearity and zero offset errors are guaranteed to be less than 0.5% for a 1V full-scale input. The full-scale differential input range is 200 mV to 1.1V.

The low drift 50 ppm/°C reference is trimmed to 1.5% accuracy and, when used with a simple resistor divider, can set the full-scale input voltage. The reference, when used with an Harris ICL7660, extends the operating supply range from 3V to 40V and allows sensing input signals below ground.

The backplane and segment drivers supply the LCD with the proper waveforms to create a discrete series of segments forming a 101 segment bar which is proportional to the input voltage, with a plus or minus annunciator to indicate the polarity. In addition, three independent TTL controllable annunciators are provided for limit or unit indication. The bargraph multiplexing scheme provides duplex contrast ratio and allows the complete system to be placed in a standard 40 pin DIP. The LCD operating voltage is externally set to adjust contrast for a range of fluid types and temperature.

The internal oscillator requires no external components and establishes the conversion rate and backplane clock frequency. The nominal conversion rate of 25 per second can be easily changed between 15 to 40 conversions per second by adding a single capacitor or overdriving the oscillator.

FEATURES

- 1% Resolution . . . 100 Data Segments Plus Zero
- No Missing Segments Guaranteed
- Single 5V Supply Operation
- Only Three Passive Components Required
- True Differential Input and Reference
- Direct LCD Display Drive Provides Duplex Contrast Ratio
- Overrange and Polarity Indication
- Three User Defined Annunciators—Easily Expandable
- Precision On-Chip Reference . . . 50 ppm/°C
- Low Average Power Consumption . . . 1.8 mW
- 40 Pin DIP or 44 Pin Surface Mount Package
- Extended Temperature Range Operation

ORDERING INFORMATION

Part Number	Temperature Range	Package Description
ICL7182CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7182CM44	0°C to +70°C	44-Pin Surface Mount

2

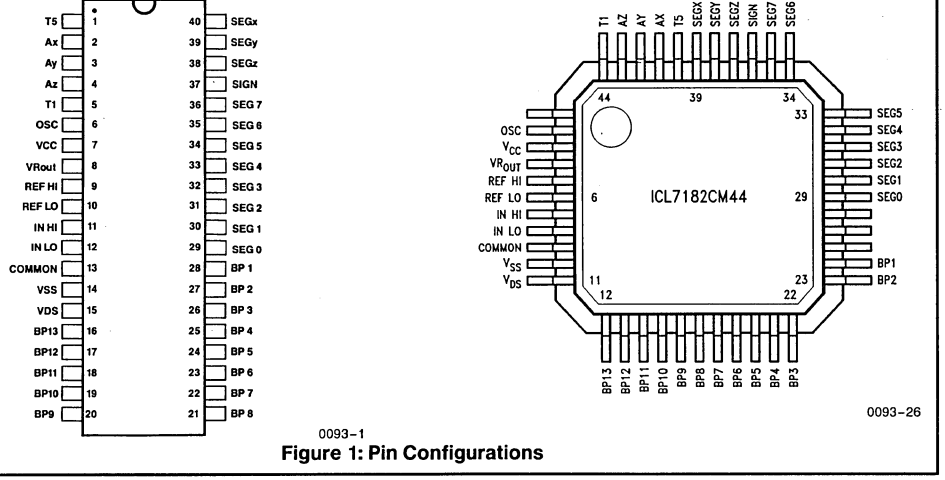


Figure 1: Pin Configurations

310675-002

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC} to V_{SS}) 10V
Supply Voltage (V_{CC} to V_{DS}) 11V
Display Drive Pin Voltage ..... (V_{CC} + 0.3V) to (V_{DS} − 0.3V)
Analog or Reference Inputs .... (V_{CC} + 0.3V) to (V_{SS} − 0.3V)
Com, Osc, Ax, Ay,
Az, T1, T5 Pins ..... (V_{CC} + 0.3V) to (V_{SS} − 0.3V)
Reference Output Current ..... 8 mA
Lead Temperature (Soldering, 10 sec) ..... 300°C
Storage Temperature Range ..... −65°C to +150°C
Operating Temperature Range ..... −25°C to +85°C
Continuous Total Power Dissipation (T_A = 25°C)
40 Pin DIP Plastic Package ..... 500 mW
44 Pin CM Plastic Package ..... 375 mW

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

Unless otherwise stated: V_{CC} = 5.0V, V_{SS} = V_{DS} = GND, T_A = 25°C, V_{REF} = 1.000V, VIN_{CM} = $VREF_{CM}$ = 2.5V, pin 6 open (Note 1)

Parameter	Test Conditions	Limits			Units
		Min	Typ	Max	
Zero Input Reading	V_{IN} = 0.0V	−0	±0	+0	Segs
Unadjusted Gain Error	V_{IN} = V_{REF}	−1	0	+1	Segs
Linearity Error	(Note 2)	−0.63	±0.2	+0.63	Segs
Rollover Error	V_{IN} = −V_{REF} (Note 3)	−0.5	±0.1	+0.5	Segs
Conversion Time			400		µs
Display Update Rate			25		Hz
Input Referred Noise	(Note 4)		500		µV
DC Power Supply Rejection	V_{CC} = 4.5 to 6.0V		0.02	0.3	Segs/V
ANALOG INPUT					
Common Mode Rejection Ratio	VIN_{CM} = 0V to 5V, V_{IN} ≅ 0V		0.02	0.1	Segs/V
Differential Mode Input			1.0	1.1	V
Average Input Current	V_{IN} = 1.0V (Note 5)		1.3		nA
REFERENCE INPUT					
Common Mode Rejection Ratio	$VREF_{CM}$ = 0.5V to 4.5V		0.01	0.1	Segs/V
Average Input Current	(Note 6)		6		nA
REFERENCE OUTPUT					
Output Voltage	V_{CC} − VRout, Iout = 0 µA	2.520	2.560	2.590	V
Temperature Coefficient	−25°C < T_A < 85°C, Iout = 0 µA		50	200	ppm/°C
Output Impedance	Iout = +10 µA to −2 mA		1.3	5	Ω
Current Into VRout Pin		10	20		µA
Current Out of VRout			8	2	mA
Output Noise	0.1 Hz to 10 Hz (Note 4)		110		µV
POWER SUPPLY					
Supply Current Average	(Note 6)		350	500	µA
Supply Current Peak	(Note 6)		1.5	2.0	mA
Supply Voltage Range	Guaranteed by PSRR	4.5	5.0	6.0	V
OSCILLATOR					
Oscillator Frequency	Osc Pin Open	26	51	72	kHz
Backplane Frequency	Osc Pin Open	25	50	70	Hz
DISPLAY DRIVE					
Display Output Impedance	V_{CC} − V_{DS} = 3V to 7V		70	200	kΩ
DC Component of Display	V_{CC} − V_{DS} = 3V to 7V	−50	±10	50	mV
V_{DS} Supply Current	V_{CC} − V_{DS} = 3V to 7V (Note 7)		60	120	µA

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) Unless otherwise stated: V_{CC} = 5.0V, V_{SS} = V_{DS} = GND, T_A = 25°C, V_{REF} = 1.000V, VIN_{CM} = $VREF_{CM}$ = 2.5V, pin 6 open (Note 1)

Parameter	Test Conditions	Limits			Units
		Min	Typ	Max	
ANNUNCIATOR INPUTS					
Input High Voltage	Operating Temp Range	2.4			V
Input Low Voltage	Operating Temp Range			0.8	V
Input Leakage	Operating Temp Range	−1	0.001	+1	µA

NOTE 1: The differential mode input voltages are defined as: V_{IN} = (IN HI − IN LO) and VREF = (REF HI − REF LO). The common mode input voltage, VIN_{CM} and $VREF_{CM}$, is defined as the average differential input voltage with respect to V_{SS}.

2: The linearity error is the deviation from a straight line which passes through negative full scale and postive full scale readings.

3: The rollover error is defined as the difference in reading for equal positive and negative inputs near full-scale.

4: Peak to peak value not exceeded 95% of the time (±2 standard deviations).

5: Defined as the average current flowing into the input with a 1.0 µF capacitor across V_{IN} or V_{REF} inputs and the common mode voltage at ½ VCC.

6: The average supply current is measured with a supply bypass capacitor and annunciator inputs tied to V_{SS}.

7: The supply current for V_{DS} flows from the V_{CC} pin.

PIN DESCRIPTION AND FUNCTION

Pin No.	Symbol	Description
1	T5	Test pin #5, buffered oscillator frequency divided by two that can typically source and sink 2 mA.
2	Ax	Annunciator Segx select, low turns on Segx, high turns off Segx.
3	Ay	Annunciator Segy select, low turns on Segy, high turns off Segy.
4	Az	Annunciator Segz select, low turns on Segz, high turns off Segz.
5	T1	Test pin #1, normally left open or tied to V_{SS}.
6	Osc	50 kHz free running oscillator control and clock input pin. The internal oscillator may be overdriven by a 30 to 80 kHz external clock driving pin 6, or the free running frequency can be reduced by adding an external capacitor between pin 6 and V_{CC}.
7	V_{CC}	Positive supply voltage.
8	VRout	Bandgap reference buffered output, down 2.56V from V_{CC}.
9	REF HI	Positive Reference Input.
10	REF LO	Negative Reference Input.
11	IN HI	Positive Analog Input.
12	IN LO	Negative Analog Input.
13	Common	Internally generated voltage which is typically within ±50 mV of ½ (V_{CC} − V_{SS}) and has 1.4 kΩ output impedance. This pin is normally left open or bypassed with a 0.1 µF capacitor to signal ground.
14	V_{SS}	Negative supply voltage, normally ground.
15	V_{DS}	Display negative voltage, establishes the pk-pk display drive.
16–28	BP13–BP1	LCD backplane drivers.
29–36	Seg0–Seg7	LCD segment drivers.
37	Sign	Positive sign segment driver.
38	Segz	Annunciator driver selected by Az.
39	Segy	Annunciator driver selected by Ay.
40	Segx	Annunciator driver selected by Ax.

NOTE: All typical values have been characterized but are not tested.

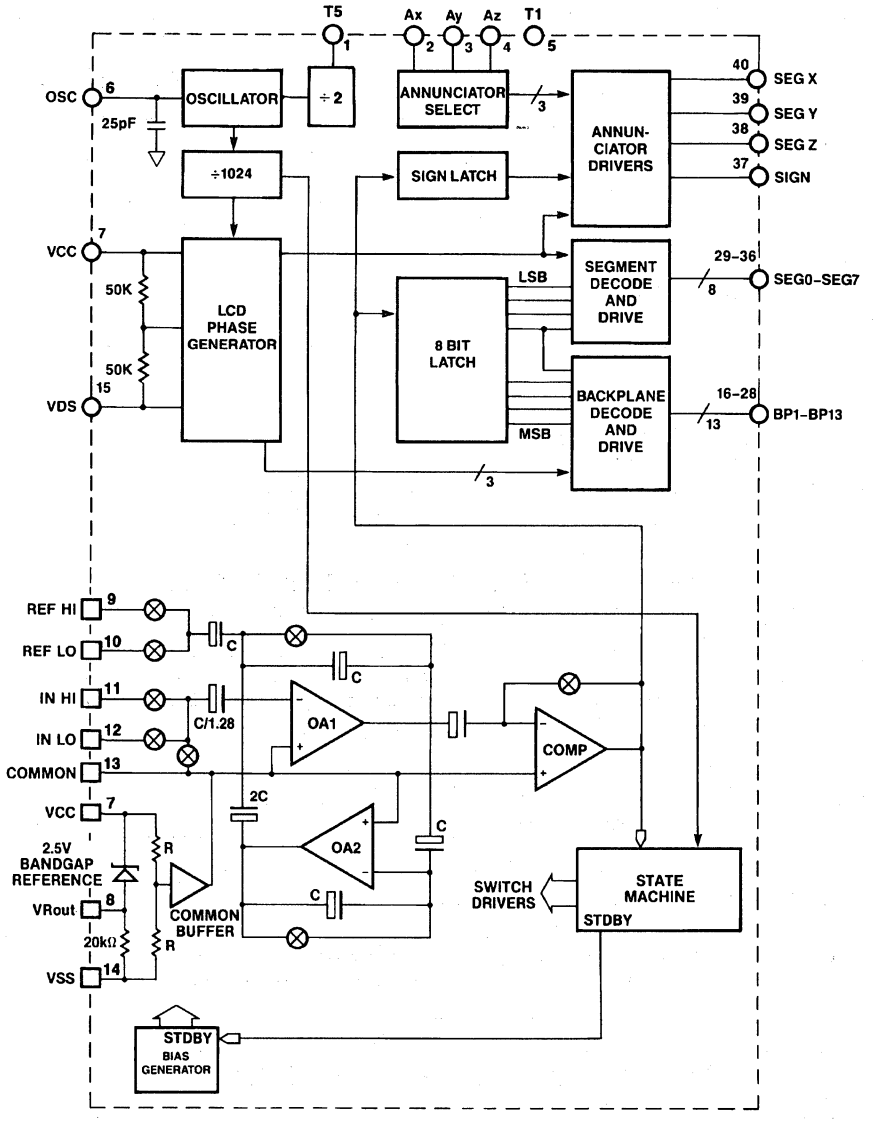


Figure 2: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

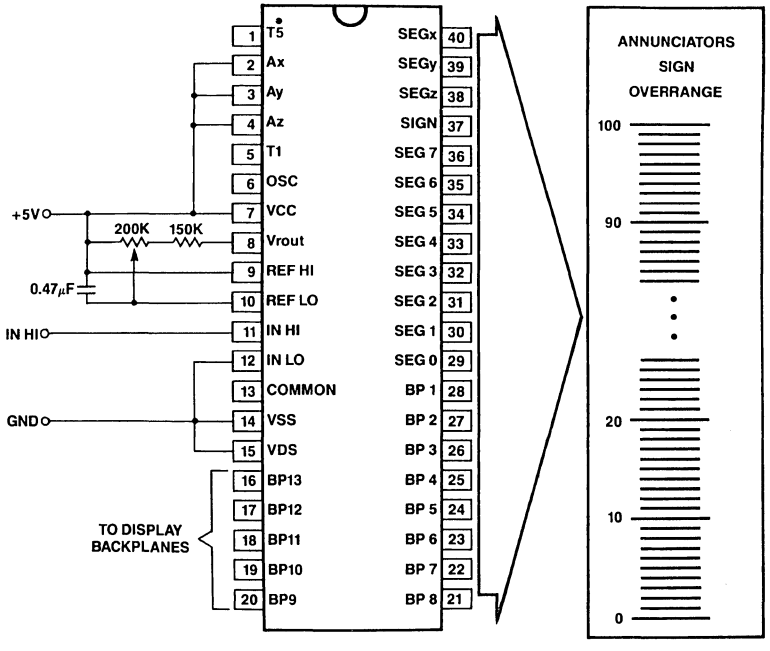
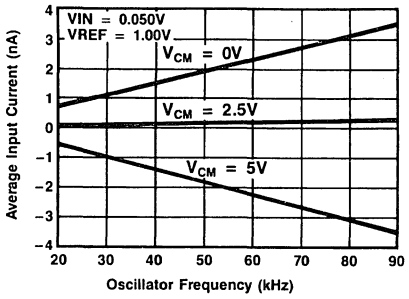


Figure 3: ICL7182 using the internal reference. Values shown are for 1.000V full-scale, 25 readings per second, single 5V supply.

TYPICAL PERFORMANCE CHARACTERISTICS

Average Analog Input Current vs. Frequency and Common Mode Voltage



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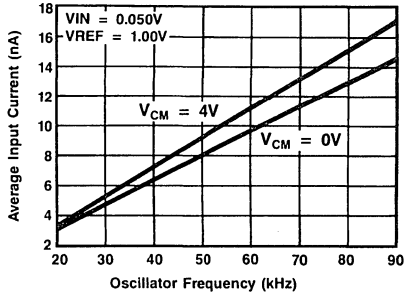
Average Reference Input Current vs. Frequency and Common Mode Voltage

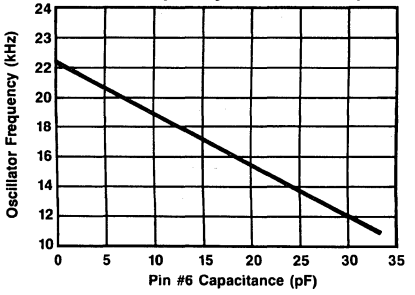


0093-5

NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Oscillator Frequency vs. Pin #6 Capacitor



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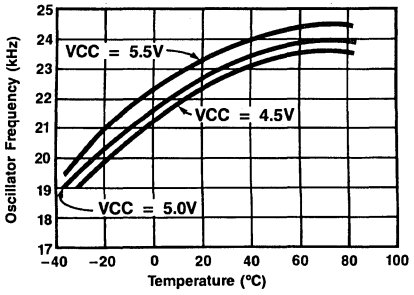
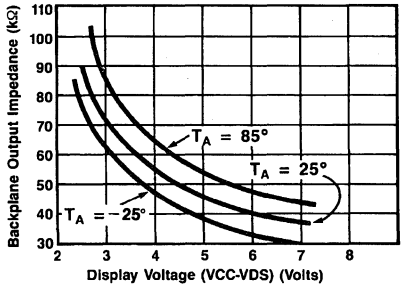
Oscillator Frequency vs. Temperature and Supply Voltage



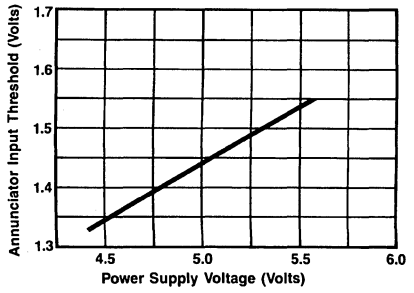
0093-7

Backplane Output Impedance vs. V_{DS} and Temperature



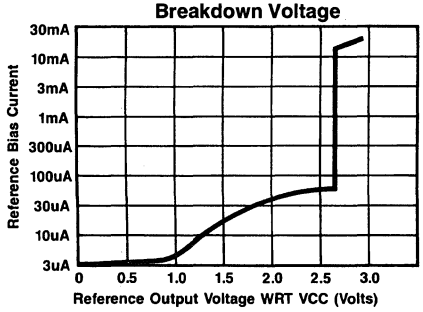
0093-8

Annunciator Input Threshold vs. Power Supply Voltage



0093-9

Reference Bias Current vs. Breakdown Voltage



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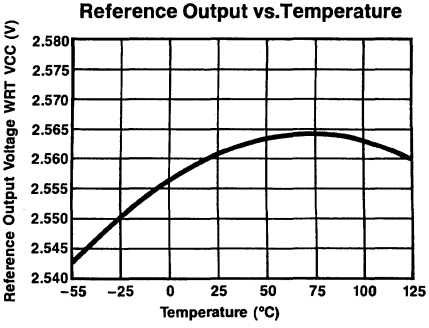
Reference Output vs.Temperature



0093-11

NOTE: All typical values have been characterized but are not tested.

FUNCTIONAL DESCRIPTION

A functional diagram of the ICL7182 A/D converter is shown in Figure 2. The device operates on the cyclic converter principle implemented with switched capacitor amplifiers. Analog switches are closed sequentially by state machine control logic to sample the input and perform a multiply-by-two and delay function. The sampled input charge is recirculated and compared to the reference to determine the weight of each bit. The sign is determined first and after 18 cycles a 9-bit binary code is latched and the display is updated.

Under normal operation the conversion requires 32 clock cycles and the display updates once every 2048 clock cycles. Before and during the conversion the supply current for the analog section increases from typically 300 μA to 1.3 mA and remains high for a total of 96 clock cycles. The operation proceeds as follows:

Clock Cycle	Operation
0–96	Supply current increases from 300 μA to 1.3 mA
0–47	Converter autozero begins
48	IN LO is sampled
49	IN HI is sampled
50–70	REF LO and REF HI are sampled once per clock cycle
71–77	Converter output is latched and display is updated
78–2047	Supply current decreases from 1.3 mA to 300 μA
2048	New conversion begins

The changing supply current may result in a noisy reading if the supply dynamic impedance is high. This can be resolved by using a supply bypass capacitor.

Analog Inputs

The analog and reference inputs are guaranteed to correctly operate within the supply voltage. Both inputs will continue to function 200 mV to 400 mV outside of the supplies but the converter specifications degrade as the input protection diodes become forward biased.

As the reference and analog inputs are sampled, transient currents flow from the inputs to charge small internal capacitors.

These transient currents occur at the leading edge of the internal clock and decay at a rate determined by the input capacitance of the converter and the source resistance. Source resistances larger than Rs given in the equation below will cause conversion errors.

$$Rs\ (max) = \frac{1}{6\ (Fosc)\ (Cin)}$$

Where: Fosc = Oscillator frequency
Cin = 40 pF, typical input capacitance
Rs = Source resistance

Input Bypass Capacitor

For source resistances larger than Rs above (typically 80 kΩ) bypass capacitors across the inputs will average these charging currents and cause a small DC current to flow through the output resistance of the analog and reference source signals. The average input current is a function of the common mode voltage and the oscillator frequency (see typical graphs). This current is typically 2 nA for the analog input and 6 nA for the reference input. The effects of the voltage drops across source resistances, due to the average value of input current, can be compensated by full-scale adjustment while the given source resistor and input bypass capacitor are in place.

Reference Output

The internal bandgap reference behaves like a 2.56V zener with the cathode tied to V_{CC} and the anode tied to VRout. The regulator circuitry maintains a low 1.3Ω output impedance for bias currents through the zener between 90 μA and 2 mA. At minimum supply voltage the internal 20 kΩ resistor will provide 10 μA of current sink into VRout. The minimum sink current may be increased by adding an external resistor from VRout to V_{SS}.

The reference is internally trimmed to within 1.5% of 2.56V. The reference output can be externally divided (see Figure 3) to establish the full-scale input. Two fixed value resistors with 1% tolerance will relate to a system accuracy of 2% RMS.

NOTE: All typical values have been characterized but are not tested.

Display Drive

The binary output of the A/D converter is encoded to drive 8 segments that serpentine across thirteen backplanes of an LCD display. The backplanes are driven with three level signals and the segment lines are driven with two level signals. The three levels of the backplane are set by the V_{CC} supply, the V_{DS} supply, and the output of a voltage divider which is connected between V_{CC} and V_{DS}. The two levels of the segment drive are set by the V_{CC} and V_{DS} supplies.

The bargraph takes advantage of the fact that above a particular segment all segments will be off and below that segment all segments will be on, also that only one backplane will have segments which are both on and off. The backplanes with all segments off are driven with an "off backplane" waveform, the backplanes with all segments on are driven with an "on backplane" waveform, and the one backplane with both on and off segments is driven with a "unique backplane" waveform. The off segments are driven with an off segment waveform and the on segments are driven with an on segment waveform with respect to the unique backplane. The sign segment and annunciator segment drives are designed for use with respect to BP1. The phasing between display waveforms is shown in Figure 4.

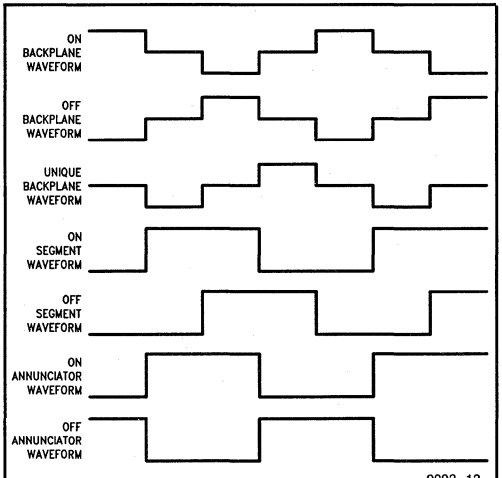


Figure 4: Display Drive Waveforms

The LCD segments appear ON when the RMS voltage between the backplane and segment drives is greater than the 90%-ON voltage of the LCD fluid, and they appear OFF when the RMS voltage is less than 10%-ON voltage of the LCD fluid. For the ½ multiplexed (duplex) waveforms used on the ICL7182 a 2.25:1 contrast ratio is achieved.

Display Set Voltage

The V_{DS} pin sets the peak-to-peak amplitude of the display drive waveforms. This voltage should be selected to give maximum contrast for a particular LCD fluid type and temperature. Good contrast ratio is obtained if V_{DS} is set within the range determined by the equation below.

$$(1.27)(Vth_{90\%}) \leq (V_{CC} - V_{DS}) \leq (2.26)(Vth_{10\%})$$

Where: $Vth_{90\%}$ = 90% ON Visual Threshold

$Vth_{10\%}$ = 10% ON Visual Threshold

For example the Hamlin Inc. type 02 LCD fluid has $Vth_{90\%}$ = 3.05V and $Vth_{10\%}$ = 2.2V, therefore the best contrast is achieved when $V_{CC} - V_{DS}$ is set between 3.9V and 5V. For most applications where V_{CC} is tied to a +5V supply the V_{DS} pin can be tied to ground.

To accommodate a large range of temperatures and fluid types the V_{DS} pin can be driven above or below V_{SS}. The voltage difference between V_{CC} and V_{DS} can vary from from 3V to 7V. For $V_{CC} - V_{DS}$ less than 3V the output impedance of the backplane drivers increase substantially. The dependence of display drive output impedance on V_{DS} and temperature is shown in the typical performance curves.

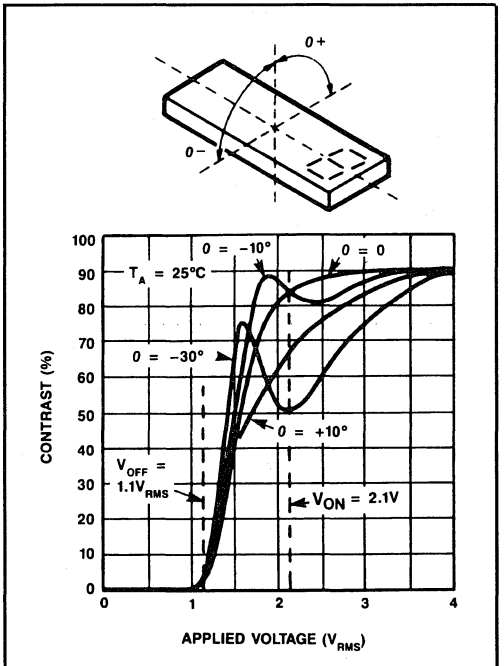


Figure 5: Contrast vs. Applied RMS Voltage

NOTE: All typical values have been characterized but are not tested.

Display Set Voltage (Continued)

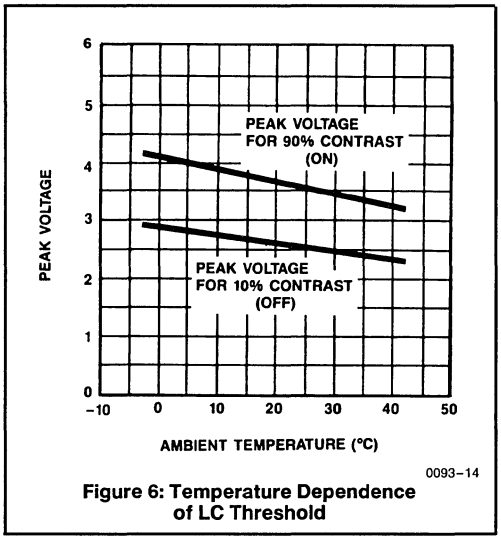


Figure 6: Temperature Dependence of LC Threshold

Temperature Effects and Temperature Compensation

The performance of the IC material is affected by temperature in two ways. The response time of the display to changes in applied RMS voltage gets longer as the display temperature drops. At very low temperatures (−20°C) some displays may take several seconds to change a new character after the new information appears at the outputs. However, for most applications above 0°C this will not be a problem with available multiplexed LCD materials, and for low-temperature applications, high-speed liquid crystal materials are available. One high temperature effect to consider deals with plastic materials used to make the polarizer. Some polarizers become soft at high temperatures and permanently lose their polarizing ability, thereby seriously degrading display contrast. Some displays also use sealing materials unsuitable for high temperature use. Thus, when specifying displays the following must be kept in mind: liquid crystal material, polarizer, and seal materials.

A more important effect of temperature is the variation of threshold voltage. For typical liquid crystal materials suitable for multiplexing, the peak voltage has a temperature coefficient of −7 to −14 mV/°C. This means that as temperature rises, the threshold voltage goes down. Assuming a fixed value for V_P, when the threshold voltage drops below $V_P/3$ OFF segments begin to be visible. Figure 6 shows the temperature dependence of peak voltage for the same liquid crystal material of Figure 5.

For applications where the display temperature does not vary widely, V_P may be set at a fixed voltage chosen to make the RMS OFF voltage, $V_P/3$, just below the threshold voltage at the highest temperature expected. This will prevent OFF segments turning ON at high temperature (this at the cost of reduced contrast for ON segments at low temperatures).

For applications where the display temperature may vary to wider extremes, the display voltage V_{DISP} (and thus V_P) may require temperature compensation to maintain sufficient contrast without OFF segments becoming visible.

Display Voltage and Temperature Compensation

These circuits allow control of the display peak voltage by bringing the bottom of the voltage divider resistor string out at pin 15. The simplest means for generating a display voltage suitable to a particular display is to connect a potentiometer from pin 15 to V_{SS} as shown in Figure 7. A potentiometer with a maximum value of 100 kΩ should give sufficient range of adjustment to suit most displays. This method for generating display voltage should be used only in applications where the temperature of the chip and display won't vary more than ±5°C (±9°F), as the resistors on the chip have a positive temperature coefficient, which will tend to increase the display peak voltage with an increase in temperature. The display voltage also depends on the power supply voltage, leading to tighter tolerances for wider temperature ranges.

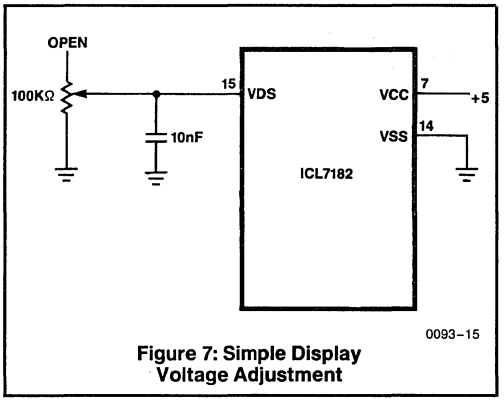
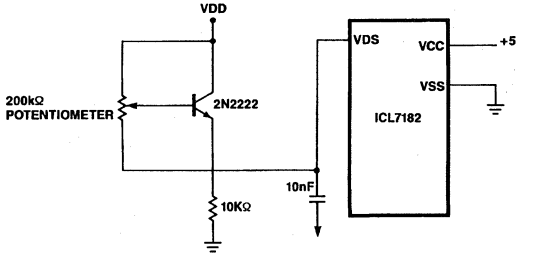


Figure 7: Simple Display Voltage Adjustment

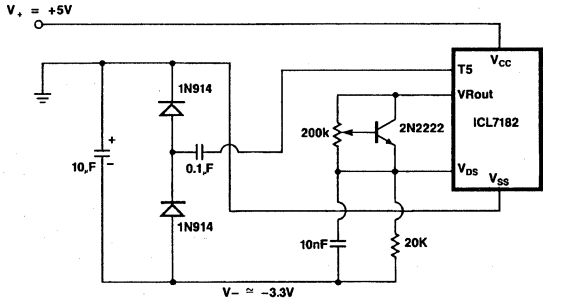
NOTE: All typical values have been characterized but are not tested.

Display Set Voltage (Continued)



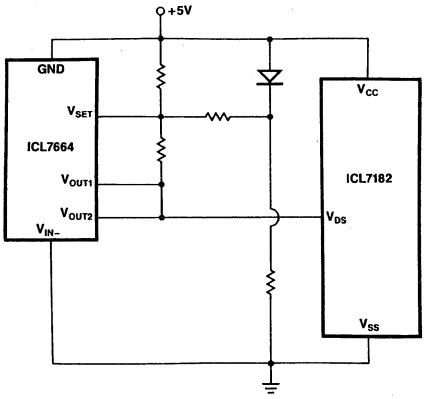
0093-16

Figure 8A: Temperature compensation and contrast adjustment for LCD fluid types which have visual threshold tempcos of ~ −10 mV/°C and operate with 3V to 4.0V.



0093-17

Figure 8B: Generating a negative supply from +5V to drive the display voltage pin below ground. This allows use of wide temperature LCD fluids which require peak-peak display drives of 3.5V to 7V. For LCD fluids which have threshold tempcos of ~ −8 mV/°C the collector of Q1 and 200 kΩ resistor should be tied to V_{ROUT}, for larger threshold tempcos of ~ −16 mV/°C this point should be tied to V_{CC}.



0093-18

Figure 9: Conceptually a flexible LCD contrast and temperature compensation using an ICL7664 can be designed in this manner. This technique allows adjusting the display voltage and temperature compensation independently.

NOTE: All typical values have been characterized but are not tested.

Display Layout

Custom displays developed for the ICL7182 need to be arranged such that the 8 segment lines serpentine across 13 backplanes. The annunciators and first eight data segments share a common backplane (BP1). An example layout is shown in Figure 10. This 1.3″ by 4.5″ display is available from Hamlin Inc. (part # 4464-363-921) for prototyping and evaluation.

Custom Display

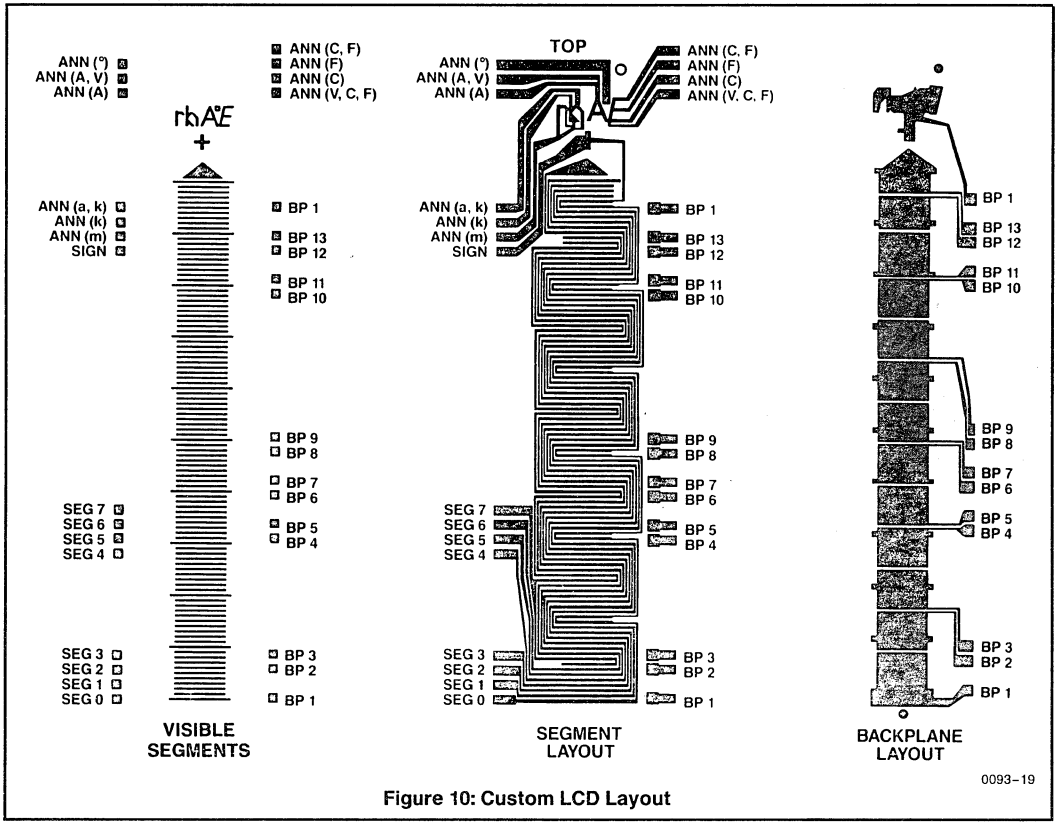
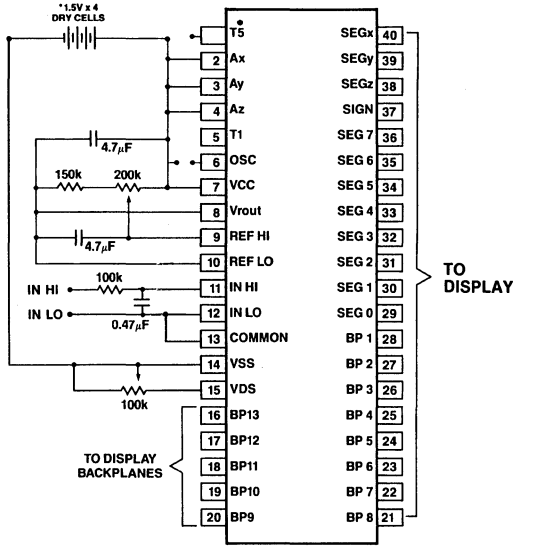


Figure 10: Custom LCD Layout

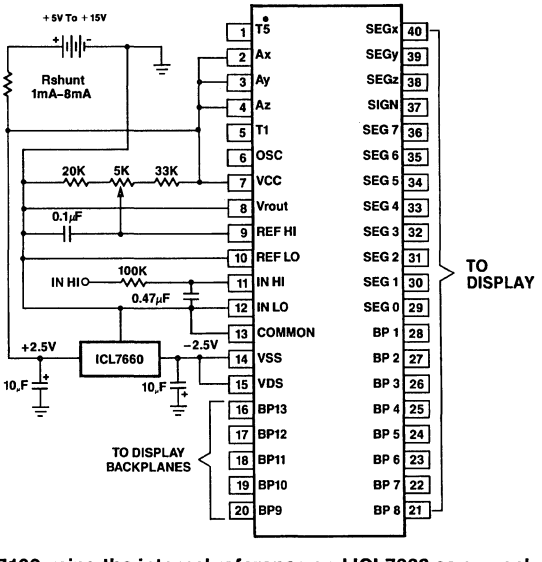
NOTE: All typical values have been characterized but are not tested.

APPLICATIONS



0093-20

Figure 11: 7182 using the internal reference. Values shown are for 1.00V full-scale, 1% adjustment sensitivity, 24 readings per second, 6V floating supply (four stacked 1.5V dry cells).*



0093-21

Figure 12: 7182 using the internal reference and ICL7660 as a supply regulator. This allows sensing ground reference bipolar inputs with a single + 5V supply. Values shown for 1.00V full-scale, 0.25% adjustment sensitivity.

NOTE: All typical values have been characterized but are not tested.

ICL7182

APPLICATIONS (Continued)

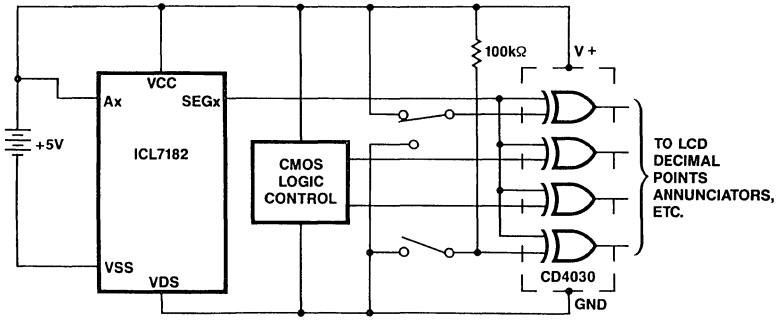


Figure 13: Using Exclusive 'OR' Gate for additional annunciator drivers.

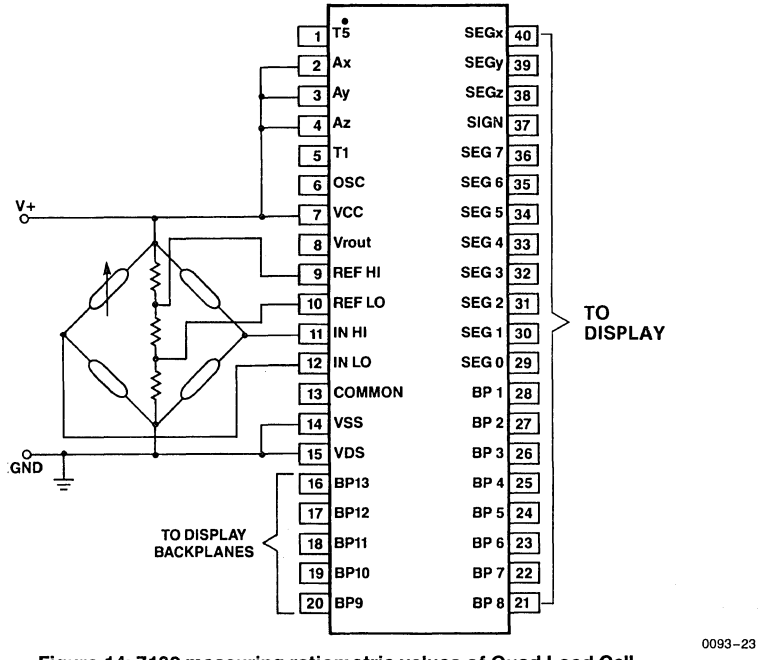
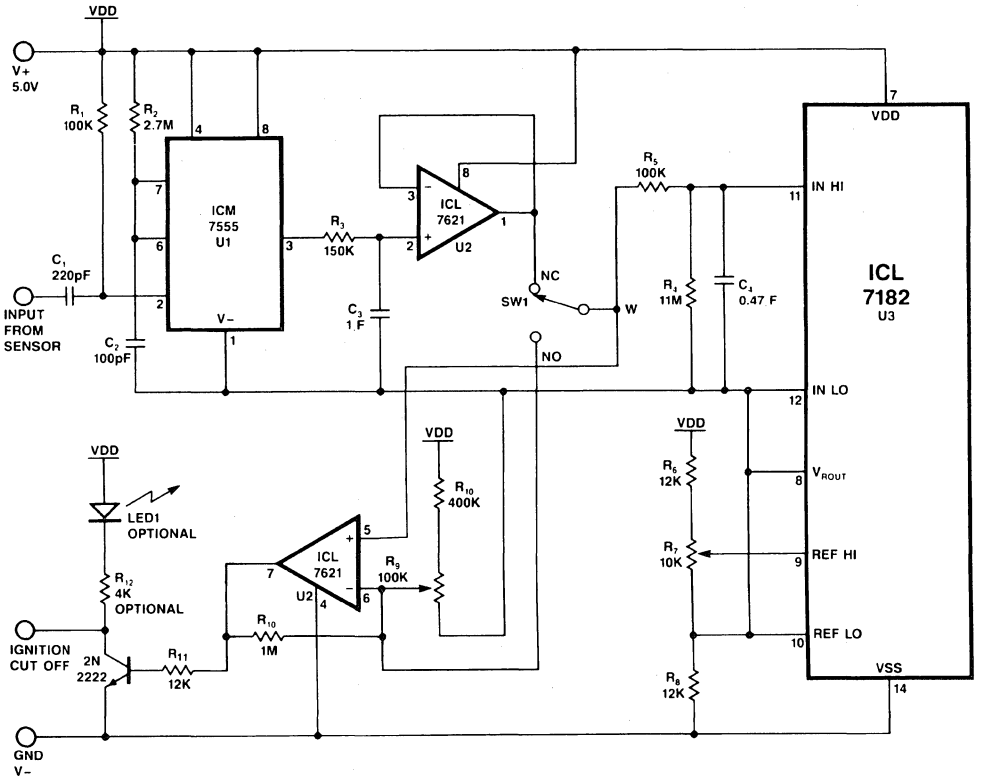


Figure 14: 7182 measuring ratiometric values of Quad Load Cell.
The resistor values within bridge are determined by the desired sensitivity.

NOTE: All typical values have been characterized but are not tested.

APPLICATIONS (Continued)



0093-24

$$\frac{V_O}{V_{IN}} = \frac{1/RC}{S + 1/R_3C_3}$$

$$fc = \frac{1}{2\pi R_3C_3}$$

SW1 Momentary
Switch SPST

V_{IN} = 264 mV @ 5000 RPM
4 Stroke V8

RPM	Hz	Period
600	10	100 ms
1000	16.7	60 ms
5000	83	12 ms
10,000	166.7	6 ms

No. of Cylinders	Events Per Cycle	Strokes Per Cycle
1	0.5	4
4	2	4
6	3	4
8	4	4

Figure 15: Tachometer with Set Point

NOTE: All typical values have been characterized but are not tested.

APPLICATIONS (Continued)

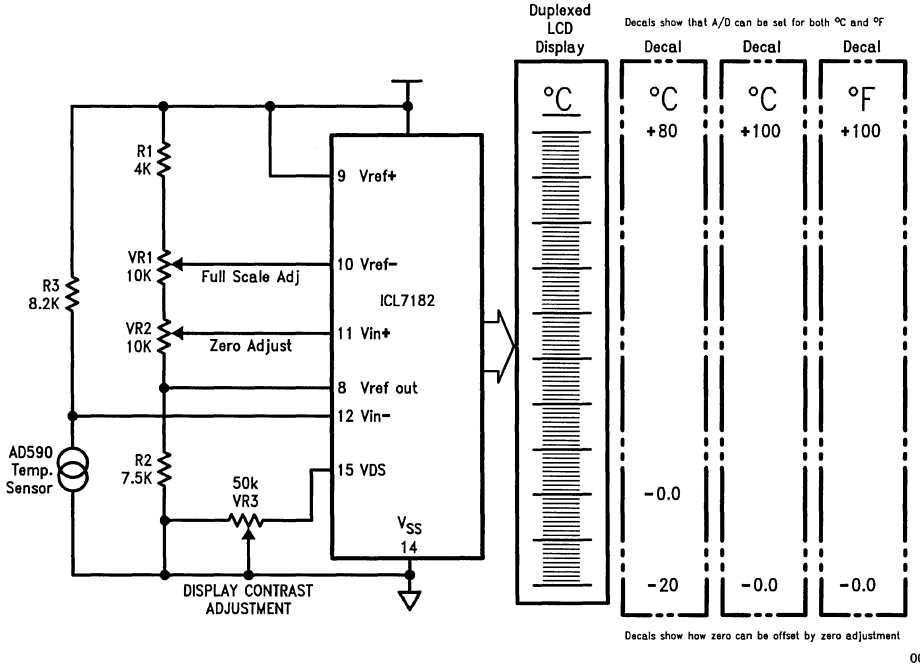


Figure 16: Basic digital thermometer, Celsius and Fahrenheit scales. This V_{DS} pin can be connected as shown in Figure 11.

NOTE: All typical values have been characterized but are not tested.

DATA ACQUISITION 3

A/D CONVERTERS INTEGRATING

HARRIS

HI-7159

PRELIMINARY

May 1991

Microprocessor Compatible 5½ Digit A/D Converter

Features

- ±200,000 Count A/D Converter
- 2V Full Scale Reading With 10μV Resolution
- 15 Conversions Per Second in 5½ Digit Mode
- 60 Conversions Per Second in 4½ Digit Mode
- Serial or Parallel Interface Modes
- Four Selectable Baud Rates
- Differential Analog Input
- Differential Reference Input
- Digital Autozero

Applications

- Weigh Scales
- Part Counting Scales
- Laboratory Instruments
- Process Control/Monitoring
- Energy Management
- Seismic Monitoring

Description

The Harris HI-7159 is a monolithic A/D converter that uses a unique dual slope technique which allows it to resolve input changes as small as 1 part in 200,000 (10μV) without the use of critical external components. Its digital autozeroing feature virtually eliminates zero drift over temperature. The device is fabricated in Harris' proprietary low noise BiMOS process, resulting in exceptional linearity and noise performance.

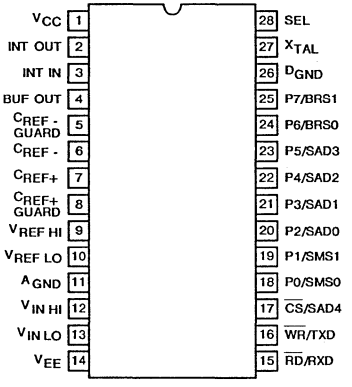
The HI-7159's resolution can be switched between a high resolution 200,000 count (5½ digit) mode, and a high speed 20,000 count (4½ digit) mode without any hardware modifications. In the 4½ digit uncompensated mode, speeds of 60 conversions per second can be achieved. The HI-7159 is designed to be easily interfaced with most microprocessors through either of its two serial and one parallel interface modes. In the serial modes, any one of four common Baud rates is available.

Ordering Information

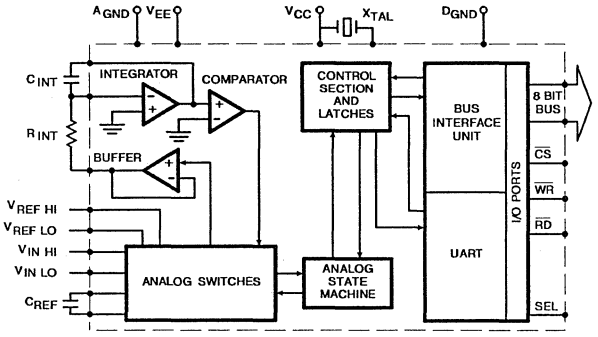
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI3-7159-5	0°C to +75°C	28 Pin Plastic DIP

Pinout

28 LEAD PLASTIC DIP
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **2471**

HARRIS SEMICONDUCTOR

ICL8052/ICL7104 and ICL8068/ICL7104
14/16-Bit μP-Compatible 2-Chip A/D Converter

GENERAL DESCRIPTION

The ICL7104, combined with the ICL8052 or ICL8068, forms a member of Harris' high performance A/D converter family. The ICL7104-16, performs the analog switching and digital function for a 16-bit binary A/D converter, with full three-state output, UART handshake capability, and other outputs for easy interfacing. The ICL7014-14 is a 14-bit version. The analog section, as with all Harris' integrating converters, provides fully precise Auto-Zero, Auto-Polarity (including ±0 null indication), single reference operation, very high input impedance, true input integration over a constant period for maximum EMI rejection, fully ratiometric operation, over-range indication, and a medium quality built-in reference. The chip pair also offers optional input buffer gain for high sensitivity applications, a built-in clock oscillator, and output signals for providing an external Auto-Zero capability in preconditioning circuitry, synchronizing external multiplexers, etc.

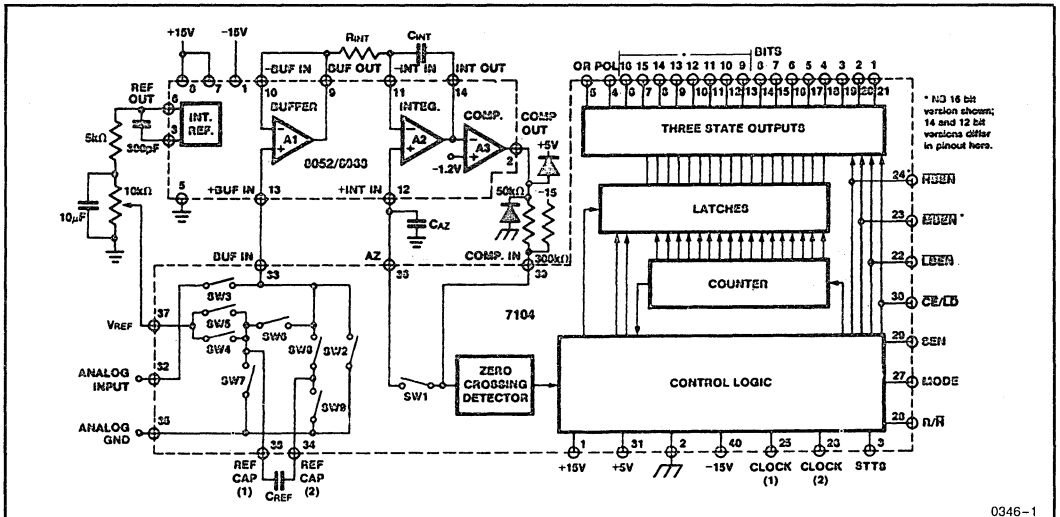
FEATURES

- 16/14 Bit Binary Three-State Latched Outputs Plus Polarity and Overrange
- Ideally Suited for Interface to UARTs and Microprocessors
- Conversion On Demand or Continuously
- Guaranteed Zero Reading for Zero Volts Input
- True Polarity at Zero Count for Precise Null Detection
- Single Reference Voltage for True Ratiometric Operation
- Onboard Clock and Reference
- Auto-Zero; Auto-Polarity
- Accuracy Guaranteed to 1 Count
- All Outputs TTL Compatible
- ±4V Analog Input Range
- Status Signal Available for External Sync, A/Z in Preamp, etc

ORDERING INFORMATION

Part Number	Temp. Range	Package
ICL8052CPD	0°C to +70°C	14-Pin Plastic DIP
ICL8052CDD	0°C to +70°C	14-Pin Ceramic DIP
ICL8052CJD	0°C to +70°C	14-Pin CERDIP
ICL8052ACPD	0°C to +70°C	14-Pin Plastic DIP
ICL8052ACDD	0°C to +70°C	14-Pin Ceramic DIP
ICL8052ACJD	0°C to +70°C	14-Pin CERDIP

Part Number	Temp. Range	Package
ICL8068CDD	0°C to +70°C	14-Pin Ceramic DIP
ICL8068ACDD	0°C to +70°C	14-Pin Ceramic DIP
ICL8068ACJD	0°C to +70°C	14-Pin CERDIP
ICL7104-14CPL	0°C to +70°C	40-Pin Plastic DIP
ICL7104-16CPL	0°C to +70°C	40-Pin Plastic DIP



0346-1

Figure 1: ICL8052A (8068A)/ICL7104 16/14 Bit A/D Converter Functional Diagram

NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL7104 and ICL8068/ICL7104

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (1) All Devices 500mW
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... 0°C to +70°C
Lead Temperature (Soldering, 10sec) ..... 300°C

ICL8052, 8068

Supply Voltage ..... ±18V
Differential Input Voltage (8068) ..... ±30V
(8052) ..... ±6V
Input Voltage (2) ..... ±15V
Output Short Circuit Duration,
All Outputs (3) ..... Indefinite

ICL7104

V^+ Supply (GND to V^+) 12V
V^{++} to V^- 32V
Positive Supply Voltage (GND to V^{++}) 17V
Negative Supply Voltage (GND to V^-) ..... −17V
Analog Input Voltage (Pins 32 – 39) (4) ..... V^{++} to V^-
Digital Input Voltage
(Pins 2 – 30) (5) ..... (GND−0.3V) to (V^+ +0.3V)

NOTE 1 Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.
2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.
4 Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.
5: Connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources not on the same power supply be applied to the ICL7104 before its power supply is established.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

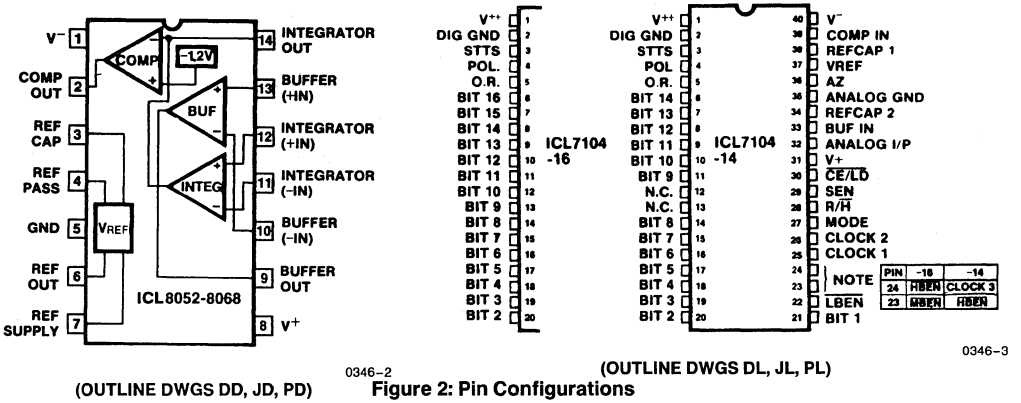


Figure 2: Pin Configurations

ICL7104 ELECTRICAL CHARACTERISTICS ($V^+ = +5V, V^{++} = +15V, V^- = -15V, T_A = 25°C$, $f_{CLOCK} = 200$ kHz)

Symbol	Characteristics		Test Conditions	Min	Typ	Max	Unit
I_{IN}	Clock Input	CLOCK 1	$V_{in} = +5V$ to 0V	±2	±7	±30	μA
I_{IN}	Comparator I/P	COMP IN (Note 1)	$V_{in} = 0V$ to +5V	−10	±0.001	+10	μA
I_{IH}	Inputs	MODE	$V_{IN} = +5V$	+1	+5	+30	μA
I_{IL}	with Pulldown		$V_{in} = 0V$	−10	±0.01	+10	μA
I_{IH}	Inputs	SEN, R/$\overline{H}$	$V_{in} = +5V$	−10	±0.01	+10	μA
I_{IL}	with Pullups	$\overline{LBEN}$, $\overline{MBEN}$, $\overline{HBEN}$, $\overline{CE/LD}$ (Note 2)	$V_{in} = 0V$	−30	−5	−1	μA

NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL7104 and ICL8068/ICL7104

ICL7104 ELECTRICAL CHARACTERISTICS

($V^+ = +5V$, $V^{++} = +15V$, $V^- = -15V$, $T_A = 25°C$, $f_{CLOCK} = 200$ kHz) (Continued)

Symbol	Characteristics		Test Conditions	Min	Typ	Max	Unit
V_{IH}	Input High Voltage	All Digital Inputs		2.5	2.0	-	V
V_{IL}	Input Low Voltage	All Digital Inputs			1.5	1.0	V
V_{OL}	Digital	$\overline{LBEN}$	$I_{OL} = 1.6mA$	—	0.27	.4	V
V_{OH}	Outputs	$\overline{MBEN}$ (16-only) (Note 3)	$I_{OH} = -10\mu A$		4.5	—	V
V_{OH}	Three-Stated On	$\overline{HBEN}$, $\overline{CE/LD}$, BIT n, POL, OR (Note 3)	$I_{OH} = -240\mu A$	2.4	3.5	—	V
I_{OL}	Digital Outputs Three-Stated Off	BIT n, POL, OR	$0 \le V_{out} \le V^+$	−10	±.001	+10	μA
V_{OL}	Non-Three State	STTS	$I_{OL} = 3.2mA$	—	0.3	.4	V
V_{OH}	Digital		$I_{OH} = -400\mu A$	2.4	3.3	—	V
V_{OL}	Output	CLOCK 2	$I_{OL} = 320\mu A$		0.5		V
V_{OH}			$I_{OH} = -320\mu A$		4.5		V
V_{OL}		CLOCK 3 (−14 ONLY)	$I_{OL} = 1.6mA$		0.27	.4	V
V_{OH}			$I_{OH} = -320\mu A$	2.4	3.5		V
$R_{DS(on)}$	Switch	Switch 1		—	25k		Ω
$R_{DS(on)}$		Switches 2,3		—	4k	20k	Ω
$R_{DS(on)}$		Switches 4,5,6,7,8,9		—	2k	10k	Ω
$I_{D(off)}$		Switch Leakage		—	15		pA
f_{CLOCK}	Clock	Clock Freq. (Note 4)		DC	200	400	kHz
I^+	Supply Currents	+5V Supply Current, All outputs high impedance	Freq. = 200kHz		200	600	μA
I^{++}		+15V Supply Current	Freq. = 200kHz		.3	1.0	mA
I^-		−15V Supply Current	Freq. = 200kHz		25	200	μA
V^+	Supply Voltage	Logic Supply	Note 5	4.0		+11.0	V
V^{++}	Range	Positive Supply		+10.0		+16.0	V
V^-		Negative Supply		−16.0		−10.0	V

NOTES: 1. This spec applies when not in Auto-Zero phase.
2. Apply only when these pins are inputs, i.e., the mode pin is low, and the 7104 is not in handshake mode.
3. Apply only when these pins are outputs, i.e., the mode pin is high or the 7104 is in handshake mode.
4. Clock circuit shown in Figs. 15 and 16.
5. V^+ must not be more positive than V^{++}

NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL7104 and ICL8068/ICL7104

ICL8068 ELECTRICAL CHARACTERISTICS (V_{SUPPLY} = ±15V unless otherwise specified)

Symbol	Characteristics	Test Conditions	8068			8068A			Unit
			Min	Typ	Max	Min	Typ	Max	
EACH OPERATIONAL AMPLIFIER									
V_{OS}	Input Offset Voltage	V_{CM} = 0V		20	65		20	65	mV
I_{IN}	Input Current (either input) (Note 1)	V_{CM} = 0V		175	250		80	150	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
	Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V_{CM} = ±2V		110			110		dB
A_V	Large Signal Voltage Gain	R_L = 50kΩ	20,000			20,000			V/V
SR	Slew Rate			6			6		V/μs
GBW	Unity Gain Bandwidth			2			2		MHz
I_{SC}	Output Short-Circuit Current			5			5		mA
COMPARATOR AMPLIFIER									
A_{VOL}	Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
$+V_O$	Positive Output Voltage Swing		+12	+13		+12	+13		V
$-V_O$	Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
VOLTAGE REFERENCE									
V_O	Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
R_O	Output Resistance			5			5		Ω
TC	Temperature Coefficient			50			40		ppm/°C
V_{SUPPLY}	Supply Voltage Range		±10		±16	±10		±16	V
I_{SUPPLY}	Supply Current Total				14		8	14	mA

ICL8052 ELECTRICAL CHARACTERISTICS (V_{SUPPLY} = ±15V unless otherwise specified)

Symbol	Characteristics	Test Conditions	8052			8052A			Unit
			Min	Typ	Max	Min	Typ	Max	
EACH OPERATIONAL AMPLIFIER									
V_{OS}	Input Offset Voltage	V_{CM} = 0V		20	75		20	75	mV
I_{IN}	Input Current (either input) (Note 1)	V_{CM} = 0V		5	50		2	10	pA
CMRR	Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
	Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V_{CM} = ±2V		110			110		dB
A_V	Large Signal Voltage Gain	R_L = 50kΩ	20,000			20,000			V/V
SR	Slew Rate			6			6		V/μs
GBW	Unity Gain Bandwidth			1			1		MHz
I_{SC}	Output Short-Circuit Current			20			20		mA
COMPARATOR AMPLIFIER									
A_{VOL}	Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
$+V_O$	Positive Output Voltage Swing		+12	+13		+12	+13		V
$-V_O$	Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V

NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL7104 and ICL8068/ICL7104

ICL8052 ELECTRICAL CHARACTERISTICS ($V_{SUPPLY} = \pm 15V$ unless otherwise specified) (Continued)

Symbol	Characteristics	Test Conditions	8052			8052A			Unit
			Min	Typ	Max	Min	Typ	Max	
VOLTAGE REFERENCE									
V_O	Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
R_O	Output Resistance			5			5		Ω
TC	Temperature Coefficient			50			40		ppm/°C
V_{SUPPLY}	Supply Voltage Range		±10		±16	±10		±16	V
I_{SUPPLY}	Supply Current Total			6	12		6	12	mA

NOTES: 1. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + R_{\theta JA}Pd$ where $R_{\theta JA}$ is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

2. This is the only component that causes error in dual-slope converter.

SYSTEM ELECTRICAL CHARACTERISTICS: ICL8068/7104 ($V^{++} = +15V$, $V^{+} = +5V$, $V^{-} = -15V$, $f_{CLOCK} = 200kHz$) (Note 4)

Characteristics	Test Conditions	8068A/7104-14			8068A/7104-16			Unit
		Min	Typ	Max	Min	Typ	Max	
Zero Input Reading	$V_{in} = 0.0V$ $V_{REF} = 2.000V$	−00000	±00000	+00000	−00000	±00000	+00000	Counts
Ratiometric Error(1)	$V_{in} = V_{REF} = 2.0000V$	−1	0	+1	−1	0	+1	LSB
Linearity over ±Full Scale (error of reading from best straight line)	$-4V \le V_{in} \le +4V$		0.5	1		0.5	1	LSB
Differential Linearity (difference between worst case step of adjacent counts and ideal step)	$-4V \le V_{in} \le +4V$		.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} = +V_{in} \cong 4V$		0.5	1		0.5	1	LSB
Noise (P-P value not exceeded 95% of time)	$V_{in} = 0V$ Full scale = 4.000V		2			2		μV
Leakage Current at Input (2)	$V_{in} = 0V$		100	165		100	165	pA
Zero Reading Drift	$V_{in} = 0V$ $0°C \le T_A \le 70°C$		0.5			0.5		μV/°C
Scale Factor Temperature (3) Coefficient	$V_{in} = +4V$ $0 \le T_A \le 50°C$ ext. ref. 0ppm/°C		2	5		2	5	ppm/°C

NOTE: All typical values have been characterized but are not tested.

SYSTEM ELECTRICAL CHARACTERISTICS: ICL8052/7104 ($V^{++} = +15V$, $V^{+} = +5V$, $V^{-} = -15V$, $f_{CLOCK} = 200kHz$) (Note 4)

Characteristics	Test Conditions	8052A/7104-14			8052A/7104-16			Unit
		Min	Typ	Max	Min	Typ	Max	
Zero Input Reading	$V_{in} = 0.0V$ $V_{REF} = 2.000V$	−00000	±00000	+00000	−00000	±00000	+00000	Counts
Ratiometric Error (3)	$V_{in} = V_{REF} = 2.0000V$	−1	0	+1	−1	0	+1	LSB
Linearity over ± Full Scale (error of reading from best straight line)	$-4V \le V_{in} \le +4V$		0.5	1		0.5	1	LSB
Differential Linearity (difference between worst case step of adjacent counts and ideal step)	$-4V \le V_{in} \le +4V$		.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} = +V_{in} \approx 4V$		0.5	1		0.5	1	LSB
Noise (P-P value not exceeded 95% of time)	$V_{in} = 0V$ Full scale = 4.000V		30			30		μV
Leakage Current at Input (2)	$V_{in} = 0V$		20	30		20	30	pA
Zero Reading Drift	$V_{in} = 0V$ $0 \le T_A \le 70°C$		0.5			0.5		μV/°C
Scale Factor Temperature Coefficient	$V_{in} = +4V$ $0 \le T_A \le 70°C$ (ext. ref. 0ppm/°C)		2			2		ppm/°C

NOTES: 1. Tested with low dielectric absorption integrating capacitor.

2. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + R_{\theta JA}Pd$ where $R_{\theta JA}$ is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

3. The temperature range can be extended to 70°C and beyond if the Auto-Zero and Reference capacitors are increased to absorb the high temperature leakage of the 8068. See note 2 above.

4. SYSTEM ELECTRICAL CHARACTERISTICS are not tested; for reference only.

NOTE: All typical values have been characterized but are not tested.

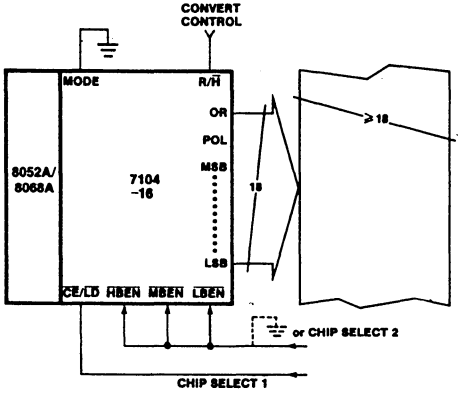


Figure 3: Full 18 Bit Three State Output

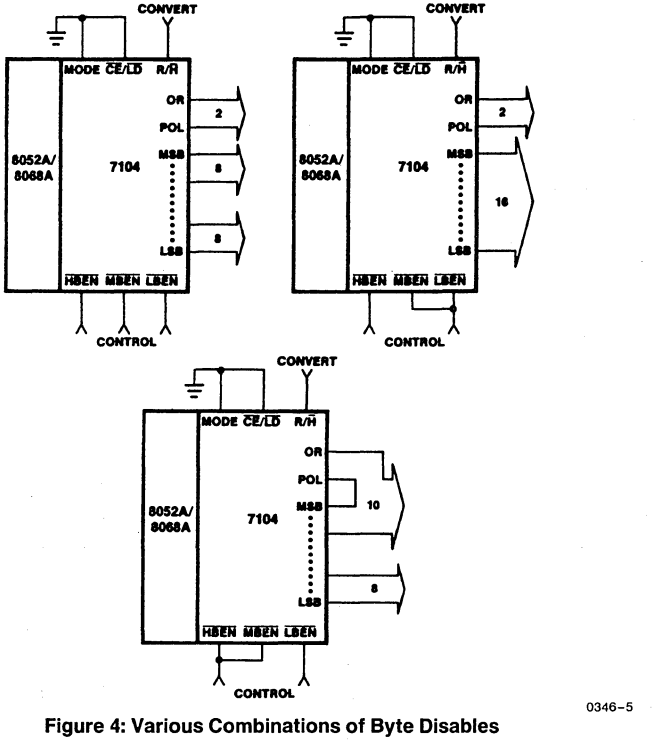


Figure 4: Various Combinations of Byte Disables

NOTE: All typical values have been characterized but are not tested.

AC CHARACTERISTICS ($V^{++} = +15V$, $V^{+} = +5V$, $V^{-} = -15V$)

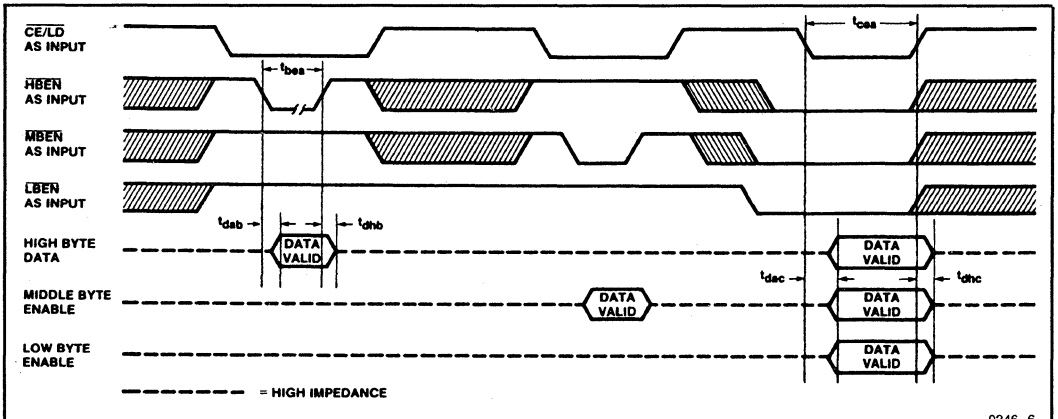


Figure 5: Direct Mode Timing Diagram

Table 1: Direct Mode Timing Requirements (Note: Not tested in production)

Symbol	Description	Min	Typ	Max	Unit
t_{bea}	$\overline{XBEN}$ Min. Pulse Width		300		ns
t_{dab}	Data Access Time from $\overline{XBEN}$		300		
t_{dhb}	Data Hold Time from $\overline{XBEN}$		200		
t_{cea}	$\overline{CE/LD}$ Min. Pulse Width		350		
t_{dac}	Data Access Time from $\overline{CE/LD}$		350		
t_{dhc}	Data Hold Time from $\overline{CE/LD}$		280		
t_{cwh}	CLOCK 1 High Time		1000		

Table 2: Handshake Timing Requirements (Note: Not tested in production.)

Name	Description	Min	Typ	Max	Unit
t_{mw}	MODE Pulse (minimum)		20		ns
t_{sm}	MODE pin set-up time		−150		
t_{me}	MODE pin high to low Z $\overline{CE/LD}$ high delay		200		
t_{mb}	MODE pin high to $\overline{XBEN}$ low Z (high) delay		200		
t_{cel}	CLOCK 1 high to $\overline{CE/LD}$ low delay		700		
t_{ceh}	CLOCK 1 high to $\overline{CE/LD}$ high delay		600		
t_{cbl}	CLOCK 1 high to $\overline{XBEN}$ low delay		900		
t_{cbh}	CLOCK 1 high to $\overline{XBEN}$ high delay		700		
t_{cdh}	CLOCK 1 high to data enabled delay		1100		
t_{cdl}	CLOCK 1 low to data disabled delay		1100		
t_{ss}	Send ENable set-up time		−350		
t_{cbz}	CLOCK 1 high to $\overline{XBEN}$ disabled delay		2000		
t_{cez}	CLOCK 1 high to $\overline{CE/LD}$ disabled delay		2000		
t_{cwh}	CLOCK 1 High Time	1250	1000		

NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL7104 and ICL8068/ICL7104

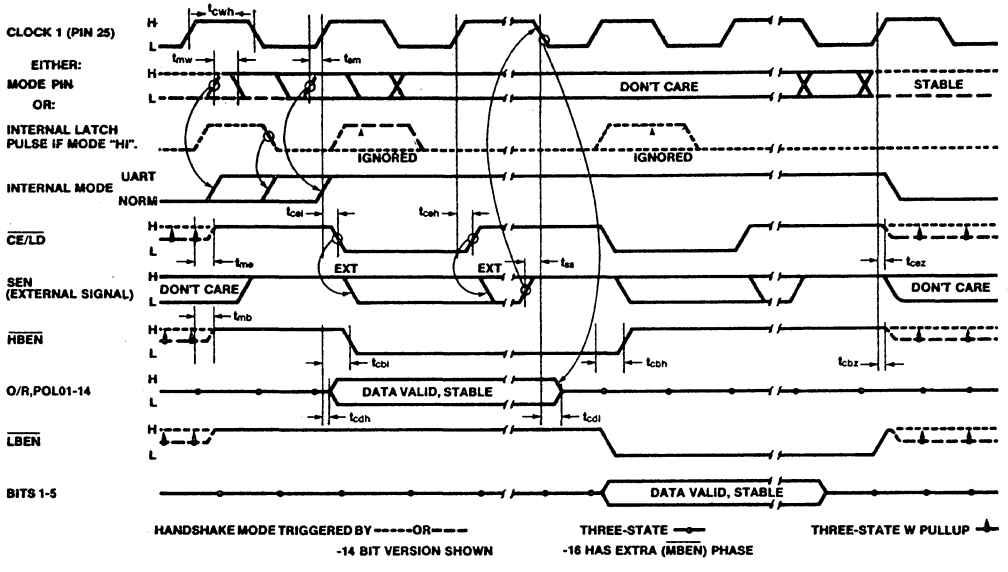


Figure 6: Handshake Mode Timing Diagram

NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL7104 and ICL8068/ICL7104

Table 3: Pin Descriptions

Pin	Symbol	Option	Description
1	V^{++}		Positive Supply Voltage Nominally +15V
2	GND		Digital Ground .0V, ground return
3	STTS		STaTuS output. HI during Integrate and Deintegrate until data is latched. LO when analog section is in Auto-Zero configuration.
4	POL		POLarity. Three-state output. HI for positive input.
5	OR		OverRange. Three-state output.
6	BIT 16 BIT 14	−16 −14	(Most significant bit)
7	BIT 15 BIT 13	−16 −14	Data Bits, Three-state outputs. See Table 4 for format of $\overline{\text{EN}}$ables and bytes. HIGH = true
8	BIT 14 BIT 12	−16 −14	
9	BIT 13 BIT 11	−16 −14	
10	BIT 12 BIT 10	−16 −14	
11	BIT 11 BIT 9	−16 −14	
12	BIT 10 nc	−16 −14	
13	BIT 9 nc	−16 −14	
14	BIT 8		
15	BIT 7		
16	BIT 6		
17	BIT 5		
18	BIT 4		
19	BIT 3		
20	BIT 2		
21	BIT 1		Least significant bit.
22	$\overline{\text{LBEN}}$		$\overline{\text{L}}$ow $\overline{\text{B}}$yte $\overline{\text{EN}}$able. If not in handshake mode (see pin 27) when LO (with $\overline{\text{CE}}/\overline{\text{LD}}$, pin 30) activates low-order byte outputs, BITS 1-8 When in handshake mode (see pin 27), serves as a low-byte flag output. See Figures 12, 13, 14.
23	$\overline{\text{MBEN}}$ $\overline{\text{HBEN}}$	−16 −14	$\overline{\text{M}}$id $\overline{\text{B}}$yte $\overline{\text{EN}}$able. Activates BITS 9-16, see $\overline{\text{LBEN}}$ (pin 22) $\overline{\text{H}}$igh $\overline{\text{B}}$yte $\overline{\text{EN}}$able. Activates BITS 9-14, POL, OR, see $\overline{\text{LBEN}}$ (pin 22)
24	$\overline{\text{HBEN}}$ CLOCK3	−16 −14	$\overline{\text{H}}$igh $\overline{\text{B}}$yte $\overline{\text{EN}}$able. Activates POL, OR, see $\overline{\text{LBEN}}$ (pin 22). RC oscillator pin. Can be used as clock output.
25	CLOCK1		Clock input. External clock or ocsillator.
26	CLOCK2		Clock output. Crystal or RC oscillator.
27	MODE		Input LO; Direct output mode where $\overline{\text{CE}}/\overline{\text{LD}}$, $\overline{\text{HBEN}}$, $\overline{\text{MBEN}}$ and $\overline{\text{LBEN}}$ act as inputs directly controlling byte outputs. If pulsed HI causes immediate entry into handshake mode (see Figure 14). If HI, enables $\overline{\text{CE}}/\overline{\text{LD}}$, $\overline{\text{HBEN}}$, $\overline{\text{MBEN}}$, and $\overline{\text{LBEN}}$ as outputs. Handshake mode will be entered and data output as in Figures 12 & 13 at conversion completion.
28	R/$\overline{\text{H}}$		Run/$\overline{\text{Hold}}$: Input HI-conversions continously performed every $2^{17}(-16)$ or $2^{15}(-14)$ clock pulses. Input LO-conversion in progress completed, converter will stop in Auto-Zero 7 counts before input integrate.
29	SEN		Send-ENable: Input controls timing of byte transmission in handshake mode. HI indicates 'send'.
30	$\overline{\text{CE}}/\overline{\text{LD}}$		$\overline{\text{C}}$hip-$\overline{\text{E}}$nable/$\overline{\text{L}}$oa$\overline{\text{D}}$. With MODE (pin 27) LO, $\overline{\text{CE}}/\overline{\text{LD}}$ serves as a master output enable; when HI, the bit outputs and POL, OR are disabled. With MODE HI, pin serves as a $\overline{\text{L}}$oa$\overline{\text{D}}$ strobe (−ve going) used in handshake mode. See Figures 12 & 13.
31	V^{+}		Positive Logic Supply Voltage. Nominally +5V.
32	AN I/P		ANalog InPut. High Side.
33	BUF IN		BUFfer INput to analog chip (ICL8052 or ICL8068)
34	REFCAP2		REFerence CAPacitor (negative side)
35	AN.GND.		ANalog GrouND. Input low side and reference low side.
36	A-Z		Auto-Zero node.
37	VREF		Voltage REFerence input (positive side).
38	REFCAP1		REFerence CAPacitor (positive side).
39	COMP-IN		COMParator INput from 8052/8068
40	V^{-}		Negative Supply Voltage. Nominally −15V.

NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL7104 and ICL8068/ICL7104

Table 4: Three-State Byte Formats and $\overline{\text{EN}}$able Pins

	$\overline{\text{CE/LD}}$																
	$\overline{\text{HBEN}}$		$\overline{\text{MBEN}}$								$\overline{\text{LBEN}}$							
7104-16	POL	O/R	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
			$\overline{\text{HBEN}}$								$\overline{\text{LBEN}}$							
7104-14	POL	O/R	B14	B13	B12	B11	B10	B9			B8	B7	B6	B5	B4	B3	B2	B1

Figure 1 shows the functional block diagram of the operating system. For a detailed explanation, refer to Figure 7 below.

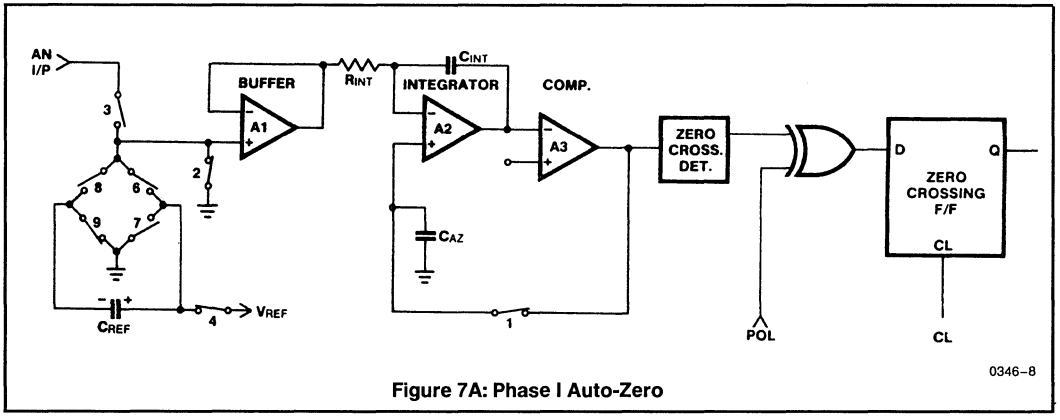


Figure 7A: Phase I Auto-Zero

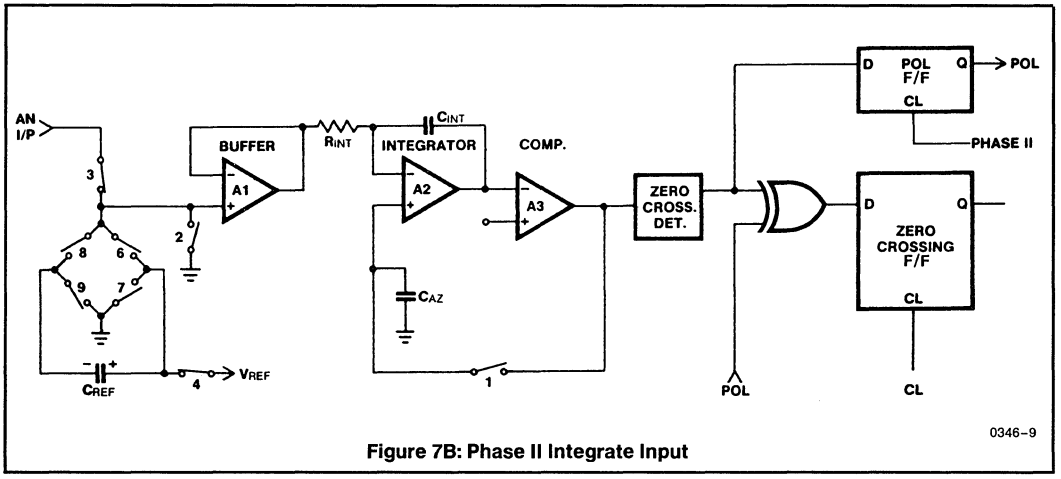


Figure 7B: Phase II Integrate Input

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

Analog Section

Figure 7 shows the equivalent Circuit of the Analog Section of both the ICL7104/8052 and the ICL7104/8068 in the 3 different phases of operation. If the Run/$\overline{\text{Hold}}$ pin is left open or tied to V+, the system will perform conversions at a rate determined by the clock frequency: 131,072 for — 16 and 32,368 for — 14 clock periods per cycle (see Figure 9 conversion timing).

Auto-Zero Phase I Figure 7A

During Auto-Zero, the input of the buffer is shorted to analog ground thru switch 2, and switch 1 closes a loop around the integrator and comparator. The purpose of the loop is to charge the Auto-Zero capacitor until the integrator output no longer changes with time. Also, switches 4 and 9 recharge the reference capacitor to V_{REF}.

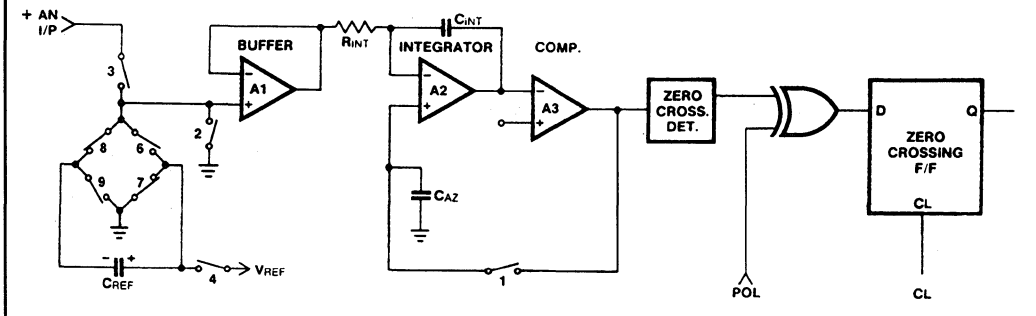


Figure 7C: Phase III + Deintegrate

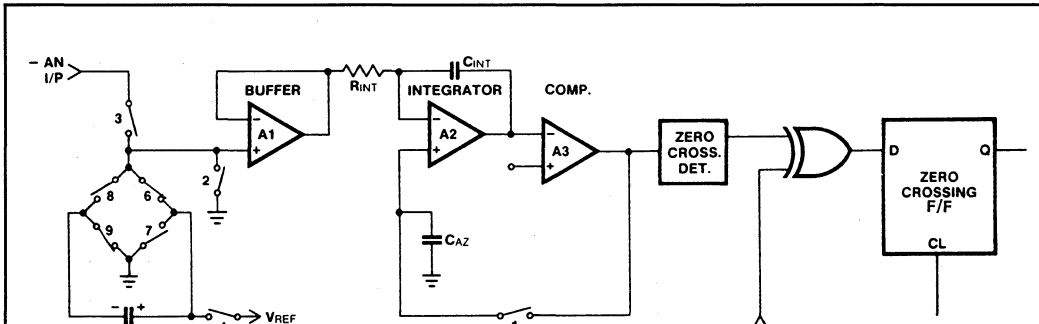


Figure 7D: Phase III − Deintegrate

NOTE: All typical values have been characterized but are not tested.

Input Integrate Phase II Figure 7B

During input integrate the Auto-Zero loop is opened and the analog input is connected to the buffer input thru switch 3. (The reference capacitor is still being charged to V_{REF} during this time.) If the input signal is zero, the buffer, integrator and comparator will see the same voltage that existed in the previous state (Auto-Zero). Thus the integrator output will not change but will remain stationary during the entire Input Integrate cycle. If V_{IN} is not equal to zero, an unbalanced condition exists compared to the Auto-Zero phase, and the integrator will generate a ramp whose slope is proportional to V_{IN}. At the end of this phase, the sign of the ramp is latched into the polarity F/F.

Deintegrate Phase III Figure 7C & D

During the Deintegrate phase, the switch drive logic uses the output of the polarity F/F in determining whether to close switches 6 and 9 or 7 and 8. If the input signal was positive, switches 7 and 8 are closed and a voltage which is V_{REF} more negative than during Auto-Zero is impressed on the buffer input. Negative inputs will cause $+V_{REF}$ to be applied to the buffer input via switches 6 and 9. Thus, the reference capacitor generates the equivalent of a (+) reference or a (−) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to the zero-crossing point established in Phase I. The time, or number of counts, required to do this is proportional to the input voltage. Since the Deintegrate phase can be twice as long as the Input integrate phase, the input voltage required to give a full scale reading $= 2V_{REF}$.

NOTE: Once a zero crossing is detected, the system automatically reverts to Auto-Zero phase for the leftover Deintegrate time (unless Run/$\overline{\text{Hold}}$ is manipulated, see Run/$\overline{\text{Hold}}$ Input in detailed description, digital section).

Buffer Gain

At the end of the auto-zero interval, the instantaneous noise voltage on the auto-zero capacitor is stored, and subtracts from the input voltage while adding to the reference voltage during the next cycle. The result is that this noise voltage effectively is somewhat greater than the input noise voltage of the buffer itself during integration. By introducing some voltage gain into the buffer, the effect of the auto-zero noise (referred to the input) can be reduced to the level of the inherent buffer noise. This generally occurs with a buffer gain of between 3 and 10. Further increase in buffer gain merely increases the total offset to be handled by the auto-zero loop, and reduces the available buffer and integrator swings, without improving the noise performance of the system. The circuit recommended for doing this with the ICL8068/ICL7104 is shown in Figure 8. With careful layout, the circuit shown can achieve effective input noise voltages on the order of 1 to 2 μV, allowing full 16-bit use with full scale inputs of as low as 150mV. Note that at this level, thermoelectric EMFs between PC boards, IC pins, etc., due to local temperature changes can be very troublesome. For further discussion, see App. Note A030.

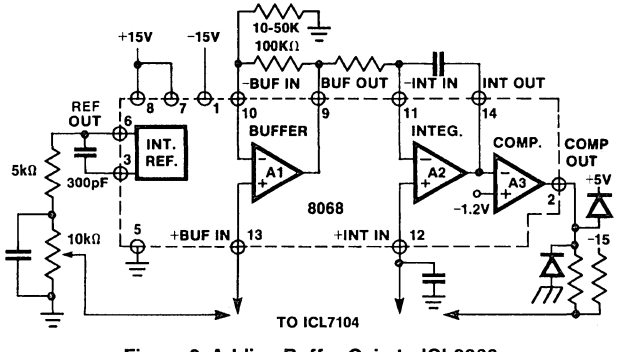
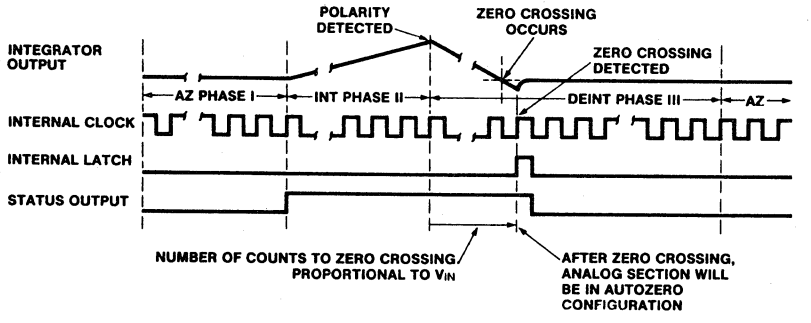


Figure 8: Adding Buffer Gain to ICL8068

Table 5: Typical Component Values ($V^{++} = +15V$, $V^{+} = 5V$, $V^{-} = -15V$, $f_{CLOCK} = 200kHz$)

ICL8052/8068 with	ICL7104-16			ICL7104-14		Unit
Full scale V_{IN}	200	800	4000	100	4000	mV
Buffer Gain	10	1	1	10	1	V/V
R_{INT}	100	43	200	47	180	kΩ
C_{INT}	.33	.33	.33	0.1	0.1	μF
C_{AZ}	1.0	1.0	1.0	1.0	1.0	μF
C_{ref}	10	1.0	1.0	10	1.0	μF
V_{REF}	100	400	2000	50	2000	mV
Resolution	3.1	12	61	6.1	244	μV

NOTE: All typical values have been characterized but are not tested.



	COUNTS		
	PHASE I	PHASE II	PHASE III
−16	32768	32768	65536
−14	8192	8192	16384

Figure 9: Conversion Timing

ICL8052 vs ICL8068

The ICL8052 offers significantly lower input leakage currents than the ICL8068, and may be found preferable in systems with high input impedances. However, the ICL8068 has substantially lower noise voltage, and for systems where system noise is a limiting factor, particularly in low signal level conditions, will give better performance.

COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. This current should be small compared to the output short circuit current such that thermal effects are kept to a minimum and linearity is not affected. Values of 5 to 40μA give good results with a nominal of 20μA. The exact value may be chosen by

$$R_{INT} = \frac{\text{full scale voltage}^*}{20\mu A}$$

*Note: If gain is used in the buffer amplifier then —

$$R_{INT} = \frac{\text{(Buffer gain) (full scale voltage)}}{20\mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor is selected to give 9 volt swing for full scale inputs. This is a compromise between possibly saturating the integrator (at +14 volts) due to tolerance build-up between the resistor, capacitor and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. In general, the value of C_{INT} is given by

$$C_{INT} = \frac{\left[\begin{matrix}\text{(32768 for } -16\text{)} \\ \text{(8192 for } -14\text{)}\end{matrix}\right] \times 20\mu A \times \text{clock period}}{\text{Integrator Output Voltage Swing}}$$

A very important characteristic of the integrating capacitor is that it have low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale (100 . . . 000) and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

Note: When gain is used in the buffer amplifier the reference capacitor should be substantially larger than the auto-zero capacitor. As a rule of thumb, the reference capacitor should be approximately the gain times the value of the auto-zero capacitor. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

NOTE: All typical values have been characterized but are not tested.

Reference Voltage

The analog input required to generate a full scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7104 at 16 bits is one part in 65536, or 15.26ppm. Thus, if the reference has a temperature coefficient of 50ppm/°C (on board reference) a temperature change of ⅓°C will introduce a one-bit absolute error. For this reason, it is recommended that an external high quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

DETAILED DESCRIPTION

Digital Section

The digital section includes the clock oscillator circuit, a 16 or 14 bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic and UART handshake logic, as shown in the Block Diagram Figure 10 (16 bit version shown).

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined under "ICL7104 Electrical Characteristics". For minimum power consumption, all inputs should swing from GND (low) to V+ (high). Inputs driven from TTL gates should have 3 – 5kΩ pullup resistors added for maximum noise immunity.

MODE Input

The MODE input is used to control the output mode of the converter. When the MODE pin is connected to GND or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in three bytes for the 7104-16 or two bytes for the 7104-14 then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

STaTuS Output

During a conversion cycle, the STaTuS output goes high at the beginning of Input Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 9 for details of this timing. This signal may be used as a "data valid" flag (data never changes while STaTuS is low) to drive interrupts, or for monitoring the status of the converter.

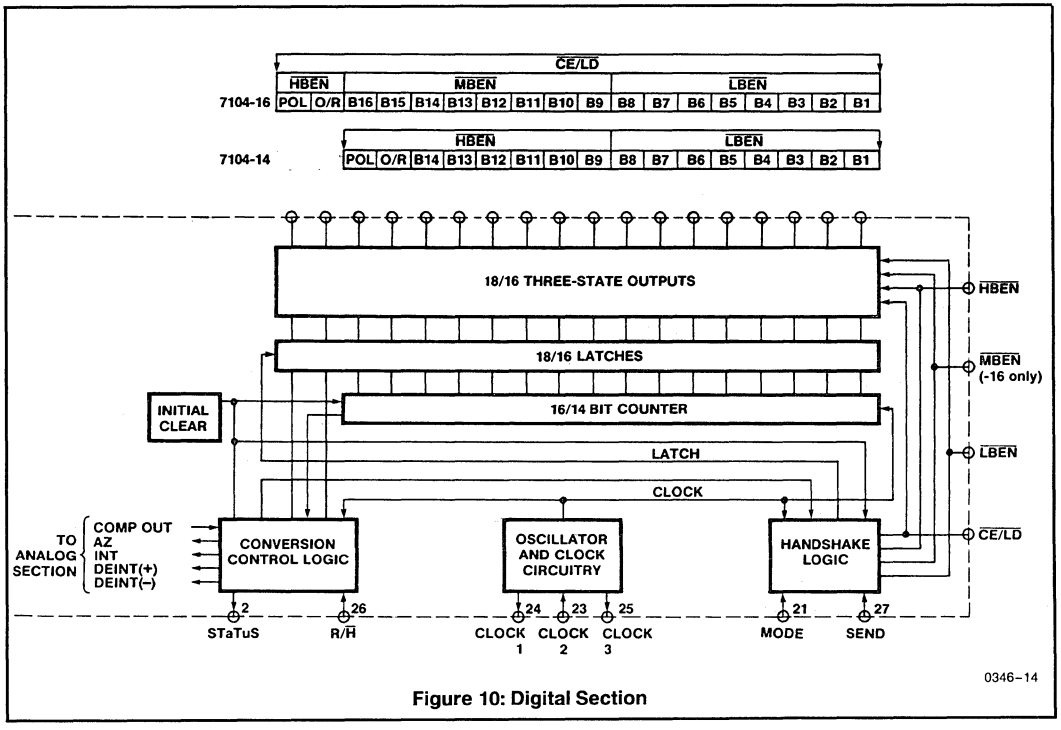


Figure 10: Digital Section

NOTE: All typical values have been characterized but are not tested.

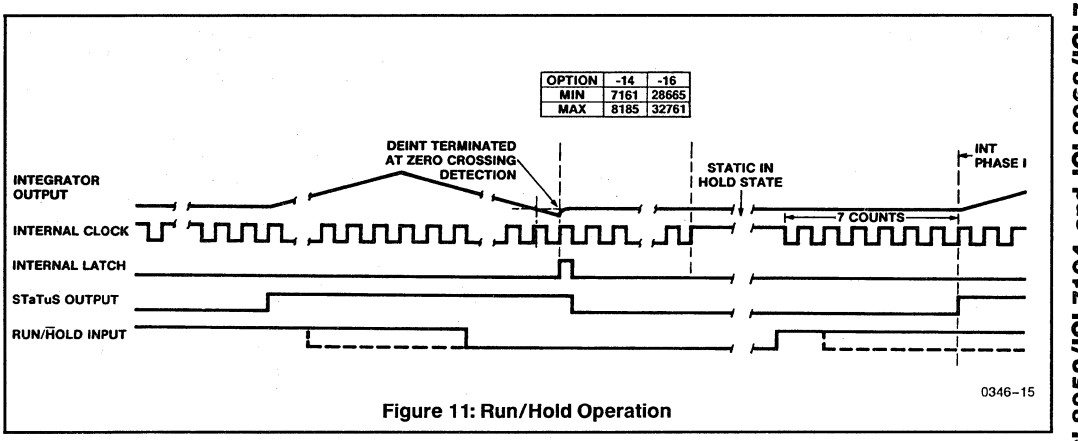


Figure 11: Run/Hold Operation

Run/Hold Input

When the Run/Hold input is connected to V+ or left open (this input has a pullup resistor to ensure a high level when the pin is left open), the circuit will continuously perform conversion cycles, updating the output latches at the end of every Deintegrate (Phase III) portion of the conversion cycle (See Figure 9). (See under "Handshake Mode" for exception.) In this mode of operation, the conversion cycle will be performed in 131,072 for 7104-16 and 32768 for 7104-14 clock periods, regardless of the resulting value.

If Run/Hold goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to eliminate the time spent in Deintegrate after the zero-crossing. If Run/Hold stays or goes low, the converter will ensure a minimum Auto-Zero time, and then wait in Auto-Zero until the Run/Hold input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STaTuS output will go high) seven clock periods after the high level is detected at Run/Hold. See Figure 11 for details.

Using the Run/Hold input in this manner allows an easy "convert on demand" interface to be used. The converter may be held at idle in Auto-Zero with Run/Hold low. When Run/Hold goes high the conversion is started, and when the STaTuS output goes low the new data is valid (or transferred) to the UART — see Handshake Mode). Run/Hold may now go low terminating Deintegrate and ensuring a minimum Auto-Zero time before stopping to wait for the next conversion. Alternately, Run/Hold can be used to minimize conversion time by ensuring that it goes low during Deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the Run/Hold input can be provided by connecting it to the CLOCK3 (-14), CLOCK2 (-16) Output. In this mode the conversion time is dependent on the input value measured. Also refer to Harris Application Bulletin A030 for a discussion of the effects this will have on Auto-Zero performance.

If the Run/Hold input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for Run/Hold to go high. As above, Integrate (Phase II) begins seven clock periods after the high level is detected.

Direct Mode

When the MODE pin is left at a low level, the data outputs [bits 1 through 8 low order byte, see Table 4 for format of middle (-16) and high order bytes] are accessible under control of the byte and chip ENable terminals as inputs. These ENable inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip ENable input is low, taking a byte ENable input low will allow the outputs of that byte to become active (three-stated on). This allows a variety of parallel data accessing techniques to be used. The timing requirements for these outputs are shown under AC Characteristics and Table 1.

It should be noted that these control inputs are asynchronous with respect to the converter clock — the data may be accessed at any time. Thus it is possible to access the data while it is being updated, which could lead to scrambled data. Synchronizing the access of data with the conversion cycle by monitoring the STaTuS output will prevent this. Data is never updated while STaTuS is low. Also note the potential bus conflict described under "Initial Clear Circuitry".

Handshake Mode

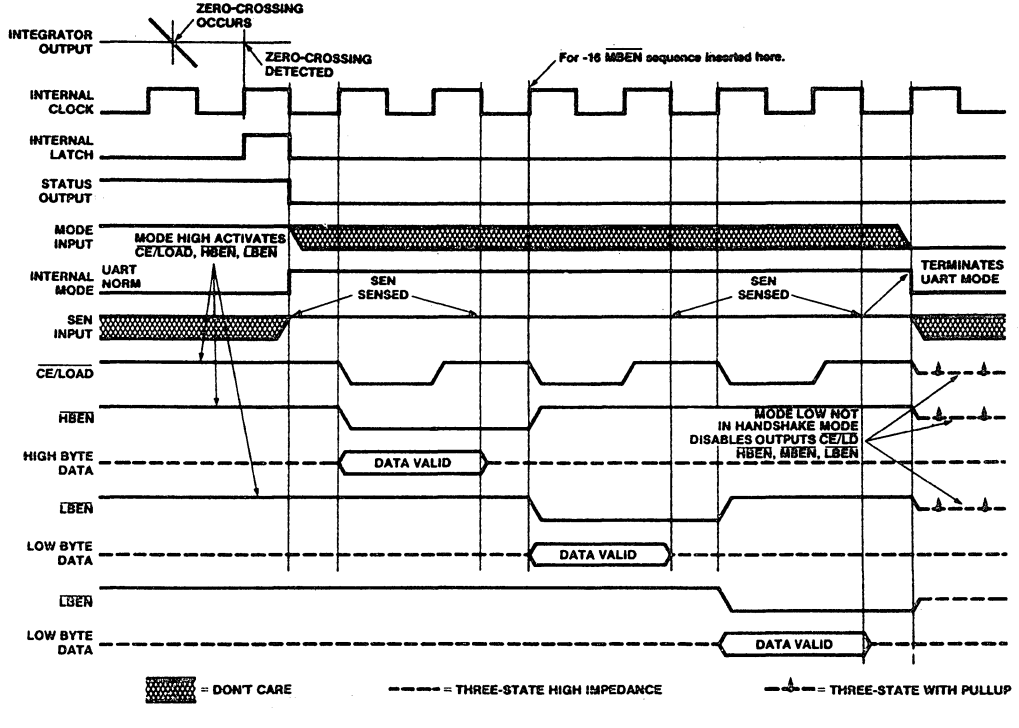
The handshake output mode is provided as an alternative means of interfacing the ICL7104 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte ENable inputs. This mode is specifically designed to allow a direct interface between the ICL7104 and industry-standard UARTs (such as the Harris CMOS UARTs, IM6402/3) with no external logic required. When triggered into the handshake mode, the ICL7104 provides all the control and flag signals necessary to sequence the three (ICL7106-16) or two (ICL7104-14) bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission to minimize the number of lines to the central controlling processor.

NOTE: All typical values have been characterized but are not tested.

Entry into the handshake mode will occur if either of two conditions are fulfilled; first, if new data is latched (i.e. a conversion is completed) while MODE pin (pin 27) is high, in which case entry occurs at the end of the latch cycle; or secondly, if the MODE pin goes from low to high, when entry will occur immediately (if new data is being latched, entry is delayed to the end of the latch cycle). While in the handshake mode, data latching is inhibited, and the MODE pin is ignored. (Note that conversion cycles will continue in the normal manner). This allows versatile initiation of handshake operation without danger of false data generation; if the MODE pin is held high, every conversion (other than those completed during handshake operations) will start a new handshake operation, while if the MODE pin is pulsed high, handshake operations can be obtained "on demand."

When the converter enters the handshake mode, or when the MODE input is high, the chip and byte $\overline{\text{EN}}$able terminals become TTL-compatible outputs which provide the control signals for the output cycle. The Send $\overline{\text{EN}}$able pin (SEN) (pin 29) is used as an indication of the ability of the external device to receive data. The condition of the line is sensed once every clock pulse, and if it is high, the next (or first) byte is enabled on the next rising CLOCK 1 (pin 25) clock edge, the corresponding byte $\overline{\text{EN}}$able line goes low, and the Chip $\overline{\text{EN}}$able/LoaD pin (pin 30) (CE/LD) goes low for one full clock pulse only, returning high.

On the next falling CLOCK 1 clock pulse edge, if SEN remains high, or after it goes high again, the byte output lines will be put in the high impedance state (or three-stated off). One half pulse later, the byte $\overline{\text{EN}}$able pin will be cleared high, and (unless finished) the $\overline{\text{CE}}$/$\overline{\text{LD}}$ and the next byte $\overline{\text{EN}}$able pin will go low. This will continue until all three (2 in the case of the 14 bit device) bytes have been sent. The bytes are individually put into the low impedance state i.e.: three-stated on during most of the time that their byte $\overline{\text{EN}}$able pin is (active) low. When receipt of the last byte has been acknowledged by a high SEN, the handshake mode will be cleared, re-enabling data latching from conversions, and recognizing the condition of the MODE pin again. The byte and chip ENable will be three-stated off, if MODE is low, but held high by their (weak) pullups. These timing relationships are illustrated in Figure 12, 13, and 14, and Table 2.



0346-16

Figure 12: Handshake with SEN Held Positive

NOTE: All typical values have been characterized but are not tested.

Figure 12 shows the sequence of the output cycle with SEN held high. The handshake mode (Internal MODE high) is entered after the data latch pulse (since MODE remains high the $\overline{CE}/\overline{LD}$, $\overline{LBEN}$, $\overline{MBEN}$ and $\overline{HBEN}$ terminals are active as outputs). The high level at the SEN input is sensed on the same high to low internal clock edge. On the next to high internal clock edge, the $\overline{CE}/\overline{LD}$ and the $\overline{HBEN}$ outputs assume a low level and the high-order byte (POL and OR, and except for -16, Bits 9 – 14) outputs are enabled. The $\overline{CE}/\overline{LD}$ output remains low for one full internal clock period only, the data outputs remain active for 1-½ internal clock periods, and the high byte $\overline{EN}$able remains low for two clock periods. Thus the $\overline{CE}/\overline{LD}$ output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte $\overline{EN}$able as an output may be used as a byte identification flag. With SEN remaining high the converter completes the output cycle using $\overline{CE}/\overline{LD}$, $\overline{MBEN}$ and $\overline{LBEN}$ while the remaining byte outputs (see Table 4) are activated. The handshake mode is terminated when all bytes are sent (3 for -16, 2 for -14).

Figure 13 shows an output sequence where the SEN input is used to delay portions of the sequence, or handshake, to ensure correct data transfer. This timing diagram shows the relationships that occur using an industry-standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEN input to the ICL7104 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{CE}/\overline{LD}$ terminal of the ICL7104 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

Assuming the UART Transmitter Buffer Register is empty, the SEN input will be high when the handshake mode is entered after new data is stored. The $\overline{CE}/\overline{LD}$ and $\overline{HBEN}$ terminals will go low after SEN is sensed, and the high order byte outputs become active. When $\overline{CE}/\overline{LD}$ goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the $\overline{HBEN}$ output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next ICL7104 internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the $\overline{HBEN}$ output returns high. At the same time, the $\overline{CE}/\overline{LD}$ and $\overline{MBEN}$ (-16) or $\overline{LBEN}$ outputs go low, and the corresponding byte outputs become active. Similarly, when the $\overline{CE}/\overline{LD}$ returns high at the end of one clock period, the enabled data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7104 internal clock high to low edge, disabling the data outputs. For the 16 bit device, the sequence is repeated for $\overline{LBEN}$. One-half internal clock later, the handshake mode will be cleared, and the chip and byte $\overline{EN}$able terminals return high and stay active (as long as MODE stays high).

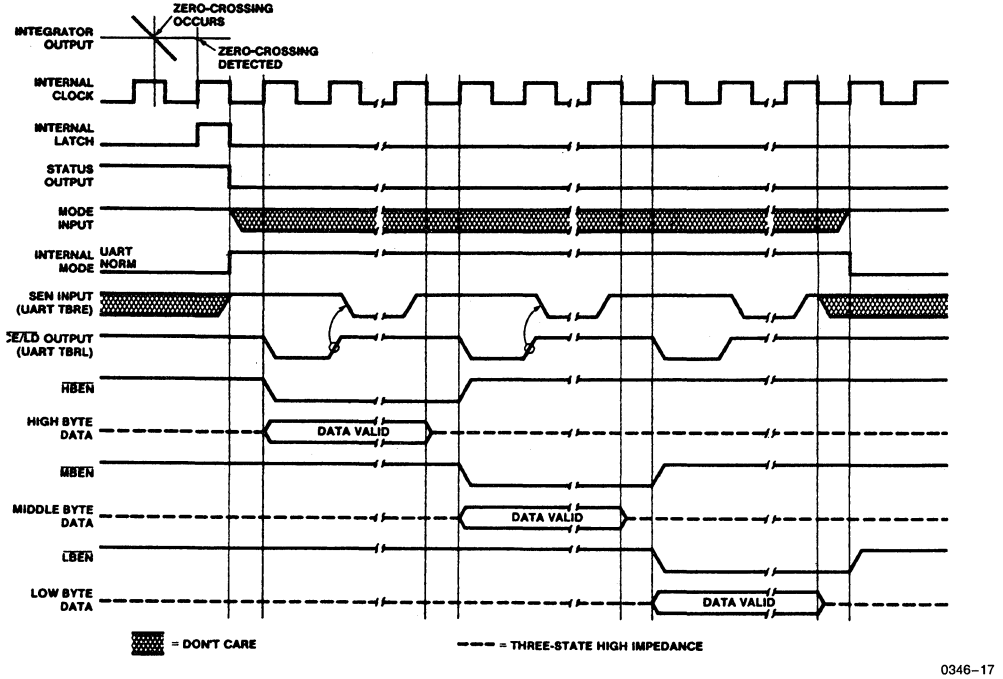


Figure 13: Handshake — Typical UART Interface Timing

NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL7104 and ICL8068/ICL7104

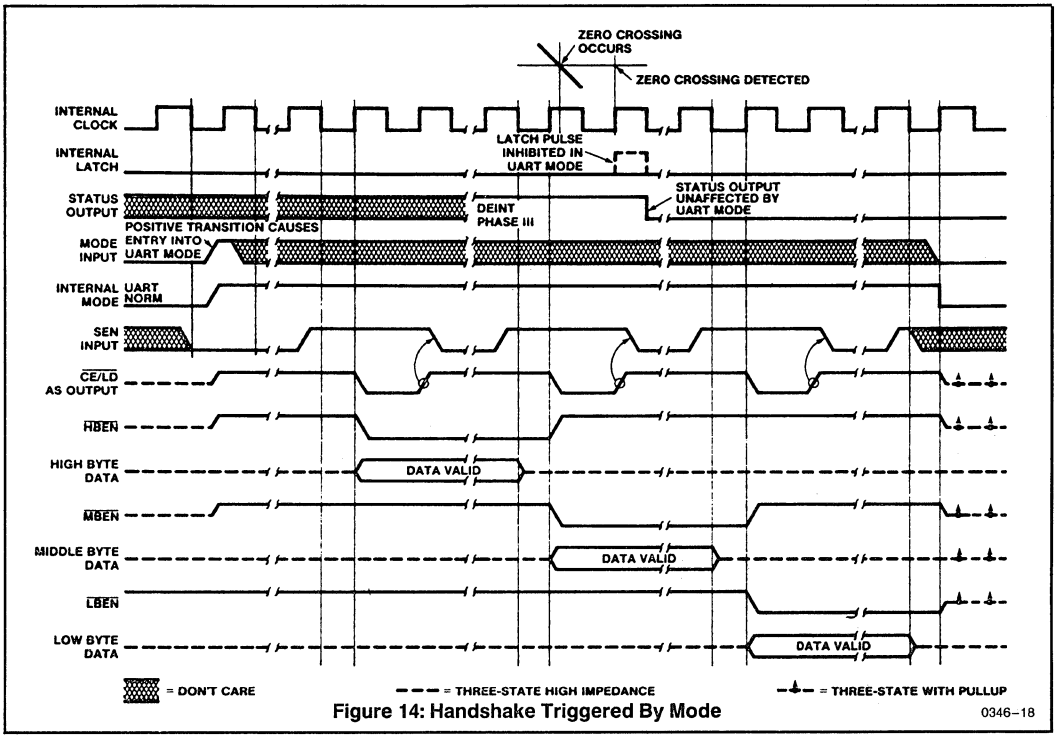


Figure 14: Handshake Triggered By Mode

0346-18

With the MODE input remaining high as in these examples, the converter will output the results of every conversion except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 14 shows a handshake output sequence triggered by such an edge. In addition, the SEN input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEN input, and the sequence for the first (high order) byte is similar to the sequence for the other bytes. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STaTuS output and Run/$\overline{\text{Hold}}$ input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

Initial Clear Circuitry

The internal logic of the 7104 is supplied by an internal regulator between V^{++} and Digital Ground. The regulator includes a low-voltage detector that will clear various registers. This is intended to ensure that on initial power-up, the control logic comes up in Auto-Zero, with the 2nd, 3rd, and 4th MSB bits cleared, and the "mode" F/F cleared (i.e. in "direct" mode). This, however, will also clear these registers if the supply voltage "glitches" to a low enough value. Additionally, if the supply voltage comes up too fast, this clear pulse may be too narrow for reliable clearing. In general, this is not a problem, but if the UART internal "MODE" F/F should come up set, the byte and chip ENable lines will become active outputs. In many systems this could lead to bus conflicts, especially in non-handshake systems. In any case, SEN should be high (held high for non-handshake systems) to ensure that the MODE F/F will be cleared as fast as possible (see Figure 12 for timing). For these and other reasons, adequate supply bypass is recommended.

Oscillator

The ICL7104-14 is provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated as an RC or crystal oscillator.

Figure 15 shows the oscillator configured for RC operation. The internal clock will be of the same frequency and phase as the voltage on the CLOCK 3 pin. The resistor and capacitor should be connected as shown. The circuit will oscillate at a frequency given by f = .45/RC. A 50 – 100kΩ resistor is recommended for useful ranges of frequency. For optimum 60Hz line rejection, the capacitor value should be chosen such that 32768 (-16), 8192 (-14) clock periods is close to an integral multiple of the 60Hz period.

NOTE: All typical values have been characterized but are not tested.

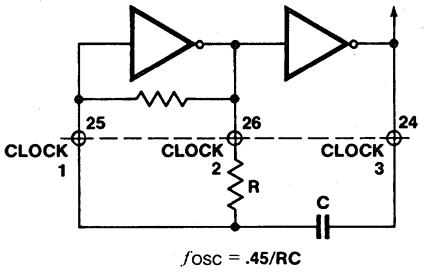


Figure 15: RC Oscillator (ICL7104-14 Only)

Note that CLOCK 3 has the same output drive as the bit outputs.

As a result of pin count limitations, the ICL7104-16 has only CLOCK 1 and CLOCK 2 available, and cannot be used as an RC oscillator. The internal clock will correspond to the inverse of the signal on CLOCK 2. Figure 16 shows a crystal oscillator circuit, which can be used with both 7104 versions. If an external clock is to be used, it should be applied to CLOCK 1. The internal clock will correspond to the signal applied to this pin.

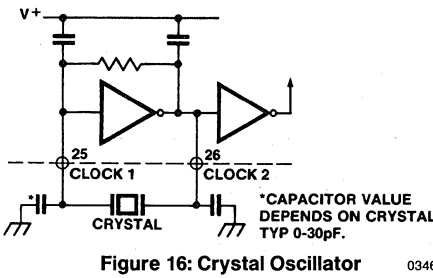


Figure 16: Crystal Oscillator

POWER SUPPLY SEQUENCING

Because of the nature of the CMOS process used to fabricate the ICL7104, and the multiple power supplies used, there are certain conditions of these supplies under which a disabling and potentially damaging SCR action can occur. All of these conditions involve the V^+ supply (nom. +5V) being more positive than the V^{++} supply. If there is any possibility of this occuring during start-up, shut down, under transient conditions during operation, or when inserting a PC board into a "hot" socket, etc., a diode should be placed between V^+ and V^{++} to prevent it. A germanium or Schottky rectifier diode would be best, but in most cases a silicon rectifier diode is adequate.

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of ICL8068 or ICL8052/7104 circuits, especially in 16-bit and high sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line. A recommended connection sequence for the ground lines is shown in Figure 17.

APPLICATIONS INFORMATION

Some applications bulletins that may be found useful are listed here:

A016 "Selecting A/D Converters", by Dave Fullagar

A017 "The Integrating A/D Converter", by Lee Evans

A018 "Do's and Dont's of Applying A/D Converters", by Peter Bradshaw and Skip Osgood

A030 "The ICL7104 — A Binary Output A/D Converter for Microprocessors", by Peter Bradshaw

R005 "Interfacing Data Converter & Microprocessors", by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

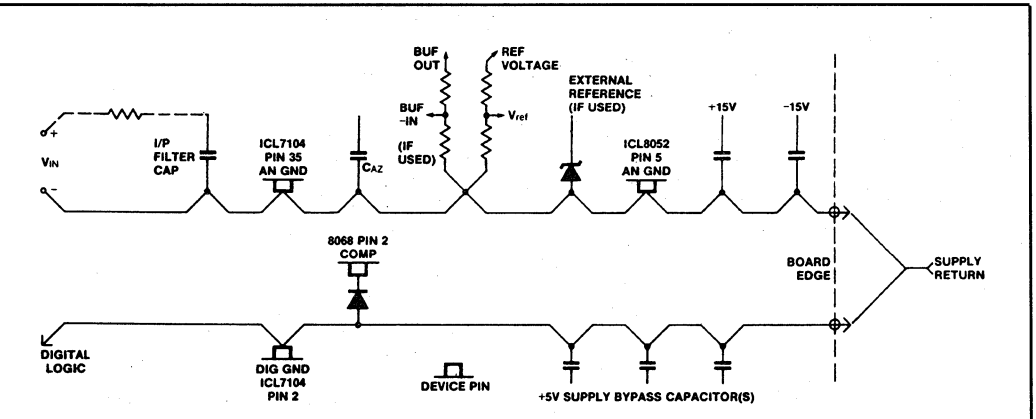


Figure 17: Grounding Sequence

NOTE: All typical values have been characterized but are not tested.

ICL8052/ICL7104 and ICL8068/ICL7104

ICL7104 with ICL8052/8068 INTEGRATING A/D CONVERTER EQUATIONS

Oscillator
CRYSTAL or RC (RC on -14 part only)
f_{OSC} Typically 200 kHz
$f_{OSC} = 0.45/RC$ (ICL7104-14 only)
$C_{OSC} > 50$ pF and $R_{OSC} > 50k$

Oscillator Period
$t_{OSC} = 1/f_{OSC}$

Integration Clock Frequency
$f_{CLOCK} = f_{OSC}$

Integration Period
$t_{INT} = 8192 \times t_{OSC}$ (7104-14)
$t_{INT} = 32768 \times t_{OSC}$ (7104-16)

60/50 Hz Rejection Criterion
t_{INT}/t_{60Hz} or t_{INT}/t_{50Hz} = Integer

Optimum Integration Current
$I_{INT} = 20\ \mu A$

Full Scale Analog Input Voltage
V_{INFS} Typ. = 200 mV to 2.0V = 2 V_{REF}

Integrate Resistor

$$R_{INT} = \frac{\text{(Buffer Gain)} \times V_{INFS}}{I_{INT}}$$

Integrate Capacitor

$$C_{INT} = \frac{(t_{INT})\,(I_{INT})}{V_{INT)}}$$

Integrator Output Voltage

$$V_{INT} = \frac{(t_{INT})\,(I_{INT})}{C_{INT}}$$

V_{INT} Typ. = 9.0V

Output Count

$$\text{Count} = 8192 \times \frac{V_{IN}}{V_{REF}} \qquad \text{(7104-14)}$$

$$\text{Count} = 32768 \times \frac{V_{IN}}{V_{REF}} \qquad \text{(7104-16)}$$

Output Type:
Binary Amplitude with Polarity and Overrange Bits.

Power Supply: ±15.0V, +5V
$V^{++} = +15V$
$V^{-} = -15V$
$V^{+} = +5V$
$V_{REF} \cong 1.75V$
If V_{REF} not used, float output pin.

Auto Zero Capacitor Values
$0.01\ \mu F < C_{AZ} < 1.0\ \mu F$

Reference Capacitor Value
C_{REF} = (Buffer Gain) × C_{AZ}

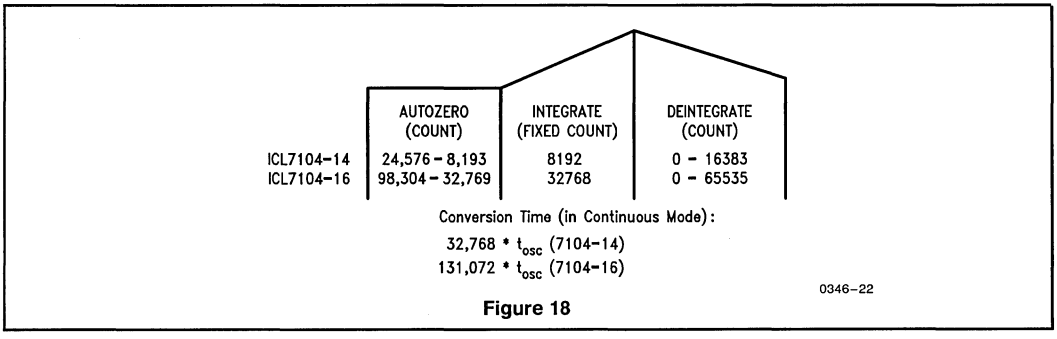


Figure 18

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICL7109
12-Bit μP-Compatible A/D Converter

GENERAL DESCRIPTION

The ICL7109 is a high performance, CMOS, low power integrating A/D converter designed to easily interface with microprocessors.

The output data (12 bits, polarity and overrange) may be directly accessed under control of two byte enable inputs and a chip select input for a simple parallel bus interface. A UART handshake mode is provided to allow the ICL7109 to work with industry-standard UARTs in providing serial data transmission, ideal for remote data logging applications. The RUN/HOLD input and STATUS output allow monitoring and control of conversion timing.

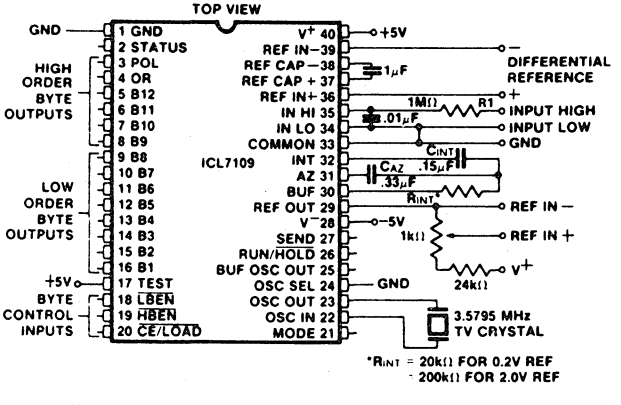
The ICL7109 provides the user with the high accuracy, low noise, low drift, versatility and economy of the dual-slope integrating A/D converter. Features like true differential input and reference, drift of less than 1μV/°C, maximum input bias current of 10pA, and typical power consumption of 20mW make the ICL7109 an attractive per-channel alternative to analog multiplexing for many data acquisition applications.

FEATURES

- **12 Bit Binary (Plus Polarity and Overrange) Dual Slope Integrating Analog-to-Digital Converter**
- **Byte-Organized TTL-Compatible Three-State Outputs and UART Handshake Mode for Simple Parallel or Serial Interfacing to Microprocessor Systems**
- **RUN/HOLD Input and STATUS Output Can Be Used to Monitor and Control Conversion Timing**
- **True Differential Input and Differential Reference**
- **Low Noise — Typically 15μV p-p**
- **1pA Typical Input Current**
- **Operates At Up to 30 Conversions Per Second**
- **On-Chip Oscillator Operates With Inexpensive 3.58MHz TV Crystal Giving 7.5 Conversions Per Second for 60Hz Rejection May Also Be Used With An RC Network Oscillator for Other Clock Frequencies**

ORDERING INFORMATION

Part Number	Temp. Range	Package
ICL7109MDL	−55°C to +125°C	40-Pin Ceramic DIP
ICL7109IDL	−25°C to +85°C	40-Pin Ceramic DIP
ICL7109IJL	−25°C to +85°C	40-Pin CERDIP
ICL7109CPL	0°C to 70°C	40-Pin Plastic DIP



(See Figure 2 for typical connection to a UART or Microcomputer)

Figure 1: Pin Configuration and Test Circuit

301655-003

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (GND to V^+) ..... +6.2V
Negative Supply Voltage (GND to V^-) ..... −9V
Analog Input Voltage (Lo or Hi) (Note 1) ..... V^+ to V^-
Reference Input Voltage (Lo or Hi) (Note 1) ..... V^+ to V^-
Digital Input Voltage (V^+ +0.3V
(Pins 2-27) (Note 2) ..... GND −0.3V

Power Dissipation (Note 3)
Ceramic Package ..... 1W @ +85°C
Plastic Package ..... 500mW @ +70°C
Operating Temperature
Ceramic Package (MDL) ..... −55°C to +125°C
Ceramic Package (IDL) ..... −25°C to +85°C
Plastic Package (CPL) ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

($V^+ = +5V$, $V^- = -5V$, GND = 0V, $T_A = 25°C$, f_{CLK} = 3.58 MHz, unless otherwise indicated.) Test circuit as shown on first page of this data sheet.

ANALOG SECTION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Zero Input Reading	V_{IN} = 0.0000V V_{REF} = 204.8 mV	−0000	±0000	+0000	Counts
	Ratiometric Error(4)	$V_{IN} = V_{REF}$ = 204.8 mV	−3		0	Counts
	Non-Linearity (Max deviation from best straight line fit)	Full Scale = 409.6mV to 2.048V Over full operating temperature range. (Note 4), (Note 6)	−1	±.2	+1	Counts
	Roll-over Error (difference in reading for equal pos. and neg. inputs near full scale)	Full Scale = 409.6mV to 2.048V (Note 5), (Note 6)	−1	±.2	+1	Counts
CMRR	Common Mode Rejection Ratio	V_{CM} ±1V, V_{IN} = 0V Full Scale = 409.6mV		50		μV/V
VCMR	Input Common Mode Range	Input Hi, Input Lo, Common (Note 4)	V^- +1.5		V^+ −1.0	V
e_n	Noise (p-p value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 409.6mV		15		μV
I_{ILK}	Leakage current at Input	V_{IN} = 0 All devices at 25°C ICL7109CPL 0°C ≤ T_A ≤ +70°C (Note 4) ICL7109IDL −25°C ≤ T_A ≤ +85°C (Note 4) ICL7109MDL −55°C ≤ T_A ≤ +125°C		1 20 100 2	10 100 250 5	pA pA pA nA
	Zero Reading Drift	V_{IN} = 0V R_1 = 0Ω (Note 4)		0.2	1	μV/°C
	Scale Factor Temperature Coefficient	V_{IN} = 408.9mV = >7770_8 reading Ext. Ref. 0 ppm/°C (Note 4)		1	5	ppm/°C
I^+	Supply Current V^+ to GND	V_{IN} = 0, Crystal Osc 3.58MHz test circuit		700	1500	μA
I_{SUPP}	Supply Current V^+ to V^-	Pins 2-21, 25, 26, 27, 29; open		700	1500	μA
V_{REF}	Ref Out Voltage	Referred to V^+, 25kΩ between V^+ and REF OUT	−2.4	−2.8	−3.2	V
	Ref Out Temp. Coefficient	25kΩ between V^+ and REF OUT		80		ppm/°C

NOTE: All typical values have been characterized but are not tested.

ICL7109

ELECTRICAL CHARACTERISTICS ($V^+ = +5V$, $V^- = -5V$, GND = 0V, $T_A = 25°C$, unless otherwise indicated.) Test circuit as shown on first page of this data sheet. (Continued)

DIGITAL SECTION

Symbol	Parameter		Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output High Voltage		$I_{OUT} = 100\mu A$ Pins 2-16, 18, 19, 20	3.5	4.3		V
V_{OL}	Output Low Voltage		$I_{OUT} = 1.6mA$		0.2	0.4	V
	Output Leakage Current		Pins 3-16 high impedance		±.01	±1	μA
	Control I/O Pullup Current		Pins 18, 19, 20 $V_{OUT} = V^+ - 3V$ MODE input at GND		5		μA
	Control I/O Loading		$\overline{HBEN}$ Pin 19 $\overline{LBEN}$ Pin 18 (Note 4)			50	pF
V_{IH}	Input High Voltage		Pins 18-21, 26, 27 referred to GND	3.0			V
V_{IL}	Input Low Voltage		Pins 18-21, 26, 27 referred to GND			1	V
	Input Pull-up Current		Pins 26, 27 $V_{OUT} = V^+ - 3V$		5		μA
	Input Pull-up Current		Pins 17, 24 $V_{OUT} = V^+ - 3V$		25		μA
	Input Pull-down Current		Pin 21 $V_{OUT} = GND + 3V$		5		μA
O_{OH}	Oscillator Output	High	$V_{OUT} = 2.5V$		1		mA
O_{OL}	Current	Low	$V_{OUT} = 2.5V$		1.5		mA
BO_{OH}	Buffered Oscillator	High	$V_{OUT} = 2.5V$		2		mA
BO_{OL}	Output Current	Low	$V_{OUT} = 2.5V$		5		mA
t_W	MODE Input Pulse Width		(Note 4)	50			ns

NOTES: 1. Input voltages may exceed the supply voltages provided the input current is limited to ±100μA
2. Due to the SCR structure inherent in the process used to fabricate these devices, connecting any digital inputs or outputs to voltages greater than V^+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources other than the same power supply be applied to the ICL7109 before its power supply is established, and that in multiple supply systems the supply to the ICL7109 be activated first.
3. This limit refers to that of the package and will not be obtained during normal operation.
4. This parameter is not production tested, but is guaranteed by design.
5. Roll-over error for $T_A = -55°C$ to $+125°C$ is ±3 counts maximum.
6. A full-scale voltage of 2.048V is used because a full scale voltage of 4.096V exceeds the devices Common Mode Voltage Range.
7. For Cerdip package the Ratiometric error can be −4 (Min.).

NOTE: All typical values have been characterized but are not tested.

TABLE 1: Pin Assignment and Function Description

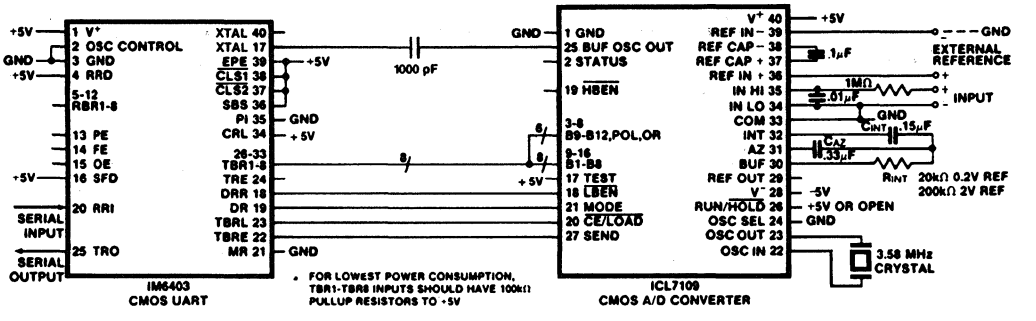
Pin	Symbol	Description		
1	GND	Digital Ground, 0V. Ground return for all digital logic.		
2	STATUS	Output High during integrate and deintegrate until data is latched. Output Low when analog section is in Auto-Zero configuration.		
3	POL	Polarity — HI for Positive input.		All three state output data bits
4	OR	Overrange — HI if Overranged.		
5	B12	Bit 12	(Most Significant Bit)	
6	B11	Bit 11	HI = true	
7	B10	Bit 10		
8	B9	Bit 9		
9	B8	Bit 8		
10	B7	Bit 7		
11	B6	Bit 6		
12	B5	Bit 5		
13	B4	Bit 4		
14	B3	Bit 3		
15	B2	Bit 2		
16	B1	Bit 1	(Least Significant Bit)	
17	TEST	Input High — Normal Operation. Input Low — Forces all bit outputs high. Note: This input is used for test purposes only. Tie high if not used.		
18	$\overline{\text{LBEN}}$	Low Byte Enable — With Mode (Pin 21) low, and $\overline{\text{CE/LOAD}}$ (Pin 20) low, taking this pin low activates low order byte outputs B1 — B8. — With Mode (Pin 21) high, this pin serves as a low byte flag output used in handshake mode. See Figures 8, 9, 10.		
19	$\overline{\text{HBEN}}$	High Byte Enable — With Mode (Pin 21) low, and $\overline{\text{CE/LOAD}}$ (Pin 20) low, taking this pin low activates high order byte outputs B9 — B12, POL, OR. — With Mode (Pin 21) high, this pin serves as a high byte flag output used in handshake mode. See Figures 8, 9, 10.		
20	$\overline{\text{CE/LOAD}}$	Chip Enable Load — With Mode (Pin 21) low. $\overline{\text{CE/LOAD}}$ serves as a master output enable. When high, B1 — B12, POL, OR outputs are disabled. — With Mode (Pin 21) high, this pin serves as a load strobe used in handshake mode. See Figures 8, 9, 10.		

Pin	Symbol	Description
21	MODE	Input Low — Direct output mode where $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19) and $\overline{\text{LBEN}}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed High — Causes immediate entry into handshake mode and output of data as in Figure 10. Input High — Enables $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19), and $\overline{\text{LBEN}}$ (Pin 18) as outputs, handshake mode will be entered and data output as in Figures 8 and 9 at conversion completion.
22	OSC IN	Oscillator Input
23	OSC OUT	Oscillator Output
24	OSC SEL	Oscillator Select — Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator — clock will be same phase and duty cycle as BUF OSC OUT. — Input low configures OSC IN, OSC OUT for crystal oscillator — clock frequency will be 1/58 of frequency at BUF OSC OUT.
25	BUF OSC OUT	Buffered Oscillator Output
26	RUN/$\overline{\text{HOLD}}$	Input High — Conversions continuously performed every 8192 clock pulses. Input Low — Conversion in progress completed, converter will stop in Auto-Zero 7 counts before integrate.
27	SEND	Input — Used in handshake mode to indicate ability of an external device to accept data. Connect to +5V if not used.
28	V−	Analog Negative Supply — Nominally −5V with respect to GND (Pin 1).
29	REF OUT	Reference Voltage Output — Nominally 2.8V down from V* (Pin 40).
30	BUFFER	Buffer Amplifier Output
31	AUTO-ZERO	Auto-Zero Node — Inside foil of C_{AZ}
32	INTEGRATOR	Integrator Output — Outside foil of C_{INT}
33	COMMON	Analog Common — System is Auto-Zeroed to COMMON
34	INPUT LO	Differential Input Low Side
35	INPUT HI	Differential Input High Side
36	REF IN +	Differential Reference Input Positive
37	REF CAP +	Reference Capacitor Positive
38	REF CAP	Reference Capacitor Negative
39	REF IN	Differential Reference Input Negative
40	V+	Positive Supply Voltage — Nominally +5V with respect to GND (Pin 1).

Note: All digital levels are positive true.

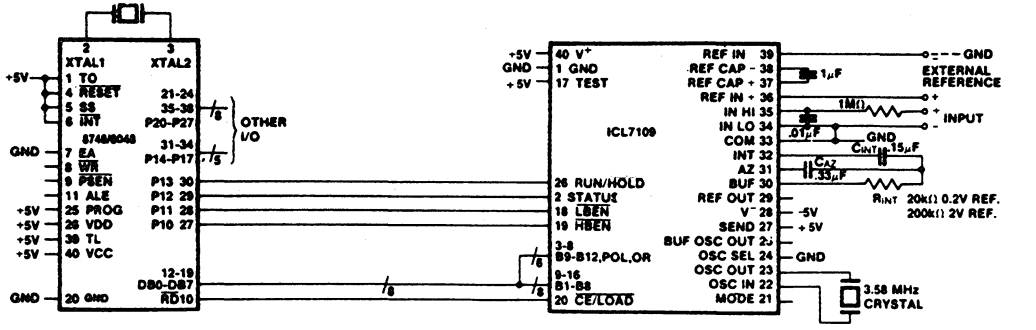
NOTE: All typical values have been characterized but are not tested.

ICL7109



0336-2

Figure 2A: Typical Connection Diagram UART Interface – To transmit latest result, send any word to UART



0336-3

Figure 2B: Typical Connection Diagram Parallel Interface With 8048 Microcomputer

DETAILED DESCRIPTION

Analog Section

Figure 3 shows the equivalent circuit of the Analog Section of the ICL7109. When the RUN/$\overline{\text{HOLD}}$ input is left open or connected to V^+, the circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle). Each measurement cycle is divided into three phases as shown in Figure 4. They are (1) Auto-Zero (AZ), (2) Signal Integrate (INT) and (3) Deintegrate (DE).

Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from their pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the AZ accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

NOTE: All typical values have been characterized but are not tested.

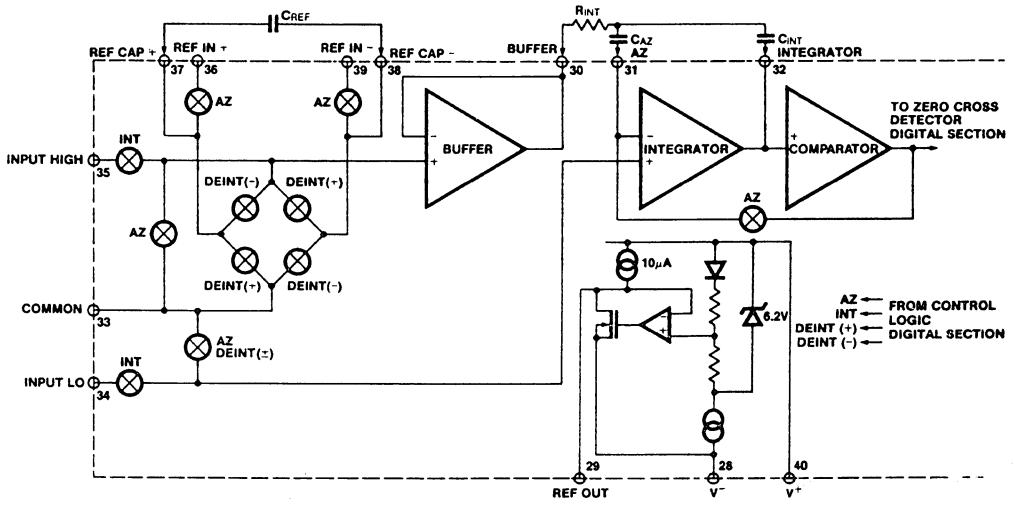


Figure 3: Analog Section

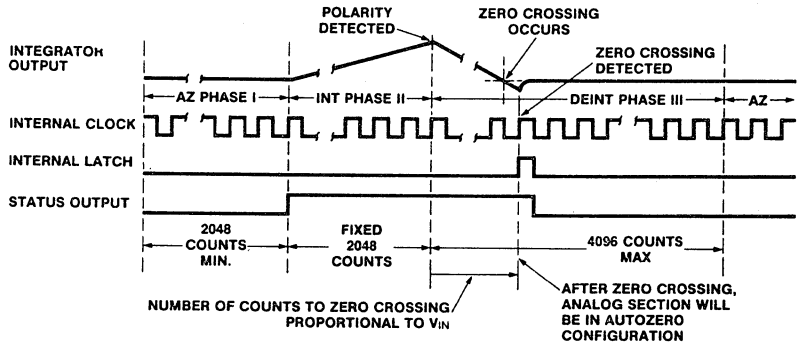


Figure 4: Conversion Timing (RUN/$\overline{\text{HOLD}}$ Pin High)

Signal Integrate Phase

During signal integrate the auto-zero loop is opened, the internal short is removed and the internal high and low inputs are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time of 2048 clock periods. Note that this differential voltage must be within the common mode range of the inputs. At the end of this phase, the polarity of the integrated signal is determined.

De-Integrate Phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged (during auto-zero) reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero crossing (established in Auto Zero) with a fixed slope. Thus the time for the output to return to zero (represented by the number of clock periods counted) is proportional to the input signal.

NOTE: All typical values have been characterized but are not tested.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 1.0 volts below the positive supply to 1.5 volts above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full scale with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

The ICL7109 has, however, been optimized for operation with analog common near digital ground. With power supplies of +5V and −5V, this allows a 4V full scale integrator swing positive or negative thus maximizing the performance of the analog section.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to deintegrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Values Selection below).

The roll-over error from these sources is minimized by having the reference common mode voltage near or at analog COMMON.

Component Value Selection

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

The most important consideration is that the integrator output swing (for full-scale input) be as large as possible. For example, with ±5V supplies and COMMON connected to GND, the nominal integrator output swing at full scale is ±4V. Since the integrator output can go to 0.3V from either supply without significantly affecting linearity, a 4V integrator output swing allows 0.7V for variations in output swing due to component value and oscillator tolerances. With ±5V supplies and a common mode range of ±1V required, the component values should be selected to provide ±3V integrator output swing. Noise and rollover errors will be slightly worse than in the ±4V case. For larger common mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and rollover errors. To improve the performance, supplies of ±6V may be used.

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 4.096 volt full scale, 200kΩ is near optimum and similarly a 20kΩ for a 409.6mV scale. For other values of full scale voltage, R_{INT} should be chosen by the relation

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$$

Integrating Capacitor

The integrating capacitor C_{INT} should be selected to give the maximum integrator output voltage swing without saturating the integrator (approximately 0.3 volt from either supply). For the ICL7109 with ±5 volt supplies and analog common connected to GND, a ±3.5 to ±4 volt integrator output swing is nominal. For 7-½ conversions per second (61.72kHz clock frequency) as provided by the crystal oscillator, nominal values for C_{INT} and C_{AZ} are 0.15μF and 0.33μF, respectively. If different clock frequencies are used, these values should be changed to maintain the integrator output voltage swing. In general, the value of C_{INT} is given by

$$C_{INT} = \frac{(2048 \times \text{clock period})(20\mu A)}{\text{integrator output voltage swing}}\ \mu F$$

An additional requirement of the integrating capacitor is that it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost up to 85°C. For the military temperature range, Teflon® capacitors are recommended. While their dielectric absorption characteristics vary somewhat from unit to unit, selected devices should give less than 0.5 count of error due to dielectric absorption.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system: a smaller physical size and a larger capacitance value lower the overall system noise. However, C_{AZ} cannot be increased without limits since it, in parallel with the integrating capacitor forms an R-C time constant that determines the speed of recovery from overloads and more important the error that exists at the end of an auto-zero cycle. For 409.6mV full scale where noise is very important and the integrating resistor small, a value of C_{AZ} twice C_{INT} is optimum. Similarly for 4.096V full scale where recovery is more important than noise, a value of C_{AZ} equal to half of C_{INT} is recommended.

For optimal rejection of stray pickup, the outer foil of C_{AZ} should be connected to the R-C summing junction and the inner foil to pin 31. Similarly the outer foil of C_{INT} should be connected to pin 32 and the inner foil to the R-C summing junction. Teflon®, or equivalent, capacitors are recommended above 85°C for their low leakage characteristics.

NOTE: All typical values have been characterized but are not tested.

Reference Capacitor

A 1μF capacitor gives good results in most applications. However, where a large reference common mode voltage exists (i.e. the reference low is not at analog common) and a 409.6mV scale is used, a larger value is required to prevent roll-over error. Generally 10μF will hold the roll-over error to 0.5 count in this instance. Again, Teflon®, or equivalent capacitors should be used for temperatures above 85°C for their low leakage characteristics.

Reference Voltage

The analog input required to generate a full scale output of 4096 counts is $V_{IN} = 2V_{REF}$. Thus for a normalized scale, a reference of 2.048V should be used for a 4.096V full scale, and 204.8mV should be used for a 0.4096V full scale. However, in many applications where the A/D is sensing the output of a transducer, there will exist a scale factor other than unity between the absolute output voltage to be measured and a desired digital output. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 409.6mV, the input voltage should be measured directly and a reference voltage of 0.341V should be used. Suitable values for integrating resistor and capacitor are 33kΩ and 0.15μF. This avoids a divider on the input. Another advantage of this system occurs when a zero reading is desired for non-zero input. Temperature and weight measurements with an offset or tare are examples. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. However, in processor-based systems using the ICL7109, it may be more efficient to perform this type of scaling or tare subtraction digitally using software.

Reference Sources

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7109 at 12 bits is one part in 4096, or 244ppm. Thus if the reference has a temperature coefficient of 80ppm/°C (onboard reference) a temperature difference of 3°C will introduce a one-bit absolute error.

For this reason, it is recommended that an external high-quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

The ICL7109 provides a REFerence OUTput (pin 29) which may be used with a resistive divider to generate a suitable reference voltage. This output will sink up to about 20mA without significant variation in output voltage, and is provided with a pullup bias device which sources about 10μA. The output voltage is nominally 2.8V below V^+, and has a temperature coefficient of ±80ppm/°C typ. When using the onboard reference, REF OUT (Pin 29) should be connected to REF− (pin 39), and REF+ should be connected to the wiper of a precision potentiometer between REF OUT and V^+. The circuit for a 204.8mV reference is shown in the test circuit. For a 2.048mV reference, the fixed resistor should be removed, and a 25kΩ precision potentiometer between REF OUT and V^+ should be used.

Note that if pins 29 and 39 are tied together and pins 39 and 40 accidentally shorted (e.g., during testing), the reference supply will sink enough current to destroy the device. This can be avoided by placing a 1kΩ resistor in series with pin 39.

DETAILED DESCRIPTION

Digital Section

The digital section includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, overrange and control logic, and UART handshake logic, as shown in Figure 5.

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined in the Electrical Characteristics Table. For minimum power consumption, all inputs should swing from GND (low) to V^+ (high). Inputs driven from TTL gates should have 3-5kΩ pullup resistors added for maximum noise immunity.

MODE Input

The MODE input is used to control the output mode of the converter. When the MODE pin is low or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

STATUS Output

During a conversion cycle, the STATUS output goes high at the beginning of Signal Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 4 for details of this timing. This signal may be used as a "data valid" flag (data never changes while STATUS is low) to drive interrupts, or for monitoring the status of the converter.

RUN/$\overline{\text{HOLD}}$ Input

When the RUN/$\overline{\text{HOLD}}$ input is high, or left open, the circuit will continuously perform conversion cycles, updating the output latches after zero crossing during the Deintegrate (Phase III) portion of the conversion cycle (See Figure 4). In this mode of operation, the conversion cycle will be performed in 8192 clock periods, regardless of the resulting value.

If RUN/$\overline{\text{HOLD}}$ goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to eliminate the time spent in Deintegrate after the zero-crossing. If RUN/$\overline{\text{HOLD}}$ stays or goes low, the converter will ensure minimum Auto-Zero time, and then wait in Auto-Zero until the RUN/$\overline{\text{HOLD}}$ input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STATUS output will go high) seven clock periods after the high level is detected at RUN/$\overline{\text{HOLD}}$. See Figure 6 for details.

NOTE: All typical values have been characterized but are not tested.

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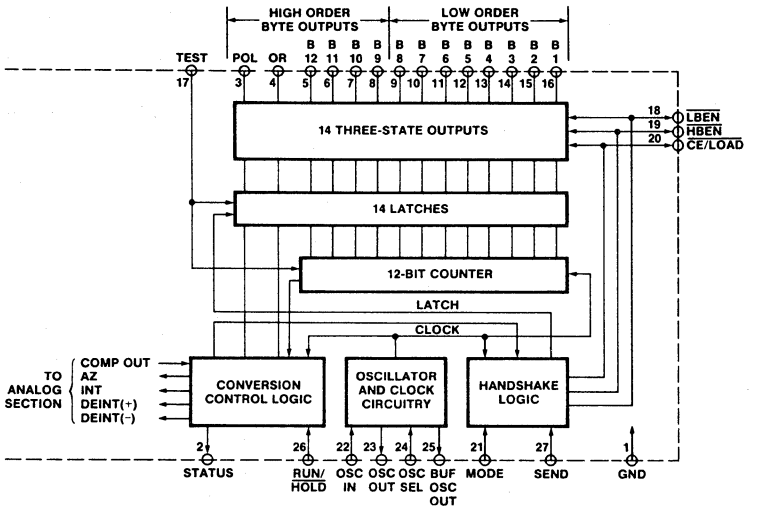


Figure 5: Digital Section

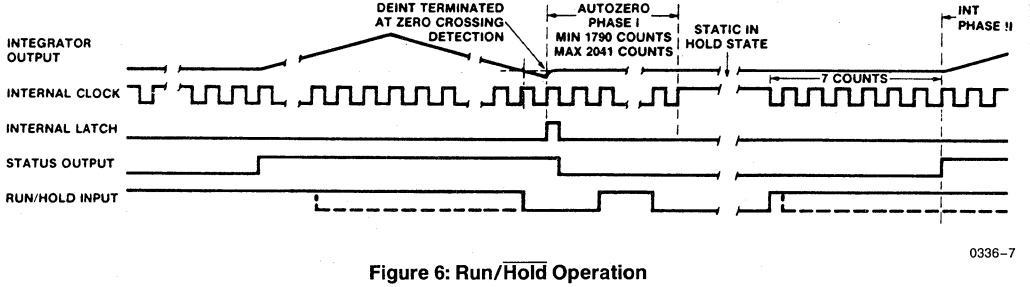


Figure 6: Run/Hold Operation

Using the RUN/$\overline{\text{HOLD}}$ input in this manner allows an easy "convert on demand" interface to be used. The converter may be held at idle in auto-zero with RUN/$\overline{\text{HOLD}}$ low. When RUN/$\overline{\text{HOLD}}$ goes high the conversion is started, and when the STATUS output goes low the new data is valid (or transferred to the UART — see Handshake Mode). RUN/$\overline{\text{HOLD}}$ may now be taken low which terminates deintegrate and ensures a minimum Auto-Zero time before the next conversion.

Alternately, RUN/$\overline{\text{HOLD}}$ can be used to minimize conversion time by ensuring that it goes low during Deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the RUN/$\overline{\text{HOLD}}$ input can be provided by connecting it to the Buffered Oscillator Output. In this mode the conversion time is dependent on the input value measured. Also refer to Harris Application Bulletin A032 for a discussion of the effects this will have on Auto-Zero performance.

If the RUN/$\overline{\text{HOLD}}$ input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for RUN/$\overline{\text{HOLD}}$ to go high. As above, Integrate (Phase II) begins seven clock periods after the high level is detected.

Direct Mode

When the MODE pin is left at a low level, the data outputs (bits 1 through 8 low order byte, bits 9 through 12, polarity and over-range high order byte) are accessible under control of the byte and chip enable terminals as inputs. These three inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip enable input is low, taking a byte enable input low will allow the outputs of that byte to become active (three-stated on). This allows a variety of parallel data accessing techniques to be used, as shown in the section entitled "Interfacing." The timing requirements for these outputs are shown in Figure 7 and Table 2.

NOTE: All typical values have been characterized but are not tested.

Table 2 — Direct Mode Timing Requirements
(See Note 4 of Electrical Characteristics)

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{BEA}	Byte Enable Width	350	220		ns
t_{DAB}	Data Access Time from Byte Enable		210	350	ns
t_{DHB}	Data Hold Time from Byte Enable		150	300	ns
t_{CEA}	Chip Enable Width	400	260		ns
t_{DAC}	Data Access Time from Chip Enable		260	400	ns
t_{DHC}	Data Hold Time from Chip Enable		240	400	ns

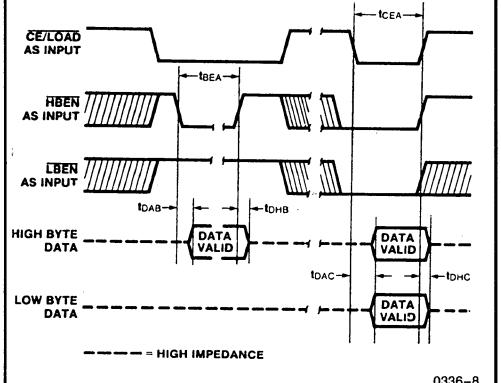


Figure 7: Direct Mode Output Timing

It should be noted that these control inputs are asynchronous with respect to the converter clock — the data may be accessed at any time. Thus it is possible to access the latches while they are being updated, which could lead to erroneous data. Synchronizing the access of the latches with the conversion cycle by monitoring the STATUS output will prevent this. Data is never updated while STATUS is low.

Handshake Mode

The handshake output mode is provided as an alternative means of interfacing the ICL7109 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte enable inputs. This mode is specifically designed to allow a direct interface between the ICL7109 and industry-standard UARTs (such as the Harris IM6402/3) with no external logic required. When triggered into the handshake mode, the ICL7109 provides all the control and flag signals necessary to sequentially transfer two bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission.

Entry into the handshake mode is controlled by the MODE pin. When the MODE terminal is held high, the ICL7109 will enter the handshake mode after new data has been stored in the output latches at the end of a conversion (See Figures 8 and 9). The MODE terminal may also be used to trigger entry into the handshake mode on demand. At any time during the conversion cycle, the low to high transition of a short pulse at the MODE input will cause immediate entry into the handshake mode. If this pulse occurs while new data is being stored, the entry into handshake mode is delayed until the data is stable. While the converter is in the handshake mode, the MODE input is ignored, and although conversions will still be performed, data updating will be inhibited (See Figure 10) until the converter completes the output cycle and clears the handshake mode.

When the converter enters the handshake mode, or when the MODE input is high, the chip and byte enable terminals become TTL-compatible outputs which provide the control signals for the output cycle (See Figures 8, 9, and 10).

In handshake mode, the SEND input is used by the converter as an indication of the ability of the receiving device (such as a UART) to accept data.

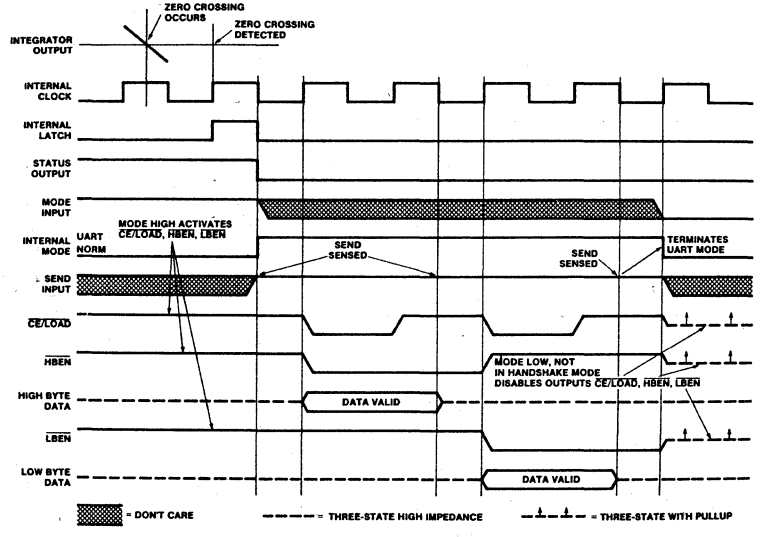
Figure 8 shows the sequence of the output cycle with SEND held high. The handshake mode (Internal MODE high) is entered after the data latch pulse, and since MODE remains high the $\overline{CE/LOAD}$, $\overline{LBEN}$ and $\overline{HBEN}$ terminals are active as outputs. The high level at the SEND input is sensed on the same high to low internal clock edge that terminates the data latch pulse. On the next low to high internal clock edge the $\overline{CE/LOAD}$ and the $\overline{HBEN}$ outputs assume a low level, and the high-order byte (bits 9 through 12, POL, and OR) outputs are enabled. The $\overline{CE/LOAD}$ output remains low for one full internal clock period only, the data outputs remain active for 1-½ internal clock periods, and the high byte enable remains low for two clock periods. Thus the $\overline{CE/LOAD}$ output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte enable as an output may be used as a byte identification flag. With SEND remaining high the converter completes the output cycle using $\overline{CE/LOAD}$ and $\overline{LBEN}$ while the low order byte outputs (bits 1 through 8) are activated. The handshake mode is terminated when both bytes are sent.

Figure 9 shows an output sequence where the SEND input is used to delay portions of the sequence, or handshake to ensure correct data transfer. This timing diagram shows the relationships that occur using an industry-standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEND input to the ICL7109 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{CE/LOAD}$ terminal of the ICL7109 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

3

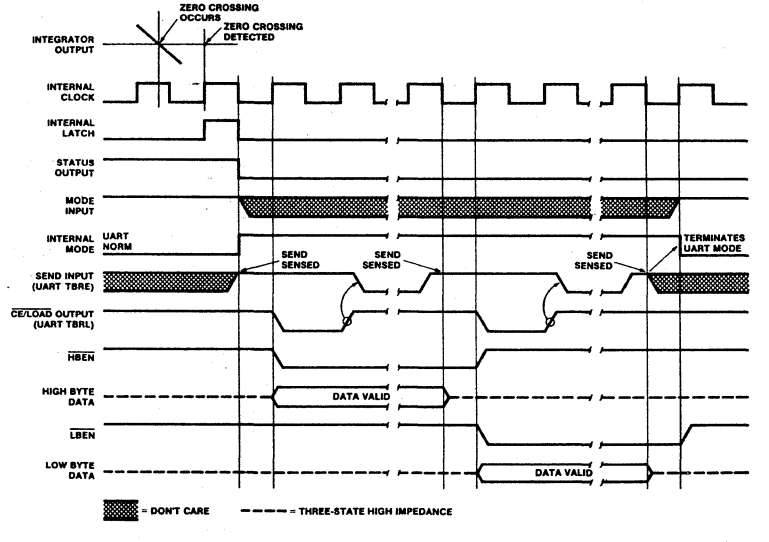
NOTE: All typical values have been characterized but are not tested.

ICL7109



0336-9

Figure 8: Handshake With Send Held Positive



0336-10

Figure 9: Handshake — Typical UART Interface Timing

NOTE: All typical values have been characterized but are not tested.

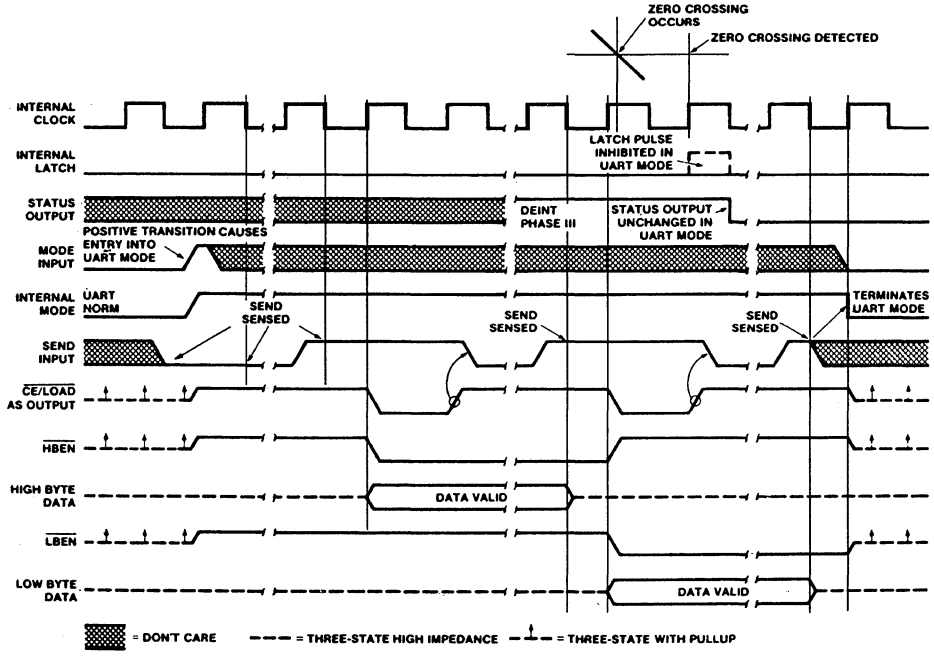


Figure 10: Handshake Triggered By Mode

Assuming the UART Transmitter Buffer Register is empty, the SEND input will be high when the handshake mode is entered after new data is stored. The $\overline{CE/LOAD}$ and $\overline{HBEN}$ terminals will go low after SEND is sensed, and the high order byte outputs become active. When $\overline{CE/LOAD}$ goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the $\overline{HBEN}$ output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next ICL7109 internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the $\overline{HBEN}$ output returns high. At the same time, the $\overline{CE/LOAD}$ and $\overline{LBEN}$ outputs go low, and the low order byte outputs become active. Similarly, when the $\overline{CE/LOAD}$ returns high at the end of one clock period, the low order data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7109 internal clock high to low edge, disabling the data outputs. One-half internal clock later, the handshake mode will be cleared, and the $\overline{CE/LOAD}$, $\overline{HBEN}$, and $\overline{LBEN}$ terminals return high and stay active (as long as MODE stays high).

With the MODE input remaining high as in these examples, the converter will output the results of every conversion except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 10 shows a handshake output sequence triggered by such an edge. In addition, the SEND input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEND input, and the sequence for the first (high order) byte is similar to the sequence for the second byte. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STATUS output and RUN/$\overline{HOLD}$ input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

Oscillator

The ICL7109 is provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated with an RC network or crystal. The OSCILLATOR SELECT input changes the internal configuration of the oscillator to optimize it for RC or crystal operation.

NOTE: All typical values have been characterized but are not tested.

When the OSCILLATOR SELECT input is high or left open (the input is provided with a pullup resistor), the oscillator is configured for RC operation, and the internal clock will be of the same frequency and phase as the signal at the BUFFERED OSCILLATOR OUTPUT. The resistor and capacitor should be connected as in Figure 11. The circuit will oscillate at a frequency given by $f = 0.45/RC$. A 100kΩ resistor is recommended for useful ranges of frequency. For optimum 60Hz line rejection, the capacitor value should be chosen such that 2048 clock periods is close to an integral multiple of the 60Hz period (but should not be less than 50pF).

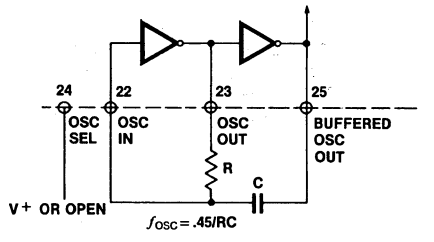


Figure 11: RC Oscillator

When the OSCILLATOR SELECT input is low a feedback device and output and input capacitors are added to the oscillator. In this configuration, as shown in Figure 12, the oscillator will operate with most crystals in the 1 to 5MHz range with no external components. Taking the OSCILLATOR SELECT input low also inserts a fixed ÷58 divider circuit between the BUFFERED OSCILLATOR OUTPUT and the internal clock. Using an inexpensive 3.58MHz TV crystal, this division ratio provides an integration time given by:

$$T_{INT} = (2048 \text{ clock periods}) \times (T_{CLOCK}) = 33.18 \text{ ms}$$

$$\text{where } T_{CLOCK} = \frac{58}{3.58 \text{ MHz}}$$

This time is very close to two 60Hz periods or 33.33ms. The error is less than one percent, which will give better than 40dB 60Hz rejection. The converter will operate reliably at conversion rates of up to 30 per second, which corresponds to a clock frequency of 245.8kHz.

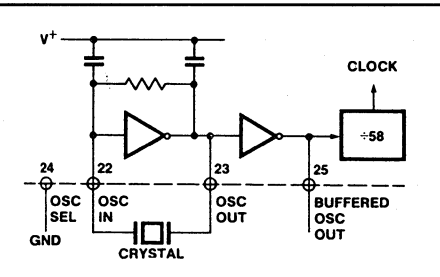


Figure 12: Crystal Oscillator

If at any time the oscillator is to be overdriven, the overdriving signal should be applied at the OSCILLATOR INPUT, and the OSCILLATOR OUTPUT should be left open. The internal clock will be of the same frequency, duty cycle, and phase as the input signal when OSCILLATOR SELECT is left open. When OSCILLATOR SELECT is at GND, the clock will be a factor of 58 below the input frequency.

When using the ICL7109 with the IM6403 UART, it is possible to use one 3.58MHz crystal for both devices. The BUFFERED OSCILLATOR OUTPUT of the ICL7109 may be used to drive the OSCILLATOR INPUT of the UART, saving the need for a second crystal. However, the BUFFERED OSCILLATOR OUTPUT does not have a great deal of drive capability, and when driving more than one slave device, external buffering should be used.

Test Input

When the TEST input is taken to a level halfway between V^+ and GND, the counter output latches are enabled, allowing the counter contents to be examined anytime.

When the TEST input is connected to GND, the counter outputs are all forced into the high state, and the internal clock is disabled. When the input returns to the ½ (V^+ −GND) voltage (or to V^+) and one clock is applied, all the counter outputs will be clocked to the low state. This allows easy testing of the counter and its outputs.

INTERFACING

Direct Mode

Figure 13 shows some of the combinations of chip enable and byte enable control signals which may be used when interfacing the ICL7109 to parallel data lines. The $\overline{CE/LOAD}$ input may be tied low, allowing either byte to be controlled by its own enable as in Figure 13A. Figure 13B shows a configuration where the two byte enables are connected together. In this configuration, the $\overline{CE/LOAD}$ serves as a chip enable, and the $\overline{HBEN}$ and $\overline{LBEN}$ may be connected to GND or serve as a second chip enable. The 14 data outputs will all be enabled simultaneously. Figure 13C shows the $\overline{HBEN}$ and $\overline{LBEN}$ as flag inputs, and $\overline{CE/LOAD}$ as a master enable, which could be the READ strobe available from most microprocessors.

Figure 14 shows an approach to interfacing several ICL7109s to a bus, ganging the $\overline{HBEN}$ and $\overline{LBEN}$ signals to several converters together, and using the $\overline{CE/LOAD}$ inputs (perhaps decoded from an address) to select the desired converter.

NOTE: All typical values have been characterized but are not tested.

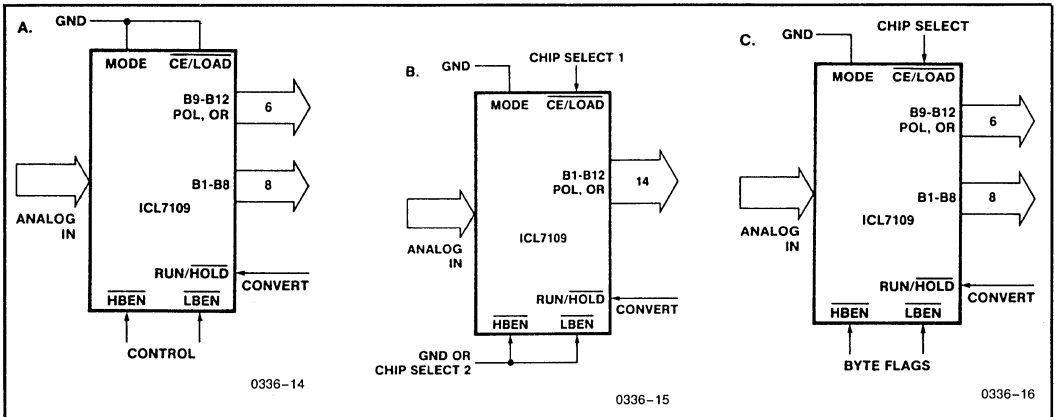


Figure 13: Direct Mode Chip and Byte Enable Combinations

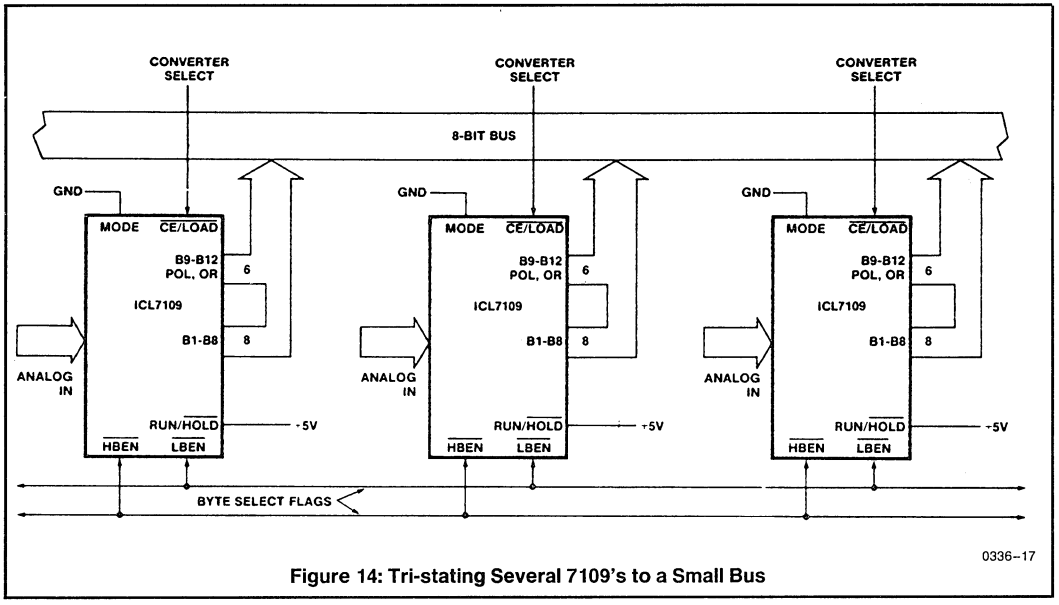


Figure 14: Tri-stating Several 7109's to a Small Bus

Some practical circuits utilizing the parallel three-state output capabilities of the ICL7109 are shown in Figures 15 through 20. Figure 15 shows a straightforward application to the Intel 8048/80/85 microprocessors via an 8255PPI, where the ICL7109 data outputs are active at all times. The I/O ports of an 8155 may be used in the same way. This interface can be used in a read-anytime mode, although a read performed while the data latches are being updated will lead to scrambled data. This will occur very rarely, in the proportion of setup-skew times to conversion time. One way to overcome this is to read the STATUS output as well, and if it is high, read the data again after a delay of more than ½ converter clock period. If STATUS is now low, the second reading is correct, and if it is still high, the first reading is correct. Alternatively, this timing problem is completely avoided by using a read-after-update sequence, as shown in Figure 16. Here the high to low transition of the STATUS output drives an interrupt to the microprocessor causing it to access the data latches. This application also shows the RUN/$\overline{\text{HOLD}}$ input being used to initiate conversions under software control.

A similar interface to Motorola MC6800 or Rockwell R650X systems is shown in Figure 17. The high to low transition of the STATUS output generates an interrupt via the

NOTE: All typical values have been characterized but are not tested.

ICL7109

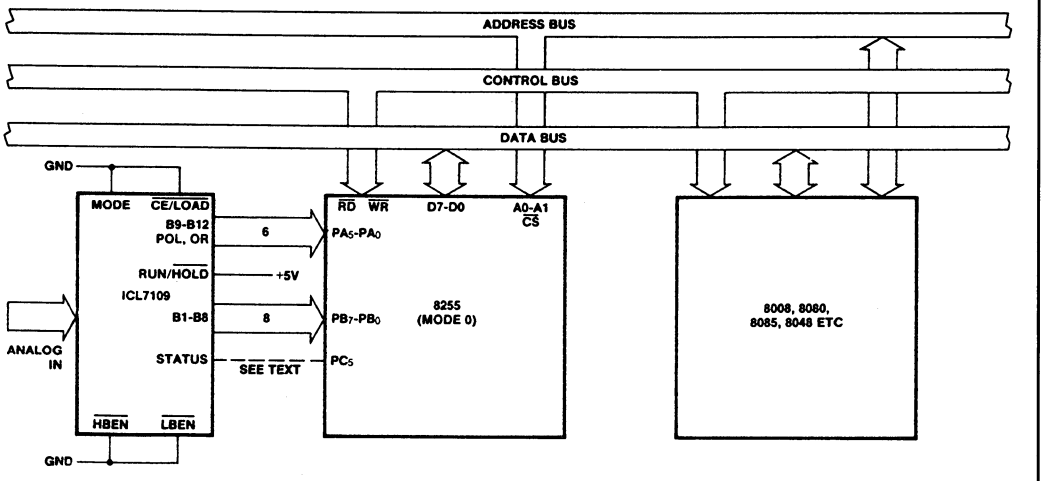


Figure 15: Full-time Parallel Interface to 8048/80/85 Microprocessors

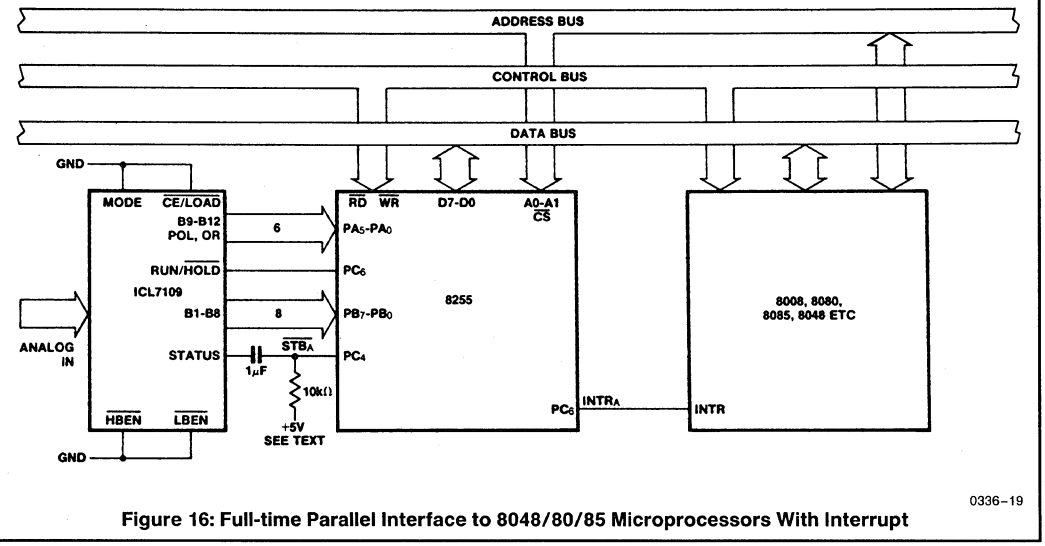


Figure 16: Full-time Parallel Interface to 8048/80/85 Microprocessors With Interrupt

Control Register B CB1 line. Note that CB2 controls the RUN/HOLD pin through Control Register B, allowing software-controlled initiation of conversions in this system as well.

The three-state output capability of the ICL7109 allows direct interfacing to most microprocessor busses. Examples of this are shown in Figures 18 and 19. It is necessary to carefully consider the system timing in this type of interface, to be sure that requirements for setup and hold times, and minimum pulse widths are met. Note also the drive limitations on long buses. Generally this type of interface is only favored if the memory peripheral address density is low so that simple address decoding can be used. Interrupt handling can also require many additional components, and using an interface device will usually simplify the system in this case.

NOTE: All typical values have been characterized but are not tested.

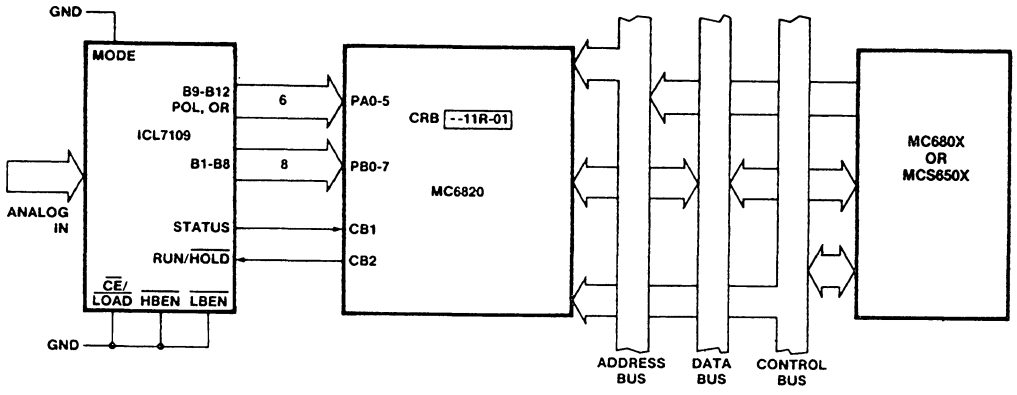


Figure 17: Full-time Parallel Interface to MC680X or MCS650X Microprocessors

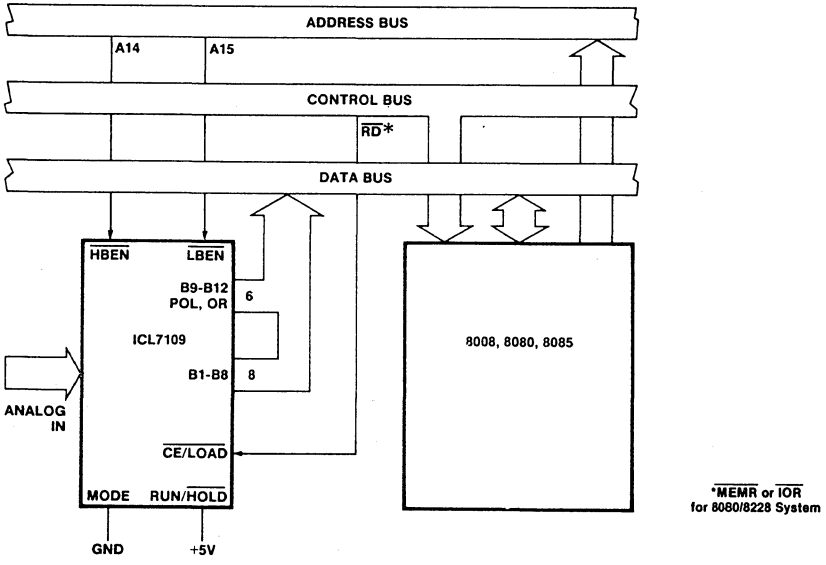


Figure 18: Direct Interface — ICL7109 to 8080/8085

NOTE: All typical values have been characterized but are not tested.

ICL7109

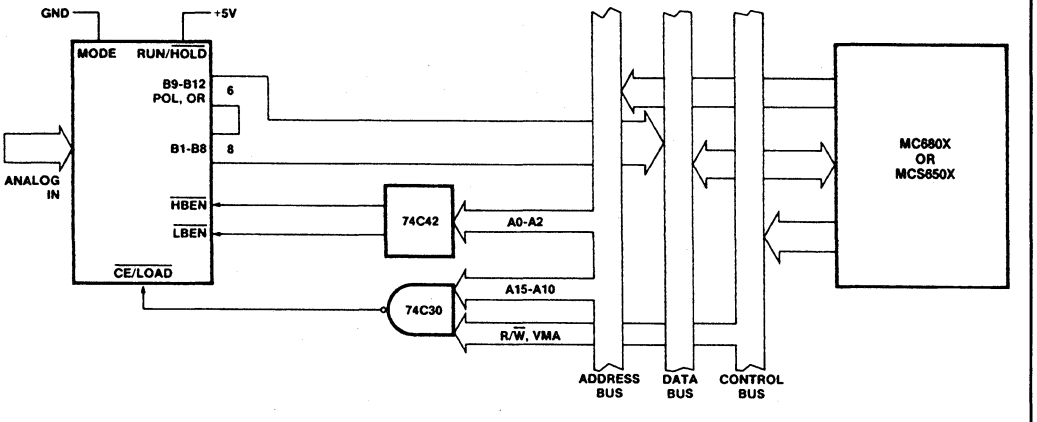


Figure 19: Direct ICL7109 — MC680X Bus Interface

Handshake Mode

The handshake mode allows ready interface with a wide variety of external devices. For instance, external latches may be clocked by the rising edge of $\overline{CE/LOAD}$, and the byte enables may be used as byte identification flags or as load enables.

Figure 20 shows a handshake interface to Intel microprocessors again using an 8255PPI. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the ICL7109, and using the $\overline{CE/LOAD}$ to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1 for the port used. If the 7109 is in handshake mode and the 8255 IBF flag is low, the next word will be strobed into the port. The strobe will cause IBF to go high (SEND goes low), which will keep the enabled byte outputs active. The PPI will generate an interrupt which when executed will result in the data being read. When the byte is read, the IBF will be reset low, which causes the ICL7109 to sequence into the next byte. This figure shows the MODE input to the ICL7109 connected to a control line on the PPI. If this output is left high, or tied high separately, the data from every conversion (provided the data access takes less time than a conversion) will be sequenced in two bytes into the system.

If this output is made to go from low to high, the output sequence can be obtained on demand, and the interrupt may be used to reset the MODE bit. Note that the RUN/$\overline{HOLD}$ input to the ICL7109 may also be driven by a bit of the 8255 so that conversions may be obtained on command under software control. Note that one port of the 8255 is not used, and can service another peripheral device. The same arrangement can also be used with the 8155.

Figure 21 shows a similar arrangement with the MC6800 or MCS650X microprocessors, except that both MODE and RUN/$\overline{HOLD}$ are tied high to save port outputs.

The handshake mode is particularly convenient for directly interfacing to industry standard UARTs (such as the Harris IM6402/6403 or Western Digital TR1602) providing a minimum component count means of serially transmitting converted data. A typical UART connection is shown in Figure 2A. In this circuit, any word received by the UART causes the UART DR (Data Ready) output to go high. This drives the MODE input to the ICL7109 high, triggering the ICL7109 into handshake mode. The high order byte is output to the UART first, and when the UART has transferred the data to the Transmitter Register, TBRE (SEND) goes high and the second byte is output. When TBRE (SEND) goes high again, $\overline{LBEN}$ will go high, driving the UART DRR (Data Ready Reset) which will signal the end of the transfer of data from the ICL7109 to the UART.

Figure 22 shows an extension of the one converter — one UART scheme to several ICL7109s with one UART. In this circuit, the word received by the UART (available at the RBR outputs when DR is high) is used to select which converter will handshake with the UART. With no external components, this scheme will allow up to eight ICL7109s to interface with one UART. Using a few more components to decode the received word will allow up to 256 converters to be accessed on one serial line.

NOTE: All typical values have been characterized but are not tested.

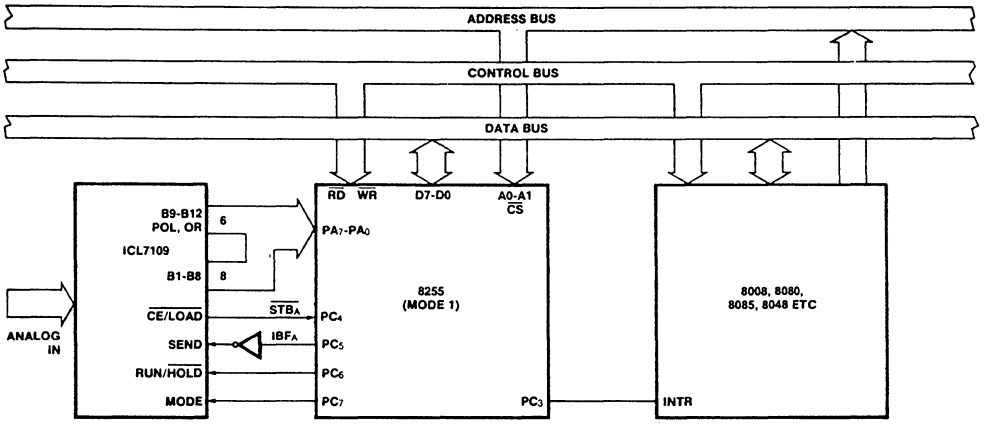


Figure 20: Handshake Interface — ICL7109 to 8048, 80/85

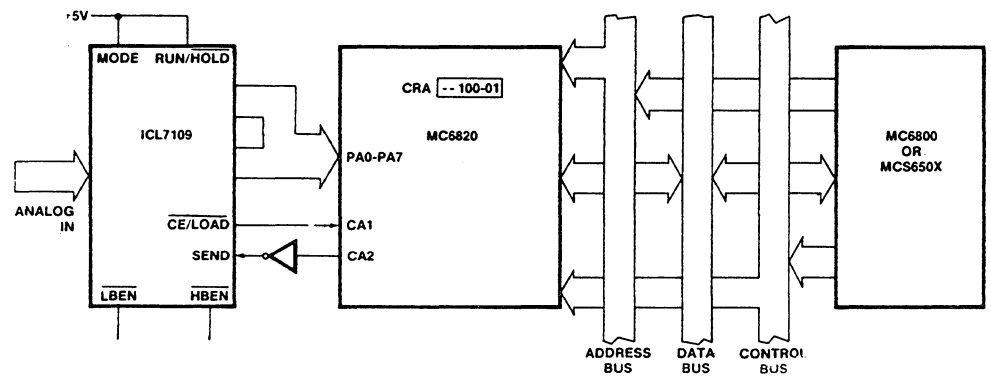


Figure 21: Handshake Interface — ICL7109 to MC6800, MCS650X

NOTE: All typical values have been characterized but are not tested.

ICL7109

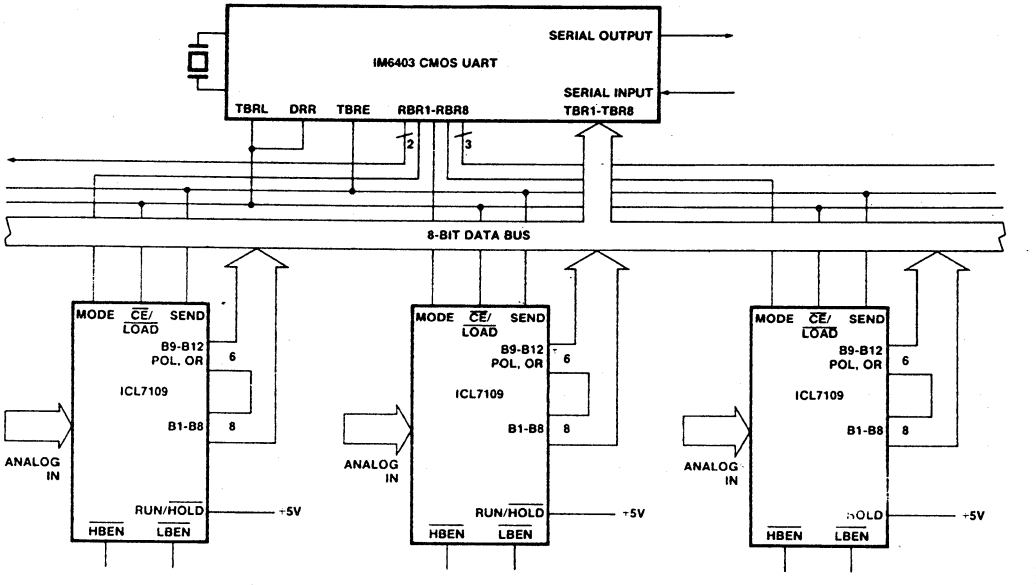


Figure 22: Multiplexing Converters with Mode Input

The applications of the ICL7109 are not limited to those shown here. The purpose of these examples is to provide a starting point for users to develop useful systems, and to show some of the variety of interfaces and uses of the ICL7109. Many of the ideas suggested here may be used in combination; in particular the uses of the STATUS, RUN/HOLD, and MODE signals may be mixed.

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar

A017 "The Integrating A/D Converters," by Lee Evans

A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood

A030 "The ICL7104 — A Binary Output A/D Converter for Microprocessors," by Peter Bradshaw

A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106 Family," by Peter Bradshaw

R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

NOTE: All typical values have been characterized but are not tested.

ICL7109
INTEGRATING A/D CONVERTER
EQUATIONS

Oscillator Frequency
$f_{OSC} = 0.45/RC$
$C_{OSC} > 50$ pF; $R_{OSC} > 50$ kΩ
f_{OSC} typ. = 60 kHz
or
$f_{OSC} = 3.58$ MHz Crystal

Oscillator Period
$t_{OSC} = RC/0.45$
$t_{OSC} = 1/3.58$ MHz (Crystal)

Integration Clock Frequency
$f_{CLOCK} = f_{OSC}$ (RC Mode)
$f_{CLOCK} = f_{OSC}/58$ (Crystal)
$t_{CLOCK} = 1/f_{CLOCK}$

Integration Period
$t_{INT} = 2048 \times t_{CLOCK}$

60/50 Hz Rejection Criterion
$t_{INT}/t_{60\ Hz}$ or $t_{INT}/t_{50\ Hz}$ = Integer

Optimum Integration Current
$I_{INT} = 20.0\ \mu A$

Full Scale Analog Input Voltage
V_{INFS} Typically = 200 mV or 2.0V

Integrate Resistor
$$R_{INT} = \frac{V_{INFS}}{I_{INT}}$$

Integrate Capacitor
$$C_{INT} = \frac{(t_{INT})(I_{INT})}{V_{INT}}$$

Integrator Output Voltage Swing
$$V_{INT} = \frac{(t_{INT})(I_{INT})}{C_{INT}}$$
V_{INT} Maximum Swing:
$(V^- + 0.5V) < V_{INT} < (V^+ - 0.5V)$
V_{INT} Typically = 2.0V

Display Count
$$COUNT = 2048 \times \frac{V_{IN}}{V_{REF}}$$

Conversion Cycle
$t_{CYC} = t_{CLOCK} \times 8192$
(In Free-Run Mode, Run/$\overline{HOLD}$ = 1)
when $f_{CLOCK} = 60$ kHz, $t_{CYC} = 133$ ms

Common Mode Input Voltage
$(V^- + 1.0V) < V_{IN} < (V^+ - 0.5V)$

Auto Zero Capacitor
$0.01\ \mu F < C_{AZ} < 1.0\ \mu F$

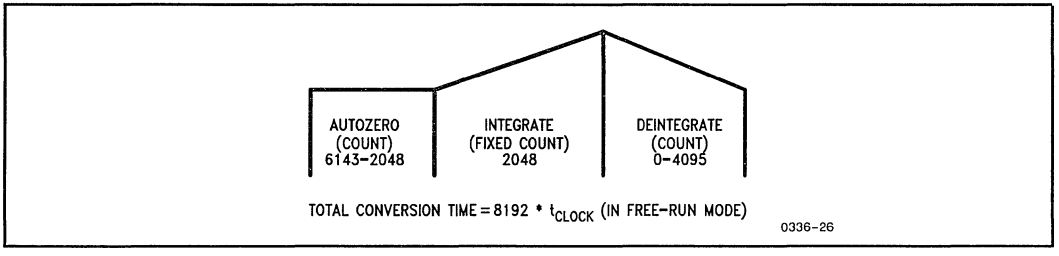
Reference Capacitor
$0.1\ \mu F < C_{REF} < 1.0\ \mu F$

V_{REF}
Biased between V^+ and V^-
$V_{REF} \cong V^+ - 2.8V$
Regulation lost when V^+ to $V^- \leq 6.4V$
If V_{REF} is not used, float output pin.

Power Supply: Dual ±5.0V
$V^+ = +5.0$ to GND
$V^- = -5.0$ to GND

Output Type:
Binary Amplitude with Polarity and Overrange Bits

Tips: Always tie TEST pin HIGH.
Don't leave any inputs floating.



NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICL7135
4½-Digit BCD Output A/D Converter

GENERAL DESCRIPTION

The Harris ICL7135 precision A/D converter, with its multiplexed BCD output and digit drivers, combines dual-slope conversion reliability with ±1 in 20,000 count accuracy and is ideally suited for the visual display DVM/DPM market. The 2.0000V full scale capability, auto-zero and auto-polarity are combined with true ratiometric operation, almost ideal differential linearity and true differential input. All necessary active devices are contained on a single CMOS I.C., with the exception of display drivers, reference, and a clock.

The intersil ICL7135 brings together an unprecedented combination of high accuracy, versatility, and true economy. It features auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10 pA max., and rollover error of less than one count. The versatility of multiplexed BCD outputs is increased by the addition of several pins which allow it to operate in more sophisticated systems. These include $\overline{\text{STROBE}}$, OVERRANGE, UNDER-RANGE, RUN/$\overline{\text{HOLD}}$ and BUSY lines, making it possible to interface the circuit to a microprocessor or UART.

FEATURES

- **Accuracy Guaranteed to ±1 Count Over Entire ±20,000 Counts (2.0000 Volts Full Scale)**
- **Guaranteed Zero Reading for 0 Volts Input**
- **1pA Typical Input Current**
- **True Differential Input**
- **True Polarity at Zero Count for Precise Null Detection**
- **Single Reference Voltage Required**
- **Over-Range and Under-Range Signals Available for Auto-Range Capability**
- **All Outputs TTL Compatible**
- **Blinking Outputs Gives Visual Indication of Over-range**
- **Six Auxiliary Inputs/Outputs Are Available for Interfacing to UARTs, Microprocessors or Other Circuitry**
- **Multiplexed BCD Outputs**

ORDERING INFORMATION

Part Number	Temp. Range	Package
ICL7135CJI	0°C to +70°C	28-Pin CERDIP
ICL7135CPI	0°C to +70°C	28-Pin Plastic DIP

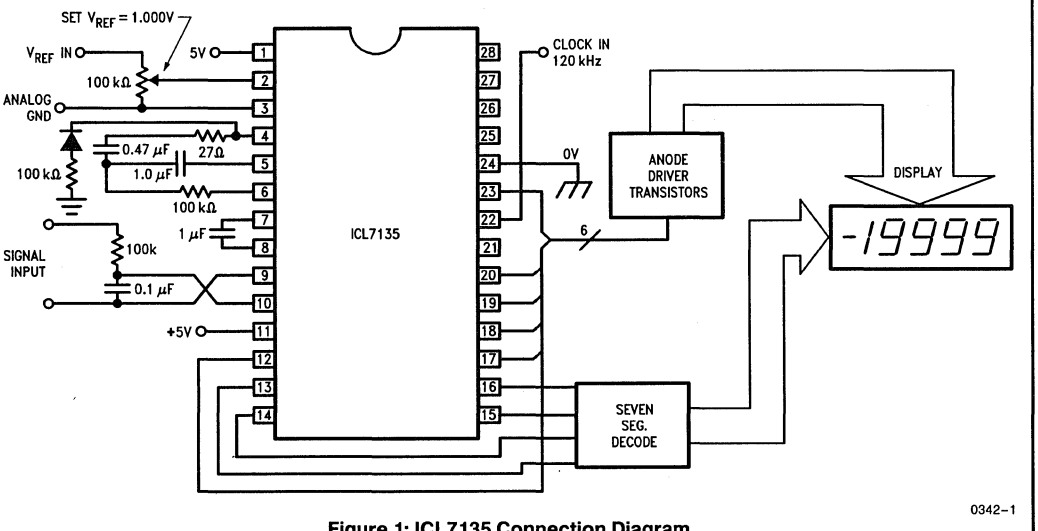


Figure 1: ICL7135 Connection Diagram

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V^+ ..... +6V
V^- ..... −9V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Gnd to V^+

Power Dissipation (Note 2)
Ceramic Package 1000mW
Plastic Package 800mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to +100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

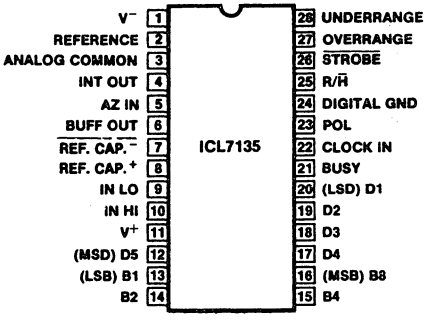


Figure 2: Pin Configuration
Outline dwgs JI, PI)

ELECTRICAL CHARACTERISTICS (Note 1)

($V^+ = +5V$, $V^- = -5V$, $T_A = 25°C$, Clock Frequency Set for 3 Reading/Sec)

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
ANALOG (Note 1) (Note 2)						
	Zero Input Reading	$V_{IN} = 0.0V$ $V_{REF} = 1.000V$	−00000	±00000	+00000	Counts
	Ratiometric Error (2)	$V_{IN} = V_{REF} = 1.000V$	−3	−1	0	Counts
	Linearity over ± Full Scale (error of reading from best straight line)	$-2V \le V_{IN} \le +2V$		0.5	1	LSB
	Differential Linearity (difference between worse case step of adjacent counts and ideal step)	$-2V \le V_{IN} \le +2V$		.01		LSB
	Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{IN} \equiv +V_{IN} \approx 2V$		0.5	1	LSB

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Note 1)

($V^+ = +5V$, $V^- = -5V$, $T_A = 25°C$, Clock Frequency Set for 3 Reading/Sec) (Continued)

Symbol	Characteristics	Test Conditions	Min	Typ	Max	Unit
e_n	Noise (P-P value not exceeded 95% of time)	$V_{IN} = 0V$ Full scale = 2.000V		15		μV
I_{ILK}	Leakage Current at Input	$V_{IN} = 0V$		1	10	pA
	Zero Reading Drift	$V_{IN} = 0V$ $0° \leq T_A \leq 70°C$		0.5	2	μV/°C
TC	Scale Factor Temperature Coefficient (3)	$V_{IN} = +2V$ $0 \leq T_A \leq 70°C$ (ext. ref. 0 ppm/°C)		2	5	ppm/°C
DIGITAL						
INPUTS						
V_{INH}			2.8	2.2		V
V_{INL}				1.6	0.8	
I_{INL}	Clock in, Run/$\overline{\text{Hold}}$, See Figure 4	$V_{IN} = 0$		0.02	0.1	mA
I_{INH}		$V_{IN} = +5V$		0.1	10	μA
OUTPUTS						
V_{OL}	All Outputs	$I_{OL} = 1.6mA$		0.25	0.40	V
V_{OH}	B_1, B_2, B_4, B_8 D_1, D_2, D_3, D_4, D_5	$I_{OH} = -1mA$	2.4	4.2		V
V_{OH}	BUSY, $\overline{\text{STROBE}}$, OVER-RANGE, UNDER-RANGE POLARITY	$I_{OH} = -10\mu A$	4.9	4.99		V
SUPPLY						
V^+	+5V Supply Range		+4	+5	+6	V
V^-	−5V Supply Range		−3	−5	−8	V
I^+	+5V Supply Current	$f_C = 0$		1.1	3.0	mA
I^-	−5V Supply Current	$f_C = 0$		0.8	3.0	
C_{PD}	Power Dissipation Capacitance	vs. Clock Freq		40		pF
CLOCK						
	Clock Freq. (Note 4)		DC	2000	1200	kHz

NOTES: 1. Tested in 4-½ digit (20,000 count) circuit shown in Figure 3, clock frequency 120kHz.

2. Tested with a low dielectric absorption integrating capacitor, the 27Ω INT. OUT resistor shorted, and $R_{INT} = 0$. See Component Selection Section.

3. The temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the ICL7135.

4. This specification relates to the clock frequency range over which the ICL7135 will correctly perform its various functions. See "Max Clock Frequency" section for limitations on the clock frequency range in a system.

NOTE: All typical values have been characterized but are not tested.

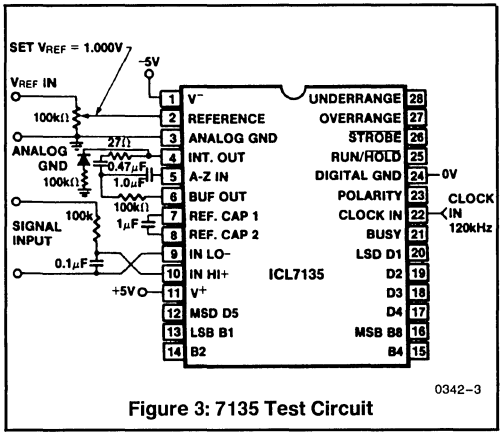


Figure 3: 7135 Test Circuit

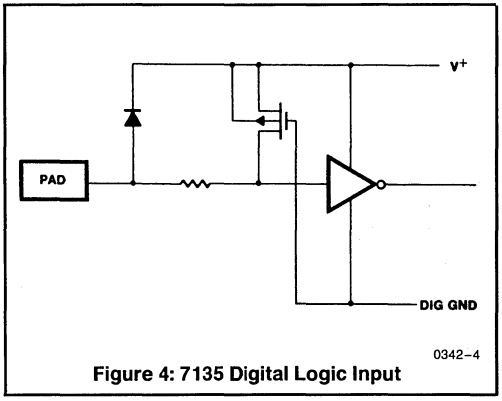


Figure 4: 7135 Digital Logic Input

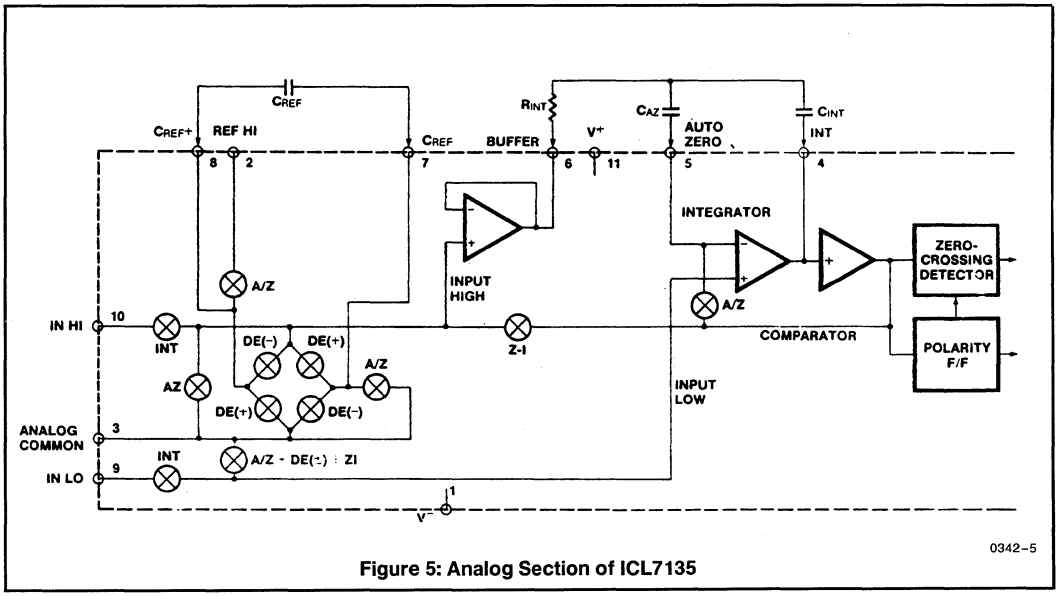


Figure 5: Analog Section of ICL7135

NOTE: All typical values have been characterized but are not tested.

ICL7135

DETAILED DESCRIPTION

Analog Section

Figure 5 shows the Block Diagram of the Analog Section for the ICL7135. Each measurement cycle is divided into four phases. They are (1) auto-zero (A-Z), (2) signal-integrate (INT), (3) deintegrate (DE) and (4) zero-integrator (ZI).

AUTO-ZERO PHASE

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

SIGNAL INTEGRATE PHASE

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is latched into the polarity F/F.

DE-INTEGRATE PHASE

The Third phase is de-integrate, or reference integrate. Input LOW is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is:

$$\text{OUTPUT COUNT} = 10{,}000 \left(\frac{V_{IN}}{V_{REF}}\right).$$

ZERO INTEGRATOR PHASE

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal condition, this phase lasts from 100 to 200 clock pulses, but after an overrange conversion, it is extended to 6200 clock pulses.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full scale swing with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

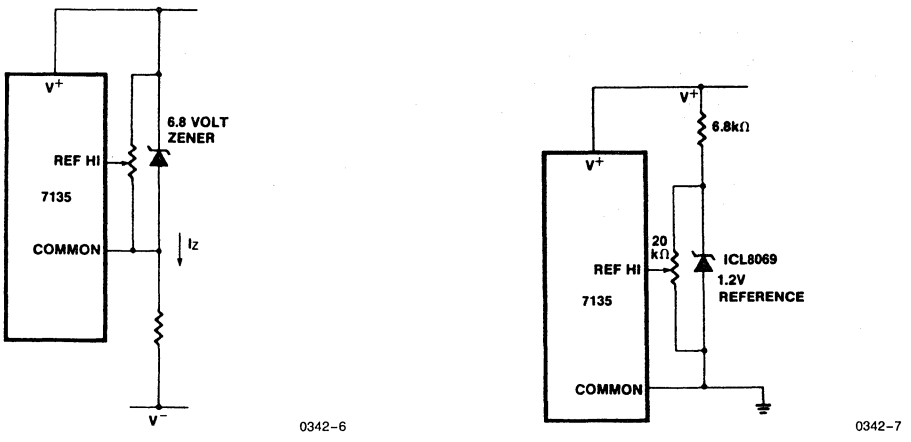


Figure 6: Using an External Reference

NOTE: All typical values have been characterized but are not tested.

Analog Common

Analog COMMON is used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in most applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The reference voltage is referenced to analog COMMON.

Reference

The reference input must be generated as a positive voltage with respect to COMMON, as shown in Figure 6.

DETAILED DESCRIPTION

Digital Section

Figure 7 shows the Digital Section of the 7135. The 7135 includes several pins which allow it to operate conveniently in more sophisticated systems. These include:

Run/$\overline{\text{HOLD}}$ (Pin 25). When high (or open) the A/D will free-run with equally spaced measurement cycles every 40,002 clock pulses. If taken low, the converter will continue the full measurement cycle that it is doing and then hold this reading as long as R/$\overline{\text{H}}$ is held low. A short positive pulse (greater than 300ns) will now initiate a new measurement cycle, beginning with between 1 and 10,001 counts of auto zero. If the pulse occurs before the full measurement cycle (40,002 counts) is completed, it will not be recognized and the converter will simply complete the measurement it is doing. An external indication that a full measurement cycle has been completed is that the first strobe pulse (see below) will occur 101 counts after the end of this cycle. Thus, if Run/$\overline{\text{HOLD}}$ is low and has been low for at least 101 counts, the converter is holding and ready to start a new measurement when pulsed high.

$\overline{\text{STROBE}}$ (Pin 26). This is a negative going output pulse that aids in transferring the BCD data to external latches, UARTs or microprocessors. There are 5 negative going $\overline{\text{STROBE}}$ pulses that occur in the center of each of the digit drive pulses and occur once and only once for each measurement cycle starting 101 pulses after the end of the full measurement cycle. Digit 5 (MSD) goes high at the end of the measurement cycle and stays on for 201 counts. In the center of this digit pulse (to avoid race conditions between changing BCD and digit drives) the first $\overline{\text{STROBE}}$ pulse goes negative for ½ clock pulse width. Similarly, after digit 5, digit 4 goes high (for 200 clock pulses) and 100 pulses later the $\overline{\text{STROBE}}$ goes negative for the second time. This continues through digit 1 (LSD) when the fifth and last $\overline{\text{STROBE}}$ pulse is sent. The digit drive will continue to scan (unless the previous signal was overrange) but no additional $\overline{\text{STROBE}}$ pulses will be sent until a new measurement is available.

BUSY (Pin 21). BUSY goes high at the beginning of signal integrate and stays high until the first clock pulse after zero-crossing (or after end of measurement in the case of an overrange). The internal latches are enabled (i.e., loaded) during the first clock pulse after busy and are latched at the end of this clock pulse. The circuit automatically reverts to auto-zero when not BUSY, so it may also be considered a $(\overline{\text{ZI}}+\overline{\text{AZ}})$ signal. A very simple means for transmitting the data down a single wire pair from a remote location would be to AND BUSY with clock and subtract 10,001 counts from the number of pulses received - as mentioned previously there is one "NO-count" pulse in each reference integrate cycle.

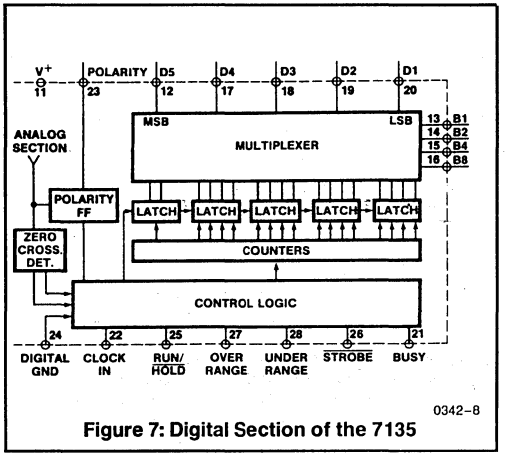


Figure 7: Digital Section of the 7135

OVER-RANGE (Pin 27). This pin goes positive when the input signal exceeds the range (20,000) of the converter. The output F/F is set at the end of BUSY and is reset to zero at the beginning of Reference integrate in the next measurement cycle.

UNDER-RANGE (Pin 28). This pin goes positive when the reading is 9% of range or less. The output F/F is set at the end of BUSY (if the new reading is 1800 or less) and is reset at the beginning of signal integrate of the next reading.

POLARITY (Pin 23). This pin is positive for a positive input signal. It is valid even for a zero reading. In other words, +0000 means the signal is positive but less than the least significant bit. The converter can be used as a null detector by forcing equal frequency of (+) and (−) readings. The null at this point should be less than 0.1 LSB. This output becomes valid at the beginning of reference integrate and remains correct until it is re-validated for the next measurement.

Digit Drives (Pins 12, 17, 18, 19 and 20). Each digit drive is a positive going signal that lasts for 200 clock pulses. The scan sequence is D_5 (MSD), D_4, D_3, D_2 and D_1 (LSD). All five digits are scanned and this scan is continuous unless an over-range occurs. Then all digit drives are blanked from the end of the strobe sequence until the beginning of Reference Integrate when D_5 will start the scan again. This can give a blinking display as a visual indication of over-range.

BCD (Pins 13, 14, 15 and 16). The Binary coded Decimal bits B_8, B_4, B_2 and B_1 are positive logic signals that go on simultaneously with the digit driver signal.

NOTE: All typical values have been characterized but are not tested.

ICL7135

COMPONENT VALUE SELECTION

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. Values of 5 to 40μA give good results, with a nominal of 20μA, and the exact value of integrating resistor may be chosen by

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor should be selected to give the maximum voltage swing which ensures that the tolerance built-up will not saturate the integrator swing (approx. 0.3 volt from either supply). For ±5 volt supplies and analog COMMON tied to supply ground, a ±3.5 to ±4 volt full scale integrator swing is fine, and 0.47μF is nominal. In general, the value of C_{INT} is given by

$$C_{INT} = \left(\frac{[10{,}000 \times \text{clock period}] \times I_{INT}}{\text{integrator output voltage swing}}\right)$$

$$= \frac{(10{,}000)\ (\text{clock period})\ (20\mu A)}{\text{integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale 0.9999, and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

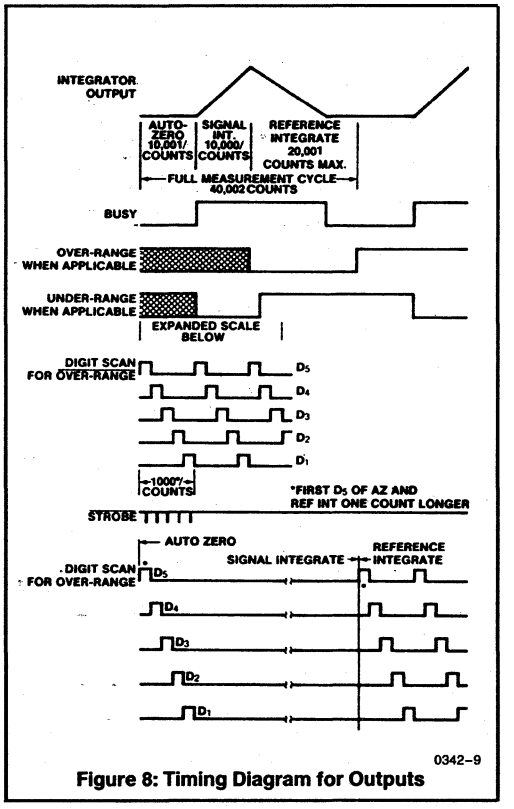


Figure 8: Timing Diagram for Outputs

Auto-Zero and Reference Capacitor

The physical size of the auto-zero capacitor has an influence on the noise of the system. A larger capacitor value reduces system noise. A larger physical size increases system noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

NOTE: All typical values have been characterized but are not tested.

The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full-scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high quality reference be used where high-accuracy absolute measurements are being made.

Rollover Resistor and Diode

A small rollover error occurs in the 7135, but this can be easily corrected by adding a diode and resistor in series between the INTegrator OUTput and analog COMMON or ground. The value shown in the schematics is optimum for the recommended conditions, but if integrator swing or clock frequency is modified, adjustment may be needed. The diode can be any silicon diode, such as 1N914. These components can be eliminated if rollover error is not important, and may be altered in value to correct other (small) sources of rollover as needed.

Max Clock Frequency

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3μs delay, and at a clock frequency of 160kHz (6μs period) half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50μV input, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at mid-point is considered desirable by most users; however, if the clock frequency is increased appreciably above 160kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many-dedicated applications where the input signal is always of one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, clock rates of up to ~1MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be constant and can be subtracted out digitally.

The clock frequency may be extended above 160kHz without this error, however, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the reference integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second order breaks will cause significant nonlinearities in the first few counts of the instrument - see Application Note A017.

The minimum clock frequency is established by leakage on the auto-zero and reference caps. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 300kHz, 200kHz, 150kHz, 120kHz, 100kHz, 40kHz, 33⅓kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 250kHz, 166⅔kHz, 125kHz, 100kHz, etc. would be suitable. Note that 100kHz (2.5 readings/second) will reject both 50 and 60Hz.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the Applications section. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

Zero-Crossing Flip-Flop

The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of phase 3. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2, so that true ratiometric readings result.

EVALUATING THE ERROR SOURCES

Errors from the "ideal" cycle are caused by:

1. Capacitor droop due to leakage.
2. Capacitor voltage change due to charge "suck-out" (the reverse of charge injection) when the switches turn off.
3. Non-linearity of buffer and integrator.
4. High-frequency limitations of buffer, integrator and comparator.
5. Integrating capacitor non-linearity (dielectric absorption.)
6. Charge lost by C_{REF} in charging C_{stray}.
7. Charge lost by C_{AZ} and C_{INT} to charge C_{stray}.

Each of these errors is analyzed for its error contribution to the converter in application notes listed on the back page, specifically A017 and A032.

NOISE

The peak-to-peak noise around zero is approximately 15μV (pk-to-pk value not exceeded 95% of the time). Near full scale, this value increases to approximately 30μV. Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of ICL7135 circuits, especially in high-sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line.

NOTE: All typical values have been characterized but are not tested.

POWER SUPPLIES

The 7135 is designed to work from ±5V supplies. However, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts.

See "differential input" for a discussion of the effects this will have on the integrator swing without loss of linearity.

TYPICAL APPLICATIONS

The circuits which follow show some of the wide variety of possibilities, and serve to illustrate the exceptional versatility of this A/D converter.

Figure 9 shows the complete circuit for a 4-½ digit (±2.000V) full scale) A/D with LED readout using the ICL8069 as a 1.2V temperature compensated voltage reference. It uses the band-gap principal to achieve excellent stability and low noise at reverse currents down to 50μA. The circuit also shows a typical R-C input filter. Depending on the application, the time-constant of this filter can be made faster, slower, or the filter deleted completely. The ½ digit LED is driven from the 7 segment decoder, with a zero reading blanked by connecting a D5 signal to RBI input of the decoder. The 2-gate clock circuit should use CMOS gates to maintain good power supply rejection.

A suitable circuit for driving a plasma-type display is shown in Figure 10. The high voltage anode driver buffer is made by Dionics. The 3 AND gates and caps driving 'BI' are needed for interdigit blanking of multiple-digit display elements, and can be omitted if not needed. The 2.5kΩ & 3kΩ resistors set the current levels in the display. A similar arrangement can be used with Nixie® tubes.

The popular LCD displays can be interfaced to the O/P of the ICL7135 with suitable display drivers, such as the ICM7211A as shown in Figure 11. A standard CMOS 4030 QUAD XOR gate is used for displaying the ½ digit, the polarity, and an 'overrange' flag. A similar circuit can be used with the ICL7212A LED driver and the ICM7235A vacuum fluorescent driver with appropriate arrangements made for the 'extra' outputs. Of course, another full driver circuit could be ganged to the one shown if required. This would be useful if additional annunciators were needed. The Figure shows the complete circuit for a 4-½ digit (±2,000V) A/D.

Figure 12 shows a more complicated circuit for driving LCD displays. Here the data is latched into the ICM7211 by the $\overline{\text{STROBE}}$ signal and 'Overrange' is indicated by blanking the 4 full digits.

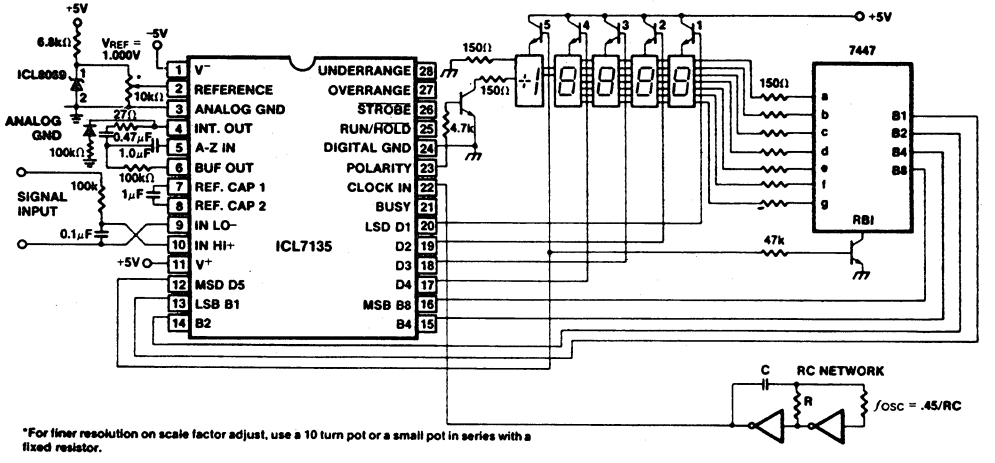


Figure 9: 4-½ Digit A/D Converter with a Multiplexed Common Anode LED Display

NOTE: All typical values have been characterized but are not tested.

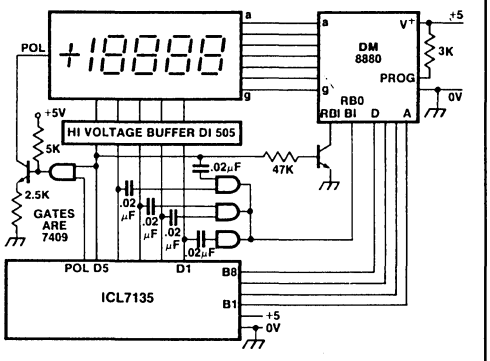


Figure 10: ICL7135 Plasma Display Circuit

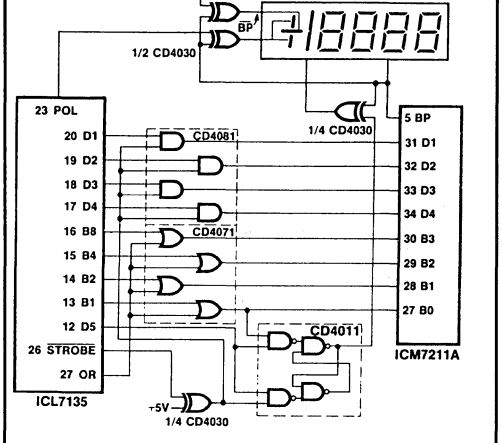


Figure 11: LCD Display with Digit Blanking on Overrange

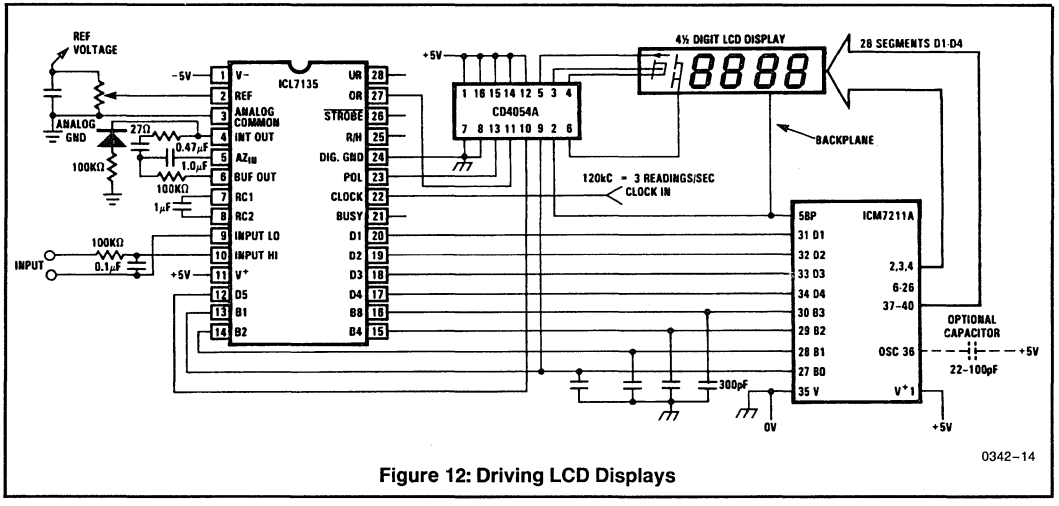


Figure 12: Driving LCD Displays

NOTE: All typical values have been characterized but are not tested.

A problem sometimes encountered with both LED & plasma-type display driving is that of clock source supply line variations. Since the supply is shared with the display, any variation in voltage due to the display reading may cause clock supply voltage modulation. When in overrange the display alternates between a blank display and the 0000 overrange indication. This shift occurs during the reference integrate phase of conversion causing a low display reading just after overrange recovery. Both of the above circuits have considerable current flowing in the digital supply from drivers, etc. A clock source using an LM311 voltage comparator with positive feedback (Figure 13) could minimize any clock frequency shift problem.

The 7135 is designed to work from ±5 volt supplies. However, if a negative supply is not available, it can be generated with an ICL7660 and two capacitors (Figure 14).

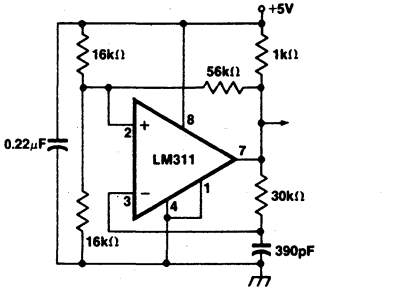


Figure 13: LM311 Clock Source

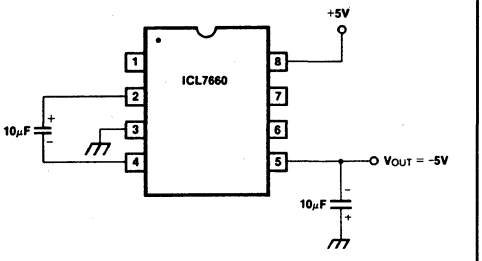


Figure 14: Generating a Negative Supply from +5V

INTERFACING WITH UARTS AND MICROPROCESSORS

Figure 15 shows a very simple interface between a free-running ICL7135 and a UART. The five $\overline{\text{STROBE}}$ pulses start the transmission of the five data words. The digit 5 word is 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. Also the polarity is transmitted indirectly by using it to drive the Even Parity Enable Pin (EPE). If EPE of the receiver is held low, a parity flag at the receiver can be decoded as a positive signal, no flag as negative. A complex arrangement is shown in Figure 16. Here the UART can instruct the A/D to begin a measurement sequence by a word on RRI. The BUSY signal resets the Data Ready Reset (DRR). Again $\overline{\text{STROBE}}$ starts the transmit sequence. A quad 2 input multiplexer is used to superimpose polarity, over-range, and under-range onto the D_5 word since in this instance it is known that $B_2 = B_4 = B_8 = 0$.

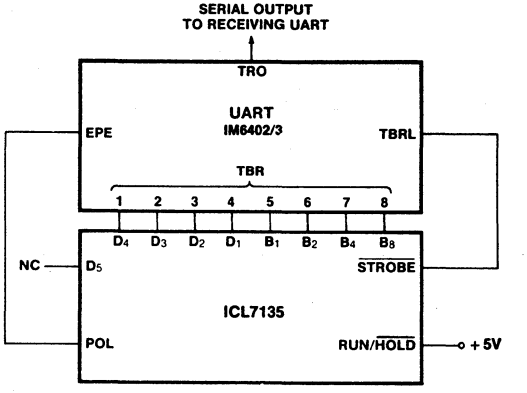
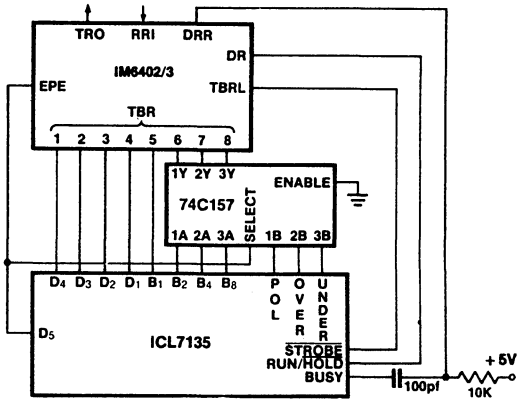


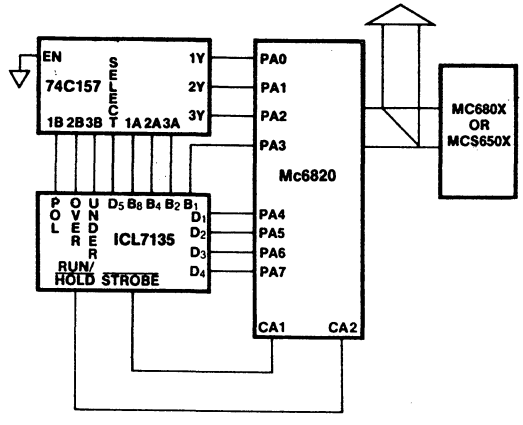
Figure 15: ICL7135 to UART Interface

NOTE: All typical values have been characterized but are not tested.



0342-18

Figure 16: Complex ICL7135 to UART Interface



0342-19

Figure 17: ICL7135 to MC6800, MCS650X Interface

3

NOTE: All typical values have been characterized but are not tested.

ICL7135

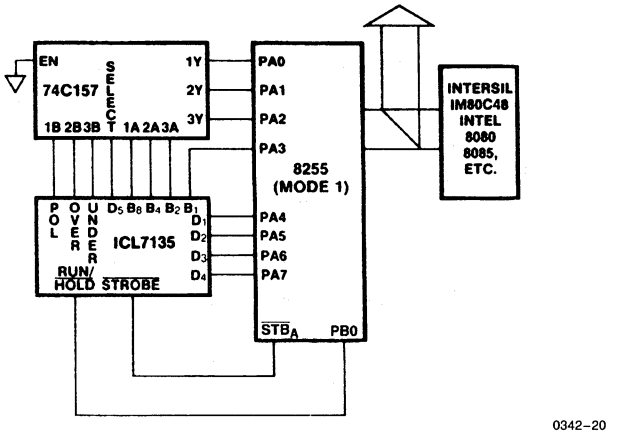


Figure 18: ICL7135 to MCS-48, −80, 85 Interface

For correct operation it is important that the UART clock be fast enough that each word is transmitted before the next $\overline{\text{STROBE}}$ pulse arrives. Parity is locked into the UART at load time but does not change in this connection during an output stream.

Circuits to interface the ICL7135 directly with three popular microprocessors are shown in Figures 17 and 18. The 8080/8048 and the MC6800 groups with 8 bit buses need to have polarity, over-range and under-range multiplexed onto the Digit 5 word — as in the UART circuit. In each case the microprocessor can instruct the A/D when to begin a measurement and when to hold this measurement.

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar

A017 "The Integrating A/D Converters," by Lee Evans

A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood

A023 "Low Cost Digital Panel Meter Designs," by David Fullager and Michael Dufort

A028 "Building an Auto-Ranging DMM Using the 8052A/7103A A/D Converter Pair," by Larry Goff

A030 "The ICL7104 — A Binary Output A/D Converter for Microprocessors", by Peter Bradshaw

A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106 Family", by Peter Bradshaw

R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976

NOTE: All typical values have been characterized but are not tested.

ICL7135
INTEGRATING A/D CONVERTER
EQUATIONS

Clock Input

The ICL7135 does not have an internal oscillator. It requires an external clock

f_{CLOCK} typ = 120 KHz

Clock Period

$t_{CLOCK} = 1/f_{CLOCK}$

Integration Period

$t_{INT} = 10000 \times t_{CLOCK}$

60/50 Hz Rejection Criterion

t_{INT}/t_{60Hz} or t_{INT}/t_{50Hz} = Integer

Optimum Integration Current

$I_{INT} = 20.0\ \mu A$

Full Scale Analog Input Voltage

V_{INFS} Typically = 200 mV or 2.0V

Integrate Resistor

$$R_{INT} = \frac{(V_{INFS})}{(I_{INT})}$$

Integrate Capacitor

$$C_{INT} = \frac{(t_{INT})\,(I_{INT})}{(V_{INT})}$$

Integrator Output Voltage Swing

$$V_{INT} = \frac{(t_{INT})\,(I_{INT})}{(C_{INT})}$$

V_{INT} Maximum Swing:

$(V^- + 0.5) < V_{INT} < (V^+ - 0.5V)$

V_{INT} typically = 2.7V

Display Count

$$COUNT = 10000 \times \frac{V_{IN}}{V_{REF}}$$

Conversion Cycle

$t_{CYC} = t_{CLOCK} \times 40002$

when f_{CLOCK} = 120 KHz, t_{CYC} = 333 ms

Common Mode Input Voltage

$(V^- + 1.0V) < V_{IN} < (V^+ - 0.5V)$

Auto Zero Capacitor

$0.01\ \mu F < C_{AZ} < 1.0\ \mu F$

Reference Capacitor

$0.1\ \mu F < C_{REF} < 1.0\ \mu F$

Power Supply: Dual ±5.0V

$V^+ = +5.0$ to GND

$V^+ = -5.0$ to GND

Output Type:

4 BCD Nibbles With

Polarity and Overrange Bits

There is no internal reference available on the ICL7135. An external reference is required due to the 7135's 4½ digit resolution.

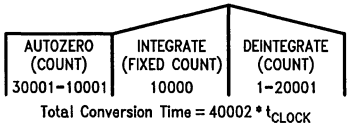


Figure 19

NOTE: All typical values have been characterized but are not tested.

DATA ACQUISITION 4

A/D SUCCESSIVE APPROXIMATION

HARRIS SEMICONDUCTOR

ADC0802 - ADC0804
8-Bit μP-Compatible A/D Converters

GENERAL DESCRIPTION

The ADC0802 family are CMOS 8-bit successive approximation A/D converters which use a modified potentiometric ladder, and are designed to operate with the 8080A control bus via three-state outputs. These converters appear to the processor as memory locations or I/O ports, and hence no interfacing logic is required.

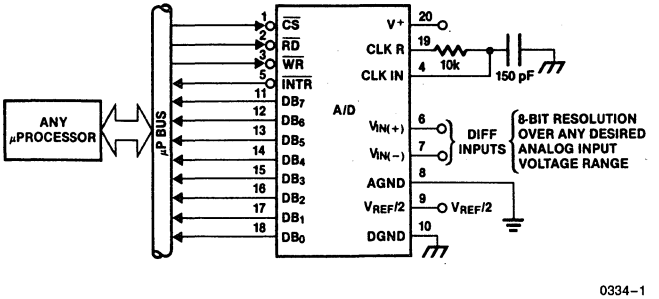
The differential analog voltage input has good common-mode-rejection, and permits offsetting the analog zero-input-voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

FEATURES

- **80C48 and 80C80/85 Bus Compatible — No Interfacing Logic Required**
- **Conversion Time < 100μs**
- **Easy Interface to Most Microprocessors**
- **Will Operate in a "Stand Alone" Mode**
- **Differential Analog Voltage Inputs**
- **Works With Bandgap Voltage References**
- **TTL Compatible Inputs and Outputs**
- **On-Chip Clock Generator**
- **0V to 5V Analog Voltage Input Range (Single +5V Supply)**
- **No Zero-Adjust Required**

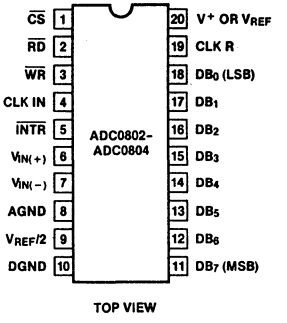
ORDERING INFORMATION

Part Number	Error	External Conditions	Temperature Range	Package
ADC0802LCN	±½ bit	$V_{REF}/2 = 2.500\ V_{DC}$	0°C to +70°C	20 pin Plastic DIP
ADC0802LCD	±¾ bit	(No Adjustments)	−40°C to +85°C	20 pin CERDIP
ADC0802LD	±1 bit		−55°C to +125°C	20 pin CERDIP
ADC0802LD/HR	±1 bit		−55°C to +125°C	20 pin CERDIP
ADC0803LCN	±½ bit	$V_{REF}/2$ Adjusted for	0°C to +70°C	20 pin Plastic DIP
ADC0803LCD	±¾ bit	Correct Full-Scale	−40°C to +85°C	20 pin CERDIP
ADC0803LD	±1 bit	Reading	−55°C to +125°C	20 pin CERDIP
ADC0804LCN	±1 bit	$V_{REF}/2 = 2.500\ V_{DC}$	0°C to +70°C	20 pin Plastic DIP
ADC0804LCD	±1 bit	(No Adjustments)	−40°C to +85°C	20 pin CERDIP



0334-1

Figure 1: Typical Application



TOP VIEW

0334-2

(Outline dwg. CD, CN)
Figure 2: Pin Configuration

NOTE: All typical values have been characterized but are not tested.

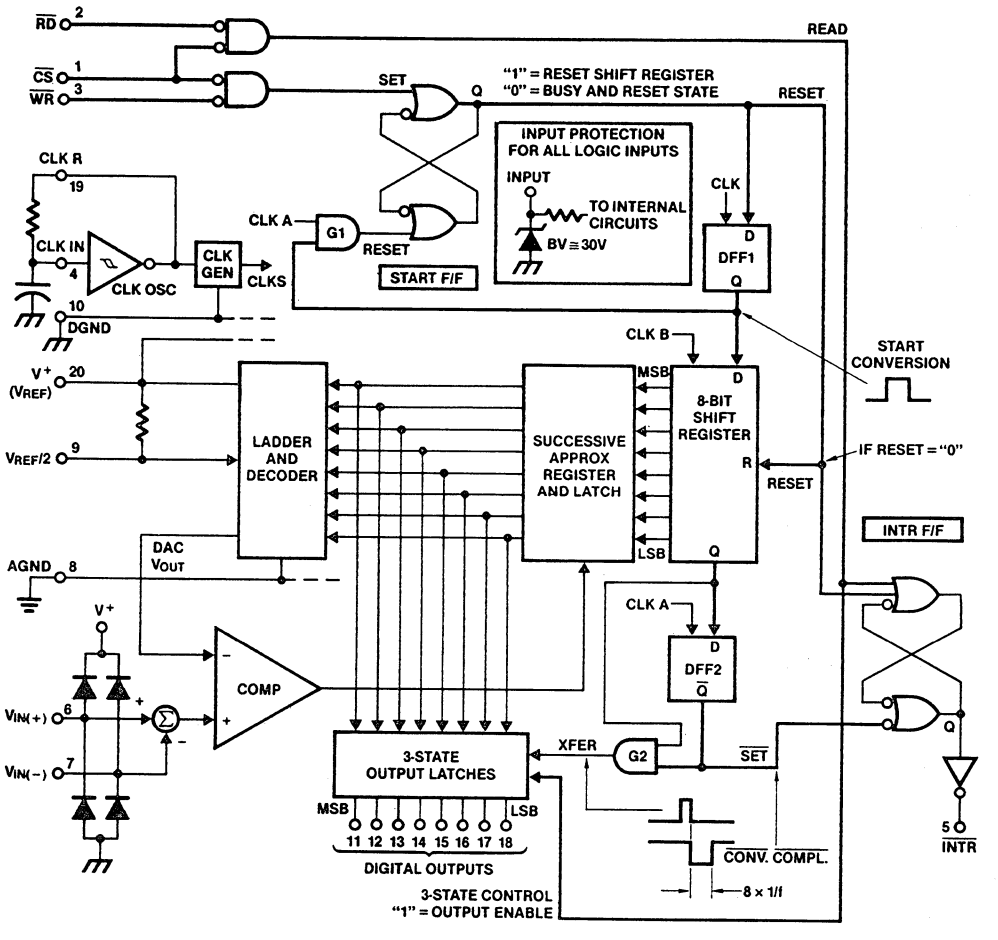


Figure 3: Functional Diagram of ADC0802–ADC0804

NOTE: All typical values have been characterized but are not tested.

ADC0802-ADC0804

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6.5V
Voltage at Any Input ..... −0.3V to (V^+ +0.3V)
Storage Temperature Range ..... −65°C to +150°C
Package Dissipation at T_A = +25°C 875mW
Lead Temperature (Soldering, 10sec) ..... 300°C

OPERATING RATINGS

Temperature Range
ADC0802/03LD ..... −55°C to +125°C
ADC0802/03/04LCD ..... −40°C to +85°C
ADC0802/03/04LCN ..... 0°C to +70°C
Supply Voltage Range ..... 4.5V to 6.3V

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS (Notes 1 and 7)

Converter Specifications: $V^+ = 5V$, $T_A = +25°C$ and $f_{CLK} = 640kHz$ unless otherwise stated.

Parameter	Test Conditions	Min	Typ	Max	Unit
ADC0802: Total Unadjusted Error	$V_{REF}/2 = 2.500V$			±½	LSB
ADC0803: Total Adjusted Error	$V_{REF}/2$ Adjusted for Correct Full-Scale Reading			±½	LSB
ADC0804: Total Unadjusted Error	$V_{REF}/2 = 2.500V$			±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3		kΩ
Analog Input Voltage Range	(Note 2)	GND−0.05		V^+ +0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range		±1/16	±⅛	LSB
Power Supply Sensitivity	$V^+ = 5V$ ±10% Over Allowed Input Voltage Range		± 1/16	± ⅛	LSB

Converter Specifications: $V^+ = 5V$, $0°C \le T_A \le +70°C$ and $f_{CLK} = 640$ kHz unless otherwise stated.

Parameter	Test Conditions	Min	Typ	Max	Unit
ADC0802: Total Unadjusted Error	$V_{REF}/2 = 2.500V$			±½	LSB
ADC0803: Total Adjusted Error	$V_{REF}/2$ Adjusted for Correct Full-Scale Reading			±½	LSB
ADC0804: Total Unadjusted Error	$V_{REF}/2 = 2.500V$			±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3		kΩ
Analog Input Voltage Range	(Note 2)	GND−0.05		V^+ +0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range		⅛	¼	LSB
Power Supply Sensitivity	$V^+ = 5V$ ±10% Over Allowed Input Voltage Range		±1/16	±⅛	LSB

NOTE: All typical values have been characterized but are not tested.

Converter Specifications: $V^+ = 5V$, $-25°C \leq T_A \leq +85°C$ and $f_{CLK} = 640$ kHz unless otherwise stated.

Parameter	Test Conditions	Min	Typ	Max	Unit
ADC0802: Total Unadjusted Error	$V_{REF}/2 = 2.500V$			$\pm 3/4$	LSB
ADC0803: Total Adjusted Error	$V_{REF}/2$ Adjusted for Correct Full-Scale Reading			$\pm 3/4$	LSB
ADC0804: Total Unadjusted Error	$V_{REF}/2 = 2.500V$			± 1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3		kΩ
Analog Input Voltage Range	(Note 2)	GND−0.05		$V^+ + 0.05$	V
DC Common-Mode Rejection	Over Analog Input Voltage Range		$\pm 1/8$	$\pm 1/4$	LSB
Power Supply Sensitivity	$V^+ = 5V \pm 10\%$ Over Allowed Input Voltage Range		$\pm 1/16$	$\pm 1/8$	LSB

Converter Specifications: $V^+ = 5V$, $-55°C \leq T_A \leq +125°C$ and $f_{CLK} = 640$ kHz unless otherwise stated.

Parameter	Test Conditions	Min	Typ	Max	Unit
ADC0802: Total Unadjusted Error	$V_{REF}/2 = 2.500V$			± 1	LSB
ADC0803: Total Adjusted Error	$V_{REF}/2$ Adjusted for Correct Full-Scale Reading			± 1	LSB
ADC0804: Total Unadjusted Error	$V_{REF}/2 = 2.500V$			$\pm 1 1/4$	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3		kΩ
Analog Input Voltage Range	(Note 2)	GND−0.05		$V^+ + 0.05$	V
DC Common-Mode Rejection	Over Analog Input Voltage Range		$\pm 1/8$	$\pm 1/4$	LSB
Power Supply Sensitivity	$V^+ = 5V \pm 10\%$ Over Allowed Input Voltage Range		$\pm 1/8$	$\pm 1/4$	LSB

4

NOTE: All typical values have been characterized but are not tested.

DC ELECTRICAL CHARACTERISTICS
Digital Levels and DC Specifications: $V^+ = 5V$ and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
CONTROL INPUTS (Note 6)						
V_{INH}	Logical "1" Input Voltage (Except Pin 4 CLK IN)	$V^+ = 5.25V$	2.0		V^+	V
V_{INL}	Logical "0" Input Voltage (Except Pin 4 CLK IN)	$V^+ = 4.75V$			0.8	V
V^+_{CLK}	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V
V^-_{CLK}	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V
V_H	CLK IN (Pin 4) Hysteresis $(V_{CLK}{}^+) - (V_{CLK}{}^-)$		0.6	1.3	2.0	V
I_{INHI}	Logical "1" Input Current (All Inputs)	$V_{IN} = 5V$		0.005	1	μA
I_{INLO}	Logical "0" Input Current (All Inputs)	$V_{IN} = 0V$	−1	−0.005		μA
I^+	Supply Current (Includes Ladder Current)	$f_{CLK} = 640kHz$, $T_A = +25°C$ and $\overline{CS} = HI$		1.3	2.5	mA

DC ELECTRICAL CHARACTERISTICS
Digital Levels and DC Specifications: $V^+ = 5V$ and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise noted. (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DATA OUTPUTS AND $\overline{INTR}$						
V_{OL}	Logical "0" Output Voltage	$I_O = 1.6mA$ $V^+ = 4.75V$			0.4	V
V_{OH}	Logical "1" Output Voltage	$I_O = -360\mu A$ $V^+ = 4.75V$	2.4			V
I_{LO}	3-State Disabled Output Leakage (All Data Buffers)	$V_{OUT} = 0V$ $V_{OUT} = 5V$	−3		3	μA μA
I_{SOURCE}	Output Short Circuit Current	V_{OUT} Short to Gnd $T_A = +25°C$	4.5	6		mA
I_{SINK}	Output Short Circuit Current	V_{OUT} Short to V^+ $T_A = +25°C$	9.0	16		mA

NOTES: 1. All voltages are measured with respect to GND, unless otherwise specified. The separate AGND point should always be wired to the DGND, being careful to avoid ground loops.

2. For $V_{IN(-)} \geq V_{IN(+)}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see **Block Diagram**) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V^+ supply. Be careful, during testing at low V^+ levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct-especially at elevated temperatures, and cause errors for analog inputs near full-scale. As long as the analog V_{IN} does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over temperature variations, initial tolerance and loading.

3. With $V^+ = 6V$, the digital logic interfaces are no longer TTL compatible.

4. With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process.

5. The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input so that timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see **Timing Diagrams**).

6. CLK IN (pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately.

7. None of these A/Ds requires a zero-adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.0V full-scale) the $V_{IN(-)}$ input can be adjusted to achieve this. See **Zero Error** on page 10 of this data sheet.

NOTE: All typical values have been characterized but are not tested.

AC ELECTRICAL CHARACTERISTICS

Timing Specifications: $V^+ = 5V$ and $T_A = +25°C$ unless otherwise stated.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
f_{CLK}	Clock Frequency	$V^+ = 6V$ (Note 3) $V^+ = 5V$	100 100	640 640	1280 800	kHz kHz
t_{conv}	Clock Periods per Conversion (Note 4)		62		73	
CR	Conversion Rate In Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS} = 0V$, $f_{CLK} = 640kHz$			8888	conv/s
$t_{W(\overline{WR})I}$	Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS} = 0V$ (Note 5)	100			ns
t_{acc}	Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	$C_L = 100pF$ (Use Bus Driver IC for Larger C_L)		135	200	ns
t_{1h}, t_{0h}	3-State Control (Delay from Rising Edge of $\overline{RD}$ to HI-Z State)	$C_L = 10pF$, $R_L = 10k$ (See **3-State Test Circuits**)		125	250	ns
t_{WI}, t_{RI}	Delay from Falling Edge of $\overline{WR}$ to Reset of $\overline{INTR}$			300	450	ns
C_{IN}	Input Capacitance of Logic Control Inputs			5		pF
C_{OUT}	3-State Output Capacitance (Data Buffers)			5		pF

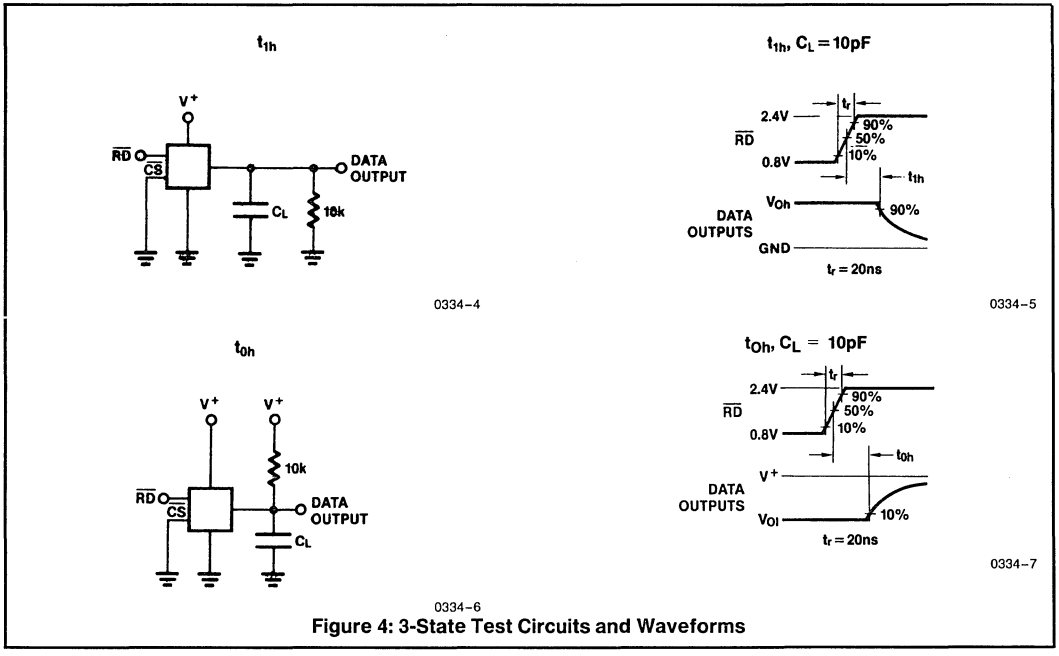
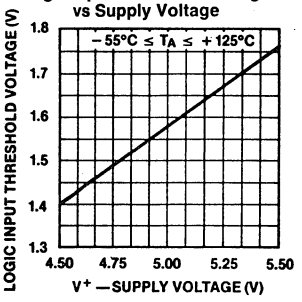


Figure 4: 3-State Test Circuits and Waveforms

NOTE: All typical values have been characterized but are not tested.

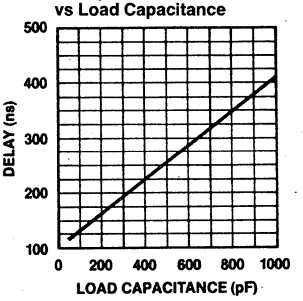
TYPICAL PERFORMANCE CHARACTERISTICS

Logic Input Threshold Voltage vs Supply Voltage



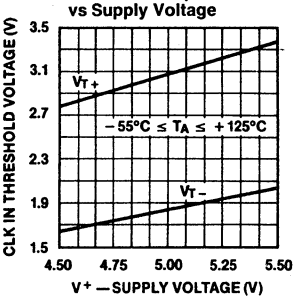
0334-8

Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs Load Capacitance



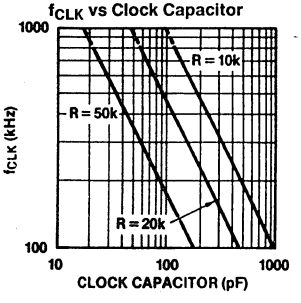
0334-9

CLK IN Schmitt Trip Levels vs Supply Voltage



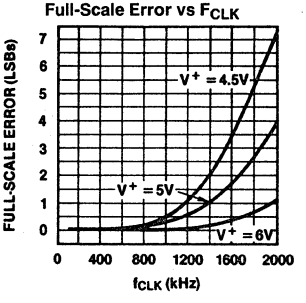
0334-10

f_{CLK} vs Clock Capacitor



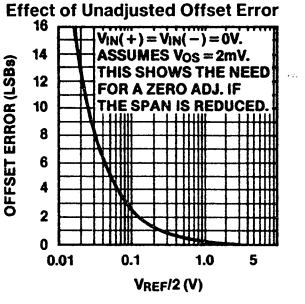
0334-11

Full-Scale Error vs F_{CLK}



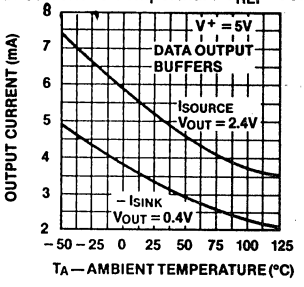
0334-12

Effect of Unadjusted Offset Error



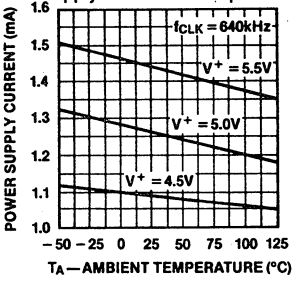
0334-13

Output Current vs Temperature $V_{REF}/2$ Voltage



0334-14

Power Supply Current vs Temperature

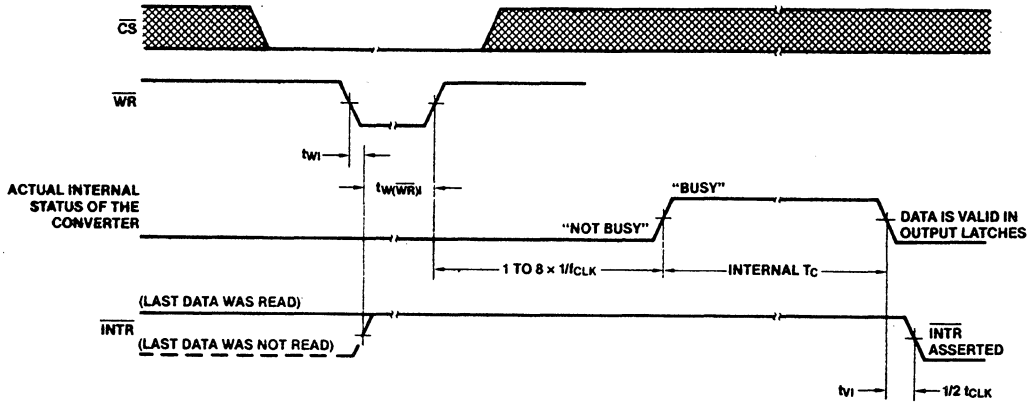


0334-15

NOTE: All typical values have been characterized but are not tested.

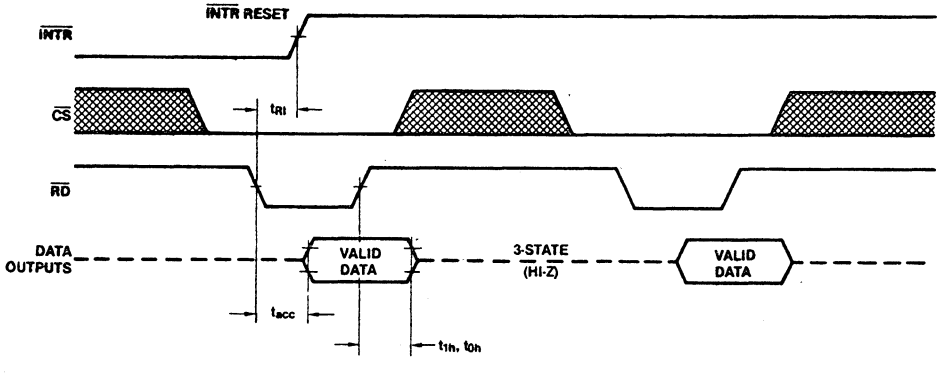
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Start Conversion



0334-16

Output Enable and Reset INTR



0334-17

Figure 5: Timing Diagrams

Note: All timing is measured from the 50% voltage points.

NOTE: All typical values have been characterized but are not tested.

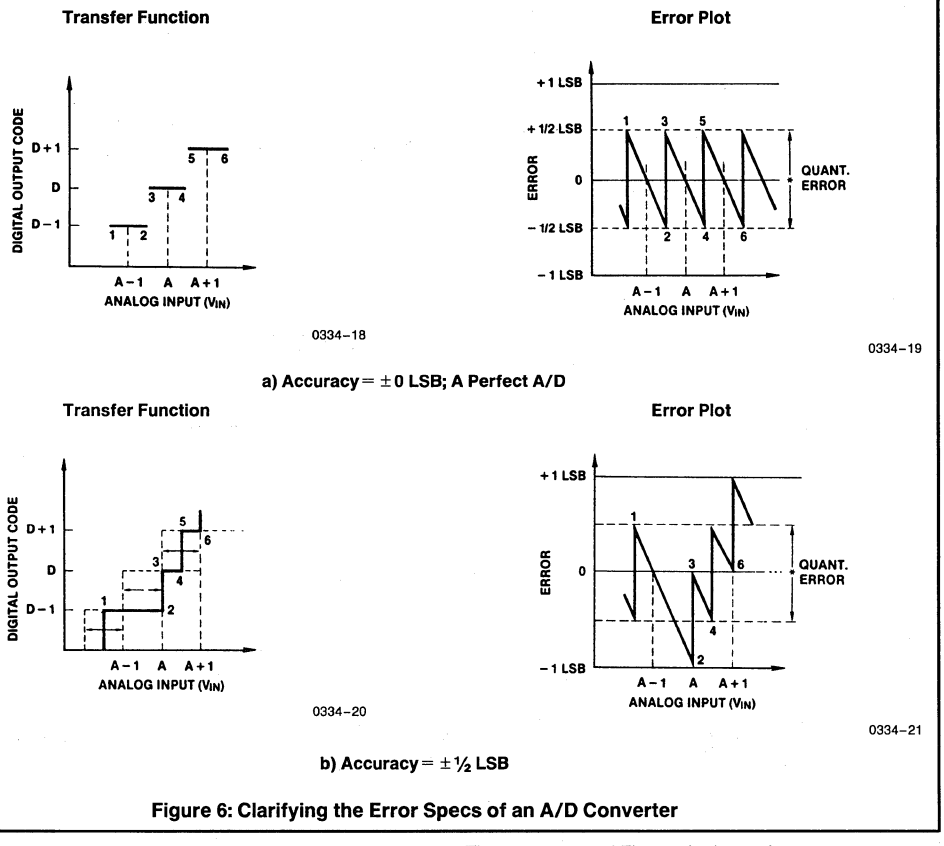


Figure 6: Clarifying the Error Specs of an A/D Converter

UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in Figure 6a. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1LSB (19.53mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes which correspond to these inputs are shown as D − 1, D, and D + 1. For the perfect A/D, not only will center-value (A − 1,A,A + 1, . . .) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ±½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages which extend ±½ LSB from the ideal center-values. Each tread (the range of analog input voltage which provides the same digital output code) is therefore 1LSB wide.

The error curve of Figure 6b shows the worst case transfer function for the ADC0802. Here the specification guarantees that if we apply an analog input equal to the LSB analog voltage center-value, the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Notice that the error includes the quantization uncertainty of the A/D. For example, the error at point 1 of Figure 6a is + ½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1LSB in magnitude, unless the device has missing codes.

NOTE: All typical values have been characterized but are not tested.

FUNCTIONAL DESCRIPTION

A functional diagram of the ADC0802 series of A/D converters is shown in Figure 3. All of the package pinouts are shown and the major logic control paths are drawn in heavier-weight lines. The device operates on the successive approximation principle (see APPLICATION NOTES A016 and A020 for a more detailed description of this principle). Analog switches are closed sequentially by successive-approximation logic until the analog differential input voltage $[V_{IN(+)} - V_{IN(-)}]$ matches a voltage derived from a tapped resistor string across the reference voltage. The most significant bit is tested first and after 8 comparisons (64 clock cycles), an 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch.

The normal operation proceeds as follows. On the high-to-low transition of the $\overline{WR}$ input, the internal SAR latches and the shift-register stages are reset, and the $\overline{INTR}$ output will be set high. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. **Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.** After the requisite number of clock pulses to complete the conversion, the $\overline{INTR}$ pin will make a high-to-low transition. This can be used to interrupt a processor, or otherwise signal the availability of a new conversion. A $\overline{RD}$ operation (with $\overline{CS}$ low) will clear the $\overline{INTR}$ line high again. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS} = 0$. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle. A conversion-in-process can be interrupted by issuing a second start command.

Digital Details

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flip-flop, DFF1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of DFF1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1"), the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This allows for asynchronous or wide $\overline{CS}$ and $\overline{WR}$ signals.

After the "1" is clocked through the 8-bit shift register (which completes the SAR operation) it appears as the input to DFF2. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the 3-state output latches. When DFF2 is subsequently clocked, the $\overline{Q}$ output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ output signal.

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the 3-state output latches will be enabled to provide the 8-bit digital outputs.

Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard TTL logic voltage levels. These signals are essentially equivalent to the standard A/D Start and Output Enable control signals, and are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function obtained by an active low pulse at the $\overline{WR}$ input (pin 3). The Output Enable function is achieved by an active low pulse at the $\overline{RD}$ input (pin 2).

Analog Operation

The analog comparisons are performed by a capacitive charge summing circuit. Three capacitors (with precise ratioed values) share a common node with the input to an auto-zeroed comparator. The input capacitor is switched between $V_{IN(+)}$ and $V_{IN(-)}$, while two ratioed reference capacitors are switched between taps on the reference voltage divider string. The net charge corresponds to the weighted difference between the input and the current total value set by the successive approximation register. A correction is made to offset the comparison by ½ LSB (see Figure 6a).

Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D gains considerable applications flexibility from the analog differential voltage input. The $V_{IN(-)}$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4mA – 20mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN(+)}$ and $V_{IN(-)}$ is 4½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_p)(2\pi f_{cm}) \left[\frac{4.5}{f_{CLK}} \right]$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

For example, with a 60Hz common-mode frequency, f_{cm}, and a 640kHz A/D clock, f_{CLK}, keeping this error to ¼ LSB (~5mV) would allow a common-mode voltage, V_P, given by:

$$V_p = \frac{[\Delta V_e(MAX)(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_p = \frac{(5 \times 10^{-3})\ (640 \times 10^3)}{(6.28)\ (60)\ (4.5)} \cong 1.9V$$

The allowed range of analog input voltage usually places more severe restrictions on input common-mode voltage levels than this.

An analog input voltage with a reduced span and a relatively large zero offset can be easily handled by making use of the differential input (see **Reference Voltage Span Adjust).**

NOTE: All typical values have been characterized but are not tested.

Analog Input Current

The internal switching action causes displacement currents to flow at the analog inputs. The voltage on the on-chip capacitance to ground is switched through the analog differential input voltage, resulting in proportional currents entering the $V_{IN(+)}$ input and leaving the $V_{IN(-)}$ input. These current transients occur at the leading edge of the internal clocks. They rapidly decay and **do not inherently cause errors** as the on-chip comparator is strobed at the end of the clock period.

Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN(+)}$ input voltage at full-scale. For a 640kHz clock frequency with the $V_{IN(+)}$ input at 5V, this DC current is at a maximum of approximately 5μA. Therefore, **bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin** for high resistance sources (>1kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the effects of the voltage drop across this input resistance, due to the average value of the input current, can be compensated by a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage at a constant conversion rate.

Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, **will not cause errors** since the input currents settle out prior to the comparison time. If a low-pass filter is required in the system, use a low-value series resistor (≤1kΩ) for a passive RC section or add an op amp RC active low-pass filter. For low-source-resistance applications, (≤1kΩ), a 0.1μF bypass capacitor at the inputs will minimize EMI due to the series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor (both the R and C are placed outside the feedback loop) from the output of an op amp, if used.

Stray Pickup

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize stray signal pickup (EMI). Both EMI and undesired digital-clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5kΩ. Larger values of source resistance can cause undesired signal pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate this pickup but can create analog scale errors as these capcitors will average the transient input switching currents of the A/D (see **Analog Input Current).** This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be compensated by a full-scale adjustment of the A/D (see **Full-Scale Adjustment)** with the source resistance and input bypass capacitor in place, and the desired conversion rate.

Reference Voltage Span Adjust

For maximum application flexibility, these A/Ds have been designed to accommodate a 5V, 2.5V or an adjusted voltage reference. This has been achieved in the design of the IC as shown in Figure 7.

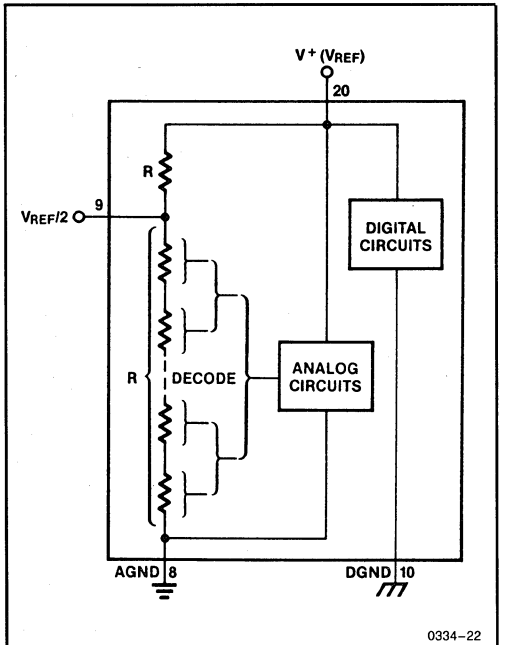
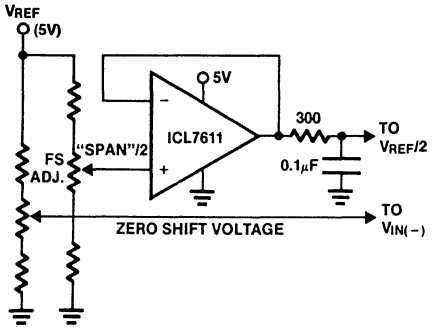


Figure 7: The $V_{REFERENCE}$ Design on the IC

Notice that the reference voltage for the IC is either ½ of the voltage which is applied to the V^+ supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. This allows for a pseudo-ratiometric voltage reference using, for the V^+ supply, a 5V reference voltage. Alternatively, a voltage less than 2.5V can be applied to the $V_{REF}/2$ input. The internal gain to the $V_{REF}/2$ input is 2 to allow this factor of 2 reduction in the reference voltage.

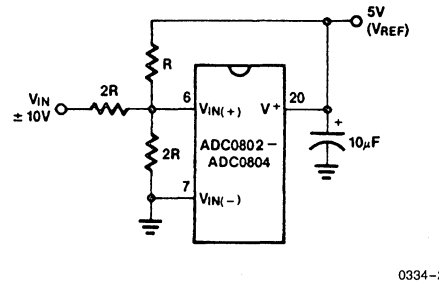
Such an adjusted reference voltage can accommodate a reduced span or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5V to 3.5V, instead of 0V to 5V, the span would be 3V. With 0.5V applied to the $V_{IN(-)}$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5V. The A/D now will encode the $V_{IN(+)}$ signal from 0.5V to 3.5V with the 0.5V input corresponding to zero and the 3.5V input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range. The requisite connections are shown in Figure 8. For expanded scale inputs, the circuits of Figures 9 and 10 can be used.

NOTE: All typical values have been characterized but are not tested.



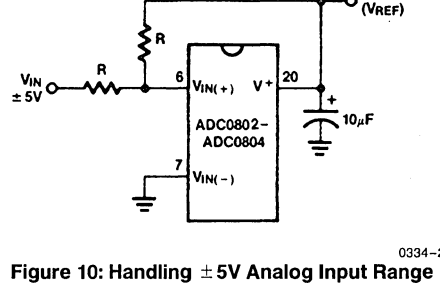
0334-23

Figure 8: Offsetting the Zero of the ADC0802 and Performing an Input Range (Span) Adjustment



0334-24

Figure 9: Handling ± 10V Analog Input Range



0334-25

Figure 10: Handling ± 5V Analog Input Range

Reference Accuracy Requirements

The converter can be operated in a pseudo-ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important accuracy factors in the operation of the A/D converter. For $V_{REF}/2$ voltages of 2.5V nominal value, initial errors of ± 10mV will cause conversion errors of ± 1LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20mV (5V span) to 10mV and 1LSB at the $V_{REF}/2$ input becomes 5mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive.

Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN(-)}$ input at this $V_{IN(MIN)}$ value (see **Applications** section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN(-)}$ input and applying a small magnitude positive voltage to the $V_{IN(+)}$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8mV for $V_{REF}/2 = 2.500V$).

Full-Scale Adjust

The full-scale adjustment can be made by applying a differential input voltage which is 1½ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9) for a digital output code which is just changing from 1111 1110 to 1111 1111. When offsetting the zero and using a span-adjusted $V_{REF}/2$ voltage, the full-scale adjustment is made by inputting V_{MIN} to the $V_{IN(-)}$ input of the A/D and applying a voltage to the $V_{IN(+)}$ input which is given by:

$$V_{IN(+)}\text{fsadj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

where:

V_{MAX} = the high end of the analog input range

and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

NOTE: All typical values have been characterized but are not tested.

Clocking Option

The clock for the A/D can be derived from an external source such as the CPU clock or an external RC network can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in Figure 11.

Heavy capacitive or DC loading of the CLocK R pin should be avoided as this will disturb normal converter operation. Loads less than 50pF, such as driving up to 7 A/D converter clock inputs from a single CLK R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the CLK R pin (do not use a standard TTL buffer).

Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in progress is not completed. The data from the previous conversion remain in this latch.

Continuous Conversions

In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to insure circuit operation. See Figure 12 for details.

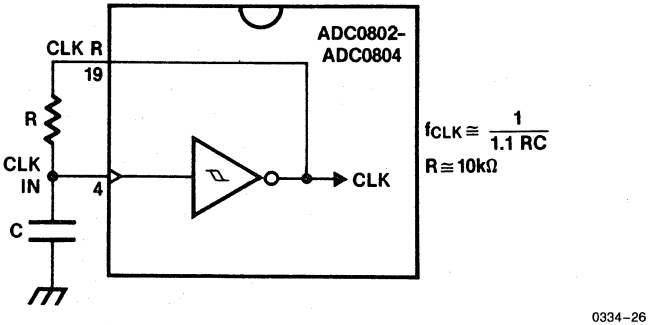


Figure 11: Self-Clocking the A/D

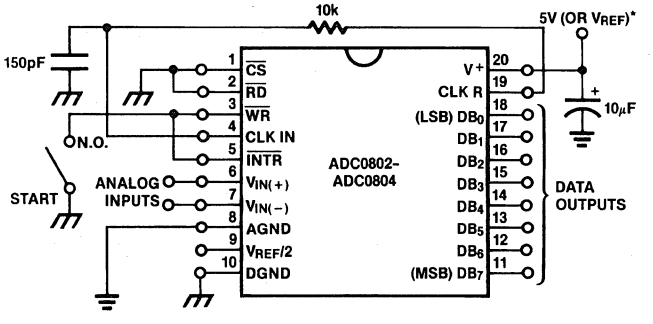


Figure 12: Free-Running Connection

NOTE: All typical values have been characterized but are not tested.

Driving the Data Bus

This CMOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in 3-state (high-impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see **Typical Performance Characteristics).**

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock-extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be 3-state buffers (low power Schottky is recommended, such as the 74LS240 series) or special higher-drive-current products which are designed as bus drivers. High-current bipolar bus drivers with PNP inputs are recommended.

Power Supplies

Noise spikes on the V^+ supply line can cause conversion errors as the comparator will respond to this noise. A low-inductance tantalum filter capacitor should be used close to the converter V^+ pin, and values of 1μF or greater are recommended. If an unregulated voltage is available in the system, a separate 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V^+ supply. An ICL7663 can be used to regulate such a supply from an input as low as 5.2V.

Wiring and Hook-Up Precautions

Standard digital wire-wrap sockets are not satisfactory for breadboarding with this A/D converter. Sockets on PC boards can be used. All logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup; therefore, shielded leads may be necessary in many applications.

A single-point analog ground should be used which is separate from the logic ground points. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ¼ LSB can usually be traced to improper board layout and wiring (see **Zero Error** for measurement). Further information can be found in A018.

TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in Figure 13.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560V and a V^+ supply voltage of 5.12V should be used. This provides an LSB value of 20mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090V (5.120 – 1½ LSB) should be applied to the $V_{IN(+)}$ pin with the $V_{IN(-)}$ pin grounded. The value of the $V_{REF}/2$ input voltage should be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

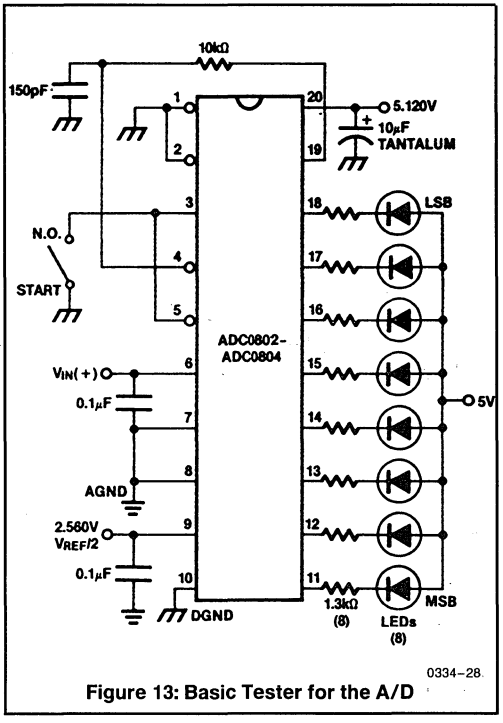


Figure 13: Basic Tester for the A/D

The digital-output LED display can be decoded by dividing the 8 bits into 2 hex characters, one with the 4 most-significant bits (MS) and one with the 4 least-significant bits (LS). The output is then interpreted as a sum of fractions times the full-scale voltage:

$$V_{OUT} = \left(\frac{MS}{16} + \frac{LS}{256}\right)(5.12)V.$$

NOTE: All typical values have been characterized but are not tested.

For example, for an output LED display of 1011 0110, the MS character is hex B (decimal 11) and the LS character is hex (and decimal) 6, so

$$V_{OUT} = \left(\frac{11}{16} + \frac{6}{256}\right)(5.12) = 3.64V.$$

Figures 14 and 15 show more sophisticated test circuits.

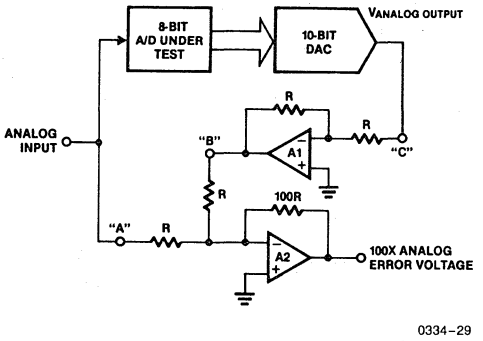


Figure 14: A/D Tester with Analog Error Output. This circuit can be used to generate "error plots" of Figure 6.

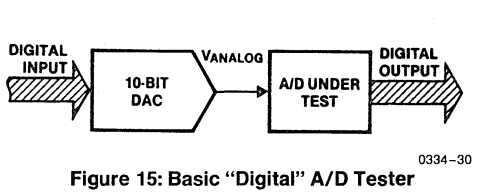


Figure 15: Basic "Digital" A/D Tester

APPLICATIONS

Interfacing 8080/85 or Z-80 Microprocessors

This converter has been designed to directly interface with 8080/85 or Z-80 Microprocessors. The 3-state output capability of the A/D eliminates the need for a peripheral interface device, although address decoding is still required to generate the appropriate $\overline{CS}$ for the converter. The A/D can be mapped into memory space (using standard memory-address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15, since they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder, but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. See A020 for more discussion of memory-mapped vs I/O-mapped interfaces. An example of an A/D in I/O space is shown in Figure 16.

The standard control-bus signals of the 8080 ($\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D, since the bus timing requirements, to allow both starting the converter, and outputting the data onto the data bus, are met. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100pF.

It is useful to note that in systems where the A/D converter is 1 of 8 or fewer I/O-mapped devices, no address-decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs, one for each I/O device.

Interfacing the Z-80 and 8085

The Z-80 and 8085 control buses are slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals have to be combined with the generalized strobes to provide the appropriate signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in Figure 17. By using $\overline{MREQ}$ in place of $\overline{IORQ}$, a memory-mapped configuration results.

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

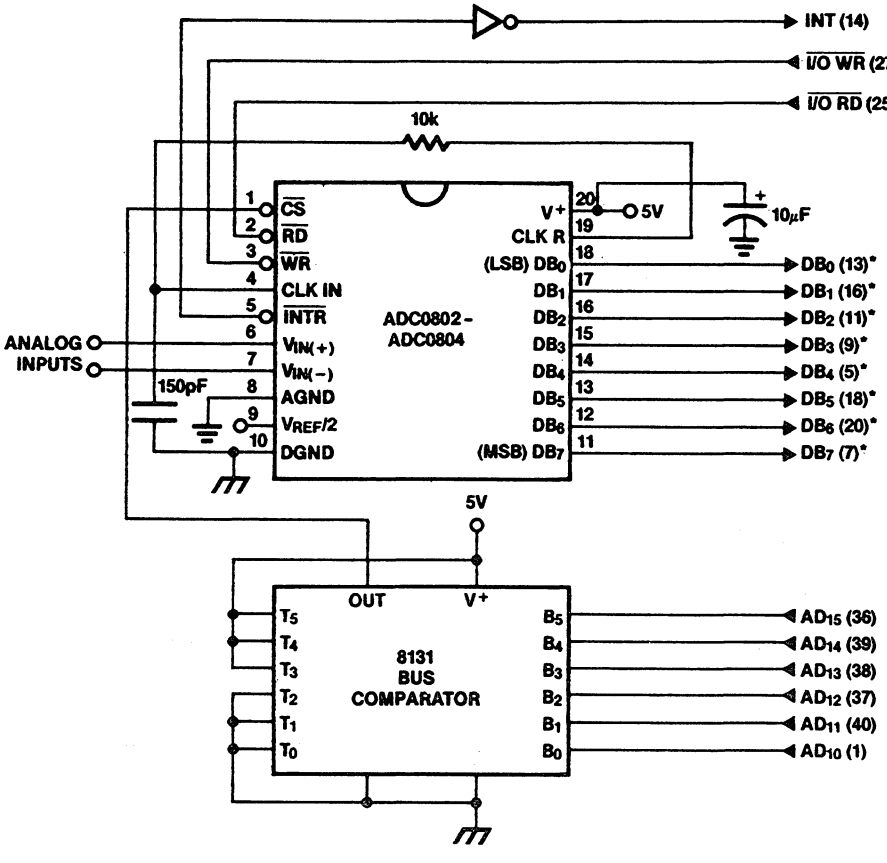
The 8085 also provides a generalized $\overline{RD}$ and $\overline{WR}$ strobe, with an IO/$\overline{M}$ line to distinguish I/O and memory requests. The circuit of Figure 17 can again be used, with IO/$\overline{M}$ in place of $\overline{IORQ}$ for a memory-mapped interface, and an extra inverter (or the logic equivalent) to provide $\overline{IO}$/M for an I/O-mapped connection.

Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived from the $\phi 2$ clock. All I/O devices are memory-mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. Figure 16 shows an interface schematic where the A/D is memory-mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using ½ DM8092. Note that in many 6800 systems, an already decoded $\frac{4}{5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HEX ADDR: 4XXX or 5XXX.

In Figure 19 the ADC0802 series is interfaced to the MC6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory-mapped in the MC6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

NOTE: All typical values have been characterized but are not tested.



0334-31

Note: Pin numbers for 8228 system controller: others are 8080A

Figure 16: ADC0802 to 8080A CPU Interface

NOTE: All typical values have been characterized but are not tested.

APPLICATION NOTES

Some applications bulletins that may be found useful are listed here:

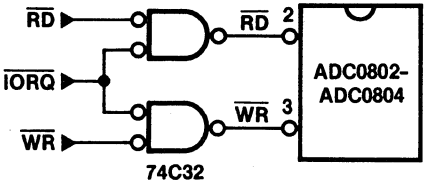
A016 "Selecting A/D Converters," by Dave Fullagar.

A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Sliger.

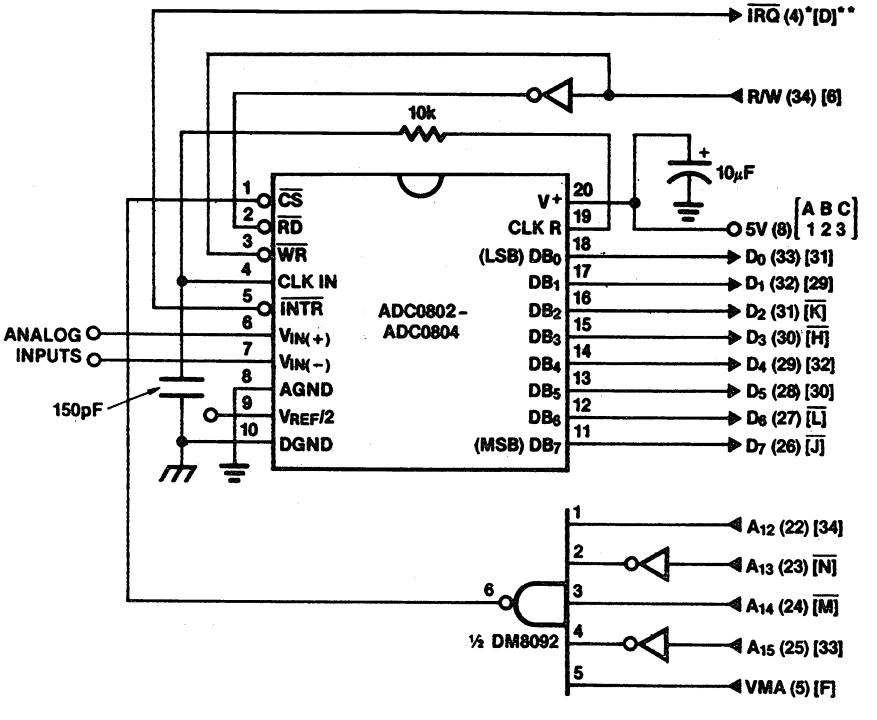
A030 "The ICL7104 — A Binary Output A/D Converter for Microprocessors," by Peter Bradshaw.

R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.



0334-32

Figure 17: Mapping the A/D as an I/O device for use with the Z-80 CPU



0334-33

***Note 1:** Numbers in parentheses refer to MC6800 CPU pinout.

****Note 2:** Numbers or letters in brackets refer to standard MC6800 system common bus code.

Figure 18: ADC0802 to MC6800 CPU Interface

NOTE: All typical values have been characterized but are not tested.

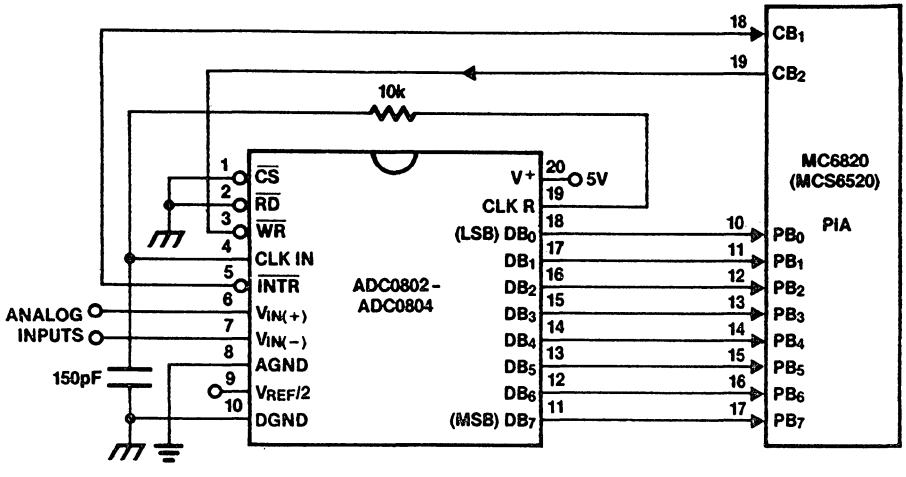


Figure 19: ADC0802 to MC6820 PIA Interface

4

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

CA3310, CA3310A

CMOS 10-Bit Analog-to-Digital Converter with Internal Track and Hold

GENERAL DESCRIPTION

The Harris CA3310 is a fast, low power, 10-bit successive approximation analog-to-digital converter, with microprocessor-compatible outputs. It uses only a single 3V to 6V supply and typically draws just 3 mA when operating at 5V. It can accept full rail-to-rail input signals, and features a built-in track and hold. The track and hold will follow high bandwidth input signals, as it has only a 100 ns (typical) input time constant.

The ten data outputs feature full high-speed CMOS three-state bus driver capability, and are latched and held through a full conversion cycle. Separate 8 MSB and 2 LSB enables, a data ready flag, and conversion start and ready reset inputs complete the microprocessor interface.

An internal, adjustable clock is provided and is available as an output. The clock may also be driven from an external source.

FEATURES

- **CMOS Low Power (15 mW Typ.)**
- **Single Supply Voltage (3V to 6V)**
- **13 μs Conversion Time**
- **Built-In Track and Hold**
- **Rail-to-Rail Input Range**
- **Latched 3-State Output Drivers**
- **Microprocessor-Compatible Control Lines**
- **Internal or External Clock**

APPLICATIONS

- **Fast, No-Droop, Sample and Hold**
- **Voice Grade Digital Audio**
- **DSP Modems**
- **Remote Low Power Data Acquisition Systems**
- **μP Controlled Systems**

ORDERING INFORMATION

Part Number	Linearity (INL, DNL)	Temperature Range	Package
CA3310E	±0.75 LSB	−40°C to +85°C	24-Pin Plastic DIP
CA3310AE	±0.5 LSB	−40°C to +85°C	24-Pin Plastic DIP
CA3310D	±0.75 LSB	−55°C to +125°C	24-Pin Ceramic DIP
CA3310AD	±0.5 LSB	−55°C to +125°C	24-Pin Ceramic DIP

NOTE: Consult sales office for availability of SOIC packages.

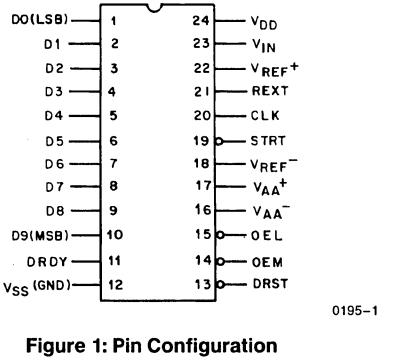


Figure 1: Pin Configuration

1851-002

NOTE: All typical values have been characterized but are not tested.

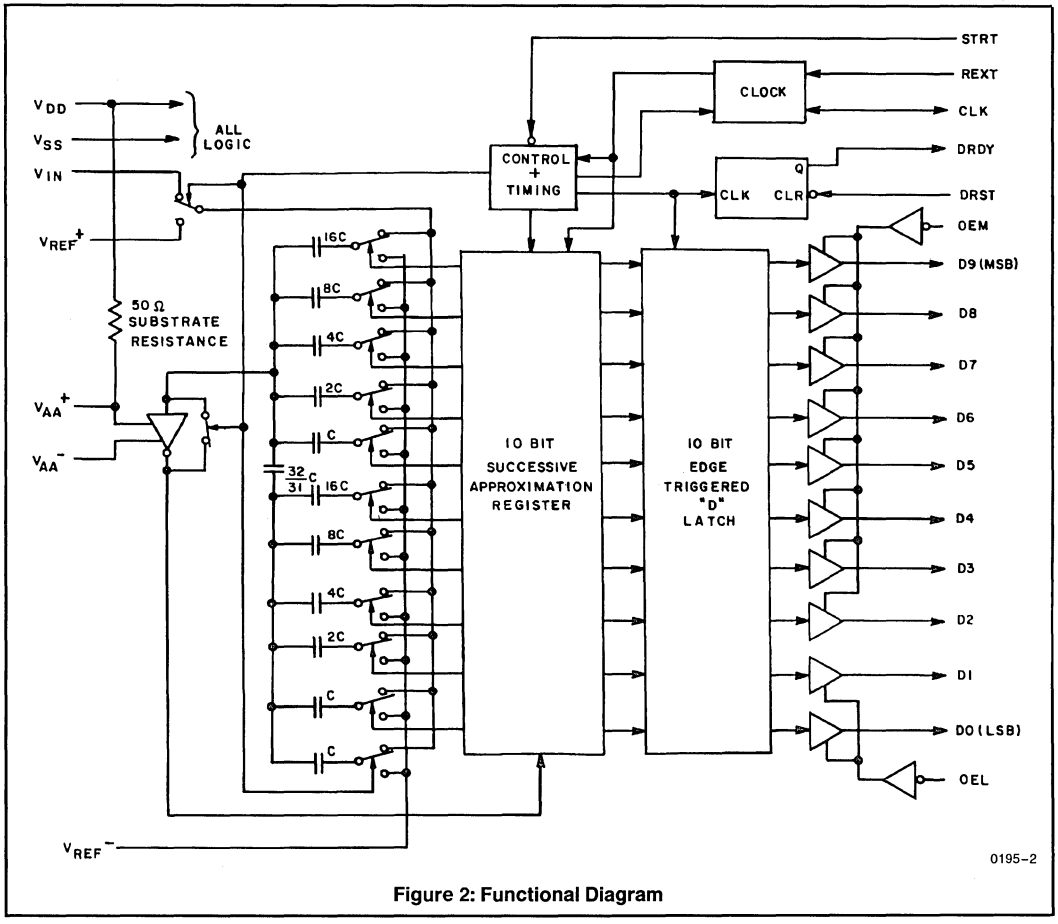


Figure 2: Functional Diagram

ABSOLUTE MAXIMUM RATINGS

Digital Supply Voltage (V_{DD})
..... V_{SS} − 0.5V to V_{SS} + 7V

Analog Supply Voltage (V_{AA}+) ..... V_{DD} ±0.5V

Any Other Terminal ..... V_{SS} − 0.5V to V_{DD} + 0.5V

DC Input or Output (Protection Diode) Current ..... ±20 mA

DC Output Drain Current, per Output ..... ±35 mA

Total DC Supply or Ground Current ..... ±70 mA

Power Dissipation per Package (P_D):
For T_A = −40°C to +85°C
(Package Type E) ..... 300 mW
For T_A = −55°C to +100°C
(Package Type D) ..... 300 mW
For T_A = +100°C to +125°C
(Package Type D) ..... Derate Linearly at 8 mW/°C

Operating-Temperature Range (T_A):
Package Type D ..... −55°C to +125°C
Package Type E ..... −40°C to +85°C

Storage Temperature (T_{STG}) ..... −65°C to +150°C

Lead Temperature (During Soldering):
At distance 1/16 in. ±1/32 in. (1.59mm ±0.79mm) from case for 10s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59mm) with solder contacting lead tips only ..... +300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_{DD} = V_{AA}^+ = 5V$, $V_{REF}^+ = 4.608V$, $V_{SS} = V_{AA}^- = V_{REF}^- = GND$, Clock = External 1 MHz (Unless Noted)

Parameter		Test Conditions	Limits			Units
			Min	Typ	Max	
ACCURACY: SEE TEXT FOR DEFINITIONS						
Resolution			10			Bits
Differential Linearity Error	CA3310			±0.5	±0.75	LSB
	CA3310A			±0.25	±0.5	LSB
Integral Linearity Error	CA3310			±0.5	±0.75	LSB
	CA3310A			±0.25	±0.5	LSB
Gain Error	CA3310			±0.25	±0.5	LSB
	CA3310A				±0.25	LSB
Offset Error	CA3310			±0.25	±0.5	LSB
	CA3310A				±0.25	LSB
ANALOG INPUT						
Input Resistance		In Series with Input Sample Capacitors		330		Ω
Input Capacitance		During Sample State		300		pF
Input Capacitance		During Hold State		20		pF
Input Current		At $V_{IN} = V_{REF}^+ = 5V$			+300	μA
		At $V_{IN} = V_{REF}^- = 0V$			−100	μA
Static Input Current		STRT = V+, CLK = V+				
		At = $V_{IN} = V_{REF}+ = 5V$			1	μA
		At = $V_{IN} = V_{REF}- = 0V$			−1	μA
Input + Full-Scale Range		(Note 2)	$V_{REF}^- + 1$		$V_{DD} + 0.3$	V
Input − Full-Scale Range		(Note 2)	$V_{SS} - 0.3$		$V_{REF}^+ - 1$	V
Input Bandwidth		From Input RC Time Constant		1.5		MHz
DIGITAL INPUTS: DRST, OEL, OEM, STRT, CLK						
High-Level Input Voltage		Over V_{DD} = 3V to 6V (Note 2)	70			% of V_{DD}
Low-Level Input Voltage		Over V_{DD} = 3V to 6V (Note 2)			30	% of V_{DD}
Input Leakage Current		Except CLK			±1	μA
Input Capacitance		(Note 2)			10	pF
Input Current		CLK Only (Note 2)			±400	μA
DIGITAL OUTPUTS: D0–D9, DRDY						
High-Level Output Voltage		$I_{SOURCE} = -4$ mA	4.6			V
Low-Level Output Voltage		$I_{SINK} = 6$ mA			0.4	V
Three-State Leakage		Except DRDY			±1	μA
Output Capacitance		Except DRDY (Note 2)			20	pF
CLK OUTPUT						
High-Level Output Voltage		$I_{SOURCE} = 100$ μA (Note 2)	4			V
Low-Level Output Voltage		$I_{SINK} = 100$ μA (Note 2)			1	V

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{DD} = V_{AA}^+ = 5V$, $V_{REF}^+ = 4.608V$, $V_{SS} = V_{AA}^- = V_{REF}^- = GND$, Clock = External 1 MHz (Unless Noted) (Continued)

Parameter	Test Conditions	Limits			Units
		Min	Typ	Max	
TIMING					
Clock Frequency	Internal, CLK and R_{EXT} Open	200	300	400	kHz
	Internal, CLK Shorted to R_{EXT}	600	800	1000	kHz
	External, Applied to CLK: Max. (Note 2) Min.	 100	4 10	2	MHz kHz
Clock Pulse Width, T_{LOW}, T_{HIGH}	External, Applied to CLK: See Figure 6 (Note 2)	100			ns
Conversion Time		13			μs
Aperture Delay, T_D APR	See Figure 6		100		ns
Clock to Data Ready Delay, T_{D1} DRDY	See Figure 6		150		ns
Clock to Data Ready Delay, T_{D2} DRDY	See Figure 6		250		ns
Clock to Data Delay, T_D Data	See Figure 6		200		ns
Start Removal Time, T_R STRT	See Figures 8 & 9 (Note 1)		−120		ns
Start Setup Time, T_{SU} STRT	See Figure 9		160		ns
Start Pulse Width, T_W STRT	See Figures 8 & 9		10		ns
Start to Data Ready Delay, T_{D3} DRDY	See Figures 8 & 9		170		ns
Clock Delay from Start, T_D CLK	See Figure 8		200		ns
Ready Reset Removal Time, T_R DRST	See Figure 10 (Note 1)		−80		ns
Ready Reset Pulse Width, T_W DRST	See Figure 10		10		ns
Ready Reset to Data Ready Delay, T_{D4} DRDY	See Figure 10		35		ns
Output Enable Delay, T_{EN}	See Figure 7		40		ns
Output Disable Delay, T_{DIS}	See Figure 7		50		ns
SUPPLIES					
Supply Operating Range, V_{DD} or V_{AA}	(Note 2)	3		6	V
Supply Current, $I_{DD} + I_{AA}$	See Figures 20 & 21		3	8	mA
Supply Standby Current	Clock Stopped During Cycle 1		3.5		mA
Analog Supply Rejection	@120 Hz, See Figure 19		25		mV/V
Reference Input Current	See Figure 16		160		μA
TEMPERATURE DEPENDENCY					
Offset Drift	@ 0 to 1 Code Transition		−4		μV/°C
Gain Drift	@ 1022 to 1023 Code Transition		−6		μV/°C
Internal Clock Speed	See Figure 5		−0.5		%/°C

NOTE 1: A (−) removal time means the signal can be removed after the reference signal.
2: Parameter not tested, but guaranteed by design or characterization.

NOTE: All typical values have been characterized but are not tested.

Table 1: Pin Description

Pin Number	Name	Function
1–10	D0–D9	Three-state outputs for data bits representing 2^0 (LSB) through 2^9 (MSB).
11	DRDY	Output flag signifying new data is available. Goes high at end of clock period 13, goes low when new conversion started. Also reset asynchronously by DRST.
12	V_{SS}	Digital ground.
13	DRST	Active low input, resets DRDY.
14	OEM	Active low input, three-state enable of D2–D9.
15	OEL	Active low input, three-state enable of D0, D1.
16	V_{AA}^-	Analog ground.
17	V_{AA}^+	Analog + supply.
18	V_{REF}^-	Reference input voltage, sets 0 code (−) end of input range.
19	STRT	Active low start conversion input. Recognized after end of clock period 13.
20	CLK	Clock input or output. Conversion functions are synchronous to high-going edge.
21	R_{EXT}	Clock adjust input when using internal clock.
22	V_{REF}^+	Reference input voltage, set 1023 code (+) end of input range.
23	V_{IN}	Analog input.
24	V_{DD}	Digital + supply.

DEVICE OPERATION

The CA3310 is a CMOS 10-bit analog-to-digital converter that uses capacitor-charge balancing to successively approximate the analog input. A binarily weighted capacitor network forms the D-to-A "Heart" of the device. Figure 2 shows a functional diagram of the CA3310.

The capacitor network has a common node which is connected to a comparator. The second terminal of each capacitor is individually switchable to the input, V_{REF}^+ or V_{REF}^-.

During the first three clock periods of a conversion cycle, the switchable end of every capacitor is connected to the input. The comparator is being auto-balanced at its trip point, thus setting the voltage at the capacitor common node.

During the fourth period, all capacitors are disconnected from the input, the one representing the MSB (D9) is connected to the V_{REF}^+ terminal, and the remaining capacitors to V_{REF}^-. The capacitor-common node, after the charges balance out, will represent whether the input was above or below ½ of ($V_{REF}^+ - V_{REF}^-$).

At the end of the fourth period, the comparator output is stored and the MSB capacitor is either left connected to V_{REF}^+ (if the comparator was high) or returned to V_{REF}^-. This allows the next comparison to be at either ¾ or ¼ of ($V_{REF}^+ - V_{REF}^-$).

At the end of periods 5 through 12, capacitors representing the next to MSB (D8) through the next to LSB (D1) are tested, the result stored, and each capacitor either left at V_{REF}^+ or at V_{REF}^-.

At the end of the 13th period, when the LSB (D0) capacitor is tested, D0 and all the previous results are shifted to the output registers and drivers. The capacitors are re-connected to the input, the comparator returns to the balance state, and the data-ready output goes active. The conversion cycle is now complete.

NOTE: All typical values have been characterized but are not tested.

DEVICE OPERATION (Continued)

Clock

The CA3310 can operate either from its internal clock or from one externally supplied. The CLK pin functions either as the clock output or input. All converter functions are synchronous with the rising edge of the clock signal.

Figure 3 shows the configuration of the internal clock. The clock output drive is low power: if used as an output, it should not have more than 1 CMOS gate load applied, and wiring capacitance should be kept to a minimum.

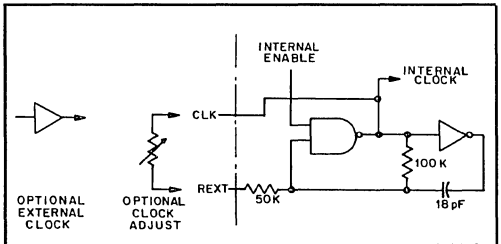


Figure 3: CA3310 Clock Circuitry

The R_{EXT} pin allows adjusting of the internal clock frequency by connecting a resistor between R_{EXT} and CLK. Figure 4 shows the typical relationship between the resistor and clock speed, while Figure 4 shows clock speed versus temperature and supply voltage.

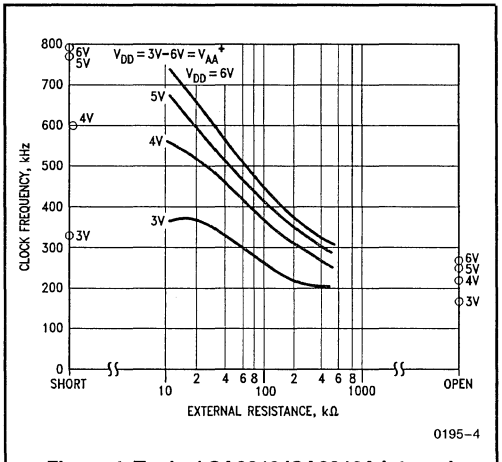


Figure 4: Typical CA3310/CA3310A internal clock frequency vs. external resistance

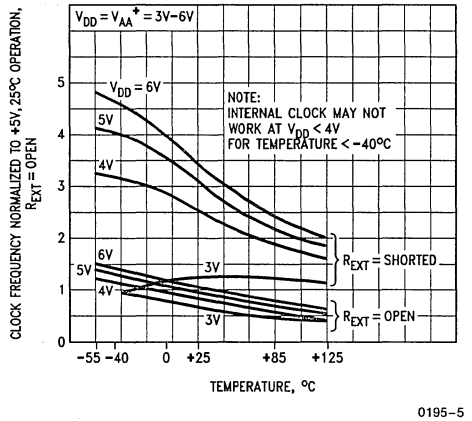


Figure 5: Typical CA3310/CA3310A internal clock frequency vs. temperature and supply voltage

The internal clock will shut down if the A/D is not restarted after a conversion. This is described under Control Timing. The clock could also be shut down with an open collector driver applied to the CLK pin. This should only be done during the sample portion (the first three periods) of a conversion cycle, and might be useful for using the device as a digital sample and hold: this is described further under Applications.

If an external clock is supplied to the CLK pin, it must have sufficient drive to overcome the internal clock source. The external clock can be shut off, but again only during the sample portion of a conversion cycle. At other times, it must be above the minimum frequency shown in the specifications.

If the internal or external clock was shut off during the conversion time (clock cycles 4 through 13) of the A/D, the output might be invalid due to balancing capacitor droop.

An external clock must also meet the minimum T_{LOW} and T_{HIGH} times shown in the specifications. A violation may cause an internal miscount and invalidate the results.

Control Signals

The CA3310 may be synchronized from an external source by using the STRT (Start Conversion) input to initiate conversions, or if STRT is tied low, may be allowed to free-run. In the free-running mode, illustrated in Figure 6, each conversion takes 13 clock periods.

NOTE: All typical values have been characterized but are not tested.

DEVICE OPERATION (Continued)

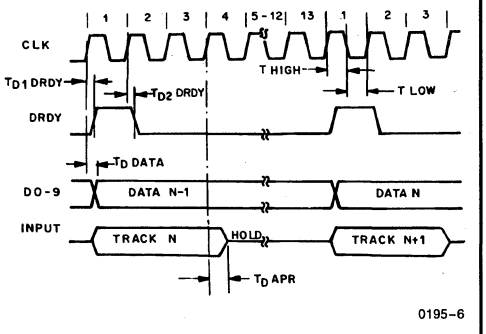


Figure 6. CA3310 Timing Diagram, Free Running, STRT Tied Low, DRST Tied High

The input is tracked from clock period 1 through period 3, then disconnected as the successive approximation takes place. After the start of the next period 1 (specified by T_D data), the output is updated.

The DRDY (Data Ready) status output goes high (specified by T_{D1} DRDY) after the start of clock period 1, and returns low (specified by T_{D2} DRDY) after the start of clock period 2. DRDY may also be asynchronously reset by a low on DRST (to be discussed later).

If the output data is to be latched externally by the DRDY signal, the trailing edge of DRDY should be used: there is no guaranteed set-up time to the leading edge.

The 10 output data bits are available in parallel on three-state bus driver outputs. When low, the OEM input enables the most significant byte (D2 through D9) while the OEL input enables the two least significant bits (D0, D1). T_{EN} and T_{DIS} specify the output enable and disable times, respectively. See Figure 7.

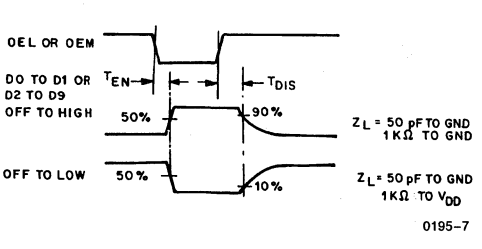


Figure 7: CA3310 Output Enable/Disable Timing Diagram

When the STRT input is used to initiate conversions, operation is slightly different depending on whether an internal or external clock is used.

Figure 8 illustrates operation with an internal clock. If the STRT signal is removed (at least T_R STRT) before clock period 1, and is not re-applied during that period, the clock will shut off after entering period 2. The input will continue to track and the DRDY output will remain high during this time.

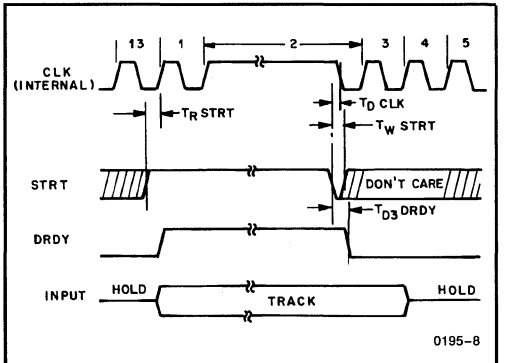


Figure 8: CA3310 Timing Diagram, STRT Pulsed Low, DRST Tied High, Internal Clock

A low signal applied to STRT (at least T_W STRT wide) can now initiate a new conversion. The STRT signal (after a delay of T_{D3} DRDY) will cause the DRDY flag to drop, and (after a delay of T_D Clk) cause the clock to restart.

Depending on how long the clock was shut off, the low portion of clock period 2 may be longer than during the remaining cycles.

The input will continue to track until the end of period 3, the same as when free-running.

Figure 9 illustrates the same operation as above, but with an external clock. If STRT is removed (at least T_R STRT) before clock period 1, and not re-applied during that period, the clock will continue to cycle in period 2. A low signal applied to STRT will drop the DRDY flag as before, and with the first positive-going clock edge that meets the T_{SU} STRT set-up time, the converter will continue with clock period 3.

The DRDY flag output, as described previously, goes active at the start of period 1, and drops at the start of period 2 or upon a new STRT command, whichever is later. It may also be controlled with the DRST (Data Ready Reset) input. Figure 10 depicts this operation.

NOTE: All typical values have been characterized but are not tested.

DEVICE OPERATION (Continued)

DRST must be removed (at least T_R DRST) before the start of period 1 to allow DRDY to go high. A low level on DRST (at least T_W DRST wide) will (after a delay of T_{D4} DRDY) drop DRDY.

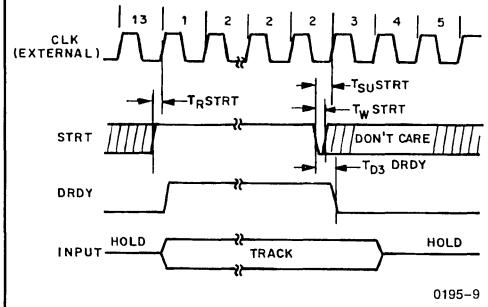


Figure 9: CA3310 Timing Diagram, STRT Pulsed Low, DRST Tied High, External Clock

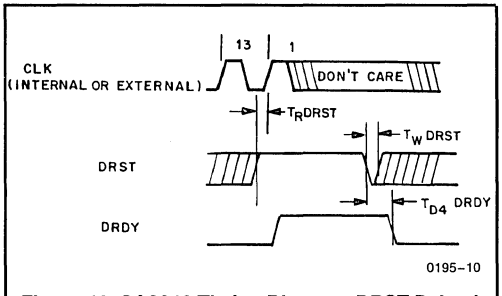


Figure 10: CA3310 Timing Diagram, DRST Pulsed Low, STRT Tied High

Analog Input

The analog input pin is a predominantly capacitive load that changes between the track and hold periods of a conversion cycle. During hold, clock period 4 through 13, the input loading is leakage and stray capacitance, typically less than 0.1 μA and 20 pF.

At the start of input tracking, clock period 1, some charge is dumped back to the input pin. The input source must have low enough impedance to dissipate the charge by the end of the tracking period. The amount of charge is dependent on supply and input voltages. Figure 11 shows typical peak input currents for various supply and input voltages, while Figure 12 shows typical average input currents. The average current is also proportional to clock frequency, and should be scaled accordingly.

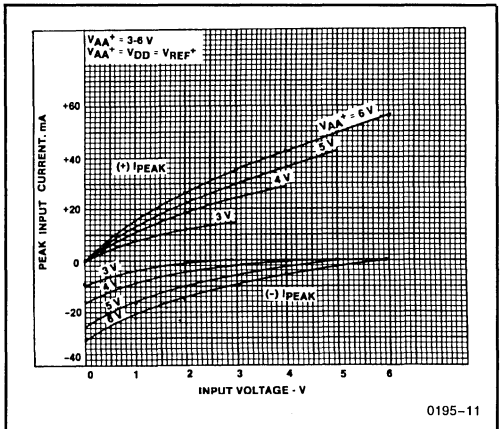


Figure 11. Typical CA3310/CA3310A Peak Input Current vs. Input Voltage

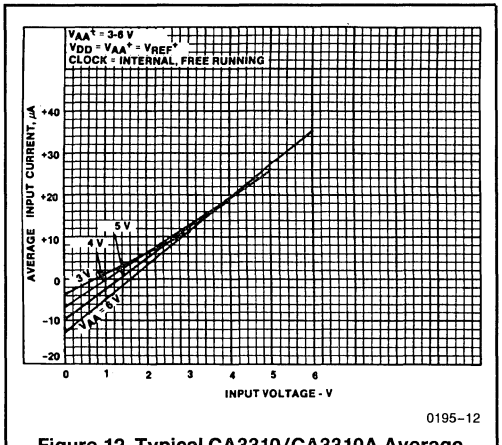


Figure 12. Typical CA3310/CA3310A Average Input Current vs. Input Voltage

During tracking, the input appears as approximately a 300 pF capacitor in series with 330Ω, for a 100 ns time constant. A full-scale input swing would settle to ½ LSB (1/2048) in 7 RC time constants. Doing continuous conversions with a 1 MHz clock provides 3 μs of tracking time, so up to 1000Ω of external source impedance (400 ns time constant) would allow proper settling of a step input.

If the clock was slower, or the converter was not restarted immediately (causing a longer sample time), a higher source impedance could be used.

NOTE: All typical values have been characterized but are not tested.

DEVICE OPERATION (Continued)

Table 2: Output Code Table

Code Description $LSB = \frac{(V_{REF+} - V_{REF-})}{1024}$	Input Voltage * $(V_{REF+} - V_{REF-}) = 4.608V$ (V)	Binary Output Code MSB D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0	Decimal Count
Zero	0.000	0	0	0	0	0	0	0	0	0	0	0
1 LSB	0.0045	0	0	0	0	0	0	0	0	0	1	1
$\frac{1}{4}(V_{REF+} - V_{REF-})$	1.152	0	1	0	0	0	0	0	0	0	0	256
$\frac{1}{2}(V_{REF+} - V_{REF-})$	2.304	1	0	0	0	0	0	0	0	0	0	512
$\frac{3}{4}(V_{REF+} - V_{REF-})$	3.456	1	1	0	0	0	0	0	0	0	0	768
$(V_{REF+} - V_{REF-}) - 1$ LSB	4.6035	1	1	1	1	1	1	1	1	1	1	1023

*The voltages listed above are the ideal centers of each output code shown as a function of its associated reference voltage.

The CA3310's low-input time constant also allows good tracking of dynamic input waveforms. The sampling rate with a 1 MHz clock is approximately 80 kHz. A Nyquist rate ($f_{SAMPLE}/2$) input sine wave of 40 kHz would have negligible attenuation and a phase lag of only 1.5 degrees.

Accuracy Specifications

The CA3310 accepts an analog input between the values of V_{REF}^- and V_{REF}^+, and quantizes it into one of 2^{10} or 1024 output codes. Each code should exist as the input is varied through a range of $1/1024 \times (V_{REF}^+ - V_{REF}^-)$, referred to as 1 LSB of input voltage. A differential linearity error, illustrated in Figure 13, occurs if an output code occurs over other than the ideal (1 LSB) input range. Note that as long as the error does not reach −1 LSB, the converter will not miss any codes.

The CA3310 output should change from a code of 000_{16} to 001_{16} at an input voltage of $(V_{REF}^- + 1\ LSB)$. It should also change from a code of $3FE_{16}$ to $3FF_{16}$ at an input of $(V_{REF}^+ - 1\ LSB)$. Any differences between the actual and expected input voltages that cause these transitions are the offset and gain errors, respectively. Figure 14 illustrates these errors.

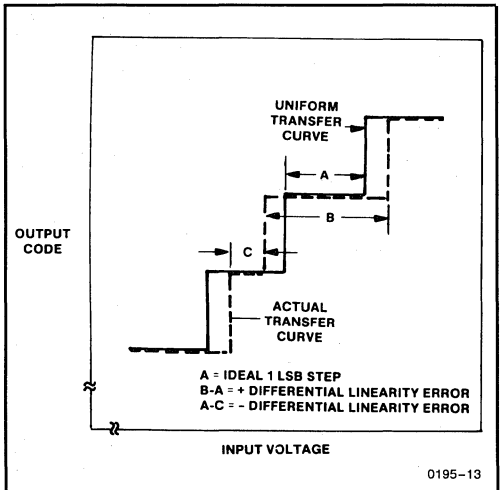


Figure 13: CA3310/CA3310A Definition of Differential Linearity Error

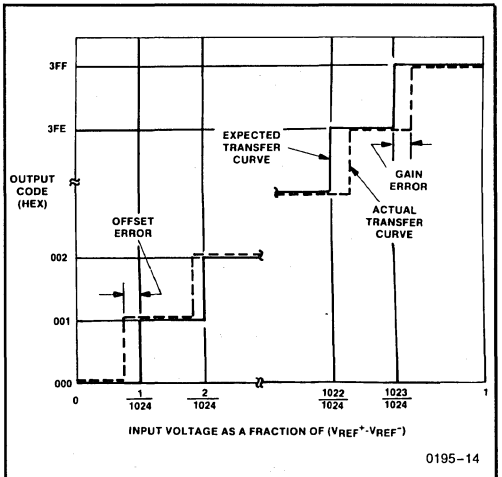


Figure 14. CA3310/CA3310A Definition of Gain and Offset Error

NOTE: All typical values have been characterized but are not tested.

DEVICE OPERATION (Continued)

As the input voltage is increased linearly from the point that causes the 000_{16} to 001_{16} transition to the point that causes the $3FE_{16}$ to $3FF_{16}$ transition, the output code should also increase linearly. Any deviation from this input-to-output correspondence is integral linearity error, illustrated in Figure 15.

Note that the integral linearity is referenced to a straight line drawn through the actual end points, not the ideal end points. For absolute accuracy to be equal to the integral linearity, the gain and offset would have to be adjusted to ideal.

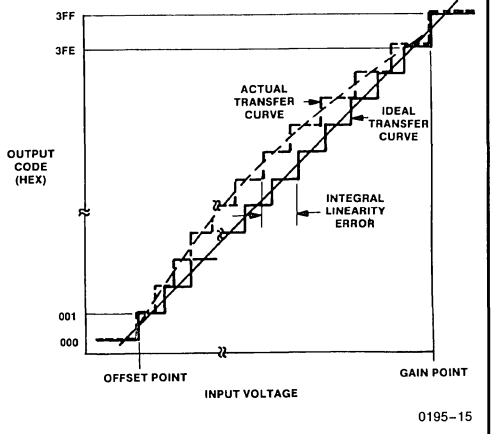


Figure 15. CA3310/CA3310A Definition of Integral Linearity Error

Offset and Gain Adjustments

The $V_{REF}+$ and $V_{REF}-$ pins, references for the two ends of the analog input range, are the only means of doing offset or gain adjustments. In a typical system, the $V_{REF}-$ might be returned to a clean ground, and offset adjustment done on an input amplifier. $V_{REF}+$ would then be adjusted for gain.

$V_{REF}-$ could be raised from ground to adjust offset or to accommodate an input source that can't drive down to ground. There are current pulses that occur, however, during the successive approximation part of a conversion cycle, as the charge-balancing capacitors are switched between $V_{REF}-$ and $V_{REF}+$. For that reason, $V_{REF}-$ and $V_{REF}+$ should be well bypassed. Figure 16 shows peak and average $V_{REF}+$ current.

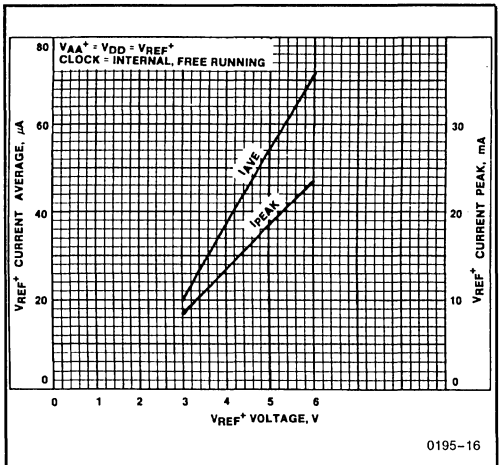


Figure 16. Typical CA3310/CA3310A $V_{REF}+$ Current vs. $V_{REF}+$ Voltage

Other Accuracy Effects

Linearity, offset, and gain errors are dependent on the magnitude of the full-scale input range, $V_{REF}+ - V_{REF}-$ Figure 17 shows how these errors vary with full-scale range.

The clocking speed is a second factor that affects conversion accuracy. Figure 18 shows the typical variation of linearity, offset, and gain errors versus clocking speed.

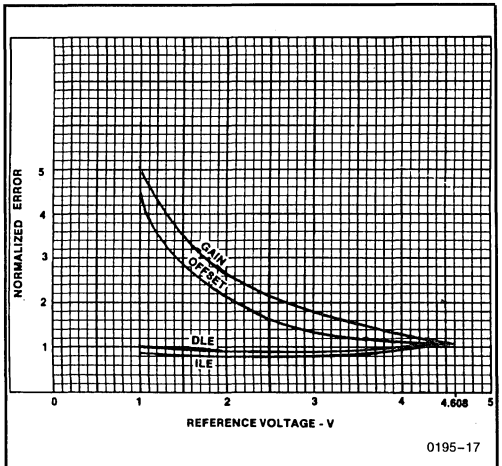


Figure 17. Typical CA3310/CA3310A Normalized Gain, Offset, Integral and Differential Linearity Errors vs. Reference Voltage

NOTE: All typical values have been characterized but are not tested.

DEVICE OPERATION (Continued)

Gain and offset drift due to temperature are kept very low by means of auto-balancing the comparator. The specifications show typical offset and gain dependency on temperature.

There is also very little linearity change with temperature, only that caused by the slight slowing of CMOS with increasing temperature. At +85°C, for instance, the ILE and DLE would be typically those for a 20% faster clock than at +25°C.

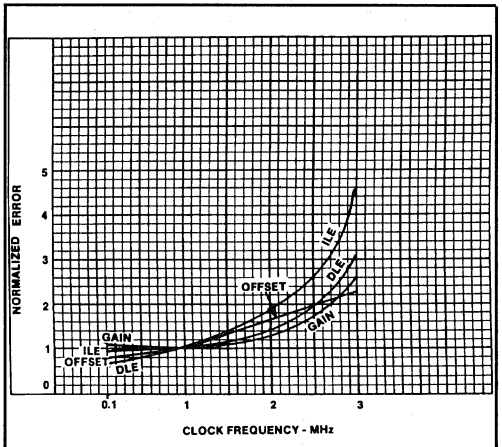


Figure 18. Typical CA3310/CA3310A Normalized Gain, Offset, Integral and Differential Linearity Errors vs. Clock Speed

Power Supplies and Grounding

V_{DD}(+) and V_{SS}(GND) are the digital supply pins: they operate all internal logic and the output drivers. Because the output drivers can cause fast current spikes in the V_{DD} and V_{SS} lines, V_{SS} should have a low impedance path to digital ground and V_{DD} should be well bypassed.

Except for V_{AA}^+, which is a substrate connection to V_{DD}, all pins have protection diodes connected to V_{DD} and V_{SS}: input transients above V_{DD} or below V_{SS} will get steered to the digital supplies. Current on these pins must be limited by external means to the values specified under maximum ratings.

The V_{AA}^+ and V_{AA}^- terminals supply the charge-balancing comparator only. Because the comparator is auto-balanced between conversions, it has good low-frequency supply rejection. It does not reject well at high frequencies, however: V_{AA}^- should be returned to a clean analog ground, and V_{AA}^+ should be RC decoupled from the digital supply.

There is approximately 50Ω of substrate impedance between V_{DD} and V_{AA}^+. This can be used, for example, as part of a low-pass R-C filter to attenuate switching supply noise. A 10 μF capacitor from V_{AA}^+ to ground would attenuate 30 kHz noise by approximately 40 dB. Note that back-to-back diodes should be placed from V_{DD} to V_{AA}^+ to handle supply to capacitor turn-on or turn-off current spikes.

Figure 19 shows V_{AA}^+ supply rejection versus frequency. Note that the frequency to be rejected scales with the clock: the 100 Hz rejection with a 100 kHz clock would be roughly equivalent to the 1 kHz rejection with a 1 MHz clock.

The supply current for the CA3310 is dependent on clock frequency, supply voltage, and temperature. Figure 20 shows the typical current versus frequency and voltage, while Figure 21 shows it versus temperature and voltage. Note that if stopped in auto-balance, the supply current is typically somewhat higher than if free-running. See Specifications.

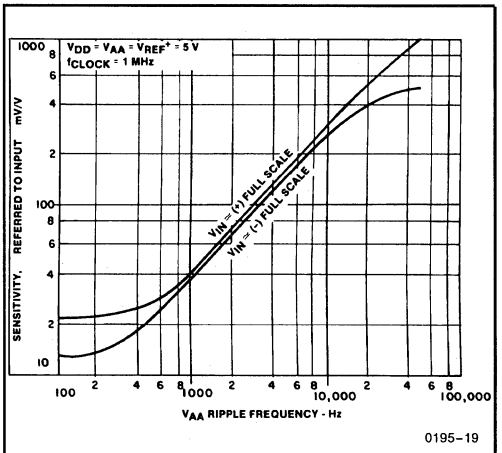


Figure 19: Typical CA3310/CA3310A V_{AA} Supply Sensitivity

NOTE: All typical values have been characterized but are not tested.

DEVICE OPERATION (Continued)

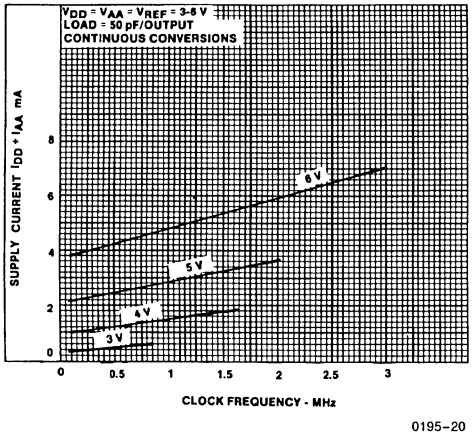


Figure 20. Typical CA3310/CA3310A Supply Current vs. Clock Frequency

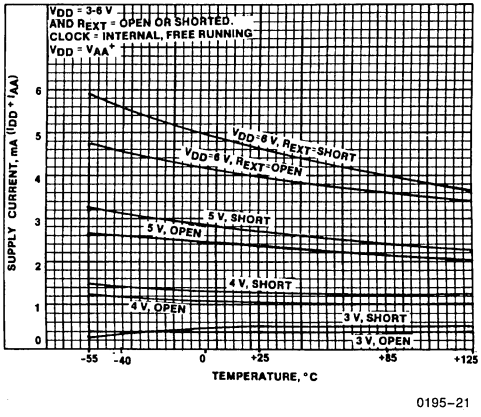


Figure 21: Typical CA3310/CA3310A Supply Current vs. Temperature

APPLICATIONS CIRCUITS

Differential Input A/D System

As the CA3310 accepts a unipolar positive-analog input, the accommodation of other ranges requires additional circuitry. The input capacitance and the input energy also force using a low-impedance source for all but slow speed use. Figure 22 shows the CA3310 with a reference, input amplifier, and input-scaling resistors for several input ranges.

The ICL7663S regulator was chosen as the reference, as it can deliver less than 0.25V input-to-output (dropout) voltage and uses very little power. As high a reference as possible is generally desirable, resulting in the best linearity and rejection of noise at the CA3310.

The tantalum capacitor sources the V_{REF} current spikes during a conversion cycle. This relieves the response and peak current requirements of the reference.

The CA3140 op-amp provides good slewing capability for high bandwidth input signals and can quickly settle the energy that the CA3310 outputs at its V_{IN} terminal. It can also drive close to the negative supply rail.

If system supply sequencing or an unknown input voltage is likely to cause the op-amp to drive above the V_{DD} supply, a diode clamp can be added from pin 8 of the op-amp to the V_{DD} supply. The minus drive current is low enough not to require protection.

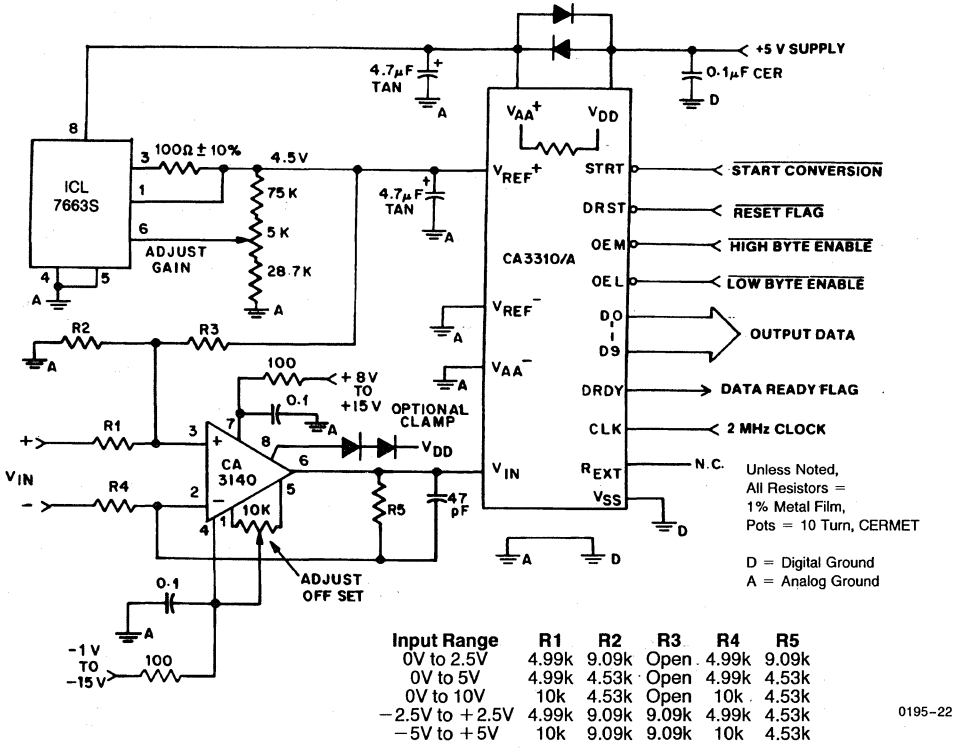
With a 2 MHz clock (~ 150 kHz sampling), Nyquist criteria would give a maximum input bandwidth of 75 kHz. The resistor values chosen are low enough to not seriously degrade system bandwidth (an op-amp settling) at that clock frequency. If A/D clock frequency and bandwidth requirements are lower, the resistor values (and input impedance) can be made correspondingly higher.

The A/D system would generally be calibrated by tying V_{IN}^- to ground and applying a voltage to V_{IN}^+ that is 0.5 LSB (1/2048 of full-scale range) above ground. The op-amp offset should be adjusted for an output code dithering between 000_{16} and 001_{16} for unipolar use, or 100_{16} and 101_{16} for bipolar use. The gain would then be adjusted by applying a voltage that is 1.5 LSB below the positive full-scale input, and adjusting the reference for an output dithering between $3FE_{16}$ and $3FF_{16}$.

4

NOTE: All typical values have been characterized but are not tested.

APPLICATIONS CIRCUITS (Continued)



Input Range	R1	R2	R3	R4	R5
0V to 2.5V	4.99k	9.09k	Open	4.99k	9.09k
0V to 5V	4.99k	4.53k	Open	4.99k	4.53k
0V to 10V	10k	4.53k	Open	10k	4.53k
−2.5V to +2.5V	4.99k	9.09k	9.09k	4.99k	4.53k
−5V to +5V	10k	9.09k	9.09k	10k	4.53k

Figure 22. Unipolar or Bipolar Differential Input and A/D Converter System

Note that R1 through R5 should be very well matched, as they affect the common-mode rejection of the A/D system. Also, if R2 and R3 are not matched, the offset adjust of the op-amp may not have enough adjustment range in biploar systems.

The common-mode input range of the system is set by the supply voltage available to the op-amp. The range that can be applied to the V_{IN}^- terminal can be calculated by:

$\left(\frac{R4}{R5} + 1\right) V_{IN}^-$ for the most negative

$\left(\frac{R4}{R5} + 1\right) (V_{IN}^+ - 2.5V) - \left(\frac{R4}{R5}\right) V_{REF}^+$ for the most positive

Single +5V Supply

If only a single 5V supply is available, an ICL7660 can be used to provide approximately +8V and −4V to the op-amp. Figure 23 shows this approach. Note that the converter and associated capacitors should be grounded to the digital supply. The 100Ω in series with each supply at the op-amp isolates digital and analog grounds.

Digital Sample and Hold

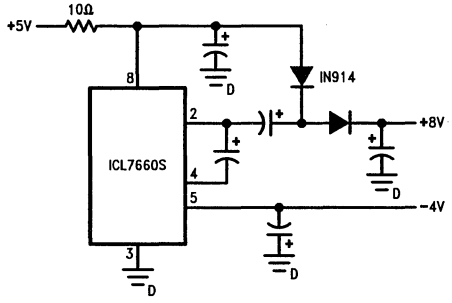
With a minimum of external logic, the CA3310 can be made to wait at the verge of ending a sample. A start pulse will then, after the internal aperture delay, capture the input and finish the conversion cycle. Figure 24 illustrates this application.

The CA3310 is connected as if to free run. The Data Ready signal is shifted through a CD74HC175, and at the low-going clock edge just before the sample would end, is used to hold the clock low.

The same signal, active high, is available to indicate the CA3310 is ready to convert. A low pulse to reset the CD74HC175 will now release the clock, and the sample will end as it goes positive. Ten cycles later, the conversion will be complete, and DRDY will go active.

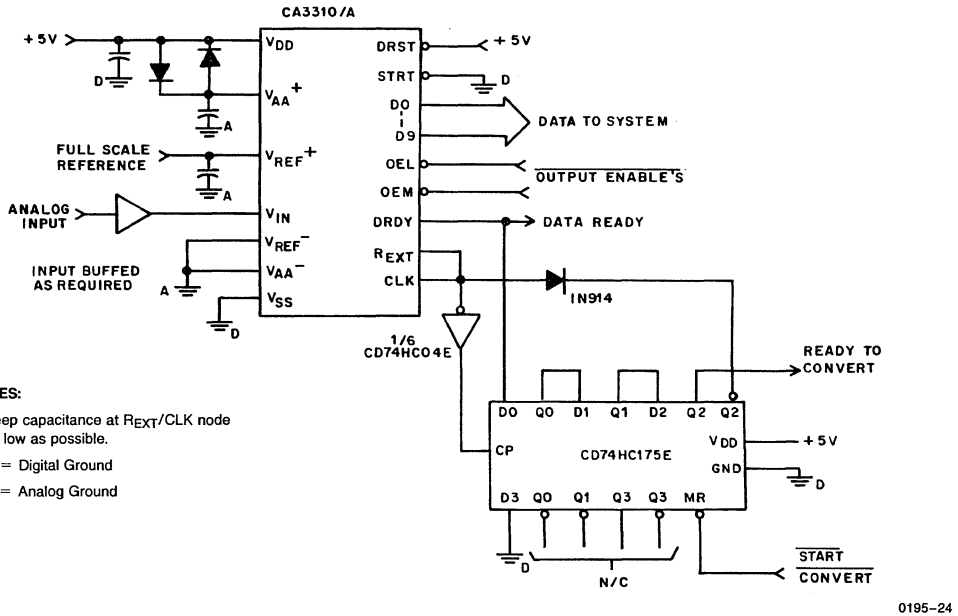
NOTE: All typical values have been characterized but are not tested.

APPLICATIONS CIRCUITS (Continued)



All Capacitors = 10 μF, 10V
D = Digital Ground

Figure 23: Plus and Minus Voltage Supply for Op-Amp



NOTES:

Keep capacitance at R_{EXT}/CLK node as low as possible.

D = Digital Ground

A = Analog Ground

Figure 24: Digital Track-and-Hold Block Diagram

NOTE: All typical values have been characterized but are not tested.

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of Harris CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6526. "Guide to Better Handling and Operation of CMOS Integrated Circuits".

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD} - V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than $V_{DD} + 0.3V$ nor less than $V_{SS} - 0.3V$. Input currents must not exceed 20 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

NOTE: All typical values have been characterized but are not tested.

HI-574A

Fast, Complete 12-Bit A/D Converter with Microprocessor Interface

Features

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8-, 12- or 16-Bit Microprocessor Bus Interface
- 150ns Bus Access Time
- No Missing Codes Over Temperature
- Minimal Set-up Time for Control Signals
- 25μs Maximum Conversion Time
- Low Noise, via Current-Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle (A_0 Input)
  - Guaranteed Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by the Start Convert Input (To Set the Conversion Length)
- Improved Second Source for AD574A and HS574
- $\pm$12V to $\pm$15V Operation

Applications

- Military and Industrial Data Acquisition Systems
- Electronic Test and Scientific Instrumentation
- Process Control Systems

Description

The HI-574A is a complete 12-bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28 pin package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

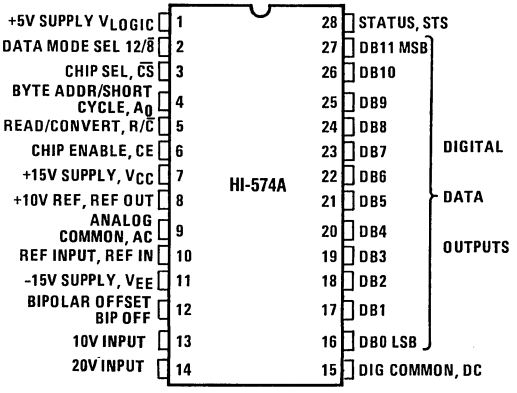
Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 20 $\pm$ 1μs.

The HI-574A offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

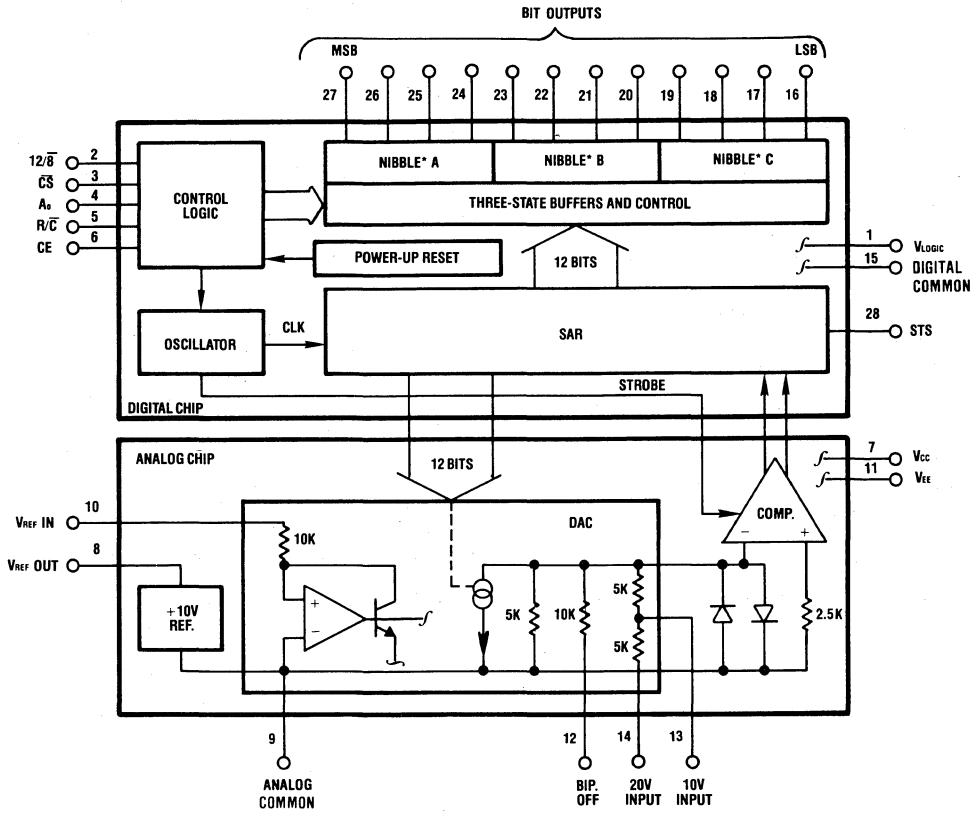
Power requirements are +5V and $\pm$12V to $\pm$15V, with typical dissipation of 385mW at $\pm$12V. All models are available in a 28 pin Sidebrazed DIP. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. For MIL-STD-883 compliant parts, request the HI-574A/883 data sheet.

Pinouts

SIDEBRAZE DIP
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.



("NIBBLE" IS A 4 BIT DIGITAL WORD.)

Specifications HI-574A

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC and Transfer Accuracy Specifications

MODEL	HI-574AJ	HI-574AK	HI-574AL	UNITS
Temperature Range		−5 (0°C to +75°C)		
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C (max)	±1	±1/2	±1/2	LSB
0°C to +75°C (max)	±1	±1/2	±1/2	LSB
Differential Linearity Error				
25°C	±1	±1	±1/2	LSBs
(Maximum resolution for which no missing codes is guaranteed)				
25°C	12	12	12	Bits
Tmin to Tmax	11	12	12	Bits
Unipolar Offset (max)				
(Adjustable to zero)	±2	±1.5	±1	LSB
Bipolar Offset (max) V_{IN} = 0V (Adjustable to zero)	±4	±4	±3	LSB
V_{IN} = −10V	±0.15	±0.1	±0.1	% of F.S.
Full Scale Calibration Error				
25°C (max), with fixed 50 Ω resistor from REF OUT to REF IN (Adjustable to zero)	±0.25	±0.25	±0.15	% of F.S.
T_{min} to T_{max}				
(No adjustment at +25°C)	±0.475	±0.375	±0.20	% of F.S.
(With adjustment to zero at +25°C)	±0.22	±0.12	±0.05	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{min} to T_{max} (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Bipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Full Scale Calibration	±9	±2	±2	LSB
	(45)	(10)	(10)	(ppm/°C)
Power Supply Rejection				
Max change in Full Scale Calibration				
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	±1	LSB
+4.5V<V_{LOGIC}<+5.5V	±1/2	±1/2	±1/2	LSB
−16.5V<V_{EE}<−13.5V or −12.6V<V_{EE}<−11.4V	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar	−5 to +5			Volts
	−10 to +10			Volts
Unipolar	0 to +10			Volts
	0 to +20			Volts
Input Impedance				
10 Volt Span	5K, ± 25%			Ohms
20 Volt Span	10K, ± 25%			Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			Volts
V_{EE}	−11.4 to −16.5			Volts
Operating Current				
I_{LOGIC}	7 TYP, 15 MAX			mA
I_{CC} +15V Supply	11 TYP, 15 MAX			mA
I_{EE} -15V Supply	21 TYP, 28 MAX			mA
Power Dissipation				
±15V, +15V	515 TYP, 720 MAX			mW
±12V, +5V	385 TYP			mW
Internal Reference Voltage, T_{min} to T_{max}	+10.00 ± 0.5 MAX			Volts
Output current,[1]	2.0 MAX			mA
available for external loads (External load should not change during conversion).				

1. *When supplying an external load (not including the ADC) and operating on* ±12V supplies, a buffer amplifier must be provided for the Reference Output.

Specifications HI-574A

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC and Transfer Accuracy Specifications

MODEL	HI-574AS	HI-574AT	HI-574AU	UNITS
Temperature Range	-2, -8 (55°C to +125°C)			
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C(max)	±1	±1/2	±1/2	LSB
0°C to +75°C(max)	±1	±1	±1	LSB
Differential Linearity Error	±1	±1	±1/2	LSBs
25°C				
(Maximum resolution for which no missing codes is guaranteed)				
25°C	12	12	12	Bits
Tmin to Tmax	11	12	12	Bits
Unipolar Offset (max)				
(Adjustable to zero)	±2	±1.5	±1	LSB
Bipolar Offset (max) V_{IN} = 0V (Adjustable to zero)	±4	±4	±3	LSB
V_{IN} = -10V	±0.15	±0.1	±0.1	% of F.S.
Full Scale Calibration Error				
25°C (max), with fixed 50 Ω resistor from				
REF OUT to REF IN (Adjustable to zero)	±0.25	±0.25	±0.15	% of F.S.
T_{min} to T_{max}				
(No adjustment at +25°C)	±0.75	±0.50	±0.275	% of F.S.
(With adjustment to zero at +25°C)	±0.50	0.25	±0.125	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{min} to T_{max} (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
	(5)	(2.5)	(2.5)	(ppm/°C)
Bipolar Offset	±2	±2	±1	LSB
	(5)	(5)	(2.5)	(ppm/°C)
Full Scale Calibration	±20	±10	±5	LSB
	(50)	(25)	(12.5)	(ppm/°C)
Power Supply Rejection				
Max change in Full Scale Calibration				
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	±1	LSB
+4.5V<V_{LOGIC}<+5.5V	±1/2	±1/2	±1/2	LSB
−16.5V<V_{EE}<−13.5V or −12.6V<V_{EE}<−11.4V	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar	−5 to +5			Volts
	−10 to +10			Volts
Unipolar	0 to +10			Volts
	0 to +20			Volts
Input Impedance				
10 Volt Span	5K Ω, ± 25%			Ohms
20 Volt Span	10K Ω, ± 25%			Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			Volts
V_{EE}	−11.4 to −16.5			Volts
Operating Current				
I_{LOGIC}	7 TYP, 15 MAX			mA
I_{CC} +15V Supply	11 TYP, 15 MAX			mA
I_{EE} -15V Supply	21 TYP, 28 MAX			mA
Power Dissipation				
±15V, +15V	515 TYP, 720 MAX			mW
±12V, +5V	385 TYP			mW
Internal Reference Voltage, T_{min} to T_{max}	+10.00 ±.05 MAX			Volts
Output current available for external loads (External load should not change during conversion)	2.0 MAX			mA

DIGITAL CHARACTERISTICS[1]
(ALL MODELS, OVER FULL TEMP. RANGE)

	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A0, 12/$\overline{8}$)[2]			
Logic "1"	+2.4V		+5.5V
Logic "0"	−0.5V		+0.8V
Current	−5μA	±0.1μA	+5μA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} — 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} — 500μA)	+2.4V		
Leakage (High - Z State, DB11-DB0 ONLY)	−5μA	±0.1μA	+5μA
Capacitance		5pF	

[1] *See "HI-574A Timing Specifications" for a detailed listing of digital timing parameters.*

[2] *Although this guaranteed threshold is higher than standard TTL (+2.0V), bus loading is much less, i.e., typical input current is only 0.25% of a TTL load.*

Absolute Maximum Ratings

(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common ..... 0 to +16.5V
V_{EE} to Digital Common ..... 0 to −16.5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common ..... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to Analog Common ..... ±16.5V
$20V_{IN}$ to Analog Common ..... ±24V
REF OUT ..... Indefinite short to common
Momentary short to V_{CC}
Junction Temperature ..... 175°C
Lead Temperature, Soldering ..... 300°C, 10 sec.
Storage Temperature ..... −65°C to +150°C

***Derate 20.8mW/°C above 75°C**

Ordering Information

PART NUMBER	INL	TEMPERATURE RANGE	PACKAGE
HI1-574AJD-5	±1 LSB	0°C to +75°C	28-Pin Ceramic Dip
HI1-574AKD-5	±0.5 LSB	0°C to +75°C	28-Pin Ceramic Dip
HI1-574ALD-5	±0.5 LSB	0°C to +75°C	28-Pin Ceramic Dip
HI1-574ASD-2	±1 LSB	-55°C to +125°C	28-Pin Ceramic Dip
HI1-574ATD-2	±0.5 LSB	-55°C to +125°C	28-Pin Ceramic Dip
HI1-574AUD-2	±0.5 LSB	-55°C to +125°C	28-Pin Ceramic Dip
HI1-574ASD/883	±1 LSB	-55°C to +125°C	28-Pin Ceramic Dip
HI1-574ATD/883	±0.5 LSB	-55°C to +125°C	28-Pin Ceramic Dip
HI1-574AUD/883	±0.5 LSB	-55°C to +125°C	28-Pin Ceramic Dip
HI4-574ASE/883	±1 LSB	-55°C to +125°C	44-Pin Ceramic LCC
HI4-574ATE/883	±0.5 LSB	-55°C to +125°C	44-Pin Ceramic LCC
HI4-574AUE/883	±0.5 LSB	-55°C to +125°C	44-Pin Ceramic LCC

Definitions of Specifications

LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-574AK, AL, AT, and AU grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-574AJ and AS grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.
Note that the linearity error is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-574AK, AL, AT, and AU grades, which

Definitions of Specifications (Continued)

guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-574AJ and AS grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1½LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

POWER SUPPLY REJECTION

The standard specifications for the HI-574A assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT-JUSTIFIED DATA

The data format used in the HI-574A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

Applying the HI-574A

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout –

Unwanted, parasitic circuit components, (L, R, and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-574A (+15V, −15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections

The typical HI-574A ground currents are 5.5mADC into pin 9 (Analog Common)and 7mADC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 1.5mA of DC current. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-574A's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device chosen to drive the HI-574A analog input will see a nominal load of 5KΩ (10V range) or 10KΩ (20V range). However, the other end of these input resistors may change ±400mV with each bit decision, creating abrupt changes in current at the analog input. Thus, the signal source must maintain its output voltage while furnishing these step changes in load current, which occur at 1.6μS intervals. This requires low output impedance and fast settling by the signal source.

The output impedance of an op amp, for example, has an open loop value which, in a closed loop, is divided by the loop gain available at a frequency of interest. The amplifier should have acceptable loop gain at 600KHz for use with the HI-574A. To check whether the output properties of a signal source are suitable, monitor the 574A's input (pin 13 or 14) with an oscilloscope while a conversion is in progress. Each of the twelve disturbances should subside in one microsecond or less. (The comparator decision is made about 1.5μS after each code change from the SAR).

If the application calls for a Sample/Hold to precede the converter, it should be noted that not all Sample/Holds are compatible with the HI-574A in the manner described above. These will require an additional wideband buffer amplifier to lower their output impedance. A simpler solution is to use the Harris HA-5320 Sample/Hold, which was designed for use with the HI-574A.

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-574A is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in Figures 2 and 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-574A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration –

Refer to Fig. 2. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem – the converter operates normally.

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is setting the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one

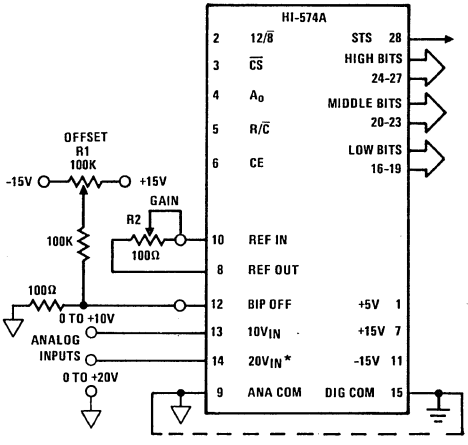


FIGURE 2. UNIPOLAR CONNECTIONS

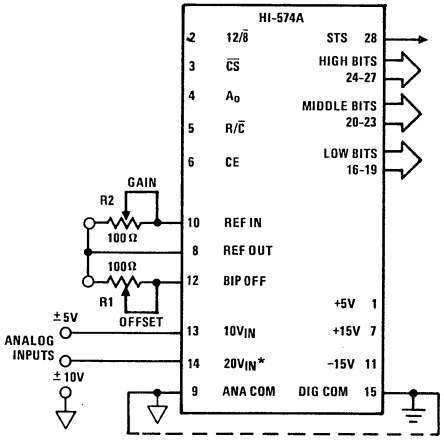


FIGURE 3 BIPOLAR INPUT CONNECTIONS

*When driving the 20V (pin 14) input, minimize capacitance on pin 13.

LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +1/2 LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is 1-1/2 LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration –

Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage 1/2 LSB above negative full scale (i.e., −4.9988V for the ±5V range, or −9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1-1/2 LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

* The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 500Ω potentiometer in series with pin 14.

CONTROLLING THE HI-574A

The HI-574A includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8 or 12 bit conversion cycle, initiating the conversion, and reading the output data when ready – choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS-compatible: (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 4.

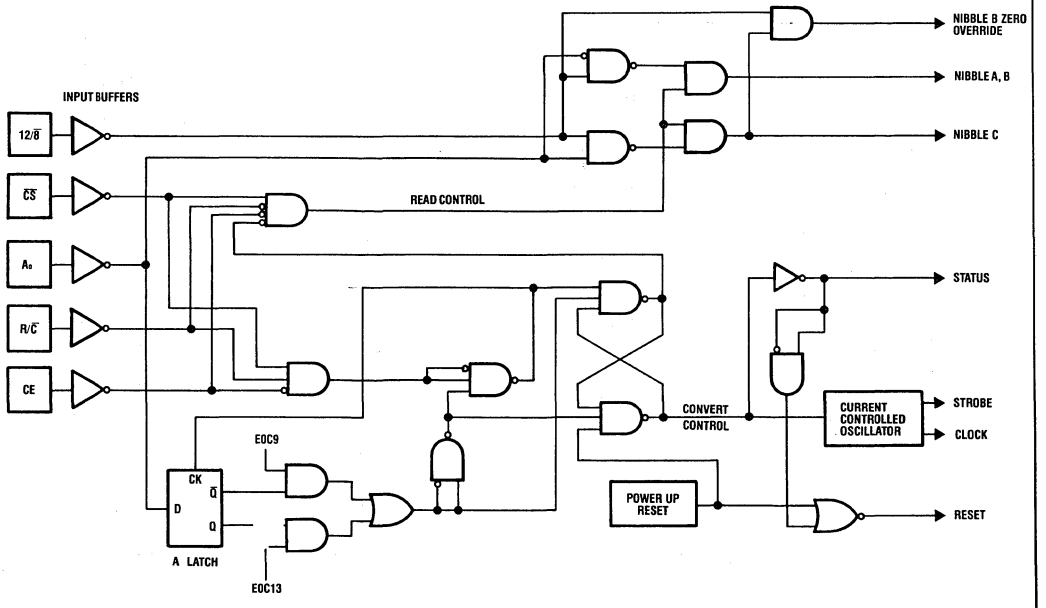


FIGURE 4. HI-574A CONTROL LOGIC

"Stand-Alone Operation"

The simplest control interface calls for a single control line connected to R/$\overline{C}$. Also, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and the output data appears in words of 12 bits each.

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 5 and 6. In general, data may be read when R/C is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed below under "Stand-Alone Mode Timing."

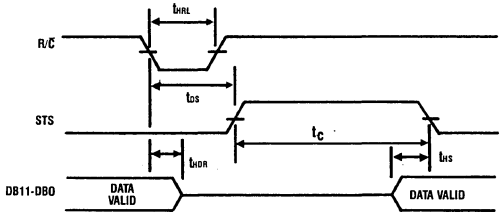


FIGURE 5. LOW PULSE FOR R/$\overline{C}$ – OUTPUTS ENABLED AFTER CONVERSION

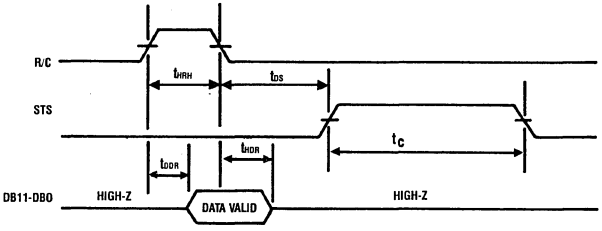


FIGURE 6. HIGH PULSE FOR R/$\overline{C}$ – OUTPUTS ENABLED WHILE R/C HIGH, OTHERWISE HIGH-Z

STAND-ALONE MODE TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
tHRL	Low R/C Pulse Width	50	–	–	ns
tDS	STS Delay From R/C	–	–	200	ns
tHDR	Data Valid After R/C Low	25	–	–	ns
tHS	STS Delay After Data Valid	300	–	1200	ns
tHRH	High R/C Pulse Width	150	–	–	ns
tDDR	Data Access Time	–	–	150	ns

Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

Conversion Length

A Convert Start transition (see Table 1) latches the state of A_0, which determines whether the conversion continues for 12 bits (A_0 low) or stops with 8 bits (A_0 high). If all 12 bits are read following an 8 bit conversion, the three LSB's will read zero and DB3 will read ONE. A_0 is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

TABLE 1

Truth Table for HI-574A Control Inputs.

Conversion Start

A conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50nS earlier, however. See the HI-574A Timing Specifications, Convert mode.

This variety of HI-574A control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 7.

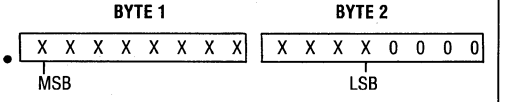
The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high. (However, if A_0 changes state after a conversion begins, an additional Start Convert signal will latch the new state of A_0, possibly causing a wrong cycle length (8 vs 12 bits) for that conversion).

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A_0. Timing constraints are illustrated in Figure 8.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS-compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16 bit data bus. The A_0 input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8 bit bytes, selected one at a time by A_0. This allows an 8 bit data bus to be connected as shown in Figure 9. A_0 is usually tied to the least significant bit of the address bus, for storing the HI-574A output in two consecutive memory locations. (With A_0 low, the 8 MSB's only are enabled. With A_0 high, 4 MSB's are disabled, bits 4 through 7 are forced to zero, and the 4 LSB's are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:



Further, A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 9 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than (t_{DD} + t_{HS}) before STS goes low. See Figure 8.

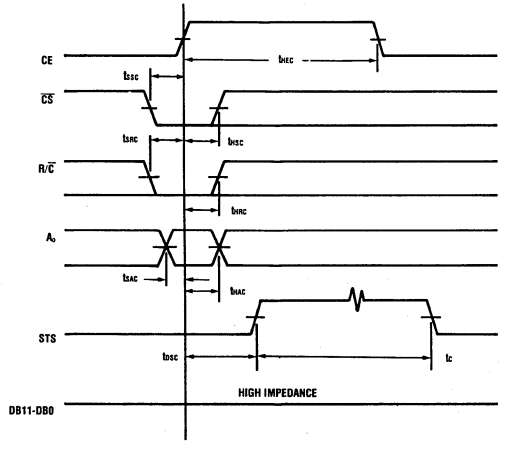


FIGURE 7. CONVERT START TIMING

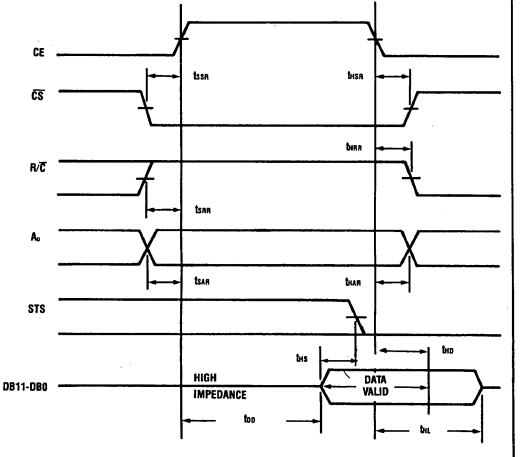


FIGURE 8. READ CYCLE TIMING

Timing Specifications +25°C Unless Otherwise Specified

Symbol	Parameter	Min	Typ	Max	Units
Convert Mode					
t_{DSC}	STS Delay from CE			200	nS
t_{HEC}	$\overline{CE}$ Pulse width	50			nS
t_{SSC}	$\overline{CS}$ to CE Setup	50			nS
t_{HSC}	$\overline{CS}$ Low during CE High	50			nS
t_{SRC}	R/$\overline{C}$ to CE Setup	50			nS
t_{HRC}	R/$\overline{C}$ Low during CE high	50			nS
t_{SAC}	A_0 to CE Setup	0			nS
t_{HAC}	A_0 Valid during CE high	50			nS
t_C	Conversion time, 12 bit cycle T min to T max	15	20	25	μS
	8 bit cycle T min to T max	10	13	17	μS
Read Mode					
t_{DD}	Access time from CE		75	150	nS
t_{HD}	Data Valid after CE low	25			nS
t_{HL}	Output float delay		100	150	nS
t_{SSR}	$\overline{CS}$ to CE setup	50			nS
t_{SRR}	R/$\overline{C}$ to CE setup	0			nS
t_{SAR}	A_0 to CE setup	50			nS
t_{HSR}	$\overline{CS}$ valid after CE low	0			nS
t_{HRR}	R/$\overline{C}$ high after CE low	0			nS
t_{HAR}	A_0 valid after CE low	50			nS
t_{HS}	STS delay after data valid	300		1200	nS

NOTE: Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

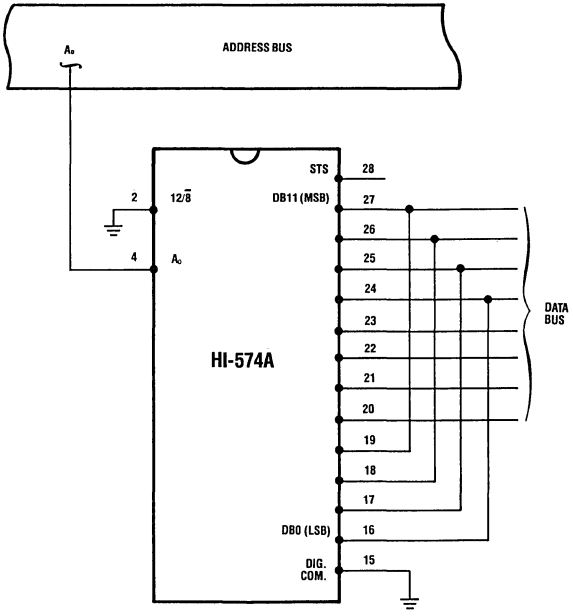


FIGURE 9 INTERFACE TO AN 8 BIT DATA BUS

DIE CHARACTERISTICS

Transistor Count		1117	Thermal Constants;	θja	48°C/W
Die Size:	Analog	204 x 104 mils		θjc	15°C/W
	Digital	158 x 84 mils	Process:		Bipolar – DI and CMOS – JI

HARRIS

HI-674A

12μs, Complete 12-Bit A/D Converter with Microprocessor Interface

Features

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8-, 12- or 16-Bit Microprocessor Bus Interface
- 150ns Bus Access Time
- No Missing Codes Over Temperature
- Minimal Set-up Time for Control Signals
- 15μs Maximum Conversion Time
- Low Noise, via Current-Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle (A_0 Input)
  - ▸ Guaranteed Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by the Start Convert Input (To Set the Conversion Length)
- Faster Version of the HI-574A
- Same Pinout as the HI-574A
- ±12V to ±15V Operation

Applications

- Military and Industrial Data Acquisition Systems
- Electronic Test and Scientific Instrumentation
- Process Control Systems

Description

The HI-674A is a complete 12-bit Analog-to-Digital Converter, including a +10V reference, clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28 pin package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

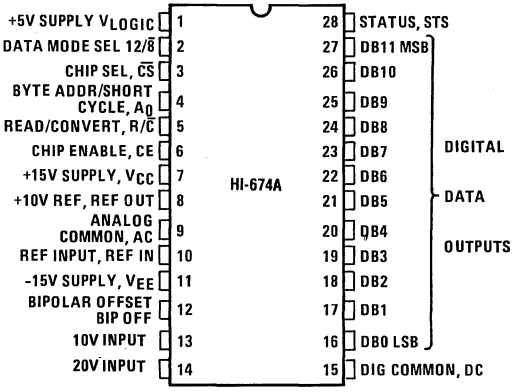
Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current-controlled for excellent stability over temperature. The oscillator is trimmed for a nominal conversion time of 12 ± 1μs.

The HI-674A offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are +5V and ±12V to ±15V, with typical dissipation of 385mW at ±12V. All models are available in a 28 pin Sidebrazed DIP. For additional Hi-Rel screening including 160 hour burn-in specify the "-8" suffix. For MIL-STD-883 compliant parts, request the HI-674A/883 data sheet.

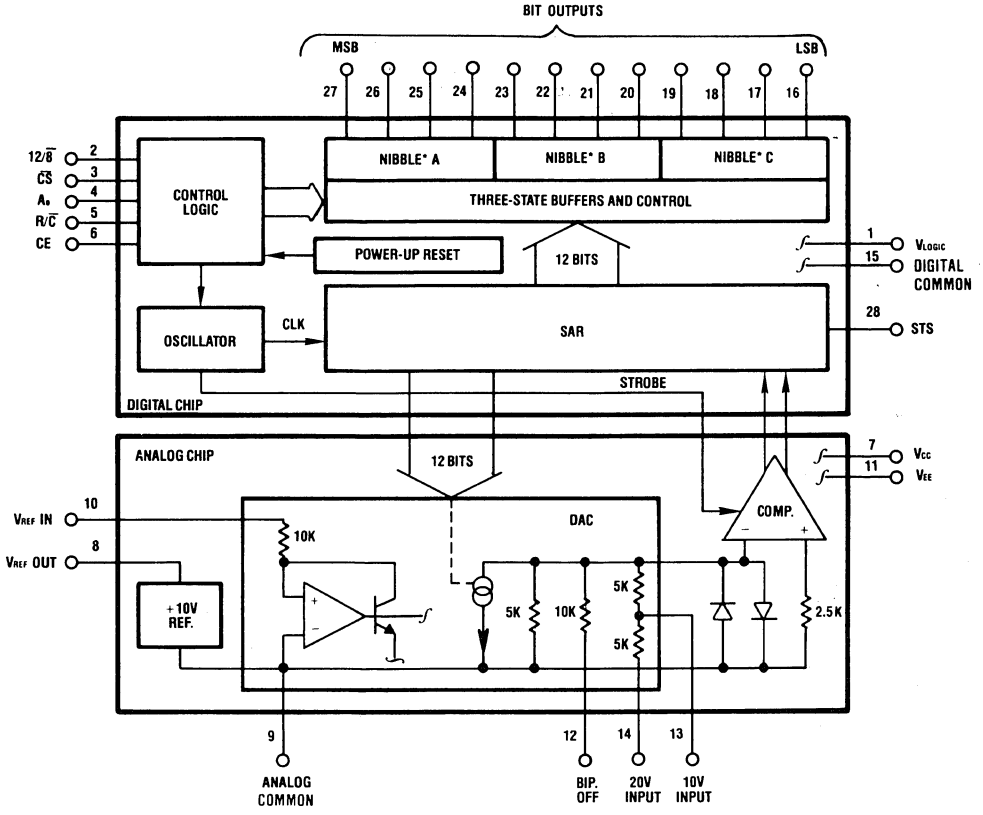
Pinout

CERAMIC DIP
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Block Diagram



*("NIBBLE" IS A 4 BIT DIGITAL WORD.)

Specifications HI-674A

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC and Transfer Accuracy Specifications

MODEL	HI-674AJ	HI-674AK	HI-674AL	UNITS
Temperature Range		-5 (0°C to +75°C)		
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C (max)	±1	±1/2	±1/2	LSB
0°C to +75°C (max)	±1	±1/2	±1/2	LSB
Differential Linearity Error	±1	±1	±1/2	LSBs
25°C				
(Maximum resolution for which no missing codes is guaranteed)				
25°C	12	12	12	Bits
Tmin to Tmax	11	12	12	Bits
Unipolar Offset (max)				
(Adjustable to zero)	±2	±1.5	±1	LSB
Bipolar Offset (max) V_{IN} = 0V (Adjustable to zero)	±4	±4	±3	LSB
V_{IN} = -10V	±0.15	±0.1	±0.1	% of F.S.
Full Scale Calibration Error				
25°C (max), with fixed 50 Ω resistor from				
REF OUT to REF IN (Adjustable to zero)	±0.25	±0.25	±0.15	% of F.S.
T_{min} to T_{max}				
(No adjustment at +25°C)	±0.475	±0.375	±0.20	% of F.S.
(With adjustment to zero at +25°C)	±0.22	0.12	0.05	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{min} to T_{max} (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Bipolar Offset	±2	±1	±1	LSB
	(10)	(5)	(5)	(ppm/°C)
Full Scale Calibration	±9	±2	±2	LSB
	(45)	(10)	(10)	(ppm/°C)
Power Supply Rejection				
Max change in Full Scale Calibration				
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	±1	LSB
+4.5V<V_{LOGIC}<+5.5V	±1/2	±1/2	±1/2	LSB
−16.5V<V_{EE}<−13.5V or −12.6V<V_{EE}<−11.4V	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar	−5 to +5			Volts
	−10 to +10			Volts
Unipolar	0 to +10			Volts
	0 to +20			Volts
Input Impedance				
10 Volt Span	5K, ± 25%			Ohms
20 Volt Span	10K, ± 25%			Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			Volts
V_{EE}	−11.4 to −16.5			Volts
Operating Current				
I_{LOGIC}	7 TYP, 15 MAX			mA
I_{CC} +15V Supply	11 TYP, 15 MAX			mA
I_{EE} -15V Supply	21 TYP, 28 MAX			mA
Power Dissipation				
±15V, +5V	515 TYP, 720 MAX			mW
±12V, +5V	385 TYP			mW
Internal Reference Voltage, T_{min} to T_{max}	+10.00 ±.05 MAX			Volts
Output current available for external loads (External load should not change during conversion)	2.0 MAX			mA

Specifications HI-674A

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC and Transfer Accuracy Specifications

MODEL	HI-674AS	HI-674AT	HI-674AU	UNITS
Temperature Range	-2, -8 (55°C to +125°C)			
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C(max)	±1	±1/2	±1/2	LSB
0°C to +75°C(max)	±1	±1	±1	LSB
Differential Linearity Error	±1	±1	±1/2	LSBs
25°C				
(Maximum resolution for which no missing codes is guaranteed)				
25°C	12	12	12	Bits
Tmin to Tmax	11	12	12	Bits
Unipolar Offset (max)				
(Adjustable to zero)	±2	±1.5	±1	LSB
Bipolar Offset (max) V_{IN} = 0V (Adjustable to zero)	±4	±4	±3	LSB
V_{IN} = -10V	±0.15	±0.1	±0.1	% of F.S.
Full Scale Calibration Error				
25°C (max), with fixed 50 Ω resistor from				
REF OUT to REF IN (Adjustable to zero)	±0.25	±0.25	±0.15	% of F.S.
T_{min} to T_{max}				
(No adjustment at +25°C)	±0.75	±0.50	±0.275	% of F.S.
(With adjustment to zero at +25°C)	±0.50	0.25	±0.125	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{min} to T_{max} (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
	(5)	(2.5)	(2.5)	(ppm/°C)
Bipolar Offset	±2	±2	±1	LSB
	(5)	(5)	(2.5)	(ppm/°C)
Full Scale Calibration	±20	±10	±5	LSB
	(50)	(25)	(12.5)	(ppm/°C)
Power Supply Rejection				
Max change in Full Scale Calibration				
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	±1	LSB
+4.5V<V_{LOGIC}<+5.5V	±1/2	±1/2	±1/2	LSB
−16.5V<V_{EE}<−13.5V or −12.6V<V_{EE}<−11.4V	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar	−5 to +5			Volts
	−10 to +10			Volts
Unipolar	0 to +10			Volts
	0 to +20			Volts
Input Impedance				
10 Volt Span	5K Ω, ± 25%			Ohms
20 Volt Span	10K Ω, ± 25%			Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			Volts
V_{EE}	−11.4 to −16.5			Volts
Operating Current				
I_{LOGIC}	7 TYP, 15 MAX			mA
I_{CC} +15V Supply	11 TYP, 15 MAX			mA
I_{EE} -15V Supply	21 TYP, 28 MAX			mA
Power Dissipation				
±15V, +15V	515 TYP, 720 MAX			mW
±12V, +5V	385 TYP			mW
Internal Reference Voltage, T_{min} to T_{max}	+10.00 ±.05 MAX			Volts
Output current available for external loads (External load should not change during conversion)	2.0 MAX			mA

4

Digital Specifications[1] (All Models, Over Full Temperature Range)

	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A0, 12/$\overline{8}$)[2]			
Logic "1"	+2.4V		+5.5V
Logic "0"	−0.5V		+0.8V
Current	−5μA	±0.1μA	+5μA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} — 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} — 500μA)	+2.4V		
Leakage (High - Z State, DB11-DB0 ONLY)	−5μA	±0.1μA	+5μA
Capacitance		5pF	

1 See "HI-674A Timing Specifications" for a detailed listing of digital timing parameters.

2 Although this guaranteed threshold is higher than standard TTL (+2.0V), bus loading is much less, i.e., typical input current is only 0.25% of a TTL load.

Absolute Maximum Ratings

(Specifications apply to all grades, except where noted)

V_{CC} to Digital Common ..... 0 to +16.5V
V_{EE} to Digital Common ..... 0 to −16.5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to
Digital Common ..... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, 10V_{IN}) to
Analog Common ..... ±16.5V
20V_{IN} to Analog Common ..... ±24V
REF OUT ..... Indefinite short to common
Momentary short to V_{CC}
Junction Temperature ..... 175°C
Lead Temperature, Soldering ..... 300°C, 10 sec.
Storage Temperature ..... −65°C to +150°C

Ordering Information

PART NUMBER	INL	TEMPERATURE RANGE	PACKAGE
HI1-674AJD-5	±1 LSB	0°C to +75°C	28 Pin Ceramic DIP
HI1-674AKD-5	±0.5 LSB	0°C to +75°C	28 Pin Ceramic DIP
HI1-674ALD-5	±0.5 LSB	0°C to +75°C	28 Pin Ceramic DIP
HI1-674ASD-2	±1 LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-674ATD-2	±0.5 LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-674AUD-2	±0.5 LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-674ASD/883	±1 LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-674ATD/883	±0.5 LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-674AUD/883	±0.5 LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI4-674ASE/883	±1 LSB	-55°C to +125°C	44 Pin Ceramic LCC
HI4-674ATE/883	±0.5 LSB	-55°C to +125°C	44 Pin Ceramic LCC
HI4-674AUE/883	±0.5 LSB	-55°C to +125°C	44 Pin Ceramic LCC

Definitions of Specifications

LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-674AK, AL, AT, and AU grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-674AJ and AS grades are guaranteed to ±1LSB max error. For these grades, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-674AK, AL, AT, and AU grades, which

Definitions of Specifications (Continued)

guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-674AJ and AS grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

UNIPOLAR OFFSET

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

BIPOLAR OFFSET

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1½LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{min} or T_{max}.

POWER SUPPLY REJECTION

The standard specifications for the HI-674A assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

LEFT-JUSTIFIED DATA

The data format used in the HI-674A is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

Applying the HI-674A

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout –

Unwanted, parasitic circuit components, (L, R, and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-674A (+15V, −15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections

The typical HI-674A ground currents are 6mADC into pin 9 (Analog Ground) and 3mADC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 3mA of DC current. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-674A's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device chosen to drive the HI-674A analog input will see a nominal load of 5KΩ (10V range) or 10KΩ (20V range). However, the other end of these input resistors may change ±400mV with each bit decision, creating abrupt changes in current at the analog input. Thus, the signal source must maintain its output voltage while furnishing these step changes in load current, which occur at 950 nS intervals. This requires low output impedance and fast settling by the signal source.

The output impedance of an op amp, for example, has an open loop value which, in a closed loop, is divided by the loop gain available at a frequency of interest. The amplifier should have acceptable loop gain at 1MHz for use with the HI-674A. To check whether the output properties of a signal source are suitable, monitor the 674A's input (pin 13 or 14) with an oscilloscope while a conversion is in progress. Each of the twelve disturbances should subside in one half microsecond or less. (The comparator decision is made about 850 nS after each code change from the SAR).

If the application calls for a Sample/Hold to precede the converter, it should be noted that not all Sample/Holds are compatible with the HI-674A in the manner described above. These will require an additional wideband buffer amplifier to lower their output impedance. A simpler solution is to use the Harris HA-5320 Sample/Hold, which was designed for use with the HI-674A.

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-674A is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in Figures 2 and 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-674A offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration –

Refer to Fig. 2. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem – the converter operates normally.

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is setting the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one

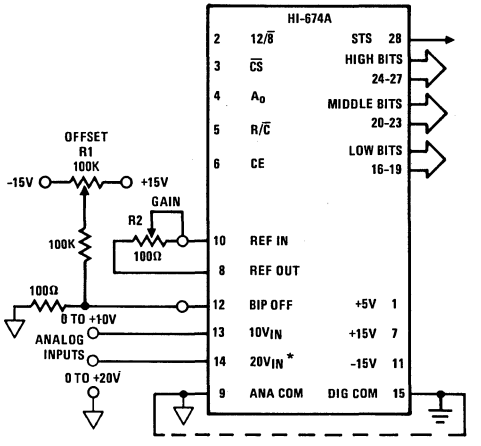


FIGURE 2. UNIPOLAR CONNECTIONS

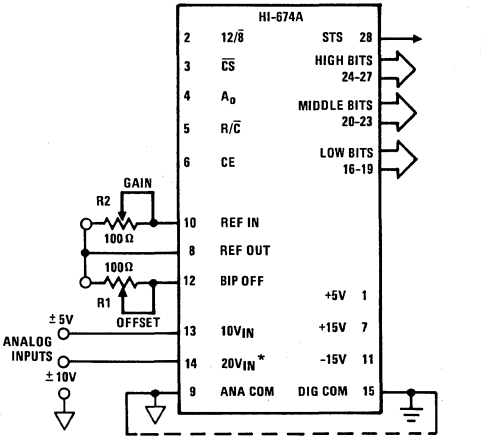


FIGURE 3 BIPOLAR INPUT CONNECTIONS

*When driving the 20V (pin 14) input, minimize capacitance on pin 13.

LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +1/2 LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is 1-1/2 LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration –

Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage 1/2 LSB above negative full scale (i.e., −4.9988V for the ±5V range, or −9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1-1/2 LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

* The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 500Ω potentiometer in series with pin 14.

CONTROLLING THE HI-674A

The HI-674A includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8 or 12 bit conversion cycle, initiating the conversion, and reading the output data when ready – choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS-compatible: (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 4.

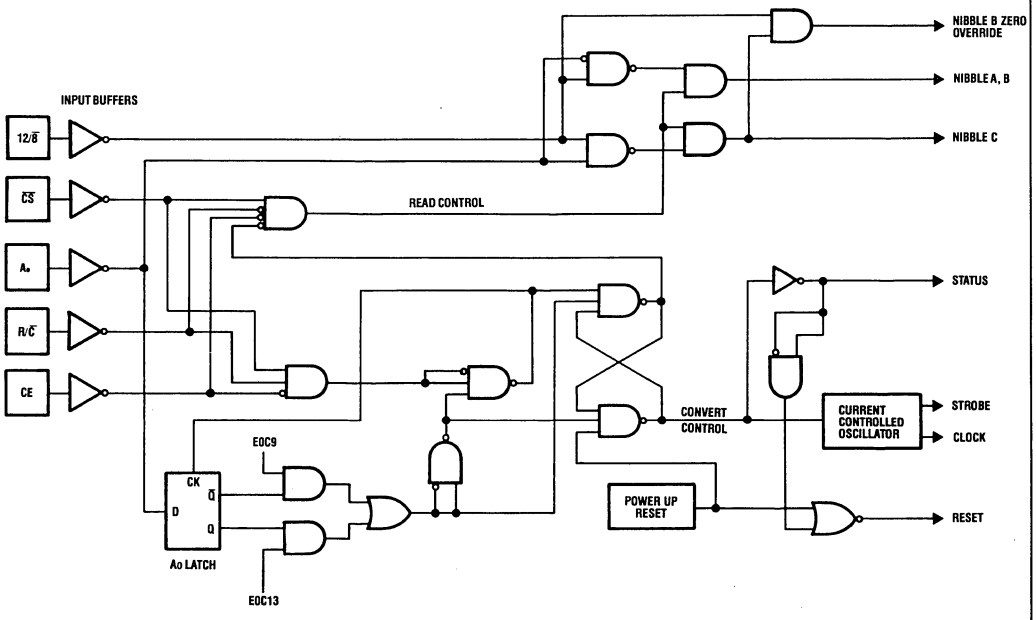


FIGURE 4. HI-674A CONTROL LOGIC

"Stand-Alone Operation"

The simplest control interface calls for a single control line connected to R/$\overline{C}$. Also, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and the output data appears in words of 12 bits each.

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 5 and 6. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed below under "Stand-Alone Mode Timing."

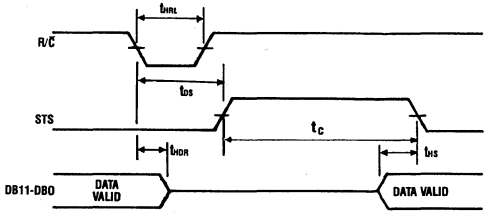


FIGURE 5. LOW PULSE FOR R/$\overline{C}$ – OUTPUTS ENABLED AFTER CONVERSION

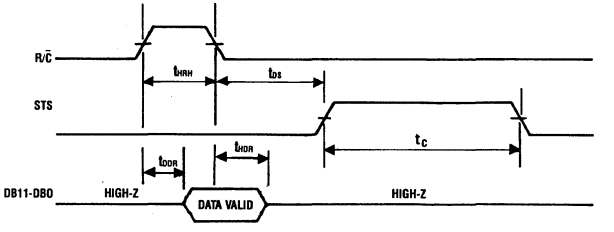


FIGURE 6. HIGH PULSE FOR R/$\overline{C}$ – OUTPUTS ENABLED WHILE R/C HIGH, OTHERWISE HIGH-Z

STAND-ALONE MODE TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
tHRL	Low R/C Pulse Width	50	-	-	ns
tDS	STS Delay From R/C	-	-	200	ns
tHDR	Data Valid After R/C Low	25	-	-	ns
tHS	STS Delay After Data Valid	25	-	850	ns
tHRH	High R/C Pulse Width	150	-	-	ns
tDDR	Data Access Time	-	-	150	ns

Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

Conversion Length

A Convert Start transition (see Table 1) latches the state of A_0, which determines whether the conversion continues for 12 bits (A_0 low) or stops with 8 bits (A_0 high). If all 12 bits are read following an 8 bit conversion, the three LSB's will read zero and DB3 will read ONE. A_0 is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

TABLE 1

Truth Table for HI-674A Control Inputs.

Conversion Start

A conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50nS earlier, however. See the HI-674A Timing Specifications, Convert mode.

This variety of HI-674A control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 7.

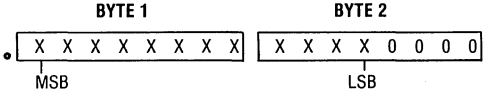
The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high. (However, if A_0 changes state after a conversion begins, an additional Start Convert signal will latch the new state of A_0, possibly causing a wrong cycle length (8 vs 12 bits) for that conversion).

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A_0. Timing constraints are illustrated in Figure 8.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS-compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16 bit data bus. The A_0 input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8 bit bytes, selected one at a time by A_0. This allows an 8 bit data bus to be connected as shown in Figure 9. A_0 is usually tied to the least significant bit of the address bus, for storing the HI-674A output in two consecutive memory locations. (With A_0 low, the 8 MSB's only are enabled. With A_0 high, 4 MSB's are disabled, bits 4 through 7 are forced to zero, and the 4 LSB's are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:



Further, A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 9 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than (t_{DD} + t_{HS}) before STS goes low. See Figure 8.

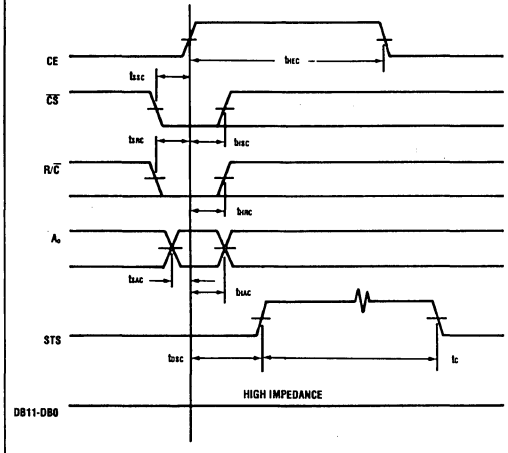


FIGURE 7. CONVERT START TIMING

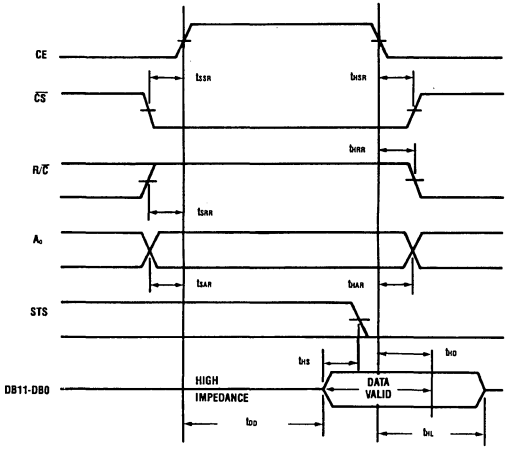


FIGURE 8. READ CYCLE TIMING

Timing Specifications +25°C Unless Otherwise Specified

Symbol	Parameter	Min	Typ	Max	Units
Convert Mode					
t_{DSC}	STS Delay from CE			200	nS
t_{HEC}	CE Pulse width	50			nS
t_{SSC}	$\overline{CS}$ to CE Setup	50			nS
t_{HSC}	$\overline{CS}$ Low during CE High	50			nS
t_{SRC}	R/$\overline{C}$ to CE Setup	50			nS
t_{HRC}	R/$\overline{C}$ Low during CE high	50			nS
t_{SAC}	A_0 to CE Setup	0			nS
t_{HAC}	A_0 Valid during CE high	50			nS
t_c	Conversion time, 12 bit cycle T min to T max	9	12	15	μS
	8 bit cycle T min to T max	6	8	10	μS
Read Mode					
t_{DD}	Access time from CE		75	150	nS
t_{HD}	Data Valid after CE low	25			nS
t_{HL}	Output float delay		100	150	nS
t_{SSR}	$\overline{CS}$ to CE setup	50			nS
t_{SRR}	R/$\overline{C}$ to CE setup	0			nS
t_{SAR}	A_0 to CE setup	50			nS
t_{HSR}	$\overline{CS}$ valid after CE low	0			nS
t_{HRR}	R/$\overline{C}$ high after CE low	0			nS
t_{HAR}	A_0 valid after CE low	50			nS
t_{HS}	STS delay after data valid	25		850	nS

NOTE: Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

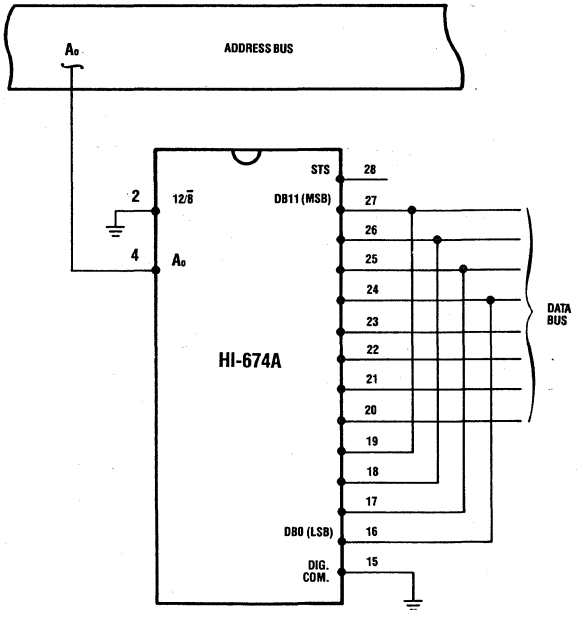


FIGURE 9. INTERFACE TO AN 8 BIT DATA BUS

Die Characteristics

Transistor Count	1117	Thermal Constants; θ_{ja}	48°C/W
Die Size; Analog	204 x 104 mils	θ_{jc}	15°C/W
Digital	158 x 84 mils	Process	Bipolar-DI
			CMOS-JI

HI-774

8μs, Complete 12-Bit A/D Converter With Microprocessor Interface

Features

- Complete 12 Bit A/D Converter With Reference and Clock
- Digital Error Correction
- Full 8-, 12-, or 16-Bit Microprocessor Bus Interface
- 150ns Bus Access Time
- No Missing Codes Over Temperature
- Minimal Setup Time For Control Signals
- 9μs Maximum Conversion Time Over Temperature
- Low Noise, Via Current-Mode Signal Transmission between Chips.
- Byte Enable/Short Cycle (A_0 Input)
  - ▸ Guarantees break-before-make action, eliminating bus contention during read operation. Latched by the Start Convert Input (To Set the Conversion Length)
- Faster Version of the HI-574A and HI-674A
- Same Pinout as HI-574A and HI-674A
- ±12V to ±15V Operation

Applications

- Industrial Data Acquisition Systems
- Electronics Test and Scientific Instrumentation
- Process Control Systems

Description

The HI-774 is a complete 12 bit Analog-to-Digital Converter, including a +10V reference clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28-pin package. The bipolar analog die features the Harris Dielectric Isolation process, whch provides enhanced AC performance and freedom from latch-up. The digital die features the Smart SAR (SSAR™), which includes a digital error correction circuit.

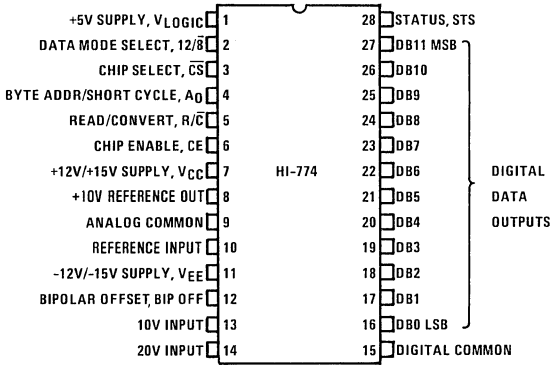
Custom design of each IC (bipolar and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current controlled for excellent stability over temperature.

The HI-774 offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The low noise buried zener reference circuit is trimmed for minimum temperature coefficient.

Power requirements are +5V and ±12V to ±15V, with typical dissipation of 390mW at ±12V. All models are packaged in a 28 pin Ceramic Sidebrazed DIP.

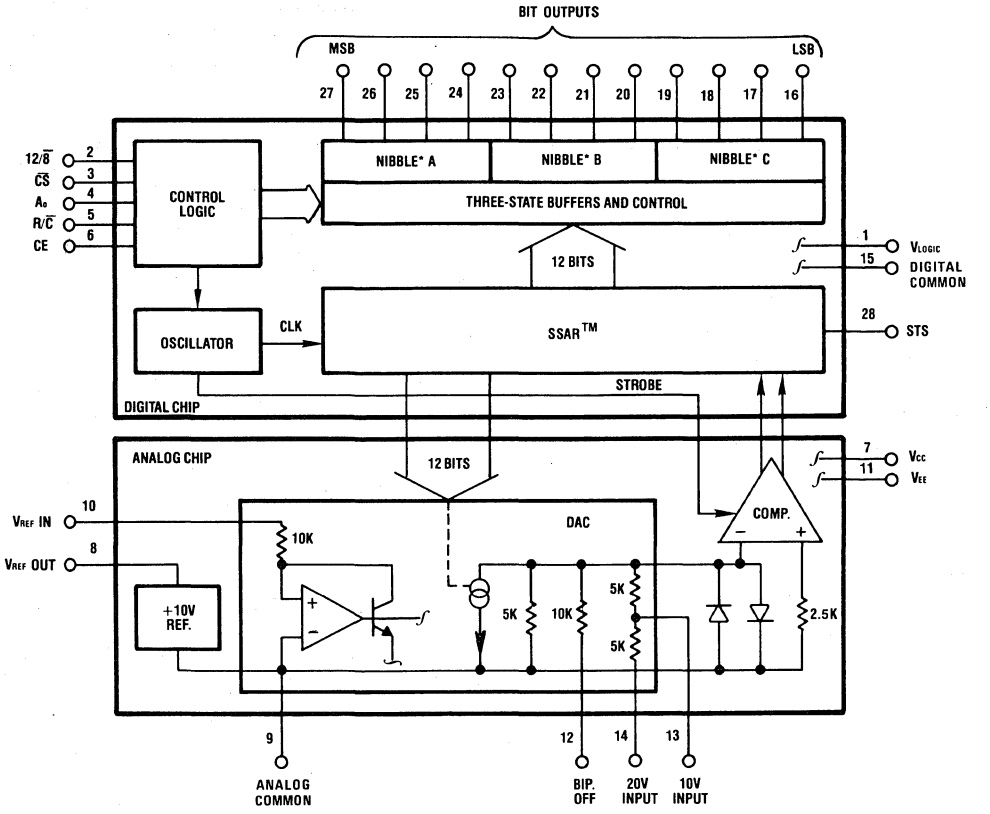
Pinout

SIDEBRAZE DIP
TOP VIEW



CAUTION: These devices are sensitive to electronic discharge. Proper I.C. handling procedures should be followed.

Block Diagram



*("NIBBLE" IS A 4 BIT DIGITAL WORD.)

Die Characteristics

Transistor Count 2117

Die Dimensions

Analog ..... 204 x 104 mils

Digital ..... 200 x 82 mils

Process ..... Bipolar-DI and CMOS-JI

Thermal Constants (°C/W)	θja	θjc
	47	14

Specifications HI-774

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC and Transfer Accuracy Specifications

MODEL	HI-774J	HI-774K	HI-774L	UNITS
Temperature Range	-5 (0°C to +75°C)			
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C(max)	±1	±1/2	±1/2	LSB
0°C to +75°C(max)	±1	±1/2	±1/2	LSB
(Maximum resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
Tmin to Tmax	11	12	12	Bits
Unipolar Offset (max)				
(Adjustable to zero)	±2	±1.5	±1	LSB
Bipolar Offset (max) V_{IN} = 0V (Adjustable to zero)	±4	±4	±3	LSB
V_{IN} = -10V	±0.15	±0.1	±0.1	% of F.S.
Full Scale Calibration Error				
25°C (max), with fixed 50 Ω resistor from REF OUT to REF IN (Adjustable to zero)	±0.25	±0.25	±0.15	% of F.S.
T_{min} to T_{max}				
(No adjustment at +25°C)	±0.475	±0.375	±0.20	% of F.S.
(With adjustment to zero at +25°C)	±0.22	±0.12	±0.05	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{min} to T_{max} (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
Bipolar Offset	±2	±2	±1	LSB
Full Scale Calibration	±9	±5	±2	LSB
Power Supply Rejection				
Max change in Full Scale Calibration				
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	±1	LSB
+4.5V<V_{LOGIC}<+5.5V	±1/2	±1/2	±1/2	LSB
−16.5V<V_{EE}<−13.5V or −12.6V<V_{EE}<−11.4V	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar		−5 to +5		Volts
		−10 to +10		Volts
Unipolar		0 to +10		Volts
		0 to +20		Volts
Input Impedance				
10 Volt Span		5K Ω, ± 25%		Ohms
20 Volt Span		10K Ω, ± 25%		Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}		+4.5 to +5.5		Volts
V_{CC}		+11.4 to +16.5		Volts
V_{EE}		−11.4 to −16.5		Volts
Operating Current				
I_{LOGIC}		7 TYP, 15 MAX		mA
I_{CC} +15V Supply		11 TYP, 15 MAX		mA
I_{EE} -15V Supply		21 TYP, 28 MAX		mA
Power Dissipation				
±15V, +15V		515 TYP, 720 MAX		mW
±12V, +5V		385 TYP		mW
Internal Reference Voltage, T_{min} to T_{max}		+10.00 ± 0.05 MAX		Volts
Output current available for external loads (External load should not change during conversion)		2.0 MAX		mA

Specifications HI-774

(Typical @ +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = −15V or −12V unless otherwise specified)

DC and Transfer Accuracy Specifications

MODEL	HI-774S	HI-774T	HI-774U	UNITS
Temperature Range	-2, -8 (55°C to +125°C)			
Resolution (max)	12	12	12	Bits
Linearity Error				
25°C(max)	±1	±1/2	±1/2	LSB
0°C to +75°C(max)	±1	±1	±1	LSB
				LSBs
(Maximum resolution for which no missing codes is guaranteed)				
25°C	11	12	12	Bits
Tmin to Tmax	11	12	12	Bits
Unipolar Offset (max)				
(Adjustable to zero)	±2	±2	±1	LSB
Bipolar Offset (max) V_{IN} = 0V (Adjustable to zero)	±4	±4	±3	LSB
V_{IN} = −10V	±0.15	±0.1	±0.1	% of F.S.
Full Scale Calibration Error				
25°C (max), with fixed 50 Ω resistor from REF OUT to REF IN (Adjustable to zero)	±0.25	±0.25	±0.15	% of F.S.
T_{min} to T_{max}				
(No adjustment at +25°C)	±0.75	±0.50	±0.275	% of F.S.
(With adjustment to zero at +25°C)	±0.50	±0.25	±0.125	% of F.S.
Temperature Coefficients				
Guaranteed max change, T_{min} to T_{max} (Using internal reference)				
Unipolar Offset	±2	±1	±1	LSB
Bipolar Offset	±2	±2	±1	LSB
Full Scale Calibration	±20	±10	±5	LSB
Power Supply Rejection				
Max change in Full Scale Calibration				
+13.5V<V_{CC}<+16.5V or +11.4V<V_{CC}<+12.6V	±2	±1	±1	LSB
+4.5V<V_{LOGIC}<+5.5V	±1/2	±1/2	±1/2	LSB
−16.5V<V_{EE}<−13.5V or −12.6V<V_{EE}<−11.4V	±2	±1	±1	LSB
Analog Inputs				
Input Ranges				
Bipolar	−5 to +5			Volts
	−10 to +10			Volts
Unipolar	0 to +10			Volts
	0 to +20			Volts
Input Impedance				
10 Volt Span	5K Ω, ± 25%			Ohms
20 Volt Span	10K Ω, ± 25%			Ohms
Power Supplies				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			Volts
V_{CC}	+11.4 to +16.5			Volts
V_{EE}	−11.4 to −16.5			Volts
Operating Current				
I_{LOGIC}	7 TYP, 15 MAX			mA
I_{CC} +15V Supply	11 TYP, 15 MAX			mA
I_{EE} -15V Supply	21 TYP, 28 MAX			mA
Power Dissipation				
±15V, +15V	515 TYP, 720 MAX			mW
±12V, +5V	385 TYP			mW
Internal Reference Voltage, T_{min} to T_{max}	+10.00 ± 0.05 MAX			Volts
Output current available for external loads (External load should not change during conversion)	2.0 MAX			mA

Digital Specifications (All Models, Over Full Temperature Range)

	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$)			
Logic "1"	+2.0V		+5.5V
Logic "0"	-0.5V		+0.8V
Current		0.1μA	+5μA
Capacitance		5pF	
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} — 1.6mA)			+0.4V
Logic "1" (I_{SOURCE} — 500μA)	+2.4V		
Logic "1" (I_{SOURCE} — 10μA)	+4.5V		
Leakage (High Z State, DB11-DB0 only)		±0.1μA	±5μA
Capacitance		5pF	

HI-774 Timing Specifications (+25°C Unless Otherwise Specified) Into a load with R_L = 3kΩ and C_L = 50pF

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
CONVERT MODE					
tDSC	STS Delay From CE	-	100	200	ns
tHEC	CE Pulse Width	50	30	-	ns
tSSC	CS to CE Setup	50	20	-	ns
tHSC	CS Low During CE High	50	20	-	ns
tSRC	R/C to CE Setup	50	0	-	ns
tHRC	R/C Low During CE High	50	20	-	ns
tSAC	A_0 to CE Setup	0	0	-	ns
tHAC	A_0 Valid During CE High	50	30	-	ns
t_c	Conversion time, 12 bit Cycle Tmin to Tmax (-5)	-	8.0	9	μs
	8 bit Cycle Tmin to Tmax (-5)	-	6.4	6.8	μs
	12 bit Cycle Tmin to Tmax (-2)	-	9	11	μs
	8 bit Cycle Tmin to Tmax (-2)	-	6.8	8.3	μs
READ MODE					
tDD	Access Time From CE	-	75	150	ns
tHD	Data Valid After CE Low	25	35	-	ns
tHL	Output Float Delay	-	70	150	ns
tSSR	CS to CE Setup	50	0	-	ns
tSRR	R/C to CE Setup	0	0	-	ns
tSAR	A_0 to CE Setup	50	25	-	ns
tHSR	CS Valid After CE Low	0	0	-	ns
tHRR	R/C High After CE Low	0	0	-	ns
tHAR	A_0 Valid After CE Low	50	25	-	ns
tHS	STS Delay After Data Valid	-	90	300	ns

NOTE: Time is measured from 50% level of digital transitions, except High Z output conditions which are measured at the 10% or 90% point.

Absolute Maximum Ratings (Specifications apply to all grades, except where noted)

V_{CC} to Digital Common ..... 0 to +16.5V
V_{EE} to Digital Common ..... 0 to -16.5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common ..... -0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, $10V_{IN}$) to Analog Common ..... ±16.5V
$20V_{IN}$ to Analog Common ..... ±24V
REF OUT ..... Indefinite short to common
Momentary short to V_{CC}
Junction Temperature ..... +175°C
Lead Temperature, Soldering ..... 300°C, 10 sec.
Storage Temperature ..... -65°C to +150°C

Definitions of Specifications

Linearity Error

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero occurs ½LSB (1.22mV for 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1½LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-774K and L, grades are guaranteed for maximum nonlinearity of ±½LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-774J grade is guaranteed to ±1LSB max error. For this grade, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

Differential Linearity Error (No Missing Codes)

A specification which guarantees no missing codes requires that every combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-774 K and L grades which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temerature ranges. The HI-774J grade guarantees no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

Unipolar Offset

The first transition should occur at a level ½LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

Bipolar Offset

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value ½LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

Full Scale Calibration Error

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1½LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

Temperature Coefficients

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25°C) value to the value at Tmin or Tmax.

Power Supply Rejection

The standard specifications for the HI-774 assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

Code Width

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10 volts for a 12-bit ADC.

Quantization Uncertainty

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±½LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

Left-Justified Data

The data format used in the HI-774 is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

Applying the HI-774

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

PHYSICAL MOUNTING AND LAYOUT CONSIDERATIONS

Layout—

Unwanted, parasitic circuit components, (L, R, and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vectorboard, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-774 (+15V, -15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSB's to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10μF tantalum type in parallel with a 0.1μF ceramic type is recommended.

Ground Connections

The typical HI-774 ground currents are 6mADC into pin 9 (Analog Common) and 3mADC out of pin 15 (Digital Common). These pins should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) 15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance since it will carry about 3mA of DC current. (Code dependent currents flow in the VCC, VEE and VLOGIC terminals, but not through the HI-774's Analog Common or Digital Common).

ANALOG SIGNAL SOURCE

The device driving the HI-774 analog input will see a nominal load of 5KΩ (10V range) or 10KΩ (20V range). However, the other end of these input resistors may change as much as $\pm$400mV with each bit decision. These input disturbances are caused by the internal DAC changing codes which causes a glitch on the summing junction. This creates abrupt changes in current at the analog input causing a "kick back" glitch from the input. Because the algorithm starts with the MSB, the first glitches will be the largest and get smaller as the conversion proceeds. These glitches can occur at 350ns intervals so an op-amp with a low output impedance and fast settling is desirable. Ultimately, the input must settle to within the window of figure 1 at the bit decision points in order to achieve 12 bit accuracy.

The HI-774 differs from the most high-speed successive approximation type ADC's in that it does not require a high performance buffer or sample and hold. With error correction the input can settle while the conversion is underway, but only during the first 4.8μs. The input must be within $\pm$0.76% of the final value when the MSB decision is made. This occurs approximately 650ns after the conversion has been initiated. Digital error correction also loosens the bandwidth requirements of the buffer or sample and hold. As long as the input "kick back" disturbances settle within the window of figure 1 the device will remain accurate. The combined effect of settling and the "kick back' disturbances must remain in the figure 1 window.

If the design is being optimized for speed, the input device should have a closed loop bandwidth to 3MHz, and a low output impedance (calculated by dividing the open loop output resistance by the open loop gain). If the application requires a high speed sample and hold the Harris HA-5330 or HA-5320 are recommended.

In any design the input (pin 13 or 14) should be checked during a conversion to make sure that the input stays within the correctable window of figure 1.

DIGITAL ERROR CORRECTION

The HI-774 features the smart sucessive approximation register (SSAR™) which includes digital error correction. This has the advantage of allowing the initial input to vary within a +31 to -32LSB window about the final value. The input can move during the first 4.8μs, after which it must remain stable within ±½LSB. With this feature a conversion can start before the input has settled completely; however, it must be within the window as described in Figure 1.

The conversion cycle starts by making the first 8-bit decisions very quickly, allowing the internal DAC to settle only to 8-bit accuracy. Then the converter goes through two error correction cycles. At this point the input must be stable within ±½LSB. These cycles correct the 8-bit word to 12-bit accuracy for any errors made (up to +16 or -32 bits). This is up one count or down two counts at 8-bit resolution. The converter then continues to make the 4LSB decisions, settling out to 12-bit accuracy. The last four bits can adjust the code in the positive direction by up to 15 bits. This results in a total correction range of +31 to -32 bits. When an 8-bit conversion is performed, the input must settle to within ±½LSB at 8 bit resolution (which equals ±8 bits at 12-bit resolution).

With the HI-774 a conversion can be initiated before the input has completely settled, as long as it meets the constraints of the Figure 1 window. This allows the user to start conversion up to 4.8μs earlier than with a typical analog to digital converter. A typical successive approximation type ADC must have a constant input during a conversion because once a bit decision is made it is locked in and cannot change.

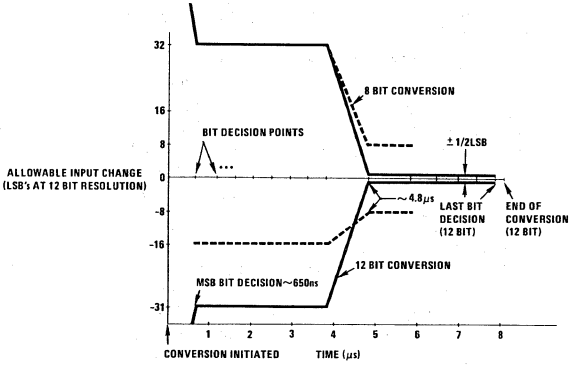


FIGURE 1. HI-774 ERROR CORRECTION WINDOW VS. TIME

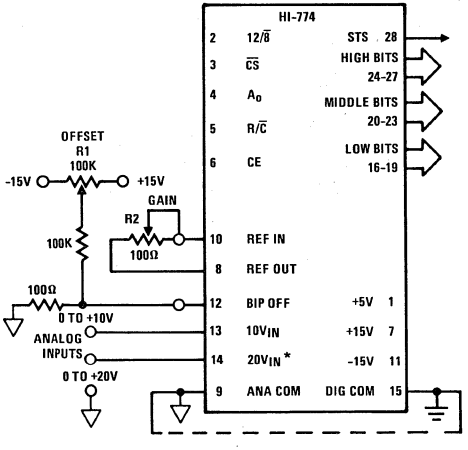


FIGURE 2. UNIPOLAR CONNECTIONS

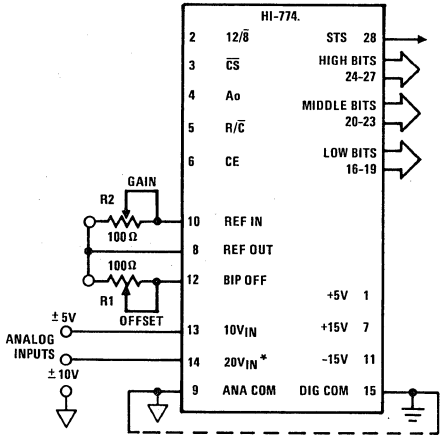


FIGURE 3. BIPOLAR INPUT CONNECTIONS

*When driving the 20V (pin 14) input, minimize capacitance on pin 13.

RANGE CONNECTIONS AND CALIBRATION PROCEDURES

The HI-774 is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in figures 2 and 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-774 offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration—

Refer to figure 2. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem—the converter operates normally.

Calibration consists in adjusting the converters's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is settling the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of +½LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is 1½LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration—

Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage ½LSB above negative full scale (i.e., -4.9988V for the ±5V range, or -9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1½LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

*The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48 range, add a 500Ω potentiometer in series with the pin 14.

Controlling the HI-774

The HI-774 includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8 or 12 bit conversion cycle, initiating the conversion, and reading the output data when ready—choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS- compatible: (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 4.

"Stand-Alone Operation"

The simplest control interface calls for a single control line connected to R/$\overline{C}$. Also, CE and 12/8 are wired high, $\overline{CS}$ and A_0 are wired low, and the output data appears in words of 12 bits each.

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 5 and 6. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed in the "Stand-Alone Mode Timing" chart.

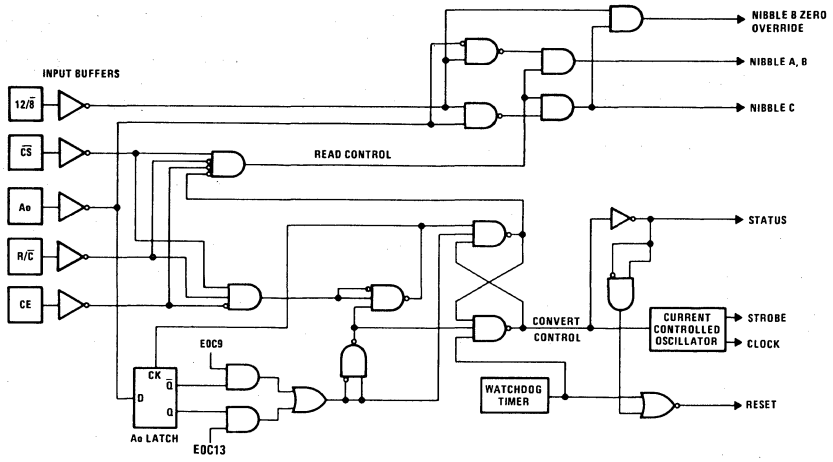


FIGURE 4. HI-774 CONTROL LOGIC

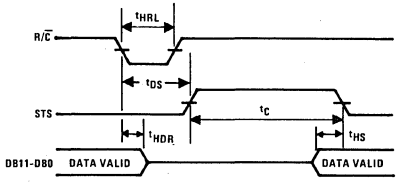


FIGURE 5. LOW PULSE FOR R/$\overline{C}$—OUTPUTS ENABLED AFTER CONVERSION

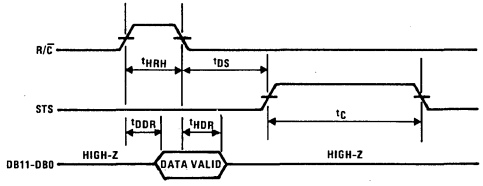


FIGURE 6. HIGH PULSE FOR R/$\overline{C}$—OUTPUTS ENABLE WHILE R/$\overline{C}$ HIGH, OTHERWISE HIGH-Z

Stand-Alone Mode Timing

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50			ns
t_{DS}	STS Delay from R/$\overline{C}$			200	ns
t_{HDR}	Data Valid After R/$\overline{C}$ Low	20			ns
t_{HS}	STS Delay After Data Valid		90	300	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150			ns
t_{DDR}	Data Access Time			150	ns

Conversion Length

A Convert Start transition (see Table 1) latches the state of A_0, which determines whether the conversion continues for 12 bits (A_0 low) or stops with 8 bits (A_0 high). If all 12 bits are read following an 8 bit conversion, the last three LSB's will read zero and DB3 will read ONE. A_0 is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

TABLE 1
TRUTH TABLE FOR HI-774 CONTROL INPUTS

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

Conversion Start

A conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50nS earlier, however. See the HI-774 Timing Specifications, Convert mode.

This variety of HI-774 control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 7.

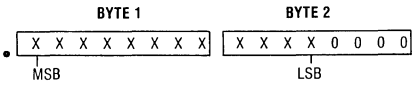
The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high.

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A_0. Timing constraints are illustrated in Figure 8.

The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS-compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12 or 16 bit data bus. The A_0 input is ignored.

With 12/8 low, the output is organized in two 8 bit bytes, selected one at a time by A_0. This allows an 8 bit data bus to be connected as shown in figure 9. A_0 is usually tied to the least significant bit of the address bus, for storing the HI-774 output in two consecutive memory locations. (With A_0 low, the 8 MSB's only are enabled. With A_0 high, 4 MSB's are disabled, bits 4 through 7 are forced low, and the 4 LSB's are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:



Further, A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 9 will never be enabled at the same time.

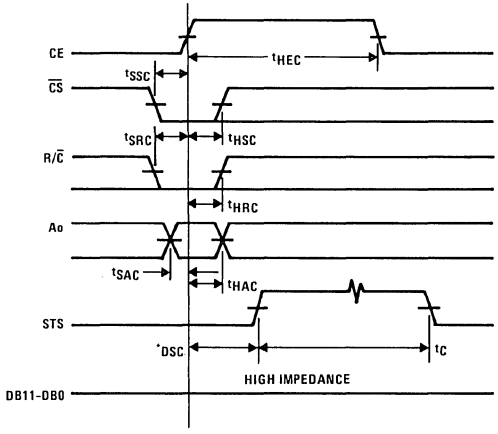


FIGURE 7. CONVERT START TIMING

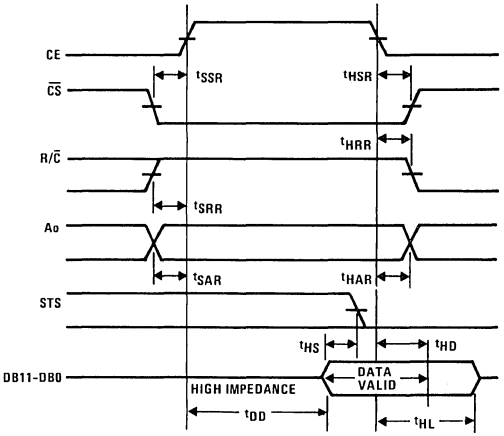


FIGURE 8. READ CYCLE TIMING

See HI-774 Timing Specifications for more information

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than ($t_{DD} + t_{HS}$) before STS goes low. See Figure 8.

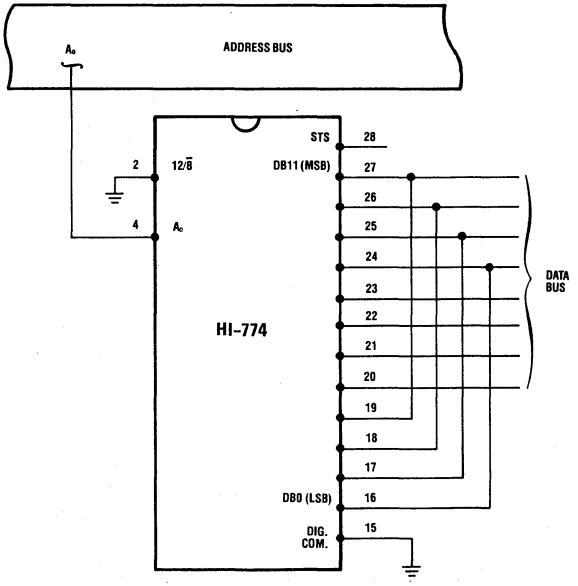


FIGURE 9. INTERFACE TO AN 8 BIT DATA BUS

Ordering Information

PART NUMBER	INL	TEMPERATURE RANGE	PACKAGE
HI1-774JD-5	±1 LSB	0°C to +75°C	28 Pin Ceramic DIP
HI1-774KD-5	±0.5 LSB	0°C to +75°C	28 Pin Ceramic DIP
HI1-774LD-5	±0.5 LSB	0°C to +75°C	28 Pin Ceramic DIP
HI1-774SD-2	±1 LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-774TD-2	±0.5 LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-774UD-2	±0.5 LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-774S/883	±1 LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-774T/883	±0.5 LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-774U/883	±0.5 LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI4-774S/883	±1 LSB	-55°C to +125°C	44 Pin Ceramic LCC
HI4-774T/883	±0.5 LSB	-55°C to +125°C	44 Pin Ceramic LCC
HI1-774U/883	±0.5 LSB	-55°C to +125°C	44 Pin Ceramic LCC

HARRIS SEMICONDUCTOR

HI-7151
10-Bit High Speed A/D Converter with Track & Hold

GENERAL DESCRIPTION

The Harris HI-7151 is a high speed 10-bit A/D converter which uses a Two Step Flash algorithm to achieve throughput rates of 100 kHz. A unique switched capacitor technique allows a new input voltage to be sampled while a conversion is taking place.

A Track and Hold amplifier is included on the chip, consisting of two high speed amplifiers and an internal hold capacitor.

Microprocessor bus interfacing is simplified by the use of standard Chip Select, Read, and Write control signals. The digital three-state outputs are byte organized for interfacing to either 8- or 16-bit systems. An Over-Range pin, together with the MSB, can be used to indicate an out-of-range condition.

The HI-7151 operates with ±5V supplies. A single +2.5V reference is required to provide a bipolar input range from −2.5V to +2.5V.

Internal high speed CMOS buffers at both the analog and reference inputs simplify external drive requirements.

ORDERING INFORMATION

Part Number	Linearity (Max. DLE)	Temperature Range	Package
HI3-7151J-5	±1 LSB	0°C to +75°C	28 Pin Plastic DIP
HI3-7151K-5	±1/2 LSB	0°C to +75°C	28 Pin Plastic DIP
HI3-7151A-9	±1 LSB	0°C to +85°C	28 Pin Plastic DIP
HI3-7151B-9	±1/2 LSB	0°C to +85°C	28 Pin Plastic DIP
HI1-7151S-2	±1 LSB	-55°C to +125°C	28 Pin Ceramic DIP
HI1-7151T-2	±1/2 LSB	-55°C to +125°C	28 Pin Ceramic DIP

FEATURES

- **10 μs Conversion Time**
- **100 kHz Continuous Throughput Rate**
- **No Offset or Gain Adjustments Necessary**
- **Internal Track and Hold Amplifier**
- **Analog and Reference Inputs Fully Buffered**
- **μP Compatible Byte Organized Outputs**
- **Low Power Consumption (150 mW)**
- **Uses a Single 2.5V Reference for ±2.5V Input Range**

APPLICATIONS

- **μP Controlled Data Acquisition Systems**
- **DSP**
  - **—Avionics**
  - **—Sonar**
- **Process Control**
  - **—Automotive Transducer Sensing**
  - **—Industrial**
- **Robotics**
- **Digital Communications**
- **Image Processing**

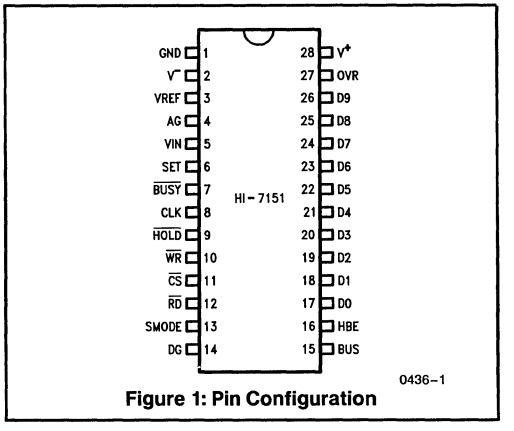


Figure 1: Pin Configuration

301673-002

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage
- V^+ to Gnd (DG/AG/GND) ..... $-0.3V < V^+ < +5.7V$
- V^- to Gnd (DG/AG/GND) ..... $-5.7V < V^- < +0.3V$

Analog Input Pins ..... $V^- - 0.3V < V_{INA} < V^+ + 0.3V$
Digital I/O Pins ..... $DG - 0.3V < V_{I/O} < V^+ + 0.3V$
Power Dissipation (Note 2) ..... <500 mW
- Derate above 75°C at −10 mW/°C

Operating Temperature Range
- HI3-7151X-5 ..... 0°C to +75°C
- HI3-7151X-9 ..... −40°C to +85°C

Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTE 1: Input voltages may exceed the supply voltage provided the input current is limited to ±1 mA.
2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

ELECTRICAL CHARACTERISTICS (Note 4)

ACCURACY $V^+ = +5V, V^- = -5V, V_{REF} = 2.50V$, fclk = 300 kHz, 50% duty cycle

Symbol	Parameter	Temperature (Note 3)	J, A Grade			K, B Grade			Units
			Min	Typ	Max	Min	Typ	Max	
RES	Resolution (Note 5) (With no missing codes)	$T_A = +25°C$	10			10			Bits
		$T_{MIN} \le T_A \le T_{MAX}$	10			10			Bits
ILE	Integral Linearity Error	$T_A = +25°C$		±0.5	±1.0		±0.3	±0.5	LSB
		$T_{MIN} \le T_A \le T_{MAX}$		±0.75	±1.0		±0.5	±0.75	LSB
DLE	Differential Linearity Error	$T_A = +25°C$			±1.0			±0.5	LSB
		$T_{MIN} \le T_A \le T_{MAX}$			±1.0			±0.75	LSB
V_{OS}	Bipolar Offset Error	$T_A = +25°C$		±1.0	±2.5		±0.6	±1.5	LSB
		$T_{MIN} \le T_A \le T_{MAX}$		±1.5	±3.0		±1.0	±2.0	LSB
eG+ & eG−	Unadjusted Gain Error	$T_A = +25°C$		±1.0	±2.5		±0.6	±1.5	LSB
		$T_{MIN} \le T_A \le T_{MAX}$		±1.5	±3.0		±1.0	±2.0	LSB

NOTE 3: T_{MIN} to T_{MAX}: See Ordering Information Table.

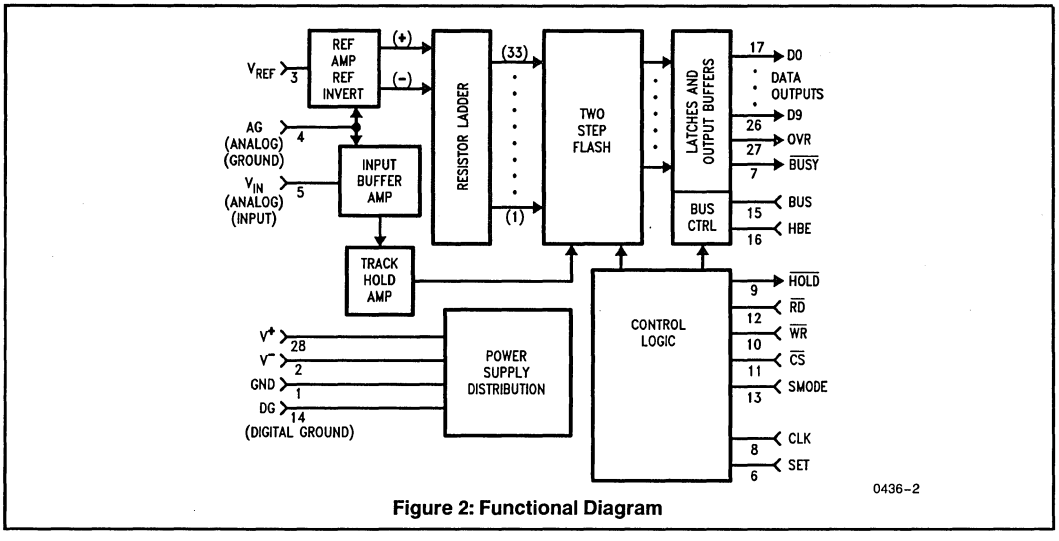


Figure 2: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued)

DC CHARACTERISTICS

$V^+ = 5V$, $V^- = -5V$, $V_{REF} = 2.50V$, $T_A = +25°C$, fclk = 300 kHz, 50% duty cycle, unless stated otherwise.

Symbol	Parameter	Conditions (Note 4)	+25°C			0°C to +75°C		−40°C to +85°C		Units	Note
			Min	Typ	Max	Min	Max	Min	Max		
ANALOG INPUT											
VIR	Analog Input Range		$-V_{REF}$		$+V_{REF}$	$-V_{REF}$	$+V_{REF}$	$-V_{REF}$	$+V_{REF}$	V	
IBI	Analog Input Bias Current	V_{IN} = 0V		0.01	100		100		100	nA	
CV_{IN}	Analog Input Capacitance			8	20					pF	5
REFERENCE INPUT											
VRR	Reference Input Range		2.2	2.5	2.6	2.2	2.6	2.2	2.6	V	6
IBR	Reference Input Bias Current	V_{REF} = 2.50V		0.01	100		100		100	nA	
CVr	Reference Input Capacitance			7	20					pF	5
TRACK AND HOLD (See text)											
SR	Slew Rate			9						V/μs	
BW	Bandwidth			1.5						MHz	
	Aperture Time			30						ns	
	Aperture Uncertainty			2						ns	
	Feedthrough in HOLD	F_{IN} = 100 kHz		−80						dB	
	Acquisition Time			1.5						μs	
LOGIC INPUTS											
V_{IH}	Input High Voltage		2.0			2.0		2.0		V	
V_{IL}	Input Low Voltage				0.8		0.8		0.8	V	
I_{IL}	Logic Input Current	V_{IN} = 0V, V^+		0.05	1		1		1	μA	
C_{IN}	Input Capacitance			5	17					pF	5
LOGIC OUTPUTS											
V_{OH}	Output High Voltage	I_{OH} = −200 μA	2.4			2.4		2.4		V	
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA			0.4		0.4		0.4	V	
I_{OL}	Output Leakage Current	$\overline{RD}$ = V^+, V_{OUT} = V^+		0.04	1		10		10	μA	
		$\overline{RD}$ = V^+, V_{OUT} = 0V	−1	−0.01		−10		−10		μA	
C_{OUT}	Output Capacitance	High-Z State		7	15					pF	5
POWER SUPPLY VOLTAGE RANGE											
V^+		Functional Operation	4.5	5.0	5.5	4.5	5.5	4.5	5.5	V	7
V^-		Only	−4.5	−5.0	−5.5	−4.5	−5.5	−4.5	−5.5	V	7
POWER SUPPLY REJECTION											
eGVS	V^+, V^- Gain Coefficient	V^+ = 5V, V^- = −4.75V, −5.25V		±0.1	±0.5		±0.6		±0.6	LSB	
		V^- = −5V, V^+ = 4.75V, 5.25V		±0.1	±0.5		±0.6		±0.6		
VOSVS	V^+, V^- Offset Coefficient	V^+ = 5V, V^- = −4.75V, −5.25V		±0.1	±0.5		±0.6		±0.6	LSB	
		V^- = −5V, V^+ = 4.75V, 5.25V		±0.1	±0.5		±0.6		±0.6		
SUPPLY CURRENTS											
I^+	V^+ Supply Current	V^+ = 5V ±10%, V^- = −5V ±10%		20	30		30		30	mA	
I^-	V^- Supply Current	V_{IN} = 0V, Digital		−10	−15		−15		−15	mA	
IGND	GND Current	Outputs are Unloaded		−8	−15		−15		−15	mA	
IDG	DG Current			−2	−3		−3		−3	mA	
IAG	AG Current			0.02	10		10		10	μA	

NOTE 4: FSR (Full Scale Range) = 2 × V_{REF} (5.00V at V_{REF} = 2.50V). LSB (Least Significant Bit) = FSR/1024 (4.88 mV at V_{REF} = 2.50V).
5: Parameter not tested. Parameter guaranteed by design, simulation, or characterization.
6: Only V_{OS} and GAIN ERROR functionality tested at 2.2V and 2.6V.
7: Guaranteed by functionality test.

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued)

AC CHARACTERISTICS

$V^+ = 5V \pm 10\%$, $V^- = -5V \pm 10\%$, $V_{REF} = 2.50V$, $T_A = +25°C$, fclk = 300 kHz, 50% duty cycle, $C_L = 100$ pF (including stray for D0–D9, OVR, $\overline{HOLD}$, $\overline{BUSY}$), unless stated otherwise

Symbol	Parameter	Conditions (Note 11)	+25°C			0°C to +75°C		−40°C to +85°C		Units	Notes
			Min	Typ	Max	Min	Max	Min	Max		
D	Clock Input Duty Cycle		45	50	55	45	55	45	55	%	5
tsps	Continuous Conversion Time		60		3tck 10	60	3tck 10	60	3tck 10	µs µs	9 9
tconv	Slow Memory Mode Conversion Time				4tck + 0.9		4tck + 0.9		4tck + 0.9	µs	5, 8
tcyc	Continuous Throughput				fclk/3		fclk/3		fclk/3/3	sps	9
tck	CLOCK Period			1/fclk							
tckhr	CLOCK to $\overline{HOLD}$ Rise Delay		150	290	500	140	525	120	525	ns	5
twrl	$\overline{WR}$ Pulse Width		200	113	tck/2	225	tck/2	225	tck/2	ns	5, 8, 10
thold	$\overline{WR}$ to $\overline{HOLD}$ Delay			80	170		200		200	ns	5,8
tbd	$\overline{BUSY}$ to DATA			40	200		230		230	ns	5, 8
twrd	$\overline{WR}$ to $\overline{RD}$ Active		100			100		100		ns	5, 8
tckhf	CLOCK to $\overline{HOLD}$ Fall Delay		50	125	250	40	275	25	275	ns	5, 9
tdata	$\overline{HOLD}$ to DATA change		100	200	400	90	550	70	550	ns	5, 9
trd	$\overline{RD}$ LO to Active			75	150		190		190	ns	5, 13
trx	$\overline{RD}$ HI to Inactive			25	60		80		80	ns	5, 14
tad	HBE to DATA			70	150		165		165	ns	5
tcd	$\overline{CS}$ to DATA			95	180		210		210	ns	5
tbusy	$\overline{RD}$ to $\overline{BUSY}$			35	200		200		200	ns	5
tr	Rise Time			50	100		125		125	ns	5, 12
tf	Fall Time			45	100		120		120	ns	5, 12

NOTE 8: Slow memory mode timing.

9: Fast memory or DMA mode of operation, except the first conversion which is equal to tconv.

10: Maximum specification to prevent multiple triggering with $\overline{WR}$.

11: All input drive signals are specified with tr = tf ≤ 20 ns and shall swing from V_{IL} −0.4V to V_{IH} +0.4V for all timing specifications. A signal is considered to change state as it crosses a 1.4V threshold (except trd & trx).

12: tr and tf load is C_L = 100 pF (including stray capacitance) to DG and is measured from the 10–90% point.

13: trd is the time required for the data output level to change by 10% in response to $\overline{RD}$ crossing a voltage level of 1.4V. High-Z to V_{OH} is measured with R_L = 2.5 kΩ and C_L = 100 pF (including stray) to DG. High-Z to V_{OL} is measured with R_L = 2.5 kΩ to V^+ and C_L = 100 pF (including stray) to DG.

14: trx is the time required for the data output level to change by 10% in response to $\overline{RD}$ crossing a voltage level of 1.4V. V_{OH} to High-Z is measured with R_L = 2.5 kΩ and C_L = 10 pF (including stray) to DG. V_{OL} to High-Z is measured with R_L = 2.5 kΩ to V^+ and C_L = 10 pF (including stray) to DG.

NOTE: All typical values have been characterized but are not tested.

TIMING DIAGRAMS

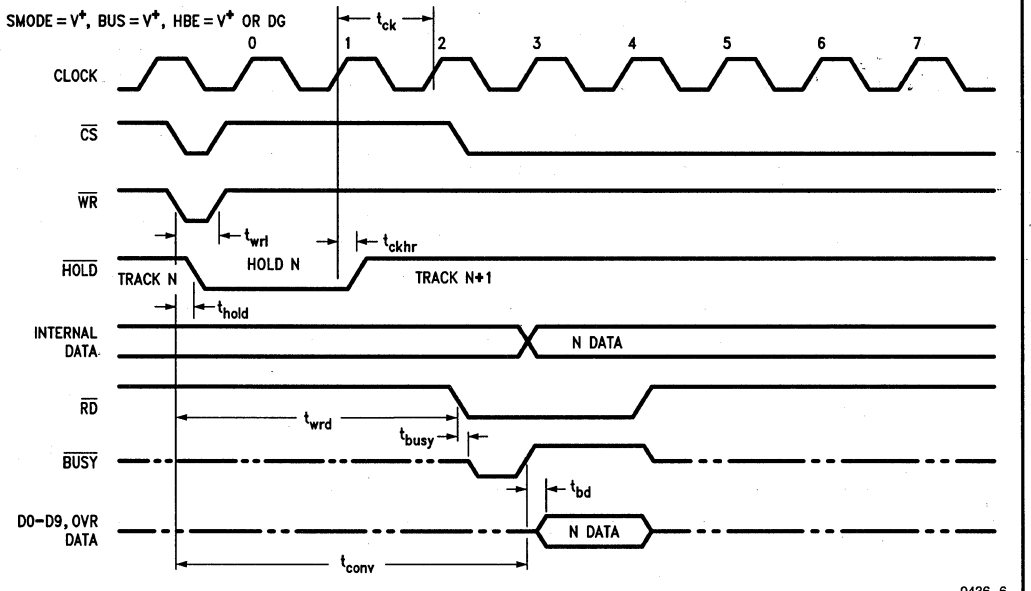


Figure 3A: Slow Memory Mode (16-Bit Data Bus)

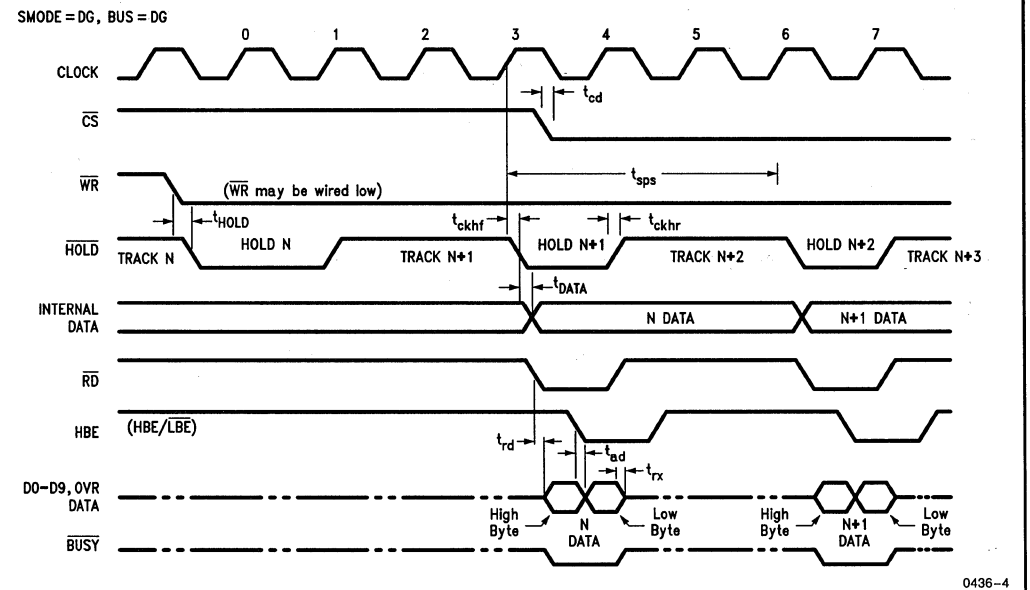


Figure 3B: Fast Memory Mode (8-Bit Data Bus)

Note: With SMODE = DG, internal logic disables the output latches form being updated during a READ operation.

NOTE: All typical values have been characterized but are not tested.

TIMING DIAGRAMS (Continued)

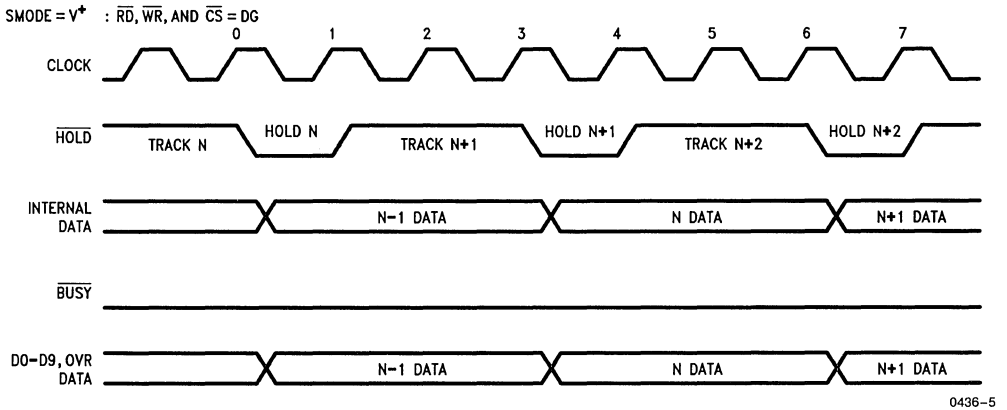


Figure 3C: DMA Mode

NOTE: All typical values have been characterized but are not tested.

Table 1: Pin Description

Pin	Name	Description
1	GND	Ground return for comparators (0V)
2	V^-	Negative supply voltage input (−5.0V)
3	V_{REF}	Reference voltage input (+2.50V)
4	AG	Analog ground reference (0V)
5	V_{IN}	Analog input voltage
6	SET	Connect to V^+ for proper operation.
7	$\overline{BUSY}$	Output High—Conversion complete Output Low—Conversion in progress. Output floats when chip is not selected ($\overline{RD}$ and $\overline{CS}$ both high).
8	CLK	Clock input
9	$\overline{HOLD}$	Indicates start of conversion. Active low.
10	$\overline{WR}$	Write input. With $\overline{CS}$ low, starts conversion when pulsed low; continuous conversions when kept low.
11	$\overline{CS}$	Chip select input. Active low.
12	$\overline{RD}$	Read input. With $\overline{CS}$ low, enables output buffers when pulsed low; outputs updated at end of conversion when kept low.
13	SMODE	Slow memory mode input. Active high.
14	DG	Digital ground (0V)
15	BUS	Bus select input High = all outputs enabled together D0–D9, OVR Low = outputs enabled by HBE
16	HBE	Byte select (HBE/LBE) input for 8-bit bus. Input high—High byte select, D8–D9, OVR Input low—Low byte select, D0–D7
17	D0	Bit 0 (Least significant, LSB) — Output Data Bits (High = True) — Low Byte
18	D1	Bit 1 — Low Byte
19	D2	Bit 2 — Low Byte
20	D3	Bit 3 — Low Byte
21	D4	Bit 4 — Low Byte
22	D5	Bit 5 — Low Byte
23	D6	Bit 6 — Low Byte
24	D7	Bit 7 — Low Byte
25	D8	Bit 8 (Most significant) — High Byte
26	D9	Bit 9 (Sign) — High Byte
27	OVR	Out of Range flag. Valid at end of conversion when output exceeds full-scale. — High Byte
28	V^+	Positive supply voltage input (+5.0V)

DETAILED DESCRIPTION

The HI-7151 is a high speed 10-bit A/D converter which achieves throughput rates of 100 kHz by use of a Two Step Flash algorithm. A pipelined operation has been achieved through the use of switched capacitor techniques which allow the device to sample a new input voltage while a conversion is taking place. The HI-7151 requires a single reference input of +2.5V, which is internally inverted to −2.5V, thereby allowing an input range of −2.5V to +2.5V. 10 bits including sign are two's complement coded. The analog and reference inputs are internally buffered by high speed CMOS buffers, which greatly simplifies the external analog drive requirements for the device.

NOTE: All typical values have been characterized but are not tested.

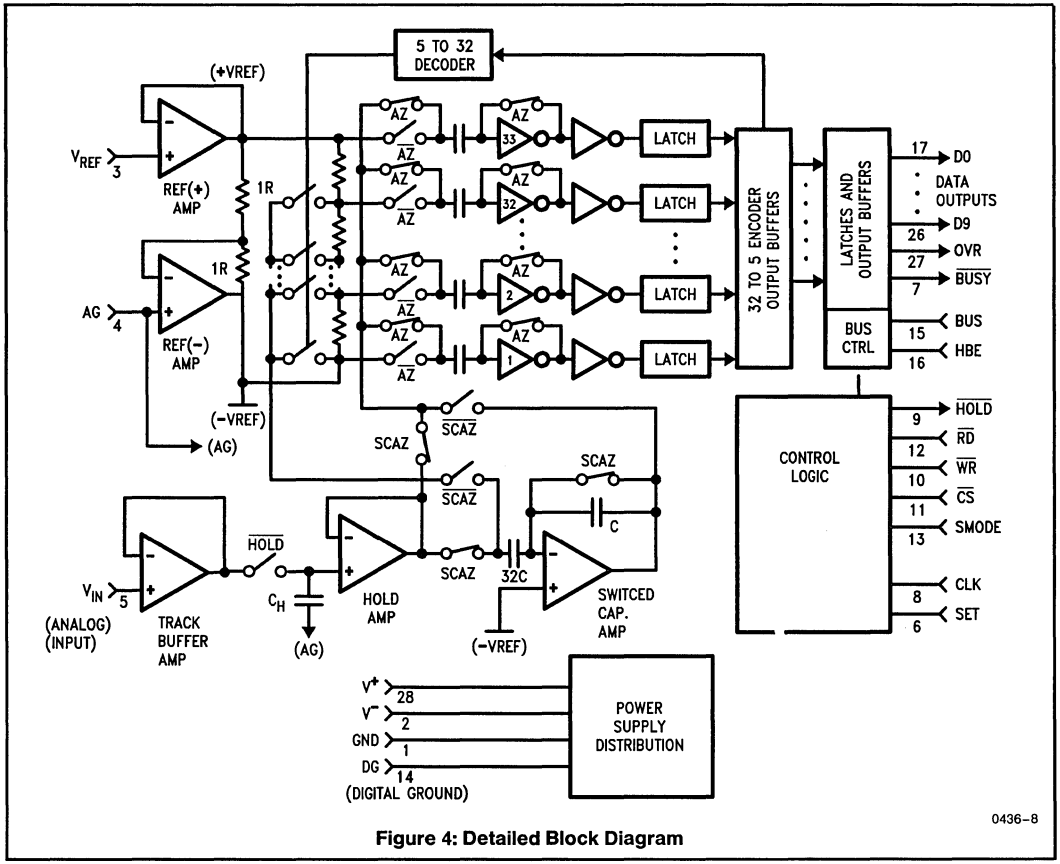


Figure 4: Detailed Block Diagram

A/D SECTION

The HI-7151 uses a conversion algorithm which is generally called a "Two Step Flash" algorithm. This algorithm enables very fast conversion rates without the penalty of high power dissipation or high cost. A detailed functional diagram is presented in Figure 4.

The input voltage is first converted into a 5-bit result (plus Out of Range information) by the flash converter. This flash converter consists of an array of 33 auto-zeroed comparators which perform a comparison between the input voltage and subdivisions of the reference voltage. These subdivisions of the reference voltage are formed by forcing the reference voltage and its negative on the two ends of a string of 32 resistors.

The reference input to the HI-7151 is buffered by a high speed CMOS amplifier which is used to drive one end of the resistor string. Another high speed amplifier configured in the inverting unity gain mode inverts the reference voltage with respect to analog ground and forces it onto the other end of the resistor string. Both reference amplifiers are offset trimmed at the factory in order to increase the accuracy of the HI-7151 and to simplify its usage.

The 5-bit result of the first flash conversion is latched into the upper five bits of double buffered latches. It is also converted back into an analog signal by choosing the ladder voltage which is closest to but less than the input voltage. The selected voltage (VTAP) is then subtracted from the input voltage. This residue is amplified by a factor of 32 and referenced to the negative reference voltage ($VSCA = (V_{IN} - VTAP) \times 32 + V_{REF}^-$). This subtraction and amplification operation is peformed by a Switched Capacitor Amplifier (SCA). The output of the SCA falls between the positive and negative reference voltages and can therefore be digitized by the original 5-bit flash converter (second flash conversion).

NOTE: All typical values have been characterized but are not tested.

HI-7151

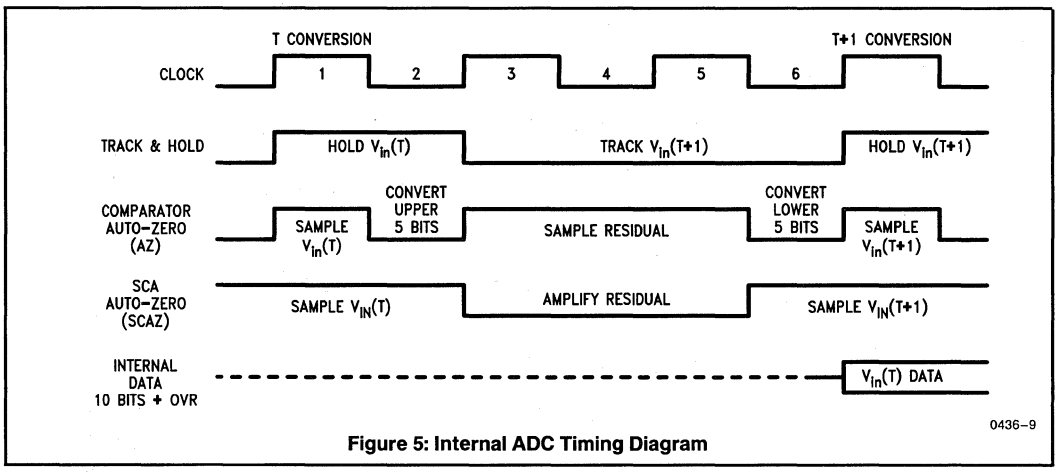


Figure 5: Internal ADC Timing Diagram

The 5-bit result of the second flash conversion is latched into the lower five bits of double buffered latches. At the end of a conversion, 10 bits of data plus an Out of Range bit are latched into the second level of latches and can then be put on the digital output pins.

The conversion takes place in three clock cycles and is illustrated in Figure 5. When the conversion begins, the track and hold goes into its hold mode for 1 clock cycle. During the first half clock cycle the comparator array is in its auto-zero mode and it samples the input voltage. During the second half clock cycle, the comparators make a comparison between the input voltage and the ladder voltages. At the beginning of the third half clock cycle, the first most significant 5-bit result becomes available. During the first clock cycle, the SCA was sampling the input voltage. After the first flash result becomes available and a ladder tap voltage has been selected the SCA amplifies the residue between the input and ladder tap voltages. During the next three half clock cycles, while the SCA output is settling to its required accuracy, the comparators go into their auto-zero mode and sample this voltage. During the sixth half clock cycle, the comparators perform another comparison whose 5-bit result becomes available on the next clock edge.

TRACK AND HOLD ANALOG INPUT

A Track and Hold amplifier has been fully integrated on the front end of the A/D converter. Because of the sampling nature of this A/D converter, the input is required to stay constant only during the first clock cycle. Therefore, the Track and Hold (T/H) amplifier "holds" the input voltage only during the first clock cycle and it acquires the input voltage for the next conversion during the remaining two clock cycles. The high input impedance of the T/H input amplifier simplifies analog interfacing. Input signals up to $\pm V_{REF}$ can be directly connected to the A/D without buffering. The A/D output code table is shown in Table 2.

Table 2: A/D Output Code Table

Analog Input		Output Data										
LSB = 2 (V_{REF})/1024	V_{REF} = 2.500V	OVR	SIGN 9	MSB 8	7	6	5	4	3	2	1	LSB 0
≥ +V_{REF}	2.500V to V+ (+OVR)	1	0	0	0	0	0	0	0	0	0	0
+V_{REF} − 1LSB	2.49512V (+FULL SCALE)	0	0	1	1	1	1	1	1	1	1	1
+1LSB	0.00488V	0	0	0	0	0	0	0	0	0	0	1
0	0.000V	0	0	0	0	0	0	0	0	0	0	0
−1LSB	−0.00488V	0	1	1	1	1	1	1	1	1	1	1
−V_{REF}	−2.500V (−FULL SCALE)	0	1	0	0	0	0	0	0	0	0	0
≤ −V_{REF} − 1LSB	−2.50488V to V− (−OVR)	1	1	0	0	0	0	0	0	0	0	0

NOTE: All typical values have been characterized but are not tested.

The timing signals for the Track and Hold amplifier are generated internally, and are also provided externally ($\overline{HOLD}$) for synchronization purposes. The T/H amplifier consists of two high speed CMOS amplifiers and an internal hold capacitor. Its typical slew rate and bandwidth are 9V/μs and 1.5 MHz respectively. It is configured to give a very small hold pedestal without the use of an external hold capacitor. The hold pedestal is typically less than 100 μV.

Acquisition of the analog input signal is the time required by the T/H for its output to reach its final value within a specified error band. This time is a function of the logic delay time, op amp slewing time, and settling time. The T/H is in the track mode for 2 clock cycles (6.7 μs @ CLK = 300 kHz) but the output typically settles to within 1/4 LSB in 1.5 μs.

Aperture delay time is the time required for the T/H switch to open following the internal hold command. This is the delay with respect to falling edge of $\overline{WR}$ and the internal hold command. It is equal to Thold (typ) − 50 ns (typ) which is typically 30 ns.

Aperture uncertainty (jitter) is a range of variation in the aperture time. The greater the aperture time the larger the uncertainty in the analog voltage being converted. If the aperture time is nulled out by advancing the hold command ($\overline{WR}$) or the signal is repetitively sampled, aperture uncertainty becomes the major source of time error. The aperture uncertainty for the T/H is typically 2 ns which sets the maximum input bandwidth to 77.7 kHz for 1 LSB resolution.

$$fmax = 1/(2\pi \times 2^n \times ta)$$

where n = resolution in bits

ta = aperture uncertainty

All of the internal amplifiers are offset trimmed at the factory to give improved accuracy and to minimize the number of external components. If necessary, offset error can be adjusted either at an external interface buffer or by using digital post correction.

REFERENCE INPUT

The reference input to the HI-7151 is buffered by a high speed CMOS amplifier. The reference input range is 2.2V to 2.6V.

POWER REQUIREMENTS

Power to the chip should be applied in the following order: V^-, V^+, and V_{REF}. In applications where V^+ is supplied prior to V^-, the positive supply current will be approximately 2 times its nominal value until V^- is applied (this is not a latchup condition).

INITIALIZATION

In fast memory and DMA modes (after proper power, V_{REF}, and clock) up to 6 clock cycles are required for circuit initialization. After circuit initialization, valid data will be available in 3 clock cycles.

MICROPROCESSOR INTERFACE

The HI-7151 can be interfaced to microprocessors through the use of standard Write, Read, Chip Select, and HBE control pins. The digital outputs are two's complement coded, three-state gated, and byte organized for bus interface with 8- and 16-bit systems. The digital outputs (D0–D9, OVR, and $\overline{BUSY}$) may be accessed under control of BUS, byte enable input HBE, chip select, and read inputs for a simple parallel bus interface. The microprocessor can read the current data in the output latches in typically 75 ns/byte (trd). An over range pin (OVR) together with the MSB (D9) pin set to either a logic 0 or 1 will indicate a positive or negative over-range condition respectively. All digital output buffers are capable of driving one TTL load.

The HI-7151 can be interfaced to a microprocessor using one of three modes: slow memory, fast memory, and DMA mode.

SLOW MEMORY MODE

In slow memory mode, the conversion will be initiated by the microprocessor by selecting the chip ($\overline{CS}$) and pulsing $\overline{WR}$ low. This mode is selected by hardwiring the SMODE pin to V^+. This mode is intended for use with microprocessors (such as the 8086) which can be forced into a WAIT state. For example, in a configuration where the $\overline{BUSY}$ output is tied to the 8086 READY input, an attempt to read the data before the conversion is complete will force the processor into a WAIT state until $\overline{BUSY}$ goes high, at which time the data at the output is valid. This resembles a 10 μs access time RAM. It allows the processor to initiate a conversion, WAIT, and READ data with a single READ instruction. When the 8-bit bus operation is selected, high and low byte data may be accessed in either order. An I/O truth table is presented in Table 3 for the slow memory mode of operation.

NOTE: All typical values have been characterized but are not tested.

Table 3: Slow Memory Mode I/O Truth Table (SMODE = V+)

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	BUS	HBE	Function
0	0	X	X	X	Initiates a conversion
1	X	X	X	X	Disables all chip commands
0	X	0	1	X	D0–D9 & OVR enabled
0	X	0	0	0	Low byte enabled: D0–D7
0	X	0	0	1	High byte enabled: D8–D9, OVR
X	X	1	X	X	Disables all outputs (High impedance)

X = don't care

FAST MEMORY MODE

The fast memory mode of operation is selected by tying the SMODE and $\overline{WR}$ pins to DG. In this mode, the chip performs continuous conversions and only $\overline{CS}$ and $\overline{RD}$ are required to read the data. Whenever the SMODE pin is low, $\overline{WR}$ is independent of $\overline{CS}$ in starting a conversion cycle. During the first conversion cycle, $\overline{HOLD}$ follows $\overline{WR}$ going low.

Data can be read a byte at a time or all 11 bits at once. The internal logic disables the output latches from being updated during a read after the high byte data is accessed. It will continue to be disabled until after the low byte data is accessed. THEREFORE, WHEN 8-BIT BUS OPERATION IS SELECTED, THE DATA MUST BE ACCESSED HIGH BYTE FIRST, LOW BYTE NEXT. If the low byte is accessed first followed by high byte, the results from the next conversion cycle will be lost because the updating of the output latch is disabled. $\overline{BUSY}$ is continuously low when accessed with a read command in this mode. An I/O truth table is presented in Table 4 for the fast memory mode of operation.

The data can be defined in time by monitoring the $\overline{HOLD}$ pin. The conversion data can be read after $\overline{HOLD}$ has gone low.

Table 4: Fast Memory Mode I/O Truth Table (SMODE = DG)

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	BUS	HBE	Function
X	0	X	X	X	Continuous conversion, $\overline{WR}$ may be tied to DG
1	X	X	X	X	Disables only the $\overline{RD}$ command
0	X	0	1	X	D0–D9 & OVR enabled
0	X	0	0	1	High byte enabled: D8–D9, OVR (enable 1st)
0	X	0	0	0	Low byte enabled: D0–D7 (must enable 2nd)
X	X	1	X	X	Disables all outputs (High impedance)

X = don't care

DMA MODE

This mode is a complete hardwire mode where the HI-7151 continuously converts. The user implements hardware to store the results in memory, bypassing the microprocessor. This mode is recognized by the chip when SMODE is hardwired to V+ and $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ are hardwired to DG. When 8-bit bus operation is selected, high and low byte data may be accessed in either order. $\overline{BUSY}$ is continuously low when accessed with a read command in this mode. An I/O truth table is presented in Table 5 for the DMA mode of operation.

Table 5: DMA Mode I/O Truth Table (SMODE = V+, $\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = DG)

BUS	HBE	Function
1	X	D0–D9 & OVR enabled
0	0	Low byte enabled: D0–D7
0	1	High byte enabled: D8–D9, OVR

X = don't care

NOTE: All typical values have been characterized but are not tested.

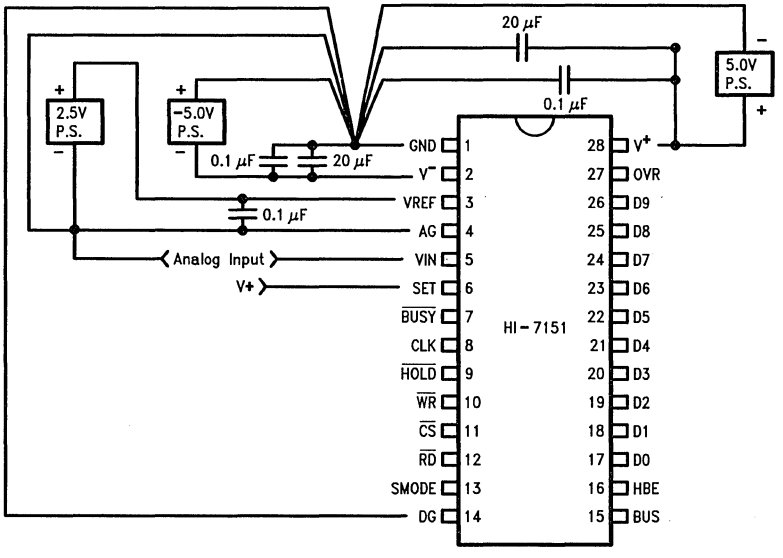


Figure 6: Ground and Power Supply Decoupling

OPTIMIZING SYSTEM PERFORMANCE

The HI-7151 has three ground pins (AG, DG, GND) for improved system accuracy. Proper grounding and bypassing is illustrated in Figure 6. The AG pin is a ground pin that does not carry any current and is used internally as a reference ground. The reference input and analog input should be referenced to the analog ground (AG) pin. The digital inputs and outputs should be referenced to the digital ground (DG) pin. The GND pin is a return point for the supply current of the comparator array. The comparator array is designed such that this current is approximately constant at all times and does not vary with input voltage. By virtue of the switched capacitor nature of the comparators, it is necessary to hold GND firmly at zero volts at all times. Therefore, the system ground star connection should be located as close to this pin as possible.

As in any analog system, good supply bypassing is necessary in order to achieve optimum system performance (minimize conversion errors). The power supplies should be bypassed with at least a 20 µF tantalum and 0.1 µF ceramic capacitors to GND. The reference input should be bypassed with a 0.1 µF ceramic capacitor to AG. The capacitor leads should be as short as possible.

The pins on the HI-7151 are arranged such that the analog pins are well isolated from the digital pins. In spite of this arrangement, there is always pin to pin coupling. Therefore the analog inputs to the device should not be driven from very high output impedance sources. PC board layout should screen the analog and reference inputs with AG. Using a soldier mask is good practice and helps reduce leakage due to moisture contamination on the PC board.

APPLICATIONS

Typical applications are illustrated in Figures 7 through 9 for the slow memory, fast memory, and DMA modes of operation. The output data is configured for 16-bit bus operation for these three applications. By tying BUS to DG and connecting the HBE input to the system address decoder, the output data can be configured for 8-bit bus systems.

Figure 10 illustrates an application where the HI-7151 is used with an analog multiplexer to form a multi-channel data acquisition system. Either slow memory or fast memory modes of operation can be selected. Fast memory mode should be selected for maximum throughput. Multiplexer channel acquisition should occur approximately 500 ns after $\overline{HOLD}$ goes high. This allows 2 clocks minus 0.5 µs for the input to settle. With a 300 kHz clock the input has up to 6.2 µs to settle.

NOTE: All typical values have been characterized but are not tested.

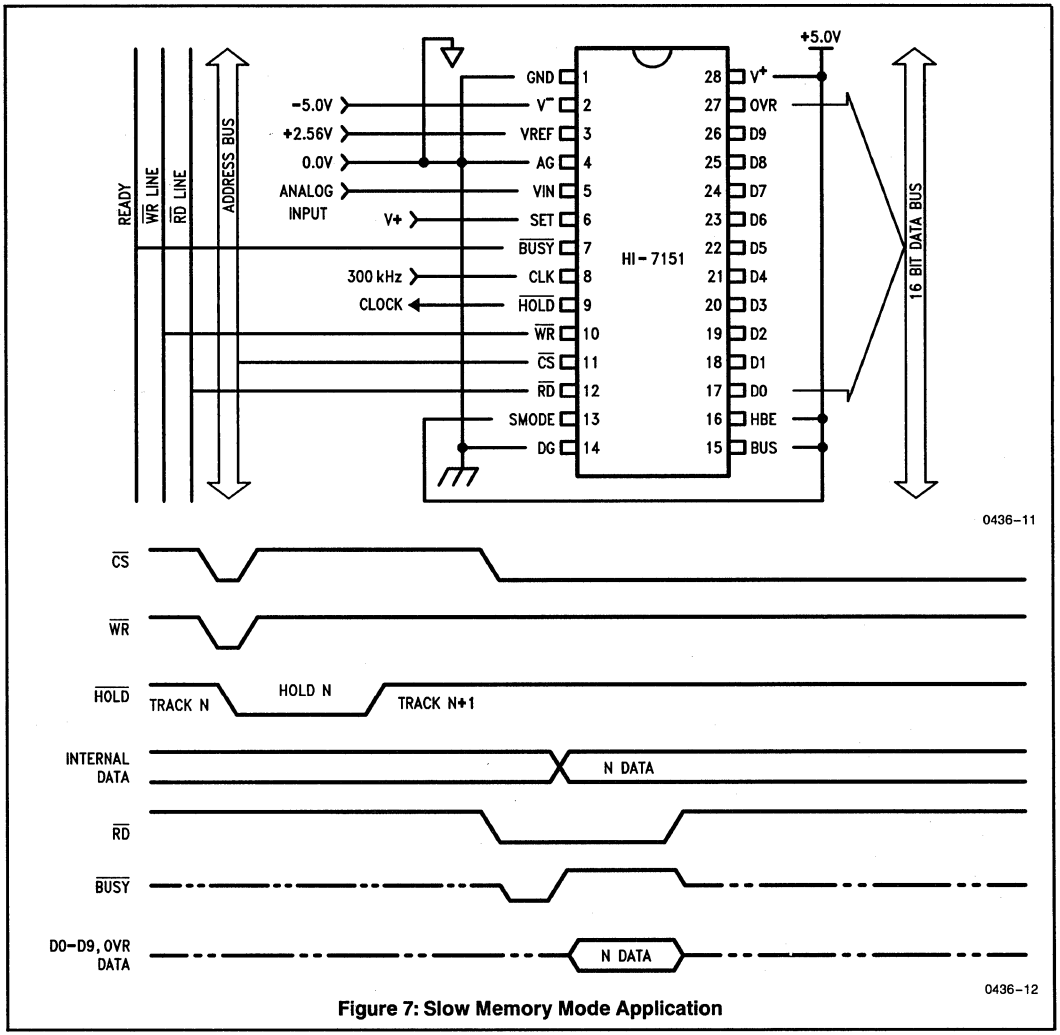


Figure 7: Slow Memory Mode Application

NOTE: All typical values have been characterized but are not tested.

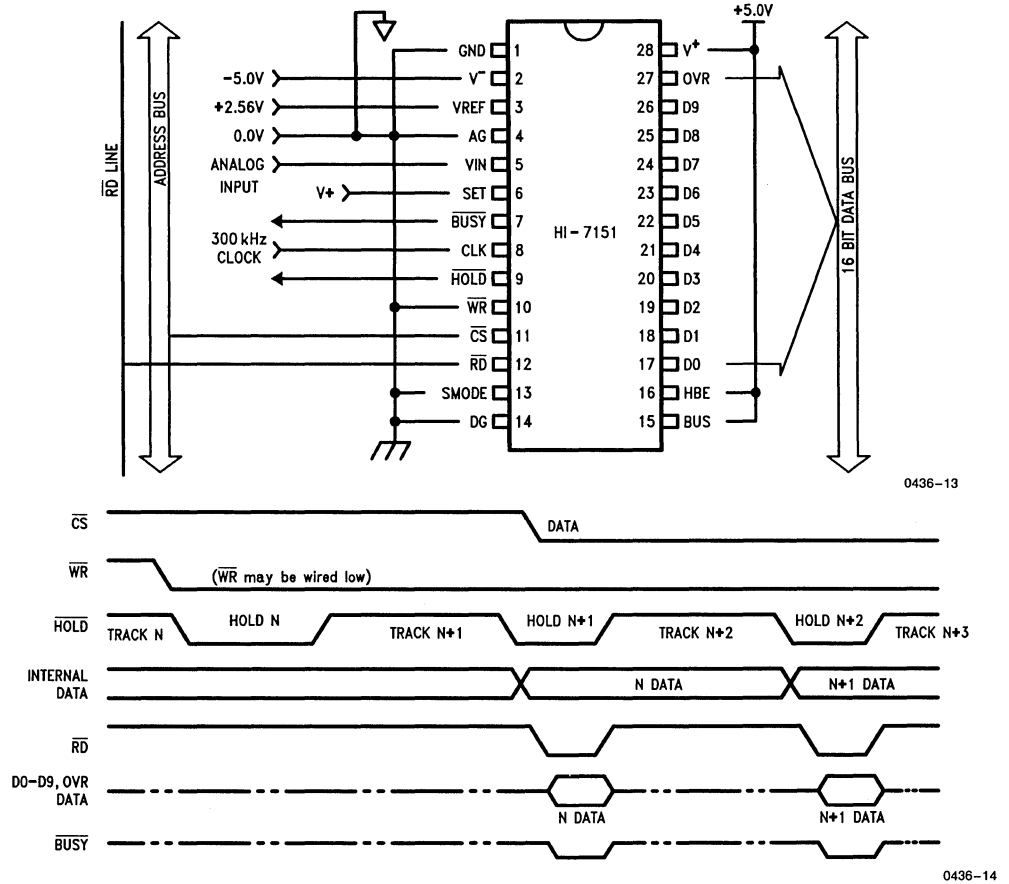


Figure 8: Fast Memory Mode Application

NOTE: All typical values have been characterized but are not tested.

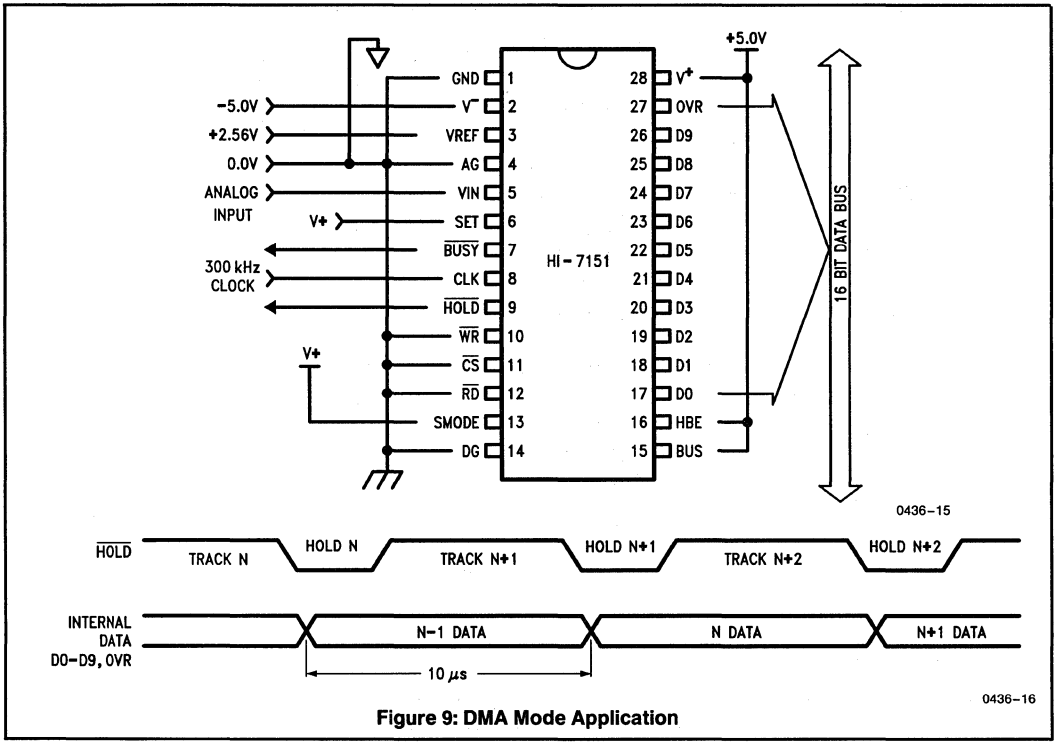


Figure 9: DMA Mode Application

An intelligent system which performs a scale factor adjustment under software control with the addition of a programmable gain block between the multiplexer and HI-7151 is illustrated in Figure 11. The microprocessor first performs a conversion and then checks the over-range status (OVR) bit. If the OVR bit is high, the microprocessor addresses a precision gain circuit for scale factor adjustment and initiates another conversion. The microprocessor must keep track of the selected scale factor.

The accuracy of the programmable gain amplifier should be better than 0.05%. For optimum system performance, op amp frequency response, settling time, and charge injection of the analog switch must be considered.

Figure 12 illustrates the HI-7151 interfaced to FIFO memories for use in DMA applications.

NOTE: All typical values have been characterized but are not tested.

HI-7151

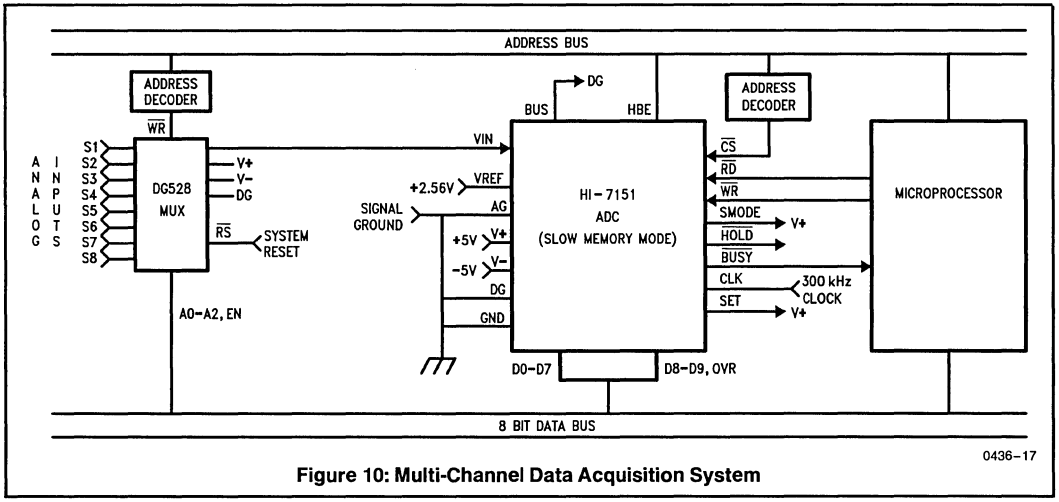


Figure 10: Multi-Channel Data Acquisition System

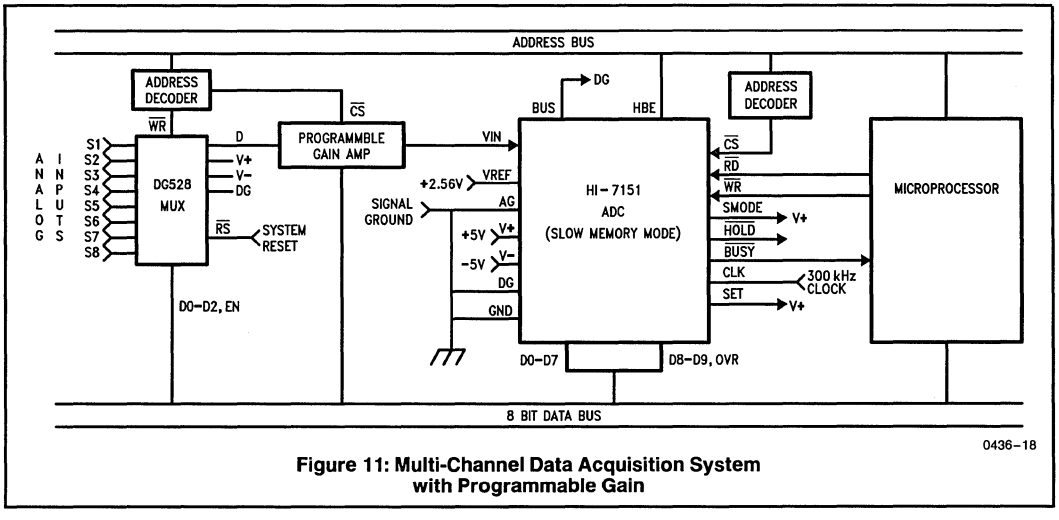


Figure 11: Multi-Channel Data Acquisition System with Programmable Gain

NOTE: All typical values have been characterized but are not tested.

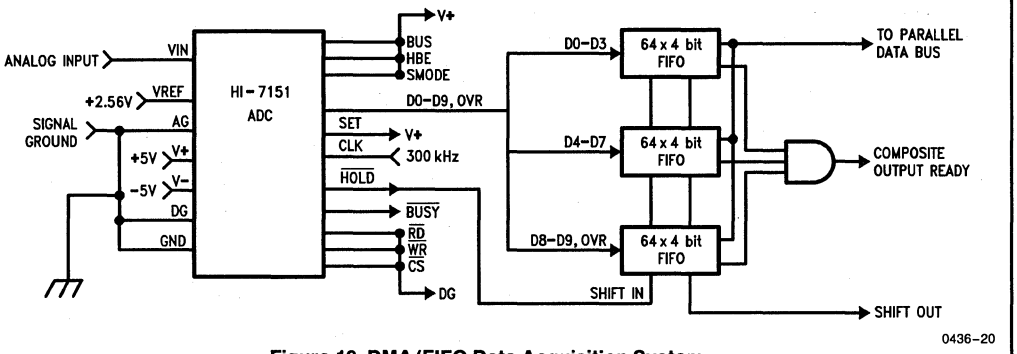


Figure 12: DMA/FIFO Data Acquisition System

NOTE: All typical values have been characterized but are not tested.

HI-7152
10-Bit High Speed A/D Converter with Track & Hold

GENERAL DESCRIPTION

The Harris HI-7152 is a high speed 10-bit A/D converter which uses a Two Step Flash algorithm to achieve throughput rates of 200 kHz. A unique switched capacitor technique allows a new input voltage to be sampled while a conversion is taking place.

A Track and Hold amplifier is included on the chip, consisting of two high speed amplifiers and an internal hold capacitor.

Microprocessor bus interfacing is simplified by the use of standard Chip Select, Read, and Write control signals. The digital three-state outputs are byte organized for interfacing to either 8- or 16-bit systems. An Over-Range pin, together with the MSB, can be used to indicate an out-of-range condition.

The HI-7152 operates with ±5V supplies. A single +2.5V reference is required to provide a bipolar input range from −2.5V to +2.5V.

Internal high speed CMOS buffers at both the analog and reference inputs simplifies external drive requirements.

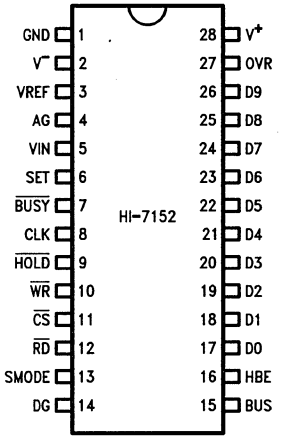


Figure 1: Pin Configuration

FEATURES

- **5 μs Conversion Time**
- **200 KHz Continuous Throughput Rate**
- **No Offset or Gain Adjustments Necessary**
- **Internal Track and Hold Amplifier**
- **Analog and Reference Inputs Fully Buffered**
- **μP Compatible Byte Organized Outputs**
- **Low Power Consumption (150 mW)**
- **Uses a Single 2.5V Reference for ±2.5V Input Range**

APPLICATIONS

- **μP Controlled Data Acquisition Systems**
- **DSP**
  - **—Avionics**
  - **—Sonar**
- **Process Control**
  - **—Automotive Transducer Sensing**
  - **—Industrial**
- **Robotics**
- **Digital Communications**
- **Image Processing**

ORDERING INFORMATION

Part Number	Linearity (Max. DLE)	Temperature Range*	Package
HI3-7152J-5	±1 LSB	0°C to +75°C	28 Pin Plastic DIP
HI3-7152K-5	±1/2 LSB	0°C to +75°C	28 Pin Plastic DIP
HI3-7152A-9	±1 LSB	0°C to +85°C	28 Pin Plastic DIP
HI3-7152B-9	±1/2 LSB	0°C to +85°C	28 Pin Plastic DIP
HI1-7152S-2	±1 LSB	-55°C to +125°C	28 Pin Ceramic DIP

4

301674-001

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage
V^+ to GND (DG/AG/GND) ..... $-0.3V < V^+ < +5.7V$
V^- to GND (DG/AG/GND)..... $-5.7V < V^- < +0.3V$
Analog Input Pins ..... $V^- - 0.3V < V_{INA} < V^+ + 0.3V$
Digital I/O Pins ..... DG $- 0.3V < V_{I/O} < V^+ + 0.3V$
Power Dissipation (Note 2) ..... <500 mW
derate above 75°C at 10 mW/°C
Operating Temperature Range
HI3-7152X-5 .....0°C to +75°C
HI3-7152X-9 .....−40°C to +85°C
Storage Temperature Range .....−65°C to +150°C
Lead Temperature (soldering, 10 sec) .....300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTE 1: Input voltages may exceed the supply voltage provided the input current is limited to ±1 mA
2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

ELECTRICAL CHARACTERISTICS (Note 4)

ACCURACY $V^+ = +5V, V^- = -5V, V_{REF} = 2.50V$. fclk = 600 kHz, 50% duty cycle.

Symbol	Parameter	Temperature (Note 3)	J, A Grade			K, B Grade			Units
			Min	Typ	Max	Min	Typ	Max	
RES	Resolution (Note 5) (with no missing codes)	$T_A = +25°C$	10			10			bits
		$T_{MIN} \le T_A \le T_{MAX}$	10			10			bits
ILE	Integral Linearity Error	$T_A = +25°C$		±0.5	±1.0		±0.3	±0.5	LSB
		$T_{MIN} \le T_A \le T_{MAX}$		±0.75	±1.0		±0.5	±0.75	LSB
DLE	Differential Linearity Error	$T_A = +25°C$			±1.0			±0.5	LSB
		$T_{MIN} \le T_A \le T_{MAX}$			±1.0			±0.75	LSB
V_{OS}	Bipolar Offset Error	$T_A = +25°C$		±1.0	±2.5		±0.6	±1.5	LSB
		$T_{MIN} \le T_A \le T_{MAX}$		±1.5	±3.0		±1.0	±2.0	LSB
eG^+ and eG^-	Unadjusted Gain Error	$T_A = +25°C$		±1.0	±2.5		±0.6	±1.5	LSB
		$T_{MIN} \le T_A \le T_{MAX}$		±1.5	±3.0		±1.0	±2.0	LSB

NOTES 3: See Ordering Information Table.
4: FSR (Full Scale Range) = 2 × V_{REF} (5.00V at V_{REF} = 2.50V). LSB (Least Significant Bit) = FSR/1024 (4.88 mV at V_{REF} = 2.50V).
5: Parameter not tested. Parameter guaranteed by design, simulation, or characterization.
6: Only V_{OS} and GAIN ERROR functionality tested at 2.2V and 2.6V.

DC CHARACTERISTICS

$V^+ = 5V, V^- = -5V, V_{REF} = 2.50V, T_A = +25°C$, fclk = 600 kHz, 50% duty cycle, unless stated otherwise.

Symbol	Parameter	Conditions (Note 4)	+25°C			0°C to +75°C		−40°C to +85°C		Units	Note
			Min	Typ	Max	Min	Max	Min	Max		
ANALOG INPUT											
VIR	Analog Input Range		$-V_{REF}$		$+V_{REF}$	$-V_{REF}$	$+V_{REF}$	$-V_{REF}$	$+V_{REF}$	V	
IBI	Analog Input Bias Current	V_{IN} = 0V		0.01	100		100		100	nA	
CV_{IN}	Analog Input Capacitance			8	20					pF	5
REFERENCE INPUT											
VRR	Reference Input Range		2.2	2.5	2.6	2.2	2.6	2.2	2.6	V	6
IBR	Reference Input Bias Current	V_{REF} = 2.50V		0.01	100		100		100	nA	
CVr	Reference Input Capacitance			7	20					pF	5

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued)

DC CHARACTERISTICS (Continued)

$V^+ = 5V$, $V^- = -5V$, $V_{REF} = 2.50V$, $T_A = +25°C$, fclk = 600 kHz, 50% duty cycle, unless stated otherwise.

Symbol	Parameter	Conditions (Note 4)	+25°C			0°C to +75°C		−40°C to +85°C		Units	Note
			Min	Typ	Max	Min	Max	Min	Max		
TRACK AND HOLD (See text)											
SR	Slew Rate			9						V/μs	
BW	Bandwidth			1.5						MHz	
	Aperture Time			30						ns	
	Aperture Uncertainty			2						ns	
	Feedthrough in HOLD	F_{IN} = 100 kHz		−80						dB	
	Acquisition Time			1.5						μs	
LOGIC INPUTS											
V_{IH}	Input High Voltage		2.0			2.0		2.0		V	
V_{IL}	Input Low Voltage				0.8		0.8		0.8	V	
I_{IL}	Logic Input Current	V_{IN} = 0V, V^+		0.05	1		1		1	μA	
C_{IN}	Input Capacitance			5	17					pF	5
LOGIC OUTPUTS											
V_{OH}	Output High Voltage	I_{OH} = −200 μA	2.4			2.4		2.4		V	
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA			0.4		0.4		0.4	V	
I_{OL}	Output Leakage Current	$\overline{RD}$ = V^+, V_{OUT} = V^+		0.04	1		10		10	μA	
		$\overline{RD}$ = V^+, V_{OUT} = 0V	−1	−0.01		−10		−10		μA	
C_{OUT}	Output Capacitance	High-Z State		7	15					pF	5
POWER SUPPLY VOLTAGE RANGE											
V^+		Functional Operation	4.5	5.0	5.5	4.5	5.5	4.5	5.5	V	7
V^-		Only	−4.5	−5.0	−5.5	−4.5	−5.5	−4.5	−5.5	V	7
POWER SUPPLY REJECTION											
eGVS	V^+, V^- Gain Coefficient	V^+ = 5V, V^- = −4.75V, −5.25V		±0.1	±0.5		±0.6		±0.6	LSB	
		V^- = −5V, V^+ = 4.75V, 5.25V		±0.1	±0.5		±0.6		±0.6		
VOSVS	V^+, V^- Offset Coefficient	V^+ = 5V, V^- = −4.75V, −5.25V		±0.1	±0.5		±0.6		±0.6	LSB	
		V^- = −5V, V^+ = 4.75V, 5.25V		±0.1	±0.5		±0.6		±0.6		
SUPPLY CURRENTS											
I^+	V+ Supply Current	V^+ = 5V ±10%,		20	30		30		30	mA	
I^-	V− Supply Current	V^- = −5V ±10%		−10	−15		−15		−15	mA	
IGND	GND Current	V_{IN} = 0V, Digital		−8	−15		−15		−15	mA	
IDG	DG Current	Outputs are Unloaded		−2	−3		−3		−3	mA	
IAG	AG Current			0.02	10		10		10	μA	

NOTES 4: FSR (Full Scale Range) = 2 × V_{REF} (5.00V at V_{REF} = 2.50V). LSB (Least Significant Bit) = FSR/1024 (4.88 mV at V_{REF} = 2.50V).

5: Parameter not tested. Parameter guaranteed by design, simulation, or characterization.

6: Only V_{OS} and GAIN ERROR functionality tested at 2.2V and 2.6V.

7: Guaranteed by functionality test.

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued)

AC CHARACTERISTICS

$V^+ = 5V \pm 10\%$, $V^- = -5V \pm 10\%$, $V_{REF} = 2.50V$, $T_A = +25°C$, fclk = 600 kHz, 50% duty cycle, $C_L = 100$ pF (including stray for D0–D9, OVR, $\overline{HOLD}$, $\overline{BUSY}$), unless stated otherwise

Symbol	Parameter	Conditions (Note 11)	+25°C			0°C to +75°C		−40°C to +85°C		Units	Note
			Min	Typ	Max	Min	Max	Min	Max		
D	Clock Input Duty Cycle		45	50	55	45	55	45	55	%	5
tsps	Continuous Conversion Time		60		3tck 5	60	3tck 5	60	3tck 5	µs µs	9 9
tconv	Slow Memory Mode Conversion Time				4tck + 0.9		4tck + 0.9		4tck + 0.9	µs	5, 8
tcyc	Continuous Throughput				fclk/3		fclk/3		fclk/3	sps	9
tck	CLOCK Period			1/fclk							
tckhr	CLOCK to $\overline{HOLD}$ Rise Delay		150	290	500	140	525	120	525	ns	5
twrl	$\overline{WR}$ Pulse Width		200	113	tck/2	225	tck/2	225	tck/2	ns	5, 8, 10
thold	$\overline{WR}$ to $\overline{HOLD}$ Delay			80	170		200		200	ns	5,8
tbd	$\overline{BUSY}$ to DATA			40	200		230		230	ns	5, 8
twrd	$\overline{WR}$ to $\overline{RD}$ Active		100			100		100		ns	5, 8
tckhf	CLOCK to $\overline{HOLD}$ Fall Delay		50	125	250	40	275	25	275	ns	5, 9
tdata	$\overline{HOLD}$ to DATA Change		100	200	400	90	550	70	550	ns	5, 9
trd	$\overline{RD}$ LO to Active			75	150		190		190	ns	5, 13
trx	$\overline{RD}$ HI to Inactive			25	60		80		80	ns	5, 14
tad	HBE to DATA			70	150		165		165	ns	5
tcd	$\overline{CS}$ to DATA			95	180		210		210	ns	5
tbusy	$\overline{RD}$ to $\overline{BUSY}$			35	200		200		200	ns	5
tr	Rise Time			50	100		125		125	ns	5, 12
tf	Fall Time			45	100		120		120	ns	5, 12

NOTES **8:** Slow memory mode timing.

9: Fast memory or DMA mode of operation, except the first conversion which is equal to tconv.

10: Maximum specification to prevent multiple triggering with $\overline{WR}$.

11: All input drive signals are specified with $tr = tf \leq 20$ ns and shall swing from $V_{IL} - 0.4V$ to $V_{IH} + 0.4V$ for all timing specifications. A signal is considered to change state as it crosses a 1.4V threshold (except trd & trx).

12: tr and tf load is $C_L = 100$ pF (including stray capacitance) to DG and is measured from the 10%–90% point.

13: trd is the time required for the data output level to change by 10% in response to $\overline{RD}$ crossing a voltage level of 1.4V. High-Z to V_{OH} is measured with $R_L = 2.5$ kΩ and $C_L = 100$ pF (including stray) to DG. High-Z to V_{OL} is measured with $R_L = 2.5$ kΩ to V^+ and $C_L = 100$ pF (including stray) to DG.

14: trx is the time required for the data output level to change by 10% in response to $\overline{RD}$ crossing a voltage level of 1.4V. V_{OH} to High-Z is measured with $R_L = 2.5$ kΩ and $C_L = 10$ pF (including stray) to DG. V_{OL} to High-Z is measured with $R_L = 2.5$ kΩ to V^+ and $C_L = 10$ pF (including stray) to DG.

NOTE: All typical values have been characterized but are not tested.

HI-7152

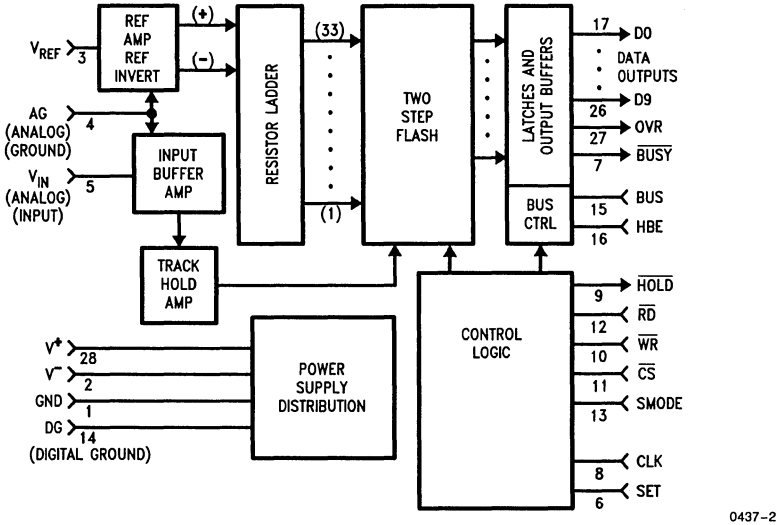


Figure 2: Functional Diagram

4

NOTE: All typical values have been characterized but are not tested.

TIMING DIAGRAMS

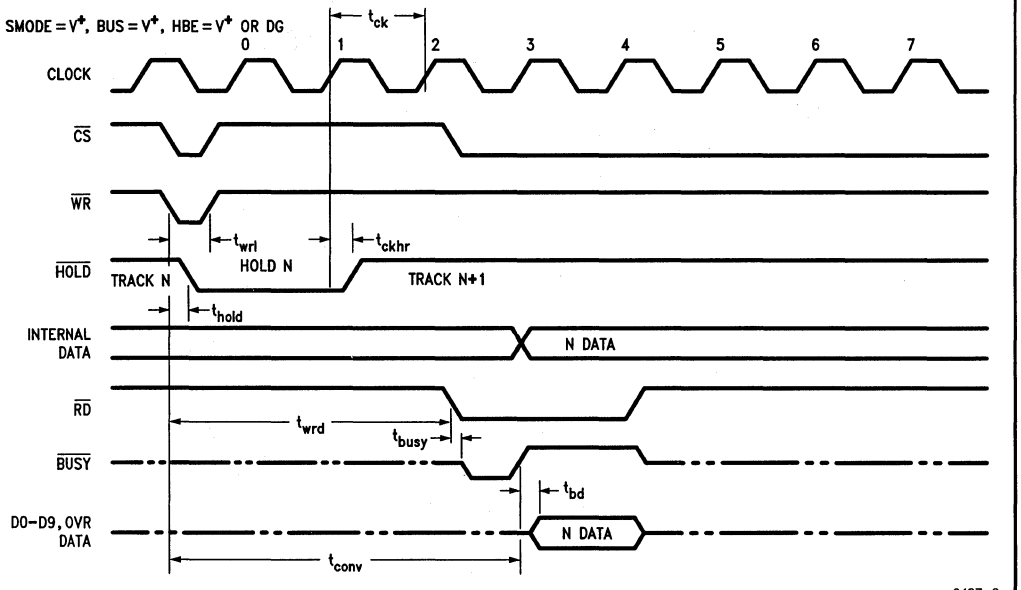
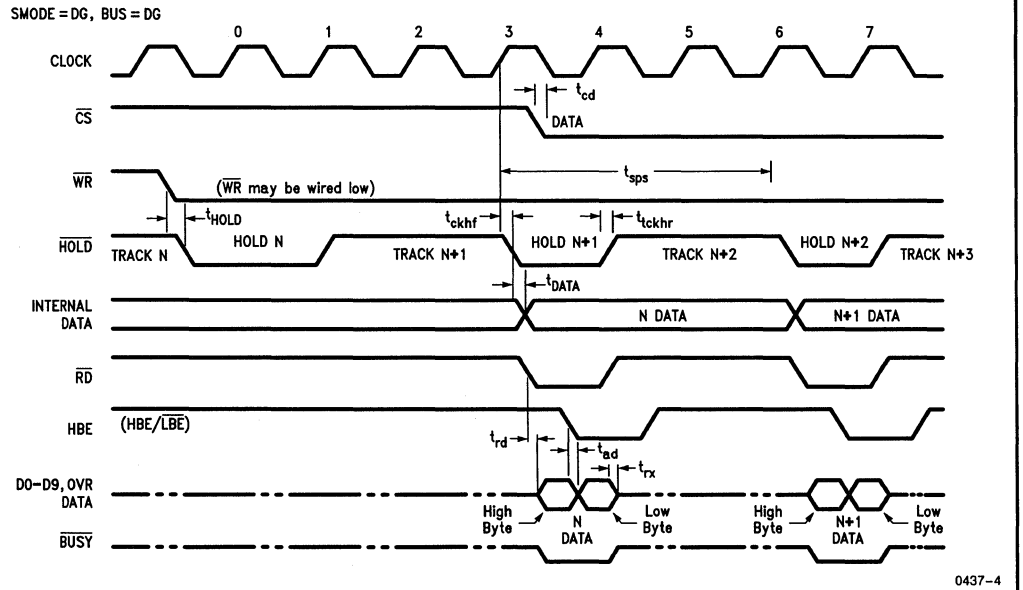


Figure 3A: Slow Memory Mode (16-Bit Data Bus)



NOTE: With SMODE = DG, Internal Logic Disables the Output Latches from Being Updated during a Read Operation.

Figure 3B: Fast Memory Mode (8-Bit Data Bus)

NOTE: All typical values have been characterized but are not tested.

HI-7152

TIMING DIAGRAMS (Continued)

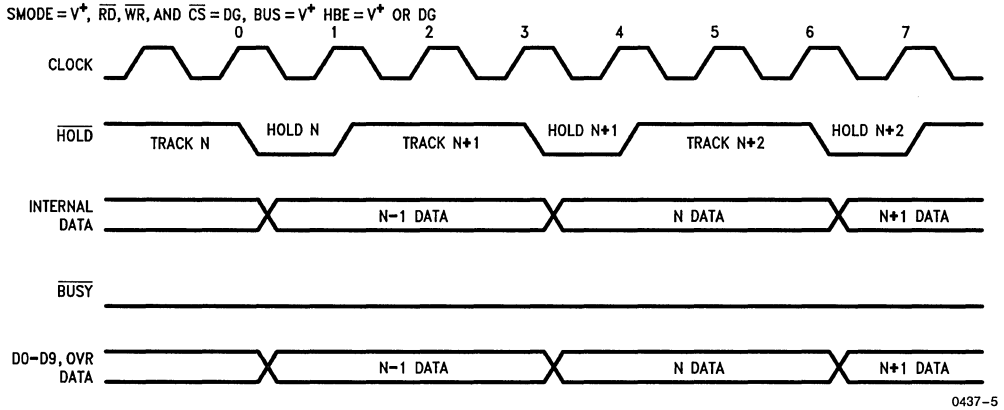


Figure 3C: DMA Mode (16-Bit Data Bus)

4

NOTE: All typical values have been characterized but are not tested.

Table 1: Pin Description

Pin	Name	Description
1	GND	Ground return for comparators (0V)
2	V^-	Negative supply voltage input (−5.0V)
3	V_{REF}	Reference voltage input (+2.50V)
4	AG	Analog ground reference (0V)
5	V_{IN}	Analog input voltage
6	SET	Connect to V^+ for proper operation.
7	$\overline{BUSY}$	Output High—Conversion complete. Output Low—Conversion in progress. Output floats when chip is not selected ($\overline{RD}$ and $\overline{CS}$ both high).
8	CLK	Clock input
9	$\overline{HOLD}$	Indicates start of conversion. Active low.
10	$\overline{WR}$	Write input. With $\overline{CS}$ low, starts conversion when pulsed low; continuous conversions when kept low.
11	$\overline{CS}$	Chip select input. Active low.
12	$\overline{RD}$	Read input. With $\overline{CS}$ low, enables output buffers when pulsed low; outputs updated at end of conversion when kept low.
13	SMODE	Slow memory mode input. Active high.
14	DG	Digital ground (0V)

Pin	Name	Description	
15	BUS	Bus select input High = all outputs enabled together D0–D9, OVR Low = outputs enabled by HBE	
16	HBE	Byte select (HBE/LBE) input for 8-bit bus. Input high—High byte select, D8–D9, OVR Input low—Low byte select, D0–D7	
17	D0	Bit 0 (Least significant, LSB)	Low Byte
18	D1	Bit 1	
19	D2	Bit 2	
20	D3	Bit 3 (Output Data Bits (High = True))	
21	D4	Bit 4	
22	D5	Bit 5	
23	D6	Bit 6	
24	D7	Bit 7	
25	D8	Bit 8 (Most significant)	High Byte
26	D9	Bit 9 (Sign)	
27	OVR	Out of Range flag. Valid at end of conversion when output exceeds full-scale.	
28	V^+	Positive supply voltage input (+5.0V)	

DETAILED DESCRIPTION

The HI-7152 is a high speed 10-bit A/D converter which achieves throughput rates of 200 kHz by use of a Two Step Flash algorithm. A pipelined operation has been achieved through the use of switched capacitor techniques which allow the device to sample a new input voltage while a conversion is taking place. The HI-7152 requires a single reference input of +2.5V, which is internally inverted to −2.5V, thereby allowing an input range of −2.5V to +2.5V. 10 bits including sign are two's complement coded. The analog and reference inputs are internally buffered by high speed CMOS buffers, which greatly simplifies the external analog drive requirements for the device.

NOTE: All typical values have been characterized but are not tested.

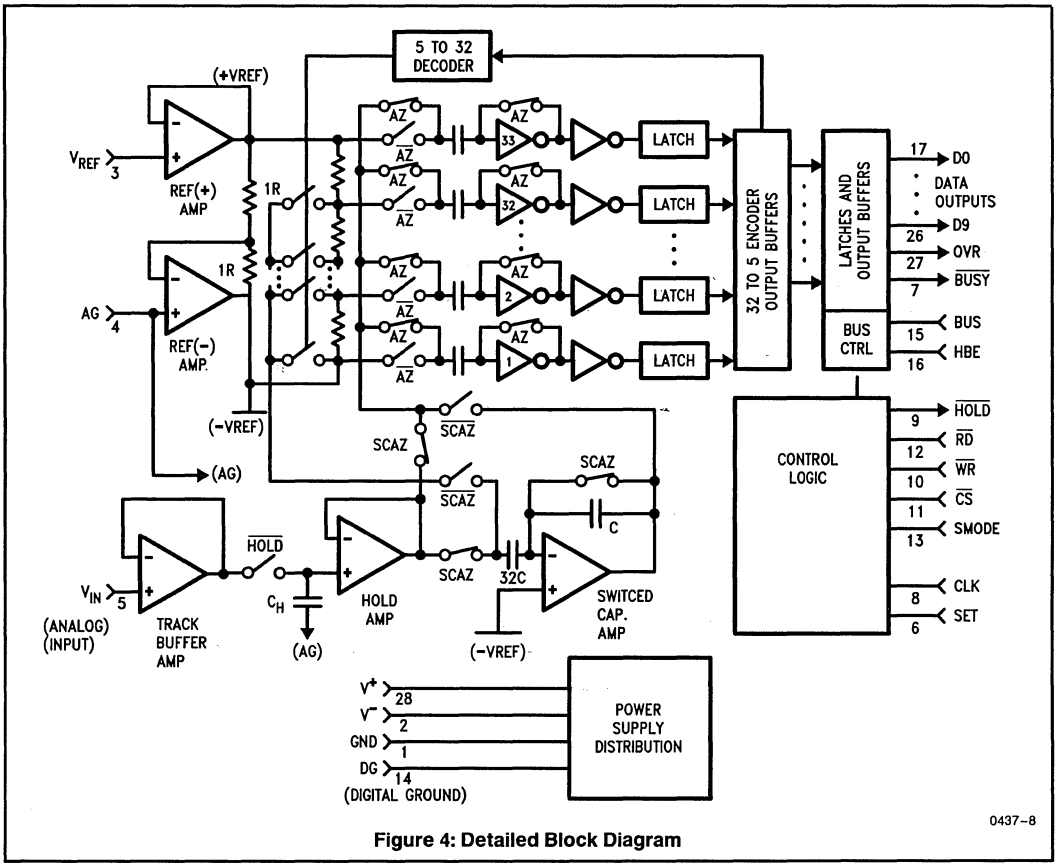


Figure 4: Detailed Block Diagram

A/D SECTION

The HI-7152 uses a conversion algorithm which is generally called a "Two Step Flash" algorithm. This algorithm enables very fast conversion rates without the penalty of high power dissipation or high cost. A detailed functional diagram is presented in Figure 4.

The input voltage is first converted into a 5-bit result (plus Out of Range information) by the flash converter. This flash converter consists of an array of 33 auto-zeroed comparators which perform a comparison between the input voltage and subdivisions of the reference voltage. These subdivisions of the reference voltage are formed by forcing the reference voltage and its negative on the two ends of a string of 32 resistors.

The reference input to the HI-7152 is buffered by a high speed CMOS amplifier which is used to drive one end of the resistor string. Another high speed amplifier configured in the inverting unity gain mode inverts the reference voltage with respect to analog ground and forces it onto the other end of the resistor string. Both reference amplifiers are offset trimmed at the factory in order to increase the accuracy of the HI-7152 and to simplify its usage.

The 5-bit result of the first flash conversion is latched into the upper five bits of double buffered latches. It is also converted back into an analog signal by choosing the ladder voltage which is closest to but less than the input voltage. The selected voltage (VTAP) is then subtracted from the input voltage. This residue is amplified by a factor of 32 and referenced to the negative reference voltage ($VSCA = (V_{IN} - VTAP) \times 32 + V_{REF}^-$). This subtraction and amplification operation is peformed by a Switched Capacitor Amplifier (SCA). The output of the SCA falls between the positive and negative reference voltages and can therefore be digitized by the original 5-bit flash converter (second flash conversion).

The 5-bit result of the second flash conversion is latched into the lower five bits of double buffered latches. At the end of a conversion, 10 bits of data plus an Out of Range bit are latched into the second level of latches and can then be put on the digital output pins.

NOTE: All typical values have been characterized but are not tested.

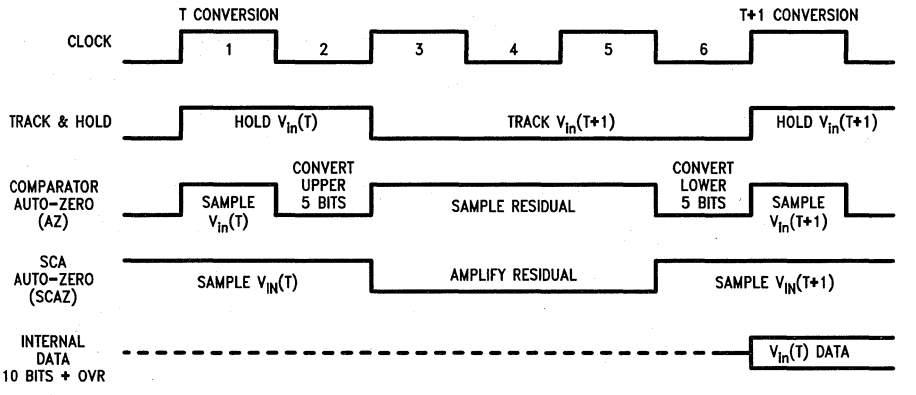


Figure 5: Internal ADC Timing Diagram

The conversion takes place in three clock cycles and is illustrated in Figure 5. When the conversion begins, the track and hold goes into its hold mode for 1 clock cycle. During the first half clock cycle the comparator array is in its auto-zero mode and it samples the input voltage. During the second half clock cycle, the comparators make a comparison between the input voltage and the ladder voltages. At the beginning of the third half clock cycle, the first most significant 5-bit result becomes available. During the first clock cycle, the SCA was sampling the input voltage. After the first flash result becomes available and a ladder tap voltage has been selected the SCA amplifies the residue between the input and ladder tap voltages. During the next three half clock cycles, while the SCA output is settling to its required accuracy, the comparators go into their auto-zero mode and sample this voltage. During the sixth half clock cycle, the comparators perform another comparison whose 5-bit result becomes available on the next clock edge.

TRACK AND HOLD ANALOG INPUT

A Track and Hold amplifier has been fully integrated on the front end of the A/D converter. Because of the sampling nature of this A/D converter, the input is required to stay constant only during the first clock cycle. Therefore, the Track and Hold (T/H) amplifier "holds" the input voltage only during the first clock cycle and it acquires the input voltage for the next conversion during the remaining two clock cycles. The high input impedance of the T/H input amplifier simplifies analog interfacing. Input signals up to $\pm V_{REF}$ can be directly connected to the A/D without buffering. The A/D output code table is shown in Table 2.

The timing signals for the Track and Hold amplifier are generated internally, and are also provided externally ($\overline{HOLD}$) for synchronization purposes. The T/H amplifier consists of two high speed CMOS amplifiers and an internal hold capacitor. Its typical slew rate and bandwidth are 9V/μs and 1.5 MHz respectively. It is configured to give a very small hold pedestal without the use of an external hold capacitor. The hold pedestal is typically less than 100 μV.

Table 2: A/D Output Code Table

Analog Input		Output Data										
LSB = 2 (V_{REF})/1024	V_{REF} = 2.500V	OVR	SIGN 9	MSB 8	7	6	5	4	3	2	1	LSB 0
$\geq +V_{REF}$	2.500 to V+ (+OVR)	1	0	0	0	0	0	0	0	0	0	0
$+V_{REF}$ − 1LSB	2.49512 (+FULL SCALE)	0	0	1	1	1	1	1	1	1	1	1
+1LSB	0.00488	0	0	0	0	0	0	0	0	0	0	1
0	0.000	0	0	0	0	0	0	0	0	0	0	0
−1LSB	−0.00488	0	1	1	1	1	1	1	1	1	1	1
$-V_{REF}$	−2.500 (−FULL SCALE)	0	1	0	0	0	0	0	0	0	0	0
$\leq -V_{REF}$ − 1LSB	−2.50488 to V− (−OVR)	1	1	0	0	0	0	0	0	0	0	0

NOTE: All typical values have been characterized but are not tested.

HI-7152

Acquisition of the analog input signal is the time required by the T/H for its output to reach its final value within a specified error band. This time is a function of the logic delay time, op amp slewing time, and settling time. The T/H is in the track mode for 2 clock cycles (3.3 μs @ CLK = 600 kHz) but the output typically settles to within ¼ LSB in 1.5 μs.

Aperture delay time is the time required for the T/H switch to open following the internal hold command. This is the delay with respect to falling edge of $\overline{WR}$ and the internal hold command. It is equal to T_{HOLD} (typ) − 50 ns (typ) which is typically 30 ns.

Aperture uncertainty (jitter) is a range of variation in the aperture time. The greater the aperture time the larger the uncertainty in the analog voltage being converted. If the aperture time is nulled out by advancing the hold command ($\overline{WR}$) or the signal is repetitively sampled, aperture uncertainty becomes the major source of time error. The aperture uncertainty for the T/H is typically 2 ns which sets the maximum input bandwidth to 77.7 kHz for 1 LSB resolution.

$F_{max} = 1/(2\pi \times 2^n \times ta)$

where n = resolution in bits

ta = aperture uncertainty

All of the internal amplifiers are offset trimmed at the factory to give improved accuracy and to minimize the number of external components. If necessary, offset error can be adjusted either at an external interface buffer or by using digital post correction.

REFERENCE INPUT

The reference input to the HI-7152 is buffered by a high speed CMOS amplifier. The reference input range is 2.2V to 2.6V.

POWER REQUIREMENTS

Power to the chip should be applied in the following order: V^-, V^+, and V_{REF}. In applications where V^+ is supplied prior to V^-, the positive supply current will be approximately 2 times its nominal value until V^- is applied (this is not a latchup condition).

INITIALIZATION

In fast memory and DMA modes (after proper power, V_{REF}, and clock) up to 6 clock cycles are required for circuit initialization. After circuit initialization, valid data will be available in 3 clock cycles.

MICROPROCESSOR INTERFACE

The HI-7152 can be interfaced to microprocessors through the use of standard Write, Read, Chip Select, and HBE control pins. The digital outputs are two's complement coded, three-state gated, and byte organized for bus interface with 8- and 16-bit systems. The digital outputs (D0–D9, OVR, and $\overline{BUSY}$) may be accessed under control of BUS, byte enable input HBE, chip select, and read inputs for a simple parallel bus interface. The microprocessor can read the current data in the output latches in typically 75 ns/byte (trd). An over range pin (OVR) together with the MSB (D9) pin set to either a logic 0 or 1 will indicate a positive or negative over-range condition respectively. All digital output buffers are capable of driving one TTL load.

The HI-7152 can be interfaced to a microprocessor using one of three modes: slow memory, fast memory, and DMA mode.

SLOW MEMORY MODE

In slow memory mode, the conversion will be initiated by the microprocessor by selecting the chip ($\overline{CS}$) and pulsing $\overline{WR}$ low. This mode is selected by hardwiring the SMODE pin to V^+. This mode is intended for use with microprocessors (such as the 8086) which can be forced into a WAIT state. For example, in a configuration where the $\overline{BUSY}$ output is tied to the 8086 READY input, an attempt to read the data before the conversion is complete will force the processor into a WAIT state until $\overline{BUSY}$ goes high, at which time the data at the output is valid. This resembles a 5 μs access time RAM. It allows the processor to initiate a conversion, WAIT, and READ data with a single READ instruction. When the 8-bit bus operation is selected, high and low byte data may be accessed in either order. An I/O truth table is presented in Table 3 for the slow memory mode of operation.

NOTE: All typical values have been characterized but are not tested.

Table 3: Slow Memory Mode I/O Truth Table (SMODE = V+)

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	BUS	HBE	Function
0	0	X	X	X	Initiates a conversion
1	X	X	X	X	Disables all chip commands
0	X	0	1	X	D0–D9 and OVR enabled
0	X	0	0	0	Low byte enabled: D0–D7
0	X	0	0	1	High byte enabled: D8–D9, OVR
X	X	1	X	X	Disables all outputs (High impedance)

X = don't care

Table 4: Fast Memory Mode I/O Truth Table (SMODE = DG)

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	BUS	HBE	Function
X	0	X	X	X	Continuous conversion, $\overline{WR}$ may be tied to DG
1	X	X	X	X	Disables only the $\overline{RD}$ command
0	X	0	1	X	D0–D9 and OVR enabled
0	X	0	0	1	High byte enabled: D8–D9, OVR (enable 1st)
0	X	0	0	0	Low byte enabled: D0–D7 (must enable 2nd)
X	X	1	X	X	Disables all outputs (High impedance)

X = don't care

FAST MEMORY MODE

The fast memory mode of operation is selected by tying the SMODE and $\overline{WR}$ pins to DG. In this mode, the chip performs continuous conversions and only $\overline{CS}$ and $\overline{RD}$ are required to read the data. Whenever the SMODE pin is low, $\overline{WR}$ is independent of $\overline{CS}$ in starting a conversion cycle. During the first conversion cycle, $\overline{HOLD}$ follows $\overline{WR}$ going low.

Data can be read a byte at a time or all 11 bits at once. The internal logic disables the output latches from being updated during a read after the high byte data is accessed. It will continue to be disabled until after the low byte data is accessed. THEREFORE, WHEN 8-BIT BUS OPERATION IS SELECTED, THE DATA MUST BE ACCESSED HIGH BYTE FIRST, LOW BYTE NEXT. If the low byte is accessed first followed by high byte, the results from the next conversion cycle will be lost because the updating of the output latch is disabled. $\overline{BUSY}$ is continuously low when accessed with a read command in this mode. An I/O truth table is presented in Table 4 for the fast memory mode of operation.

The data can be defined in time by monitoring the $\overline{HOLD}$ pin. The conversion data can be read after $\overline{HOLD}$ has gone low.

DMA MODE

This mode is a complete hardwire mode where the HI-7152 continuously converts. The user implements hardware to store the results in memory, bypassing the microprocessor. This mode is recognized by the chip when SMODE is hardwired to V+ and $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ are hardwired to DG. When 8-bit bus operation is selected, high and low byte data may be accessed in either order. $\overline{BUSY}$ is continuously low when accessed with a read command in this mode. An I/O truth table is presented in Table 5 for the DMA mode of operation.

Table 5: DMA Mode I/O Truth Table (SMODE = V+, $\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = DG)

BUS	HBE	Function
1	X	D0–D9 and OVR enabled
0	0	Low byte enabled: D0–D7
0	1	High byte enabled: D8–D9, OVR

X = don't care

NOTE: All typical values have been characterized but are not tested.

OPTIMIZING SYSTEM PERFORMANCE

The HI-7152 has three ground pins (AG, DG, GND) for improved system accuracy. Proper grounding and bypassing is illustrated in Figure 6. The AG pin is a ground pin that does not carry any current and is used internally as a reference ground. The reference input and analog input should be referenced to the analog ground (AG) pin. The digital inputs and outputs should be referenced to the digital ground (DG) pin. The GND pin is a return point for the supply current of the comparator array. The comparator array is designed such that this current is approximately constant at all times and does not vary with input voltage. By virtue of the switched capacitor nature of the comparators, it is necessary to hold GND firmly at zero volts at all times. Therefore, the system ground star connection should be located as close to this pin as possible.

As in any analog system, good supply bypassing is necessary in order to achieve optimum system performance (minimize conversion errors). The power supplies should be bypassed with 20 μF tantalum and 0.1 μF ceramic capacitors to GND. The reference input should be bypassed with a 0.1 μF ceramic capacitor to AG. The capacitor leads should be as short as possible.

The pins on the HI-7152 are arranged such that the analog pins are well isolated from the digital pins. In spite of this arrangement, there is always pin to pin coupling. Therefore the analog inputs to the device should not be driven from very high output impedance sources. PC board layout should screen the analog and reference inputs with AG. Using a soldier mask is good practice and helps reduce leakage due to moisture contamination on the PC board.

APPLICATIONS

Typical applications are illustrated in Figures 7 through 9 for the slow memory, fast memory, and DMA modes of operation. The output data is configured for 16-bit bus operation for these three applications. By tying BUS to DG and connecting the HBE input to the system address decoder, the output data can be configured for 8-bit bus systems.

Figure 10 illustrates an application where the HI-7152 is used with an analog multiplexer to form a multi-channel data acquisition system. Either slow memory or fast memory modes of operation can be selected. Fast memory mode should be selected for maximum throughput. Multiplexer channel acquisition should occur approximately 500 ns after $\overline{HOLD}$ goes high. This allows 2 clocks minus 0.5 μs for the input to settle. With a 600 kHz clock the input has up to 2.8 μs to settle.

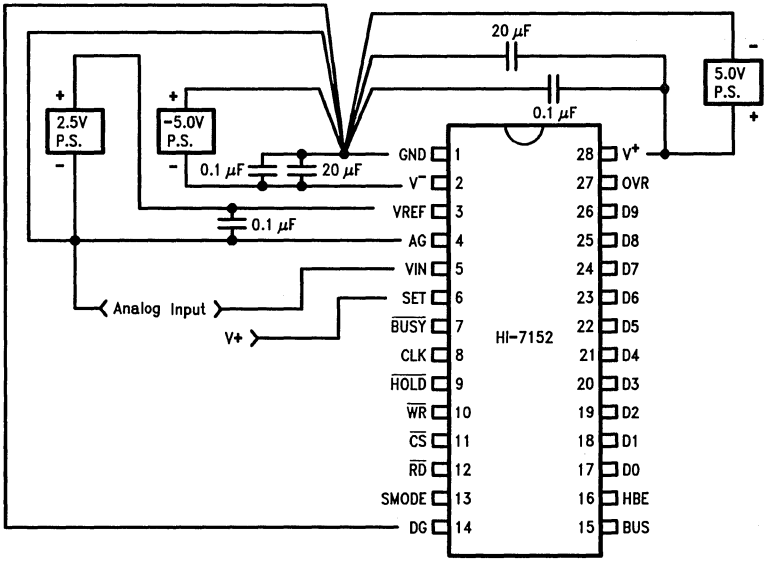


Figure 6: Ground and Power Supply Decoupling

NOTE: All typical values have been characterized but are not tested.

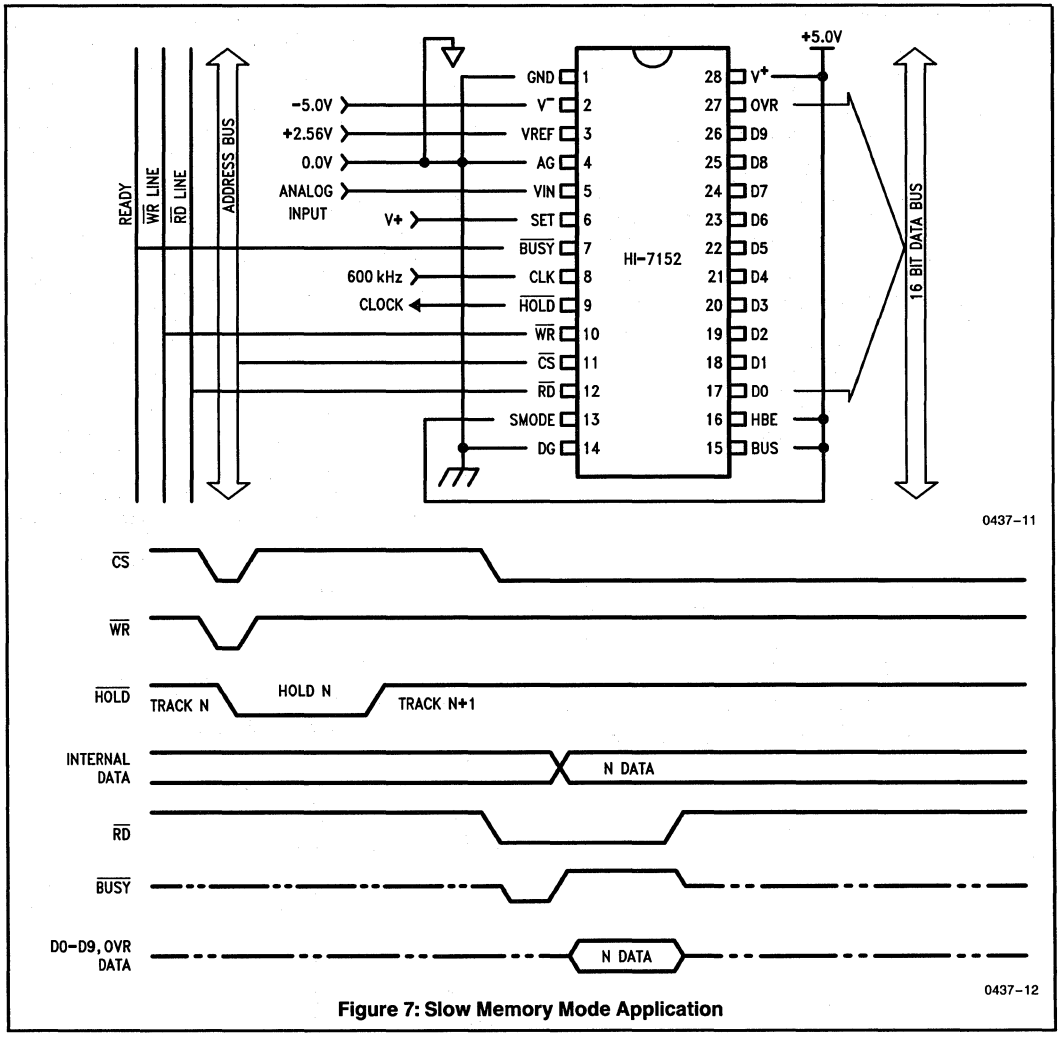


Figure 7: Slow Memory Mode Application

NOTE: All typical values have been characterized but are not tested.

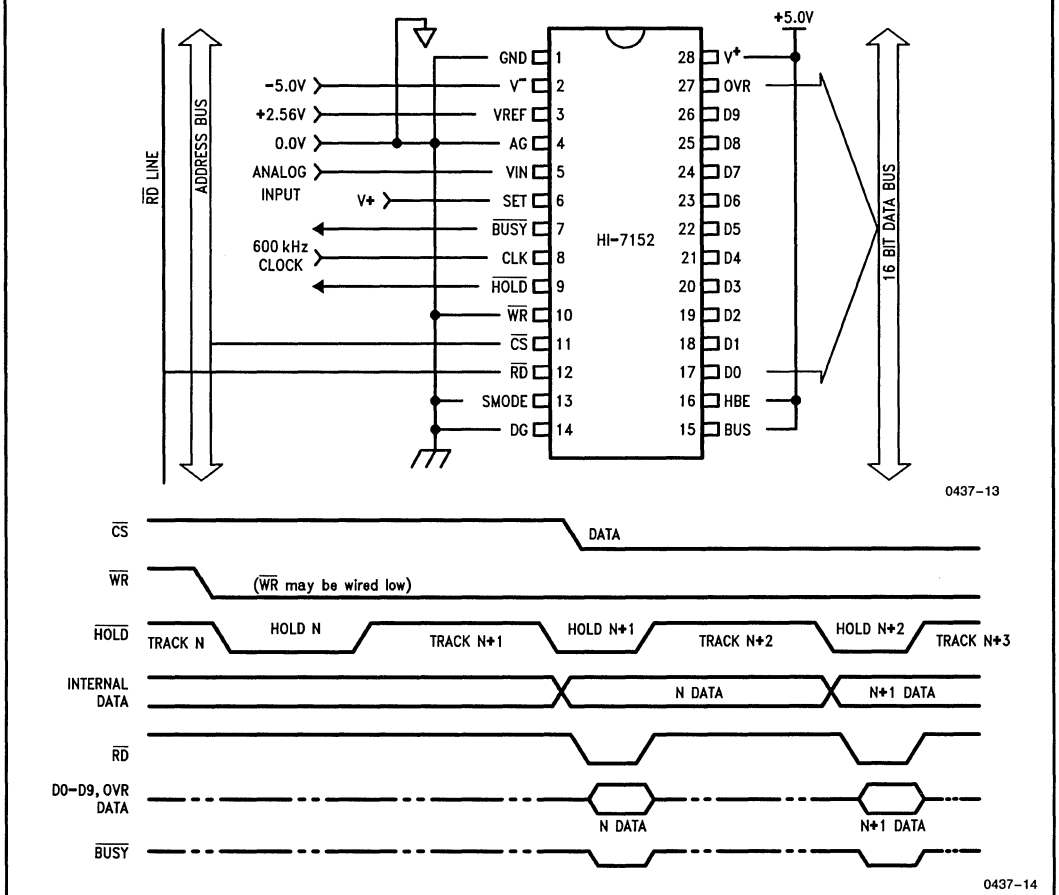


Figure 8: Fast Memory Mode Application

NOTE: All typical values have been characterized but are not tested.

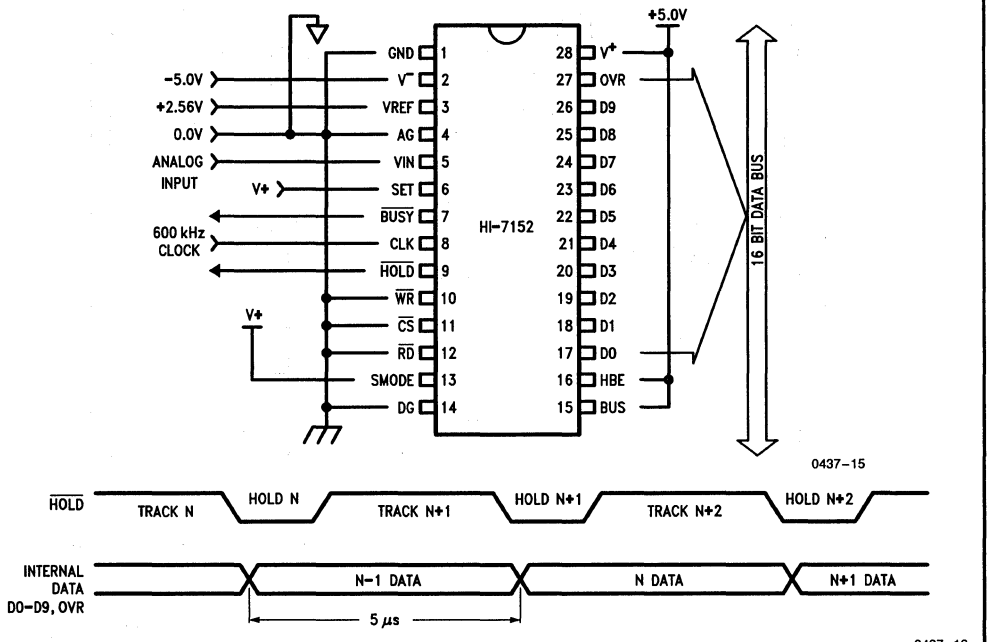


Figure 9: DMA Mode Application

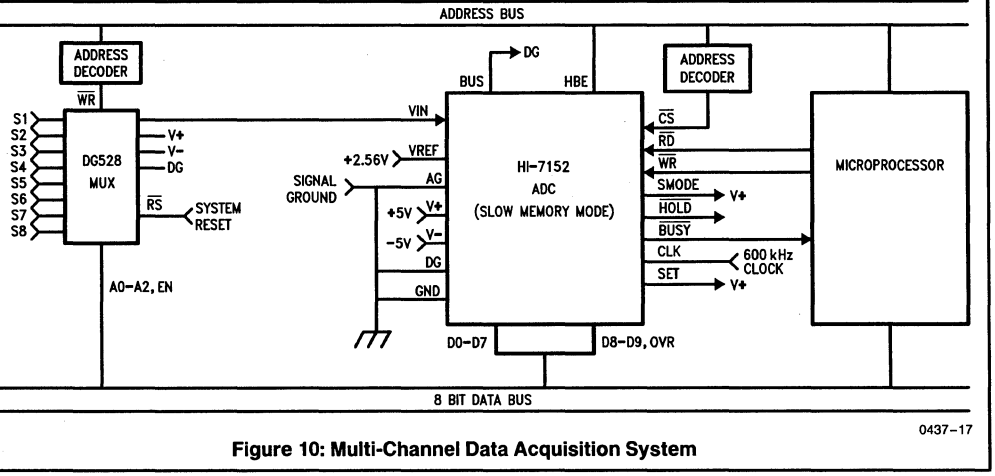


Figure 10: Multi-Channel Data Acquisition System

NOTE: All typical values have been characterized but are not tested.

An intelligent system which performs a scale factor adjustment under software control with the addition of a programmable gain block between the multiplexer and HI-7152 is illustrated in Figure 11. The microprocessor first performs a conversion and then checks the over-range status (OVR) bit. If the OVR bit is high, the microprocessor addresses a precision gain circuit for scale factor adjustment and initiates another conversion. The microprocessor must keep track of the selected scale factor.

The accuracy of the programmable gain amplifier should be better than 0.05%. For optimum system performance, op amp frequency response, settling time, and charge injection of the analog switch must be considered.

Figure 12 illustrates the HI-7152 interfaced to FIFO memories for use in DMA applications.

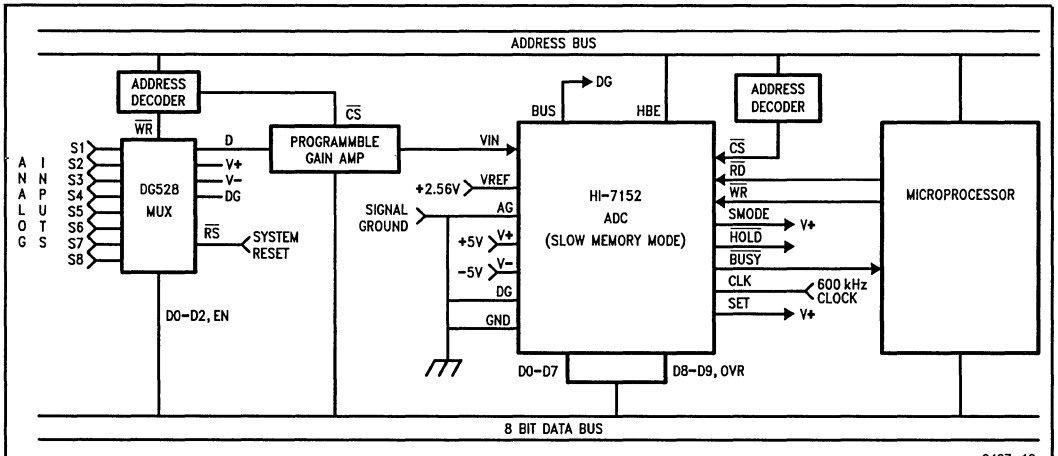


Figure 11: Multi-Channel Data Acquisition System with Programmable Gain

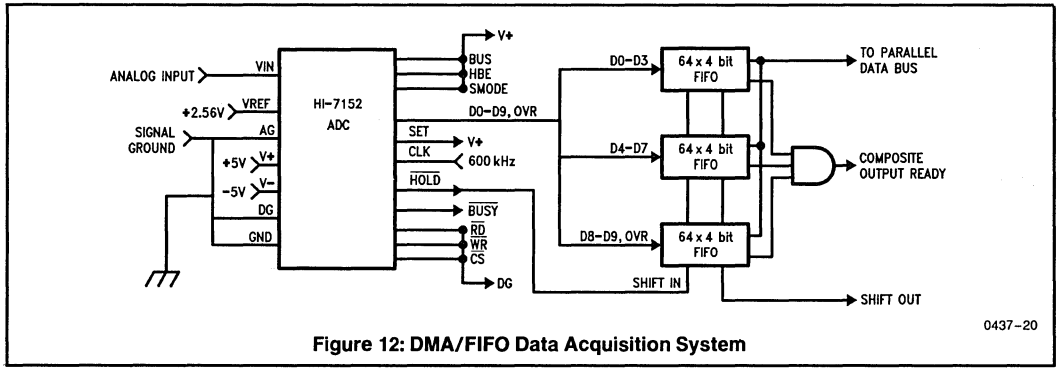


Figure 12: DMA/FIFO Data Acquisition System

NOTE: All typical values have been characterized but are not tested.

HARRIS

HI-7153

8-Channel 10 Bit High Speed Sampling A/D Converter

September 1991

Features

- 5μs Conversion Time
- 8-Channel Multiplexer
- 200,000 Channels/Second Throughput Rate
- Over 9 Effective Bits at 20kHz
- No Offset or Gain Adjustments Necessary
- Analog and Reference Inputs Fully Buffered
- On-Chip Track and Hold Amplifier
- μP Compatible Interface
- 2's Complement Data Output
- 150mW Power Consumption
- Only a Single 2.5V Reference Required for a ±2.5V Input Range
- Out-of-Range Flag

Applications

- μP Controlled Data Acquisition Systems
- DSP
  - ▸ Avionics
  - ▸ Sonar
- Process Control
  - ▸ Automotive Transducer Sensing
  - ▸ Industrial
- Robotics
- Digital Communications

General Description

The HI-7153 is an 8-channel high speed 10 bit A/D converter which uses a Two Step Flash algorithm to achieve through-put rates of 200kHz. The converter features an 8-channel CMOS analog multiplexer with random channel addressing. A unique switched capacitor technique allows a new input voltage to be sampled while a conversion is taking place.

Internal high speed CMOS buffers at both the analog and reference inputs simplifies interface requirements.

A Track and Hold amplifier is included on the chip, consisting of two high speed amplifiers and an internal hold capacitor, reducing external circuitry.

Microprocessor bus interfacing is simplified by the use of standard Chip Select, Read, and Write control signals. The digital three-state outputs are byte organized for bus interface to 8 or 16 bit systems. An Out-of-Range pin, together with the MSB bit, can be used to indicate an under or over-range condition.

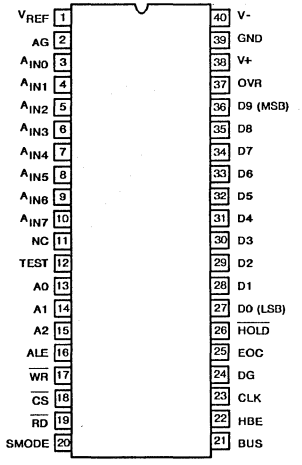
The HI-7153 operates with ±5V supplies. Only a single +2.5V reference is required to provide a bipolar input range from -2.5V to +2.5V.

Ordering Information

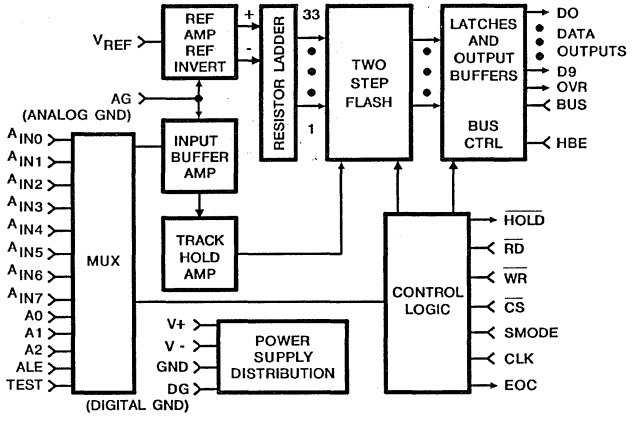
PART NO.	LINEARITY (MAX. ILE)	TEMPERATURE RANGE	PACKAGE
HI3-7153J-5	±1.0 LSB	0°C to +75°C	40 Pin Plastic DIP
HI3-7153A-9	±1.0 LSB	-40°C to +85°C	40 Pin Plastic DIP
HI1-7153S-2	±1.0 LSB	-55°C to +125°C	40 Pin Ceramic DIP
HI1-7153S/883	±1.0 LSB	-55°C to +125°C	40 Pin Ceramic DIP

Pinout

HI-7153
TOP VIEW



Functional Diagram



File Number 2787.2

HARRIS SEMICONDUCTOR

ICL7112
12-Bit High-Speed CMOS μP-Compatible A/D Converter

GENERAL DESCRIPTION

The ICL7112 is a monolithic 12-bit resolution, fast successive approximation A/D converter. It uses thin film resistors and CMOS circuitry combined with an on-chip PROM calibration table to achieve 12-bit linearity without laser trimming. Special design techniques used in the DAC and comparator result in high speed operation, while the fully static silicon-gate CMOS circuitry keeps the power dissipation very low.

Microprocessor bus interfacing is eased by the use of standard memory WRite and ReaD cycle timing and control signals, combined with Chip Select and Address pins. The digital output pins are byte-organized and three-state gated for bus interface to 8- and 16-bit systems.

The ICL7112 provides separate Analog and Digital grounds for increased system accuracy. Operating with ±5V supplies, the ICL7112 accepts 0V to +10V input with a −10V reference or 0V to −10V input with a +10V reference.

FEATURES

- **12-Bit Resolution and Accuracy**
- **No Missing Codes**
- **Microprocessor Compatible Byte-Organized Buffered Outputs**
- **Auto-Zeroed Comparator for Low Offset Voltage**
- **Low Linearity and Gain Errors**
- **Low Power Consumption (60 mW)**
- **No Gain or Offset Adjustment Necessary**
- **Provides 3% Useable Overrange**
- **Fast Conversion (40 μsec.)**

ORDERING INFORMATION

Part Number	Resolution with No Missing Codes	Temperature Range	Package
ICL7112JCDL	11 Bits	0°C to +70°C	40 Pin Ceramic
ICL7112KCDL	12 Bits	0°C to +70°C	40 Pin Ceramic
ICL7112LCDL	12 Bits*	0°C to +70°C	40 Pin Ceramic
ICL7112JIDL	11 Bits	−25°C to +85°C	40 Pin Ceramic
ICL7112KIDL	12 Bits	−25°C to +85°C	40 Pin Ceramic
ICL7112LIDL	12 Bits*	−25°C to +85°C	40 Pin Ceramic
ICL7112JMDL	11 Bits	−55°C to +125°C	40 Pin Ceramic
ICL7112KMDL	12 Bits	−55°C to +125°C	40 Pin Ceramic
ICL7112LMDL	12 Bits*	−55°C to +125°C	40 Pin Ceramic

*Over Operating Temperature Range

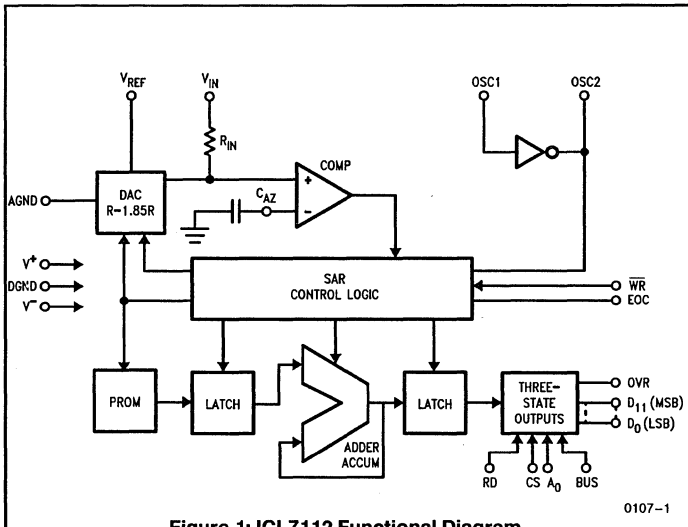


Figure 1: ICL7112 Functional Diagram

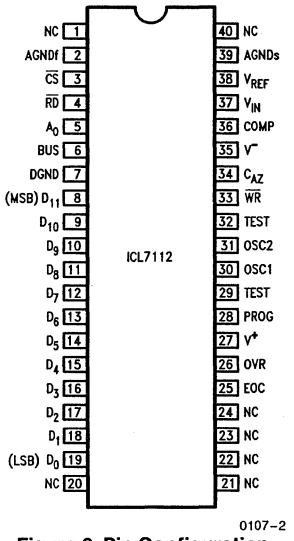


Figure 2: Pin Configuration (Outline Dwg. DL)

301657-002

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V^+ to DGND ..... −0.3V to +6.5V
Supply Voltage V^- to DGND ..... +0.3V to −6.5V
V_{REF}, V_{IN} to DGND ..... ±25V
AGND to DGND ..... +1V to −1V
V_{REF}, V_{IN}, AGND Current ..... 25 mA
Digital I/O Pin Voltages ..... −0.3V to (V^+ +0.3V)
PROG to DGND Voltage ..... V^- to (V^+ +0.3)

Note 1: All voltages with respect to DGND, unless otherwise noted.

2: Assumes all leads soldered or welded to printed circuit board.

Operating Temperature
ICL7112XCXX ..... 0°C to +70°C
ICL7112XIXX ..... −25°C to +70°C
ICL7112XMXX ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Power Dissipation (Note 2) ..... 500 mW
derate above 70°C @10 mW/°C
Lead Temperature (soldering, 10 sec.) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

Test Conditions: V^+ = +5V, V^- = −5V, V_{REF} = −10.0V, T_A = +25°C, f_{clk} = 500 kHz unless otherwise noted.

Symbol	Parameter	Test Conditions			J			K			L			Units
					Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Accuracy														
RES	Resolution						12							Bits
RES(NMC)	Resolution with No Missing Codes	Notes 1, 2, 3		Rm Tmin–Tmax	11 10			12 11			12 12			Bits
I_{LE}	Integral Linearity Error	Notes 1, 2		Rm Tmin–Tmax			±0.024 ±0.030			±0.012 ±0.020			±0.012 ±0.020	%FSR
FSE	Unadjusted Full Scale Error	Adjustable to Zero	C	Rm Tmin–Tmax			±0.10 ±0.12			±0.08 ±0.10			±0.08 ±0.10	%FSR
			I	Rm Tmin–Tmax			±0.10 ±0.13			±0.08 ±0.11			±0.08 ±0.11	
			M	Rm Tmin–Tmax			±0.10 ±0.14			±0.08 ±0.12			±0.08 ±0.12	
ZE	Zero Error	Notes 1, 2		Rm Tmin–Tmax			±1 ±1.5			±1 ±1.5			±1 ±1.5	LSB
Analog Input														
V_{IN}	Analog Input Range				0		10.3	0		10.3	0		10.3	V
R_{IN}	Input Resistance	Notes 2, 5			4		9	4		9	4		9	KΩ
$T_C(R_{IN})$	Temperature Coefficient of R_{IN}			Tmin–Tmax		−300			−300			−300		ppm/°C
Reference Input														
V_{REF}	Analog Reference					−10.0			−10.0			−10.0		V
R_{REF}	Reference Resistance					5			5			5		KΩ
Power Supply Sensitivity														
PSRR	Power Supply Rejection Ratio	V^+, V^- = 4.5V–5.5V		Rm Tmin–Tmax		±0.5	±1 ±2		±0.5	±1 ±2		±0.5	±1 ±2	LSB

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5V$, $V^- = -5V$, $V_{REF} = -10.0V$, $T_A = +25°C$, $f_{clk} = 500$ kHz unless otherwise noted. (Continued)

Symbol	Parameter	Test Conditions	J			K			L			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Logic Input												
V_{IL}	Low State Input Voltage	Tmin–Tmax			0.8			0.8			0.8	V
V_{IH}	High State Input Voltage	Tmin–Tmax	2.4			2.4			2.4			V
I_{LIH}	Logic Input Current	$0 < V_{IN} < V^+$		1	10		1	10		1	10	µA
C_{IN}	Logic Input Capacitance			15			15			15		pF
Logic Output												
V_{OL}	Low State Output Voltage	$I_{OUT} = 1.6$ mA Tmin–Tmax			0.4			0.4			0.4	V
V_{OH}	High State Output Voltage	$I_{OUT} = -200$ µA Tmin–Tmax	2.8			2.8			2.8			V
I_{OX}	Three-State Output Current	$0 < V_{OUT} < V^+$		1			1			1		µA
C_{OUT}	Logic Output Capacitance	Three-State		15			15			15		pF
Power Requirements												
V_{SUPPLY}	Supply Voltage Range	Functional Operation Only	±4.5		±6.0	±4.5		±6.0	±4.5		±6.0	V
I_{SUPPLY}	Supply Current, I+, I–	Rm Tmin–Tmax		2	4 6		2	4 6		2	4 6	mA

NOTES 1: Full scale range (FSR) is 10V (reference adjusted).
2: Assume all leads are soldered or welded to printed circuit board.
3: "J" and "K" versions not production tested. Guaranteed by Integral Linearity Dest.
4: Typical values are not tested, for reference only.
5: Not production tested. Guaranteed by design.

4

NOTE: All typical values have been characterized but are not tested.

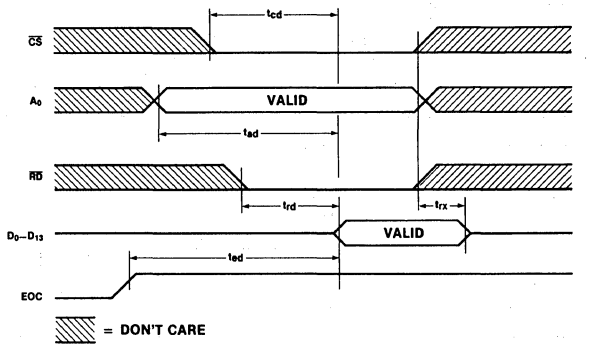


Figure 3: Read Cycle Timing

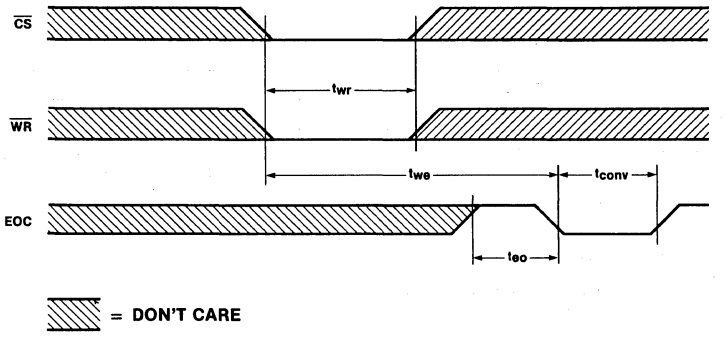


Figure 4: Write Cycle Timing

AC ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5.0V$, $V^- = -5.0V$, $T_A = +25°C$, $f_{clk} = 500kHz$ unless otherwise noted. Data derived from extensive characterization testing. Parameters are not production tested.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
READ CYCLE TIMING						
t_{cd}	Prop. Delay $\overline{CS}$ to Data	$\overline{RD}$ Low, A_0 Valid			200	ns
t_{ad}	Prop. Delay A_0 to Data	$\overline{CS}$ Low, $\overline{RD}$ Low			200	
t_{rd}	Prop. Delay $\overline{RD}$ to Data	$\overline{CS}$ Low, A_0 Valid			200	
t_{rx}	Prop. Delay Data to Three State				150	
t_{ed}	Prop. Delay EOC High to Data				200	
WRITE CYCLE TIMING						
t_{wr}	$\overline{WR}$ Low Time		150			ns
t_{we}	Prop. Delay $\overline{WR}$ Low to EOC Low	Wait Mode	1		2	
t_{eo}	EOC High Time	Free-Run Mode	0.5		1.5	1/fclk
t_{conv}	Conversion Time				20	
f_{clk}	Clock Frequency Range	Functional Operation Only		500		kHz

NOTE: All typical values have been characterized but are not tested.

TABLE 1: PIN DESCRIPTIONS

PIN	NAME	FUNCTION	
1		No connection	
2	$AGND_f$	FORCE input for Analog Ground	
3	$\overline{CS}$	Chip Select enables reading and writing (active low)	
4	$\overline{RD}$	$\overline{ReaD}$ (active low)	
5	A_0	Byte select (low = $D_0 - D_7$, high = $D_8 - D_{11}$, OVR)	
6	BUS	Bus select (low = outputs enabled by A_0, high = all outputs enabled together)	
7	DGND	Digital GrouND return	
8	D_{11}	Bit 11 (most significant bit)	High Byte
9	D_{10}	Bit 10	
10	D_9	Bit 9	
11	D_8	Bit 8	
12	D_7	Bit 7 Output	
13	D_6	Bit 6 Data	
14	D_5	Bit 5 Bits	Low Byte
15	D_4	Bit 4 (High = True)	
16	D_3	Bit 3	
17	D_2	Bit 2	
18	D_1	Bit 1	
19	D_0	Bit 0 (least significant bit)	
20		No Connection	
21		No Connection	
22		No Connection	
23		No Connection	
24		No Connection	
25	EOC	End Of Conversion flag (low = busy, high = conversion complete)	
26	OVR	OVerRange flag (valid at end of conversion when output code exceeds full-scale, three-state output enabled with high byte)	
27	V^+	Positive power supply input	
28	PROG	Used for programming only. Must tie to V^+ for normal operation	
29	TEST	Used for programming only. Must tie to V^+ for normal operation	
30	OSC1	Oscillator inverter input	
31	OSC2	Oscillator inverter output	
32	TEST	Must tie to V^+ for normal operation	
33	$\overline{WR}$	$\overline{WR}$ite pulse input (low starts new conversion)	
34	C_{AZ}	Auto-zero capacitor connection*	
35	V^-	Negative power supply input	
36	COMP	Used in test, tie to V^-	
37	V_{IN}	SENSE line for input voltage	
38	V_{REF}	SENSE line for reference input	
39	$AGND_s$	SENSE line for analog ground	
40		No connection	

***NOTE:** The voltage on C_{AZ} is driven: Never connect directly to ground.

TABLE 2: I/O CONTROL

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	A_0	BUS	FUNCTION
0	0	x	x	x	Initiates a Conversion
1	x	x	x	x	Disables all Chip Commands
0	x	0	0	0	Low Byte is Enabled
0	x	0	1	0	High Byte is Enabled
0	x	0	x	1	Low and High Bytes Enabled Together
x	x	1	x	x	Disables Outputs (High-Impedance)

TABLE 3: TRANSFER FUNCTION

INPUT VOLTAGE	EXPECTED OUTPUT CODE			
$V_{REF} = -10.0V$	OVR	MSB		LSB
0	0	0	0000000000	0
+0.00244	0	0	0000000000	1
+0.30029	0	0	0000111101	1
+4.99756	0	0	1111111111	1
+5.00000	0	1	0000000000	0
+9.99512	0	1	1111111111	0
+9.99756	0	1	1111111111	1
+10.00000	1	0	0000000000	0
+10.00244	1	0	0000000000	1
+10.29000	1	0	0000111101	1

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

The ICL7112 is basically a successive approximation A/D converter with an internal structure much more complex than a standard SAR-type converter. Figure 1 shows the functional diagram of the ICL7112 12-bit A/D converter. The additional circuitry incorporated into the ICL7112 is used to perform error correction and to maintain the operating speed in the 40μs range.

The internal DAC of the ICL7112 is designed around a radix of 1.85 rather than the traditional 2.00. This radix gives each bit of the DAC a weight of approximately 54% of the previous bit. The result is a useable range that extends to 3% beyond the full-scale input of the A/D. The actual value of each bit is measured and stored in the on-chip PROM. The absolute value of each bit weight then becomes relatively unimportant because of the error correction action of the ICL7112.

The output of the high-speed auto-zeroed comparator is fed to the data input of a successive approximation register (SAR). This register is uniquely designed for the ICL7112 in that it tests bit pairs instead of individual bits in the manner of a standard SAR. At the beginning of the conversion cycle, the SAR turns on the MSB (D_{11}) and the MSB-4 bit (D_7). The sequence continues for each bit pair, B_x and B_{x-4}, until only the four LSBs remain. The sequence concludes by testing the four LSBs individually.

The SAR output is fed to the DAC register and to the preprogrammed PROM where it acts as PROM address. PROM data is fed to a full-adder/accumulator where the decoded results from each successive phase of the conversion are summed with the previous results. After 20 clock cycles, the accumulator contains the final binary data which is latched and sent to the three-state output buffers. The accuracy of the A/D converter depends primarily upon the accuracy of the data that has been programmed into the PROM during the final test portion of the manufacturing process.

The error correcting algorithm built into the ICL7112 reduces the initial accuracy requirements of the DAC. The overlap in the testing of bit pairs reduces the accuracy requirements on the comparator which has been optimized for speed. Since the comparator is auto-zeroed, no external adjustment is required to get ZERO code for ZERO input voltage.

Twenty clock cycles are required for the complete 12-bit conversion. The auto-zero circuitry associated with the comparator is employed during the last three clock cycles of the conversion to cancel the effect of offset voltage. Also during this time, the SAR and accumulator are reset in preparation for the start of the next conversion.

The overflow output of the full-adder is also the OVer-Range (OVR) output of the ICL7112. Unlike standard SAR-type A/D converters, the ICL7112 has the capability of providing valid useable data for inputs that exceed the full-scale range by as much as 3%.

OPTIMIZING SYSTEM PERFORMANCE

When using A/D converters with 12 or more bits of resolution, special attention must be paid to grounding and the elimination of potential ground loops. A ground loop can be formed by allowing the return current from the ICL7112's DAC to flow through traces that are common to other analog circuitry. If care is not taken, this current can generate small unwanted voltages that add to or detract from the reference or input voltages of the A/D converter.

Figures 5 and 6 show two different grounding techniques. Although the difference between the two circuits may not be readily apparent, the circuit of Figure 5 is very likely to have significant ground loop errors which the circuit of Figure 6 avoids. In Figure 5, the supply currents for analog ground, digital ground, and the reference voltage all flow through a lead common to the input. This will generate a DC offset voltage due to the currents flowing in the resistance of the common lead. This offset voltage will vary with the input voltage and with the digital output. Even the auto-zero loop of the ICL7112 cannot remove this error.

Figure 6 shows a much better arrangement. The ground and reference currents do not flow through the input common lead, eliminating any error voltages. Note that the supply currents and any other analog system currents must also be returned carefully to analog ground. The clamp diodes will protect the ICL7112 against signals which could result from separate analog and digital grounds. The absolute maximum voltage rating between AGND and DGND is $\pm$1.0V. The two inverse-parallel diodes clamp this voltage to less than $\pm$0.7V.

INPUT WARNING

As with any CMOS integrated circuit, no input voltages should be applied to the ICL7112 until the $\pm$5V power supplies have stabilized.

INTERFACING TO DIGITAL SYSTEMS

The ICL7112 provides three-state data output buffers, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and bus select inputs (A_0 and BUS) for interfacing to a wide variety of microcomputers and digital systems. The I/O Control Truth Table shows the functions of the digital control lines. The BUS select and A_0 lines are provided to enable the output data onto either 8-bit or 16-bit data buses. A conversion is initiated by a $\overline{WR}$ pulse (pin 33) when $\overline{CS}$ (pin 3) is low. Data is enabled on the bus when the chip is selected and $\overline{RD}$ (pin 4) is low.

Figure 7 illustrates a typical interface to an 8-bit microcomputer. The "Start and Wait" operation requires the fewest external components and is initiated by a low level on the $\overline{WR}$ input to the ICL7112 after the I/O or memory-mapped address decoder has brought the $\overline{CS}$ input low. After executing a delay or utility routine for a period of time greater than the conversion time of the ICL7112, the processor issues two consecutive bus addresses to read output data into two bytes of memory. A low level on A_0 enables the LSBs and a high level enables the MSBs.

NOTE: All typical values have been characterized but are not tested.

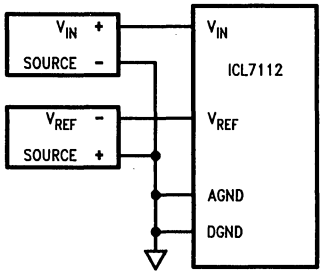


Figure 5: Improper Grounding Technique Will Cause Ground Loop Errors

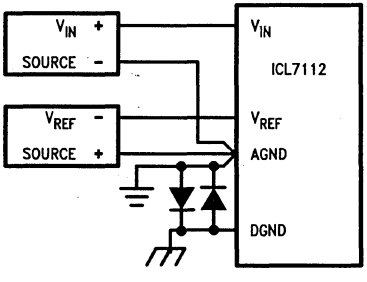
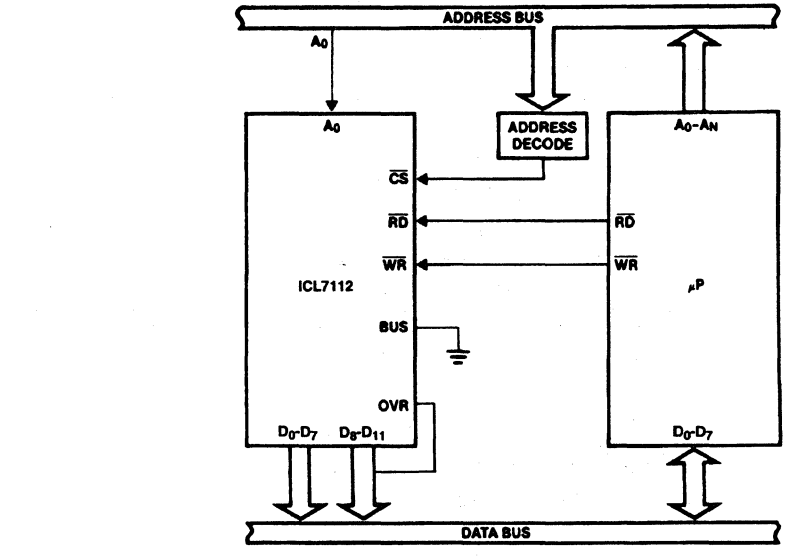


Figure 6: Recommended Grounding Technique to Eliminate Ground Loop Errors

NOTE: All typical values have been characterized but are not tested.



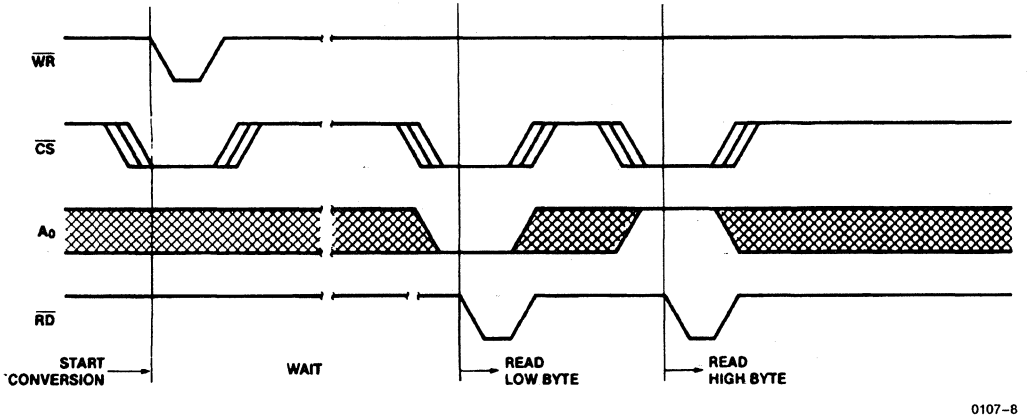


Figure 7: "Start and Wait" Operation

NOTE: All typical values have been characterized but are not tested.

By adding a three-state buffer and two control gates, the End-of-Conversion (EOC) output can be used to control a "Start and Poll" interface (Figure 8). In this mode, the A_0 and $\overline{CS}$ lines connect the EOC output to the data bus along with the most significant byte of data. After pulsing the $\overline{WR}$ line to initiate a conversion, the microprocessor continually reads the most significant byte until it detects a high level on the EOC bit. The "Start and Poll" interface increases data throughput compared with the "Start and Wait" method by eliminating delays between the conversion termination and the microprocessor read operation.

Other interface configurations can be used to increase data throughput without monopolizing the microprocessor during waiting or polling operations by using the EOC line as an interrupt generator as shown in Figure 9. After the conversion cycle is initiated, the microprocessor can continue to execute routines that are independent of the A/D converter until the converter's output register actually holds valid data. For fastest data throughput, the ICL7112 can be connected directly to the data bus but controlled by way of a Direct Memory Access (DMA) controller as shown in Figure 10.

APPLICATIONS

Figure 11 shows a typical application of the ICL7112 12-bit A/D converter. A bipolar input voltage range of +10V to −10V is the result of using the current through R_2 to force a ½ scale offset on the input amplifier (A_1). The output of A_1 swings from 0V to −10V. The overall gain of the A/D is varied by adjusting the 100kΩ trim resistor, R_5. Since the ICL7112 is automatically zeroed every conversion, the system gain and offset stability will be superb as long as a reference with a tempco of 1ppm/°C and stable external resistors are used.

It is important to note that since the 7112's DAC current flows in A_1, the amplifier should be a wideband (GBW>20MHz) type to minimize errors.

The clock for the ICL7112 is taken from whatever system clock is available and divided down to the level for a conversion time of 40 μs. Output data is controlled by the BUS and A_0 inputs. Here they are set for 8-bit bus operation with BUS grounded and A_0 under the control of the address decode section of the external system.

Because the ICL7112's internal accumulator generates accurate output data for input signals as much as 3% greater than full-scale, and because the converter's OVR output flags overrange inputs, a simple microprocessor routine can be employed to precisely measure and correct for system gain and offset errors. Figure 12 shows a typical data acquisition system that uses a 10.0V reference, input signal multiplexer, and input signal Track/Hold amplifier. Two of the multiplexer's input channels are dedicated to sampling the system analog ground and reference voltage. Here, as in Figure 11, bipolar operation is accommodated by an offset resistor between the reference voltage and the summing junction of A_1. A flip-flop in IC_3 sets IC_2's Track/Hold input after the microprocessor has initiated a WR command, and resets when EOC goes high at the end of the conversion.

The first step in the system calibration routine is to select the multiplexer channel that is connected to system analog ground and initiate a conversion cycle for the ICL7112. The results represent the system offset error which comes from the sum of the offsets from IC_1, IC_2, and A_1. Next the channel connected to the reference voltage is selected and measured. These results, minus the system offset error, represent the system full-scale range. A gain error correction factor can be derived from this data. Since the ICL7112 provides valid data for inputs that exceed full-scale by as much as 3%, the OVR output can be thought of as a valid 13th data bit. Whenever the OVR bit is high, however, the total 12-bit result should be checked to insure that it falls within 100% and 103% of full-scale. Data beyond 103% of full-scale should be discarded.

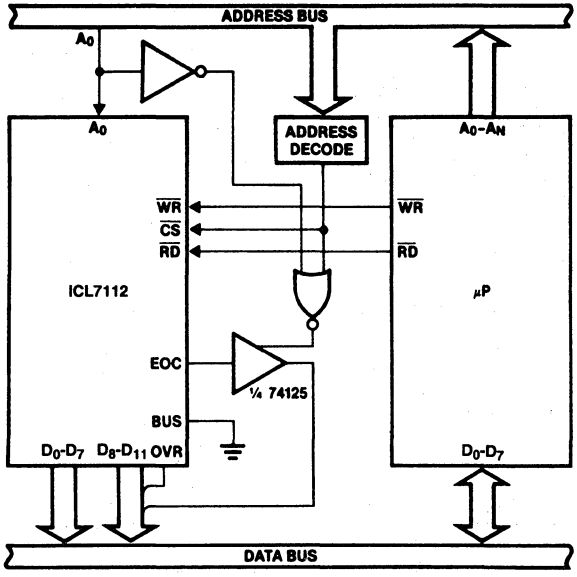
CLOCK CONSIDERATIONS

The ICL7112 provides an internal inverter which is brought out to pins OSC1 and OSC2, for crystal or ceramic resonator oscillator operation. The clock frequency is calculated from:

$$f_{CLK} = \frac{20}{t_{conv}}$$

NOTE: All typical values have been characterized but are not tested.

(A)



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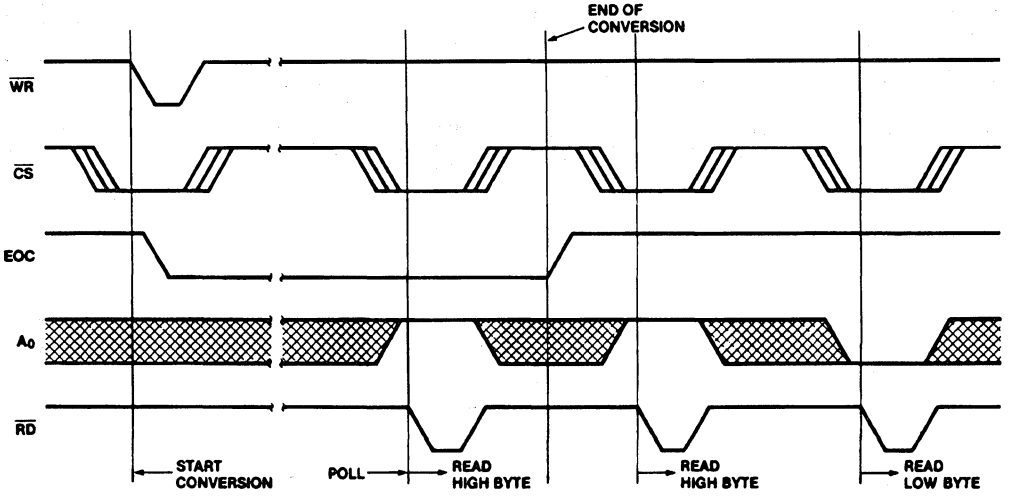
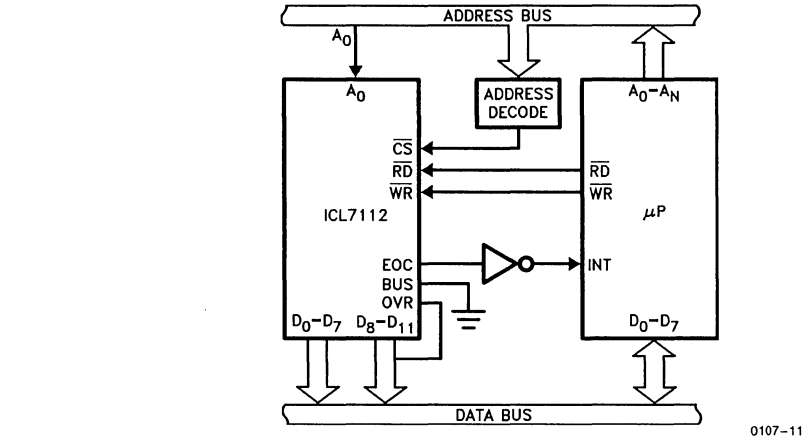
(B)



0107-10

Figure 8: "Start and Poll" Operation

NOTE: All typical values have been characterized but are not tested.



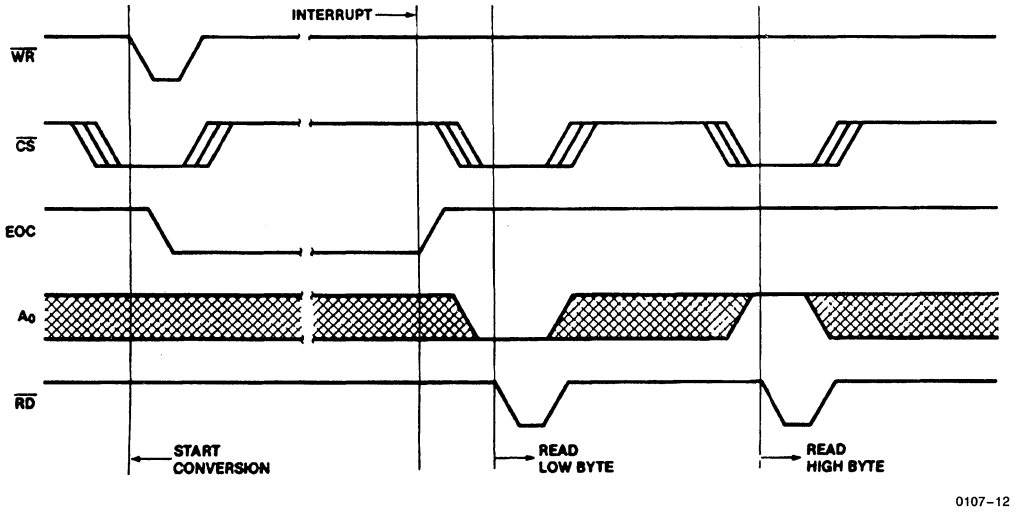
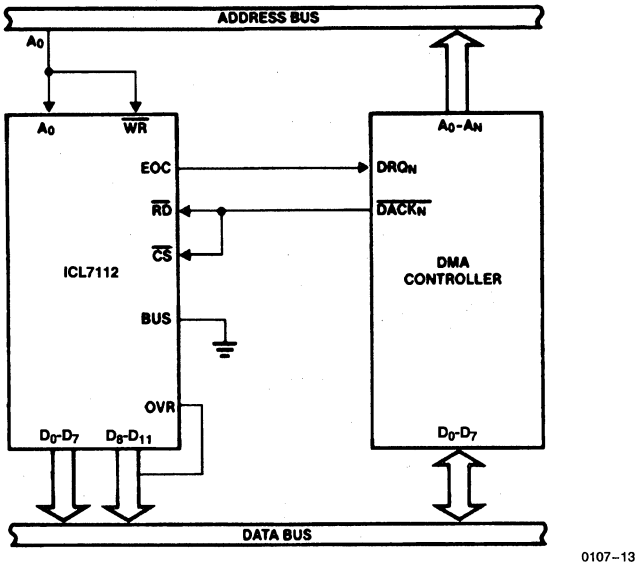


Figure 9: Using EOC as an Interrupt

NOTE: All typical values have been characterized but are not tested.



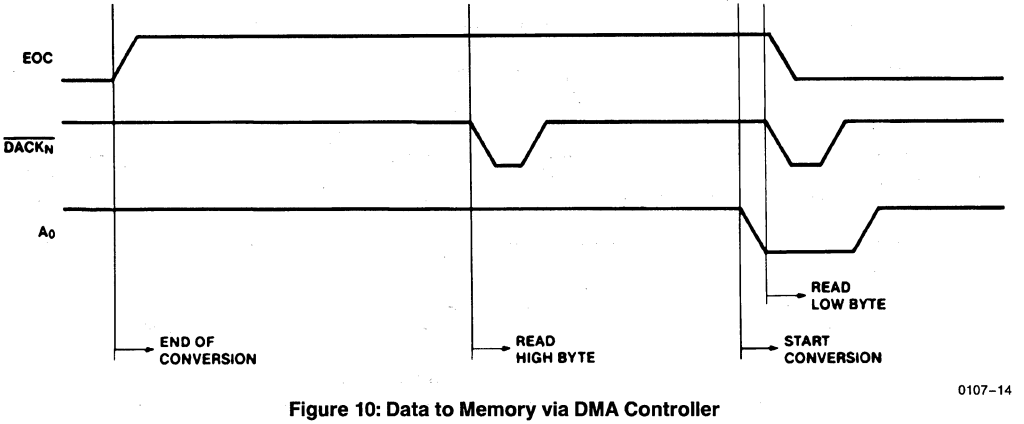


Figure 10: Data to Memory via DMA Controller

NOTE: All typical values have been characterized but are not tested.

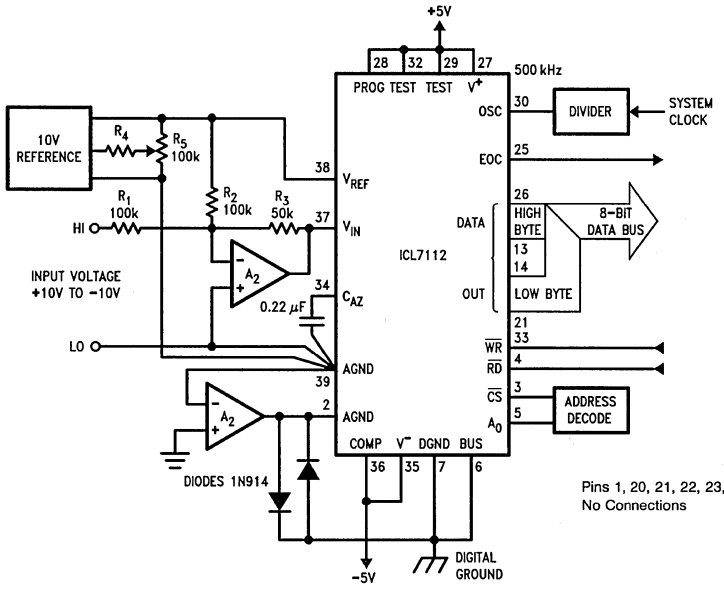


Figure 11: Typical Application with Bipolar Input Range, Forced Ground, and 10 Volt Ultra-Stable Reference

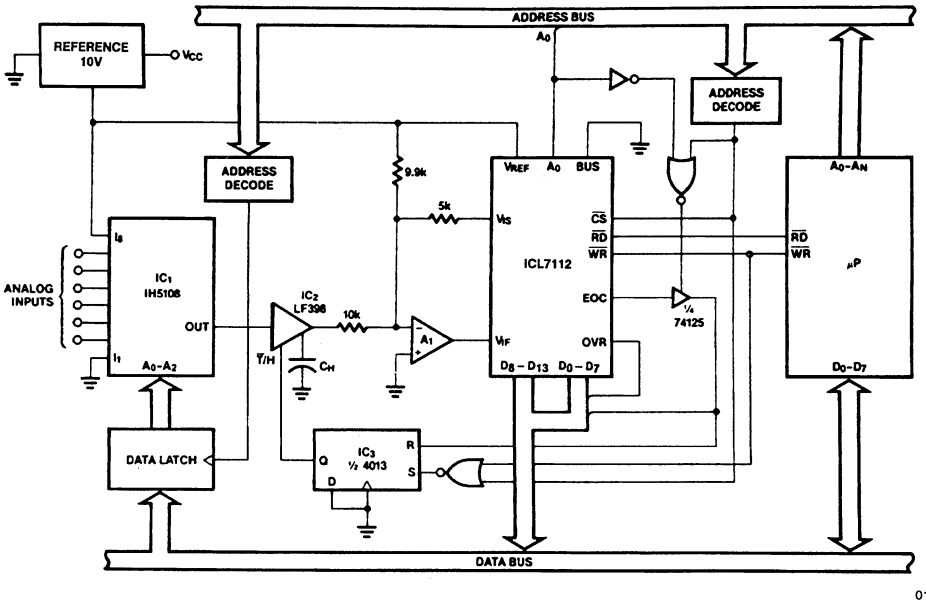


Figure 12: Multi-Channel Data Acquisition System with Zero and Reference Lines Brought to Multiplexer for System Gain and Offset Error Correction

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICL7115
14-Bit High-Speed CMOS μP-Compatible A/D Converter

GENERAL DESCRIPTION

The ICL7115 is the first monolithic 14-bit resolution, fast successive approximation A/D converter. It uses thin film resistors and CMOS circuitry combined with an on-chip PROM calibration table to achieve ±0.009% linearity without laser trimming. Special design techniques used in the DAC and comparator result in high speed operation, while the fully static silicon-gate CMOS circuitry keeps the power dissipation very low.

Microprocessor bus interfacing is made easy by the use of standard WRite and ReaD cycle timing and control signals, combined with Chip Select and Address pins. The digital output pins are byte-organized and three-state gated for bus interface to 8 and 16-bit systems.

The ICL7115 provides separate Analog and Digital grounds. Analog ground, voltage reference and input voltage pins are separated into force and sense lines for increased system accuracy. Operating with ±5V supplies, the ICL7115 accepts 0V to +10V input with a −10V reference or 0V to −10V input with a +10V reference.

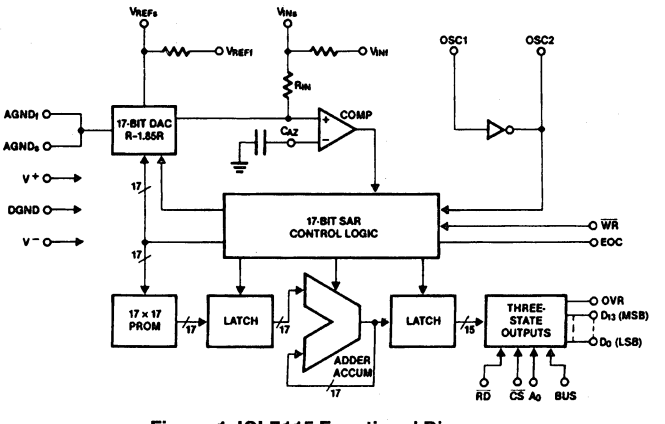
FEATURES

- **14-Bit Resolution (LSB = 610 μV)**
- **No Missing Codes to 14 Bits**
- **Microprocessor Compatible Byte-Organized Buffered Outputs**
- **Fast Conversion (40μs)**
- **Auto-Zeroed Comparator for Low Offset Voltage**
- **Low Linearity and Gain Error**
- **Low Power Consumption (60mW)**
- **No Gain or Offset Adjustment Necessary**
- **Provides 3% Useable Overrange**
- **FORCE/SENSE and Separate Digital and Analog Ground Pins for Increased System Accuracy**

ORDERING INFORMATION

Part Number	Resolution(1) with No Missing Codes	Temp. Range	Package
ICL7115JCDL	12 Bits	0°C to +70°C	40 Pin Ceramic
ICL7115KCDL	13 Bits	0°C to +70°C	40 Pin Ceramic
ICL7115LCDL	14 Bits	0°C to +70°C	40 Pin Ceramic
ICL7115JIDL	12 Bits	−25°C to +85°C	40 Pin Ceramic
ICL7115KIDL	13 Bits	−25°C to +85°C	40 Pin Ceramic
ICL7115LIDL	14 Bits	−25°C to +85°C	40 Pin Ceramic
ICL7115JMDL	12 Bits	−55°C to +125°C	40 Pin Ceramic
ICL7115KMDL	13 Bits	−55°C to +125°C	40 Pin Ceramic
ICL7115LMDL	14 Bits	−55°C to +125°C	40 Pin Ceramic
ICL7115JMLL	12 Bits	−55°C to +125°C	40 Pin LCC
ICL7115KMLL	13 Bits	−55°C to +125°C	40 Pin LCC

NOTE 1: Specified at 25°C.



0337-2

Figure 1: ICL7115 Functional Diagram

301659-005

NOTE: All typical values have been characterized but are not tested.

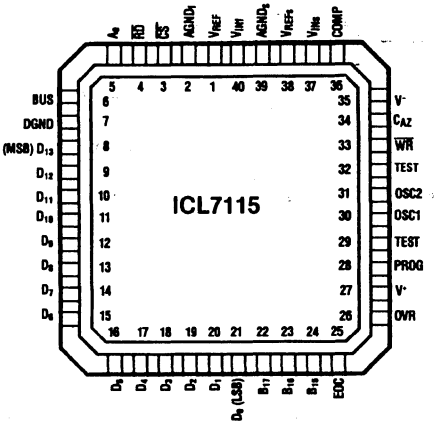
ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage V^+ to DGND ..... −0.3V to +6.5V
Supply Voltage V^- to DGND ..... +0.3V to −6.5V
V_{REFs}, V_{REFf}, V_{INs}, V_{INf} to DGND ..... +25V to −25V
$AGND_s$, $AGND_f$ to DGND ..... +1V to −1V
Current in FORCE and SENSE Lines 25mA
Digital I/O Pin Voltages ..... −0.3V to V^+ +0.3V
PROG to DGND Voltage ..... V^- to V^+ +0.3V

Operating Temperature Range
ICL7115XCXX ..... 0°C to +70°C
ICL7115XIXX ..... −25°C to +85°C
ICL7115XMXX ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation 500mW
derate above 70°C @ 10mW/°C
Lead Temperature (Soldering, 10sec) ..... 300°C

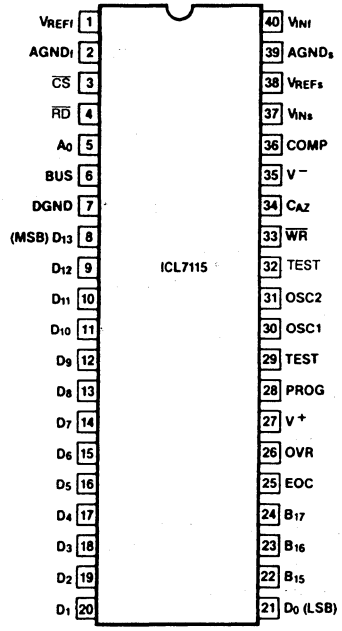
NOTE 1: All voltages with respect to DGND, unless otherwise noted.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*



0337-17

(Outline DWG LL)



0337-1

(Outline DWG DL)

Figure 2: Pin Configuration

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5.0V$, $V^- = -5.0V$, $V_{ref} = -10.0V$, $T_A = +25°C$, $F_{clk} = 500kHz$ unless otherwise noted.

Symbol	Parameter	Test Conditions		J			K			L			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ACCURACY													
RES	Resolution					14							Bits
RES(NMC)	Resolution with No Missing Codes	(Notes 1, 2, 3)	Rm	12			13			14			Bits
			Tmin–Tmax	11			12			13			
I_{LE}	Integral Linearity Error	(Notes 1, 2)	Rm			±0.018			±0.012			±0.009	%FSR
			Tmin–Tmax			±0.024			±0.020			±0.018	
FSE	Unadjusted Full Scale Error	Adjustable to Zero	C Rm			±0.10			±0.08			±0.08	%FSR
			C Tmin–Tmax			±0.12			±0.10			±0.10	
			I Rm			±0.10			±0.08			±0.08	
			I Tmin–Tmax			±0.13			±0.11			±0.11	
			M Rm			±0.10			±0.08			±0.08	
			M Tmin–Tmax			±0.14			±0.12			±0.12	
ZE	Zero Error	(Notes 1,2)	Rm			±1			±1			±1	LSB
			Tmin–Tmax			±1.5			±1.5			±1.5	
ANALOG INPUT													
V_{IN}	Analog Input Range			0		10.3	0		10.3	0		10.3	V
R_{IN}	Input Resistance	(Notes 2, 3)		4		9	4		9	4		9	kΩ
$T_C(R_{IN})$	Temperature Coefficient of R_{IN}		Tmin–Tmax		−300			−300			−300		ppm/°C
REFERENCE INPUT													
V_{REF}	Analog Reference				−10.0			−10.0			−10.0		V
R_{REF}	Reference Resistance				5			5			5		kΩ
POWER SUPPLY SENSITIVITY													
PSRR	Power Supply Rejection Ratio	V^+, V = 4.5V–5.5V	Rm		±0.5	±1		±0.5	±1		±0.5	±1	LSB
			Tmin–Tmax			±2			±2			±2	
LOGIC INPUT													
V_{IL}	Low State Input Voltage		Tmin–Tmax			0.8			0.8			0.8	V
V_{IH}	High State Input Voltage		Tmin–Tmax	2.4			2.4			2.4			V
I_{LIH}	Logic Input Current	$0 < V_{IN} < V^+$			1	10		1	10		1	10	μA
C_{IN}	Logic Input Capacitance				15			15			15		pF

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

Test Conditions: $V^+ = +5.0V$, $V^- = -5.0V$, $V_{ref} = -10.0V$, $T_A = +25°C$, $F_{clk} = 500kHz$ unless otherwise noted.
(Continued)

Symbol	Parameter	Test Conditions	J			K			L			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
LOGIC OUTPUT												
V_{OL}	Low State Output Voltage	$I_{OUT} = 1.6$ mA Tmin–Tmax			0.4			0.4			0.4	V
V_{OH}	High State Output Voltage	$I_{OUT} = -200\ \mu A$ Tmin–Tmax	2.8			2.8			2.8			V
I_{OX}	Three-State Output Current	$0 < V_{OUT} < V^+$		1			1			1		µA
C_{OUT}	Logic Output Capacitance	Three-State		15			15			15		pF
POWER REQUIREMENTS												
V_{SUPPLY}	Supply Voltage Range	Functional Operation Only	±4.5		±6.0	±4.5		±6.0		±4.5	±6.0	V
I_{SUPPLY}	Supply Current I+, I−	Rm Tmin–Tmax		2	4 6		2	4 6		2	4 6	mA

NOTE 1: Full-scale range (FSR) is 10V (reference adjusted).
2: Assume all leads soldered or welded to printed circuit board.
3: Guaranteed, not tested.
4: Typical values are not tested, for reference only.

4

NOTE: All typical values have been characterized but are not tested.

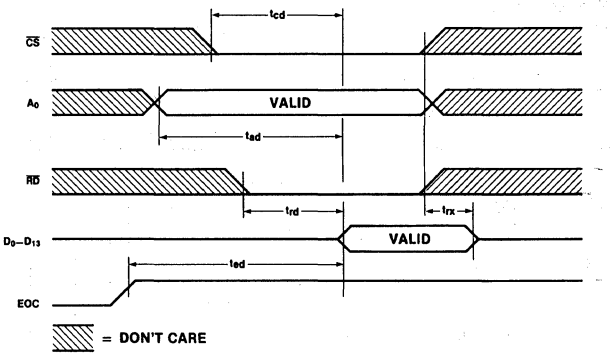


Figure 3: Read Cycle Timing

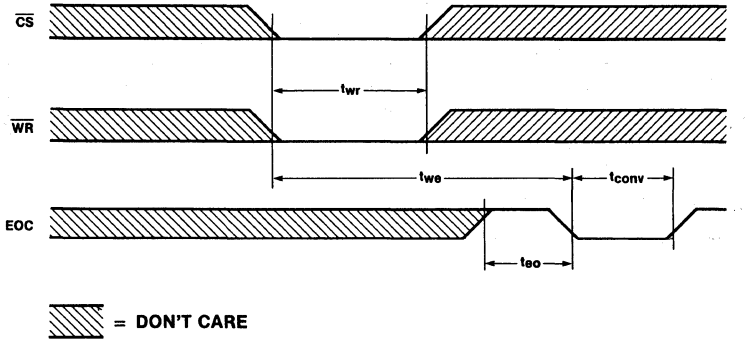


Figure 4: Write Cycle Timing

AC ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: $V^+ = +5.0V$, $V^- = -5.0V$, $V_{ref} = -10.0V$, $F_{clk} = 500kHz$, $T_A = +25°C$ unless otherwise noted. Data derived from extensive characterization testing. Parameters are not production tested.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
READ CYCLE TIMING						
t_{cd}	Prop. Delay $\overline{CS}$ to Data	$\overline{RD}$ Low, A_0 Valid			200	
t_{ad}	Prop. Delay A_0 to Data	$\overline{CS}$ Low, $\overline{RD}$ Low			200	
t_{rd}	Prop. Delay $\overline{RD}$ to Data	$\overline{CS}$ Low, A_0 Valid			200	ns
t_{rx}	Prop. Delay Data to Three State				150	
t_{ed}	Prop. Delay EOC High to Data				200	
WRITE CYCLE TIMING						
t_{wr}	$\overline{WR}$ Low Time		150			ns
t_{we}	Prop. Delay $\overline{WR}$ Low to EOC Low	Wait Mode	1		2	
t_{eo}	EOC High Time	Free-Run Mode	0.5		1.5	1/fclk
t_{conv}	Conversion Time				20	
f_{clk}	Clock Frequency	Functional Operation Only		500		kHz

NOTE: All typical values have been characterized but are not tested.

TABLE 1: PIN DESCRIPTIONS

PIN	NAME	FUNCTION	
1	V_{REFf}	FORCE line for reference input.	
2	$AGND_f$	FORCE input for analog ground	
3	$\overline{CS}$	Chip Select enables reading and writing (active low)	
4	$\overline{RD}$	$\overline{ReaD}$ (active low)	
5	A_0	Byte select (low = $D_0 - D_7$, high = $D_8 - D_{13}$, OVR)	
6	BUS	Bus select (low = outputs enabled by A_0, high = all outputs enabled together)	
7	DGND	Digital GrouND return	
8	D_{13}	Bit 13 (most significant bit)	High Byte
9	D_{12}	Bit 12	
10	D_{11}	Bit 11	
11	D_{10}	Bit 10	
12	D_9	Bit 9 Output	
13	D_8	Bit 8 Data	
14	D_7	Bit 7 Bits	Low Byte
15	D_6	Bit 6 (High = True)	
16	D_5	Bit 5	
17	D_4	Bit 4	
18	D_3	Bit 3	
19	D_2	Bit 2	
20	D_1	Bit 1	
21	D_0	Bit 0 (least significant bit)	
22	B_{15}	Used for programming only (Do not connect—Leave Open)	
23	B_{16}		
24	B_{17}		
25	EOC	End Of Conversion flag (low = busy, high = conversion complete)	
26	OVR	OVerRange flag (valid at end of conversion when output code exceeds full-scale, three-state output enabled with high byte)	
27	V+	Positive power supply input	
28	PROG	Used for programming only. Must tie to V+ for normal operation	
29	TEST	Used for programming only. Must tie to V+ for normal operation	
30	OSC1	Oscillator inverter input	
31	OSC2	Oscillator inverter output	
32	TEST	Used for programming only. Must tie to V+ for normal operation.	
33	$\overline{WR}$	$\overline{WR}$ite pulse input (low starts new conversion)	
34	C_{AZ}	Auto-zero capacitor connection*	
35	V−	Negative power supply input	
36	COMP	Used in test, tie to V−	
37	V_{INs}	SENSE line for input voltage	
38	V_{REFs}	SENSE line for reference input	
39	$AGND_s$	SENSE line for analog ground	
40	V_{INf}	FORCE line for input voltage	

***NOTE:** The voltage on C_{AZ} is driven:
Never connect directly to ground.

TABLE 2: I/O CONTROL

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	A_0	BUS	FUNCTION
0	0	x	x	x	Initiates a Conversion
1	x	x	x	x	Disables all Chip Commands
0	x	0	0	0	Low Byte is Enabled
0	x	0	1	0	High Byte is Enabled
0	x	0	x	1	Low and High Bytes Enabled Together
x	x	1	x	x	Disables Outputs (High-Impedance)

TABLE 3: TRANSFER FUNCTION

INPUT VOLTAGE	EXPECTED OUTPUT CODE			
$V_{REF} = -10.0V$	OVR	MSB		LSB
+0.00000	0	0	0000000000000	0
+0.00061	0	0	0000000000000	1
+0.29968	0	0	0000111101010	1
+4.99939	0	0	1111111111111	1
+5.000	0	1	0000000000000	0
+9.99878	0	1	1111111111111	0
+9.99939	0	1	1111111111111	1
+10.00000	1	0	0000000000000	0
+10.00061	1	0	0000000000000	1
+10.29968	1	0	0000111101010	1

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

The ICL7115 is basically a successive approximation A/D converter with an internal structure much more complex than a standard SAR-type converter. Figure 1 shows the functional diagram of the ICL7115 14-bit A/D converter. The additional circuitry incorporated into the ICL7115 is used to perform error correction and to maintain the operating speed in the 40μs range.

The internal 17-bit DAC of the ICL7115 is designed around a radix of 1.85 rather than the traditional 2.00. This radix gives each bit of the DAC a weight of approximately 54% of the previous bit. The result is a useable range that extends to 3% beyond the full-scale input of the A/D. The actual value of each bit is measured and stored in the on-chip PROM. The absolute value of each bit weight then becomes relatively unimportant because of the error correction action of the ICL7115.

The output of the high-speed auto-zeroed comparator is fed to the data input of a 17-bit successive approximation register (SAR). This register is uniquely designed for the ICL7115 in that it tests bit pairs instead of individual bits in the manner of a standard SAR. At the beginning of the conversion cycle, the SAR turns on the MSB (B_{16}) and the MSB-4 bit (B_{12}). The sequence continues for each bit pair, B_X and B_{X-4}, until only the four LSBs remain. The sequence concludes by testing the four LSBs individually.

The SAR output is fed to the DAC register and to the preprogrammed 17-word by 17-bit PROM where it acts as PROM address. PROM data is fed to a 17-bit full-adder/accumulator where the decoded results from each successive phase of the conversion are summed with the previous results. After 20 clock cycles, the accumulator contains the final binary data which is latched and sent to the three-state output buffers. The accuracy of the A/D converter depends primarily upon the accuracy of the data that has been programmed into the PROM during the final test portion of the manufacturing process.

The error correcting algorithm built into the ICL7115 reduces the initial accuracy requirements of the DAC. The overlap in the testing of bit pairs reduces the accuracy requirements on the comparator which has been optimized for speed. Since the comparator is auto-zeroed, no external adjustment is required to get ZERO code for ZERO input voltage.

Twenty clock cycles are required for the complete 14-bit conversion. The auto-zero circuitry associated with the comparator is employed during the last three clock cycles of the conversion to cancel the effect of offset voltage. Also during this time, the SAR and accumulator are reset in preparation for the start of the next conversion.

The overflow output of the 17-bit full-adder is also the OVerRange (OVR) output of the ICL7115. Unlike standard SAR-type A/D converters, the ICL7115 has the capability of providing valid useable data for inputs that exceed the full-scale range by as much as 3%.

OPTIMIZING SYSTEM PERFORMANCE

The FORCE and SENSE inputs for V_{IN} and V_{REF} are also shown driven by external op-amps. This technique eliminates the effect of small voltage drops which can appear between the input pin of the IC package and the actual resistor on the chip. If the small gauge wire and the bonds that connect the chip to its package have more than 300mΩ of total series resistance, the result can be a voltage error equivalent to 1LSB. If no op-amps are used for V_{IN} and V_{REF}, connections should be made directly to the SENSE lines. The external op-amps also serve to transform the relatively low impedance at the V_{IN} and V_{REF} pins into a high impedance. The input offset voltages of these amplifiers should be kept low in order to maintain the overall A/D converter system accuracy.

When using A/D converters with more than 12 bits of resolution, special attention must be paid to grounding and the elimination of potential ground loops. A ground loop can be formed by allowing the return current from the ICL7115's DAC to flow through traces that are common to other analog circuitry. If care is not taken, this current can generate small unwanted voltages that add to or detract from the reference or input voltages of the A/D converter.

Ground loops can be eliminated by the use of the analog ground FORCE and SENSE lines provided on the ICL7115 as shown in Figures 5 and 6. In Figure 5 the FORCE line is the only point that is connected to system analog ground. In Figure 6, the op-amp A_3 forces the voltage at AGND to be equal to analog system ground. The addition of this op-amp overcomes the main deficiency of the arrangement in Figure 5: the V_{IN} and V_{REF} sources are not referenced to true analog system ground.

The clamp diodes in Figure 6 are required because spurious op-amp output on AGNDf during power-on can exceed the absolute max rating of $\pm$1.0V between AGDf and DGND. The two inverse-parallel diodes clamp the voltage between AGNDs and DGND to $\pm$0.7V.

INPUT WARNING

As with any CMOS integrated circuit, no input voltages should be applied to the ICL7115 until the $\pm$5V power supplies have stabilized.

INTERFACING TO DIGITAL SYSTEMS

The ICL7115 provides three-state data output buffers, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, and bus select inputs (A_0 and BUS) for interfacing to a wide variety of microcomputers and digital systems. The I/O Control Truth Table shows the functions of the digital control lines. The BUS select and A_0 lines are provided to enable the output data onto either 8-bit or 16-bit data buses. A conversion is initiated by a $\overline{WR}$ pulse (pin 33) when $\overline{CS}$ (pin 3) is low. Data is enabled on the bus when the chip is selected and $\overline{RD}$ (pin 4) is low.

Figure 7 illustrates a typical interface to an 8-bit microcomputer. The "Start and Wait" operation requires the fewest external components and is initiated by a low level on the $\overline{WR}$ input to the ICL7115 after the I/O or memory-mapped address decoder has brought the $\overline{CS}$ input low. After executing a delay or utility routine for a period of time greater than the conversion time of the ICL7115, the processor issues two consecutive bus addresses to read output data into two bytes of memory. A low level on A_0 enables the LSBs and a high level enables the MSBs.

NOTE: All typical values have been characterized but are not tested.

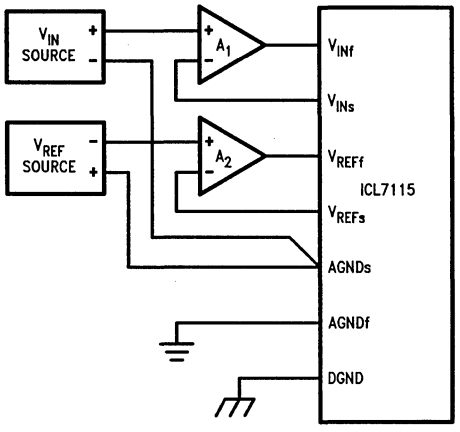


Figure 5: V_{IN} and V_{REF} Input Buffers

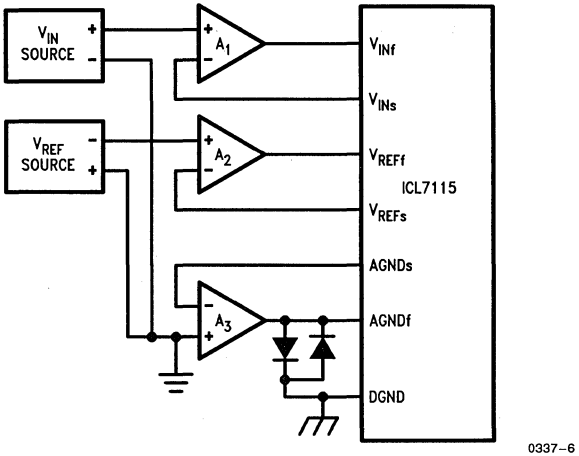
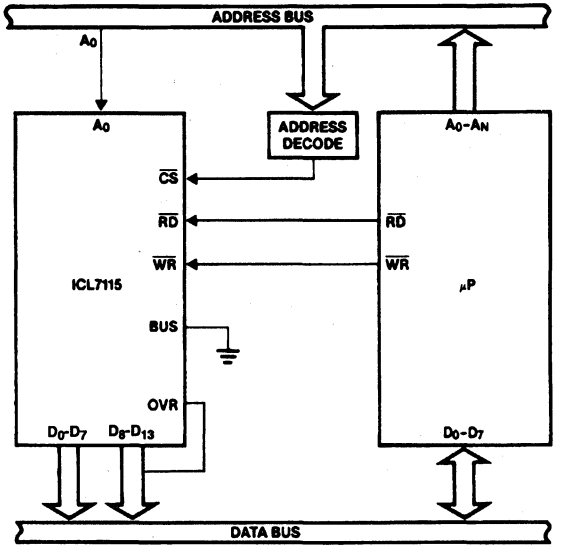


Figure 6: Using a Forced Ground

NOTE: All typical values have been characterized but are not tested.



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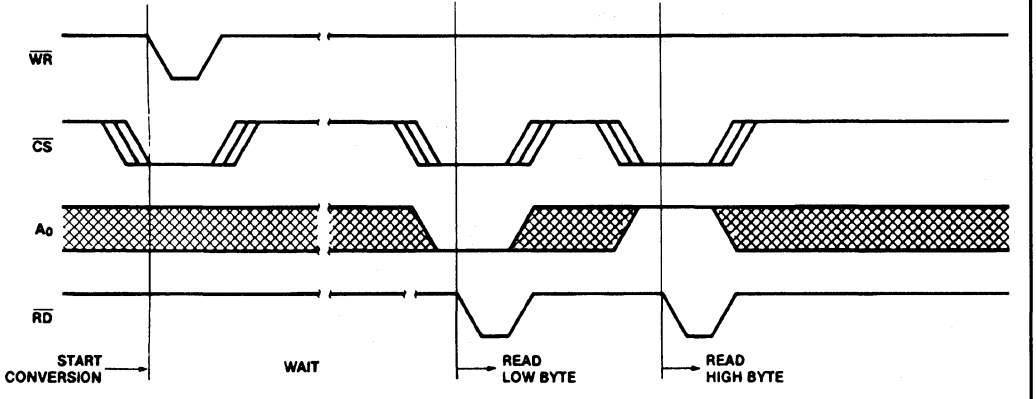


0337-8

Figure 7: "Start and Wait" Operation

NOTE: All typical values have been characterized but are not tested.

By adding a three-state buffer and two control gates, the End-of-Conversion (EOC) output can be used to control a "Start and Poll" interface (Figure 8). In this mode, the A_0 and $\overline{CS}$ lines connect the EOC output to the data bus along with the most significant byte of data. After pulsing the $\overline{WR}$ line to initiate a conversion, the microprocessor continually reads the most significant byte until it detects a high level on the EOC bit. The "Start and Poll" interface increases data throughput compared with the "Start and Wait" method by eliminating delays between the conversion termination and the microprocessor read operation.

Other interface configurations can be used to increase data throughput without monopolizing the microprocessor during waiting or polling operations by using the EOC line as an interrupt generator as shown in Figure 9. After the conversion cycle is initiated, the microprocessor can continue to execute routines that are independent of the A/D converter until the converter's output register actually holds valid data. For fastest data throughput, the ICL7115 can be connected directly to the data bus but controlled by way of a Direct Memory Access (DMA) controller as shown in Figure 10.

APPLICATIONS

Figure 11 shows a typical application of the ICL7115 14-bit A/D converter. A bipolar input voltage range of +5V to −5V is the result of using the current through R_2 to force a ½ scale offset on the input amplifier (A_2). The output of A_2 swings from 0V to −5V. The overall gain of the A/D is varied by adjusting the 100kΩ trim resistor, R_5. Since the ICL7115 is automatically zeroed every conversion, the system gain and offset stability will be superb as long as a reference with a tempco of 1ppm/°C and stable external resistors are used.

In Figure 11, note that the 0.22μF auto-zero capacitor is connected directly between the C_{AZ} pin and analog ground SENSE. A_3 forces the analog ground of the ICL7115 to be the zero reference for the input signal. Its offset voltage is not important in this example because the voltage to be digitized is referred to the analog ground SENSE line rather than system analog ground. It is important to note that since the 7115's DAC current flows in A_1, A_2 and A_3 these amplifiers should be wideband (GBW>20MHz) types to minimize errors.

The clock for the ICL7115 is taken from whatever system clock is available and divided down to the 500kHz level for a conversion time of 40μs. Output data is controlled by the BUS and A_0 inputs. Here they are set for 8-bit bus operation with BUS grounded and A_0 under the control of the address decode section of the external system.

Because the ICL7115's internal accumulator generates accurate output data for input signals as much as 3% greater than full-scale, and because the converter's OVR output flags overrange inputs, a simple microprocessor routine can be employed to precisely measure and correct for system gain and offset errors. Figure 12 shows a typical data acquisition system that uses a 5.0V reference, input signal multiplexer, and input signal Track/Hold amplifier. Two of the multiplexer's input channels are dedicated to sampling the system analog ground and reference voltage. Here, as in Figure 11, bipolar operation is accommodated by an offset resistor between the reference voltage and the summing junction of A_1. A flip-flop in IC_3 sets IC_2's Track/Hold input after the microprocessor has initiated a WR command, and resets when EOC goes high at the end of the conversion.

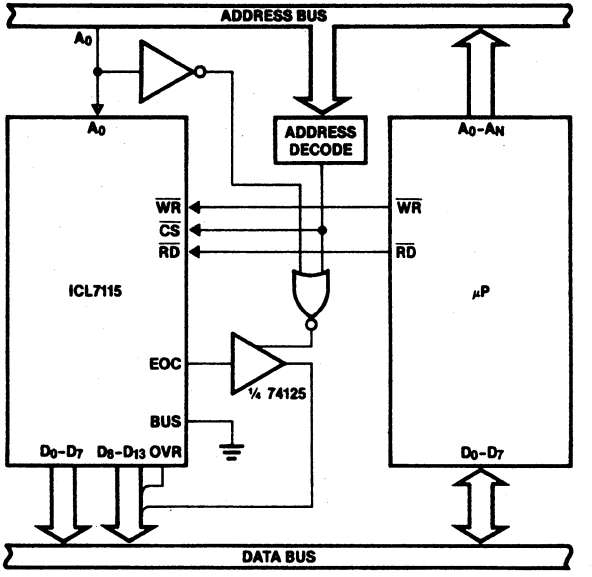
The first step in the system calibration routine is to select the multiplexer channel that is connected to system analog ground and initiate a conversion cycle for the ICL7115. The results represent the system offset error which comes from the sum of the offsets from IC_1, IC_2, and A_1. Next the channel connected to the reference voltage is selected and measured. These results, minus the system offset error, represent the system full-scale range. A gain error correction factor can be derived from this data. Since the ICL7115 provides valid data for inputs that exceed full-scale by as much as 3%, the OVR output can be thought of as a valid 15th data bit. Whenever the OVR bit is high, however, the total 14-bit result should be checked to insure that it falls within 100% and 103% of full-scale. Data beyond 103% of full-scale should be discarded.

The ICL7115 provides an internal inverter which is brought out to pins OSC1 and OSC2, for crystal or ceramic resonator oscillator operation. The clock frequency is calculated from:

$$f_{CLK} = \frac{20}{t_{conv}} \text{ for 14-bit operation}$$

NOTE: All typical values have been characterized but are not tested.

(A)



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(B)

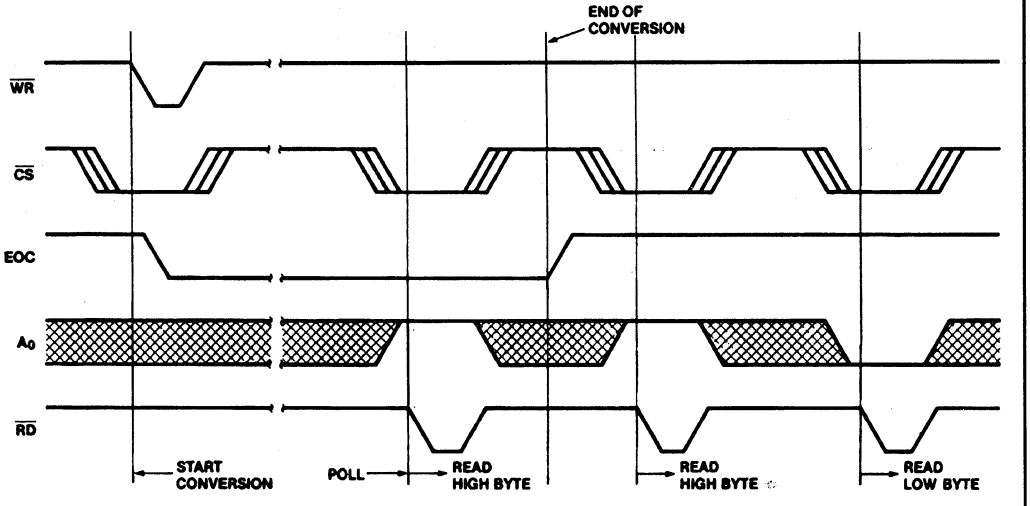

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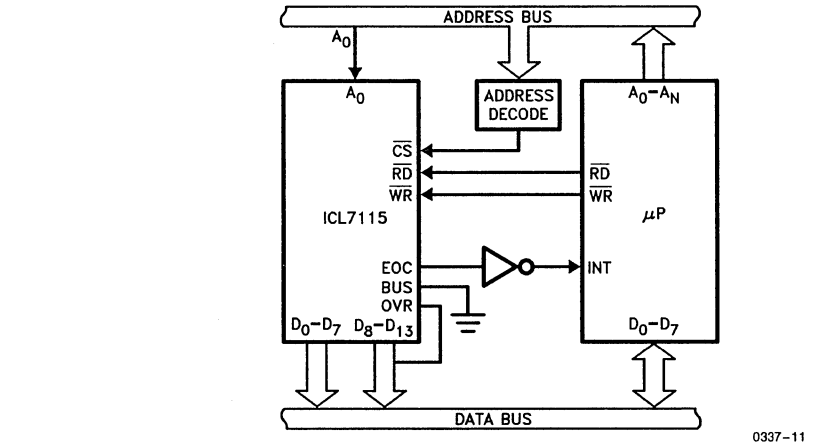
Figure 8: "Start and Poll" Operation

NOTE: All typical values have been characterized but are not tested.



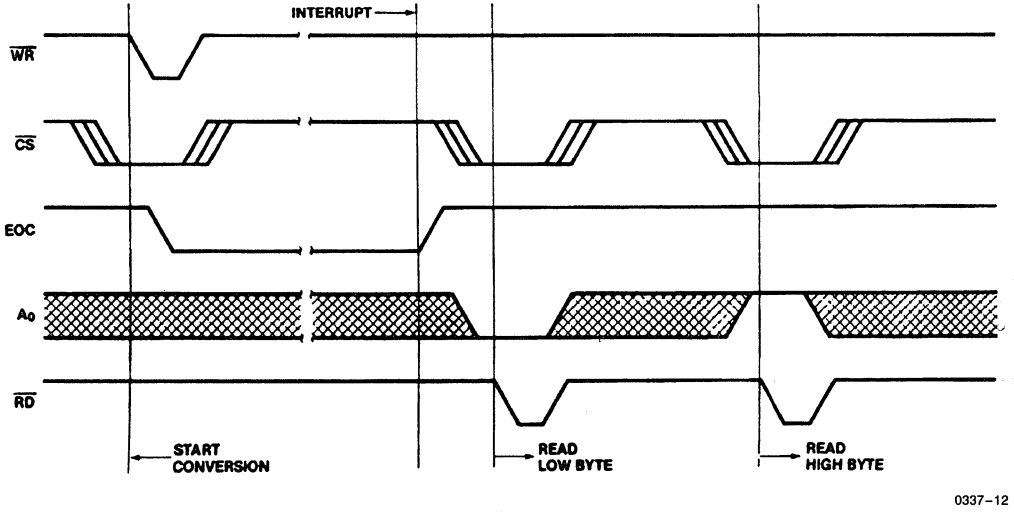
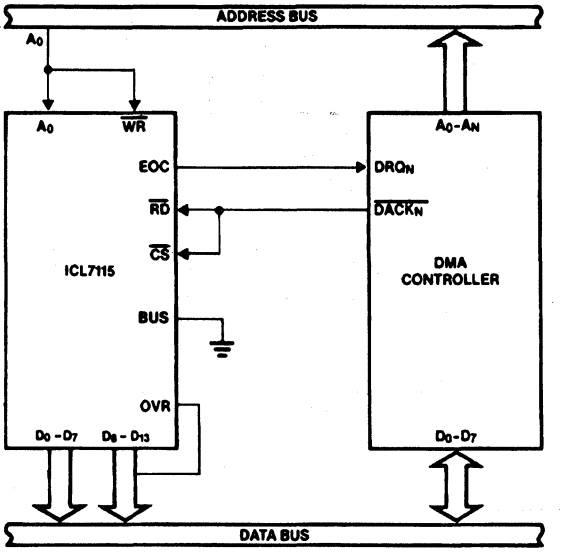
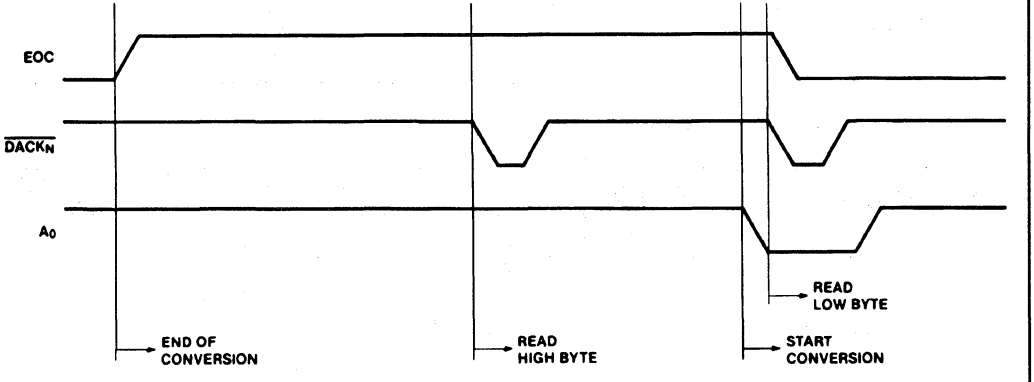


Figure 9: Using EOC as an Interrupt

NOTE: All typical values have been characterized but are not tested.



0337-13



0337-14

Figure 10: Data to Memory via DMA Controller

NOTE: All typical values have been characterized but are not tested.

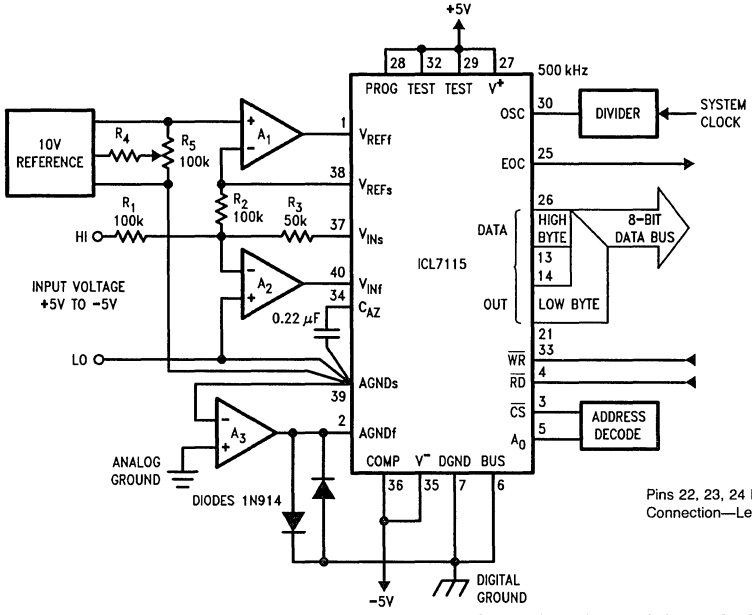


Figure 11: Typical Application with Bipolar Input Range, Forced Ground, and 10 Volt Ultra-Stable Reference

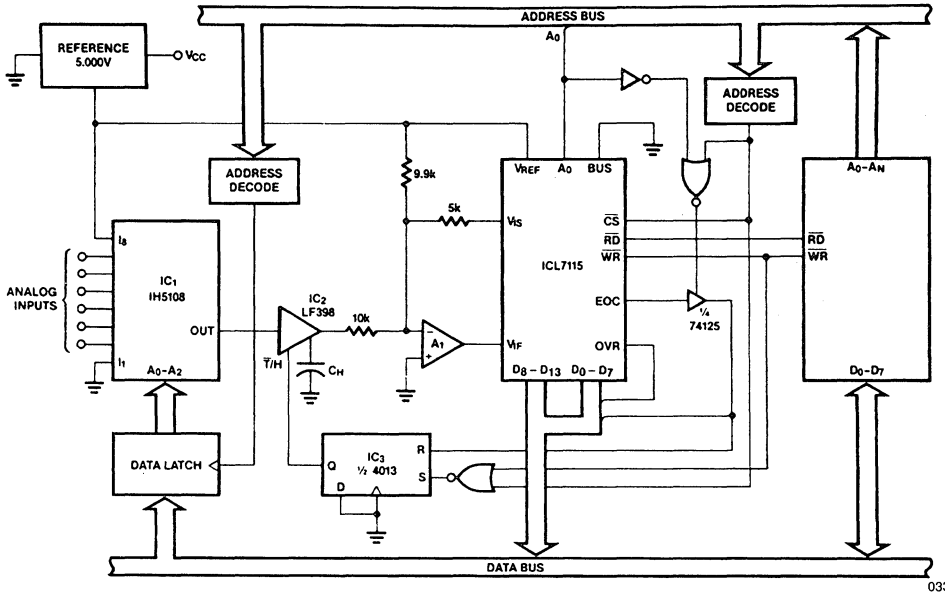


Figure 12: Multi-Channel Data Acquisition System with Zero and Reference Lines Brought to Multiplexer for System Gain and Offset Error Correction

NOTE: All typical values have been characterized but are not tested.

DATA ACQUISITION 5

A/D CONVERTERS FLASH

HARRIS SEMICONDUCTOR

CA3304, CA3304A

CMOS Video-Speed 4-Bit Flash Analog-to-Digital Converter

GENERAL DESCRIPTION

The Harris CA3304 is a CMOS parallel (FLASH) analog-to-digital converter designed for applications demanding both low-power consumption and high-speed digitization. Digitizing at 25 MHz, for example, requires only about 35 mW.

The CA3304 operates over a wide, full-scale signal input-voltage range of ½ volt up to the DC supply voltage. Power consumption is as low as 10 mW, depending upon the clock frequency selected.

The intrinsic high conversion rate makes the CA3304 types ideally suited for digitizing high-speed signals. The overflow bit makes possible the connection of two or more CA3304s in series to increase the resolution of the conversion system. A series connection of two CA3304s may be used to produce a 5-bit, 25 MHz converter. Operation of two CA3304s in parallel doubles the conversion speed (i.e., increases the sampling rate from 25 MHz to 50 MHz). A data change pin indicates when the present output differs from the previous, thus allowing compaction of data storage.

Sixteen paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3304. Fifteen comparators are required to quantize all input voltage levels in this 4-bit converter, and the additional comparator is required for the overflow bit.

FEATURES

- **CMOS/SOS Low Power with Video Speed (25 mW typ)**
- **Parallel Conversion Technique**
- **Single Power Supply Voltage (3V to 7.5V)**
- **25 MHz Sampling Rate (40 ns Conversion Time) at 5V Supply**
- **4-Bit Latched 3-State Output with Overflow and Data Change Outputs**
- **⅛ LSB Maximum Nonlinearity (A Version)**
- **Inherent Resistance to Latch-Up Due to SOS Process**
- **Bipolar Input Range with Optional Second Supply**

APPLICATIONS

- **TV Video Digitizing (Industrial/Security)**
- **High-Speed A/D Conversion**
- **Ultrasound Signature Analysis**
- **Transient Signal Analysis**
- **High-Energy Physics Research**
- **General-Purpose Hybrid ADCs**
- **Optical Character Recognition**
- **Radar Pulse Analysis**
- **Motion Signature Analysis**
- **Robot Vision**

ORDERING INFORMATION

Part Number	Linearity (INL, DNL)	Sampling Rate	Temperature Range	Package
CA3304E	±0.25 LSB	25MHz (40ns)	-40°C to +85°C	16 Pin Plastic DIP
CA3304AE	±0.125 LSB	25MHz (40ns)	-40°C to +85°C	16 Pin Plastic DIP
CA3304M	±0.25 LSB	25MHz (40ns)	-40°C to +85°C	16 Pin Plastic SOIC
CA3304AM	±0.125 LSB	25MHZ (40ns)	-40°C to +85°C	16 Pin Plastic SOIC
CA3304D	±0.25 LSB	25MHz (40ns)	-55°C to +125°C	16 Pin Ceramic DIP
CA3304AD	±0.125 LSB	25MHz (40ns)	-55°C to +125°C	16 Pin Ceramic DIP

16 LEAD CERAMIC DIP
16 LEAD PLASTIC DIP
16 LEAD SOIC

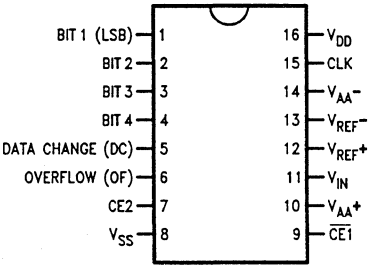


Figure 1: Pin Configuration

1790-00

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage Range (V_{DD} or V_{AA}^+)
(Voltage Referenced to V_{SS} or V_{AA}^- Terminal, Whichever, is More Negative) . . . . . −0.5V to +8V

Input Voltage Range
CE1, CE2 Inputs . . . . . V_{SS} − 0.5V to V_{DD} + 0.5V
Clock, V_{REF}^+, V_{REF}^-, V_{IN} Inputs . . . . . V_{AA} − 0.5V to V_{AA} + 0.5V

DC Input Current
Any Input . . . . . ±20 mA

Power Dissipation per Package (P_D)
For T_A = −55°C to +55°C . . . . . 315 mW
For T_A = +55°C to +125°C . . . . . Derate Linearly at 3.3 mW/°C

Operating Temperature Range (T_A)
CA3304D, CA3304AD . . . . . −55°C to +125°C
CA3304E, CA3304AE . . . . . −40°C to +85°C

Storage Temperature Range (T_{stg}) . . . . . −65°C to +150°C

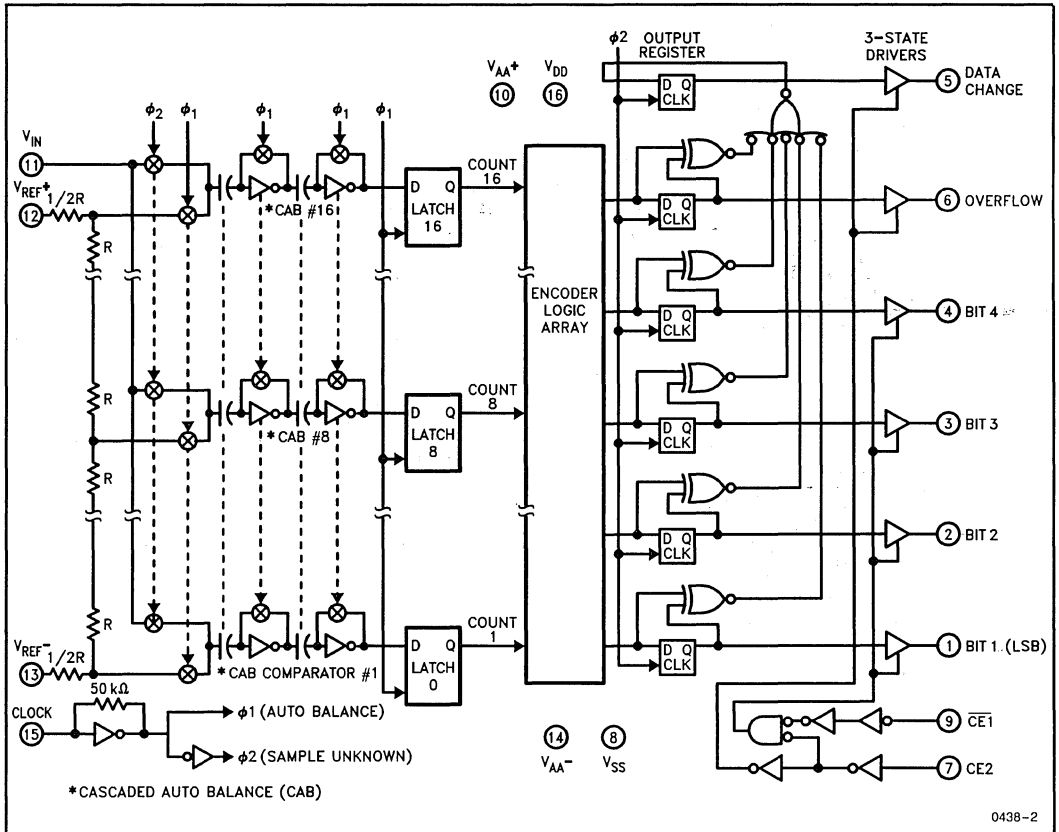
Lead Temperature (During Soldering)
At Distance 1/16 in. ± 1/32 in. (1.59mm ±0.79mm) from Case for 10s Max. . . . . +265°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Supply Voltage Range (V_{DD} or V_{AA}^+) . . . . . 3V to 7.5V

Recommended V_{AA}^+ Voltage Range . . . . . V_{DD} − 1V to V_{DD} + 2.5V

Recommended V_{AA}^- Voltage Range . . . . . V_{SS} − 2.5V to V_{SS} + 1V



NOTE: $\overline{CE1}$ and CE2 inputs and data outputs have standard CMOS protection networks to V_{DD} and V_{SS}. Anaolog inputs and clock have standard CMOS protection networks to V_{AA}^+ and V_{AA}^-

Figure 2: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $V_{REF}^+ = 2V$, $V_{DD} = V_{AA}^+ = 5V$, $V_{AA}^- = V_{REF}^- = V_{SS} = GND$, $f_{CLK} = 25$ MHz unless noted otherwise.

Parameter			Test Conditions	Limits			Units
				Min	Typ	Max	
Resolution				4			Bits
Input Errors	Integral Linearity Error	CA3304A			±0.1	±0.125	LSB
		CA3304			±0.125	±0.25	
	Differential Linearity Error	CA3304A			±0.1	±0.125	
		CA3304			±0.125	±0.25	
	Quantizing Error (Inherent)					±0.5	
	Offset Error (Unadjusted)	CA3304A				±0.75	
		CA3304				±1.0	
	Gain Error (Unadjusted)	CA3304A				±0.75	
		CA3304				±1.0	
Input Range	V_{REF}^+ Range		(Note 4)	$V_{AA}^- + 0.5$		V_{AA}^+	V
	V_{REF}^- Range		(Note 4)	V_{AA}^-		$V_{AA}^+ - 0.5$	
	Full-Scale Input Range		(Note 1, 4)	0.5		V_{AA}	
Input Loading	Input Capacitance				10		pF
	Input Current		$V_{IN} = 2.0V$ (Note 2)		150	200	μA
	Resistor Ladder Impedance		$V_{IN} = 5V$, CLK = Low	640		960	Ω
Conversion Timing	Maximum Conversion Speed		CLK = Square Wave	25	30		MSPS
	Auto-Balance Time (ϕ1)			20		∞	ns
	Sample Time (ϕ2)			20		5000	
	Aperture Delay				3		
Allowable Input Bandwidth			(Note 4)	DC		$f_{CLK}/2$	MHz
−3 dB Input Bandwidth					40		
Output Timing	Data Valid Delay		(Note 4)		30	40	ns
	Data Hold Time		(Note 4)	15	25		
	Output Enable Time				15		
	Output Disable Time				10		
Device Current, I_{AA}			Continuous Clock		5.5		mA
			Continuous ϕ2		0.4		
			Continuous ϕ1		2		

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{REF}^+ = 2V, V_{DD} = V_{AA}^+ = 5V, V_{AA}^- = V_{REF}^- = V_{SS} = GND, f_{CLK} = 25 MHz unless noted otherwise. (Continued)

Parameter			Test Conditions	Limits			Units
				Min	Typ	Max	
Device Current, I_{DD}			Continuous Clock		1.5		mA
	V_{AA}^+ = 5V, V_{SS} = $\overline{CEI}$ = V_{AA}^- = CLK = GND		Continuous ϕ2		5	10	
	V_{AA}^+ = 7V		Continuous ϕ1		5	20	
Digital Inputs	Maximum V_{IN}, Low	CLOCK	(Note 3, 4)			0.3 x V_{AA}	V
		$\overline{CE1}$, CE2	(Note 4)			0.3 x V_{DD}	
	Minimum V_{IN}, High	CLOCK	(Note 3, 4)	0.7 x V_{AA}			
		$\overline{CE1}$, CE2	(Note 4)	0.7 x V_{DD}			
	Input Leakage, except CLK		V = 0V, 5V			±1	µA
	Input Leakage, CLK		(Note 3)		±100	±150	
Digital Outputs	Output Low (Sink) Current		V_O = 0.4V	6			mA
	Output High (Source) Current		V_O = 4.6V	−3			
	3-State Leakage Current		V_O = 0V, 5V		±0.2	±5	µA

NOTES 1: Full-scale input range, $V_{REF}^+ - V_{REF}^-$, may be in the range of 0.5V to $V_{AA}^+ - V_{AA}^-$ volts. Linearity errors increase at lower full-scale ranges, however.

2: Input current is due to energy transferred to the input at the start of the sample period. The average value is dependent on input and V_{DD} voltage.

3: The CLK input is a CMOS inverter with a 50 kΩ feedback resistor. It operates from the V_{AA}^+ and V_{AA}^- supplies. It may be AC-coupled with a 1V peak-to-peak minimum source.

4: Parameter not tested, but guaranteed by design or characterization.

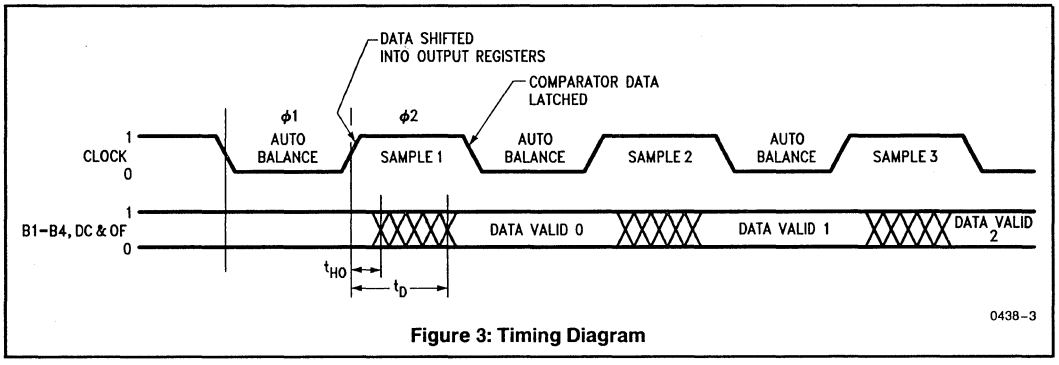


Figure 3: Timing Diagram

NOTE: All typical values have been characterized but are not tested.

CA3304, CA3304A

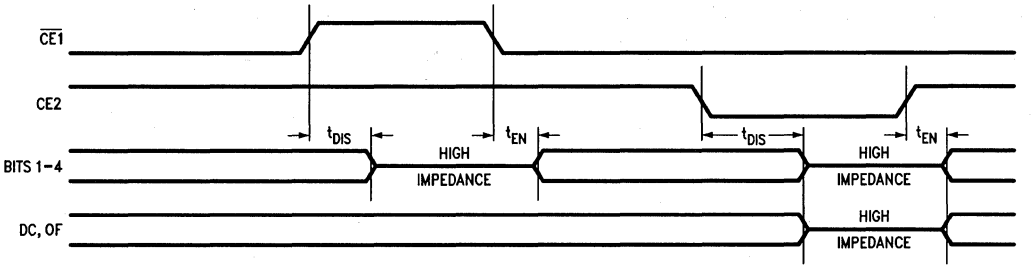
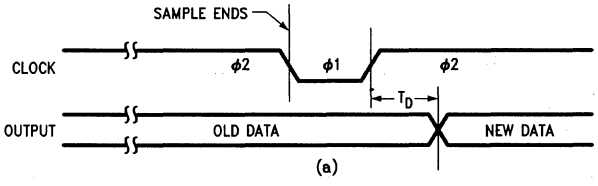
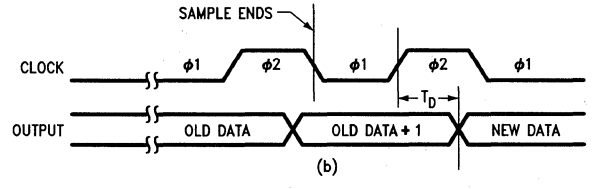


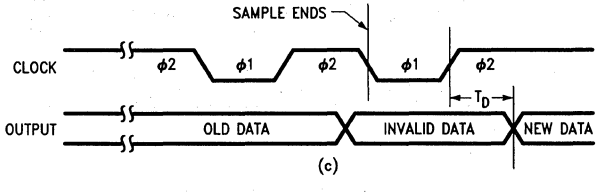
Figure 4: Output Enable/Disable Timing



With $\phi 2$ as standby state (fastest method, but standby limited to 5 μs maximum)



With $\phi 1$ as standby state (indefinite standby, double pulse needed)



With $\phi 2$ as standby state (indefinite standby, lower power than 5b)

Figure 5: Pulse-Mode Timing Diagrams

NOTE: All typical values have been characterized but are not tested.

Table 1: Pin Description

Pin	Name	Description
1	Bit 1	Bit 1 (LSB)
2	Bit 2	Bit 2
3	Bit 3	Bit 3
4	Bit 4	Bit 4 (MSB)
5	DC	Data Change
6	OF	Overflow
7	CE2	Three-state output enable input, active low. See Table 2.
8	V_{SS}	Digital Ground
9	$\overline{CE1}$	Three-state output enable input, active high. See Table 2.
10	V_{AA}^+	Analog power supply, +5V
11	V_{IN}	Analog signal input
12	V_{REF}^+	Reference Voltage Positive Input
13	V_{REF}^-	Reference Voltage Negative Input
14	V_{AA}^-	Analog Ground
15	CLK	Clock Input
16	V_{DD}	Digital Power Supply, +5V

Output Data Bits (High = True)

Table 2: Chip Enable Truth Table

$\overline{CE1}$	CE2	Bit 1–Bit 4	DC, OF
0	1	Valid	Valid
1	1	Three-State	Valid
X	0	Three-State	Three-State

X = Don't Care

DEVICE OPERATION

A sequential parallel technique is used by the CA3304 converter to obtain its high-speed operation. The sequence consists of the "Auto Balance" phase and the "Sample Unknown" phase (Refer to the circuit diagram). Each conversion takes one clock cycle.* The "Auto Balance" (ϕ1) occurs during the Low period of the clock cycle, and the "Sample Unknown" (ϕ2) occurs during the High period of the clock cycle.

***Note:** This device requires only a single-phase clock. The terminology of ϕ1 and ϕ2 refers to the High and Low periods of the same clock.

During the "Auto Balance" phase, a transmission-gate switch is used to connect each of 16 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{tap}(N) = [(V_{REF}/16) \times N] - [V_{REF}/(2 \times 16)]$$
$$= V_{REF}[(2N - 1)/32]$$

Where: $V_{tap}(N)$ = Reference ladder tap voltage at point N.
V_{REF} = Voltage across V_{REF}^- to V_{REF}^+
N = Tap number (1 through 16)

The other side of the capacitor is connected to a single-stage inverting amplifier whose output is shorted to its input by a switch. This biases the amplifier at its intrinsic trip point, which is approximately $(V_{DD} - V_{SS})/2$. The capacitors now charge to their associated tap voltages, priming the circuit for the next phase.

In the "Sample Unknown" phase, all ladder tap switches are opened, the comparator amplifiers are no longer shorted, and V_{IN} is switched to all 16 capacitors. Since the other end of the capacitor is now looking into an effectively open circuit, any voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators whose tap voltages were lower than V_{IN} will drive the comparator outputs to a "low" state. All comparators whose tap voltages were higher than V_{IN} will drive the comparator outputs to a "high" state. A second, capacitor-coupled, auto-zeroed amplifier further amplifies the outputs.

The status of all these comparator amplifiers are stored at the end of this phase (ϕ2), by a secondary latching amplifier stage. Once latched, the status of the 16 comparators is decoded by a 16-to-5-bit decode array and the results are clocked into a storage register at the rising edge of the next ϕ2.

If the input is greater than 31/32 x V_{REF}, the overflow output will go "high". (The bit outputs will remain high). If the output differs from that of the previous conversion, the data change output will go "high".

A 3-state buffer is used at the output of the 7 storage registers which are controlled by two chip-enable signals. $\overline{CE1}$ will independently disable B1 through B4 when it is in a high state. CE2 will independently disable B1 through B4 and the OF and DC buffers when it is in the low state.

CONTINUOUS CLOCK OPERATION

One complete conversion cycle can be traced through the CA3304 via the following steps. (Refer to timing diagram Figure 3). The rising edge of the clock input will start a "sample" phase. During this entire "High" state of the clock, the 16 comparators will track the input voltage and the 16 latches will track the comparator outputs. At the falling edge of the clock, all 16 comparator outputs are captured by the 16 latches. This ends the "sample" phase and starts the "auto balance" phase for the comparators. During this "Low" state of the clock the output of the latches propagates through the decode array and a 6-bit code appears at the D inputs of the output registers. On the next rising edge of the clock, this 6-bit code is shifted into the output registers and appears with time delay t_d as valid data at the output of the 3-state drivers. This also marks the start of a new "sample" phase, thereby repeating the conversion process for this next cycle.

NOTE: All typical values have been characterized but are not tested.

PULSE MODE OPERATION

For sampling high-speed nonrecurrent or transient data, the converter may be operated in a pulse mode in one of three ways. The fastest method is to keep the converter in the Sample Unknown phase, $\phi 2$, during the standby state. The device can now be pulsed through the Auto Balance phase with as little as 20ns. The analog value is captured on the leading edge of $\phi 1$ and is transferred into the output registers on the trailing edge of $\phi 1$. We are now back in the standby state, $\phi 2$, and another conversion can be started within 20ns, but not later than 5μs due to the eventual droop of the commutating capacitors. Another advantage of this method is that it has the potential of having the lowest power drain. The larger the time ratio between $\phi 2$ and $\phi 1$, the lower the power consumption. (See timing diagram Figure 5a).

The second method uses the Auto Balance phase, $\phi 1$, as the standby state. In this state the converter can stay indefinitely waiting to start a conversion. A conversion is performed by strobing the clock input with two $\phi 2$ pulses. The first pulse starts a Sample Unknown phase and captures the analog value in the comparator latches on the trailing edge. A second $\phi 2$ pulse is needed to transfer the date into the output registers. This occurs on the leading edge of the second pulse. The conversion now takes place in 40ns, but the repetition rate may be as slow as desired. The disadvantage to this method is the slightly higher device dissipation due to the low ratio of $\phi 2$ to $\phi 1$. (See timing diagram Figure 5b).

For applications requiring both indefinite standby and lowest power, standby can be in the $\phi 2$ (Sample Unknown) state with two $\phi 1$ pulses to generate valid data (see Figure 5c). The conversion process now takes 60ns. [Note that the above numbers do not include the t_D (Output Delay) time.]

INCREASED ACCURACY

In most cases the accuracy of the CA3304 should be sufficient without any adjustments. In applications where accuracy is of utmost importance, two adjustments can be made to obtain better accuracy; i.e., offset trim and gain trim.

OFFSET TRIM

In general offset correction can be done in the preamp circuitry by introducing a DC shift to V_{IN} or by the offset trim of the op-amp. When this is not possible the V_{REF}^- input can be adjusted to produce an offset trim.

The theoretical input voltage to produce the first transition is ½ LSB. The equation is as follows:

$$V_{IN} \text{ (0 to 1 transition)} = \tfrac{1}{2} \text{ LSB} = \tfrac{1}{2}(V_{REF}/16)$$
$$= V_{REF}/32$$

Adjust offset by applying this input voltage and adjusting the V_{REF}^- voltage or input amplifier offset until an output code alternating between 0 and 1 occurs.

GAIN TRIM

In general the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the op-amp. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V_{IN} should be set to the 15 to overflow transition. That voltage is ½ LSB less than V_{REF}^+ and is calculated as follows:

$$V_{IN} \text{ (15 to 16 transition)} = V_{REF} - V_{REF}/32$$
$$= V_{REF}\,(31/32)$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 15 to overflow transition. Now adjust V_{REF}^+ until that transition occurs on the outputs.

LAYOUT, INPUT AND SUPPLY CONSIDERATIONS

The CA3304 should be mounted on a ground-planed, printed-circuit board, with good high-frequency decoupling capacitors mounted as close as possible. If the supply is noisy, decouple V_{AA}^+ with a resistor as shown in Figure 6a. The CA3304 outputs current spikes to its input at the start of the auto-balance and sample clock phases. A low impedance source, such as a locally-terminated 50Ω coax cable, should be used to drive the input terminal. A fast-settling buffer such as the HA-5033, HA-5242, or CA3450 should be used if the source is high impedance. The V_{REF} terminals also have current spikes, and should be well bypassed.

Care should be taken to keep digital signals away from the analog input, and to keep digital ground currents away from the analog ground. If possible, the analog ground should be connected to digital ground only at the CA3304.

BIPOLAR OPERATION

The CA3304, with separate analog (V_{AA}^+, V_{AA}^-) and digital (V_{DD}, V_{SS}) supply pins, allows true bipolar or negative input operation. The V_{AA}^- pin may be returned to a negative supply (observing maximum voltage ratings to V_{AA}^+ or V_{DD} and recommended rating to V_{SS}), thus allowing the V_{REF}^- potential also to be negative. Figure 6b shows operation with an input range of -1V to $+1$V. Similarly, V_{AA}^+ and V_{REF}^+ could be maintained at a higher voltage than V_{DD}, for an input range above the digital supply.

DIGITAL INPUT AND OUTPUT LEVELS

The clock input is a CMOS inverter operating from and with logic input levels determined by the V_{AA} supplies. If V_{AA}^+ or V_{AA}^- are outside the range of the digital supplies, it may be necessary to level shift the clock input to meet the required 30% to 70% of V_{AA} input swing. Figure 6b shows an example for a negative V_{AA}^-.

An alternate way of driving the clock is to capacitively couple the pin from a source of at least 1V peak-to-peak. An internal 50 kΩ feedback resistor will keep the DC level at the intrinsic trip point. Extremely non-symmetrical clock waveforms should be avoided, however.

The remaining digital inputs and outputs are referenced to V_{DD} and V_{SS}. If TTL or other lower voltage sources are to drive the CA3304, either pull-up resistors or CD74HCT series "QMOS" buffers are recommended.

NOTE: All typical values have been characterized but are not tested.

5-BIT RESOLUTION

To obtain 5-bit resolution, two CA3304s can be wired together. Necessary ingredients include an open-ended ladder network, an overflow indicator, three-state outputs, and chip-enable controls—all of which are available on the CA3304.

The first step for connecting a 5-bit circuit is to totem-pole the ladder networks, as illustrated in Figure 7. Since the absolute-resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overflow output of the lower device now becomes the fifth bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overflow signal to the $\overline{CE1}$ control of the lower A/D converter and the CE2 control of the upper A/D converter. The three-state outputs of the two devices (bits 1 through 4) are now connected in parallel to complete the circuitry.

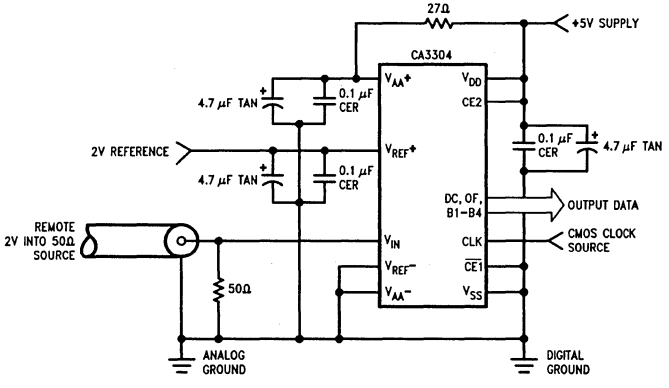


Figure 6a: Typical CA3304 Unipolar Circuit Configuration

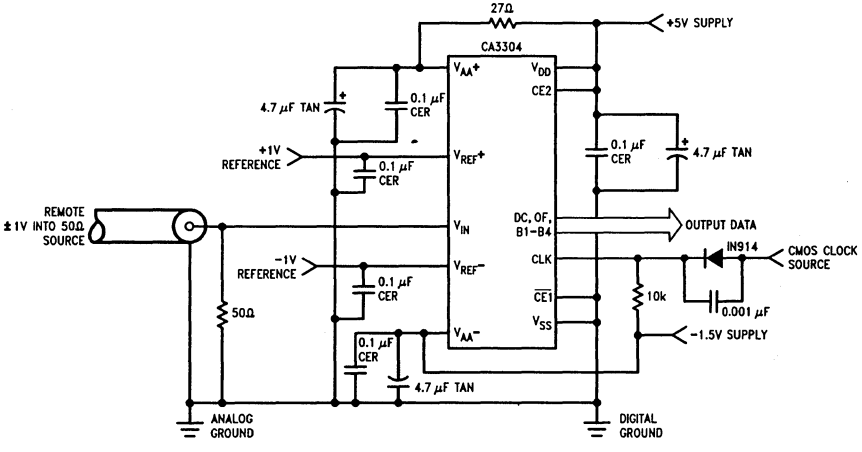


Figure 6b: Typical CA3304 Bipolar Circuit Configuration

NOTE: All typical values have been characterized but are not tested.

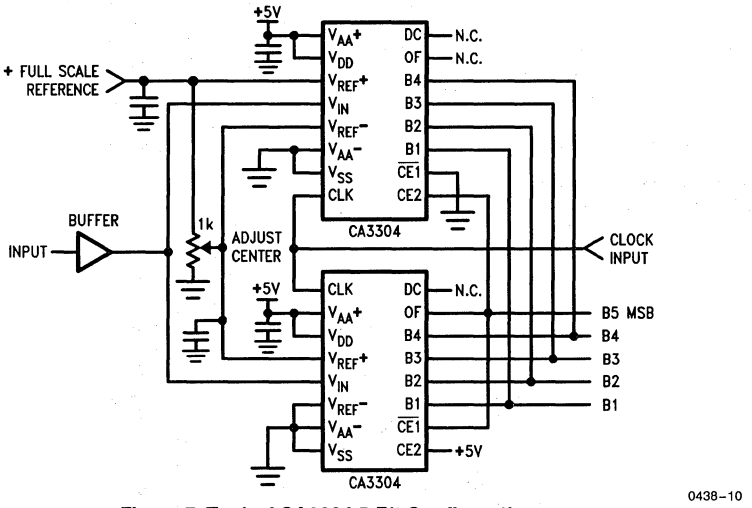


Figure 7: Typical CA3304 5-Bit Configuration

Table 3: Output Code Table

Code Description	Input Voltage (V)					Output Code					Decimal Count
	$V_{REF}^+ = 1V$ $V_{REF}^- = -1V$	1.6V 0V	2V 0V	3.2V 0V	4.8V 0V	0F	B4	B3	B2	B1	
Zero	−1.000	0	0	0	0	0	0	0	0	0	0
1 LSB	−0.875	0.1	0.125	0.2	0.3	0	0	0	0	1	1
2 LSB	−0.750	0.2	0.250	0.4	0.6	0	0	0	1	0	2
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
½ Full Scale − 1 LSB	−0.125	0.7	0.875	1.4	2.1	0	0	1	1	1	7
½ Full Scale	0	0.8	1.000	1.6	2.4	0	1	0	0	0	8
½ Full Scale + 1 LSB	0.125	0.9	1.125	1.8	2.7	0	1	0	0	1	9
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
Full Scale − 1 LSB	0.750	1.4	1.750	2.8	4.2	0	1	1	1	0	14
Full Scale	0.875	1.5	1.875	3.0	4.5	0	1	1	1	1	15
Overflow	1.000	1.6	2.000	3.2	4.8	1	1	1	1	1	31
Step Size	0.125	0.1	0.125	0.2	0.3						

NOTE: The voltages listed are the ideal centers of each output code shown as a function of its associated reference voltage. See Ideal Transfer Curve Figure 8. The output code should exist for an input equal to the ideal center voltage ± ½ of the step size.

NOTE: All typical values have been characterized but are not tested.

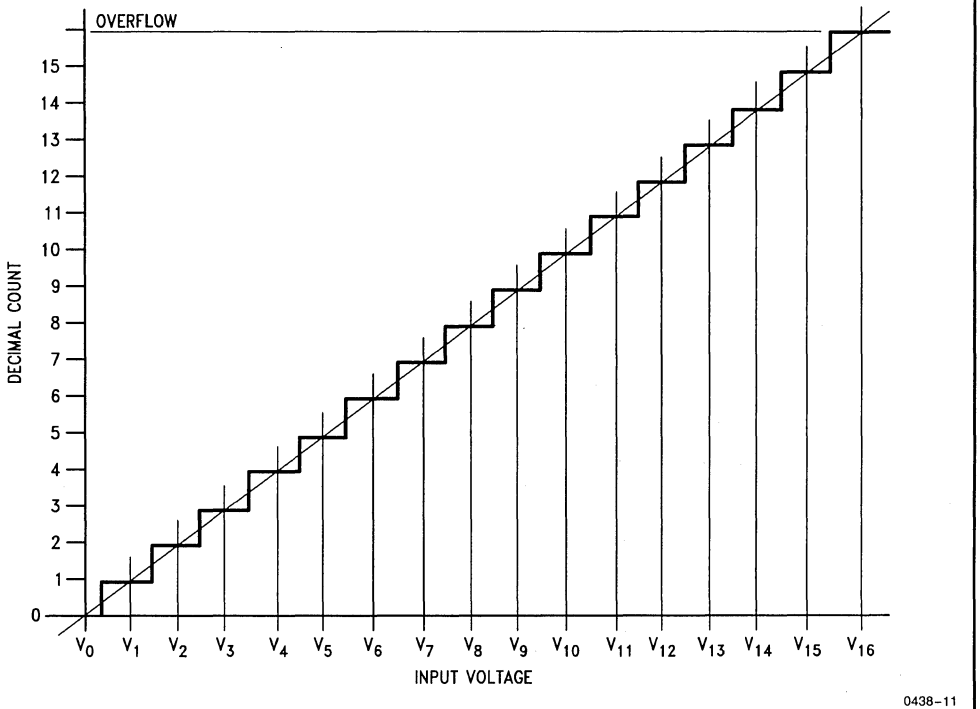


Figure 8: Ideal Transfer Curve

OPERATING AND HANDLING CONSIDERATIONS

1. HANDLING

All inputs and outputs of CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. OPERATING

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause the power supply voltages to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} or $V_{AA}{}^{+}$ nor less than V_{SS} or $V_{AA}{}^{-}$ (depending upon which supply the protection network is referenced. See Maximum Ratings). Input currents must not exceed 20 mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to any supply potential may damage CMOS devices by exceeding the maximum device dissipation.

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

CA3306, CA3306A, CA3306C

CMOS Video-Speed 6-Bit Flash Analog-to-Digital Converter

GENERAL DESCRIPTION

The Harris CA3306 family are CMOS parallel (FLASH) analog-to-digital converters designed for applications demanding both low-power consumption and high-speed digitization. Digitizing at 15 MHz, for example, requires only about 50 mW.

The CA3306 family operates over a wide, full-scale signal input-voltage range of 1V up to the DC supply voltage. Power consumption is as low as 15 mW, depending upon the clock frequency selected. The CA3306 types may be directly retrofitted into CA3300 sockets, offering improved linearity at a lower reference voltage and higher operating speed with a 5V supply.

The intrinsic high conversion rate makes the CA3306 types ideally suited for digitizing high-speed signals. The overflow bit makes possible the connection of two or more CA3306s in series to increase the resolution of the conversion system. A series connection of two CA3306s may be used to produce a 7-bit high-speed converter. Operation of two CA3306s in parallel doubles the conversion speed (i.e., increases the sampling rate from 15 MHz to 30 MHz).

Sixty-four paralleled auto-balanced comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3306. Sixty-three comparators are required to quantize all input voltage levels in this 6-bit converter, and the additional comparator is required for the overflow bit.

FEATURES

- CMOS Low Power with Video Speed (−70 mW typ)
- Parallel Conversion Technique
- Signal Power Supply Voltage (3V to 7.5V)
- 15-MHz Sampling Rate with Single 5V Supply
- 6-Bit Latched 3-State Output with Overflow Bit
- Pin-For-Pin Retrofit for the CA3300

APPLICATIONS

- TV Video Digitizing
- High-Speed A/D Conversion
- Ultrasound Signature Analysis
- Transient Signal Analysis
- High-Energy Physics Research
- High-Speed Oscilloscope Storage/Display
- General-Purpose Hybrid ADCs
- Optical Character Recognition
- Radar Pulse Analysis
- Motion Signature Analysis
- Robot Vision

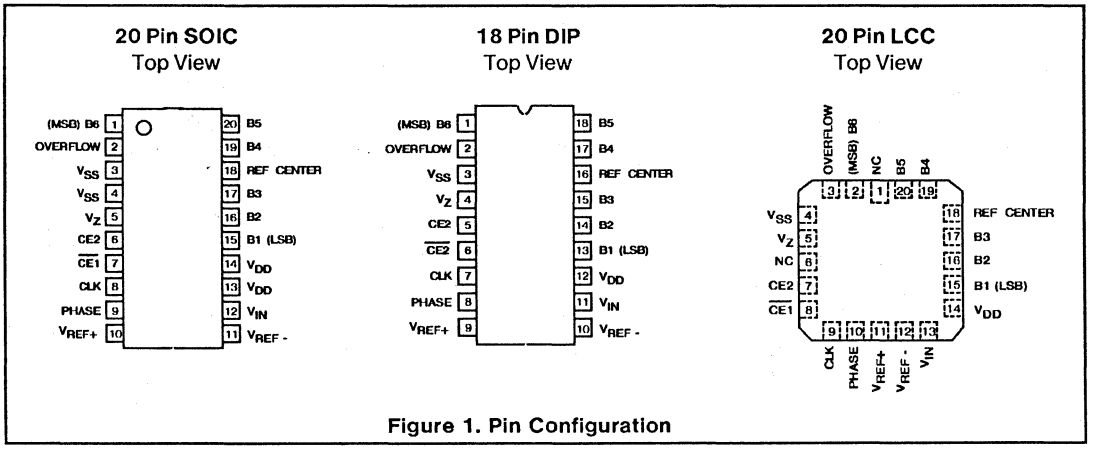


Figure 1. Pin Configuration

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

DC Supply-Voltage Range, (V_{DD})
(Voltage Referenced
to V_{SS} Terminal) ..... −0.5V to +8.5V

Input Voltage Range
All Inputs except Zener ..... −0.5V to V_{DD} + 0.5V

DC Input Current
CLK, PH, $\overline{CE1}$, CE2, V_{IN} ..... ±20 mA

Power Dissipation per Package (P_D):
For T_A = −55°C to +55°C ..... 315 mW
For T_A = +55°C to +125°C ..... Derate Linearly at 3.3 mW/°C

Operating Temperature Range (T_A):
Ceramic Package—D Suffix ..... −55°C to +125°C
Plastic Package—E Suffix ..... −40°C to +85°C

Storage Temperature Range (T_{STG}) .... −65°C to +150°C

Lead Temperature (During Soldering):
At Distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from
Case for 10s Max. ..... +265°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Supply Voltage Range ..... 3V to 8V

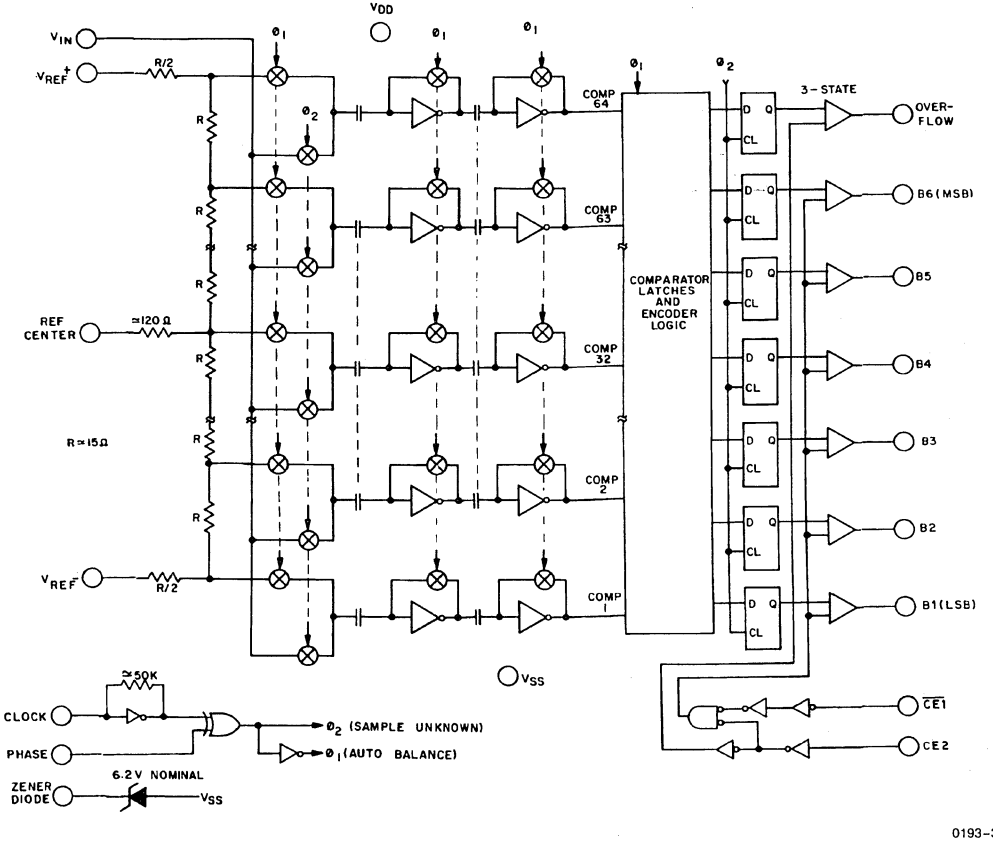


Figure 2: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

CA3306, CA3306A, CA3306C

ELECTRICAL CHARACTERISTICS

@ T_A = 25° C, V_{DD} = 5V, $V_{REF}+$ = 4.8V, V_{SS} = $V_{REF}-$ = GND, Clock = 15 MHz Square Wave for CA3306 or CA3306A, 10 MHz for CA3306C .

Parameter		Test Conditions	Limits			Units
			Min	Typ	Max	
Resolution			6			Bits
Integral Linearity Error	3306, 3306C 3306A			±0.25 ±0.2	±0.5 ±0.25	LSB
Differential Linearity Error	3306, 3306C 3306A			±0.25 ±0.2	±0.5 ±0.25	
Quantizing Error		Inherent			±0.5	
Offset Error	3306, 3306C 3306A	(Note 1)		±0.5 ±0.25	±1 ±0.5	
Gain Error	3306, 3306C 3306A	(Note 2)		±0.5 ±0.25	±1 ±0.5	
Positive Full Scale Input Range		(Note 3, 4)	1	4.8	V_{DD} + 0.5	V
Negative Full Scale Input Range		(Note 3, 4)	−0.5	0	V_{DD} − 1	
Input Capacitance				15		pF
Input Current		V_{IN} = 4.92V, V_{DD} = 5V			±500	μA
Resistor Ladder Impedance			650	1100	1550	Ω
Maximum Conversion Speed	3306C 3306, 3306A		10 15	13 20		MSPS
Maximum Conversion Speed	3306C 3306, 3306A	(Note 4) $\phi1$, $\phi2 \geq$ Minimum	12 18			
Auto Balance Time ($\phi1$)	3306C 3306, 3306A		50 33		∞ ∞	ns
Sample Time ($\phi2$)	3306C 3306, 3306A	(Note 4)	33 22		5000 5000	
Aperture Delay				8		
Aperture Jitter				100		ps_{p-p}
Allowable Input Bandwidth		(Note 4)	DC		$f_{CLOCK}/2$	MHz
−3 dB Input Bandwidth				30		
Output Data Valid Delay (T_D)	3306C 3306, 3306A			35 30	50 40	ns
Output Data Hold Time	(T_H)	(Note 4)	15	25		
Output Enable Time	(T_{EN})			20		
Output Disable Time	(T_{DIS})			15		
I_{DD} Current, Refer to Figure 3	3306C 3306, 3306A	Continuous Conversion (Note 4)		11 14	20 25	mA
I_{DD} Current		Continuous $\phi1$		7.5	15	
Maximum V_{IN}, Logic 0		All Digital Inputs (Note 4)			$0.3 \times V_{DD}$	V
Minimum V_{IN}, Logic 1		All Digital Inputs (Note 4)	$0.7 \times V_{DD}$			

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS @ T_A = 25° C, V_{DD} = 5V, $V_{REF}+$ = 4.8V, V_{SS} = $V_{REF}-$ = GND, Clock = 15 MHz Square Wave for CA3306 or CA3306A, 10 MHz for CA3306C (Continued)

Parameter	Test Conditions	Limits			Units
		Min	Typ	Max	
Digital Input Current	Except CLK, V_{IN} = 0V, 5V		±1	±5	μA
Digital Input Current	CLK Only		±100	±200	
Digital Output 3-State Leakage	V_{OUT} = 0V, 5V		±1	±5	
Digital Output Source Current	V_{OUT} = 4.6V	−1.6			mA
Digital Output Sink Current	V_{OUT} = 0.4V	3.2			
Zener Voltage	I_Z = 10 mA	5.4	6.2	7.4	V
Zener Dynamic Impedance	I_Z = 10 mA, 20 mA		12	25	Ω
Gain Temperature Coefficient			+0.1		mV/°C
Offset Temperature Coefficient			−0.1		
Zener Temperature Coefficient			−0.5		

NOTES 1: OFFSET ERROR is the difference between the input voltage that causes the 00 to 01 output code transition and ($V_{REF}+ - V_{REF}-$)/128.

2: GAIN ERROR is the difference the input voltage that causes the $3F_{16}$ to overflow output code transition and ($V_{REF}+ - V_{REF}-$) × 127/128.

3: The total input voltage range, set by $V_{REF}+$ and $V_{REF}-$, may be in the range of 1 to (V_{DD} + 1) V.

4: Parameter not tested, but guaranteed by design or characterization.

ORDERING INFORMATION

Part Number	Linearity (INL, DNL)	Sampling Rate	Temperature Range	Package
CA3306E	±0.5 LSB	15 MHz (67 ns)	-40°C to +85°C	18-Pin Plastic DIP
CA3306AE	±0.25 LSB	15 MHz (67 ns)	-40°C to +85°C	18-Pin Plastic DIP
CA3306CE	±0.5 LSB	10 MHz (100 ns)	-40°C to +85°C	18-Pin Plastic DIP
CA3306M	±0.5 LSB	15 MHz (67 ns)	-40°C to +85°C	20-Pin Plastic SOIC
CA3306CM	±0.5 LSB	10 MHz (100 ns)	-40°C to +85°C	20-Pin Plastic SOIC
CA3306D	±0.5 LSB	15 MHz (67 ns)	-55°C to +125°C	18-Pin Ceramic DIP
CA3306AD	±0.25 LSB	15 MHz (67 ns)	-55°C to +125°C	18-Pin Ceramic DIP
CA3306CD	±0.5 LSB	10 MHz (100 ns)	-55°C to +125°C	18-Pin Ceramic DIP
CA3306J3	±0.5 LSB	15 MHz (67 ns)	-55°C to +125°C	20-Pin LCC
CA3306CJ3	±0.5 LSB	10 MHz (100 ns)	-55°C to +125°C	20-Pin LCC

NOTE: All typical values have been characterized but are not tested.

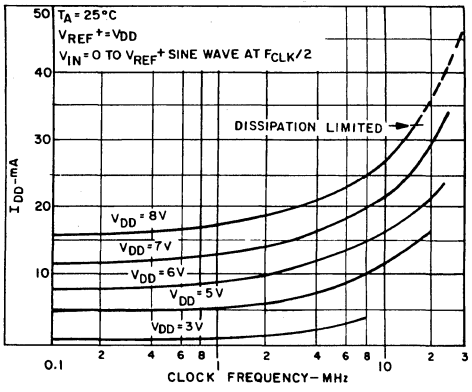


Figure 3: Typical I_{DD} as a Function Of V_{DD}

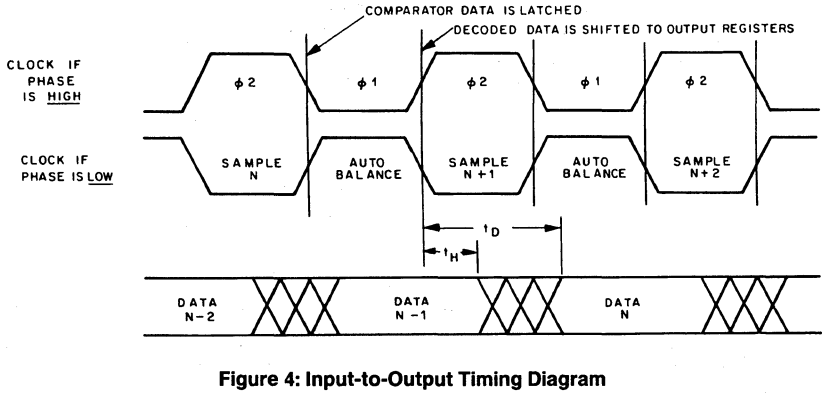


Figure 4: Input-to-Output Timing Diagram

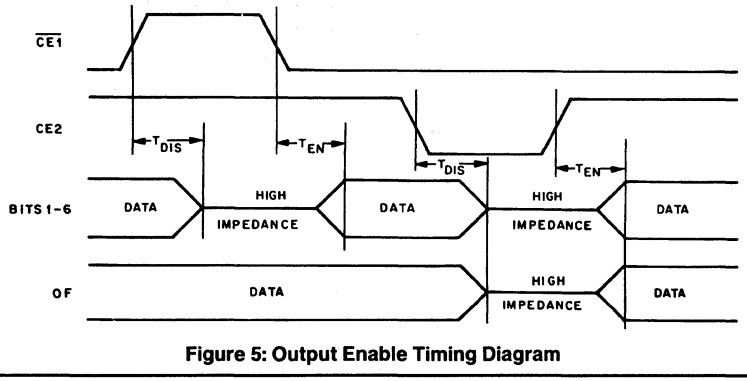
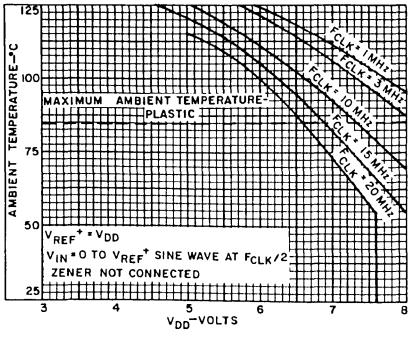


Figure 5: Output Enable Timing Diagram

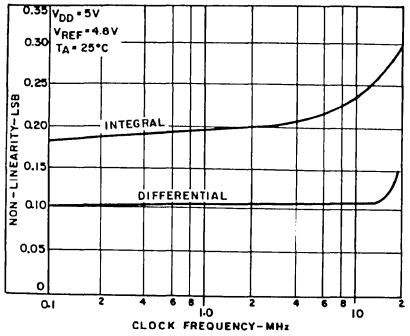
NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS



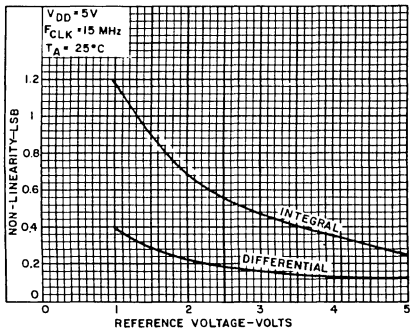
0193-4

Typical Maximum Ambient Temperature as a Function of Supply Voltage



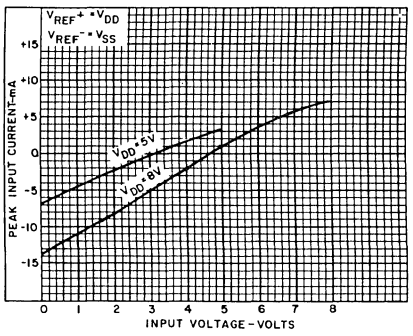
0193-5

Typical Non-Linearity as a Function of Clock Speed



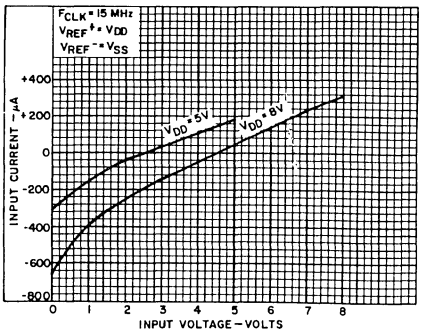
0193-6

Typical Non-Linearity as a Function of Reference Voltage



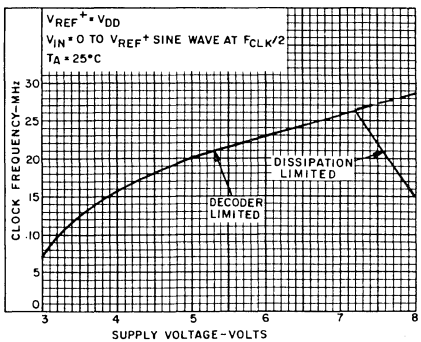
0193-7

Typical Peak Input Current as a Function of Input Voltage



0193-8

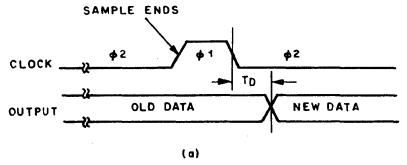
Typical Average Input Current as a Function of Input Voltage



0193-9

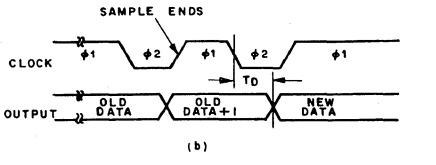
Typical Maximum Clock Frequency as a Function of Supply Voltage

NOTE: All typical values have been characterized but are not tested.



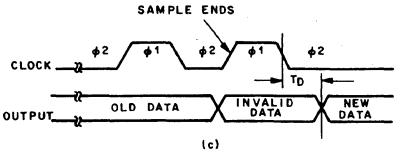
0193-13

With $\phi 2$ as Standby State (Fastest Method but Standby $\leq 5\ \mu s$)



0193-14

With $\phi 1$ as Standby State (Indefinite Standby, Double Pulse Needed)



0193-15

With $\phi 2$ as Standby State (Indefinite Standby, Lower Power Than 6(b)

Figure 6: Pulse-Mode Timing Diagrams

NOTE: Phase Control is low for all diagrams.

Table 1: Pin Description

Pin	Name	Description
1	B6	Bit 6, Output (MSB)
2	OF	Overflow, Output
3	V_{SS}	Digital Ground
4	V_Z	Zener Reference Output
5	CE2	Three-state Output Enable Input, Active Low. See Table 2.
6	$\overline{CE1}$	Three-state Output Enable Input, Active High. See Table 2.
7	CLK	Clock Input
8	PHASE	Sample clock phase control input. When PHASE is low, "Sample Unknown" occurs when the clock is low and "Auto Balance" occurs when the clock is high (see text).
9	V_{REF+}	Reference Voltage Positive Input
10	V_{REF-}	Reference Voltage Negative Input
11	V_{IN}	Analog Signal Input
12	V_{DD}	Power Supply, +5V
13	B1	Bit 1, Output (LSB)
14	B2	Bit 2, Output
15	B3	Bit 3, Output
16	REF (ctr)	Reference Ladder Midpoint
17	B4	Bit 4, Output
18	B5	Bit 5, Output

Table 2: Chip Enable Truth Table

$\overline{CE1}$	CE2	B1-B6	OF
0	1	Valid	Valid
1	1	Three-state	Valid
X	0	Three-state	Three-state

X = don't care

DEVICE OPERATION

A sequential parallel technique is used by the CA3306 converter to obtain its high-speed operation. The sequence consists of the "Auto Balance" phase $\phi 1$ and the "Sample Unknown" phase $\phi 2$. (Refer to the circuit diagram.) Each conversion takes one clock cycle.* With the phase control low, the "Auto Balance" ($\phi 1$) occurs during the High period of the clock cycle, and the "Sample Unknown" ($\phi 2$) occurs during the low period of the clock cycle.

During the "Auto Balance" phase, a transmission-gate switch is used to connect each of 64 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{TAP}(N) = [(V_{REF}/64) \times N] - [V_{REF}/(2 \times 64)]$$
$$= V_{REF}[(2N - 1)/128]$$

Where: $V_{TAP}(N)$ = reference ladder tap voltage at point N
V_{REF} = voltage across V_{REF}^- to V_{REF}^+
N = tap number (1 through 64)

*This device requires only a single-phase clock. The terminology of $\phi 1$ and $\phi 2$ refers to the High and Low periods of the same clock.

NOTE: All typical values have been characterized but are not tested.

DEVICE OPERATION (Continued)

The other side of the capacitor is connected to a single-stage inverting amplifier whose output is shorted to its input by a switch. This biases the amplifier at its intrinsic trip point, which is approximately, $(V_{DD} - V_{SS})/2$. The capacitors now charge to their associated tap voltages, priming the circuit for the next phase.

In the "Sample Unknown" phase, all ladder tap switches are opened, the comparator amplifiers are no longer shorted, and V_{IN} is switched to all 64 capacitors. Since the other end of the capacitor is now looking into an effectively open circuit, any voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators whose tap voltages were lower than V_{IN} will drive the comparator outputs to a "low" state. All comparators whose tap voltages were higher than V_{IN} will drive the comparator outputs to a "high" state. A second, capacitor-coupled, auto-zeroed amplifier further amplifies the outputs.

The status of all these comparator amplifiers are stored at the end of this phase ($\phi 2$), by a secondary latching amplifier stage. Once latched, the status of the 64 comparators is decoded by a 64-to-7-bit decode array and the results are clocked into a storage register at the rising edge of the next $\phi 2$.

A 3-state buffer is used at the output of the 7 storage registers which are controlled by two chip-enable signals. $\overline{CE1}$ will independently disable B1 through B6 when it is in a high state. CE2 will independently disable B1 through B6 and the OF buffers when it is in the low state (Table 2).

To facilitate usage of this device a phase-control input is provided which can effectively complement the clock as it enters the chip. Also, an on-board zener is provided for use as a reference voltage.

Continuous Clock Operation

One complete conversion cycle can be traced through the CA3306 via the following steps. (Refer to timing diagram, Figure 4.) With the phase control in a "High" state, the rising edge of the clock input will start a "sample" phase. During this entire "High" state of the clock, the 64 comparators will track the input voltage and the 64 latches willtrack the comparator outputs. At the falling edge of the clock, after the specified aperture delay, all 64 comparator outputs are captured by the 64 latches. This ends the "sample" phase and starts the "auto balance" phase for the comparators. During this "Low" state of the clock the output of the latches propagates through the decode array and a 7-bit code appears at the D inputs of the output registers. On the next rising edge of the clock, this 7-bit code is shifted into the output registers and appears with time delay t_D as valid data at the output of the 3-state drivers. This also marks the start of a new "sample" phase, thereby repeating the conversion process for this next cycle.

Pulse Mode Operation

For sampling high-speed nonrecurrent or transient data, the converter may be operated in a pulse mode in one of three ways. The fastest method is to keep the converter in the Sample Unknown phase, $\phi 2$, during the standby state. The device can now be pulsed through the Auto Balance phase with a single pulse. The analog value is captured on the leading edge of $\phi 1$ and is transferred into the output registers on the trailing edge of $\phi 1$. We are now back in the standby state, $\phi 2$, and another conversion can be started, but not later than 5μs due to the eventual droop of the commutating capacitors. Another advantage of this method is that it has the potential of having the lowest power drain. The larger the time ratio between $\phi 2$ and $\phi 1$, the lower the power consumption. (See timing diagram, Figure 6.)

The second method uses the Auto Balance phase, $\phi 1$, as the standby state. In this state the converter can stay indefinitely waiting to start a conversion. A conversion is performed by strobing the clock input with two $\phi 2$ pulses. The first pulse starts a Sample Unknown phase and captures the analog value in the comparator latches on the trailing edge. A second $\phi 2$ pulse is needed to transfer the data into the output registers. This occurs on the leading edge of the second pulse. The conversion now takes slightly longer, but the repetition rate may be as slow as desired. The disadvantage to this method is the higher device dissipation due to the low ratio of $\phi 2$ to $\phi 1$. (See timing diagram, Figure 6b.)

For applications requiring both indefinite standby and lowest power, standby can be in the $\phi 2$ (Sample Unknown) state with two $\phi 1$ pulses to generate valid data (see Figure 6c). Valid data now appears two full clock cycles after starting the conversion process.

Analog Input Considerations

The CA3306 input terminal is characterized by a small capacitance (see Specifications) and a small voltage-dependent current (See Typical Performance Characteristics). The signal-source impedance should be kept low, however, when operating the CA3306 at high clock rates.

5

NOTE: All typical values have been characterized but are not tested.

DEVICE OPERATION (Continued)

The CA3306 outputs a short (less than 10 ns) current spike of up to several mA amplitude (See Typical Performance Characteristics) at the beginning of the sample phase. (To a lesser extent, a spike also appears at the beginning of auto balance.) The driving source must recover from the spike by the end of the same phase, or a loss of accuracy will result.

A locally terminated 50Ω or 75Ω source is generally sufficient to drive the CA3306. If gain is required, a high-speed, fast-settling op amp, such as the HA-5033, HA-2542, or CA3450 is recommended.

Digital Input And Output Interfacing

The two chip-enable and the phase-control inputs are standard CMOS units. They should be driven from less than $0.3 \times V_{DD}$ to at least $0.7 \times V_{DD}$. This can be done from 74HC series CMOS (QMOS), TTL with pull-up resistors, or, if V_{DD} is greater than the logic supply, open collector or open drain drivers plus pull-ups. (See Figure 11.)

The clock input is more critical to timing variations, such as $\phi 1$ becoming too short, for instance. Pull-up resistors should generally be avoided in favor of active drivers. The clock input may be capacitively coupled, as it has an internal 50kΩ feedback resistor on the first buffer stage, and will seek its own trip point. A clock source of at least 1 V_{p-p} is adequate, but extremely non-symmetrical waveforms should be avoided.

The output drivers have full rail-to-rail capability. If driving CMOS systems with V_{DD} below the V_{DD} of the CA3306, a CD74HC4050 or CD74HC4049 should be used to step down the voltage. If driving LSTTL systems, no step-down should be necessary, as most LSTTLs will take input swings up to 10V to 15V.

Although the output drivers are capable of handling typical data bus loading, the capacitor charging currents will produce local ground disturbances. For this reason, an external bus driver is recommended.

Increased Accuracy

In most cases the accuracy of the CA3306 should be sufficient without any adjustments. In applications where accuracy is of utmost importance, three adjustments can be made to obtain better accuracy; i.e., offset trim, gain trim, and midpoint trim.

Offset Trim

In general offset correction can be done in the preamp circuitry by introducing a DC shift to V_{IN} or by the offset trim of the op amp. When this is not possible the V_{REF}^- input can be adjusted to produce an offset trim. The theoretical input voltage to produce the first transition is ½ LSB. The equation is as follows:

$$V_{IN} \text{ (0 to 1 transition)} = \tfrac{1}{2} \text{ LSB} = \tfrac{1}{2}(V_{REF}/64)$$
$$= V_{REF}/128$$

If V_{IN} for the first transition is less than the theoretical, then a single-turn 50Ω pot connected between V_{REF}^- and ground will accomplish the adjustment. Set V_{IN} to ½ LSB and trim the pot until the 0 to 1 transition occurs.

If V_{IN} for the first transition is greater than the theoretical, then the 50Ω pot should be connected between V_{REF}^- and a negative voltage of about 2 LSB's. The trim procedure is as stated previously.

Gain Trim

In general the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the op amp. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V_{IN} should be set to the 63 to overflow transition. That voltage is ½ LSB less than V_{REF}^+ and is calculated as follows:

$$V_{IN} \text{ (63 to 64 transition)} = V_{REF} - V_{REF}/128$$
$$= V_{REF} \text{ (127/128)}$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 63 to overflow transition. Now adjust V_{REF}^+ until that transition occurs on the outputs.

Midpoint Trim

The reference center (RC) is available to the user as the midpoint of the resistor ladder. To trim the midpoint, the offset and gain trims should be done first. The theoretical transition from count 31 to 32 occurs at 31½ LSB's. That voltage is as follows:

$$V_{IN} \text{ (31 to 32 transition)} = 31.5\ (V_{REF}/64)$$
$$= V_{REF} \text{ (63/128)}$$

An adjustable voltage follower can be connected to the RC pin or a 2k pot can be connected between V_{REF}^+ and V_{REF}^- with the wiper connected to RC. Set V_{IN} to the 31 to 32 transition voltage, then adjust the voltage follower or the pot until the transition occurs on the output bits.

NOTE: All typical values have been characterized but are not tested.

DEVICE OPERATION (Continued)

The Reference Center point can also be used to create unique transfer functions. The user must remember, however, that there is approximately 120Ω in series with the RC pin.

APPLICATIONS

7-Bit Resolution

To obtain 7-bit resolution, two CA3306s can be wired together. Necessary ingredients include an open-ended ladder network, an overflow indicator, three-state outputs, and chip-enabler controls—all of which are available on the CA3306.

The first step for connecting a 7-bit circuit is to totem-pole the ladder networks, as illustrated in Figure 8. Since the absolute-resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overflow output of the lower device now becomes the seventh bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overflow signal to the $\overline{CE1}$ control of the lower A/D converter and the CE2 control of the upper A/D converter. The three-state outputs of the two devices (bits 1 through 6) are now connected in parallel to complete the circuitry.

Doubled Sampling Speed

The phase control and both positive and negative true chip enables allow the parallel connection of two CA3306s to double the sampling speed. Figure 9 shows this configuration. One converter samples on the positive phase of the clock, and the second on the negative. The outputs are also alternately enabled. Care should be taken to provide a near square-wave clock if operating at close to the maximum clock speed for the devices.

8-Bit to 12-Bit Conversion Techniques

To obtain 8-to-12-bit resolution and accuracy, use a feed-forward conversion technique. Two A/D converters will be needed to convert up to 11 bits; three A/D converters to convert 12 bits. The high speed of the CA3306 allows 12-bit conversions in the 500-to-900 ns range.

The circuit diagram of a high-speed 12-bit A/D converter is shown in Figure 10. In the feed-forward conversion method two sequential conversions are made. Converter A first does a coarse conversion to 6 bits. The output is applied to a 6-bit D/A converter whose accuracy level is good to 12 bits. The D/A converter output is then subtracted from the input voltage, multiplied by 32, and then converted by a second flash A/D converter, which is connected in a 7-bit configuration. The answers from the first and second conversions are added together with bit 1 of the first conversion overlapping bit 7 of the second conversion.

When using this method, take care that:

- The linearity of the first converter is better than ½ LSB.
- An offset bias of 1 LSB ($1/_{64}$) is subtracted from the first conversion since the second converter is unipolar.
- The D/A converter and its reference are accurate to the total number of bits desired for the final conversion (the A/D converter need only be accurate to 6 bits).

The first converter can be offset-biased by adding a 20Ω resistor at the bottom of the ladder and increasing the reference voltage by 1 LSB. If a 6.4V reference is used in the system, for example, then the first CA3306 will require a 6.5V reference.

5

NOTE: All typical values have been characterized but are not tested.

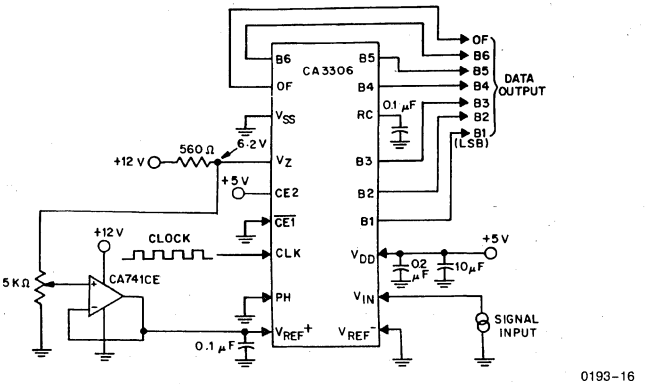


Figure 7: Typical CA3306 6-Bit Configuration, 5V Supply

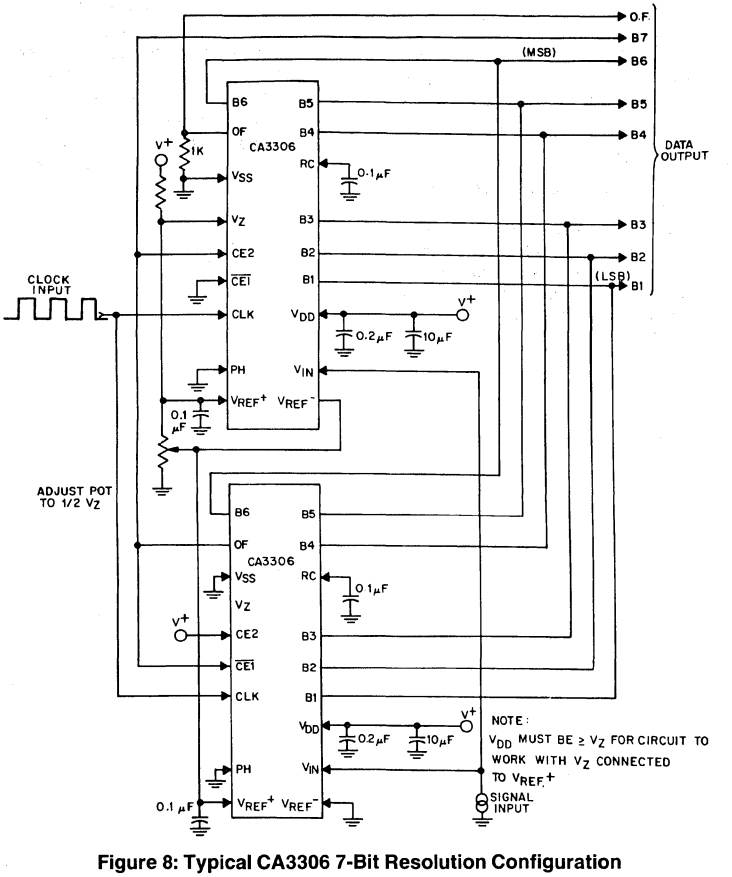


Figure 8: Typical CA3306 7-Bit Resolution Configuration

NOTE: All typical values have been characterized but are not tested.

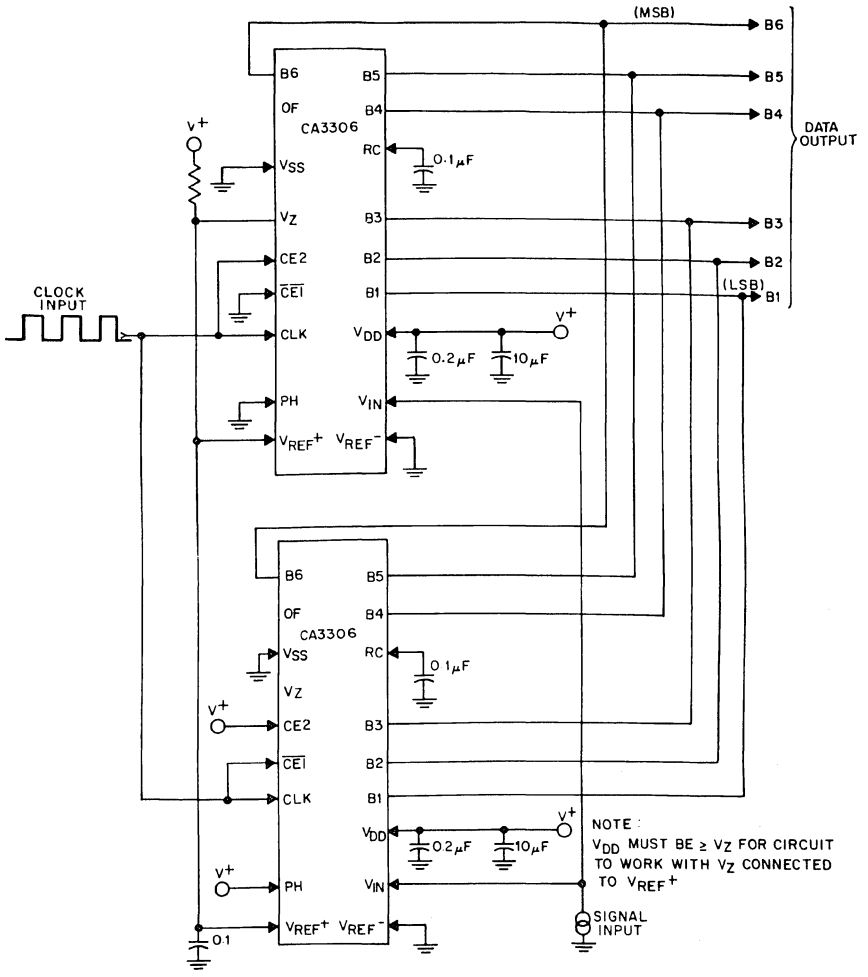


Figure 9: Typical CA3306 6-Bit Resolution Configuration with Double Sampling Rate Capability

NOTE: All typical values have been characterized but are not tested.

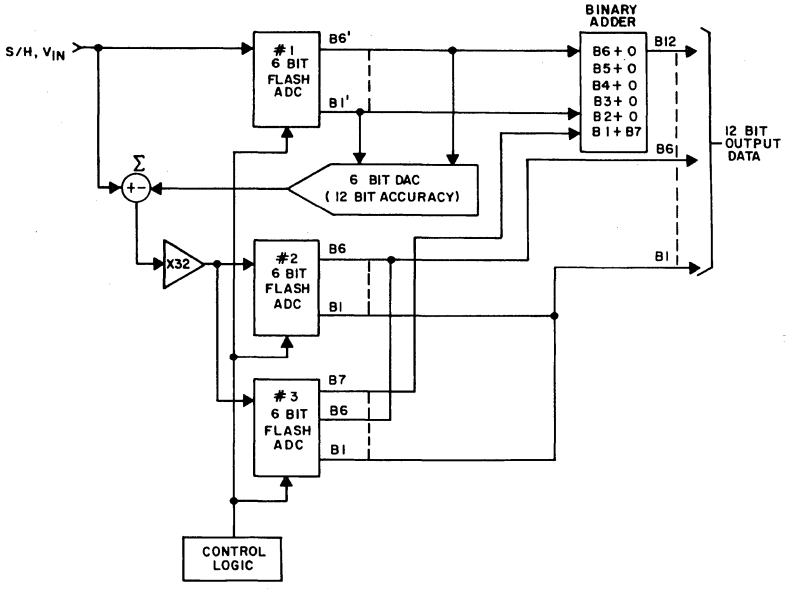


Figure 10: Typical CA3306, 800 ns, 12-Bit ADC System

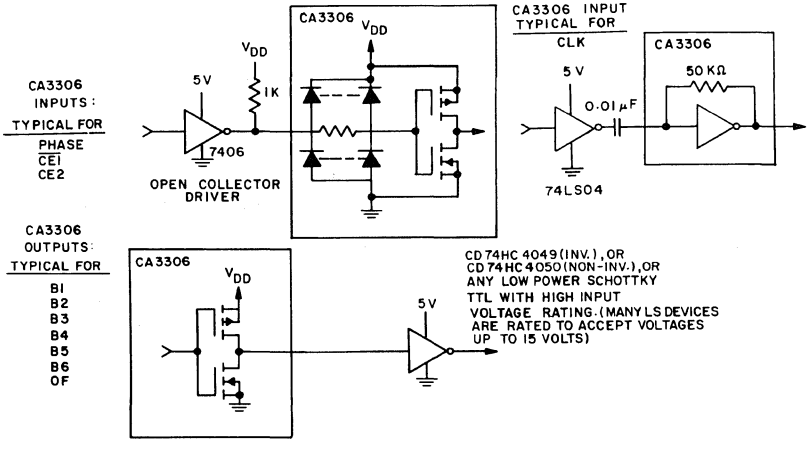


Figure 11: 5V Logic Interface Circuit for V_{DD} > 5.5V

NOTE: All typical values have been characterized but are not tested.

Table 3: Output Code Table

Code Description	Input Voltage* V_{REF} 6.40 (V)	V_{REF} 5.12 (V)	V_{REF} 4.80 (V)	V_{REF} 3.20 (V)	Binary Output Code (LSB) 0F	B6	B5	B4	B3	B2	B1	Decimal Count
Zero	0.00	0.00	0.00	0.00	0	0	0	0	0	0	0	0
1 LSB	0.10	0.08	0.075	0.05	0	0	0	0	0	0	1	1
2 LSB	0.20	0.16	0.15	0.10	0	0	0	0	0	1	0	2
"			"					"				"
"			"					"				"
"			"					"				"
"			"					"				"
½ Full Scale − 1 LSB	3.10	2.48	2.325	1.55	0	0	1	1	1	1	1	31
½ Full Scale	3.20	2.56	2.40	1.60	0	1	0	0	0	0	0	32
½ Full Scale + 1 LSB	3.30	2.64	2.475	1.65	0	1	0	0	0	0	1	33
"			"					"				"
"			"					"				"
"			"					"				"
"			"					"				"
Full Scale − 1 LSB	6.20	4.96	4.65	3.10	0	1	1	1	1	1	0	62
Full Scale	6.30	5.04	4.725	3.15	0	1	1	1	1	1	1	63
Overflow	6.40	5.12	4.80	3.20	1	1	1	1	1	1	1	127

*The voltages listed above are the ideal centers of each output code shown as a function of its associated reference voltage.

OPERATING AND HANDLING CONSIDERATIONS

1. Handling

All inputs and outputs of Harris CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD} - V_{SS}$ to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 20 mA even when the power supply is off. The zener (pin 4) is the only terminal allowed to exceed V_{DD}.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

CA3318C

CMOS Video Speed 8-Bit Flash Analog-to-Digital Converter

GENERAL DESCRIPTION

The Harris CA3318C is a CMOS parallel (FLASH) analog-to-digital converter designed for applications demanding both low-power consumption and high-speed digitization.

The CA3318 operates over a wide full-scale input-voltage range of 4V up to 7.5V with maximum power consumptions depending upon the clock frequency selected. When operated from a 5V supply at a clock frequency of 15 MHz, the typical power consumption of the CA3318 is 150 mW.

The intrinsic high conversion rate makes the CA3318 ideally suited for digitizing high-speed signals. The overflow bit makes possible the connection of two or more CA3318's in series to increase the resolution of the conversion system. A series connection of two CA3318's may be used to produce a 9-bit high-speed converter. Operation of two CA3318's in parallel doubles the conversion speed (i.e., increases the sampling rate from 15 to 30 MHz).

256 paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3318.

255 comparators are required to quantize all input voltage levels in this 8-bit converter, and the additional comparator is required for the overflow bit.

FEATURES

- **CMOS Low Power with SOS Speed (150 mW Typ.)**
- **Parallel Conversion Technique**
- **15-MHz Sampling Rate (67 ns Conversion Time)**
- **8-Bit Latched 3-State Output with Overflow Bit**
- **±1 LSB Accuracy (Typ.)**
- **Single Supply Voltage (4 to 7.5V)**
- **2 Units in Series Allow 9-Bit Output**
- **2 Units in Parallel Allow 30 MHz Sampling Rate**

APPLICATIONS

- **TV Video Digitizing (Industrial/Security/Broadcast)**
- **High-Speed A/D Conversion**
- **Ultrasound Signature Analysis**
- **Transient Signal Analysis**
- **High-Energy Physics Research**
- **High-Speed Oscilloscope Storage/Display**
- **General-Purpose Hybrid ADCs**
- **Optical Character Recognition**
- **Radar Pulse Analysis**
- **Motion Signature Analysis**
- **μP Data Acquisition Systems**

ORDERING INFORMATION

Part Number	Linearity (INL)	Sampling Rate	Temperature Range	Package
CA3318CE	±1.25 LSB	15MHz (67ns)	-40°C to +85°C	24 Pin Plastic DIP
CA3318CM	±1.5 LSB	15MHz (67ns)	-40°C to +85°C	24 Pin Plastic SOIC
CA3318CD	±1.5 LSB	15MHz (67ns)	-40°C to +85°C	24 Pin Ceramic DIP

NOTE: Consult sales office for availability of SOIC package.

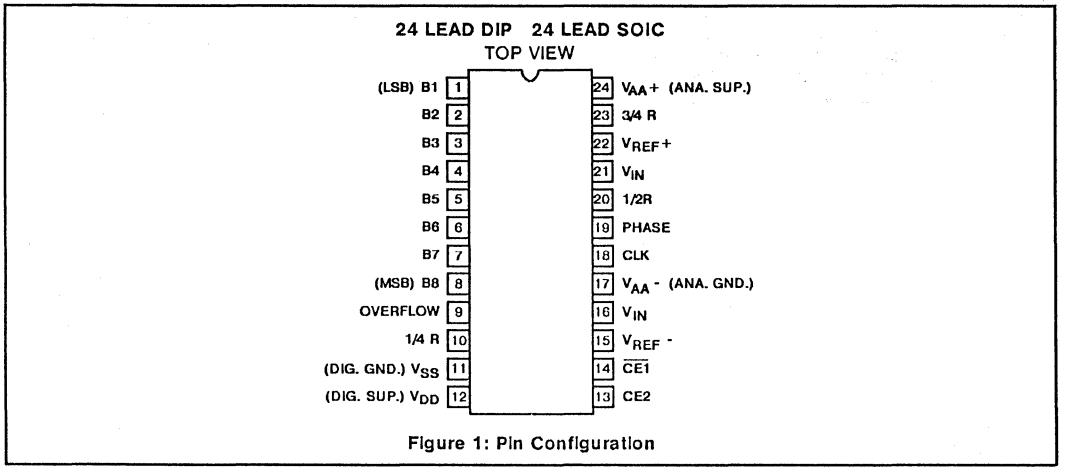


Figure 1: Pin Configuration

1908-002

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage Range (V_{DD} or V_{AA}^+)
(Referenced to V_{SS} or V_{AA}^- Terminal, Whichever is More Negative) ..... −0.5V to +8V

Input Voltage Range
CE2 and $\overline{CE1}$ ..... V_{AA}^- − 0.5V to V_{DD} +0.5V
Clock, Phase, V_{REF}^-,
½ Ref ..... V_{AA}^- − 0.5V to V_{AA}^+ + 0.5V
¼ Ref ..... V_{SS} − 0.5V to V_{DD} + 0.5V
V_{IN}, ¾ REF, V_{REF}^+ ..... V_{AA}^- − 0.5V to V_{AA}^- +7.5V

Output Voltage Range
Bits 1–8, Overflow
(Outputs Off) ..... V_{SS} − 0.5V to V_{DD} + 0.5V

DC Input Current ..... ±20 mA
Clock, Phase, $\overline{CE1}$, CE2, V_{IN}, Bits 1–8, Overflow

Power Dissipation per Package (P_D)
For T_A = −40°C to +55°C ..... 315 mW
For T_A = 55°C to 85°C ..... Derate Linearly at 3.3 mW/°C

Temperature Range
Operating ..... −40°C to +85°C
Storage ..... −65°C to +150°C

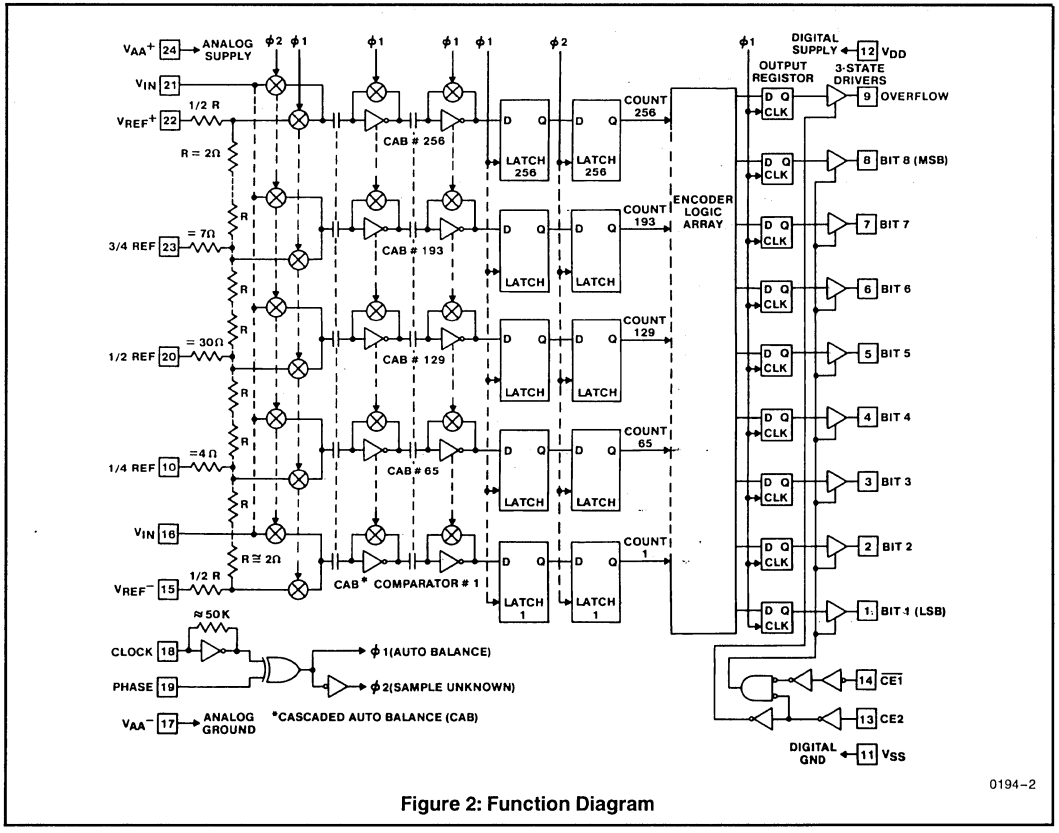
Lead Temperature (During Soldering)
At Distance 1/16 in. ± 1/32 in. (1.59 mm ± 0.79 mm) from Case for 10s Max ..... +265°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Voltage Range (V_{DD} or V_{AA}^+) ..... 4V Min to 7.5V Max

Recommended V_{AA}^+ Operating Range ..... V_{DD} ±1V

Recommended V_{AA}^- Operating Range ..... V_{SS} ±1V



0194-2

Figure 2: Function Diagram

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

Parameter	Test Conditions at 25°C $V_{AA}+ = V_{DD} = 5V$, $V_{REF}+ = 6.4V$, $V_{REF}- = V_{AA}- = V_{SS}$, CLK = 15 MHz, All Ref. Points Adjusted (Unless Otherwise Noted)	Limits			Units
		Min	Typ	Max	
Resolution		8			Bits
Integral Linearity Error				±1.5	LSB
Differential Linearity Error				+1, −0.8	LSB
Quantizing Error				±0.5	LSB
Maximum Input Bandwidth	(Note 1) CA3318C	2.5			MHz
Offset Error, Unadjusted	$V_{IN} = V_{REF}- + ½$ LSB	−0.5	4.5	6.4	LSB
Gain Error Unadjusted	$V_{IN} = V_{REF}+ - ½$ LSB	−1.5	0	1.5	LSB
V_{IN} and $(V_{REF}+) - (V_{REF}-)$ Full Scale Range	(Notes 2, 4)	4		7	V
V_{IN} Input Capacitance			30		pF
V_{IN} Input Current (See Text)	$V_{IN} = 5.0V$, $V_{REF}+ = 5.0V$			3.5	mA
Ladder Impedance		270	500	800	Ω
Max. Conversion Speed	CLK = Square Wave	15	17		MSPS
Auto Balance Time ($\phi 1$)		33		∞	ns
Sample Time ($\phi 2$)	(Note 4)	25		500	ns
Aperture Delay			15		ns
Aperture Jitter			100		pS
Differential Gain Error	Unadjusted		2		%
Differential Phase Error	Unadjusted		1		%
Data Valid Time (T_D)	(Note 4)		50	65	ns
Data Hold Time (T_H)	(Note 4)	25	40		ns
Output Enable Time (T_{EN})			18		ns
Output Disable Time (T_{DIS})			18		ns
Device Current ($I_{DD} + I_{AA}$) (Excludes I_{REF})	Continuous Conversion (Note 4)		30	60	mA
	Auto Balance ($\phi 1$)		30	60	
Digital Inputs:					
Low Level Input Voltage V_{OL}: $\overline{CE1}$, CE2	(Note 4)			0.2 V_{DD}	V
CLK, Phase	(Note 4)			0.2 V_{AA}	V
High Level Input Voltage V_{IN}: $\overline{CE1}$, CE2	(Note 4)	0.7 V_{DD}			V
CLK, Phase	(Note 4)	0.7 V_{AA}			V
Input Leakage Current, I_I: Except CLK Input	(Note 3)		±0.2	±5	μA
Input Capacitance, C_I			3		pF

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued)

Parameter	Test Conditions at 25°C $V_{AA}+ = V_{DD} = 5V$, $V_{REF}+ = 6.4V$, $V_{REF}- = V_{AA}- = V_{SS}$, CLK = 15 MHz, All Ref. Points Adjusted (Unless Otherwise Noted)	Limits			Units
		Min	Typ	Max	
Digital Outputs:					
Output Low (Sink) Current	$V_O = 0.4V$	4	10		mA
Output High (Source) Current	$V_O = 4.5V$	−4	−6		mA
3-State Output Off-State Leakage Current, I_{OZ}			±0.2	±5	μA
Output Capacitance, C_O			4		pF

NOTE 1: A full scale sine wave input of greater than $F_{clock}/2$ or the specified input bandwidth (whichever is less) may cause an erroneous output code. The −3 dB bandwidth for frequency response purposes is greater than 30 MHz.

2: V_{IN} (Full Scale) or $V_{REF}+$ should not exceed $V_{AA}+ + 1.5V$ for accuracy.

3: The clock input is a CMOS inverter with a 50 kΩ feedback resistor and may be AC coupled with 1 V_{p-p} min. source.

4: Parameter not tested, but guaranteed by design or characterization.

Table 1: Pin Description

Pin	Name	Description
1	B1	Bit 1 (LSB)
2	B2	Bit 2
3	B3	Bit 3
4	B4	Bit 4
5	B5	Bit 5
6	B6	Bit 6
7	B7	Bit 7
8	B8	Bit 8 (MSB)
9	OF	Overflow
10	¼ R	Reference Ladder ¼ Point
11	V_{SS}	Digital Ground
12	V_{DD}	Digital Power Supply, +5V
13	CE2	Three-State Output Enable Input, Active Low. See Table 2.
14	$\overline{CE1}$	Three-State Output Enable Input, Active High. See Table 2.
15	$V_{REF}-$	Reference Voltage Negative Input
16	V_{IN}	Analog Signal Input
17	$V_{AA}-$	Analog Ground
18	CLK	Clock Input
19	PHASE	Sample clock phase control input. When PHASE is low, "Sample Unknown" occurs when the clock is low and "Auto Balance" occurs when the clock is high (see text).

Output Data Bits (High = True)

Table 1: Pin Description (Continued)

Pin	Name	Description
20	½ R	Reference Ladder Midpoint
21	V_{IN}	Analog Signal Input
22	$V_{REF}+$	Reference Voltage Positive Input
23	¾ R	Reference Ladder ¾ Point
24	$V_{AA}+$	Analog Power Supply, +5V

Table 2: Chip Enable Truth Table

$\overline{CE1}$	CE2	B1–B8	OF
0	1	Valid	Valid
1	1	Three-State	Valid
X	0	Three-State	Three-State

X = Don't Care

DEVICE OPERATION

A sequential parallel technique is used by the CA3318 converter to obtain its high-speed operation. The sequence consists of the "Auto-Balance" phase, $\phi 1$, and the "Sample Unknown" phase, $\phi 2$. (Refer to the circuit diagram.) Each conversion takes one clock cycle*. With the phase control (pin 19) high, the "Auto-Balance" ($\phi 1$) occurs during the high period of the clock cycle, and the "Sample Unknown" ($\phi 2$) occurs during the low period of the clock cycle.

*This device requires only a single-phase clock. The terminology of $\phi 1$ and $\phi 2$ refers to the high and low periods of the same clock.

NOTE: All typical values have been characterized but are not tested.

During the "Auto-Balance" phase, a transmission switch is used to connect each of the first set of 256 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{tap}(N) = [(N/256)\,V_{REF}] - (1/512)\,V_{REF}]$$
$$= [(2N-1)/512]\,V_{REF}$$

Where:

$V_{tap}(n)$ = reference ladder tap voltage at point n.

V_{REF} = voltage across $V_{REF}-$ to $V_{REF}+$

N = tap number (1 through 256)

The other side of these capacitors are connected to single-stage amplifiers whose outputs are shorted to their inputs by switches. This balances the amplifiers at their intrinsic trip points, which is approximately $(V_{AA}+ - V_{AA}-)/2$. The first set of capacitors now charges to their associated tap voltages.

At the same time a second set of commutating capacitors and amplifiers is also auto-balanced. The balancing of the second-stage amplifier at its intrinsic trip point removes any tracking differences between the first and second amplifier stages. The cascaded auto-balance (CAB) technique, used here, increases comparator sensitivity and temperature tracking.

In the "Sample Unknown" phase, all ladder tap switches and comparator shorting switches are opened. At the same time V_{IN} is switched to the first set of commutating capacitors. Since the other end of the capacitors are now looking into an effectively open circuit, any input voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators that had tap voltages greater than V_{IN} will go to a "high" state at their outputs. All comparators that had tap voltages lower than V_{IN} will go to a "low" state.

The status of all these comparator amplifiers is ac coupled through the second-stage comparator and stored at the end of this phase ($\phi 2$) by a latching amplifier stage. The latch feeds a second latching stage, triggered at the end of $\phi 1$. This delay allows comparators extra settling time. The status of the comparators is decoded by a 256 to 9-bit decoder array, and the results are clocked into a storage register at the end of the next $\phi 2$.

A 3-stage buffer is used at the output of the 9 storage registers which are controlled by two chip-enable signals. $\overline{CE1}$ will independently disable B1 through B8 when it is in a high state. CE2 will independently disable B1 through B8 and the OF buffers when it is in the low state.

To facilitate usage of this device, a phase control input is provided which can effectively complement the clock as it enters the chip.

Continuous-Clock Operation

One complete conversion cycle can be traced through the CA3318 via the following steps. (Refer to timing diagram.) With the phase control in a "low" state, the rising edge of the clock input will start a "sample" phase. During this entire "high" state of the clock, the comparators will track the input voltage and the first-stage latches will track the comparator outputs. At the falling edge of the clock, all 256 comparator outputs are captured by the 256 latches. This ends the "sample" phase and starts the "auto-balance" phase for the comparators. During this "low" state of the clock, the output of the latches settles and is captured by a second row of latches when the clock returns high. The second-stage latch output propagates through the decode array, and a 9-bit code appears at the D inputs of the output registers. On the next falling edge of the clock, this 9-bit code is shifted into the output registers and appears with time delay t_d as valid data at the output of the 3-state drivers. This also marks the end of the next "sample" phase, thereby repeating the conversion process for this next cycle.

Pulse-Mode Operation

The CA3318 needs two of the same polarity clock edges to complete a conversion cycle: If, for instance, a negative going clock edge ends sample "N", then data "N" will appear after the next negative going edge. Because of this requirement, and because there is a maximum sample time of 500 ns (due to capacitor droop), most pulse or intermittent sample applications will require double clock pulsing.

If an indefinite standby state is desired, standby should be in auto-balance, and the operation would be as in Figure 5A.

If the standby state is known to last less than 500ns and lowest average power is desired, then operation could be as in Figure 5B.

Increased Accuracy

In most cases the accuracy of the CA3318 should be sufficient without any adjustments. In applications where accuracy is of utmost importance, five adjustments can be made to obtain better accuracy, i.e., offset trim; gain trim; and 1/4, 1/2 and 3/4 point trim.

NOTE: All typical values have been characterized but are not tested.

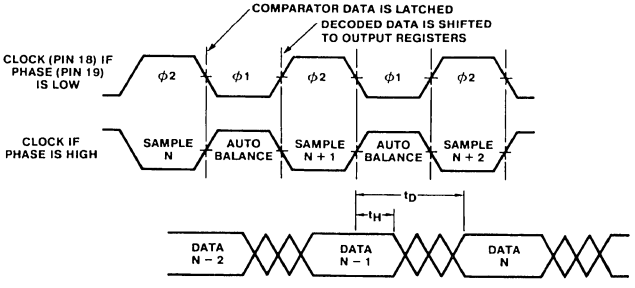


Figure 3: Input to Output Timing Diagram

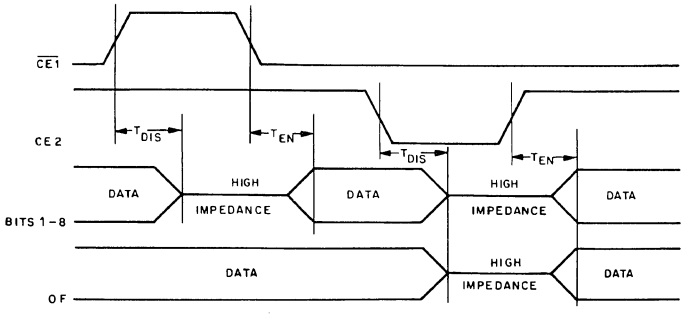
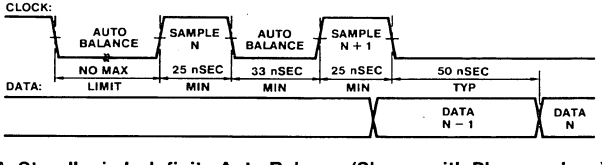
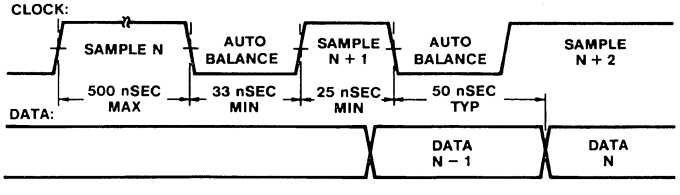


Figure 4: Output Enable Timing Diagram



A: Standby in Indefinite Auto Balance (Shown with Phase = Low)



B: Standby in Sample (Shown with Phase = Low)

Figure 5: Pulse Mode Operation

NOTE: All typical values have been characterized but are not tested.

Offset Trim

In general, offset correction can be done in the preamp circuitry by introducing a dc shift to V_{IN} or by the offset trim of the op amp. When this is not possible the $V_{REF}-$ input can be adjusted to produce an offset trim. The theoretical input voltage to produce the first transition is ½ LSB. The equation is as follows:

$$V_{IN} \text{ (0 to 1 transition)} = ½ \text{ LSB} = ½ (V_{REF}/256) = V_{REF}/512$$

If V_{IN} for the first transition is less than the theoretical, then a single-turn 50Ω pot connected between $V_{REF}-$ and ground will accomplish the adjustment. Set V_{IN} to ½ LSB and trim the pot until the 0-to-1 transition occurs.

If V_{IN} for the first transition is greater than the theoretical, then the 50Ω pot should be connected between $V_{REF}-$ and a negative voltage of about 2 LSB's. The trim procedure is as stated previously.

Gain Trim

In general, the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the op amp. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V_{IN} should be set to the 255 to overflow transition. That voltage is ½ LSB less than $V_{REF}+$ and is calculated as follows:

$$V_{IN} \text{ (255 to 256 transition)} = V_{REF} - V_{REF}/512 = V_{REF} (511/512)$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 255 to overflow transition. Now adjust $V_{REF}+$ until that transition occurs on the outputs.

¼ Point Trims

The ¼, ½ and ¾ points on the reference ladder are brought out for linearity adjusting or if the user wishes to create a non-linear transfer function. The ¼ points can be driven by the reference drivers shown (Figure 7) or by 2-K pots connected between $V_{REF}+$ and $V_{REF}-$. The ½ (mid-) point should be set first by applying an input of 257/512 × (V_{REF}) and adjusting for an output changing from 128 to 129. Similarly the ¼ and ¾ points can be set with inputs of 129/512 and 385/512 × (V_{REF}) and adjusting for counts of 192 to 193 and 64 to 65. (Note that the points are actually ¼, ½ and ¾ of full scale +1 LSB.)

9-Bit Resolution

To obtain 9-bit resolution, two CA3318's can be wired together. Necessary ingredients include an open-ended ladder network, an overflow indicator, three-state outputs, and chip-enable controls—all of which are available on the CA3318.

The first step for connecting a 9-bit circuit is to totem-pole the ladder networks, as illustrated in Figure 8. Since the absolute resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overflow output of the lower device now becomes the ninth bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overflow signal to the $\overline{CE1}$ control of the lower A/D converter and the CE2 control of the upper A/D converter. The three-state outputs of the two devices (bits 1 through 8) are now connected in parallel to complete the circuitry. The complete circuit for a 9-bit A/D converter is shown in Figure 9.

Grounding/Bypassing

The analog and digital supply grounds of a system should be kept separate and only connected at the A/D. This keeps digital ground noise out of the analog data to be converted. Reference drivers, input amps, reference taps, and the V_{AA} supply should be bypassed at the A/D to the analog side of the ground. See Figure 10 for a block diagram of this concept. All capacitors shown should be low impedance 0.1 μF ceramics and should be mounted as close to the A/D as possible. If $V_{AA}+$ is derived from V_{DD}, a small (10Ω resistor or inductor and additional filtering (4.7 μF tantalum) may be used to keep digital noise out of the analog system.

Input Loading

The CA3318 outputs a current pulse to the V_{IN} terminal at the start of every sample period. This is due to capacitor charging and switch feedthrough and varies with input voltage and sampling rate. The signal source must be capable of recovering from the pulse before the end of the sample period to guarantee a valid signal for the A/D to convert. Suitable high speed amplifiers include the HA-5033, HA-2542; and CA3450. Figure 11 is an example of an amplifier which recovers fast enough for sampling at 15 MHz.

Output Loading

The CMOS digital output stage, although capable of driving large loads, will reflect these loads into the local ground. It is recommended that a local QMOS buffer such as CD74HC541E be used to isolate capacitive loads.

NOTE: All typical values have been characterized but are not tested.

Table 3: Output Code Table

Code Description	Input Voltage* V_{REF} 6.40V (V)	Input Voltage* V_{REF} 5.12V (V)	Binary Output Code OF	MSB B8	B7	B6	B5	B4	B3	B2	LSB B1	Decimal Count
Zero	0.00	0.00	0	0	0	0	0	0	0	0	0	0
1 LSB	0.025	0.02	0	0	0	0	0	0	0	0	1	1
2 LSB	0.05	0.04	0	0	0	0	0	0	0	1	0	2
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
¼ Full Scale	1.60	1.28	0	1	0	0	0	0	0	0	0	64
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
½ Full Scale −1 LSB	3.175	2.54	0	0	1	1	1	1	1	1	1	127
½ Full Scale	3.20	2.56	0	1	0	0	0	0	0	0	0	128
½ Full Scale +1 LSB	3.225	2.58	0	1	0	0	0	0	0	0	1	129
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
¾ Full Scale	4.80	3.84	0	1	1	0	0	0	0	0	0	192
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
Full Scale −1 LSB	6.35	5.08	0	1	1	1	1	1	1	1	0	254
Full Scale	6.375	5.10	0	1	1	1	1	1	1	1	1	255
Over Flow	6.40	5.12	1	1	1	1	1	1	1	1	1	511

* The voltages listed above are the ideal centers of each output code shown as a function of its associated reference voltage.

Reducing Power

Most power is consumed while in the auto-balance state. When operating at lower than 15 MHz clock speed, power can be reduced by stretching the sample ($\phi 2$) time. The constraints are a minimum balance time ($\phi 1$) of 33ns, and a maximum sample time of 500ns. Longer sample times cause droop in the auto-balance capacitors. Power can also be reduced in the reference string by switching the reference on only during auto-balance.

Clock Input

The Clock and Phase inputs feed buffers referenced to $V_{AA}+$ and $V_{AA}-$. Phase should be tied to one of these two potentials, while the clock (if DC coupled) should be driven at least from 0.2 to 0.7 $\times$ ($V_{AA}+ - V_{AA}-$). The clock may also be AC coupled with at least a 1 V_{p-p} swing. This allows TTL drive levels or 5V QMOS levels when $V_{AA}+$ is greater than 5V.

NOTE: All typical values have been characterized but are not tested.

CA3318C

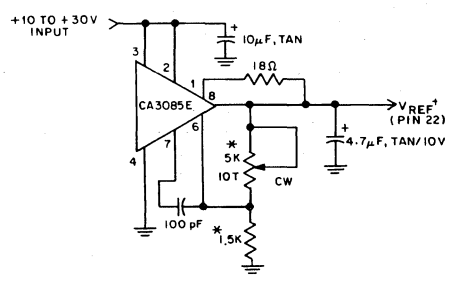


Figure 6: Typical Voltage Reference Source for Driving $V_{REF}+$ Input

NOTE: Bypass $V_{REF}+$ to Analog Ground Near A/D with 0.1 μF Ceramic Cap. Parts Marked (*) Should Have Low Temperature Drift.

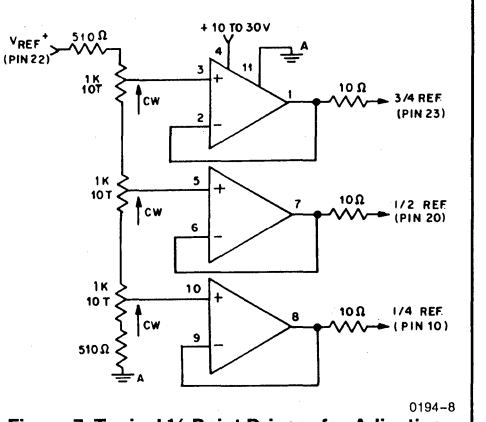


Figure 7: Typical ¼ Point Drivers for Adjusting Linearity (Use for Maximum Linearity)

NOTE: All Op Amps = ¾ CA324E

Bypass All Reference Points to Analog Ground Near A/D with 0.1 μF Ceramic Caps.

Adjust $V_{REF}+$ First, then ½, ¾ and ¼ Points.

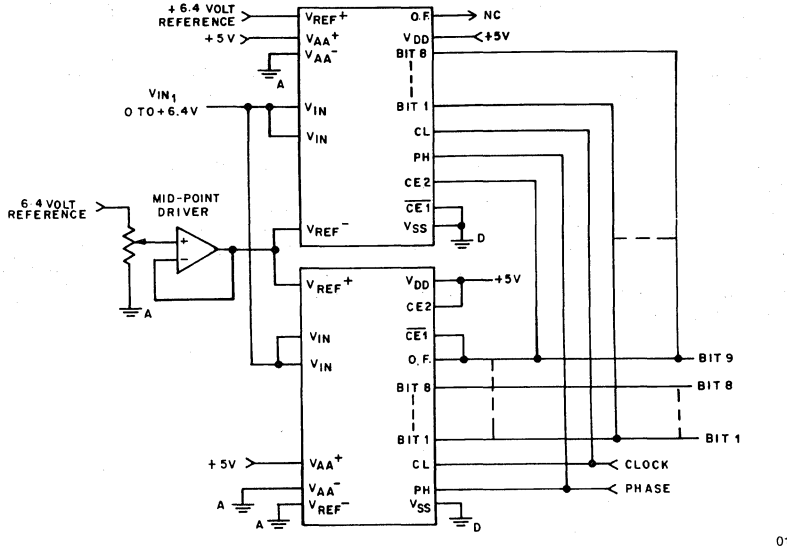


Figure 8: Using two CA3318's for 9-Bit Resolution

NOTE: Reference Taps and V_{AA} Should be Bypassed to AGND with 0.1 μF Low Impedance Caps.

The Mid-Point Driver must be Stable with Capacitive Loads.

NOTE: All typical values have been characterized but are not tested.

CA3318C

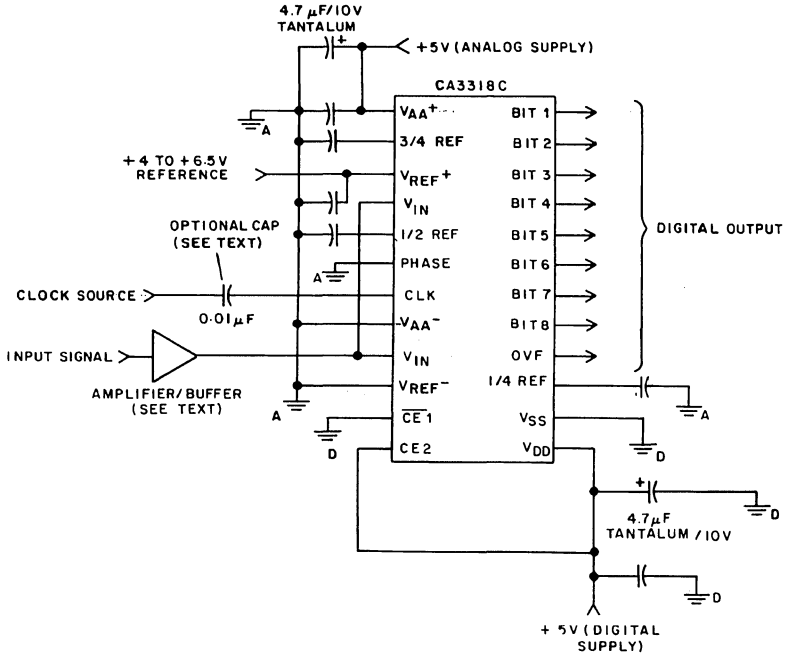


Figure 9: Typical Circuit Configuration for the CA3318 with No Linearity Adjust

NOTE: All Capacitors = 0.1 μF, Low Inductance Ceramic (Unless Noted)

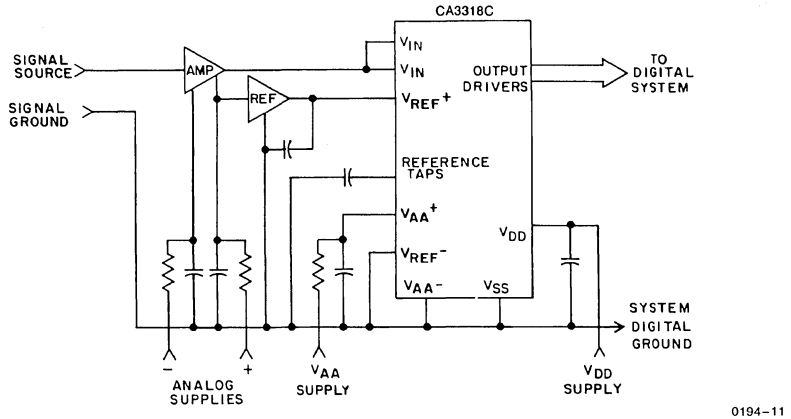


Figure 10: Typical System Grounding/Bypassing

NOTE: All typical values have been characterized but are not tested.

CA3318C

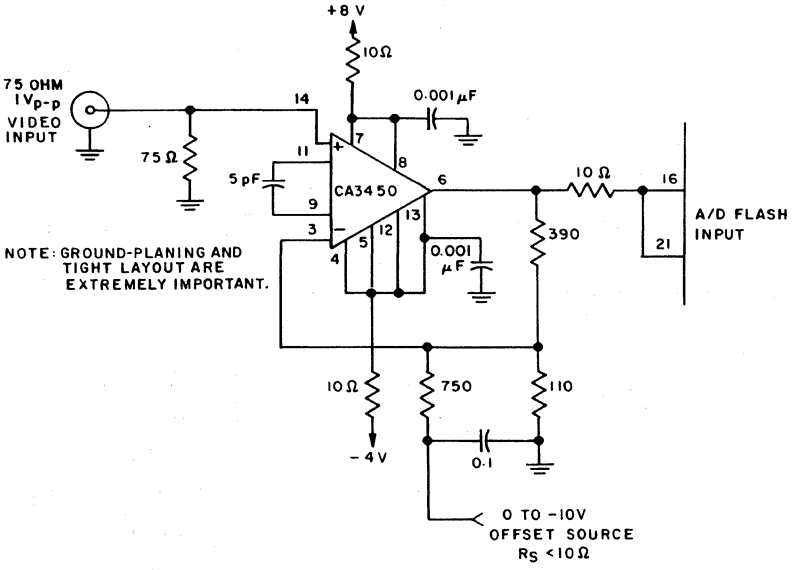


Figure 11: Typical High Bandwidth Amplifier for Driving the CA3318

OPERATING AND HANDLING CONSIDERATIONS

1. **Handling**

   All inputs and outputs for CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525 "Guide to Better Handling and Operation of CMOS Integrated Circuits".

2. **Operating**

   Operating Voltage

   During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause $V_{DD}-V_{SS}$ to exceed the absolute maximum rating.

Input Signals

As shown in the maximum ratings, all inputs except V_{in}, ¾ REF, and $V_{REF}+$ have diodes to V_{DD} or $V_{AA}+$ and from V_{SS} or $V_{AA}-$. V_{in}, ¾ REF, and $V_{REF}+$ have, instead, 10V zener diodes to $V_{AA}-$. No current of greater than 20 mA should be allowed through any of these diodes, even when the supplies are off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

NOTE: All typical values have been characterized but are not tested.

HARRIS HI-5700

PRELIMINARY

April 1990

8 Bit, 20MSPS Flash A/D Converter

Features

- 20MSPS Conversion Rate
- 9MHz Full Power Input Bandwidth
- No Missing Codes
- Sample and Hold Not Required
- ±3/4 LSB Differential Linearity Error (Typical)
- CMOS/TTL Compatible
- Single +5V Supply Voltage
- Improved Replacement for MP7684
  - Higher Operating Frequency
  - Higher Output Drive
  - Lower Leakage Current
  - Lower Reference Current

Applications

- Video Digitizing
- Radar Systems
- Medical Imaging
- Communication Systems
- High Speed Data Acquisition Systems

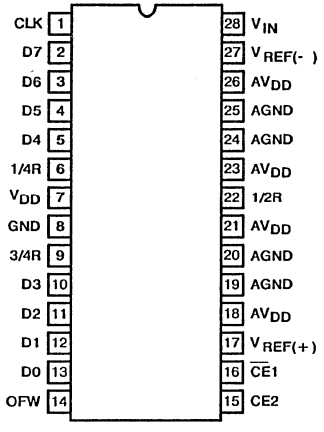
Description

The HI-5700 is a monolithic, 8-bit, CMOS FLASH Analog-to-Digital Converter. Fabricated in the Harris L7 CMOS process, it is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 20MSPS speed is made possible by a parallel architecture which also eliminates the need for an external sample and hold circuit. The HI-5700 delivers ±3/4 LSB differential nonlinearity while consuming only 550mW typically. Latched outputs are provided which present valid data to the output bus one clock cycle after the convert command is received. An overflow bit is provided to allow the series connection of two converters, thus achieving 9-bit resolution.

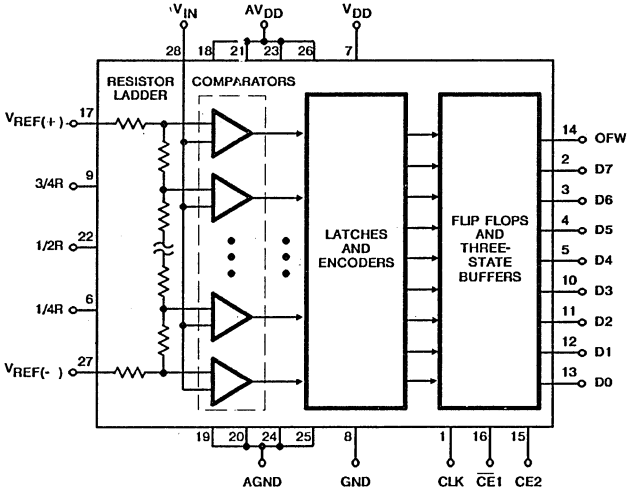
The HI-5700 is available in Commercial and Industrial Temperature ranges. It comes in 28 pin Plastic DIP.

Pinout

28 PIN (PLASTIC DIP)
TOP VIEW



Simplified Block Diagram

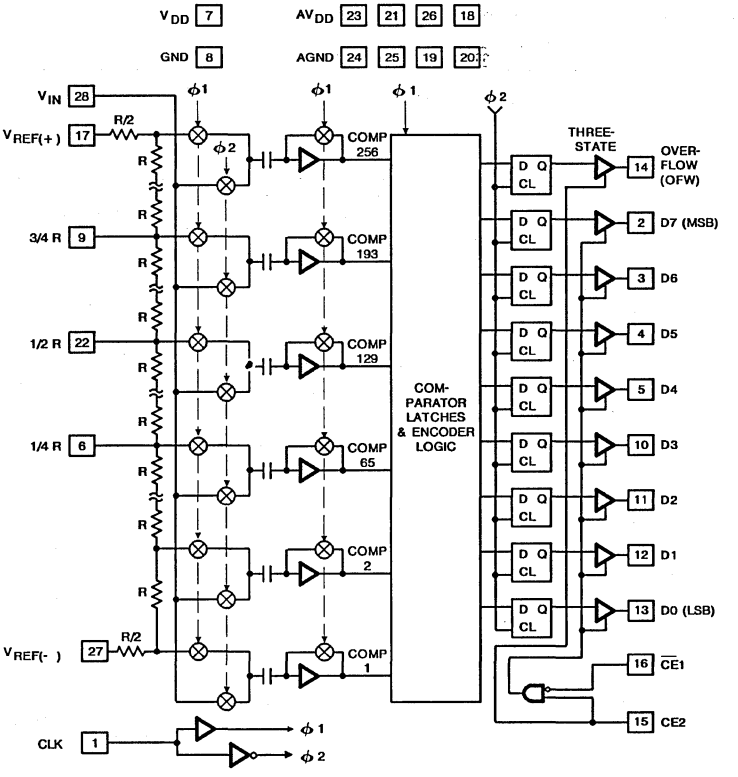


Pin Description

PIN NUMBER	NAME	DESCRIPTION
1	CLK	Clock Input Pin
2	D7	Bit 7 Output (MSB)
3	D6	Bit 6 Output
4	D5	Bit 5 Output
5	D4	Bit 4 Output
6	1/4R	1/4th Point of R Ladder
7	V_{DD}	Power Supply of Digital Circuit
8	GND	Digital Ground
9	3/4R	3/4th Point of R Ladder
10	D3	Bit 3 Output
11	D2	Bit 2 Output
12	D1	Bit 1 Output
13	D0	Bit 0 Output (LSB)
14	OFW	Digital Output Overflow Pin

PIN NUMBER	NAME	DESCRIPTION
15	CE2	Chip Enable Control Pin (See Truth Table)
16	$\overline{CE1}$	Chip Enable Control Pin (See Truth Table)
17	$V_{REF(+)}$	Reference Voltage (+) Input Pin
18	AV_{DD}	Power Supply of Analog Circuit
19	AGND	Analog Circuit Ground
20	AGND	Analog Circuit Ground
21	AV_{DD}	Power Supply of Analog Circuit
22	1/2R	Mid Point of R Ladder
23	AV_{DD}	Power Supply of Analog Circuit
24	AGND	Analog Ground
25	AGND	Analog Ground
26	AV_{DD}	Power Supply of Analog Circuit
27	$V_{REF(-)}$	Reference Voltage (-) Input
28	V_{IN}	Analog Input

Block Diagram



Specifications HI-5700

Absolute Maximum Ratings (Note 1)

V_{DD} to GND 7.0V
AGND to GND ..... ±0.5V
All Other Pins (Max) ..... V_{DD} +0.5V
All Other Pins (Min) ..... GND -0.5V
Total Power Dissipation T_A = -40°C to +85°C 1000mW

Operating Temperature Range

HI-5700 A ..... -40°C to +85°C
HI-5700 J ..... 0°C to +75°C
Junction Temperature ..... +150°C
Storage Temperature ..... -65°C to +150°C

Electrical Specifications: AV_{DD} = V_{DD} = +5.0V; $V_{REF(+)}$ = +4.0V; $V_{REF(-)}$ = GND = AGND = 0V; F_S = Specified Clock Frequency @ 50% Duty Cycle; C_L = 30pF; Full Temperature Range, Unless Otherwise Specified.

PARAMETER (Note 2)		TEST CONDITIONS	HI-5700 A/J MIN	HI-5700 A/J TYP	HI-5700 A/J MAX	UNITS
SYSTEM PERFORMANCE						
Resolution			8	–	–	Bits
Integral Linearity Error (INL)	T_A = +25°C	F_S = 250KHz, f_{in} = 58Hz ramp	–	±¾	±2	LSB
	T_A = Full	F_S = 250KHz, f_{in} = 58Hz ramp	–	–	±2¼	LSB
	T_A = +25°C	F_S = 10MHz, f_{in} = 2.4KHz ramp	–	±1¼	–	LSB
	T_A = +25°C	F_S = 15MHz, f_{in} = 3.5KHz ramp	–	±1¾	–	LSB
	T_A = +25°C	F_S = 20MHz, f_{in} = 4.7KHz ramp	–	±2	–	LSB
	T_A = +25°C	F_S = 25MHz, f_{in} = 5.9KHz ramp	–	±3½	–	LSB
Differential Linearity Error (DNL)	T_A = +25°C	F_S = 250KHz, f_{in} = 58Hz ramp	–	±¾	–	LSB
	T_A = Full	F_S = 250KHz, f_{in} = 58Hz ramp	–	–	+1¾/–1	LSB
	T_A = +25°C	F_S = 10MHz, f_{in} = 2.4KHz ramp	–	±¾	–	LSB
	T_A = +25°C	F_S = 15MHz, f_{in} = 3.5KHz ramp	–	±¾	–	LSB
	T_A = +25°C	F_S = 20MHz, f_{in} = 4.7KHz ramp	–	±9/10	–	LSB
	T_A = +25°C	F_S = 25MHz, f_{in} = 5.9KHz ramp	–	±1¼	–	LSB
Minimum Conversion Rate	T_A = Full	No Missing Codes	–	–	0.125	MSPS
Maximum Conversion Rate	T_A = +25°C	No Missing Codes	–	24	–	MSPS
	T_A = Full	No Missing Codes		19		MSPS
Full Power Input Bandwidth		FS = 14MHz	–	9	–	MHz
Signal to Noise Ratio (SNR)		F_S = 1.0MHz, f_{in} = 100kHz	–	47	–	dB
$= \frac{\text{RMS Signal}}{\text{RMS Noise}}$		F_S = 10MHz, f_{in} = 100kHz	–	47	–	dB
		F_S = 10MHz, f_{in} = 3.0MHz	–	43	–	dB
Signal to Noise Ratio (SINAD)		F_S = 1.0MHz, f_{in} = 100kHz	–	45	–	dB
$= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$		F_S = 10MHz, f_{in} = 100kHz	–	44	–	dB
		F_S = 10MHz, f_{in} = 3.0MHz	–	35	–	dB
Total Harmonic Distortion		F_S =10MHz, f_{in} =100kHz	–	-49	–	dBc
		F_S =10MHz, f_{in} = 3.0MHz	–	-37	–	dBc
Aperture Delay, t_{AP}			–	6	–	ns
Aperture Jitter, t_{AJ}			–	30	–	ps
V_{IO} Error			–	4	6	LSB
Full Scale Error			–	1	3	LSB
SWITCHING CHARACTERISTICS						
Data Output Enable Time, T_{EN}			–	20	–	ns
Data Output Disable Time, T_{DIS}			–	20	–	ns
Data Output Delay, t_{OD}			–	25	–	ns
ELECTRICAL CHARACTERISTICS						
Total Reference Resistance			210	425	560	Ω
Analog Input Resistance			–	10	–	MΩ
Analog Input Capacitance			–	60	–	pF
Analog Input Bias Current		DC	–	0.01	1.0	µA
Input Logic High Voltage, V_{IH}			2.0	–	–	V
Input Logic Low Voltage, V_{IL}			–	–	0.8	V
Input Logic High Current			–	–	1	µA
Input Logic Low Current			–	–	1	µA
Digital Input Capacitance			–	7	–	pF
Output Logic Sink Current, IOL		V_O = 0.4V	–	3	–	mA
Output Logic Source Current, IOH		V_O = 4.6V	–	-3	–	mA
Digital Output Capacitance		CE2 = 0V	–	5	–	pF
Digital Output Leakage		CE2 = 0V	–	–	1	µA
Supply Currrent		F_S = 4MSPS	–	110	–	mA
Supply Current vs. Clock		F_S > 4MSPS	–	2.3	–	mA/MHz
Power Supply Rejection Ratio		5VDC ±10%	–	±1	±3	LSB

NOTES: 1. Absolute Maximum Ratings are limiting values applied individually beyond which the device may be damaged. Functional Operation under any of these conditions is not necessarily implied.

2. See Glossary of Terms.

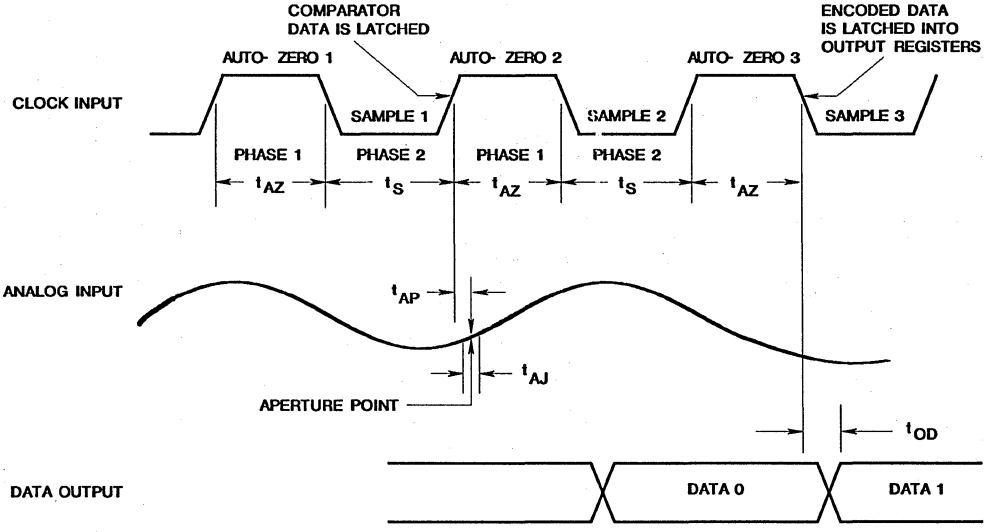
Timing Parameters C_L = 30pF

t_S = Sample Time ..... 25ns ≤ t_S ≤ 5µs
t_{AZ} = Auto Zero Time ..... ≥ 25ns
t_{AP} = Aperture Delay Time ..... ≈ 6ns
t_{AJ} = Aperture Jitter ..... ≈ 30ps
t_{OD} = Data Output Delay..... ≈ 25ns

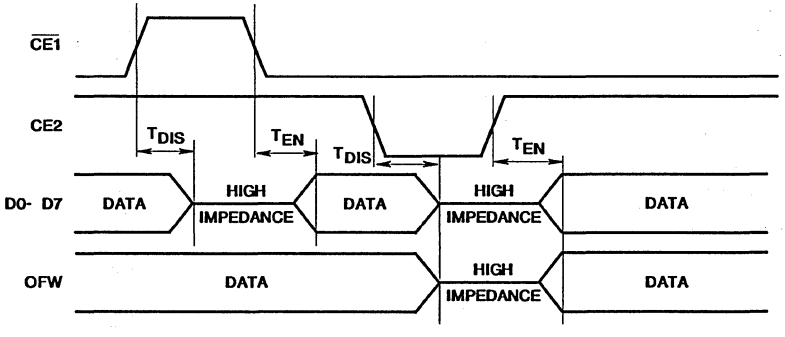
TRUTH TABLE

$\overline{CE1}$	CE2	D0-D7	OFW
0	1	Vallid	Valid
1	1	Hi-Z	Valid
X	0	Hi-Z	Hi-Z

Timing Diagram

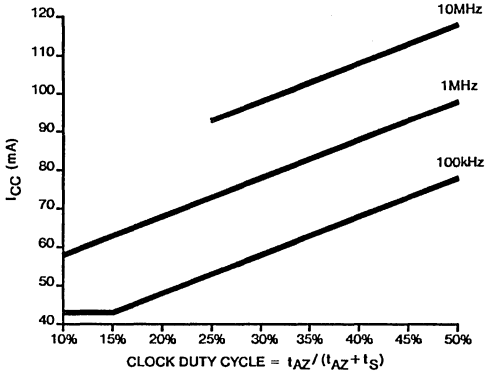


OUTPUT ENABLE TIMING DIAGRAM

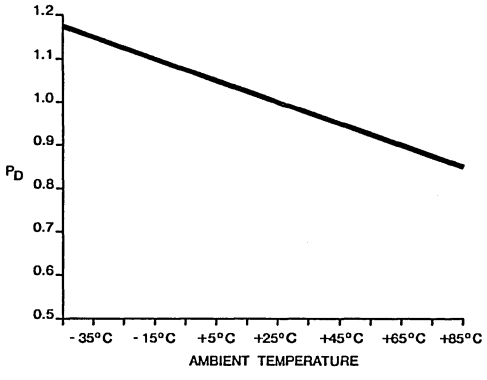


Performance Curves

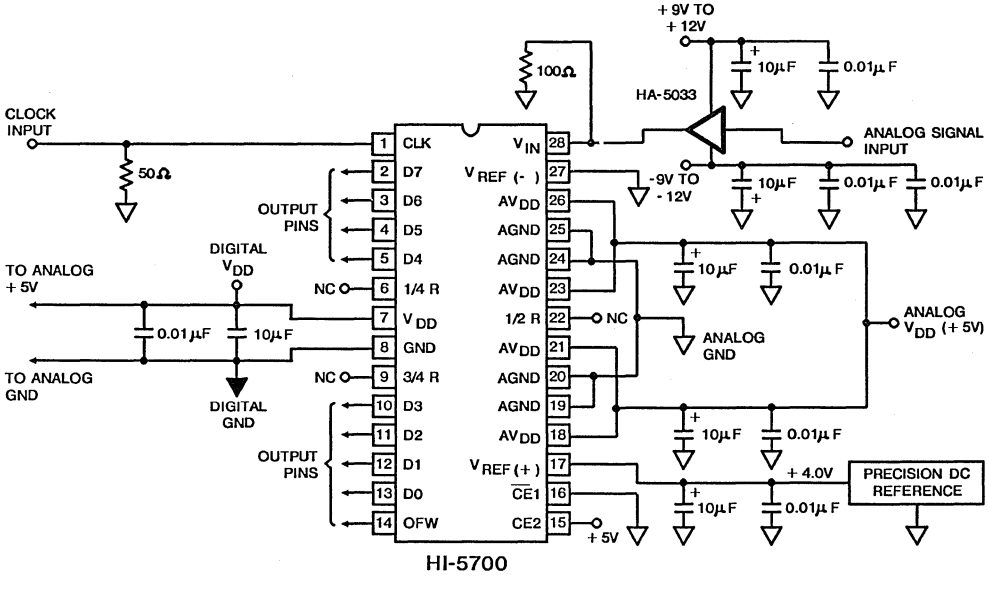
SUPPLY CURRENT vs. CLOCK DUTY CYCLE



NORMALIZED P_D vs. TEMPERATURE



Application Circuit



Theory of Operation

The HI-5700 is an 8-bit analog-to-digital converter based on a parallel CMOS "flash" architecture. This flash technique is an extremely fast method of A/D conversion because all bit decisions are made simultaneously. Very dense circuitry is required to realize this technique, however, since a separate comparator is used to detect each code transition. In all, 256 comparators are used in the HI-5700: (2^8-1) comparators to encode the output word, plus an additional comparator to detect Overflow.

While bipolar flash converters usually compare the input signal to a string of reference voltages in real time, the CMOS HI-5700 works by alternately switching between a "Sample" mode and an "Auto-Zero" mode. Splitting up the comparison process in this CMOS technique offers a number of significant advantages. The offset voltage of each CMOS comparator is dynamically cancelled with each conversion cycle such that offset voltage drift is virtually eliminated during operation. In addition, the power consumption of CMOS circuitry is lower than bipolar, and the input clock may be slowed or completely halted to further reduce power. The block diagram and timing diagram illustrate how the HI-5700 CMOS flash converter operates.

The input clock which controls the operation of the HI-5700 is first split into a non-inverting (Phase 1) clock and an inverting (Phase 2) clock. These two clocks, in turn, synchronize all internal timing of analog switches and control logic within the converter.

In the "Auto-Zero" mode, all "Phase 1" switches close and "Phase 2" switches open. The output of each comparator is momentarily tied to its own input, self-biasing the comparator midway between GND and AV_{DD} and presenting a low impedance to a small input capacitor. Each capacitor, in turn, is connected to a reference voltage tap from the resistor ladder. The Auto-Zero mode quickly pre-charges all 256 input capacitors between the self-bias voltage and each respective tap voltage.

In the "Sample" mode, all "Phase 1" switches open and "Phase 2" switches close. This suddenly places each comparator into a sensitive high-gain amplifier configuration. In this open loop state, the input impedance is very high (like the input of a CMOS gate) and any small voltage shift at the input will now drive the output either high or low. The "Phase 2" state also switches each input capacitor from its reference tap to the input signal. This instantly transfers any voltage difference between the reference tap and input voltage to the comparator input. All 256 comparators are thus driven simultaneously to a defined logic output. For example, if the input voltage is at mid-scale, capacitors pre-charged near zero during "Phase 1" will push comparator inputs higher than the self-bias voltage at "Phase 2"; capacitors pre-charged near the reference voltage push the respective comparator inputs lower than the bias point. In general, all capacitors pre-charged by taps above the input voltage force a "low" voltage at comparator inputs; those pre-charged below the input voltage force "high" inputs at the comparators.

During the next "Phase 1" Auto-Zero state, comparator output data is latched into the encoder logic block and the first stage of encoding takes place. The following "Phase 2" state completes the encoding process. The 8 data bits (plus overflow bit) are latched into the output flip-flops at the next falling clock edge. The Overflow bit is set if the input voltage exceeds ($V_{REF(+)}$-1/2LSB). The output bus may be either enabled or disabled according to the state of $\overline{CE1}$ and CE2 (see Truth Table). When disabled, output bits assume a high impedance state.

As shown in the timing diagram, the digital output word becomes valid after the second "Phase 1" state after sampling. There is thus a one and a half clock cycle delay between input sample and digital output. "Data Output Delay" time indicates the slight time delay for data to become valid the in "Phase 1" state. Refer to the Glossary of Terms for other definitions.

Applications Information

Signal Source

The input to the HI-5700 should be driven by a high output drive amplifier or buffer such as the HA-5033. The signal source must handle significant transient currents from the large dynamic capacitive load that occurs during conversion. The signal source may drive above or below the power supply rails, but should not exceed about 0.5V beyond the rails or damage may occur. Input voltages of -0.5V to 1/2LSB are converted to all zeros; input voltages of ($V_{REF(+)}$-1/2LSB) to (AV_{DD}+0.5V) are converted to all ones with Overflow bit set.

Power Supplies

The HI-5700 operates nominally from 5 volt supplies but will work from 3 volts to 6 volts. Power to the device is split such that analog and digital circuits within the HI-5700 are powered separately. The analog supply should be well regulated and "clean" from significant noise, especially high frequency noise. The digital supply should match the analog supply within about 0.5 volts and should be referenced externally to the analog supply at a single point. Analog and digital grounds should not be separated by more than 0.5 volts. It is recommended that power supply decoupling capacitors be placed as close to the supply pins as possible. A combination of 0.01µF ceramic and 10µF tantalum capacitors are recommended for this purpose as shown in the application circuit schematic.

Reducing Power Consumption

Power dissipation in the HI-5700 is related to clock frequency and clock duty cycle. For a fixed 50% clock duty cycle, power may be reduced by lowering the clock frequency. For given conversion frequency, power may be reduced by reducing the Auto-Zero ("Phase 1") portion of the clock duty cycle (up to the minimum t_{AZ} limit). This relationship is illustrated in the Performance Curves. Power can be minimized by halting the clock in the Sample ("Phase 2") state.

Applications Information (Continued)

Voltage Reference

The reference voltage is applied across the resistor ladder at the input of the converter, between $V_{REF(+)}$ and $V_{REF(-)}$. In most applications, $V_{REF(-)}$ is simply tied to analog ground such that the reference source drives $V_{REF(+)}$. The reference must be capable of supplying enough current to drive the minimum ladder resistance of 210 Ohms over temperature.

The HI-5700 is specified for a reference voltage of 4.0 volts, but will operate with voltages as high as the AV_{DD} supply. In the case of 4.0 volt reference operation, the converter encodes the analog input into a binary output in LSB increments of $(V_{REF(+)} - V_{REF(-)})/256$, or 15.6mV. Reducing the reference voltage reduces the LSB size proportionately and will thus increase linearity errors. The minimum practical reference voltage is about 2.5 volts. Because the reference voltage terminals are subjected to internal transient currents during conversion, it is important to drive the reference pins from a low impedance source and to decouple thoroughly. Again, ceramic and tantalum (0.01µF and 10µF) capacitors near the package pin are recommended. It is not necessary to decouple the 1/4REF, 1/2REF and 3/4REF tap point pins for most applications.

It is possible to elevate $V_{REF(-)}$ from ground if necessary. In this case, the $V_{REF(-)}$ pin must be driven from a low impedance reference capable of sinking the current through the resistor ladder. Careful decoupling is again recommended.

Digital Control and Interface

The HI-5700 provides a standard high speed interface to external CMOS and TTL logic families. Two chip enable inputs control the three-state outputs of output bits D0 through D7 and the Overflow (OFW) bit. As indicated in the Truth Table, all output bits are high impedance when CE2 is low, and output bits D0 through D7 are independently controlled by $\overline{CE1}$.

Clock

The clock should be properly terminated to digital ground near the clock input pin. Clock frequency defines the conversion frequency and controls the converter as described in the "Theory of Operation" section. The Auto-Zero ("Phase 1") half cycle of the clock may be reduced to 25ns; the Sample ("Phase 2") half cycle may be varied from a minimum of 25ns to a maximum of 5µs. Refer to the Timing Parameters table and the Timing Diagram for more information.

Zeroing Full Scale Error and V_{IO} Error

Full Scale Error may be zeroed by adjusting the reference voltage higher or lower such that the 254 to 255 code transition occurs at the ideal location. V_{IO} Error may be adjusted in a similar fashion if a negative reference voltage is used. In this case the negative reference should be adjusted such that the 0 to 1 code transition occures at the ideal location.

Glossary of Terms

Aperture Delay: Aperture delay is the time delay between the external sample command (the rising edge of the clock) and the time at which the signal is actually sampled. This delay is due to clock path propagation delays.

Aperture Jitter: This is the rms variation in the aperture delay due to random noise effects.

Differential Linearity Error: The differential linearity error is the difference in LSBs between the spacing of the measured midpoint of adjacent codes and the spacing of ideal midpoints of adjacent codes. The ideal spacing of each midpoint is 1.0LSB. The range of values that are possible are minimum of -1.0LSB (which implies a missing code) to positive values that can exceed +1.0LSB.

Full Power Input Bandwidth: Full power bandwidth is the frequency at which the amplitude of the fundamental of the digital output word has decreased 3dB below the amplitude of an input sine wave. The input sine wave has a peak to peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Full Scale Error: Full Scale Error is the difference between the actual input voltage of the 254 to 255 code transition and the ideal value of $(V_{REF(+)} - 1.5LSB)$. This error is expressed in LSBs.

Integral Linearity Error: The integral linearity error is the difference in LSBs between the measured code centers and the ideal code centers. The ideal code centers are calculated using a straight line drawn between the endpoints of the converter's transfer function.

LSB: Least Significant Bit = $(V_{REF(+)} - V_{REF(-)})/256$. All HI-5700 specifications are given for a 15.6mV LSB size ($V_{REF(+)} = 4.0V$, $V_{REF(-)} = 0.0V$).

Power Supply Rejection Ratio: PSRR is expressed in LSBs and is the maximum shift in code transition points due to a power supply voltage shift. This is measured at the 0 to 1 code transition point and the 254 to 255 code transition point with a power supply voltage shift from the nominal value of 5.0V.

Signal to Noise Ratio (SNR); The ratio in dB of the rms signal to rms noise at specified input and sampling frequencies.

Signal to Noise Ratio (SINAD): The ratio in dB of the rms signal to the rms sum of the noise and harmonic distortion at specified input and sampling frequencies.

Total Harmonic Distortion (THD): The ratio in dB of the rms sum of the first five harmonic components to the rms signal for a specified input and sampling frequency.

V_{IO} Error: The difference between the actual input voltage of the 0 to 1 code transition and the ideal value of $(V_{REF(-)} + 0.5LSB)$. V_{IO} Error is expressed in LSBs.

DATA ACQUISITION 6

D/A CONVERTERS

CMOS D/A Converters

Type	Res. (Bits)	Settling Time to ½ LSB	Integral Non-Linearity (± %FSR : LSB)	Diff. Non-Linearity (± LSB)	Gain Error (±%FSR)	Output I/V	Input Buffer	Power Supply (V)	Temp. Range (°C)	Comment
AD7523	8	200ns max.	0.2 : ½ 0.1 : ¼ 0.05 : ⅛	Guaranteed monotonic	1.8 max.	I	No	5 to 16	0 to +70 -55 to +125	Multiplying DAC Industry standard
CA3338 CA3338A	8	20ns	0.4 : 1 0.3 : ¾	¾ ½		V	Yes	5	-40 to +85 -55 to +125	Video applications Low glitch
AD7520 AD7530	10	500ns	0.2 : 2 0.1 : 1 0.05 : ½		0.3	I	No	5 to 16	0 to +70 -25 to +85 -55 to +125	Multiplying DAC Industry standard
AD7533	10	800ns max.	0.2 : 2 0.1 : 1 0.05 : ½		1.5 max	I	No	5 to 16	0 to +70	Multiplying DAC Industry standard Low cost
AD7521 AD7531	12	500ns	0.2 : 8 0.1 : 4 0.05 : 2		0.3	I	No	5 to 16	0 to +70 -25 to +85 -55 to +125	Multiplying DAC Industry standard
AD7541	12	1µs max.	0.024 : 1 0.012 : ½ 0.012 : ½	 >½	0.4 max.	I	No	5 to 16	0 to +70 -25 to +85 -55 to +125	Multiplying DAC High performance Industry standard
AD7545	12	2µs max.	0.05 : 2 0.024 : 1 0.012 : ½	4 1 1	0.6 0.4 0.2	I	Yes	5 to 15	0 to +70 -40 to +85 -55 to +125	Mulitplying DAC Industry standard
ICL7134	14	1µs	0.012 : 3/2 0.006 : 1 0.003 : ½	12 Bit 13 mono- 14 tonic	0.024 0.012 0.006	I	Yes double	3.5 to 6.0	0 to +70 -25 to +85 -55 to +125	On-chip PROM Controlled Correction DAC
ICL7121	16	3µs max.	0.009 : 6 0.006 : 4 0.003 : 2 (1 LSB typ.)	14 Bit 15 mono- 16 tonic	0.04 0.02 0.01	I	Yes	4.5 to 5.5	0 to +70 -55 to +125	On-chip PROM Controlled Correction DAC

Bipolar D/A Converters

Type	Res. (Bits)	Settling Time to ½ LSB	Integral Non-Linearity (± %FSR : LSB)	Diff. Non-Linearity (± LSB)	Gain Error (±%FSR)	Output I/V	Input Buffer	Power Supply (V)	Temp. Range (°C)	Comment
ICL8018A ICL8019A	4	200ns (12 bits)	0.01 Maximum absolute error at any 0.1 Input Code			I	No	+5 -15	0 to +70 -55 to +125	4-bit expandable current-switch
HI-562A	12	300ns	0.012 : ½	½	0.024	I	No	+5 -15	0 to +75 -25 to +85 -55 to +125	Industry standard
HI565A	12	350ns	0.012 : ½	¾	0.1	I	No	±12	0 to +75 -55 to +125	On-chip +10V reference
HI-DAC80V	12	1.5µs	0.012 : ½	¾	0.3 max.	V	No	±15	0 to +75	On-chip reference and output op-amp
HI-DAC85V	12	1.5µs	0.012 : ½	½	0.15 max.	V	No	±15	-25 to +85	On-chip reference and output op-amp
HI-DAC16B HI-DAC16C	16	1µs (14 bits)	0.002 : 3/2 0.0045 : 3 (typ.)	1 2 (typ.)	0.1	I	No	±15	0 to +75	High temperature stability

HARRIS SEMICONDUCTOR

AD7520/AD7530 AD7521/AD7531

10/12-Bit Multiplying D/A Converters

GENERAL DESCRIPTION

The AD7520/AD7530 and AD7521/AD7531 are monolithic, high accuracy, low cost 10-bit and 12-bit resolution, multiplying digital-to-analog converters (DAC). Harris' thin-film on CMOS processing gives up to 10-bit accuracy with TTL/CMOS compatible operation. Digital inputs are fully protected against static discharge by diodes to ground and positive supply.

Typical applications include digital/analog interfacing, multiplication and division, programmable power supplies, CRT character generation, digitally controlled gain circuits, integrators and attenuators, etc.

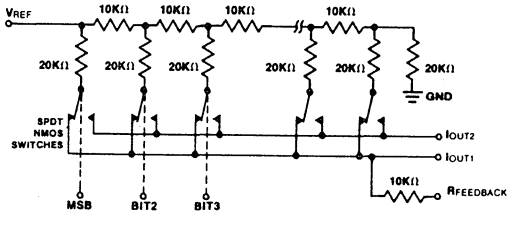
The AD7530 and AD7531 are identical to the AD7520 and AD7521, respectively, with the exception of output leakage current and feedthrough specifications,

FEATURES

- **AD7520/AD7530: 10 Bit Resolution; 8, 9 and 10 Bit Linearity**
- **AD7521/AD7531: 12 Bit Resolution; 8, 9 and 10 Bit Linearity**
- **Low Power Dissipation: 20mW (Max)**
- **Low Nonlinearity Tempco: 2 ppm of FSR/°C**
- **Current Settling Time: 500ns to 0.05% of FSR**
- **Supply Voltage Range: +5V to +15V**
- **TTL/CMOS Compatible**
- **Full Input Static Protection**
- **/883B Processed Versions Available**

ORDERING INFORMATION

Nonlinearity	Part Number/Package		
	Plastic DIP	CERDIP	CERDIP
0.2% (8-Bit)	AD7520JN AD7530JN AD7521JN AD7531JN	AD7520JD	AD7520SD AD7520SD/883B AD7521SD/883B
0.1% (9-Bit)	AD7520KN AD7530KN AD7521KN AD7531KN	AD7520KD	AD7520TD AD7520TD/883B
0.05% (10-Bit)	AD7520LN AD7530LN AD7521LN AD7531LN	AD7520LD	AD7520UD AD7520UD/883B
TEMPERATURE RANGE	0°C to +70°C	−25°C to +85°C	−55°C to +125°C



0330-1

(Switches shown for Digital Inputs "High")
(Resistor values are nominal)
Figure 1: Functional Diagram

300105-004

NOTE: All typical values have been characterized but are not tested.

AD7520/AD7530
AD7521/AD7531

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Supply Voltage (V^+) ..... +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... V^+ to GND
Output Voltage Compliance ..... −100mV to V^+
Power Dissipation (package)
up to +75°C 450mW
derate above +75°C @ ..... 6mW/°C

Operating Temperature
JN, KN, LN Versions ..... 0°C to +70°C
JD, KD, LD Versions ..... −25°C to 85°C
SD, TD, UD Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to 150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

CAUTION:

1) The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

2) Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and $R_{FEEDBACK}$.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

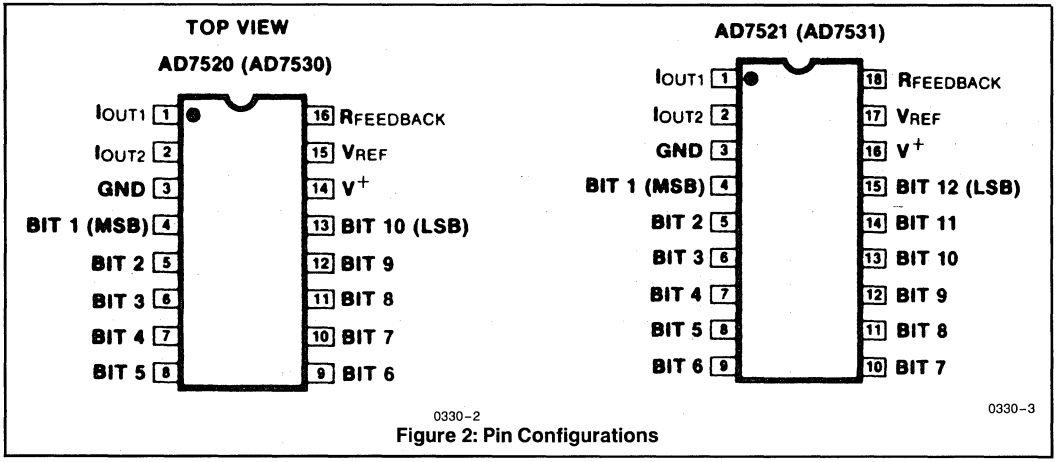


Figure 2: Pin Configurations

ELECTRICAL CHARACTERISTICS ($V^+ = +15V$, $V_{REF} = +10V$, $T_A = 25°C$ unless otherwise specified)

Parameter			Test Conditions		AD7520 (AD7530)	AD7521 (AD7531)	Unit	Limit
DC ACCURACY (Note 1)								
Resolution					10	12	Bits	
Nonlinearity (Note 2)	VERSION	J, S	S, T, U: over −55°C to +125°C	Fig. 3	±0.2 (8-Bit)		% of FSR	Max
		K, T		Fig. 3	±0.1 (9-Bit)		% of FSR	Max
		L, U	−10V ≤ V_{REF} ≤ +10V	Fig. 3	±0.05 (10-Bit)		% of FSR	Max
Nonlinearity Tempco (Notes 2 and 3)			−10V ≤ V_{REF} ≤ +10V		±2		ppm of FSR/°C	Max
Gain Error (Note 2)					±0.3		% of FSR	Typ
Gain Error Tempco (Notes 2 and 3)					±10		ppm of FSR/°C	Max

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS ($V^+ = +15V$, $V_{REF} = +10V$, $T_A = 25°C$ unless otherwise specified) (Continued)

Parameter		Test Conditions		AD7520 (AD7530) / AD7521 (AD7531)	Unit	Limit
Output Leakage Current (either output)		Over the specified temperature range		±200 (±300)	nA	Max
Power Supply Rejection (Note 2)			Fig. 4	±0.005	% FSR/% ΔV^+	Typ
AC ACCURACY (Note 3)						
Output Current Settling Time		To 0.05% of FSR (All digital inputs low to high and high to low)	Fig. 8	500	ns	Typ
Feedthrough Error		V_{REF} = 20V pp, 100kHz (50kHz) All digital inputs low	Fig. 7	10	mV pp	Max
REFERENCE INPUT						
Input Resistance		All digital inputs high I_{OUT1} at ground.		5k 10k 20k	Ω	Min Typ Max
ANALOG OUTPUT						
Voltage Compliance (both outputs)		(Note 3)		See absolute max. ratings		
Output Capacitance (Note 3)	I_{OUT1} I_{OUT2}	All digital inputs high	Fig. 6	120 37	pF pF	Typ Typ
	I_{OUT1} I_{OUT2}	All digital inputs low	Fig. 6	37 120	pF pF	Typ Typ
Output Noise (both outputs) (Note 3)			Fig. 5	Equivalent to 10kΩ Johnson noise		Typ
DIGITAL INPUTS						
Low State Threshold		Over the specified temp range		0.8	V	Max
High State Threshold				2.4	V	Min
Input Current (V_{IN} = 0V or +15V)				±1	μA	Max
Input Coding		See Tables 1 & 2		Binary/Offset Binary		
POWER REQUIREMENTS						
Power Supply Voltage Range				+5 to +15	V	
I^+ (Excluding Ladder Network)		All digital inputs at 0V or V^+		±1	μA	Typ
		All digital inputs high or low		2	mA	Max
Total Power Dissipation (Including the ladder network)				20	mW	Typ

NOTES: **1.** Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design, not subject to test.
4. Accuracy not guaranteed unless outputs at GND potential.

NOTE: All typical values have been characterized but are not tested.

TEST CIRCUITS

NOTE: The following test circuits apply for the AD7520. Similar circuits are used for the AD7530, AD7521 and AD7531.

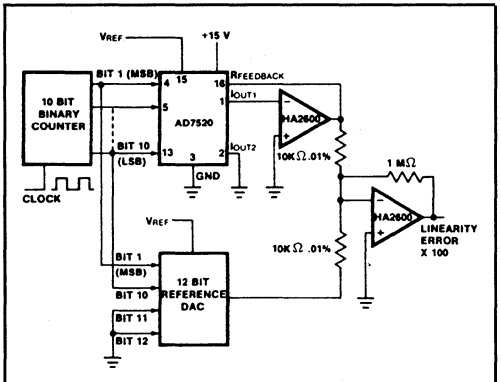


Figure 3: Nonlinearity

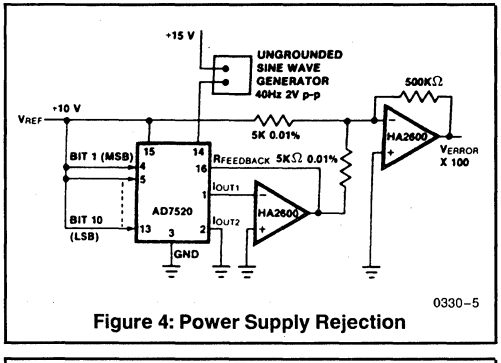


Figure 4: Power Supply Rejection

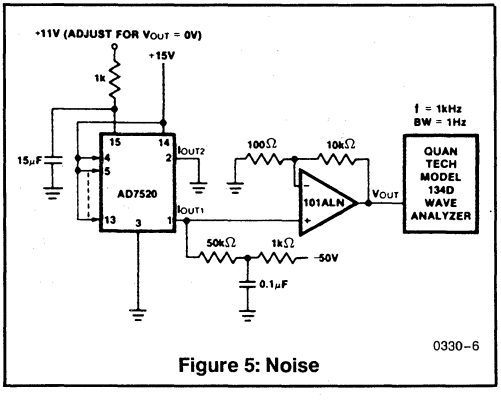


Figure 5: Noise

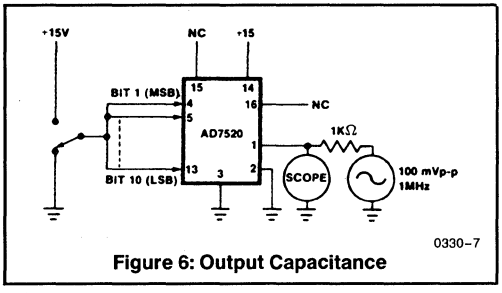


Figure 6: Output Capacitance

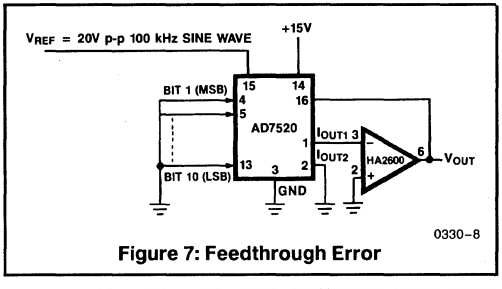


Figure 7: Feedthrough Error

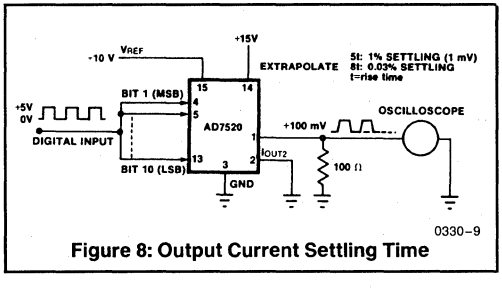


Figure 8: Output Current Settling Time

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a "best straight line" through the actual plot of transfer function. Normally expressed as a percentage of full scale range or in (sub)multiples of 1 LSB.

RESOLUTION: It is addressing the smallest distinct analog output change that a D/A converter can produce. It is commonly expressed as the number of converter bits. A converter with resolution of n bits can resolve output changes of 2^{-n} of the full-scale range, e.g. 2^{-n} V_{REF} for a unipolar conversion. Resolution by no means implies linearity.

SETTLING TIME: Time required for the output of a DAC to settle to within specified error band around its final value (e.g. ½ LSB) for a given digital input change, i.e. all digital inputs LOW to HIGH and HIGH to LOW.

GAIN ERROR: The difference between actual and ideal analog output values at full-scale range, i.e. all digital inputs at HIGH state. It is expressed as a percentage of full-scale range or in (sub)multiples of 1 LSB.

NOTE: All typical values have been characterized but are not tested.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to I_{OUT1} with all digital inputs LOW.

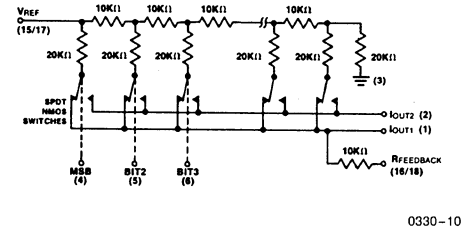
OUTPUT CAPACITANCE: Capacitance from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal when all digital inputs are LOW or on I_{OUT2} terminal when all digital inputs are HIGH.

DETAILED DESCRIPTION

The AD7520, AD7530, AD7521 and AD7531 are monolithic, multiplying D/A converters. A highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit, CMOS level shifters permit low power TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 9. The NMOS SPDT switches steer the ladder leg currents between I_{OUT1} and I_{OUT2} buses which must be held either at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.



(Switches shown for Digital Inputs "High")

Figure 9: AD7520/21/30/31 Functional Diagram

Converter errors are further reduced by using separate metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 10). This configuration results in TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an ON resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors and highly accurate leg currents.

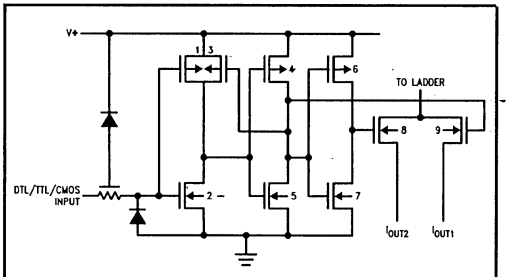


Figure 10: CMOS Switch

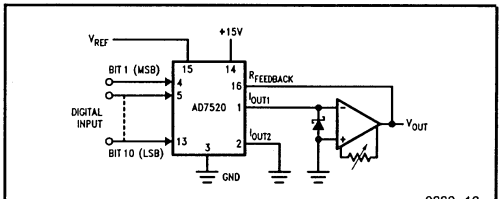


Figure 11: Unipolar Binary Operation (2-Quadrant Multiplication)

TABLE 1
CODE TABLE — UNIPOLAR BINARY OPERATION

Digital Input	Analog Output
1111111111	$-V_{REF}(1-2^{-n})$
1000000001	$-V_{REF}(1/2+2^{-n})$
1000000000	$-V_{REF}/2$
0111111111	$-V_{REF}(1/2-2^{-n})$
0000000001	$-V_{REF}(2^{-n})$
0000000000	0

NOTE: 1. $LSB = 2^{-n} V_{REF}$
2. n = 10 for 7520, 7530
n = 12 for 7521, 7531

APPLICATIONS

Unipolar Binary Operation

The circuit configuration for operating the AD7520 in unipolar mode is shown in Figure 11. Similar circuits can be used for AD7521, AD7530 and AD7531. With positive and negative V_{REF} values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1.

NOTE: All typical values have been characterized but are not tested.

ZERO OFFSET ADJUSTMENT

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V at V_{OUT}.

GAIN ADJUSTMENT

1. Connect all digital inputs to V+.
2. Monitor V_{OUT} for a $-V_{REF}$ (1-2^{-n}) reading. (n = 10 for AD7520/30 and n = 12 for AD7521/31).
3. To decrease V_{OUT}, connect a series resistor (0 to 250Ω) between the reference voltage and the V_{REF} terminal.
4. To increase V_{OUT}, connect a series resistor (0 to 250Ω) in the I_{OUT1} amplifier feedback loop.

Bipolar (Offset Binary) Operation

The circuit configuration for operating the AD7520 in the bipolar mode is given in Figure 12. Similar circuits can be used for AD7521, AD7530 and AD7531. Using offset binary digital input codes and positive and negative reference voltage values, 4-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

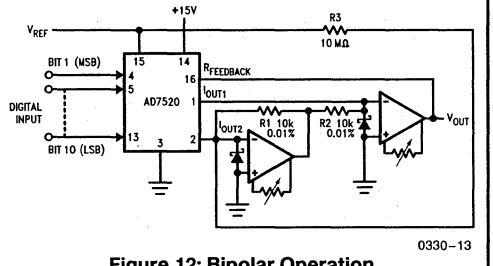


Figure 12: Bipolar Operation (4-Quadrant Multiplication)

TABLE 2
CODE TABLE — BIPOLAR (OFFSET BINARY) OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}(1-2^{-(n-1)})$
1000000001	$-V_{REF}(2^{-(n-1)})$
1000000000	0
0111111111	$V_{REF}(2^{-(n-1)})$
0000000001	$V_{REF}(1-2^{-(n-1)})$
0000000000	V_{REF}

NOTE: 1. LSB = $2^{-(n-1)}$ V_{REF}
2. n = 10 for 7520 and 7521
= 12 for 7530 and 7531

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to I_{OUT1} bus. A "Logic 0" input forces the bit current to I_{OUT2} bus. For any code the I_{OUT1} and I_{OUT2} bus currents are complements of one another. The current amplifier at I_{OUT2} changes the polarity of I_{OUT2} current and the transconductance amplifier at I_{OUT1} output sums the two currents. This configuration doubles the output range. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistor, (10 Megohm), from V_{REF} to I_{OUT2}.

OFFSET ADJUSTMENT

1. Adjust V_{REF} to approximately +10V.
2. Connect all digital inputs to "Logic 1".
3. Adjust I_{OUT2} amplifier offset adjust trimpot for 0V ±1mV at I_{OUT2} amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust I_{OUT1} amplifier offset adjust trimpot for 0V ±1 mV at V_{OUT}.

GAIN ADJUSTMENT

1. Connect all digital inputs to V+.
2. Monitor V_{OUT} for a $-V_{REF}$ (1-2$^{-(n-1)}$) volts reading. (n = 10 for AD7520 and AD7530, and n = 12 for AD7521 and AD7531).
3. To increase V_{OUT}, connect a series resistor of up to 250Ω between V_{OUT} and $R_{FEEDBACK}$.
4. To decrease V_{OUT}, connect a series resistor of up to 250Ω between the reference voltage and the V_{REF} terminal.

NOTE: All typical values have been characterized but are not tested.

Analog/Digital Division

With the AD7520 connected in its normal multiplying configuration as shown in Figure 11, the transfer function is:

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}\right)$$

where the coefficients A_x assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 13, the transfer function becomes:

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero isn't defined. With the LSB (Bit-10) ON, the gain is 1023. With all bits ON, the gain is 1 (±1 LSB).

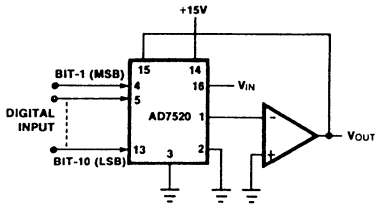


Figure 13: Analog/Digital Divider

For further information on the use of this device, see the following Application Bulletins:

A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood

A002 "Principles of Data Acquisition and Conversion".

A042 "Interpretation of Data Converter Accuracy Specifications".

6

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

AD7523
8-Bit Multiplying D/A Converter

GENERAL DESCRIPTION

The AD7523 is a monolithic, low cost, high performance, 10 bit accurate, multiplying digital-to-analog converter (DAC), in a 16-pin DIP.

Harris' thin-film resistors on CMOS circuitry provide 8-bit resolution (8, 9 and 10-bit accuracy), with TTL/CMOS compatible operation.

The AD7523's accurate four quadrant multiplication, full military temperature range operation, full input protection from damage due to static discharge by clamps to V+ and GND, and very low power dissipation make it a very versatile converter.

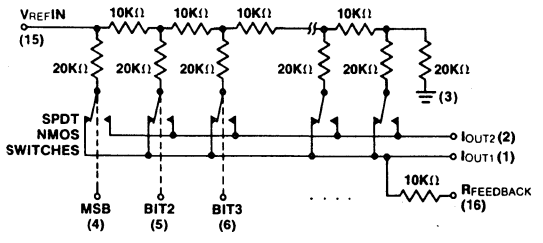
Low noise audio gain controls, motor speed controls, digitally controlled gain and attenuators are a few of the wide range of applications of the 7523.

FEATURES

- **8, 9 and 10 Bit Linearity**
- **Low Gain and Linearity Temperature Coefficients**
- **Full Temperature Range Operation**
- **Static Discharge Input Protection**
- **DTL/TTL/CMOS Compatible**
- **+5 to +15 Volts Supply Range**
- **Fast Settling Time: 150ns Max at 25°C**
- **Four Quadrant Multiplication**

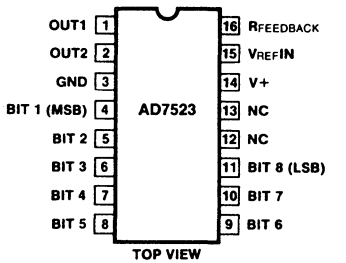
ORDERING INFORMATION

Nonlinearity	Part Number/Package	
	Plastic DIP	CERDIP
0.2% (8 Bit)	AD7523JN	
0.1% (9 Bit)	AD7523KN	AD7523TD/HR
0.05% (10 Bit)	AD7523LN	
TEMPERATURE RANGE	0°C to +70°C	−55°C to +125°C



0331-1

Figure 1: Functional Diagram (Switches shown for Digital Inputs "High")



0331-2

Figure 2: Pin Configuration

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

Supply Voltage (V^+) ..... +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... V^+ to GND
Output Voltage Compliance ..... −100mV to V^+
Power Dissipation:
Plastic Package —
up to +70°C 670mW
derate above +70°C by ..... 8.3mW/°C
Ceramic Package —
up to 75°C 450mW
derate above 75°C by ..... 6mW/°C
Operating Temperatures
JN, KN, LN Versions ..... 0°C to +70°C
TD Version ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

CAUTION:

1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

2. Do not apply voltages higher than VDD and lower than GND to any terminal except $V_{REF} + R_{FEEDBACK}$.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

($V^+ = +15V$, $V_{REF} = +10V$, $V_{OUT1} = V_{OUT2} = 0V$ unless otherwise specified)

Parameter			Test Conditions	T_A +25°C	T_A Min–Max	Unit	Limit
DC ACCURACY (Note 1)							
Resolution				8	8	Bits	Min
Nonlinearity (Note 2)	J		$-10V \le V_{REF} \le +10V$ $V_{OUT1} = V_{OUT2} = 0V$	±0.2	±0.2	% of FSR	Max
	K	T		±0.1	±0.1	% of FSR	Max
	L			±0.05	±0.05	% of FSR	Max
Monotonicity				Guaranteed			
Gain Error (Note 2)			All Digital Inputs high.	±1.5	±1.8	% of FSR	Max
Nonlinearity Tempco (Notes 2 and 3)			$-10V\ V_{REF}\ +10V$	±2		ppm of FSR/°C	Max
Gain Error Tempco (Notes 2 and 3)				±10		ppm of FSR/°C	Max
Output Leakage Current (either output)			$V_{OUT1} = V_{OUT2} = 0$	±50	±200	nA	Max
AC ACCURACY							
Power Supply Rejection (Note 2)			$V^+ = 14.0$ to 15.0V	±0.02	±0.03	% of FSR/% ΔV^+	Max
Output Current Settling Time (Note 3)			To 0.2% of FSR, $R_L = 100\Omega$	150	200	ns	Max
Feedthrough Error (Note 3)			V_{REF} = 20V pp, 200kHz sine wave. All digital inputs low.	±½	±1	LSB	Max
REFERENCE INPUT							
Input Resistance (Pin 15)			All digital inputs high. I_{OUT1} at ground.	5K		Ω	Min
				20K			Max
Temperature Coefficient (Note 3)				−500		ppm/°C	Max
ANALOG OUTPUT							
Output Capacitance (Note 3)	C_{OUT1}		All digital inputs high	100		pF	Max
	C_{OUT2}			30		pF	Max
	C_{OUT1}		All digital inputs low	30		pF	Max
	C_{OUT2}			100		pF	Max

NOTE: All typical values have been characterized but are not tested.

AD7523

ELECTRICAL CHARACTERISTICS

($V^+ = +15V$, $V_{REF} = +10V$, $V_{OUT1} = V_{OUT2} = 0V$ unless otherwise specified) (Continued)

Parameter	Test Conditions	T_A +25°C	T_A Min-Max	Unit	Limit
DIGITAL INPUTS					
Low State Threshold		0.8		V	Max
High State Threshold		2.4		V	Min
Input Current (Low or high)	$V_{IN} = 0V$ or $+15V$	±1		μA	Max
Input Coding	See Tables 1 & 2	Binary/Offset Binary			
Input Capacitance (Note 3)		4		pF	Max
POWER REQUIREMENTS					
Power Supply Voltage Range	Accuracy is tested and guaranteed at $V^+ = +15V$, only.	+5 to +16		V	
I^+ (Excluding Ladder Network)	All digital inputs High or Low	2	2.5	mA	Max

NOTES: **1.** Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

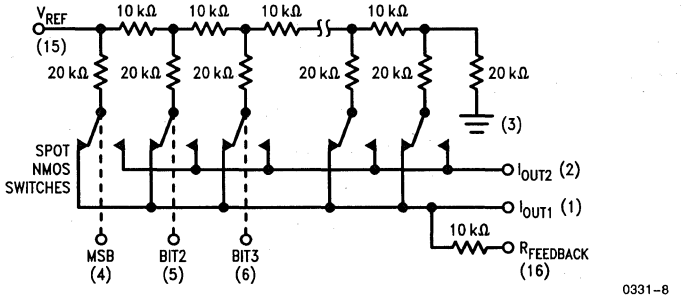
DETAILED DESCRIPTION

The AD7523 is a monolithic multiplying D/A converter. A highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit, CMOS level shifters permit low power TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 3. The NMOS SPDT switches steer the ladder leg currents between I_{OUT1} and I_{OUT2} buses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.

Converter errors are further reduced by using separate metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 4). This configuration results in TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an ON resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors and highly accurate leg currents.



(Switches shown for Digital Inputs "High")

Figure 3: AD7523 Functional Diagram

NOTE: All typical values have been characterized but are not tested.

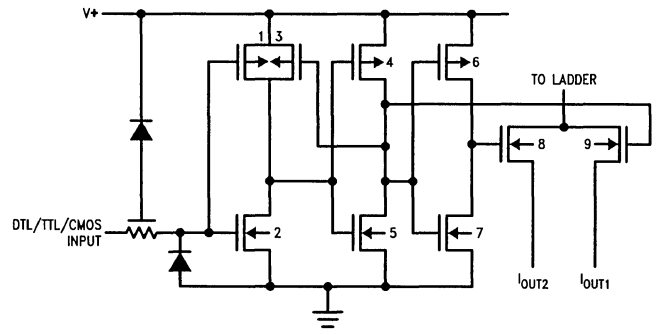
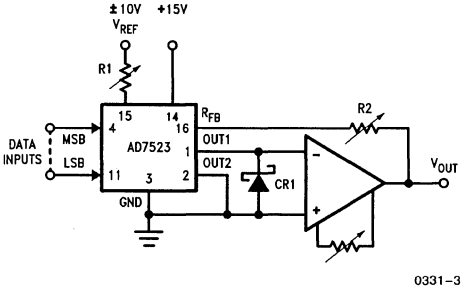


Figure 4: CMOS Switch

APPLICATIONS

UNIPOLAR OPERATION



NOTES: 1. R1 and R2 used only if gain adjustment is required.
2. CR1 protects AD7523 against negative transients.

Figure 5: Unipolar Binary Operation

APPLICATIONS

Unipolar Binary Operation

The circuit configuration for operating the AD7523 in unipolar mode is shown in Figure 5. With positive and negative V_{REF} values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1.

ZERO OFFSET ADJUSTMENT

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±1 mV (max) at V_{OUT}.

GAIN ADJUSTMENT

1. Connect all digital inputs to V^+.
2. Monitor V_{OUT} for a $-V_{REF}$ $(1 - 1/2^8)$ reading.
3. To increase V_{OUT}, connect a series resistor, R2, (0 to 250Ω) in the I_{OUT1} amplifier feedback loop.
4. To decrease V_{OUT}, connect a series resistor, R1, (0 to 250Ω) between the reference voltage and the V_{REF} terminal.

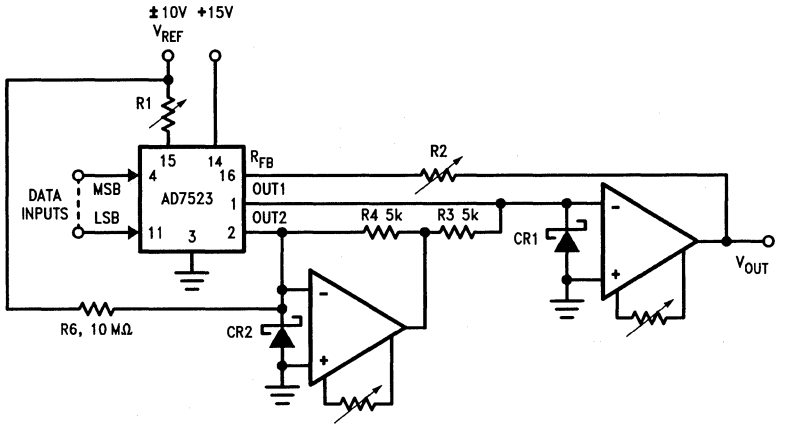
Table 1. Unipolar Binary Code Table

Digital Input MSB LSB	Analog Output
11111111	$-V_{REF}\left(\frac{255}{256}\right)$
10000001	$-V_{REF}\left(\frac{129}{256}\right)$
10000000	$-V_{REF}\left(\frac{128}{256}\right)=-\frac{V_{REF}}{2}$
01111111	$-V_{REF}\left(\frac{127}{256}\right)$
00000001	$-V_{REF}\left(\frac{1}{256}\right)$
00000000	$-V_{REF}\left(\frac{0}{256}\right)=0$

NOTE: 1 LSB $=(2^{-8})$ $(V_{REF})=\left(\frac{1}{256}\right)$ (V_{REF})

NOTE: All typical values have been characterized but are not tested.

BIPOLAR OPERATION



NOTES:
1. R3/R4 MATCH 0.1% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. CR1 & CR2 PROTECT AD7523 AGAINST NEGATIVE TRANSIENTS.

Figure 6: Bipolar Operation (4-Quadrant Multiplication)

Bipolar (Offset Binary) Operation

The circuit configuration for operating the AD7523 in the bipolar mode is given in Figure 6. Using offset binary digital input codes and positive and negative reference voltage values, Four-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

Table 2. Bipolar (Offset Binary) Code Table

Digital Input MSB LSB	Analog Output
11111111	$-V_{REF}\left(\frac{127}{128}\right)$
10000001	$-V_{REF}\left(\frac{1}{128}\right)$
10000000	0
01111111	$+V_{REF}\left(\frac{1}{128}\right)$
00000001	$+V_{REF}\left(\frac{127}{128}\right)$
00000000	$+V_{REF}\left(\frac{128}{128}\right)$

NOTE: 1 LSB = (2^{-7}) $(V_{REF}) = \left(\frac{1}{128}\right)$ (V_{REF})

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to I_{OUT1} bus. A "Logic 0" input forces the bit current to I_{OUT2} bus. For any code the I_{OUT1} and I_{OUT2} bus currents are complements of one another. The current amplifier at I_{OUT2} changes the polarity of I_{OUT2} current and the transconductance amplifier at I_{OUT1} output sums the two currents. This configuration doubles the output range. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistor, (10 MΩ), from V_{REF} to I_{OUT2} (Figure 6).

OFFSET ADJUSTMENT

1. Adjust V_{REF} to approximately +10V.
2. Connect all digital inputs to "Logic 1".
3. Adjust I_{OUT2} amplifier offset adjust trimpot for 0V ±1 mV at I_{OUT2} amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust I_{OUT1} amplifier offset adjust trimpot for 0V ±1 mV at V_{OUT}.

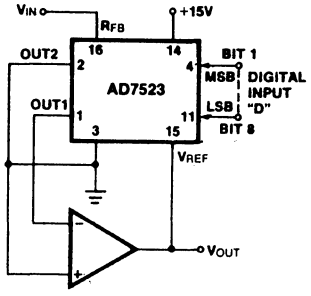
GAIN ADJUSTMENT

1. Connect all digital inputs to V+.
2. Monitor V_{OUT} for a $-V_{REF}$ $(1 - 1/2^7)$ volts reading.
3. To increase V_{OUT}, connect a series resistor, R2, of up to 250Ω between V_{OUT} and $R_{FEEDBACK}$.
4. To decrease V_{OUT}, connect a series resistor, R1, of up to 250Ω between the reference voltage and the V_{REF} terminal.

NOTE: All typical values have been characterized but are not tested.

AD7523

POWER DAC DESIGN USING AD7523



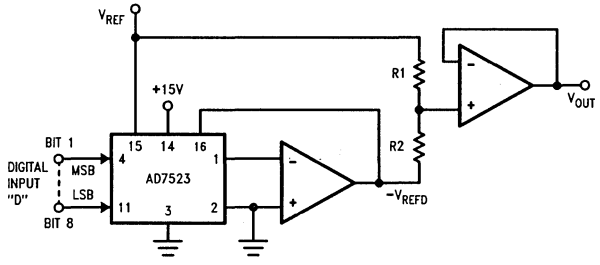
$V_{OUT} = -V_{IN}/D$
WHERE:

$$D = \frac{BIT1}{2^1} + \frac{BIT2}{2^2} + \cdots \frac{BIT8}{2^8}$$

$$\left(0 \le D \le \frac{255}{256}\right)$$

0331-6

Figure 7: Divider (Digitally Controlled Gain)



0331-7

$$V_{OUT} = V_{REF}\left[\left(\frac{R_2}{R_1 + R_2}\right) - \left(\frac{R_1 D}{R_1 + R_2}\right)\right]$$

$$\text{Where } D = \frac{\text{Bit 1}}{2^1} + \frac{\text{Bit 2}}{2^2} + \cdots \frac{\text{Bit 8}}{2^8}$$

$$\left(0 \le D \le \frac{255}{256}\right)$$

Figure 8: Modified Scale Factor and Offset

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a "best straight line" through the actual plot of transfer function. Normally expressed as a percentage of full scale range or in (sub)multiples of 1 LSB.

RESOLUTION: It is addressing the smallest distinct analog output change that a D/A converter can produce. It is commonly expressed as the number of converter bits. A converter with resolution of n bits can resolve output changes of 2^{-n} of the full-scale range, e.g. 2^{-n} V_{REF} for a unipolar conversion. Resolution by no means implies linearity.

SETTLING TIME: Time required for the output of a DAC to settle to within specified error band around its final value (e.g. ½ LSB) for a given digital input change, i.e., all digital inputs LOW to HIGH and HIGH to LOW.

GAIN ERROR: The difference between actual and ideal analog output values at full-scale range, i.e., all digital inputs at HIGH state. It is expressed as a percentage of full-scale range or in (sub)multiples of 1 LSB.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to I_{OUT1} with all digital inputs LOW.

OUTPUT CAPACITANCE: Capacitance from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal when all digital inputs are LOW or on I_{OUT2} terminal when all digital inputs are HIGH.

For further information on the use of this device, see the following Application Notes:

A002 "Principles of Data Acquisition and Conversion"

A018 "Do's and Don'ts of Applying A/D Converters," by Peter Bradshaw and Skip Osgood

A042 "Interpretation of Data Conversion Accuracy Specifications"

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

AD7533
10-Bit Multiplying D/A Converter

GENERAL DESCRIPTION

The Harris AD7533 is a low cost, monolithic 10-bit, four-quadrant multiplying digital-to-analog converter (DAC). Harris' thin-film resistor on CMOS circuitry provide 10, 9 and 8 bit accuracy over full temperature range. The device also provides +5V to +15V supply voltage range, full input protection from damage due to static discharge by clamps to V^+ and ground and very low power dissipation.

Applications for the AD7533 include programmable gain amplifiers, digitally controlled attenuators, function generators and control systems.

FEATURES

- **8, 9 and 10 Bit Linearity**
- **Low Gain and Linearity Tempcos**
- **Full Temperature Range Operation**
- **Full Input Static Protection**
- **TTL/CMOS Direct Interface**
- **+5 to +15 Volts Supply Range**
- **Low Power Dissipation**
- **Fast Settling Time**
- **Four Quadrant Multiplication**
- **Direct AD7520 Equivalent**

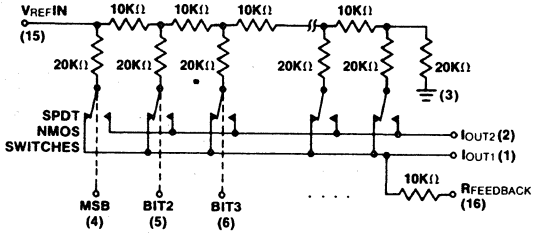
ORDERING INFORMATION

Nonlinearity	Temperature Range
	0°C to +70°C
±0.2% (8-bit)	AD7533JN
±0.1% (9-bit)	AD7533KN
±0.05% (10-bit)	AD7533LN

PACKAGE IDENTIFICATION

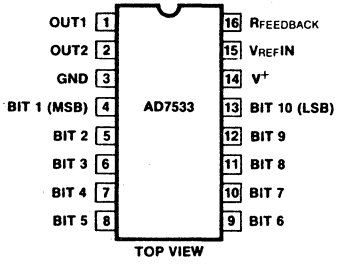
AD7533 T D/N

- D/N — Package: N — 18-Pin Plastic DIP
- T — Nonlinearity and Temperature Range: J,K,L — Commercial 0°C to +70°C
- AD7533 — Basic Part Number



0332-1

Figure 1: Functional Diagram



0332-2

Figure 2: Pin Configuration

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

V^+ ..... +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... V^+ to GND
Output Voltage Compliance ..... −0.1V to V^+
Power Dissipation
Plastic Package:
up to 70°C 670mW
derates above 70°C by ..... 8.3mW/°C

Operating Temperature Range:
JN, KN, LN Versions ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

CAUTION:

1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

2. Do not apply voltages lower than ground or higher than V^+ to any pin except V_{REF} and R_{FB}.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

($V^+ = +15V$, $V_{REF} = +10V$, $V_{OUT1} = V_{OUT2} = 0V$ unless otherwise specified.)

Parameter		Test Conditions	T_A +25°C	T_A Min–Max	Limit	Unit
DC ACCURACY (Note 1)						
Resolution			10	10	Min	Bit
Nonlinearity (Note 2)	J		±0.2	±0.2	Max	% of FSR
	K	$-10V \le V_{REF} \le +10V$	±0.1	±0.1	Max	% of FSR
	L	$V_{OUT1} = V_{OUT2} = 0V$	±0.05	±0.05	Max	% of FSR
Gain Error (Note 2 and 5)		All Digital Inputs High	±1.4	±1.5	Max	% of FSR
Output Leakage Current (either output)		$V_{REF} = \pm 10V$	±50	±200	Max	nA
AC ACCURACY						
Power Supply Rejection (Note 2)		$V^+ = 14.0$ to 17.0V	±0.005	±0.008	Max	% of FSR/%ΔV^+
Output Current Settling Time (Note 3)		To 0.05% of FSR, $R_L = 100\Omega$	600	800	Max	ns
Feedthrough Error (Note 3)		$V_{REF} = 20V_{PP}$, 100kHz sine wave. Digital inputs low.	±0.05	±0.1	Max	% FSR
REFERENCE INPUT						
Input Resistance (Pin 15)		All digital inputs high.	5k		Min	Ω
			20k		Max	
Temperature Coefficient			−300		Typ	ppm/°C
ANALOG OUTPUT						
Voltage Compliance (Note 3)		Both outputs. See maximum ratings	−100mV to V^+			
Output Capacitance (Note 3)	C_{OUT1}	All digital inputs high	100		Max	pF
	C_{OUT2}		35		Max	pF
	C_{OUT1}	All digital inputs low	35		Max	pF
	C_{OUT2}		100		Max	pF

NOTE: All typical values have been characterized but are not tested.

AD7533

ELECTRICAL CHARACTERISTICS

($V^+ = +15V$, $V_{REF} = +10V$, $V_{OUT1} = V_{OUT2} = 0$ unless otherwise specified.) (Continued)

Parameter	Test Conditions	T_A +25°C	T_A Min-Max	Limit	Unit
DIGITAL INPUTS					
Low State Threshold		0.8		Max	V
High State Threshold		2.4		Min	V
Input Current Low or High	$V_{IN} = 0V$ and V^+	±1		Max	μA
Input Coding	See Tables 1 & 2	Binary/Offset Binary			
Input Capacitance (Note 3)		5		Max	pF
POWER REQUIREMENTS					
V_{DD}	Rated Accuracy	+15 ±10%			V
Power Supply Voltage Range		+5 to +16			V
I^+ (Excluding Ladder Network)	Digital Inputs High or Low	2	2.5	Max	mA
	Digital Inputs = 0V or V^+	100	150	Max	μA

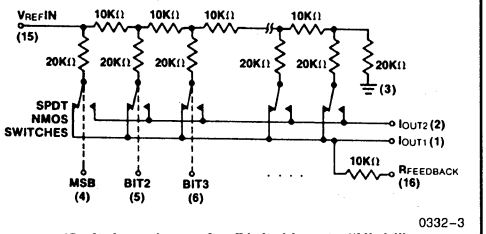
NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.
5. Full scale (FS) = $-(V_{REF}) \bullet (1023/1024)$

Specifications subject to change without notice.

DETAILED DESCRIPTION

The Harris AD7533 is a 10 bit, monolithic, multiplying D/A converter. A highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit. CMOS level shifters permit low power TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 3. The NMOS SPDT switches steer the ladder leg currents between IOUT1 and IOUT2 busses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.



(Switches shown for Digital Inputs "High")
Figure 3

NOTE: All typical values have been characterized but are not tested.

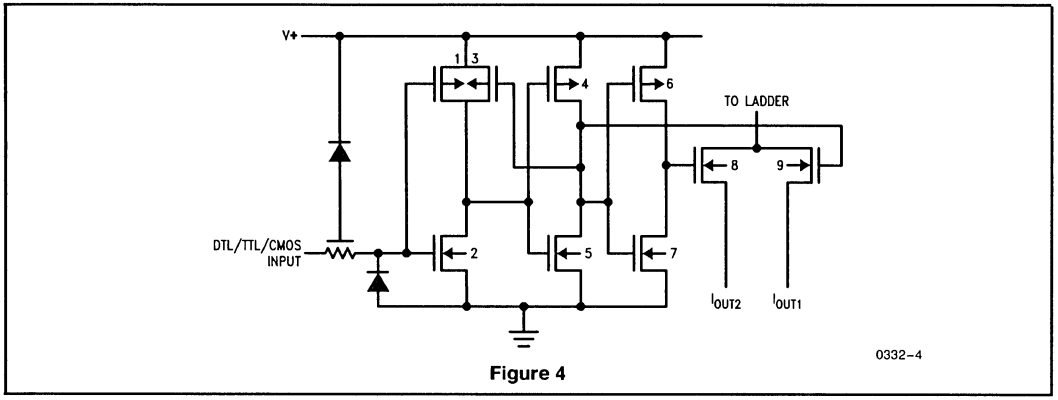
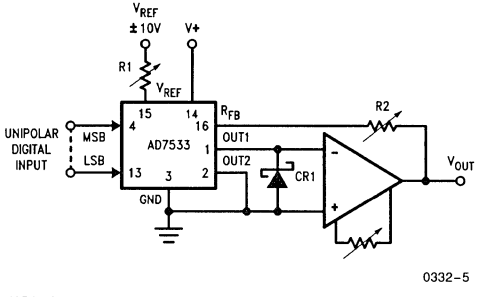


Figure 4

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 4). This configuration results in TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors resulting in accurate leg currents.

APPLICATIONS

UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)



NOTES: 1. R1 and R2 used only if gain adjustment is required.
2. Schottky diode CR1 (HP5082-2811 or equiv) protects OUT1 terminal against negative transients.

Figure 5: Unipolar Binary Operation (2-Quadrant Multiplication)

Table 1. Unipolar Binary Code

Digital Input MSB LSB	Nominal Analog Output (V_{OUT} as shown in Figure 3)
1111111111	$-V_{REF}\left(\frac{1023}{1024}\right)$
1000000001	$-V_{REF}\left(\frac{513}{1024}\right)$
1000000000	$-V_{REF}\left(\frac{512}{1024}\right)=-\frac{V_{REF}}{2}$
0111111111	$-V_{REF}\left(\frac{511}{1024}\right)$
0000000001	$-V_{REF}\left(\frac{1}{1024}\right)$
0000000000	$-V_{REF}\left(\frac{0}{1024}\right)=0$

NOTES: 1. Nominal Full Scale for the circuit of Figure 5 is given by

$$FS=-V_{REF}\left(\frac{1023}{1024}\right)$$

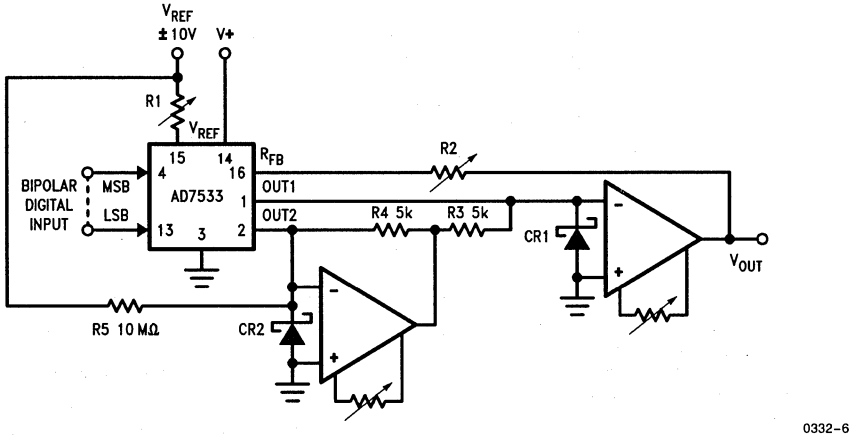
2. Nominal LSB magnitude for the circuit of Figure 5 is given by

$$LSB=V_{REF}\left(\frac{1}{1024}\right)$$

6

NOTE: All typical values have been characterized but are not tested.

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)



NOTES: 1. R3/R4 match 0.05% or better.
2. R1 and R2 used only if gain adjustment is required.
3. Schottky diodes CR1 and CR2 (HP5082-2811 or equiv) protect OUT1 and OUT2 terminals against negative transients.

Figure 6: Bipolar Operation (4-Quadrant Multiplication)

Table 2. Bipolar (Offset Binary) Code Table

Digital Input MSB LSB	Nominal Analog Output (V_{OUT} as shown in Figure 4)
1111111111	$-V_{REF}\left(\frac{511}{512}\right)$
1000000001	$-V_{REF}\left(\frac{1}{512}\right)$
1000000000	0
0111111111	$+V_{REF}\left(\frac{1}{512}\right)$
0000000001	$+V_{REF}\left(\frac{511}{512}\right)$
0000000000	$+V_{REF}\left(\frac{512}{512}\right)$

NOTES: 1. Nominal Full Scale for the circuit of Figure 6 is given by

$$FSR = V_{REF}\left(\frac{1023}{512}\right)$$

2. Nominal LSB magnitude for the circuit of Figure 6 is given by

$$LSB = V_{REF}\left(\frac{1}{512}\right)$$

APPLICATIONS

Unipolar Binary Operation

The circuit configuration for operating the AD7533 in unipolar mode is shown in Figure 5. With positive and negative V_{REF} values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1.

ZERO OFFSET ADJUSTMENT

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±1 mV at V_{OUT}.

GAIN ADJUSTMENT

1. Connect all digital inputs to V+.
2. Monitor V_{OUT} for a $-V_{REF}(1 - 2^{-10})$ reading.
3. To decrease V_{OUT}, connect a series resistor (0Ω to 250Ω) between the reference voltage and the V_{REF} terminal.
4. To increase V_{OUT}, connect a series resistor (0Ω to 250Ω) in the I_{OUT1} amplifier feedback loop.

NOTE: All typical values have been characterized but are not tested.

Bipolar (Offset Binary) Operation

The circuit configuration for operating the AD7533 in the bipolar mode is given in Figure 6. Using offset binary digital input codes and positive and negative reference voltage values, 4-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to I_{OUT1} bus. A "Logic 0" input forces the bit current to I_{OUT2} bus. For any code the I_{OUT1} and I_{OUT2} bus currents are complements of one another. The current amplifier at I_{OUT2} changes the polarity of I_{OUT2} current and the transconductance amplifier at I_{OUT1} output sums the two currents. This configuration doubles the output range. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistor, (10 MΩ), from V_{REF} to I_{OUT2}.

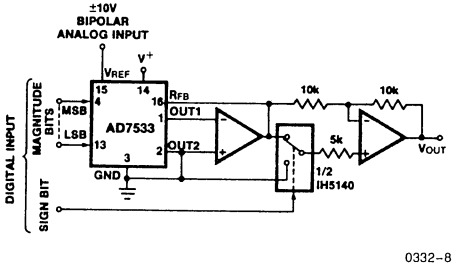


Figure 7: 10-Bit and Sign Multiplying DAC

OFFSET ADJUSTMENT

1. Adjust V_{REF} to approximately +10V.
2. Connect all digital inputs to "Logic 1".
3. Adjust I_{OUT2} amplifier offset adjust trimpot for 0V ±1 mV at I_{OUT2} amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust I_{OUT1} amplifier offset adjust trimpot for 0V ±1 mV at V_{OUT}.

GAIN ADJUSTMENT

1. Connect all digital inputs to V+.
2. Monitor V_{OUT} for a $-V_{REF}(1 - 2^{-9})$ volts reading.
3. To increase V_{OUT}, connect a series resistor of up to 250Ω between V_{OUT} and $R_{FEEDBACK}$.
4. To decrease V_{OUT}, connect a series resistor of up to 250Ω between the reference voltage and the V_{REF} terminal.

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a "best straight line" through the actual plot of transfer function. Normally expressed as a percentage of full scale range or in (sub)multiples of 1 LSB.

RESOLUTION: It is addressing the smallest distinct analog output change that a D/A converter can produce. It is commonly expressed as the number of converter bits. A converter with resolution of n bits can resolve output changes of 2^{-n} of the full-scale range, e.g. 2^{-n} V_{REF} for a unipolar conversion. Resolution by no means implies linearity.

SETTLING TIME: Time required for the output of a DAC to settle to within specified error band around its final value (e.g., ½ LSB) for a given digital input change, i.e. all digital inputs LOW to HIGH and HIGH to LOW.

GAIN ERROR: The difference between actual and ideal analog output values at full-scale range, i.e. all digital inputs at HIGH state. It is expressed as a percentage of full-scale range or in (sub)multiples of 1 LSB.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to I_{OUT1} with all digital inputs LOW.

OUTPUT CAPACITANCE: Capacitance from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal when all digital inputs are LOW or on I_{OUT2} terminal when all digital inputs are HIGH.

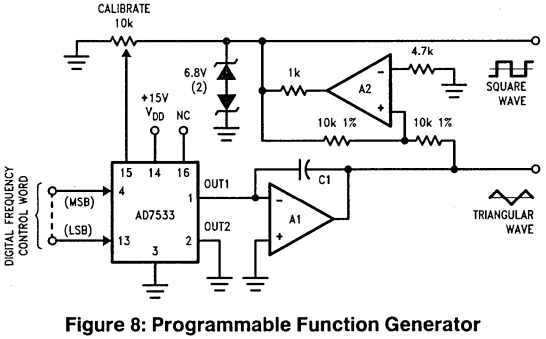


Figure 8: Programmable Function Generator

NOTE: All typical values have been characterized but are not tested.

AD7541
12-Bit Multiplying D/A Converter

GENERAL DESCRIPTION

The Harris AD7541 is a monolithic, low cost, high performance, 12-bit accurate, multiplying digital-to-analog converter (DAC).

Harris' wafer level laser-trimmed thin-film resistors on CMOS circuitry provide true 12-bit linearity with TTL/CMOS compatible operation.

Special tabbed-resistor geometries (improving time stability), full input protection from damage due to static discharge by diode clamps to V+ and ground, large I_{OUT1} and I_{OUT2} bus lines (improving superposition errors) are some of the features offered by Harris AD7541.

Pin compatible with AD7521, this new DAC provides accurate four quadrant multiplication over the full military temperature range.

FEATURES

- **12 Bit Linearity (0.01%)**
- **Pretrimmed Gain**
- **Low Gain and Linearity Tempcos**
- **Full Temperature Range Operation**
- **Full Input Static Protection**
- **DTL/TTL/CMOS Compatible**
- **+5 to +15 Volts Supply Range**
- **Low Power Dissipation (20mW)**
- **Current Settling Time: 1μs to 0.01% of FSR**
- **Four Quadrant Multiplication**
- **883B Processed Versions Available**

ORDERING INFORMATION

Nonlinearity	Part Number/Temperature Range		
	0°C to +70°C	−25°C to +85°C	−55°C to +125°C
0.02% (11-bit)	AD7541JN	AD7541AD	AD7541SD
0.01% (12-bit)	AD7541KN	AD7541BD	AD7541TD
0.01% (12-bit) Guaranteed Monotonic	AD7541LN	–	–

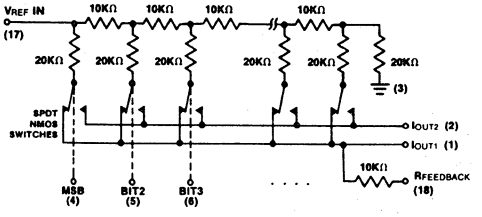


Figure 1: Functional Diagram (Switches shown for Digital Inputs 'High')

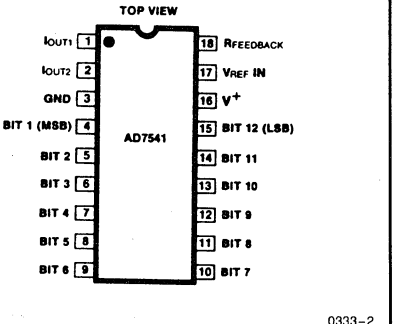


Figure 2: Pin Configuration (Outline dwgs DN, PN)

300150-004

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS ($T_A = 25°C$ unless otherwise noted)

$V+$ ..... +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... GND to $V+$
Output Voltage Compliance ..... −100mV to $V+$
Power Dissipation (package):
up to +75°C 450mW
derate above +75°C by ..... 6mW/°C

Operating Temperature Range:
JN, KN, LN Versions ..... 0°C to +70°C
AD, BD Versions ..... −25°C to +85°C
SD, TD Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

CAUTION

1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

2. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and $R_{FEEDBACK}$.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

($V+ = +15V$, $V_{REF} = +10V$, $V_{OUT1} = V_{OUT2} = 0V$, $T_A = 25°C$ unless otherwise specified)

Parameter				Test Conditions	TA +25°C	TA Min-Max	Limit	Fig.	Unit
DC ACCURACY (Note 1)									
Resolution					12	12	Min		Bits
Nonlinearity (Note 2)	A	S	J		±0.024	±0.024	Max	3	% of FSR
	B	T	K	$-10V \le V_{REF} \le +10V$	±0.012	±0.012	Max		% of FSR
			L	$V_{OUT1} = V_{OUT2} = 0V$	±0.012	±0.012	Max		% of FSR
					Guaranteed Monotonic				
Gain Error (Note 2)				$-10V \le V_{REF} \le +10V$	±0.3	±0.4	Max		% of FSR
Output Leakage Current (either output)				$V_{OUT1} = V_{OUT2} = 0$	±50	±200	Max		nA
AC ACCURACY (Note 3)									
Power Supply Rejection (Note 2)				$V+ = 14.5$ to $15.5V$	±0.005	±0.01	Max	4	% of FSR/%/% $\Delta V+$
Output Current Settling Time				To 0.01% of FSR	1		Max	8	µs
Feedthrough Error				$V_{REF} = 20V$ pp, 10kHz. All digital inputs low.	1		Max	7	mV pp
REFERENCE INPUT									
Input Resistance				All digital inputs high. I_{OUT1} at ground.	5		Min		kΩ
					10		Typ		
					20		Max		
ANALOG OUTPUT									
Voltage Compliance (Note 4)				Both outputs. See maximum ratings.	−100mV to $V+$				
Output Capacitance (Note 3)	C_{OUT1}			All digital inputs high	200		Max	6	pF
	C_{OUT2}				60		Max		pF
	C_{OUT1}			All digital inputs low	60		Max	6	pF
	C_{OUT2}				200		Max		pF
Output Noise (both outputs)					Equivalent to 10KΩ Johnson noise		Typ	5	

NOTE: All typical values have been characterized but are not tested.

AD7541

ELECTRICAL CHARACTERISTICS

($V^+ = +15V$, $V_{REF} = +10V$, $V_{OUT1} = V_{OUT2} = 0V$, $T_A = 25°C$ unless otherwise specified) (Continued)

Parameter	Test Conditions	TA +25°C	TA Min-Max	Limit	Fig.	Unit
DIGITAL INPUTS						
Low State Threshold (V_{INL})		0.8		Max		V
High State Threshold (V_{INH})		2.4		Min		V
Input Current	$V_{IN} = 0$ or V^+	±1		Max		μA
Input Coding	See Tables 1 & 2	Binary/Offset Binary				
Input Capacitance (Note 3)		8		Max		pF
POWER REQUIREMENTS						
Power Supply Voltage Range	Accuracy is not guaranteed over this range	+5 to +16				V
I^+ (Excluding Ladder Network)	All digital inputs High or Low	2.0	2.5	Max		mA
Total Power Dissipation (Including the ladder)		20		Typ		mW

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

Specifications subject to change without notice.

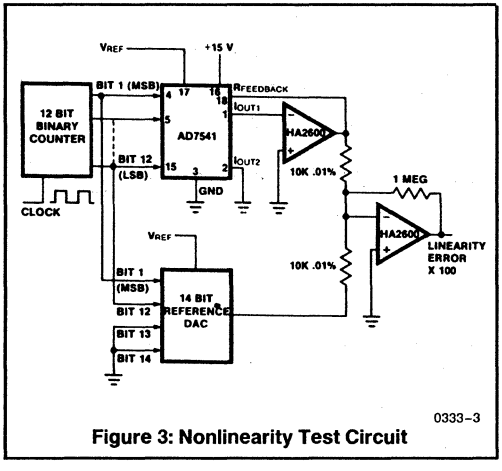


Figure 3: Nonlinearity Test Circuit

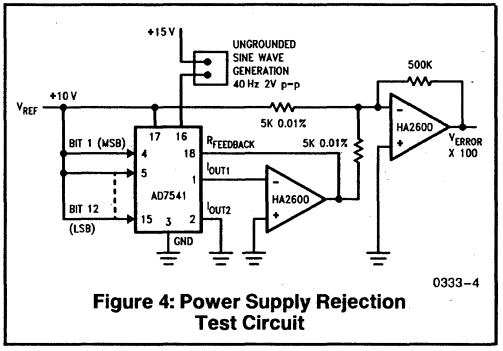


Figure 4: Power Supply Rejection Test Circuit

NOTE: All typical values have been characterized but are not tested.

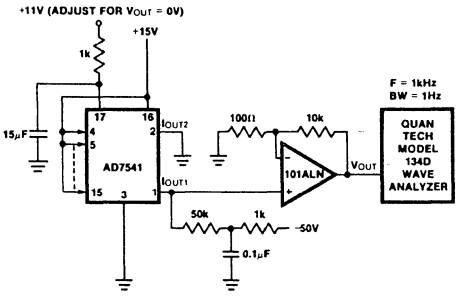


Figure 5: Noise Test Circuit

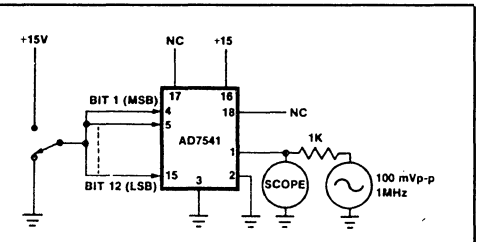


Figure 6: Output Capacitance Test Circuit

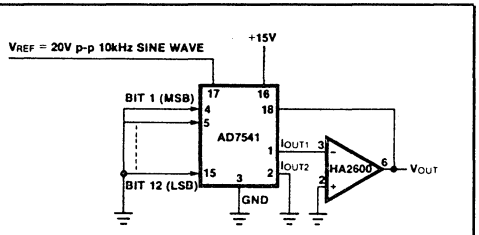


Figure 7: Feedthrough Error Test Circuit

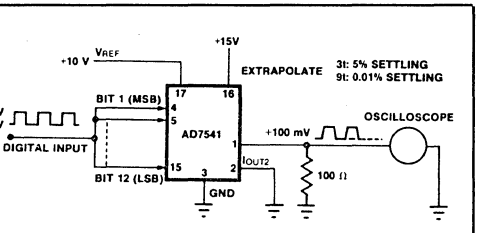


Figure 8: Output Current Settling Time Test Circuit

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within ½ LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

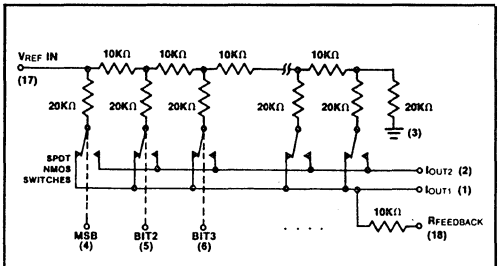
FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

DETAILED DESCRIPTION

The Harris AD7541 is a 12 bit, monolithic, multiplying D/A converter. Highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit. CMOS level shifters provide low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.



(Switches shown for Digital Inputs "High")

Figure 9: AD7541 Functional Diagram

NOTE: All typical values have been characterized but are not tested.

AD7541

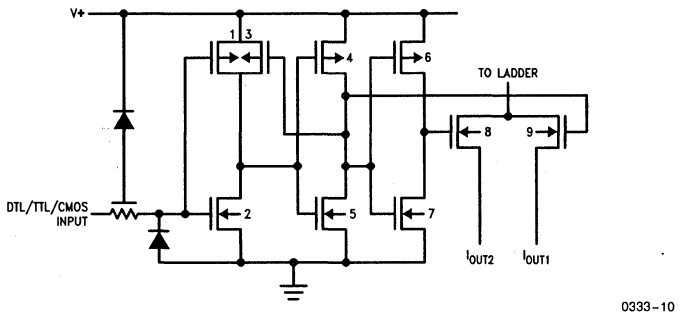


Figure 10: CMOS Switch

A simplified equivalent circuit of the DAC is shown in Figure 9. The NMOS SPDT switches steer the ladder leg currents between IOUT1 and IOUT2 buses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code. Converter errors are further eliminated by using wider metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

Each circuit is laser-trimmed, at the wafer level, to better than 12 bits linearity. For the first four bits of the ladder, special trim-tabbed geometries are used to keep the body of the resistors, carrying the majority of the output current, undisturbed. The resultant time stability of the trimmed circuits is comparable to that of untrimmed units.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first (Figure 10). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors, resulting in accurate leg currents.

APPLICATIONS

General Recommendations

Static performance of the AD7541 depends on I_{OUT1} and I_{OUT2} (pin 1 and pin 2) potentials being exactly equal to GND (pin 3).

The output amplifier should be selected to have a low input bias current (typically less than 75nA), and a low drift (depending on the temperature range). The voltage offset of the amplifier should be nulled (typically less than $\pm 200\mu V$).

The bias current compensation resistor in the amplifier's non-inverting input can cause a variable offset. Non-inverting input should be connected to GND with a low resistance wire.

Ground-loops must be avoided by taking all pins going to GND to a common point, using separate connections.

The V^+ (pin 18) power supply should have a low noise level and should not have any transients exceeding +17 volts.

Unused digital inputs must be connected to GND or V_{DD} for proper operation.

A high value resistor ($\sim 1M\Omega$) can be used to prevent static charge accumulation, when the inputs are open-circuited for any reason.

When gain adjustment is required, low tempco (approximately 50ppm/°C) resistors or trim-pots should be selected.

UNIPOLAR BINARY OPERATION

The circuit configuration for operating the AD7541 in unipolar mode is shown in Figure 11. With positive and negative VREF values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1. A Schottky diode (HP5082-2811 or equivalent) prevents I_{OUT1} from negative excursions which could damage the device. This precaution is only necessary with certain high speed amplifiers.

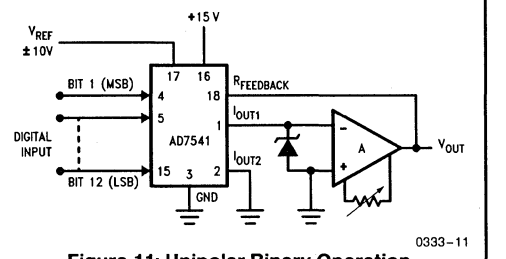


Figure 11: Unipolar Binary Operation (2-Quadrant Multiplication)

NOTE: All typical values have been characterized but are not tested.

Zero Offset Adjustment

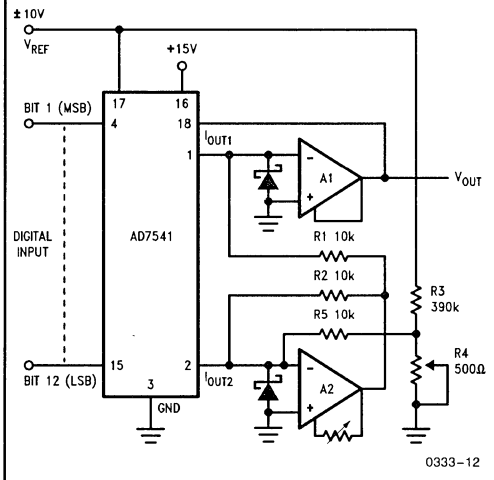
1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±0.5mV (max) at VOUT.

Gain Adjustment

1. Connect all digital inputs to VDD.
2. Monitor VOUT for a $-VREF\ (1-1/2^{12})$ reading.
3. To increase VOUT, connect a series resistor, (0 to 250 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 250 ohms), between the reference voltage and the VREF terminal.

Table 1: Code Table — Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}\ (1-1/2^{12})$
100000000001	$-V_{REF}\ (1/2+1/2^{12})$
100000000000	$-V_{REF}/2$
011111111111	$-V_{REF}\ (1/2-1/2^{12})$
000000000001	$-V_{REF}\ (1/2^{12})$
000000000000	0



Note: R1 and R2 should be 0.01%, low-TCR resistors.

Figure 12: Bipolar Operation (4-Quadrant Multiplication)

BIPOLAR (OFFSET BINARY) OPERATION

The circuit configuration for operating the AD7541 in the bipolar mode is given in Figure 12. Using offset binary digital input codes and positive and negative reference voltage values Four-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to IOUT1 bus. A "Logic 0" input forces the bit current to IOUT2 bus. For any code the IOUT1 and IOUT2 bus currents are complements of one another. The current amplifier at IOUT2 changes the polarity of IOUT2 current and the transconductance amplifier at IOUT1 output sums the two currents. This configuration doubles the output range of the DAC. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistive divider, from VREF to IOUT2.

Offset Adjustment

1. Adjust V_{REF} to approximately +10V.
2. Set R4 to zero.
3. Connect all digital inputs to "Logic 1".
4. Adjust I_{OUT1} amplifier offset zero adjust trimpot for 0V ±0.1mV at I_{OUT2} amplifier output.
5. Connect a short circuit across R2.
6. Connect all digital inputs to "Logic 0".
7. Adjust I_{OUT2} amplifier offset zero adjust trimpot for 0V ±0.1mV at I_{OUT1} amplifier output.
8. Remove short circuit across R2.
9. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
10. Adjust R4 for 0V ±0.2mV at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to VDD.
2. Monitor VOUT for a $-VREF\ (1-1/2^{11})$ volts reading.
3. To increase VOUT, connect a series resistor, (0 to 250 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 250 ohms), between the reference voltage and the VREF terminal.

Table 2: Code Table Bipolar (Offset Binary) Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}\ (1-1/2^{11})$
100000000001	$-V_{REF}\ (1/2^{11})$
100000000000	0
011111111111	$V_{REF}\ (1/2^{11})$
000000000001	$V_{REF}\ (1-1/2^{11})$
000000000000	V_{REF}

6

NOTE: All typical values have been characterized but are not tested.

AD7541

DYNAMIC PERFORMANCE

The dynamic performance of the DAC, also depends on the output amplifier selection. For low speed or static applications, AC specifications of the amplifier are not very critical. For high-speed applications slew-rate, settling-time, openloop gain and gain/phase-margin specifications of the amplifier should be selected for the desired performance.

The output impedance of the AD7541 looking into I_{OUT1} varies between 10kΩ ($R_{Feedback}$ alone) and 5KΩ ($R_{Feedback}$ in parallel with the ladder resistance).

Similarly the output capacitance varies between the minimum and the maximum values depending on the input code. These variations necessitate the use of compensation capacitors, when high speed amplifiers are used.

A capacitor in parallel with the feedback resistor (as shown in Figure 13) provides the necessary phase compensation to critically damp the output.

A small capacitor connected to the compensation pin of the amplifier may be required for unstable situations causing oscillations. Careful PC board layout, minimizing parasitic capacitances, is also vital.

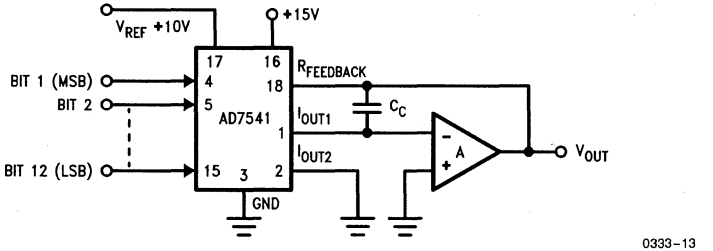


Figure 13: General DAC Circuit with Compensation Capacitor, C_C

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

AD7545
12-Bit Buffered Multiplying CMOS DAC

GENERAL DESCRIPTION

The AD7545 is a low cost monolithic 12-bit CMOS multiplying DAC with on-board data latches. Data is loaded in a single 12-bit wide word which allows interfacing directly to most 12- and 16-bit bus systems. Loading of the input latches is under the control of the $\overline{CS}$ and $\overline{WR}$ inputs. A logic low on these control inputs makes the input latches transparent allowing direct unbuffered operation of the DAC.

FEATURES

- **12-Bit Resolution**
- **Low Gain T.C.: 2ppm/°C typ**
- **Fast TTL Compatible Data Latches**
- **Single +5V to +15V Supply**
- **Low Power**
- **Low Cost**

ORDERING INFORMATION

Part Number	Temperature Range	Package
AD7545JN	0°C to +70°C	20 Pin Plastic DIP
AD7545KN	0°C to +70°C	20 Pin Plastic DIP
AD7545AN	-40°C to +85°C	20 Pin Plastic DIP
AD7545BN	-40°C to +85°C	20 Pin Plastic DIP
AD7545AD	-40°C to +85°C	20 Pin Ceramic DIP
AD7545BD	-40°C to +85°C	20 Pin Ceramic DIP
AD7545SD	-55°C to +125°C	20 Pin Ceramic DIP
AD7545SQ/883	-55°C to +125°C	20 Pin Ceramic DIP

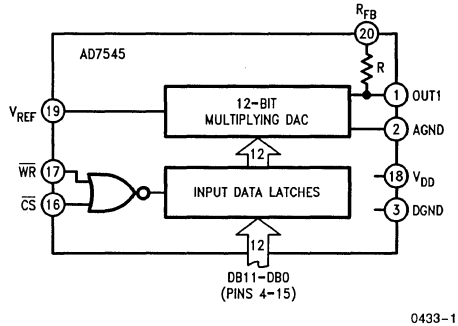


Figure 1: Functional Diagram

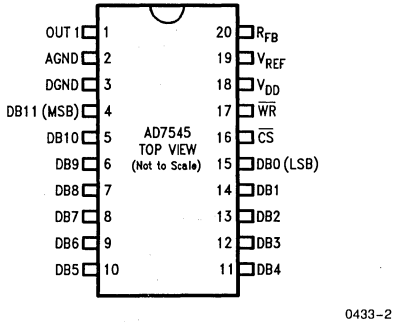


Figure 2: Pin Configuration

6

300152-001

NOTE: All typical values have been characterized but are not tested.

AD7545

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} to DGND ..... −0.3V, +17V

Digital Input Voltage to DGND ..... −0.3V, V_{DD} +0.3V

V_{RFB}, V_{REF} to DGND ..... ±25V

V_{PIN1} to DGND ..... −0.3V, V_{DD} +0.3V

AGND to DGND ..... −0.3V, V_{DD} +0.3V

Power Dissipation (Any Package) to +75°C ..... 450 mW

Derates above 75°C by ..... 6 mW/°C

Operating Temperature

Commercial

(J, K) Grades ..... 0°C to +70°C

Industrial

(A, B) Grades ..... −40°C to +85°C

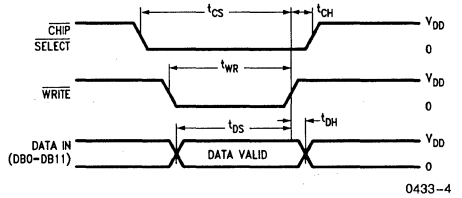
Extended

(S) Grades ..... −55°C to +125°C

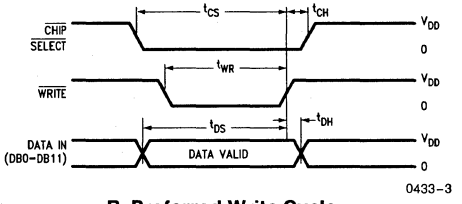
Storage Temperature ..... −65°C to +150°C

Lead Temperature (Soldering, 10 secs) ..... +300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*



A: Typical Write Cycle



B: Preferred Write Cycle

MODE SELECTION

WRITE MODE:

$\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB0–DB11) inputs.

HOLD MODE:

Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB0–DB11) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

NOTES:

V_{DD} = +5V; $t_r = t_f$ = 20 ns

V_{DD} = +15V; $t_r = t_f$ = 40 ns

All input signal rise and fall times measured from 10% to 90% of V_{DD}.

Timing measurement reference level is $(V_{IH} + V_{IL})/2$.

Since input data latches are transparent for $\overline{CS}$ and $\overline{WR}$ both low, it is preferred to have data valid before $\overline{CS}$ and $\overline{WR}$ both go low. This prevents undesirable changes at the analog output while the data inputs settle.

Figure 3: Write Cycle Timing Diagram

CIRCUIT INFORMATION—D/A CONVERTER SECTION

Figure 4 shows a simplified circuit of the D/A converter section of the AD7545. Note that the ladder termination resistor is connected to AGND. R is typically 11 kΩ.

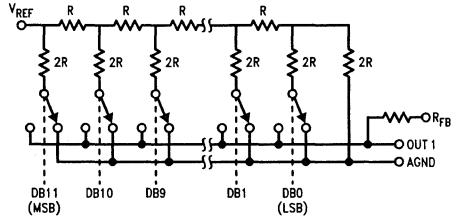


Figure 4: Simplified D/A Circuit of AD7545

The binary weighted currents are switched between the OUT1 bus line and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state. One of the current switches is shown in Figure 5.

The capacitance at the OUT1 bus line, C_{OUT1}, is code dependent and varies from 70 pF (all switches to AGND) to 200 pF (all switches to OUT1).

The input resistance at V_{REF} (Figure 4) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to the value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor.)

NOTE: All typical values have been characterized but are not tested.

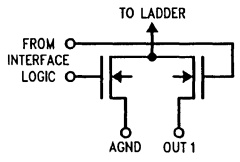


Figure 5: N-Channel Current Steering Switch

CIRCUIT INFORMATION— DIGITAL SECTION

Figure 6 shows the digital structure for one bit.

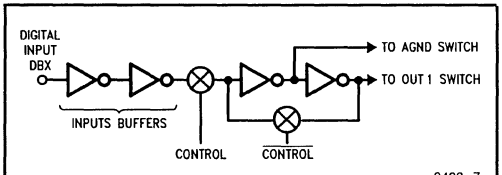


Figure 6: Digital Input Structure

The digital signals CONTROL and $\overline{\text{CONTROL}}$ are generated from $\overline{CS}$ and $\overline{WR}$.

The input buffers are simple CMOS inverters designed such that when the AD7545 is operated with V_{DD} = 5V, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When V_{IN} is in the region of 2.0V to 3.5V the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7545 may be operated with any supply voltage in the range 5V $\leq V_{DD} \leq$ 15V. With V_{DD} = +15V the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

APPLICATION

Output Offset: CMOS current-steering D/A converters exhibit a code dependent output resistance which in turn causes a code dependent amplifier noise gain. The effect is a code dependent differential nonlinearity term at the amplifier output which depends on V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation it is recommended that V_{OS} be no greater than (25×10^{-6}) (V_{REF}) over the temperature range of operation.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7545. In more complex systems where the AGND and DGND connection is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7545 AGND and DGND pins (1N914 or equivalent).

Digital Glitches: When $\overline{WR}$ and $\overline{CS}$ are both low the latches are transparent and the D/A converter inputs follow the data inputs. In some bus systems, data on the data bus is not always valid for the whole period during which $\overline{WR}$ is low and as a result invalid data can briefly occur at the D/A converter inputs during a write cycle. Such invalid data can cause unwanted glitches at the output of the D/A converter. The solution to this problem, if it occurs, is to retime the write pulse ($\overline{WR}$) so that it only occurs when data is valid.

Another cause of digital glitches is capacitive coupling from the digital lines to the OUT1 and AGND terminals. This should be minimized by isolating the analog pins of the AD7545 (Pins 1, 2, 19, 20) from the digital pins by a ground track run between pins 2 and 3 and between pins 18 and 19 of the AD7545. Note how the analog pins are at one end of the package and separated from the digital pins by V_{DD} and DGND to aid isolation at the board level. On-chip capacitive coupling can also give rise to crosstalk from the digital to analog sections of the AD7545, particularly in circuits with high currents and fast rise and fall times. This type of crosstalk is minimized by using V_{DD} = +5V. However, great care should be taken to ensure that the +5V used to power the AD7545 is free from digitally induced noise.

Temperature Coefficients: The gain temperature coefficient of the AD7545 has a maximum value of 5 ppm/°C and a typical value of 2 ppm/°C. This corresponds to worst case gain shifts of 2 LSBs and 0.8 LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full scale range, the temperature coefficient of R1 and R2 should also be taken into account.

6

NOTE: All typical values have been characterized but are not tested.

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND unless otherwise specified

Parameter	Test Conditions Comments	Version	V_{DD} = +5V Limits		V_{DD} = +15V Limits		Units
			T_A = +25°C	T_{min}, T_{max} (Note 1)	T_A = +25°C	T_{min}, T_{max} (Note 1)	
STATIC PERFORMANCE							
Resolution		All	12	12	12	12	Bits
Relative Accuracy		J, A, S K, B	±2 ±1	±2 ±1	±2 ±1	±2 ±1	LSB max LSB max
Differential Nonlinearity	10-Bit Monotonic T_{min} to T_{max} 12-Bit Monotonic T_{min} to T_{max}	J, A, S K, B	±4 ±1	±4 ±1	±4 ±1	±4 ±1	LSB max LSB max
Gain Error (Using Internal RFB) (Note 2)	DAC Register Loaded with 1111 1111 1111 Gain Error is Adjustable Using the Circuits of Figures 7 and 8	J, A, S K, B	±20 ±10	±20 ±10	±25 ±15	±25 ±15	LSB max LSB max
Gain Temperature Coefficient (Note 3) ΔGain/ΔTemperature	Typical Value is 2 ppm/°C for V_{DD} = +5V	All	±5	±5	±10	±10	ppm/°C max
DC Supply Rejection ΔGain/ΔV_{DD}	ΔV_{DD} = ±5%	All	0.015	0.03	0.01	0.02	% per % max
Output Leakage Current at OUT1	DB0–DB11 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V	J, K A, B S	10 10 10	50 50 200	10 10 10	50 50 200	nA max nA max nA max

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND unless otherwise specified (Continued)

Parameter	Test Conditions Comments	Version	V_{DD} = +5V Limits		V_{DD} = +15V Limits		Units
			T_A = +25°C	T_{min}, T_{max} (Note 1)	T_A = +25°C	T_{min}, T_{max} (Note 1)	
DYNAMIC PERFORMANCE							
Current Settling Time (Note 3)	To ½ LSB. OUT1 load = 100Ω. DAC output measured from falling edge of $\overline{WR}$. $\overline{CS}$ = 0V.	All	2	2	2	2	μs max
Propagation Delay (Note 3) (from Digital Input Change to 90% of final Analog Output)	OUT1 LOAD = 100Ω C_{EXT} = 13 pF (Note 4)	All	300		250		ns max
Digital to Analog Glitch Impulse	V_{REF} = AGND	All	400		250		nV sec typ
AC Feedthrough (Note 5) At OUT1	V_{REF} = ±10V, 10 kHz Sinewave	All	5	5	5	5	mVp-p typ
REFERENCE INPUT							
Input Resistance (Pin 19 to GND)	Input Resistance TC = −300 ppm/°C typ Typical Input Resistance = 11 kΩ	All	7 25	7 25	7 25	7 25	kΩ min kΩ max
ANALOG OUTPUTS							
Output Capacitance (Note 3) C_{OUT1} C_{OUT1}	 DB0–DB11 = 0V, $\overline{WR}$, $\overline{CS}$ = 0V DB0–DB11 = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0V	 All All	 70 200	 70 200	 70 200	 70 200	 pF max pF max
DIGITAL INPUTS							
Input High Voltage V_{IH}		All	2.4	2.4	13.5	13.5	V min
Input Low Voltage V_{IL}		All	0.8	0.8	1.5	1.5	V max
Input Current (Note 6) I_{IN}	V_{IN} = 0 or V_{DD}	All	±1	±10	±1	±10	μA max
Input Capacitance (Note 3) DB0–DB11 $\overline{WR}$, $\overline{CS}$	 V_{IN} = 0 V_{IN} = 0	 All All	 7 20	 7 20	 7 20	 7 20	 pF max pF max

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND unless otherwise specified (Continued)

Parameter	Test Conditions/Comments	Version	V_{DD} = +5V Limits		V_{DD} = +15V Limits		Units
			T_A = +25°C	T_{min}, T_{max} (Note 1)	T_A = +25°C	T_{min}, T_{max} (Note 1)	
SWITCHING CHARACTERISTICS (Note 3)							
Chip Select to Write Setup Time t_{CS}	See Figure 3	All	280 200	380 270	180 120	200 150	ns min ns typ
Chip Select to Write Hold Time t_{CH}	See Figure 3	All	0	0	0	0	ns min
Write Pulse Width t_{WR}	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$ See Figure 3	All	 250 175	 400 280	 160 100	 240 170	 ns min ns typ
Data Setup Time t_{DS}	See Figure 3	All	140 100	210 150	90 60	120 80	ns min ns typ
Data Hold Time t_{DH}	See Figure 3	All	10	10	10	10	ns min
POWER SUPPLY							
I_{DD}	All Digital Inputs V_{IL} or V_{IH} All Digital Inputs 0V or V_{DD} All Digital Inputs 0V or V_{DD}	All	2 100 10	2 500 10	2 100 10	2 500 10	mA max μA max μA typ

NOTE 1: Temperature Ranges as follows: J, K versions: 0°C to +70°C
A, B versions: −20°C to +85°C
S version: −55°C to +125°C

2: This includes the effect of 5 ppm max gain TC.

3: Parameter not tested. Parameter guaranteed by design, simulation, or characterization.

4: DB0–DB11 = 0V to V_{DD} or V_{DD} to 0V.

5: Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.

6: Logic inputs are MOS gates. Typical input current (+25°C) is less than 1 nA.

Specifications subject to change without notice.

BASIC APPLICATIONS

Figures 7 and 8 show simple unipolar and bipolar circuits using the AD7545. Resistor R1 is used to trim for full scale. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. Note that the circuits of Figures 7 and 8 have constant input impedance at the V_{REF} terminal.

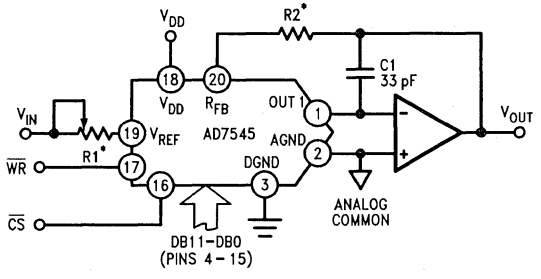
The circuit of Figure 7 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to $-V_{IN}$ (note the inversion introduced by the op amp) or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20 \leq V_{IN} \leq +20V$ (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD}. Table 2 shows the code relationship for the circuit of Figure 7.

Table 1: Recommended Trim Resistor Values vs. Grades for $V_{DD} = +5V$

TRIM RESISTOR	J/A/S	K/B
R1	500Ω	200Ω
R2	150Ω	68Ω

Table 2. Unipolar Binary Code Table for Circuit of Figure 7

Binary Number in DAC Register			Analog Output
1111	1111	1111	$-V_{IN}\left\{\frac{4095}{4096}\right\}$
1000	0000	0000	$-V_{IN}\left\{\frac{2048}{4096}\right\} = -\frac{1}{2}V_{IN}$
0000	0000	0001	$-V_{IN}\left\{\frac{1}{4096}\right\}$
0000	0000	0000	0V



*Refer to Table 1.

Figure 7: Unipolar Binary Operation

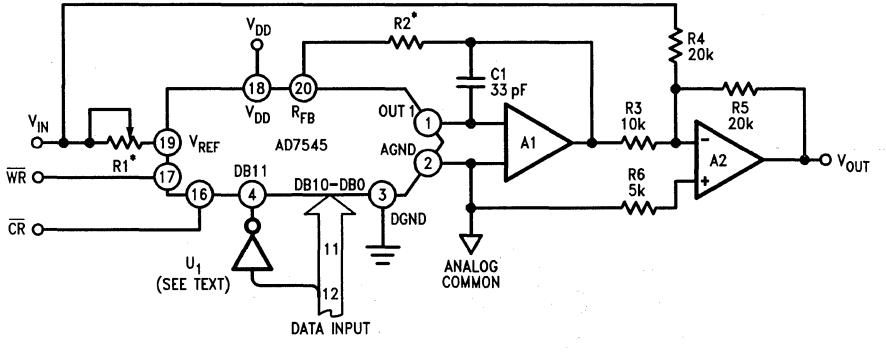
NOTE: All typical values have been characterized but are not tested.

AD7545

Figure 8 and Table 3 illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code and inverter U_1 on the MSB line converts 2's complement input code to offset binary code. If appropriate, inversion of the MSB may be done in software using an exclusive -OR instruction and the inverter omitted. R3, R4 and R5 must be selected to match within 0.01% and they should be the same type of resistor (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

Table 3: 2's Complement Code Table for Circuit of Figure 8

Data Input			Analog Output
0111	1111	1111	$+V_{IN} \bullet \left\{\frac{2047}{2048}\right\}$
0000	0000	0001	$+V_{IN} \bullet \left\{\frac{1}{2048}\right\}$
0000	0000	0000	0V
1111	1111	1111	$-V_{IN} \bullet \left\{\frac{1}{2048}\right\}$
1000	0000	0000	$-V_{IN} \bullet \left\{\frac{2048}{2048}\right\}$



*For Values of R1 and R2
See Table 1.

Figure 8: Bipolar Operation (2's Complement Code)

The choice of the operational amplifiers in Figures 7 and 8 depends on the application and the trade off between required precision and speed. Below is a list of operational amplifiers which are good candidates for many applications. The main selection criteria for these operational amplifiers is to have low V_{OS}, low V_{OS} drift, low bias current and low settling time.

These amplifiers need to maintain the low nonlinearity and monotonic operation of the D/A while providing enough speed for maximum converter performance.

Operational Amplifiers:

HA5127 Ultra Low Noise, Precision
HA5137 Ultra Low Noise, Precision, Wide Band
HA5147 Ultra Low Noise, Precision, High Slew Rate
HA5170 Precision, JFET Input

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

CA3338, CA3338A

CMOS Video-Speed 8-Bit R-2R Digital-to-Analog Converter

GENERAL DESCRIPTION

The Harris CA3338 family are CMOS/SOS high-speed R-2R voltage output digital-to-analog converters. They operate from a single 5V supply at video speeds, and can produce "rail-to-rail" output swings. Internal level shifters and a pin for an optional second supply provide for an output range below the digital ground. The data complement control allows the inversion of input data while the latch enable control provides either feed-through or latched operation. Both ends of the R-2R ladder network are available externally and may be modulated for gain or offset adjustments. In addition, "glitch" energy has been kept very low by segmenting and "bar graph" decoding of the upper 3 bits.

The CA3338 is manufactured on a sapphire substrate to give low dynamic power dissipation, low output capacitance, and inherent latch-up resistance.

FEATURES

- **CMOS/SOS Low Power**
- **R-2R Output, Segmented for Low "Glitch"**
- **CMOS or TTL Compatible Inputs**
- **Fast Settling: 20 ns (typ.) to ½ LSB**
- **Feedthrough Latch for Clocked or Unclocked Use**
- **Single or Dual Supplies, 4.5V to 7.5V Total**
- **½ LSB Accuracy (Typ.)**
- **Data Complement Control**
- **High Update Rate: 50 MHz (Typ.)**
- **Unipolar or Bipolar Operation**

APPLICATIONS

- **TV/Video Display**
- **High-Speed Oscilloscope Display**
- **Digital Waveform Generator**
- **Feed-Forward A/D Systems**

ORDERING INFORMATION

Part Number	Linearity (INL, DNL)	Temperature Range	Package
CA3338A	±1.0 LSB	-40°C to +85°C	16 Pin Plastic DIP
CA3338AE	±0.75 LSB	-40°C to +85°C	16 Pin Plastic DIP
CA3338D	±1.0 LSB	-55°C to +125°C	16 Pin Ceramic DIP
CA3338AD	±0.75 LSB	-55°C to +125°C	16 Pin Ceramic DIP
CA3338M	±1.0 LSB	-40°C to +85°C	16 Pin Plastic SOIC
CA3338AM	±0.75 LSB	-40°C to +85°C	16 Pin Plastic SOIC

16 LEAD CERAMIC DIP
16 LEAD PLASTIC DIP
16 LEAD SOIC

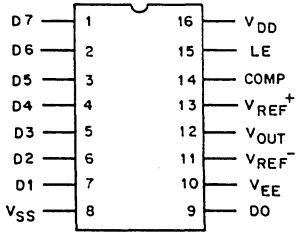


Figure 1: Pin Configuration

1850-001

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

DC Supply-Voltage Range
($V_{DD} - V_{SS}$ or $V_{DD} - V_{EE}$, whichever is greater) . . . . . −0.5V to +8V

Input Voltage Range
Digital Inputs (LE, COMP, D0–D7) . . . . . V_{SS} − 0.5V to V_{DD} +0.5V
Analog Pins
(V_{REF}^+, V_{REF}^-, V_{OUT}) . . . . . V_{DD} − 8V to V_{DD} + 0.5V

DC Input Current
Digital Inputs (LE, COMP, D0–D7) . . . . . ±20 mA

Power Dissipation per Package (P_D):
For T_A = −55°C to +55°C . . . . . 315 mW
For T_A = +55°C to +125°C
. . . . . Derate Linearly at 3.3 mW/°C

Operating-Temperature Range (T_A):
Ceramic Package—D Suffix . . . . . −55°C to +125°C
Plastic Package—E Suffix . . . . . −40°C to +85°C

Storage-Temperature
Range (T_{STG}) . . . . . −65°C to +150°C

Lead Temperature (During Soldering):
At Distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10s max. . . . . +265°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Supply Voltage Range . . . . . 4.5V to 7.5V

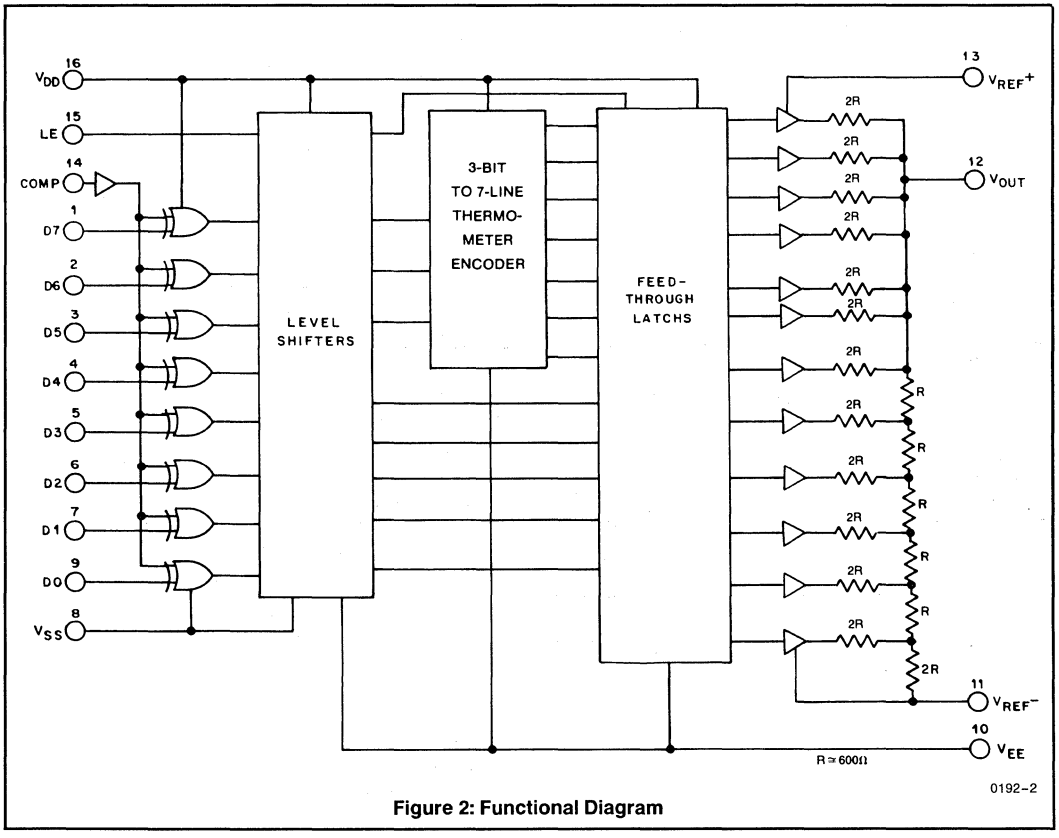


Figure 2: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{DD} = 5V$, $V_{REF}^+ = 4.608V$, $V_{SS} = V_{EE} = V_{REF}^- = GND$, LE clocked at 20 MHz, $R_L \geq 1\ M\Omega$ (unless otherwise specified)

Parameter	Test Conditions	Limits			Units
		Min	Typ	Max	
Accuracy					
Resolution		8			Bits
Integral Linearity Error	See Figure 6				
CA3338				±1	LSB
CA3338A				±0.75	LSB
Differential Linearity Error	See Figure 6				
CA3338				±0.75	LSB
CA3338A				±0.5	LSB
Gain Error	Input Code = FF_{16}; See Fig. 5				
CA3338				±0.75	LSB
CA3338A				±0.5	LSB
Offset Error	Input Code = 00_{16}; See Fig. 5			±0.25	LSB
Digital Input Timing					
Update Rate	To Maintain ½ LSB Settling	DC	50		MHz
Update Rate	$V_{REF}^- = V_{EE} = -2.5V$, $V_{REF}^+ = +2.5V$	DC	20		MHz
Set Up Time T_{SU1}	For Low Glitch		−2		ns
Set Up Time T_{SU2}	For Data Store		8		ns
Hold Time T_H	For Data Store		5		ns
Latch Pulse Width T_W	For Data Store		5		ns
Latch Pulse Width T_W	$V_{REF}^- = V_{EE} = -2.5V$, $V_{REF}^+ = +2.5V$		25		ns
Output Parameters	R_L Adjusted for 1 V_{p-p} Output				
Output Delay T_{D1}	From LE Edge		25		ns
Output Delay T_{D2}	From Data Changing		22		ns
Rise Time T_R	10 to 90% of Output		4		ns
Settling Time T_S	10% to Settling to ½ LSB		20		ns
Output Impedance	$V_{REF+} = 6V$, $V_{DD} = 6V$	120	160	200	Ω
Glitch Area			150		pV-s
Glitch Area	$V_{REF}^- = V_{EE} = -2.5V$, $V_{REF}^+ = +2.5V$		250		pV-s
Reference Voltage					
V_{REF}^+ Range	(+) Full Scale (Note 1)	$V_{REF}^- + 3$		V_{DD}	V
V_{REF}^- Range	(−) Full Scale (Note 1)	V_{EE}		$V_{REF}^+ - 3$	V
V_{REF}^+ Input Current	$V_{REF+} = 6V$, $V_{DD} = 6V$		40	50	mA
Supply Voltage					
Static I_{DD} or I_{EE}	LE = Low, D_0–D_7 = High		100	220	μA
	LE = Low, D_0–D_7 = Low			100	μA
Dynamic I_{DD} or I_{EE}	V_{OUT} = 10 MHz, 0V to 5V Sq. Wave		20		mA
Dynamic I_{DD} or I_{EE}	V_{OUT} = 10 MHz, ±2.5V Sq. Wave		25		mA
V_{DD} Rejection	50 kHz Sine Wave Applied		3		mV/V
V_{EE} Rejection	50 kHz Sine Wave Applied		1		mV/V
Digital Inputs	D0–D7, LE, COMP				
High Level Input Voltage	(Note 1)	2			V
Low Level Input Voltage	(Note 1)			0.8	V
Leakage Current			±1	±5	μA
Capacitance			5		pF
Temperature Coefficients					
Output Impedance			200		PPM/°C

NOTE 1: Parameter not tested, but guaranteed by design or characterization.

NOTE: All typical values have been characterized but are not tested.

Table 1: Pin Descriptions

Pin	Name	Description
1	D7	Most Significant Bit
2	D6	Input
3	D5	Data
4	D4	Bits
5	D3	(High = True)
6	D2	
7	D1	
8	V_{SS}	Digital ground
9	D_0	Least Significant Bit. Input Data Bit.
10	V_{EE}	Analog ground
11	V_{REF-}	Reference voltage negative input
12	V_{OUT}	Analog output
13	V_{REF+}	Reference voltage positive input
14	COMP	Data complement control input. Active high.
15	LE	Latch enable input. Active low.
16	V_{DD}	Digital power supply, +5V

DIGITAL SIGNAL PATH

The digital inputs (LE, COMP, and D0–D7) are of TTL compatible HCT High Speed CMOS design: the loading is essentially capacitive and the logic threshold is typically 1.5V.

The 8 data bits, D0 (weighted 2^0) through D7 (weighted 2^7), are applied to Exclusive OR gates (see Figure 2). The COMP (data complement) control provides the second input to the gates: if COMP is high, the data bits will be inverted as they pass through.

The input data and the LE (latch enable) signals are next applied to a level shifter. The inputs, operating between the levels of V_{DD} and V_{SS}, are shifted to operate between V_{DD} and V_{EE}. V_{EE} optionally at ground or at a negative voltage, will be discussed under bipolar operation. All further logic elements except the output drivers operate from the V_{DD} and V_{EE} supplies.

The upper 3 bits of data, D5 through D7, are input to a 3-to-7 line bar graph encoder. The encoder outputs and D0 through D4 are applied to a feedthrough latch, which is controlled by LE (latch enable).

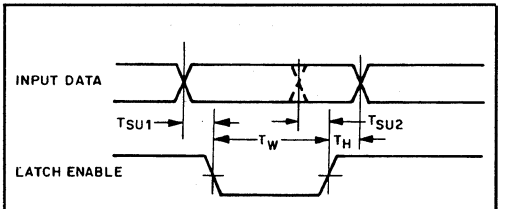


Figure 3: Data to Latch Enable Timing

LATCH OPERATION

Data is fed from input to output while LE is low: LE should be tied low for non-clocked operation.

Non-clocked operation or changing data while LE is low is not recommended for applications requiring low output "glitch" energy: there is no guarantee of the simultaneous changing of input data or the equal propagation delay of all bits through the converter. Several parameters are given if the converter is to be used in either of these modes: T_{D2} gives the delay from the input changing to the output changing (10%), while t_{SU2} and T_H give the set up and hold times (referred to LE rising edge) needed to latch data. See Figures 3 and 4.

Clocked operation is needed for low "glitch" energy use. Data must meet the given T_{SU1} set up time to the LE falling edge, and the T_H hold time from the LE rising edge. The delay to the output changing, T_{D1}, is now referred to the LE falling edge.

There is no need for a square wave LE clock; LE must only meet the minimum TW pulse width for successful latch operation. Generally, output timing (desired accuracy of settling) sets the upper limit of usable clock frequency.

OUTPUT STRUCTURE

The latches feed data to a row of high current CMOS drivers, which in turn feed a modified R-2R ladder network.

The "N" channel (pull down) transistor of each driver plus the bottom "2R" resistor are returned to V_{REF}^-; this is the (−) full-scale reference. The "P" channel (pull up) transistor of each driver is returned to V_{REF}^+, the (+) full-scale reference.

In unipolar operation, V_{REF}^- would typically be returned to analog ground, but may be raised above ground (see specifications). There is substantial code dependent current that flows from V_{REF}^+ to V_{REF}^- (see V_{REF}^+ input current in specifications), so V_{REF}^- should have a low impedance path to ground.

NOTE: All typical values have been characterized but are not tested.

OUTPUT STRUCTURE (Continued)

In bipolar operation, V_{REF}^- would be returned to a negative voltage (the maximum voltage rating to V_{DD} must be observed). V_{EE}, which supplies the gate potential for the output drivers, must be returned to a point at least as negative as V_{REF}^-. Note that the maximum clocking speed decreases when the bipolar mode is used.

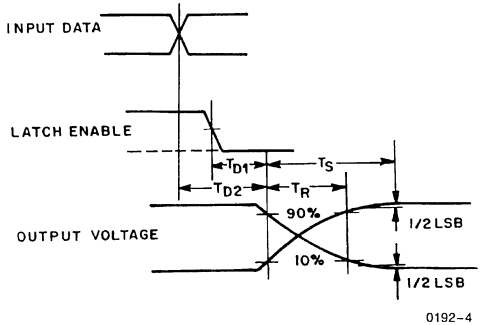


Figure 4: Data and Latch Enable to Output Timing

STATIC CHARACTERISTICS

The ideal 8-bit D/A would have an output equal to V_{REF}^- with an input code of 00_{16} (zero scale output), and an output equal to 255/256 of V_{REF}^+ (referred to V_{REF}^-) with an input code of FF_{16} (full-scale output). The difference between the ideal and actual values of these two parameters are the OFFSET and GAIN errors respectively: see Figure 5.

If the code into an 8-bit D/A is changed by 1 count, the output should change by 1/255 (full-scale output—zero-scale output). A deviation from this step-size is a differential linearity error: see Figure 6. Note that the error is expressed in fractions of the ideal step size (usually called an LSB). Also note that if the (−) differential linearity error is less (in absolute numbers) than 1 LSB, the device is monotonic. (The output will always increase for increasing code or decrease for decreasing code).

If the code into an 8-bit D/A is at any value, say "N", the output voltage should be N/255 of the full-scale output (referred to the zero-scale output). Any deviation from that output is an integral linearity error, usually expressed in LSB's. See Figure 6.

Note that OFFSET and GAIN errors do not affect integral linearity, as the linearity is referenced to actual zero and full-scale outputs, not ideal. Absolute accuracy would have to also take these errors into account.

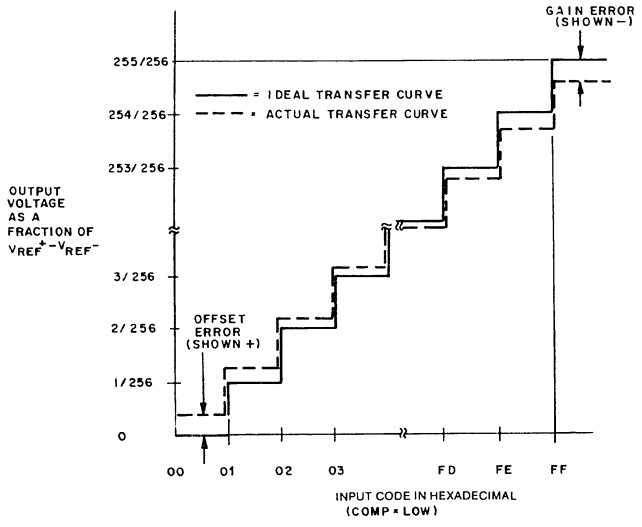


Figure 5: D/A Offset and Gain Error

NOTE: All typical values have been characterized but are not tested.

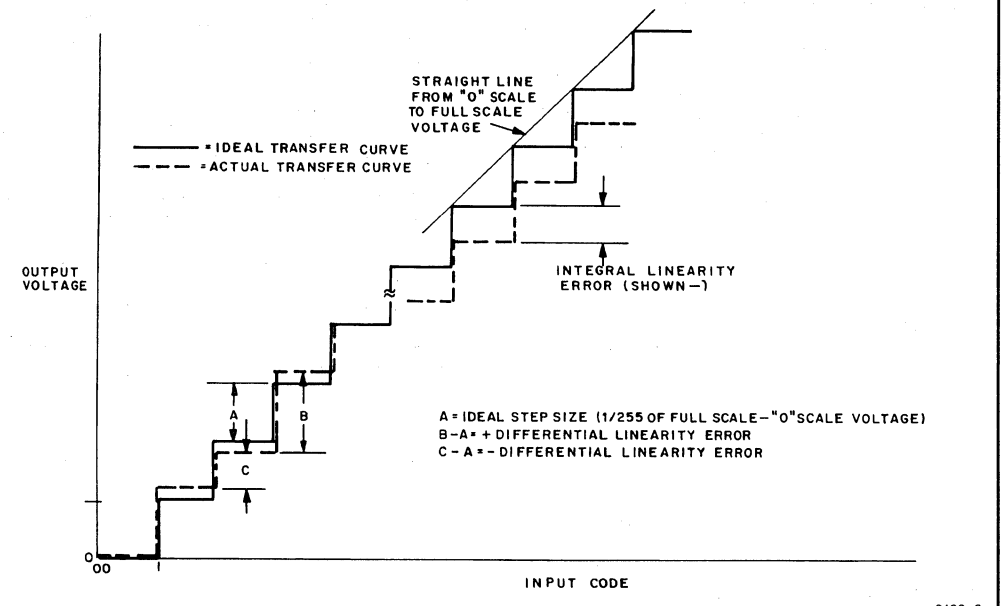


Figure 6: D/A Integral and Differential Linearity Error

DYNAMIC CHARACTERISTICS

Keeping the full-scale range ($V_{REF}^+ - V_{REF}^-$) as high as possible gives the best linearity and lowest "glitch" energy (referred to 1V). This provides the best "P" and "N" channel gate drives (hence saturation resistance) and propagation delays. The V_{REF}^+ (and V_{REF}^- if bipolar) terminal should be well bypassed as near the chip as possible.

"Glitch" energy is defined as a spurious voltage that occurs as the output is changed from one voltage to another. In a binary input converter, it is usually highest at the most significant bit transition ($7F_{16}$ to 80_{16} for an 8 bit device), and can be measured by displaying the output as the input code alternates around that point. The "glitch" energy is the area between the actual output display and an ideal one LSB step voltage (subtracting negative area from positive), at either the positive or negative-going step. It is usually expressed in pV-s.

The CA3338 uses a modified R-2R ladder, where the 3 most significant bits drive a bar graph decoder and 7 equally weighted resistors. This makes the "glitch" energy at each $\frac{1}{8}$ scale transition ($1F_{16}$ to 20_{16}, $3F_{16}$ to 40_{16}, etc.) essentially equal, and far less than the MSB transition would otherwise display.

For the purpose of comparison to other converters, the output should be resistively divided to 1V full-scale. Figure 7 shows a typical hook-up for checking "glitch" energy or settling time.

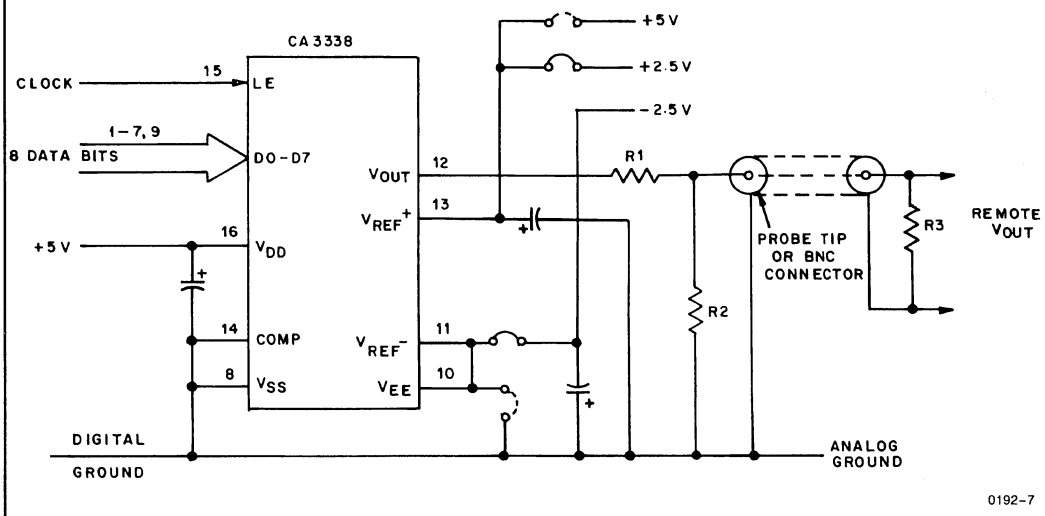
The settling time of the A/D is mainly a function of the output resistance (approximately 160Ω in parallel with the load resistance) and the load plus internal chip capacitance. Both "glitch" energy and settling time measurements require very good circuit and probe grounding: a probe tip connector such as Tektronix part number 131-0258-00 is recommended.

APPLICATIONS

The output of the CA3338 can be resistively divided to match a doubly terminated 50Ω or 75Ω line, although peak-to-peak swings of less than 1V may result. The output magnitude will also vary with the converter's output impedance. Figure 7 shows such an application. Note that because of the HCT input structure, the CA3338 could be operated up to +7.5V V_{DD} and V_{REF}^+ supplies and still accept 0V to 5V CMOS input voltages.

If larger voltage swings or better accuracy is desired, a high speed output buffer, such as the HA-5033, HA-2542, or CA3450, can be employed. Figure 8 shows a typical application, with the output capable of driving ±2V into multiple 50Ω terminated lines.

NOTE: All typical values have been characterized but are not tested.



Function:	Connector	R1	R2	R3	V_{OUT} (PK-PK)
Oscilloscope Display	Probe Tip	82Ω	62Ω	N/C	1V
Match 93Ω Cable	BNC	75	160	93	1V
Match 75Ω Cable	BNC	18	130	75	1V
Match 50Ω Cable	BNC	Short	75	50	0.79V

NOTES 1: V_{OUT}(PK) is approximate, and will vary as R_{OUT} of D/A varies.

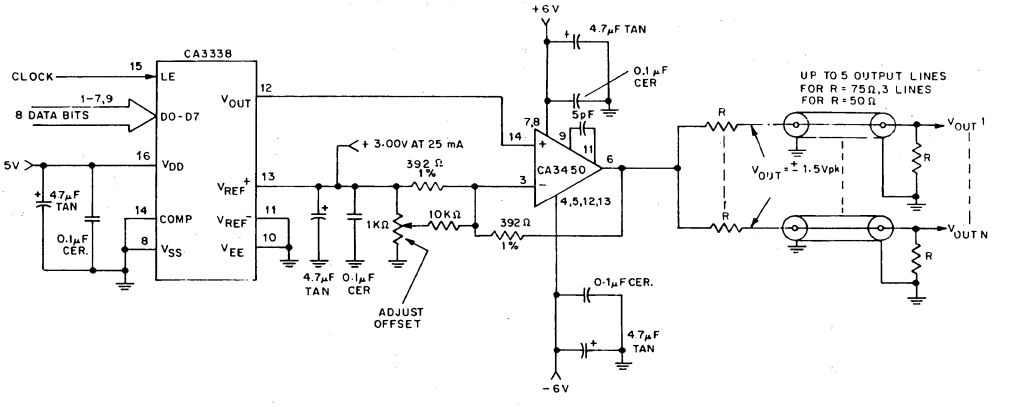
2: All drawn capacitors are 0.1 μF multilayer ceramic//4.7 μF tantalum.

3: Dashed connections are for unipolar operation, solid for bipolar.

Figure 7: CA3338 Dynamic Test Circuit

6

NOTE: All typical values have been characterized but are not tested.



NOTES 1: Both V_{REF}^+ pin and 392Ω resistor should be bypassed within ¼ in.

2: Keep nodal capacitance at CA3450 pin 3 as low as possible.

3: V_{OUT} Range = ±3V at CA3450.

Figure 8: CA3338 and CA3450 for Driving Multiple Coaxial Lines

Table 2: Output Voltage vs Input Code and V_{REF}

V_{REF}^+ V_{REF}^- Step Size	5.12V 0 0.0200V	5.00V 0 0.0195V	4.608V 0 0.0180V	2.56V −2.56V 0.0200V	2.50V −2.50V 0.0195V
Input Code					
$1111\ 1111_2 = FF_{16}$	5.1000V	4.9805V	4.5900V	2.5400V	2.4805V
$1111\ 1110_2 = FE_{16}$	5.0800	4.9610	4.5720	2.5200	2.4610
•					
•					
•					
$1000\ 0001_2 = 81_{16}$	2.5800	2.5195	2.3220	0.0200	0.0195
$1000\ 0000_2 = 80_{16}$	2.5600	2.5000	2.3040	0.0000	0.0000
$0111\ 1111_2 = 7F_{16}$	2.5400	2.4805	2.2860	−0.0200	−0.0195
•					
•					
•					
$0000\ 0001_2 = 01_{16}$	0.0200	0.0195	0.0180	−2.5400	−2.4805
$0000\ 0000_2 = 00_{16}$	0.0000	0.0000	0.0000	−2.5600	−2.5000

NOTE: All typical values have been characterized but are not tested.

OPERATING AND HANDLING OPERATIONS

1. **Handling**

   All inputs and outputs of CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. **Operating**

   Operating Voltage

   During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause the absolute maximum ratings to be exceeded.

   Input Signals

   To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 20 mA even when the power supply is off.

   Unused Inputs

   A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or GND, whichever is appropriate.

NOTE: All typical values have been characterized but are not tested.

HARRIS

HI-562A

12-Bit High Speed Monolithic Digital-to-Analog Converter

Features

- Output Current ..... 2mA, F.S.
- Monolithic Construction
- Extremely Fast Settling ..... 300ns To 0.01% (Typ)
- Low Gain Drift ..... ±10ppm/°C (Max)
- Linearity Guaranteed Over Temperature... ±1/2 LSB (Max)
- Designed for Minimum Glitches
- Monotonic Over Temperature

Applications

- CRT Display Generation
- High Speed A/D Converters
- Video Signal Reconstruction
- Waveform Synthesizers
- High Speed Data Acquisition
- High-Rel Applications
- Precision Instruments

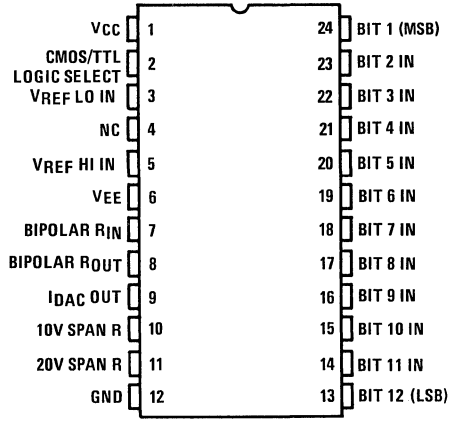
Description

The Harris HI-562A is the first monolithic digital-to-analog converter to combine both high speed performance and 12-bit accuracy on the same chip. The HI-562A's fast output current settling of 300ns to 0.01% is achieved using Dielectric Isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-562A by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-ON and turn-OFF switching times. This creates within the chip a very uniform and constant thermal distribution for excellent linearity and also completely eliminates thermal transients during switching. High stability thin film resistor processing together with laser trimming provide the HI-562A with guaranteed 12-bit linearity to within ±1/2LSB maximum at +25°C for -4 and -5 parts and to within ±1/4LSB maximum at +25°C for -2 and -8 parts. The HI-562A is recommended as a replacement for higher cost hybrid and modular units for increased reliability and accuracy in applications such as CRT displays, precision instruments and data acquisition systems requiring throughput rates as high as 3.3MHz for full range transitions. Its small size makes it an ideal choice as the heart of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-562A is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

The HI-562A is offered in commercial, industrial and military grades. The HI-562A is available in a 24 pin Ceramic Sidebraze DIP. For MIL-STD-883 compliant parts, request the HI-562A/883 data sheet.

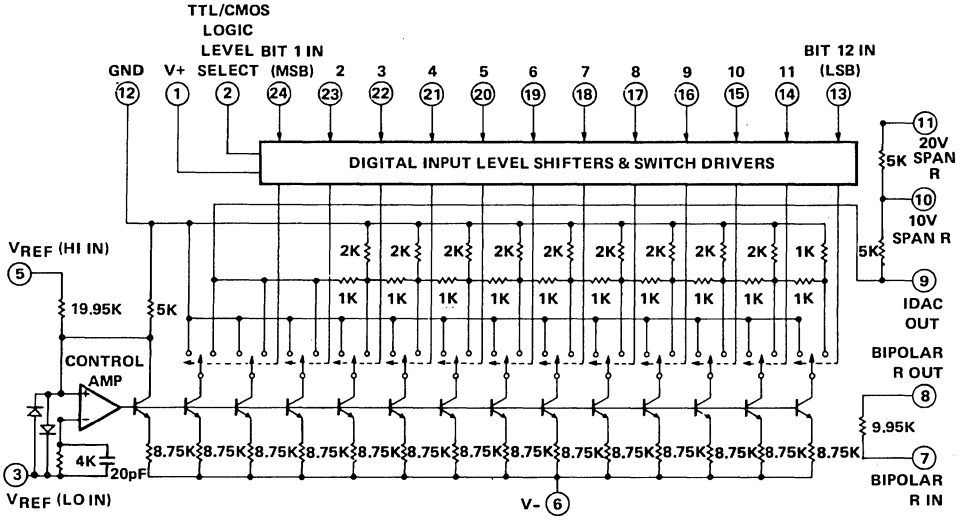
Pinouts

HI1-562A (CERAMIC SIDEBRAZE DIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC handling procedures.

Functional Diagram



NOTE: Pin Numbers Refer to DIP Package Only.

Specifications HI-562A

Absolute Maximum Ratings (Referred to GND, Note 1)

Power Supply Inputs
- V_{ps+} ..... +20V
- V_{ps-} ..... -20V

Reference Inputs
- V_{REF} (High) ..... ±16.5V

Digital Inputs
- Bits 1-12 (TTL) ..... -1V, +7.5V
- Bits 1-12 (CMOS) ..... -1V, V_{ps+}
- CMOS/TTL Logic Select ..... -1V, +16.5V

Outputs
- Pins 7, 8, 10, 11 ..... $\pm V_{ps}$
- Pin 9 ..... $+V_{ps}$, -5V

Junction Temperature ..... +175°C

Operating Temperature Range

HI-562A-2 ..... -55°C to +125°C
HI-562A-4 ..... -25°C to +85°C
HI-562A-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications

(@ +25°C, V_{ps+} = +5V, V_{ps-} = -15V, V_{REF} = +10V, CMOS/TTL Logic Select = GND, Unless Otherwise Specified.)

PARAMETER	CONDITION	HI-562A-2 MIN	HI-562A-2 TYP	HI-562A-2 MAX	HI-562A-4/HI-562A-5 MIN	HI-562A-4/HI-562A-5 TYP	HI-562A-4/HI-562A-5 MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (Note 3)	Bit ON "Logic 1"							
TTL/CMOS Input Voltage (Note 2)	Bit OFF "Logic 0"							
Logic "1"		2.0			2.0			V
Logic "0"	(V_{ps+} <9.5V)			0.8			0.8	V
TTL/CMOS Input Current (Note 2)	Pin 2 Tied to Pin 12							
Logic "1"	Over Full Temperature Range		20	±500		20	±500	nA
Logic "0"			-50	-100		-50	-100	µA
CMOS Input Voltage								
Logic "1"		0.7V_{ps+}			0.7V_{ps+}			V
Logic "0"	Pin 2 Tied to Pin 1 ($V_{ps+} \geq$ +9.5V)			0.3V_{ps+}			0.3V_{ps+}	V
CMOS Input Current								
Logic "1"	Over Full Temperature Range		20	±500		20	±500	nA
Logic "0"			-50	-100		50	-100	µA
Reference Input								
Input Resistance	(±20%)		19.95K			19.95K		Ω
Input Voltage			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Over Full Temperature Range			12			12	Bits
Nonlinearity (Note 3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over Full Temperature Range		±1/2	±1			±1	LSB
Differential Nonlinearity (Note 3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over Full Temperature Range		MONOTONICITY GUARANTEED					
Relative Accuracy (Note 6)	With 50Ω (1%) Resistors							
Gain Error	All Bits ON		±0.024	±0.25		±0.024	±0.25	%FSR
Bipolar Offset Error	All Bits OFF		±0.024	±0.25		±0.024	±0.25	%FSR
Unipolar Offset Error	All Bits OFF		±0.012	±0.05		±0.012	±0.05	%FSR (Note 4)
Adjustment Range	See Operating Instructions							
Gain	With 100Ω Trim		±0.3			±0.3		%FSR
Bipolar Offset	Potentiometers		±0.6			±0.6		%FSR
Temperature Stability	Drift Specified With Internal Span Resistors For Volt. Output							
Gain Drift (Note 3)	Over Full Temperature Range		±6	±10			±10	ppm of FSR/°C
Offset Drift (Note 3)	Over Full Temperature Range							
Unipolar Offset	All Bits OFF			±2			±2	ppm of FSR/°C
Bipolar Offset	All Bits OFF			±4			±4	
Differential Nonlin.	Over Full Temperature Range		±1	±2		±1	±2	ppm of FSR/°C
Settling Time (Note 3) to ±1/2LSB	All Bits ON-to-OFF or OFF-to-ON		300	400		300	400	ns

Specifications HI-562A

Electrical Specifications (Continued)

PARAMETER	CONDITIONS	HI-562A-2 MIN	HI-562A-2 TYP	HI-562A-2 MAX	HI-562A-4/HI-562A-5 MIN	HI-562A-4/HI-562A-5 TYP	HI-562A-4/HI-562A-5 MAX	UNITS
Major Carry Transient								
Peak Amplitude Settling	From 011...1 to 100...0		0.7			0.7		mA
Time to 90% Complete	or 100...0 to 011...1		35			35		ns
Power Supply Sensitivity (Note 3)								
Unipolar Offset								
V_{ps+} @ +5V or +15V	All Bits OFF		±0.5			±0.5		ppm of
V_{ps-} @ -15V	"		±0.5			±0.5		FSR/
Bipolar Offset								$\%V_{ps}$
V_{ps+} @ +5V or +15V	All Bits OFF, Bipolar Mode		±1.5			±1.5		ppm of
V_{ps-} @ -15V	"		±1.5			±1.5		FSR/
Gain								$\%V_{ps}$
V_{ps+} @ +5V or +15V	All Bits ON			±3.5			±3.5	ppm of
V_{ps-} @ -15V				±7.5			±7.5	FSR/
								$\%V_{ps}$
OUTPUT CHARACTERISTICS								
Output Current								
Unipolar		-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar		±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance			2K			2K		Ω
Capacitance			20			20		pF
Output Voltage Ranges								
Unipolar	Using External Op Amp		0 to+5			0 to +5		V
	and Internal Scaling Resistors.		0 to +10			0 to +10		V
Bipolar	See Figure 1 and Table 1		±2.5			±2.5		V
	For Connections		±5			±5		V
			±10			±10		V
Compliance Limit (Note 3)		-3		+10	-3		+10	V
Compliance Voltage (Note 3)	Over Full Temperature Range		±1.0			±1.0		V
Output Noise	0.1 to 10Hz (All Bits ON)		30			30		μV_{p-p}
	0.1 to 5MHz (All Bits ON)		100			100		μV_{p-p}
POWER REQUIREMENTS								
V_{ps+} (Note 7)	Over Full Temperature Range	4.5	5	16.5	4.75	5	16.5	V
V_{ps-}	Over Full Temperature Range	-13.5	-15	-16.5	-13.5	-15	-16.5	V
I_{ps+} (Note 5)	All Bits ON or OFF in Either		8	15		8	15	mA
I_{ps-} (Note 5)	TTL or CMOS Mode (25°C)		16	23		16	23	mA
I_{ps+} (Note 5)	Same as Above Except		11	20		11	20	mA
I_{ps-} (Note 5)	Over Full Temperature Range		20	30		20	30	mA
Power Dissipation (25°C)	V_{ps+} = +5V, V_{ps-} = -15V		280	420		280	420	mW

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{ps+} tolerance is ±10% for HI-562A-2, and ±5% for HI-562A-4, -5.
3. See Definitions.
4. FSR is "Full Scale Range" and is 20V for ±10V ranges, 10V for ±5V ranges, etc., or 2mA (±20%) for current output.
5. After 30 seconds warm-up.
6. Using an external op amp with internal span resistors and specified external trim resistors in place of potentiomenters R1 and R2. Errors are adjustable to zero using R1 and R2 potentiometers. (See Operating Instructions Figure 2.)
7. The HI-562A is designed for V_{ps+} = 5V, but +4.5V ≤ V_{ps+} ≤ 16.5V may be connected if convenient (For V_{ps+} above +5V, there is an increase in power dissipation but little change in performance.)

Die Characteristics

Transistor Count 150
Die Dimensions ..... 103 x 209 mils

Thermal Impedance (°C/W)	θ_{ja}	θ_{jc}
Sidebraze DIP	50	15
Ceramic LCC	81	40

Tie Substrate to ..... V_{REF} Low (Analog Ground)
Process ..... Bipolar-DI

Definitions of Specifications

Digital Inputs

The HI-562A accepts digital input codes in binary format and may be user connected for any one of three binary codes: Straight Binary, Two's Complement, or Offset Binary (see Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement*
MSB LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	1/2 FS	Zero	-FS
111...111	+FS - 1 LSB	+FS - 1 LSB	1/2 FS - 1 LSB
011...111	1/2 FS - 1 LSB	Zero - 1 LSB	+FS - 1 LSB
*Invert MSB with external inverter to obtain Two's Complement Coding			

Accuracy

INTEGRAL NONLINEARITY — The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL NONLINEARITY — The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY — The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

Settling Time

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low.

Drift

GAIN DRIFT — The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low (+25°C - T_L) ranges by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT — The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C - T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, +5V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%Vps).

Compliance

Compliance Voltage is the maximum output range for which specified accuracy limits are guaranteed. Compliance Limit implies functional operation only and makes no claims to accuracy.

Glitch

A glitch on the output of a D/A converter is a large transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

Operating Instructions

Decoupling and Grounding

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-562A (preferably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

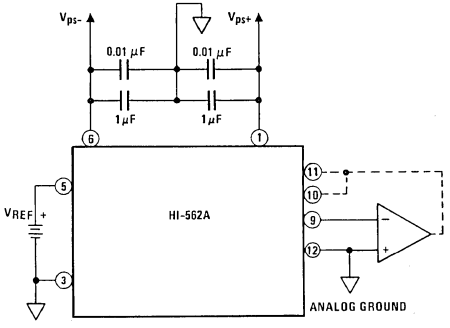
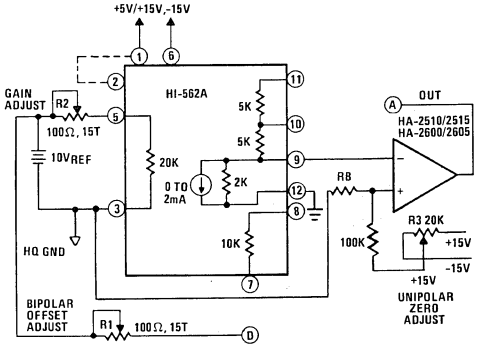


FIGURE 1.

Unipolar and Bipolar Voltage Output Connections

CONNECTIONS — Using an external resistive load, the output compliance should not exceed ±1V to maintain specified accuracy. For higher output voltages, accuracy can be maintained by using an external op amp and the internal span resistors as shown in Figure 2 and defined in Table 1 for unipolar and bipolar modes.



*For TTL and DTL compatibility, connect +5V to pin 1 and tie pin 2 to pin 12. For CMOS compatibility, connect digital power supply (9.5V ≤ VDD ≤ +12V) to pin 1 and short pin 2 to pin 1.

**Bias resistor, RB, should be chosen to equalize op amp offset voltage due to bias current. Its value is calculated from the parallel combination of the current source output resistance (2K) and the op amp feedback resistor. See Table 1 for values of RB.

FIGURE 2.

TABLE 1.

	CONNECTIONS					
	OUTPUT RANGE	PIN 7 TO	PIN 8 TO	PIN 10 TO	PIN 11 TO	BIAS (RB) RESISTOR
Unipolar Mode	0 to +10V	NC	NC	A	NC	1.43K
	0 to +5V	NC	NC	A	9	1.11K
Bipolar Mode	±10V	D	9	NC	A	760Ω
	±5V	D	9	A	NC	840Ω
	±2.5V	D	9	A	9	766Ω

External Gain and Zero Calibration (See Figure 2)

The input reference resistor (20K nominal) and bipolar offset resistors shown in Figure 2 are both intentionally set low by 50Ω to allow the user to externally trim-out initial errors to a very high degree of precision. The adjustments are made in the voltage output mode using an external op amp as current-to-voltage converter and the HI-562A internal scaling resistors as feedback elements for optimum accuracy and temperature coefficient. For best accuracy over temperature, select an op amp that has good front-end temperature coefficients such as the HA-2600/2605 with offset voltage and offset current tempco's of 5µV/°C in 1nA/°C, respectively. For high speed voltage mode applications where fast settling is required, the HA-2510/2515 is recommended for better than 1.5µs settling to 0.01%. Using either one, potentiometer R3 conveniently nulls unipolar offset plus op amp offset in one operation (for HA-2510/2515 and HA-2600/2605 use R3 = 20K and 100K, respectively). For bipolar mode operation, R3 should be used to null op amp offset to optimize its tempco (i.e., short 9 to A and adjust R3 for zero before calibrating in bipolar mode). The gain and bipolar offset adjustment range using 100Ω potentiometers is ±12 LSB and ±25 LSB, respectively. If desired, the potentiometers can be replaced with fixed 50Ω (1%) resistors resulting in an initial gain and bipolar offset accuracy of typically ±1/2 LSB.

UNIPOLAR CALIBRATION

Step 1: Unipolar Offset
- Turn all bits OFF
- Adjust R3 for zero volts output

Step 2: Gain
- Turn all bits ON
- Adjust R2 for an output of FS - 1 LSB
  That is, adjust for:
  9.9976V for 0V to +10V range
  4.9988V for 0V to +5V range

BIPOLAR CALIBRATION

Step 1: Bipolar Offset
- Turn all bits OFF
- Adjust R1 for an output of:
  -10V for ±10V range
  -5V for ±5V range
  -2.5V for ±2.5V range

Step 2: Gain
- Turn bit 1 (MSB) ON; all other bits OFF
- Adjust R2 for zero volts output

HARRIS

HI-565A

High Speed Monolithic Digital-to-Analog Converter with Reference

Features

- DAC AND REFERENCE ON A SINGLE CHIP
- PIN COMPATIBLE WITH AD565A
- VERY HIGH SPEED: SETTLES TO 1/2 LSB IN 250ns, MAX. FULL SCALE SWITCHING TIME 30ns, TYP.
- GUARANTEED FOR OPERATION WITH ±12V SUPPLIES
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- 1/2 LSB MAX NONLINEARITY GUARANTEED OVER TEMPERATURE
- LOW GAIN DRIFT (MAX, DAC PLUS REFERENCE) 25ppm/°C
- LOW POWER DISSIPATION 250mW

Applications

- CRT DISPLAYS
- HIGH SPEED A/D CONVERTERS
- SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIS

Description

The HI-565A is a fast, 12 bit current output, digital to analog converter. The monolithic chip includes a precision voltage reference, thin-film R-2R ladder, reference control amplifier and twelve high-speed bipolar current switches.

The Harris Semiconductor dielectric isolation process provides latch-free operation while minimizing stray capacitance and leakage currents, to produce an excellent combination of speed and accuracy. Also, ground currents are minimized to produce a low and constant current through the ground terminal, which reduces error due to code-dependent ground currents.

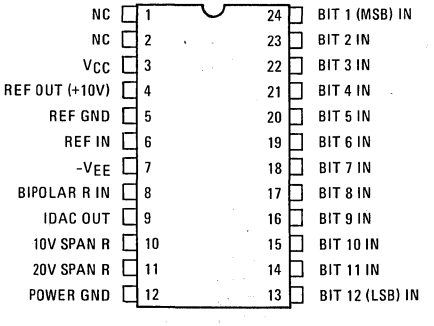
HI-565A dice are laser trimmed for a maximum integral non-linearity error of ±1/4 LSB at +25°C. In addition, the low noise buried zener reference is trimmed both for absolute value and minimum temperature coefficient.

The HI-565A is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. See Ordering Information.

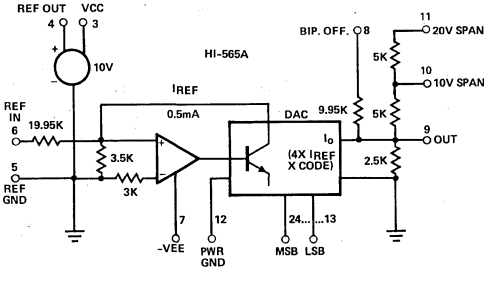
Package is a 24 pin side-brazed ceramic DIP. Power dissipation is typically 250mW, with ±15V supplies.

Pinout

TOP VIEW



Functional Diagram



Specifications HI-565A

Absolute Maximum Ratings*

V_{CC} to Power Ground . . . . . 0V to +18V
V_{EE} to Power Ground . . . . . 0V to -18V
Voltage on DAC Output (Pin 9) . . . . . -3V to +12V
Digital Inputs (Pins 13-24) to Power Ground . . . . . -1V to +7.0V
Ref In to Reference Ground . . . . . ±12V
Bipolar Offset to Reference Ground . . . . . ±12V
Junction Temperature . . . . . 175°C

10V Span R to Reference Ground . . . . . ±12V
20V Span R to Reference Ground . . . . . ±24V
Ref Out . . . . . Indefinite Short to Power Ground
Momentary Short to V_{CC}
Operating Temperature Ranges:
HI-565AS, T-2 . . . . . -55°C to +125°C
HI-565AJ, K-5 . . . . . 0°C to +75°C
HI-565AS, T-8 . . . . . -55°C to +125°C

*Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired.

Electrical Specifications (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, unless otherwise specified)

MODEL	HI-565AJ, HI-565AS			HI-565AK, HI-565AT			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
DATA INPUTS (Note 1) (Pins 13 to 24)							
TTL or 5V CMOS (T_{MIN} to T_{MAX})							
Input Voltage							
Bit ON Logic "1"	+2.0		+5.5	+2.0		+5.5	V
Bit OFF Logic "0"			+0.8			+0.8	V
Logic Current (Each Bit)							
Bit ON Logic "1"		.01	+1.0		.01	+1.0	μA
Bit OFF Logic "0"		-2.0	-20		-2.0	-20	μA
RESOLUTION			12			12	Bits
OUTPUT							
Current Unipolar (All Bits On)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar (All Bits on or Off)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance (Exclusive of Span Resistors)	1.8k	2.5k	3.2k	1.8k	2.5k	3.2k	Ω
Offset Unipolar		0.01	0.05		0.01	0.05	% of F.S.
Bipolar (Figure 2, R_3 = 50Ω Fixed)		0.05	0.15		0.05	0.1	% of F.S.
Capacitance		20			20		pF
Compliance Voltage, T_{MIN} to T_{MAX}	-1.5		+10	-1.5		+10	V
ACCURACY (Error Relative to Full Scale)							
+25°C		±1/4 (0.006)	±1/2 (0.012)		±1/8 (0.003)	±1/4 (0.006)	LSB % of F.S.
T_{MIN} to T_{MAX}		±1/2 (0.012)	±3/4 (0.018)		±1/4 (0.006)	±1/2 (0.012)	LSB % OF F.S.
DIFFERENTIAL NONLINEARITY							
+25°C		±1/2	±3/4		±1/4	±1/2	LSB
T_{MIN} to T_{MAX}	MONOTONICITY GUARANTEED						
TEMPERATURE COEFFICIENTS							
With Internal Reference							
Unipolar Zero		1	2		1	2	ppm/°C
Bipolar Zero		5	10		5	10	ppm/°C
Gain (Full Scale)		15	40		10	25	ppm/°C
Differential Nonlinearity		2			2		ppm/°C
SETTLING TIME TO 1/2 LSB							
With High Z External Load (Note 2)		350	500		350	500	ns
With 75Ω External Load		150	250		150	250	ns

Specifications HI-565A

MODEL	HI-565AJ, HI-565AS MIN	HI-565AJ, HI-565AS TYP	HI-565AJ, HI-565AS MAX	HI-565AK, HI-565AT MIN	HI-565AK, HI-565AT TYP	HI-565AK, HI-565AT MAX	UNITS
FULL SCALE TRANSITION (From 50% of Logic Input to 90% of Analog Output)							
Rise Time		15	30		15	30	ns
Fall Time		30	50		30	50	ns
TEMPERATURE RANGE							
Operating (HI-565AJ/K)	0		+75	0		+75	°C
(HI-565AS/T)	-55		+125	-55		+125	°C
Storage							
D Package (All)	-65		+150	-65		+150	°C
N Package (J, K)	-25		+150	-25		+150	°C
POWER REQUIREMENTS							
I_{CC}, +11.4 to +16.5V DC		9.0	11.8		9.0	11.8	mA
I_{EE}, -11.4 to -16.5V DC		-9.5	-14.5		-9.5	-14.5	mA
POWER SUPPLY GAIN SENSITIVITY (Note 3)							
V_{CC} = +11.4 to +16.5 VDC		3	10		3	10	ppm of F.S./%
V_{EE} = -11.4 to -16.5 VDC		15	25		15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGES (See Table 1)	0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			0 to +5 -2.5 to +2.5 0 to +10 -5 to +5 -10 to +10			V V V V V
EXTERNAL ADJUSTMENTS							
Gain Error with Fixed 50Ω Resistor for R2 (Figure 1)		±0.1	±0.25		±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resistor for R3 (Figure 2)		±0.05	±0.15		±0.05	±0.1	% of F.S.
Gain Adjustment Range (Figure 1)	±0.25			±0.25			% of F.S.
Bipolar Zero Adjustment Range	±0.15			±0.15			% of F.S.
REFERENCE INPUT							
Input Impedance	15K	20K	25K	15K	20K	25K	
REFERENCE OUTPUT							
Voltage	9.90	10.00	10.10	9.90	10.00	10.10	V
Current (Available for External Loads)	1.5	2.5		1.5	2.5		mA
POWER DISSIPATION		250	375		250	375	mW

NOTES:
1. Guaranteed but not tested over the operating temperature range.
2. See settling time discussion and Figure 3.
3. The Power Supply Gain Sensitivity is tested in reference to a V_{CC}, V_{EE} of ±15V.

Definitions of Specifications

DIGITAL INPUTS

The HI-565A accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight Binary, Two's Complement*, or Offset Binary, (See Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement*
MSB...LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	½FS	Zero	-FS
111...111	+FS – 1 LSB	+FS – 1 LSB	Zero – 1 LSB
011...111	½FS – 1 LSB	Zero – 1 LSB	+FS – 1 LSB

*Invert MSB with external inverter to obtain Two's Complement Coding

ACCURACY

NONLINEARITY – Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY – For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition, settling to within 1/2 LSB of final value.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst-case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance Voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance Limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

Applying the HI-565A

OP AMP SELECTION

The HI-565A's current output may be converted to voltage using the standard connections shown in Figures 1 and 2. The choice of operational amplifier should be reviewed for each application, since a significant trade-off may be made between speed and accuracy.

For highest precision, use an HA-5130. This amplifier contributes negligible error, but requires about 11μs to settle within ±0.1% following a 10V step.

The Harris Semiconductor HA-2600 is the best all-around choice for this application, and it settles in 1.5μs (also to ±0.1% following a 10V step). Remember, settling time for the DAC-amplifier combination is $\sqrt{t_D^2 + t_A^2}$, where t_D, t_A are settling times for the DAC and amplifier.

NO-TRIM OPERATION

The HI-565A will perform as specified without calibration adjustments. To operate without calibration, substitute 50Ω resistors for the 100Ω trimming potentiometers: In Figure 1 replace R2 with 50Ω ; also remove the network on pin 8 and connect 50Ω to ground. For bipolar operation in Figure 2, replace R3 and R4 with 50Ω resistors.

Applying the HI-565A, (Continued)

Table 1 – Operating Modes and Calibration

MODE	CIRCUIT CONNECTIONS: OUTPUT RANGE	PIN10 TO	PIN 11 TO	RESISTOR (R)	CALIBRATION: APPLY INPUT CODE	ADJUST	TO SET V_O
Unipolar (See Fig. 1)	0 to +10V	V_O	Pin 10	1.43K	All 0's All 1's	R1 R2	0V +9.99756V
	0 to +5V	V_O	Pin 9	1.1K	All 0's All 1's	R1 R2	0V +4.99878V
Bipolar (See Fig. 2)	±10V	NC	V_O	1.69K	All 0's All 1's	R3 R4	-10V +9.99512V
	±5V	V_O	Pin 10	1.43K	All 0's All 1's	R3 R4	-5V +4.99756V
	±2.5V	V_O	Pin 9	1.1K	All 0's All 1's	R3 R4	-2.5V +2.49878V

With these changes, performance is guaranteed as shown under Specifications, "External Adjustments". Typical unipolar zero will be ±1/2 LSB plus the op amp offset.

The feedback capacitor C must be selected to minimize settling time.

CALIBRATION

Calibration provides the maximum accuracy from a converter by adjusting its gain and offset errors to zero. For the HI-565A, these adjustments are similar whether the current output is used, or whether an external op amp is added to convert this current to a voltage. Refer to Table 1 for the voltage output case, along with Figure 1 or 2.

Calibration is a two step process for each of the five output ranges shown in Table 1. First adjust the negative full scale (zero for unipolar ranges). This is an offset adjust which translates the output characteristic, i.e. affects each code by the same amount.

Next adjust positive FS. This is a gain error adjustment, which rotates the output characteristic about the negative FS value.

For the bipolar ranges, this approach leaves an error at the zero code, whose maximum value is the same as for integral nonlinearity error. In general, only two values of output may be calibrated exactly; all others must tolerate some error. Choosing the extreme end points (plus and minus full scale) minimizes this distributed error for all other codes.

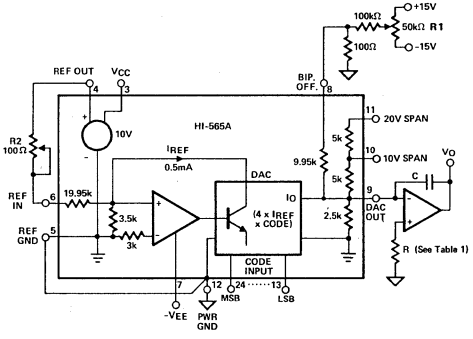


FIGURE 1. UNIPOLAR VOLTAGE OUTPUT

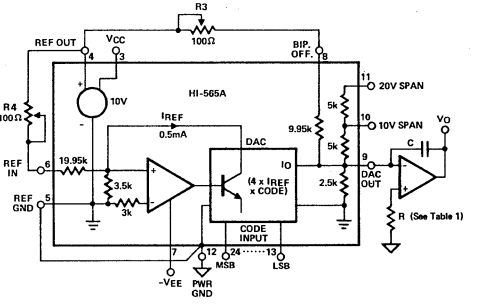


FIGURE 2. BIPOLAR VOLTAGE OUTPUT

Settling Time

This is a challenging measurement, in which the result depends on the method chosen, the precision and quality of test equipment and the operating configuration of the DAC (test conditions). As a result, the different techniques in use by converter manufacturers can lead to consistently different results. An engineer should understand the advantage and limitations of a given test method before using the specified settling time as a basis for design.

The approach used for several years at Harris Analog Products Division calls for a strobed comparator to sense final perturbations of the DAC output waveform. This gives the LSB a reasonable magnitude (814μV for the HI-565A), which provides the comparator with enough overdrive to establish an accurate ±1/2 LSB window about the final settled value. Also, the required test conditions simulate the DAC's environment for a common application – use in a successive approximation A/D converter. Considerable experience has shown this to be a reliable and repeatable way to measure settling time.

The usual specification is based on a 10V step, produced by simultaneously switching all bits from off-to-on (t_{ON}) or on-to-off (t_{OFF}). The slower of the two cases is specified, as measured from 50% of the digital input transition to the final entry within a window of ±1/2 LSB about the settled value. Four measurements characterize a given type of DAC:

(a) t_{ON}, to final value +1/2 LSB
(b) t_{ON}, to final value -1/2 LSB
(c) t_{OFF}, to final value +1/2 LSB
(d) t_{OFF}, to final value -1/2 LSB

(Cases (b) and (c) may be eliminated unless the overshoot exceeds 1/2 LSB). For example, refer to Figure 3 for the measurement of case (d).

PROCEDURE

As shown in Figure 3B, settling time equals t_X plus the comparator delay (t_D = 15ns). To measure t_X,

- Adjust the delay on generator # 2 for a t_X of several microseconds. This assures that the DAC output has settled to its final value.
- Switch on the LSB (+5V).
- Adjust the V_{LSB} supply for 50 percent triggering at COMPARATOR OUT. This is indicated by traces of equal brightness on the oscilloscope display as shown in Figure 3B. Note DVM reading.
- Switch the LSB to Pulse (P).
- Readjust the V_{LSB} supply for 50% triggering as before, and note DVM reading. One LSB equals one tenth the difference in the DVM readings noted above.
- Adjust the V_{LSB} supply to reduce the DVM reading by 5 LSB's (DVM reads 10X, so this sets the comparator to sense the final settled value minus 1/2 LSB). Comparator output disappears.
- Reduce generator # 2 delay until comparator output reappears, and adjust for "equal brightness".
- Measure t_X from scope as shown in Figure 3B. Settling time equals $t_X + t_D$, i.e. t_X +15ns.

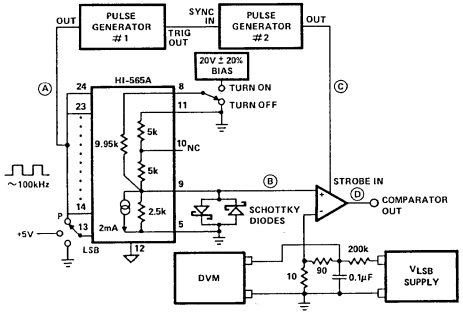


FIGURE 3A.

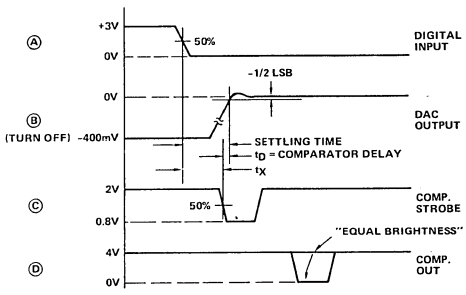


FIGURE 3B.

Other Considerations

GROUNDS

The HI-565A has two ground terminals, pin 5 (REF GND) and pin 12 (PWR GND). These should not be tied together near the package unless that point is also the system signal ground to which all returns are connected. (If such a point exists, then separate paths are required to pins 5 and 12).

The current through pin 5 is near-zero DC*; but pin 12 carries up to 1.75mA of code – dependent current from bits 1, 2, and 3. The general rule is to connect pin 5 directly to the system "quiet" point, usually called signal or analog ground. Connect pin 12 to the local digital or power ground. Then, of course, a single path must connect the analog/signal and digital/power grounds.

LAYOUT

Connections to pin 9 (I_{OUT}) on the HI-565A are most critical for high speed performance. Output capacitance of the DAC is only 20pF, so a small change or additional capacitance may alter the op amp's stability and affect settling time. Connections to pin 9 should be short and few. Component leads should be short on the side connecting to pin 9 (as for feedback capacitor C). See the Settling Time section.

BYPASS CAPACITORS

Power supply bypass capacitors on the op amp will serve the HI-565A also. If no op amp is used, a 0.01μF ceramic capacitor from each supply terminal to pin 12 is sufficient, since supply current variations are small.

*Current cancellation is a two-step process within the HI-565A in which code-dependent variations are eliminated, then the resulting DC current is supplied internally. First an auxiliary 9 bit R-2R ladder is driven by the complement of the DAC's input code. Together, the main and auxiliary ladders draw a continuous 2.25mA from the internal ground node, regardless of input code. Part of this DC current is supplied by the zener voltage reference, and the remainder is sourced from the positive supply via a current mirror which is laser trimmed for zero current through the external terminal (pin 5).

Die Characteristics

Transistor Count	200
Die Size	179 x 107 mils
Thermal Constants; θ_{ja}	51°C/W
θ_{jc}	16°C/W
Tie Substrate to:	Ref. Ground
Process:	Bipolar - DI

HARRIS

HI-DAC16B/ DAC16C

16-Bit D to A Converter

Features

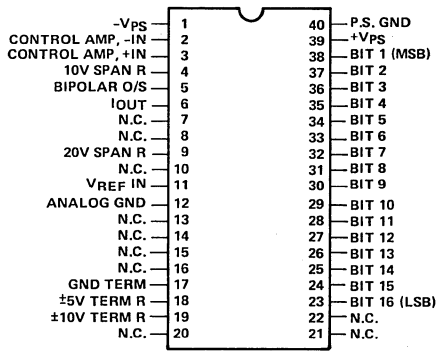
- 16 BIT RESOLUTION
- MONOLITHIC DI BIPOLAR CONSTRUCTION
- FAST SETTLING TIME — 1 μs TO .003%FS
- LOW DIFF. NONLIN. DRIFT — ± 0.3ppm/°C
- LOW GAIN DRIFT — ± 1ppm/°C
- ON-CHIP SPAN & OFFSET RESISTORS
- TTL/5V-CMOS COMPATIBLE
- LOW UNIPOLAR OFFSET — ≤ 1/2LSB@ +25°C
- LOW UNIPOLAR OFFSET T.C. — ± 0.2ppm/°C
- EXCELLENT STABILITY

Applications

- HIGH RESOLUTION CONTROL SYSTEMS
- HIGH FIDELITY AUDIO RECONSTRUCTION
- PRECISION FUNCTION GENERATION AND INSTRUMENTATION

Pinout

TOP VIEW



Description

The HARRIS HI-DAC16 is a 16-bit, current output D/A converter. Single chip construction includes thin-film application resistors for use with an external op amp. These permit standard output voltage ranges of 0 to +5V, 0 to +10V, ±2.5V, ±5V and ±10V. The HI-DAC16B is monotonic to 15 bits; and the HI-DAC16C to 14 bits.

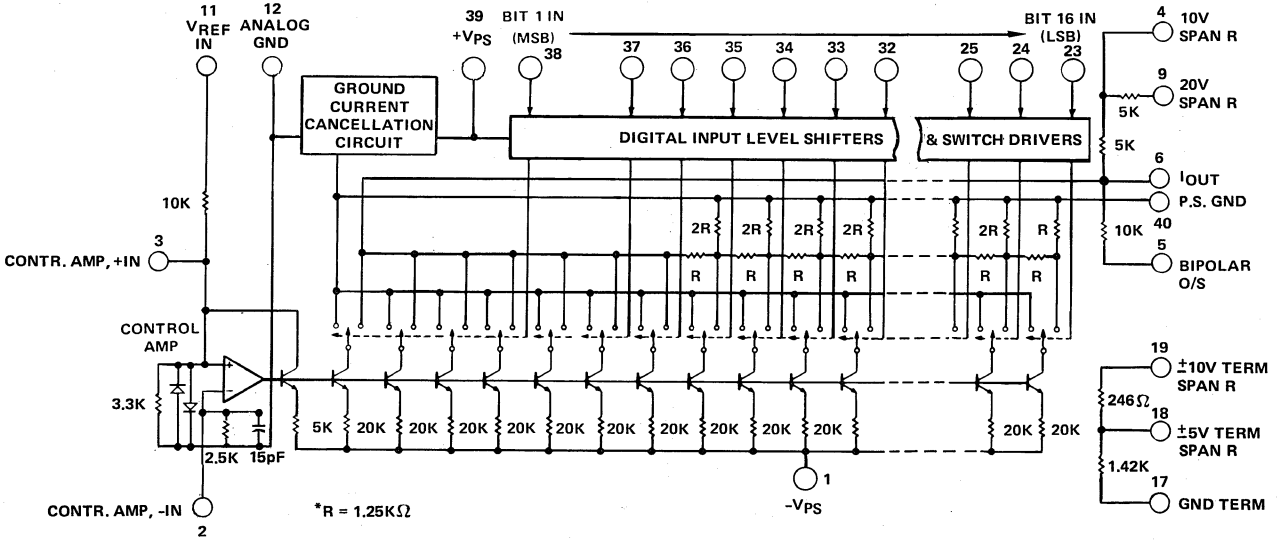
Reference and span resistors have adjacent placement on the chip for optimum match and thermal tracking. Futhermore, this layout feature helps minimize the superposition error caused by self-heating of the span resistor, reducing it to less than 1/10LSB. This and other design innovations have produced exceptionally stable operation over temperature. Typical temperature coefficients are ± 1ppm/°C for gain error and 0.3ppm/°C for differential non-linearity error.

The internal architecture is an extension of the earlier HI-562 with several major improvements. All code dependent ground currents are steered to a separate non-critical path, namely, power supply ground. This feature allows the precision ground of the converter to be sensed with virtually zero voltage drop referred to system ground. The result is the complete elimination of non-linearities due to code dependent ground currents while yielding an extremely low unipolar offset of less than 1/2LSB. Because of this separation, the user may route the precision ground some distance to the system ground without degrading converter accuracy.

The HARRIS HI-DAC16 delivers a stable, accurate output without sacrifice in speed. Settling time to within ±0.003% is one microsecond. Overall performance of this monolithic device should be attractive for applications such as high fidelity audio and high-resolution control systems.

Two accuracy grades are offered, and typical power dissipation is 465mW. Package is a 40 pin ceramic DIP. For further information, see Application Note 539.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.


11
VREF IN
12
ANALOG GND
39
+VPS
BIT 1 IN (MSB)
38
37
36
35
34
33
32
25
24
BIT 16 IN (LSB)
23
4
10V SPAN R
9
20V SPAN R
5K
5K
6
IOUT
P.S. GND
40
5
BIPOLAR O/S
GROUND CURRENT CANCELLATION CIRCUIT
DIGITAL INPUT LEVEL SHIFTERS
& SWITCH DRIVERS
10K
3
CONTR. AMP, +IN
CONTROL AMP
3.3K
2.5K
15pF
CONTR. AMP, -IN
2
*R = 1.25KΩ
2R
R
10K
5K
20K
1
-VPS
19
±10V TERM SPAN R
246Ω
18
±5V TERM SPAN R
1.42K
17
GND TERM

Specifications HI-DAC16B/DAC16C

Absolute Maximum Ratings (Referred to Ground)

Power Supply Inputs	$V_{ps}+$	+20V	Junction Temperature	175°C
	$V_{ps}-$	−20V	Operating Temperature Range	
Reference Inputs	V_{REF} (Hi)	$\pm V_{ps}$		
Digital Inputs	Bits 1 to 16	−1V, +12V	HI-DAC 16B/C	0°C to +75°C
Outputs		$\pm V_{ps}$	Storage Temperature Range	−65°C to +150°C

Electrical Specifications (T_A = +25°C, V_{ps} = ±15V, V_{ref} = +10V, unless otherwise specified)

PARAMETER	CONDITIONS	HI-DAC16B MIN	HI-DAC16B TYP	HI-DAC16B MAX	HI-DAC16C MIN	HI-DAC16C TYP	HI-DAC16C MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs	Bit ON "Logic 1" Bit OFF "Logic 0"							
Input Voltage								
Logic "1"	Full Temperature Range	2.0			2.0			V
Logic "0"				0.8			0.8	V
Input Current								
Logic "1"			20	500		20	500	nA
Logic "0"		-50			-50			µA
Reference Input								
Input Resistance			10			10		kΩ
Input Voltage			10			10		V
TRANSFER CHARACTERISTICS								
Resolution	Full Temperature Range		16			16		Bits
Nonlinearity	25°C		±0.0023			±0.0045		%FSR(3)
	Full Temperature Range			±0.0045			±0.009	
Differential Nonlinearity	25°C		±0.0015			±0.003		%FSR
	Full Temperature Range			±0.003			±0.006	
Relative Accuracy (5)	With 100Ω(1%) Trim Resistors							
Unipolar Gain Error	All Bits ON		±0.1	±0.25		±0.1	±0.25	
Bipolar Offset Error	All Bits OFF		±0.15	±0.43		±0.15	±0.43	%FSR
Unipolar Offset Error			±0.002	±0.05		±0.002	±0.05	
Adjustment Range	See Operating Instructions							
Gain	Using Trim Potentiometers			±3			±3	%FSR
Bipolar Offset	as shown in Figure 1			±0.43			±0.43	
Temperature Stability	Drift specified with internal span resistors for voltage output							
Gain Drift (2)	Full Temperature Range		±1	±5		±1	±5	ppm of FSR/°C
Offset Drift (2)								
Unipolar Offset	All Bits OFF		±0.2			±0.2		
Bipolar Offset			±0.5			±0.5		
Differential Nonlinearity	Full Temperature Range		±0.3			±0.3		
Settling Time (2) to ±0.003%FS	All Bits ON-to-OFF or OFF-to-ON		1.0			1.0		µs

Specifications HI-DAC16B/DAC16C

PARAMETER	CONDITIONS	HI-DAC16B			HI-DAC16C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Glitch (2)	From 0111 . . .1 to 100 . . . 0 or 100 . . . 0 to 011 . . . 1		1300			1300		mV–ns
Power Supply (2) Rejection Ratio, PSRR (3) V_{ps}+ V_{ps}-			1.5 1.5			1.5 1.5		ppm of FSR/% V_{ps}
OUTPUT CHARACTERISTICS								
Output Current Unipolar Bipolar		-1.6 ±0.8	-2 ±1	-2.4 ±1.2	-1.6 ±0.8	-2 ±1	-2.4 ±1.2	mA
Resistance			2.5k			2.5k		
Capacitance			10			10		pF
Output Voltage Ranges Unipolar Bipolar	Using external op amp and internal scaling resistors. See Figure 1 and Table 1 for connections		0 to +5 0 to +10 ±2.5 ±5 ±10			0 to +5 0 to +10 ±2.5 ±5 ±10		V
Compliance Limit (2)		-3		+10	-3		+10	V
Compliance Voltage (2)	Full Temperature Range		±1			±1		V
Output Noise	0.1 to 5MHz (All bits ON)		30			30		μVRMS
POWER REQUIREMENTS								
V_{ps}+ (7) V_{ps}-	Full Temperature Range	13.5 -13.5	+15 -15	16.5 -16.5	13.5 -13.5	+15 -15	16.5 -16.5	V
I_{ps}+ (4) I_{ps}- (4)	All Bits ON or OFF Full Temperature Range	-25	+13 -18	+18	-25	+13 -18	+18	mA
Power Dissipation			465			465		mW

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impared. Functional operation under any of these conditions is not necessarily implied.
2. See Definitions.
3. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc., or 2mA (±20%) for current output.
4. After 30 seconds warm-up.
5. Using an external op amp with internal span resistors and specified external trim resistors in place of potentiometers R_1 and R_2. Errors are adjustable to zero using R_1 and R_2 potentiometers. (See Operating Instructions Figure 2.)

Definition of Specifications

DIGITAL INPUTS

The HI-DAC 16B/C accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight Binary, Two's Complement, or Offset Binary. (See Operation Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement *
MSB LSB			
000...000	Zero	-FS 9(Full Scale)	Zero
100...000	½FS	Zero	−FS
111...111	+FS − 1 LSB	+FS − 1 LSB	Zero − 1 LSB
011...111	½FS − 1 LSB	Zero − 1 LSB	+FS − 1 LSB

*Invert MSB with external inverter to obtain Two's Complement Coding

ACCURACY

INTEGRAL NONLINEARITY – The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to "end-point linearity" for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL NONLINEARITY – The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY – The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H −25°C) and low ranges (+25°C−T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H −25°C) and low (+25°C −T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in −15V, or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance Voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance Limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON–OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Calculated as the product of duration and amplitude.)

Operating Instructions

UNIPOLAR AND BIPOLAR VOLTAGE OUTPUT CONNECTIONS

FIGURE 1

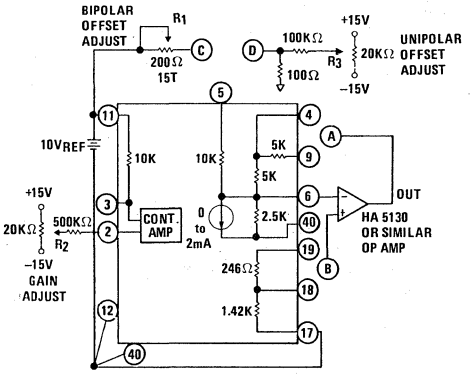


TABLE 1

	OUTPUT RANGE	CONNECTIONS			
		PIN5 to	PIN4 to	PIN9 to	PIN B to
UNIPOLAR MODE	0 to +10V	D	A	N.C.	19
	0 to +5V	D	A	PIN6	*
BIPOLAR MODE	±10V	C	N.C.	A	19
	±5V	C	A	N.C.	18
	±2.5V	C	A	6	*

*Connect an external 1.1K ohm resistor to ground.

GAIN AND ZERO CALIBRATION

The HI-DAC16B/C input reference resistor, bipolar offset resistor and span resistors are optimized for excellent tracking over temperature. LASER trimming of the reference circuit resistors corrects the unipolar Gain and Offset errors to high accuracy. The remaining error can be adjusted with trimming potentiometers. The bipolar Gain and Offset errors are greater since the LASER correction is done in the unipolar mode, however these too are easily adjusted. Figure 1 illustrates the connections for unipolar and bipolar operation. Trimming potentiometers R_1, R_2, and R_3 are required for adjustment.

UNIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (00..0)
- Adjust R_3 for zero volts output

Step 2: Gain
- Turn all bits ON (11..1)
- Adjust R_2 for an output of FS-1LSB

That is, adjust for:

9.999847 for +10V range
4.999924 for +5V range

BIPOLAR CALIBRATION

Step 1: Offset
Turn all bits OFF (00..0)
Adjust R_1 for an output of
−10V for ± 10V range
−5V for ± 5V range
−2.5V for ± 2.5V range

Step 2: Gain
Turn all bits ON (11..1)
Adjust R_2 for FS-1LSB output
That is, adjust for:

9.999695 for ±10V range
4.999847 for ± 5V range
2.499924 for ± 2.5V range

Other Considerations

GROUNDS

The HI-DAC16 has two ground terminals, pin 12 (REF GND) and pin 40 (PWR GND). These should not be tied together near the package unless that point is also the system signal ground to which all returns are connected. (If such a point exists, then separate paths are required to pins 12 and 40).

The current through pin 12 is near-zero DC*, but pin 40 carries up to 1.75mA of code - dependent current from bits 1, 2, and 3. The general rule is to connect pin 12 directly to the system signal, or analog ground. Connect pin 40 to the local digital or power ground. Then, of course, a single path must connect the analog/signal and digital/power grounds.

Other Considerations (Continued)

*Current cancellation is a two-step process in which code-dependent variations are eliminated, then the resulting DC current is supplied internally. First, an auxiliary 13-bit R-2R Ladder is driven by the complement of the DAC's input code. Together the main and auxiliary ladders draw a continuous 3.25mA from the internal ground node, regardless of input code. Part of this DC current is supplied by the zener voltage reference, and the remainder is sourced from the positive supply via a current mirror which is laser trimmed for zero current through the external terminal (pin 12).

LAYOUT

Connections to pin 6 (I_{OUT}) on the HI–DAC16 are most critical for high speed performance. Output capacitance of the DAC is only 10pF, so a small additional capacitance will alter the op amp's stability and affect settling time. Connections to pin 6 should be short and few. Component leads should be short on the side connecting to pin 6.

BYPASS CAPACITORS

Power supply bypass capacitors on the op amp will serve the HI–DAC16 also. If no op amp is used, a 0.01μF ceramic capacitor from each supply terminal to pin 40 is sufficient, since supply current variations are small.

THERMAL EFFECTS

A consideration when using the DAC16 is Temperature Stability. In applications where full scale shift could be a problem, the use of a heat sink and/or a cooling fan is suggested. This will decrease the magnitude of the total variation by lowering the effective thermal resistance between the package and its environment. The device should be kept in a stable isothermal environment, and a warm-up time consistent with accuracy requirements should be provided.

SELECTING AN OPERATIONAL AMPLIFIER

The HI-DAC16 is a high resolution, high accuracy DAC. Many applications will require an op-amp used as a current-to-voltage converter at the DAC output. (Careful consideration should be given the choice of this amplifier as a poor selection can seriously degrade the inherent qualities of the DAC.)

The HA-5130 is an excellent choice to maintain high accuracy with an average Offset Drift of only 0.4 μV/°C leading to an error over temperature of 30 μV (0.0003% FSR for a 10V FS). Initial offset and bias current are 10 μV and 3nA respectively, while input noise current of 0.2pA/ $\sqrt{\text{Hz}}$. Settling time is adequate for most audio applications. (11 μs typ. to 0.1%).

COMPOSITE AMPLIFIER

It is desirable at times to have an output amplifier which combines the qualities of those op-amps available to the designer. For instance one may wish to combine the excellent front-end characteristics of the HA-5130 with the speed of a device such as the HA-2540 (t_{settle} =250ns to 0.1%). In these instances there is the option of the composite amplifier. The basic configuration is shown in Figure 2.

COMPOSITE AMPLIFIER

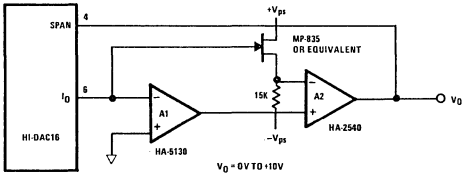


FIGURE 2

The composite amplifier may be used to achieve a compromise depending on the requirements of a design. Trade-offs in performance can be made and the following equations apply:

Offset; $$V_{OFF} = \frac{V_{OFF2}}{A_{01}} + V_{OFF1}$$

Bias; $$I_{BIAS} = I_{BIAS2} + I_{BIAS1}$$

Gain; $$\frac{V_0}{V_1} = A_V(S) = A_{V2}(S)\,[1 + A_{V1}(S)]$$

The amplifier A_2 should be of wide bandwidth and fast settling time.

Die Characteristics

Transistor Count		190
Die Size:		215 x 125 mils
Thermal Constants;	θ_{ja}	41°C/W
	θ_{jc}	11°C/W
Tie Substrate to:		Analog Ground
Process:		Bipolar - DI

HARRIS

HI-DAC80V

12Bit, Low Cost, Monolithic Digital to Analog Converter

June 1989

Features

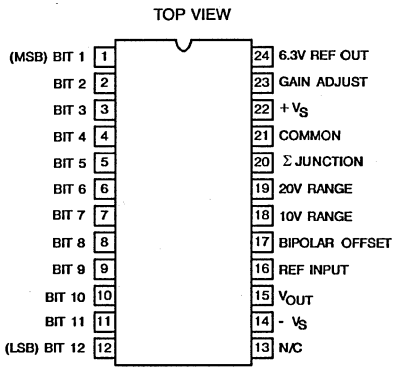
- DAC 80V Alternate Source
- Monolithic Construction
- Fast Settling
- Guaranteed Monotonic
- Wafer Laser Trimmed
- Applications Resistors On-Chip
- On-Board Reference
- Dielectric Isolation (DI) Process
- ±12V Supply Operation

Applications

- High Speed A/D Converters
- Precision Instrumentation
- CRT Display Generation

Pinout

TOP VIEW



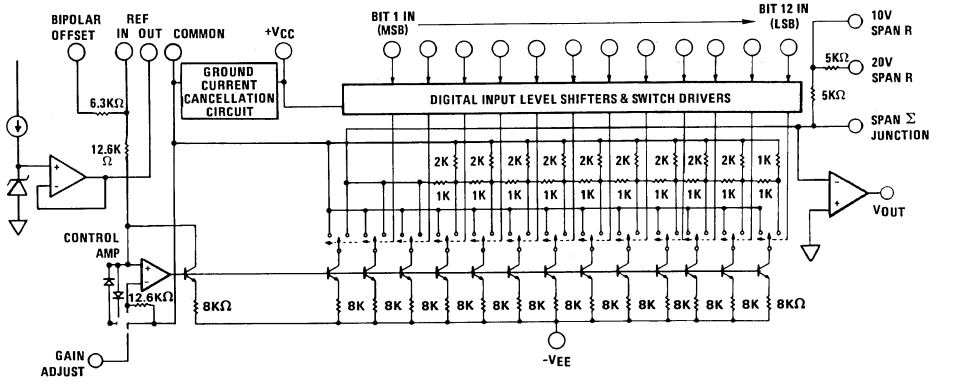
Description

The HI-DAC80V is a monolithic direct replacement for the popular DAC80 and AD DAC80. Single chip construction along with several design innovations make the HI-DAC80V the optimum choice for low cost, high reliability applications. Harris' unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching times and minimum glitch. On board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy.

Internally the HI-DAC80V eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

The HI-DAC80V is available as a voltage output device which is guaranteed over the 0°C to +75°C temperature range. It includes a buried zener reference featuring low temperature coefficient as well as an on board operational amplifier. The HI-DAC80V requires only two power supplies and will operate in the range of ± (11.4V to 16.5V).

Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Power Supply Inputs $+V_S$ ..... +20V
$-V_S$ ..... -20V
Reference: Input (Pin 16) ..... $+V_S$
Output Drain 2.5mA
Digital Inputs (Bits 1 to 12) ..... -1V to $+V_S$
Max Junction Temperature ..... +175°C
Operating Temperature Range ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications Unless Otherwise Specified, T_A = +25°C, V_S ±12V to ±15V (Note 5), Pin 16 to Pin 24.

PARAMETER	CONDITIONS	HI-DAC80V-5			UNITS
		MIN	TYP	MAX	
RESOLUTION		-	-	12	Bits
DIGITAL INPUT (Note 3)					
Logic Levels	TTL Compatible				
Logic "1"	At +1µA	+2	-	+5.5	Volts
Logic "0"	At -100µA	0	-	+0.8	Volts
ACCURACY (Note 3)					
Linearity Error	Full Temperature	-	±1/4	±1/2	LSB
Differential Linearity Error	Full Temperature	-	±1/2	±3/4	LSB
Monotonicity	Full Temperature	Guaranteed			
Gain Error (Notes 2, 4)	Full Temperature	-	±0.1	±0.3	%FSR
Offset Error (Note 2)	Full Temperature	-	±0.05	±0.15	%FSR
DRIFT (Note 3)					
Total Bipolar Drift (Includes Gain, Offset and Linearity Drifts.)	Full Temperature	-	-	±20	PPM/°C
Total Error	Full Temperature				
Unipolar (Note 6)		-	±0.08	±0.15	%FSR
Bipolar (Note 6)		-	±0.06	±0.1	%FSR
Gain	With Internal Reference	-	±15	±30	PPM/°C
	Without Internal Reference	-	±7	-	PPM/°C
Unipolar Offset		-	±1	±3	PPM/°C
Bipolar Offset		-	±5	±10	PPM/°C
CONVERSION SPEED					
Setting Time (Note 3)	Full Scale Transition all Bits				
With 10K Feedback	ON to OFF or OFF to ON	-	3	-	µs
With 5K Feedback	to ±0.01% of FSR	-	1.5	-	µs
For 1 LSB Change		-	1.5	-	µs
Slew Rate		10	15	-	V/µs

Specifications HI-DAC80V

Electrical Specifications (Continued) Unless Otherwise Specified, T_A = +25°C, V_S ±12V to ±15V (Note 5), Pin 16 to Pin 24.

PARAMETER	CONDITIONS	HI-DAC80V-5 MIN	HI-DAC80V-5 TYP	HI-DAC80V-5 MAX	UNITS
ANALOG OUTPUT					
Output Ranges		-	±2.5	-	V
		-	±5	-	V
		-	±10	-	V
		-	0 to 5	-	V
		-	0 to 10	-	V
Output current		±5	-	-	mA
Output Resistance		-	0.05	-	Ω
Short Circuit Duration	To Common		Continuous		
INTERNAL REFERENCE					
Output Voltage		6.250	+6.3	6.350	V
Output Impedence		-	1.5	-	Ω
External Current		-	-	+2.5	mA
Tempco of Drift		-	5	-	PPM/°C
POWER SUPPLY SENSITIVITY (Note 3, 5)					
+15V Supply		-	0.001	0.002	%FSR
-15V Supply		-	0.001	0.002	$\%V_S$
POWER SUPPLY REQUIREMENTS (Note 5)					
Voltage Range					
$+V_S$	Full Temperature	+11.4	+15	+16.5	V
$-V_S$	Full Temperature	-11.4	-15	-16.5	V
Current					
$+I_S$	Full Temperature V_S = ±15V	-	+12	+15	mA
$-I_S$	Full Temperature V_S = ±15V	-	-15	-20	mA

NOTES:
1. Absolute maximum ratings are limiting values applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Adjustable to zero using external potentiometers.
3. See definitions.
4. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc.
5. The HI-DAC80V will operate with supply voltages as low as ±11.4V. It is recommended that output voltage range -10V to +10V not be used if the supply voltages are less than ±12.5V.
6. With Gain and Offset errors adjusted to zero at +25°C.

Definitions of Specifications

Digital Inputs

The HI-DAC80V accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

DIGITAL INPUT	ANALOG OUTPUT		
	COMPLEMENTARY STRAIGHT BINARY	COMPLEMENTARY OFFSET BINARY	COMPLEMENTARY TWO'S COMPLEMENT*
MSB...LSB			
000...000	+Full Scale	+Full Scale	-LSB
100...000	Mid Scale-1 LSB	-1 LSB	+Full Scale
111...111	Zero	-Full Scale	Zero
011...111	+1/2 Full Scale	Zero	-Full Scale

* Invert MSB with external inverter to obtain CTC Coding.

Settling Time

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low. In a 12 bit system ±1/2 LSB = ±0.012% of FSR.

Thermal Drift

Thermal drift is based on measurements at +25°C, at high (T_H) and low (T_L) temperatures. Drift calculations are made for the high (T_H-25°C) and low (+25°C-T_L) ranges, and the larger of the two values is given as a specification representing worst case drift.

Gain Drift, Offset Drift, Reference Drift and Total Bipolar Drift are calculated in parts per million per °C as follows:

$$\text{Gain Drift} = \frac{\Delta\ \text{FSR}/\Delta^{\circ}\text{C}}{\text{FSR}} \times 10^6$$

$$\text{Offset Drift} = \frac{\Delta\ \text{Offset}/\Delta^{\circ}\text{C}}{\text{FSR}} \times 10^6$$

$$\text{Reference Drift} = \frac{\Delta\ V_{REF}/\Delta^{\circ}\text{C}}{V_{REF}} \times 10^6$$

$$\text{Total Bipolar Drift} = \frac{V_O/\Delta^{\circ}\text{C}}{\text{FSR}} \times 10^6$$

NOTE: FSR = Full Scale Output Voltage -Zero Scale Output Voltage

Δ FSR = FSR (T_H) - FSR (+25°C)
or FSR (+25°C) - FSR (T_L)
V_O = Steady-state response to any input code.

Total Bipolar Drift is the variation of output voltage with temperature, in the bipolar mode of operation. It represents the net effect of drift in Gain, Offset, Linearity and Reference Voltage. Total Bipolar Drift values are calculated, based on measurements as explained above. Gain and Offset need not be calibrated to zero at +25°C. The specified limits for TBD apply for any input code and for any power supply setting within the specified operating range.

Accuracy

LINEARITY ERROR (Short for "Integral Linearity Error." Also, sometimes called "Integral Nonlinearity" and "Nonlinearity".)- The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to end-point linearity for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL LINEARITY ERROR - The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY - The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

TOTAL ERROR - The net output error resulting from all internal effects (primarily non-ideal Gain, Offset, Linearity and Reference Voltage). Supply voltages may be set to any values within the specified operating range. Gain and offset errors must be calibrated to zero at +25°C. Then the specified limits for Total Error apply for any input code and for any temperature within the specified operating range.

Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in $-V_S$, or $+V_S$ supplies. It is specified under DC conditions and expressed as full scale range percent of change divided by power supply percent change.

$$\text{P.S.S.} = \frac{\dfrac{\Delta\ \text{Full Scale Range} \times 100}{\text{Full Scale Range (Nominal)}}}{\dfrac{\Delta\ V_S \times 100}{V_S\ \text{(Nominal)}}}$$

Glitch

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale i.e. the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the Product of duration and amplitude.)

Decoupling and Grounding

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in figure 1 should be used. Decoupling capacitors should be connected close to the HI-DAC80V (preferably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

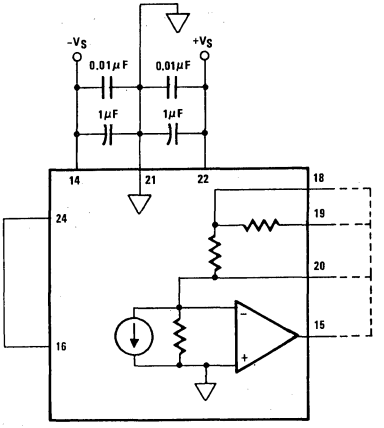


FIGURE 1.

Reference Supply

An internal 6.3 Volt reference is provided on board the HI-DAC80V. The voltage (pin 24) is accurate to ±0.8% and must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-DAC80V. All gain adjustments should be made under constant load conditions.

Output Voltage Ranges

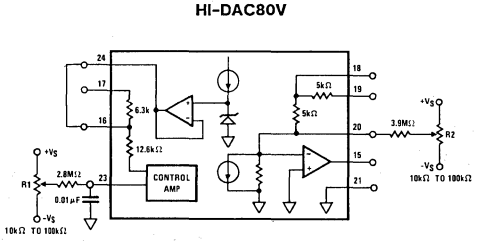


FIGURE 2.

RANGE CONNECTIONS

	RANGE	CONNECT PIN 15	CONNECT PIN 17	CONNECT PIN 19
Unipolar	0 to +5V	18	N.C.	20
	0 to +10V	18	N.C.	N.C.
Bipolar	±2.5V	18	20	20
	±5V	18	20	N.C.
	±10V	19	20	15

Gain and Offset Calibration

UNIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for zero volts out

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for FS-1LSB
- That is:
  - 4.9988 for 0 to +5V range
  - 9.9976 for 0 to +10V range

BIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for Negative FS
- That is:
  - -10V for ±10V range
  - -5V for ±5V range
  - -2.5V for ±2.5 range

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for positive FS-1LSB
- That is:
  - +9.9951V for ±10V range
  - +4.9976V for ±5V range
  - +2.4988V for ±2.5V range

This Bipolar procedure adjusts the output range end points. The maximum error at zero (half scale) will not exceed the Linearity error. See the "Accuracy" specifications.

Die Characteristics

Transistor Count 214
Die Size ..... 108 x 163 mils
Thermal Impedance;
θ_{ja} ..... 79°C/W
θ_{jc} ..... 20°C/W
Tie Substrate to: ..... Ground
Process ..... Bipolar-DI

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-DAC80V-5	0°C to +75°C	24 Pin Ceramic DIP
HI3-DAC80V-5	0°C to +75°C	24 Pin Plastic DIP

Note: The Ceramic DIP package will be discontinued in the future and is not recommended for new designs.

HARRIS

HI-DAC85V

12Bit, Low Cost, Monolithic Digital to Analog Converter

June 1989

Features

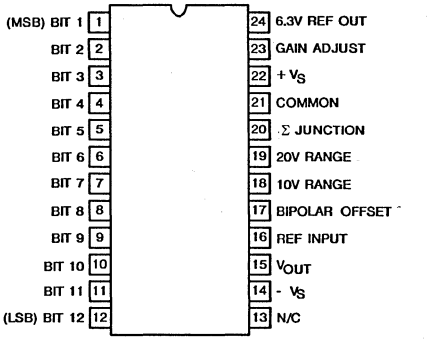
- DAC 85V Alternate Source
- Monolithic Construction
- Fast Settling
- Guaranteed Monotonic
- Wafer Laser Trimmed
- Applications Resistors On-Chip
- On-Board Reference
- Dielectric Isolation (DI) Process
- ±12V Supply Operation

Applications

- High Speed A/D Converters
- Precision Instrumentation
- CRT Display Generation

Pinout

HI1-DAC85V-4 (PLASTIC DIP)
TOP VIEW



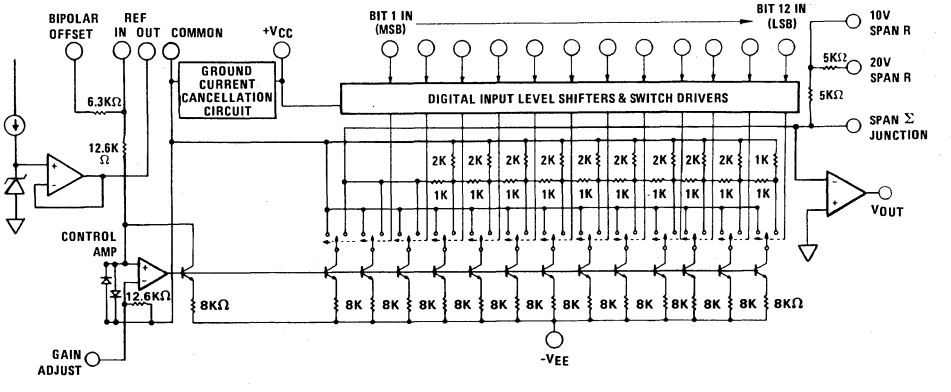
Description

The HI-DAC85V is a monolithic direct replacement for the popular DAC85 and AD DAC85 as well as the HI-5685V. Single chip construction along with several design innovations make the HI-DAC85V the optimum choice for low cost, high reliability applications. Harris' unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching times and minimum glitch. On board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy.

Internally the HI-DAC85V eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R-2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

The HI-DAC85V is available as a voltage output device which is guaranteed over the -25°C to +85°C temperature range. It includes a buried zener reference featuring low temperature coefficient as well as an on board operational amplifier. The HI-DAC85V requires only two power supplies and will operate in the range of ± (11.4V to 16.5V).

Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Power Supply Inputs $+V_S$ ..... +20V
$-V_S$ ..... -20V
Reference: Input (Pin 16) ..... $+V_S$
Output Drain 2.5mA
Digital Inputs (Bits 1 to 12) ..... -1V to $+V_S$
Max Junction Temperature ..... +175°C
Operating Temperature Range ..... -25°C to +85°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications

Unless Otherwise Specified, T_A = +25°C, V_S ±12V to ±15V (Note 5), Pin 16 to Pin 24.

PARAMETER	CONDITIONS	HI-DAC85V-4 MIN	HI-DAC85V-4 TYP	HI-DAC85V-4 MAX	UNITS
RESOLUTION		-	-	12	Bits
DIGITAL INPUT (Note 3)					
Logic Levels	TTL Compatible.				
Logic "1"	At +1µA	+2	-	+5.5	Volts
Logic "0"	At -100µA	0	-	+0.8	Volts
ACCURACY (Note 3)					
Integral Linearity Error	At +25°C	-	-	±1/2	LSB
	Full Temperature	-	±1/4	±1/2	LSB
Differential Linearity Error	Full Temperature	-	±1/4	±1/2	LSB
Monotonicity	Full Temperature	Guaranteed			
Gain Error (Notes 2, 4)	Full Temperature: Ceramic DIP	-	±0.1	±0.15	%FSR
	Plastic DIP	-	±0.1	±0.2	%FSR
Offset Error (Note 2)	Full Temperature	-	±0.05	±0.1	%FSR
DRIFT (Note 3)					
Gain		-	-	±20	PPM/°C
Unipolar Offset		-	±1	±3	PPM/°C
Bipolar Offset		-	±5	±10	PPM/°C
CONVERSION SPEED					
Setting Time (Note 3)	to ±0.01% of FSR				
With 10K Feedback	Full Scale Transition all Bits	-	3	-	µs
With 5K Feedback	ON to OFF or OFF to ON	-	1.5	-	µs
For 1 LSB Change		-	1.5	-	µs
Slew Rate		10	15	-	V/µs

Specifications HI-DAC85V

Electrical Specifications (Continued) Unless Otherwise Specified, T_A = +25°C, V_S ±12V to ±15V (Note 5), Pin 16 to Pin 24.

PARAMETER	CONDITIONS	HI-DAC85V-4 MIN	HI-DAC85V-4 TYP	HI-DAC85V-4 MAX	UNITS
ANALOG OUTPUT					
Output Ranges		-	±2.5	-	V
		-	±5	-	V
		-	±10	-	V
		-	0 to 5	-	V
		-	0 to 10	-	V
Output current		±5	-	-	mA
Output Resistance		-	0.05	-	Ω
Short Circuit Duration	To Common		Continuous		
INTERNAL REFERENCE					
Output Voltage		6.250	+6.3	6.350	V
Output Impedence		-	1.5	-	Ω
External Current		-	-	+2.5	mA
Tempco of Drift		-	5	-	PPM/°C
POWER SUPPLY SENSITIVITY (Note 3, 5)					
+15V Supply		-	0.001	0.002	%FSR
-15V Supply		-	0.001	0.002	$\%V_S$
POWER SUPPLY REQUIREMENTS (Note 5)					
Voltage Range					
$+V_S$	Full Temperature	+11.4	+15	+16.5	V
$-V_S$	Full Temperature	-11.4	-15	-16.5	V
Current					
$+I_S$	Full Temperature $V_S = \pm 15V$	-	+12	+15	mA
$-I_S$	Full Temperature $V_S = \pm 15V$	-	-15	-20	mA

NOTES:
1. Absolute maximum ratings are limiting values applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Adjustable to zero using external potentiometers.
3. See definitions.
4. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc.
5. The HI-DAC85V will operate with supply voltages as low as ±11.4V. It is recommended that output voltage range -10V to +10V not be used if the supply voltages are less than ±12.5V.
6. With Gain and Offset errors adjusted to zero at +25°C.

Definitions of Specifications

Digital Inputs

The HI-DAC85V accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

DIGITAL INPUT	ANALOG OUTPUT		
	COMPLEMENTARY STRAIGHT BINARY	COMPLEMENTARY OFFSET BINARY	COMPLEMENTARY TWO'S COMPLEMENT*
MSB...LSB			
000...000	+Full Scale	+Full Scale	-LSB
100...000	Mid Scale-1 LSB	-1 LSB	+Full Scale
111...111	Zero	-Full Scale	Zero
011...111	+1/2 Full Scale	Zero	-Full Scale

* Invert MSB with external inverter to obtain CTC Coding.

Settling Time

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of ±1/2 LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low. In a 12 bit system ±1/2 LSB = ±0.012% of FSR.

Thermal Drift

Thermal drift is based on measurements at +25°C, at high (T_H) and low (T_L) temperatures. Drift calculations are made for the high (T_H-25°C) and low (+25°C-T_L) ranges, and the larger of the two values is given as a specification representing worst case drift.

Gain Drift, Offset Drift, Reference Drift and Total Bipolar Drift are calculated in parts per million per °C as follows:

$$\text{Gain Drift} = \frac{\Delta\ \text{FSR}/\Delta^\circ\text{C}}{\text{FSR}} \times 10^6$$

$$\text{Offset Drift} = \frac{\Delta\ \text{Offset}/\Delta^\circ\text{C}}{\text{FSR}} \times 10^6$$

$$\text{Reference Drift} = \frac{\Delta\ V_{REF}/\Delta^\circ\text{C}}{V_{REF}} \times 10^6$$

$$\text{Total Bipolar Drift} = \frac{V_O/\Delta^\circ\text{C}}{\text{FSR}} \times 10^6$$

NOTE: FSR = Full Scale Output Voltage -Zero Scale Output Voltage

Δ FSR = FSR (T_H) - FSR (+25°C)
or FSR (+25°C) - FSR (T_L)
V_O = Steady-state response to any input code.

Total Bipolar Drift is the variation of output voltage with temperature, in the bipolar mode of operation. It represents the net effect of drift in Gain, Offset, Linearity and Reference Voltage. Total Bipolar Drift values are calculated, based on measurements as explained above. Gain and Offset need not be calibrated to zero at +25°C. The specified limits for TBD apply for any input code and for any power supply setting within the specified operating range.

Accuracy

LINEARITY ERROR (Short for "Integral Linearity Error." Also, sometimes called "Integral Nonlinearity" and "Nonlinearity".)- The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to end-point linearity for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

DIFFERENTIAL LINEARITY ERROR - The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

MONOTONICITY - The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for increasing code, or decrease for decreasing code.

TOTAL ERROR - The net output error resulting from all internal effects (primarily non-ideal Gain, Offset, Linearity and Reference Voltage). Supply voltages may be set to any values within the specified operating range. Gain and offset errors must be calibrated to zero at +25°C. Then the specified limits for Total Error apply for any input code and for any temperature within the specified operating range.

Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in $-V_S$, or $+V_S$ supplies. It is specified under DC conditions and expressed as full scale range percent of change divided by power supply percent change.

$$\text{P.S.S.} = \frac{\dfrac{\Delta\ \text{Full Scale Range} \times 100}{\text{Full Scale Range (Nominal)}}}{\dfrac{\Delta\ V_S \times 100}{V_S\ \text{(Nominal)}}}$$

Glitch

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale i.e. the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the Product of duration and amplitude.)

Decoupling and Grounding

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in figure 1 should be used. Decoupling capacitors should be connected close to the HI-DAC85V (preferably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

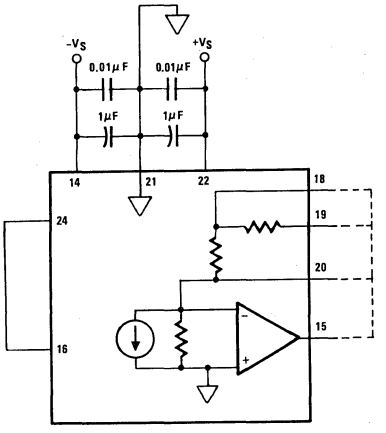


FIGURE 1.

Reference Supply

An internal 6.3 Volt reference is provided on board the HI-DAC85V. The voltage (pin 24) is accurate to ±0.8% and must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-DAC85V. All gain adjustments should be made under constant load conditions.

Output Voltage Ranges

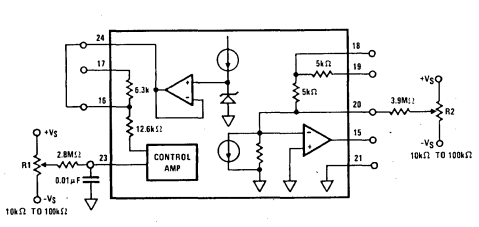


FIGURE 2.

RANGE CONNECTIONS

	RANGE	CONNECT PIN 15	CONNECT PIN 17	CONNECT PIN 19
Unipolar	0 to +5V	18	N.C.	20
	0 to +10V	18	N.C.	N.C.
Bipolar	±2.5V	18	20	20
	±5V	18	20	N.C.
	±10V	19	20	15

Gain and Offset Calibration

UNIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for zero volts out

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for FS-1LSB
- That is:
  - 4.9988 for 0 to +5V range
  - 9.9976 for 0 to +10V range

BIPOLAR CALIBRATION

Step 1: Offset
- Turn all bits OFF (11...1)
- Adjust R_2 for Negative FS
- That is:
  - -10V for ±10V range
  - -5V for ±5V range
  - -2.5V for ±2.5 range

Step 2: Gain
- Turn all bits ON (00...0)
- Adjust R_1 for positive FS-1LSB
- That is:
  - +9.9951V for ±10V range
  - +4.9976V for ±5V range
  - +2.4988V for ±2.5V range

This Bipolar procedure adjusts the output range end points. The maximum error at zero (half scale) will not exceed the Linearity error. See the "Accuracy" specifications.

Die Characteristics

Transistor Count 214
Die Size ..... 108 x 163 mils
Thermal Impedance;
θ_{ja} ..... 79°C/W
θ_{jc} ..... 20°C/W
Tie Substrate to: ..... Ground
Process ..... Bipolar-DI

Ordering Information

Part Number	Temperature Range	Package
HI1-DAC85V-4	-25°C to +85°C	24-Pin Plastic DIP
HI3-DAC85V-4	-25°C to +85°C	24-Pin Plastic DIP
HI3-DAC85V-9	-40°C to +85°C	24-Pin Plastic DIP

NOTES: The HI-DAC85V are now available in plastic DIP packages. The ceramic DIP package will be discontinued in the future and is not recommended for new designs. Below is the ordering information for plastic packages.

HARRIS SEMICONDUCTOR

ICL7121
16-Bit Multiplying Microprocessor-Compatible D/A Converter

GENERAL DESCRIPTION

The ICL7121 achieves 0.003% linearity without laser trimming by combining a four quadrant multiplying DAC using thin film resistors with an on-chip PROM-controlled correction circuit. Silicon-gate CMOS circuitry keeps the power dissipation very low.

Microprocessor bus interfacing is eased using standard memory $\overline{WR}$ite cycle timing and control. The input buffer register is loaded with the 16-bit input and directly controls the output switches. The register is transparent if $\overline{WR}$ and $\overline{CS}$ are held low.

The ICL7121 is designed and programmed for bipolar operation. There is an offset resistor to the output which should be connected to $-V_{REF}$ and an inverter on the MSB line, giving the DAC a 2's complement bipolar transfer function. Two extra resistors are included on the chip to facilitate the reference inversion, so that only an external op amp is needed.

FEATURES

- **16-Bit Resolution**
- **Low Integral Linearity Error—0.003% FSR**
- **Monotonic to 16 Bits Over Full Military Temperature Range (LM Grade)**
- **Microprocessor Compatible with Buffered Inputs**
- **Bipolar Application Requires No External Resistors**
- **Output Current Settling Time 3 μs Max (1 μs Typ)**
- **Low Linearity and Gain Temperature Coefficients**
- **Low Power Dissipation (25 mW)**
- **Full Four-Quadrant Multiplication**
- **Low Differential Nonlinearity Error at Bipolar Zero**

ORDERING INFORMATION

Part Number	Temperature Range	Package	Monotonicity
ICL7121JCJI	0°C to +70°C	28-Pin CERDIP	14 Bits
ICL7121JMJI	−55°C to +125°C	28-Pin CERDIP	
ICL7121KCJI	0°C to +70°C	28-Pin CERDIP	15 Bits
ICL7121KMJI	−55°C to +125°C	28-Pin CERDIP	
ICL7121LCJI	0°C to +70°C	28-Pin CERDIP	16 Bits
ICL7121LMJI	−55°C to +125°C	28-Pin CERDIP	

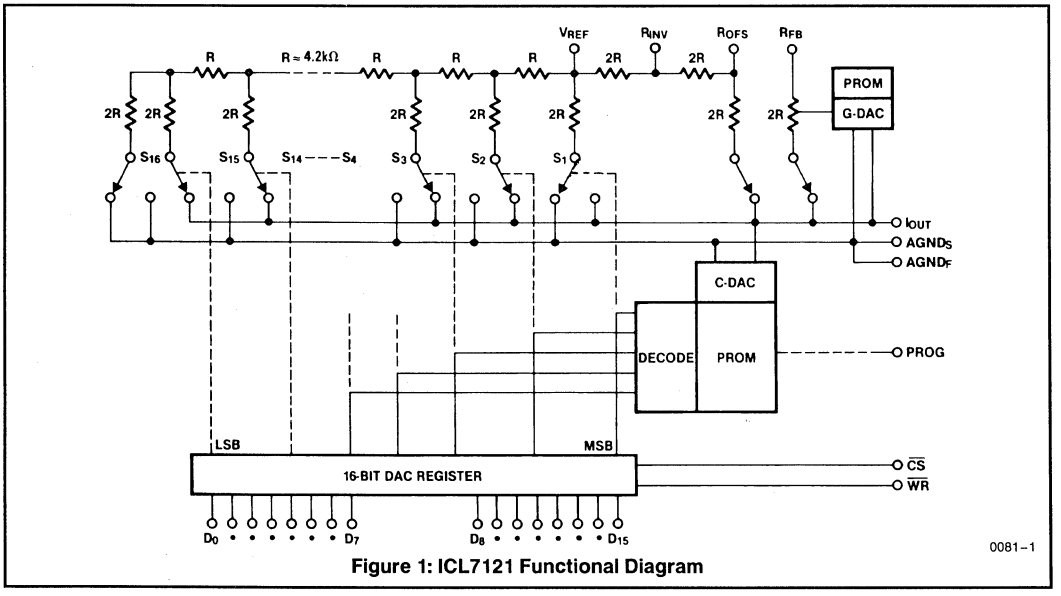


Figure 1: ICL7121 Functional Diagram

301660-005

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage V^+ to DGND ..... −0.3V to 7.5V
V_{REF}, R_{OFS}, R_{INV}, R_{FB} to DGND ..... ±25V
Current in $AGND_F$, $AGND_S$ ..... 25 mA
D_N, $\overline{WR}$, $\overline{CS}$, PROG, I_{OUT},
$AGND_F$, $AGND_S$ ..... −0.3V to (V^+ + 0.3V)
Operating Temperature
ICL7121C ..... 0°C to +70°C
ICL7121M ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Power Dissipation (Note 2) ..... 500 mW
derate above 70°C @ 10 mW/°C
Lead Temperature (soldering, 10 sec) ..... 300°C

NOTE 1: All voltages with respect to DGND.
2: Assumes all leads soldered or welded to printed circuit board.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

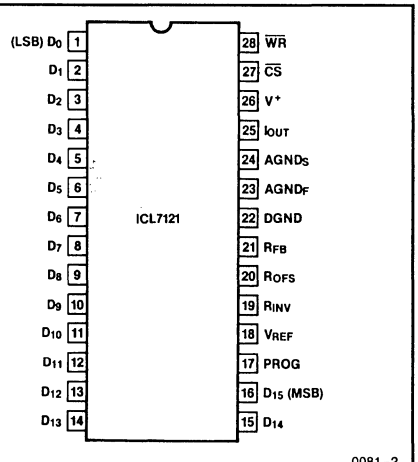


Figure 2: Pin Configuration (Outline Dwg. JI)

ELECTRICAL CHARACTERISTICS

V^+ = +5V, V_{REF} = +5V, T_A = +25°C, AGND = DGND, I_{OUT} at ground potential, unless otherwise specified

Parameter	Test Conditions/Comments		Limits Min	Limits Typ	Limits Max	Units
DC ACCURACY						
Resolution			16			Bits
Monotonicity	Guaranteed by DLE Test (Note 3)	J	14			Bits
		K	15			
		L	16			
Differential Linearity Error at Bipolar Zero	T_A = +25°C	J, K			±1	LSB
		L			±½	
	Operating Temperature Range	J, K			±1½	
		L			±1	
Differential Linearity Error DLE	T_A = +25°C	J			±0.006	%FSR
		K			±0.003	
		L			+0.003 −0.0015	
	Operating Temperature Range	J, KC			±0.006	
		LC, KM			+0.0045 −0.003	
		LM			+0.0045 −0.0015	
Integral Linearity Error ILE	T_A = +25°C	J		±0.003	±0.006	%FSR
		K, L		±0.0015	±0.003	
	Operating Temperature Range	J		±0.006	±0.009	
		K, LM		±0.003	±0.006	
		LC		±0.0015	±0.003	
Integral Linearity Error Temperature Coefficient		J		±0.3	±1.2	ppm/°C
		K, L		±0.2	±0.9	

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued)

$V^+ = +5V$, $V_{REF} = +5V$, $T_A = +25°C$, AGND = DGND, I_{OUT} at ground potential, unless otherwise specified

Parameter	Test Conditions/Comments		Limits			Units
			Min	Typ	Max	
DC ACCURACY (Continued)						
Unadjusted Gain Error	$T_A = +25°C$	J		±0.004	±0.012	%FSR
		K		±0.003	±0.009	
		L		±0.002	±0.006	
	Operating Temperature Range	J		±0.02	+0.04	
		K, L		±0.01	±0.02	
Unadjusted Gain Error Temperature Coefficient	(Note 4)	J		±1.0	±5.2	ppm/°C
		K, L		±0.5	±2.0	
Unadjusted Output Offset	DAC Register Outputs All LOW, (Note 6)			±4	±15	mV
Output Offset Temperature Drift	Same Conditions as Above, (Note 4)				±5	µV/°C
AC ACCURACY						
Power Supply Rejection	$\Delta V^+ = 5V \pm 10\%$, $T_A = +25°C$			±30	±100	ppm/V
	Operating Temperature Range			±50	±150	
Output Current Settling Time	To ½ LSB, (Note 4)			1.8	3	µs
REFERENCE INPUT						
Input Resistance	I_{OUT} at Ground		3	4.2	6	kΩ
ANALOG OUTPUT						
Output Capacitance (I_{OUT} Terminal)	DAC Register Outputs All LOW			150		pF
	DAC Register Outputs All HIGH			300		
DIGITAL INPUTS						
LOW State Threshold	Operating Temperature Range				0.8	V
HIGH State Threshold			2.4			
Input Current	Inputs between DGND to V^+			±0.001	±1	µA
Input Capacitance	(Note 4)			15		pF
POWER SUPPLY						
Supply Voltage Range*	Functional Operation, (Note 5)		4.5		5.5	V
Supply Current (Excluding Ladder Network)	$T_A = +25°C$ Digital Inputs HIGH or LOW			0.6	1.5	mA
	Operating Temperature Range Digital Inputs HIGH or LOW			1.0	2.5	

NOTES 3: Military temperature range parts are also tested to stated limits at −55°C and +125°C.
4: Guaranteed by characterization but not tested on a production basis.
5: Guaranteed by PSRR test.
6: Refer to Figure 4. Measured at output of amplifier A1 (A1 having zero offset). $V_{REF} = +5V$. Adjustable to zero with external potentiometer.

SWITCHING CHARACTERISTICS $V^+ = +5V$, $T_A = +25°C$; see Timing Diagram, Figure 3 (Note 4)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
t_{CWs}	$\overline{\text{C}}$hip $\overline{\text{S}}$elect-$\overline{\text{WR}}$ite Set-Up Time		0			ns
t_{CWh}	$\overline{\text{C}}$hip $\overline{\text{S}}$elect-$\overline{\text{WR}}$ite Hold Time		0			
$t_{\overline{WR}}$	$\overline{\text{WR}}$ite Pulse Width Low		200			
t_{DWs}	Data-$\overline{\text{WR}}$ite Set-Up Time		200			
t_{CWh}	Data-$\overline{\text{WR}}$ite Hold Time		0			

NOTE: All typical values have been characterized but are not tested.

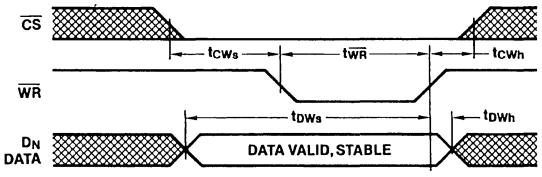


Figure 3: Timing Diagram

Table 1. Pin Assignment and Function Description

Pin	Name	Description
1	D_0	Least Significant Bit
2	D_1	
3	D_2	
4	D_3	
5	D_4	Input
6	D_5	
7	D_6	Data
8	D_7	
9	D_8	Bits
10	D_9	
11	D_{10}	(HIGH = True)
12	D_{11}	
13	D_{12}	
14	D_{13}	
15	D_{14}	
16	D_{15}	Most Significant Bit
17	PROG	Used for programming only. Tie to +5V for normal operation.
18	V_{REF}	V_{REF} input to ladder.
19	R_{INV}	Summing node for inverting amplifier.
20	R_{OFS}	Bipolar offset resistor, to $-V_{REF}$.
21	R_{FB}	Feedback resistor for voltage output applications.
22	DGND	Digital Ground return.
23	$AGND_F$	Analog Ground Force Line. Used to carry current from internal Analog GrouND connections.
24	$AGND_S$	Analog Ground Sense line. Reference point for external circuitry. Pin should carry minimal current.
25	I_{OUT}	Current output pin.
26	V^+	Positive supply voltage.
27	$\overline{CS}$	Chip Select. Active low. Enables writing to register.
28	$\overline{WR}$	WRite input. Active low. Writes into register. Equivalent to $\overline{CS}$.

DEFINITION OF TERMS

INTEGRAL LINEARITY ERROR: Error contributed by deviation of the DAC transfer function from a "best straight line" through the actual plot of transfer function. Normally expressed as a percentage of full scale range or in (sub)multiples of 1 LSB.

DIFFERENTIAL LINEARITY ERROR: The difference between ideal and actual value of the analog output "step size" for any two adjacent digital input code. The ideal "step size" is equal to 2^{-n} of full scale for an n-bit DAC or 1 LSB. It is expressed in (sub)multiples of 1 LSB.

RESOLUTION: It is addressing the smallest distinct analog output change that a D/A converter can produce. It is commonly expressed as the number of converter bits. A converter with resolution of n bits can resolve output changes of 2^{-n} of the full-scale range, e.g., 2^{-n} V_{REF} for a unipolar conversion. Resolution by no means implies linearity.

SETTLING TIME: Time required for the output of a DAC to settle to within a specified error band around its final value (e.g., ½ LSB) for a given digital input change, i.e., all digital inputs LOW to HIGH and HIGH to LOW.

GAIN ERROR: The difference between actual and ideal analog output values at full-scale range, i.e., all digital inputs at HIGH state. It is expressed as a percentage of full-scale range or in (sub)multiples of 1 LSB.

OUTPUT CAPACITANCE: Capacitance from I_{OUT} terminal to ground.

DETAILED DESCRIPTION

The ICL7121 consists of a 16-bit primary DAC, PROM controlled correction DACs, input buffer registers, and microprocessor interface logic. The 16-bit primary DAC is an R-2R thin film resistor ladder with N-channel MOS SPDT current steering switches. Precise balancing of the switch resistances and all other resistors in the ladder results in excellent temperature stability.

The low linearity error is acheived by programming a floating polysilicon gate PROM array which controls a 12-bit correction DAC (C-DAC). The most significant bits of the primary DAC register address this PROM array. Thus for every combination of the primary DAC's most significant bits a different C-DAC code is selected, allowing correction of superposition errors. These errors are caused by bit interaction on the primary ladder's current bus and by voltage non-linearity in the feedback resistor. Superposition errors cannot be corrected by any method that corrects individual bits only, such as laser trimming.

The onboard PROM also controls the 6-bit gain DAC. The G-DAC reduces gain error to less than 0.006% FSR by diverting to analog ground up to 2% of the current flowing in R_{FB}.

Since the PROM programming occurs in packaged form, it corrects for resistor shifts caused by the thermal stresses of packaging, unlike wafer-level trimming methods. Also, since the thin film resistors do not suffer laser trimming stresses, no degradation of time-stability results.

NOTE: All typical values have been characterized but are not tested.

APPLICATIONS

Bipolar Operation

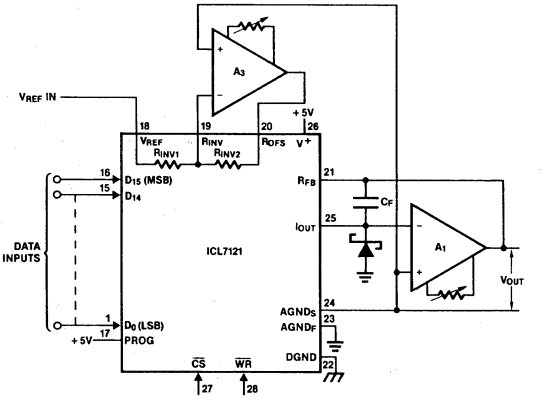
The circuit diagram for the normal configuration of the ICL7121 is shown in Figure 4. The positive and negative reference voltages allow full four-quadrant multiplication. Amplifier A_3, together with the internal resistors R_{INV1} and R_{INV2}, forms a simple voltage inverter circuit to generate $-V_{REF}$ for the R_{OFS} offset input pin. This will give the nominal "digital input code/analog output value" relationship of Table 2. Note that the value of R_{FB} is equal to 2R so full scale range is $2V_{REF}$.

The offset binary transfer function can be achieved simply by inverting the MSB. Inversion of the MSB can be done by an inverter or may be done in software.

Table 2. 2's Complement Bipolar Operation

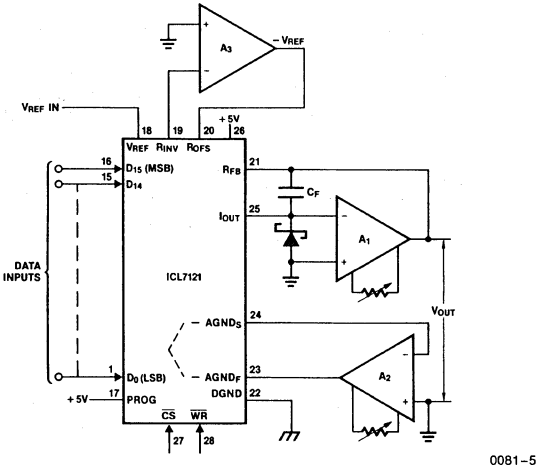
Digital Input				Analog Output
MSB			LSB	
0111	1111	1111	1111	$-V_{REF}\,(1 - 1/2^{15})$
0111	1111	1111	1110	$-V_{REF}\,(1 - 1/2^{14})$
0000	0000	0000	0001	$-V_{REF}\,(1/2^{15})$
0000	0000	0000	0000	0
1111	1111	1111	1111	$+V_{REF}\,(1/2^{15})$
1000	0000	0000	0010	$+V_{REF}\,(1 - 1/2^{14})$
1000	0000	0000	0001	$+V_{REF}\,(1 - 1/2^{15})$
1000	0000	0000	0000	$+V_{REF}$

Amplifier A_1 is the output amplifier. An additional amplifier A_2 may be used to force $AGND_F$ if the ground reference point is established elsewhere than at the DAC, as in Figure 5.



0081-4

Figure 4: Bipolar Operation, Four-Quadrant



0081-5

Figure 5: Bipolar Operation with Forced Ground

NOTE: All typical values have been characterized but are not tested.

A feedback compensation capacitor, C_F, improves the settling time by reducing ringing. This capacitor is normally in the 10 pF–40 pF range, depending on layout and the output amplifier selected. If C_F is too small, ringing or oscillation can occur when using an op amp with a high gain-bandwidth. If C_F is too large, the response of the output amplifier will be overdamped and will settle slowly.

The input circuits of some high speed op amps will sink large currents to their negative supply during power up and power down. The Schottky diode at I_{OUT} limits any negative-going transitions to less than −0.4V, avoiding the SCR latchup which could result if significant current was injected into the parasitic diode between I_{OUT} and DGND of the ICL7121. This diode is not needed when using the ICL7650 ultra low V_{OS} op amp.

Digital Interface

The ICL7121 has a 16-bit latch onboard and can interface directly to a 16-bit data bus. As shown in Figure 6, external latches or peripheral ICs can be used to interface to an 8-bit data bus. To ensure that the data is written into the onboard latch, the data must be valid 200 ns before the rising edge of $\overline{WR}$. If $\overline{WR}$ and $\overline{CS}$ are both low, the onboard latch is transparent and the input data is directly applied to the internal R-2R ladder switches. While this simplifies interfacing in non-microprocessor systems, having $\overline{WR}$ low before data is valid may cause additional glitches in some microprocessor systems. To avoid these glitches, data must be valid at the time $\overline{WR}$ goes low.

All digital interfaces can suffer from capacitive coupling between the digital lines and the analog section. There are two general precautions that will reduce this capacitive coupling problem: 1) reduce stray capacitance between digital lines and analog lines; and 2) reduce the number of transitions on the digital inputs. Careful board layout and shielding can minimize the capacitive coupling (see Figure 8). The activity on the digital input lines can be reduced by using external latches or peripheral interface ICs between the microprocessor bus and the ICL7121. This will reduce the number of transitions on the digital data and control lines of the ICL7121, thereby reducing the amount of digital noise coupled into sensitive analog sections.

OPERATIONAL AMPLIFIER SECTION

The input offset voltage, input current, gain, and bandwidth of the op amps used affect the circuit performance. Since the output impedance of I_{OUT} varies with the digital input code, the input current of amplifier A_1 will cause a code-dependent error at V_{OUT}, degrading the linearity. The input bias current should be significantly less than 1 LSB current, which is about 10 nA. In a similar manner, any offset voltage in A_1 will also cause linearity errors. The offset voltage of the output amplifier should be significantly less than 1 LSB (153 μV at V_{REF} = 5V).

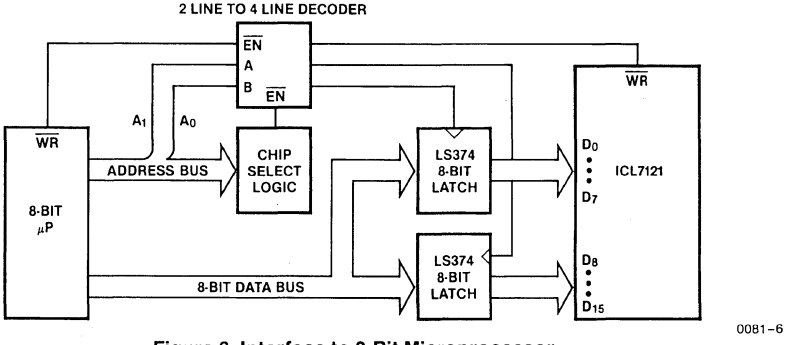


Figure 6: Interface to 8-Bit Microprocessor

NOTE: All typical values have been characterized but are not tested.

The voltage output settling time is highly dependent on the slew rate and gain-bandwidth of A_1, so for high speed operation a high speed op amp such as the HA2600 is recommended. For applications where high speed is not required, the ICL7650 or ICL7652 can be used for A_1. Since the ICL7650/52 offset voltage is less than 5 μV, no offset trimming is needed. To get a full 5V output swing from these op amps, $\pm$7.5V supplies should be used for the ICL7650/52.

Amplifier A_3, which is used to generate the inverted reference, needs only to have a stable offset and to be able to drive a 3 kΩ load. Since this is strictly a DC amplifier, the low noise ICL7652 is an ideal choice. Any variation in the offset voltage of A_3 will result in a drift in the bipolar zero, but will not affect the linearity of the ICL7121.

Amplifier A_2, used to generate a high quality ground, also needs a low offset and the ability to sink up to 2 mA.

MULTIPLYING MODE PERFORMANCE

While the ICL7121 can perform full four-quadrant multiplication, full 0.003% linearity is guaranteed only at V_{REF} = +5V. This is because the voltage coefficient of resistance of the R-2R ladder and the feedback resistor are significant at the 14- or 16-bit level. This effect is most significant at higher voltages, and adds errors on the order of 0.01% for a $\pm$10V full-scale. While the ICL7121 is tested and specified for V_{REF} = +5V, the R-2R ladder has the same voltage across it when V_{REF} = −5V. Therefore, voltage coefficients do not add any error with a −5V reference voltage.

GROUND LOOPS

Careful consideration must be given to ground loops in any high accuracy system. The current into the analog ground point inside the chip varies significantly with the input code value, and the inevitable resistances between this point and any external connection point can lead to significant voltage drop errors. For this reason, two separate leads are brought out from this point on the IC: $AGND_S$ and $AGND_F$. The varying current should be absorbed through the $AGND_F$ pin, and the $AGND_S$ pin will then accurately reflect the voltage on the internal current summing point, as shown in Figure 7. Output signals should ideally be referenced to the sense pin $AGND_S$, as shown in the application circuits.

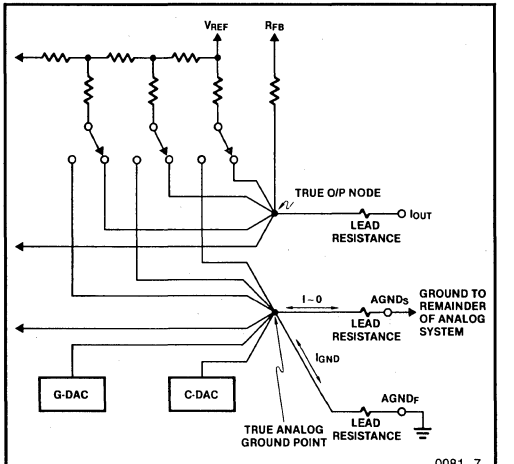
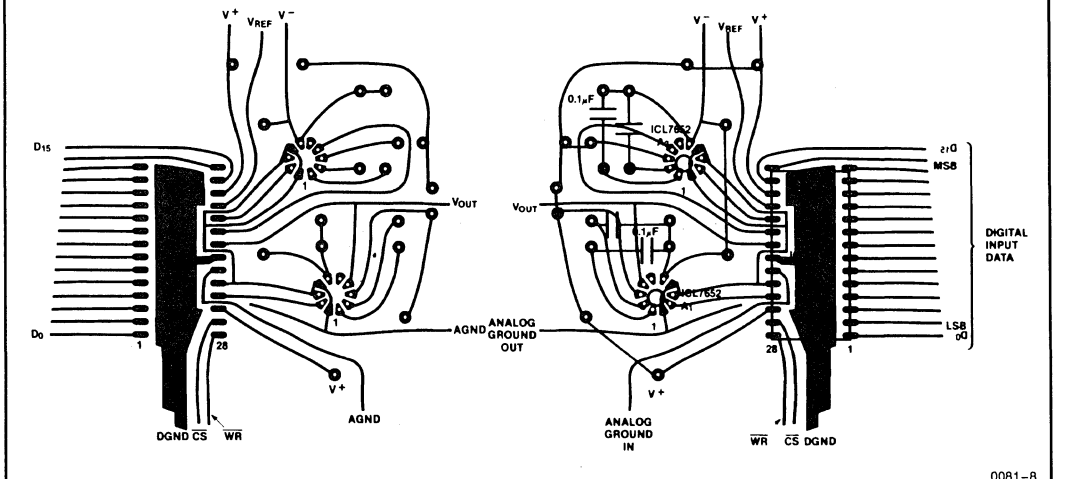


Figure 7: Eliminating Ground Loops



a. Printed Circuit Side of Board **b. Top Side with Component Placement**

Figure 8: Printed Circuit Board Layout (Single Sided Board)

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICL7134
14-Bit Multiplying μP-Compatible D/A Converter

GENERAL DESCRIPTION

The ICL7134 combines a four-quadrant multiplying DAC using thin film resistor and CMOS circuitry with an on-chip PROM-controlled correction circuit to achieve true 14-bit linearity without laser trimming.

Microprocessor bus interfacing is eased using standard memory WRite cycle timing and control signal use. Two input buffer registers are separately loaded with the 8 least significant bits (LS register) and the 6 most significant bits (MS register). Their contents are then transferred to the 14-bit DAC register, which controls the current switches. The DAC register can also be loaded directly from the data inputs, in which case the MS and LS registers are transparent.

The ICL7134 is available in two versions. The ICL7134U is programmed for unipolar operation while the ICL7134B is programmed for bipolar applications. The V_{REF} input to the most significant bit of the DAC is separated from the reference input to the remainder of the ladder. For unipolar use, the two reference inputs are tied together, while for bipolar operation, the polarity of the MSB reference is reversed, giving the DAC a true 2's complement input transfer function. Two resistors which facilitate the reference inversion are included on the chip, so only an external op-amp is needed. The PROM is coded to correct for errors in these resistors as well as the inversion of the MSB.

FEATURES

- **14-Bit Linearity (0.003% FSR)**
- **No Gain Adjustment Necessary**
- **Microprocessor-Compatible With Double Buffered Inputs**
- **Bipolar Application Requires No Extra Adjustments or External Resistors**
- **Low Linearity and Gain Temperature Coefficients**
- **Low Power Dissipation**
- **Full Four-Quadrant Multiplication**
- **883B Processed Versions Available**

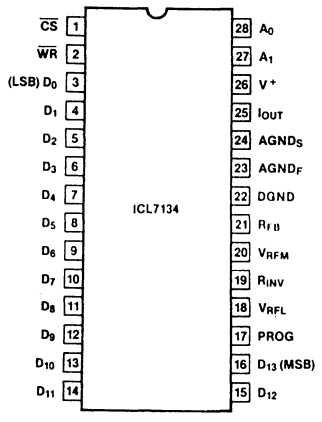


Figure 1: Pin Configuration (Outline dwg JI)

ORDERING INFORMATION

Non-Linearity at 25°C	Temperature Range		
	0°C to +70°C	−25°C to +85°C	−55°C to +125°C
Bipolar Versions			
0.01% (12-bit)	ICL7134BJCJI	ICL7134BJIJI	ICL7134BJMJI
0.006% (13-bit)	ICL7134BKCJI	ICL7134BKIJI	ICL7134BKMJI
0.003% (14-bit)	ICL7134BLCJI	ICL7134BLIJI	ICL7134BLMJI
Unipolar Versions			
0.01% (12-bit)	ICL7134UJCJI	ICL7134UJIJI	ICL7134UJMJI
0.006% (13-bit)	ICL7134UKCJI	ICL7134UKIJI	ICL7134UKMJI
0.003% (14-bit)	ICL7134ULCJI	ICL7134ULIJI	ICL7134ULMJI

PACKAGE: 28-pin CERDIP only

301664-005

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V^+ to DGND) ..... −0.3V to 7.5V
V_{RFL}, V_{RFM}, R_{INV}, R_{FB} to DGND ..... ±15V
I_{OUT}, $AGND_F$, $AGND_S$ ..... −0.1V to V^+
Current in $AGND_S$, $AGND_F$ 25mA
An, Dn, $\overline{WR}$, $\overline{CS}$, PROG ..... −0.3V to V^+ +0.3V

Operating Temperature Range
ICL7134XXC ..... 0°C to +70°C
ICL7134XXI ..... −25°C to +85°C
ICL7134XXM ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation (Note 2) 500mW
Derate Linearly Above 70°C @ 10mW/°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Note 1: All voltages with respect to DGND.

Note 2: Assumes all leads soldered or welded to printed circuit board.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

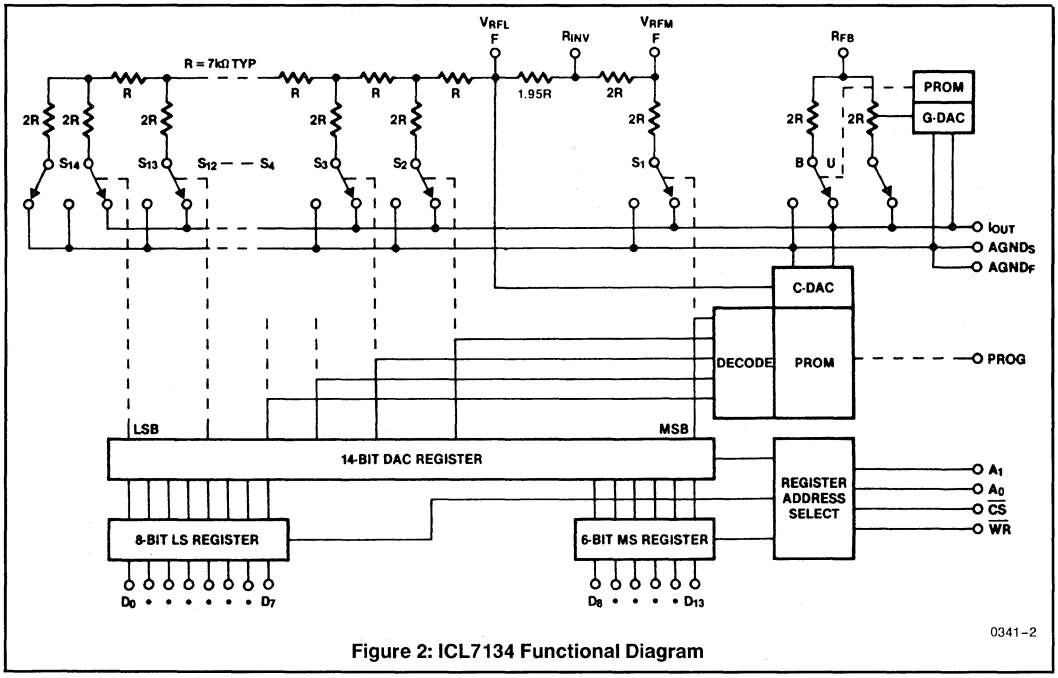


Figure 2: ICL7134 Functional Diagram

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

(V^+ = +5V, V_{REF} = +10V, T_A = +25°C, AGND = DGND, I_{OUT} at ground potential, unless otherwise specified.)

Parameter	Test Conditions/Comments		Value			Units
			Min	Typ	Max	
DC ACCURACY						
Monotonicity	(Note 3)	J	12			Bits
		K	13			
		L	14			
Gain Error	(Notes 1 and 2) Figure 4	J			±0.024	% FSR
		K			±0.012	
		L			±0.006	
Gain Error Temperature Coefficient	(Note 3)			±2	±8	ppm/°C
Output Leakage Current (I_{OUT} Terminal)	T_A = +25°C				±10	nA
	Operating Temperature Range			±60		
Long Term Stability of I_{OUT}	1000 Hours, +125°C, (Note 3)			±10		ppm/month
AC ACCURACY						
Power Supply Rejection	ΔV^+ = ±10%, Figure 5 T_A = +25°C			±10	±100	ppm/V
	Operating Temperature Range				±150	
Feedthrough Error	V_{REF} = 20 V_{P-P}, 10 kHz Sinewave, Figure 6	U		250		μV_{P-P}
		B		500		
Output Current Settling Time	To ½ LSB, Figure 7			1		µs
Output Noise	Equivalent to Johnson Noise of 7 kΩ Resistor, Typical					
REFERENCE INPUT						
Input Resistance	V_{RFL} = V_{RFM}, I_{OUT} at Ground		4	7	10	kΩ
ANALOG OUTPUT						
Output Capacitance (I_{OUT} Terminal)	DAC Register Outputs All LOW			160		pF
	DAC Register Outputs All HIGH			235		
DIGITAL INPUTS						
Low State Threshold	Operating Temperature Range				0.8	V
High State Threshold			2.4			
Input Current	Inputs between DGND to V^+				±1	µA
Input Capacitance	(Note 3)			15		pF
POWER SUPPLY						
Supply Voltage Range	Functional Operation, (Note 4)		3.5		6.0	V
Supply Current	Excluding Ladder Network (Note 5)			1.0	2.5	mA

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS ($V^+ = +5V$, $V_{REF} = +10V$, $T_A = +25°C$, AGND = DGND, I_{OUT} at ground potential, unless otherwise specified.) (Continued)

Parameter	Test Conditions/Comments		Value			Units
			Min	Typ	Max	
DC ACCURACY						
Resolution			14			Bits
Non-Linearity	(Notes 1 and 2) Figure 4	J			±0.012	% FSR
		K			±0.006	
		L			±0.003	
Non-Linearity Temperature Coefficient	Operating Temperature Range (Note 3)			±1	±2	ppm/°C

NOTES 1: Full-Scale Range (FSR) is 10V for unipolar mode, 20V (±10V) for bipolar mode.
2: Using internal feedback and reference inverting resistors.
3: Guaranteed by design, not production tested.
4: Gain error tested to 0.040% FSR. Specifications are not guaranteed.
5: D0–D13 connected to 2.4V.

SWITCHING CHARACTERISTICS ($V^+ = 5V$, $T_A = 25°C$, see Timing Diagram)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{AWs}	Address-$\overline{WR}$ite Set-Up Time		150			ns
t_{AWh}	Address-$\overline{WR}$ite Hold Time	(Note 3)	0			
t_{CWs}	$\overline{C}$hip $\overline{S}$elect-$\overline{WR}$ite Set-Up Time	(Note 3)	0			
t_{CWh}	$\overline{C}$hip $\overline{S}$elect-$\overline{WR}$ite Hold Time	(Note 3)	0			
$t_{\overline{WR}}$	$\overline{WR}$ite Pulse Width Low		200			
t_{DWs}	Data-$\overline{WR}$ite Set-Up Time		200			
t_{DWh}	Data-$\overline{WR}$ite Hold Time	(Note 3)	0			

Using 14 Bit Transparent Addressing

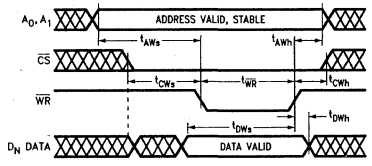


Figure 3A: Timing Diagram

Using Full Buffer 8 Bit Addressing Capability

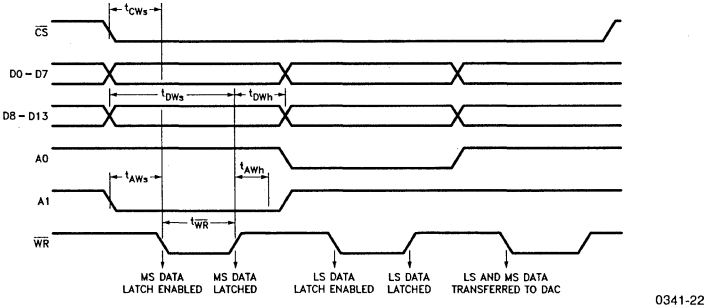


Figure 3B: ICL7134 Timing

NOTE: All typical values have been characterized but are not tested.

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a straight line through the end points of the actual plot of transfer function. Normally expressed as a percentage of full scale range or in (sub)multiples of 1 LSB.

RESOLUTION: It is addressing the smallest distinct analog output change that a D/A converter can produce. It is commonly expressed as the number of converter bits. A converter with resolution of n bits can resolve output changes of 2^{-n} of the full-scale range, e.g., $2^{-n}V_{REF}$ for a unipolar conversion. Resolution by no means implies linearity.

SETTLING TIME: Time required for the output of a DAC to settle to within specified error band around its final value (e.g., ½ LSB) for a given digital input change, i.e., all digital inputs LOW to HIGH and HIGH to LOW.

GAIN ERROR: The difference between actual and ideal analog output values at full-scale range, i.e., all digital inputs at HIGH state. It is expressed as a percentage of full-scale range or in (sub)multiples of 1 LSB.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to I_{OUT} with all digital inputs LOW.

OUTPUT CAPACITANCE: Capacitance from I_{OUT} terminal to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT} terminal when all DAC register outputs are LOW.

Table 1: Pin Descriptions

Pin	Symbol	Description	
1	$\overline{CS}$	Chip Select (active low). Enables register write.	
2	$\overline{WR}$	WRite, (active low). Writes in register. Equivalent to $\overline{CS}$.	
3	D_0	Bit 0	Least significant
4	D_1	Bit 1	Input Data Bits (High = True)
5	D_2	Bit 2	
6	D_3	Bit 3	
7	D_4	Bit 4	
8	D_5	Bit 5	
9	D_6	Bit 6	
10	D_7	Bit 7	
11	D_8	Bit 8	
12	D_9	Bit 9	
13	D_{10}	Bit 10	
14	D_{11}	Bit 11	
15	D_{12}	Bit 12	
16	D_{13}	Bit 13	Most significant.
17	PROG	Used for programming only. Tie to +5V for normal operation.	
18	V_{RFL}	V_{REF} for lower bits.	
19	R_{INV}	Summing node for reference inverting amplifier.	
20	V_{RFM}	V_{REF} for MSB only (bipolar).	
21	R_{FB}	Feedback resistor for voltage output applications.	
22	DGND	Digital GrouND return.	
23	$AGND_F$	Analog GrouND force lines. Use to carry current from internal Analog GrouND connections. Tied internally to $AGND_S$.	
24	$AGND_S$	Analog GrouND sense line. Reference point for external circuitry. Pin should carry minimal current; tied internally to $AGND_F$.	
25	I_{OUT}	Current output pin.	
26	V^+	Positive voltage.	
27	A_1	Address 1	Registers Select Lines
28	A_0	Address 0	

NOTE: All typical values have been characterized but are not tested.

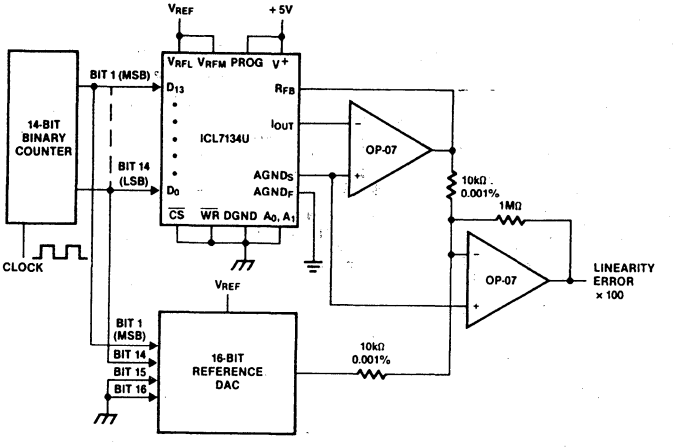


Figure 4: Non-Linearity Test Circuit

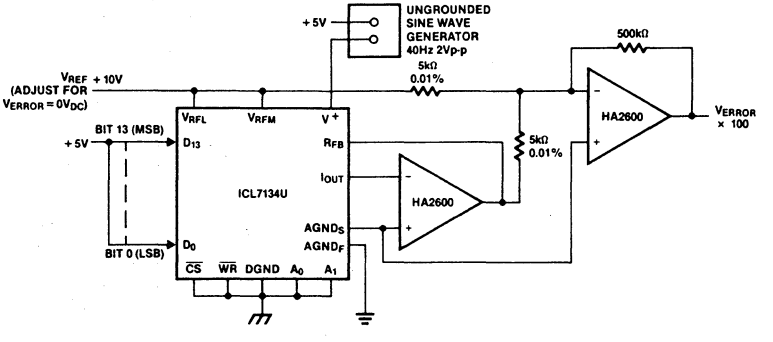


Figure 5: Power Supply Rejection Test Circuit

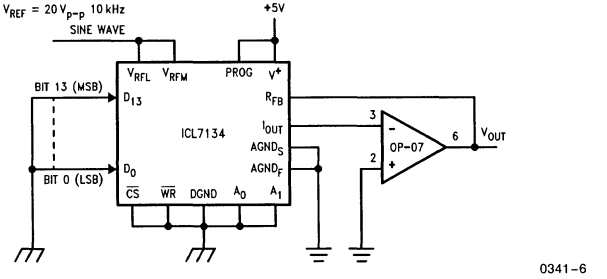
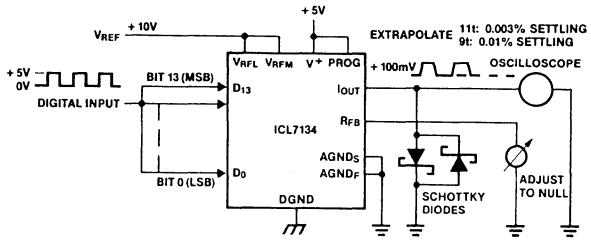


Figure 6: Feedthrough Error Test Circuit

NOTE: All typical values have been characterized but are not tested.



0341-7

Figure 7: Output Current Settling Time Test Circuit

DETAILED DESCRIPTION

The ICL7134 consists of a 14-bit primary DAC, two PROM controlled correction DACs, input buffer registers, and microprocessor interface logic (Figure 2). The 14-bit primary DAC is an R-2R thin film resistor ladder with N-channel MOS SPDT current steering switches. Precise balancing of the switch resistances, and all other resistances in the ladder, results in excellent temperature stability.

True 14-bit linearity is achieved by programming a floating polysilicon gate PROM array which controls two correction DAC circuits. A 6-bit gain correction DAC, or G-DAC, diverts up to 2% of the feedback resistor's current to Analog GounND and reduces the gain error to less than 1 LSB, or 0.006%. The 5 most significant outputs of the DAC register address a 31-word PROM array that controls a 12-bit linearity correction DAC, or C-DAC. For every combination of the primary DAC's 5 most significant bits, a different C-DAC code is selected. This allows correction of superposition errors, caused by bit interaction on the primary resistor ladder's current output bus and by voltage non-linearity in the feedback resistor. Superposition errors cannot be corrected by any method which corrects individual bits only, such as laser trimming. Since the PROM programming occurs in packaged form, it corrects for resistor shifts caused by the thermal stresses of packaging. These packaging shifts limit the accuracy that can be achieved using wafer level correction methods such as laser trimming, which has also been found to degrade the time stability of thin film resistors at the 14-bit level.

Analog Section

The ICL7134 inherently provides both unipolar and bipolar operation. The bipolar application circuit (Figure 8) requires one additional op-amp but no external resistors. The two on-chip resistors, R_{INV1} and R_{INV2}, together with the op-amp, form a voltage inverter which drives the MSB reference terminal, V_{RFM}, to $-V_{REF}$, where V_{REF} is the voltage applied at the less significant bits' reference terminal, V_{RFL}. Notice the values of 1.95R and 2R for the R_{INV1} and R_{INV2}. The V_{RFM} absolute value is about 2.5% higher than the V_{RFL}. This is necessary so that the gain error can be corrected. This reverses the weight of the MSB, and gives the DAC a 2's complement transfer function. The op-amp and reference connection to V_{RFM} and V_{RFL} can be reversed, without affecting linearity, but a small gain error will be introduced. For unipolar operation the V_{RFM} and V_{RFL} terminals are both tied to V_{REF}, and the R_{INV} pin is left unconnected.

Since the PROM correction codes required are different for bipolar and unipolar operation, the ICL7134 is available in two different versions; the ICL7134U, which is corrected for unipolar operation, and the ICL7134B, which is programmed for bipolar application. The feedback resistance is also different in the two versions, and is switched under PROM control from 'R' in the unipolar device to '2R' in the bipolar part. These feedback resistors have a dummy (always ON) switch in series to compensate for the effect of the ladder switches. This greatly improves the gain temperature coefficient and the power supply rejection of the device.

Digital Section

Two levels of input buffer registers allow loading of data from an 8-bit or 16-bit data bus. The A_0 and A_1 pins select one of four operations: 1) load the LS-buffer register with the data at inputs D_0 to D_7; 2) load the MS-buffer register with the data at inputs D_8 to D_{13}; 3) load the DAC register with the contents of the MS and LS-buffer registers and 4) load the DAC register directly from the data input pins (see Table 2). The $\overline{CS}$ and $\overline{WR}$ pins must be low to allow data transfers to occur. When direct loading is selected ($\overline{CS}$, $\overline{WR}$, A_0 and A_1 low) the registers are transparent, and the data input pins control the DAC output directly. The other modes of operation allow double buffered loading of the DAC from an 8-bit bus.

These input data pins are also used to program the PROM under control of the PROG pin. This is done in manufacturing, and for normal operation the PROG pin should be tied to V+ (+5V).

Table 2: Data Loading Controls

Control I/P				ICL7134 Operation
A_0	A_1	$\overline{CS}$	$\overline{WR}$	
X	X	X	1	No operation, device not selected.
X	X	1	X	
0	0	0	0	Load all registers from data bus.
0	1	0	0	Load LS register from data bus.
1	0	0	0	Load MS register from data bus.
1	1	0	0	Load DAC register from MS and LS register.

Note: Data is latched on LO-HI transition of either $\overline{WR}$ or $\overline{CS}$.

NOTE: All typical values have been characterized but are not tested.

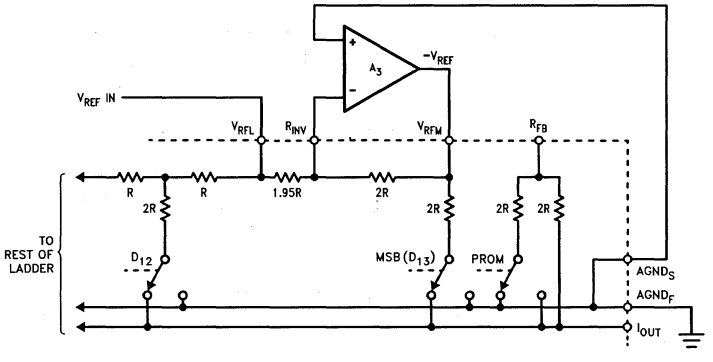


Figure 8: Bipolar Operation, with Inverted V_{REF} to MSB

APPLICATIONS

General Recommendations

GROUND LOOPS

Careful consideration must be given to ground loops in any 14-bit accuracy system. The current into the analog ground point inside the chip varies significantly with the input code value, and the inevitable resistances between this point and any external connection point can lead to significant voltage drop errors. For this reason, two separate leads are brought out from this point on the IC, the $AGND_F$ and $AGND_S$ pins. The varying current should be absorbed through the $AGND_F$ pin, and the $AGND_S$ pin will then accurately reflect the voltage on the internal current summing point, as shown in Figure 9. Thus output signals should be referenced to the sense pin $AGND_S$, as shown in the various application circuits.

OPERATIONAL AMPLIFIER SELECTION

To maintain static accuracy, the I_{OUT} potential must be exactly equal to the $AGND_S$ potential. Thus output amplifier selection is critical, in particular low input bias current (less than 2nA), low offset voltage drift (depending on the temperature range) and low offset voltage (less than 25μV) are advisable if the highest accuracy is needed. Maintaining a low input offset over a 0V to 10V range also requires that the output amplifier has a high open loop gain ($A_{VOL} > 400k$ for effective input offset less than 25μV).

The reference inverting amplifier used in the bipolar mode circuit must also be selected carefully. If 14-bit accuracy is desired without adjustment, low input bias current (less than 1nA), low offset voltage (less than 50μV), and high gain (greater than 400k) are recommended. If a fixed reference voltage is used, the gain requirement can be relaxed. For highest accuracy (better than 13 bits), an additional op-amp may be needed to correct for IR drop on the Analog GrouND line (op-amp A_2 in Figure 11). This op-amp should be selected for low bias current (less than 2nA) and low offset voltage (less than 50μV).

The op-amp requirements can be readily met by use of an ICL7650 chopper stabilized device. For faster settling time, an HA26XX can be used with an ICL7650 providing automatic offset null (see A053 applications note for details).

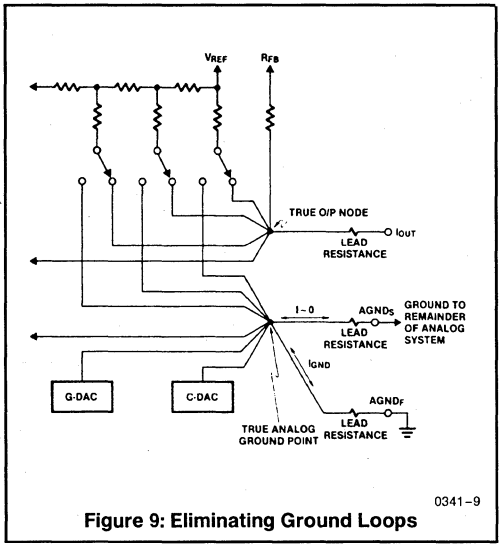


Figure 9: Eliminating Ground Loops

The output amplifier's non-inverting input should be tied directly to $AGND_S$. A bias current compensation resistor is of limited use since the output impedance at the summing node depends on the code being converted in an unpredictable way. If gain adjustment is required, low tempco (approximately 50ppm/°C) resistors or trim-pots should be selected.

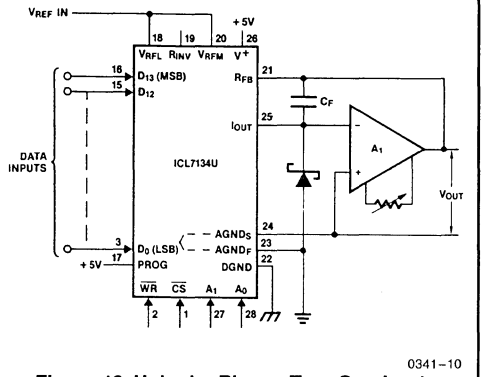
POWER SUPPLIES

The V^+ (pin 25) power supply should have a low noise level, and no transients exceeding 7 volts. Note that the absolute maximum for digital input voltage is $V^+ + 0.3V$, therefore V^+ must be applied before digital inputs are allowed to go high. Unused digital inputs must be connected to GND or V^+ for proper operation.

NOTE: All typical values have been characterized but are not tested.

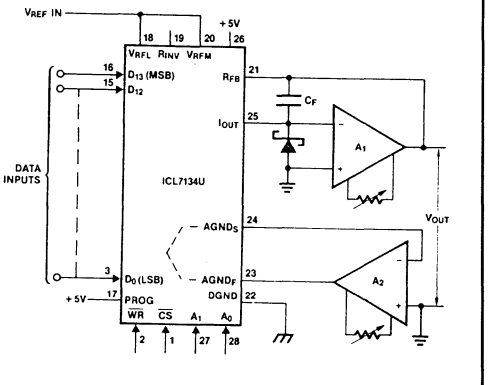
Unipolar Binary Operation (ICL7134U)

The circuit configuration for unipolar mode operation (ICL7134U) is shown in Figure 10. With positive and negative V_{REF} values the circuit is capable of two-quadrant multiplication. The "digital input code/analog output value" table for unipolar mode is given in Table 3. The Schottky diode (HP5082-2811 or equivalent) protects I_{OUT} from negative excursions which could damage the device, and is only necessary with certain high speed amplifiers. For applications where the output reference ground point is established somewhere other than at the DAC, the circuit of Figure 11 can be used. Here, op-amp A_2. removes the slight error due to IR voltage drop between the internal Analog GrouND node and the external ground connection. For 13-bit or lower accuracy, omit A_2 and connect $AGND_F$ and $AGND_S$ directly to ground through as low a resistance as possible.



0341-10

Figure 10: Unipolar Binary, Two-Quadrant Multiplying Circuit



0341-11

Figure 11: Unipolar Binary Operation with Forced Ground

Table 3: Code Table — Unipolar Binary Operation

Digital Input	Analog Output
1111111111111111	$-V_{REF}(1-1/2^{14})$
1000000000000001	$-V_{REF}(1/2+1/2^{14})$
1000000000000000	$-V_{REF}/2$
0111111111111111	$-V_{REF}(1/2-1/2^{14})$
0000000000000001	$-V_{REF}(1/2^{14})$
0000000000000000	0

ZERO OFFSET ADJUSTMENT

1. Connect all data inputs and $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND.
2. Adjust offset zero-adjust trim-pot of the operational amplifier A_2, if used, for a maximum of 0V $\pm 50\mu V$ at $AGND_S$.
3. Adjust the offset zero-adjust trim-pot of the output op-amp, A_1, for a maximum of 0V $\pm 50\mu V$ at V_{OUT}.

GAIN ADJUSTMENT (OPTIONAL)

1. Connect all data inputs to V+, connect $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND.
2. Monitor V_{OUT} for a $-V_{REF}(1-1/2^{14})$ reading.
3. To decrease V_{OUT}, connect a series resistor of 5Ω or less between the reference voltage and the V_{RFM} and V_{RFL} terminals (pins 20 and 18).
4. To increase V_{OUT}, connect a series resistor of 5Ω or less between A_1 output and the R_{FB} terminal (pin 21).

Bipolar (2's Complement) Operation (ICL7134B)

The circuit configuration for bipolar mode operation (ICL7134B) is shown in Figure 12. Using 2's complement digital input codes and positive and negative reference voltage values, four-quadrant multiplication is obtained. The "digital input code/analog output value" table for bipolar mode is given in Table 4. Amplifier A_3, together with internal resistors R_{INV1} and R_{INV2}, forms a simple voltage inverter circuit. The MSB ladder leg sees a reference input of approximately $-V_{REF}$, so the MSB's weight is reversed from the polarity of the other bits. In addition, the ICL7134B's feedback resistance is switched to 2R under PROM control, so that the bipolar output range is $+V_{REF}$ to $-V_{REF}$ $(1-1/2^{13})$. Again, the grounding arrangement of Figure 11 can be used, if necessary.

Table 4: Code Table — Bipolar (2's Complement) Operation

Digital Input	Analog Output
0111111111111111	$-V_{REF}(1-1/2^{13})$
0000000000000001	$-V_{REF}(1/2^{13})$
0000000000000000	0
1111111111111111	$V_{REF}(1/2^{13})$
1000000000000001	$V_{REF}(1-1/2^{13})$
1000000000000000	V_{REF}

NOTE: All typical values have been characterized but are not tested.

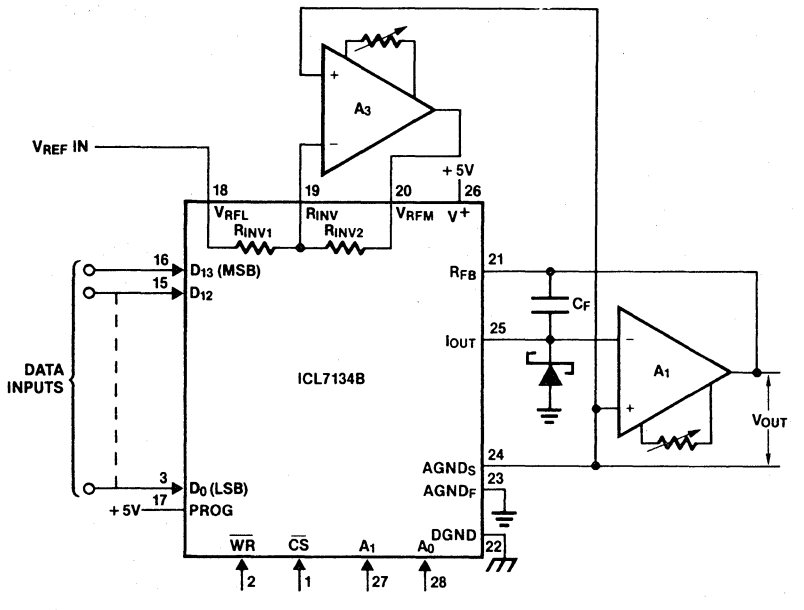


Figure 12: Bipolar (2's Complement), Four-Quadrant Multiplying Circuit

OFFSET ADJUSTMENT

1. Connect all data inputs and $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND.
2. Adjust the offset zero-adjust trim-pot of the operational amplifier A_2, if used, for a maximum of 0V $\pm 50\mu V$ at $AGND_S$.
3. Set data to 00000 . . . . 00. Adjust the offset zero-adjust trim-pot of the output op-amp A_1, for a maximum of 0V $\pm 50\mu V$ at V_{OUT}.
4. Connect D_{13} (MSB) data input to V^+.
5. Adjust the offset zero-adjust trim-pot of op-amp A_3 for a maximum of 0V $\pm 50\mu V$ at the R_{INV} terminal (pin 19).

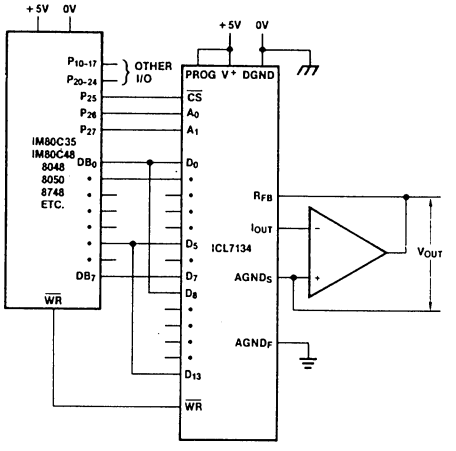
GAIN ADJUSTMENT (OPTIONAL)

1. Connect $\overline{WR}$, $\overline{CS}$, A_0 and A_1 to DGND.
2. Connect D_0, $D_1 \ldots D_{12}$ to V^+, D_{13} (MSB) to DGND.
3. Monitor V_{OUT} for a $-V_{REF}$ $(1 - 1/2^{13})$ reading.
4. To increase V_{OUT}, connect a series resistor of 10Ω or less between the A_1 output and the R_{FB} terminal (pin 21).
5. To decrease V_{OUT}, connect a series resistor of 5Ω or less between the reference voltage and the V_{RFL} terminal (pin 18).

Processor Interfacing

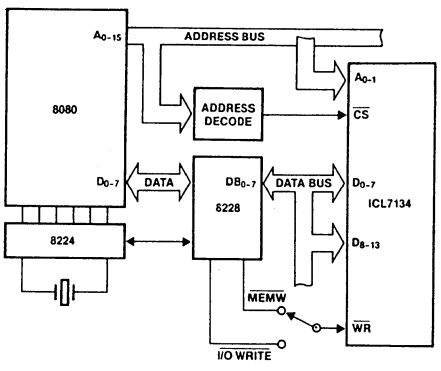
The ease of interfacing to a processor can be seen from Figure 13, which shows the ICL7134 connected to an 8035 or any other processor such as an 8049. The data bus feeds into both register inputs; three port lines, in combination with the $\overline{WR}$ line, control the byte-wide loading into these registers and then the DAC register. A complete DAC set-up requires 4 write instructions to the port, to set up the address and $\overline{CS}$ lines, and 3 external data transfers, one a dummy for the final transfer to the DAC register.

NOTE: All typical values have been characterized but are not tested.



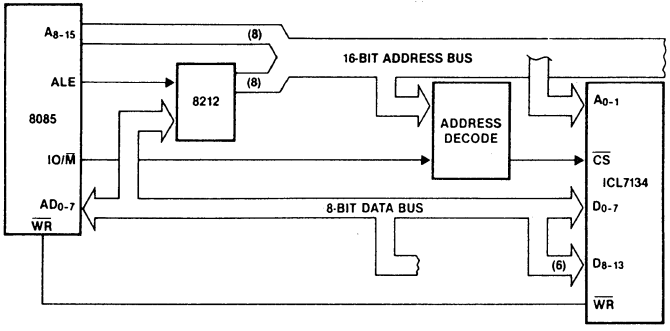
0341-13

Figure 13: ICL7134 Interface to 8048 System



0341-14

Figure 14: Interface to 8080 System



0341-15

Figure 15: 8085 System Interface

NOTE: All typical values have been characterized but are not tested.

A similar arrangement can be used with an 8080A, 8228, and 8224 chip set. Figure 14 shows the circuit, which can be arranged as a memory-mapped interface (using $\overline{MEMW}$) or as an I/O-mapped interface (using I/O $\overline{WRITE}$). See A020 and R005 for discussions of the relative merits of memory-mapped versus I/O-mapped interfacing, as well as some other ideas on interfacing with 8080 processors. The 8085 processor has a very similar interface, except that the control lines available are slightly different, as shown in Figure 15. The decoding of the IO/M line, which controls memory-mapped or I/O-mapped operation, is arbitrary, and can be omitted if not necessary. Neither the MC680X nor R650X processor families offer specific I/O operations. Figure 16 shows a suitable interface to either of these systems, using a direct connection. Several other decoding options can be used, depending on the other control signals generated in the system. Note that the R650X family does not require VMA to be decoded with the address lines.

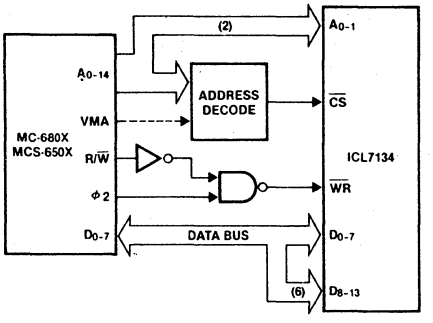


Figure 16: R650X and MC680X Families' Interface to ICL7134

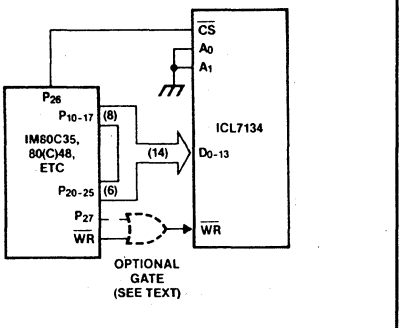


Figure 17: Avoiding Digital Feedthrough in an 8048 to ICL7134 Interface

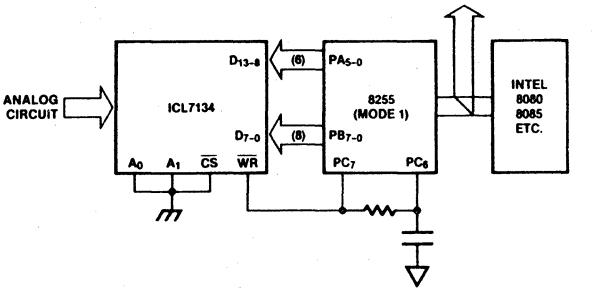


Figure 18: ICL7134 to 8048/80/85 Interface with Low Feedthrough

NOTE: All typical values have been characterized but are not tested.

Digital Feedthrough

All of the direct interfaces shown above can suffer from a capacitive coupling problem. The 14 data pins, and 4 control pins, all tied to active lines on a microprocessor bus, and in close proximity to the sensitive DAC circuitry, can couple pseudo-random spikes into the analog output. Careful board layout and shielding can minimize the problems (see **PC layout**), and clearly wire-wrap type sockets should never be used. Nevertheless, the inherent capacitance of the package alone can lead to unacceptable digital feedthrough in many cases. The only solution is to keep the digital input lines as inactive as possible. One easy way to do this is to use the peripheral interface circuitry available with all the systems previously discussed. These generally allow only 8 bits to be updated at any one time, but a little ingenuity will avoid difficulties with DAC steps that would result from partial updates. The problem can be solved for the 8048 family by tying the 14 port lines to the data input lines, with CS, A_0 and A_1 held low, and using only the $\overline{WR}$ line to enter the data into the DAC (as shown in Figure 17). $\overline{WR}$ is well separated from the analog lines on the ICL7134, and is usually not a very active line in 8048 systems. Additional "protection" can be achieved by gating the processor $\overline{WR}$ line with another port line. The same type of technique can be employed in the 8080/85 systems by using an 8255 PIA (peripheral Interface adapter) (Figure 18) and in the MC680X and R650X systems by using an MC6820 (R6520) PIA.

Successive Approximation A/D Converters

Figure 19 shows an ICL7134B-based circuit for a bipolar input high speed A/D converter, using two AM25L03s to form a 14-bit successive approximation register. The comparator is a two-stage circuit with an HA2605 front-end amplifier, used to reduce settling time problems at the summing node (see A020). Careful offset-nulling of this amplifier is needed, and if wide temperature range operation is desired, an auto-null circuit using an ICL7650 is probably advisable (see A053). The clock, using two Schmitt trigger TTL gates, runs at a slower rate for the first 8 bits, where settling-time is most critical, than for the last 6 bits. The short-cycle line is shown tied to the 15th bit; if fewer bits are required, it can be moved up accordingly. The circuit will free-run if the HOLD/$\overline{RUN}$ input is held low, but will stop after completing a conversion if the pin is high at that time. A low-going pulse will restart it. The STATUS output indicates when the device is operating, and the falling edge indicates the availability of new data. A unipolar version may be constructed by tying the MSB (D_{13}) on an ICL7134U to pin 14 on the first AM25L03, deleting the reference inversion amplifier A_4, and tying V_{RFM} to V_{RFL}.

PC BOARD LAYOUT

Great care should be taken in the board layout to minimize ground loop and similar "hidden resistor" problems, as well as to minimize digital signal feedthrough. A suitable layout for the immediate vicinity of the ICL7134 is shown in Figure 20, and may be used as a guide.

APPLICATION NOTES

Some applications bulletins that may be found useful are listed here:

A002 "Principles of Data Acquisition and Conversion"

A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood.

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing," by Ed Sliger.

A042 "Interpretation of Data Converters Accuracy Specifications"

R005 "Interfacing Data Converters & Microprocessors," by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

Most of these are available in the Harris Data Acquisition Handbook, together with other material.

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NOTE: All typical values have been characterized but are not tested.

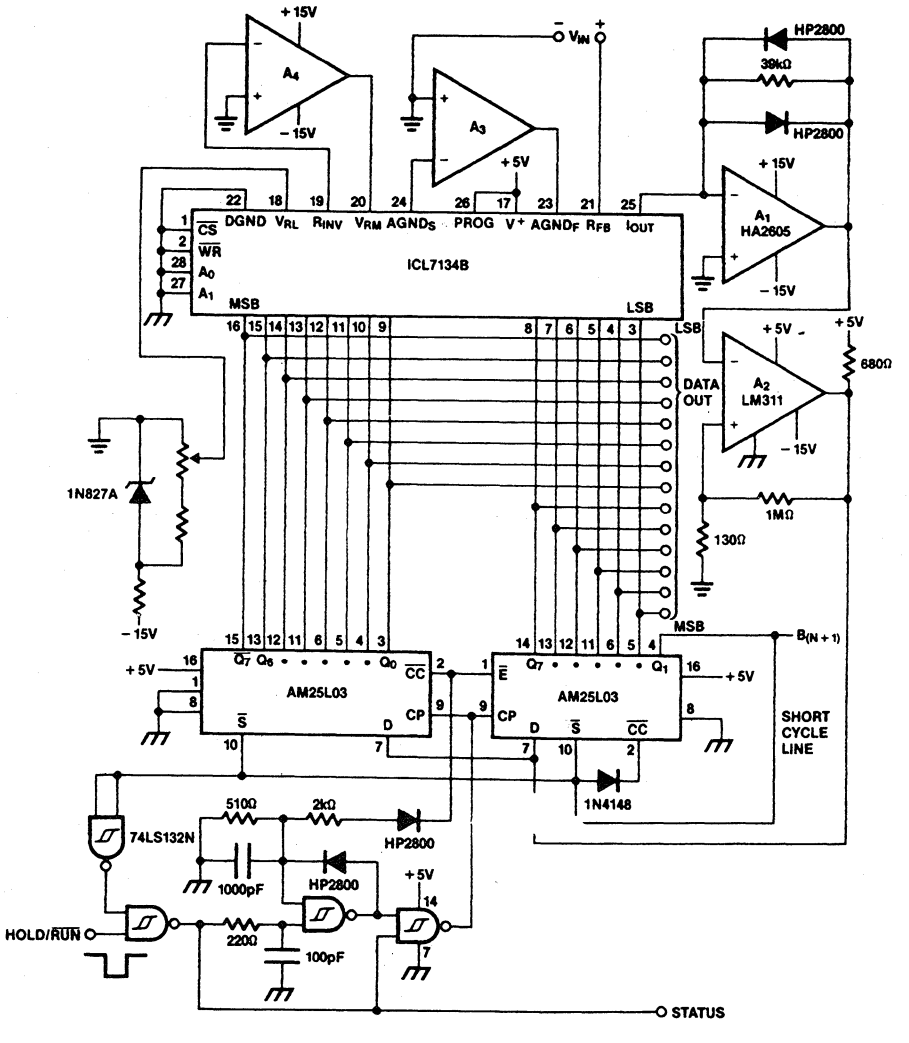
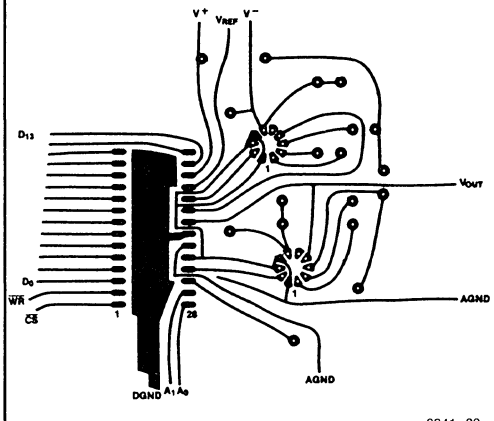


Figure 19: Successive Approximation A/D Converter

NOTE: All typical values have been characterized but are not tested.



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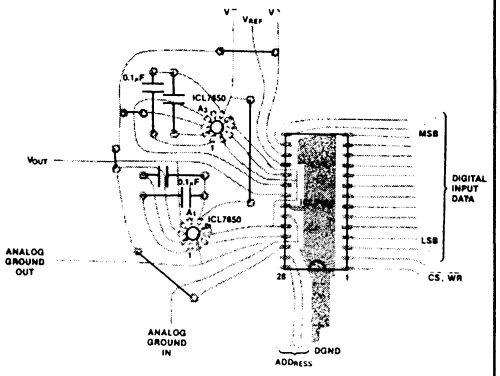
(a) Printed Circuit Side of Card (Single Sided Board)



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(b) Top Side with Component Placement

Figure 20: Printed Circuit Board Layout (Bipolar Circuit, see Figure 12)

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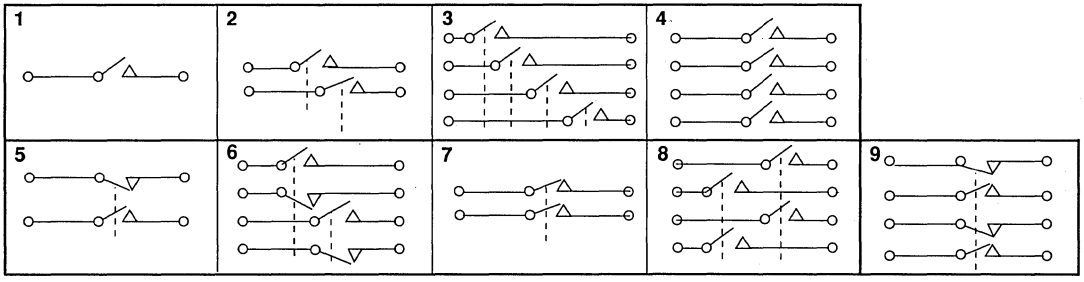
NOTE: All typical values have been characterized but are not tested.

DATA ACQUISITION 7

ANALOG SWITCHES

Switch Selector Guide



SPST (1)	Dual SPST (2)	Quad SPST (3)	4PST (4)	SPDT (5)	Dual SPDT (6)	DPST (7)	Dual DPST (8)	DPDT (9)

JFET SWITCHES

	DG180 DG181 DG182	IH401A		DG186 DG187 DG188	DG189 DG190 DG191		DG183 DG184 DG185	

CMOS SWITCHES

HI-5040 IH5140	DG200 DG300A HI-200 HI-222 HI-300 HI-304 HI-381 HI-5041 HI-5048 IH5041 IH5341	DG201 DG201A DG202 DG211 DG212 DG308A DG309 HI-201 HI-201HS IH5052 IH5053 IH5352	HI-5047 HI-5047A	DG301A HI-301 HI-305 HI-387 HI-5042 HI-5050 IH5142	DG303A HI-303 HI-307 HI-390 HI-5043 HI-5051 IH5043 IH5143 IH5151	HI-5044 IH5144	DG302A HI-302 HI-306 HI-384 HI-5045 HI-5049 IH5145	HI-5046 HI-5046A

PART#	SWITCH TOPOLOGY	TECHNOLOGY	RDS (on) MAX (1) @ 25°C (Ω)	IS (off) MAX @ 25°C (nA)	LOGIC INPUT SWITCH 'ON'	LOGIC LEVELS VINL (V)	LOGIC LEVELS VINH (V)	ANALOG SIGNAL RANGE (v)	SUPPLY VOLTAGE V+ (V)	SUPPLY VOLTAGE V− (V)	SUPPLY VOLTAGE VL (2) (V)	SWITCHING TIME TON (ns)	SWITCHING TIME TOFF (ns)	COMMENTS	PACKAGE & TEMPERATURE RANGE (4) PLASTIC DIP	PLASTIC SOIC	PLASTIC PLCC	CERDIP	METAL CAN
HI-5040	SINGLE SPST	36V CMOS-DI	50	0.8 typ	1	0.8	3.0	V− to V+	+15	−15	+5	1000	500		C			C,M	
IH5140	(fig. 1)	36V CMOS-JI	50	0.5	1	0.8	2.4	±11 typ	+15	−15	+5	150	125		C			C,M	
DG180	DUAL	36V N-JFET	10	10	1	0.8	2.0	V− +7.5to V+	+15	−15	+5	300	250	Low Ron					I,M
DG181	SPST	36V N-JFET	30	1	1	0.8	2.0	V− +7.5to V+	+15	−15	+5	150	130						I,M
DG182	(fig. 2)	36V N-JFET	75	1	1	0.8	2.0	V− +5 to V+	+15	−15	+5	250	130						I,M
DG200		36V CMOS-JI	80	5	0	0.8	2.4	V− to V+	+15	−15	n/a	1000	500		C			I,M	I,M
DG300A		44V CMOS-JI	50	5	1	0.8	4.0	V− to V+	+15	−15	n/a	150typ	130typ		C			C,I,M	C,I,M
HI-200		44V CMOS-DI	80	50	0	0.8	2.4	V− to V+	+15	−15	n/a	240typ	500typ		C	C,I		C,I,M	C,I,M
HI-222		36V CMOS-DI	50	2.5	0	0.8	2.0	V− to V+	+15	−15	n/a	200	200	RF/Video T switch		C,I	C	C,I	
HI-300		44V CMOS-DI	50	5	1	0.8	4.0	V− to V+	+15	−15	n/a	300	250					C,M	C,M
HI-304		44V CMOS-DI	50	5	1	3.5	11.0	V− to V+	+15	−15	n/a	250	150					C,M	C,M
HI-381		44V CMOS-DI	50	5	1	0.8	4.0	V− to V+	+15	−15	n/a	300	250					C	C,M
HI-5041		36V CMOS-DI	50 typ	0.8 typ	1	0.8	3.0	V− to V+	+15	−15	n/a	1000	500	Ron matching 10Ωmax @ 25°C				C,M	
HI-5048		36V CMOS-DI	25 typ	0.8 typ	1	0.8	3.0	V− to V+	+15	−15	n/a	1000	500	Ron matching 5Ωmax @ 25°C	C			C,M	
IH5041		36V CMOS-JI	80	5	1	0.8	2.4	±10 typ	+15	−15	+5	1000	500		C			C,M	
IH5141		36V CMOS-JI	75	5	1	0.8	2.4	±10 typ	+15	−15	+5	175	150		C			C,M	
IH5341		36V CMOS-JI	75	1	1	0.8	2.4	V− to V+	+15	−15	+5	300	150	RF/Video T switch	C				I,M
DG201	QUAD	36V CMOS-JI	100	5	0	0.8	2.4	V− to V+	+15	−15	n/a	1000	500		C			I, M	
DG201A	SPST	44V CMOS-JI	200	5	0	0.8	2.4	V− to V+	+15	−15	n/a	600	450		C			C,I,M	
DG202	(fig. 3)	44V CMOS-JI	200	5	1	0.8	2.4	V− to V+	+15	−15	n/a	600	450		C			C,I,M	
DG211		44V CMOS-JI	175	5	0	0.8	2.4	V− to V+	+15	−15	+5	1000	500		C	C			
DG212		44V CMOS-JI	175	5	1	0.8	2.4	V− to V+	+15	−15	+5	1000	500		C	C			
DG308A		44V CMOS-JI	100	5	1	3.5	11.0	V− to V+	+15	−15	n/a	200	150		C	C		C,I,M	
DG309		44V CMOS-JI	100	5	0	3.5	11.0	V− to V+	+15	−15	n/a	200	150		C	C		C,I,M	
HI-201		44V CMOS-DI	80	50	0	0.8	2.4	V− to V+	+15	−15	n/a	185typ	220typ		C	C,I	C	C,I,M	
HI-201HS		36V CMOS-DI	50	1	0	0.8	2.4	V− to V+	+15	−15	n/a	50	50	High speed	C,I	C,I	C,I	C,I,M	
IH-5052		36V CMOS-JI	100	5	0	0.8	2.4	±10 typ	+15	−15	+5	1000	500					C,M	
IH-5053		36V CMOS-JI	100	5	1	0.8	2.4	±10 typ	+15	−15	+5	1000	500					C,M	
IH-5352		36V CMOS-JI	75	2	1	0.8	2.4	V− to V+	+15	−15	+5	300	150	RF/Video T switch	C			I,M	
HI-5047	4PST	36V CMOS-DI	50 typ	0.8 typ	1	0.8	3.0	V− to V+	+15	−15	n/a	1000	500	Ron matching 10Ωmax @ 25°C	C			C,M	
HI-5047A	(fig. 4)	36V CMOS-DI	25 typ	0.8 typ	1	0.8	3.0	V− to V+	+15	−15	n/a	1000	500	Ron matching 5Ωmax @ 25°C	C			C,M	
DG186	SPDT	36V N-JFET	10	10	(3)	0.8	2.0	V− +7.5to V+	+15	−15	+5	300	250	Low Ron				I,M	
DG187	(fig. 5)	36V N-JFET	30	1	(3)	0.8	2.0	V− +7.5to V+	+15	−15	+5	150	130					I,M	
DG188		36V N-JFET	75	1	(3)	0.8	2.0	V− +5 to V+	+15	−15	+5	250	130					I,M	
DG301A		44V CMOS-JI	50	5	(3)	0.8	4.0	V− to V+	+15	−15	n/a	150typ	130typ		C			C,I,M	C,I,M
HI-301		44V CMOS-JI	50	5	(3)	0.8	4.0	V− to V+	+15	−15	n/a	300	250					C,M	C,M
HI-305		44V CMOS-DI	50	5	(3)	3.5	11.0	V− to V+	+15	−15	n/a	250	150					C,M	C,M
HI-387		44V CMOS-DI	50	5	(3)	0.8	4.0	V− to V+	+15	−15	n/a	300	250					C,M	C,M
HI-5042		36V CMOS-DI	50	0.8	(3)	0.8	3.0	V− to V+	+15	−15	n/a	1000	500	Ron matching 10Ωmax @ 25°C				C,M	
HI-5050		36V CMOS-DI	25 typ	0.8 typ	(3)	0.8	3.0	V− to V+	+15	−15	n/a	1000	500	Ron matching 5Ωmax @ 25°C				C,M	
IH5142		36V CMOS-JI	75	5	(3)	0.8	2.4	±10 typ	+15	−15	+5	300	150		C			C,M	

Switch Selector Guide

(Continued)

PART#	SWITCH TOPOLOGY	TECHNOLOGY	RDS (on) MAX (1) @ 25°C (Ω)	IS (off) MAX @ 25°C (nA)	LOGIC INPUT SWITCH "ON"	LOGIC LEVELS VINL (V)	LOGIC LEVELS VINH (V)	ANALOG SIGNAL RANGE (v)	SUPPLY VOLTAGE V+ (V)	SUPPLY VOLTAGE V− (V)	SUPPLY VOLTAGE VL (2) (V)	SWITCHING TIME TON (ns)	SWITCHING TIME TOFF (ns)	COMMENTS	PACKAGE & TEMPERATURE RANGE (4) PLASTIC DIP	PLASTIC SOIC	PLASTIC PLCC	CERDIP	METAL CAN
DG189	DUAL	36V N-JFET	10	10	(3)	0.8	2.0	V− +7.5 to V+	+15	−15	+5	300	250	Low Ron				I,M	
DG190	SPDT	36V N-JFET	30	1	(3)	0.8	2.0	V− +7.5 to V+	+15	−15	+5	150	130					I,M	
DG191	(fig. 6)	36V N-JFET	75	1	(3)	0.8	2.0	V− +5 to V+	+15	−15	+5	250	130					I,M	
DG303A		44V CMOS-JI	50	5	(3)	0.8	4.0	V− to V+	+15	−15	n/a	150 typ	130 typ		C			C,I,M	
HI-303		44V CMOS-DI	50	5	(3)	0.8	4.0	V− to V+	+15	−15	n/a	300	250					C,M	
HI-307		44V CMOS-DI	50	5	(3)	3.5	11.0	V− to V+	+15	−15	n/a	250	150					C,M	
HI-390		44V CMOS-DI	50	5	(3)	0.8	4.0	V− to V+	+15	−15	n/a	300	250					C,M	
HI-5043		36V CMOS-DI	50 typ	0.8 typ	(3)	0.8	3.0	V− to V+	+15	−15	n/a	1000	500	Ron matching 10Ωmax @ 25°C	C	C,I	C	C,M	
HI-5051		36V CMOS-DI	25 typ	0.8 typ	(3)	0.8	3.0	V− to V+	+15	−15	n/a	1000	500	Ron matching 5Ωmax @ 25°C	C	C,I	C	C,M	
IH5043		36V CMOS-JI	80	5	(3)	0.8	2.4	±10 typ	+15	−15	+5	1000	500		C	C		C,M	
IH5143		36V CMOS-JI	75	5	(3)	0.8	2.4	±10 typ	+15	−15	+5	300	150		C			C,M	
IH5151		36V CMOS-JI	30	2	(3)	0.8	2.4	V− to V+	+15	−15	+5	500	250		c			C,M	
HI-5044	DUAL DPST	36V CMOS-DI	50 typ	0.8 typ	1	0.8	3.0	V− TO V+	+15	−15	n/a	1000	500	Ron matching 10Ωmax @ 25°C	C			C,M	
IH5144	(fig. 7)	36V CMOS-JI	75	5	1	0.8	2.4	±10 typ	+15	−15	+5	300	150		C			C,M	
DG183	DUAL DPST	36V N-JFET	10	10	1	0.8	2.0	V− +7.5 to V+	+15	−15	+5	300	250	Low Ron				I,M	
DG184	(fig 8)	36V N-JFET	30	1	1	0.8	2.0	V− +7.5 to V+	+15	−15	+5	150	130					I,M	
DG185		36V N-JFET	75	1	1	0.8	2.0	V− +5 to V+	+15	−15	+5	250	130					I,M	
DG302A		44V CMOS-JI	50	5	1	0.8	4.0	V− to V+	+15	−15	n/a	150 typ	130 typ		C			C,I,M	
HI-302		44V CMOS-DI	50	5	1	0.8	4.0	V− to V+	+15	−15	n/a	300	250					C,M	
HI-306		44V CMOS-DI	50	5	1	3.5	11.0	V− to V+	+15	−15	n/a	250	150					C,M	
HI-384		44V CMOS-DI	50	5	1	0.8	4.0	V− to V+	+15	−15	n/a	300	250					C,M	
HI-5045		36V CMOS-DI	50 typ	0.8 typ	1	0.8	3.0	V− to V+	+15	−15	n/a	1000	500	Ron matching 10Ωmax @ 25°C	C	C,I	C	C,M	
HI-5049		36V CMOS-DI	25 typ	0.8 typ	1	0.8	3.0	V− to V+	+15	−15	n/a	1000	500	Ron matching Ωmax @ 25°C	C	C,I	C	C,M	
IH5145		36V CMOS-JI	75	5	1	0.8	2.4	± 10 typ	+15	−15	+5	300	150		C			C,M	
HI-5046	DPDT	36V CMOS-DI	50 typ	0.8 typ	(3)	0.8	3.0	V− to V+	+15	−15	n/a	1000	500	Ron matching Ωmax @ 25°C	C			C,M	
HI-5046A	(fig 9)	36V CMOS-DI	25 typ	0.8 typ	(3)	0.8	3.0	V− to V+	+15	−15	n/a	1000	500	Ron matching Ωmax @ 25°C	C			C,M	

Notes: 1. The RDS (on) of a CMOS switch varies as a function of supply voltage, analog signal voltage, and temperature.
2. Logic supply voltage, if required.
3. Refer to data sheet for the switch states of SPDT and DPDT switches.
4. Refer to the individual data sheet for specific package lead count and temperature range information.
The following temperature range conventions are used: C = commercial temp range, I = industrial temp range, M = military temp range

P-CHANNEL JFET SWITCH CONFIGURATION				OUTPUT CONFIGURATION	CHARACTERISTICS LOGIC LEVEL	CHARACTERISTICS Rds (on) MAX @25°C	CHARACTERISTICS ID (off) MAX @25°C	CHARACTERISTICS t (on) & t (off) MAX @25°C	PACKAGE & TEMP RANGE (1) PLASTIC DIP	PACKAGE & TEMP RANGE (1) CERAMIC DIP
SINGLE	DUAL	TRIPLE	QUAD							
	IH5017		IH5009	COMMON	+15V	100Ω	±0.5nA	500ns	C	C,M
IH5022	IH5018	IH5014	IH5010		+5V	150Ω			C	C,M
	IH5019		IH5011	SEPARATE	+15V	100Ω			C	C,M
IH5024	IH5020	IH5016	IH5012		+5V	150Ω			C	C,M

Note: 1. Refer to the data sheet for specific package lead count and temperature range information.
C = commercial temperature range, M = military temperature range

HARRIS SEMICONDUCTOR

DG180-191
High-Speed Driver With JFET Switch

GENERAL DESCRIPTION

The DG180 thru DG191 series of analog gates consist of 2 or 4 N-channel junction-type field-effect transistors (JFET) designed to function as electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2V) to control the ON-OFF state of each switch. The driver is designed to provide a turn-off speed which is faster than turn-on speed, so that break-before-make action is achieved when switching from one channel to another. In the ON state, each switch conducts current equally well in both directions. In the OFF condition, the switches will block voltages up to 20V peak-to-peak. Switch-OFF input-output isolation is 50dB at 10MHz, due to the low output impedance of the FET-gate driving circuit.

FEATURES

- **Constant ON-Resistance for Signals to ±10V (DG182, 185, 188, 191), to ±7.5V (All Devices)**
- **±15V Power Supplies**
- **<2nA Leakage From Signal Channel in Both ON and OFF States**
- **TTL, DTL, RTL Direct Drive Compatibility**
- **t_{on}, t_{off} < 150ns, Break-Before-Make Action**
- **Cross-talk and Open Switch Isolation > 50dB at 10MHz (75Ω Load)**
- **JAN 38510 Approved**

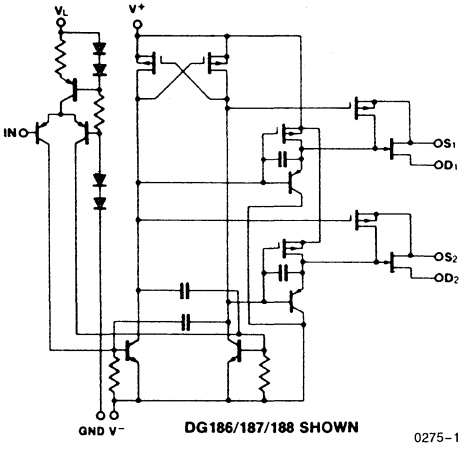
ORDERING INFORMATION

Part Number	Type	$r_{DS(on)}$ (Max)
DG180	Dual SPST	10
DG181	Dual SPST	30
DG182	Dual SPST	75
DG183	Dual DPST	10
DG184	Dual DPST	30
DG185	Dual DPST	75
DG186	SPDT	10
DG187	SPDT	30
DG188	SPDT	75
DG189	Dual SPDT	10
DG190	Dual SPDT	30
DG191	Dual SPDT	75

DG 181 X Y

- PACKAGE
  - A – 10-PIN METAL CAN
  - L – 14-PIN FLAT PACK
  - P – CERAMIC DIP
- TEMPERATURE
  - A – MILITARY (−55°C to +125°C)
  - B – INDUSTRIAL (−20°C to +85°C)
- DEVICE TYPE
- DRIVER

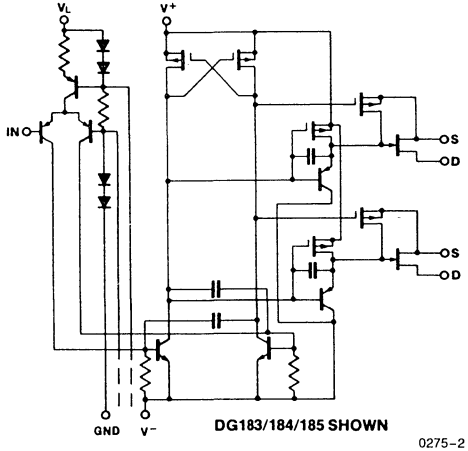
ONE AND TWO CHANNEL SPDT AND SPST CIRCUIT CONFIGURATION



DG186/187/188 SHOWN

0275-1

TWO CHANNEL DPST CIRCUIT CONFIGURATION



DG183/184/185 SHOWN

0275-2

Figure 1: Functional Diagram (Typical Channel)

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

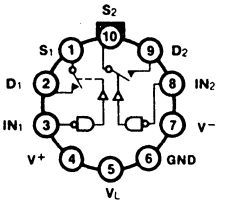
V^+-V^-	36V	GND–V^-	27V
V^+-V_D	33V	GND–V_{IN}	20V
V_D-V^-	33V	Current (S or D) See Note 3	200mA
V_D-V_S	±22V	Storage Temperature	−65°C to +150°C
V_L-V^-	36V	Operating Temperature	−55°C to +125°C
V_L-V_{IN}	8V	Power Dissipation*	450 (TW), 750 (FLAT), 825(DIP)mW
V_L–GND	8V	Lead Temperature (Soldering, 10sec)	300°C
V_{IN}–GND	8V		

*Device mounted with all leads welded or soldered to PC board. Derate 6mW/°C (TW); 10mW/°C (FLAT); 11mW/°C (DIP) above 75°C.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DUAL SPST (DG180, 181, 182)

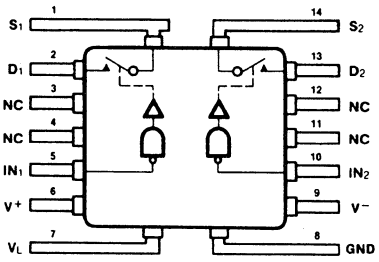
Metal Can Package



0275-3

(OUTLINE DWG TO-100)

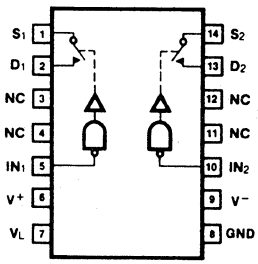
Flat Package



0275-4

(OUTLINE DWG FD-2)

Ceramic

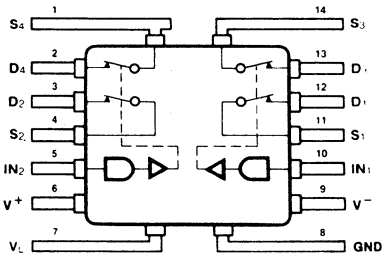


0275-5

(OUTLINE DWG DD)

DUAL DPST (DG183, 184, 185)

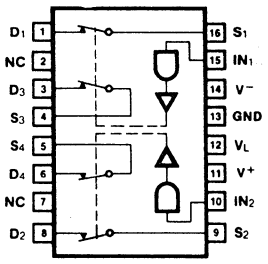
Flat Package



0275-6

(OUTLINE DWG FD-2)

Ceramic



0275-7

(OUTLINE DWG DD)

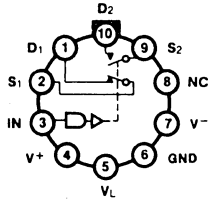
Figure 2: Pin Configurations and Switching State Diagram

NOTE: All typical values have been characterized but are not tested.

DG180-191

SPDT (DG186, 187, 188)

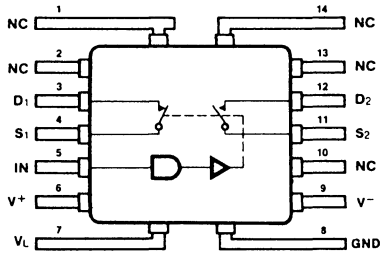
Metal Can Package



0275-8

(OUTLINE DWG TO-100)

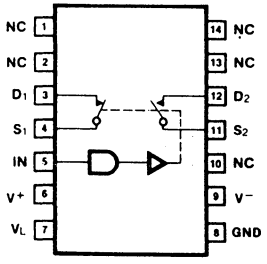
Flat Package



0275-9

(OUTLINE DWG FD-2)

Ceramic

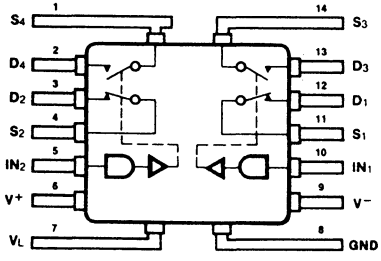


0275-10

(OUTLINE DWG DD)

DUAL SPDT (DG189, 190, 191)

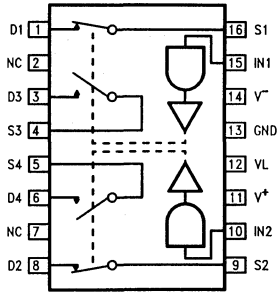
Flat Package



0275-11

(OUTLINE DWG FD-2)

Ceramic



0275-12

(OUTLINE DWG DE)

Figure 2: Pin Configurations and Switching State Diagram (Cont.)

ELECTRICAL CHARACTERISTICS ($V^+ = +15V$, $V^- = -15V$, $V_L = 5V$, Unless Noted)

Parameter	Device No.	Test Conditions (Note 1)	A Series			B Series			Units
			−55°C	+25°C	+125°C	−20°C	+25°C	+85°C	
SWITCH									
$I_{S(off)}$	DG181, 182, 184, 185 187, 188, 190, 191 (DG180, 183, 186, 189)	$V_S = 10V$, $V_D = -10V$, $V^+ = 10V$ $V^- = -20V$, V_{IN} = "OFF"		±1 ±(10)	100 (1000)		±5 (15)	100 (300)	nA
	DG181, 184, 187, 190 (DG180, 183, 186, 189)	$V_S = 7.5V$, $V_D = -7.5V$ V_{IN} = "OFF"		±1 ±(10)	100 (1000)		±5 (15)	100 (300)	nA
	DG182, 185, 188, 191	$V_S = 10V$, $V_D = -10V$ V_{IN} = "OFF"		±1	100		±5	100	nA
$I_{D(off)}$	DG181, 182, 184, 185 187, 188, 190, 191 (DG180, 183, 186, 189)	$V_S = 10V$, $V_D = -10V$, $V^+ = 10V$ $V^- = -20V$, V_{IN} = "OFF"		±1 ±(10)	100 (1000)		±5 (15)	100 (300)	nA
	DG181, 184, 187, 190 (DG180, 183, 186, 189)	$V_S = 7.5V$, $V_D = -7.5V$ V_{IN} = "OFF"		±1 ±(10)	100 (1000)		±5 (15)	100 (300)	nA
	DG182, 185, 188, 191	$V_S = 10V$, $V_D = -10V$ V_{IN} = "OFF"		±1	100		±5	100	nA

NOTE: All typical values have been characterized but are not tested.

DG180-191

ELECTRICAL CHARACTERISTICS ($V^+ = +15V$, $V^- = -15V$, $V_L = 5V$, Unless Noted) (Continued)

Parameter	Device No.	Test Conditions (Note 1)	A Series			B Series			Units
			−55°C	+25°C	+125°C	−20°C	+25°C	+85°C	
SWITCH (Continued)									
$I_{D(on)} + I_{S(on)}$	DG180, 181, 183, 184 186, 187, 189, 190	$V_D = V_S = -7.5V$, V_{IN} = "ON"		±2	−200		−10	−200	nA
	DG182, 185, 188, 191	$V_D = V_S = -10V$, V_{IN} = "ON"		±2	−200		−10	−200	nA
INPUT									
I_{INL}	ALL	$V_{IN} = 0V$	−250	−250	−250	−250	−250	−250	µA
I_{INH}	ALL	$V_{IN} = 5V$		10	20		10	20	µA
DYNAMIC									
t_{on}	10Ω Switches	See switching time test circuit		300			350		ns
	30Ω Switches			150			180		
	75Ω Switches			250			300		
t_{off}	10Ω Switches			250			300		
	30Ω and 75Ω Switches			130			150		
$C_{S(off)}$	DG181, 182, 184, 185, 187, 188, 190, 191 (DG180, 183, 186 189)	$V_S = -5V$, $I_D = 0$, f = 1MHz	9 typical (21 typical)						pF
$C_{D(off)}$		$V_D = +5V$, $I_S = 0$, f = 1MHz	6 typical (17 typical)						
$C_{D(on)} + C_{S(on)}$		$V_D = V_S = 0$, f = 1MHz	14 typical (17 typical)						
OFF Isolation		$R_L = 75Ω$, $C_L = 3pF$	Typically > 50dB at 10MHz (See Note 2)						
SUPPLY									
I^+	DG180, 181, 182, 189 190, 191	$V_{IN} = 5V$		1.5			1.5		mA
	DG183, 184, 185			0.1			0.1		
	DG186, 187, 188			0.8			0.8		
I^-	DG180, 181, 182, 189 190, 191			−5.0			−5.0		
	DG183, 184, 185			−4.0			−4.0		
	DG186, 187, 188			−3.0			−3.0		
I_L	DG180, 181, 182, 183 184, 185, 189, 190, 191			4.5			4.5		
	DG186, 187, 188			3.2			3.2		
I_{GND}	ALL			−2.0			−2.0		
I^+	DG180, 181, 182, 189 190, 191	$V_{IN} = 0V$		1.5			1.5		
	DG183, 184, 185			3.0			3.0		
	DG186, 187, 188			0.8			0.8		
I^-	DG180, 181, 182, 189 190, 191			−5.0			−5.0		
	DG183, 184, 185			−5.5			−5.5		
	DG186, 187, 188			−3.0			−3.0		
I_L	DG180, 181, 182, 183 184, 185, 189, 190, 191			4.5			4.5		
	DG186, 187, 188			3.2			3.2		
I_{GND}	ALL			−2.0			−2.0		

NOTES 1. See Switching State Diagrams for V_{IN} "ON" and V_{IN} "OFF" Test Conditions.
2. Off Isolation typically > 55dB at 1MHz for DG180, 183, 186, 189.
3. Saturation Drain Current for DG180, 183, 186, 189 only, typically 300mA (2ms Pulse Duration). Maximum Current on all other devices (any terminal) 30mA.

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS MAXIMUM RESISTANCES ($r_{DS(ON)}$ MAX) (Continued)

Device Number	Conditions (Note 1) $V^+ = 15V, V^- = -15V, V_L = 5V$		Military Temperature			Industrial Temperature			Units
			−55°C	+25°C	+125°C	−20°C	+25°C	+85°C	
DG180	$V_D = -7.5V$		10	10	20	15	15	25	Ω
DG181	$V_D = -7.5V$		30	30	60	50	50	75	Ω
DG182	$V_D = -10V$		75	75	100	100	100	150	Ω
DG183	$V_D = -7.5V$		10	10	20	15	15	25	Ω
DG184	$V_D = -7.5V$		30	30	60	50	50	75	Ω
DG185	$V_D = -10V$	$I_S = -10mA$	75	75	150	100	100	150	Ω
DG186	$V_D = -7.5V$		10	10	20	15	15	25	Ω
DG187	$V_D = -7.5V$	V_{IN} = "ON"	30	30	60	50	50	75	Ω
DG188	$V_D = -10V$		75	75	150	100	100	150	Ω
DG189	$V_D = -7.5V$		10	10	20	15	15	25	Ω
DG190	$V_D = -7.5V$		30	30	60	50	50	50	Ω
DG191	$V_D = -10V$		75	75	150	100	100	150	Ω

APPLICATION HINT (for design only): Normally the minimum signal handling capability of the DG180 through DG191 family is 20V peak-to-peak for the 75Ω switches and 15V peak-to-peak for the 10Ω and 30Ω (refer I_D and I_S tests above). For other Analog Signals, the following guidelines can be used: proper switch turn-off requires that $V^- \leq V_{ANALOG}(peak) - V_p$ where $V_p = 7.5V$ for the 10Ω AND 30Ω switches and $V_p = 5.0V$ for 75Ω switches e.g., −10V minimum (−peak) analog signal and a 75Ω switch (Vp = 5V), requires that $V^- \leq -10V - 5V = -15V$.

Logic Input for "OFF" to "ON" Condition (DG180/181/182 Shown)

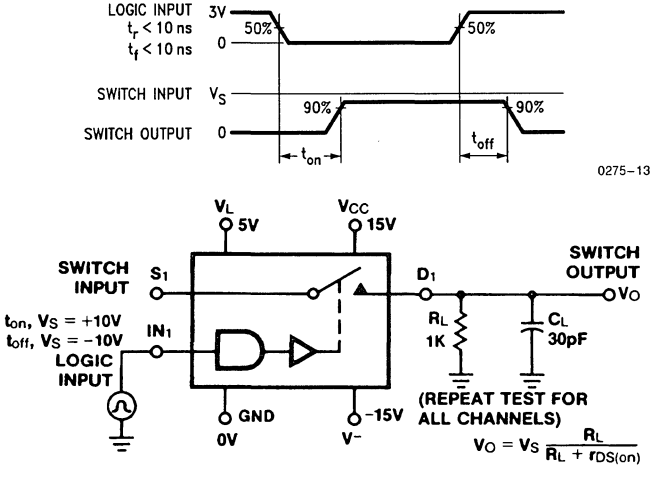


Figure 3: Switching Time Test Circuits

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

NOTE: All typical values have been characterized but are not tested.

DUAL SPST - DG180/181/182

TEST CONDITIONS

DG180/181/182	
V_{IN} "ON" = 0.8V	All Channels
V_{IN} "OFF" = 2.0V	All Channels

SWITCH STATES ARE
FOR LOGIC "1" INPUT = 2.0V

DUAL DPST - DG183/184/185

TEST CONDITIONS

DG183/184/185	
V_{IN} "ON" = 2.0V	All Channels
V_{IN} "OFF" = 0.8V	All Channels

SWITCH STATES ARE
FOR LOGIC "1" INPUT = 2.0V

SPDT - DG186/187/188

TEST CONDITIONS

DG186/187/188	
V_{IN} "ON" = 2.0V	Channel 1
V_{IN} "ON" = 0.8V	Channel 2
V_{IN} "OFF" = 2.0V	Channel 2
V_{IN} "OFF" = 0.8V	Channel 1

SWITCH STATES ARE
FOR LOGIC "1" INPUT = 2.0V

DUAL SPDT - DG189/190/191

TEST CONDITIONS

DG189/190/191	
V_{IN} "ON" = 2.0V	Channels 1 & 2
V_{IN} "ON" = 0.8V	Channels 3 & 4
V_{IN} "OFF" = 2.0V	Channels 3 & 4
V_{IN} "OFF" = 0.8V	Channels 1 & 2

SWITCH STATES ARE
FOR LOGIC "1" INPUT = 2.0V

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

DG200
CMOS Dual SPST Analog Switches

GENERAL DESCRIPTION

The DG200 solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. They provide ease-of-use and performance advantages not previously available from solid state switches. Destructive latch-up of solid state analog gates has been eliminated by HARRIS's CMOS technology.

The DG200 is completely spec and pin-out compatible with the industry standard device.

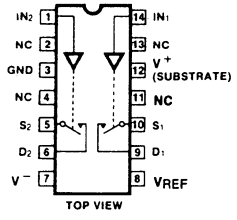
FEATURES

- **Switches Greater Than 28Vpp Signals With ± 15V Supplies**
- **Break-Before-Make Switching t_{off} 250ns, t_{on} 700ns Typical**
- **TTL, DTL, CMOS, PMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **Complete Monolithic Construction**
- **Industry Standard (DG200)**

ORDERING INFORMATION

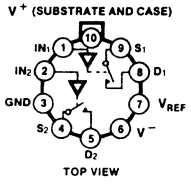
Industry Standard Part	Package	Temperature Range
DG200AA	10-Pin Metal Can	−55°C to +125°C
DG200AK	14-Pin CERDIP	−55°C to +125°C
DG200AL	14-Pin Flat Pak	−55°C to +125°C
DG200BA	10-Pin Metal Can	−25°C to +85°C
DG200BK	14-Pin CERDIP	−25°C to +85°C
DG200BL	14-Pin Flat Pak	−25°C to +85°C
DG200CJ	14-Pin Epoxy Dip	0°C to +70°C

CERDIP & EPOXY DUAL-IN-LINE PACKAGE (outline dwgs JD, PD)



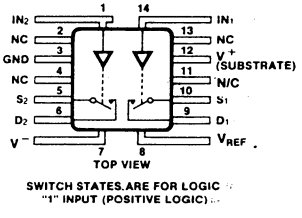
0276-1

METAL CAN PACKAGE (outline dwg TO-100)



0276-2

FLAT PACKAGE (outline dwg FD-2)



SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

0276-3

Figure 1: Pin Configurations

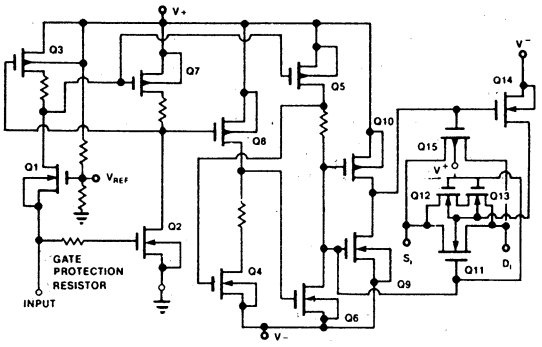
NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V^+-V^- ..... <36V
V^+-V_D ..... <30V
V_D-V^- ..... <30V
V_D-V_S ..... <28V
V_{IN}-GND ..... <20V
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation 450mW

(All Leads Soldered to a P.C. Board.) Derate 6mW/°C Above 75°C.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*



0276-4

Figure 2: Functional Diagram (1/2 DG200)

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = +15V, V^- = −15V)

Per Channel		Test	Min/Max Limits						Units
			Military			Comℓ/Industrial			
Symbol	Characteristic	Conditions	−55°C	+25°C	+125°C	0/−25°C	+25°C	+70°C/+85°C	
$I_{IN(ON)}$	Input Logic Current	V_{IN} = 0.8V See Notes 2, 3	±10	±1	±10		±10	±10	μA
$I_{IN(OFF)}$	Input Logic Current	V_{IN} = 2.4V See Notes 2, 3	±10	±1	±10		±10	±10	μA
$r_{DS(ON)}$	Drain-Source On Resistance	I_S = 10mA V_{ANALOG} = ±10V	70	70	100	80	80	100	Ω
$r_{DS(ON)}$	Channel-to-Channel $r_{DS(ON)}$ Match			25 (typ)			30 (typ)		Ω
V_{ANALOG}	Min. Analog Signal Handling Capability			±15			±15		V
$I_{D(OFF)}$	Switch OFF Leakage Current	V_{ANALOG} = −14V to +14V		±2	100		±5	100	nA
$I_{S(OFF)}$	Switch OFF Leakage Current	V_{ANALOG} = −14V to +14V		±2	100		±5	100	nA

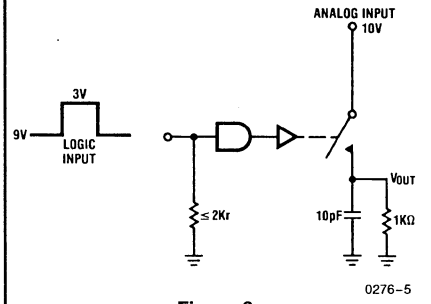
NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$, $V^+ = +15V$, $V^- = -15V$) (Continued)

Per Channel		Test Conditions	Min/Max Limits						Units
			Military			Com'l/Industrial			
Symbol	Characteristic		−55°C	+25°C	+125°C	0/−25°C	+25°C	+70°C/+85°C	
$I_{D(ON)} + I_{S(ON)}$	Switch ON Leakage Current	$V_D = V_S = -14V$ to $+14V$		±2	200		±10	200	nA
t_{on}	Switch "ON" Time See Note 1	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to $+10V$ See Fig. 3		1.0			1.0		µs
t_{off}	Switch "OFF" Time	$R_L = 1k\Omega$, $V_{ANALOG} = -10V$ to $+10V$ See Fig. 3		0.5			0.5		µs
$Q_{(INJ.)}$	Charge Injection	See Fig. 4		15 (typ)			20 (typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	$f = 1MHz$, $R_L = 100\Omega$, $C_L \leq 5pF$ See Fig. 5 (Note 1)		54 (typ)			50 (typ)		dB
I_{V1}	+ Power Supply Quiescent Current	$V_{IN} = 0V$ or $V_{IN} = 5V$	1000	1000	2000	1000	1000	2000	µA
I_{V2}	−Power Supply Quiescent Current		1000	1000	2000	1000	1000	2000	µA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off		54 (typ)			50 (typ)		dB

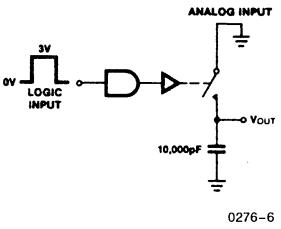
NOTE 1: Pull Down Resistor must be ≤ 2kΩ
2: Typical values are for design aid only, not guaranteed and not subject to production testing.

TEST CIRCUITS



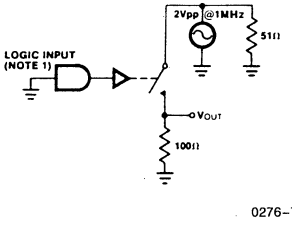
0276-5

Figure 3



0276-6

Figure 4



0276-7

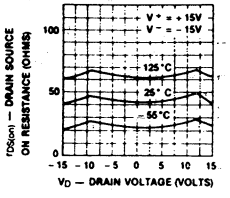
Figure 5

NOTE 3: All channels are turned off by high "1" logic inputs and all channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Peak input current required for transition is typically −120µA.

NOTE: All typical values have been characterized but are not tested.

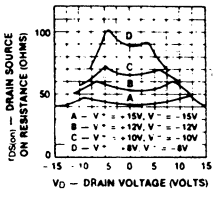
TYPICAL PERFORMANCE CHARACTERISTICS

$r_{DS(on)}$ vs V_D and Temperature



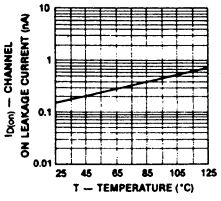
0276-8

$r_{DS(on)}$ vs V_D and Power Supply Voltage



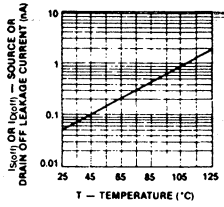
0276-9

$I_{D(on)}$ vs Temperature*



0276-10

$I_{S(off)}$ or $I_{D(off)}$ vs Temperature*



0276-11

APPLICATIONS

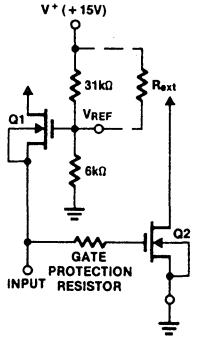
Using the V_{REF} Terminal

The DG200 has an internal voltage divider setting the TTL threshold on the input control lines for V^+ equal to +15V. The schematic shown here with nominal resistor values, gives approximately 2.4V on the V_{REF} pin. As the TTL input signal goes from +0.8V to +2.4V, Q1 and Q2 switch states to turn the switch ON and OFF.

If the power supply voltage is less than +15V, then a resistor must be added between V^+ and the V_{REF} pin, to restore +2.4V at V_{REF}. The table shows the value of this resistor for various supply voltages, to maintain TTL compatibility. If CMOS logic levels on a +5V supply are being used, the threshold shifts are less critical, but a separate column of suitable values is given in the table. For logic swings of −5V to +5V, no resistor is needed.

In general, the "low" logic level should be <0.8V to prevent Q1 and Q2 from both being ON together (this will cause incorrect switch function). With open collector logic, and a low value of pull-up resistor, the logic "low" level can be above 0.8V. In this case, HARRIS can supply parts with thresholds >1.5V, allowing the user to define the "low" as <1.5V (consult factory). The V_{REF} point should be set at least 2.6V above this "low" state, or to >4.1V. An external resistor of 27kΩ between V^+ and V_{REF} is required, for a +15V supply.

V^+ Supply (V)	TTL Resistor (kΩ)	CMOS Resistor (kΩ)
+15	–	–
+12	100	–
+10	51	–
+9	(34)	34
+8	(27)	27
+7	18	18



0276-12

Figure 6.

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

DG201
Quad SPST CMOS Analog Switch

GENERAL DESCRIPTION

The DG201 solid-state analog switches are designed using an improved, high-voltage CMOS monolithic technology. They provide performance advantages not previously available from solid-state switches. Destructive latch-up of solid-state analog gates has been eliminated by HARRIS's CMOS technology.

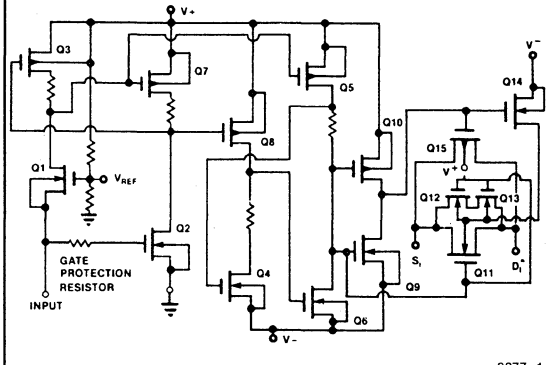
The DG201 is completely specification and pin-out compatible with the industry standard device.

FEATURES

- **Switches Greater Than $28V_{p-p}$ Signals With ±15V Supplies**
- **Break-Before-Make Switching t_{off} = 250ns, t_{on} = Typically 500ns**
- **TTL, DTL, CMOS, PMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **Complete Monolithic Construction**
- **Industry Standard (DG201)**

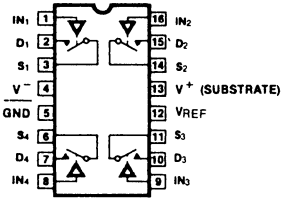
ORDERING INFORMATION

Industry Standard Part Number	Temperature Range	Package
DG201AK	−55°C to +125°C	16-Pin CERDIP
DG201BK	−25°C to +85°C	16-Pin CERDIP
DG201CJ	0°C to +70°C	16-Pin Plastic DIP



0277-1

Figure 1: Functional Diagram (¼ DG201) Switch Open For Logic "1" Input



0277-2

Figure 2: Pin Configuration (Outline dwgs JE, PE) DUAL-IN-LINE PACKAGE

7

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- ..... <36V
V^+ to V_D ..... <30V
V_D to V^- ..... <30V
V_D to V_S ..... <28V
V_{REF} to V^- ..... <33V
V_{REF} to V_{IN} ..... <30V
V_{REF} to GND ..... <20V

V_{IN} to GND ..... <20V
Current (Any Terminal) ..... <30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation 450mW
Derate 6mW/°C Above 70°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

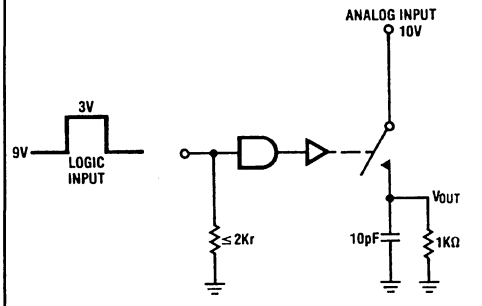
DG201 ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = +15V, V^- = −15V)

Per Channel		Test Conditions	Min/Max Limits						Units
			Military			Commercial			
Symbol	Characteristic		−55°C	+25°C	+125°C	0°C	+25°C	+70°C/+85°C	
$I_{IN(ON)}$	Input Logic Current	V_{IN} = 0.8V See Note 1	10	±1	10	±1	±1	10	µA
$I_{IN(OFF)}$	Input Logic Current	V_{IN} = 2.4V See Note 1	10	±1	10	±1	±1	10	µA
$R_{DS(ON)}$	Drain-Source On Resistance	I_S = 10mA V_{ANALOG} = ±10V	80	80	125	100	100	125	Ω
$R_{DS(ON)}$	Channel to Channel $R_{DS(ON)}$ Match			25 (typ)			30 (typ)		Ω
V_{ANALOG}	Analog Signal Handling Capability			±15 (typ)			±15 (typ)		V
$I_{D(OFF)}$	Switch OFF Leakage Current	V_{ANALOG} = −14V to +14V		±1	100		±5	100	nA
$I_{S(OFF)}$	Switch OFF Leakage Current	V_{ANALOG} = −14V to +14V		±1	100		±5	100	nA
$I_{D(ON)}$ + $I_{S(ON)}$	Switch ON Leakage Current	V_D = V_S = ±14V		±2	200		±5	200	nA
t_{on}	Switch "ON" Time See Note 2	R_L = 1kΩ, V_{ANALOG} = −10V to +10V See Figure 3		1.0			1.0		µs
t_{off}	Switch "OFF" Time See Note 2	R_L = 1kΩ, V_{ANALOG} = −10V to +10V See Figure 3		0.5			0.5		µs
$Q_{(INJ.)}$	Charge Injection	See Figure 4		15 (typ)			20 (typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	f = 1MHz, R_L = 100Ω, C_L ≤ 5pF See Figure 5		54 (typ)			50 (typ)		dB
I^+_Q	+ Power Supply Quiescent Current	V_{IN} = 0V to 5V	2000	1000	2000	2000	1000	2000	µA
I^-_Q	−Power Supply Quiescent Current		2000	1000	2000	2000	1000	2000	µA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off		54 (typ)			50 (typ)		dB

NOTE 1: Typical values are for design aid only, not guaranteed and not subject to production testing.

NOTE: All typical values have been characterized but are not tested.

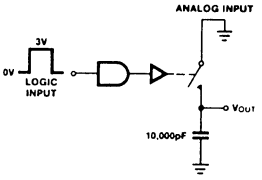
TEST CIRCUITS



0277-3

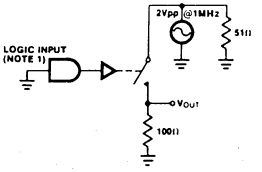
(Note 2)

Figure 3



0277-4

Figure 4

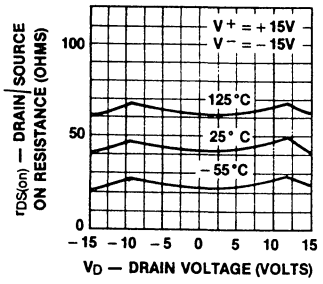


0277-5

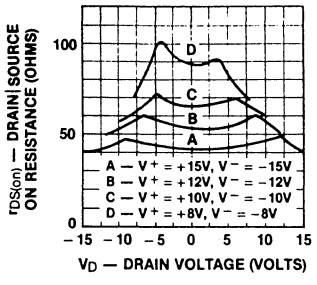
Figure 5

NOTE 2: All channels are turned off by high "1" logic inputs and all channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Peak input current required for transition is typically −120μA. Pull down resistor, if used, ≤ 2KΩ.

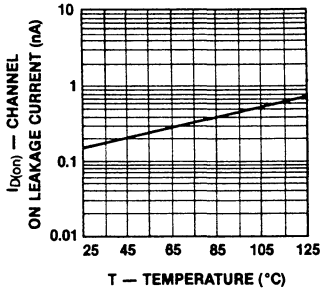
TYPICAL PERFORMANCE CHARACTERISTICS



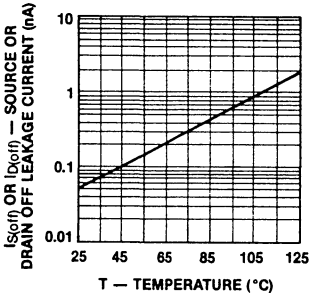
0277-6



0277-7



0277-8



0277-9

NOTE: All typical values have been characterized but are not tested.

APPLICATIONS

Using the V_{REF} Terminal

The DG201 has an internal voltage divider that sets the TTL threshold on the input control lines for $V+ = 15V$. The schematic is shown here, with nominal resistor values, giving approximately 2.4V on the V_{REF} pin. As the TTL input signal goes from +0.8V to +2.4V, Q1 and Q2 switch states to turn the switch ON and OFF.

If the power supply voltage is less than +15V, then a resistor needs to be added between $V+$ and V_{REF} pin, to restore +2.4V at V_{REF}. The table shows the value of this resistor for various supply voltages, to maintain TTL compatibility. If CMOS logic levels with a +5V supply are being used, the threshold shifts are less critical, but a separate column of suitable values is given in the table. For logic swings of −5V to +5V, no resistor is needed.

In general, the "low" logic level should be <0.8V to prevent Q1 and Q2 from both being ON together (this will cause incorrect switch function). With open collector logic, and a low value of pull-up resistor, the logic 'low' level can be above 0.8V. In this case, HARRIS can supply parts with thresholds >1.5V(consult factory). The V_{REF} point should be set at least 2.6V above this "low" state, or to >4.1V. An external resistor of 27kΩ and V_{REF} is required, for a +15V supply.

V+ Supply (V)	TTL Resistor (kΩ)	CMOS Resistor (kΩ)
+15	–	–
+12	100	–
+10	51	–
+9	(34)	34
+8	(27)	27
+7	18	18

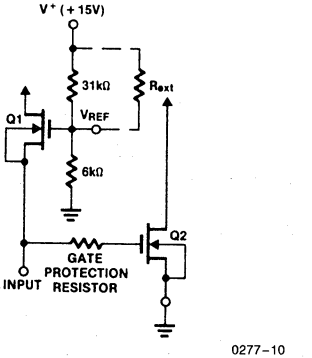


Figure 6

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

DG201A/DG202
Quad Monolithic SPST CMOS Analog Switches

GENERAL DESCRIPTION

The DG201A (normally open) and DG202 (normally closed) quad SPST analog switches are designed using Harris' new 44V CMOS process. These bidirectional switches are latch-proof and feature break-before-make switching. Designed to block signals up to 30V peak-to-peak in the OFF state, the DG201A/DG202 offer the advantages of low on resistance ($\leq 175\Omega$), wide input signal range (± 15V) and provide both TTL and CMOS compatibility.

The DG201A/DG202 are specification and pin-out compatible with the industry standard devices.

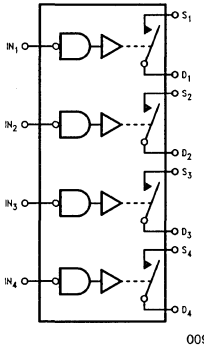
FEATURES

- **± 15V Input Signal Range**
- **Low $R_{DS(on)}$ ($\leq 175\Omega$)**
- **TTL, CMOS Compatible**
- **Latch Proof**
- **True Second Source**
- **44V Maximum Supply Ratings**
- **Logic Inputs Accept Negative Voltages**

ORDERING INFORMATION

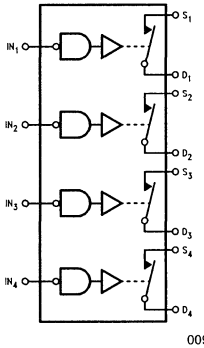
Part Number	Temperature Range	Package
DG201AAK	−55°C to +125°C	16-Pin CERDIP
DG201ABK	−25°C to +85°C	16-Pin CERDIP
DG201ACK	0°C to +70°C	16-Pin CERDIP
DG201ACJ	0°C to +70°C	16-Pin Plastic DIP
DG202AK	−55°C to +125°C	16-Pin CERDIP
DG202BK	−25°C to +85°C	16-Pin CERDIP
DG202CK	0°C to +70°C	16-Pin CERDIP
DG202CJ	0°C to +70°C	16-Pin Plastic DIP

DG201A



0096-1

DG202



0096-2

Four SPST Switches Per Package*

Truth Table

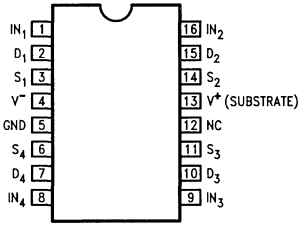
Logic	DG201A	DG202
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8V
Logic "1" ≥ 2.4V

*Switches Shown for Logic "1" Input

Figure 1: Functional Diagram

Dual-In-Line Package



0096-3

Top View

Figure 2: Pin Configuration

307010-001

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- 44V
V^- to Ground ..... −25V
V_{in} to Ground (Note 1) ..... (V^- − 2V), (V^+ + 2V)
V_S or V_D to V^+ (Note 1) ..... +2, (V^- − 2V)
V_S or V_D to V^- (Note 1) ..... −2, (V^+ + 2V)
Current, Any Terminal Except S or D ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) ..... 70 mA
Operating Temperature
C Suffix ..... 0°C to +70°C
B Suffix ..... −25°C to +85°C
A Suffix ..... −55°C to +125°C

Storage Temperature
C Suffix ..... −65°C to +125°C
A & B Suffix ..... −65°C to +150°C
Lead Temperature (Soldering, 10s) ..... 300°C
Power Dissipation*
CERDIP Package** ..... 900 mW
Plastic Package*** ..... 470 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C
***Derate 6.5 mW/°C above 25°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS $V^+ = 15V, V^- = -15V, GND = 0V, T_A = 25°C$

Symbol	Parameter	Test Conditions		DG201AA/DG202A			DG201AB, C/DG202B, C			Units
				Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
SWITCH										
V_{ANALOG}	Analog Signal Range			−15		15	−15		15	V
$R_{DS(on)}$	Drain Source On Resistance	$V_D = \pm 10V$, $V_{in} = 0.8V$ (DG201A) $I_S = 1$ mA, $V_{in} = 2.0V$ (DG202)			115	175		115	200	Ω
$I_{S(off)}$	Source OFF Leakage Current	$V_{in} = 2.4V$ (DG201A) $V_{in} = 0.8V$ (DG202)	$V_S = 14V, V_D = -14V$		0.01	1.0		0.01	5.0	nA
			$V_S = -14V, V_D = 14V$	−1.0	−0.02		−5.0	−0.02		
$I_{D(off)}$	Drain OFF Leakage Current		$V_S = -14V, V_D = 14V$		0.01	1.0		0.01	5.0	nA
			$V_S = 14V, V_D = -14V$	−1.0	−0.02		−5.0	−0.02		
$I_{D(on)}$ (Note 4)	Drain ON Leakage Current	$V_{in} = 0.8V$ (DG201A) $V_{in} = 2.4V$ (DG202)	$V_D = V_S = 14V$		0.1	1.0		0.1	5.0	μA
			$V_D = V_S = -14V$	−1.0	−0.15		−5.0	−0.15		
INPUT										
I_{INH}	Input Current with Voltage High	$V_{in} = 2.4V$		−1.0	−0.0004		−1.0	−0.0004		μA
		$V_{in} = 15V$			0.003	1.0		0.003	1.0	
I_{INL}	Input Current with Voltage Low	$V_{in} = 0V$		−1.0	−0.0004		−1.0	−0.0004		μA

NOTE 1: Signals on V_S, V_D, or V_{in} exceeding V^+ or V^- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

2: Typical values are for design aid only, not guaranteed and not subject to production testing.

3: The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.

4: $I_{D(on)}$ is leakage from driver into ON switch.

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS $V^+ = 15V, V^- = -15V, GND = 0V, T_A = 25°C$ (Continued)

Symbol	Parameter	Test Conditions	DG201AA/DG202A			DG201AB, C/DG202B, C			Units
			Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
DYNAMIC									
t_{on}	Turn-ON Time	See Figure 3		480	600		480	600	ns
t_{off}	Turn-OFF Time			370	450		370	450	ns
Q	Charge Injection	C_L = 1000 pF, R_S = 0, V_S = 0V		20			20		pC
$C_{S(off)}$	Source OFF Capacitance	f = 140 kHz, V_{in} = 5V, V_S = 0V		5.0			5.0		pF
$C_{D(off)}$	Drain OFF Capacitance	f = 140 kHz, V_{in} = 5V, V_D = 0V		5.0			5.0		pF
$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	f = 140 kHz, V_{in} = 0V, $V_S = V_D$ = 0V		16			16		pF
DIRR	OFF Isolation	V_{in} = 5V, Z_L = 75Ω, V_S = 2.0V, f = 100 kHz		70			70		dB
CCRR	Crosstalk (Channel to Channel)			90			90		
SUPPLY									
I^+	Positive Supply Current	All Channels ON or OFF		0.9	2		0.9	2	mA
I^-	Negative Supply Current		−1	−0.3		−1	−0.3		mA
T_A = over operating temperature range									
SWITCH									
V_{ANALOG}	Analog Signal Range		−15		15	−15		15	V
$R_{DS(on)}$	Drain-Source ON Resistance	V_D = ±10V, V_{in} = 0.8V (DG201A) I_S = 1 mA, V_{in} = 2.4V (DG202)			250			250	Ω
$I_{S(off)}$	Source OFF Leakage Current	V_{in} = 2.4V (DG201A) V_{in} = 0.8V (DG202) V_S = 14V, V_D = −14V			100			100	nA
		V_S = −14V, V_D = 14V	−100			−100			
$I_{D(off)}$	Drain OFF Leakage Current	V_S = −14V, V_D = 14V			100			100	nA
		V_S = 14V, V_D = −14V	−100			−100			
$I_{D(on)}$ (Note 4)	Drain ON Leakage Current	V_{in} = 0.8V (DG201A) $V_D = V_S$ = 14V			200			200	µA
		V_{in} = 2.4V (DG202) $V_D = V_S$ = −14V	−200			−200			
INPUT									
I_{INH}	Input Current with Voltage High	V_{in} = 2.4V	−10			−10			µA
		V_{in} = 15V			10			10	
I_{INL}	Input Current with Voltage Low	V_{in} = 0V	−10			−10			µA

NOTE 1: Signals on V_S, V_D, or V_{in} exceeding V^+ or V^- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

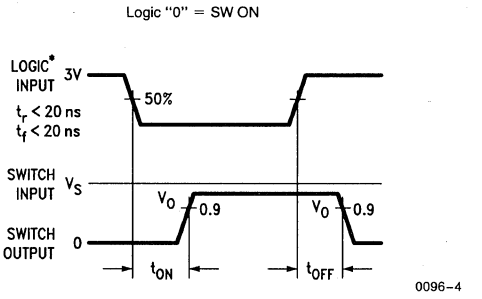
2: Typical values are for design aid only, not guaranteed and not subject to production testing.

3: The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.

4: $I_{D(on)}$ is leakage from driver into ON switch.

NOTE: All typical values have been characterized but are not tested.

TEST CIRCUITS



*Logic Shown for DG201A, Invert for DG202.

$$V_O = V_S \frac{R_L}{R_L + R_{DS(on)}}$$

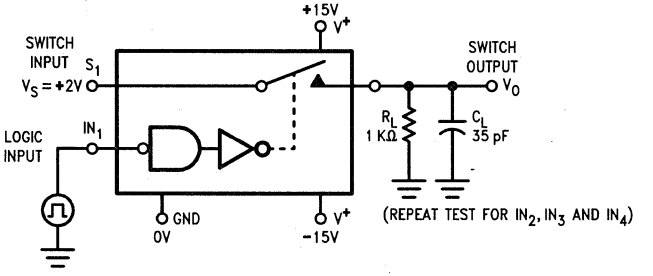
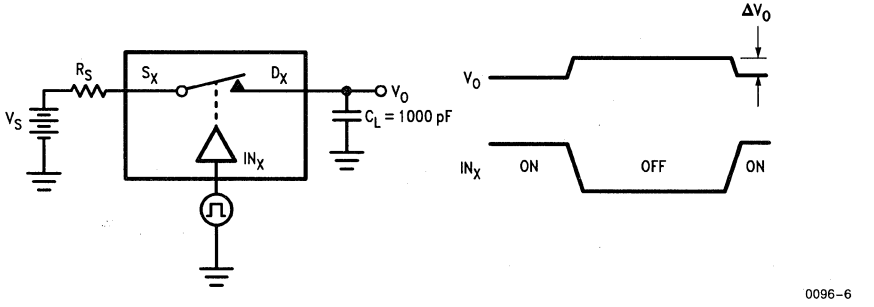


Figure 3: t_{on} and t_{off} Switching Test



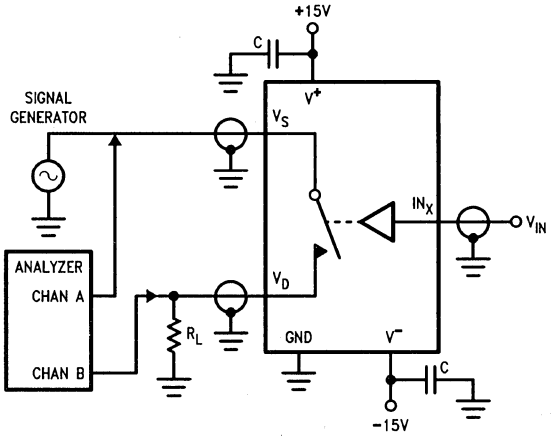
ΔV_O = measured voltage error due to charge injection

The error voltage in coulombs is $\Delta Q = C_L = \Delta V_O$.

Figure 4: Charge Injection Test Circuit

NOTE: All typical values have been characterized but are not tested.

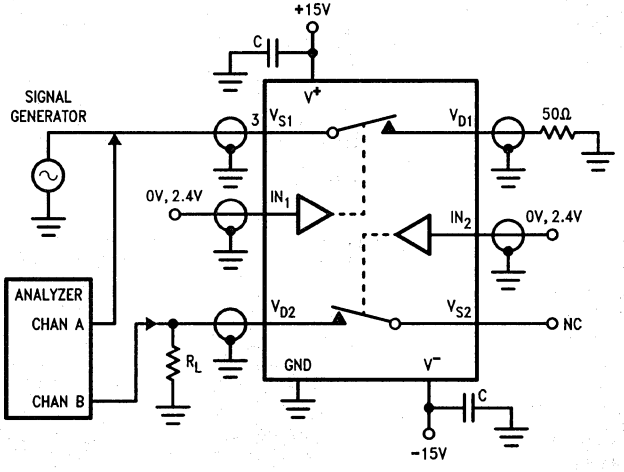
TEST CIRCUITS (Continued)



C = 0.001 µF // 0.1 µF
Chip Capacitors

$$DIRR = 20 \text{ Log} \left| \frac{V_S}{V_D} \right|$$

Figure 5: Off Isolation Test Circuit



C = 0.001 µF // 0.1 µF
Chip Capacitors

$$DIRR = 20 \text{ Log} \left| \frac{V_{S1}}{V_{D2}} \right|$$

Figure 6: Channel to Channel Crosstalk Test Circuit

7

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

DG211/DG212
SPST 4-Channel Analog Switch

GENERAL DESCRIPTION

The DG211 and DG212 are low cost, CMOS monolithic, QUAD SPST analog switches. These can be used in general purpose switching applications for communications, instrumentation, process control and computer peripheral equipment. Both devices provide true bidirectional performance in the ON condition and will block signals to 30V peak-to-peak in the OFF condition. The DG211 and DG212 differ only in that the digital control logic is inverted, as shown in the truth table.

DG211 and DG212 are available in 16-pin Dual-In-Line plastic packages or 16-pin small outline packages and are rated for operation over 0°C to 70°C.

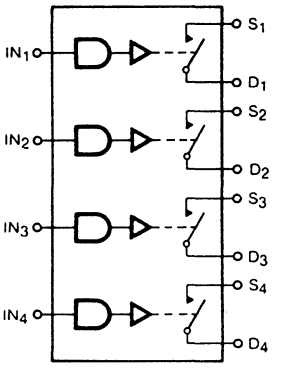
FEATURES

- **Switches ±15V Analog Signals**
- **TTL Compatibility**
- **Logic Inputs Accept Negative Voltages**
- **$R_{ON} \leq 175$ Ohm**

ORDERING INFORMATION

Part Number	Temperature Range	Package
DG211CJ	0°C to +70°C	16-Pin Plastic DIP
DG212CJ	0°C to +70°C	16-Pin Plastic DIP
DG211CY	0°C to +70°C	16-Pin SOIC
DG212CY	0°C to +70°C	16-Pin SOIC

DG211



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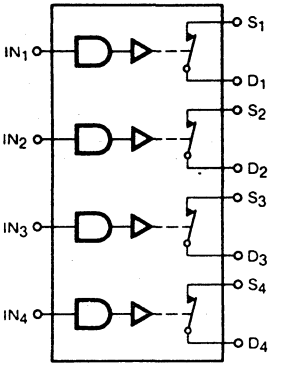
DG212



0278-2

Four SPST Switches per Package
Switches Shown for Logic "1" Input

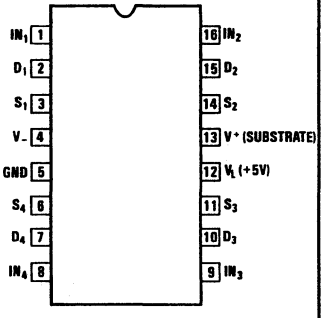
Truth Table

Logic	DG211	DG212
0	ON	OFF
1	OFF	ON

Logic "0" ≤ 0.8V
Logic "1" ≥ 2.4V

Figure 1: Functional Diagrams

Dual-In-Line or S.O. Package



0278-3

TOP VIEW

Figure 2: Pin Configuration

307020-002

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- 44V
V_{IN} to Ground ..... V^-, V^+
V_L to Ground ..... −0.3V, 25V
V_S or V_D to V^+ ..... 0, −36V
V_S or V_D to V^- 0, 36V
V^+ to Ground 25V
V^- to Ground ..... −25V
Current, Any Terminal Except S or D 30mA
Continuous Current, S or D 20mA
Peak Current, S or D
(Pulsed at 1msec, 10% duty cycle max) 70mA
Storage Temperature ..... −65°C to +125°C
Operating Temperature ..... 0°C to +70°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation (Package)*
16 Pin Plastic DIP** 470mW

* Device mounted with all leads soldered or welded to PC board.
** Derate 6.5mW/°C above 25°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Test Conditions V_1 = +15V, V_2 = −15V, V_L = +5V, GND		Limits MIN[1]	Limits TYP[2]	Limits MAX	Units
SWITCH							
V_{ANALOG}	Analog Signal Range	V^- = −15V, V_L = +5V		−15		15	V
$R_{DS(ON)}$	Drain-Source On Resistance	V_D = ±10V, V_{IN} = 2.4V — DG212 I_S = 1mA, V_{IN} = 0.8V — DG211			150	175	Ω
$I_{S(off)}$	Source OFF Leakage Current	V_{IN} = 2.4V DG211 V_{IN} = 0.8V DG212	V_S = 14V, V_D = −14V		0.01	5.0	nA
			V_S = −14V, V_D = 14V	−5.0	−0.02		
$I_{D(off)}$	Drain OFF Leakage Current		V_D = 14V, V_S = −14V		0.01	5.0	
			V_D = −14V, V_S = 14V	−5.0	−0.02		
$I_{D(ON)}$	Drain ON Leakage Current[3]	V_S = V_D = −14V, V_{IN} = 0.8V, DG211 V_{IN} = 2.4V, DG212			0.1	5.0	
				−5.0	−0.15		
INPUT							
I_{INH}	Input Current With Input Voltage High	V_{IN} = 2.4V		−1.0	−0.0004		μA
		V_{IN} = 15V			0.003	1.0	
I_{INL}	Input Current With Input Voltage Low	V_{IN} = 0V		−1.0	−0.0004		
DYNAMIC							
t_{on}	Turn-ON Time	See Switching Time Test Circuit[5] V_S = 10V, R_L = 1kΩ, C_L = 35pF			460	1000	ns
t_{off1}	Turn-OFF Time				360	500	
t_{off2}					450		
$C_{S(off)}$	Source OFF Capacitance	V_S = 0V, V_{IN} = 5V, f = 1MHz[2]			5		pF
$C_{D(off)}$	Drain OFF Capacitance	V_D = 0V, V_{IN} = 5V, f = 1MHz[2]			5		
$C_{D+S(on)}$	Channel ON Capacitance	V_D = V_S = 0V, V_{IN} = 0V, f = 1MHz[2]			16		
OIRR	OFF Isolation[4]	V_{IN} = 5V, R_L = 1kΩ, C_L = 15pF, V_S = 1VRMS, f = 100kHz[2]			70		dB
CCRR	Crosstalk (Channel to Channel)				90		
SUPPLY							
I^+	Positive Supply Current	V_{IN} = 0 and 2.4V			0.1	10	μA
I^-	Negative Supply Current				0.1	10	
I_L	Logic Supply Current				0.1	10	

NOTES: **1.** The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
2. For design reference only, not 100% tested.
3. $I_{D(on)}$ is leakage from driver into "ON" switch.
4. OFF Isolation = $20\log\frac{V_S}{V_D}$, V_S = input to OFF switch, V_D = output.
5. Switching times only sampled.

NOTE: All typical values have been characterized but are not tested.

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note the V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

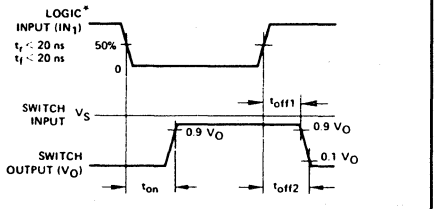


Figure 3: Switching Time Test Circuit
Logic shown for DG211. Invert for DG212.

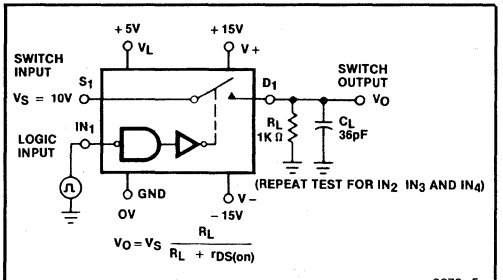


Figure 4: Switching Time Test Circuit

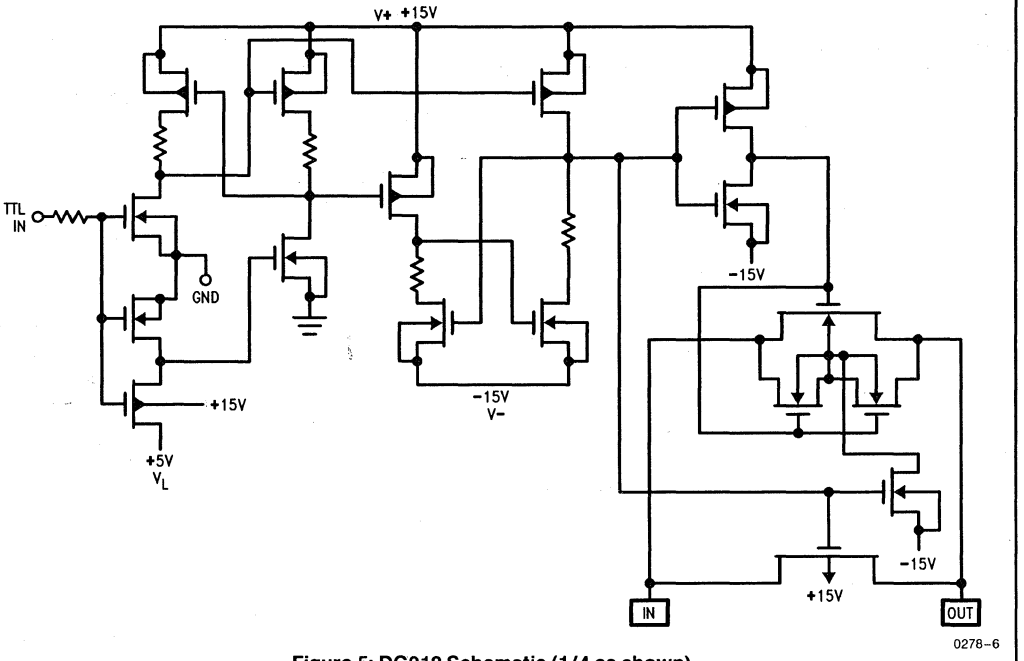


Figure 5: DG212 Schematic (1/4 as shown)

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

DG300A/DG301A/ DG302A/DG303A
TTL Compatible CMOS Analog Switches

GENERAL DESCRIPTION

The DG300A–303A family of monolithic CMOS switches are a truly compatible second source of the original manufacturer. The switches are latch-proof and are designed to block signals up to 30 volts peak-to-peak when OFF. Featuring low leakage and low power consumption, these switches are ideally suited for precision application in instrumentation, communication, data acquisition and battery-powered applications. Other key features include Break-Before-Make switching, TTL and CMOS compatibility, and low ON resistance. Single supply operation (for positive switch voltages) is possible by connecting V^- to 0 volts.

The DG300A–DG303A family is available over commercial, industrial, and military temperature range.

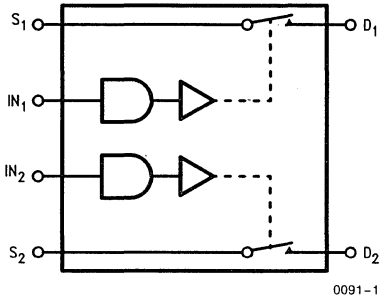
FEATURES

- **Low Power Consumption**
- **Break-Before-Make Switching t_{off} 130 ns, t_{on} 150 ns Typical**
- **TTL, CMOS Compatible**
- **Low $R_{DS(on)}$ ($\leq 50\Omega$)**
- **Single Supply Operation**
- **True Second Source**

ORDERING INFORMATION

Part Number	Temperature Range	Package
DG300A/301A/ 302A/303AAK	-55°C to +125°C	14-Pin CERDIP
DG300A/301A/ 302A/303ABK	-25°C to +85°C	14-Pin CERDIP
DG300A/301A/ 302A/303ACK	0°C to +70°C	14-Pin CERDIP
DG300A/301A/ 302A/303ACJ	0°C to +70°C	14-Pin Plastic DIP
DG300A/301AAA	-55°C to +125°C	10-Pin Metal Can
DG300A/301ABA	-25°C to +85°C	10-Pin Metal Can
DG303ACY	0°C to +70°C	16-Pin SOIC

DG300A



Two SPST Switches per Package*

Truth Table

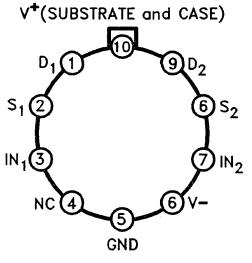
Logic	Switch
0	OFF
1	ON

Logic "0" ≤ 0.8V
Logic "1" ≥ 4.0V

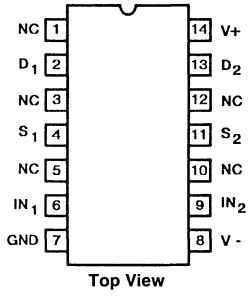
*Switches Shown for Logic "1" Input

Figure 1: Functional Diagrams

Metal Can Package



Dual-In-Line Package



16 Lead SOIC
TOP VIEW

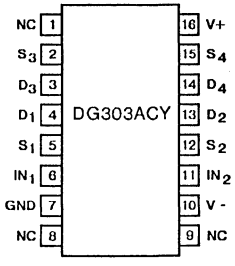


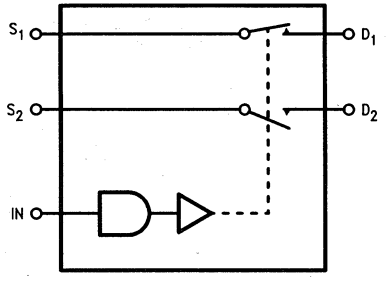
Figure 2: Pin Configurations

307025-001

NOTE: All typical values have been characterized but are not tested.

DG300A/DG301A/DG302A/DG303A

DG301A



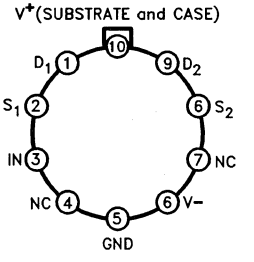
0091-4

One SPDT Switch per Package*

Truth Table**

Logic	SW1	SW2
0	OFF	ON
1	ON	OFF

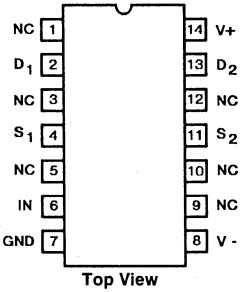
Metal Can Package



0091-5

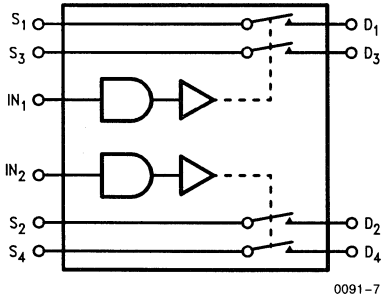
Top View

Dual-In-Line Package



Top View

DG302A



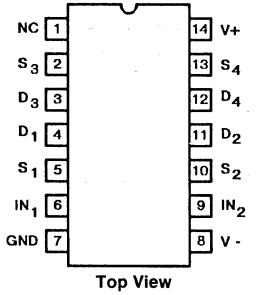
0091-7

Two DPST Switches per Package*

Truth Table**

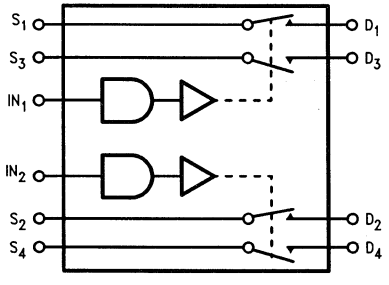
Logic	Switch
0	OFF
1	ON

Dual-In-Line Package



Top View

DG303A



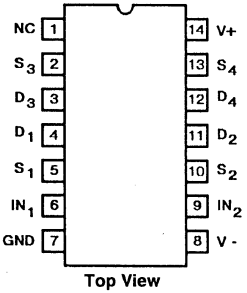
0091-9

Two SPDT Switches per Package*

Truth Table**

Logic	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

Dual-In-Line Package



Top View

*Switches Shown for Logic "1" Input
**Logic "0" ≤ 0.8V, Logic "1" ≥ 4.0V

Figure 1: Functional Diagrams (Continued)

Figure 2: Pin Configurations (Continued)

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- 44V
V^- to Ground ..... −25V
V_{IN} to Ground (Note 1) ..... (V^- − 2V), (V^+ + 2V)
V_S or V_D to V^+ (Note 1) ..... +2, (V^- − 2V)
V_S or V_D to V^- (Note 1) ..... −2, (V^+ + 2V)
Current, Any Terminal Except S or D ..... 30 mA
Continuous Current, S or D ..... 30 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) ..... 100 mA
Operating Temperature
C Suffix ..... 0°C to +70°C
B Suffix ..... −25°C to +85°C
A Suffix ..... −55°C to +125°C
Storage Temperature
C Suffix ..... −65°C to +125°C
A & B Suffix ..... −65°C to +150°C
Lead Temperature (Soldering, 10s) ..... 300°C
Power Dissipation*
CERDIP Package** ..... 825 mW
Plastic Package*** ..... 470 mW
Metal Can**** ..... 450 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 11 mW/°C above 75°C
***Derate 6.5 mW/°C above 25°C
****Derate 6 mW/°C above 75°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS $V^+ = 15V, V^- = -15V, GND = 0V, T_A = 25°C$

Symbol	Parameter	Test Conditions		DG300A–DG303AA			DG300A–DG303AB/C			Units
				Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
SWITCH										
V_{ANALOG}	Analog Signal Range	I_S = 10 mA, V_{IN} = 0.8V or 4V		−15		15	−15		15	V
$R_{DS(on)}$	Drain-Source ON Resistance	V_{IN} = 0.8V or V_{IN} = 4.0V	I_S = −10 mA, V_D = 10V		30	50		30	50	Ω
			I_S = 10 mA, V_D = −10V		30	50		30	50	
$I_{S(off)}$	Source OFF Leakage Current		V_S = 14V, V_D = −14V		0.1	1		0.1	5	nA
			V_S = −14V, V_D = 14V	−1	−0.1		−5	−0.1		
$I_{D(off)}$	Drain OFF Leakage Current		V_S = −14V, V_D = 14V		0.1	1		0.1	5	nA
			V_S = 14V, V_D = −14V	−1	−0.1		−5	−0.1		
$I_{D(on)}$	Drain ON Leakage Current		V_D = V_S = 14V		0.1	1		0.1	5	nA
			V_D = V_S = −14V	−2	−0.1		−5	−0.1		
INPUT										
I_{INH}	Input Current w/Voltage High	V_{IN} = 5.0V		−1	−0.001		−1	−0.001		μA
		V_{IN} = 15V			0.001	1		0.001	1	
I_{INL}	Input Current w/Voltage Low	V_{IN} = 0V		−1	−0.001		−1	−0.001		μA
DYNAMIC										
t_{on}	Turn-ON Time	See Figure 5			150	300		150		ns
t_{off}	Turn-OFF Time				130	250		130		ns
$t_{on}-t_{off}$	Break-Before-Make Interval	See Figure 4 DG301A/303A			50			50		ns
Q	Charge Injection	C_L = 1 μF, R_S = 0, V_S = 0			3			3		mV
$C_{S(off)}$	Source OFF Capacitance	f = 1 MHz, V_{IN} = 0.8V or V_{IN} = 4.0V	V_S = 0		14			14		pF
$C_{D(off)}$	Drain OFF Capacitance		V_D = 0		14			14		pF
$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		V_S = V_D = 0		40			40		pF

NOTE: All typical values have been characterized but are not tested.

DG300A/DG301A/DG302A/DG303A

ELECTRICAL CHARACTERISTICS $V^+ = 15V, V^- = -15V, GND = 0V, T_A = 25°C$ (Continued)

Symbol	Parameter	Test Conditions		DG300A–DG303AA Min	DG300A–DG303AA Typ (Note 2)	DG300A–DG303AA Max	DG300A–DG303AB/C Min	DG300A–DG303AB/C Typ (Note 2)	DG300A–DG303AB/C Max	Units
DYNAMIC (Continued)										
C_{IN}	Input Capacitance	f = 1 MHz	V_{IN} = 0		6			6		pF
			V_{IN} = 15V		7			7		
DIRR (Note 4)	OFF Isolation	V_{IN} = 0, R_L = 1k			62			62		dB
CCRR	Crosstalk (Channel to Channel)	$V_S = 1V_{RMS}$, f = 500 kHz			74			74		
SUPPLY										
I^+	Positive Supply Current	V_{IN} = 4V (One Input) (All Others = 0)			0.23	0.5		0.23	0.5	mA
I^-	Negative Supply Current			−10	−0.001		−10	−0.001		µA
I^+	Positive Supply Current	V_{IN} = 0.8V (All Inputs)			0.001	10		0.001	10	µA
I^-	Negative Supply Current			−10	−0.001		−10	−0.001		µA

T_A = over operating temperature range

Symbol	Parameter	Test Conditions		DG300A–DG303AA Min	DG300A–DG303AA Typ (Note 2)	DG300A–DG303AA Max	DG300A–DG303AB/C Min	DG300A–DG303AB/C Typ (Note 2)	DG300A–DG303AB/C Max	Units
SWITCH										
V_{ANALOG}	Analog Signal Range	I_S = 10 mA, V_{IN} = 0.8V or 4V		−15		15	−15		15	V
$R_{DS(on)}$	Drain-Source ON Resistance	V_{IN} = 0.8V or V_{IN} = 4.0V	I_S = −10 mA, V_D = 10V			75			75	Ω
			I_S = 10 mA, V_D = −10V			75			75	
$I_{S(off)}$	Source OFF Leakage Current		V_S = 14V, V_D = −14V			100			100	nA
			V_S = −14V, V_D = 14V	−100			−100			
$I_{D(off)}$	Drain OFF Leakage Current		V_S = −14V, V_D = 14V			100			100	nA
			V_S = 14V, V_D = −14V	−100			−100			
$I_{D(on)}$	Drain ON Leakage Current		$V_D = V_S$ = 14V			100			100	nA
			$V_D = V_S$ = −14V	−200			−200			
INPUT										
I_{INH}	Input Current w/Voltage High	V_{IN} = 5.0V		−1						µA
		V_{IN} = 15V				1				
I_{INL}	Input Current w/Voltage Low	V_{IN} = 0V		−1						µA
SUPPLY										
I^+	Positive Supply Current	V_{IN} = 4V (One Input) (All Others = 0)				1				mA
I^-	Negative Supply Current			−100						µA
I^+	Positive Supply Current	V_{IN} = 0.8V (All Inputs)				100				µA
I^-	Negative Supply Current			−100						µA

NOTE 1: Signals on V_S, V_D, or V_{IN} exceeding V^+ or V^- will be clamped by internal diodes. Limit diode forward current to maximum current ratings.

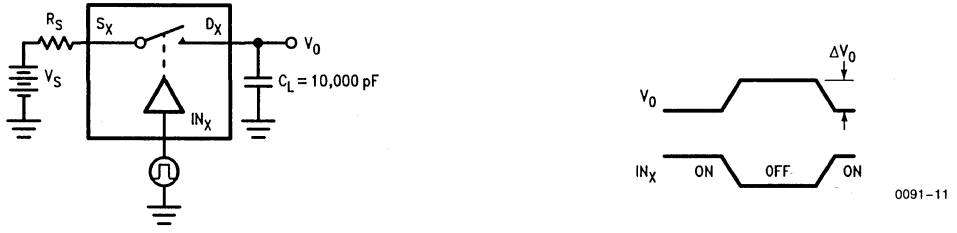
2: For design only, not 100% tested.

3: The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

4: OFF isolation = 20 log V_S/V_D, where V_S = input to OFF switch, and V_D = output.

NOTE: All typical values have been characterized but are not tested.

SWITCHING INFORMATION



ΔV_O Δ Measured Voltage Error Due to Charge Injection.

The Error Voltage in Coulombs is $\Delta Q = C_L \times \Delta V_O$.

Figure 3: Charge Injection Test Circuit

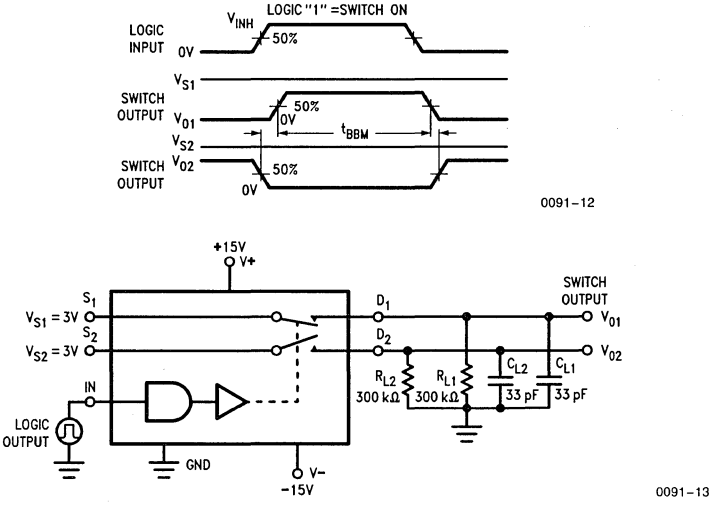


Figure 4: Break-Before-Make Switching Test SPDT (DG301A, DG303A)

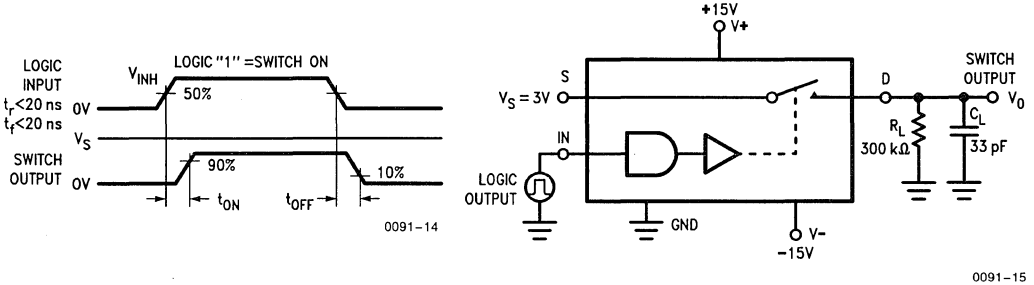


Figure 5: t_{on} and t_{off} Switching Test

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

DG308A/DG309
Quad Monolithic SPST CMOS Analog Switches

GENERAL DESCRIPTION

The DG308A/DG309 quad monolithic SPST CMOS switches are latch-proof and are designed to block signals up to 30 volts peak-to-peak when OFF. Featuring low ON resistance, low power consumption, and rail-to-rail analog signal range, these switches are ideally suited for high speed switching applications in communications, instrumentation and process control. The DG308A "normally-closed" and DG309 "normally-open" switches have single and dual supply capability. The input thresholds are CMOS compatible.

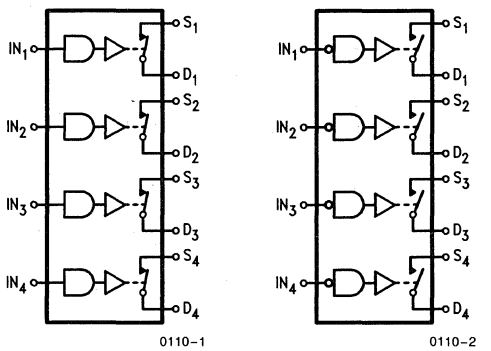
The DG308A/DG309 switches are available over commercial, industrial, and military temperature ranges.

FEATURES

- **Low Power Consumption**
- **CMOS Compatible**
- **±15V Analog Signal Range**
- **Single or Dual Supply Capability**
- **Alternate Source**

ORDERING INFORMATION

Part Number	Temperature Range	Package
DG308AAK/309AK	−55°C to +125°C	16-Pin CERDIP
DG308ABK/309BK	−25°C to +85°C	16-Pin CERDIP
DG308ACK/309CK	0°C to +70°C	16-Pin CERDIP
DG308ACJ/309ACJ	0°C to +70°C	16-Pin Plastic DIP
DG308ACY/309CY	0°C to +70°C	16-Pin SOIC



Four SPST Switches Per Package

Truth Table

Logic	DG308A	DG309
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 3.5V
Logic "1" ≥ 11V

Switches Shown for Logic "1" Input

Figure 1: Functional Diagrams

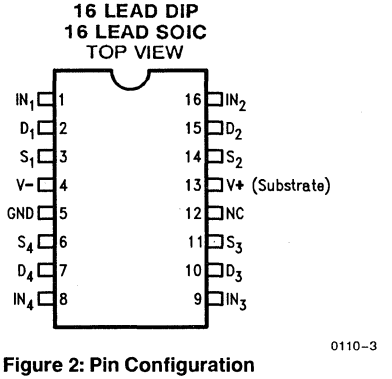


Figure 2: Pin Configuration

307035-003

NOTE: All typical values have been characterized but are not tested.

DG308A/DG309

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- 44V
V^- to Ground ..... −25V
V_{in} to Ground (Note 1) ..... (V^- − 2V), (V^+ + 2V)
V_S or V_D to V^+ (Note 1) ..... +2, (V^- − 2V)
V_S or V_D to V^- (Note 1) ..... −2, (V^+ + 2V)
Current, Any Terminal Except S or D ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) ..... 70 mA
Operating Temperature
C Suffix ..... 0°C to +70°C
B Suffix ..... −25°C to +85°C
A Suffix ..... −55°C to +125°C
Storage Temperature
C Suffix ..... −65°C to +125°C
A & B Suffix ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Power Dissipation*
CERDIP Package** ..... 900 mW
Plastic Package*** ..... 470 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C
***Derate 6.5 mW/°C above 25°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS $V^+ = 15V, V^- = -15V, GND = 0V, T_A = 25°C$

Symbol	Parameter	Test Conditions		DG308AA, DG309A			DG308AB/C, DG309B/C			Units
				Min	Typ(Note 2)	Max	Min	Typ(Note 2)	Max	
SWITCH										
V_{ANALOG}	Analog Signal Range			−15		15	−15		15	V
$R_{DS(on)}$	Drain-Source ON Resistance	V_{in} = 11V (DG308A)	I_S = −1 mA, V_D = −10V		60	100		60	100	Ω
			I_S = 1 mA, V_D = −10V		60	100		60	100	
$I_{D(on)}$	Drain ON Leakage Current	V_{in} = 3.5V (DG309)	$V_D = V_S$ = 14V		0.1	1		0.1	5	nA
			$V_D = V_S$ = −14V	−2	−0.1		−5	−0.1		
$I_{S(off)}$	Source OFF Leakage Current	V_{in} = 3.5V (DG308A)	V_S = 14V, V_D = −14V		0.1	1		0.1	5	nA
			V_S = −14V, V_D = 14V	−1	−0.1		−5	−0.1		
$I_{D(off)}$	Drain OFF Leakage Current	V_{in} = 11V (DG309)	V_S = −14V, V_D = 14V		0.1	1		0.1	5	nA
			V_S = 14V, V_D = −14V	−1	−0.1		−5	−0.1		
INPUT										
I_{INH}	Input Current w/ Voltage High	V_{in} = 15V			0.001	1		0.001	1	μA
I_{INL}	Input Current w/Voltage Low	V_{in} = 0V		−1	−0.001		−1	−0.001		μA
DYNAMIC										
t_{on}	Turn-ON Time	See Figure 4			130	200		130	200	ns
t_{off}	Turn-OFF Time				90	150		90	150	ns
Q	Charge Injection	C_L = 1 μF, R_S = 0, V_S = 0			−10			−10		pC
$C_{S(off)}$	Source OFF Capacitance	f = 140 kHz	V_S = 0 V_{in} = 0V (DG308A V_{in} = 15V (DG309)		11			11		pF
$C_{D(off)}$	Drain OFF Capacitance		V_D = 0 V_{in} = 0V (DG308A) V_{in} = 15V (DG309)		8			8		pF
$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		$V_S = V_D$ = 0 V_{in} = 15V (DG308A) V_{in} = 0V (DG309)		27			27		pF
OIRR (Note 4)	OFF Isolation	V_{in} = 0V (DG308A) V_{in} = 15V (DG309) Z_L = 75Ω, V_S = $2V_{p-p}$ f = 500 kHz			78			78		dB

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS $V^+ = 15V, V^- = -15V, GND = 0V, T_A = 25°C$

Symbol	Parameter	Test Conditions	DG308AA, DG309A			DG308AB/C, DG309B/C			Units
			Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
SUPPLY									
I^+	Positive Supply Current	All Channels "ON" or "OFF" V_{in} = 0V or 15V		0.001	10		0.001	100	μA
I^-	Negative Supply Current		−10	−0.001		−100	−0.001		μA

T_A = over operating temperature range

Symbol	Parameter	Test Conditions		DG308AA, DG309A			DG308AB/C, DG309B/C			Units
				Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
SWITCH										
V_{ANALOG}	Analog Signal Range			−15		15	−15		15	V
$R_{DS(on)}$	Drain-Source ON Resistance	V_{in} = 11V (DG308A)	I_S = −1 mA, V_D = 10V			150			125	Ω
			I_S = 1 mA, V_D = −10V			150			125	
$I_{D(on)}$	Drain ON Leakage Current	V_{in} = 3.5V (DG309)	$V_D = V_S$ = 14V			100			200	nA
			$V_D = V_S$ = −14V	−200			−200			
$I_{S(off)}$	Source OFF Leakage Current	V_{in} = 3.5V (DG308A)	V_S = 14V, V_D = −14V			100			100	nA
			V_S = −14V, V_D = 14V	−100			−100			
$I_{D(off)}$	Drain OFF Leakage Current	V_{in} = 11V (DG309)	V_S = −14V, V_D = 14V			100			100	nA
			V_S = 14V, V_D = −14V	−100			−100			
INPUT										
I_{INH}	Input Current w/ Voltage High	V_{in} = 15V				1			1	μA
I_{INL}	Input Current w/Voltage Low	V_{in} = 0V		−1			−1			μA
SUPPLY										
I^+	Positive Supply Current	V_{in} = 0V or 15V				100			100	μA
I^-	Negative Supply Current			−100			−100			μA

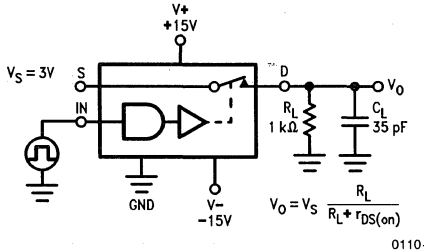
NOTES 1: Signals on V_S, V_D or V_{in} exceeding V^+ or V^- will be clamped by internal diodes. Limit diode forward current to maximum current ratings.

2: Typical values are for design aid only, not guaranteed and not subject to production testing.

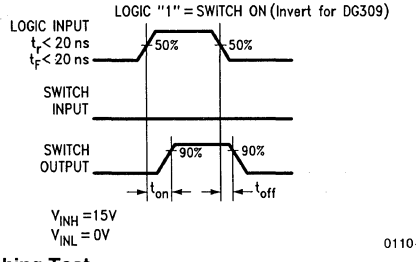
3: The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

4: OFF isolation = 20 log V_D/V_S, where V_S = input to OFF switch, and V_D = output.

SWITCHING INFORMATION



0110-4



0110-5

Figure 3: t_{on} and t_{off} Switching Test

NOTE: All typical values have been characterized but are not tested.

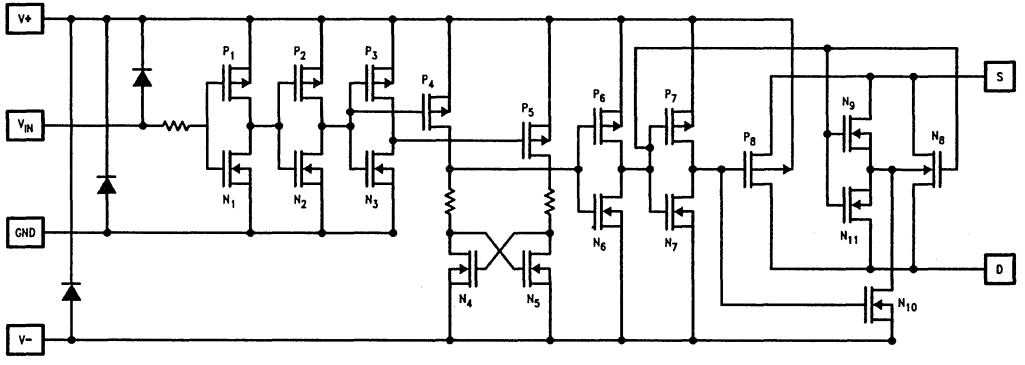


Figure 4: DG308A Schematic Diagram (One Channel)

NOTE: All typical values have been characterized but are not tested.

HARRIS

HI-200

Dual SPST CMOS Analog Switch

Features

- Analog Voltage Range ..... ±15V
- Analog Current Range 80mA
- Turn-On Time 240ns
- Low R_{ON} 55Ω
- Low Power Dissipation 15mW
- TTL/CMOS Compatible

Applications

- High Frequency Analog Switching
- Sample and Hold Circuits
- Digital Filters
- Operational Amplifier Gain Switching Networks

Description

HI-200 is a monolithic device comprising two independently selectable SPST switches which feature fast switching speeds (240ns) combined with low power dissipation (15mW at +25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and CMOS processing, HI-200 operates without any applications problems induced by latch-up or SCR mode phenomena.

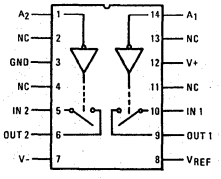
All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-200 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters, and op amp gain switching networks.

HI-200 is available in DIP and (TO-99) Metal Cans. HI-200-2 is specified from -55°C to +125°C while HI-200-5 operates from 0°C to +75°C. HI-200 is functionally and pin compatible with other available "200 series" switches.

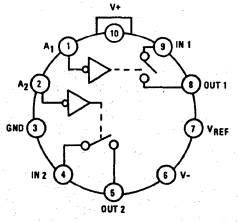
Pinouts

TOP VIEWS

HI-200 DIP, SOIC
TOP VIEW

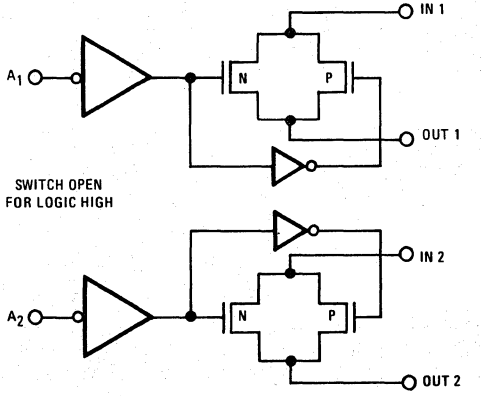


HI2-0200
TOP VIEW



CASE TIED TO V-

Functional Diagram



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI2-0200-5	0°C to +75°C	10-Pin Metal Can
HI1-0200-5	0°C to +75°C	14-Pin CERDIP
HI2-0200-4	-25°C to +85°C	10-Pin Metal Can
HI3-0200-5	0°C to +75°C	14-Pin Plastic DIP
HI2-0200-7	0°C to +75°C + 96 Hr. Burn-In	10-Pin Metal Can
HI1-0200-7	0°C to +75°C + 96 Hr. Burn-In	14-Pin CERDIP
HI1-0200-2	-55°C to +125°C	14-Pin CERDIP
HI1-0200-4	-25°C to +85°C	14-Pin CERDIP
HI2-0200-2	-55°C to +125°C	10-Pin Metal Can

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Specifications HI-200

Absolute Maximum Ratings

Supply Voltage ..... 44V (±22)
V_{REF} to Ground ..... +20V, -5V
Digital Input Voltage ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Analog Input Voltage (One Switch) ..... $+V_{SUPPLY}$ +2.0V
$-V_{SUPPLY}$ -2.0V
Total Power Dissipation* 450mW

Operating Temperature Range

HI-200-2 ..... -55°C to +125°C
HI-200-4 ..... -25°C to +85°C
HI-200-5 ..... 0°C to +75°C
Storage Temperature ..... -65°C to +150°C

*Derate 6mW/°C Above T_A = +75°C

Electrical Specifications Unless Otherwise Specified: Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V

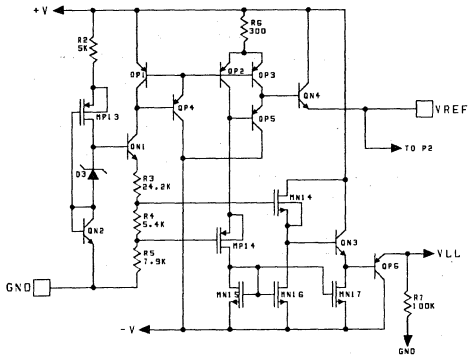
PARAMETER	TEMP	HI-200-2 -55°C to +125°C MIN	TYP	MAX	HI-200-5** 0°C to +75°C MIN	TYP	MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15	-	+15	-15	-	+15	V
R_{ON}, On Resistance (Note 1)	+25°C	-	55	70	-	55	80	Ω
	Full	-	80	100	-	72	100	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 6)	+25°C	-	1	5	-	1	50	nA
	Full	-	100	500	-	10	500	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 6)	+25°C	-	1	5	-	1	50	nA
	Full	-	100	500	-	10	500	nA
$I_{D(ON)}$, On Leakage Current (Note 6)	+25°C	-	1	5	-	1	50	nA
	Full	-	100	500	-	10	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full	-	-	0.8	-	-	0.8	V
V_{AH}, Input High Threshold	Full	2.4	-	-	2.4	-	-	V
I_A, Input Leakage Current (High or Low) (Note 2)	Full	-	-	1.0	-	-	1.0	µA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break-Before Make Delay (Note 3)	+25°C	-	60	-	-	60	-	ns
t_{ON}, Switch On Time	+25°C	-	240	500	-	240	-	ns
t_{OFF}, Switch Off Time	+25°C	-	330	500	-	500	-	ns
"Off Isolation" (Note 4)	+25°C	-	70	-	-	70	-	dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C	-	5.5	-	-	5.5	-	pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C	-	5.5	-	-	5.5	-	pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C	-	11	-	-	11	-	pF
C_A, Digital Input Capacitance	+25°C	-	5	-	-	5	-	pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C	-	0.5	-	-	0.5	-	pF
POWER REQUIREMENTS (Note 5)								
P_D, Power Dissipation	+25°C	-	15	-	-	15	-	mW
	Full	-	-	60	-	-	60	mW
I^+, Current	+25°C	-	0.5	-	-	0.5	-	mA
	Full	-	-	2.0	-	-	2.0	mA
I^-, Current	+25°C	-	0.5	-	-	0.5	-	mA
	Full	-	-	2.0	-	-	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = 1mA
2. Digital Inputs are MOS gates — Typical Leakage is Less Than 1nA.
3. V_{AH} = 4.0V.
4. V_A = 5V, R_L = 1kΩ, C_L = 10pF, V_S = $3V_{RMS}$, f = 100kHz.
5. V_A = +3V or V_A = 0V for Both Switches.
6. Refer to Leakage Current Measurement Diagram on Page 3-8.

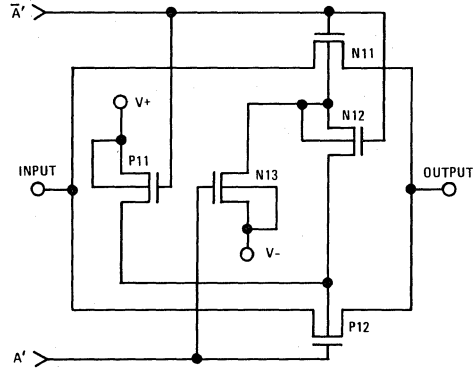
**NOTE: HI-200-4 Has Same Specifications as HI-200-5 Over the Temperature Range -20°C to +85°C.

Schematic Diagrams

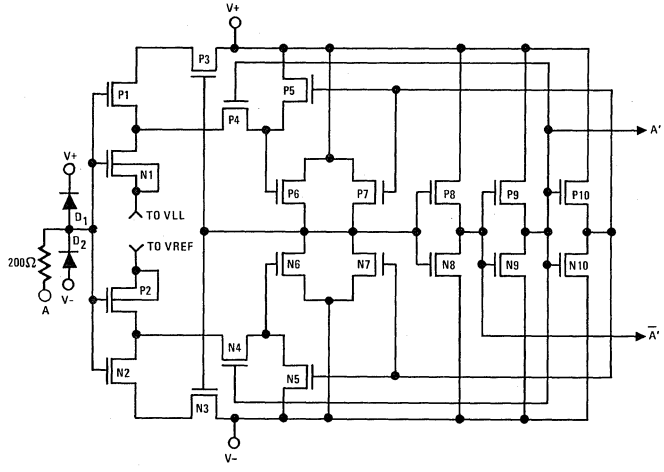
TTL/CMOS REFERENCE CIRCUIT
V-REF CELL



SWITCH CELL



DIGITAL INPUT BUFFER
AND LEVEL SHIFTER

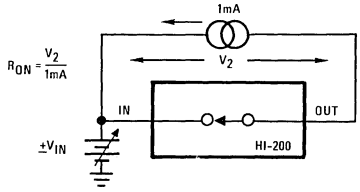


ALL N-CHANNEL BODIES TO V-
ALL P-CHANNEL BODIES TO V+
EXCEPT AS SHOWN.

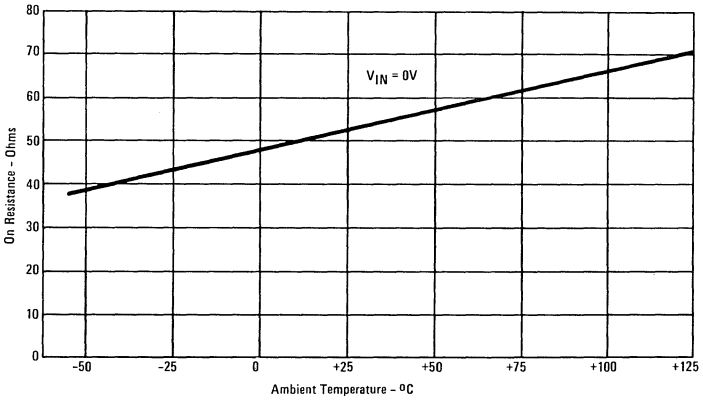
Performance Characteristics and Test Circuits

Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$ and V_{REF} = Open

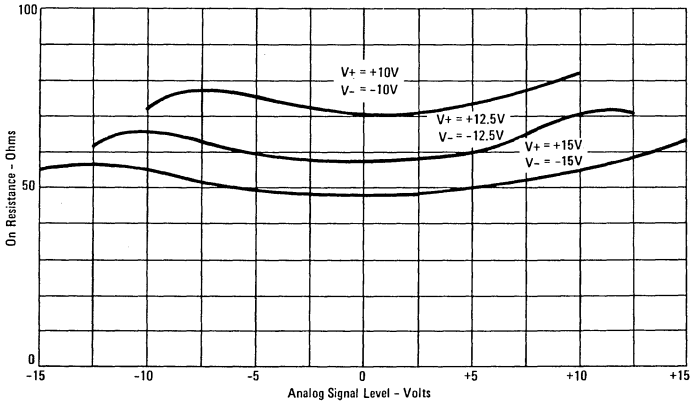
ON RESISTANCE vs. ANALOG SIGNAL LEVEL, SUPPLY VOLTAGE AND TEMPERATURE



ON RESISTANCE vs. TEMPERATURE

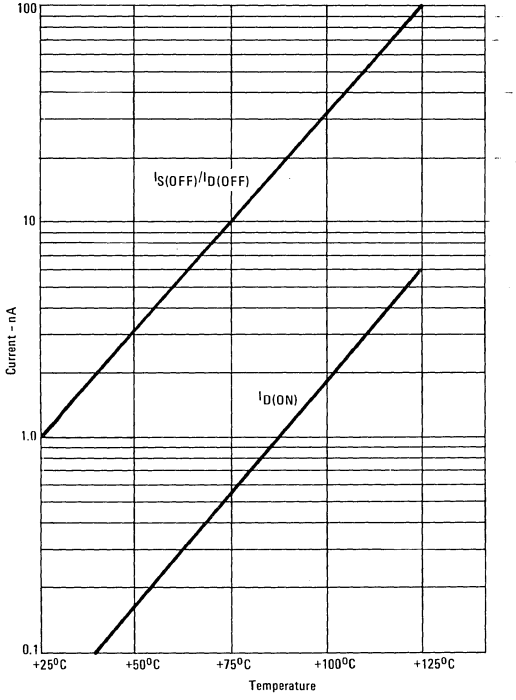


(HI-200)
ON RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

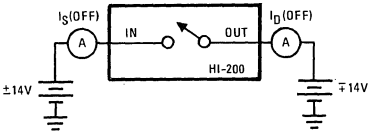


Performance Characteristics and Test Circuits (Continued)

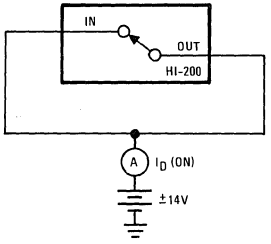
SWITCH LEAKAGE CURRENT vs. TEMPERATURE (HI-200)



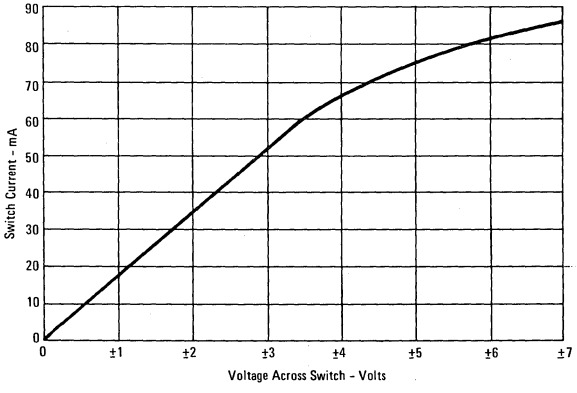
OFF LEAKAGE CURRENT vs. TEMPERATURE



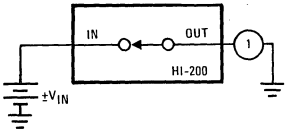
ON LEAKAGE CURRENT vs. TEMPERATURE



SWITCH CURRENT vs. VOLTAGE

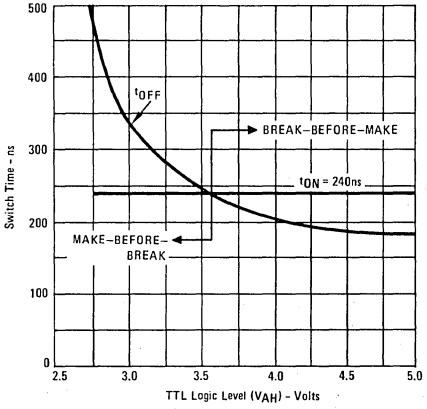


SWITCH CURRENT vs. VOLTAGE

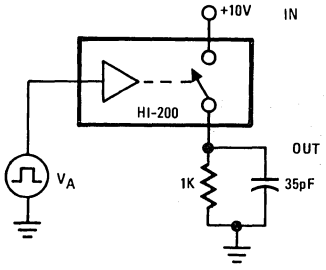


Performance Characteristics and Test Circuits (Continued)

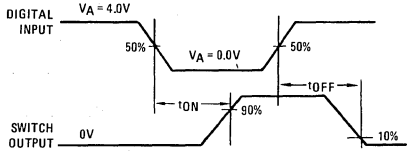
(HI-200)
SWITCH TIME vs. TTL LOGIC LEVEL



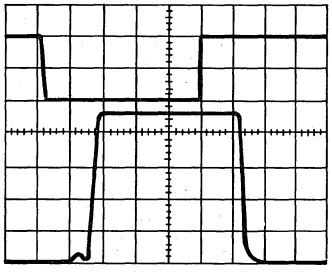
ON/OFF SWITCH TIME vs. LOGIC LEVEL



Switching Waveforms

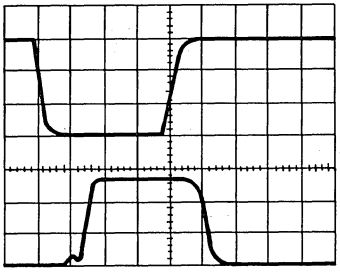


t_{ON}, t_{OFF} (TTL INPUT)
V_{AH} = +4.0V



TOP: TTL Input VERTICAL: 2V/Div.
BOTTOM: Output HORIZONTAL: 200ns/Div.

t_{ON}, t_{OFF} (CMOS INPUT)
V_{REF} = OPEN, V_{AH} = +15V



TOP: CMOS Input VERTICAL: 5V/Div.
BOTTOM: Output HORIZONTAL: 200ns/Div.

HARRIS

HI-201

September 1991

Quad SPST CMOS Analog Switch

Features

- Analog Voltage Range ..... ±15V
- Analog Current Range 80mA
- Turn-On Time 185ns
- Low R_{ON} 55Ω
- Low Power Dissipation 15mW
- TTL/CMOS Compatible

Applications

- High Frequency Analog Switching
- Sample and Hold Circuits
- Digital Filters
- Operational Amplifier Gain Switching Networks

Description

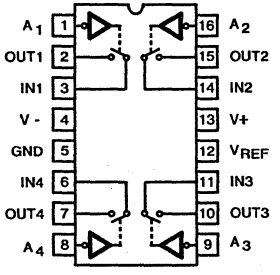
HI-201 is a monolithic device comprising four independently selectable SPST switches which feature fast switching speeds (185ns) combined with low power dissipation (15mW at +25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and CMOS processing, HI-201 operates without any applications problems induced by latch-up or SCR mode phenomena.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-201 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters, and op amp gain switching networks.

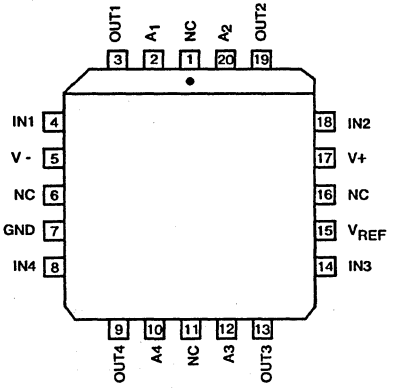
HI-201 is available in a 16 lead Dual-In-Line package. HI-201-2 is specified from -55°C to +125°C while HI-201-5 operates from 0°C to +75°C. HI-201 is functionally and pin compatible with other available "200 series" switches.

Pinouts

HI1-201-X
16 PIN DIP
TOP VIEW



HI-201
20 PIN PLCC, LCC
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0201-7	0°C to +75°C +96 Hr. Burn-In	16-Pin Ceramic DIP
HI1-0201-5	0°C to +75°C	16-Pin Ceramic DIP
HI1-0201-4	-25°C to +85°C	16-Pin Ceramic DIP
HI4P0201-5	0°C to +75°C	20-Pin PLCC
HI9P0201-5	0°C to +75°C	16-Pin SOIC
HI9P0201-9	-40°C to +85°C	16-Pin SOIC
HI1-0201-2	-55°C to +125°C	16-Pin Ceramic DIP
HI3-0201-5	0°C to +75°C	16-Pin Plastic DIP

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Specifications HI-201

Absolute Maximum Ratings

Supply Voltage Between Pins 4 and 13 ..... 44V (±22)
V_{REF} to Ground ..... +20V, -5V
Digital Input Voltage ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Analog Input Voltage (One Switch) ..... $+V_{SUPPLY}$ +2.0V
$-V_{SUPPLY}$ -2.0V
Analog Current — Continuous, Peak 30mA, 80mA
Total Dissipation* 750mW

Operating Temperature Range

HI-201-2 ..... -55°C to +125°C
HI-201-4 ..... -25°C to +85°C
HI-201-5 ..... 0°C to +75°C
Storage Temperature ..... -65°C to +150°C

*Derate 8mW/°C Above T_A = +75°C

Electrical Specifications Unless Otherwise Specified: Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V
For Test Conditions Consult Peformance Characteristics

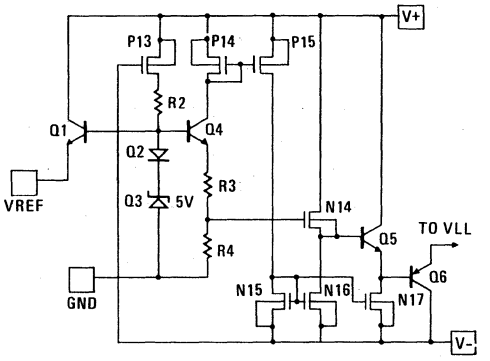
PARAMETER	TEMP	HI-201-2 -55°C to +125°C MIN	TYP	MAX	HI-201-5** 0°C to +75°C MIN	TYP	MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15	-	+15	-15	-	+15	V
R_{ON}, On Resistance (Note 1)	+25°C	-	55	70	-	55	80	Ω
	Full	-	80	100	-	75	100	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 6)	+25°C	-	2	5	-	2	50	nA
	Full	-	-	500	-	-	250	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 6)	+25°C	-	2	5	-	2	50	nA
	Full	-	35	500	-	35	250	nA
$I_{D(ON)}$, On Leakage Current (Note 6)	+25°C	-	2	5	-	2	50	nA
	Full	-	-	500	-	-	250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full	-	-	0.8	-	-	0.8	V
V_{AH}, Input High Threshold	Full	2.4	-	-	2.4	-	-	V
I_A, Input Leakage Current (High or Low) (Note 2)	Full	-	-	1.0	-	-	1.0	µA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break-Before Make Delay (Note 3)	+25°C	-	30	-	-	30	-	ns
t_{ON}, Switch On Time	+25°C	-	185	500	-	185	-	ns
	Full	-	1000	-	-	1000	-	ns
t_{OFF}, Switch Off Time	+25°C	-	220	500	-	220	-	ns
	Full	-	1000	-	-	1000	-	ns
"Off Isolation" (Note 4)	+25°C	-	80	-	-	80	-	dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C	-	5.5	-	-	5.5	-	pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C	-	5.5	-	-	5.5	-	pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C	-	11	-	-	11	-	pF
C_A, Digital Input Capacitance	+25°C	-	5	-	-	5	-	pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C	-	0.5	-	-	0.5	-	pF
POWER REQUIREMENTS (Note 5)								
P_D, Power Dissipation	+25°C	-	15	-	-	15	-	mW
	Full	-	-	60	-	-	60	mW
I^+, Current (Pin 13)	+25°C	-	0.5	-	-	0.5	-	mA
	Full	-	-	2.0	-	-	2.0	mA
I^-, Current (Pin 4)	+25°C	-	0.5	-	-	0.5	-	mA
	Full	-	-	2.0	-	-	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = 1mA
2. Digital Inputs are MOS gates — Typical Leakage is Less Than 1nA.
3. V_{AH} = 4.0V.
4. V_A = 5V, R_L = 1kΩ, C_L = 10pF, V_S = $3V_{RMS}$, f = 100kHz.
5. V_A = +3V or V_A = 0V for All Switches.
6. Refer to Leakage Current Measurement Diagram on Page 3-8.

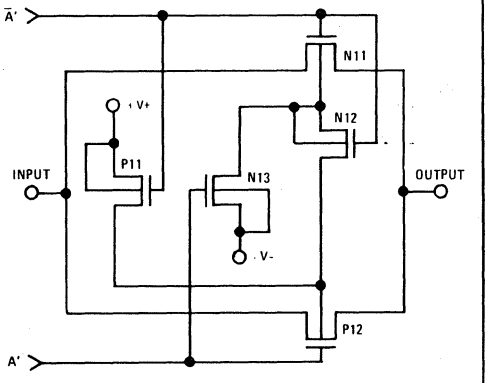
**NOTE: HI-201-4 Has Same Specifications as HI-201-5 Over the Temperature Range -25°C to +85°C.

Schematic Diagrams

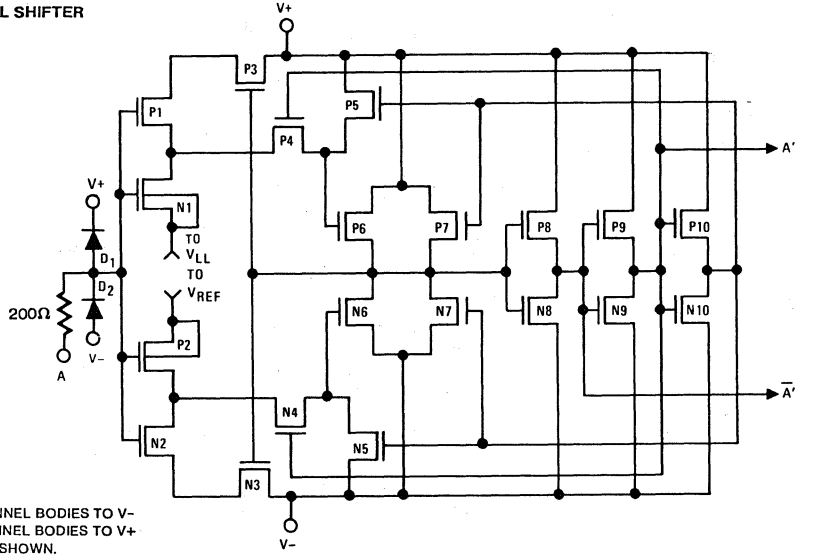
TTL/CMOS REFERENCE CIRCUIT
V-REF CELL



SWITCH CELL

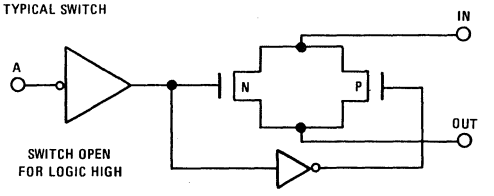


DIGITAL INPUT BUFFER
AND LEVEL SHIFTER



ALL N-CHANNEL BODIES TO V-
ALL P-CHANNEL BODIES TO V+
EXCEPT AS SHOWN.

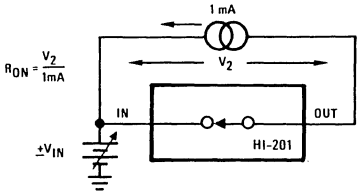
Functional Diagram



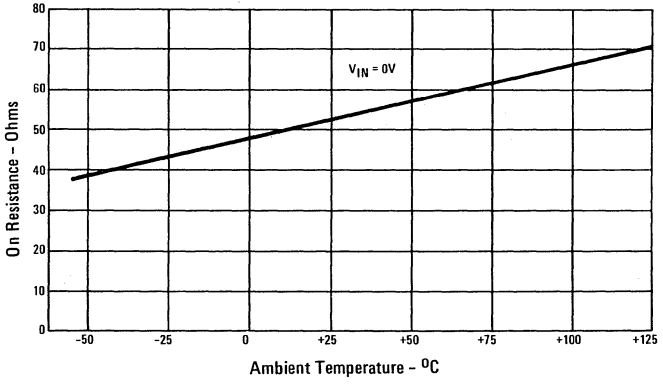
Performance Characteristics and Test Circuits

Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$ and V_{REF} = Open

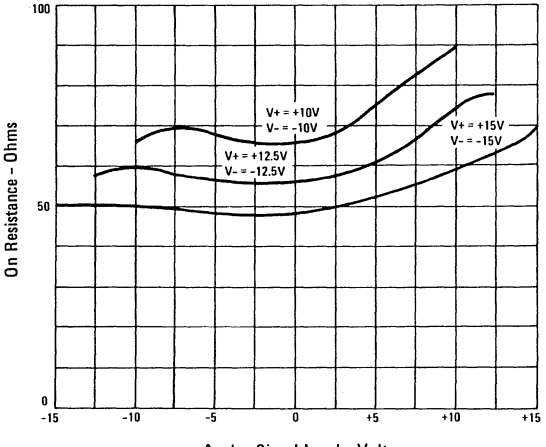
ON RESISTANCE vs. ANALOG SIGNAL LEVEL, ... SUPPLY VOLTAGE AND TEMPERATURE



ON RESISTANCE vs. TEMPERATURE

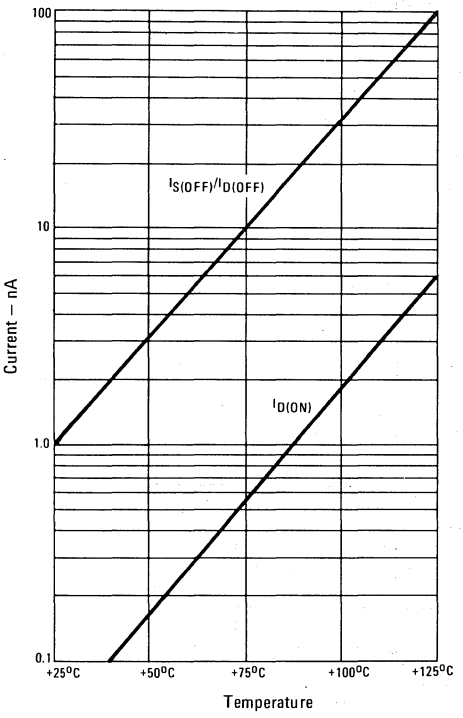


(HI-201)
ON RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

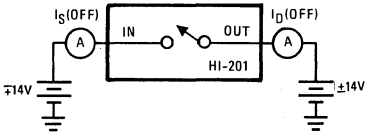


Performance Characteristics and Test Circuits (Continued)

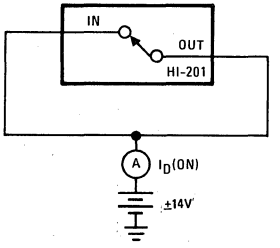
SWITCH LEAKAGE CURRENT vs. TEMPERATURE (HI-201)



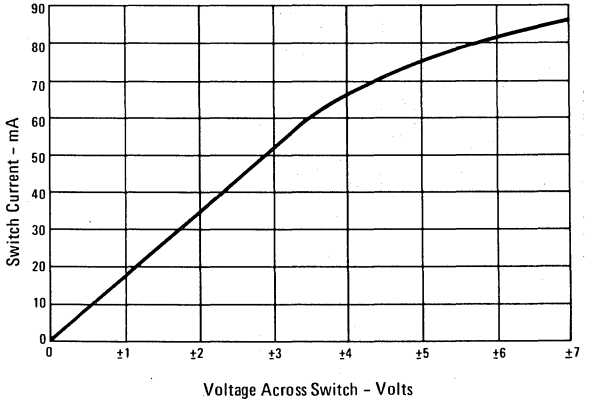
OFF LEAKAGE CURRENT vs. TEMPERATURE



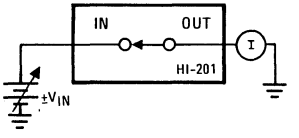
ON LEAKAGE CURRENT vs. TEMPERATURE



SWITCH CURRENT vs. VOLTAGE

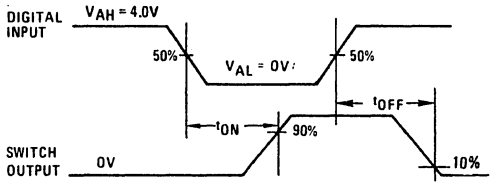


SWITCH CURRENT vs. VOLTAGE

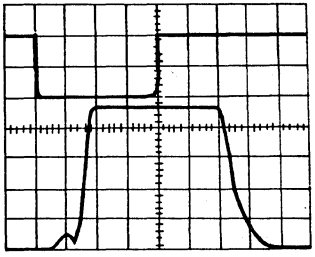


Switching Waveforms

LOGIC "0" = SWITCH ON

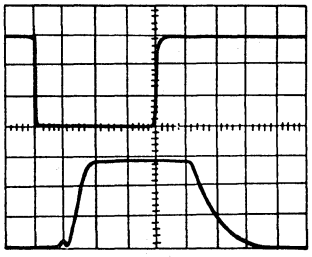


t_{ON}, t_{OFF} (TTL INPUT)
V_{IN} = +4.0V



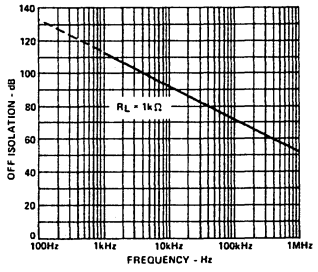
TOP: TTL Input VERTICAL: 2V/Div.
BOTTOM: Output HORIZONTAL: 100ns/Div.

t_{ON}, t_{OFF} (CMOS INPUT)
V_{REF} = OPEN, V_{IN} = +15V



TOP: CMOS Input VERTICAL: 5V/Div.
BOTTOM: Output HORIZONTAL: 100ns/Div.

OFF ISOLATION vs. FREQUENCY



For More Information See Application Notes 520, 521, 531, 532 and 557 in Section 10 of Data Book.

HARRIS

HI-201HS

High Speed Quad SPST CMOS Analog Switch

January 1988

Features

- Fast Switching Times ..... t_{ON} = 30ns, t_{OFF} = 40ns
- Low "ON" Resistance 30Ω
- Pin Compatible with Standard HI-201
- Wide Analog Voltage Range (±15V Supplies) .. ±15V
- Low Charge Injection (±15V Supplies) 10pC
- TTL Compatible
- Symmetrical Switching Analog Current Range 80mA

Applications

- High Speed Multiplexing
- High Frequency Analog Switching
- Sample and Hold Circuits
- Digital Filters
- Operational Amplifier Gain Switching Networks
- Integrator Reset Circuits

Description

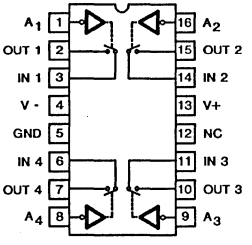
The HI-201HS is a monolithic CMOS Analog Switch featuring very fast switching speeds and low ON resistance. This integrated circuit consists of four independently selectable SPST switches and is pin compatible with the industry standard HI-201 switch.

Fabricated using silicon-gate technology and the Harris Dielectric Isolation process, this TTL compatible device offers improved performance over previously available CMOS analog switches. Featuring maximum switching times of 50ns, low ON resistance of 50Ω maximum, and a wide analog signal range, the HI-201HS is designed for any application where improved switching performance, particularly switching speed, is required. (A more detailed discussion on the design and application of the HI-201HS can be found in Application Note 543).

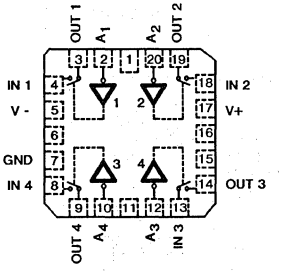
The HI-201HS is available in a 16 pin Ceramic DIP package. The HI-201HS-2 is specified over the temperature range from -55°C to +125°C and the HI-201HS-5 version from 0°C to +75°C. HI-201HS-4 is also offered from -25°C to +85°C.

Pinouts

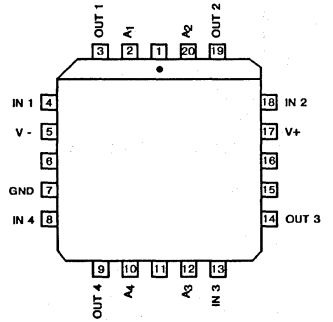
16 LEAD CERAMIC DIP
TOP VIEW



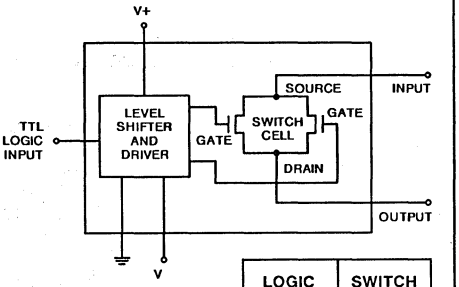
20 LEADLESS CERAMIC CHIP
TOP VIEW



20 PLASTIC LEAD CERAMIC CHIP



Functional Diagram



LOGIC	SWITCH
0	ON
1	OFF

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
HI1-0201HS-5	0°C to +75°C	16 Pin Ceramic DIP
HI3-0201HS-4	-25°C to +85°C	16 Pin Plastic DIP
HI1-0201HS-2	-55°C to +125°C	16 Pin Ceramic DIP
HI1-0201HS-4	-25°C to +85°C	16 Pin Ceramic DIP
HI4P0201HS-4	-25°C to +85°C	20 Pin PLCC
HI4P0201HS-5	0°C to +75°C	20 Pin PLCC
HI3-0201HS-5	0°C to +75°C	16 Pin Plastic DIP
HI1-0201HS-7	0°C to +75°C	16 Pin Ceramic DIP
HI4-0201HS/883	-55°C to +125°C	20 Pin LCC

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Specifications HI-201HS

Absolute Maximum Ratings

Supply Voltage (Between Pins 4 and 13) 36V
Digital Input Voltage (Pins 1, 8, 9, 16) ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Analog Input Voltage (One Switch) ..... $+V_{SUPPLY}$ +2.0V
Pins 2, 3, 6, 7, 10, 11, 14, 15 $-V_{SUPPLY}$ -2.0V
Analog Current — Continuous Peak 30mA, 80mA
Total Power Dissipation (Note 2) 750mW
Maximum Junction Temperature ..... +175°C

Operating Temperature Range

HI-201HS-2 ..... -55°C to +125°C
HI-201HS-4 ..... -25°C to +85°C
HI-201HS-5 ..... 0°C to +75°C
Storage Temperature ..... -65°C to +150°C

Electrical Specifications

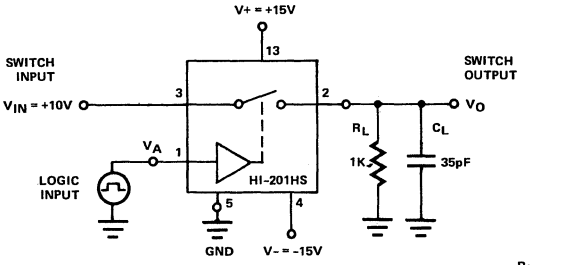
Unless Otherwise Specified: Supplies = +15V, -15V; V_{AH} (Logic Level High) = 3.0V, V_{AL} (Logic Level Low) = +0.8V, GND = 0V

PARAMETER	TEMP	HI-201HS-2 MIN	HI-201HS-2 TYP	HI-201HS-2 MAX	HI-201HS-5/-4 MIN	HI-201HS-5/-4 TYP	HI-201HS-5/-4 MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15	-	+15	-15	-	+15	V
R_{ON}, On Resistance (Note 3)	+25°C	-	30	50	-	30	50	Ω
	Full	-	-	75	-	-	75	Ω
R_{ON} Match	+25°C	-	3	-	-	3	-	%
$I_{S(OFF)}$, Off Input Leakage Current	+25°C	-	0.3	10	-	0.3	10	nA
	Full	-	-	100	-	-	50	nA
$I_{D(OFF)}$, Off Output Leakage Current	+25°C	-	0.3	10	-	0.3	10	nA
	Full	-	-	100	-	-	50	nA
$I_{D(ON)}$, On Leakage Current	+25°C	-	0.1	10	-	0.1	10	nA
	Full	-	-	100	-	-	50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full	-	-	0.8	-	-	0.8	V
V_{AH}, Input High Threshold	+25°C	2.0	-	-	2.0	-	-	V
	Full	2.4	-	-	2.4	-	-	V
I_{AL}, Input Leakage Current (Low)	+25°C	-	200	-	-	200	-	µA
	Full	-	-	-500	-	-	-500	µA
I_{AH}, Input Leakage Current (High)	+25°C	-	20	-	-	20	-	µA
	Full	-	-	+40	-	-	+40	µA
SWITCHING CHARACTERISTICS								
t_{ON}, Switch On Time (Note 4)	+25°C	-	30	50	-	30	50	ns
t_{OFF1}, Switch Off Time (Note 4)	+25°C	-	40	50	-	40	50	ns
t_{OFF2}, Switch Off Time (Note 4)	+25°C	-	150	-	-	150	-	ns
Output Settling Time 0.1%	+25°C	-	180	-	-	180	-	ns
"Off Isolation" (Note 5)	+25°C	-	72	-	-	72	-	dB
Crosstalk (Note 6)	+25°C	-	86	-	-	86	-	dB
Charge Injection (Note 7)	+25°C	-	10	-	-	10	-	pC
$C_{S(OFF)}$, Input Switch Capacitance	+25°C	-	10	-	-	10	-	pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C	-	10	-	-	10	-	pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C	-	30	-	-	30	-	pF
C_A, Digital Input Capacitance	+25°C	-	18	-	-	18	-	pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C	-	0.5	-	-	0.5	-	pF
POWER REQUIREMENTS (Note 8)								
P_D, Power Dissipation	+25°C	-	120	-	-	120	-	mW
	Full	-	-	240	-	-	240	mW
I^+, Current (Pin 13)	+25°C	-	4.5	-	-	4.5	-	mA
	Full	-	-	10.0	-	-	10.0	mA
I^-, Current (Pin 4)	+25°C	-	3.5	-	-	3.5	-	mA
	Full	-	-	6	-	-	6	mA

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. Derate 8mW/°C above T_A = +75°C, θ_{ja} = 100°C/W, θ_{jc} = 32°C/W.
3. V_{OUT} = ±10V, I_{OUT} = 1mA.
4. R_L = 1kΩ, C_L = 35pF, V_{IN} = +10V, V_A = +3V. (See Switching Waveforms).
5. V_A = 3V, R_L = 1kΩ, C_L = 10pF, V_{IN} = $3V_{RMS}$, f = 100kHz.
6. V_A = 3V, R_L = 1kΩ, V_{IN} = $3V_{RMS}$, f = 100kHz.
7. C_L = 1000pF, V_{IN} = 0V, R_{IN} = 0Ω, $\Delta Q = C_L \times \Delta V_O$.
8. V_A = 3V or V_A = 0 for all switches.
9. V_A = 4V.

Test Circuit

SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF1}, t_{OFF2})

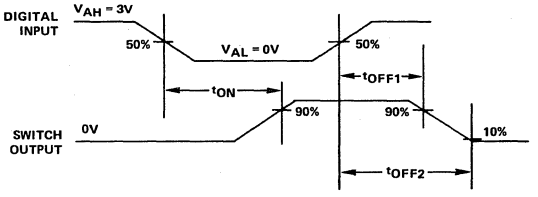


$$V_O = V_{IN} \frac{R_L}{R_L + R_{ON}}$$

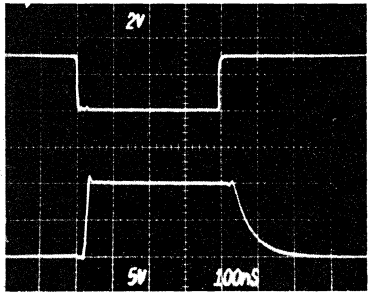
C_L INCLUDES $C_{FIXTURE} + C_{PROBE}$

Switching Waveforms

LOGIC "0" = SWITCH ON



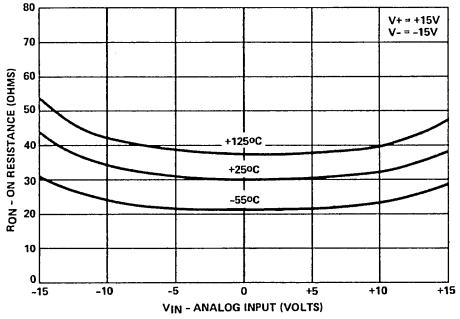
t_{ON}, t_{OFF}(TTL INPUT)
V_{AH} = +3.0V



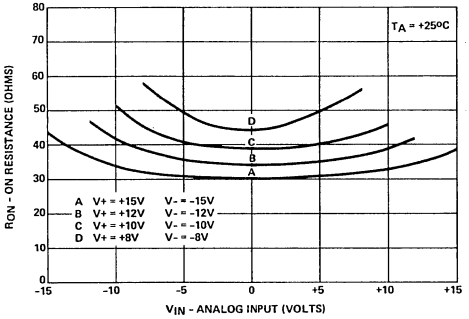
TOP: TTL Input (2V/Div.)
BOTTOM: Output (5V/Div.) HORIZONTAL: 100ns/Div.

Typical Performance Curves

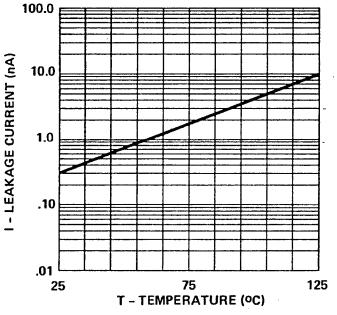
"ON" RESISTANCE vs. ANALOG SIGNAL LEVEL AND TEMPERATURE



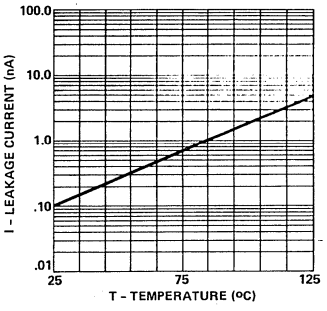
"ON" RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE



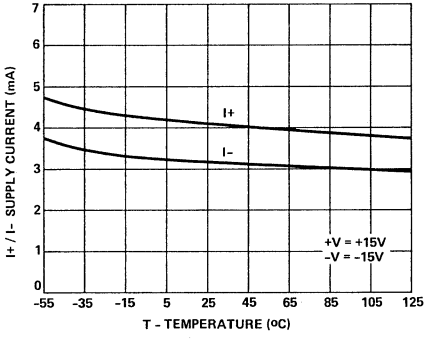
$I_{S(OFF)}$ OR $I_{D(OFF)}$ vs. TEMPERATURE*



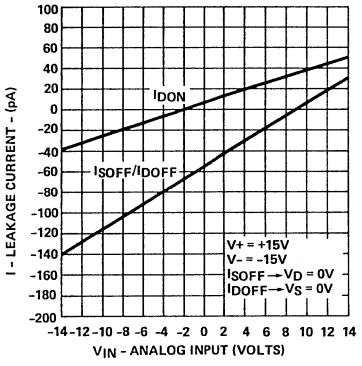
$I_{D(ON)}$ vs. TEMPERATURE*



SUPPLY CURRENT vs. TEMPERATURE



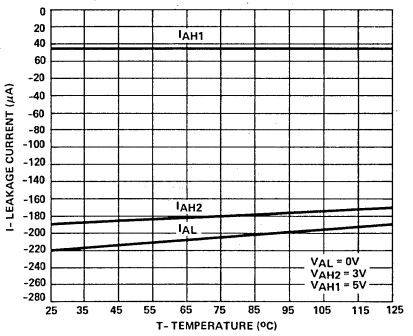
LEAKAGE CURRENT vs. ANALOG INPUT VOLTAGE



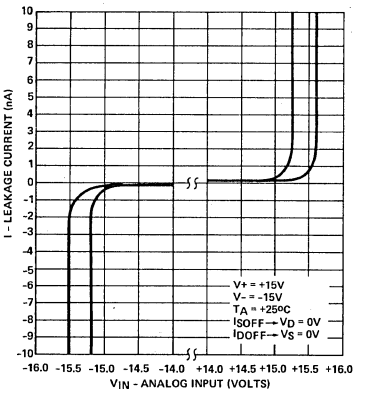
* THEORETICALLY, LEAKAGE CURRENT WILL CONTINUE TO DECREASE BELOW +25°C. BUT DUE TO ENVIRONMENTAL CONDITIONS, LEAKAGE MEASUREMENTS BELOW THIS TEMPERATURE ARE NOT REPRESENTATIVE OF ACTUAL SWITCH PERFORMANCE.

Typical Performance Curves (Continued)

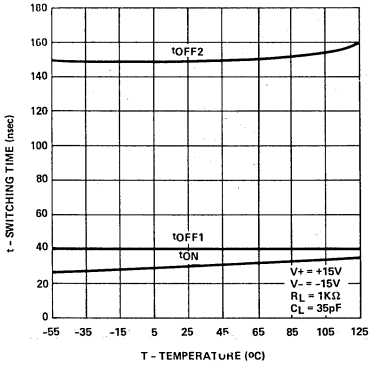
DIGITAL INPUT LEAKAGE CURRENT vs. TEMPERATURE*



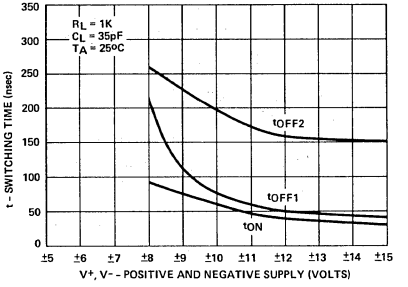
LEAKAGE CURRENT vs. ANALOG INPUT VOLTAGE
(V_{IN} > +14V, V_{IN} < -14V)



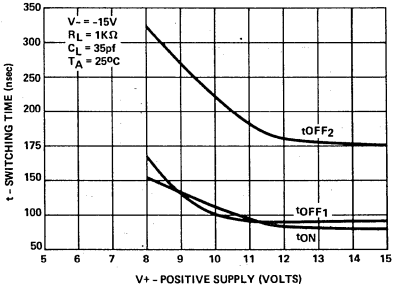
SWITCHING TIME vs. TEMPERATURE



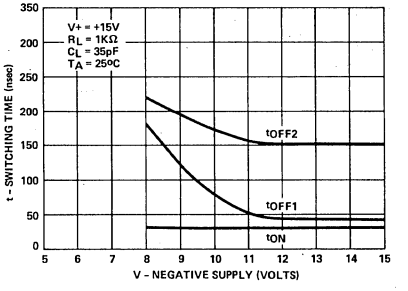
SWITCHING TIME vs. POSITIVE AND NEGATIVE SUPPLY VOLTAGE



SWITCHING TIME vs. POSITIVE SUPPLY VOLTAGE



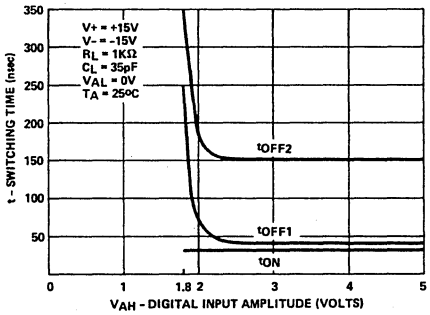
SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE



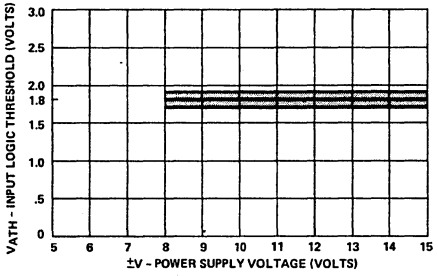
* THEORETICALLY, LEAKAGE CURRENT WILL CONTINUE TO DECREASE BELOW +25°C. BUT DUE TO ENVIRONMENTAL CONDITIONS, LEAKAGE MEASUREMENTS BELOW THIS TEMPERATURE ARE NOT REPRESENTATIVE OF ACTUAL SWITCH PERFORMANCE.

Typical Performance Curves (Continued)

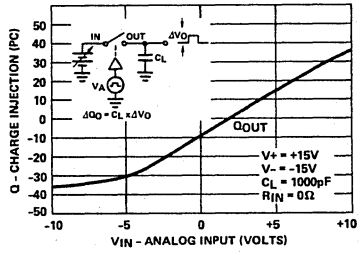
SWITCHING TIME vs. INPUT LOGIC AMPLITUDE



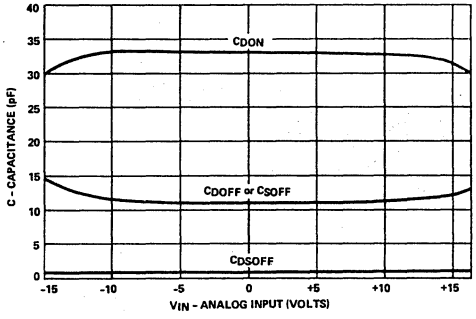
INPUT SWITCHING THRESHOLD vs. POSITIVE AND NEGATIVE SUPPLY VOLTAGES



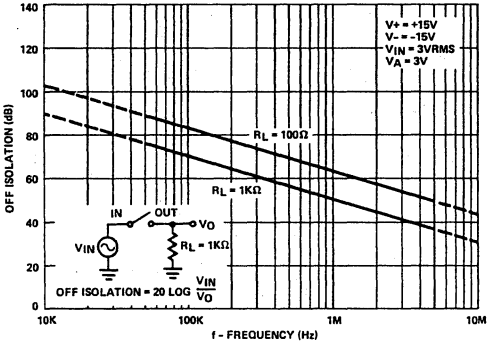
CHARGE INJECTION vs. ANALOG INPUT



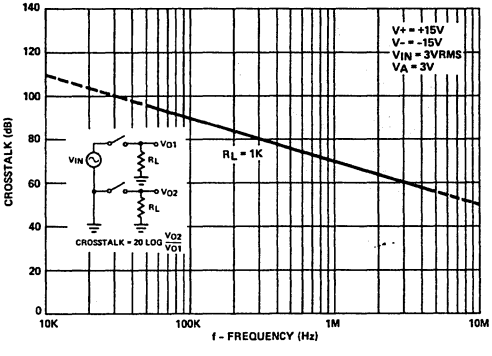
CAPACITANCE vs. ANALOG INPUT



OFF ISOLATION vs. FREQUENCY



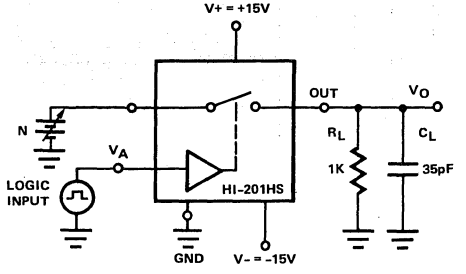
CROSSTALK vs. FREQUENCY



Switching Characteristics

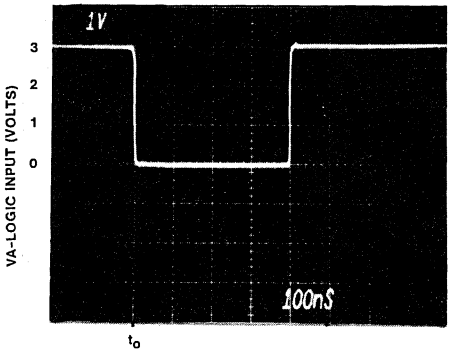
SWITCHING CHARACTERISTICS vs. INPUT VOLTAGE

Typical delay, t_{ON}, t_{OFF}, settling time and switching transients in this circuit.

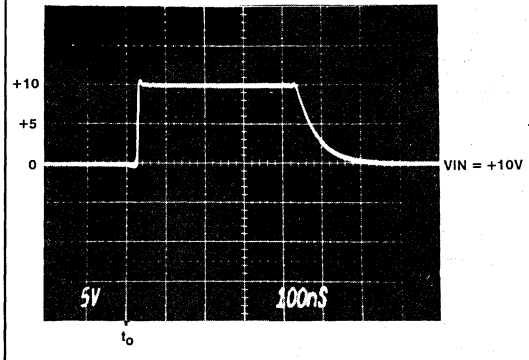


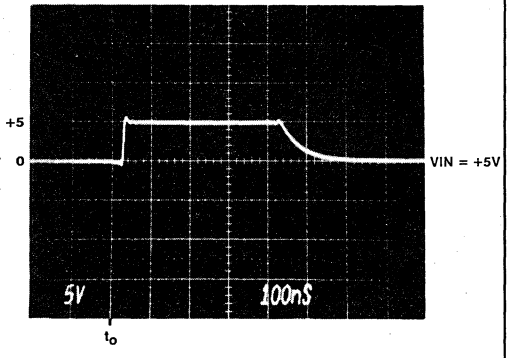
If R_L or C_L is increased, there will be corresponding increases in rise and/or fall RC times.

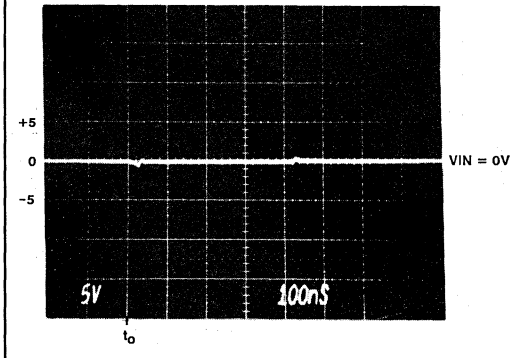
LOGIC INPUT

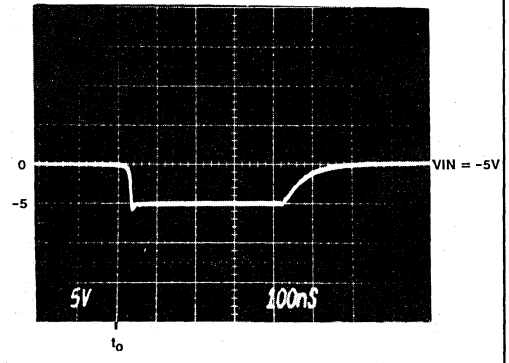


V_O - OUTPUT SWITCHING WAVEFORMS



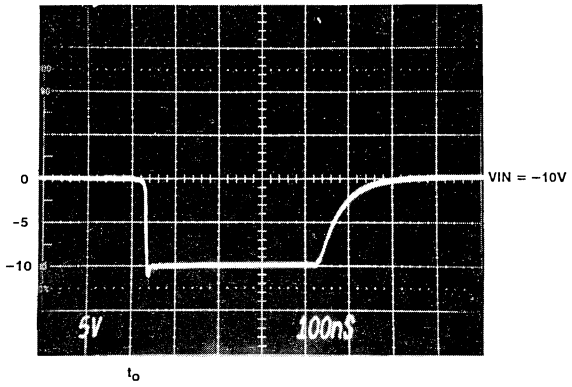






Switching Characteristics (Continued)

V_O - OUTPUT SWITCHING WAVEFORMS



Application Information

LOGIC COMPATIBILITY

The HI-201HS is TTL compatible. Its logic inputs (Pins 1, 8, 9, 16) are designed to react to digital inputs which exceed a fixed, internally generated TTL switching threshold. The HI-201HS can also be driven with CMOS logic (0-15V), although the switch performance with CMOS logic will be inferior to that with TTL logic (0-5V).

The logic input design of the HI-201HS is largely responsible for its fast switching speed. It is a design which features a unique input stage consisting of complementary vertical PNP and NPN bipolar transistors. This design differs from that of the standard HI-201 product where the logic inputs are MOS transistors.

Although the new logic design enhances the switching speed performance, it also increases the logic input leakage currents. Therefore, the HI-201HS will exhibit larger digital input leakage currents in comparison to the standard HI-201 product.

CHARGE INJECTION

Charge injection is the charge transferred, through the internal gate-to-channel capacitances, from the digital logic input to the analog output. To optimize charge injection performance for the HI-201HS, it is advisable to provide a TTL logic input with fast rise and fall times.

If the power supplies are reduced from ±15V, charge injection will become increasingly dependent upon the digital input frequency. Increased logic input frequency will result in larger output error due to charge injection.

POWER SUPPLY CONSIDERATIONS

The electrical characteristics specified in this data sheet are guaranteed for power supplies $\pm V_S = \pm 15V$. Power supply voltages less than ±15V will result in reduced switch performance. The following information is intended as a design aid only:

POWER SUPPLY VOLTAGES	SWITCH PERFORMANCE
$\pm 12 < \pm V_S \pm 15V$	Minimal Variation
$\pm V_S < \pm 12V$	Parametric Variation becomes Increasingly Large (Increased ON Resistance, Longer Switching Times).
$\pm V_S < \pm 10V$	Not Recommended.
$\pm V_S > \pm 16V$	Not Recommended.

SINGLE SUPPLY

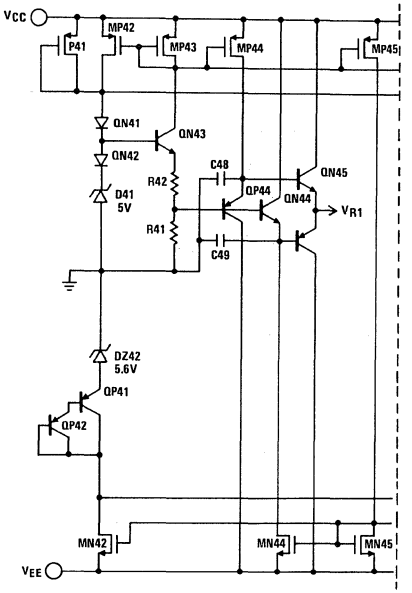
The switch operation of the HI-201HS is dependent upon an internally generated switching threshold voltage optimized for ±15V power supplies. The HI-201HS does not provide the necessary internal switching threshold in a single supply system. Therefore, if single supply operation is required, the HI-300 series of switches is recommended. The HI-300 series will remain operational to a minimum +5V single supply.

Switch performance will degrade as power supply voltage is reduced from optimum levels (±15V). So it is recommended that a single supply design be thoroughly evaluated to ensure that the switch will meet the requirements of the application.

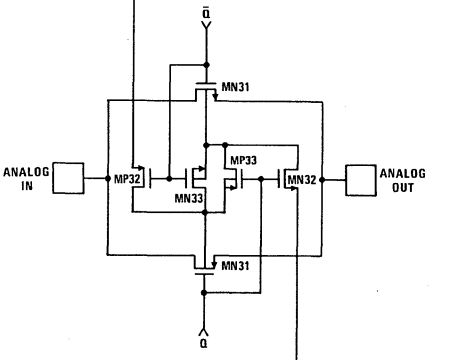
For Further Information See Application Notes 520, 521, 531, 532, 543 and 557 in Section 10 of Data Book.

Schematic Diagrams

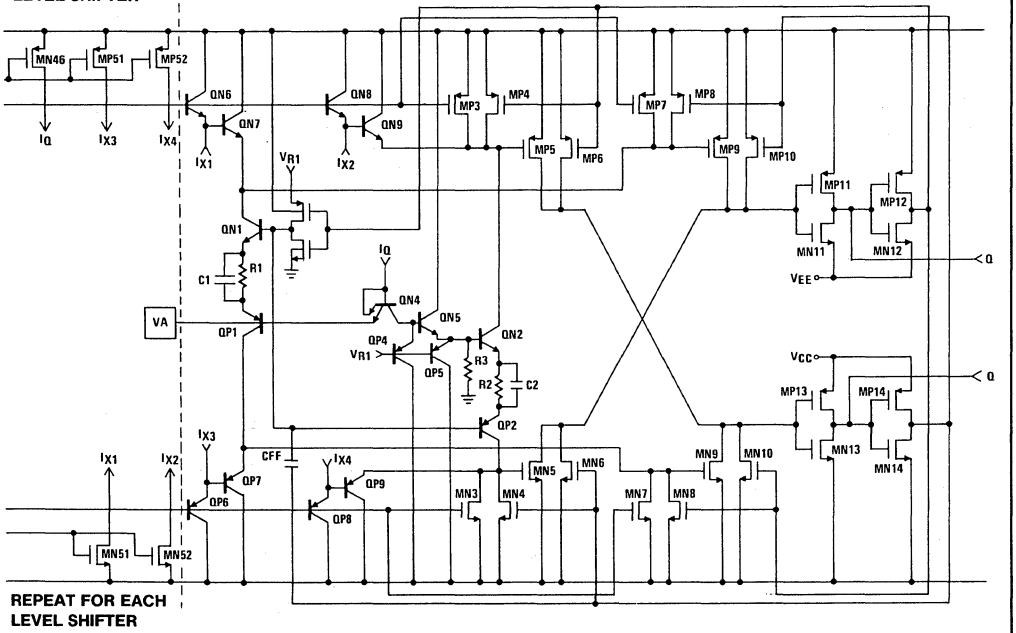
TTL/CMOS REFERENCE CIRCUIT



SWITCH CELL



DIGITAL INPUT AND LEVEL SHIFTER



REPEAT FOR EACH LEVEL SHIFTER

HARRIS HI-222

December 1988

High Frequency/Video Switch

Features

- Wideband Operation ..... 200 MHz
- Differential Gain 0.03%
- Differential Phase..... 0.003 Degrees
- Switching Speed 100ns
- R_{ON} 35Ω
- Off Isolation @ 10 MHz ..... -65dB
- Crosstalk @ 10 MHz ..... -80dB

Applications

- Routing Switchers
- Production Mixers
- High Definition TV
- Radar Signal Conditioning
- Medical Imaging
- Heads-Up Displays
- Simulators
- Sonar

Description

The HI-222 is a high frequency analog switch that complements the Harris family of high speed op amps and buffers. Fabricated with our Dielectric Isolation process and using silicon gate technology, many key parameters have been enhanced.

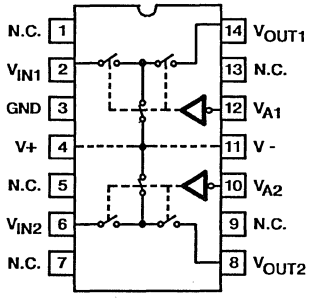
Crosstalk and off isolation are optimized with a T-switch configuration and the use of nonconnected pins for extended shielding. Other features of the HI-222 include wideband operation, low R_{ON}, fast switching speeds and low differential gain and phase. The characteristics of this TTL compatible device make it ideal for designs where improved switching performance is required.

The primary application of this dual SPST switch is the routing of high frequency signals in equipment ranging from video production mixers to military RF circuits.

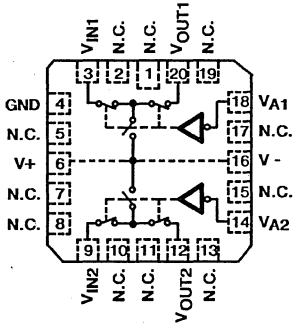
The HI-222 is available in a 14 pin Ceramic DIP with -5, -9 and /883 temperature options, and in a Plastic DIP with a -5 option. A Plastic Leaded Chip Carrier (PLCC) with a -5 option and a Leadless Chip Carrier (LCC) with a /883 option are also offered. For additional information on the /883 products, please refer to the Harris Military Analog Product Data Book.

Pinouts

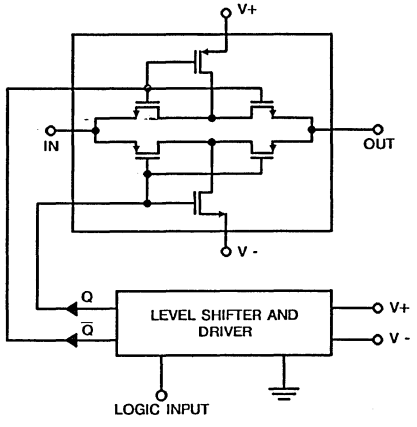
(CERAMIC/PLASTIC DIP) LOGIC "1" INPUT
TOP VIEW



(LCC/PLCC) LOGIC "0" INPUT
TOP VIEW



Functional Diagram



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI4P0222-5	0°C to +75°C	20-Pin PLCC
HI1-0222-5	0°C to +75°C	14-Pin CERDIP
HI3-0222-5	0°C to +75°C	14-Pin Plastic DIP
HI1-0222-9	-40°C to +85°C	14-Pin CERDIP

NOTE: Source and Drain are arbitrarily depicted as Analog Input and Output, respectively. They may be interchanged without affecting performance. All nonconnected pins should be tied to ground.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

Specifications HI-222

Absolute Maximum Ratngs (Note 1)

Voltage Between V+ and V- Terminals 36V
$\pm V_S$ to Ground (V+, V-) ..... $\pm$18V
Digital and Analog Input Voltage (V_A, V_S, V_D) ..... $\pm V_S$ $\pm$2V
I_{peak} (S to D) (Pulse at 0.8ms, 10% Duty Cycle Max) 100mA
I_{peak} (Any Pin, 50% Duty Cycle) 28mA
Continuous Current (Any Pin) 15mA
Junction Temperature ..... +175°C
Storage Temperature Range ..... -65°C to +150°C
ESD Rating ..... < 2000V
Lead Temperature (Soldering 10 sec) ..... 300°C

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic/Plastic DIP Package	75°C/W	17°C/W
Ceramic LCC Package	76°C/W	19°C/W

Package Power Dissipation Limit at +75°C
Ceramic/Plastic DIP and Ceramic LCC Package 1.0W
Package Power Dissipation Derating Factor Above +75°C
Ceramic/Plastic DIP Package ..... 13.4mW/°C
Ceramic LCC Package ..... 13.2mW/°C
Operating Temp. Range HI-222-5 ..... $0°C \leq T_A \leq +75°C$
HI-222-9 ..... $-40°C \leq T_A \leq +85°C$

D.C. Electrical Specifications

$\pm V_S = \pm 15V$. $V_{AH} = 2.0V$, $V_{AL} = 0.8V$, Unless Otherwise Specified

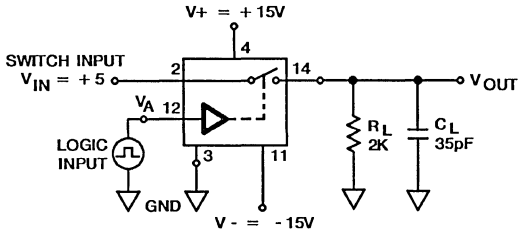
PARAMETER	TEMP	HI-222-9 MIN	HI-222-9 TYP	HI-222-9 MAX	HI-222-5 MIN	HI-222-5 TYP	HI-222-5 MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15	-	+15	-15	-	+15	V
R_{ON}, ON Resistance (Note 2)	+25°C	-	35	50	-	35	50	Ω
	Full	-	-	75	-	-	75	Ω
$I_{S(OFF)}$ Leakage	+25°C	-	0.1	2.5	-	0.1	2.5	nA
	Full	-	-	200	-	-	200	nA
$I_{D(OFF)}$ Leakage	+25°C	-	0.1	2.5	-	0.1	2.5	nA
	Full	-	-	200	-	-	200	nA
$I_{D(ON)}$ Leakage	+25°C	-	0.3	2.5	-	0.3	2.5	A
	Full	-	-	200	-	-	200	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Low Threshold	Full	-	-	0.8	-	-	0.8	V
V_{AH}, High Threshold	Full	2.0	-	-	2.0	-	-	V
I_{AL}, Low Level Leakage	+25°C	-	0.1	1.0	-	0.1	1.0	µA
	Full	-	-	1.0	-	-	1.0	µA
I_{AH}, High Level Leakage	+25°C	-	0.1	1.0	-	0.1	1.0	µA
	Full	-	-	1.0	-	-	1.0	µA
SWITCHING CHARACTERISTICS								
t_{ON} (Note 3)	+25°C	-	100	200	-	100	200	ns
t_{OFF} (Note 3)	+25°C	-	70	200	-	70	200	ns
Off-Isolation @10MHz (Note 4)	+25°C	-	-65	-	-	-65	-	dB
Crosstalk @10MHz (Note 4)	+25°C	-	-80	-	-	-80	-	dB
Differential Gain (Note 5)	+25°C	-	0.03	-	-	0.03	-	%
Differential Phase (Note 5)	+25°C	-	0.003	-	-	0.003	-	degrees
Gain Tolerance @1MHz (Note 6)	+25°C	-	0.05	-	-	0.05	-	dB
@ 8MHz	+25°C	-	0.15	-	-	0.15	-	dB
Bandwidth (Note 6)	+25°C	-	200	-	-	200	-	MHz
$C_{S(OFF)}$, Switch Input Capacitance	+25°C	-	12	-	-	12	-	pF
$C_{D(OFF)}$, Switch Output Capacitance	+25°C	-	28	-	-	28	-	pF
$C_{D(ON)}$, Switch Output Capacitance	+25°C	-	83	-	-	83	-	pF
C_A, Digital Address Capacitance	+25°C	-	5	-	-	5	-	pF
$C_{DS(OFF)}$, Drain-to-Source Capacitance	+25°C	-	0.2	-	-	0.2	-	pF
POWER REQUIREMENTS								
I± @ ±15V Quiescent Current	+25°C	-	2.5	4.0	-	2.5	4.0	mA
	Full	-	-	6.0	-	-	6.0	mA
P_D, Quiescent Power Dissipation	+25°C	-	75	120	-	75	120	mW
	Full	-	-	180	-	-	180	mW

NOTES:

1. As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.
2. $V_{OUT} = \pm 5V$, $I_{OUT} = 7.5mA$
3. $V_{IN} = +5V$, $R_L = 2k\Omega$, $C_L = 40pF$. V_A levels are 0.0V to 3.0V for switch under test. Switch not under test has $V_A = 4.0V$.
4. $V_{IN} = 300mV_{p-p}$, $R_L = 50\Omega$, $V_{AH} = +2.0V$, $V_{AL} = 0.8$, f = 10.0MHz.
5. $V_{IN} = 300mV_{p-p}$, $V_{OFFSET} = 1.0$, f = 3.58MHz and 4.43MHz, $V_{AL} = 0V$, $R_L = 2K\Omega$.
6. $V_{IN} = 300mV_{p-p}$, $R_L = 50\Omega$, $V_{AL} = 0.8V$.

Test Circuit

SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF1})

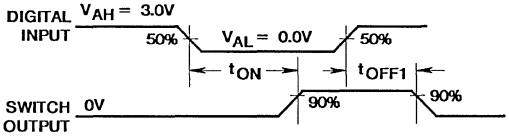


$$V_O = V_{IN} \frac{R_L}{R_L + R_{ON}}$$

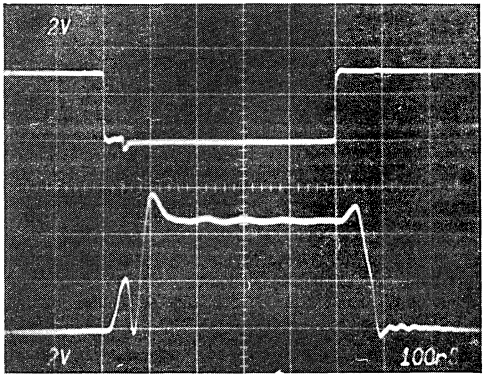
C_L Includes $C_{FIXTURE} + C_{PROBE}$

Switching Waveforms

LOGIC "0" = SWITCH ON



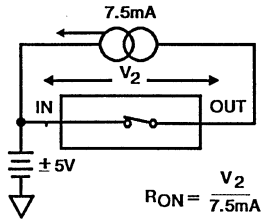
t_{ON}, t_{OFF}, $V_{AL} = 0.0V$, $V_{AH} = 3.0V$



Top: (2V/Div.)
Bottom: Output (2V/Div.)
Horizontal: 100ns/Div.

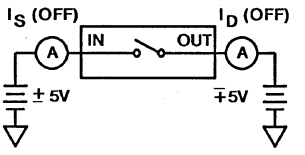
Test Circuits

R_{DS}



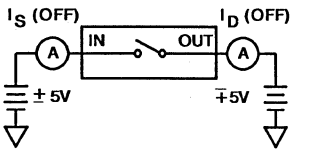
V_{IN} = ±5V, I = 7.5mA, V_A = 0.8V

$I_{S(OFF)}$



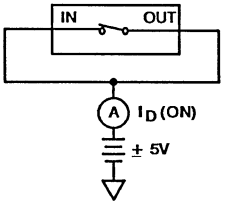
V_{IN} = ±5V, V_{OUT} = ∓5V, V_A = 2.0V

$I_{D(OFF)}$



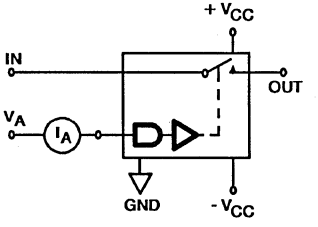
V_{IN} = ±5V, V_{OUT} ∓5V, V_A = 2.0V

$I_{D(ON)}$



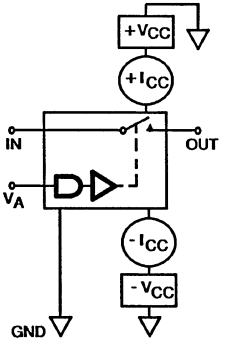
V_{IN} = ±5V, V_{OUT} = ±5V, V_A = 0.8V

ADDRESS CURRENT



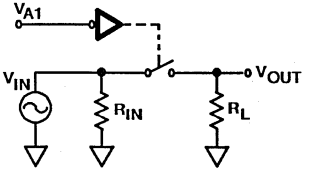
V_{AH} = 2.0V, V_{AL} = 0.8V

SUPPLY CURRENTS



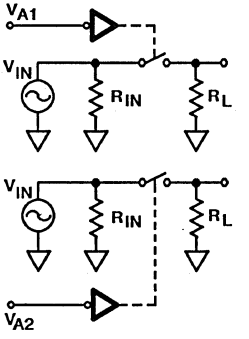
V_A = 0.8V, 2.0V

OFF ISOLATION



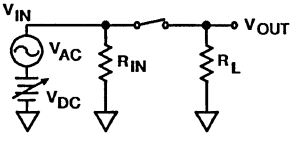
V_{IN} = 300mV$_{p-p}$, f = 10MHz, R_{IN} = R_L = 50Ω, V_{A1} = 2.0V

CROSSTALK



V_{IN} = 300mV$_{p-p}$, f = 10MHz, R_{IN} = R_L = 50Ω
V_{A1} = 2.0V, V_{A2} = 0.8V

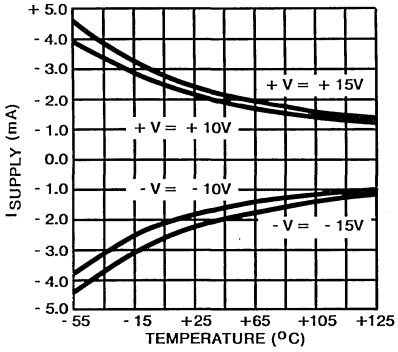
DIFFERENTIAL GAIN, PHASE



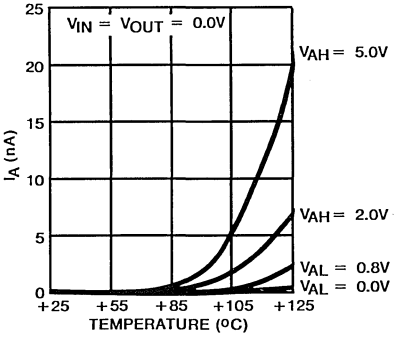
V_{AC} = 300mV$_{p-p}$, f = 3.58MHz and 4.43MHz,
V_{DC} = 0.0V to 1.0V, R_L = 2kΩ, R_{IN} = 50Ω

Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

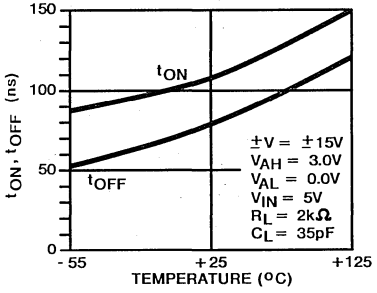
SUPPLY CURRENT vs. TEMPERATURE vs. SUPPLY VOLTAGE



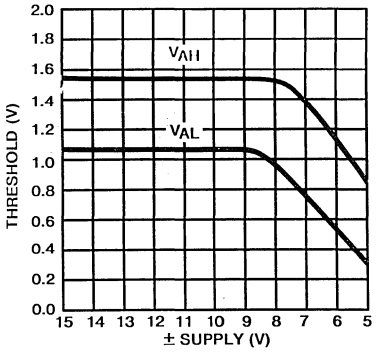
STEADY STATE ADDRESS INPUT CURRENT vs. TEMPERATURE



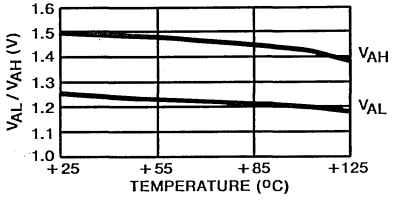
SWITCHING TIME vs. TEMPERATURE



SWITCHING THRESHOLD vs. ±SUPPLY VOLTAGE

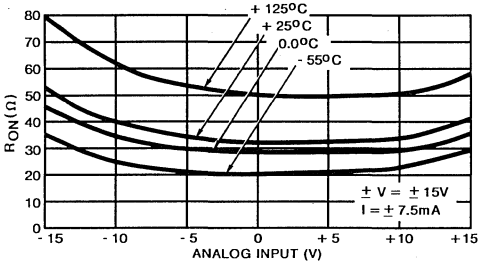


ADDRESS INPUT THRESHOLD vs. TEMPERATURE

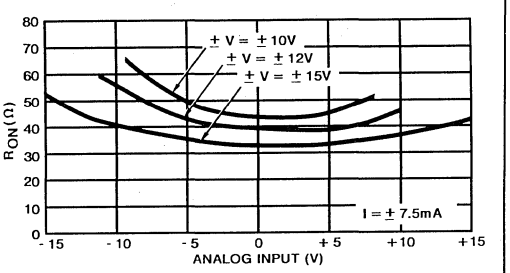


Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

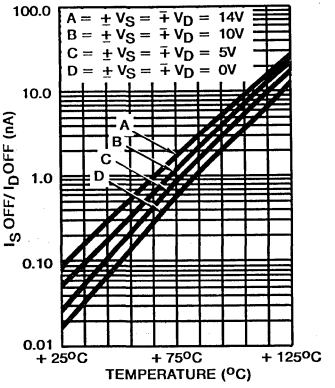
R_{ON} vs. ANALOG INPUT vs. TEMPERATURE



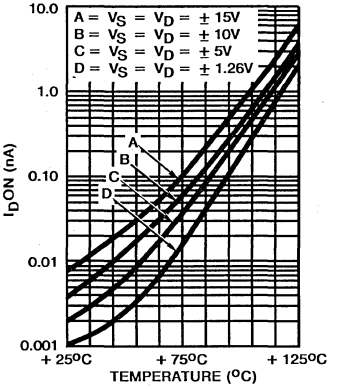
R_{ON} vs. ANALOG INPUT vs. SUPPLY VOLTAGE



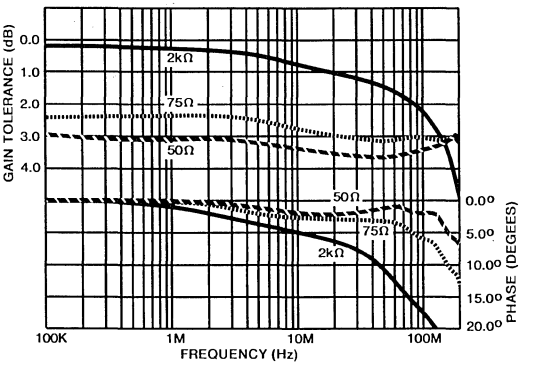
I_{SOFF}/I_{DOFF} vs. TEMPERATURE vs. ANALOG INPUT



I_{DON} vs. TEMPERATURE vs. ANALOG INPUT

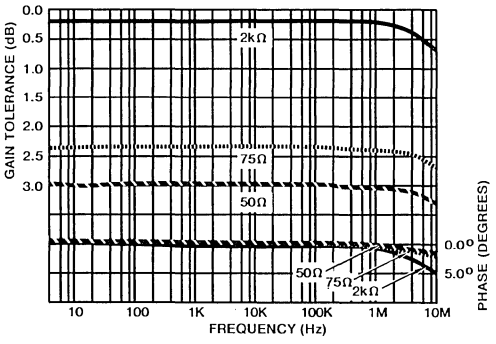


BANDWIDTH

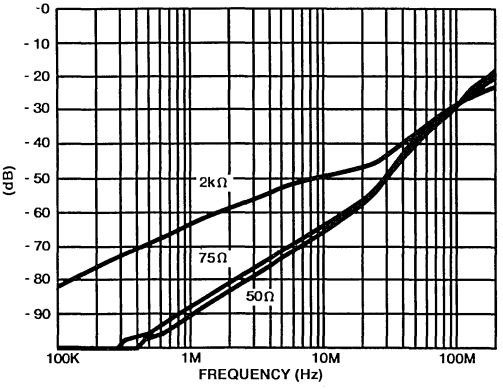


Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm 15V$

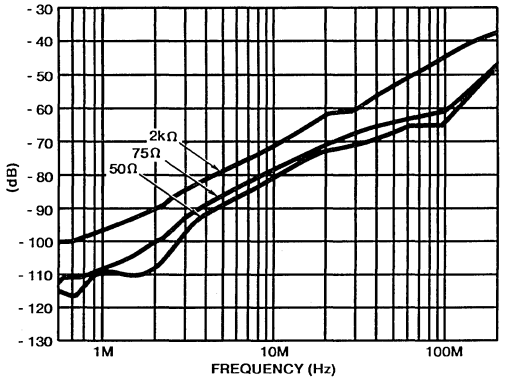
GAIN TOLERANCE



OFF ISOLATION

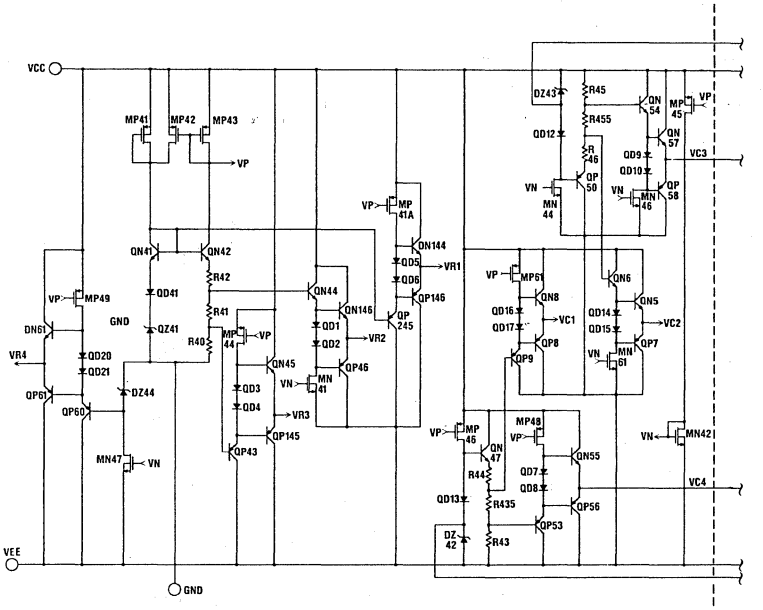


CROSSTALK



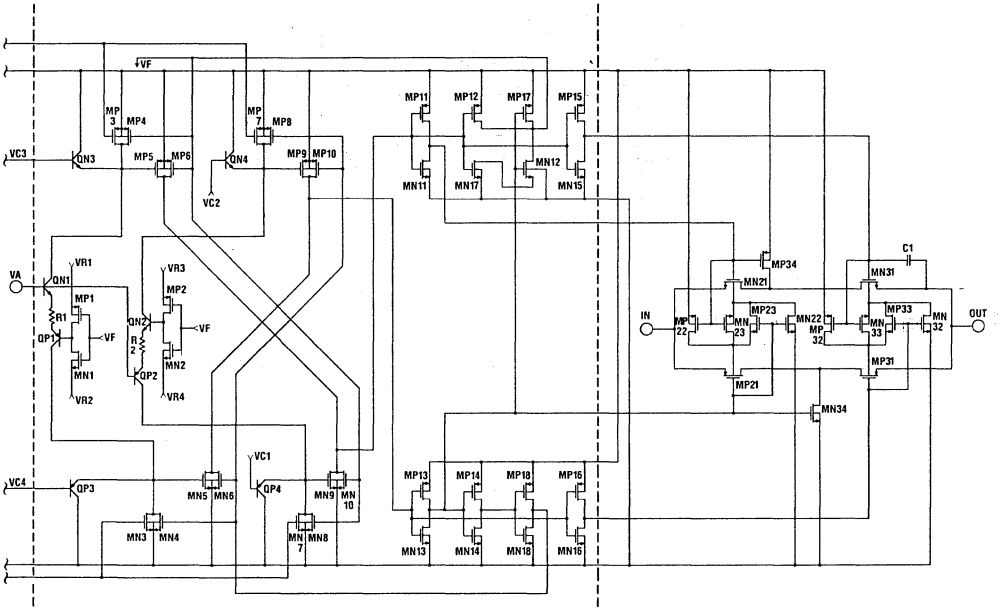
Schematic Diagram

BIAS NETWORK



LEVEL SHIFTER

SWITCH



HI-300 thru HI-307

CMOS Analog Switches

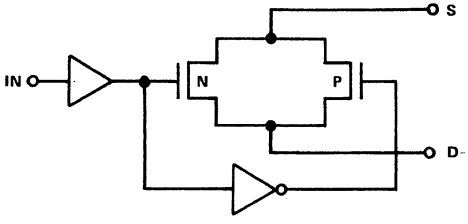
Features

- Analog Signal Range (±15V Supplies) ..... ±15V
- Low Leakage (Typical @ +25°C) 40pA
- Low Leakage (Typical @ +125°C) 1nA
- Low On Resistance (Typical @ +25°C) 35Ω
- Break-Before-Make Delay (Typical) 60ns
- Charge Injection 30pC
- TTL, CMOS Compatible
- Symetrical Switch Elements
- Low Operating Power ..... 1.0mW (Typical for HI-300 - 303)

Applications

- Sample and Hold i.e. Low Leakage Switching
- Op Amp Gain Switching i.e. Low On Resistance
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Functional Diagram



TYPICAL SWITCH 300 SERIES

Description

The HI-300 through HI-307 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These switches feature break-before-make switching, (HI-301, 303, 305 & 307 only), low and nearly constant ON resistance over the full analog signal range, and low power dissipation, (a few milliwatts for the HI-300 - 303, a few hundred microwatts for the HI-304 - 307).

The HI-300 - 303 are TTL compatible and have a logic "0" condition with an input less than 0.8V and a logic "1" condition with an input greater than 4.0V. The HI-304 - 307 switches are CMOS compatible and have a low state with an input less than 3.5V and a high state with an input greater than 11V. (See pinouts for switch conditions with a logic "1" input.)

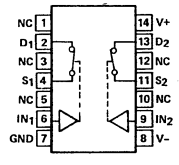
All the devices are available in a 14 pin Epoxy or Ceramic DIP. The HI-300, 301, 304 and 305 are also available in a 10 pin Metal Can. Each of the switch types are available in either the -55°C to +125°C or 0°C to +75°C operating ranges.

Pinouts (SWITCH STATES ARE FOR A LOGIC "1" INPUT)

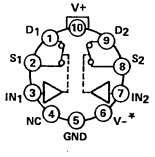
DUAL SPST HI-300 & HI-304

TOP VIEWS

DIP



METAL CAN



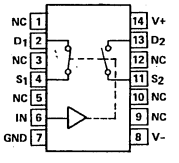
LOGIC	SWITCH
0	OFF
1	ON

* The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

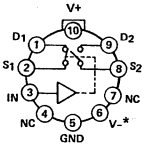
SPDT HI-301 & HI-305

TOP VIEWS

DIP



METAL CAN



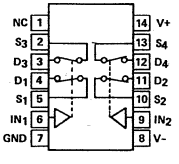
LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

* The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

DUAL DPST HI-302 & HI-306

TOP VIEW

DIP

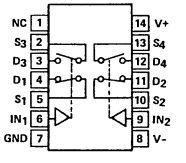


LOGIC	SWITCH
0	OFF
1	ON

DUAL SPDT HI-303 & HI-307

TOP VIEW

DIP



LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Specifications HI-300 - HI-307

Absolute Maximum Ratings (Note 1)

Voltage Between Supplies ..... 44V (±22)
Digital Input Voltage ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Analog Input Voltage ..... $+V_{SUPPLY}$ +1.5V
$-V_{SUPPLY}$ -1.5V
Total Power Dissipation* 14 Pin Epoxy DIP 526mW
14 Pin Ceramic DIP 588mW
10 Pin Metal Can* 435mW

Operating Temperature Range

HI-3XX-2 ..... -55°C to +125°C
HI-3XX-5 ..... 0°C to +75°C
Storage Temperature ..... -65°C to +150°C

*Derate 6.9mW/0°C Above T_A = +70°C

Electrical Specifications

Unless Otherwise Specified: Supplies = +15V, -15V; V_{IN} = Logic Input.
HI-300-303: V_{IN} - for Logic "1" = 4V, for Logic "0" = 0.8V
HI-304-307: V_{IN} - for Logic "1" = 11V, for Logic "0" = 3.5V

PARAMETER	TEMP	-55°C To +125°C			0°C To +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15	-	+15	-15	-	+15	V
R_{ON}, On Resistance (Note 2)	+25°C	-	35	50	-	35	50	Ω
	Full	-	40	75	-	40	75	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 3)	+25°C	-	0.04	1	-	0.04	5	nA
	Full	-	1	100	-	0.2	100	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 3)	+25°C	-	0.04	1	-	0.04	5	nA
	Full	-	1	100	-	0.2	100	nA
$I_{D(ON)}$, On Leakage Current (Note 4)	+25°C	-	0.03	1	-	0.03	5	nA
	Full	-	0.5	100	-	0.2	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{INL}, Input Low Level*	Full	-	-	0.8	-	-	0.8	V
V_{INH}, Input High Level*	Full	4	-	-	4	-	-	V
V_{INL}, Input Low Level**	Full	-	-	3.5	-	-	3.5	V
V_{INH}, Input High Level**	Full	11	-	-	11	-	-	V
I_{INL}, Input Leakage Current (Low) (Note 5)	Full	-	-	1	-	-	1	µA
I_{INH}, Input Leakage Current (High) (Note 5)	Full	-	-	1	-	-	1	µA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break-Before Make Delay***	+25°C	-	60	-	-	60	-	ns
t_{ON}, Switch On Time*	+25°C	-	210	300	-	210	300	ns
t_{OFF}, Switch Off Time*	+25°C	-	160	250	-	160	250	ns
t_{ON}, Switch Off Time**	+25°C	-	160	250	-	160	250	ns
t_{OFF}, Switch Off Time**	+25°C	-	100	150	-	100	150	ns
"Off Isolation" (Note 6)	+25°C	-	60	-	-	60	-	dB
Charge Injection (Note 7)	+25°C	-	3	-	-	3	-	mV
$C_{S(OFF)}$, Input Switch Capacitance	+25°C	-	16	-	-	16	-	pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C	-	14	-	-	14	-	pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C	-	35	-	-	35	-	pF
C_{IN}, (High) Digital Input Capacitance	+25°C	-	5	-	-	5	-	pF
C_{IN}, (Low) Digital Input Capacitance	+25°C	-	5	-	-	5	-	pF
POWER REQUIREMENTS								
I^+, Current* (Note 8)	+25°C	-	0.09	0.5	-	0.09	0.5	mA
	Full	-	-	1	-	-	1	mA
I^-, Current* (Note 8)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
I^+, Current* (Note 9)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
I^-, Current* (Note 9)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
I^+, Current** (Note 10)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
I^-, Current** (Note 10)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
I^+, Current** (Note 11)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
I^-, Current** (Note 11)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA

*HI-300 Thru HI-303 Only; **HI-304 Thru HI-307 Only; ***HI-301, HI-303, HI-305, HI-307 Only

Electrical Specifications Notes:

1. As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.
2. V_S = ±10V, I_{OUT} = -10mA. On resistance derived from the voltage measured across the switch under the above conditions.
3. V_S = ±14V, V_D = ±14V.
4. $V_S = V_D$ = ±14V.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. $V_S = 1V_{RMS}$, f = 500kHz, C_L = 15pF, R_L = 1k.
7. V_S = 0V, C_L = 10,000pF, Logic Drive = 5V pulse. (HI-300 - 303) Switches are symmetrical; S and D may be interchanged. Logic Drive = 15V (HI-304 - 307).
8. V_{IN} = 4V (One Input) (All Other Inputs = 0V).
9. V_{IN} = 0.8V (All Inputs).
10. V_{IN} = 15V (All Inputs).
11. V_{IN} = 0V (All Inputs).
12. To drive from DTL/TTL circuits, pull-up resistors to +5V supply are recommended.

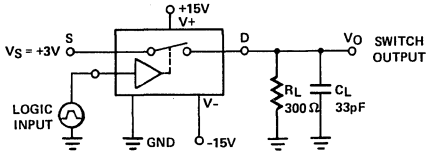
Test Circuits

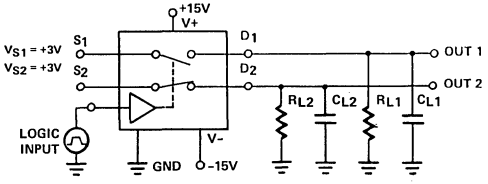
SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})

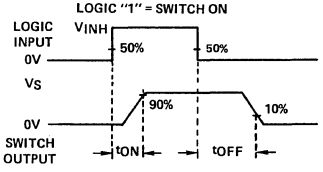
SWITCH TYPE	V_{INH}
HI-300 thru HI-303	4V
HI-304 thru HI-307	15V

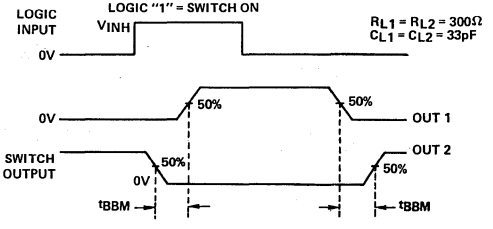
BREAK-BEFORE-MAKE TEST CIRCUIT (t_{BBM})

SWITCH TYPE	V_{INH}
HI-301, HI-303	5V
HI-305, HI-307	15V







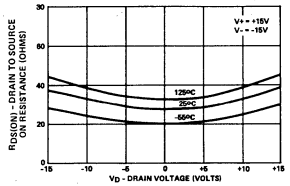


Ordering Information

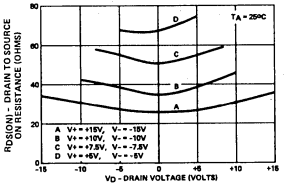
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI2-0304-5	0°C to +75°C	10-Pin Metal Can
HI2-0304-2	-55°C to +125°C	10-Pin Metal Can
HI1-0304-5	0°C to +75°C	14-Pin CERDIP
HI1-0304-2	-55°C to +125°C	14-Pin CERDIP
HI1-0305-2	-55°C to +125°C	14-Pin CERDIP
HI2-0305-5	0°C to +75°C	10-Pin Metal Can
HI2-0305-2	-55°C to +125°C	10-Pin Metal Can
HI1-0305-5	0°C to +75°C	14-Pin CERDIP
HI1-0306-5	0°C to +75°C	14-Pin CERDIP
HI1-0306-2	-55°C to +125°C	14-Pin CERDIP
HI1-0307-5	0°C to +75°C	14-Pin CERDIP
HI1-0307-2	-55°C to +125°C	14-Pin CERDIP

Typical Performance Curves

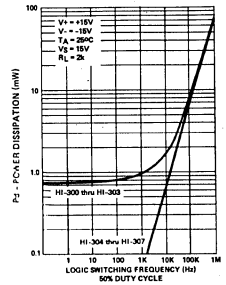
$R_{DS(ON)}$ vs. V_D and Temperature



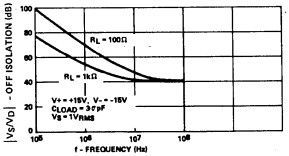
$R_{DS(ON)}$ vs. V_D and Power Supply Voltage



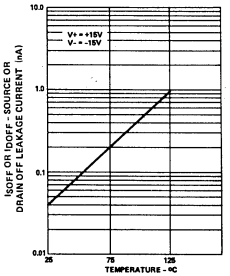
Device Power Dissipation vs. Switching Frequency Single Logic Input



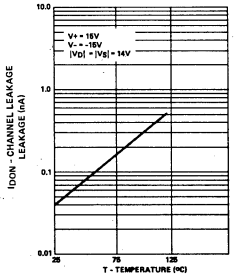
Off Isolation vs. Frequency



$I_{S(OFF)}$ or $I_{D(OFF)}$ vs. Temperature *

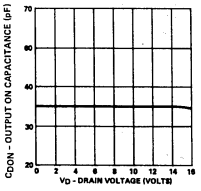


$I_{D(ON)}$ vs. Temperature *

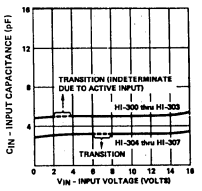


* The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

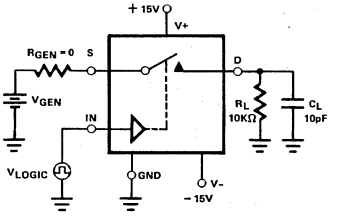
Output On Capacitance vs. Drain Voltage



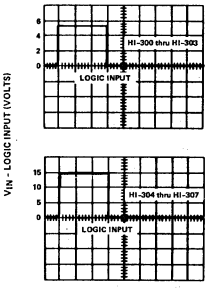
Digital Input Capacitance vs. Input Voltage

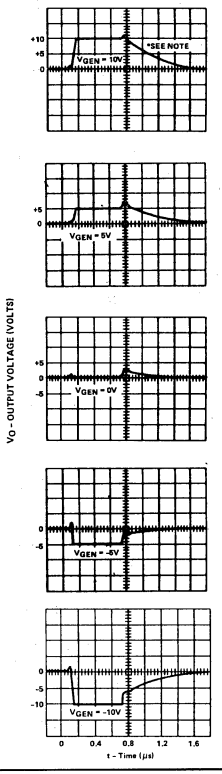


Typical delay, rise, fall, settling times, and switching transients in this circuit.



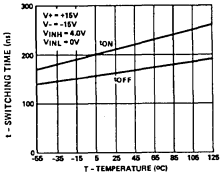
If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



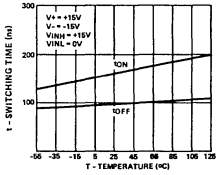


Typical Performance Curves (Continued)

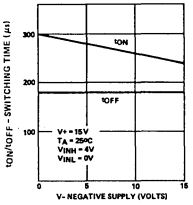
SWITCHING TIME VS. TEMPERATURE HI-300 thru HI-303



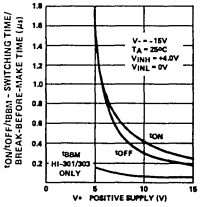
SWITCHING TIME VS. TEMPERATURE HI-304 thru HI-307



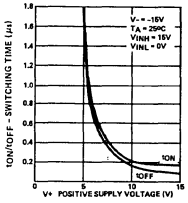
SWITCHING TIME VS. NEGATIVE SUPPLY VOLTAGE HI-300 thru HI-303



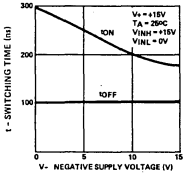
SWITCHING TIME AND BREAK BEFORE MAKE TIME VS. POSITIVE SUPPLY VOLTAGE HI-300 thru HI-303



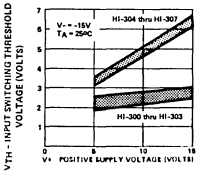
SWITCHING TIME VS. POSITIVE SUPPLY VOLTAGE HI-304 thru HI-307



SWITCHING TIME VS. NEGATIVE SUPPLY VOLTAGE HI-304 thru HI-307

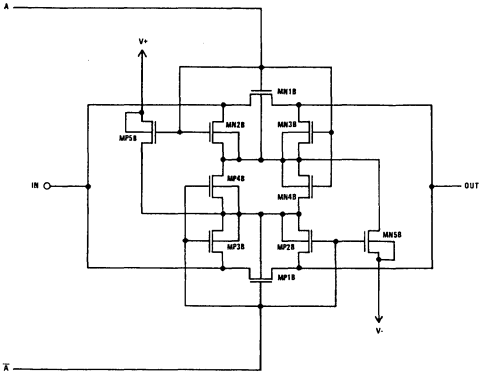


INPUT SWITCHING THRESHOLD VS. POSITIVE SUPPLY VOLTAGE HI-300 thru HI-307

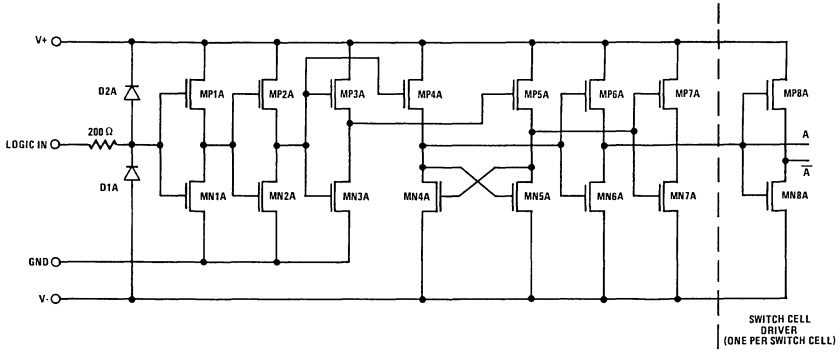


Schematic Diagrams

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



HI-381/384/387/390

CMOS Analog Switches

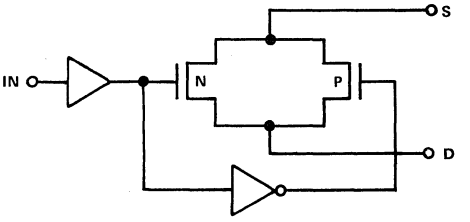
Features

- Analog Signal Range (±15V Supplies) ..... ±15V
- Low Leakage (Typical @ +25°C) 40pA
- Low Leakage (Typical @ +125°C) 1nA
- Low On Resistance (Typical @ +25°C) 35Ω
- Break-Before-Make Delay (Typical) 60ns
- Charge Injection 30pC
- TTL Compatible
- Symetrical Switch Elements
- Low Operating Power 1.0mW

Applications

- Sample and Hold i.e. Low Leakage Switching
- Op Amp Gain Switching i.e. Low On Resistance
- Portable Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Functional Diagram



TYPICAL SWITCH 300 SERIES

Description

The HI-381 through HI-390 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These devices are TTL compatible and are available in four switching configurations. (See device pinout for particular switching function with a logic "1" input.)

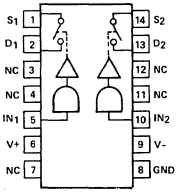
These switches feature low leakage and supply currents, low and nearly constant ON resistance over the analog signal range, break-before-make switching and low power dissipation.

The HI-381 and HI-387 switches are available in a 14 pin Epoxy or Ceramic DIP or 10 pin Metal Can. The HI-384 and HI-390 are available in a 16 pin Epoxy or Ceramic DIP. Each of the individual switch types are available in the -55°C to +125°C and 0°C to +75°C operating ranges.

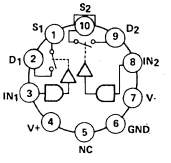
Pinouts (SWITCH STATES ARE FOR A LOGIC "1" INPUT)

DUAL SPST HI-381
TOP VIEWS

DIP



METAL CAN

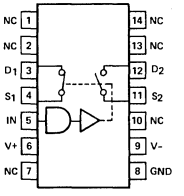


LOGIC	SW 1-2
0	OFF
1	ON

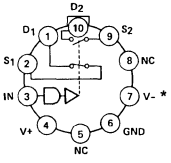
* The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

SPDT HI-387
TOP VIEWS

DIP



METAL CAN

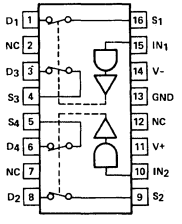


LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

* The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

DUAL DPST HI-384
TOP VIEW

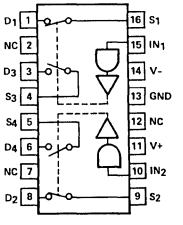
DIP



LOGIC	SW 1-4
0	OFF
1	ON

DUAL SPDT HI-390
TOP VIEW

DIP



LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Voltage Between Supplies ..... 44V (±22)
Digital Input Voltage ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Analog Input Voltage ..... $+V_{SUPPLY}$ +1.5V
$-V_{SUPPLY}$ -1.5V
Total Power Dissipation* 14 Pin Epoxy DIP 526mW
14 Pin Ceramic DIP 588mW
16 Pin Epoxy DIP 625mW
16 Pin Ceramic DIP 685mW
10 Pin Metal Can* 435mW

Operating Temperature Range

HI-3XX-2 ..... -55°C to +125°C
HI-3XX-5 ..... 0°C to +75°C
Storage Temperature ..... -65°C to +150°C

*Derate 6.9mW/°C Above T_A = +70°C

Electrical Specifications

Unless Otherwise Specified: Supplies = +15V, -15V; V_{IN} = Logic Input.
V_{IN} for Logic "1" = 4V, for Logic "0" = 0.8V

PARAMETER	TEMP	-55°C to +125°C			0°C to +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15	-	+15	-15	-	+15	V
R_{ON}, On Resistance (Note 2)	+25°C	-	35	50	-	35	50	Ω
	Full	-	40	75	-	40	75	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 3)	+25°C	-	0.04	1	-	0.04	5	nA
	Full	-	1	100	-	0.2	100	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 3)	+25°C	-	0.04	1	-	0.04	5	nA
	Full	-	1	100	-	0.2	100	nA
$I_{D(ON)}$, On Leakage Current (Note 4)	+25°C	-	0.03	1	-	0.03	5	nA
	Full	-	0.5	100	-	0.2	100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{INL}, Input Low Level	Full	-	-	0.8	-	-	0.8	V
V_{INH}, Input High Level	Full	4	-	-	4	-	-	V
I_{INL}, Input Leakage Current (Low) (Note 5)	Full	-	-	1	-	-	1	µA
I_{INH}, Input Leakage Current (High) (Note 5)	Full	-	-	1	-	-	1	µA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break-Before Make Delay (HI-387/390 Only)	+25°C	-	60	-	-	60	-	ns
t_{ON}, Switch On Time	+25°C	-	210	300	-	210	300	ns
t_{OFF}, Switch Off Time	+25°C	-	160	250	-	160	250	ns
"Off Isolation" (Note 6)	+25°C	-	60	-	-	60	-	dB
Charge Injection (Note 7)	+25°C	-	3	-	-	3	-	mV
$C_{S(OFF)}$, Input Switch Capacitance	+25°C	-	16	-	-	16	-	pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C	-	14	-	-	14	-	pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C	-	35	-	-	35	-	pF
C_{IN}, (High) Digital Input Capacitance	+25°C	-	5	-	-	5	-	pF
C_{IN}, (Low) Digital Input Capacitance	+25°C	-	5	-	-	5	-	pF
POWER REQUIREMENTS								
I^+, Current (Note 8)	+25°C	-	0.09	0.5	-	0.09	0.5	mA
	Full	-	-	1	-	-	1	mA
I^-, Current (Note 8)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
I^+, Current (Note 9)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
I^-, Current (Note 9)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA

Electrical Specifications Notes:

1. As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.
2. V_S = ±10V, I_{OUT} = -10mA. On resistance derived from the voltage measured across the switch under the above conditions.
3. $-V_S$ = ±14V, V_D = ±14V.
4. $V_S = V_D$ = ±14V.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. $V_S = 1V_{RMS}$, f = 500kHz, C_L = 15pF, R_L = 1k, $C_L = C_{FIXTURE} + C_{PROBE}$, "off isolation" = $20_{Log}\ V_S/V_D$.
7. V_S = 0V, C_L = 10,000pF, Logic Drive = 5V pulse. Switches are symmetrical; S and D may be interchanged.
8. V_{IN} = 4V (One Input) (All Other Inputs = 0V).
9. V_{IN} = 0.8V (All Inputs).
10. To drive from DTL/TTL circuits, pull-up resistors to +5V supply are recommended.

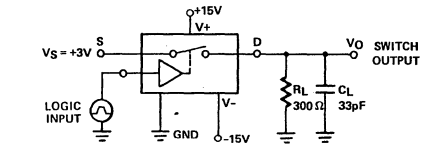
Test Circuits

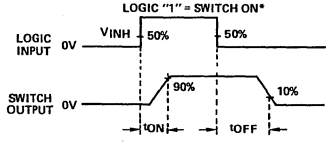
SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})

SWITCH TYPE	V_{INH}
HI-381 thru HI-390	5V

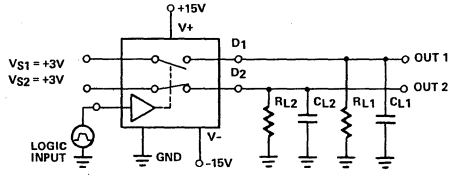
BREAK-BEFORE-MAKE TEST CIRCUIT (t_{BBM})

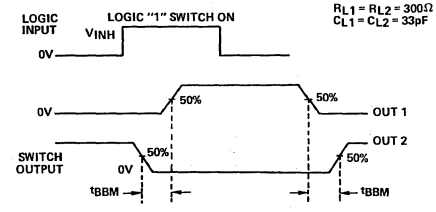
SWITCH TYPE	V_{INH}
HI-387, HI-390	5V





*INVERTED LOGIC FOR HI-381



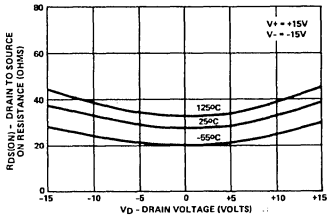


Ordering Information

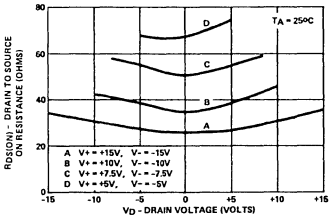
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0381-5	0°C to +75°C	14-Pin CERDIP
HI1-0381-2	-55°C to +125°C	14-Pin CERDIP
HI2-0381-2	-55°C to +125°C	10-Pin Metal Can
HI2-0381-5	0°C to +75°C	10-Pin Metal Can
HI1-0384-5	0°C to +75°C	16-Pin CERDIP
HI1-0384-2	-55°C to +125°C	16-Pin CERDIP
HI2-0387-2	-55°C to +125°C	10-Pin Metal Can
HI1-0387-2	-55°C to +125°C	16-Pin CERDIP
HI1-0387-5	0°C to +75°C	16-Pin CERDIP
HI2-0387-5	0°C to +75°C	10-Pin Metal Can
HI1-0390-5	0°C to +75°C	16-Pin CERDIP
HI1-0390-2	-55°C to +125°C	16-Pin CERDIP

HI-381/384/387/390 Typical Performance Curves

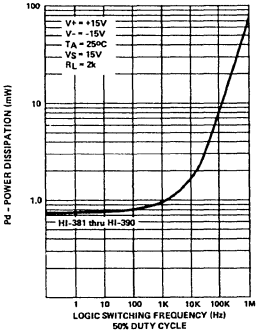
$R_{DS(ON)}$ VS. V_D AND TEMPERATURE



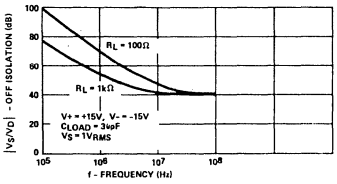
$R_{DS(ON)}$ VS. V_D AND POWER SUPPLY VOLTAGE



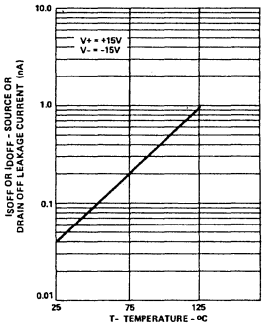
DEVICE POWER DISSIPATION VS. SWITCHING FREQUENCY SINGLE LOGIC INPUT



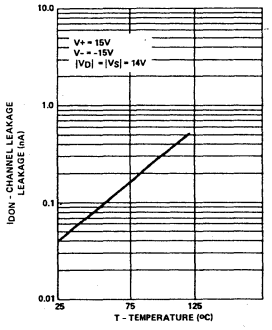
OFF ISOLATION VS. FREQUENCY



I_{SOFF} OR I_{DOFF} VS. TEMPERATURE*

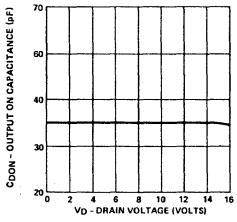


I_{DON} VS. TEMPERATURE*

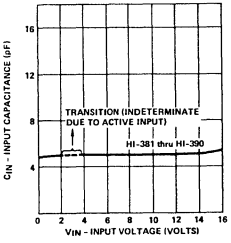


* The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

OUTPUT ON CAPACITANCE VS. DRAIN VOLTAGE

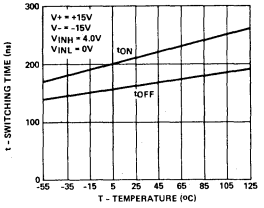


DIGITAL INPUT CAPACITANCE VS. INPUT VOLTAGE

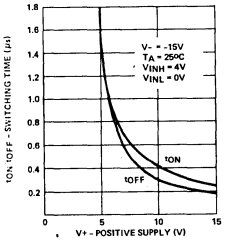


HI-381/384/387/390 Typical Performance Curves (Continued)

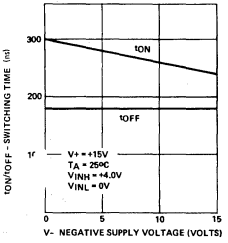
SWITCHING TIME vs. TEMPERATURE HI-381 THRU HII-390



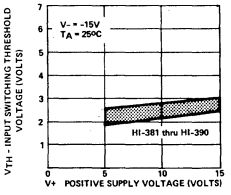
SWITCHING TIME vs. POSITIVE SUPPLY VOLTAGE HI-381 THRU HI-390



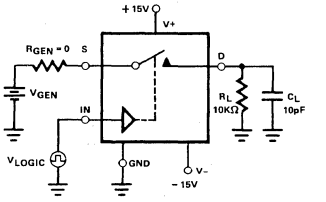
SWITCHING TIME vs. NEGATIVE SUPPLY VOLTAGE HI-381 THRU HI-390



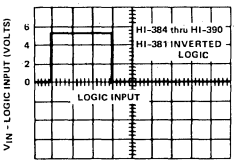
INPUT SWITCHING THRESHOLD vs. POSITIVE SUPPLY VOLTAGE HI-381 THRU HI-390

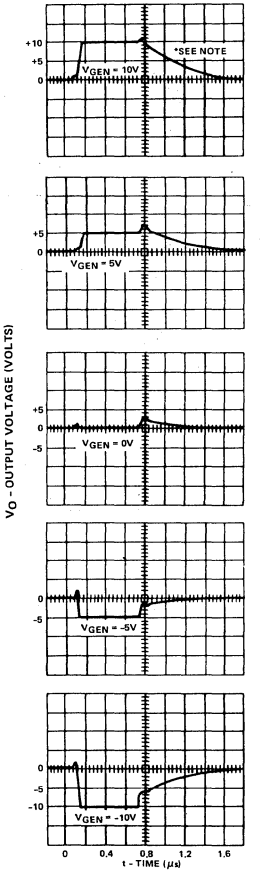


Typical delay, rise, fall, settling times, and switching transients in this circuit.



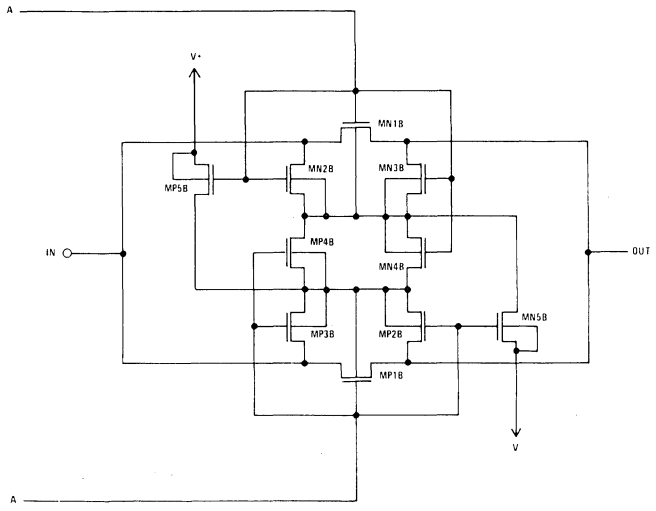
If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



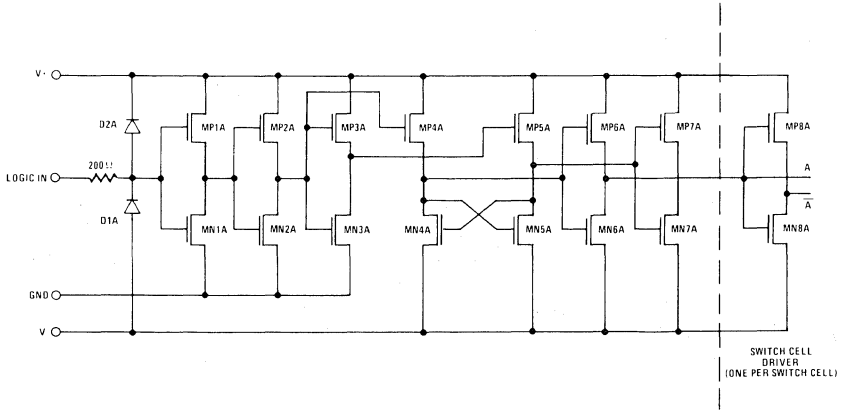


* NOTE: The turn-off time is primarily limited here by the RC time constant (100ns) of the load.

Schematic Diagrams



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



HARRIS HI-5040 thru HI-5051 HI-5046A and HI-5047A

September 1991

CMOS Analog Switches

Features

- Wide Analog Signal Range ..... ±15V
- Low "ON" Resistance (Typical) 25Ω
- High Current Capability (Typical) 80mA
- Break-Before-Make Switching
  - Turn-On Time (Typical) 370ns
  - Turn-Off Time (Typical) 280ns
- No Latch-Up
- Input MOS Gates Are Protected From Electrostatic Discharge
- DTL, TTL, CMOS, PMOS Compatible

Applications

- High Frequency Switching
- Sample and Hold
- Digital Filters
- Operational Amplifier Gain Switching

Description

This family of CMOS analog switches offers low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 80mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 25Ω for HI-5048 through HI-5051 and HI-5046A/5047A and 50Ω for HI-5040 through HI-5047.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at +25°C). This family of switches also features very low power operation (1.5mW at +25°C).

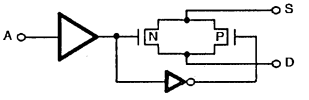
There are 14 devices in this switch series which are differentiated by type of switch action and value of R_{ON} (see Functional Diagram). All devices are available in 16 pin DIP packages. The HI-5040/5050 switches can directly replace IH-5040 series devices except IH5048, and are functionally compatible with the DG 180/190 family. Each switch type is available in the -55°C to +125°C and 0°C to +75°C performance grades.

Functional Description

PART NUMBER	TYPE	R_{ON}
HI-5040	SPST	75Ω
HI-5041	DUAL SPST	75Ω
HI-5042	SPDT	75Ω
HI-5043	DUAL SPDT	75Ω
HI-5044	DPST	75Ω
HI-5045	DUAL DPST	75Ω
HI-5046	DPDT	75Ω
HI-5046A	DPDT	25Ω
HI-5047	4PST	75Ω
HI-5047A	4PST	25Ω
HI-5048	DUAL SPST	25Ω
HI-5049	DUAL DPST	25Ω
HI-5050	SPDT	25Ω
HI-5051	DUAL SPDT	25Ω

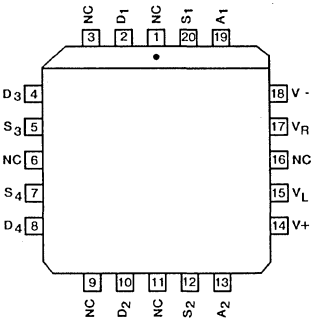
Functional Diagram

TYPICAL DIAGRAM

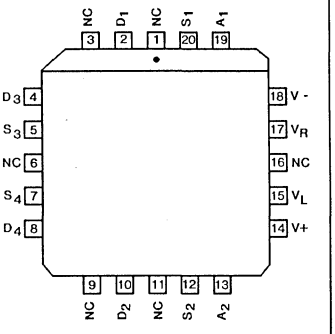


Pinouts

HI-5043/51 20 LEAD PLCC
TOP VIEW



HI-5045/49 20 LEAD PLCC
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings

Supply Voltage (V+, V–) 36V
V_R to Ground ..... V+, V–
Digital and Analog Input Voltage ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Analog Current (S to D) Continous 30mA
Analog Current (S to D) Peak 80mA
Total Power Dissipation* 450mW

Operating Temperature Range

HI-50XX-2 ..... -55°C to +125°C
HI-50XX-5 ..... 0°C to +75°C
Storage Temperature ..... -65°C to +150°C

*Derate 6mW/°C Above T_A = +75°C

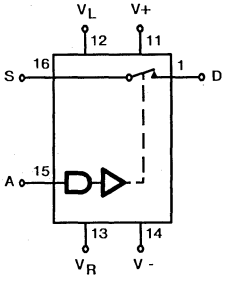
Electrical Specifications Unless Otherwise Specified Supplies = +15V, -15V; V_R = 0V; V_{AH} (Logic Level High) = 3.0V, V_{AL} (Logic Level Low) = +0.8V, V_L = +5V For Test Conditions, Consult Performance Characteristics, Unused Pins are Grounded.

PARAMETER	TEMP	-55°C To +125°C			0°C To +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15	–	+15	-15	–	+15	V
R_{ON}, On Resistance (Note 1a)	+25°C	–	50	–	–	50	–	Ω
	Full	–	–	75	–	–	75	Ω
R_{ON}, On Resistance (Note 1b)	+25°C	–	25	–	–	25	–	Ω
	Full	–	–	50	–	–	50	Ω
R_{ON}, Channel-to-Channel Match (Note 1a)	+25°C	–	2	10	–	2	10	Ω
R_{ON}, Channel-to-Channel Match (Note 1b)	+25°C	–	1	5	–	1	5	Ω
$I_{S(OFF)} = I_{D(OFF)}$, Off Input or Output	+25°C	–	0.8	–	–	0.8	–	nA
Leakage Current	Full	–	100	500	–	100	500	nA
$I_{D(ON)}$, On Leakage Current	+25°C	–	0.01	–	–	0.01	–	nA
	Full	–	2	500	–	2	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full	–	–	0.8	–	–	0.8	V
V_{AH}, Input High Threshold	Full	3.0	–	–	3.0	–	–	V
I_A, Input Leakage Current (High or Low)	Full	–	0.01	1.0	–	0.01	1.0	µA
SWITCHING CHARACTERISTICS								
t_{ON}, Switch On Time	+25°C	–	370	1000	–	370	1000	ns
t_{OFF}, Switch Off Time	+25°C	–	280	500	–	280	500	ns
Charge Injection (Note 2)	+25°C	–	5	20	–	5	–	mV
"Off Isolation" (Note 3)	+25°C	75	80	–	–	80	–	dB
"Crosstalk" (Note 3)	+25°C	80	88	–	–	88	–	dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C	–	11	–	–	11	–	pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C	–	11	–	–	11	–	pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C	–	22	–	–	22	–	pF
C_A, Digital Input Capacitance	+25°C	–	5	–	–	5	–	pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C	–	0.5	–	–	0.5	–	pF
POWER REQUIREMENTS								
P_D, Quiescent Power Dissipation	+25°C	–	1.5	–	–	1.5	–	mW
I^+, +15V Quiescent Current	Full	–	–	0.3	–	–	0.5	mA
I^-, -15V Quiescent Current	Full	–	–	0.3	–	–	0.5	mA
I_L, +5V Quiescent Current	Full	–	–	0.3	–	–	0.5	mA
I_R, Ground Quiescent Current	Full	–	–	0.3	–	–	0.5	mA

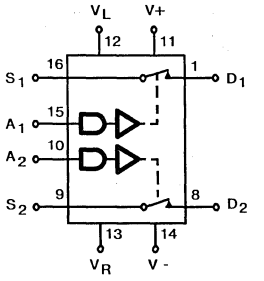
NOTES:
1. V_{OUT} = ±10V, I_{OUT} = 1mA
   a). For HI-5040 thru HI-5047
   b). For HI-5048 thru HI-5051, HI-5046A/5047A.
2. V_{IN} = 0V, C_L = 10,000pF.
3. R_L = 100Ω, f = 100kHz, V_{IN} = $2.0V_{p-p}$, C_L = 5pF.

Switch Functions SWITCH STATES ARE FOR LOGIC "1" INPUT

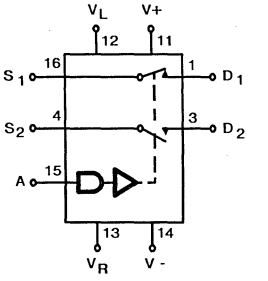
SPST
HI-5040 (75Ω)



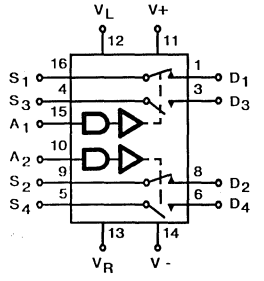
DUAL SPST
HI-5041 (75Ω)



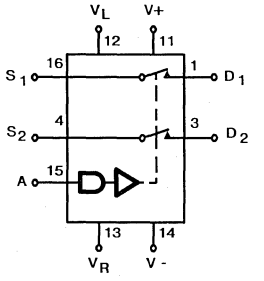
SPDT
HI-5042 (75Ω)



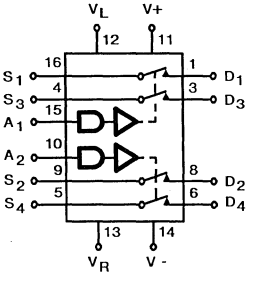
DUAL SPDT
HI-5043 (75Ω)



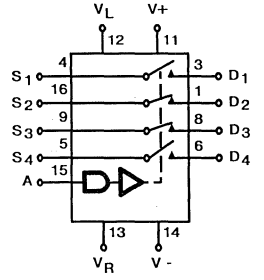
DPST
HI-5044 (75Ω)



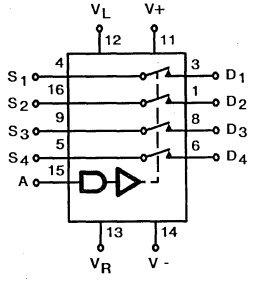
DUAL DPST
HI-5045 (75Ω)



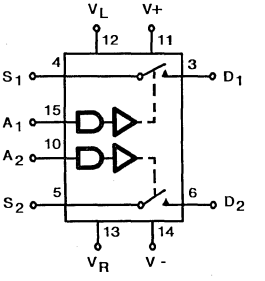
DPDT
HI-5046 (75Ω)
HI-5046A (25Ω)



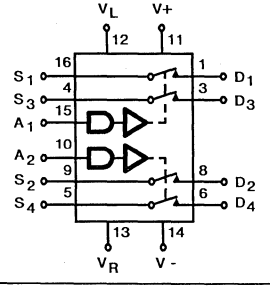
4PST
HI-5047 (75Ω)
HI-5047A (25Ω)



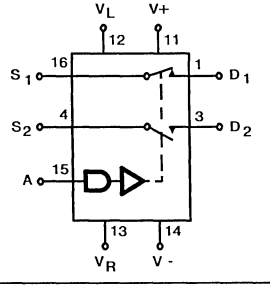
DUAL SPST
HI-5048 (25Ω)



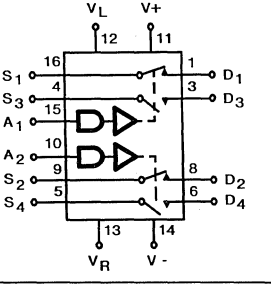
DUAL DPST
HI-5049 (25Ω)



SPDT
HI-5050 (25Ω)



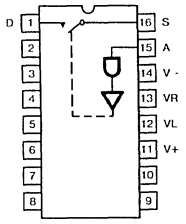
DUAL SPDT
HI-5051 (25Ω)



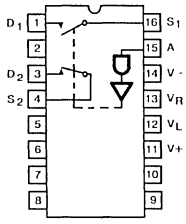
Pin Configurations SWITCH STATES ARE FOR LOGIC "0" INPUT

SINGLE CONTROL

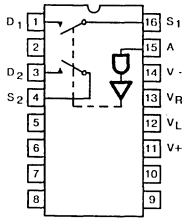
SPST
HI-5040 (75Ω)



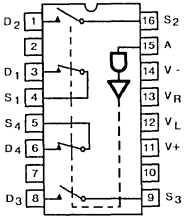
SPDT
HI-5042 (75Ω)
HI-5050 (25Ω)



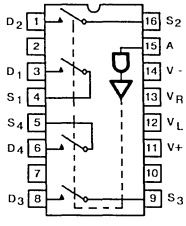
DPST
HI-5044 (75Ω)



DPDT
HI-5046 (75Ω)
HI-5046A (25Ω)

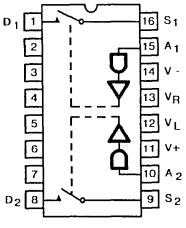


4PST
HI-5047 (75Ω)
HI-5047A(25Ω)

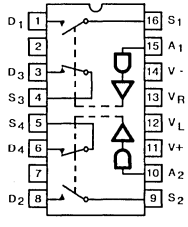


DUAL CONTROL

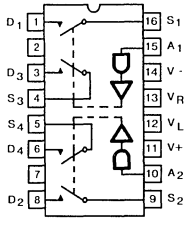
DUAL SPST
HI-5041 (75Ω)



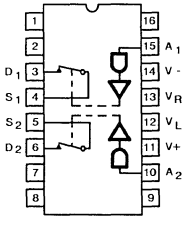
DUAL SPDT
HI-5043 (75Ω)
HI-5051 (25Ω)



DUAL DPST
HI-5045 (75Ω)
HI-5049 (25Ω)



DUAL SPST
HI-5048 (25Ω)

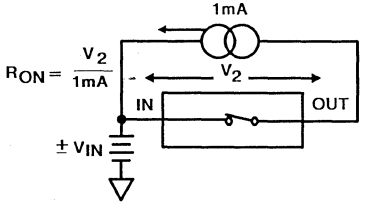


NOTE: Unused pins may be internally connected. Ground all unused pins.

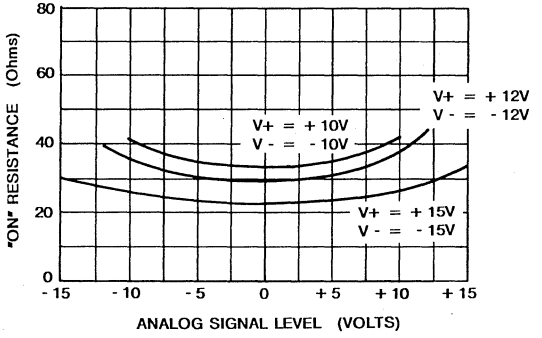
Performance Characteristics and Test Circuits

Unless Otherwise Specified: $T_A = +25^oC$, V+ = +15V, V- = -15V, $V_L = +5V$, $V_R = 0V$, $V_{AH} = 3.0V$ and $V_{AL} = 0.8V$

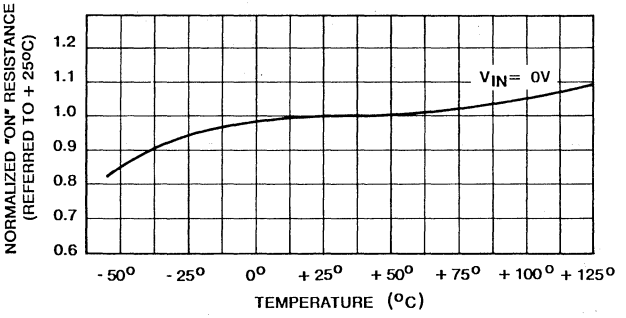
"ON" RESISTANCE vs. ANALOG SIGNAL LEVEL, SUPPLY VOLTAGE AND TEMPERATURE



"ON" RESISTANCE vs. ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

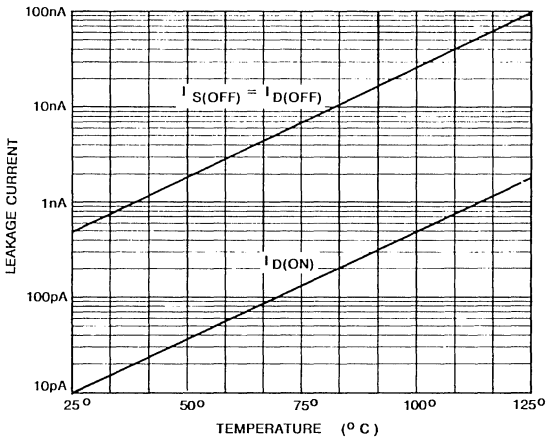


NORMALIZED "ON" RESISTANCE vs. TEMPERATURE

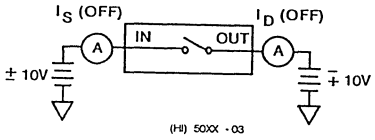


Performance Characteristics and Test Circuits (Continued)

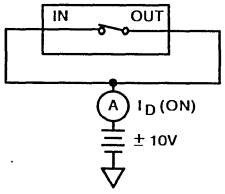
ON/OFF LEAKAGE CURRENT vs. TEMPERATURE



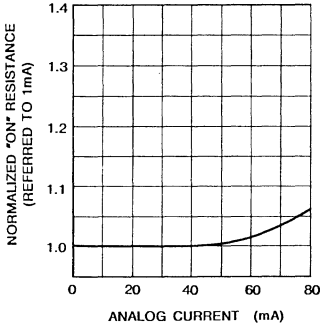
OFF LEAKAGE CURRENT vs. TEMPERATURE



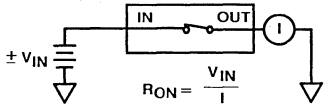
ON LEAKAGE CURRERT vs. TEMPERATURE



NORMALIZED "ON" RESISTANCE vs. ANALOG CURRENT

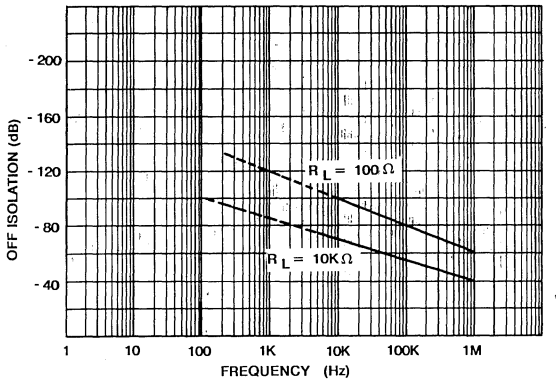


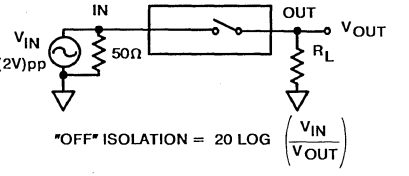
"ON" RESISTANCE vs. ANALOG CURRENT



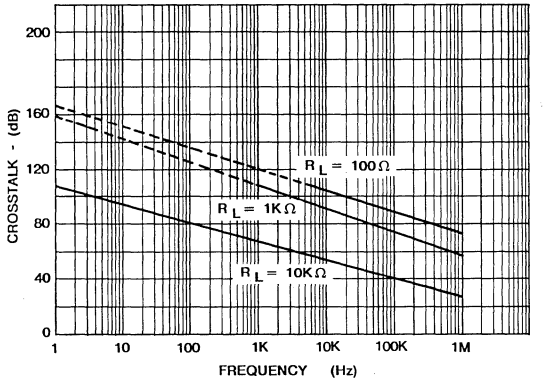
Performance Characteristics and Test Circuits (Continued)

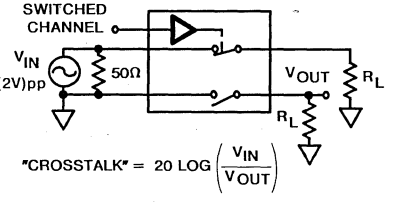
"OFF" ISOLATION vs. FREQUENCY



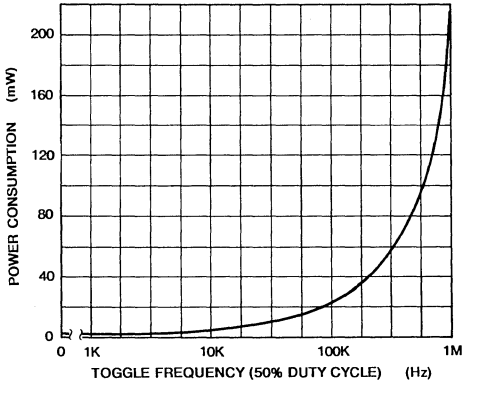


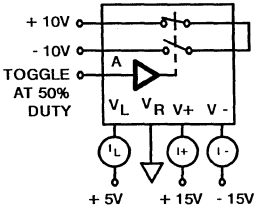
CROSSTALK vs. FREQUENCY





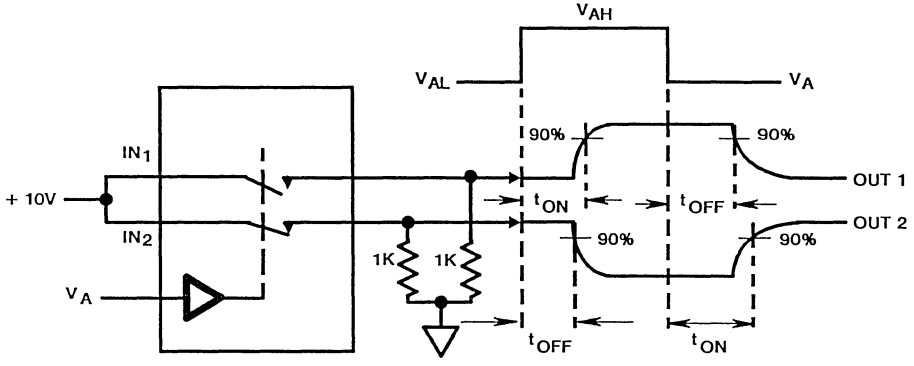
POWER CONSUMPTION vs. FREQUENCY



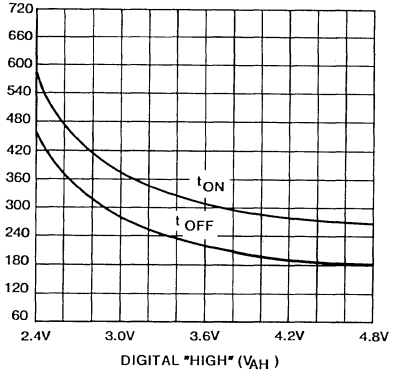


Switching Characteristics

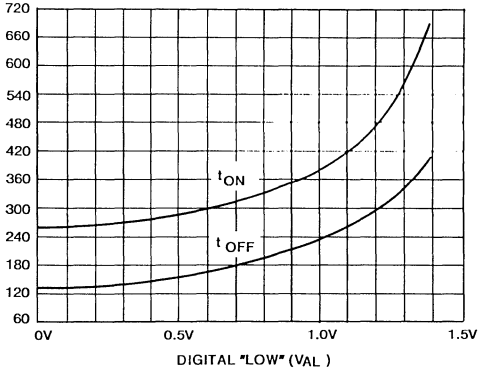
ON/OFF SWITCH TIME vs. LOGIC LEVEL



SWITCHING TIMES FOR POSITIVE DIGITAL TRANSITION

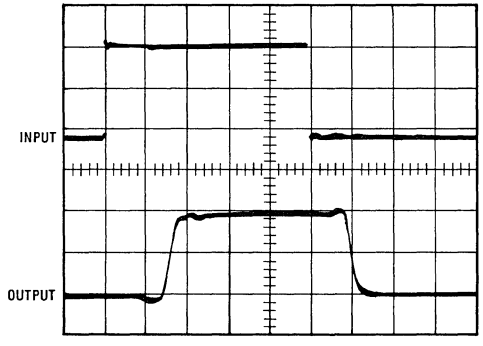


SWITCHING TIMES FOR NEGATIVE DIGITAL TRANSITION

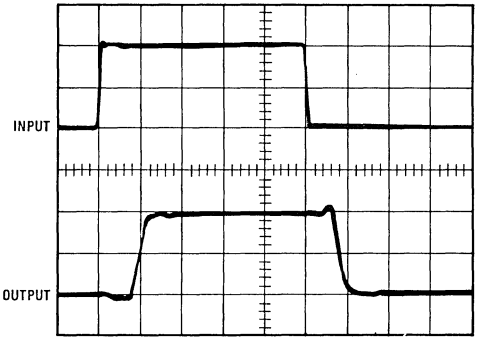


Switching Waveforms

Top: TTL Input (1V/Div.)
V_{AH} = 3V, V_{AL} = 0.8V
Bottom: Output (5V/Div.)
Horizontal: 200ns/Div.

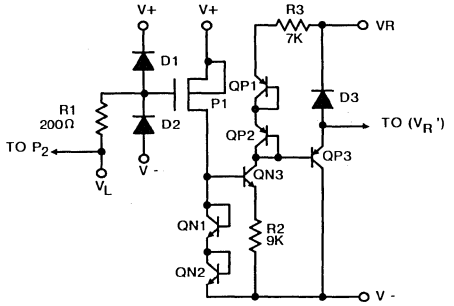


Top: CMOS Input (5V/Div.)
V_{AH} = 10V, V_{AL} = 0V
Bottom: Output (5V/Div.)
Horizontal: 200ns/Div.



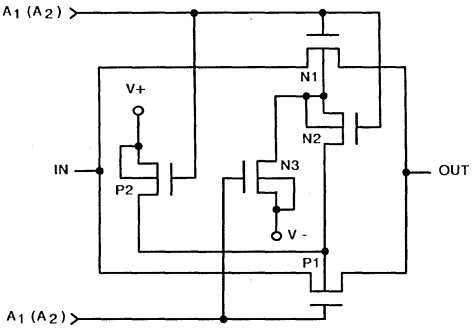
Switching Characteristics

TTL/CMOS REFERENCE CIRCUIT*

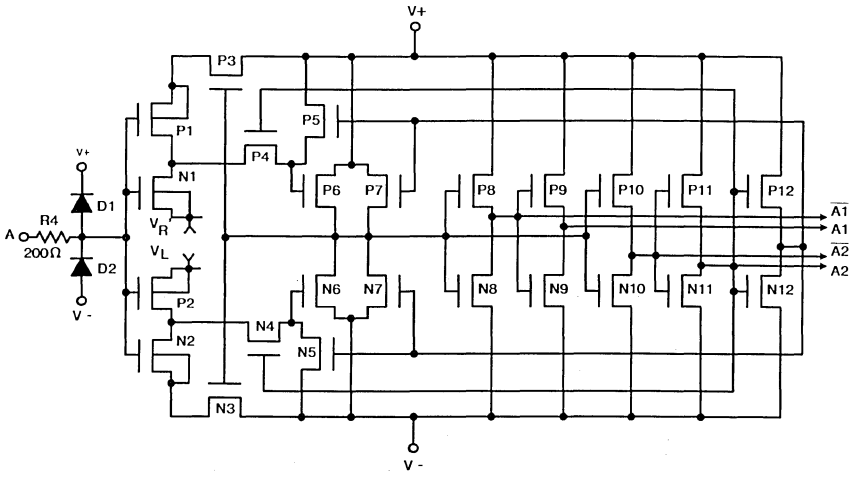


*Connect V+ to V_L for minimizing power consumption when driving from CMOS circuits

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



ALL N-CHANNEL
BODIES TO V-

ALL P-CHANNEL
BODIES TO V+

EXCEPT AS SHOWN

For Further Information Refer to Application Notes 520, 521, 531, 532, and 557 in Section 10 of Data Book.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-5040-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP
HI3-5040-5	0°C to +75°C	16-Pin Plastic DIP
HI1-5040-2	-55°C to +125°C	16-Pin CERDIP
HI1-5040-5	0°C to +75°C	16-Pin CERDIP
HI3-5041-5	0°C to +75°C	16-Pin Plastic DIP
HI1-5041-5	0°C to +75°C	16-Pin CERDIP
HI1-5041-2	-55°C to +125°C	16-Pin CERDIP
HI1-5041-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP
HI3-5042-5	0°C to +75°C	16-Pin Plastic DIP
HI1-5042-5	0°C to +75°C	16-Pin CERDIP
HI1-5042-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP
HI1-5042-2	-55°C to +125°C	16-Pin CERDIP
HI1-5043-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP
HI4P5043-5	0°C to +75°C	20-Pin PLCC
HI1-5043-2	-55°C to +125°C	16-Pin CERDIP
HI3-5043-5	0°C to +75°C	16-Pin Plastic DIP
HI1-5043-5	0°C to +75°C	16-Pin CERDIP
HI1-5044-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP
HI1-5044-5	0°C to +75°C	16-Pin CERDIP
HI3-5044-5	0°C to +75°C	16-Pin Plastic DIP
HI1-5044-2	-55°C to +125°C	16-Pin CERDIP
HI1-5045-5	0°C to +75°C	16-Pin CERDIP
HI1-5045-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP
HI1-5045-2	-55°C to +125°C	16-Pin CERDIP
HI3-5045-5	0°C to +75°C	16-Pin Plastic DIP
HI4P5045-5	0°C to +75°C	20-Pin PLCC
HI1-5046-2	-55°C to +125°C	16-Pin CERDIP
HI1-5046-5	0°C to +75°C	16-Pin CERDIP
HI1-5046-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP
HI3-5046-5	0°C to +75°C	16-Pin Plastic DIP
HI1-5046A-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP
HI3-5046A-5	0°C to +75°C	16-Pin Plastic DIP
HI1-5046A-2	-55°C to +125°C	16-Pin CERDIP
HI1-5046A-5	0°C to +75°C	16-Pin CERDIP
HI1-5047-5	0°C to +75°C	16-Pin CERDIP
HI1-5047-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP
HI1-5047-2	-55°C to +125°C	16-Pin CERDIP
HI3-5047-5	0°C to +75°C	16-Pin Plastic DIP
HI1-5047A-5	0°C to +75°C	16-Pin CERDIP
HI1-5047A-2	-55°C to +125°C	16-Pin CERDIP
HI3-5047A-5	0°C to +75°C	16-Pin Plastic DIP
HI1-5047A-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP
HI1-5048-5	0°C to +75°C	16-Pin CERDIP
HI1-5048-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP
HI3-5048-5	0°C to +75°C	16-Pin Plastic DIP
HI1-5048-2	-55°C to +125°C	16-Pin CERDIP
HI4P5049-5	0°C to +75°C	20-Pin PLCC
HI1-5049-5	0°C to +75°C	16-Pin CERDIP
HI1-5049-2	-55°C to +125°C	16-Pin CERDIP
HI3-5049-5	0°C to +75°C	16-Pin Plastic DIP
HI1-5049-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP
HI1-5050-5	0°C to +75°C	16-Pin CERDIP
HI1-5050-2	-55°C to +125°C	16-Pin CERDIP
HI3-5050-5	0°C to +75°C	16-Pin Plastic DIP
HI1-5050-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP
HI1-5051-5	0°C to +75°C	16-Pin CERDIP
HI1-5051-2	-55°C to +125°C	16-Pin CERDIP
HI1-5051-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP
HI4P5051-5	0°C to +75°C	20-Pin PLCC
HI3-5051-5	0°C to +75°C	16-Pin Plastic DIP

HARRIS SEMICONDUCTOR

IH401A
QUAD Varafet Analog Switch

GENERAL DESCRIPTION

The IH401A is made up of 4 monolithically constructed combinations of a varactor type diode and an N-channel JFET. The JFET itself is very similar to the popular 2N4391, and the driver diode is specially designed, such that its capacitance is a strong function of the voltage across it. The driver diode is electrically in series with the gate of the N-channel FET and simulates a back-to-back diode structure. This structure is needed to prevent forward biasing the source-to-gate or drain-to-gate junctions of the JFET when used in switching applications.

Previous applications of JFETs required the addition of diodes, in series with the gate, and then perhaps a gate-to-source referral resistor or a capacitor in parallel with the diode; therefore, at least 3 components were required to perform the switch function. The IH401A does this same job in one component (with a great deal better performance characteristics).

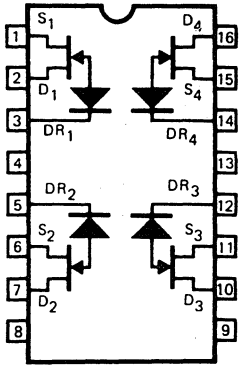
Like a standard JFET, to practically perform a solid state switch function a translator should be added to drive the diode. This translator takes the TTL levels and converts them to voltages required to drive the diode/FET system (typically a 0V to −15V translation and a 3V to +15V shift). With ±15V power supplies, the IH401A will typically switch $22V_{p\text{-}p}$ at any frequency from DC to 20MHz, with less than 50Ω $R_{DS(on)}$.

FEATURES

- $R_{DS(on)} = 35\Omega$ Typical
- $I_{D(off)}$ of 10pA Typical
- Switching Times of 25ns for t_{on} and 75ns for t_{off} ($R_L = 1k\Omega$)
- Built-In Overvoltage Protection (±25V)
- Charge Injection Error of 3mV Typical Into 0.01μF Capacitor
- $C_{iss} < 1pF$ Typical
- Can Be Used for Hybrid Construction

ORDERING INFORMATION

Part Number	Package
IH401A	CERDIP



0283-1

Figure 1: Pin Configuration (Outline Dwg JE)

7

NOTE: All typical values have been characterized but are not tested.

IH401A

ABSOLUTE MAXIMUM RATINGS

V_S to V_D 35V
V_G to V_S, V_D 35V
Operating Temperature ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS AT 25°C/125°C

Symbol	Characteristic	Test Conditions	IH401A			Units
			Min	Typ	Max	
$R_{DS(on)}$	Switch "on" Resistance	V_{DRIVE} = 15V, V_{DRAIN} = −10V, I_D = 10mA		35	50	Ω
V_P	Pinch-Off Voltage	I_D = 1nA, V_{DS} = 10V	2	4	5	V
$I_{D(off)}$	Switch "off" Current or "off" Leakage	V_{DRIVE} = −15V, V_{SOURCE} = −10V, V_{DRAIN} = +10V		10	±500	pA
$I_{D(off)}$	Switch "off" Leakage at 125°C	V_{DRIVE} = −15V, V_{SOURCE} = −10V, V_{DRAIN} = +10V		0.25	50	nA
$I_{S(off)}$	Switch "off" Current	V_{DRIVE} = −15V, V_{DRAIN} = −10V, V_{SOURCE} = +10V		10	±500	pA
$I_{S(off)}$	Switch "off" Leakage at 125°C	V_{DRIVE} = −15V, V_{SOURCE} = −10V, V_{DRAIN} = +10V		0.3	50	nA
$I_{D(on)} + I_{S(on)}$	Switch Leakage when Turned "on"	$V_D = V_S$ = −10V, V_{DRIVE} = +15V		0.02	±2	nA
V_{analog}	AC Input Voltage Range without Distortion	See Figure 3	20	22		V_{p-p}
V_{inject}	Charge Injection Amplitude	See Figure 4		3		mV_{p-p}
BV_{diode}	Diode Reverse Breakdown Voltage. This Correlates to Overvoltage Protection	$V_D = V_S$ = −V, I_{DRIVE} = 1μA, $_{DRIVE}$ = 0V	−30	−45		V
BV_{GSS}	Gate to Source or Gate to Drain Reverse Breakdown Voltage	V_{DRIVE} = −V, $V_D = V_S$ = 0V, $_{DRIVE}$ = 1μA	30	41		V
I_{DSS}	Maximum Current Switch can Deliver (Pulsed)	V_{DRIVE} = 15V, V_S = 0V, $_D$ = +10V	35	55		mA
t_{on}	Switch "on" time (Note 1)	See Figure 2		50		ns
t_{off}	Switch "off" time (Note 1)	See Figure 2		150		ns

NOTE: Driving waveform must be >100ns rise and fall time.

NOTE: All typical values have been characterized but are not tested.

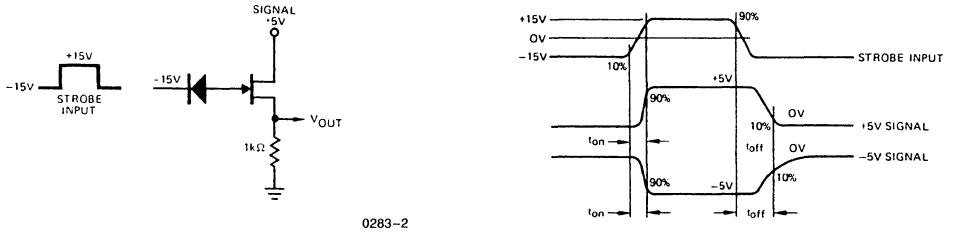


Figure 2: Switching Time Test Circuit and Waveforms

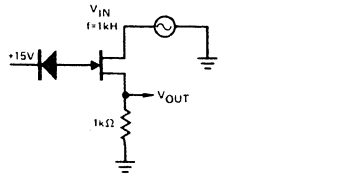


Figure 3: Analog Input Voltage Range Test Circuit

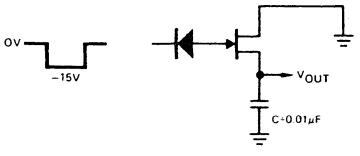


Figure 4: Charge Injection Test Circuit

APPLICATIONS

IH401 Family

In general, the IH401A family can be used in any application formally using a JFET/isolation diode combination (2N4391 or similar). Like standard FET circuits, the IH401A requires a translator for normal analog switch function. The translator is used to boost the TTL input signals to the ±15V analog supply levels which allow the IH401A to handle ±10V analog signals. A typical simple PNP translator is shown in Figure 5.

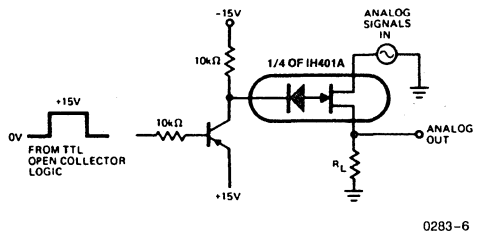


Figure 5

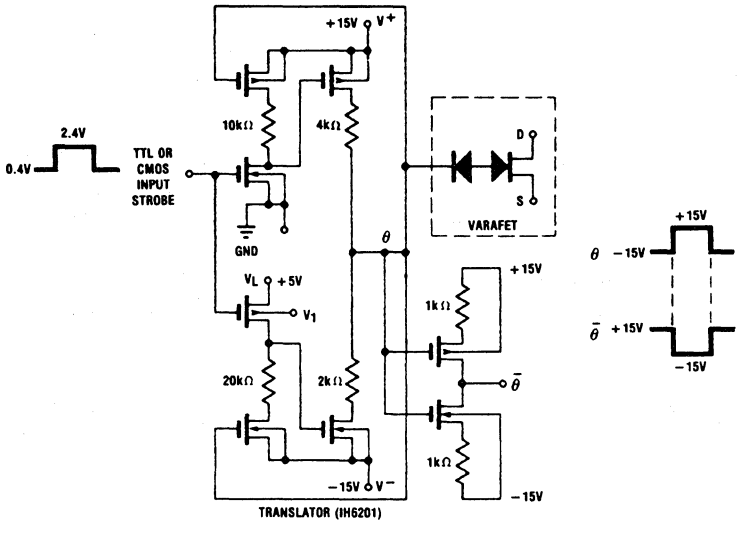
Although this simple PNP circuit represents a minimum of components, it requires open collector TTL input and $t_{(off)}$ is limited by the collector load resistor (approximately 1.5μs for 10kΩ). Improved switching speed can be obtained by increasing the complexity of the translator stage.

A translator which overcomes the problems of the simple PNP stage is the Harris IH6201.* This translator driving an IH401A varafet produces the following typical features:

- t_{on} time of approx. 200ns } break before
- t_{off} time of approx. 80ns } make switch
- TTL compatible strobing levels of +2.4V / 0.4V
- $I_{D(on)} + I_{S(on)}$ typically 20pA up to ±10V analog signals
- $I_{D(off)}$ or $I_{S(off)}$ typically 20pA
- Quiescent current drain of approx. 100nA in either "on" or "off" case

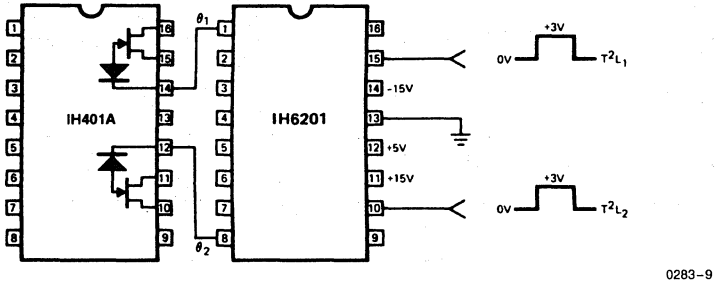
*The IH6201 is a dual translator (two independent translators per package) constructed from monolithic CMOS technology. The schematic of one-half IH6201, driving one-fourth of an IH401A, is shown in Figure 6.

NOTE: All typical values have been characterized but are not tested.



NOTE: Each translator output has a θ and $\overline{\theta}$ output. $\overline{\theta}$ is just the inverse of θ i.e., ($\overline{\theta}$ output is 180° out of phase with respect to θ output).

Figure 6: IH6201 Driving An IH401A



NOTE: Either switch is turned on when strobe input goes high.

Figure 7: Dual SPST Analog Switch

NOTE: All typical values have been characterized but are not tested.

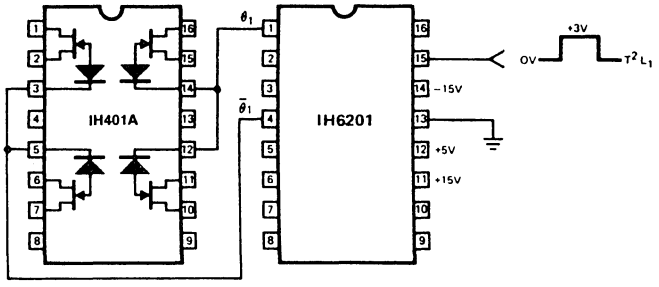


Figure 8: DPDT Analog Switch

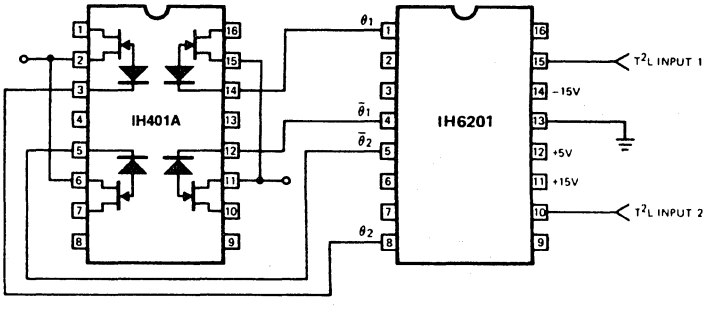


Figure 9: Dual SPDT Analog Switch

A very useful feature of this system is that one-half of an IH6201 and one-half of an IH401A can combine to make a SPDT switch, or an IH6201 plus an IH401A can make a dual SPDT analog switch. (See Figure 9)

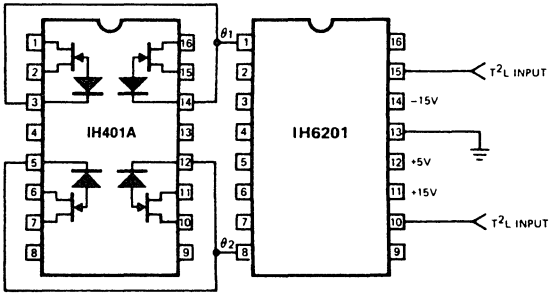


Figure 10: Dual DPST Analog Switch

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

IH5009-5012, 5014, 5016-5020, 5022, 5024
Virtual Ground Analog Switch

GENERAL DESCRIPTION

The IH5009 series of analog switches were designed to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost is a primary design objective, performance and versatility have not been sacrificed.

Each package contains up to four channels of analog gating and is designed to eliminate the need for an external driver. The odd numbered devices are designed to be driven directly from TTL open collector logic (15 volts) while the even numbered devices are driven directly from low level TTL logic (5 volts). Each channel simulates a SPDT switch. SPST switch action is obtained by leaving the diode cathode unconnected; for SPDT action, the cathode should be grounded (0V). The parts are intended for high performance multiplexing and commutating usage. A logic "0" turns the channel ON and a logic "1" turns the channel OFF.

FEATURES

- **Switches Analog Signals Up to 20 Volts Peak-to-Peak**
- **Each Channel Complete – Interfaces With Most Integrated Logic**
- **Switching Speeds Less Than 0.5μs**
- **$I_{D(OFF)}$ Less Than 500pA Typical at 70°C**
- **Effective $r_{ds(ON)}$ – 5Ω to 50Ω**
- **Commercial and Military Temperature Range Operation**

ORDERING INFORMATION

Basic Part Number	Channels	Logic Level	Packages
IH5009	4	+15	DD,PD
IH5010	4	+5	DD,PD
IH5011	4	+15	DE,PE
IH5012	4	+5	DE,PE
IH5014	3	+5	DD,PD
IH5016	3	+5	DE,PE
IH5017	2	+15	DD,PA
IH5018	2	+5	DD,PA
IH5019	2	+15	DE,PA
IH5020	2	+5	DE,PA
IH5022	1	+5	DD,PA
IH5024	1	+5	DE,PA

NOTE: Mil-Temperature range (−55°C to +125°C) available in ceramic packages only.

IH50XX M DE

- DE → Package
  - PA – 8-pin PLASTIC DIP
  - PD – 14-PIN PLASTIC DIP
  - PE – 16-PIN PLASTIC DIP
  - DD – 14-PIN CERAMIC DIP
  - DE – 16-PIN CERAMIC DIP
- M → TEMPERATURE RANGE
  - M = MILITARY (−55°C to +125°C)
  - C = COMMERCIAL (0°C to +70°C)
- IH50XX → BASIC PART NUMBER

NOTE: All typical values have been characterized but are not tested.

IH5009-5012, 5014, 5016-5020, 5022, 5024

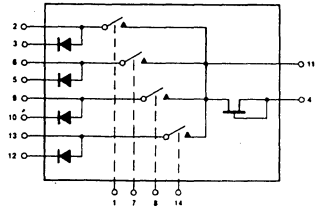
ABSOLUTE MAXIMUM RATINGS

Positive Analog Signal Voltage 30V
Negative Analog Signal Voltage ..... −15V
Diode Current 10mA
Power Dissipation (Note) 500mW
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Operating Temperature
5009C Series ..... 0°C to +70°C
5009M Series ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperature, derate at rate of 5m/W°C.

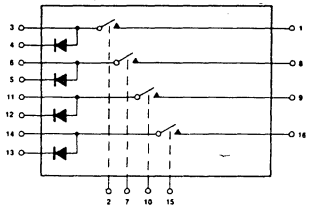
NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

IH5009 ($r_{DS(ON)} \leq 100\Omega$) IH5010 ($r_{DS(ON)} \leq 150\Omega$) 14 PIN DIP (OUTLINE DWGS DD, PD, JD)



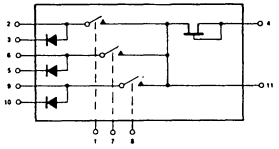
0284-1

IH5011 ($r_{DS(ON)} \leq 100\Omega$) IH5012 ($r_{DS(ON)} \leq 150\Omega$) 16 PIN DIP (OUTLINE DWGS DE, PE, JE)



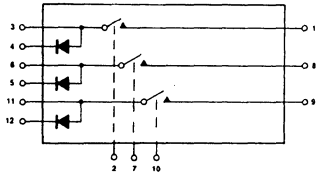
0284-2

IH5014 ($r_{DS(ON)} \leq 150\Omega$) 14 PIN DIP (OUTLINE DWGS DD, PE, JE)



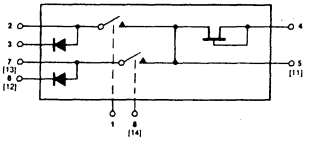
0284-3

IH5016 ($r_{DS(ON)} \leq 150\Omega$) 16 PIN DIP (OUTLINE DWGS DE, PE, JE)



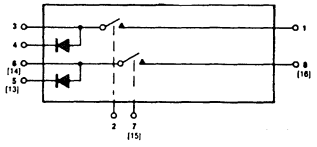
0284-4

IH5017 ($r_{DS(ON)} \leq 100\Omega$) IH5018 ($r_{DS(ON)} \leq 150\Omega$) 8 PIN DIP (OUTLINE DWGS DD, PA, JD)



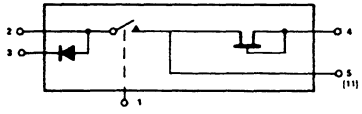
0284-5

IH5019 ($r_{DS(ON)} \leq 100\Omega$) IH5020 ($r_{DS(ON)} \leq 150\Omega$) 8 PIN DIP (OUTLINE DWGS DE, PA, JE)



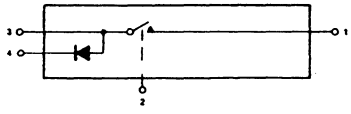
0284-6

IH5022 ($r_{DS(ON)} \leq 150\Omega$) 8 PIN DIP (OUTLINE DWGS DD, PA, JD)



0284-7

IH5024 ($r_{DS(ON)} \leq 150\Omega$) 8 PIN DIP (OUTLINE DWGS DE, PA, JE)



0284-8

(Note: Numbers in brackets refer to CERDIP packages.)

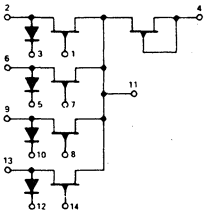
Figure 1: Pin Connections

NOTE: All typical values have been characterized but are not tested.

IH5009-5012, 5014, 5016-5020, 5022, 5024

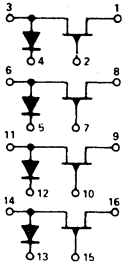
FOUR CHANNEL

IH5009 ($r_{DS(ON)} \leq 100\Omega$)
IH5010 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP



0284-9

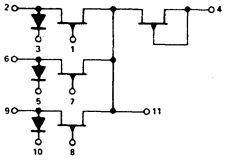
IH5011 ($r_{DS(ON)} \leq 100\Omega$)
IH5012 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP



0284-10

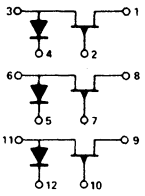
THREE CHANNEL

IH5014 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP



0284-11

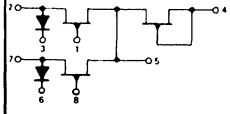
IH5016 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP



0284-12

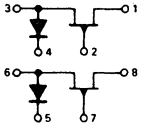
TWO CHANNEL

IH5017 ($r_{DS(ON)} \leq 100\Omega$)
IH5018 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



0284-13

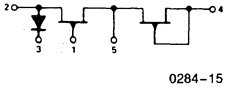
IH5019 ($r_{DS(ON)} \leq 100\Omega$)
IH5020 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



0284-14

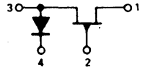
SINGLE CHANNEL

IH5022 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



0284-15

IH5024 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP



0284-16

Figure 2: Device Schematics and Pin Connections

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (per channel)

Symbol (Note 1)	Characteristic	Type (Note 4)	TEST Conditions (Note 2)	Specification Limit				Units
				−55°C (M) 0°C (C)	25°C		+125°C (M) +70°C (C)	
				Min/Max	Typ	Min/Max	Min/Max	
$I_{IN(ON)}$	Input Current-ON	ALL	$V_{IN}=0V$, $I_D=2mA$		0.01	±0.5	100	μA
$I_{IN(OFF)}$	Input Current-OFF	5V Logic Ckts	$V_{IN}=+4.5V$, $V_A=±10V$		0.04	±0.5	20	nA
$I_{IN(OFF)}$	Input Current-OFF	15V Logic Ckts	$V_{IN}=+11V$, $V_A=±10V$		0.04	±0.5	20	nA
$V_{IN(ON)}$	Channel Control Voltage-ON	5V Logic Ckts	See Figure 7, Note 3	0.5		0.5	0.5	V
$V_{IN(ON)}$	Channel Control Voltage-ON	15V Logic Ckts	See Figure 8, Note 3	1.5		1.5	1.5	V
$V_{IN(OFF)}$	Channel Control Voltage-OFF	5V Logic Ckts	See Figure 6, Note 3			4.5	4.5	V
$V_{IN(OFF)}$	Channel Control Voltage-OFF	15V Logic Ckts	See Figure 8, Note 3			11.0	11.0	V
$I_{D(OFF)}$	Leakage Current-OFF	5V Logic Ckts	$V_{IN}=+4.5V$, $V_A=±10V$		0.02	±0.5	20	nA
$I_{D(OFF)}$	Leakage Current-OFF	15V Logic Ckts	$V_{IN}=+11V$, $V_A=±10V$		0.02	±0.5	20	nA
$I_{D(ON)}$	Leakage Current-ON	5V Logic Ckts	$V_{IN}=0V$, $I_S=1mA$		0.30	±1.0	1000 (M) 200 (C)	nA
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	$V_{IN}=0V$, $I_S=1mA$		0.10	±0.5	500 (M) 100 (C)	nA
$I_{D(ON)}$	Leakage Current-ON	5V Logic Ckts	$V_{IN}=0V$, $I_S=2mA$			1.0	10	μA
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	$V_{IN}=0V$, $I_S=2mA$			2.0	100	μA
$r_{DS(ON)}$	Drain-Source ON-Resistance	5V Logic Ckts	$I_D=2mA$, $V_{IN}=0.5V$	150	90	150	385 (M) 240 (C)	Ω
$r_{DS(ON)}$	Drain-Source ON-Resistance	15V Logic Ckts	$I_D=2mA$, $V_{IN}=1.5V$	100	80	100	250 (M) 160 (C)	Ω
$t_{(on)}$	Turn-ON Time	All	See Figures 5 & 6		150	500		ns
$t_{(off)}$	Turn-OFF Time	All	See Figures 5 & 6		300	500		ns
CT	Cross Talk	All	f=100Hz		120			dB

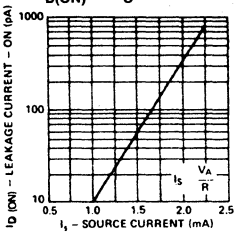
NOTES: 1. (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.
2. Refer to Figure 2 for definition of terms.
3. $V_{IN(ON)}$ and $V_{IN(OFF)}$ are test conditions guaranteed by the tests of $r_{DS(ON)}$ and $I_{D(OFF)}$ respectively.
4. "5V Logic CKTS" applies to even-numbered devices. "15V Logic CKTS" applies to odd-numbered devices.

NOTE: All typical values have been characterized but are not tested.

IH5009-5012, 5014, 5016-5020, 5022, 5024

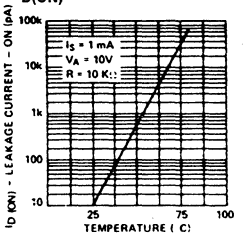
TYPICAL PERFORMANCE CHARACTERISTICS (per channel)

$I_{D(ON)}$ vs. I_S AT 25°C



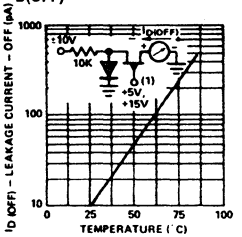
0284-17

$I_{D(ON)}$ vs. TEMPERATURE



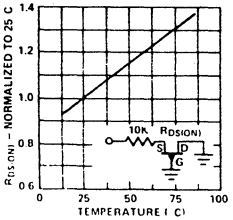
0284-18

$I_{D(OFF)}$ vs. TEMPERATURE



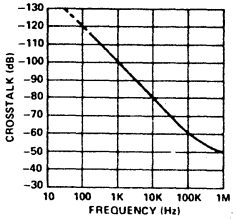
0284-19

$R_{DS(ON)}$ vs. TEMPERATURE (NORMALIZED TO 25°C VALUE)



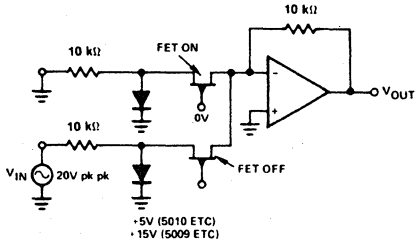
0284-20

CROSSTALK AS A FUNCTION OF FREQUENCY



0284-21

CROSSTALK MEASUREMENT CIRCUIT



0284-22

DETAILED DESCRIPTION

The signals seen at the drain of a junction FET type analog switch can be arbitrarily divided into two categories; those which are less than ±200mV, and those which are greater than ±200mV. The former category includes all those circuits where switching is performed at the virtual ground point of an op-amp, and it is primarily towards these applications that the IH5009 family of circuits is directed.

By limiting the analog signal at the switching point to ±200mV, no external driver is required and the need for additional power supplies is eliminated.

Devices are available with both common drains and with uncommitted drains.

Those devices which feature common drains have another FET in addition to the channel switches. This FET, which has gate and source connected such that $V_{GS}=0$, is intended to compensate for the on-resistance of the switch. When placed in series with the feedback resistor (Figure 3) the gain is given by:

$$\text{GAIN}=\frac{10\text{k}\Omega + r_{DS(ON)}\text{(compensator)}}{10\text{k}\Omega + r_{DS(\text{switch})}}.$$

NOTE: All typical values have been characterized but are not tested.

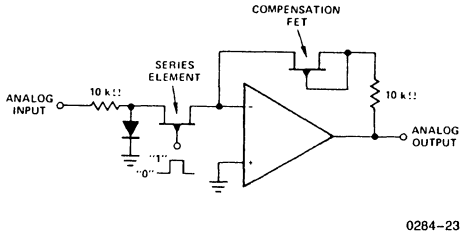


Figure 3: Use of Compensation FET

Clearly, the gain error caused by the switch is dependent on the match between the FETs rather than the absolute value of the FET on-resistance. For the standard product, all the FETs in a given package are guaranteed to match within 50Ω. Selections down to 5Ω are available however. Contact factory for details. Since the absolute value of $r_{DS(ON)}$ is guaranteed only to be less than 100Ω or 150Ω, a substantial improvement in gain accuracy can be obtained by using the compensating FET.

DEFINITION OF TERMS

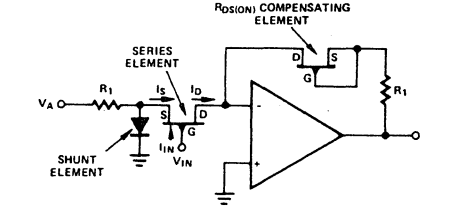


Figure 4.

NOISE IMMUNITY

The advantage of SPDT switching is high noise immunity when the series elements is OFF. For example, if a ±10V analog input is being switched by TTL open collector logic, the series switch is OFF when the logic level is at +15 volts. At this time, the diode conducts and holds the source at approximately +0.7 volts with an AC impedance to ground of 25 ohms. Thus random noise superimposed on the +10 volt analog input will not falsely trigger the FET since the noise voltage will be shunted to ground.

When switching a negative voltage, the input further increases the OFF voltage beyond pinch-off, so there is no danger of the FET turning on.

SWITCHING CHARACTERISTICS

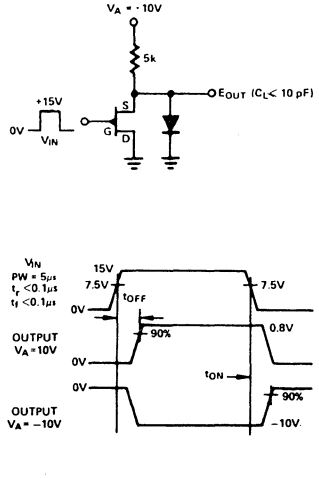


Figure 5: High Level Logic

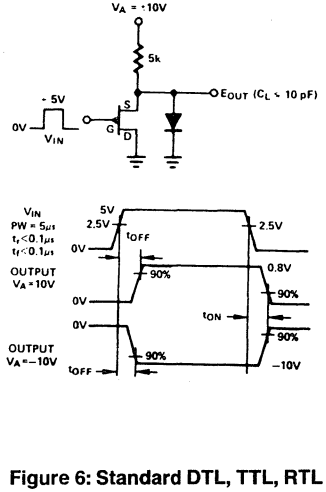


Figure 6: Standard DTL, TTL, RTL

NOTE: All typical values have been characterized but are not tested.

IH5009-5012, 5014, 5016-5020, 5022, 5024

LOGIC INTERFACE CIRCUITS

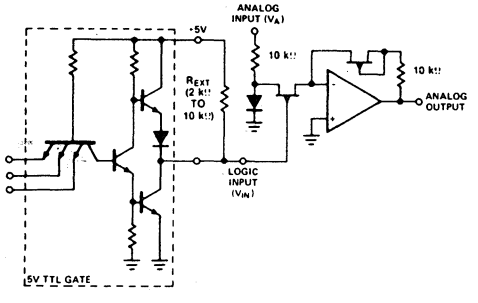


Figure 7: Interfacing with +5V Logic

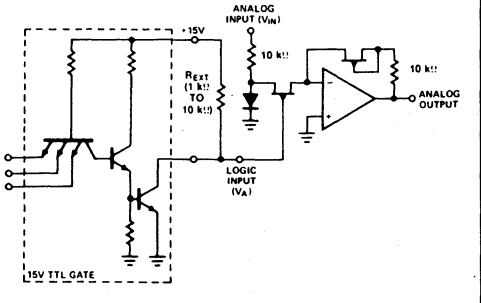


Figure 8: Interfacing with +15V Open Collector Logic

APPLICATIONS (Note)

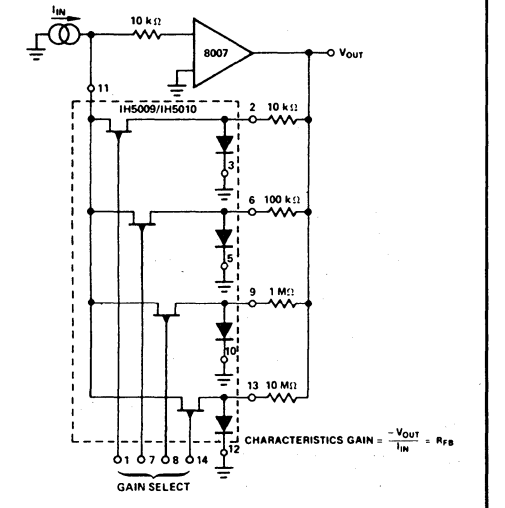


Figure 9

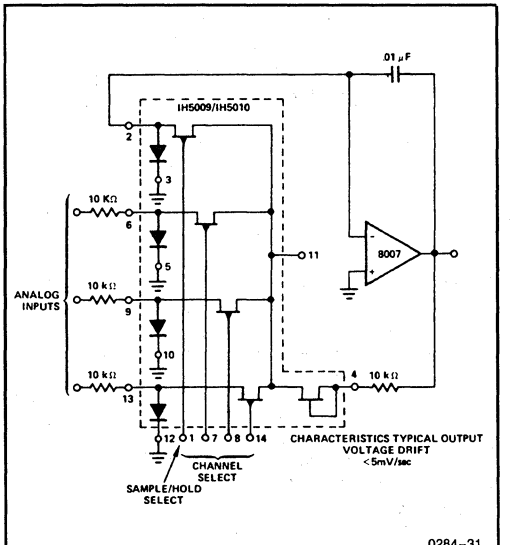


Figure 10

NOTE: Additional applications information is given in Application Bulletins A003 "Understanding and Applying the Analog Switch" and A004 "The 5009 Series of Low Cost Analog Switches".

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

IH5043
High-Level CMOS Analog Switch

GENERAL DESCRIPTION

The IH5043 analog switch uses an improved, high voltage CMOS monolithic technology. These devices provide ease-of-use and performance advantages not previously available from solid state switches.

Key performance advantage is TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 1mA. Also, the IH5043 guarantees Break-Before-Make switching, accomplished by extending the t_{on} time (300ns TYP), so that it exceeds t_{off} time (200ns TYP). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. The need for external logic required to avoid channel to channel shorting during switching is eliminated.

The IH5043 improves upon and is pin-for-pin and electrical replacement for other solid state switches.

FEATURES

- See HI504X and IH514X for Other Functions
- Dual SPDT
- Switches Greater Than 20Vpp Signals With ±15V Supplies
- Quiescent Current Less Than 1μA
- Break-Before-Make Switching t_{off} 200ns, t_{on} 300ns Typical
- TTL, DTL, CMOS, PMOS Compatible

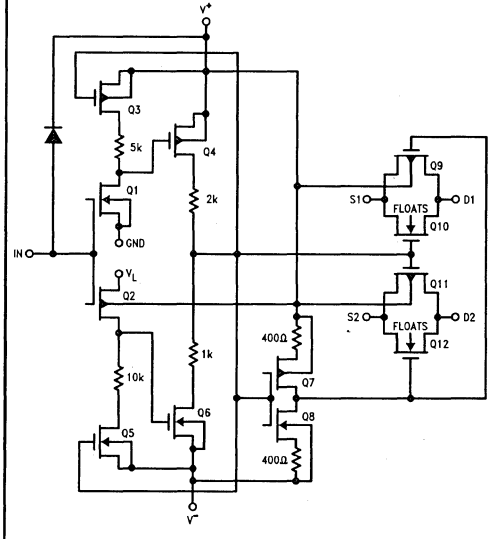


Figure 1: Functional Driver, Typical Driver, Gate - IH5043

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5043MJE	-55°C to +125°C	16 Pin Ceramic DIP
IH5043CJE	0°C to +70°C	16 Pin Ceramic DIP
IH5043CPE	0°C to +70°C	16 Pin Plastic DIP
IH5043CY	0°C to +70°C	16 Pin SOIC

7

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V^+-V^- ..... <36V
V^+-V_D ..... <30V
V_D-V^- ..... <30V
V_D-V_S ..... < ±22V
V_L-V^- ..... <33V
V_L-V_{IN} ..... <30V
V_L-GND ..... <20V
V_{IN}-GND ..... <20V

Current (Any Terminal) ..... <30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature
M ..... −55°C to +125°C
C ..... 0°C to +70°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6mW/°C Above 70°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS (@ 25°C, V^+ = +15V, V^- = −15V, V_L = +5V)

Per Channel		Test Conditions	Min/Max Limits						Units
			Military			Commercial			
Symbol	Characteristic		−55°C	+25°C	+125°C	0	+25°C	+70°C	
$I_{IN(ON)}$	Input Logic Current	V_{IN} = 2.4V	±1	±1	10	±1	±1	10	µA
$I_{IN(OFF)}$	Input Logic Current	V_{IN} = 0.8V	±1	±1	10	±1	±1	10	µA
$r_{DS(on)}$	Drain-Source On Resistance	I_S = 10mA V_{ANALOG} = −10V to +10V	75	75	150	80	80	130	Ω
$\Delta r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match			25 (typ)			30 (typ)		Ω
V_{ANALOG}	Min. Analog Signal Handling Capability			±11 (typ)			±10 (typ)		V
$I_{D(OFF)}$/ $I_{S(OFF)}$	Switch OFF Leakage Current	V_{ANALOG} = −10V to +10V		±1	100		±5	100	nA
$I_{D(ON)}$ + $I_{S(ON)}$	Switch On Leakage Current	V_D = V_S = −10V to +10V		±2	200		±10	100	nA
t_{on}	Switch "ON" Time	R_L = 1kΩ, V_{ANALOG} = −10V to +10V See Fig. 3		1000			1000		ns
t_{off}	Switch "OEF" Time	R_L = 1kΩ, V_{ANALOG} = −10V to +10V See Fig. 3		500			500		ns
$Q_{(INJ.)}$	Charge Injection	See Fig. 4		15 (typ)			20 (typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	f = 1MHz, R_L = 100Ω, C_L ≤ 5pF See Fig. 5		54 (typ)			50 (typ)		dB
I^+_Q	V^+ Power Supply Quiescent Current		±1	±1	10	10	10	100	µA
I^-_Q	V^- Power Supply Quiescent Current	V^+ = +15V, V^- = −15V, V_L = +5V	±1	±1	10	10	10	100	µA
I^-_{LQ}	+5V Supply Quiescent Current		±1	±1	10	10	10	100	µA
I_{GND}	Gnd Supply Quiescent Current		±1	1	10	10	10	100	µA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off; Any Other Channel Switches as per Fig. 6		54 (typ)			50 (typ)		dB

Note: Typical values are for design aid only, not guaranteed and not subject to production testing.

NOTE: All typical values have been characterized but are not tested.

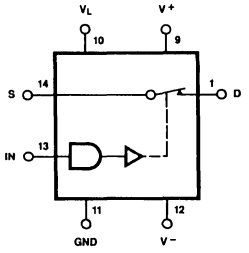
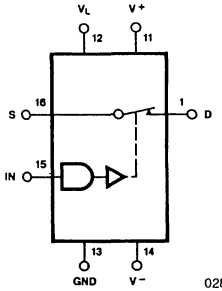
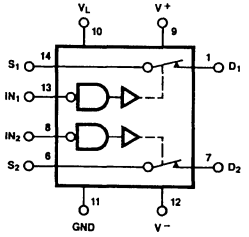
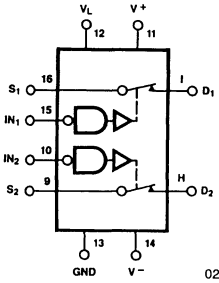
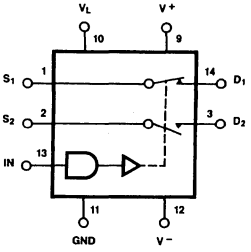
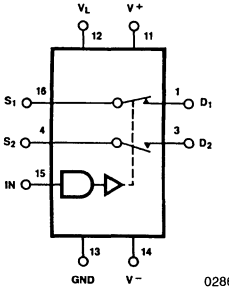
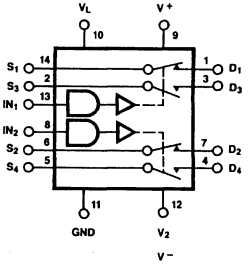
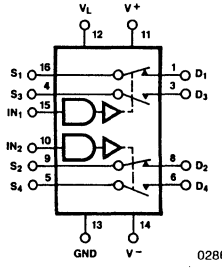
SWITCH STATES ARE FOR LOGIC "1" INPUT	(OUTLINE DWG FD-2)	(OUTLINE DWGS DE, JE, PE, Y)
SPST IH5040 ($r_{DS(on)} < 75\Omega$)	 0286-2	 0286-3
DUAL SPST IH5041 ($r_{DS(on)} < 75\Omega$)	 0286-4	 0286-5
SPDT IH5042 ($r_{DS(on)} < 75\Omega$)	 0286-7	 0286-8
DUAL SPDT IH5043 ($r_{DS(on)} < 75\Omega$)	 0286-10	 0286-11

Figure 2: Switching State Diagrams

NOTE: All typical values have been characterized but are not tested.

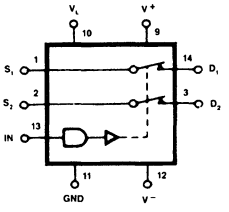
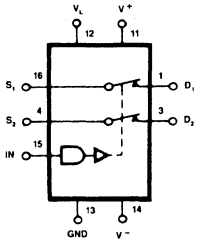
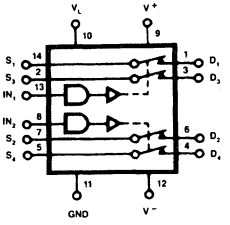
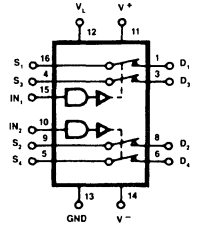
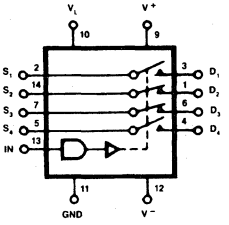
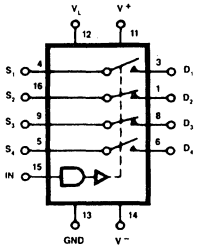
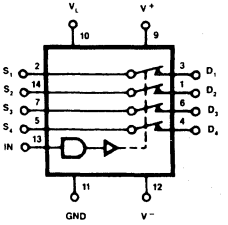
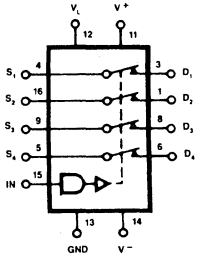
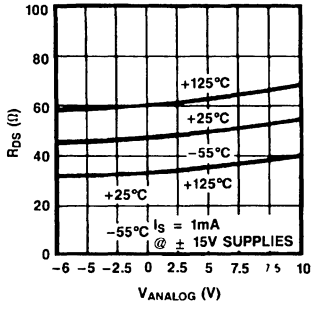
SWITCH STATES ARE FOR LOGIC "1" INPUT	(OUTLINE DWG FD-2)	(OUTLINE DWGS DE, JE, PE)
DPST IH5044 ($r_{DS(on)} < 75\Omega$)	 0286-12	 0286-13
DUAL DPST IH5045 ($r_{DS(on)} < 75\Omega$)	 0286-15	(DG185 EQUIVALENT)  0286-16
DPDT IH5046 ($r_{DS(ON)} < 75\Omega$)	 0286-17	 0286-18
4PST IH5047 ($r_{DS\ (ON)} < 75\Omega$)	 0286-19	 0286-20

Figure 2: Switching State Diagrams (Cont.)

NOTE: All typical values have been characterized but are not tested.

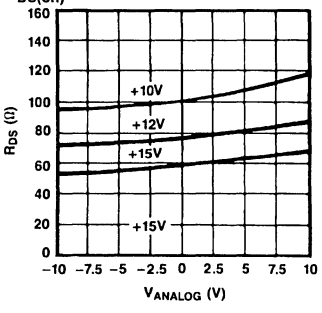
TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel)

$R_{DS(on)}$ vs V_{ANALOG} SIGNAL



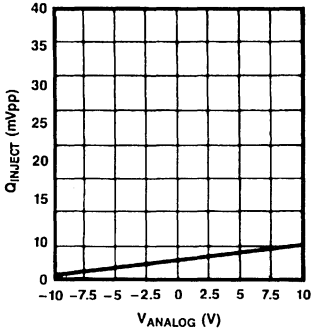
0286-21

$R_{DS(on)}$ vs POWER SUPPLY VOLTAGE

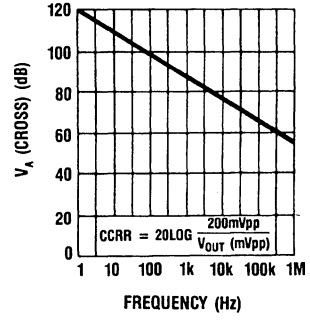


0286-22

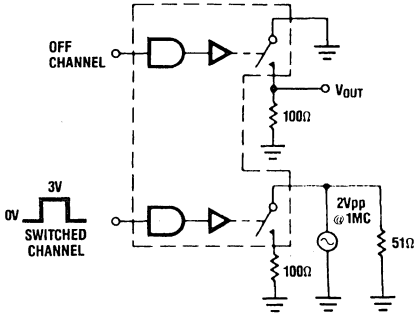
CHARGE INJECTION vs V_{ANALOG} (SEE FIG. B) C_L = 10,000pF



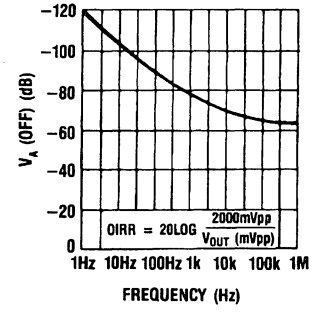
0286-23



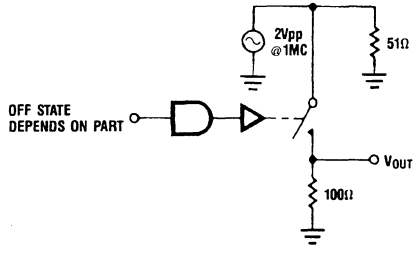
0286-24



0286-25



0286-26

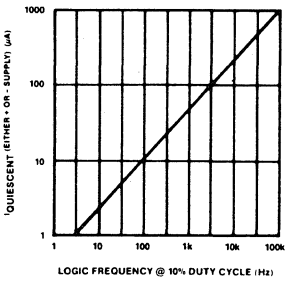


0286-27

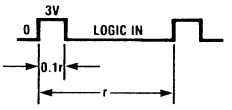
NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (CONT.)

POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE

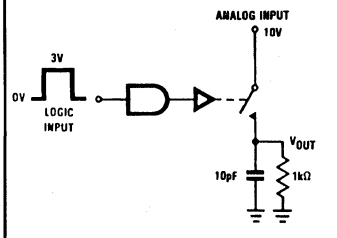


0286-28



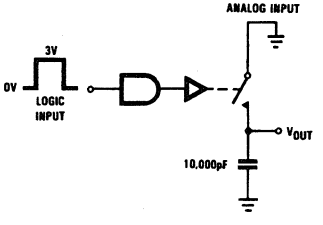
0286-29

TEST CIRCUITS



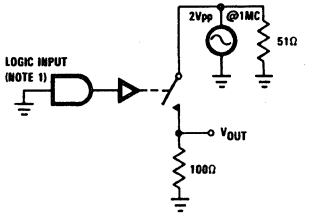
0286-30

Figure 3



0286-31

Figure 4

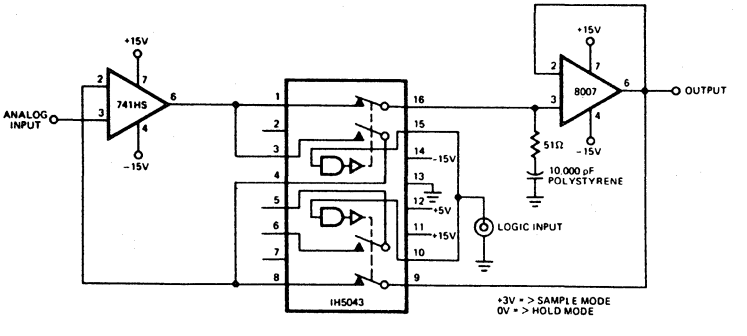


0286-32

Figure 5

NOTE 1: Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

APPLICATIONS



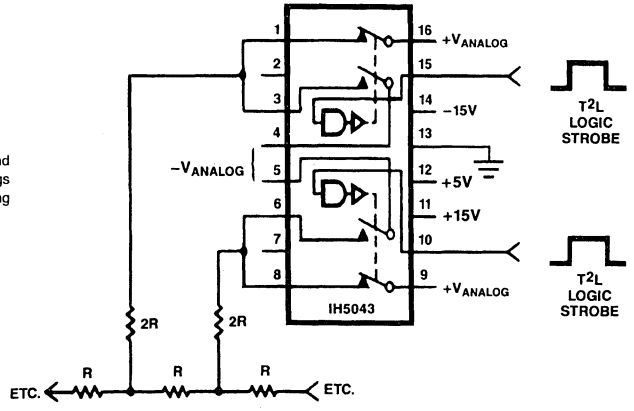
0286-33

Figure 6: Improved Sample & Hold Using IH5043

NOTE: All typical values have been characterized but are not tested.

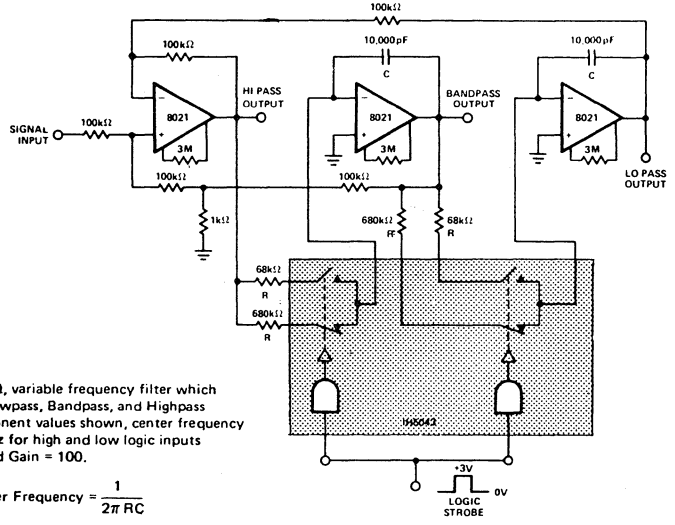
APPLICATIONS (Continued)

EXAMPLE: If $-V_{ANALOG} = -10VDC$ and $+V_{ANALOG} = +10VDC$ then Ladder Legs are switched between $\pm 10VDC$, depending upon state of Logic Strobe.



0286-34

Figure 7: Using the CMOS Switch to Drive an R/2R Ladder Network (2 Legs)



Constant gain, constant Q, variable frequency filter which provides simultaneous Lowpass, Bandpass, and Highpass outputs. With the component values shown, center frequency will be 235Hz and 23.5Hz for high and low logic inputs respectively, Q = 100, and Gain = 100.

$$f_n = \text{Center Frequency} = \frac{1}{2\pi RC}$$

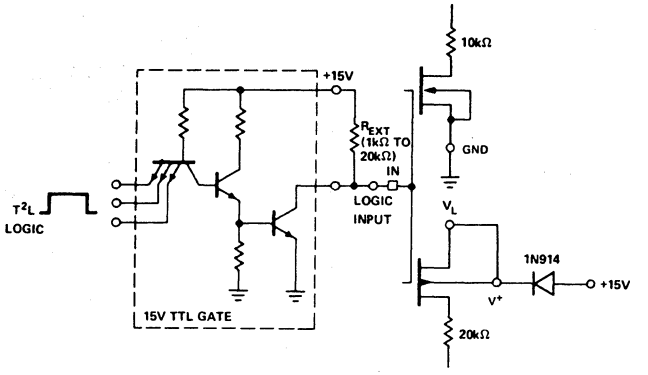
0286-35

Figure 8: Digitally Tuned Low Power Active Filter

7

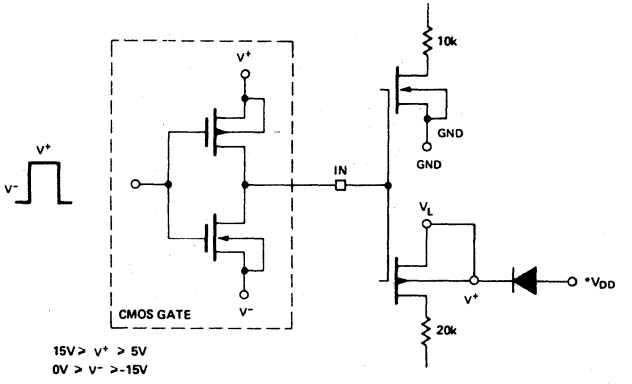
NOTE: All typical values have been characterized but are not tested.

APPLICATIONS (Continued)



0286-36

Figure 9: Interfacing with TTL Open Collector Logic (Typ. Example for + 15V Case Shown)



0286-37

Figure 10: Interfacing with CMOS Logic

NOTE: All typical values have been characterized but are not tested.

IH5040-IH5047

APPLICATIONS (Continued)

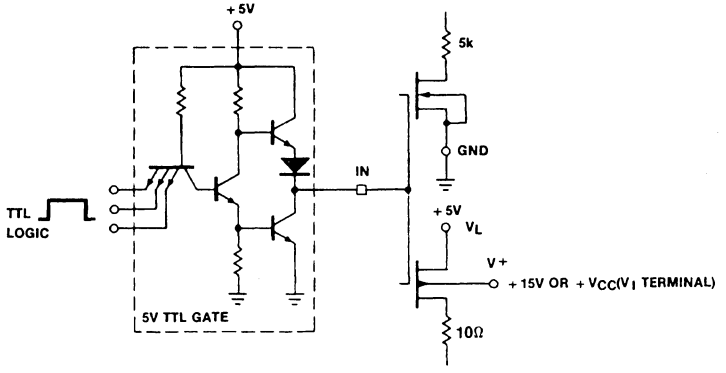


Figure 11: TTL Logic Interface

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

IH5052/IH5053
QUAD CMOS Analog Switch

GENERAL DESCRIPTION

The IH5052/3 analog switches use an improved, high voltage CMOS technology, which provides performance advantages not previously available from solid state switches. Key performance advantages are TTL compatibility and ultra low-power operation — the quiescent current requirement is less than 10μA.

The IH5052/3 also guarantees Break-Before-Make switching. This is accomplished by extending the t_{ON} time (400ns TYP.) such that it exceeds t_{OFF} time (200ns TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON, and eliminates the need for external logic required to avoid channel to channel shorting during switching. With a logical "0" (0.8V or less) at its control inputs, the IH5052 switches are closed, while the IH5053 switches are closed with a logical "1" (2.4V or more) at its control inputs.

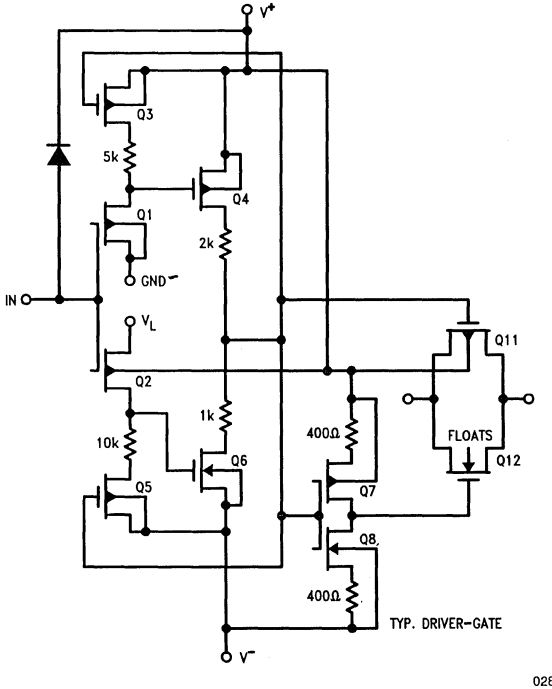
FEATURES

- **Switches Greater Than 20Vpp Signals With ±15V Supplies**
- **Quiescent Current Less Than 10μA**
- **Break-Before-Make Switching t_{off} 100ns, t_{on} 250ns Typical**
- **TTL, CMOS Compatible**
- **IH5052 4 Normally Closed Switches**
- **IH5053 4 Normally Open Switches**
- **Low $R_{DS(ON)}$ 50Ω Typical**

ORDERING INFORMATION

IH505X C DE

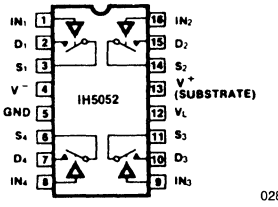
- DE = 16-Pin Ceramic DIP (Package)
- C = Commercial, M = Military (Temperature Range)
- Basic Part Number



0288-1

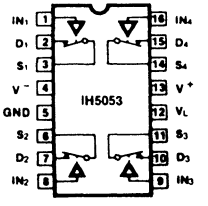
Figure 1: Functional Diagram

Outline Dwgs DE
Dual-In-Line Package



0288-19

Switch States are for Logic "1" Input



0288-2

Figure 2: Pin Configurations

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$ ..... <36V
$V^+ - V_D$ ..... <30V
$V_D - V^-$ ..... <30V
$V_D - V_S$ ..... < ±22V
$V_L - V^-$ ..... <33V
$V_L - V_{IN}$ ..... <30V
V_L - GND ..... <20V
V_{IN} - GND ..... <20V
Current (Any Terminal) ..... <30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6mW/°C Above 70°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

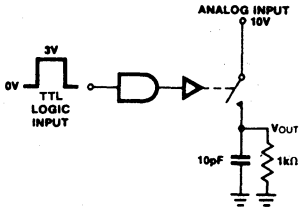
ELECTRICAL CHARACTERISTICS (T_A = 25°C, V^+ = +15V, V^- = −15V, V_L = +5V)

Per Channel		Test Conditions	Min/Max Limits						Units
			Military			Commercial			
Symbol	Characteristic		−55°C	+25°C	+125°C	0	+25°C	+70°C	
$I_{IN(ON)}$	Input Logic Current	V_{IN} = 2.4V (IH5053) = 0.8V (IH5052)	10	±1	10		±10		µA
$I_{IN(OFF)}$	Input Logic Current	V_{IN} = 0.8V (IH5053) = 2.4V (IH5052)	10	±1	10		±10		µA
$r_{DS(ON)}$	Drain-Source On Resistance	I_S = 10mA, V_{analog} = −10V to +10V	75	75	100	80	80	100	Ω
$\Delta r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match			25 (typ)			30 (typ)		Ω
V_{ANALOG}	Min. Analog Signal Handling Capability			±11 (typ)			±10 (typ)		V
$I_{D(OFF)}$ / $I_{S(OFF)}$	Switch OFF Leakage Current	V_{ANALOG} = −10V to +10V		±1	100		±5	100	nA
$I_{D(ON)}$ + $I_{S(ON)}$	Switch On Leakage Current	$V_D = V_S$ = −10V to +10V		±2	200		±10	100	nA
t_{ON}	Switch "ON" Time	R_L = 1kΩ, V_{analog} = −10V to +10V See Fig. 3		500			1000		ns
t_{OFF}	Switch "OFF" Time	R_L = 1kΩ, V_{analog} = −10V to +10V See Fig. 3		250			500		ns
$Q_{(INJ.)}$	Charge Injection	See Fig. 4		15 (typ)			20 (typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	f = 1MHz, R_L = 100Ω, $C_L \leq$ 5pF See Fig. 5		54 (typ)			50 (typ)		dB
I^+	+ Power Supply Quiescent Current	V^+ = +15V, V^- = −15V, V_L = +5V with GND	10	10	100	10	10	100	µA
I^-	− Power Supply Quiescent Current		10	10	100	10	10	100	µA
I_{VL}	+5V Supply Quiescent Current		10	10	100	10	10	100	µA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off		54 (typ)			50 (typ)		dB

NOTE 1: Typical values are for design aid only, not guaranteed and not subject to production testing.

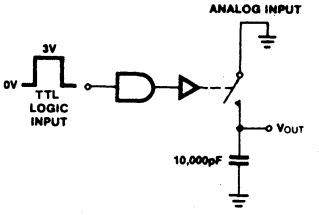
NOTE: All typical values have been characterized but are not tested.

TEST CIRCUITS



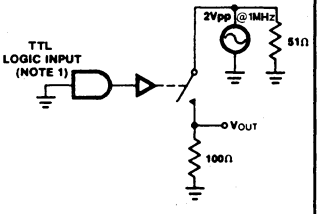
0288-3

Figure 3



0288-4

Figure 4



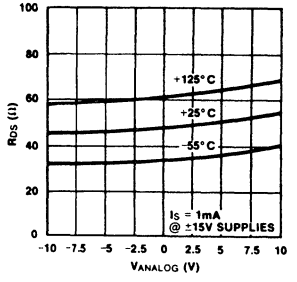
0288-5

Figure 5

NOTE 1: The 5053 is turned on by high "1" logic inputs and the 5052 is turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

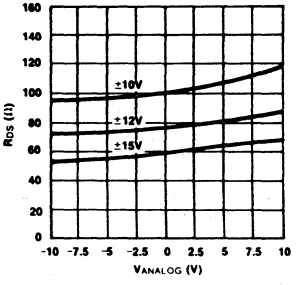
TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel)

$r_{DS(ON)}$ vs V_{ANALOG} SIGNAL



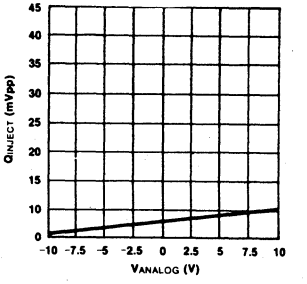
0288-6

$r_{DS(ON)}$ vs POWER SUPPLY VOLTAGE



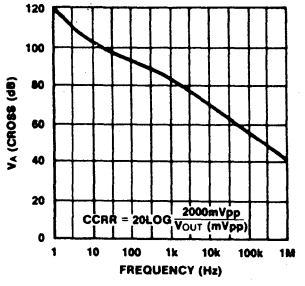
0288-7

CHARGE INJECTION vs V_{ANALOG} (SEE Figure B) C_L = 10,000pF

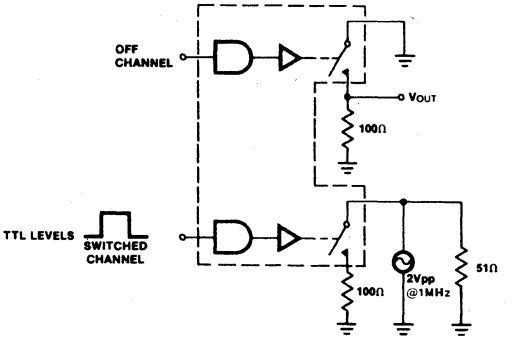


0288-8

CROSS COUPLING REJECTION vs FREQUENCY



0288-9



0288-10

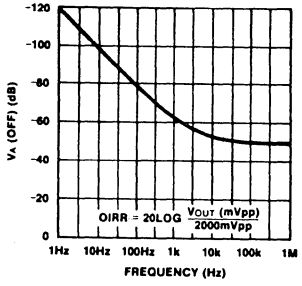
Cross Coupling Rejection Test Circuit

NOTE: All typical values have been characterized but are not tested.

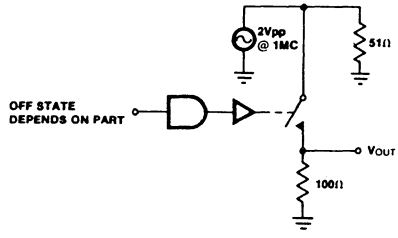
IH5052/IH5053

TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel) (Continued)

OFF ISOLATION vs FREQUENCY



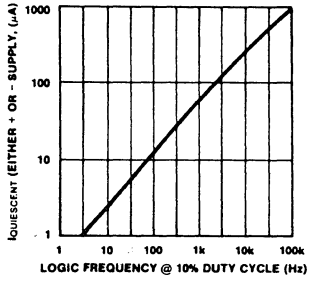
0288-11



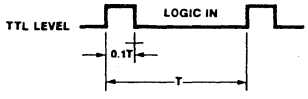
0288-12

Off Isolation Test Circuit

POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE

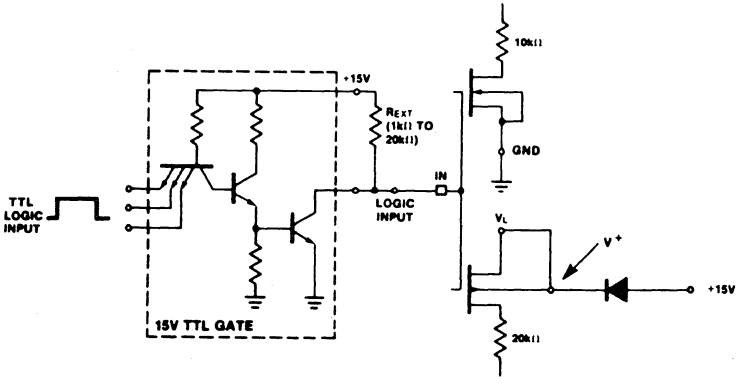


0288-13



0288-14

Logic Input Waveform



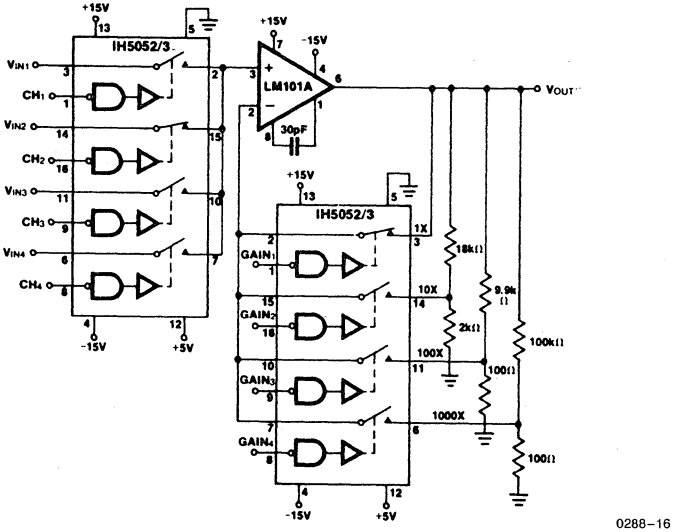
0288-15

Figure 6: + 15V Open Collector TTL Interface to IH5052/5053

NOTE: All typical values have been characterized but are not tested.

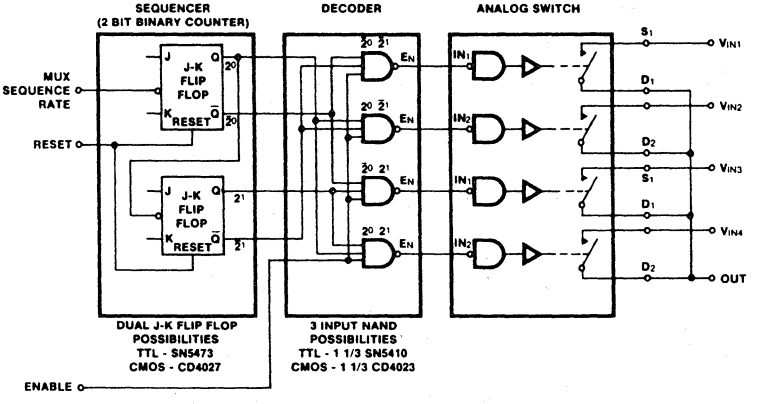
APPLICATIONS

PROGRAMMABLE GAIN NON-INVERTING AMPLIFIER WITH SELECTABLE INPUTS



0288-16

Figure 7: Active Low Pass Filter with Digitally Selected Break Frequency



0288-17

TRUTH TABLE (IH5052)

Enable	Mux Sequence Rate	Sequencer Output		Switch States (—Denotes Off)			
		2^0	2^1	SW1	SW2	SW3	SW4
0	0	0	0	—	—	—	—
1	0	0	0	ON	—	—	—
1	1 pulse	1	0	—	ON	—	—
1	2 pulses	0	1	—	—	—	—
1	3 pulses	1	1	—	—	—	ON
1	4 pulses	0	0	ON	—	—	—

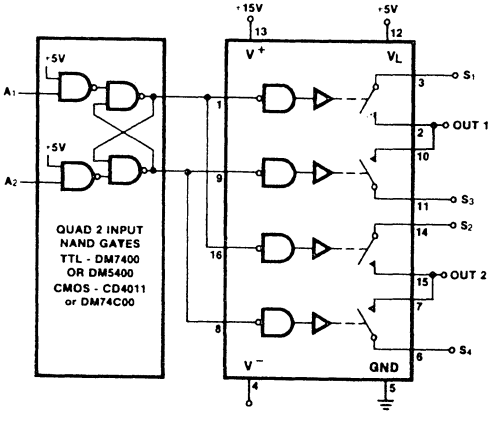
Figure 8: 4-Channel Sequencing MUX

NOTE: All typical values have been characterized but are not tested.

IH5052/IH5053

A LATCHING DPDT SWITCH

The latch feature insures positive switching action in response to non-repetitive or erratic commands. The A_1 and A_2 inputs are normally low. A HIGH input to A_2 turns S_1 and S_2 ON, a HIGH to A_1 turns S_3 and S_4 ON. Desirable for use with limit detectors, peak detectors, or mechanical contact closures.



0288-18

Figure 9: A Latching DPDT

TRUTH TABLE (IH5052)

Command		State of Switches After Command	
A_2	A_1	S_3 & S_4	S_1 & S_2
0	0	same	same
0	1	on	off
1	0	off	on
1	1	INDETERMINATE	

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

IH5140-IH5145
High-Level CMOS Analog Switch

GENERAL DESCRIPTION

The IH5140 Family of CMOS switches utilizes Harris' latch-free junction isolated processing to build the fastest switches currently available. These switches can be toggled at a rate of greater than 1MHz with super fast t_{on} times (80ns typical) and faster t_{off} times (50ns typical), guaranteeing break before make switching. This family of switches combines the speed of the hybrid FET DG180 family with the reliability and low power consumption of a monolithic CMOS construction.

OFF leakages are guaranteed to be less than 200pA at 25°C. Very low quiescent power is dissipated in either the ON or the OFF state of the switch. Maximum power supply current is 1μA from any supply and typical quiescent currents are in the 10nA range which makes these devices ideal for portable equipment and military applications.

The IH5140 Family is completely compatible with TTL (5V) logic, TTL open collector logic and CMOS logic. It is pin compatible with Harris' IH5040 family and part of the DG180/190 family as shown in the switching state diagrams.

ORDERING INFORMATION

Order Part Number	Function	Package	Temperature Range
IH5140 MJE	SPST	16 Pin CERDIP	−55°C to 125°C
IH5140 CJE	SPST	16 Pin CERDIP	0°C to 70°C
IH5140 CPE	SPST	16 Pin Plastic DIP	0°C to 70°C
IH5141 MJE	Dual SPST	16 Pin CERDIP	−55°C to 125°C
IH5141 CJE	Dual SPST	16 Pin CERDIP	0°C to 70°C
IH5141 CPE	Dual SPST	16 Pin Plastic DIP	0°C to 70°C
IH5142 MJE	SPDT	16 Pin CERDIP	−55°C to 125°C
IH5142 CJE	SPDT	16 Pin CERDIP	0°C to 70°C
IH5142 CPE	SPDT	16 Pin Plastic DIP	0°C to 70°C
IH5143 MJE	Dual SPDT	16 Pin CERDIP	−55°C to 125°C
IH5143 CJE	Dual SPDT	16 Pin CERDIP	0°C to 70°C
IH5143 CPE	Dual SPDT	16 Pin Plastic DIP	0°C to 70°C
IH5144 MJE	DPST	16 Pin CERDIP	−55°C to 125°C
IH5144 CJE	DPST	16 Pin CERDIP	0°C to 70°C
IH5144 CPE	DPST	16 Pin Plastic DIP	0°C to 70°C
IH5145 MJE	Dual DPST	16 Pin CERDIP	−55°C to 125°C
IH5145 CJE	Dual DPST	16 Pin CERDIP	0°C to 70°C
IH5145 CPE	Dual DPST	16 Pin Plastic DIP	0°C to 70°C

Note: 1. Ceramic (side braze) devices also available; consult factory.
2. MIL temp range parts also available with MIL-STD-883 processing.

FEATURES

- **Super Fast Break-Before-Make Switching**
- **t_{on} 80ns Typ, t_{off} 50ns Typ (SPST Switches)**
- **Power Supply Currents Less Than 1μA**
- **OFF Leakages Less Than 100pA @ 25°C Typical**
- **Non-latching With Supply Turn-off**
- **Single Monolithic CMOS Chip**
- **Plug-in Replacements for IH5040 Family and Part of the DG180 Family to Upgrade Speed and Leakage**
- **Greater Than 1MHz Toggle Rate**
- **Switches Greater Than 20Vp-p Signals With ±15V Supplies**
- **TTL, CMOS Direct Compatibility**
- **Internal Diode in Series with V^+ for Fault Protection**

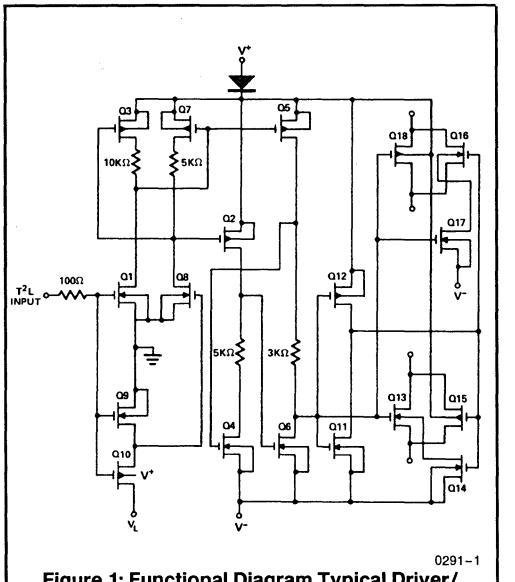


Figure 1: Functional Diagram Typical Driver/ Gate – IH5142

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

$V^+ - V^-$ ..... <36V
$V^+ - V_D$ ..... <30V
$V_D - V^-$ ..... <30V
$V_D - V_S$ ..... <±22V
$V_L - V^-$ ..... <33V
$V_L - V_{IN}$ ..... <30V
V_L ..... <20V
V_{IN} ..... <20V

Current (Any Terminal) ..... <30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Lead Temperature (Soldering 10sec) ..... 300°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6 mW/°C Above 70°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

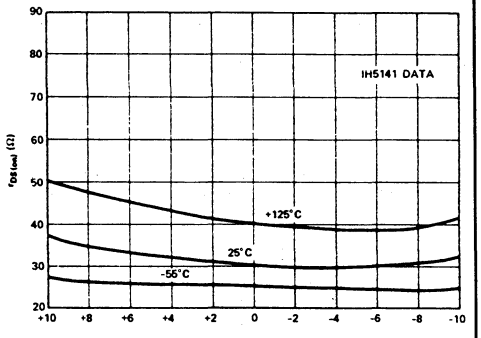
ELECTRICAL CHARACTERISTICS (@ 25°C, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$)

Per Channel		Test Conditions	Min/Max Limits						Units
			Military			Commercial			
Symbol	Characteristic		−55°C	+25°C	+125°C	0	+25°C	+70°C	
LOGIC INPUT									
I_{INH}	Input Logic Current	$V_{IN} = 2.4V$ Note 1	±1	±1	10		±10	10	µA
I_{INL}	Input Logic Current	$V_{IN} = 0.8V$ Note 1	±1	±1	10		±10	10	µA
SWITCH									
$r_{DS(on)}$	Drain-Source On Resistance	$I_S = -10mA$ $V_{ANALOG} = -10V$ to $+10V$	50	50	75	75	75	100	Ω
$\Delta r_{DS(on)}$	Channel to Channel $r_{DS(on)}$ Match			25 (typ)			30 (typ)		Ω
V_{ANALOG}	Min. Analog Signal Handling Capability			±11 (typ)			±10 (typ)		V
$I_{D(off)}$ + $I_{S(off)}$	Switch OFF Leakage Current	$V_D = +10V$, $V_S = -10V$ $V_D = -10V$, $V_S = +10V$		±.5 ±.5	100 100		±5 ±5	100 100	nA
$I_{D(on)}$ + $I_{S(on)}$	Switch On Leakage Current	$V_D = V_S = -10V$ to $+10V$		±1	200		±2	200	nA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off; Any Other Channel Switches See Performance Characteristics		54 (typ)			50 (typ)		dB
t_{on} t_{off}	Switch "ON" Time Switch "OFF" Time	See switching time specifications and timing diagrams.							
$Q_{(INJ.)}$	Charge Injection	See Performance Characteristics		10 (typ)			15 (typ)		pC
OIRR	Min. Off Isolation Rejection Ratio	$f = 1MHz$, $R_L = 100\Omega$, $C_L \leq 5pF$ See Performance Characteristics		54 (typ)			50 (typ)		dB
SUPPLY									
I^+	+ Power Supply Quiescent Current	$V^+ = +15V$, $V^- = -15V$, $V_L = +5V$ See Performance Characteristics	1.0	1.0	10.0	10	10	100	µA
I^-	− Power Supply Quiescent Current		1.0	1.0	10.0	10	10	100	µA
I_L	+5V Supply Quiescent Current		1.0	1.0	10.0	10	10	100	µA
I_{GND}	Gnd Supply Quiescent Current		1.0	1.0	10.0	10	10	100	µA

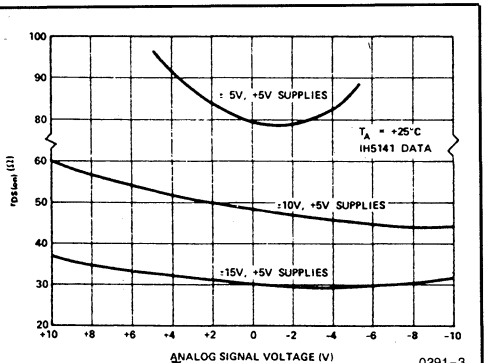
NOTES: 1. Some channels are turned on by high (1) logic inputs and other channels are turned on by low (0) inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to find logical value of logic input required to produce ON or OFF state.
2. Typical values are for design aid only, not guaranteed and not subject to production testing.

NOTE: All typical values have been characterized but are not tested.

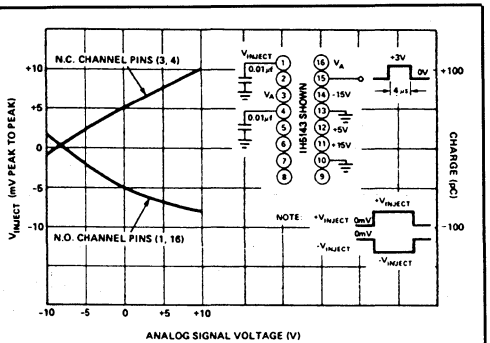
TYPICAL PERFORMANCE CHARACTERISTICS



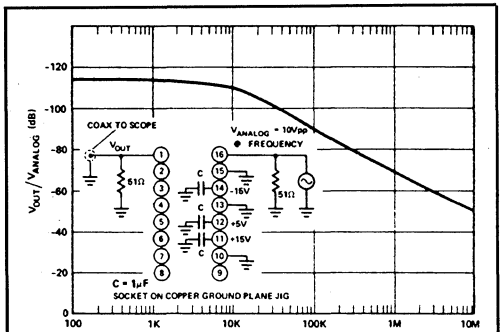
$r_{DS(on)}$ vs. Temp., @ ±15V, +5V Supplies



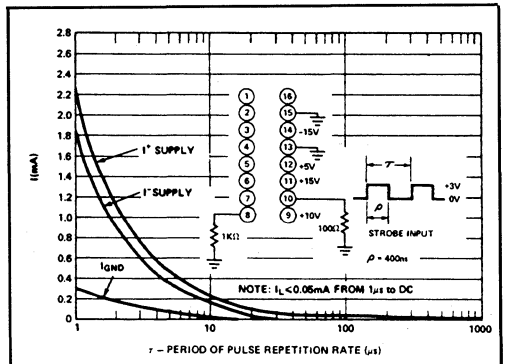
$r_{DS(on)}$ vs. Power Supplies



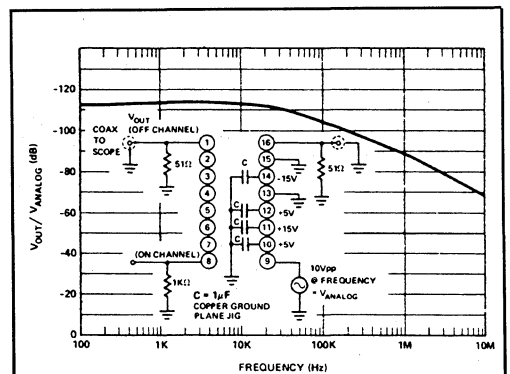
Charge Injection vs. Analog Signal



"OFF" Isolation vs. Frequency



Power Supply Currents vs. Logic Strobe Rate



Channel to Channel Cross Coupling Rejection vs. Frequency

NOTE: All typical values have been characterized but are not tested.

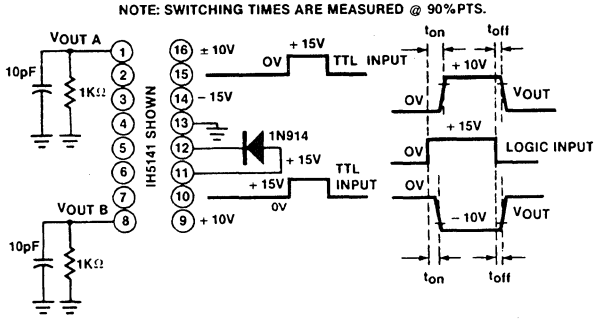
IH5140-IH5145

SWITCHING TIME SPECIFICATIONS

(t_{on}, t_{off} are maximum specifications and t_{on}-t_{off} is minimum specifications)

Part Number	Symbol	Characteristic	Test Conditions	Military			Commercial			Units
				−55°C	+25°C	+125°C	0	+25°C	+70°C	
IH5140-5141	t_{on}	Switch "ON" time	Figure 2*		100			150		ns
	t_{off}	Switch "OFF" time			75			125		
	t_{on}-t_{off}	Break-before-make			10			5		
	t_{on}	Switch "ON" time	Figure 3		150			175		ns
	t_{off}	Switch "OFF" time			125			150		
	t_{on}-t_{off}	Break-before-make			*10 (typ)			5		
IH5142-5143	t_{on}	Switch "ON" time	Figure 2*		175			250		ns
	t_{off}	Switch 'OFF" time			125			150		
	t_{on}-t_{off}	Break-before-make			10			5		
	t_{on}	Switch "ON" time	Figure 3		200			300		ns
	t_{off}	Switch "OFF" time			125			150		
	t_{on}-t_{off}	Break-before-make			*10 (typ)			5		
	t_{on}	Switch "ON" time	Figure 4*		175			250		ns
	t_{off}	Switch "OFF" time			125			150		
	t_{on}-t_{off}	Break-before-make			10			5		
	t_{on}	Switch "ON" time	Figure 5*		200			300		ns
	t_{off}	Switch "OFF" time			125			150		
	t_{on}-t_{off}	Break-before-make			10			5		
IH5144-5145	t_{on}	Switch "ON" time	Figure 2*		175			250		ns
	t_{off}	Switch "OFF" time			125			150		
	t_{on}-t_{off}	Break-before-make			10			5		
	t_{on}	Switch "ON" time	Figure 3		200			300		ns
	t_{off}	Switch "OFF" time			125			150		
	t_{on}-t_{off}	Break-before-make			*10			5		

NOTE: SWITCHING TIMES ARE MEASURED @ 90% PTS. * Typical values for design aid only, not guaranteed nor subject to production testing.



0291-8

Figure 2.

NOTE: All typical values have been characterized but are not tested.

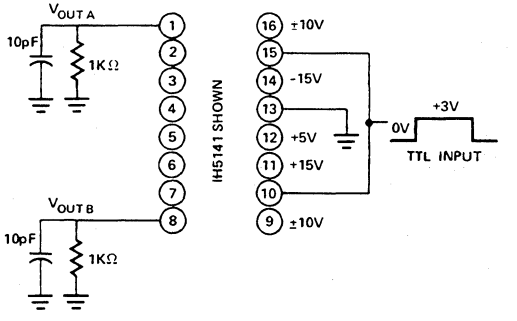


Figure 3.

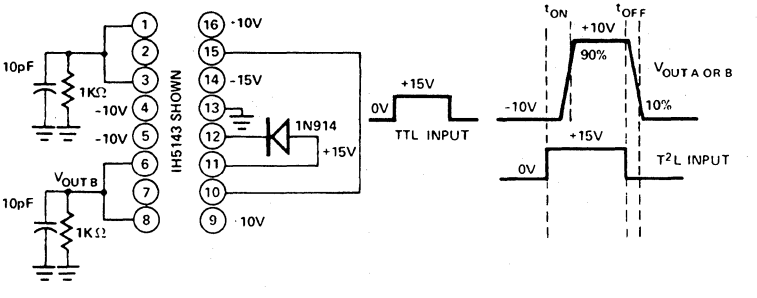


Figure 4.

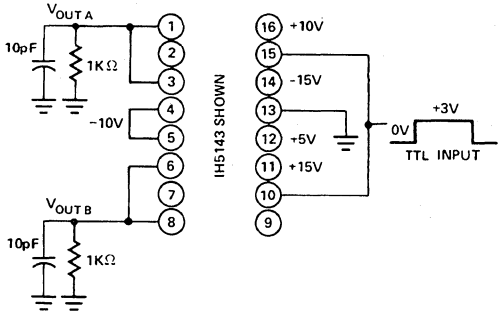
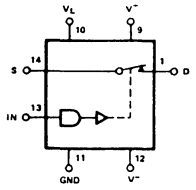


Figure 5.

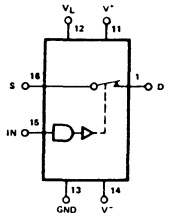
NOTE: All typical values have been characterized but are not tested.

FLATPACK (FD-2)



0291-12

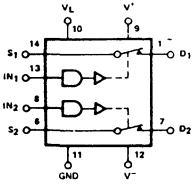
DIP (JE, PE)



0291-13

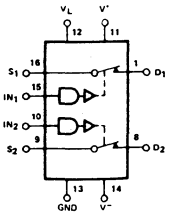
SPST
IH5140 ($r_{DS(on)} < 75\Omega$)

FLATPACK (FD-2)



0291-14

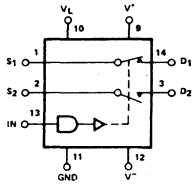
DIP (JE, PE)



0291-15

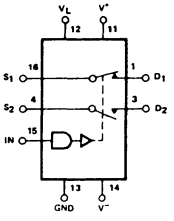
DUAL SPST
IH5141 ($r_{DS(on)} < 75\Omega$)

FLATPACK (FD-2)



0291-17

DIP (JE, PE)



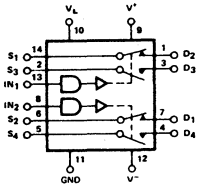
0291-18

SPDT
IH5142 ($r_{DS(on)} < 75\ \Omega$)

Figure 6: Switching State Diagrams

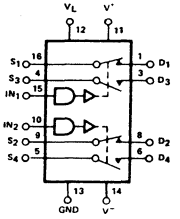
NOTE: All typical values have been characterized but are not tested.

FLATPACK (FD-2)



0291-20

DIP (JE, PE) (DG191 EQUIVALENT)

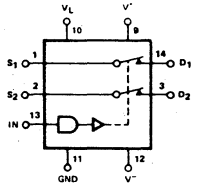


0291-21

DUAL SPDT
IH5143 ($r_{DS(on)}$ < 75Ω)

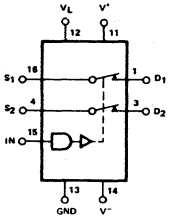
SWITCH STATES ARE FOR LOGIC "1" INPUT

FLATPACK (FD-2)



0291-22

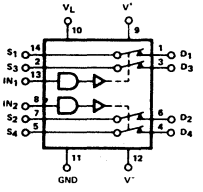
DIP (JE, PE)



0291-23

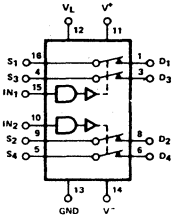
DPST
IH5144 ($r_{DS(on)}$ < 75Ω)

FLATPACK (FD-2)



0291-25

DIP (JE, PE) (DG185 EQUIVALENT)



0291-26

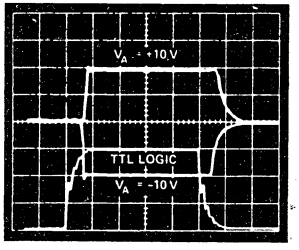
DUAL DPST
IH5145 ($r_{DS(on)}$ < 75Ω)

Figure 6: Switching State Diagrams (Continued)

NOTE: All typical values have been characterized but are not tested.

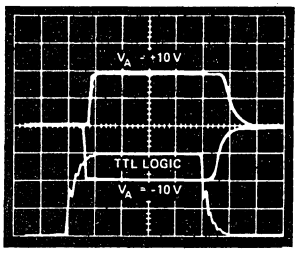
TYPICAL SWITCHING WAVEFORMS SCALE: VERT. = 5V/DIV. HORIZ. = 100ns/DIV.

TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 8)



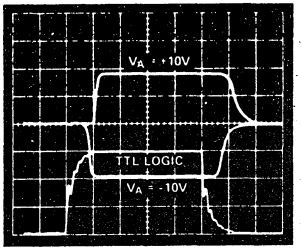
-55°C

0291-27



+25°C

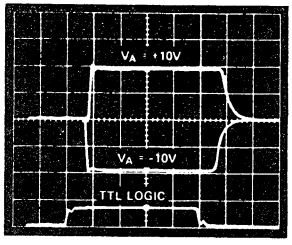
0291-28



+125°C

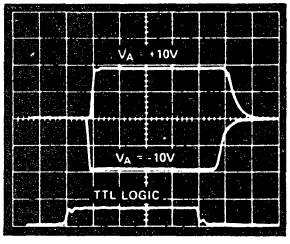
0291-29

TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 9)



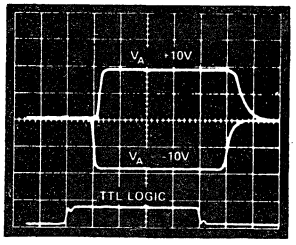
-55°C

0291-30



+25°C

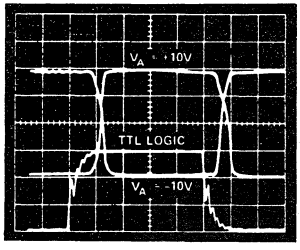
0291-31



+125°C

0291-32

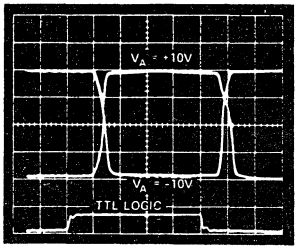
TTL OPEN COLLECTOR LOGIC DRIVE
(Corresponds to Figure 10)



+25°C

0291-33

TTL OPEN COLLECTOR LOGIC DRIVE
(Corresponds to Figure 11)



+25°C

0291-34

NOTE: All typical values have been characterized but are not tested.

APPLICATION NOTE

To maximize switching speed on the IH5140 family, TTL open collector logic (15V with a 1kΩ or less collector resistor) should be used. This configuration will result in (SPST) t_{on} and t_{off} times of 80ns and 50ns, for signals between −10V and +10V. The SPDT and DPST switches are approximately 30ns slower in both t_{on} and t_{off} with the same drive configuration. 15V CMOS logic levels can be used (0V to +15V), but propagation delays in the CMOS logic will slow down the switching (typical 50ns → 100ns delays).

When driving the IH5140 Family from either +5V TTL or CMOS logic, switching times run 20ns slower than if they were driven from +15V logic levels. Thus t_{on} is about 105ns, and t_{off} 75ns for SPST switches, and 135ns and 105ns (t_{on}, t_{off}) for SPDT or DPST switches. The low level drive can be made as fast as the high level drive if ±5V strobe levels are used instead of the usual 0V → +3.0V drive. Pin 13 is taken to −5V instead of the usual GND and strobe input is taken from +5V to −5V levels as shown in Figure 7.

The typical channel of the IH5140 family consists of both P and N-channel MOSFETs. The N-channel MOSFET uses a "Body Puller" FET to drive the body to −15V (±15V supplies) to get good breakdown voltages when the switch is in the off state (See Fig. 8). This "Body Puller" FET also allows the N-channel body to electrically float when the switch is in the on state producing a fairly constant $R_{DS}(ON)$ with different signal voltages. While this "Body Puller" FET improves switch performance, it can cause a problem when analog input signals are present (negative signals only) and power supplies are off. This fault condition is shown in Figure 9.

Current will flow from −10V analog voltage through the drain to body junction of Q1, then through the drain to body junction of Q3 to GND. This means that there is 10V across two forward-biased silicon diodes and current will go to whatever value the input signal source is capable of supplying. If the analog input signal is derived from the same supplies as the switch this fault condition cannot occur. Turning off the supplies would turn off the analog signal at the same time.

This fault situation can also be eliminated by placing a diode in series with the negative supply line (pin 14) as shown in Figure 10. Now when the power supplies are off and a negative input signal is present this diode is reverse biased and no current can flow.

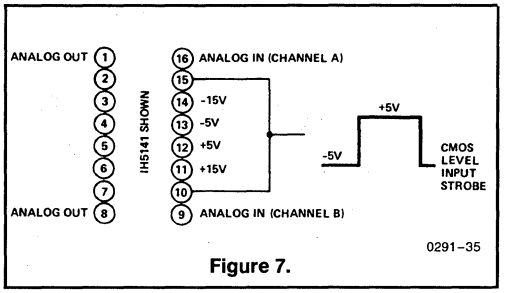


Figure 7.

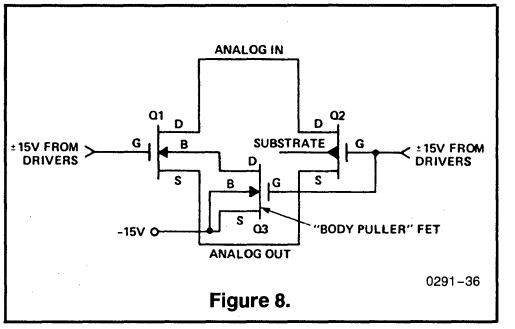


Figure 8.

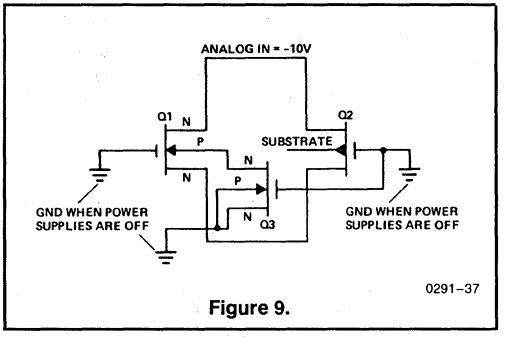


Figure 9.

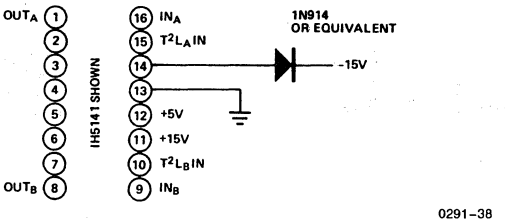


Figure 10.

NOTE: All typical values have been characterized but are not tested.

APPLICATIONS

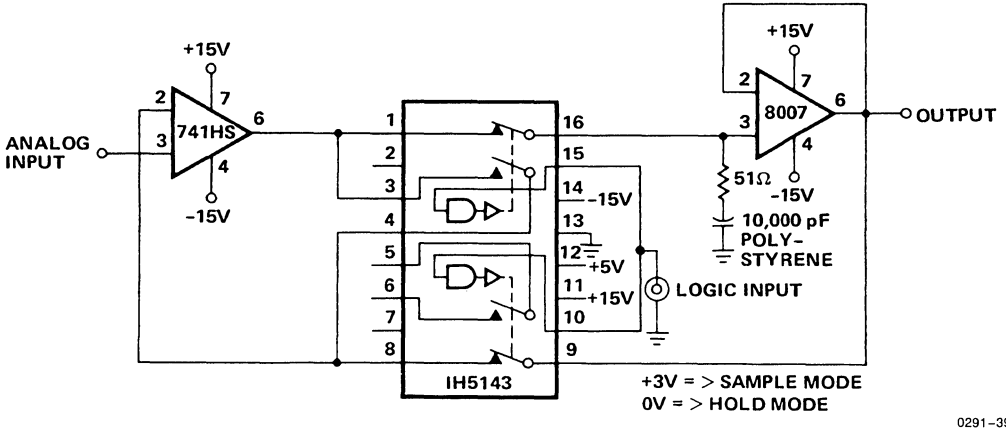
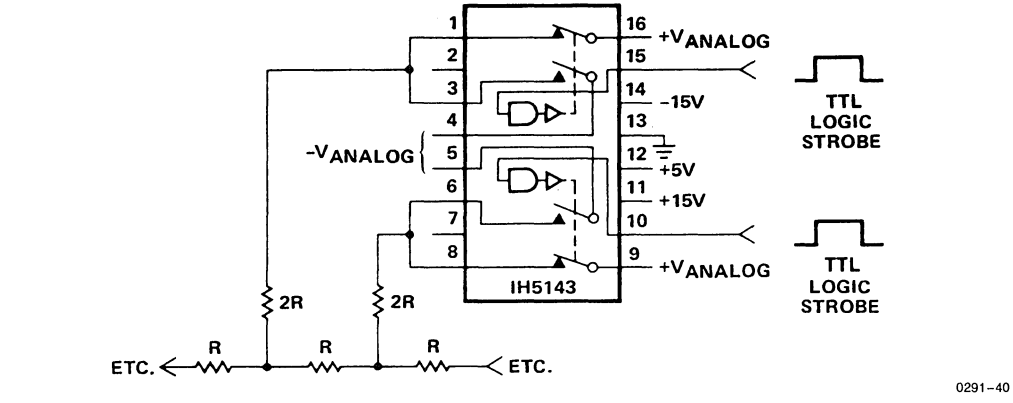


Figure 11: Improved Sample and Hold Using IH5143

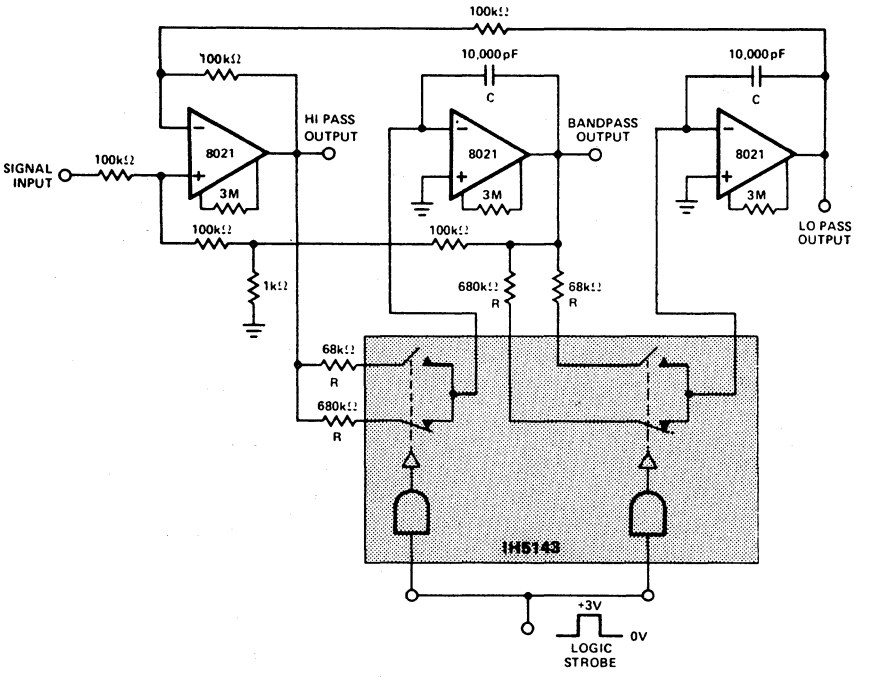


EXAMPLE: If $-V_{ANALOG} = -10VDC$ and $+V_{ANALOG} = +10VDC$ then Ladder Legs are switched between $\pm 10VDC$, depending upon state of Logic Strobe.

Figure 12: Using the CMOS Switch to Drive an R/2R Ladder Network (2 Legs)

NOTE: All typical values have been characterized but are not tested.

APPLICATIONS (Continued)



0291-41

CONSTANT GAIN, CONSTANT Q, VARIABLE FREQUENCY FILTER WHICH PROVIDES SIMULTANEOUS LOWPASS, BANDPASS, AND HIGHPASS OUTPUTS. WITH THE COMPONENT VALUES SHOWN, CENTER FREQUENCY WILL BE 235Hz AND 23.5Hz FOR HIGH AND LOW LOGIC INPUTS RESPECTIVELY, Q = 100, AND GAIN = 100.

$$f_n = \text{CENTER FREQUENCY} = \frac{1}{2\pi RC}$$

Figure 13: Digitally Tuned Low Power Active Filter

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

IH5151
High-Level CMOS Analog Switches

GENERAL DESCRIPTION

The IH5151 family of solid state analog switches are designed using an improved, high voltage CMOS technology. Destructive latchup has been eliminated. Early CMOS switches were destroyed when power supplies were removed with an input signal present; the IH5151 CMOS technology has eliminated this problem.

Key performance advantages of the 5151 series are TTL compatibility and ultra low-power operation. $R_{DS(on)}$ switch resistance is typically in the 14Ω To 18Ω Area, for signals in the −10V to +10V range. Quiescent current is less than 10μA. The 5151 also guarantees Break-Before-Make switching which is logically accomplished by extending the t_{ON} time (200nsec typ.) such that it exceeds t_{OFF} time (120nsec typ.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. The need for external logic required to avoid channel to channel shorting during switching is thus eliminated.

See HI-514X for other functions.

FEATURES

- **Low $R_{DS(ON)}$ — 25Ω**
- **Switches Greater Than 20Vpp Signals With ±15V Supplies**
- **Quiescent Current Less Than 100μA**
- **Break-Before-Make Switching t_{OFF} 120nsec Typ., t_{ON} 200nsec Typical**
- **TTL, CMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **Complete Monolithic Construction**
- **±5V to ±15V Supply Range**

CMOS ANALOG SWITCH PRODUCT CONDITIONING

- **The Following Processes Are Performed 100% in Accordance With MIL-STD-883**
- **Precap Visual — Method 2010, Cond. B**
- **Stabilization Bake — Method 1008**
- **Temperature Cycle — Method 1010**
- **Centrifuge — Method 2001, Cond. E**
- **Hermeticity — Method 1014, Cond. A, C**
- **(Leak Rate $< 5 \times 10^{-7}$ atm cc/s)**

ORDERING INFORMATION

ORDER PART NUMBER	FUNCTION	PACKAGE	TEMPERATURE RANGE	HARRIS EQUIVALENT
IH5151MJE	Dual SPDT	16 Pin Cerdip	-55°C to +125°C	HI-5051
IH5151CJE	Dual SPDT	16 Pin Cerdip	0°C to 70°C	HI-5051
IH5151CPE	Dual SPDT	16 Pin Plastic DIP	0°C to 70°C	HI-5051

NOTES: 1. Ceramic (side braze) devices also available; consult factory.
2. MIL temp range parts also available with MIL-STD-883 processing.

7

304300-003

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V^+, V^- ..... <36V
V^+, V_D ..... <30V
V_D, V^- ..... <30V
V_D, V_S ..... < ±22V
V_L, V^- ..... <33V
V_L, V_{IN} ..... <30V
V_L ..... <20V
V_{IN} ..... <20V
Current (Any Terminal) ..... <50mA
Storage Temperature ..... −65°C to +150°C

Operating Temperature ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6mW/°C Above 70°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

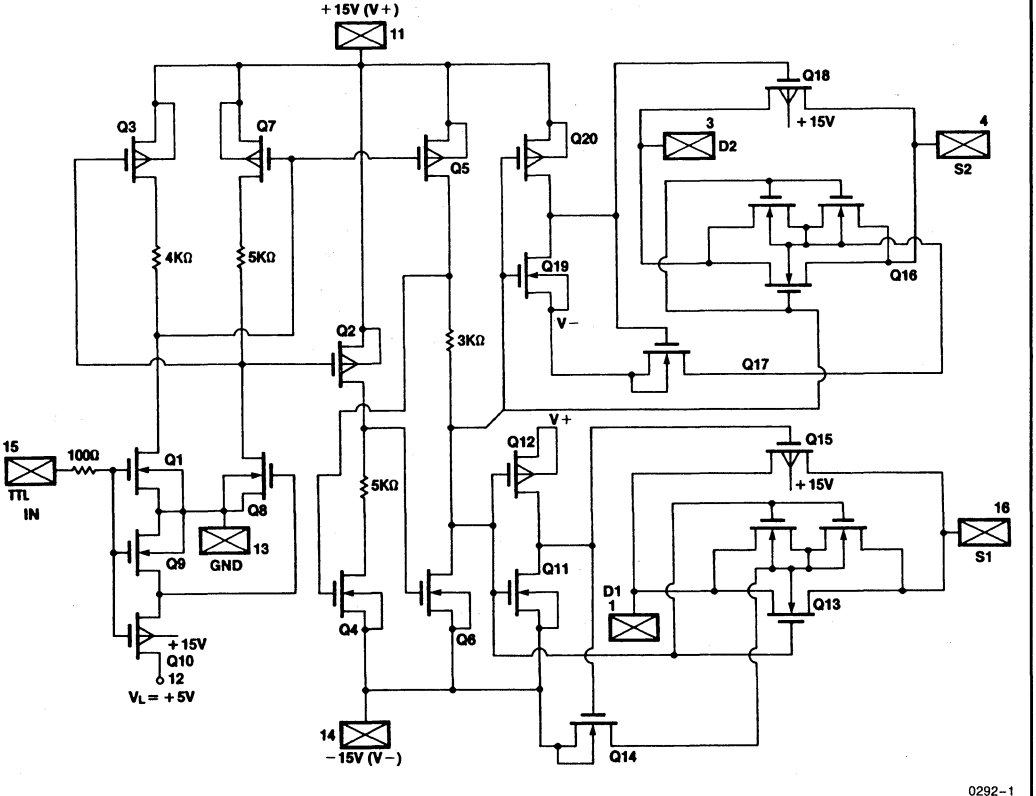


Figure 1: Functional Diagram (Typical Switch Schematic – IH5150 in 16 pin DIP PKG.)

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (T_A @ 25°C, $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$)

Per Channel		Test Conditions	Min/Max Limits						Units
			Military			Commercial			
Symbol	Characteristic		−55°C	+25°C	+125°C	0	+25°C	+70°C	
$I_{IN(ON)}$	Input Logic Current	$V_{IN} = 2.4V$ (Note 1)	±1	±1	±10		±1	±10	µA
$I_{IN(OFF)}$	Input Logic Current	$V_{IN} = 0.8V$ (Note 1)	±1	±1	±10		±1	±10	µA
$R_{DS(ON)}$	Drain-Source On Resistance	$V_D = \pm 10V$, $I_S = -10mA$	25	25	50		30		Ω
$\Delta R_{DS(ON)}$	Channel to Channel $R_{DS(ON)}$ Match			10 (Typ)			15 (Typ)		Ω
V_{ANALOG}	Min. Analog Signal Handling Capability			±14 (Typ)			±14 (Typ)		V
$I_{D(OFF)}$ $I_{S(OFF)}$	Switch OFF Leakage Current	$V_{ANALOG} = -10V$ to $+10V$		±1.0	100		±2.0	100	nA
$I_{D(ON)} + I_{S(ON)}$	Switch On Leakage Current	$V_D = V_S = -10V$ to $+10V$		±1.0	100		±2.0	100	nA
$Q_{(INJ)}$	Charge Injection	See Figure 4		(10) (Typ)			(10) (Typ)		mV
OIRR	Min. Off Isolation Rejection Ratio	$f = 1MHz$, $R_L = 100\Omega$, $C_L \leq 5pF$, See Figure 5		54 (Typ)			50 (Typ)		dB
SUPPLY									
I^+	+Power Supply Quiescent Current	$V_1 = +15V$, $V_2 = -15V$. $V_L = +5V$, $V_R = 0$	10	10	100		10		µA
I^-	−Power Supply Quiescent Current		10	10	100		10		µA
I_L	+5V Supply Quiescent Current		10	10	100		10		µA
I_{GND}	Gnd Supply Quiescent Current		10	10	100		10		µA
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio	One Channel Off; Any Other Channel Switches as per Figure 8		54 (Typ)			50 (Typ)		dB

NOTE 1. Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to find logical value of logic input required to produce "ON" or "OFF" state.

SWITCHING TIME SPECIFICATION

IH5148 SPST SWITCH

Symbol	Parameter	Test Conditions	Min	Max	Units
t_{on}	Switch "on" time	$R_L = 1K\Omega$, $V_{ANALOG} = -10V$		250	ns
t_{off}	Switch "off" time	$T_O + 10V$; See Figures 3 and 6		200	ns

IH5149 DPST SWITCH

Symbol	Parameter	Test Conditions	Min	Max	Units
t_{on}	Switch "on" time	$R_L = 1K\Omega$, $V_{ANALOG} = -10V$		350	ns
t_{off}	Switch "off" time	$T_O + 10V$; See Figures 3 and 6		250	ns

IH5150 & IH5151 SPDT SWITCH

Symbol	Parameter	Test Conditions	Min	Max	Units
t_{on}	Switch "on" time	$R_L = 1K\Omega$, $V_{ANALOG} = -10V$		500	ns
t_{off}	Switch "off" time	$T_O + 10V$; See Figures 3 and 6		250	ns

NOTE 2. For IH5150 & IH5151 devices, channels which are off for logic input ≥ 2.4V (Pins 3 & 4 on 5150, & Pins 3 & 4, 5 & 6 on 5151) have slower t_{on} time, than channels on Pins 1, 16, & 8, 9. This is done so switch will maintain break-before-make action when connected in DT configuration, i.e. Pin 1 connected in Pin 3.

NOTE: All typical values have been characterized but are not tested.

IH5148-IH5151

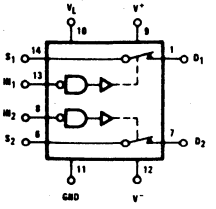
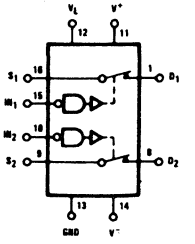
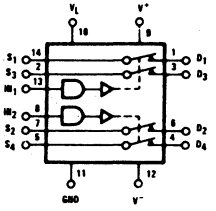
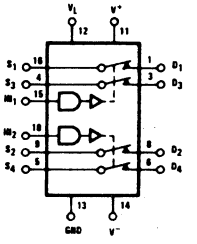
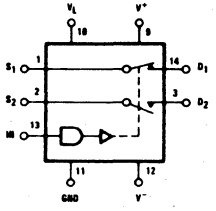
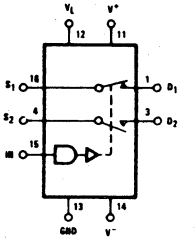
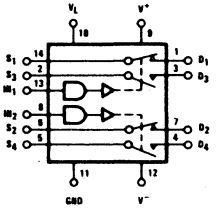
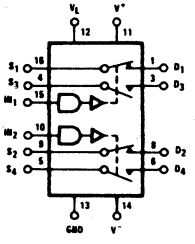
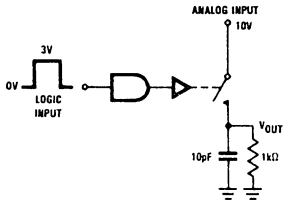
SWITCH STATES ARE FOR LOGIC "1" INPUT	FLAT PACKAGE	DIP (DE) PACKAGE
DUAL SPST IH5148	 0292-2	 0292-3
DUAL DPST IH5149	 0292-5	 0292-6
SPDT IH5150	 0292-7	 0292-8
DUAL SPDT IH5151	 0292-10	 0292-11

Figure 2: Switching State Diagrams

NOTE: All typical values have been characterized but are not tested.

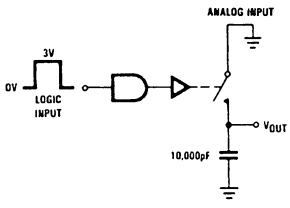
IH5148-IH5151

TEST CIRCUITS



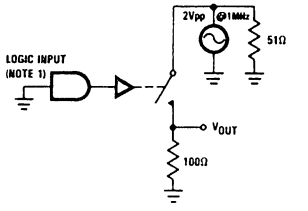
0292-12

Figure 3



0292-13

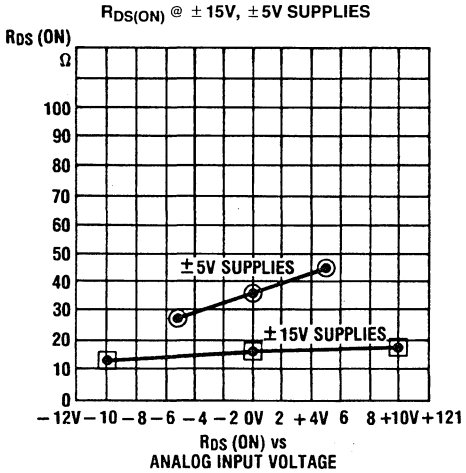
Figure 4



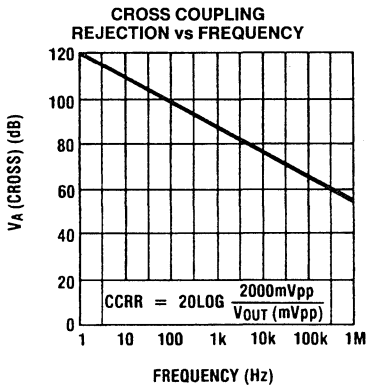
0292-14

Figure 5

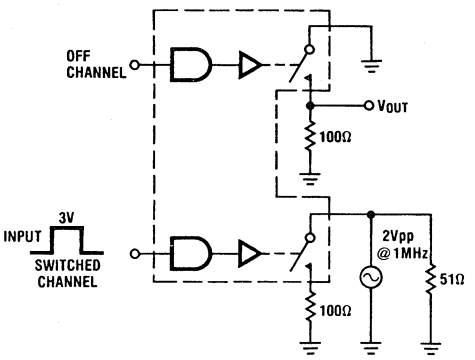
TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel)



0292-15



0292-16



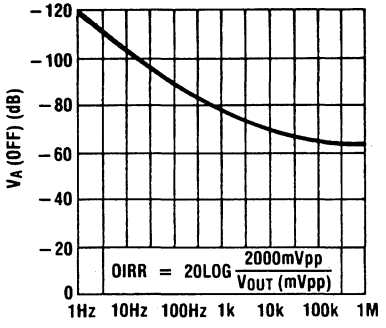
0292-17

CROSS COUPLING
REJECTION TEST CIRCUIT

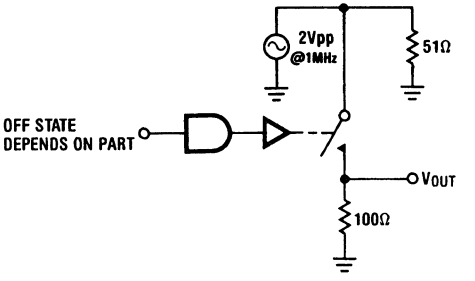
NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (Per Channel) (Continued)

OFF ISOLATION vs FREQUENCY



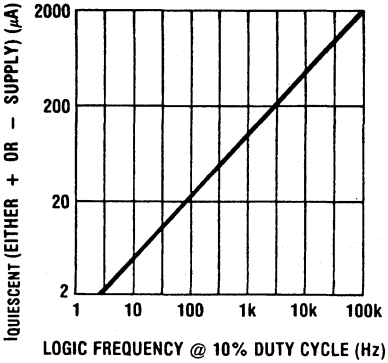
0292-18



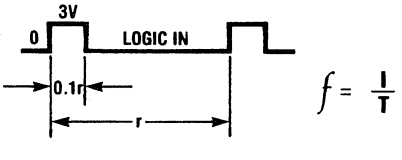
0292-19

OFF ISOLATION TEST CIRCUIT

POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE

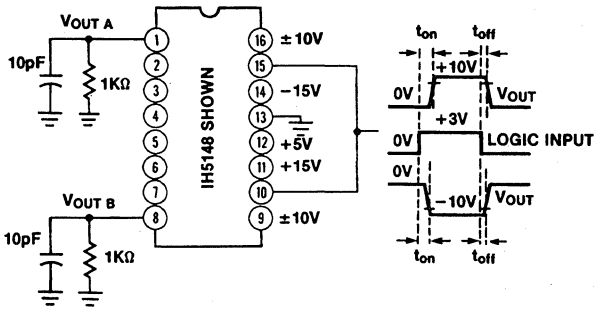


0292-20



0292-21

LOGIC INPUT WAVEFORM



0292-22

Figure 6: Switching Time Test Circuit

NOTE: All typical values have been characterized but are not tested.

Nulling Out Charge Injection:

Charge injection (Qinj. on spec. sheet) is caused by gate to drain, or gate to source capacitance of the output switch MOSFET. The gates of these MOSFETs typically swing from −15V to +15V as a rapidly changing pulse; thus this 30Vpp pulse is coupled through gate capacitance to output load capacitance, and the output "step" is a voltage divider from this combination. For example:

$$\text{Qinject (Vpp)} \cong \frac{C_{gate}}{C_{Load}} \times 30\text{V step.}$$

i.e.

$C_{gate} = 1.5\text{pF}$, $C_{Load} = 1000\text{pF}$, then

$$\text{Qinject(Vpp)} = \frac{1.5\text{pF}}{1000\text{pF}} \times 30\text{V step} = 45\text{mVpp}$$

Thus if you are using switch in a Sample & Hold application with $C_{sample} = 1000\text{pF}$, a 45mVpp "Sample to Hold error step" will occur.

To null this error step out to zero the following circuit can be used:

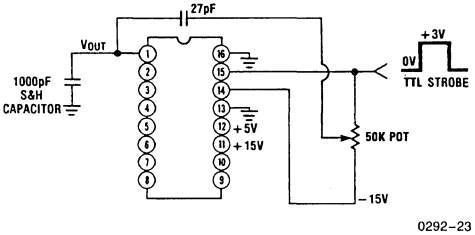


Figure 7: Adjustable Charge Injection Compensation Circuit

The circuit shown above nulls out charge injection effects on switch pins 1 and 16; a similar circuit would be required on switch pins 8 and 9.

Simply adjust the pot until $V_{OUT} = 0\text{mVpp}$ pulse, with $V_{ANALOG} = 0\text{V}$.

If you do not desire to do any adjusting, but wish the least amount of charge injection possible, then the following circuit should be used:

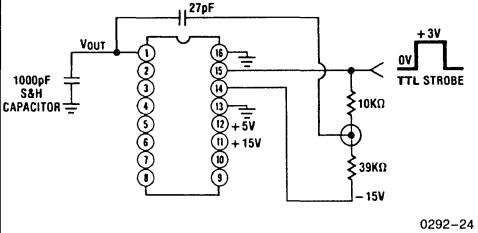


Figure 8: No-Adjust Charge Injection Compensation Circuit

This configuration will produce a typical charge injection of $V_{OUT} \leq 10\text{mVpp}$ into the 1000pF S & H capacitor shown.

Fault Condition Protection

If your system has analog voltage levels which are independent of the ±15V (Power Supplies), and these analog levels can be present when supplies are shut off, you should add fault protection diodes as shown below:

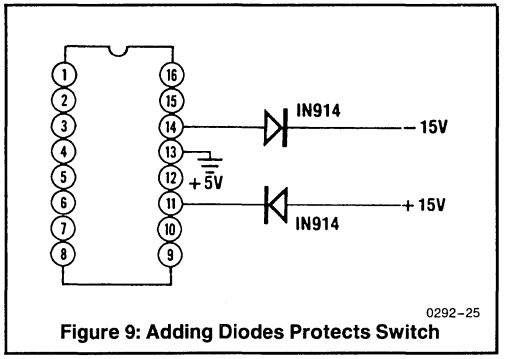


Figure 9: Adding Diodes Protects Switch

If the analog input levels are below ±15V, the pn junctions of Q13 & Q15 are reversed biased. However if the ±15V supplies are shut off and analog levels are still present, the configuration becomes:

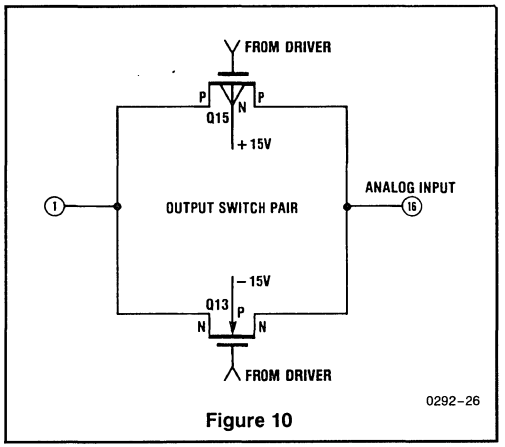


Figure 10

NOTE: All typical values have been characterized but are not tested.

The need for these diodes, in this circumstance, is shown below:

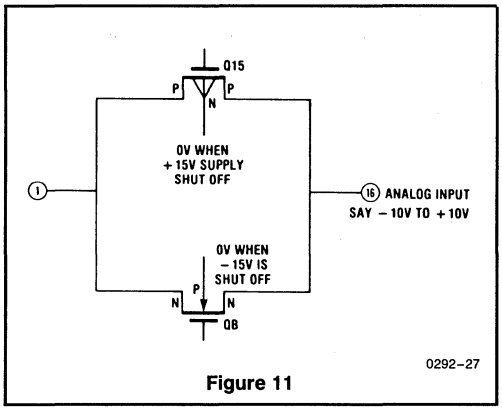


Figure 11

If ANALOG in is greater than 1V, then the pn junction of Q15 is forward biased and excessive current will be drawn. The addition of IN914 diodes prevents the fault currents from destroying the switch. A similar event would occur if ANALOG in was less than or equal to −1V, wherein Q13 would become forward biased. The IN914 diodes form a "back to back" diode arrangement with Q13 & Q15 bodies.

This structure provides a degree of overvoltage protection when supplies are on normally, and analog input level exceeds supplies.

This circuit will switch up to about ±18V ANALOG overvoltages. Beyond this drain(N) to body(P) breakdown VOLTAGE of Q13 limits overvoltage protection.

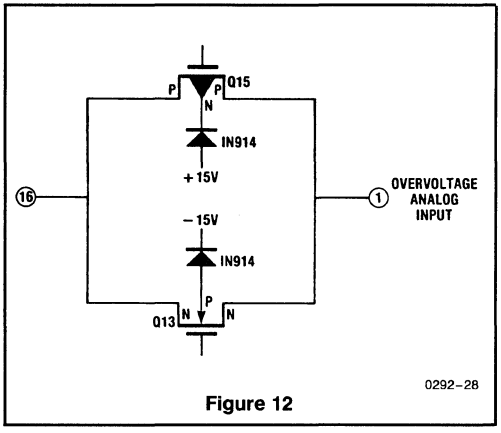


Figure 12

NOTE: All typical values have been characterized but are not tested.

IH5341
Dual SPST CMOS RF/Video Switch

GENERAL DESCRIPTION

The IH5341 is a dual SPST, CMOS monolithic switch which uses a "Series/Shunt" ("T" switch) configuration to obtain high "OFF" isolation while maintaining good frequency response in the "ON" condition.

Construction of remote and portable video equipment with extended battery life is facilitated by the extremely low current requirements. Switching speeds are typically t_{on} = 150ns and t_{off} = 80ns, and "Break-Before-Make" switching is guaranteed.

Switch "ON" resistance is typically 40Ω–50Ω with ±15V power supplies, increasing to typically 175Ω for ±5V supplies. The devices are available in TO-100 and 14-pin epoxy DIP packages.

FEATURES

- $R_{DS(on)} < 75\Omega$
- **Switch Attenuation Varies Less Than 3dB From DC to 100MHz**
- **"OFF" Isolation > 70dB Typical @ 10MHz**
- **Cross Coupling Isolation > 60dB @ 10MHz**
- **Compatible With TTL, CMOS Logic**
- **Wide Operating Power Supply Range**
- **Power Supply Current ≤ 1μA**
- **"Break-Before-Make" Switching**
- **Fast Switching (80ns/150ns Typ)**

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH5341CPD	0 to +70°C	14-pin PLASTIC DIP
IH5341ITW	−20°C to +85°C	10-pin TO-100
IH5341MTW	−55°C to +125°C	10-pin TO-100

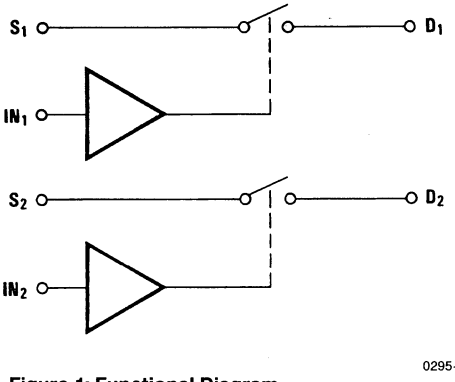
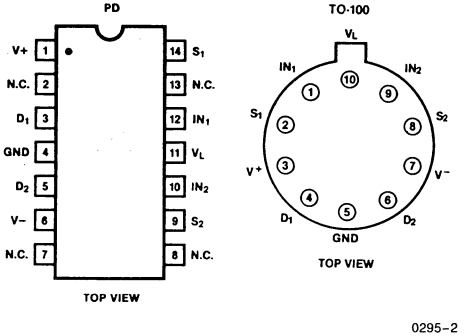


Figure 1: Functional Diagram (Switches are open for a logical "0" control input, and closed for a logical "1" control input.)



Outline dwg: PD **Outline dwg: TW**

Figure 2: Pin Configurations

305528-003

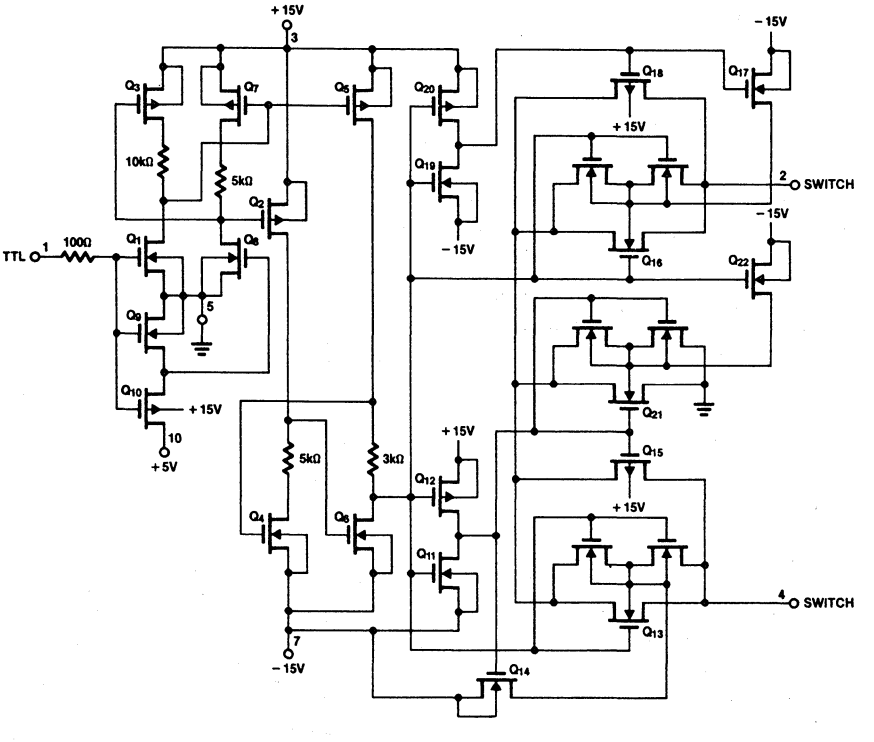
NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V+ to Ground ..... +18V
V− to Ground ..... −18V
V_L to Ground ..... V+ to V−
Logic Control Voltage ..... V+ to V−
Analog Input Voltage ..... V+ to V−
Current (any Terminal) 50mA
Operating Temperature:
(M Version) ..... −55°C to +125°C
(I Version) ..... −25°C to +85°C
(C Version) ..... 0°C to +70°C

Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation 250mW
Derate above 25°C @ ..... 7.5mW/°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*



0295–3

Figure 3: Equivalent Schematic Diagram IH5341ITW (½ of actual circuit on chip shown)

NOTE: All typical values have been characterized but are not tested.

DC ELECTRICAL CHARACTERISTICS

$V^+ = +15V$, $V_L = +5V$, $V^- = -15V$, $T_A = 25°C$ unless otherwise specified.

Symbol	Parameter	Test Conditions	Typ	M Grade Device			I/C Grade Device			Units
				−55°C	+25°C	+125°C	−25/ 0°C	+25°C	+85/ +70°C	
V^+ V_L V^-	Supply Voltage Ranges Positive Supply Logic Supply Negative Supply	(Note 3)	 4.5>16 4.5>V^+ −4>−16							V
$R_{DS(on)}$	Switch "ON" Resistance (Note 4)	$V_D = \pm 5V$ $I_S = 10mA$, $V_{IN} \geq 2.4V$ $V_D = \pm 10V$		75 125	75 125	100 175	75 150	75 150	100 175	Ω
$R_{DS(on)}$	Switch "ON" Resistance	$V^+ = V_L = +5V$, $V_{IN} = 3V$ $V^- = -5V$, $V_D = \pm 3V$ $I_S = 10mA$		250	250	350	300	300	350	
$\Delta R_{DS(on)}$	On Resistance Match Between Channels	$I_S = 10mA$, $V_D = \pm 5V$	5							
V_{IH} V_{IL}	Logical "1" Input Voltage Logical "0" Input Voltage		>2.4 <0.8							V
$I_{D(off)}$ or $I_{S(off)}$	Switch "OFF" Leakage (Notes 2 and 4)	$V_{S/D} = \pm 5V$ $V_{IN} \leq 0.8V$ $V_{S/D} = \pm 14V$			±0.5 ±0.5	50 50		±1.0 ±1.0	100 100	nA
$I_{D(on)}$ + $I_{S(on)}$	Switch "ON" Leakage	$V_{S/D} = \pm 5V$ $V_{IN} \geq 2.4V$ $V_{S/D} = \pm 14V$			±1 ±1	50 100		±2 ±2	100 100	
I_{IN}	Input Logic Current	$V_{IN} \geq 2.4V$ or $<0V$	0.1	±1	±1	10	±1	±1	10	
I^+	Positive Supply Quiescent Current	$V_{IN} = 0V$ or $+5V$	0.1	1	1	10	1	1	10	µA
I^-	Negative Supply Quiescent Current	$V_{IN} = 0V$ or $+5V$	0.1	1	1	10	1	1	10	
I_L	Logic Supply Quiescent Current	$V_{IN} = 0V$ or $+5V$	0.1	1	1	10	1	1	10	

NOTES: 1. Typical values are not tested in production. They are given as a design aid only.
2. Positive and negative voltages applied to opposite sides of switch, in both directions successively.
3. These are the operating voltages at which the other parameters are tested, and are not directly tested.
4. The logic inputs are either greater than or equal to 2.4V or less than or equal to 0.8V, as required, for this test.

AC ELECTRICAL CHARACTERISTICS

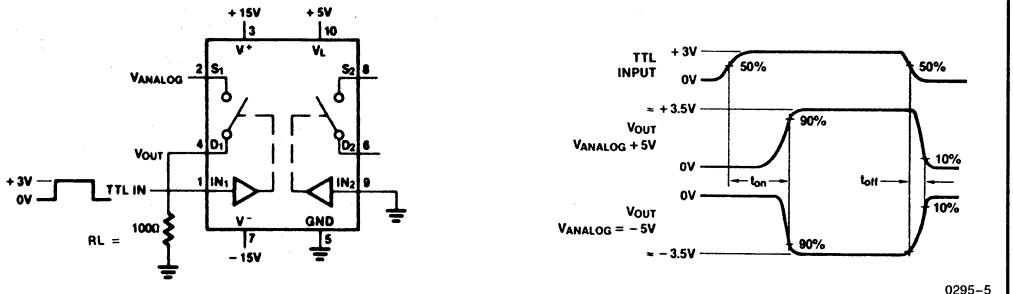
$V^+ = +15V$, $V_L = +5V$, $V^- = 0V$, $T_A = 25°C$ unless otherwise specified (Note 5).

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{on}	Switch "ON" Time	See Figure 4		150	300	ns
t_{off}	Switch "OFF" Time	See Figure 4		80	150	
OIRR	"OFF" Isolation Rejection Ratio	See Figure 5 (Note 6)		70		dB
CCRR	Cross Coupling Rejection Ratio	See Figure 6 (Note 6)		60		
f_{3dB}	Switch Attenuation 3dB Frequency	See Figure 7 (Note 6)		100		

NOTES: 5. All AC parameters are sample tested only.
6. Test circuit should be built on copper clad ground plane board, with correctly terminated coax leads, etc.

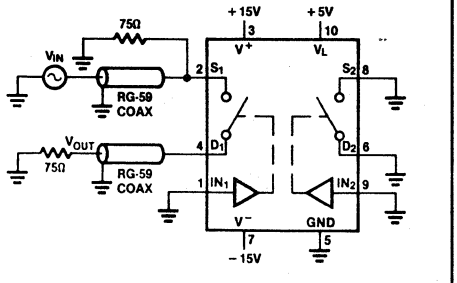
NOTE: All typical values have been characterized but are not tested.

TEST CIRCUITS



Note: Only one channel shown. Other acts identically.

Figure 4: Switching Time Test Circuit and Waveforms

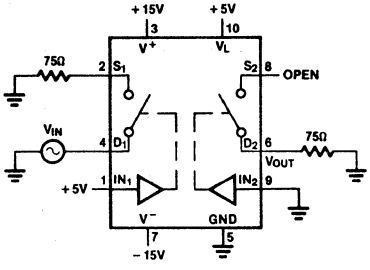


$V_{IN} = \pm 5V\ (10V_{p\text{-}p})$ @ f = 10MHz

$$OIRR = 20\log\frac{V_{IN}}{V_{OUT}}$$

Note: Only one channel shown. Other acts identically.

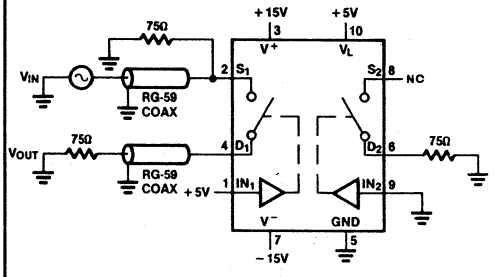
Figure 5: OFF Isolation Test Circuit



$V_{IN} = 225mVrms$ @ f = 10MHz

$$CCRR = 20\log\frac{V_{IN}}{V_{OUT}}$$

Figure 6: Cross-Coupling Rejection Test Circuit



$$ATTN: = 20\ \log_{10}\frac{R_L}{R_{DS(on)} + R_L}$$

Nominally, at DC, this ratio is equal to −4dB. When the attenuation reaches −1dB, the frequency at which this occurs is f_{3dB}.

Note: Only one channel shown. Other acts identically.

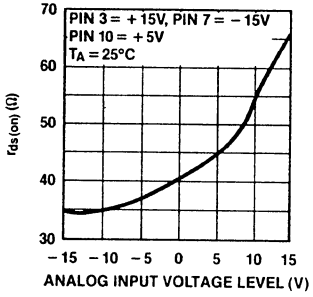
Figure 7: Switch Attenuation Versus Frequency, Test Circuit

NOTE: All typical values have been characterized but are not tested.

IH5341

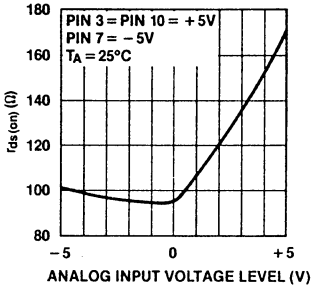
TYPICAL PERFORMANCES CHARACTERISTICS

$R_{DS(on)}$ Versus Analog Input Voltage with ±15V Power Supplies



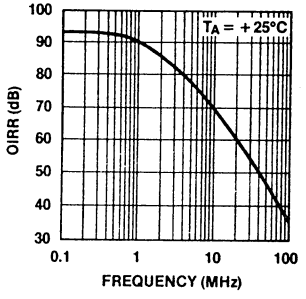
0295-9

$R_{DS(on)}$ Versus Analog Input Level with ±5V Power Supplies



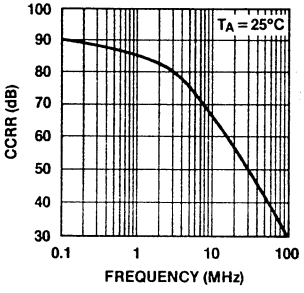
0295-10

OIRR (OFF Isolation Rejection) Versus Frequency (See Figure 5)



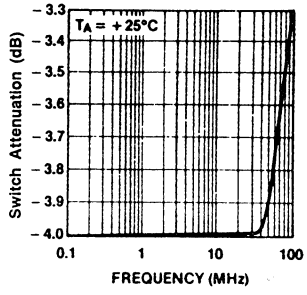
0295-11

CCRR (Cross Coupling Rejection) Versus Frequency (See Figure 6)

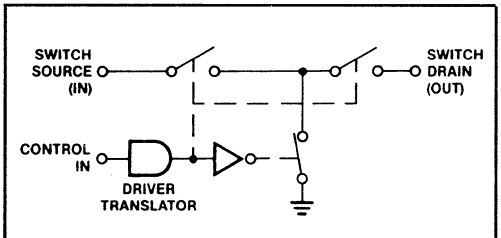


0295-12

Typical Switch Attenuation Versus Frequency (R_L = 75Ω, See Figure 7)

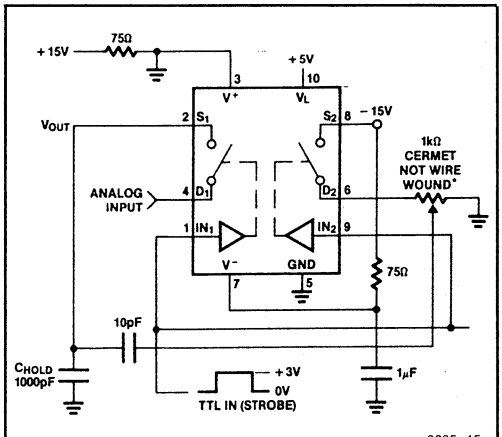


0295-13



0295-14

Figure 8: Internal Switch Configuration



0295-15

*Adjust pot for 0mV$_{p-p}$ step @ V_{OUT} with no analog (AC) signal present

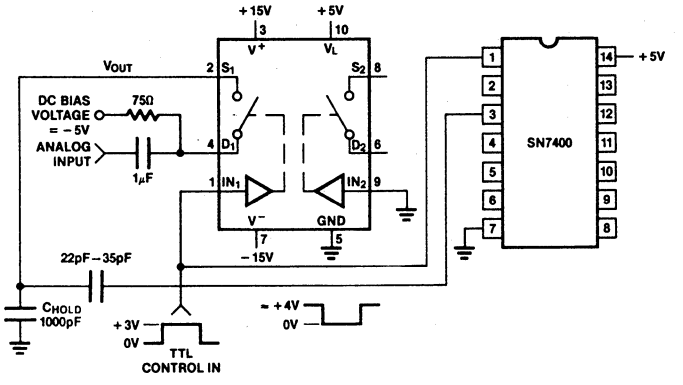
Figure 9: Charge Injection Compensation

DETAILED DESCRIPTION

As can be seen in Figure 8, the switch circuitry is of the so-called "T" configuration, where a shunt switch is closed when the switch is open. This provides much better isolation between the input and the output than a single series switch does, especially at high frequencies. The result is excellent performance in the Video and RF region compared to conventional Analog Switches.

The input level shifting circuit is similar to that of the IH5140 Series of Analog Switches, giving very high speed and guaranteed "Break-before-Make" action, with negligible static power consumption and TTL compatibility.

NOTE: All typical values have been characterized but are not tested.



0295-16

Figure 10: Alternative Compensation Circuit

APPLICATIONS

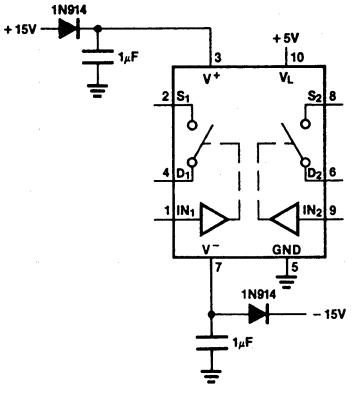
Charge Compensation Techniques

Charge injection results from the signals out of the level translation circuit being coupled through the gate-channel and gate-source/drain capacitances to the switch inputs and outputs. This feedthrough is particularly troublesome in Sample-and-Hold or Track-and-Hold applications, as it causes a Sample (Track) to Hold offset. The IH5341 devices have a typical injected charge of 30pC-50pC (corresponding to 30mV-50mV in a 1000pF capacitor), at $V_{S/D}$ of about 0V.

This Sample (Track) to Hold offset can be compensated by bringing in a signal equal in magnitude but of the opposite polarity. The circuit of Figure 9 accomplishes this charge injection compensation by using one side of the device as a S & H (T & H) switch, and the other side as a generator of a compensating signal. The 1kΩ potentiometer allows the user to adjust the net injected charge to exactly zero for any analog voltage in the −5V to +5V range.

Since individual parts are very consistent in their charge injection, it is possible to replace the potentiometer with a pair of fixed resistors, and achieve less than 5mV error for all devices without adjustment.

An alternative arrangement, using a standard TTL inverter to generate the required inversion, is shown in Figure 10. The capacitor needs to be increased, and becomes the only method of adjustment. A fixed value of 22pF is good for analog values referred to ground, while 35pF is optimum for AC coupled signals referred to −5V as shown in the figure. The choice of −5V is based on the virtual disappearance at this analog level of the transient component of switching charge injection. This combination will lead to a virtually "glitch-free" switch.



0295-17

Figure 11: Overvoltage Protection Circuit

Overvoltage Spike Protection

If sustained operation with no supplies but with analog signals applied is possible, it is recommended that diodes (such as 1N914) be inserted in series with the supply lines to the IH5341. Such conditions can occur if these signals come from a separate power supply or another location, for example. The diodes will be reverse biased under this type of operation, preventing heavy currents from flowing from the analog source through the IH5341.

The same method of protection will provide over ±25V overvoltage protection on the analog inputs when the supplies are present. The schematic for this connection is shown in Figure 11.

NOTE: All typical values have been characterized but are not tested.

IH5352
QUAD SPST CMOS RF/Video Switch

GENERAL DESCRIPTION

The IH5352 is a QUAD SPST, CMOS monolithic video switch which uses a "Series/Shunt" ("T" switch) configuration to obtain high "OFF" isolation while maintaining good frequency response in the "ON" condition.

Construction of remote and portable video equipment with extended battery life is facilitated by the extremely low current requirements. Switching speeds are typically t_{on} = 150ns and t_{off} = 80ns, and "Break-Before-Make" switching is guaranteed.

Switch "ON" resistance is typically 40Ω-50Ω with ±15V power supplies, increasing to typically 175Ω for ±5V supplies.

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH5352CPE	0°C to +70°C	16-Pin Plastic DIP
IH5352IJE	-25°C to +85°C	16-Pin CERDIP
IH5352MJE	-55°C to +125°C	16-Pin CERDIP
IH5352CBP	0°C to +70°C	20-Pin SOIC
IH5352IBP	-125°C to +85°C	20-Pin SOIC

FEATURES

- $R_{DS(on)}$ <75Ω
- Switch Attenuation Varies Less Than 3dB From DC to 100MHz
- "OFF" Isolation >70dB Typical @ 10MHz
- Cross Coupling Isolation >60dB @ 10MHz
- Directly Compatible with TTL, CMOS Logic
- Wide Operating Power Supply Range
- Power Supply Current <1μA
- "Break-Before-Make" Switching
- Fast Switching (80ns/150ns Typ)

APPLICATIONS

- Video Switch
- Communications Equipment
- Disk Drives
- Instrumentation
- CATV

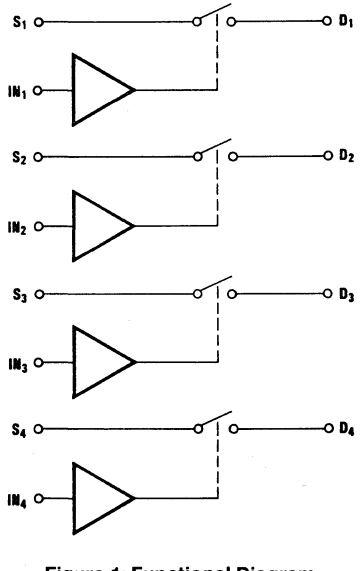


Figure 1: Functional Diagram (Switches are open for a logic "0" control input, and closed for a logic "1" control input.)

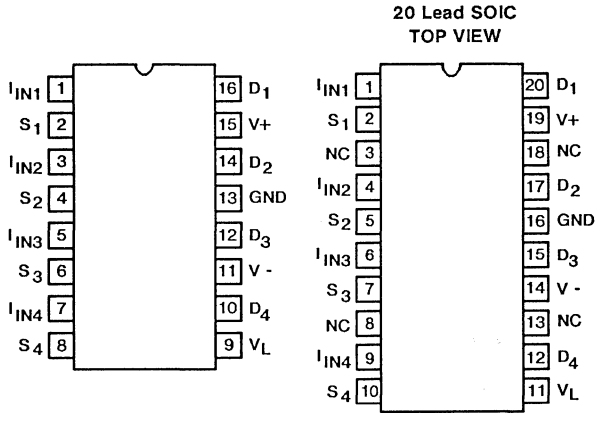


Figure 2: Pin Configurations
Package Outline Drawing: PE, JE

7

305529-004

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

V^+ to Ground ..... +18V
V^- to Ground ..... −18V
V_L to Ground ..... V^+ to V^-
Logic Control Voltage ..... V^+ to V^-
Analog Input Voltage ..... V^+ to V^-
Current (any terminal) ..... <50mA
Operating Temperature:
(M Version) ..... −55°C to +125°C
(I Version) ..... −20°C to +85°C
(C Version) ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature
(Soldering, 10sec) ..... 300°C
Power Dissipation:
CERDIP 450mW
derate 4mW/°C above 25°C
Plastic 350mW
derate 3mW/°C above 25°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC ELECTRICAL CHARACTERISTICS

$V^+ = +15V$, $V^- = -15V$, $V_L = +5V$, $T_A = 25°C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Typ @25°C	Maximum Ratings						Units
				M Grade Device			I/C Grade Device			
				−55°C	+25°C	+125°C	−25/0°C	+25°C	+85/ +70°C	
	Supply Voltage Ranges:									
V^+	Positive Supply	(Note 3)	5 to 15							V
V_L	Logic Supply	(Note 3)	5 to 15							V
V^-	Negative Supply	(Note 3)	−5 to −15							V
$R_{DS(on)}$	Switch "ON" Resistance (Note 4)	I_S = 10mA, V_D = ±5V	50	75	75	100	75	75	100	Ω
		$V_{IN} \geq 2.4V$, V_D = ±10V	100	125	125	175	150	150	175	Ω
$R_{DS(on)}$	Switch "ON" Resistance	I_S = 10mA, V^+ = V_L = +5V V^- = −5V, V_D = ±3V, V_{IN} = 3V	175	250	250	350	300	300	350	Ω
$\Delta R_{DS(on)}$	On Resistance Match Between Channels	I_S = 10mA, V_D = ±5V	5							Ω
V_{IH}	Logical "1" Input Voltage		>2.4							V
V_{IL}	Logical "0" Input Voltage		<0.8							V
$I_{D(off)}$ or $I_{S(off)}$	Switch 'OFF' Leakage (Note 2 and 4)	$V_{S/D}$ = ±5V $V_{S/D}$ = ±14V $V_{IN} \leq 0.8V$			±1.0 ±1.0	50 50		±2.0 ±2.0	100 100	nA
$I_{D(on)}$ + $I_{S(on)}$	Switch 'ON' Leakage	$V_{S/D}$ = ±5V $V_{S/D}$ = ±14V $V_{IN} \geq 2.4V$			±1.0 ±1.0	100 100		±2.0 ±2.0	100 100	nA
I_{IN}	Logic Control Input Current	$V_{IN} \geq 2.4V$ or <0V	0.1	±1	±1	10	±1	±1	10	µA
I^+	Positive Supply Quiescent Current	V_{IN} = 0V or +5V	0.1	1	1	10	1	1	10	µA
I^-	Negative Supply Quiescent Current	V_{IN} = 0V or +5V	0.1	1	1	10	1	1	10	µA
I_L	Logic Supply Quiescent Current	V_{IN} = 0V or +5V	0.1	1	1	10	1	1	10	µA

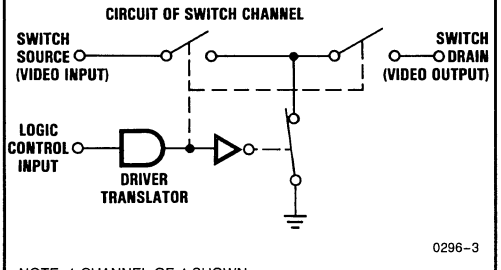
NOTE: All typical values have been characterized but are not tested.

AC ELECTRICAL CHARACTERISTICS

$V^+ = +15V$, $V_L = +15V$, $V^- = -15V$, $T_A = 25°C$ unless otherwise specified (Note 5).

Symbol	Parameter	Min	Typ	Max	Unit
t_{on}	Switch "ON" Time		150	300	ns
t_{off}	Switch "OFF" Time		80	150	
OIRR	"OFF" Isolation Rejection Ratio		70		dB
CCRR	Cross Coupling Rejection Ratio		60		
f_{3dB}	Switch Attenuation 3dB Frequency		100		MHz

Notes: **1.** Typical values are not tested in production. They are given as a design aid only.
2. Positive and negative voltages applied to opposite sides of switch, in both directions successively.
3. These are the operating voltages at which the other parameters are tested, and are not directly tested.
4. The logic inputs are either greater than or equal to 2.4V or less than or equal to 0.8V, as required, for this test.
5. All AC parameters are sample tested only.



NOTE: 1 CHANNEL OF 4 SHOWN

Figure 3: Internal Switch Configuration

DETAILED DESCRIPTION

Figure 3 shows the internal circuit of one channel of the IH5352. This is identical to the IH5341 "T-Switch" configuration. Here, a shunt switch is closed, and the two series switches are open when the video switch channel is open or off. This provides much better isolation between the input and output terminals than a simple series switch does, especially at high frequencies. The result is excellent off-isolation in the Video and RF frequency ranges when compared to conventional analog switches.

The control input level shifting circuitry is very similar to that of the IH5140 series of Analog Switches, and gives very high speed, guaranteed "Break-Before-Make" action, low static power consumption and TTL compatibility.

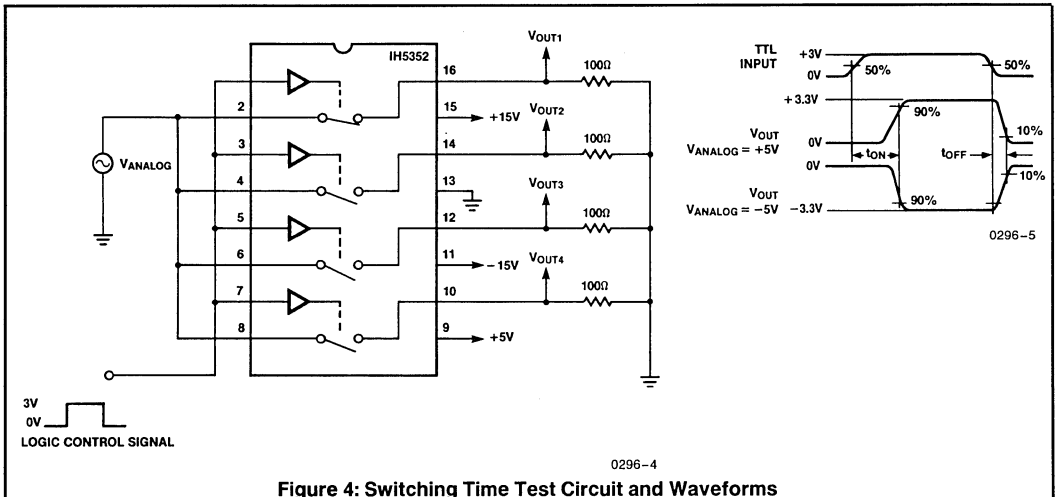
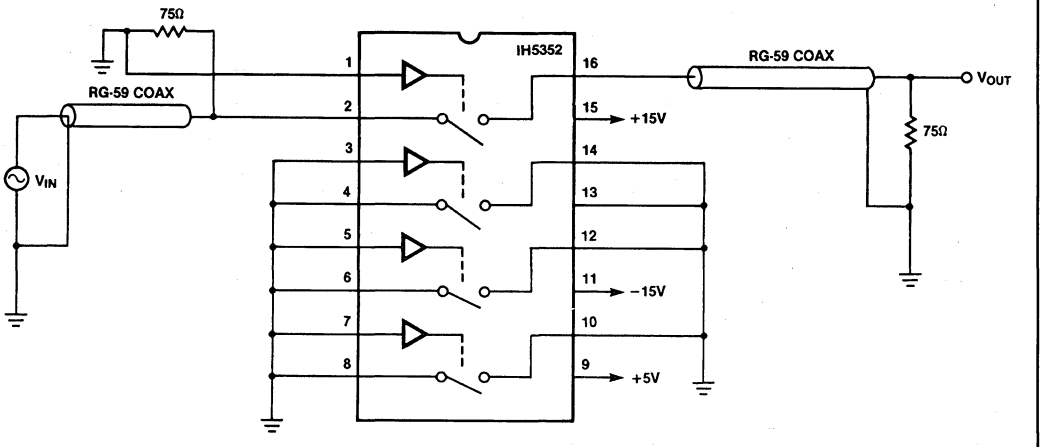


Figure 4: Switching Time Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

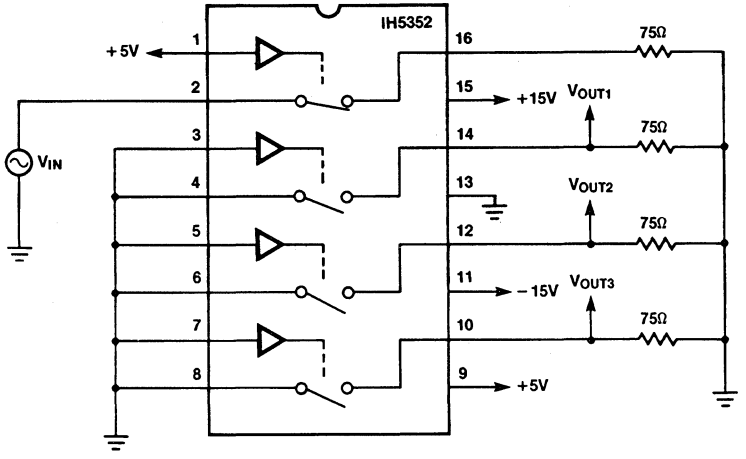


0296-6

$$OIRR = 20 \text{ LOG } \frac{V_{IN}}{V_{OUT}}$$

V_{IN} = 5V pn SINEWAVE @ 10MHz

Figure 5: Off Isolation Test Circuit



0296-7

$$CCRR = 20 \text{ LOG } \frac{V_{IN}}{V_{OUT}}$$

V_{IN} = 225mV RMS SINEWAVE @ 10MHz

Figure 6: Cross-Coupling Rejection Test Circuit

NOTE: All typical values have been characterized but are not tested.

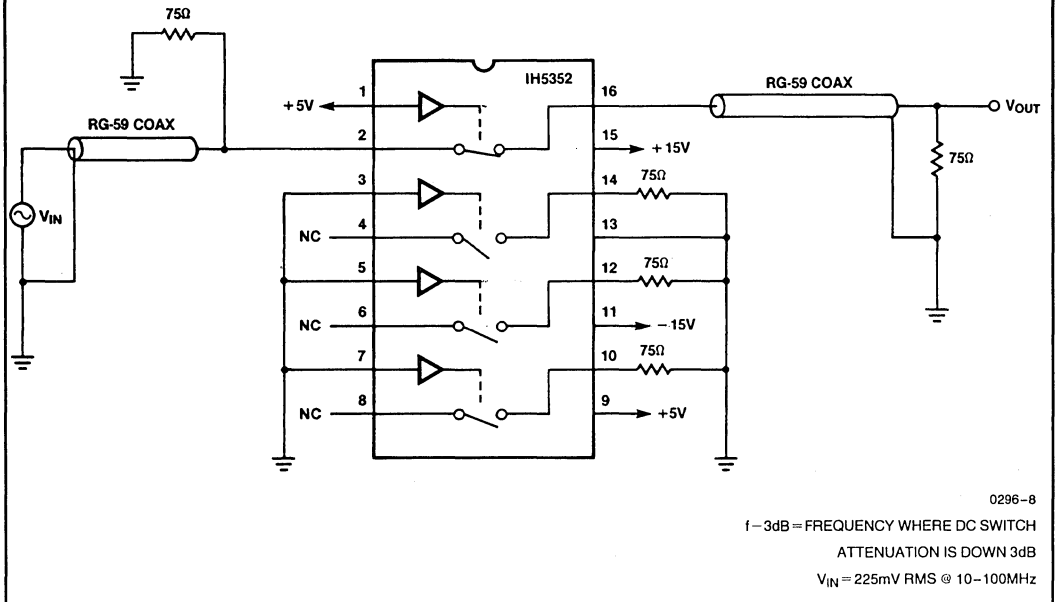


Figure 7: Switch Attenuation −3dB Frequency Test Circuit

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

IH6201
Dual CMOS Driver/Voltage Translator

GENERAL DESCRIPTION

The IH6201 is a CMOS, Monolithic, Dual Voltage Translator; it takes low level TTL or CMOS logic signals and converts them to higher levels (i.e. to ±15V swings). This translator is typically used in making solid state switches, or analog gates.

When used in conjunction with the IH401A Varafets, the combination makes a complete solid state switch capable of switching signals up to 22Vpp and up to 20MHz in frequency. This switch is a "break-before-make" type (i.e. t_{off} time< t_{on} time). The combination has typical $t_{off} \approx$ 80ns and typ. $t_{on} \approx$ 200ns for signals up to 20Vpp in amplitude.

A TTL "1" input strobe will force the θ driver output up to V^+ level; the $\overline{\theta}$ output will be driven down to the V^- level. When the TTL input goes to "0", the θ output goes to V^- and $\overline{\theta}$ goes to V^+; thus θ and $\overline{\theta}$ are 180° out of phase with each other. These complementary outputs can be used to create a wide variety of functions such as SPDT and DPDT switches, etc.; alternatively the complementary outputs can be used to drive N and P channel MOSFETs, to make a complete CMOS analog gate.

The driver typically uses +5V and ±15V power supplies, however a wide range of V^+ and V^- is also possible. It is necessary that $V^+ > 5V$ for the driver to work properly, however.

FEATURES

- **Driven Direct From TTL or CMOS Logic**
- **Translates Logic Levels Up to 30V Levels**
- **Switches $20V_{ACPP}$ Signals When Used in Conjunction With the IH401A Varafet (As An Analog Gate)**
- **$t_{ON} \leq 300ns$ & $t_{OFF} \leq 200ns$ for 30V Level Shifts**
- **Quiescent Supply Current ≤ 100μA for Any State (D.C.)**
- **Provides Both Normal & Inverted Outputs**

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH6201CJE	0°C to 70°C	16 Pin CERDIP
IH6201MJE	−55°C to 125°C	16 Pin CERDIP
IH6201CPE	0°C to 70°C	16 Pin Plastic

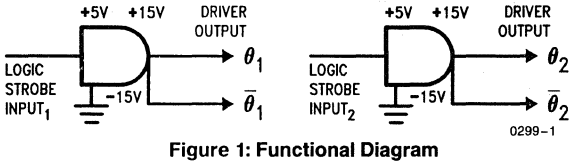
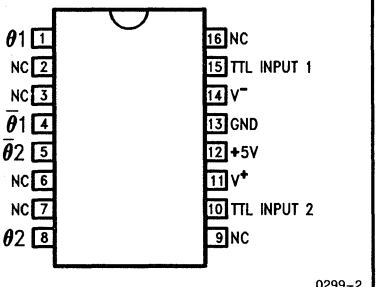


Figure 1: Functional Diagram



(Outline dwgs DE,JE,PE)

Figure 2: Pin Configuration

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- 35V
V^+ 35V
V^- 35V
V^+ to V_{IN} 40V
Operating Temperature ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL SPECIFICATIONS $V^+ = +15V, V^- = -15V, V_L = +5V$

Item	Test Conditions	IH6201CDE			IH6201MDE			Units
		−25°C	+25°C	+85°C	−55°C	+25°C	+125°C	
θ or $\overline{\theta}$ driver output swing	V_{IN} = 0V ⊓⊔ +3V Fig. 5B		28			28		V_{pp}
V_{IN} strobe level ("1")for proper translation	$\theta \geq 14V$ $\overline{\theta} \geq -14V$	3.0	3.0	3.0		2.4		$V_{D.C.}$
V_{IN} strobe level ("0")for proper translation	$\theta \geq -14V$ $\overline{\theta} \geq 14V$	0.4	0.4	0.4		0.8		$V_{D.C.}$
I_{IN} input strobe current draw (for 0V – 5V range)	V_{IN} = 0V or +5V	±1	±1	10	±1	±1	10	μA
t_{on} time	V_{IN} = 0V ⊓⊔ C_L = 30pF switching turn-on time fig. 5B		500			500		ns
t_{off} time	V_{IN} = 0V ⊓⊔ C_L = 30pF switching turn-off time fig. 5B		500			500		ns
I^+ (V^+) power supply quiescent current	V_{IN} = 0V or +5V	100	100	100	100	100	100	μA
I^- (V^-) power supply quiescent current	V_{IN} = 0V or +5V	100	100	100	100	100	100	μA
I_L (V_L) power supply quiescent current	V_{IN} = 0V or +5V	100	100	100	100	100	100	μA

7

NOTE: All typical values have been characterized but are not tested.

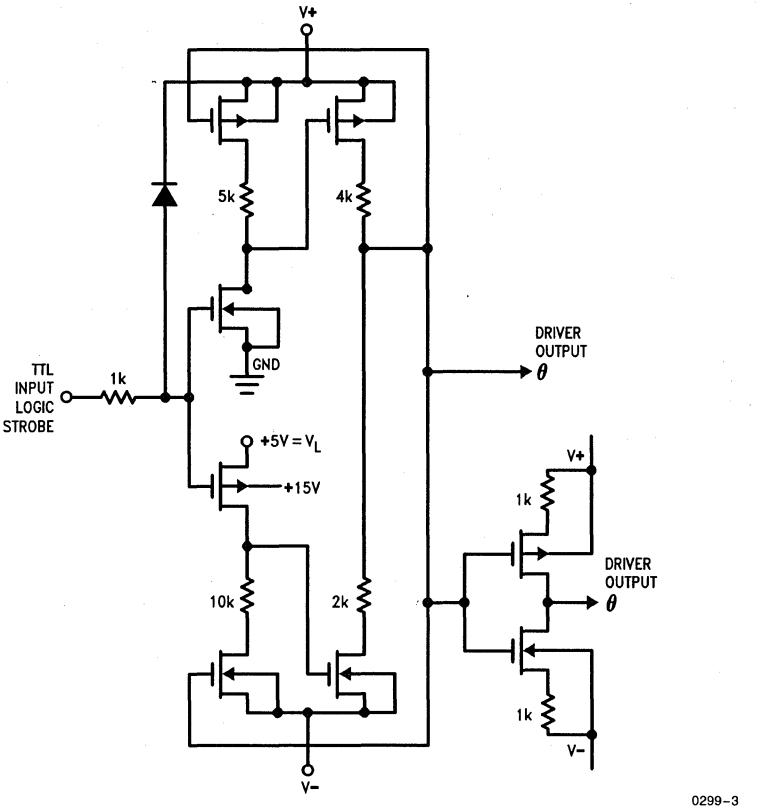


Figure 3: Schematic Diagram (One Channel)

APPLICATIONS

Input Drive Capability

The strobe input lines are designed to be driven from TTL logic levels; this means 0.8V to 2.4V levels max. and min. respectively. For those users who require 0.8V to 2.0V operation, a pull-up resistor is recommended from the TTL output to +5V line. This resistor is not critical and can be in the 1kΩ to 10kΩ range.

When using 4000 series CMOS logic, the input strobe is connected direct to the 4000 series gate output and no pull up resistors, or any other interface, is necessary.

When the input strobe voltage level goes below Gnd (i.e. to −15V) the circuit is unaffected as long as V^+ to V_{IN} does not exceed absolute maximum rating.

Output Drive Capability

The translator output is designed to drive the IH401A Varafets; these are N-channel JFETS with built-in driver diodes. Driver diodes are necessary to isolate the signal source from the driver/translator output; this prevents a forward bias condition between the signal input and the $+V_{CC}$ supply. The IH6201 will drive any JFET provided some sort of isolation is added.

NOTE: All typical values have been characterized but are not tested.

You will notice in Figure 4 that a "referral" resistor has been added from 2N4391 gate to its source. This resistor is needed to compensate for the inadequate charge area curve for isolation diode i.e. if C vs. V plot for diode ≤ 2 [C vs. V plot for output JFET] switch won't function; then adding this resistor overcomes this condition. The "referral" resistor is normally in the 100kΩ to 1MΩ range and is not too critical.

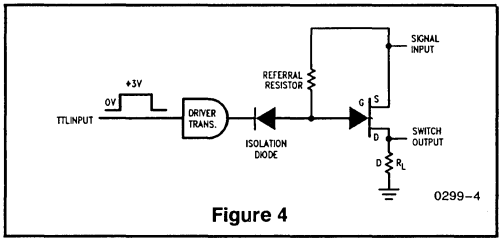


Figure 4

Making a Complete Solid State Switch That Can Handle 20Vpp Signals

The limitation on signal handling capability comes from the output gating device. When a JFET is used, the pinch-off of the JFET acting with the V^- supply does the limiting. In fact max. signal handling capability = 2 (Vp + (V^-)) Vpp where Vp = pinch-off voltage of JFET chosen. i.e. Vp = 7V, $V^- = -15V$ ∴ max. signal handling = 2 (7V + (−15V)) Vpp = 2(7V − 15)Vpp = 2(−8Vpp) = 16Vpp. Obviously to get ≥ 20Vpp, Vp ≥ 5V with $V^- = -15V$. Another simple way to get 20Vpp with Vp = 7V, is to increase V^- to −17V. In fact using $V^+ = +12V$ or +15V and setting $V^- = -18V$ allows one to switch 20Vpp with the IH401A. The advantage of using the Vp = 7V pinch-off (along with unsymmetrical supplies), over the Vp = 5V pinch-off (and ±15V supplies), is that you will have a much lower $R_{DS(ON)}$ for the Vp = 7 JFET (i.e. for the 2N4391).

$r_{DS(ON)} \approx 22\Omega$, $V_p = 7V$ $\quad$ $r_{DS(ON)} \approx 35\Omega$, $V_p = 5V$

The IH6201 is a dual translator, each containing 4 CMOS FET pairs. The schematic of one-half of an IH6201, driving one-quarter of an IH401A, is shown in Figure 5A.

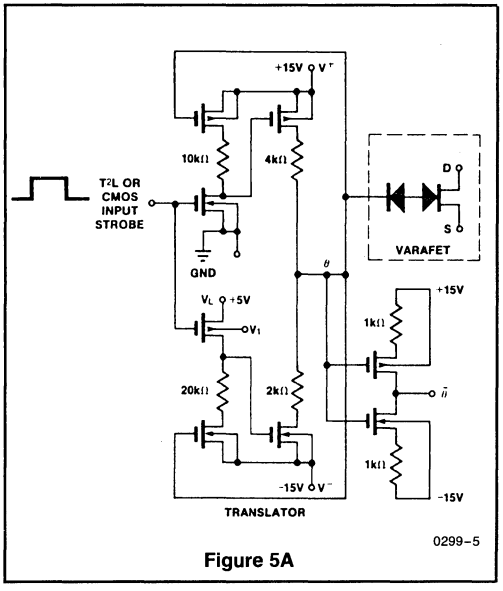


Figure 5A

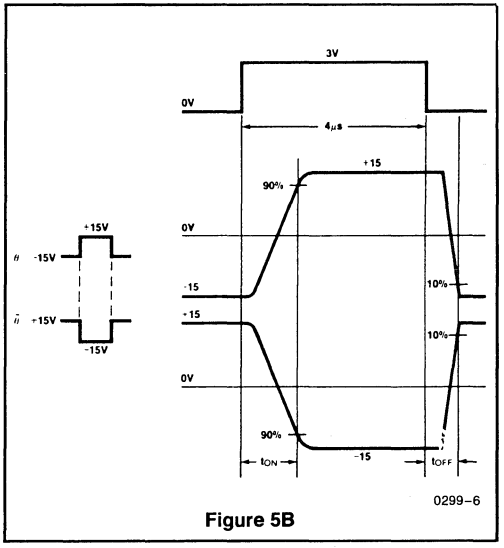


Figure 5B

NOTE: Each translator output has a θ and $\bar{\theta}$ output. θ is just the inverse of $\bar{\theta}$.

A very useful feature of this system is that one-half of an IH6201 and one-half of an IH401A can combine to make a SPDT switch, or an IH6201 plus an IH401A can make a dual SPDT analog switch (See Figure 8).

NOTE: All typical values have been characterized but are not tested.

APPLICATIONS (Continued)

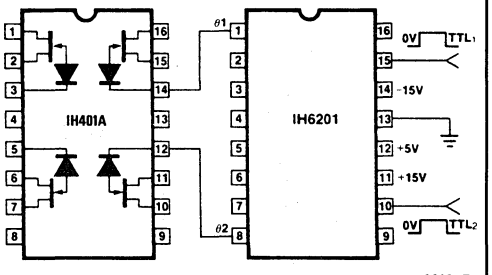


Figure 6: Dual SPST Analog Switch

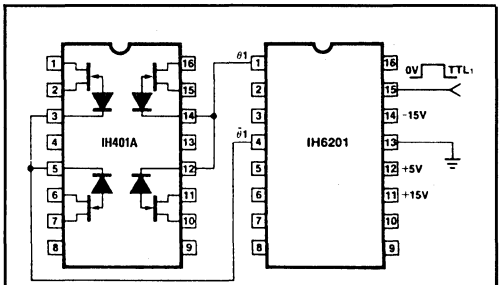


Figure 7: DPDT Analog Switch

NOTE: Either switch is turned on when strobe input goes high.

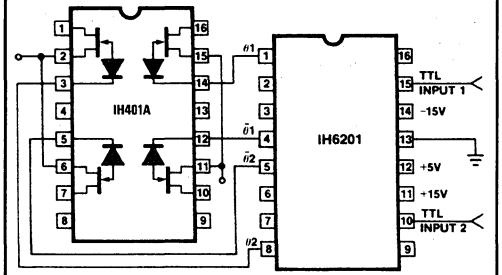


Figure 8: Dual SPDT

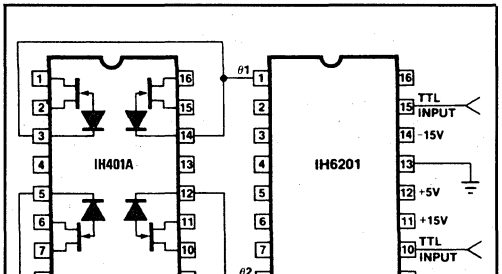


Figure 9: Dual DPST

NOTE: All typical values have been characterized but are not tested.

DATA ACQUISITION 8

MULTIPLEXERS

ANALOG MULTIPLEXERS SELECTION GUIDE

GENERAL PURPOSE DEVICE NUMBER (S)	CONFIGURATION	Rds (ON)–OHMS
DG508A, HI508, IH6108	8-CHANNEL SINGLE ENDED	450
DG506A, HI506	16-CHANNEL SINGLE ENDED	450
DG509A, HI509, IH6208	4-CHANNEL DIFFERENTIAL	450
DG507A, HI507	8-CHANNEL DIFFERENTIAL	450
FAULT PROTECTED DEVICE NUMBER (S)	**CONFIGURATION**	**Rds (ON)–OHMS**
HI-508A, IH5108	8-CHANNEL SINGLE ENDED	1800
HI-506A, IH5116	16-CHANNEL SINGLE ENDED	1800
HI-509A, IH5208	4-CHANNEL DIFFERENTIAL	1800
HI-507A, IH5216	8-CHANNEL DIFFERENTIAL	1800
µPROCESSOR COMPATIBLE DEVICE NUMBER(S)	**CONFIGURATION**	**Rds (ON)– OHMS**
DG526	16-CHANNEL SINGLE ENDED	400
DG527	8-CHANNEL DIFFERENTIAL	400
DG528	8-CHANNEL SINGLE ENDED	450
DG529	4-CHANNEL DIFFERENTIAL	450
MODE PROGRAMMABLE DEVICE NUMBER (S)	**PROGRAMMABLE CONFIGURATION**	**Rds (ON)–OHMS**
HI-516	16-CHANNEL/DUAL 8-CHANNEL	750
HI-518	8-CHANNEL/DUAL 4-CHANNEL	750
SPECIAL PURPOSE DEVICE NUMBER	**CONFIGURATION**	**Rds (ON)–OHMS**
HI-524	4-CHANNEL VIDEO, LOW CROSSTALK	1500*
HI-539	DIFF., 4-CHANNEL, LOW LVL MATCHED	900

NOTE: MOST Rds (ON) VALUES ARE MAXIMUM AT 25°C.
*THIS IS THE MAXIMUM VALUE OVER THE ENTIRE 0° TO 70°C TEMP RANGE

HARRIS SEMICONDUCTOR

DG506A/DG507A
16-Channel/Dual 8-Channel CMOS Analog Multiplexer

GENERAL DESCRIPTION

The DG506A/DG507A are CMOS monolithic 16-channel and dual 8-channel analog multiplexers, which can also be used as demultiplexers. The DG506A uses 4 address inputs to control its 16 channels, and the DG507A uses 3 address inputs to control its dual 8 channels. An enable input is provided. When the enable input is high, a channel is selected by the address inputs, and when low, all channels are off.

A channel in the ON state conducts current equally well in both directions. In the OFF state each channel blocks voltages up to the supply rails. The address inputs and the enable input are TTL and CMOS compatible over the full specified operating temperature range. Both DG506A and DG507A are available in the military, industrial, and commercial temperature ranges.

The DG506A/507A are pin-out compatible with the industry standard devices.

FEATURES

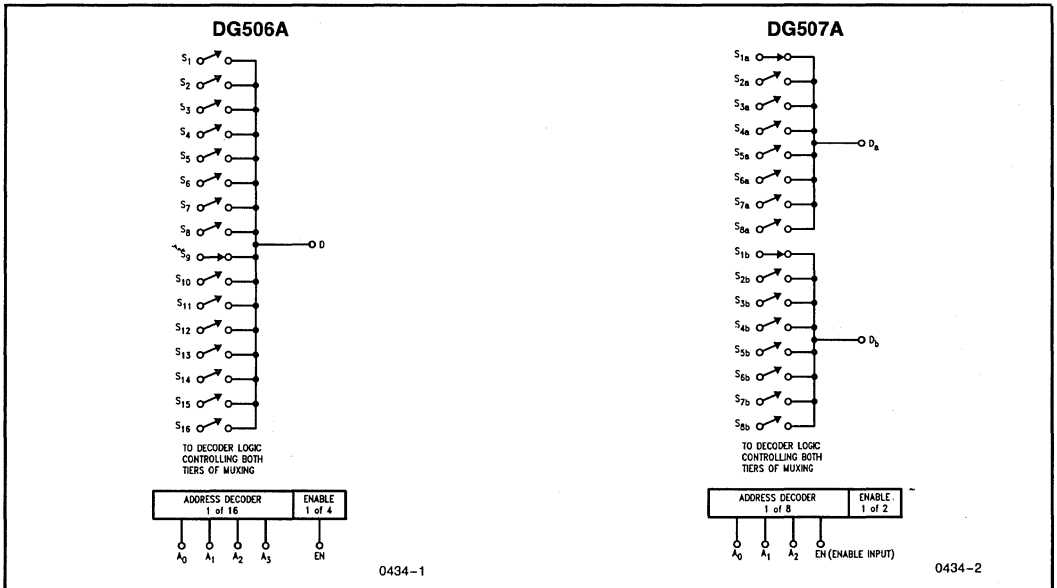
- **Low Power Consumption**
- **TTL and CMOS Compatible Address and Enable Inputs**
- **44V maximum Power Supply Rating**
- **HIGH Latch-Up Immunity**
- **Break-Before-Make Switching**
- **Alternate Source**

APPLICATIONS

- **Data Acquisition Systems**
- **Communication Systems**
- **Signal Multiplexing/Demultiplexing**
- **Audio Signal Multiplexing**

ORDERING INFORMATION

Part Number	Temperature Range	Package
DG506AAK/507AAK	−55°C to +125°C	28-Pin CERDIP
DG506ABK/507ABK	−25°C to +85°C	28-Pin CERDIP
DG506ACK/507ACK	0°C to +70°C	28-Pin CERDIP
DG506ACJ/507ACJ	0°C to +70°C	28-Pin Plastic DIP



4 Line Binary Address Inputs
(0 0 0 1) and EN @ 5V
Above Example Shows Channel 9 Turned ON.

3 Line Binary Address Inputs
(0 0 0) and EN = 5V
Above Example Shows Channels 1a & 1b ON.

Figure 1: Functional Diagrams

307050-002

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- 44V
V^- to Ground ..... −25V
V_{IN} to Ground (Note 1) ..... (V^- − 2V), (V^+ + 2V)
V_S or V_D to V^+ (Note 1) ..... +2, (V^- − 2V)
V_S or V_D to V^- (Note 1) ..... −2, (V^+ + 2V)
Current, Any Terminal except S or D ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA
Operating Temperature
C Suffix ..... 0°C to +70°C
B Suffix ..... −25°C to +85°C
A Suffix ..... −55°C to +125°C
Storage Temperature
C Suffix ..... −65°C to +125°C
A & B Suffix ..... −65°C to +150°C
Lead Temperature (Soldering, 10 Sec.) ..... 300°C
Power Dissipation*
28-Pin CERDIP Package** ..... 1200 mW
28-Pin Plastic Package*** ..... 625 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 16 mW/°C above 75°C
***Derate 8.3 mV/°C above 75°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS (Note 3)

$V^+ = -15V$, $V^- = -15V$, $V_{EN} = 2.4V$, GND = 0V, $T_A = 25°C$, unless otherwise specified.

Symbol	Parameter		Test Conditions		DG506AA, DG507AA			DG506AB/C, DG507AB/C			Units
					Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
SWITCH											
V_{ANALOG}	Analog Signal Range		(Note 6)		−15		15	−15		15	V
$R_{DS(ON)}$	Drain-Source ON Resistance		Sequence Each Switch On $V_{AL} = 0.8V$ and $V_{AH} = 2.4V$	$I_S = -200\ \mu A$, $V_D = +10V$		270	400		270	450	Ω
				$I_S = -200\ \mu A$, $V_D = -10V$		230	400		230	450	
$\Delta R_{DS(ON)}$	Greatest Change in Drain Source ON Resistance between Channels		$-10V \le V_S \le +10V$ $\Delta R_{DS(on)} = \frac{R_{DS(on)max} - R_{DS(on)min}}{R_{DS(on)avg.}}$			6			6		%
$I_{S(OFF)}$	Source OFF Leakage Current		$V_{EN} = 0V$	$V_S = +10V$, $V_D = -10V$	−1	0.002	1	−5	0.002	5	nA
				$V_S = -10V$, $V_D = +10V$	−1	−0.005	1	−5	−0.005	5	
$I_{D(OFF)}$	Drain OFF Leakage Current	DG506A	$V_{EN} = 0V$	$V_S = -10V$, $V_D = +10V$	−10	0.02	10	−20	0.02	20	nA
				$V_S = +10V$, $V_D = -10V$	−10	−0.03	10	−20	−0.03	20	
		DG507A		$V_S = -10V$, $V_D = +10V$	−5	0.007	5	−10	0.007	10	
				$V_S = +10V$, $V_D = -10V$	−5	−0.015	5	−10	−0.015	10	
$I_{D(ON)}$ (Note 5)	Drain ON Leakage Current	DG506A	Sequence Each Switch On $V_{AL} = 0.8V$ and $V_{AH} = 2.4V$	$V_D = V_{S(ALL)} = +10V$	−10	0.03	10	−20	0.03	20	nA
				$V_D = V_{S(ALL)} = -10V$	−10	−0.06	10	−20	−0.06	20	
		DG507A		$V_D = V_{S(ALL)} = +10V$	−5	0.015	5	−10	0.015	10	
				$V_D = V_{S(ALL)} = -10V$	−5	−0.03	5	−10	−0.03	10	

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued)

$V^+ = 15V$, $V^- = -15V$, GND = 0V, $V_{EN} = 2.4V$, $T_A = 25°C$, unless otherwise specified.

Symbol	Parameter		Test Conditions		DG506AA, DG507AA			DG506AB/C, DG507AB/C			Units
					Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
INPUT											
I_{AH}	Address Input Current, Input Voltage High		$V_A = 2.4V$		−10	−0.002		−10	−0.002		µA
			$V_A = 15V$			0.006	10		0.006	10	
I_{AL}	Address Input Current Input Voltage Low		$V_{EN} = 2.4V$	All $V_A = 0V$	−10	−0.002		−10	−0.002		µA
			$V_{EN} = 0V$		−10	−0.002		−10	−0.002		
DYNAMIC											
$t_{transition}$	Switching Time of Multiplexer		See Figure 3			0.6	1		0.6		µs
t_{open}	Break-Before-Make Interval		See Figure 5			0.2			0.2		µs
$t_{ON(EN)}$	Enable Turn-ON Time		See Figure 4			1	1.5		1		µs
$t_{OFF(EN)}$	Enable Turn-OFF Time					0.4	1.0		0.4		µs
OIRR (Note 4)	OFF Isolation		$V_{EN} = 0V$, $R_L = 1 k\Omega$, $C_L = 15 pF$, $V_S = 7 V_{RMS}$, f = 500 kHz			68			68		dB
$C_{S(OFF)}$	Source OFF Capacitance		$V_S = 0V$	$V_{EN} = 0V$, f = 140 kHz		6			6		pF
$C_{D(OFF)}$	Drain OFF Capacitance	DG506A	$V_D = 0V$			45			45		
		DG507A				23			23		
Q	Charge Injection		See Figure 8			6			6		pC
SUPPLY											
I^+	Positive Supply Current		$V_{EN} = 5.0V$	All $V_A = 0V$		1.3	2.4		1.3	2.4	mA
I^-	Negative Supply Current				−1.5	−0.7		−1.5	−0.7		
I^+ Standby	Positive Supply Current		$V_{EN} = 0V$			1.3	2.4		1.3	2.4	
I^- Standby	Negative Supply Current				−1.5	−0.7		−1.5	−0.7		

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued)

T_A = over Operating Temperature Range, $V^+ = 15V$, $V^- = -15V$, GND = 0V, $V_{EN} = 2.4V$, unless otherwise specified.

Symbol	Parameter		Test Conditions		DG506AA, DG507AA			DG506AB/C, DG507AB/C			Units
					Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
SWITCH											
V_{ANALOG}	Analog Signal Range		(Note 6)		−15		15	−15		15	V
$R_{DS(ON)}$	Drain-Source ON Resistance		Sequence Each Switch On $V_{AL} = 0.8V$ $V_{AH} = 2.4V$	$I_S = -200\ \mu A$, $V_D = 10V$			500			550	Ω
				$I_S = -200\ \mu A$, $V_D = -10V$			500			550	
$I_{S(OFF)}$	Source OFF Leakage Current		$V_{EN} = 0V$	$V_S = +10V$, $V_D = -10V$			50			50	nA
				$V_S = -10V$, $V_D = +10V$	−50			−50			
$I_{D(OFF)}$	Drain OFF Leakage Current	DG506A	$V_{EN} = 0V$	$V_S = -10V$, $V_D = +10V$			300			300	nA
				$V_S = +10V$, $V_D = -10V$	−300			−300			
		DG507A		$V_S = -10V$, $V_D = +10V$			200			200	
				$V_S = +10V$, $V_D = -10$	−200			−200			
$I_{D(ON)}$ (Note 5)	Drain ON Leakage Current	DG506A	Sequence Each Switch On $V_{AL} = 0.8V$ and $V_{AH} = 2.4V$	$V_D = V_{S(ALL)} = +10V$			300			300	nA
				$V_D = V_{S(ALL)} = -10V$	−300			−300			
		DG507A		$V_D = V_{S(ALL)} = +10V$			200			200	
				$V_D = V_{S(ALL)} = -10V$	−200			−200			
INPUT											
I_{AH}	Address Input Current, Input Voltage High		$V_A = 2.4V$		−30			−30			μA
			$V_A = 15V$				30			30	
I_{AL}	Address Input Current, Input Voltage Low		$V_{EN} = 2.4V$	All $V_A = 0V$	−30			−30			μA
			$V_{EN} = 0V$		−30			−30			
SUPPLY											
I^+	Positive Supply Current		$V_{EN} = 5.0V$	All $V_A = 0V$			2.4			2.4	mA
I^-	Negative Supply Current				−1.5			−1.5			
I^+ Standby	Positive Supply Current		$V_{EN} = 0V$				2.4			2.4	
I^- Standby	Negative Supply Current				−1.5			−1.5			

NOTES 1: Signals on V_S, V_D or V_{IN} exceeding V^+ or V^- will be clamped by internal diodes. Limit diode forward current to maximum current ratings.

2: Typical values are for design aid only, not guaranteed and not subject to production testing.

3: The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

4: OFF isolation = 20 log $|V_S|/|V_D|$, where V_S = input to OFF switch, and V_D = output due to V_S.

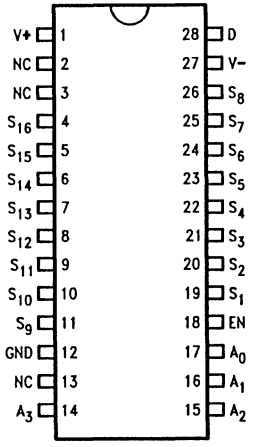
5: $I_{D(ON)}$ is leakage from driver into "ON" switch.

6: Parameter not tested. Parameter guaranteed by design or characterization.

NOTE: All typical values have been characterized but are not tested.

DG506A/DG507A

DG506A
28 Lead DIP
28 Lead SOIC
Top View



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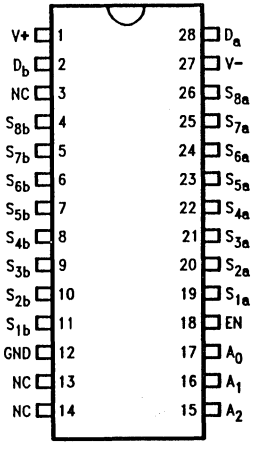
DG507A
28 Lead DIP
28 Lead SOIC
Top View



0434-4

Figure 2: Pin Configurations

TRUTH TABLES

DG506A

A_3	A_2	A_1	A_0	EN	ON Switch
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

DG507A

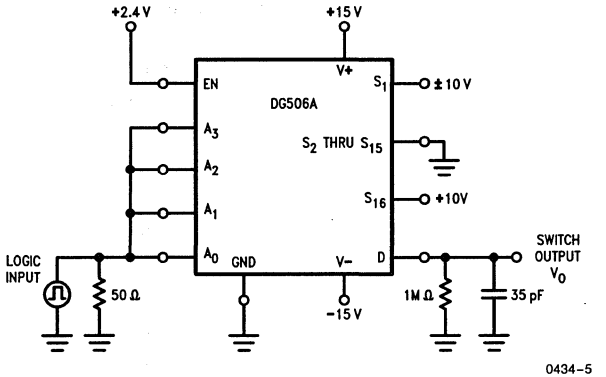
A_2	A_1	A_0	EN	ON Switch
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

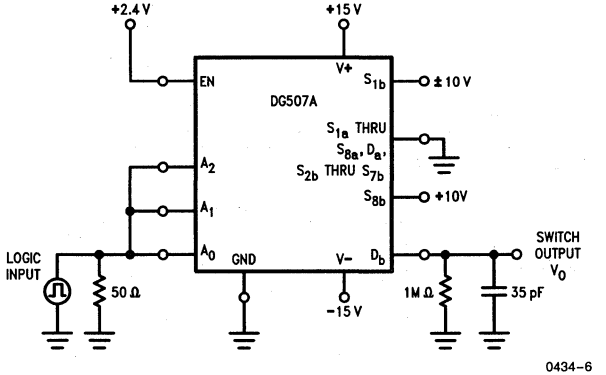
Logic "0" = V_{AL}, $V_{ENL} \leq 0.8V$, Logic "1" = V_{AH}, $V_{ENH} \geq 2.4V$.

8

NOTE: All typical values have been characterized but are not tested.

SWITCHING INFORMATION





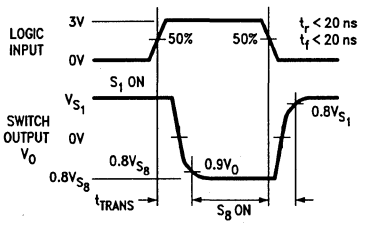
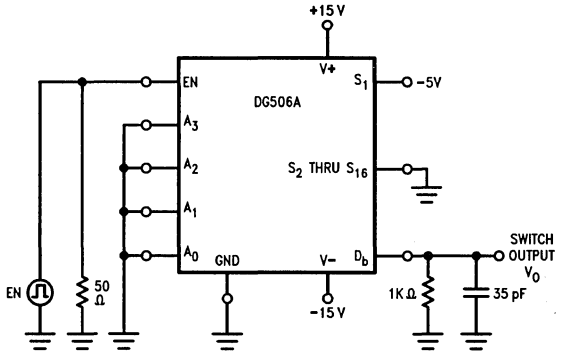
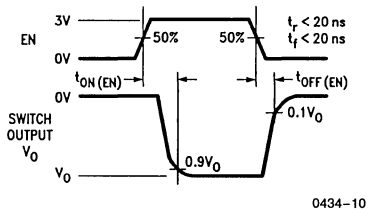


Figure 4: $t_{transition}$ Switching Time Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

SWITCHING INFORMATION (Continued)





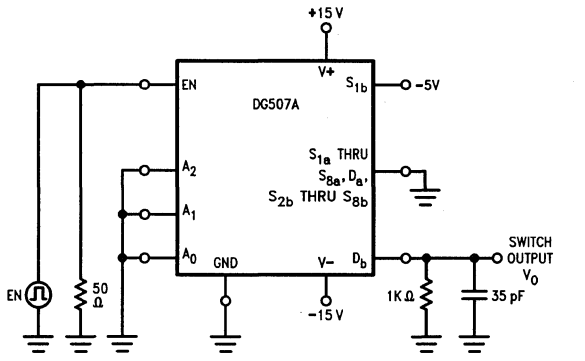


Figure 5: Enable t_{on} and t_{off} Switching Time Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

SWITCHING INFORMATION (Continued)

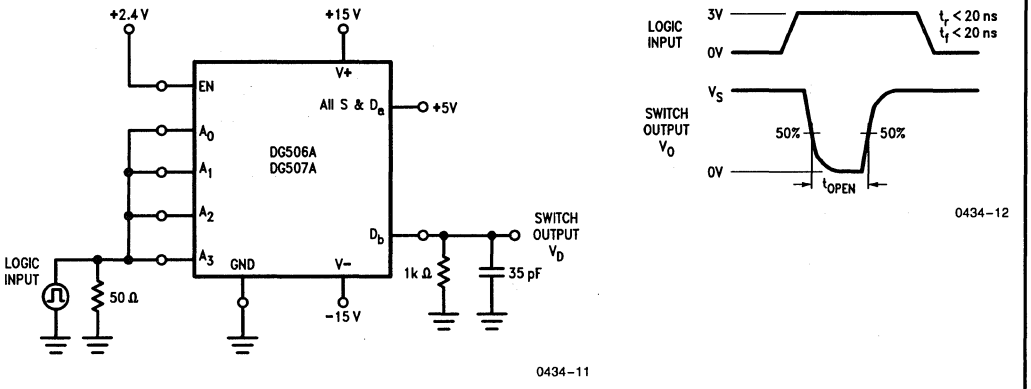


Figure 6: t_{open} (Break-Before-Make) Switching Time Test Circuit and Waveforms

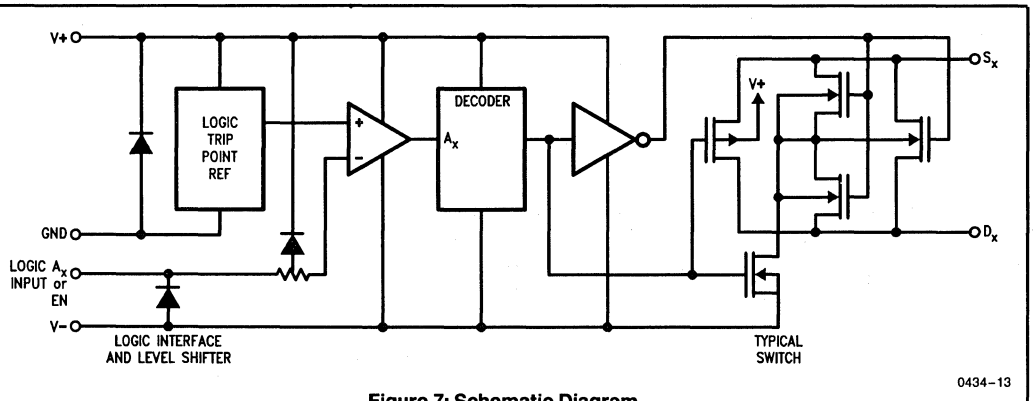
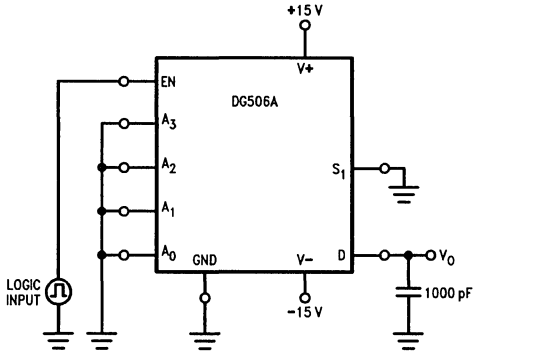


Figure 7: Schematic Diagram

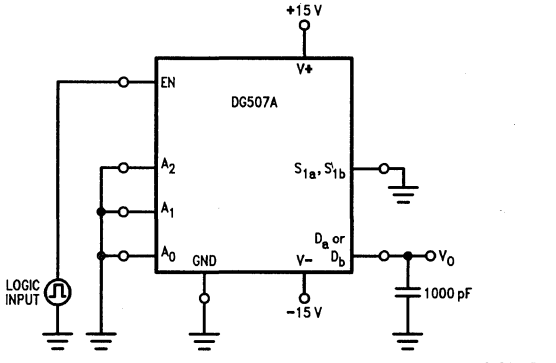
LOGIC INPUTS

The address and enable inputs are fully TTL/CMOS compatible over the full supply range of ±5V to ±20V. These inputs are protected from positive and negative transients by clamping diodes.

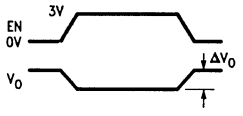
NOTE: All typical values have been characterized but are not tested.



0434-14



0434-15



0434-16

ΔV_O is the measured voltage error due to charge injection. The error voltage in Coulombs is $Q = C_L \times \Delta V_O$.

Figure 8: Charge Injection Test Circuit and Waveforms

8

NOTE: All typical values have been characterized but are not tested.

DG506A/DG507A

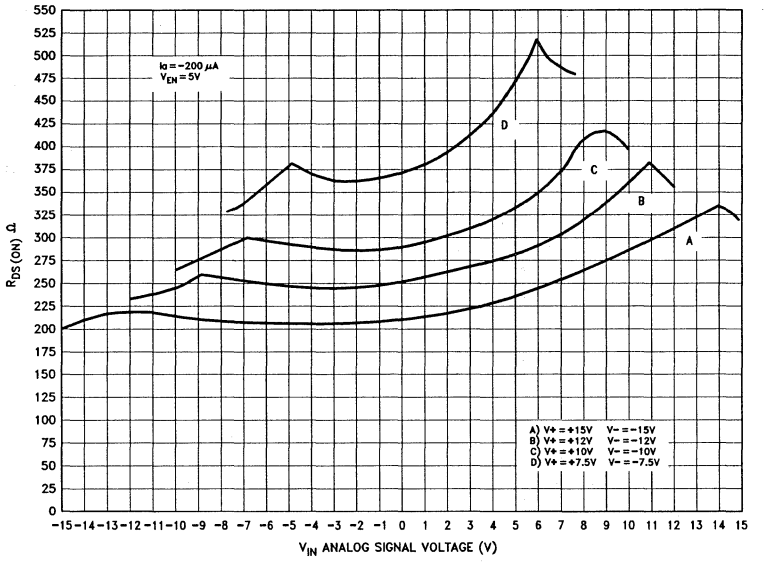


Figure 9: $R_{DS(on)}$ vs Analog Signal Voltage vs Supply Voltage

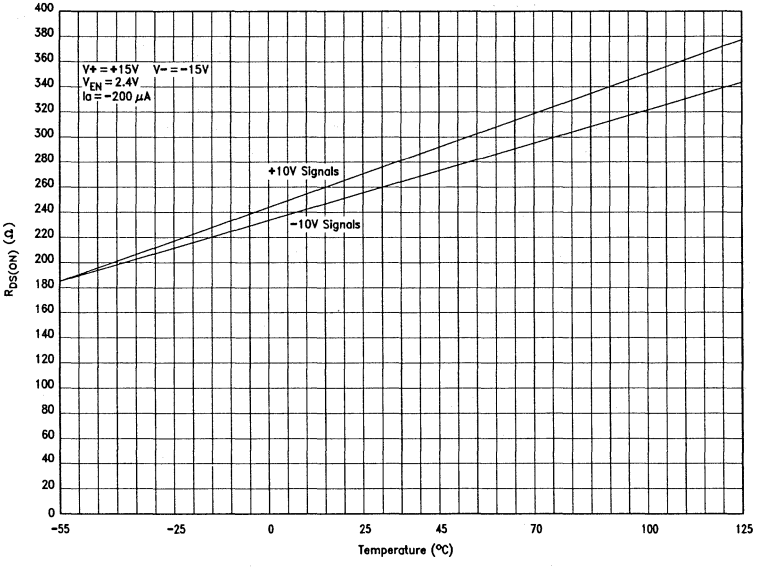


Figure 10: Typical $R_{DS(on)}$ Variation with Temperature

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

DG508A/DG509A
8-Channel/Dual 4-Channel CMOS Analog Multiplexer

GENERAL DESCRIPTION

The DG508A/DG509A are CMOS monolithic 8-channel and dual 4-channel analog multiplexers, which can also be used as demultiplexers. The DG508A uses 3 address inputs to control its 8 channels, and the DG509A uses 2 address inputs to control its dual 4 channels. An enable input is provided. When the enable input is high, a channel is selected by the address inputs, and when low, all channels are off.

A channel in the ON state conducts current equally well in both directions. In the OFF state each channel blocks voltage up to the supply rails. The address inputs and the enable input are TTL and CMOS compatible over the full specified operating temperature range. Both DG508A and DG509A are available in the military, industrial, and commercial temperature ranges.

FEATURES

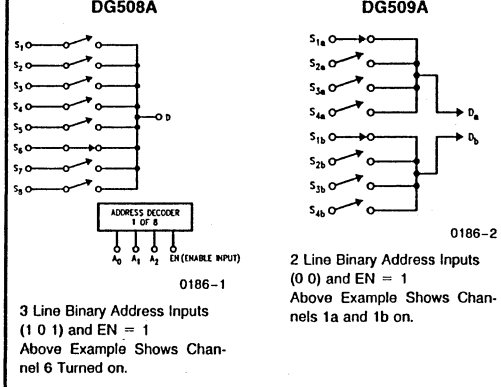
- Low Power Consumption
- TTL and CMOS Compatible Address and Enable Inputs
- 44V Maximum Power Supply Rating
- High Latchup Immunity
- Break-Before-Make Switching
- Alternate Source

APPLICATIONS

- Data Acquisition Systems
- Communication Systems
- Signal Multiplexing/Demultiplexing
- Audio Signal Multiplexing

ORDERING INFORMATION

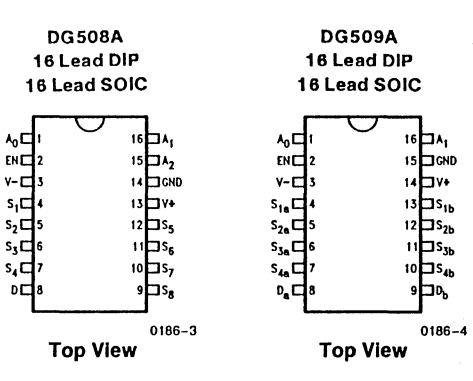
Part Number	Temp. Range	Package
DG508AAK/509AAK	-55°C to +125°C	16-Pin CERDIP
DG508ABK/509ABK	-25°C to +85°C	16-Pin CERDIP
DG508ACK/509ACK	0°C to +70°C	16-Pin CERDIP
DG508ACJ/509ACJ	0°C to +70°C	16-Pin Plastic DIP
DG508ACY/509ACY	0°C to +70°C	16-Pin SOIC



3 Line Binary Address Inputs (1 0 1) and EN = 1
Above Example Shows Channel 6 Turned on.

2 Line Binary Address Inputs (0 0) and EN = 1
Above Example Shows Channels 1a and 1b on.

Figure 1: Functional Diagrams



Top View — Top View

Figure 2: Pin Configurations

8

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- 44V
V^- to Ground ..... −25V
V_{IN} to Ground (Note 1) ..... (V^- − 2V), (V^+ + 2V)
V_S or V_D to V^+ (Note 1) ..... +2, (V^- − 2V)
V_S or V_D to V^- (Note 1) ..... −2, (V^+ + 2V)
Current, Any Terminal except S or D ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) ..... 40 mA
Operating Temperature
C Suffix ..... 0°C to +70°C
B Suffix ..... −25°C to +85°C
A Suffix ..... −55°C to +125°C
Storage Temperature
C Suffix ..... −65°C to +125°C
A & B Suffix ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Power Dissipation*
CERDIP Package** ..... 900 mW
Plastic Package*** ..... 470 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 12 mW/°C above 75°C

***Derate 6.3 mW/°C above 75°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS (Note 3)

V^+ = 15V, V^- = −15V, V_{EN} = 2.4V, GND = 0V, T_A = 25°C, unless otherwise specified.

Symbol	Parameter		Test Conditions		DG508AA, DG509AA			DG508AB/C, DG509AB/C			Units
					Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
SWITCH											
V_{ANALOG}	Analog Signal Range		(Note 6)		−15		15	−15		15	V
$R_{DS(on)}$	Drain-Source ON Resistance		Sequence Each Switch On V_{AL} = 0.8V and V_{AH} = 2.4V	I_S = −200 μA, V_D = +10V		270	400		270	450	Ω
				I_S = −200 μA, V_D = −10V		230	400		230	450	
$\Delta R_{DS(on)}$	Greatest Change in Drain Source ON Resistance between Channels		$-10V \le V_S \le 10V$ $\Delta R_{DS(ON)} = \frac{R_{DS(on)max} - R_{DS(on)min}}{R_{DS(on)avg}}$			6			6		%
$I_{S(off)}$	Source OFF Leakage Current		V_{EN} = 0V	V_S = 10V, V_D = −10V		0.002	1		0.002	5	nA
				V_S = −10V, V_D = 10V	−1	−0.005		−5	−0.005		
$I_{D(off)}$	Drain OFF Leakage Current	DG508A	V_{EN} = 0V	V_S = −10V, V_D = 10V		0.01	10		0.01	20	nA
				V_S = 10V, V_D = −10V	−10	−0.015		−20	−0.015		
		DG509A		V_S = −10V, V_D = 10V		0.005	10		0.005	20	
				V_S = 10V, V_D = −10V	−10	−0.008		−20	−0.008		
$I_{D(on)}$ (Note 5)	Drain ON Leakage Current	DG508A	Sequence Each Switch On V_{AL} = 0.8V and V_{AH} = 2.4V	$V_D = V_{S(all)}$ = 10V		0.015	10		0.015	20	nA
				$V_D = V_{S(all)}$ = −10V	−10	−0.03		−20	−0.03		
		DG509A		$V_D = V_{S(all)}$ = 10V		0.007	10		0.007	20	
				$V_D = V_{S(all)}$ = −10V	−10	−0.015		−20	−0.015		
INPUT											
I_{AH}	Address Input Current, Input Voltage High		V_A = 2.4V		−10	−0.002		−10	−0.002		μA
			V_A = 15V			0.006	10		0.006	10	μA
I_{AL}	Address Input Current, Input Voltage Low		V_{EN} = 2.4V	All V_A = 0V	−10	−0.002		−10	−0.002		μA
			V_{EN} = 0V		−10	−0.002		−10	−0.002		μA

NOTE: All typical values have been characterized but are not tested.

DG508A/509A

ELECTRICAL CHARACTERISTICS (Continued)

$V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, GND = 0V, $T_A = 25°C$, unless otherwise specified.

Symbol	Parameter		Test Conditions		DG508AA, DG509AA			DG508AB/C, DG509AB/C			Units
					Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
DYNAMIC											
$t_{transition}$	Switching Time of Multiplexer		See Figure 4			0.6	1		0.6		µs
t_{open}	Break-Before-Make Interval		See Figure 5			0.2			0.2		µs
$t_{on(EN)}$	Enable Turn-ON Time		See Figure 6			1	1.5		1		µs
$t_{off(EN)}$	Enable Turn-OFF Time					0.4	1		0.4		µs
OIRR (Note 4)	OFF Isolation		V_{EN} = 0V, R_L = 1 kΩ, C_L = 15 pF V_S = 7 VRMS, f = 500 kHz			68			68		dB
$C_{S(off)}$	Source OFF Capacitance		V_S = 0V	V_{EN} = 0V, f = 140 kHz		5			5		pF
$C_{D(off)}$	Drain OFF Capacitance	DG508A	V_D = 0V			25			25		
		DG509A				12			12		
Q	Charge Injection		See Figure 7			4			4		pC
SUPPLY											
I^+	Positive Supply Current		V_{EN} = 2.4V	All V_A = 0V or 2.4V		1.3	2.4		1.3	2.4	mA
I^-	Negative Supply Current				−1.5	−0.7		−1.5	−0.7		
I^+ Standby	Positive Supply Current		V_{EN} = 0V			1.3	2.4		1.3	2.4	
I^- Standby	Negative Supply Current				−1.5	−0.7		−1.5	−0.7		

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

T_A = over operating temperature range, V+ = 15V, V− = −15V, V_{EN} = 2.4V, GND = 0V, unless otherwise specified.

Symbol	Parameter		Test Conditions		DG508AA, DG509AA			DG508AB/C, DG509AB/C			Units
					Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
SWITCH											
V_{ANALOG}	Analog Signal Range		(Note 6)		−15		15	−15		15	V
$R_{DS(on)}$	Drain-Source ON Resistance		Sequence Each Switch On V_{AL} = 0.8V and V_{AH} = 2.4V	I_S = −200 µA, V_D = 10V			500			550	Ω
				I_S = −200 µA, V_D = −10V			500			500	
$I_{S(off)}$	Source OFF Leakage Current		V_{EN} = 0V	V_S = 10V, V_D = −10V			50			50	nA
				V_S = −10V, V_D = 10V	−50			−50			
$I_{D(off)}$	Drain OFF Leakage Current	DG508A	V_{EN} = 0V	V_S = −10V, V_D = 10V			200			200	nA
				V_S = 10V, V_D = −10V	−200			−200			
		DG509A		V_S = −10V, V_D = 10V			100			100	
				V_S = 10V, V_D = −10V	−100			−100			
$I_{D(on)}$ (Note 5)	Drain ON Leakage	DG508A	Sequence Each Switch On V_{AL} = 0.8V and V_{AH} = 2.4V	$V_D = V_{S(all)}$ = 10V			200			200	nA
				$V_D = V_{S(all)}$ = −10V	−200			−200			
		DG509A		$V_D = V_{S(all)}$ = 10V			100			100	
				$V_D = V_{S(all)}$ = −10V	−100			−100			
INPUT											
I_{AH}	Address Input Current, Input Voltage High		V_A = 2.4V		−30			−30			µA
			V_A = 15V				30			30	µA
I_{AL}	Address Input Current, Input Voltage Low		V_{EN} = 2.4V	All V_A = 0V	−30			−30			µA
			V_{EN} = 0V		−30			−30			µA
SUPPLY											
I^+	Positive Supply Current		V_{EN} = 5.0V	All V_A = 0			2.4			2.4	mA
I^-	Negative Supply Current				−1.5			−1.5			
I^+ Standby	Positive Supply Current		V_{EN} = 0V				2.4			2.4	
I^- Standby	Negative Supply Current				−1.5			−1.5			

NOTE 1: Signals on V_S, V_D, or V_{IN} exceeding V^+ or V^- will be clamped by internal diodes. Limit diode forward current to maximum current ratings.

2: Typical values are for design aid only, not guaranteed and not subject to production testing.

3: The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

4: OFF isolation = 20 log $|V_S|/|V_D|$, where V_S = input to OFF switch, and V_D = output due to V_S.

5: $I_{D(on)}$ is leakage from driver into "ON" switch.

6: Parameter not tested. Parameter guaranteed by design or characterization.

NOTE: All typical values have been characterized but are not tested.

DG508A/509A

TRUTH TABLES

DG508A

A_2	A_1	A_0	EN	ON Switch
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2, EN
Logic "1" = $V_{AH} \geq 2.4V$
Logic "0" = $V_{AL} \leq 0.8V$

DG509A

A_1	A_0	EN	ON Switch Pair
X	X	0	NONE
0	0	1	1a, 1b
0	1	1	2a, 2b
1	0	1	3a, 3b
1	1	1	4a, 4b

A_0, A_1, EN
Logic "1" = $V_{AH} \geq 2.4V$
Logic "0" = $V_{AL} \leq 0.8V$

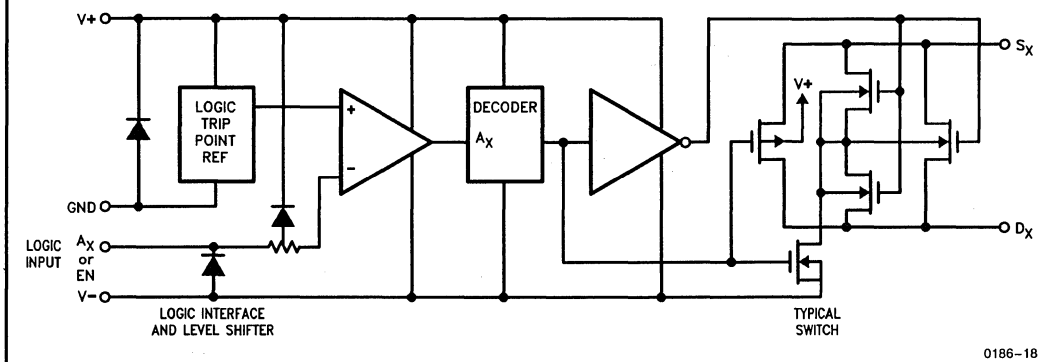


Figure 3: Schematic Diagram

LOGIC INPUTS

The address and enable inputs are fully TTL/CMOS compatible over the full supply range of ±5V to ±20V.

These inputs are protected from positive and negative transients by clamping diodes.

NOTE: All typical values have been characterized but are not tested.

SWITCHING INFORMATION

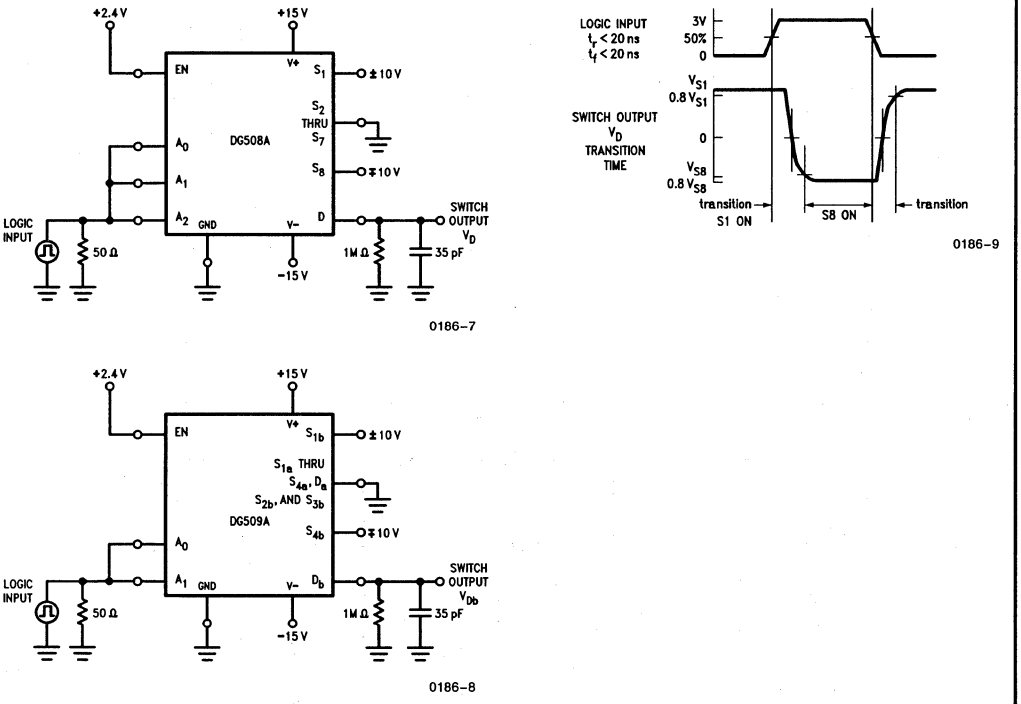


Figure 4: $t_{transition}$ Switching Time Test Circuit and Waveforms

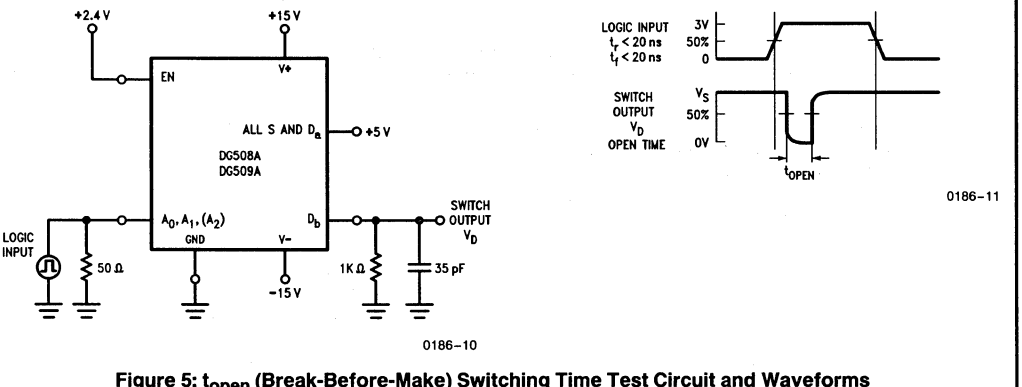


Figure 5: t_{open} (Break-Before-Make) Switching Time Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

SWITCHING INFORMATION (Continued)

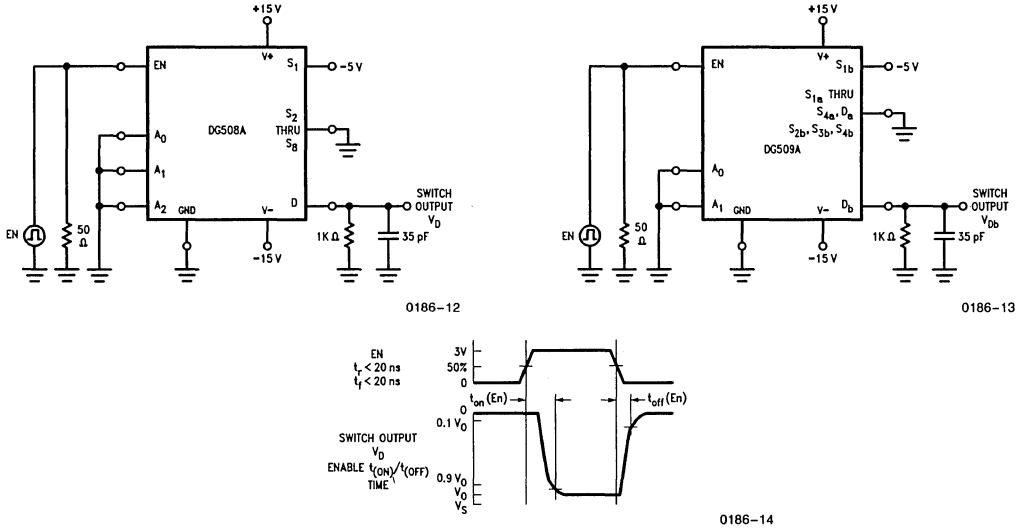
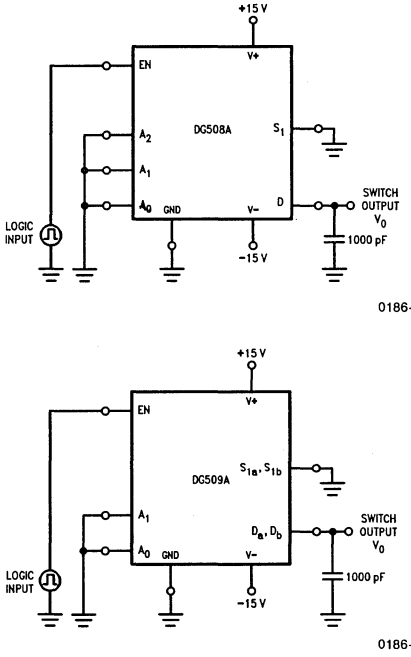
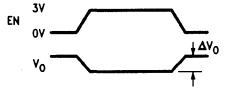


Figure 6: Enable t_{on} and t_{off} Switching Time Test Circuit and Waveforms





ΔV_O is the measured voltage error due to charge injection. The error voltage in Coulombs is $Q = C_L \times \Delta V_O$.

Figure 7: Charge Injection Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

SWITCHING INFORMATION (Continued)

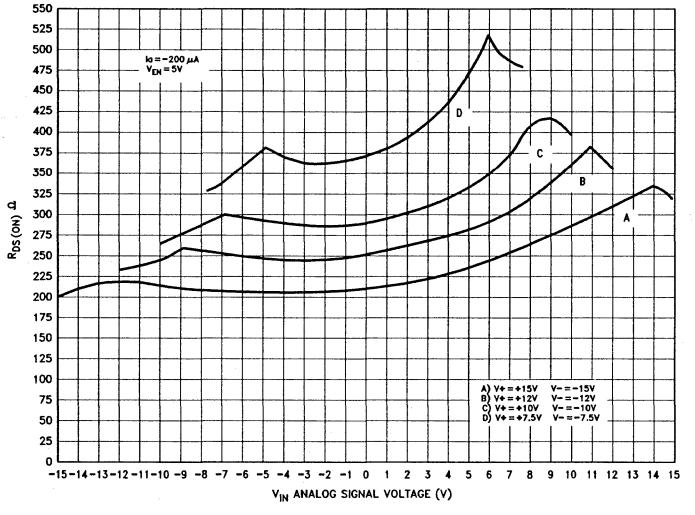


Figure 8: $R_{DS(on)}$ vs Analog Signal Voltage vs Supply Voltage

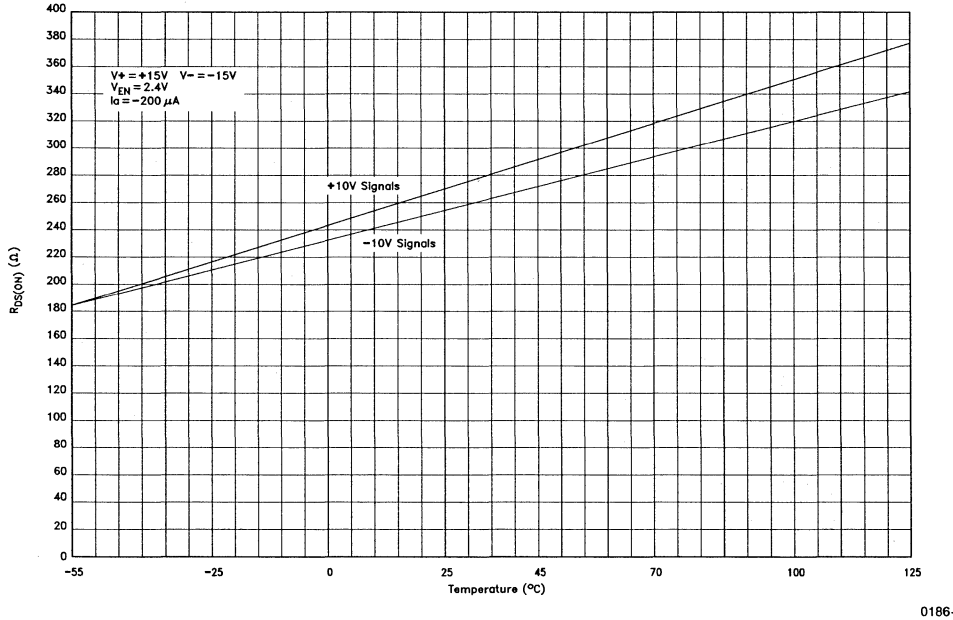


Figure 9: Typical $R_{DS(on)}$ Variation with Temperature

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

DG526/DG527
16-Channel/Dual 8-Channel CMOS Latchable Multiplexers

GENERAL DESCRIPTION

The DG526/DG527 are CMOS monolithic 16-channel and dual 8-channel analog multiplexers, with on-chip address and control latches to simplify design in microprocessor based applications. The DG526 uses 4 address inputs to control its 16 channels and the DG527 uses 3 address inputs to control its 8 pairs of channels. The enable pin is used to enable the address latches during the $\overline{WR}$ pulse. It can be hard wired to the logic supply if one of the channels will always be used (except during a reset) or it can be tied to address decoding circuitry for memory mapped operation. The $\overline{RS}$ pin is used to clear all latches regardless of the state of any other latch or control line. The $\overline{WR}$ pin is used to transfer the state of the address control lines to their latches, except during a reset or when EN is low.

A channel in the ON state conducts current equally well in both directions. In the OFF state each channel blocks voltage up to the supply rails. The address inputs, $\overline{WR}$, $\overline{RS}$ and the enable input are TTL and CMOS compatible over the full specified operation temperature range. Both DG526 and DG527 are available in the military, industrial, and commercial temperature ranges.

FEATURES

- **Direct RESET**
- **TTL and CMOS Compatible Address and Enable Inputs**
- **44V Maximum Power Supply Rating**
- **Break-Before-Make Switching**
- **Alternate Source**

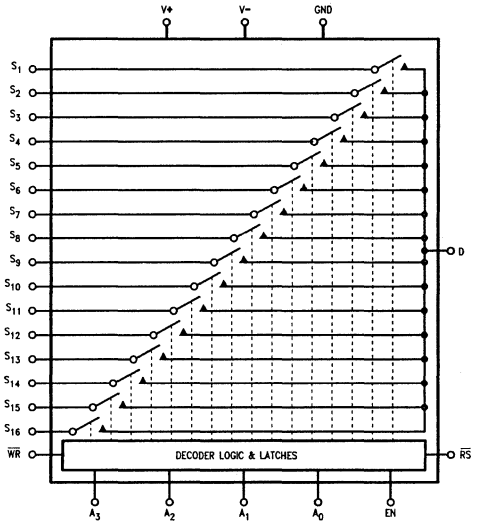
APPLICATIONS

- **Data Acquisition Systems**
- **Communication Systems**
- **Automatic Test Equipment**
- **Microprocessor Controlled System**

ORDERING INFORMATION

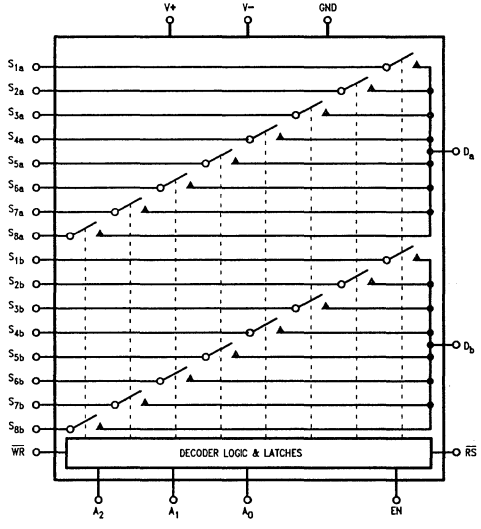
Part Number	Temperature Range	Package
DG526AK/527AK	−55°C to +125°C	28-Pin CERDIP
DG526BK/527BK	−25°C to +85°C	28-Pin CERDIP
DG526CK/527CK	0°C to +70°C	28-Pin CERDIP
DG526CJ/527CJ	0°C to +70°C	28-Pin Plastic DIP

DG526
16 Channel Single Ended Multiplexer



0435-1

DG527
Differential 8 Channel Multiplexer



0435-2

Figure 1: Functional Diagrams

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NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- 44V
V^- to Ground ..... −25V
V_{IN} to Ground (Note 1) ..... V^- − 2V), (V^+ + 2V)
V_S or V_D to V^+ (Note 1) ..... +2, (V^- − 2V)
V_S or V_D to V^- (Note 1) ..... −2, (V^+ + 2V)
Current, any Terminal except S or D ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Max) ..... 40 mA
Operating Temperature
C Suffix ..... 0°C to +70°C
B Suffix ..... −25°C to +85°C
A Suffix ..... −55°C to +125°C
Storage Temperature
C Suffix ..... −65°C to +125°C
A & B Suffix ..... −65°C to +150°C
Lead Temperature (Soldering, 10 Sec) ..... 300°C
Power Dissipation*
28 Pin-CERDIP Package** ..... 1200 mW
28 Pin-Plastic Package*** ..... 625 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 16 mW/°C above +75°C.
***Derate 8.3 mW/°C above +75°C.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS (Note 3)

V^+ = 15V, V^- = −15V, GND = 0V, $\overline{WR}$ = 0V, $\overline{RS}$ = 2.4V, EN = 2.4V, T_A = 25°C, unless otherwise specified

Symbol	Parameter		Test Conditions		DG526, DG527 Min	DG526, DG527 Typ (Note 2)	DG526, DG527 Max	Units
SWITCH								
V_{ANALOG}	Analog Signal Range		(Note 7)		−15		15	V
$R_{DS(ON)}$	Drain-Source ON Resistance		Sequence Each Switch On V_{AL} = 0.8V and V_{AH} = 2.4V	I_S = −200 μA, V_D = +10V		270	400	Ω
				I_S = −200 μA, V_D = −10V		230	400	
$\Delta R_{DS(ON)}$	Greatest Change in Drain Source ON Resistance between Channels		−10V ≤ V_S ≤ +10V $\Delta R_{DS(on)} = \frac{R_{DS(on)max} - R_{DS(on)min}}{R_{DS(on)avg.}}$			6		%
$I_{S(OFF)}$	Source OFF Leakage Current		V_{EN} = 0V	V_S = +10V, V_D = −10V	−1	0.02	1	nA
				V_S = −10V, V_D = +10V	−1	0.02	1	
$I_{D(OFF)}$	Drain OFF Leakage Current	DG526	V_{EN} = 0V	V_S = −10V, V_D = +10V	−10	0.2	10	nA
				V_S = +10V, V_D = −10V	−10	0.2	10	
		DG527		V_S = −10V, V_D = +10V	−5	0.2	5	
				V_S = +10V V_D = −10V	−5	0.2	5	
$I_{D(ON)}$ (Note 5)	Drain ON Leakage Current	DG526	Sequence Each Switch On V_{AL} = 0.8V and V_{AH} = 2.4V	$V_D = V_{S(ALL)}$ = + 10V	−10	0.2	10	nA
				$V_D = V_{S(ALL)}$ = −10V	−10	0.2	10	
		DG527		$V_D = V_{S(ALL)}$ = +10V	−5	0.2	5	
				$V_D = V_{S(ALL)}$ = −10V	−5	0.2	5	

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued)

T_A = 25°C, V^+ = 15V, V^- = −15V, GND = 0V, $\overline{WR}$ = 0V, $\overline{RS}$ = 2.4V, EN = 2.4V, unless otherwise specified

Symbol	Parameter	Test Conditions		DG526, DG527 Min	DG526, DG527 Typ (Note 2)	DG526, DG527 Max	Units
INPUT							
I_{AH}	Address Input Current, Input Voltage High	V_A = 2.4V		−10	0.02		µA
		V_A = 15V			0.02	10	µA
I_{AL}	Address Input Current, Input Voltage Low	V_{EN} = 2.4V	All V_A = 0V, $\overline{RS}$ = 0V, $\overline{WR}$ = 0V	−10	0.01		µA
		V_{EN} = 0V		−10	0.01		µA
DYNAMIC							
$t_{transition}$	Switching Time of Multiplexer	See Figure 6			0.65	1	µs
t_{open}	Break-Before-Make Interval	See Figure 7			0.2		µs
t_{on} (EN, $\overline{WR}$)	Enable and Write Turn-ON Time	See Figures 4 and 9 (Note 7)			0.7	1.5	µs
t_{off} (EN, $\overline{RS}$)	Enable and Reset Turn-OFF Time	See Figures 5 and 10 (Note 7)			0.4	1	µs
OIRR (Note 4)	OFF Isolation	V_{EN} = 0V, R = 1 kΩ, C_L = 15 pF, V_S = 7 VRMS, f = 500 kHz			55		dB
C_{in}	Logic Input Capacitance	f = 1 MHz			6		pF
$C_{S(off)}$	Source OFF Capacitance	V_S = 0V	V_{EN} = 0V, f = 140 kHz		10		pF
$C_{D(off)}$	Drain OFF Capacitance, DG526	V_D = 0V			65		pF
	Drain OFF Capacitance, DG527	V_D = 0V			35		pF
Q	Charge Injection	See Figure 11			6		pC
SUPPLY							
I^+	Positive Supply Current	V_{EN} = 0V	All V_A = 0V		2.0	3.0	mA
I^-	Negative Supply Current	V_{EN} = 0V	All V_A = 0V	−2.0	−1.2		mA

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued)

T_A = over operating temperature range, $V^+ = 15V$, $V^- = -15V$, GND = 0V, $\overline{WR}$ = 0V, $\overline{RS}$ = 2.4V, EN = 2.4V, unless otherwise specified

Symbol	Parameter		Test Conditions		DG526, DG527 Min	DG526, DG527 Typ (Note 2)	DG526, DG527 Max	Units
SWITCH								
V_{ANALOG}	Analog Signal Range		(Note 7)		−15		15	V
$\Delta R_{DS(on)}$	Greatest Change in Drain Source ON Resistance between Channels		$-10V \le V_S \ge +10V$			6		%
$R_{DS(on)}$	Drain-Source ON Resistance		Sequence Each Switch On V_{AL} = 0.8V V_{AH} = 2.4V	$I_S = -200\ \mu A$, $V_D = 10V$			500	Ω
				$I_S = -200\ \mu A$, $V_D = -10V$			500	
$I_{S(Off)}$	Source OFF Leakage Current		V_{EN} = 0V	$V_S = +10V$, $V_D = -10V$	−50		50	nA
				$V_S = -10V$, $V_D = +10V$	−50		50	
$I_{D(off)}$	Drain OFF Leakage Current	DG526	V_{EN} = 0V	$V_S = -10V$, $V_D = +10V$	−300		300	nA
				$V_S = +10V$, $V_D = -10V$	−300		300	
		DG527		$V_S = -10V$, $V_D = +10V$	−200		200	
				$V_S = +10V$, $V_D = -10V$	−200		200	
$I_{D(ON)}$ (Note 5)	Drain ON Leakage Current	DG526	Sequence Each Switch On V_{AL} = 0.8V and V_{AH} = 2.4V	$V_D = V_{S(ALL)} = +10V$	−300		300	nA
				$V_D = V_{S(ALL)} = -10V$	−300		300	
		DG527		$V_D = V_{S(ALL)} = +10V$	−200		200	
				$V_D = V_{S(ALL)} = -10V$	−200		200	
INPUT								
I_{AH}	Address Input Current Input Voltage High		V_A = 2.4V		−30			μA
			V_A = 15V				30	μA
I_{AL}	Address Input Current, Input Voltage Low		V_{EN} = 2.4V	All V_A = 0V	−10			μA
			V_{EN} = 0V	$\overline{RS}$ = 0V, $\overline{WR}$ = 0V	−10			μA
SUPPLY								
I^+	Positive Supply Current		V_{EN} = 0V, All V_A = 0V				4.5	mA
I^-	Negative Supply Current				−3.2			

NOTE 1. Signals on V_S, V_D or V_{IN} exceeding V^+ or V^- will be clamped by internal diodes. Limit diode forward current to maximum current rating.

2. Typical values are for design aid only, not guaranteed and not subject to production testing.

3. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

4. OFF isolation = 20 log $|V_S|/|V_D|$, where V_S = input to OFF switch, and V_D = output due to V_S.

5. $I_{D(ON)}$ is leakage from driver into "ON" switch.

6. Period of Reset ($\overline{RS}$) pulse must be at least 50 μs during or after power ON.

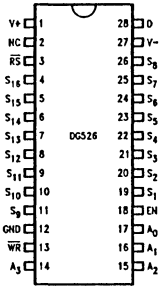
7. Parameter not tested. Parameter guaranteed by design or characterization.

NOTE: All typical values have been characterized but are not tested.

DG526/DG527

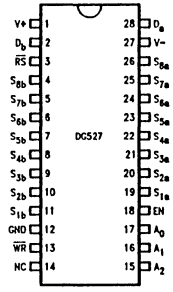
Dual-In-Line Packages

DG526
28 Lead DIP
28 Lead SOIC



0435-3

DG527
28 Lead DIP
28 Lead SOIC



0435-4

Figure 2: Pin Configurations

Truth Tables

DG526

	A_3	A_2	A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	ON Switch
Latching	X	X	X	X	X	↗	1	Maintains Previous Switch State
Reset	X	X	X	X	X	X	0	None (Latches Cleared)
	X	X	X	X	0	0	1	None
	0	0	0	0	1	0	1	1
	0	0	0	1	1	0	1	2
	0	0	1	0	1	0	1	3
	0	0	1	1	1	0	1	4
	0	1	0	0	1	0	1	5
	0	1	0	1	1	0	1	6
	0	1	1	0	1	0	1	7
Transparent	0	1	1	1	1	0	1	8
Operation	1	0	0	0	1	0	1	9
	1	0	0	1	1	0	1	10
	1	0	1	0	1	0	1	11
	1	0	1	1	1	0	1	12
	1	1	0	0	1	0	1	13
	1	1	0	1	1	0	1	14
	1	1	1	0	1	0	1	15
	1	1	1	1	1	0	1	16

Logic "0" = V_{AL}, $V_{ENL} \leq 0.8V$

DG527

	A_2	A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	ON Switch
Latching	X	X	X	X	↗	1	Maintains Previous Switch State
Reset	X	X	X	X	X	0	None (Latches Cleared)
	X	X	X	0	0	1	None
	0	0	0	1	0	1	1
Transparent	0	0	1	1	0	1	2
Operation	0	1	0	1	0	1	3
	0	1	1	1	0	1	4
	1	0	0	1	0	1	5
	1	0	1	1	0	1	6
	1	1	0	1	0	1	7
	1	1	1	1	0	1	8

Logic "1" = V_{AH}, $V_{ENH} \geq 2.4V$

Minimum Input Timing Requirements

Parameter	Measured Terminal	Min Limits Over Full Temp Range	Unit	Test Circuit
t_{WW} WRITE Pulse Width	$\overline{WR}$	300	ns	See Figure 4
t_{DW} A,EN Data Valid to WRITE	A_0, A_1, A_2, (A_3), EN, $\overline{WR}$	180		
t_{WD} A,EN Data Valid after WRITE	A_0, A_1, A_2, (A_3), EN, $\overline{WR}$	30		
$t_{\overline{RS}}$ RESET Pulse Width	$\overline{RS}$	500		See Figure 5 V_S = 5V

NOTE: All typical values have been characterized but are not tested.

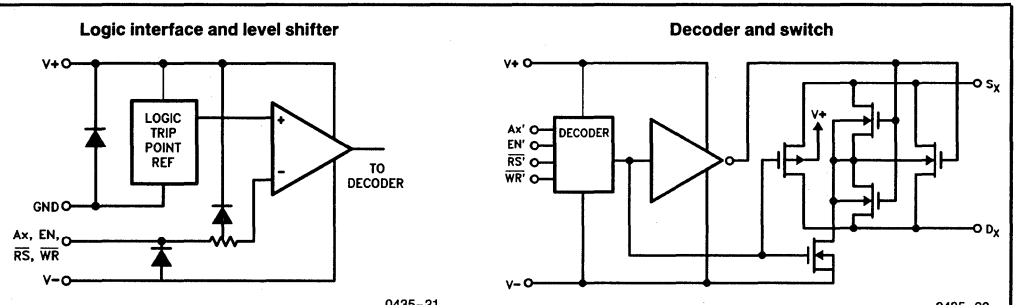


Figure 3: Schematic Diagrams

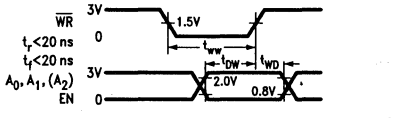


Figure 4: $\overline{WR}$ Timing Waveforms

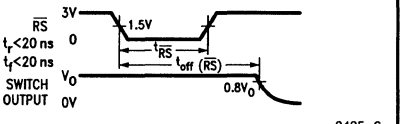


Figure 5: $\overline{RS}$ Timing Waveforms

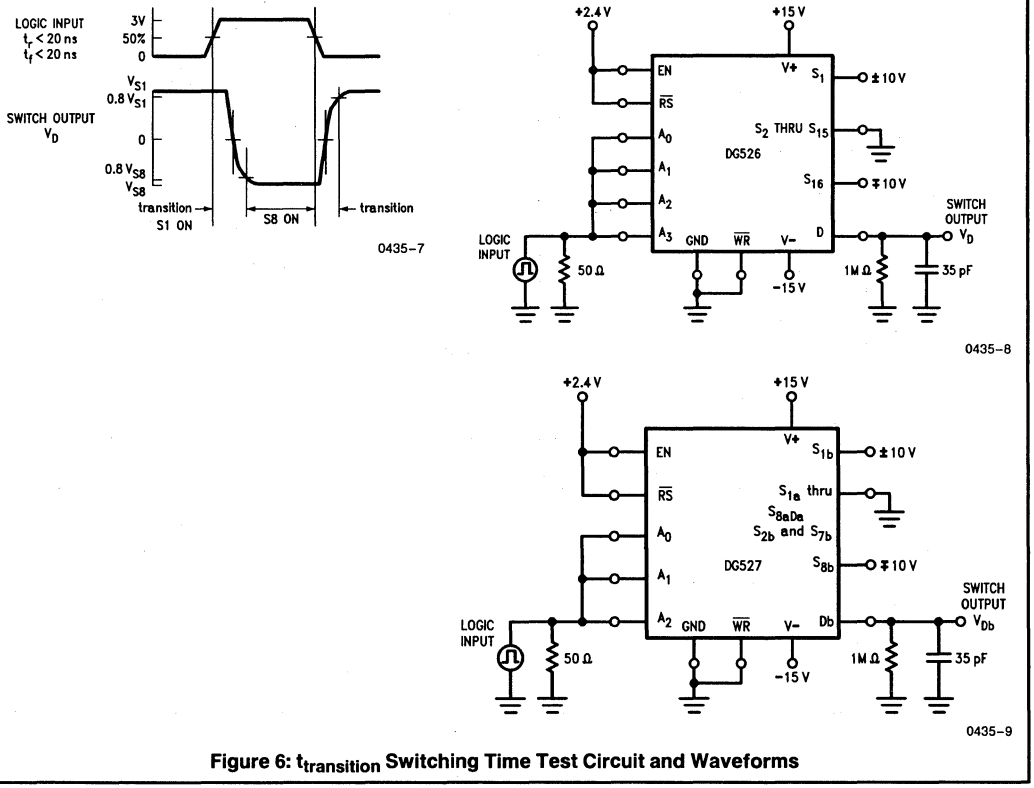


Figure 6: $t_{transition}$ Switching Time Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

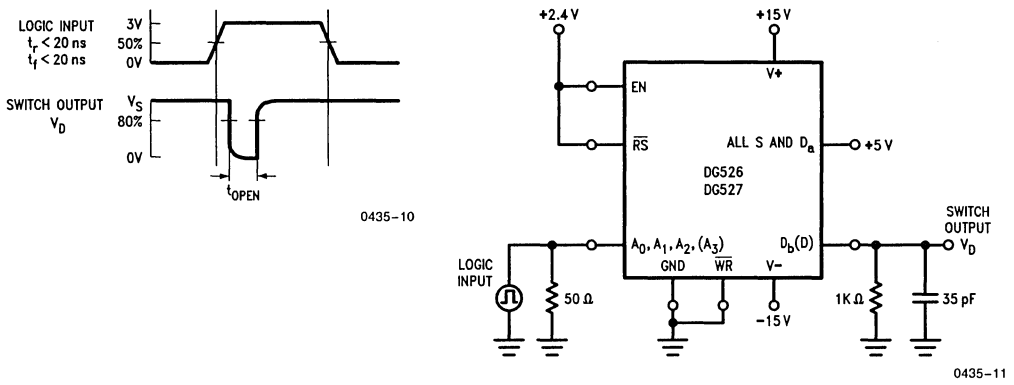


Figure 7: t_{open} (Break-Before-Make) Switching Time Test Circuit and Waveforms

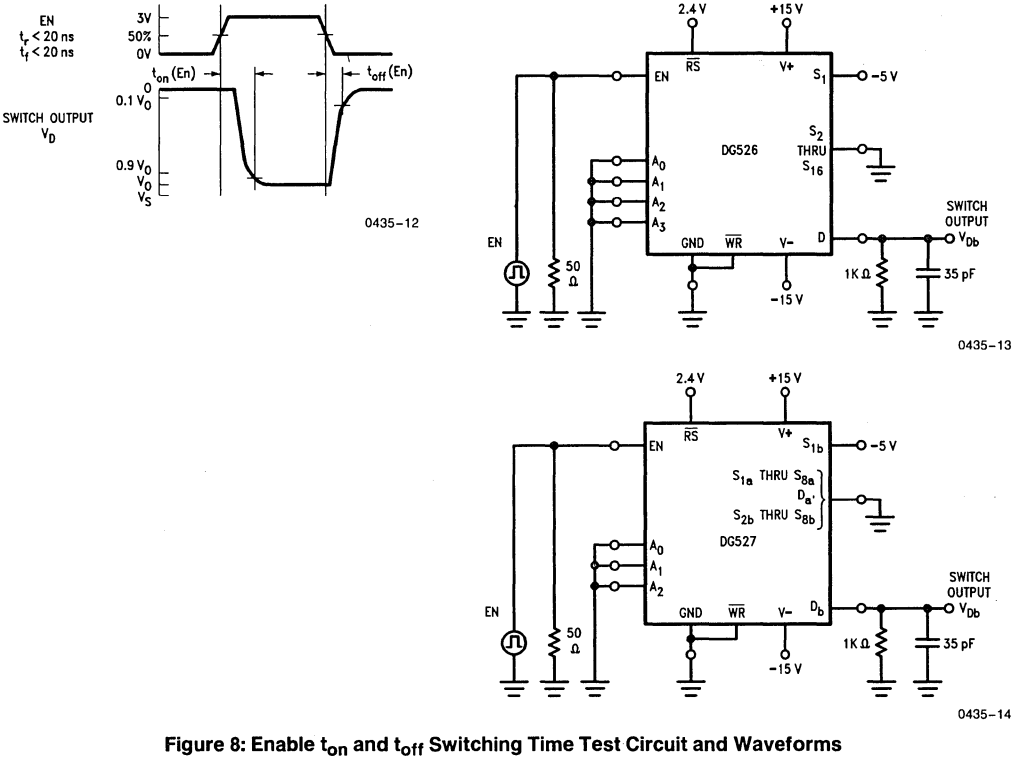
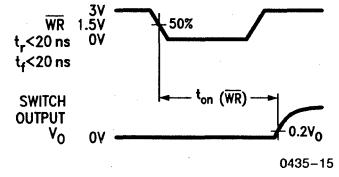


Figure 8: Enable t_{on} and t_{off} Switching Time Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.



Device must be reset prior to applying $\overline{WR}$ pulse

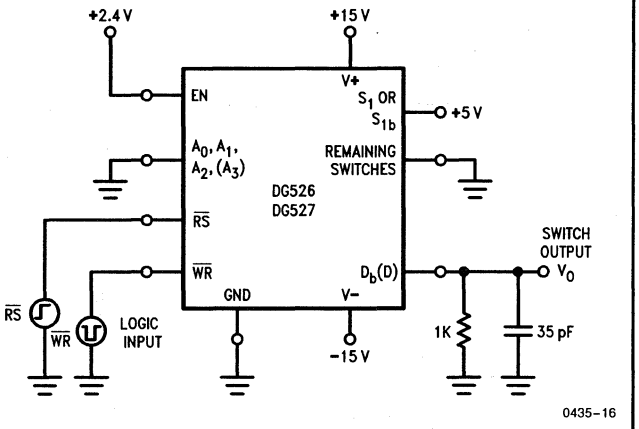
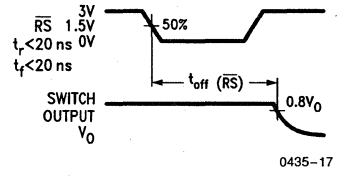


Figure 9: Write t_{on} Switching Time Test Circuit and Waveforms



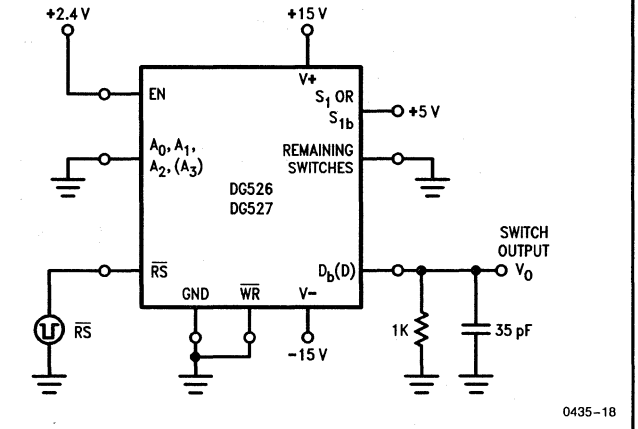
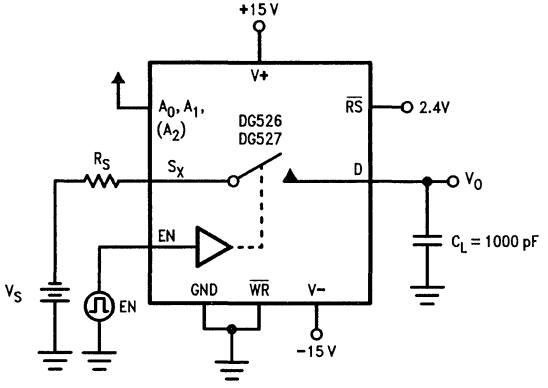
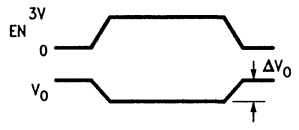


Figure 10: Reset t_{off} Switching Time Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.





0435-20

ΔV_O is the measured voltage error due to charge injection. The error voltage in Coulombs is $Q = C_L \times \Delta V_O$.

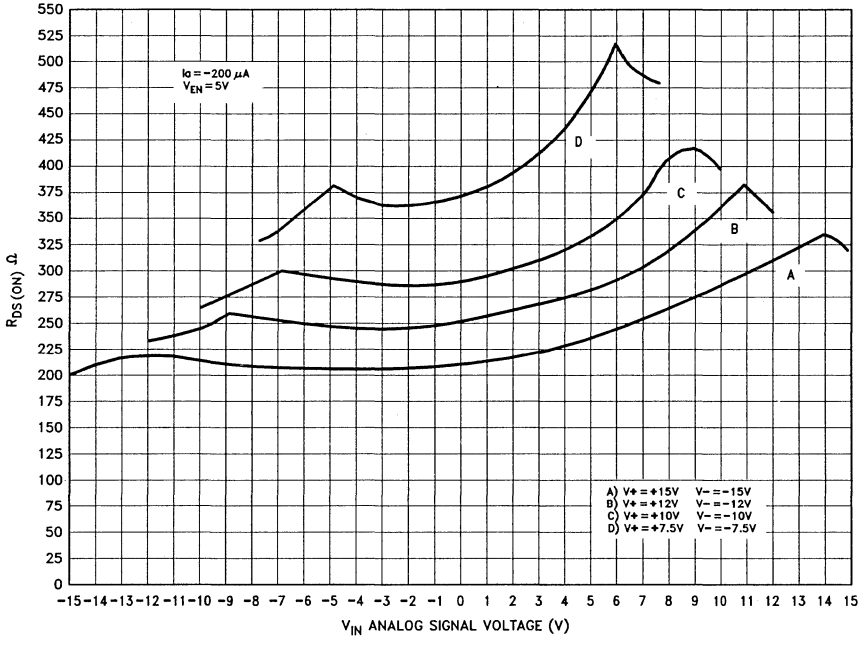
0435-19

Figure 11: Charge Injection Test Circuit and Waveforms

Logic Inputs

The address, enable $\overline{WR}$ and $\overline{RS}$ inputs are fully TTL/CMOS compatible over the full supply range of ±5V to ±20V.

These inputs are protected from positive and negative transients by clamping diodes.



0435-23

Figure 12: $R_{DS(on)}$ vs Analog Signal Voltage vs Supply Voltage

8

NOTE: All typical values have been characterized but are not tested.

DG526/DG527

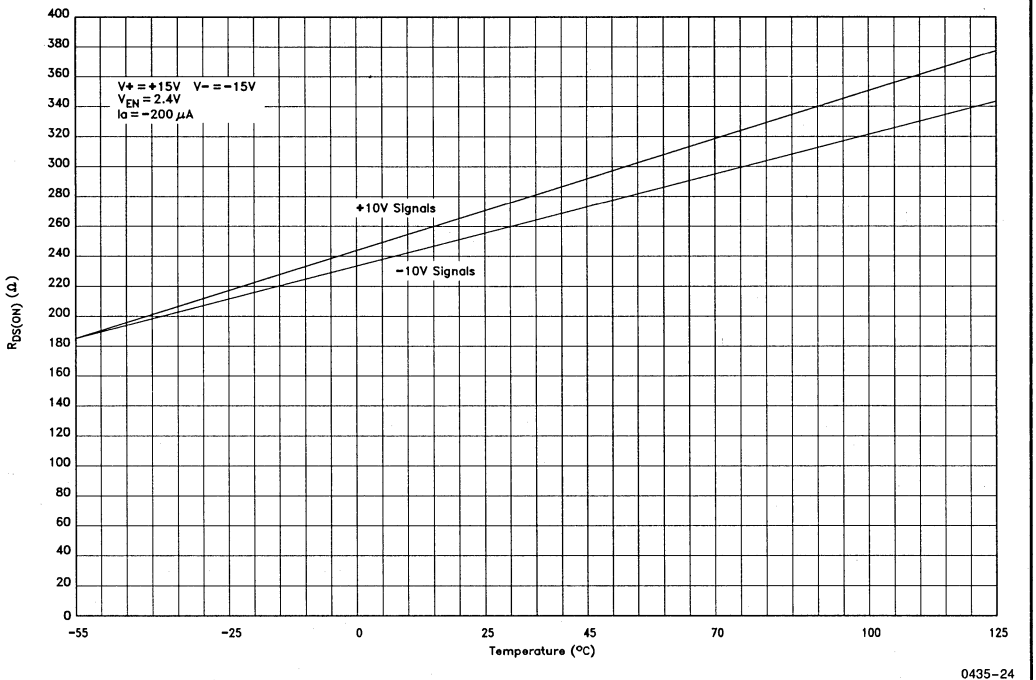


Figure 13: Typical $R_{DS(on)}$ Variation with Temperature

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

DG528/DG529
8-Channel/Dual 4-Channel Latchable Multiplexers

GENERAL DESCRIPTION

The DG528/DG529 are CMOS monolithic 8-channel and dual 4-channel latchable analog multiplexers, with on-chip address and control latches to simplify design in microprocessor based applications. The DG528 uses 3 address inputs to control its 8 channels and the DG529 uses 2 address inputs to control its dual 4 channels. The enable pin is used to enable the address latches during the $\overline{WR}$ pulse. It can be hard-wired to the logic supply if one of the channels will always be used (except during a reset) or it can be tied to address decoding circuitry for memory mapped operation. The $\overline{RS}$ pin is used to clear all latches regardless of the state of any other latch or control line. The $\overline{WR}$ pin is used to transfer the state of the address control lines to their latches, except during a reset or when EN is low.

A channel in the ON state conducts current equally well in both directions. In the OFF state each channel blocks voltage up to the supply rails. The address inputs and the enable input are TTL and CMOS compatible over the full specified operating temperature range. Both DG528 and DG529 are available in the military, industrial, and commercial temperature ranges.

FEATURES

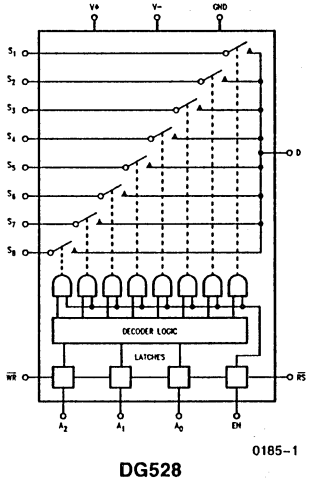
- Low Power Consumption
- TTL and CMOS Compatible Inputs
- 44V Maximum Power Supply Rating
- High Latchup Immunity
- Break-Before-Make Switching
- Alternate Source

APPLICATIONS

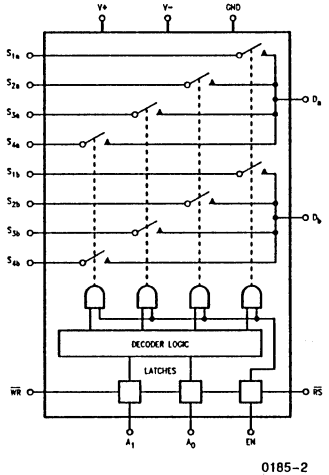
- Data Acquisition Systems
- Communications Systems
- Automatic Test Equipment
- Microprocessor Controlled System

ORDERING INFORMATION

Part Number	Temp. Range	Package
DG528AK/529AK	-55°C to +125°C	18-Pin CERDIP
DG528BK/529BK	-25°C to +85°C	18-Pin CERDIP
DG528CK/529CK	0°C to +70°C	18-Pin CERDIP
DG528CJ/529CJ	0°C to +70°C	18-Pin Plastic DIP
DG528CY/529CY	0°C to +70°C	18-Pin SOIC



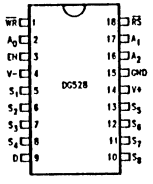
DG528
8-Channel Single-Ended Multiplexer with Latches



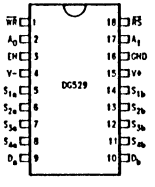
DG529
Dual 4-Channel Multiplexer with Latches

Figure 1: Functional Diagrams

DG528
18 Lead DIP
18 Lead SOIC



DG529
18 Lead DIP
18 Lead SOIC



Top View

Figure 2: Pin Configurations

8

307125-003

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V+ to V− 44V
V− to Ground ..... −25V
V_{IN} to Ground (Note 1) ..... (V− − 2V), (V+ + 2V)
V_S or V_D to V+ (Note 1) ..... +2, (V− − 2V)
V_S or V_D to V− (Note 1) ..... −2, (V+ + 2V)
Current, Any Terminal except S or D ..... 30 mA
Continuous Current, S or D ..... 20 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% duty cycle max) ..... 40 mA
Operating Temperature
C Suffix ..... 0°C to +70°C
B Suffix ..... −25°C to +85°C
A Suffix ..... −55°C to +125°C
Storage Temperature
C Suffix ..... −65°C to +125°C
A & B Suffix ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C
Power Dissipation*
CERDIP Package** ..... 900 mW
Plastic Package*** ..... 470 mW

*Device mounted with all leads soldered or welded to PC board

**Derate 12 mW/°C above 75°C

***Derate 6.3 mW/°C above 75°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS (Note 3)

V+ = 15V, V− = −15V, GND = 0V, $\overline{WR}$ = 0V, $\overline{RS}$ = 2.4V, EN = 2.4V, T_A = 25°C unless otherwise specified.

Symbol	Parameter		Test Conditions (Note 6)		DG528A, DG529A			DG528B/C, DG529B/C			Units
					Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
SWITCH											
V_{ANALOG}	Analog Signal Range		(Note 7)		−15		15	−15		15	V
$R_{DS(on)}$	Drain-Source ON Resistance		V_D = ±10V, V_{AL} = 0.8V, V_{AH} = 2.4V, I_S = −200 μA Sequence Each Switch ON			270	400		270	450	Ω
$\Delta R_{DS(on)}$	Greatest Change in Drain Source ON Resistance between Channels		−10V ≤ V_S ≤ 10V $\Delta R_{DS(on)} = \frac{R_{DS(on)max} - R_{DS(on)min}}{R_{DS(on)avg.}}$			6			6		%
$I_{S(off)}$	Source OFF Leakage Current		V_{EN} = 0V	V_S = ±10V, V_D = ∓10V	−1	−0.005	1	−5	−0.005	5	nA
$I_{D(off)}$	Drain OFF Leakage Current	DG528	V_{EN} = 0V	V_S = ∓10V, V_D = ±10V	−10	−0.015	10	−20	0.015	20	
		DG529		V_S = ∓10V, V_D = ±10V	−10	−0.008	10	−20	−0.008	20	
$I_{D(on)}$ (Note 5)	Drain ON Leakage Current	DG528	Sequence Each Switch On V_{AL} = 0.8V, V_{AH} = 2.4V	$V_{S(all)}$ = V_D = ±10V	−10	−0.03	10	−20	−0.03	20	
		DG529		$V_{S(all)}$ = V_D = ±10V	−10	−0.015	10	−20	−0.015	20	
INPUT											
I_{AH}	Address Input Current, Input Voltage High		V_A = 2.4V		−10	−0.002		−10	−0.002		μA
			V_A = 15V			0.006	10		0.006	10	μA
I_{AL}	Address Input Current, Input Voltage Low		V_{EN} = 2.4V	$V_{A(all)}$ = 0V	−10	−0.002		−10	−0.002		μA
			V_{EN} = 0V	$\overline{RS}$ = 0V, $\overline{WR}$ = 0V	−10	−0.002		−10	−0.002		μA

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued)

V+ = 15V, V− = −15V, GND = 0V, $\overline{WR}$ = 0V, $\overline{RS}$ = 2.4V, EN = 2.4V, T_A = 25°C unless otherwise specified.

Symbol	Parameter		Test Conditions (Note 6)		DG528A, DG529A			DG528B/C, DG529B/C			Units
					Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
DYNAMIC											
$t_{transition}$	Switching Time of Multiplexer		See Figure 6			0.6	1		0.6		µs
t_{open}	Break-Before-Make Interval		See Figure 7			0.2			0.2		µs
$t_{on(EN, \overline{WR})}$	Enable and Write Turn-ON Time		See Figures 8 and 9 (Note 7)			1	1.5		1		µs
$t_{off(EN, \overline{RS})}$	Enable and Reset Turn-OFF Time		See Figures 8 and 9 (Note 7)			0.4	1		0.4		µs
OIRR (Note 4)	OFF Isolation		V_{EN} = 0V, R_L = 1 kΩ, C_L = 15 pF V_S = 7 VRMS, f = 500 kHz			68			68		dB
C_{IN}	Logic Input Capacitance		f = 1 MHz			2.5			2.5		pF
$C_{S(off)}$	Source OFF Capacitance		V_S = 0V	V_{EN} = 0V, f = 140 kHz		5			5		pF
$C_{D(off)}$	Drain OFF Capacitance	DG528	V_D = 0V			25			25		
		DG529				12			12		
Q	Charge Injection		See Figure 11			4			4		pC
SUPPLY											
I+	Positive Supply Current		V_{EN} = 0V, $V_{A(all)}$ = 0V				2.5			2.5	mA
I−	Negative Supply Current				−1.5			−1.5			

ELECTRICAL CHARACTERISTICS

T_A = over operating temperature range, V+ = 15V, V− = −15V, GND = 0V, $\overline{WR}$ = 0V, $\overline{RS}$ = 2.4V, EN = 2.4V unless otherwise specified.

Symbol	Parameter		Test Conditions (Note 6)		DG528A, DG529A			DG528B/C, DG529B/C			Units
					Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
SWITCH											
V_{ANALOG}	Analog Signal Range		(Note 7)		−15		15	−15		15	V
$R_{DS(on)}$	Drain-Source ON Resistance		V_D = ±10V, V_{AL} = 0.8V, V_{AH} = 2.4V, I_S = −200 µA Sequence Each Switch ON				500			500	Ω
$I_{S(off)}$	Source OFF Leakage Current		V_{EN} = 0V	V_S = ±10V, V_D = ∓10V	−50		50	−50		50	nA
$I_{D(off)}$	Drain OFF Leakage Current	DG528	V_{EN} = 0V	V_S = ∓10V, V_D = ±10V	−200		200	−200		200	
		DG529		V_S = ∓10V, V_D = ±10V	−100		100	−100		100	
$I_{D(on)}$ (Note 5)	Drain ON Leakage Current	DG528	Sequence Each Switch On	$V_{S(all)}$ = V_D = +10V	−200		200	−200		200	
		DG529	V_{AL} = 0.8V, V_{AH} = 2.4V	$V_{S(all)}$ = V_D = −10V	−100		100	−100		100	

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued)

T_A = over operating temperature range, V+ = 15V, V− = −15V, GND = 0V, $\overline{WR}$ = 0V, $\overline{RS}$ = 2.4V, EN = 2.4V unless otherwise specified.

Symbol	Parameter	Test Conditions (Note 6)		DG528A, DG529A			DG528B/C, DG529B/C			Units
				Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
INPUT										
I_{AH}	Address Input Current, Input Voltage High	V_A = 2.4V		−30			−30			µA
		V_A = 15V				30			30	µA
I_{AL}	Address Input Current, Input Voltage Low	V_{EN} = 2.4V	$V_{A(all)}$ = 0V	−30			−30			µA
		V_{EN} = 0V	$\overline{RS}$ = 0V, $\overline{WR}$ = 0V	−30			−30			µA
SUPPLY										
I^+	Positive Supply Current	V_{EN} = 0V, $V_{A(all)}$ = 0V				2.5			2.5	mA
I^-	Negative Supply Current			−1.5			−1.5			

NOTES 1: Signals on V_S, V_D, or V_{IN} exceeding V+ or V− will be clamped by internal diodes. Limit diode forward current to maximum current ratings.

2: Typical values are for design aid only, not guaranteed and not subject to production testing.

3: The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.

4: OFF isolation = 20 log $\frac{|V_S|}{|V_D|}$, where V_S = input to OFF switch, and V_D = output due to V_S.

5: $I_{D(on)}$ is leakage from driver into "ON" switch.

6: Period of Reset ($\overline{RS}$) pulse must be at least 50 µs during or after power ON.

7: Parameter not tested. Parameter guaranteed by design or characterization.

TRUTH TABLES

DG528

A_2	A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	On Switch
X	X	X	X	↗	1	Maintains previous switch condition
X	X	X	X	X	0	NONE (latches cleared)
X	X	X	0	0	1	NONE
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

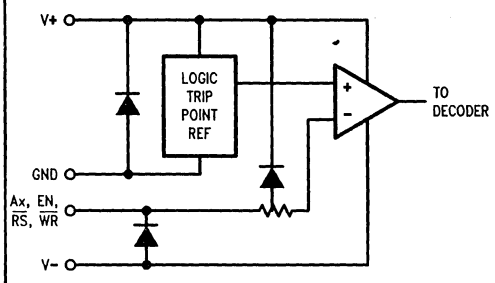
DG529

A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	On Switch
X	X	X	↗	1	Maintains previous switch condition
X	X	X	X	0	NONE (latches cleared)
X	X	0	0	1	NONE
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

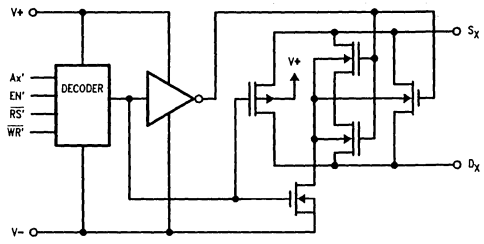
Logic "1": $V_{AH} \geq 2.4V$

Logic "0": $V_{AL} \leq 0.8V$

NOTE: All typical values have been characterized but are not tested.



Logic Interface and Level Shifter



Decoder and Switch

Figure 3: Schematic Diagrams

Minimum Input Timing Requirements					
Symbol	**Parameter**	**Measured Terminal**	**Min. Limits over Full Temp. Range**	**Units**	**Test Circuit**
t_{WW}	WRITE Pulse Width	$\overline{WR}$	300	ns	See Figure 4
t_{DW}	A, EN Data Valid to WRITE (Stabilization Time)	A_0, A_1, (A_2), EN, $\overline{WR}$	180		
t_{WD}	A, EN Data Valid after WRITE (Hold Time)	A_0, A_1, (A_2), EN, $\overline{WR}$	30		
$t_{\overline{RS}}$	RESET Pulse Width (Note 6)	$\overline{RS}$	500		See Figure 5 V_S = 5V

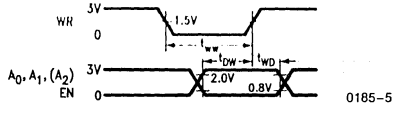


Figure 4: $\overline{WR}$ Timing Waveforms

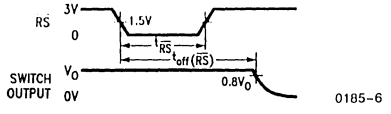


Figure 5: $\overline{RS}$ Timing Waveforms

8

NOTE: All typical values have been characterized but are not tested.

SWITCHING INFORMATION

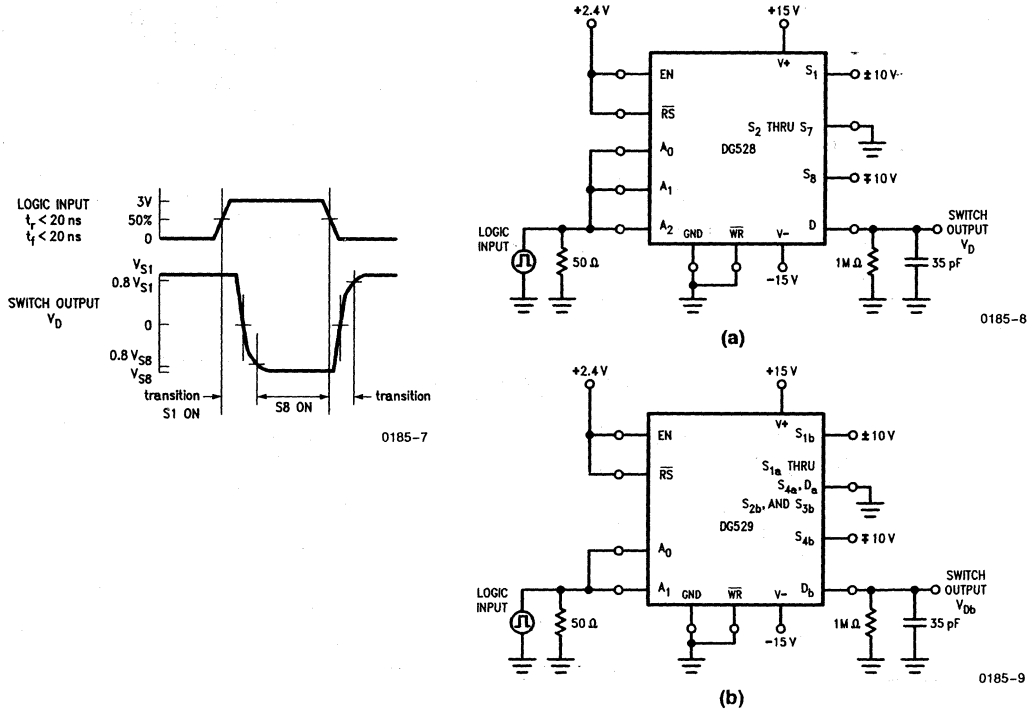


Figure 6: $t_{transition}$ Switching Time Test Circuit and Waveforms

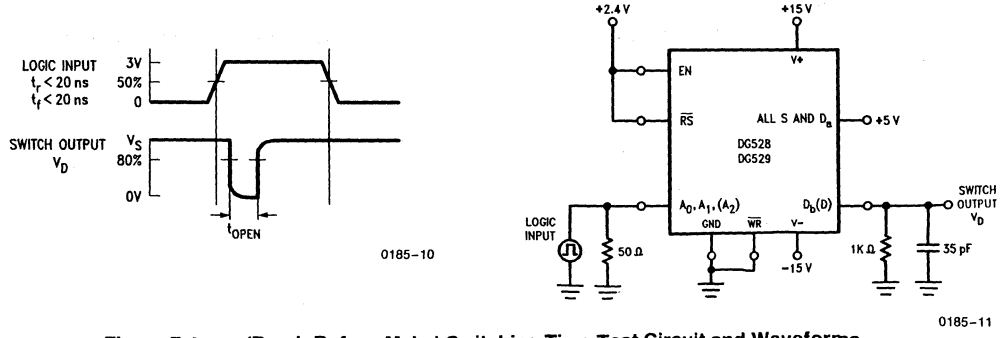


Figure 7: t_{open} (Break-Before-Make) Switching Time Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

SWITCHING INFORMATION (Continued)

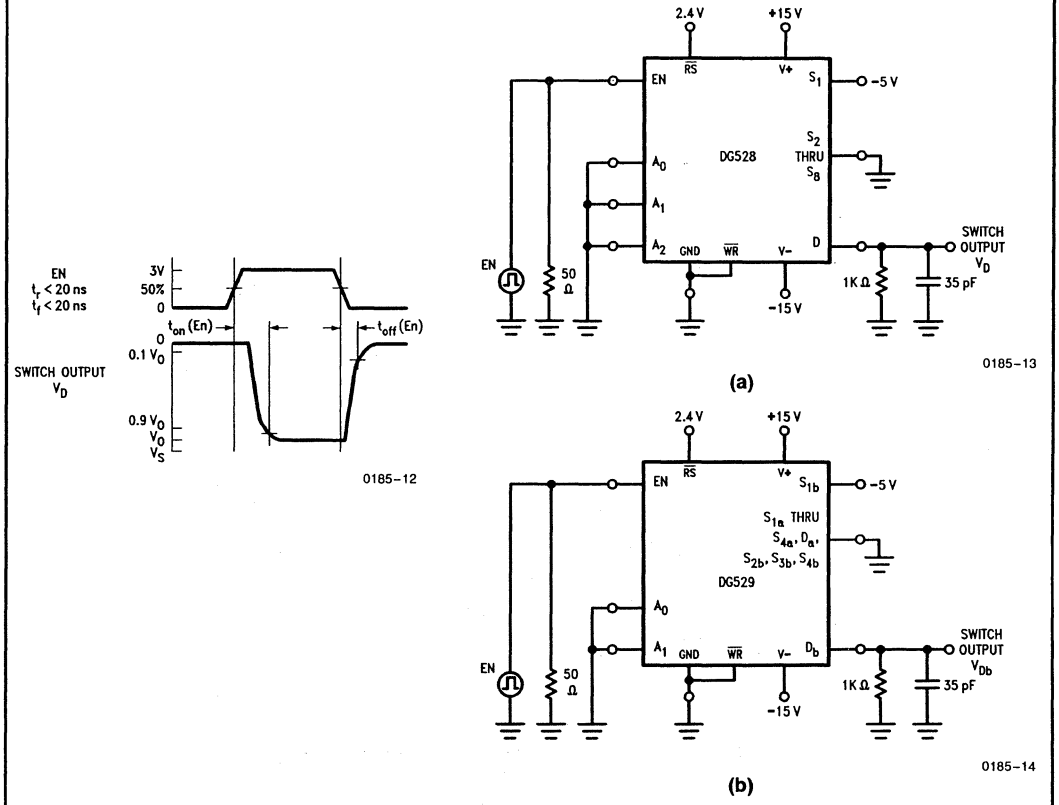


Figure 8: Enable t_{ON} and t_{OFF} Switching Time Test Circuit and Waveforms

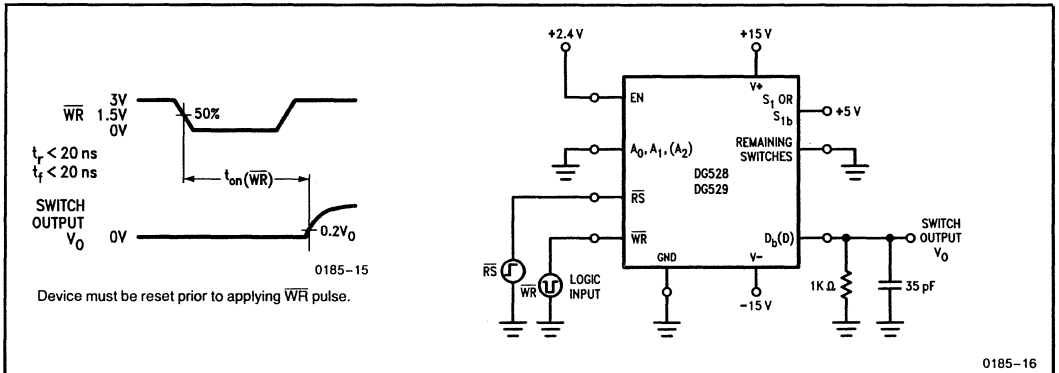


Figure 9: Write t_{ON} Switching Time Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

SWITCHING INFORMATION (Continued)

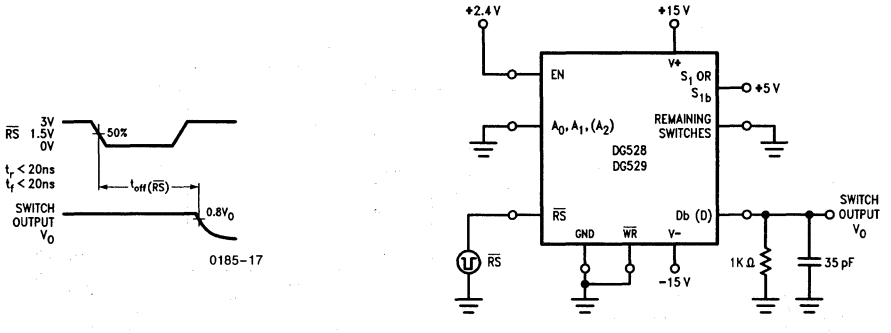
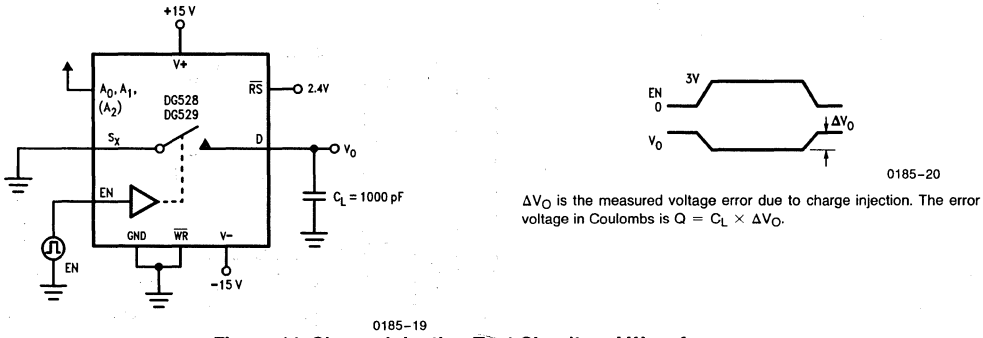


Figure 10: Reset t_{OFF} Switching Time Test Circuit and Waveforms



ΔV_O is the measured voltage error due to charge injection. The error voltage in Coulombs is $Q = C_L \times \Delta V_O$.

Figure 11: Charge Injection Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

SWITCHING INFORMATION (Continued)

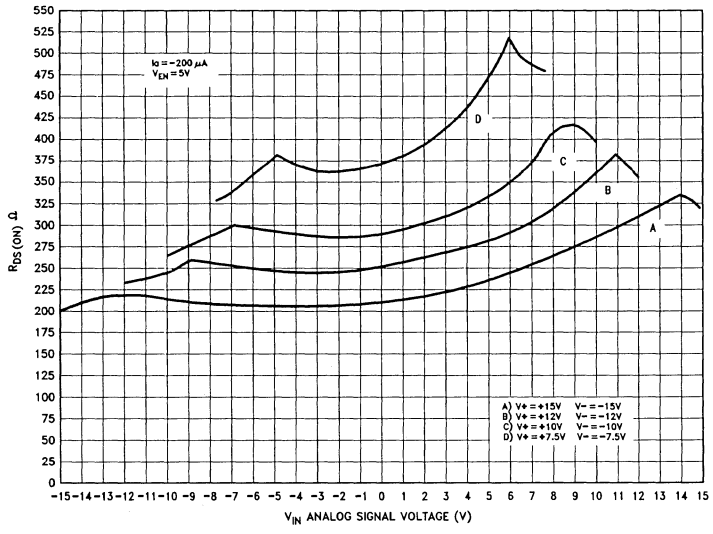


Figure 12: $R_{DS(ON)}$ vs Analog Signal Voltage vs Supply Voltage

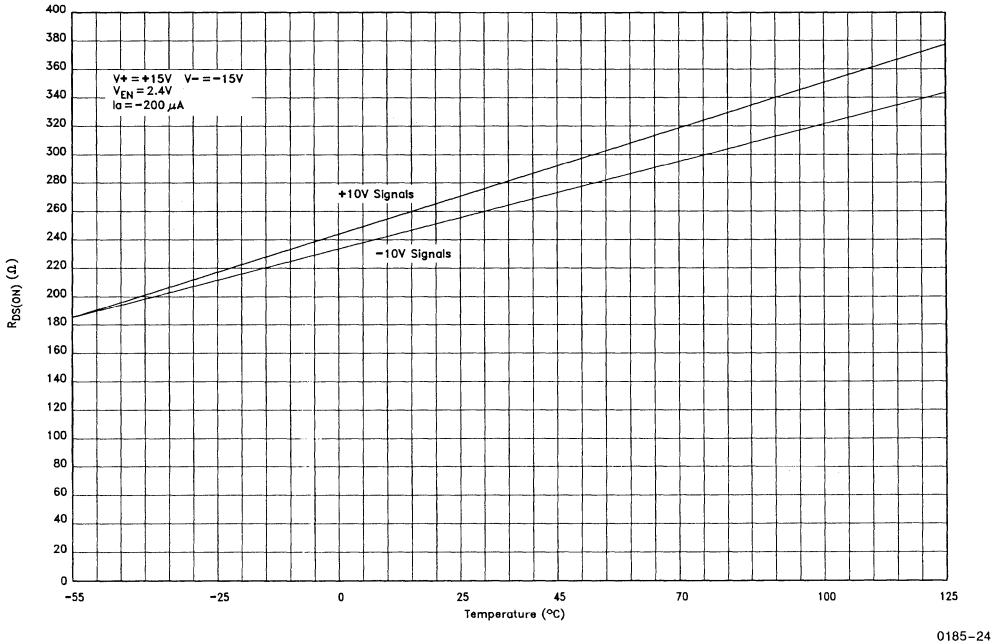


Figure 13: Typical $R_{DS(ON)}$ Variation with Temperature

NOTE: All typical values have been characterized but are not tested.

HARRIS

HI-1818A/1828A

Low Resistance Single 8/Differential 4 Channel CMOS Analog Multiplexers

Features

- Signal Range ..... ±15V
- "ON" Resistance (Typ.) 250Ω
- Input Leakage (Max) 50nA
- Access Time (Typ.) 350ns
- Power Consumption (Typ.) 5mW
- DTL/TTL Compatible Address
- -55°C to +125°C Operation

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Demultiplexing
- Selector Switch

Description

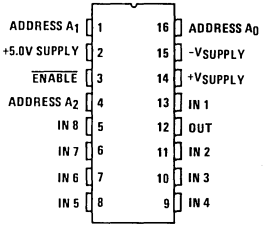
The HI-1818A/1828A are monolithic high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit (enable) input for disabling all channels. Dielectric Isolation (DI) processing is used for enhanced reliability and performance (see Application Note 521). Substrate leakage and parasitic capacitance are much lower, resulting in extremely low static errors and high throughput rates. Low output leakage (typically 0.1nA) and low channel ON resistance (250Ω) assure optimum performance in low level or current mode applications.

The HI-1818A is a single-ended 8 channel multiplexer, while the HI-1828A is a differential 4 channel version. Either device is ideally suited for medical instrumentation, telemetry systems, and microprocessor based data acquisition systems.

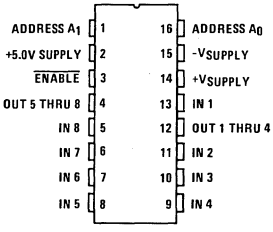
The HI-1818A/1828A is offered in a 16 pin Ceramic or Plastic DIP and a 20 pin Plastic Leaded Chip Carrier (PLCC). For MIL-STD-883 compliant parts, request the HI-1818A/883; HI-1828A/883 data sheet.

Pinouts

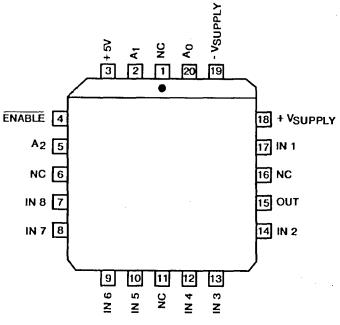
HI-1818A CERAMIC/PLASTIC DIP
TOP VIEW



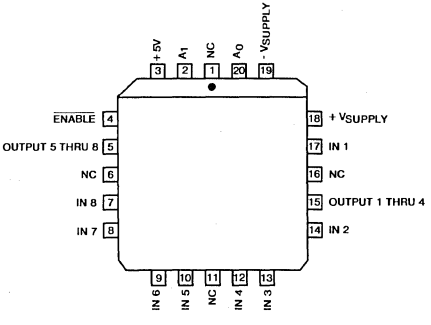
HI-1828A CERAMIC/PLASTIC DIP
TOP VIEW



HI-1818A PLASTIC LEADED CHIP CARRIER
TOP VIEW



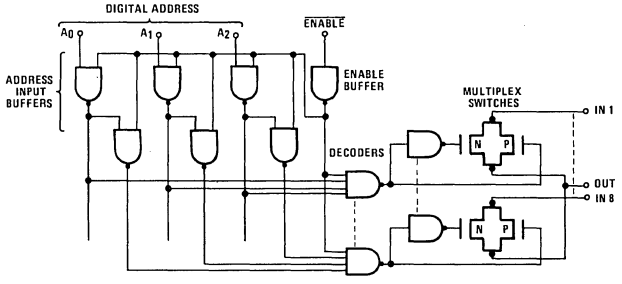
HI-1828A PLASTIC LEADED CHIP CARRIER
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Functional Diagrams

HI-1818A

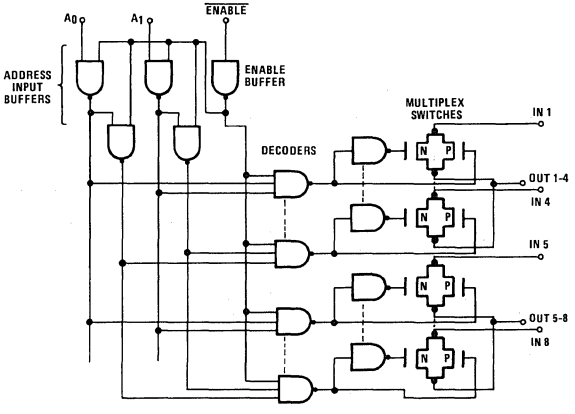


TRUTH TABLES

HI-1818A

ADDRESS A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
L	L	L	L	1
L	L	H	L	2
L	H	L	L	3
L	H	H	L	4
H	L	L	L	5
H	L	H	L	6
H	H	L	L	7
H	H	H	L	8
X	X	X	H	NONE

HI-1828A



HI-1828A

ADDRESS A_1	A_0	$\overline{EN}$	"ON" CHANNELS
L	L	L	1 and 5
L	H	L	2 and 6
H	L	L	3 and 7
H	H	L	4 and 8
X	X	H	NONE

Die Characteristics

Transistor Count 210

Die Dimensions ..... 67.7 x 103.5 mils

Substrate Potential* ..... $-V_{SUPPLY}$

Process: ..... CMOS-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	111	41
Plastic DIP	81	33

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Specifications HI-1818A/1828A

Absolute Maximum Ratings (Note 1)

Voltage Between Supply Pins 40.0V
Logic Supply Voltage 30.0V
Analog Input Voltage:
$+V_{IN}$ ..... $+V_{SUPPLY}$ +2V
$-V_{IN}$ ..... $-V_{SUPPLY}$ -2V
Junction Temperature (Max) ..... 175°C
Storage Temperature Range ..... -65°C to +150°C
Digital Input Voltage ..... $-V_{SUPPLY}$ to $+V_{SUPPLY}$
Operating Temperature Ranges:
HI-1818A/1828A-2, -8 ..... -55°C to +125°C
HI-1818A/1828A-5 ..... 0°C to 75°C

Electrical Specifications

Unless Otherwise Specified: Supplies = +15V, -15V, +5V; V_{AL} = 0.4V, V_{AH} = 4.0V

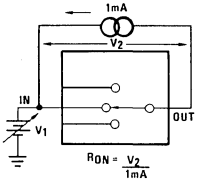
PARAMETER	TEMP	HI-1818A/1828A -2, -8 MIN	HI-1818A/1828A -2, -8 TYP	HI-1818A/1828A -2, -8 MAX	HI-1818A/1828A -5 MIN	HI-1818A/1828A -5 TYP	HI-1818A/1828A -5 MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_{IN}, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, ON Resistance (Note 2)	+25°C		250	400		250	400	Ω
	Full			500			500	Ω
*I_S(OFF), Input Leakage Current	Full			50			50	nA
*I_D(ON), On Channel Leakage Current								
(HI-1818A)	Full			250			250	nA
(HI-1828A)	Full			125			125	nA
I_D(OFF) Output Leakage Current								
(HI-1818A)	Full			250			250	nA
(HI-1828A)	Full			125			125	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.4			0.4	V
V_{AH}, Input High Threshold (Note 3)	Full	4.0			4.0			V
I_A, Input Leakage Current	Full			1			1	μA
SWITCHING CHARACTERISTICS								
T_S, Access Time (Note 4)	+25°C		350	500		350		ns
	Full			1000			1000	ns
Break-Before-Make Delay	+25°C		25			100		ns
Settling Time (0.1%)	+25°C		1.08			1.08		μs
(0.025%)	+25°C		2.8			2.8		μs
C_{IN}, Channel Input Capacitance	+25°C		4			4		pF
C_{OUT}, Channel Output Capacitance								
(HI-1818A)	+25°C		20			20		pF
(HI-1828A)	+25°C		10			10		pF
C_{DS}(OFF), Drain-To-Source Capacitance	+25°C		0.6			0.6		pF
C_D, Digital Input Capacitance	+25°C		5			5		pF
t_{ON}(EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
t_{OFF}(EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
POWER REQUIREMENTS								
P_D, Power Dissipation	Full			27.5			27.5	mW
*I+, Current	Full			0.5			0.5	mA
*I-, Current	Full			1			1	mA
*I_L, Current	Full			1			1	mA

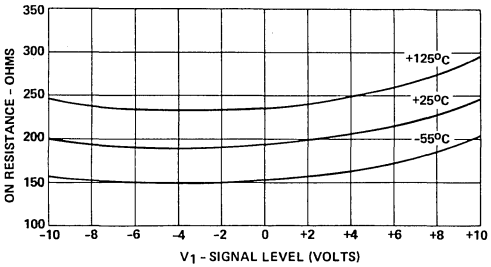
*100% Tested for Dash 8. Leakage currents not tested at -55°C.

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = -1mA.
3. To drive from DTL/TTL circuits, 1kΩ pull-up resistors to +5.0V supply are recommended.
4. Time measured to 90% of final output level; V_{OUT} = -5.0V to +5.0V, Digital Inputs = 0V to +4.0V.

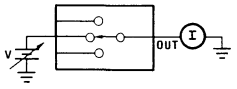
Performance Characteristics

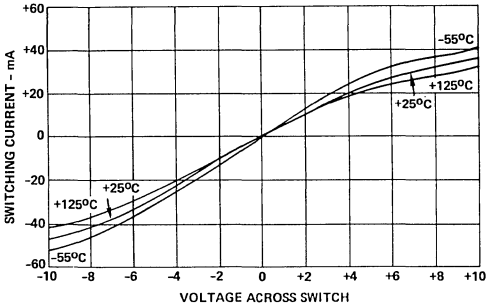
ON RESISTANCE vs. ANALOG SIGNAL LEVEL





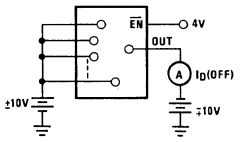
ON CHANNEL CURRENT vs. VOLTAGE

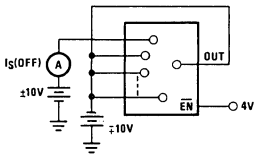




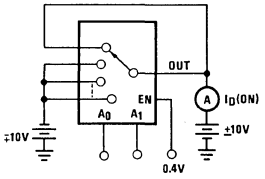
LEAKAGE CURRENTS vs. TEMPERATURE *

OFF LEAKAGE

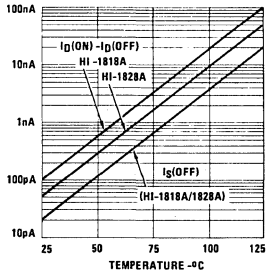




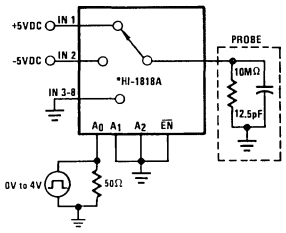
ON LEAKAGE



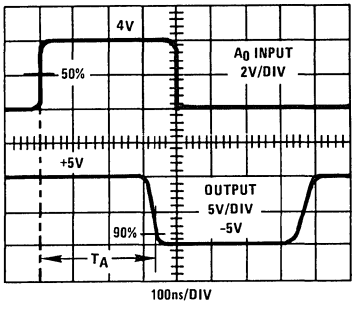
*Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for $I_{D(OFF)}$: +10V/-10V and -10V/+10V).



ACCESS TIME

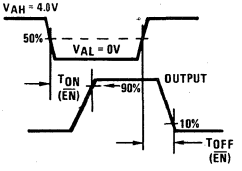


*Similar connection for HI-1828A.

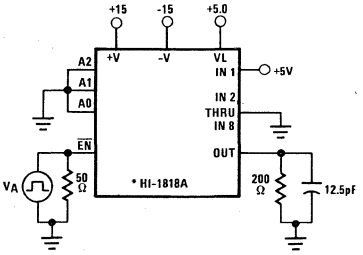


Switching Waveforms

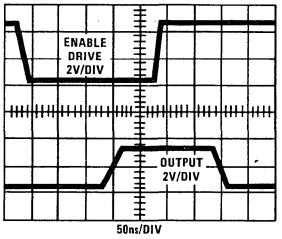
ENABLE DRIVE



ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

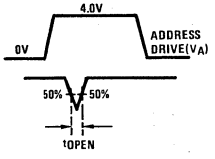


ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

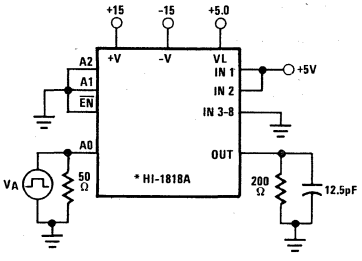


*Similar Connection For HI-1828A

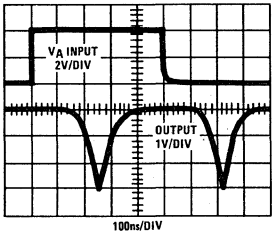
ADDRESS DRIVE



BREAK-BEFORE-MAKE DELAY (t_{OPEN})



BREAK-BEFORE-MAKE DELAY (t_{OPEN})



*Similar Connection For HI-1828A

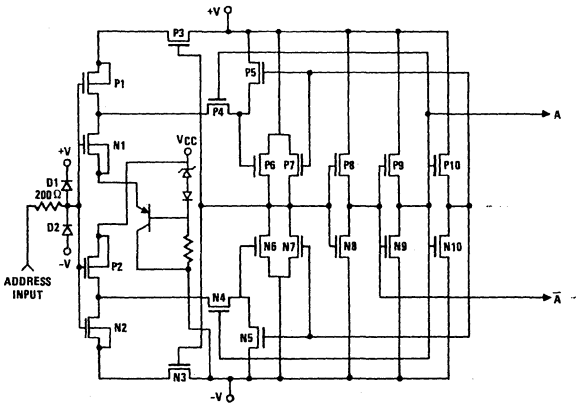
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI3-1818A-5	0°C to +75°C	16-Pin Plastic DIP
HI1-1818A-2	-55°C to +125°C	16-Pin CERDIP
HI1-1818A-5	0°C to +75°C	16-Pin CERDIP
HI1-1818A-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP
HI4P1818A-5	0°C to +75°C	20-Pin PLCC
HI1-1828A-5	0°C to +75°C	16-Pin CERDIP
HI1-1828A-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP
HI3-1828A-5	0°C to +75°C	16-Pin Plastic DIP
HI4P1828A-5	0°C to +75°C	20-Pin PLCC
HI1-1828A-2	-55°C to +125°C	16-Pin CERDIP

Schematic Diagrams

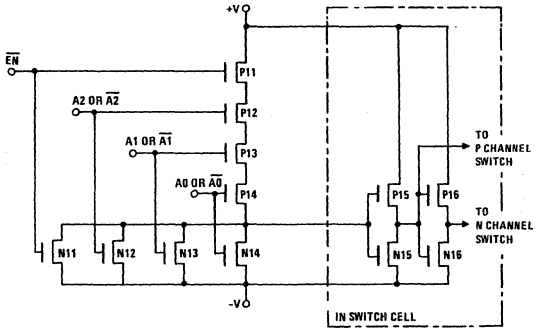
ADDRESS INPUT BUFFER

All N-Channel Bodies to V-
All P-Channel Bodies to V+
Unless Otherwise Indicated



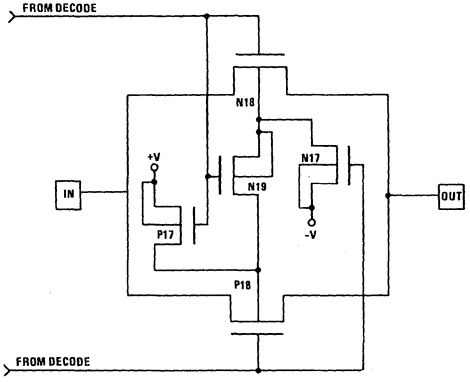
ADDRESS DECODER

All N-Channel Bodies to V-
All P-Channel Bodies to V+
A_2 or $\overline{A_2}$ not used for HI-1828A



MULTIPLEXER SWITCH

All N-Channel Bodies to V-
All P-Channel Bodies to V+
Unless Otherwise Indicated



HARRIS

HI-506/507

Single 16/Differential 8 Channel CMOS Analog Multiplexers

Features

- Low On Resistance (Typ.) 180Ω
- Wide Analog Signal Range ..... ±15V
- TTL/CMOS Compatible ... 2.4V (Logic "1")
- Access Time (Typ) 250ns
- 44V Maximum Power Supply
- Break-Before-Make Switching
- No Latch-up
- Replaces DG506A/DG506AA and DG507A/DG507AA

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Demultiplexing
- Selector Switch

Description

These monolithic CMOS multiplexers each include an array of sixteen analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latch-up. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS (See Application Note 521). With the low ON resistance (180Ω typical), this allows low static error, fast channel switching rates, and fast settling.

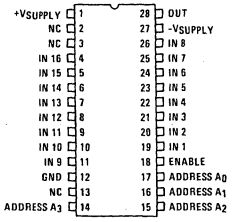
The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for "1" and maximum 0.8V for "0". This allows direct interface without pull-up resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and diode clamp to each supply.

The HI-506 is a sixteen channel single-ended multiplexer, and the HI-507 is an eight channel differential version. Each device is available in a 28 pin Ceramic or Plastic DIP, 28 pad Leadless Chip Carrier (LCC), and 28 pin Plastic Leaded Chip Carrier (PLCC) packages. If input overvoltage protection is needed, the HI-546/547 multiplexers are recommended. For further information see Application Notes 520 and 521.

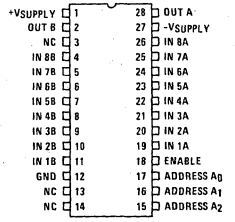
The HI-506/507 is offered in both commercial and military grades. For additional Hi-Rel screening including 160 hour burn-in specify the "-8" suffix. For MIL-STD-883 compliant parts, request the HI-506/883 or HI-507/883 data sheet.

Pinouts

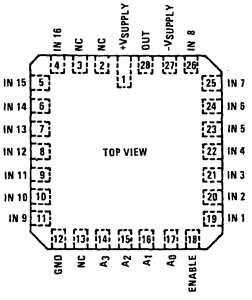
HI1-506 (CERAMIC DIP)
HI3-506 (PLASTIC DIP)
TOP VIEW



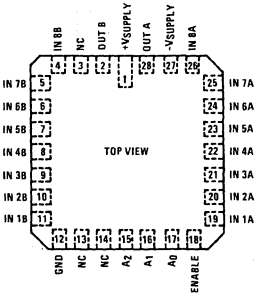
HI1-507 (CERAMIC DIP)
HI3-507 (PLASTIC DIP)
TOP VIEW



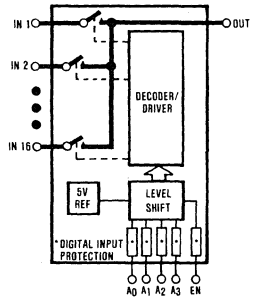
HI4-506 (CERAMIC LCC)
HI4P506 (PLCC)
TOP VIEW



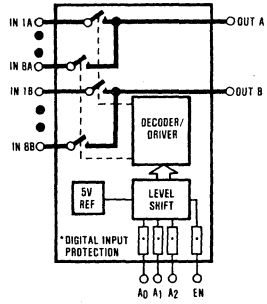
HI4-507 (CERAMIC LCC)
HI4P507 (PLCC)
TOP VIEW



Functional Diagrams



HI-506



HI-507

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ 44V
$V_{SUPPLY(+)}$ to GND 22V
$V_{SUPPLY(-)}$ to GND 25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first
Analog Signal Overvoltage (Note 7)
$+V_S$ ..... $+V_{SUPPLY}$ +2V
$-V_S$ ..... $-V_{SUPPLY}$ -2V
Continuous Current, S or D: 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% duty cycle max): 40mA
Junction Temperature ..... +175°C
Operating Temperature Ranges:
HI-506/507-2, -8 ..... -55°C to +125°C
HI-506/507-4 ..... -25°C to +85°C
HI-506/507-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications Unless Otherwise Specified:

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V;
V_{AL} (Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-506/HI-507 -2, -8 MIN.	TYP.	MAX.	HI-506/507 -4, -5 MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		180	300		180	400	Ω
	Full			400			500	Ω
ΔR_{ON}, (Any Two Channels)	+25°C		5			5		%
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.3			0.3		nA
HI-506	Full			300			300	nA
HI-507	Full			200			200	nA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.3			0.3		nA
HI-506	Full			300			300	nA
HI-507	Full			200			200	nA
*I_{DIFF}, Differential Off Output Leakage Current (HI-507 Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold	Full			+0.8			+0.8	V
*V_{AH}, Input High Threshold	Full	+2.4			+2.4			V
*I_A, Input Leakage Current (High or Low) (Note 4)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		250	500		250		ns
	Full			1000			1000	ns
*t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
*t_{ON} (EN), Enable Delay (ON)	+25°C		250	500		250		ns
	Full			1000			1000	ns
*t_{OFF} (EN), Enable Delay (OFF)	+25°C		250	500		250		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.01%)	+25°C		2.4			2.4		μs
"Off Isolation" (Note 5)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-506	+25°C		44			44		pF
HI-507	+25°C		22			22		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.08			0.08		pF
POWER REQUIREMENTS								
*I+, Current, Pin 1 (Note 6)	Full		1.5	3.0		1.5	3.0	mA
*I-, Current Pin 27 (Note 6)	Full		0.4	1.0		0.4	1.0	mA

*100% tested for Dash 8. Leakage currents not tested at -55°C.

TRUTH TABLES

HI-506

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = -1mA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
5. V_{EN} = 0.8V, R_L = 1K, C_L = 15pF, V_S = $7V_{RMS}$, f = 100kHz.
6. V_{EN}, V_A = 0V or 2.4V.
7. Signal voltage at any analog input or output (S or D) will be clamped to the supply rail by internal diodes. Limit the resulting current as shown under absolute maximum ratings. If an overvoltage condition is anticipated (analog input exceeds either power supply voltage), the Harris HI-546/547 multiplexers are recommended.

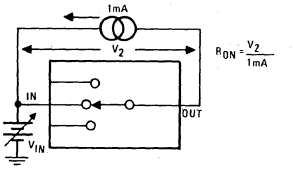
8

Performance Characteristics and Test Circuits

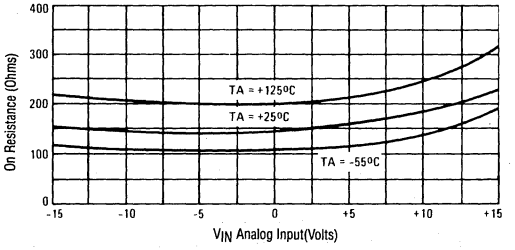
Unless Otherwise Specified; T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = 2.4 V, V_{AL} = 0.8 V.

ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

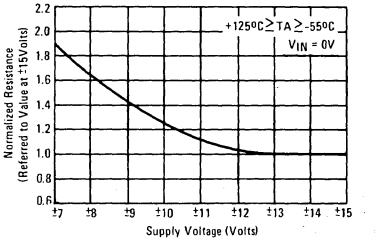
TEST CIRCUIT NO. 1



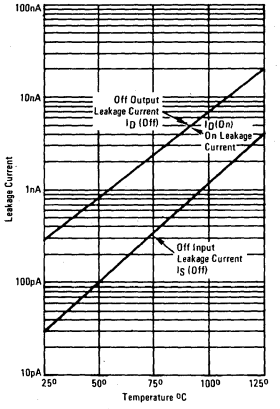
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



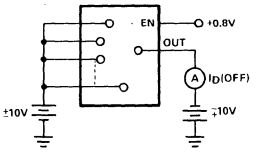
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



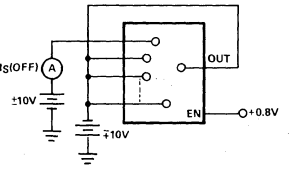
LEAKAGE CURRENT VS. TEMPERATURE



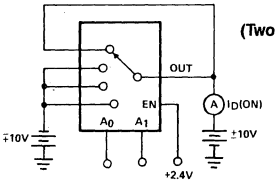
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

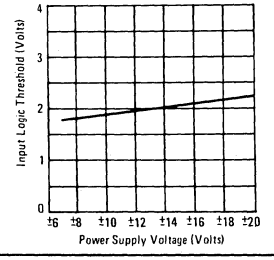


TEST CIRCUIT NO. 4*

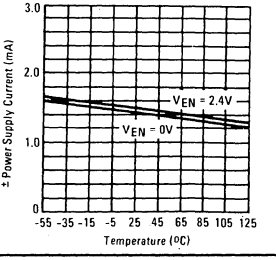


***Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for $I_{D(OFF)}$ +10 V/−10 V and −10 V/+10 V.)**

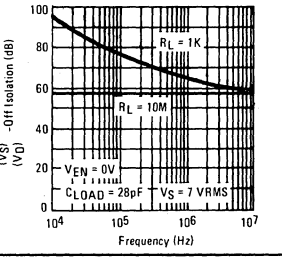
LOGIC THRESHOLD vs. POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT vs. TEMPERATURE

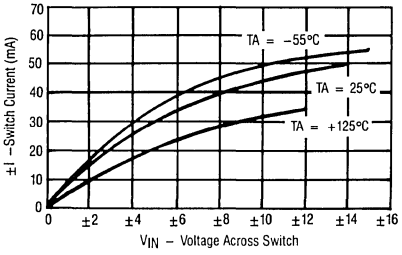


OFF ISOLATION vs. FREQUENCY



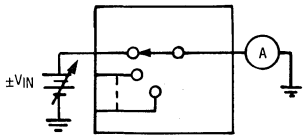
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

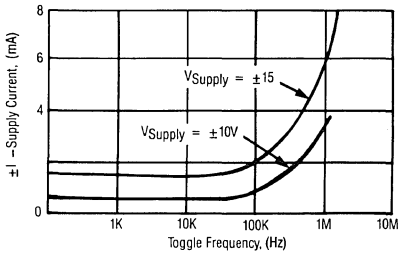


TEST CIRCUIT NO. 5

ON CHANNEL CURRENT vs. VOLTAGE

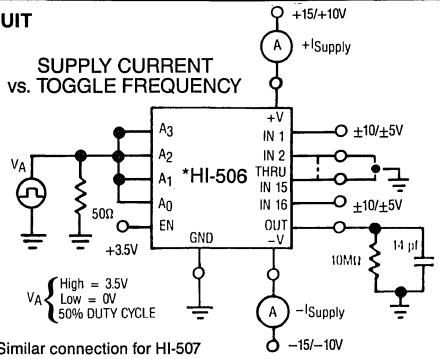


SUPPLY CURRENT vs. TOGGLE FREQUENCY



TEST CIRCUIT NO. 6

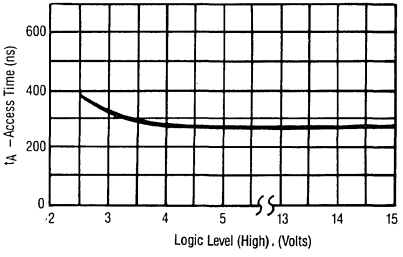
SUPPLY CURRENT vs. TOGGLE FREQUENCY



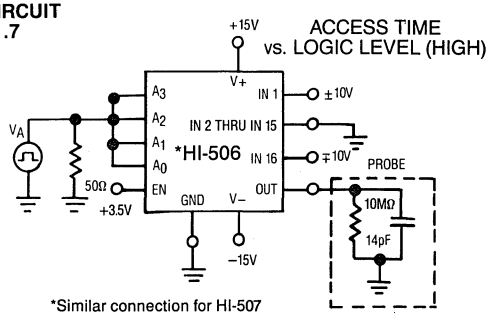
*Similar connection for HI-507

TEST CIRCUIT NO .7

ACCESS TIME VS. LOGIC LEVEL (HIGH)

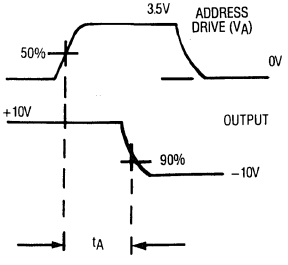


ACCESS TIME vs. LOGIC LEVEL (HIGH)

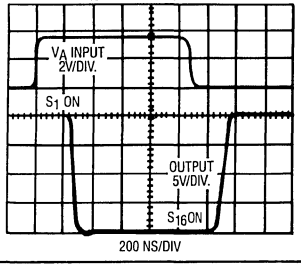


*Similar connection for HI-507

Switching Waveforms



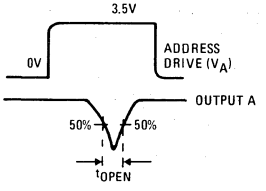
ACCESS TIME

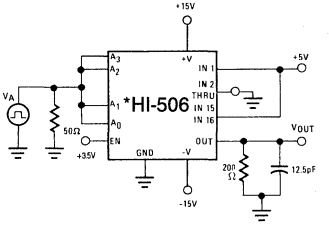


Switching Waveforms (continued)

TEST CIRCUIT NO. 8

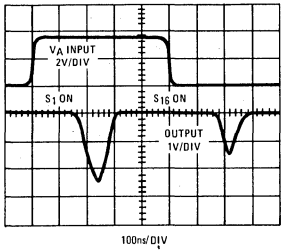
BREAK-BEFORE-MAKE DELAY (t_{OPEN})





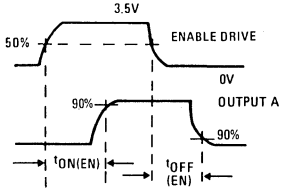
*Similar connection for HI-507

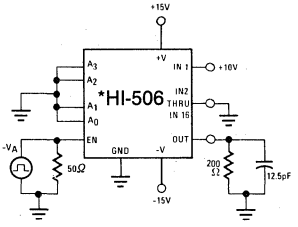
BREAK-BEFORE-MAKE DELAY(t_{OPEN})



TEST CIRCUIT NO. 9

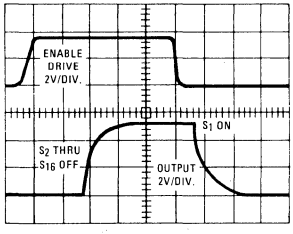
ENABLE DELAY $t_{ON(EN)}$,$t_{OFF(EN)}$





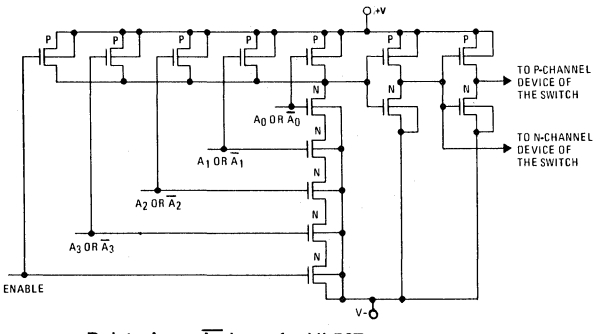
*Similar connection for HI-507

ENABLE DELAY $t_{ON(EN)}$,$t_{OFF(EN)}$



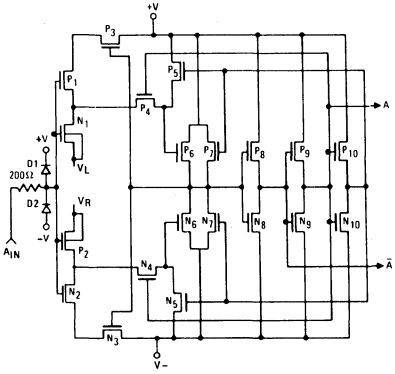
Schematic Diagrams

ADDRESS DECODER



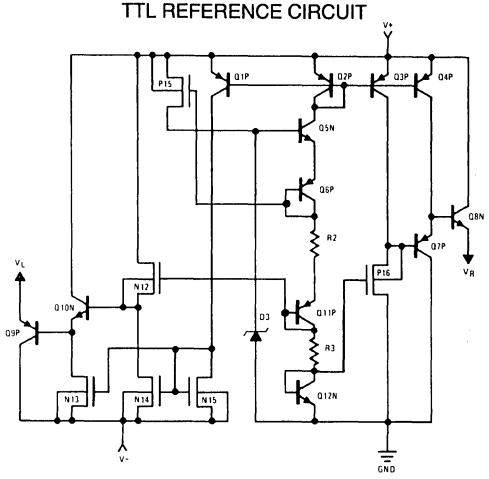
Delete A_3 or $\overline{A_3}$ Input for HI-507

ADDRESS INPUT BUFFER LEVER SHIFTER

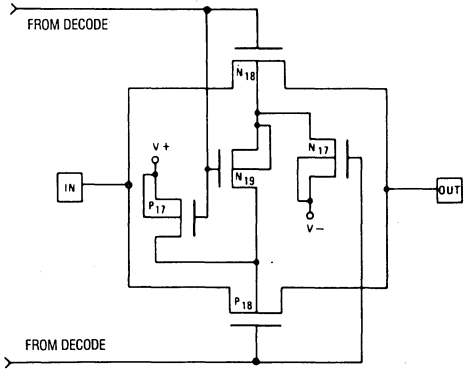


All N-Channel Bodies to V–
All P-Channel Bodies to V+
Unless Otherwise Indicated

TTL REFERENCE CIRCUIT



MULTIPLEX SWITCH



Die Characteristics

Transistor Count		421
Die Dimensions		129 x 82 mils
Substrate Potential*		$-V_{SUPPLY}$
Process		CMOS-DI
Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	51	20
Ceramic LCC	81	40

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI9P0506-9	-40°C to +85°C	28-Pin SOIC
HI3-0506-5	0°C to +75°C	28-Pin Plastic DIP
HI1-0506-7	0°C to +75°C + 96 Hr. Burn-In	28-Pin CERDIP
HI9P0506-5	0°C to +75°C	28-Pin SOIC
HI4P0506-5	0°C to +75°C	28-Pin PLCC
HI1-0506-5	0°C to +75°C	28-Pin CERDIP
HI1-0506-4	-25°C to +85°C	28-Pin CERDIP
HI1-0506-2	-55°C to +125°C	28-Pin CERDIP
HI1-0507-4	-25°C to +85°C	28-Pin CERDIP
HI4P0507-5	0°C to +75°C	28-Pin PLCC
HI9P0507-5	0°C to +75°C	28-Pin SOIC
HI1-0507-5	0°C to +75°C	28-Pin CERDIP
HI3-0507-5	0°C to +75°C	28-Pin Plastic DIP
HI1-0507-7	0°C to +75°C + 96 Hr. Burn-In	28-Pin CERDIP
HI9P0507-9	-40°C to +85°C	28-Pin SOIC
HI1-0507-2	-55°C to +125°C	28-Pin CERDIP

HARRIS HI-506A/507A

Single 16/Differential 8 Channel CMOS Analog Multiplexers with Active Overvoltage Protection

Features

- Analog Overvoltage Protection... $70V_{p-p}$
- No Channel Interaction During Overvoltage
- ESD Resistant..... >4,000V
- 44V Maximum Power Supply
- Fail Safe with Power Loss (No Latch-Up)
- Break-Before-Make Switching
- Analog Signal Range ..... ±15V
- Access Time (Typical) 500ns
- Standby Power (Typical) 7.5mW

Applications

- Data Acquisition
- Industrial Controls
- Telemetry

Description

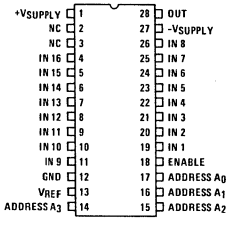
The HI-506A and HI-507A are analog multiplexers with Active Overvoltage Protection. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. Digital inputs will also sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-506A and HI-507A ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The HI-506A is a 16 channel device and the HI-507A is an 8 channel differential version. If input overvoltage protection is not needed, the HI-506 and HI-507 multiplexers are recommended. For further information see Application Notes 520 and 521.

Each device is available in a 28 pin Plastic or Ceramic DIP and a 28 pad Ceramic LCC package.

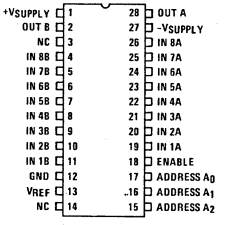
The HI-506A/507A are offered in both commercial and military grades. Additional Hi-Rel screening including 160 hour burn-in is specified by the "-8" suffix. For MIL-STD-883 compliant parts, request the HI-546/883 or HI-547/883 data sheets.

Pinouts

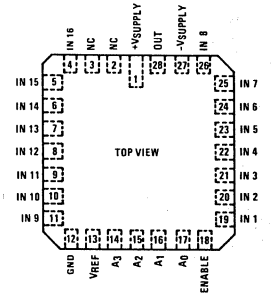
HI1-506A (CERAMIC DIP)
HI3-506A (PLASTIC DIP)
TOP VIEW



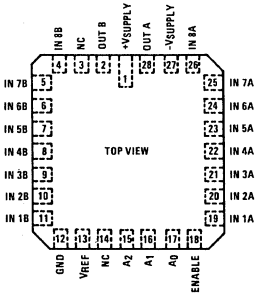
HI1-507A (CERAMIC DIP)
HI3-507A (PLASTIC DIP)
TOP VIEW



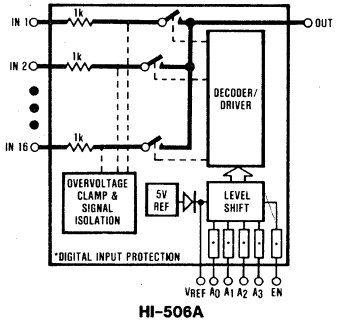
HI4-506A (CERAMIC LCC)
TOP VIEW



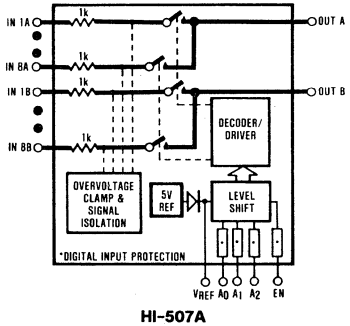
HI4-507A (CERAMIC LCC)
TOP VIEW



Functional Diagrams



HI-506A



HI-507A

CAUTION:- These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ 44V
$V_{SUPPLY(+)}$ to GND 22V
$V_{SUPPLY(-)}$ to GND 25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first
Analog Signal Overvoltage
$+V_S$ ..... $+V_{SUPPLY}$ +20V
$-V_S$ ..... $-V_{SUPPLY}$ -20V
Continuous Current, S or D: 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% duty cycle max): 40mA
Junction Temperature ..... +175°C
Operating Temperature Ranges:
HI-506A/507A-2, -8 ..... -55°C to +125°C
HI-506A/507A-4 ..... -25°C to +85°C
HI-506A/507A-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications Unless Otherwise Specified:

Supplies = +15V, -15V; V_{REF} pin = Open; V_{AH} (Logic Level High) = +4.0V;
V_{AL} (Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-506A/HI-507A -2, -8 MIN.	TYP.	MAX.	HI-506A/507A -4, -5 MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		1.2	1.5		1.5	1.8	kΩ
	Full		1.5	1.8		1.8	2.0	kΩ
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-506A	Full			300			300	nA
HI-507A	Full			200			200	nA
*I_D (OFF), with Input Overvoltage Applied (Note 4)	+25°C		4.0			4.0		nA
	Full			2.0				μA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-506A	Full			300			300	nA
HI-507A	Full			200			200	nA
I_{DIFF}, Differential Off Output Leakage Current (HI-507A Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold TTL Drive	Full			0.8			0.8	V
*V_{AH}, Input High Threshold (Note 8)	Full	4.0			4.0			V
V_{AL} MOS Drive (Note 9)	+25°C			0.8			0.8	V
V_{AH} MOS Drive (Note 9)	+25°C	6.0			6.0			V
*I_A, Input Leakage Current (High or Low) (Note 5)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		0.5			0.5		μs
	Full			1.0			1.0	μs
*t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
*t_{ON} (EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
*t_{OFF} (EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.01%)	+25°C		3.5			3.5		μs
"Off Isolation" (Note 6)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-506A	+25°C		50			50		pF
HI-507A	+25°C		25			25		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current Pin 1 (Note 7)	Full		0.5	2.0		0.5	2.0	mA
*I-, Current Pin 27 (Note 7)	Full		0.02	1.0		0.02	1.0	mA

*100% tested for Dash 8. Leakage currents not tested at -55°C.

TRUTH TABLES

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = -100 μA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Analog Overvoltage = ±33 V.
5. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1 nA at 25°C.
6. V_{EN} = 0.8 V, R_L = 1 K, C_L = 15 pF, V_S = 7 V_{RMS}, f = 100 kHz.
7. V_{EN}, V_A = 0 V or 4.0 V.
8. To drive from DTL/TTL Circuits, 1 kΩ pull-up resistors to +5.0 V supply are recommended.
9. V_{REF} = +10 V.

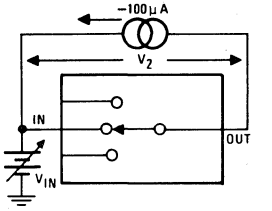
Performance Characteristics and Test Circuits

Unless Otherwise Specified: T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = +4 V, V_{AL} = 0.8 V And V_{Ref} = Open.

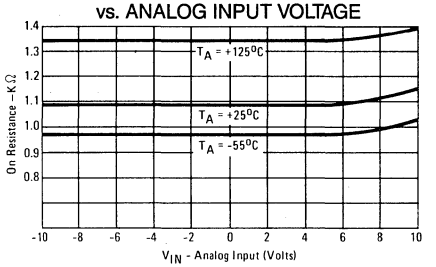
ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

$R_{ON} = \frac{V_2}{100\mu A}$

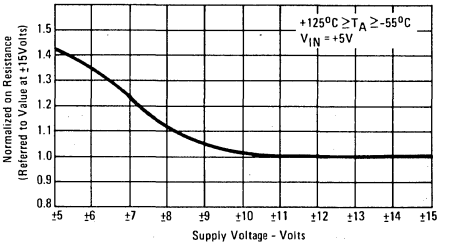
TEST CIRCUIT NO. 1



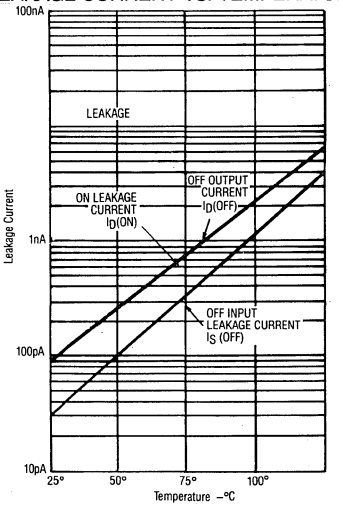
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



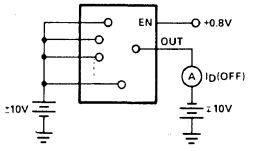
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



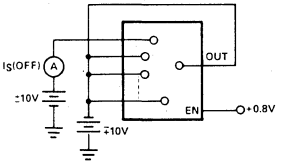
LEAKAGE CURRENT VS. TEMPERATURE



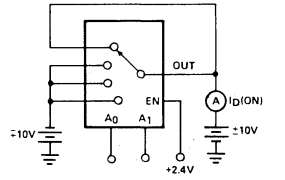
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

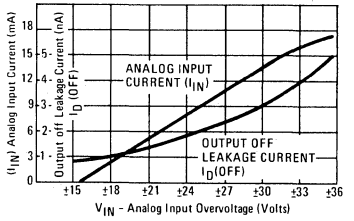


TEST CIRCUIT NO. 4*



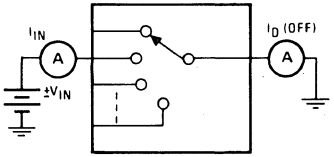
***Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for $I_{D(OFF)}$: +10 V/−10 V and −10 V/+10 V.)**

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



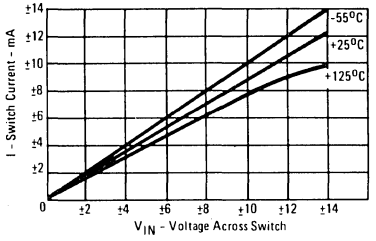
TEST CIRCUIT NO. 5

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



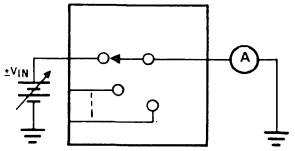
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

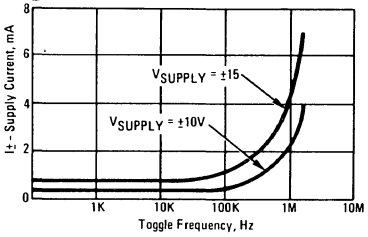


TEST CIRCUIT NO. 6

ON CHANNEL CURRENT vs. VOLTAGE

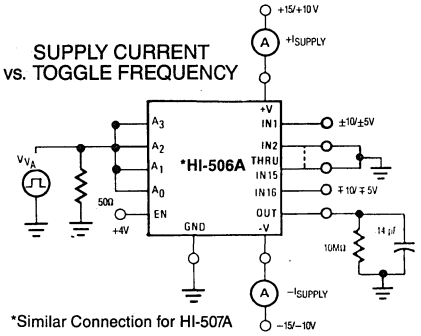


SUPPLY CURRENT vs. TOGGLE FREQUENCY



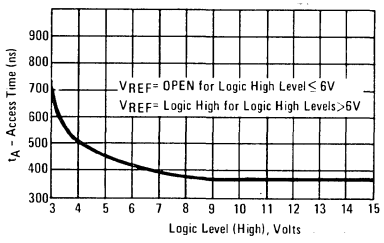
TEST CIRCUIT NO. 7

SUPPLY CURRENT vs. TOGGLE FREQUENCY



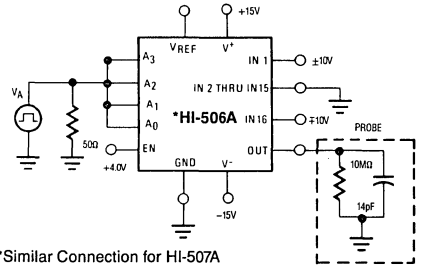
*Similar Connection for HI-507A

ACCESS TIME VS. LOGIC LEVEL (HIGH)



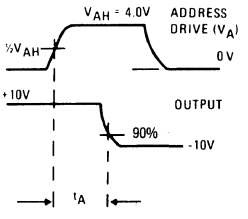
TEST CIRCUIT NO. 8

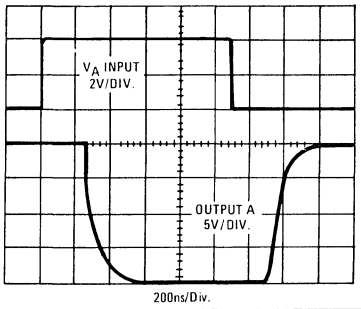
ACCESS TIME vs. LOGIC LEVEL (HIGH)



*Similar Connection for HI-507A

Switching Waveforms

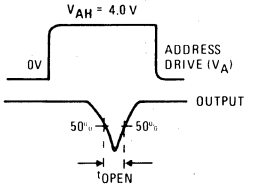


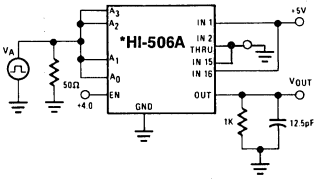


Switching Waveforms (continued)

TEST CIRCUIT NO. 9

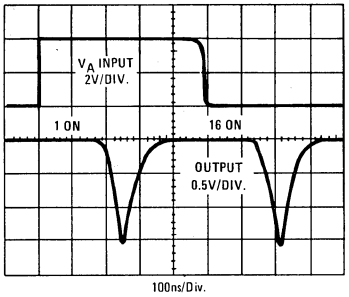
BREAK-BEFORE-MAKE DELAY (tOPEN)





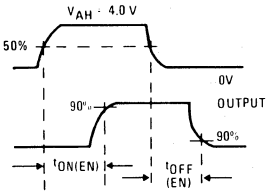
*Similar Connection for HI-507A

BREAK-BEFORE-MAKE DELAY(tOPEN)

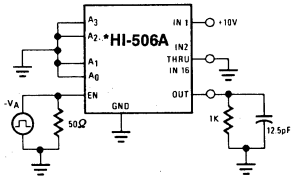


TEST CIRCUIT NO. 10

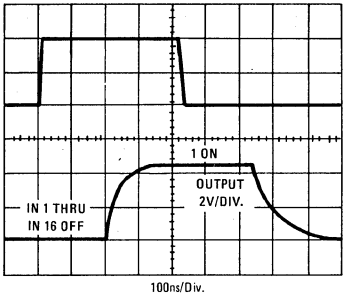
ENABLE DRIVE



ENABLE DELAY ($t_{ON(EN)}$,$t_{OFF(EN)}$)

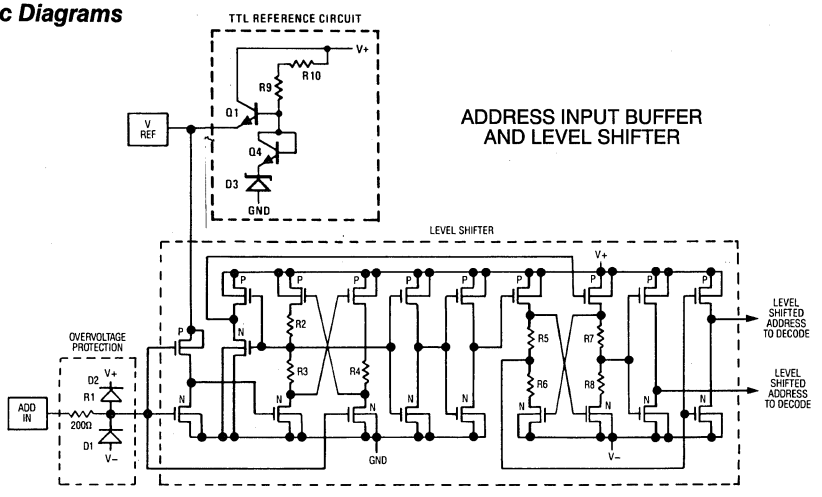


ENABLE DELAY ($t_{ON(EN)}$,$t_{OFF(EN)}$)

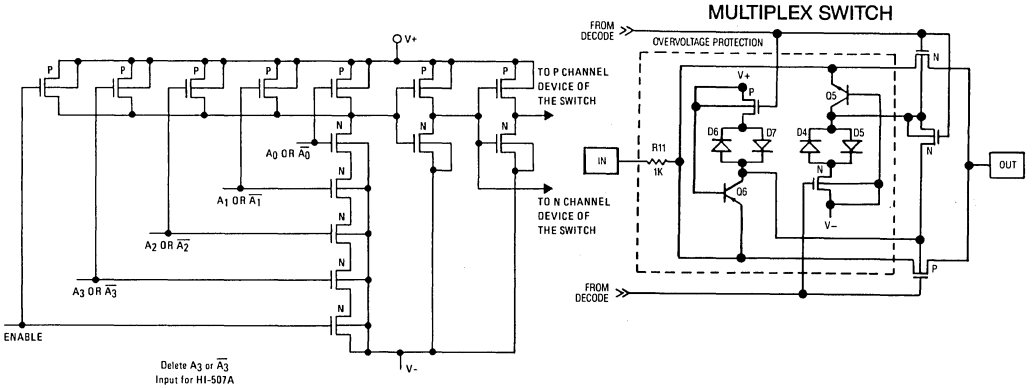


*Similar Connection for HI-507A

Schematic Diagrams



Schematic Diagrams (continued)



Die Characteristics

Transistor Count		485
Die Dimensions		159 x 84 mils
Substrate Potential*		$-V_{SUPPLY}$
Process		CMOS-DI
Thermal Constants ($^oC/W$)	θ_{ja}	θ_{jc}
Ceramic DIP	50	18
Ceramic LCC	81	40

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

HARRIS

HI-508/509

Single 8/Differential 4 Channel CMOS Analog Multiplexers

Features

- Low On Resistance (Typ)..... 180Ω
- Wide Analog Signal Range ..... ±15V
- TTL/CMOS Compatible ..... 2.4V (Logic "1")
- Fast Access 250ns
- Fast Settling (0.01%) 600ns
- 44V Maximum Power Supply
- Break-Before-Make Switching
- No Latch-Up
- Replaces DG508A/DG508AA and DG509A/DG509AA

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Demultiplexing
- Selector Switch

Description

These monolithic CMOS multiplexers each include an array of eight analog switches, a digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latch-up. Also, DI offers much lower substrate leakage and parasitic capacitance than conventional junction-isolated CMOS (see Application Note 521). Combined with the low ON resistance (180Ω typical), these benefits allow low static error, fast channel switching rates, and fast settling.

Switches are guaranteed to break-before-make, so that two channels are never shorted together.

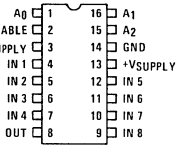
The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for "1" and maximum 0.8V for "0". This allows direct interface without pull-up resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and a diode clamp to each supply.

The HI-508 is an eight channel single-ended multiplexer, and the HI-509 is a four channel differential version. Each device is available in a 16 pin Plastic or Ceramic DIP, a 20 pin Plastic Leaded Chip Carrier (PLCC) or 20 pad Ceramic Leadless Chip Carrier (LCC). If input overvoltage protection is needed, the HI-548/549 multiplexers are recommended.

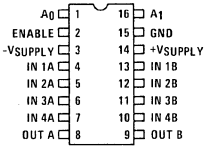
The HI-508/509 is offered in both commercial and military grades, suitable for spacecraft/military applications. For additional Hi-Rel screening including 160 hour burn-in, specify the "-8" suffix. For further information see Application Notes 520 and 521. For MIL-STD-883 compliant parts, request the HI-508/883 or HI-509/883 data sheets.

Pinouts

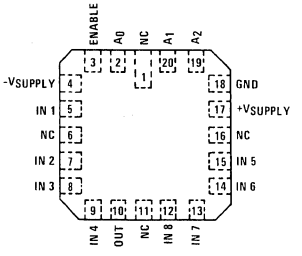
HI1-508 (CERAMIC DIP)
HI3-508 (PLASTIC DIP)
TOP VIEW



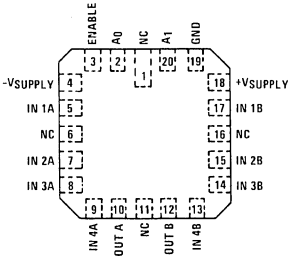
HI1-509 (CERAMIC DIP)
HI3-509 (PLASTIC DIP)
TOP VIEW



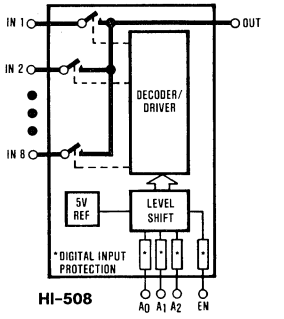
HI4-508 (CERAMIC LCC)
HI4P508 (PLCC)
TOP VIEW



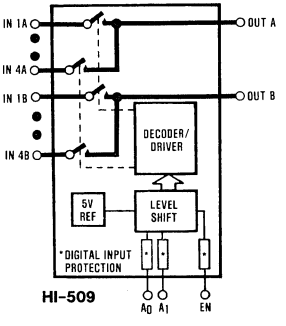
HI4-509 (CERAMIC LCC)
HI4P509 (PLCC)
TOP VIEW



Functional Diagrams



HI-508



HI-509

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ 44V
$V_{SUPPLY(+)}$ to GND 22V
$V_{SUPPLY(-)}$ to GND 25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first
Analog Signal Overvoltage (Note 7)
$+V_S$ ..... $+V_{SUPPLY}$ +2V
$-V_S$ ..... $-V_{SUPPLY}$ -2V
Continuous Current, S or D: 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% duty cycle max): 40mA
Junction Temperature ..... +175°C
Operating Temperature Ranges:
HI-508/509-2, -8 ..... -55°C to +125°C
HI-508/509-4 ..... -25°C to +85°C
HI-508/509-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications Unless Otherwise Specified:

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V;
V_{AL} (Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-508/HI-509 -2, -8 MIN.	TYP.	MAX.	HI-508/509 -4, -5 MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		180	300		180	400	Ω
	Full			400			500	Ω
$\triangle R_{ON}$, Any Two Channels	+25°C		5			5		%
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.3			0.3		nA
HI-508	Full			200			200	nA
HI-509	Full			100			100	nA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.3			0.3		nA
HI-508	Full			200			200	nA
HI-509	Full			100			100	nA
*I_{DIFF}, Differential Off Output Leakage Current (HI-509 Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold	Full			0.8			0.8	V
*V_{AH}, Input High Threshold	Full	2.4			2.4			V
*I_A, Input Leakage Current (High or Low) (Note 4)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		250	500		250		ns
	Full			1000			1000	ns
*t_{OPEN}, Break-Before-Make Interval	+25°C	25	80		25	80		ns
*t_{ON} (EN), Enable Turn-On	+25°C		250	500		250		ns
	Full			1000			1000	ns
*t_{OFF} (EN), Enable Turn-Off	+25°C		250	500		250		ns
	Full			1000			1000	ns
t_S, Settling Time to 0.1%	+25°C		360			360		ns
to 0.01%	+25°C		600			600		ns
"Off Isolation" (Note 5)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-508	+25°C		22			22		pF
HI-509	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		.08			.08		pF
POWER REQUIREMENTS								
*I+, Positive Supply Current (Note 6)	Full		1.5	2.4		1.5	2.4	mA
*I-, Negative Supply Current (Note 6))	Full		0.4	1		0.4	1	mA
P_D, Power Dissipation	Full			51			51	mW

*100% tested for Dash 8. Leakage currents not tested at -55°C.

TRUTH TABLES

HI-508

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509

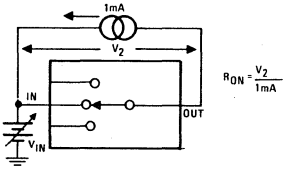
A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = -1mA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
5. V_{EN} = 0.8V, R_L = 1K, C_L = 15pF, V_S = $7V_{RMS}$, f = 100kHz. Worst case isolation occurs on channel 4 due to proximity of the output pins.
6. V_{EN}, V_A = 0V or 2.4V.
7. Signal voltage at any analog input or output (S or D) will be clamped to the supply rail by internal diodes. Limit the resulting current as shown under absolute maximum ratings. If an overvoltage condition is anticipated (analog input exceeds either power supply voltage), the Harris HI-548/549 multiplexers are recommended.

Performance Characteristics and Test Circuits

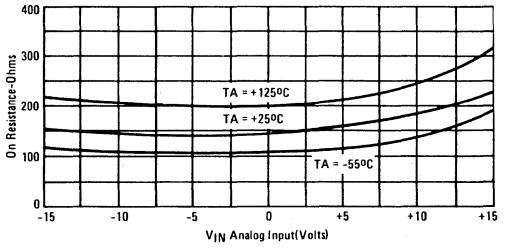
Unless Otherwise Specified; T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = 2.4 V, V_{AL} = 0.8 V.

ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

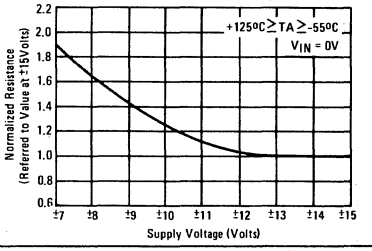


TEST CIRCUIT NO. 1

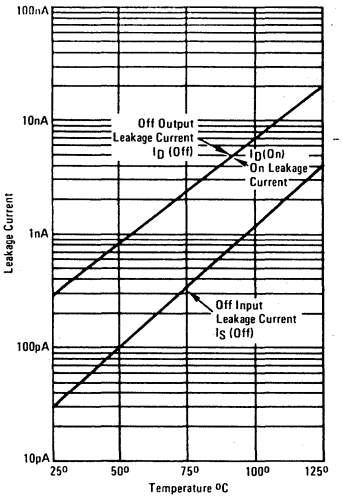
ON RESISTANCE vs. ANALOG INPUT VOLTAGE, TEMPERATURE



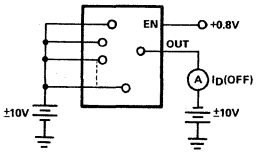
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



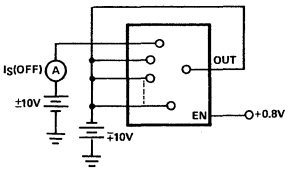
LEAKAGE CURRENT VS. TEMPERATURE



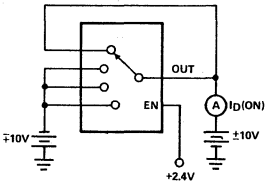
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 4*

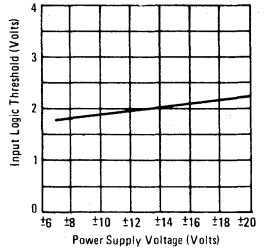


TEST CIRCUIT NO. 3*

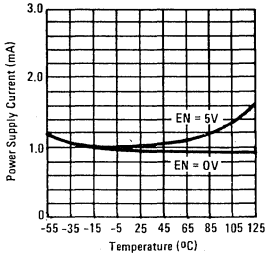


***Two measurements per channel: +10 V/–10 V and –10 V/+10 V. (Two measurements per device for $I_{D(OFF)}$: +10 V/–10 V and –10 V/+10 V.)**

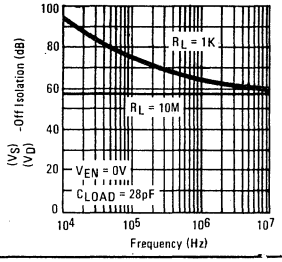
LOGIC THRESHOLD vs. POWER SUPPLY VOLTAGE



POWER SUPPLY CURRENT vs. TEMPERATURE

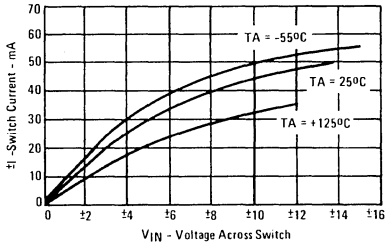


OFF ISOLATION vs. FREQUENCY



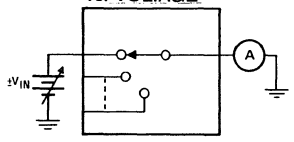
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

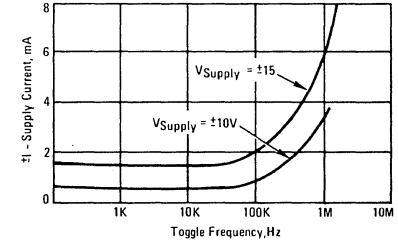


TEST CIRCUIT NO. 5

ON CHANNEL CURRENT vs. VOLTAGE

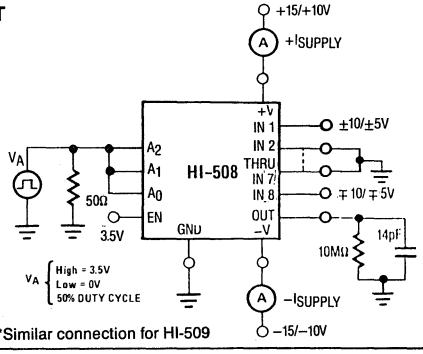


SUPPLY CURRENT vs. TOGGLE FREQUENCY



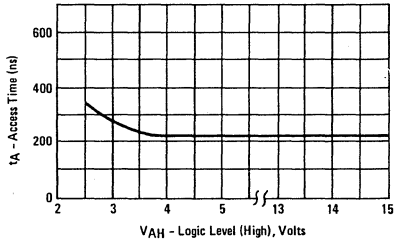
TEST CIRCUIT NO. 6

SUPPLY CURRENT vs. TOGGLE FREQUENCY



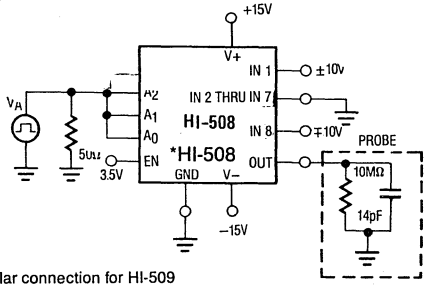
*Similar connection for HI-509

ACCESS TIME vs. LOGIC LEVEL (HIGH)



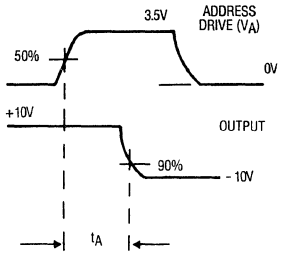
TEST CIRCUIT NO. 7

ACCESS TIME vs. LOGIC LEVEL (HIGH)

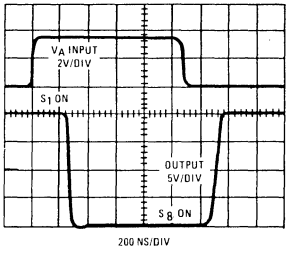


*Similar connection for HI-509

Switching Wav



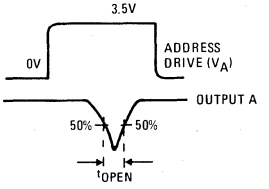
ACCESS TIME



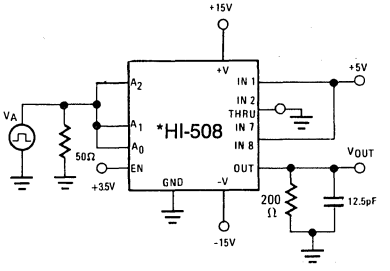
Switching Waveforms (continued)

TEST CIRCUIT NO. 8

ADDRESS DRIVE

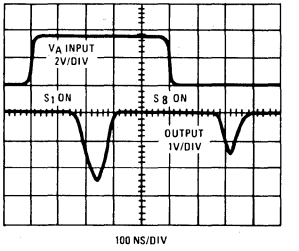


BREAK-BEFORE-MAKE DELAY (t_{OPEN})



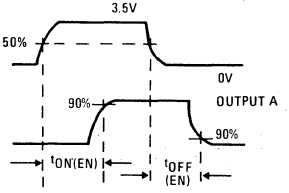
*Similar connection for HI-509

BREAK-BEFORE-MAKE DELAY(t_{OPEN})

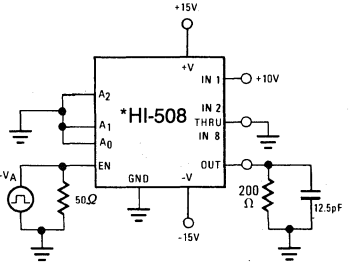


TEST CIRCUIT NO. 9

ENABLE DRIVE

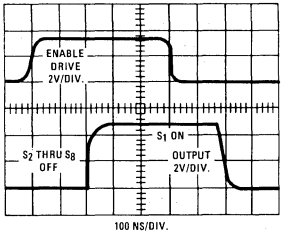


ENABLE DELAY ($t_{ON(EN)}$,$t_{OFF(EN)}$)



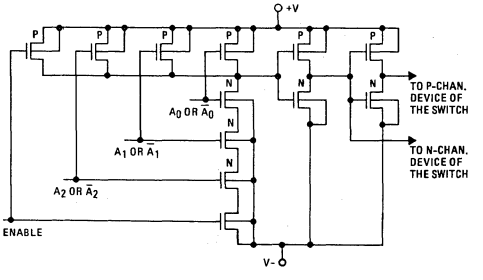
*Similar connection for HI-509

ENABLE DELAY ($t_{ON(EN)}$,$t_{OFF(EN)}$)



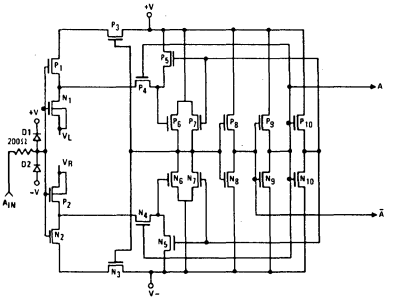
Schematic Diagrams

ADDRESS DECODER



Delete A_2 or $\bar{A}_2$ Input for HI-509

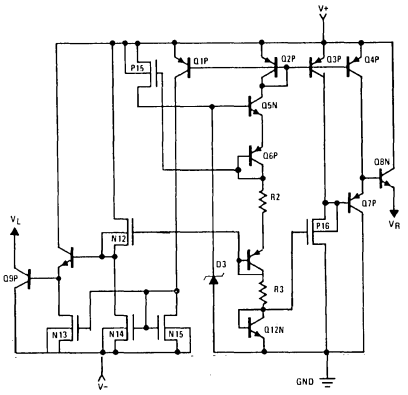
ADDRESS INPUT BUFFER LEVER SHIFTER



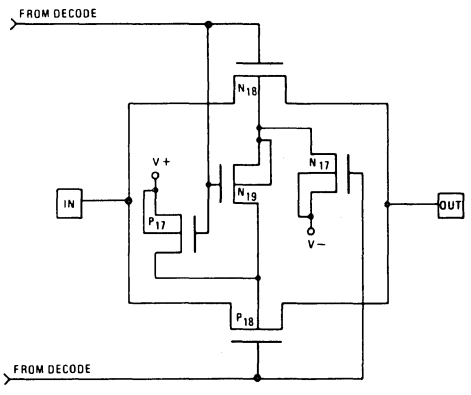
All N-Channel Bodies to V–
All P-Channel Bodies to V+ Unless Otherwise Indicated

Schematic Diagrams (continued)

TTL REFERENCE CIRCUIT

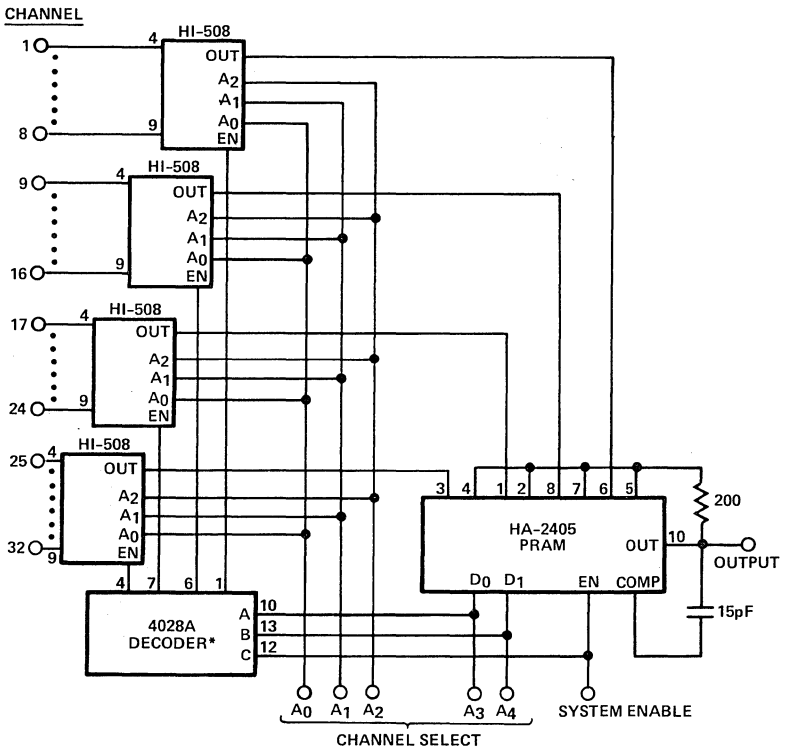


MULTIPLEX SWITCH



Applications

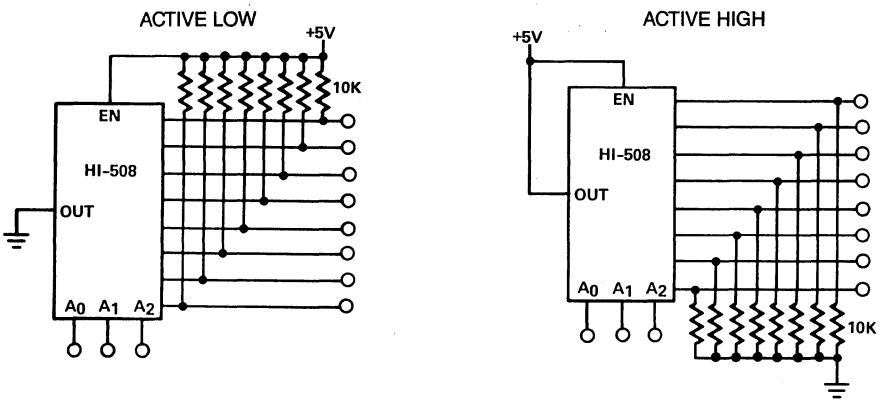
32 CHANNEL BUFFERED MULTIPLEXER *HI-508



*Optional; Provides Greater Isolation for AC Signals.

Applications (continued)

ONE OF 8 DECODER



Die Characteristics

Transistor Count 243
Die Dimensions ..... 81.9 x 90.2 mils
Substrate Potential* ..... $-V_{SUPPLY}$
Process ..... CMOS-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	110	41
Plastic DIP	80	31
Ceramic LCC	82	24

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0508-5	0°C to +75°C	16-Pin CERDIP
HI3-0508-5	0°C to +75°C	16-Pin Plastic DIP
HI1-0508-4	-25°C to +85°C	16-Pin CERDIP
HI1-0508-2	-55°C to +125°C	16-Pin CERDIP
HI4P0508-5	0°C to +75°C	20-Pin PLCC
HI1-0508-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP
HI9P0508-9	-40°C to +85°C	16-Pin SOIC
HI9P0508-5	0°C to +75°C	16-Pin SOIC
HI1-0509-4	-25°C to +85°C	16-Pin CERDIP
HI1-0509-5	0°C to +75°C	16-Pin CERDIP
HI3-0509-5	0°C to +75°C	16-Pin Plastic DIP
HI4P0509-5	0°C to +75°C	20-Pin PLCC
HI1-0509-2	-55°C to +125°C	16-Pin CERDIP
HI1-0509-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP

HARRIS HI-508A/509A

Single 8/Differential 4 Channel CMOS Analog Multiplexers with Active Overvoltage Protection

Features

- Analog Overvoltage Protection ... $70V_{p-p}$
- No Channel Interaction During Overvoltage
- ESD Resistant ..... > 4,000V
- 44V Maximum Power Supply
- Fail Safe with Power Loss (No Latch-Up)
- Break-Before-Make Switching
- Analog Signal Range ..... ±15V
- Access Time (Typical) 500ns
- Standby Power (Typical) 7.5mW

Applications

- Data Acquisition
- Industrial Controls
- Telemetry

Description

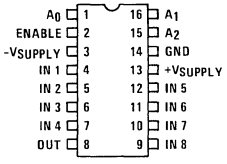
The HI-508A and HI-509A are analog multiplexers with Active Overvoltage Protection. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. Digital inputs will also sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-508A and HI-509A ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The HI-508A is an 8 channel device and the HI-509 is a 4 channel differential version. If input overvoltage protection is not needed, the HI-508 and HI-509 multiplexers are recommended. For further information see Application Notes 520 and 521.

Each device is available in a 16 pin Plastic or Ceramic DIP and a 20 pad Ceramic LCC package.

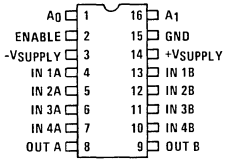
The HI-508A/509A are offered in both commercial and military grades. Additional Hi-Rel screening including 160 hour burn-in is specified by the "-8" suffix. For MIL-STD-883 compliant parts, request the HI-548/883 or HI-549/883 data sheets.

Pinouts

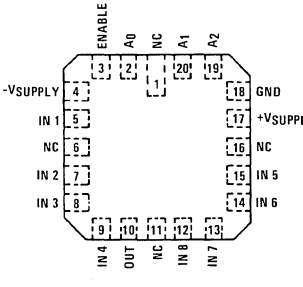
HI1-508A (CERAMIC DIP)
HI3-508A (PLASTIC DIP)
TOP VIEW



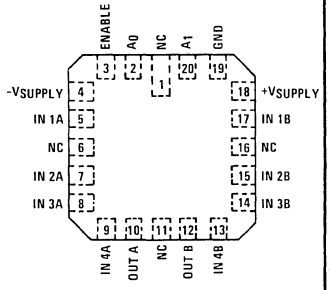
HI1-509A (CERAMIC DIP)
HI3-509A (PLASTIC DIP)
TOP VIEW



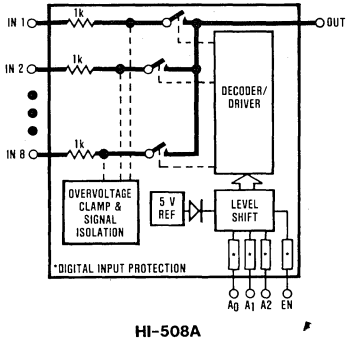
HI4-508A (CERAMIC LCC)
TOP VIEW



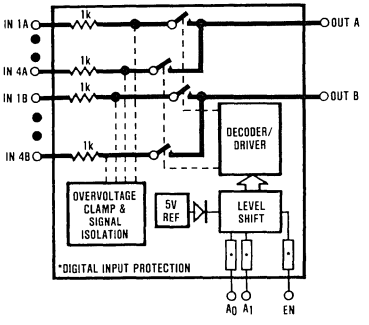
HI4-509A (CERAMIC LCC)
TOP VIEW



Functional Diagrams



HI-508A



HI-509A

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Specifications HI-508A/509A

Absolute Maximum Ratings (Note 1)

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ 44V
$V_{SUPPLY(+)}$ to GND 22V
$V_{SUPPLY(-)}$ to GND 25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first
Analog Signal Overvoltage (Note 7)
$+V_S$ ..... $+V_{SUPPLY}$ +20V
$-V_S$ ..... $-V_{SUPPLY}$ -20V

Continuous Current, S or D: 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% duty cycle max): 40mA
Junction Temperature ..... +175°C
Operating Temperature Ranges:
HI-508A/509A-2, -8 ..... -55°C to +125°C
HI-508A/509A-4 ..... -25°C to +85°C
HI-508A/509A-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications Unless Otherwise Specified:

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V;
V_{AL} (Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-508A/HI-509A -2, -8 MIN.	TYP.	MAX.	HI-508A/509A -5 MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		1.2	1.5		1.5	1.8	kΩ
	Full		1.5	1.8		1.8	2.0	kΩ
*I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
*I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-508A	Full			200			200	nA
HI-509A	Full			100			100	nA
*$I_{D(OFF)}$ with Input Overvoltage Applied (Note 4)	+25°C		4.0			4.0		nA
	Full			2.0				μA
*I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-508A	Full			200			200	nA
HI-509A	Full			100			100	nA
I_{DIFF}, Differential Off Output Leakage Current (HI-509A Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
*V_{AL}, Input Low Threshold (Note 8)	Full			0.8			0.8	V
*V_{AH}, Input High Threshold	Full	4.0			4.0			V
*I_A, Input Leakage Current (High or Low) (Note 5)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
*t_A, Access Time	+25°C		0.5			0.5		μs
	Full			1.0			1.0	μs
*t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
*t_{ON} (EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
*t_{OFF} (EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.01%)	+25°C		3.5			3.5		μs
"OFF Isolation" (Note 6)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-508A	+25°C		25			25		pF
HI-509A	+25°C		12			12		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current (Note 7)	Full		0.5	2.0		0.5	2.0	mA
*I-, Current (Note 7)	Full		0.02	1.0		0.02	1.0	mA

*100% tested for Dash 8. Leakage currents not tested at -55°C.

TRUTH TABLES

HI-508A

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

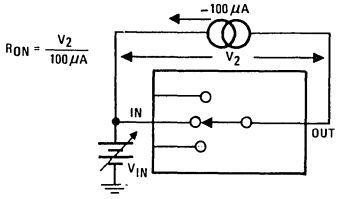
NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = -100μA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Analog Overvoltage = ±33V.
5. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
6. V_{EN} = 0.8V, R_L = 1K, C_L = 15pF, V_S = $7V_{RMS}$, f = 100kHz. Worst Case isolation occurs on channel 4 due to proximity of the output pins.
7. V_{EN}, V_A = 0V or 4.0V.
8. To drive from DTL/TTL Circuits, 1kΩ pull-up resistors to +5.0V supply are recommended.

Performance Characteristics and Test Circuits

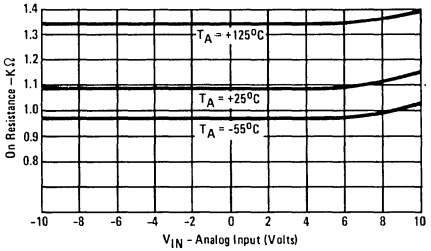
Unless Otherwise Specified T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = +4 V, V_{AL} = 0.8 V

ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

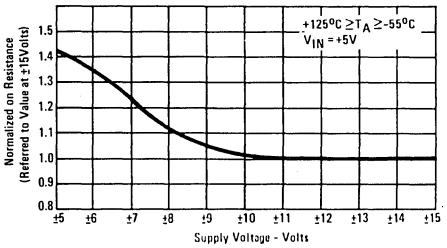
TEST CIRCUIT NO. 1



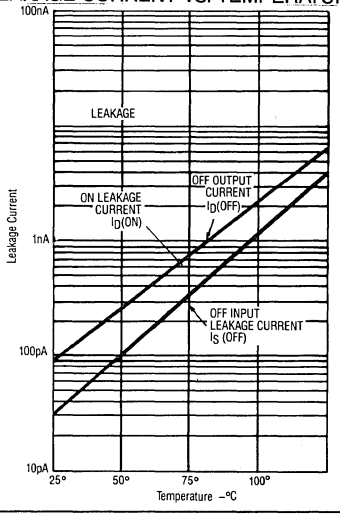
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



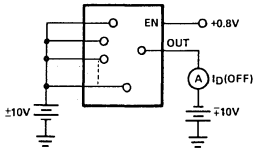
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



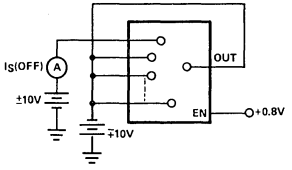
LEAKAGE CURRENT VS. TEMPERATURE



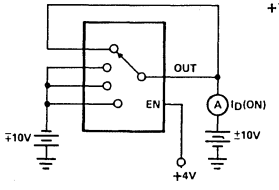
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

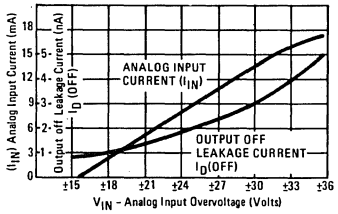


TEST CIRCUIT NO. 4*



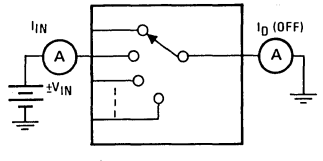
***Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for $I_{D(OFF)}$: +10 V/−10 V and −10 V/+10 V.)**

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



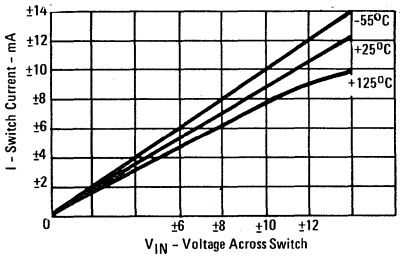
TEST CIRCUIT NO. 5

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



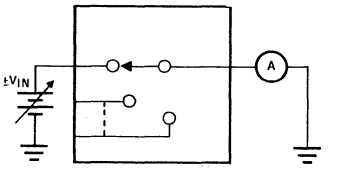
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

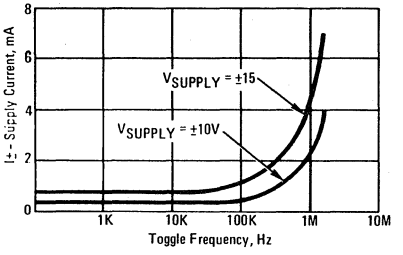


TEST CIRCUIT NO. 6

ON CHANNEL CURRENT vs. VOLTAGE

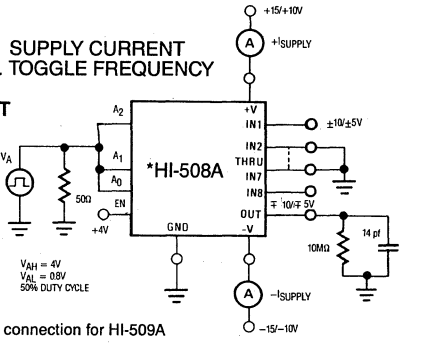


SUPPLY CURRENT vs. TOGGLE FREQUENCY



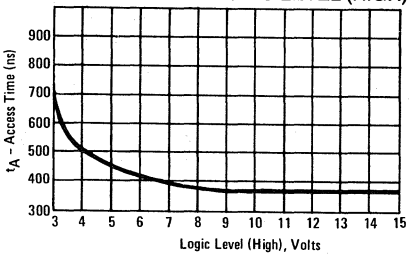
TEST CIRCUIT NO. 7

SUPPLY CURRENT vs. TOGGLE FREQUENCY



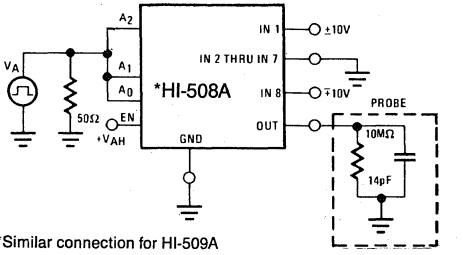
*Similar connection for HI-509A

ACCESS TIME VS. LOGIC LEVEL (HIGH)



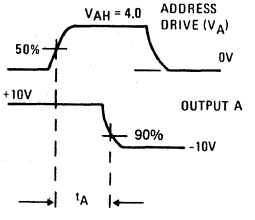
TEST CIRCUIT NO. 8

ACCESS TIME vs. LOGIC LEVEL (HIGH)

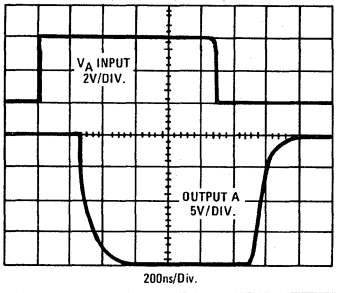


*Similar connection for HI-509A

Switching Waveforms



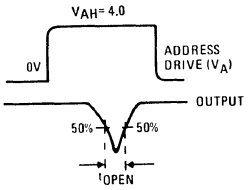
ACCESS TIME

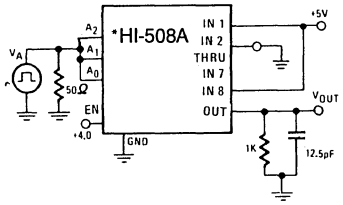


Switching Waveforms (continued)

TEST CIRCUIT NO. 9

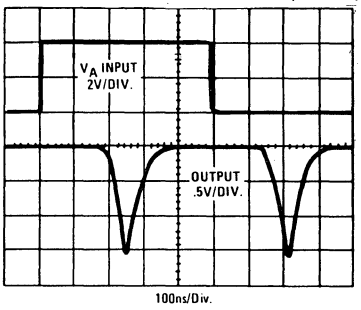
BREAK-BEFORE-MAKE DELAY(tOPEN)





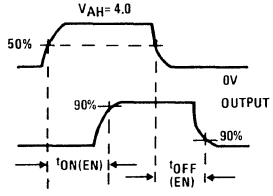
*Similar connection for HI-509A

BREAK-BEFORE-MAKE DELAY (tOPEN)

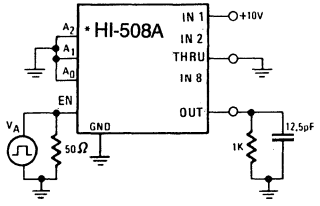


TEST CIRCUIT NO. 10

ENABLE DRIVE

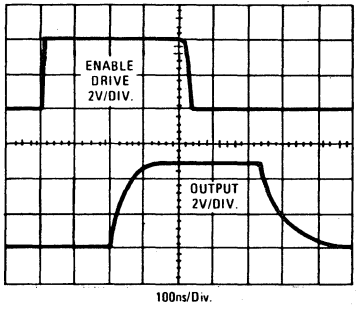


ENABLE DELAY (tON(EN),tOFF(EN))

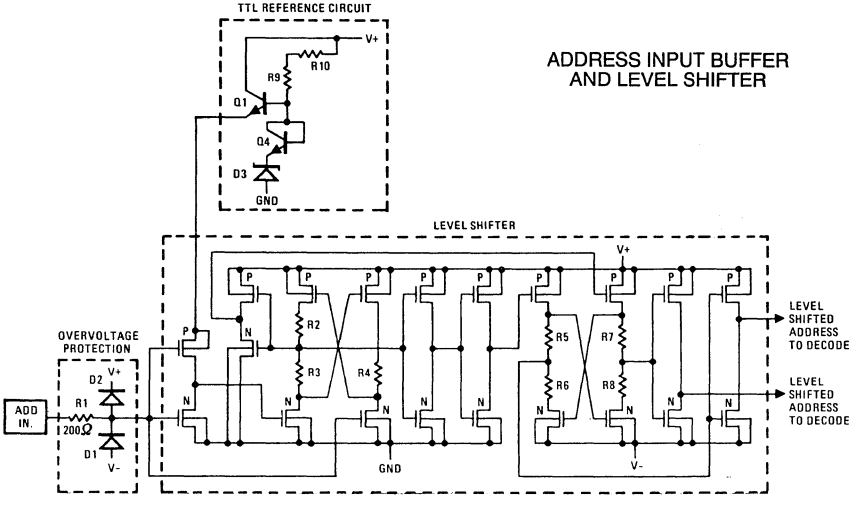


*Similar connection for HI-509A

ENABLE DELAY (tON(EN),tOFF(EN))

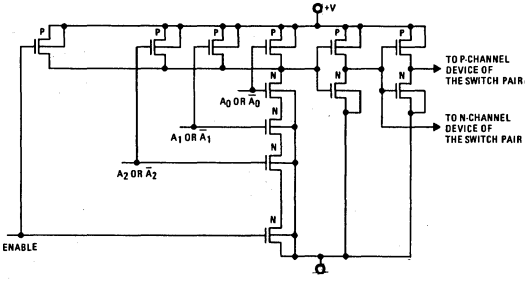


Schematic Diagrams

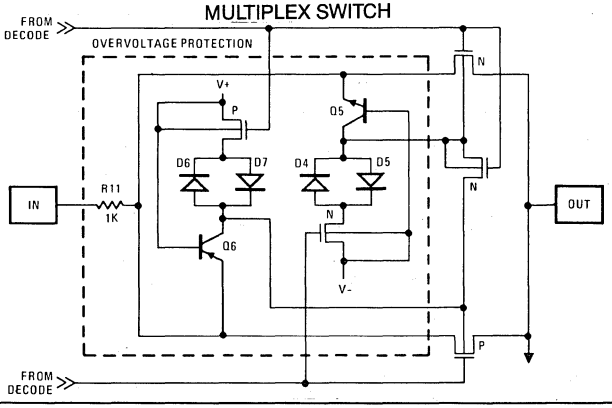


Schematic Diagrams (continued)

ADDRESS DECODER



MULTIPLEX SWITCH



Die Characteristics

Transistor Count	253
Die Dimensions	108 x 83 mils
Substrate Potential*	$-V_{SUPPLY}$
Process	CMOS-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	104	35
Plastic DIP	75	23
Ceramic LCC	76	19

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-508A-5	0°C to +75°C	16-Pin CERDIP
HI3-508A-5	0°C to +75°C	16-Pin Plastic DIP
	-25°C to +85°C	16-Pin CERDIP
HI1-508A-2	-55°C to +125°C	16-Pin CERDIP
	0°C to +75°C	20-Pin PLCC
HI1-508A-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP
	-25°C to +85°C	16-Pin CERDIP
HI1-509A-5	0°C to +75°C	16-Pin CERDIP
HI3-509A-5	0°C to +75°C	16-Pin Plastic DIP
	0°C to +75°C	20-Pin PLCC
HI1-509A-2	-55°C to +125°C	16-Pin CERDIP
HI1-509A-7	0°C to +75°C + 96 Hr. Burn-In	16-Pin CERDIP

HARRIS

HI-516

16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer

Features

- Access Time (Typical) 130ns
- Settling Time (0.1%) 250ns
- Low Leakage (Typical)
  - I_S(OFF) 10pA
  - I_D(OFF) 30pA
- Low Capacitance (Max)
  - C_S(OFF) 10pF
  - C_D(OFF) 25pF
- High Off Isolation at 500kHz (Min) 55dB
- Low Charge Injection Error 20mV
- Single Ended to Differential Selectable (SDS)
- Logic Level Selectable (LLS)

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Industrial Control

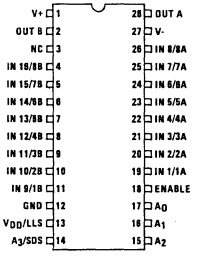
Description

The HI-516 is a monolithic dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A3 enables the HI-516 to be user programmed either as a single ended 16-channel multiplexer by connecting 'out A' to 'out B' and using A3 as a digital address input, or as an 8-channel differential multiplexer by connecting A3 to the V- supply. The substrate leakages and parasitic capacitances are reduced substantially by using the Harris Dielectric Isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current (I_DOFF < 100pA at 25°C) and fast settling (t_{SETTLE} = 800ns to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process control.

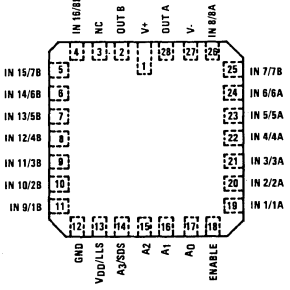
The HI-516 is available in 28 pin Ceramic or Plastic DIPs or in 28 pin Ceramic LCC or PLCC packages. For Mil-Std-883 compliant parts, request the HI-516/883 data sheet.

Pinouts

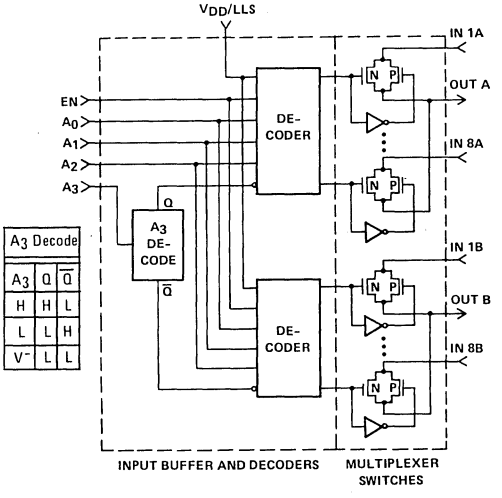
CERAMIC/PLASTIC DIP
TOP VIEW



LCC/PLCC
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Specifications HI-516

Absolute Maximum Ratings (Note 1)

Voltage Between Supply Pins 33V
Analog Input Voltage
- $+V_{IN}$ ..... $+V_{SUPPLY}$ +2V
- $-V_{IN}$ ..... $-V_{SUPPLY}$ -2V

Digital Input Voltage
- TTL Levels Selected (V_{DD}/LLS Pin = GND or Open)
  - $+V_A$ ..... +6V
  - $-V_A$ ..... -6V
  - $+A_3$/SDS ..... $+V_{SUPPLY}$ +2V
  - $-A_3$/SDS ..... $-V_{SUPPLY}$ -2V
- CMOS Levels Selected (V_{DD}/LLS Pin = V_{DD})
  - $+V_A$ ..... $+V_{SUPPLY}$ +2V
  - $-V_A$ ..... -2V

Junction Temperature (Max) ..... 175°C
Operating Temperature Ranges:
- HI-516-2, -8 ..... -55°C to +125°C
- HI-516-5 ..... 0°C to +75°C

Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications

(Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = GND. (Note 2)

PARAMETER	TEMP	HI-516-2, -8 MIN	HI-516-2, -8 TYP	HI-516-2, -8 MAX	HI-516-5 MIN	HI-516-5 TYP	HI-516-5 MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_{IN}, Analog Signal Range (Note 3)	Full	-14		+14	-15		+15	V
R_{ON}, On Resistance (Note 4)	+25°C		620	750		620	750	Ω
	Full			1,000			1,000	Ω
I_S (OFF), Off Input Leakage Current	+25°C		0.01			0.01		nA
	Full			50			50	nA
I_D(OFF), Off Output Leakage Current	+25°C		0.03			0.03		nA
	Full			100			100	nA
I_D(ON), On Channel Leakage Current	+25°C		0.04			0.04		nA
	Full			100			100	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
V_{AL} Input Low Threshold (CMOS)	Full			$0.3V_{DD}$			$0.3V_{DD}$	V
V_{AH} Input High Threshold (CMOS)	Full	$0.7V_{DD}$			$0.7V_{DD}$			V
I_{AH} Input Leakage Current (High)	Full			1			1	μA
I_{AL} Current (Low)	Full			25			25	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		130	175		130	175	ns
	Full			225			225	ns
t_{OPEN}, Break before make delay	+25°C	10	20		10	20		ns
t_{ON}(EN), Enable Delay (ON)	+25°C		120	175		120	175	ns
t_{OFF}(EN), Enable Delay (OFF)	+25°C		140	175		140	175	ns
Settling Time (0.1%)	+25°C		250			250		ns
(0.01%)	+25°C		800			800		ns
Charge Injection Error (Note 5)	+25°C			20			20	mV
Off Isolation (Note 6)	+25°C	55			55			dB
C_S(OFF), Channel Input Capacitance	+25°C			10			10	pF
C_D(OFF), Channel Output Capacitance	+25°C			25			25	pF
C_A, Digital Input Capacitance	+25°C			10			10	pF
C_{DS}(OFF), Input to Output Capacitance	+25°C		0.02			0.02		pF
POWER REQUIREMENTS								
PD, Power Dissipation	Full			750			900	mW
I^+, Current (Note 7)	Full			25			30	mA
I^-, Current (Note 7)	Full			25			30	mA

NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{DD}/LLS pin = open or grounded for TTL compatibility. V_{DD}/LLS pin = V_{DD} for CMOS Compatibility
3. At temperatures above 90°C, care must be taken to fassure V_{IN} remains at least 1.0V below the V_{SUPPLY} for proper operation.
4. V_{IN} = ±10V, I_{OUT} = -100μA
5. V_{IN} = 0V, C_L = 100pF, Enable input pulse = 3V, f = 500kHz.
6. V_{EN} = 0.8V, V_S = $3V_{RMS}$, f = 500kHz, C_L = 40pF, R_L = 1K, Pin 3 grounded.
7. V_{EN} = +2.4V

TRUTH TABLES

HI-516 USED AS A 16-CHANNEL MULTIPLEXER OR 8 CHANNEL DIFFERENTIAL MULTIPLEXER *

USE A_3 AS DIGITAL ADDRESS INPUT					ON CHANNEL TO	
ENABLE	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	NONE	NONE
H	L	L	L	L	1A	NONE
H	L	L	L	H	2A	NONE
H	L	L	H	L	3A	NONE
H	L	L	H	H	4A	NONE
H	L	H	L	L	5A	NONE
H	L	H	L	H	6A	NONE
H	L	H	H	L	7A	NONE
H	L	H	H	H	8A	NONE
H	H	L	L	L	NONE	1B
H	H	L	L	H	NONE	2B
H	H	L	H	L	NONE	3B
H	H	L	H	H	NONE	4B
H	H	H	L	L	NONE	5B
H	H	H	L	H	NONE	6B
H	H	H	H	L	NONE	7B
H	H	H	H	H	NONE	8B

* For 16-Channel single-ended function, tie 'out A' to 'out B', for dual 8-channel function use the A_3 address pin to select between MUX A and MUX B, where MUX A is selected with A_3 low.

HI-516 USED AS A DIFFERENTIAL 8-CHANNEL MULTIPLEXER

A_3 CONNECT TO V^- SUPPLY				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

Die Characteristics

Transistor Count 647
Die Dimension ..... 89 x 146 mils
Substrate Potential* ..... $-V_{SUPPLY}$
Process: ..... CMOS-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	50	18
Ceramic LCC	81	40

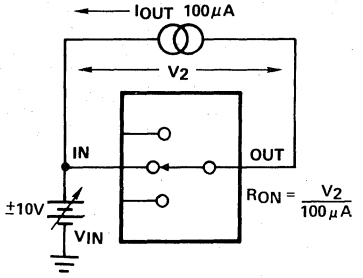
*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Ordering Information

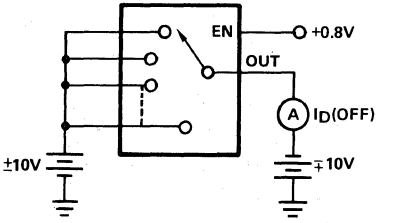
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI4P0516-5	0°C to +75°C	28-Pin PLCC
HI3-0516-5	0°C to +75°C	28-Pin Plastic DIP
HI1-0516-5	0°C to +75°C	28-Pin CERDIP
HI1-0516-2	-55°C to +125°C	28-Pin CERDIP

Performance Characteristics and Test Circuits

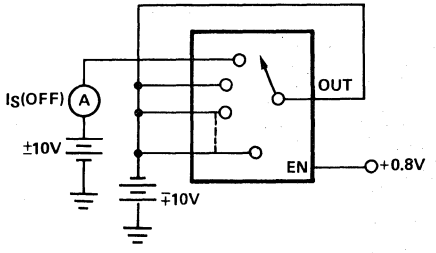
TEST CIRCUIT NO. 1
ON RESISTANCE vs. INPUT SIGNAL LEVEL



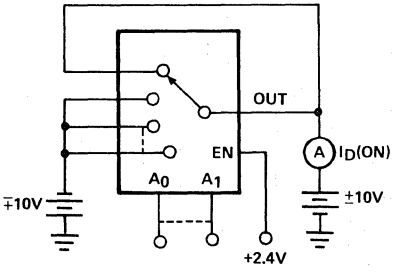
TEST CIRCUIT NO. 2*



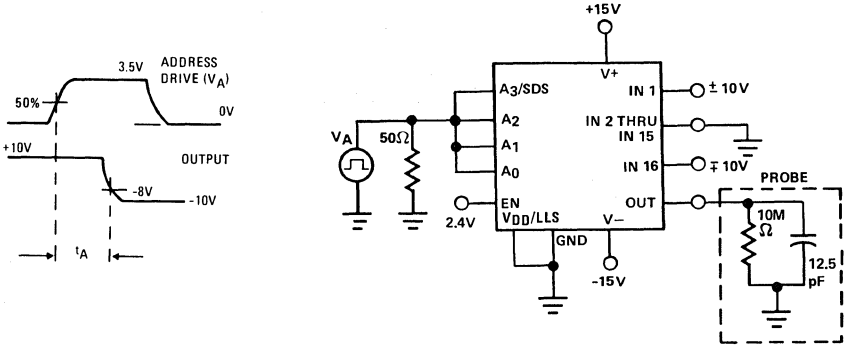
TEST CIRCUIT NO. 3*



TEST CIRCUIT NO. 4*



TEST CIRCUIT NO. 5
ACCESS TIME

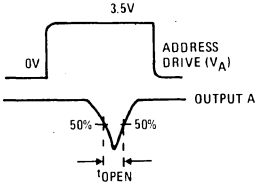


*Two measurements per channel: +10V/-10V and -10V/+10V.
(Two measurements per device for $I_{D(OFF)}$: +10V/-10V and -10V/+10V)

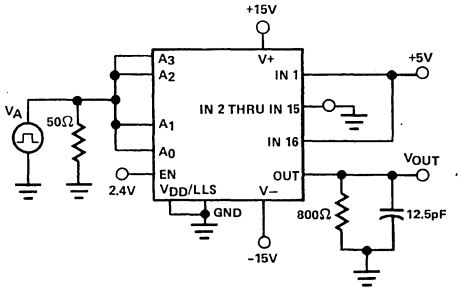
Performance Characteristics and Test Circuits (Continued)

TEST CIRCUIT NO. 6

ENABLE DRIVE

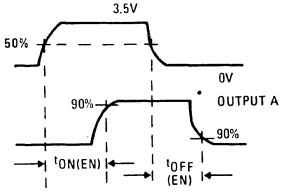


BREAK-BEFORE MAKE DELAY (t_{OPEN})

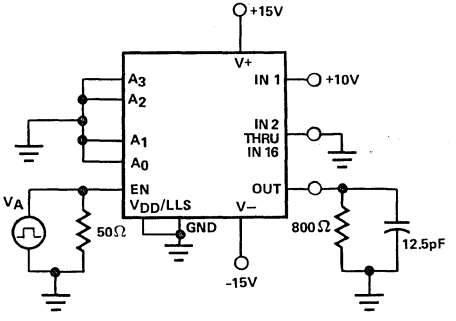


TEST CIRCUIT NO. 7

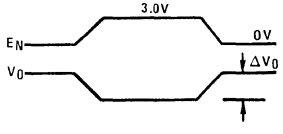
ENABLE DRIVE



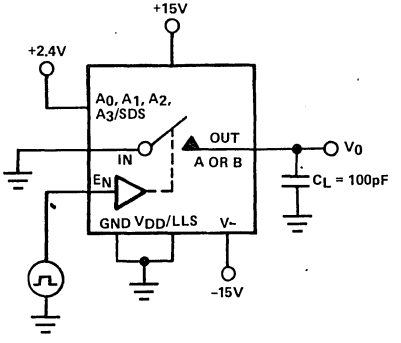
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



TEST CIRCUIT NO. 8
CHARGE INJECTION TEST CIRCUIT



ΔV_O IS THE MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION. THE ERROR VOLTAGE IN COULOMBS IS $Q = C_L \times \Delta V_O$.



HI-518

8 Channel/Differential
4 Channel CMOS High Speed Analog Multiplexer

Features

- Access Time (Typical) 130ns
- Settling Time (0.1%) 250ns
- Low Leakage (Typical)
  - I_S(OFF) 5pA
  - I_D(OFF) 15pA
- Low Capacitance (Max)
  - C_S(OFF) 5pF
  - C_D(OFF) 10pF
- High Off Isolation at 500kHz (Min) 45dB
- Low Charge Injection Error 25mV
- Single Ended to Differential Selectable (SDS)
- Logic Level Selectable (LLS)

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Industrial Control

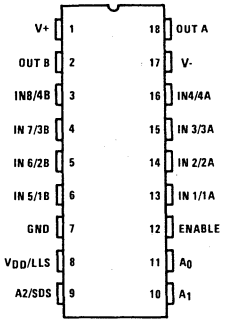
Description

The HI-518 is a monolithic dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_2 enables the HI-518 to be user programmed either as a single ended 8-channel multiplexer by connection 'out A' to 'out B' and using A_2 as a digital address input, or as a 4-channel differential multiplexer by connecting A_2 to V- supply. The substrate leakages and parasitic capacitances are reduced substantially by using the Harris dielectric isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current (I_DOFF < 100pA @ +25°C) and fast settling (t_{SETTLE} = 800ns to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process control.

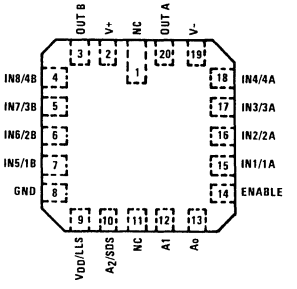
The HI-518 is available in an 18 lead Ceramic or Plastic dual-in-line package and a 20 pin LCC or PLCC package. It is offered in two operating ranges: -55°C to +125°C and 0°C to +75°C. For MIL-STD-883 compliant parts, request the HI-518/883 data sheet.

Pinouts

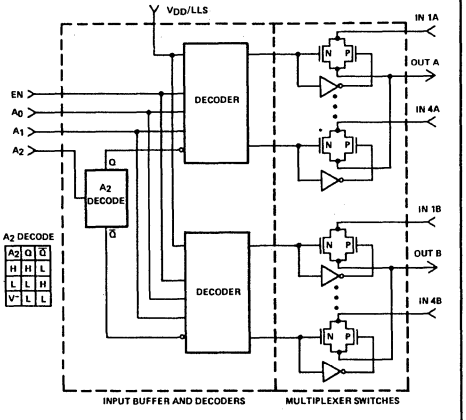
CERAMIC/PLASTIC DIP
TOP VIEW



LCC/PLCC
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Absolute Maximum Ratings (Note 1)

Analog Input Voltage
- $+V_{IN}$ ..... $+V_{SUPPLY}$ +2V
- $-V_{IN}$ ..... $-V_{SUPPLY}$ -2V

Digital Input Voltage

TTL Levels Selected (V_{DD}/LLS Pin = GND or Open)
- $+V_A$ ..... +6V
- $-V_A$ ..... -6V
- A2/SDS ..... $+V_{SUPPLY}$ +2V
- A2/SDS ..... $-V_{SUPPLY}$ -2V

Voltage Between Supply Pins 33V

CMOS Levels Selected (V_{DD}/LLS Pin = V_{DD})
- $+V_A$ ..... $+V_{SUPPLY}$ +2V
- $-V_A$ ..... -2V

Operating Temperature Ranges
- HI-518-2/-8 ..... -55°C to +125°C
- HI-518-5 ..... 0°C to +75°C

Storage Temperature Range ..... -65°C to +150°C

Junction Temperature (Max) ..... 175°C

Electrical Specifications (Unless Otherwise Specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = GND (Note 2)

PARAMETER	TEMP	HI-518-2, -8 MIN	HI-518-2, -8 TYP	HI-518-2, -8 MAX	HI-518-5 MIN	HI-518-5 TYP	HI-518-5 MAX	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_{IN} Analog Signal Range (Note 3)	Full	-14		+14	-15		+15	V
R_{ON} On Resistance (Note 4)	+25°C		480	750		480	750	Ω
	Full			1000			1000	Ω
I_S (OFF) Off Input	+25°C		0.01			0.01		nA
Leakage Current	Full			50			50	nA
I_D (OFF) Off Output	+25°C		0.015			0.015		nA
Leakage Current	Full			50			50	nA
I_D (ON) On Channel	+25°C		0.015			0.015		nA
Leakage Current	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
V_{AL} Input Low Threshold (CMOS)	Full			$0.3V_{DD}$			$0.3V_{DD}$	V
V_{AH} Input High Threshold (CMOS)	Full	$0.7V_{DD}$			$0.7V_{DD}$			V
I_{AH} Input Leakage Current (High)	Full			1			1	μA
I_{AL} Input Leakage Current (Low)	Full			20			20	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		130	175		130	175	ns
	Full			225			225	ns
t_{OPEN}, Break before make Delay	+25°C	10	20		10	20		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		120	175		120	175	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		140	175		140	175	ns
'Settling Time (0.1%)	+25°C		250			250		ns
(0.01%)	+25°C		800			800		ns
Charge Injection Error (Note 5)	+25°C			25			25	mV
Off Isolation (Note 6)	+25°C	45			45			dB
C_S (OFF) Channel Input Capacitance	+25°C			5			5	pF
C_D (OFF) Channel Output Capacitance	+25°C			10			10	pF
C_A, Digital Input Capacitance	+25°C			5			5	pF
CDS (OFF) Input to Output Capacitance	+25°C		0.02			0.02		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full			450			540	mW
I^+, Current (Note 7)	Full			15			18	mA
I^-, Current (Note 7)	Full			15			18	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{DD}/LLS Pin = Open or Grounded for TTL compatibility. V_{DD}/LLS pin = V_{DD} for CMOS compatibility.
3. At temperatures above +90°C, care must be taken to assure V_{IN} remains at least 1.0V below the V_{SUPPLY}.
4. V_{IN} = ±10V, I_{OUT} = -100μA.
5. V_{IN} = 0V, C_L = 100pF, Enable Input Pulse = 3V, f = 500kHz.
6. C_L = 40pF, R_L = 1k. Due to the pin to pin capacitance between IN 8/4B and OUT B channel 8/4B exhibits 60dB of OFF Isolation under the above test conditions.
7. V_{EN} = 2.4V.

Truth Tables

HI-518 USED AS A 8 CHANNEL MULTIPLEXER OR 4 CHANNEL DIFFERENTIAL MULTIPLEXER

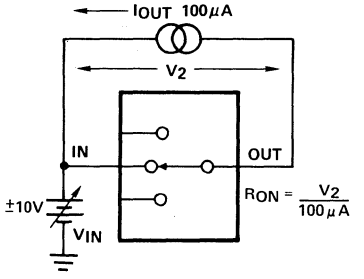
USE A_2 AS DIGITAL ADDRESS INPUT				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	NONE	NONE
H	L	L	L	1A	NONE
H	L	L	H	2A	NONE
H	L	H	L	3A	NONE
H	L	H	H	4A	NONE
H	H	L	L	NONE	1B
H	H	L	H	NONE	2B
H	H	H	L	NONE	3B
H	H	H	H	NONE	4B

HI-518 USED AS DIFFERENTIAL 4 CHANNEL MULTIPLEXER

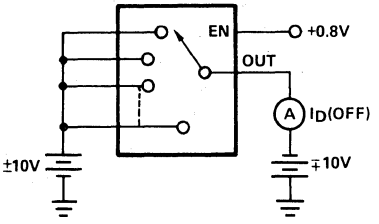
A_2 CONNECT TO V^- SUPPLY			ON CHANNEL TO	
ENABLE	A_1	A_0	OUT A	OUT B
L	X	X	NONE	NONE
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

Performance Characteristics and Test Circuits

TEST CIRCUIT NO. 1
ON RESISTANCE vs. INPUT SIGNAL LEVEL



TEST CIRCUIT NO. 2*



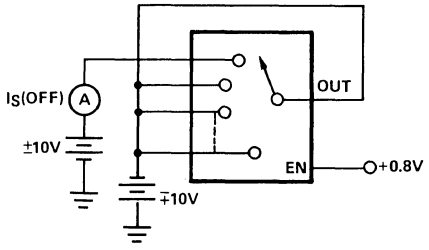
*Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for I_D(OFF): +10V/-10V and -10V/+10V)

Ordering Information

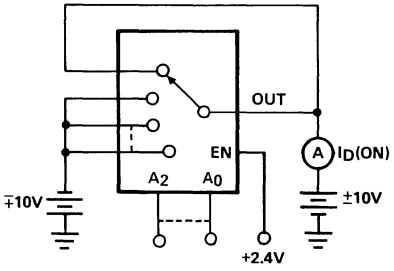
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI3-0518-5	0°C to +75°C	18-Pin Plastic DIP
HI1-0518-5	0°C to +75°C	18-Pin CERDIP
HI1-0518-2	-55°C to +125°C	18-Pin CERDIP
HI4P0518-5	0°C to +75°C	20-Pin PLCC

Performance Characteristics and Test Circuits (Continued)

TEST CIRCUIT NO. 3*



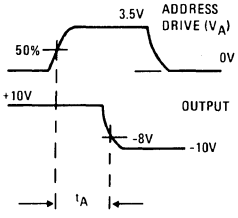
TEST CIRCUIT NO. 4*

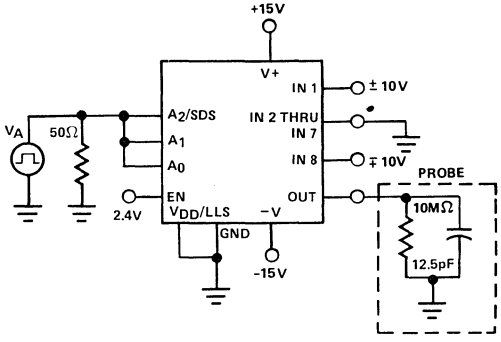


*Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for I_D(OFF): +10V/-10V and -10V/+10V)

TEST CIRCUIT NO. 5

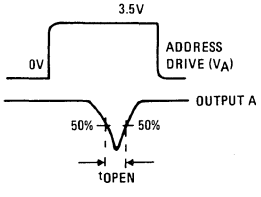
ACCESS TIME



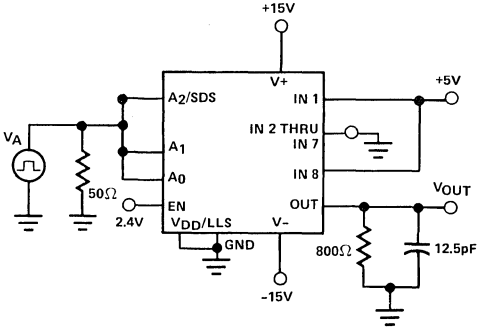


TEST CIRCUIT NO. 6

ENABLE DRIVE



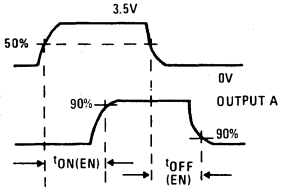
BREAK-BEFORE MAKE DELAY (t_{OPEN})



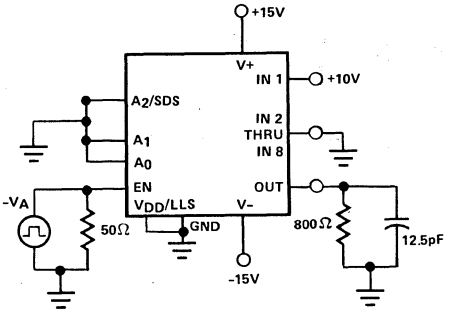
Performance Characteristics and Test Circuits (Continued)

TEST CIRCUIT NO. 7

ENABLE DRIVE

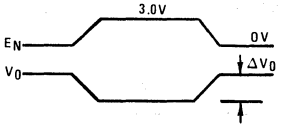


ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

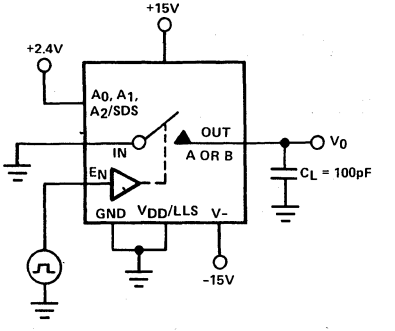


TEST CIRCUIT NO. 8

CHARGE INJECTION TEST CIRCUIT



ΔV_O IS THE MEASURED VOLTAGE ERROR DUE TO CHARGE INJECTION. THE ERROR VOLTAGE IN COULOMBS IS $Q = C_L X \Delta V_O$.



Die Characteristics

Transistor Count		356
Die Dimensions		89 x 93 mils
Substrate Potential*		$-V_{SUPPLY}$
Process:		CMOS-DI
Thermal Constants ($^oC/W$)	θ_{ja}	θ_{jc}
Ceramic DIP	84	25
Plastic DIP	81	33
Ceramic LCC	78	21

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

HARRIS

HI-524

4 Channel Wideband and Video Multiplexer

Features

- Crosstalk (10MHz)..... < -60dB
- Fast Access Time 150ns
- Fast Settling Time 200ns
- TTL Compatible

Applications

- Wideband Switching
- Radar
- TV Video
- ECM

Description

The HI-524 is a four channel CMOS analog multiplexer designed to process single-ended signals with bandwidths up to 10MHz. The chip includes a 1 of 4 decoder for channel selection and an enable input to inhibit all channels (chip select).

Three CMOS transmission gates are used in each channel, as compared to the single gate in more conventional CMOS multiplexers. This provides a double barrier to the unwanted coupling of signals from each input to the output. In addition, Dielectric Isolation (DI) processing helps to insure the Crosstalk is less than -60dB at 10MHz.

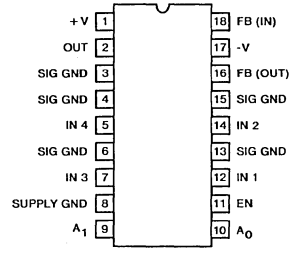
The HI-524 is designed to operate into a wideband buffer amplifier such as the Harris HA-2541. The multiplexer chip includes two "ON" switches in series, for use as a feedback element with the amplifier. This feedback resistance matches and tracks the channel R_{ON} resistance, to minimize the amplifier V_{OS} and its variation with temperature.

The HI-524 is well suited to the rapid switching of video and other wideband signals in telemetry, instrumentation, radar and video systems. It is packaged in an 18 pin ceramic or plastic DIP and a 20 pin plastic leaded chip carrier or a 20 pin ceramic leadless chip carrier and operates on ±15V supplies.

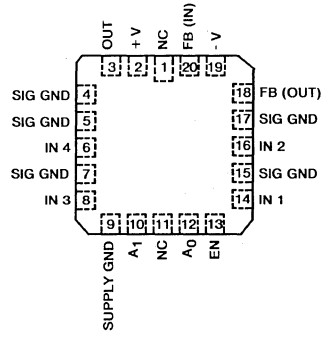
For MIL-STD-883 compliant parts, request the HI-524/883 data sheet.

Pinouts

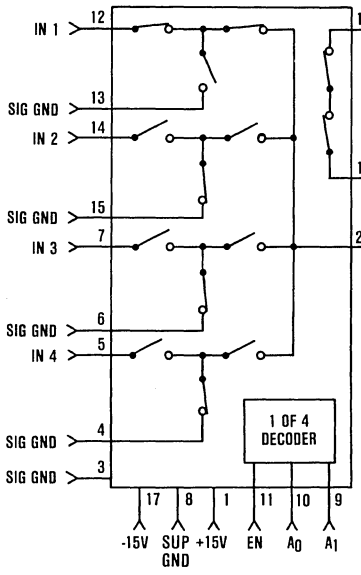
CERAMIC/PLASTIC DIP
TOP VIEW



LCC/PLCC
TOP VIEW



Functional Diagram



TRUTH TABLE

A_1	A_0	EN	ON CHANNEL
X	X	L	NONE
L	L	H	1*
L	H	H	2
H	L	H	3
H	H	H	4

*Channel 1 is shown selected in the diagram

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Specifications HI-524

Absolute Maximum Ratings (Note 1)

Voltage Between Supply 33V
Digital Input Voltage:
$+V_A$ ..... +6V
$-V_A$ ..... -6V
Analog Input Voltage
$+V_{IN}$ ..... $+V_{SUPPLY}$ +2V
$-V_{IN}$ ..... $-V_{SUPPLY}$ -2V
Either Supply to Ground 16.5V
Junction Temperature (Max) ..... 175°C

Operating Temperature Range

HI-524-2/-8 ..... -55°C to +125°C
HI-524-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications

(Unless otherwise specified) Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} = (Logic Level Low) = +0.8V; V_{EN} = +2.4V.

PARAMETER	TEMP	HI-524 -2/-8 MIN	HI-524 -2/-8 TYP	HI-524 -2/-8 MAX	HI-524 -5 MIN	HI-524 -5 TYP	HI-524 -5 MAX	UNITS
ANALOG CHANNEL SPECIFICATIONS								
V_{IN}, Analog Signal Range	Full	-10		+10	-10		+10	V
R_{ON}, On Resistance (Note 2)	+25°C		700			700		Ω
	Full			1.5K			1.5K	Ω
I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.2			0.2		nA
	Full			50			50	nA
$I_{D\ (OFF)}$, Off Output Leakage Current (Note 3)	+25°C		0.2			0.2		nA
	Full			50			50	nA
I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.7			0.7		nA
	Full			50			50	nA
3dB Bandwidth: (Note 4)	+25°C		8			8		MHz
DIGITAL INPUT SPECIFICATIONS								
V_{AL} Input Low Threshold (TTL)	Full			0.8			0.8	V
V_{AH} Input High Threshold (TTL)	Full	2.4			2.4			V
I_{AH} Input Leakage Current (High)	Full		0.05	1		0.05	1	μA
A_L Current (Low)	Full			25			25	μA
SWITCHING SPECIFICATIONS								
t_A, Access Time (Note 5)	+25°C		150	300		150	300	ns
t_{OPEN}, Break-Before-Make Delay (Note 5)	+25°C		20			20		ns
t_{ON} (EN), Enable Delay (ON), R_L = 500Ω	+25°C		180	300		180		ns
t_{OFF} (EN), Enable Delay (OFF), R_L = 500Ω	+25°C		180	250		180		ns
Settling Time (0.1%) (Note 5)	+25°C		200			200		ns
(0.01%)	+25°C		600			600		ns
Crosstalk (Note 6)	+25°C		-65			-65		dB
C_S(OFF), Channel Input Capacitance	+25°C		4			4		pF
C_D(OFF), Channel Output Capacitance	+25°C		10			10		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full			750			750	mW
I+, Current (Note 7)	Full			25			25	mA
I-, Current (Note 7)	Full			25			25	mA

NOTES:

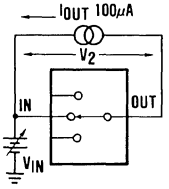
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{IN} = 0V; I_{OUT} = 100μA (See Test Circuits #1)
3. V_O = ±10V; V_{IN} = ±10V (See Test Circuits #2, 3, 4,)
4. MUX output is buffered with HA-5033 amplifier.
5. **6V Step, ±3V to ±3V, See Test Circuit #5.**
6. V_{IN} = 10MHz, $3V_{p-p}$ on one channel, with any other channel selected. (Worst case is channel 3 selected with input on channel 4). MUX output is buffered with HA-2541 as shown in Applications section. Terminate all channels with 75Ω.
7. Supply currents vary less than 0.5mA for switching rates from DC to 2MHz.

Performance Characteristics and Test Circuits

Unless otherwise specified T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V

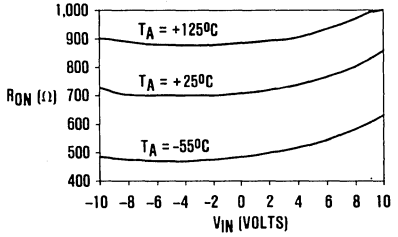
ON RESISTANCE

TEST CIRCUIT NO. 1

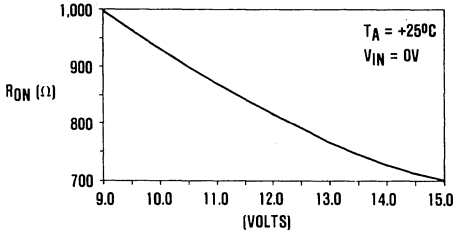


$$R_{ON} = \frac{V2}{100\mu A}$$

ON RESISTANCE vs. ANALOG INPUT VOLTAGE

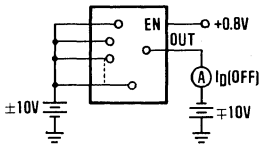


ON RESISTANCE vs. SUPPLY VOLTAGE

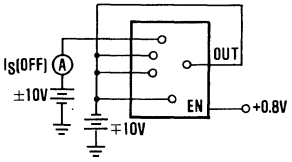


LEAKAGE CURRENT

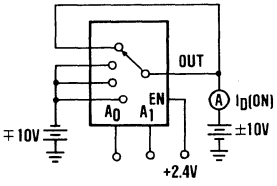
TEST CIRCUIT NO. 2*



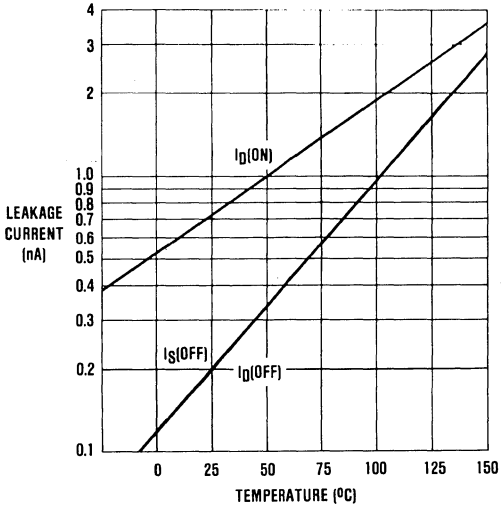
TEST CIRCUIT NO. 3*



TEST CIRCUIT NO. 4*



LEAKAGE CURRENT vs. TEMPERATURE

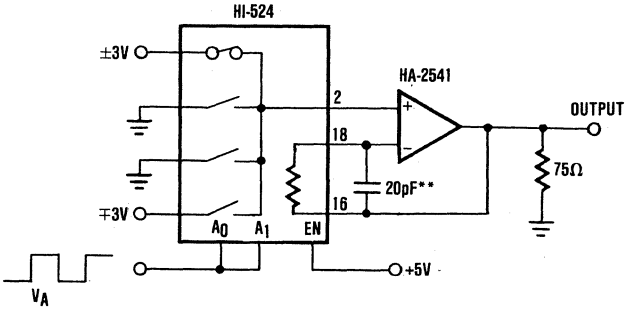


*Two measurements per channel:
+10V/-10V and -10V/+10V
(Two measurements and per device for I_D(OFF):
+10V/-10V and -10V/+10V.)

Performance Characteristics and Test Circuits (Continued)

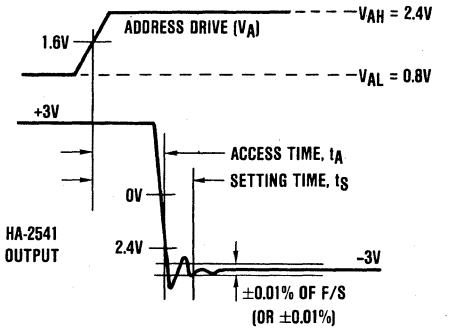
TEST CIRCUIT NO. 5

SETTLING TIME
ACCESS TIME
BREAK-BEFORE-MAKE DELAY*

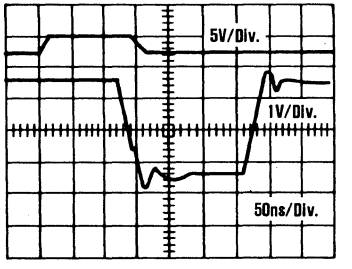


* This test requires channel inputs 1 and 4 at the same level.
** Capacitor value may be selected to optimize AC performance.

(Use Differential comparator plug-in on scope for settling time measurement)

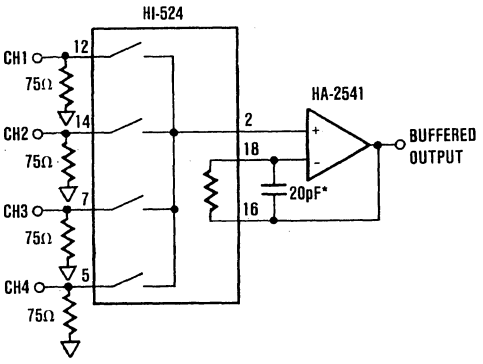


ACCESS TIME



Applications

Often it is desirable to buffer the HI-524 output, to avoid loading errors due to the channel "ON" resistance:



* Capacitor value may be selected to optimize AC performance.

The buffer amplifier should offer sufficient bandwidth and slew rate to avoid degradation of the anticipated signals. For video switching, the HA-5033 and HA-2542 offer good performance plus ±100mA output current for driving coaxial cables. For general wideband applications, the HA-2541 offers the convenience of unity gain stability plus 90ns settling (to ±0.1%) and ±10V output swing. Also, the HI-524 includes a feedback resistance for use with the HA-2541. This resistance matches and tracks the channel "ON" resistance, to minimize offset voltage due to the buffer's bias currents.

Note that the on-chip feedback element between pins 16 and 18 includes two switches in series, to simulate a channel resistance. These switches open for V_{EN} = Low. This allows two or more HI-524's to operate into one HA-2541, with their feedback elements connected in parallel. Thus, only the selected multiplexer provides feedback, and the amplifier remains stable.

All HI-524 DIP package pins labeled 'SIG GND' (pins 3, 4, 6, 13, 15) should be externally connected to signal ground for best crosstalk performance.

Bypass capacitors (0.1 to 1.0μF) are recommended from each HI-524 supply pin to power ground (pins 1 and 17 to pin 8 DIP package). Locate the buffer amplifier near the HI-524 so the two capacitors may bypass both devices.

If an analog input 1V or greater is present when supplies are off, a low resistance is seen from that input to a supply line. (For example, the resistance is approximately 160Ω for an input of -3V.) Current frow may be blocked by a diode in each supply line, or limited by a resistor in series with each channel. the best solution, of course, is to arrange that no digital or analog inputs are present when the power supplies are off.

Die Characteristics

Transistor Count 599
Die Dimensions ..... 146 x 88.6 mils
Substrate Potential* ..... $-V_{SUPPLY}$
Process: ..... CMOS-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	81	22
Plastic DIP	78	30
Ceramic LCC	76	19

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0524-5	0°C to +75°C	18-Pin CERDIP
HI1-0524-2	-55°C to +125°C	18-Pin CERDIP
HI4P0524-5	0°C to +75°C	20-Pin PLCC
HI3-0524-5	0°C to +75°C	18-Pin Plastic DIP

HI-539

Monolithic, 4 Channel, Low Level, Differential Multiplexer

Features

- **Differential Performance, Typical:**
  - **Low ΔR_{ON}, +125°C.....5.5Ω**
  - **Low $\Delta I_{D(ON)}$, +125°C 0.6nA**
  - **Low Δ(Charge Injection).....0.1pC**
  - **Low Crosstalk.....-124dB**
- **Settling Time, ±0.01%.....900ns**
- **Wide Supply Range.....±5V to ±18V**
- **Break-Before-Make Switching**
- **No Latch-Up**

Applications

- **Low Level Data Acquisition**
- **Precision Instrumentation**
- **Test Systems**

Description

The Harris HI-539 is a monolithic, four channel, differential multiplexer. Two digital inputs are provided for channel selection, plus an Enable input to disconnect all channels.

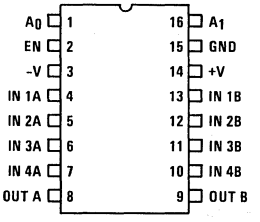
Performance is guaranteed for each channel over the voltage range ±10V, but is optimized for low level differential signals. Leakage current, for example, which varies slightly with input voltage, has its distribution centered at zero input volts.

In most monolithic multiplexers, the net differential offset due to thermal effects becomes significant for low level signals. This problem is minimized in the HI-539 by symmetrical placement of critical circuitry with respect to the few heat producing devices.

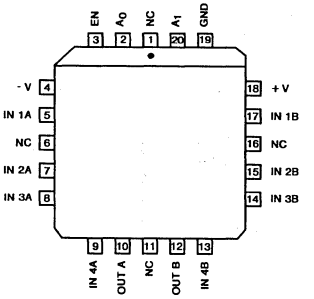
Supply voltages are ±15V and power consumption is only 2.5mW. The HI-539 is packaged in a 16 pin Ceramic or Plastic DIP, and a 20 pin Plastic Leaded Chip Carrier.

Pinouts

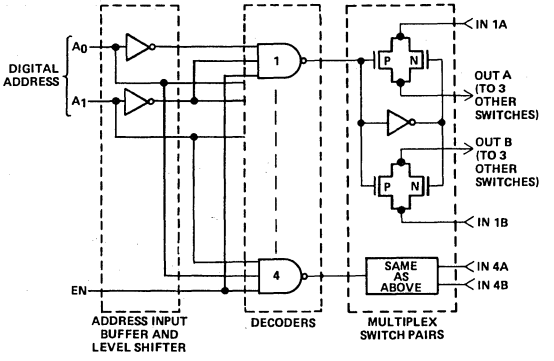
HI1-539 CERAMIC DIP
HI3-539 PLASTIC DIP
TOP VIEW



HI4P539 PLCC
TOP VIEW



Functional Diagram



CAUTION: Electronic devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Specifications HI-539

Absolute Maximum Ratings

Voltage Between Supply Pins (-V, +V) 40V
Voltage From Either Supply to Gnd 20V
Analog Input Voltage, V_{IN} ..... $-V \leq V_{IN} \leq +V$
Digital Input Voltage, V_A ..... $-V \leq V_A \leq +V$
Junction Temperature (Max) ..... 175°C

$I_{Source\ or\ Drain}$ 20mA
Operating Temperature Range
HI-539-2, -8 ..... -55°C to +125°C
HI-539-4 ..... -25°C to +85°C
HI-539-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications

(Unless otherwise specified) Supplies = ±15V, V_{EN} = +4.0V, V_{AH} (Logic Level High) = +4.0V, V_{AL} (Logic Level Low) = +0.8V. See the "Performance Characteristics and Test Circuits". Selected parameters are defined in "Definitions".

PARAMETER	TEMP	HI-539-2, -8 TYP	HI-539-2, -8 MAX (MIN)	HI-539-4, -5 TYP	HI-539-4, -5 MAX (MIN)	UNITS
ANALOG CHANNEL CHARACTERISTICS						
V_{IN}, Analog Signal Range	Full		(-10)/+10		(-10)/+10	V
R_{ON}, On Resistance V_{IN} = 0V	+25°C	650	850	650	850	Ω
V_{IN} = ± 10V	+25°C	700	900	700	900	Ω
V_{IN} = 0V	Full	950	1.3k	800	1k	Ω
V_{IN} = ± 10V	Full	1.1k	1.4k	900	1.1k	Ω
ΔR_{ON} [Side A - Side B]						
V_{IN} = 0V	+25°C	4.0	24	4.0	24	Ω
V_{IN} = ± 10V	+25°C	4.5	27	4.5	27	Ω
V_{IN} = 0V	Full	4.75	28	4.0	24	Ω
V_{IN} = ± 10V	Full	5.5	33	4.5	27	Ω
$I_{S(OFF)}$, Off Input Leakage Current (Note 1)						
Condition 0V	+25°C	30		30		pA
Condition ± 10V	+25°C	100		100		pA
Condition 0V	Full	2	10	0.2	1	nA
Condition ± 10V	Full	5	25	0.5	2.5	nA
$\Delta I_{S(OFF)}$, [Side A - Side B]						
Condition 0V	+25°C	3		3		pA
Condition ± 10V	+25°C	10		10		pA
Condition 0V	Full	0.2	2	0.02	0.2	nA
Condition ± 10V	Full	0.5	5	0.05	0.5	nA
$I_{D(OFF)}$, Off Output Leakage Current (Note 1)						
Condition 0V	+25°C	30		30		pA
Condition ± 10V	+25°C	100		100		pA
Condition 0V	Full	2	10	0.2	1	nA
Condition ± 10V	Full	5	25	0.5	2.5	nA
$\Delta I_{D(OFF)}$, [Side A - Side B]						
Condition 0V	+25°C	3		3		pA
Condition ± 10V	+25°C	10		10		pA
Condition 0V	Full	0.2	2	0.02	0.2	nA
Condition ± 10V	Full	0.5	5	0.05	0.5	nA
$I_{D(ON)}$, On Channel Leakage Current (Note 1)						
Condition 0V	+25°C	50		50		pA
Condition ± 10V	+25°C	150		150		pA
Condition 0V	Full	5	25	0.5	2.5	nA
Condition ± 10V	Full	6	40	0.8	4.0	nA
$\Delta I_{D(ON)}$ [Side A - Side B]						
Condition 0V	+25°C	10		10		pA
Condition ± 10V	+25°C	30		30		pA
Condition 0V	Full	0.5	5	0.05	0.5	nA
Condition ± 10V	Full	0.6	6	0.08	0.8	nA
ΔV_{OS}, Differential Offset Voltage (Note 2)	+25°C	0.02		0.02		μV
	Full	0.70		0.08		μV

Specifications HI-539

PARAMETER	TEMP	HI-539-2, -8 TYP	HI-539-2, -8 MAX (MIN)	HI-539-4, -5 TYP	HI-539-4, -5 MAX (MIN)	UNITS
DIGITAL INPUT CHARACTERISTICS						
V_{AL}, Input Low Threshold	Full		0.8		0.8	V
V_{AH}, Input High Threshold	Full		(4.0)		(4.0)	V
I_{AH}, Input Leakage Current (High)	Full		1		1	μA
I_{AL}, Input Leakage Current (Low)	Full		1		1	μA
SWITCHING CHARACTERISTICS						
T_A, Access Time	+25°C	250	750	250	750	ns
	Full		1,000		1,000	ns
T_{open}, Break-Before-Make Delay	+25°C	85	(30)	85	(30)	ns
	Full		(30)		(30)	ns
$T_{ON(EN)}$, Enable Delay On	+25°C	250	750	250	750	ns
	Full		1,000		1,000	ns
$T_{OFF(EN)}$, Enable Delay Off	+25°C	160	650	160	650	ns
	Full		900		900	ns
Settling Time, to ±0.01%	+25°C	0.9		0.9		μs
Charge Injection (Output)	Full	3		3		pC
Δ Charge Injection (Output)	Full	0.1		0.1		pC
Charge Injection (Input)	Full	10		10		pC
Differential Crosstalk (Note 3)	+25°C	124		124		dB
Single Ended Crosstalk (Note 3)	+25°C	100		100		dB
$C_{S(OFF)}$, Channel Input Capacitance	Full	5		5		pF
$C_{D(OFF)}$, Channel Output Capacitance	Full	7		7		pF
$C_{D(ON)}$, Channel On Output Capacitance	Full	17		17		pF
C_{DS}, Input to Output Capacitance (Note 4)	Full	0.08		0.08		pF
C_A, Digital Input Capacitance	Full	3		3		pF
POWER REQUIREMENTS						
P_D, Power Dissipation	+25°C	2.3		2.3		mW
	Full		45		45	mW
I+ Current	+25°C	0.150		0.150		mA
	Full		2.0		2.0	mA
I- Current	+25°C	0.001		0.001		mA
	Full		1.0		1.0	mA
±V, Supply Voltage Range	Full	±15	(±5)/ ±18	±15	(±5)/ ±18	V

NOTES:

1. See Test Circuits #2, 3, 4. The condition ±10V means:
   $I_{S(OFF)}$ and $I_{D(OFF)}$: (V_S = +10V, V_D = -10V), then (V_S = -10V, V_D = +10V)
   $I_{D(ON)}$: (+10V, then -10V)
2. ΔV_{OS} (Exclusive of thermocouple effects) = R_{ON} $\Delta I_{D(ON)}$ + $I_{D(ON)}$ ΔR_{ON}.
   See Applications section for discussion of additional V_{OS} error.
3. V_{IN} = 1kHz, 15V_{p-p} on all but the selected channel. See Test Circuit #9.
4. Calculated from typical Single-Ended Crosstalk performance.

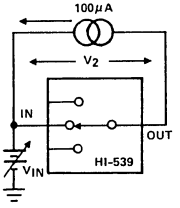
Performance Characteristics and Test Circuits

(Unless otherwise specified T_A = 25°C, +V = +15V, -V = -15V, V_{AH} = +4V and V_{AL} = +0.8V)

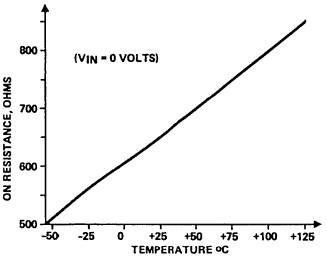
ON RESISTANCE MEASUREMENT

TEST CIRCUIT NO. 1

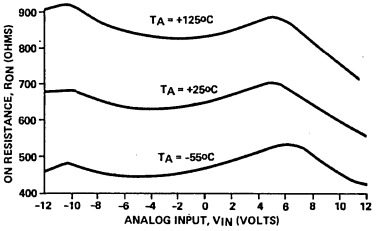
$R_{ON} = \frac{V_2}{100\mu A}$



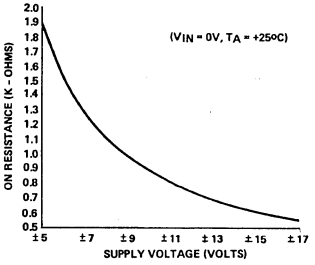
ON RESISTANCE vs. TEMPERATURE



ON RESISTANCE vs. ANALOG INPUT VOLTAGE

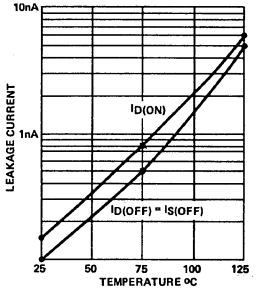


ON RESISTANCE vs. SUPPLY VOLTAGE

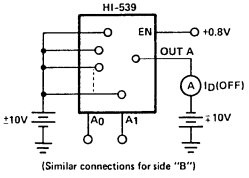


LEAKAGE CURRENT

LEAKAGE CURRENT vs. TEMPERATURE

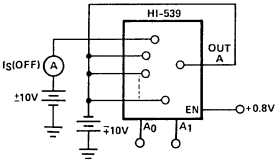


TEST CIRCUIT NO. 2*



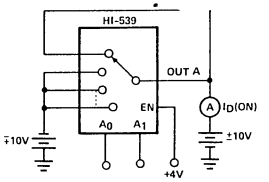
(Similar connections for side "B")

TEST CIRCUIT NO. 3*



(Similar connections for side "B")

TEST CIRCUIT NO. 4*



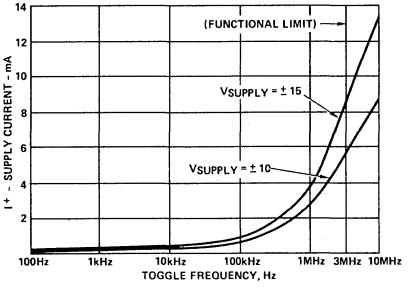
(Similar connections for side "B")

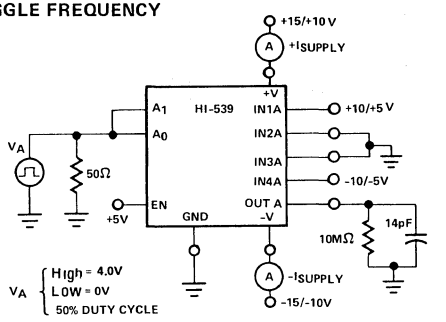
*Three measurements = +10V/-10V, -10V/+10V, and 0V

Test Circuits (Continued)

TEST CIRCUIT NO. 5

SUPPLY CURRENT vs. TOGGLE FREQUENCY

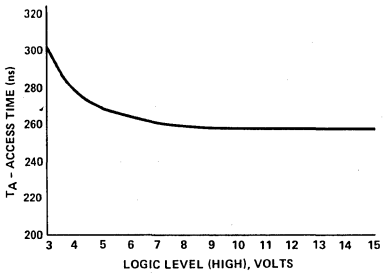


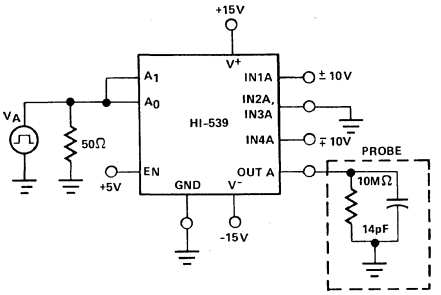


(SIMILAR CONNECTIONS FOR "B" SIDE

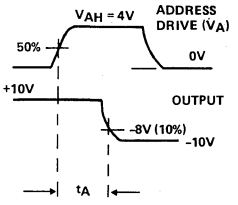
TEST CIRCUIT NO. 6

ACCESS TIME vs. LOGIC LEVEL (HIGH)

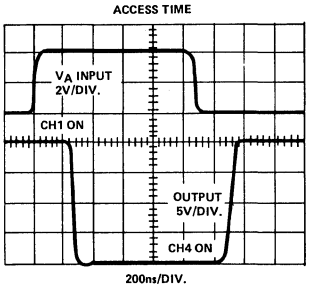




(SIMILAR CONNECTIONS FOR "B" SIDE)



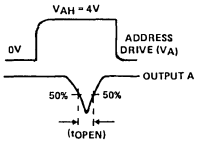
Example: t_A for 4V logic level

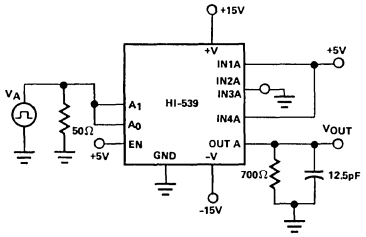


Test Circuits (Continued)

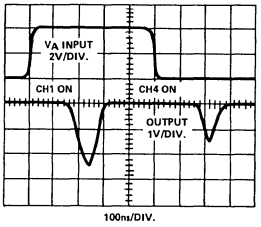
TEST CIRCUIT NO. 7

ADDRESS DRIVE





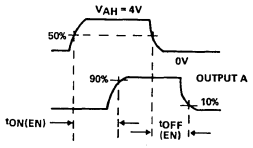
BREAK-BEFORE-MAKE DELAY (t_{OPEN})

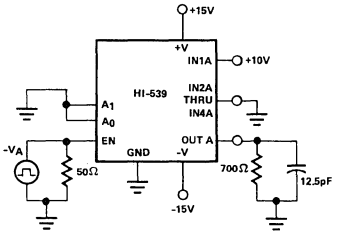


(SIMILAR CONNECTION FOR "B" SIDE)

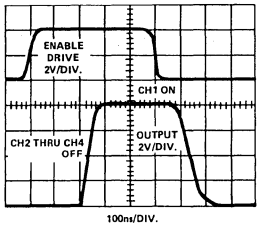
TEST CIRCUIT NO. 8

ENABLE DRIVE





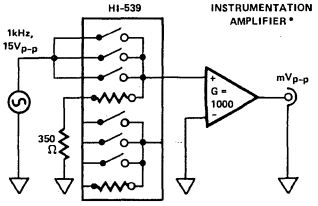
ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)



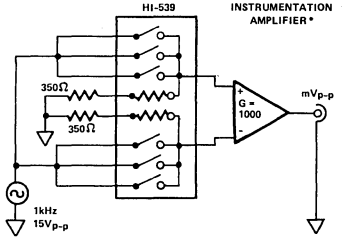
(SIMILAR CONNECTION FOR "B" SIDE)

TEST CIRCUIT NO. 9

SINGLE-ENDED CROSSTALK



DIFFERENTIAL CROSSTALK



*AD606 or BB3630, FOR EXAMPLE

Definitions

CHARGE INJECTION – Charge (in pC) transferred, during a transition between channels, through the internal gate-to-channel capacitance. The resulting voltage error varies inversely with the output (or input) capacitance.

CROSSTALK – Signal at the multiplexer output, coupling though the C_{DS} capacitance of an OFF channel. Amplitude is proportional to source resistance for the ON channel. See Test Circuit # 9 for single-ended and differential versions of crosstalk.

DIFFERENTIAL LEAKAGE CURRENT ($\Delta I_{S(OFF)}$, $\Delta I_{D(OFF)}$, $\Delta I_{D(ON)}$) – The absolute difference in leakage for the two sides of a channel.

DIFFERENTIAL OFFSET VOLTAGE (ΔV_{OS}) – Voltage between the multiplexer output terminals with both channel input terminals shorted to ground.

DIFFERENTIAL ON RESISTANCE (ΔR_{ON}) – The absolute difference in Qn Resistance for the two sides of a channel.

INPUT TO OUTPUT CAPACITANCE (C_{DS}) – Capacitance from one input terminal of a channel to the corresponding output of the multiplexer. This parameter is responsible for Crosstalk.

Applications

GENERAL

The HI-539 accepts inputs in the range -15V to +15V, with performance guaranteed over the ±10V range. At these higher levels of analog input voltage it is comparable to the HI-509, and is plug-in compatible with that device (as well as the HI-509A). However, as mentioned earlier, the HI-539 was designed to introduce minimum error when switching low level inputs.

Special care is required in working with these low level signals. The main concern with signals below 100mV is that noise, offset voltage, and other aberrations can represent a large percentage error. A shielded, differential signal path is essential, especially to maintain a noise level below 50 μVrms.

LOW LEVEL SIGNAL TRANSMISSION

The transmission cable carrying the transducer signal is critical in a low level system. It should be as short as practical and rigidly supported. Signal conductors should be tightly twisted for minimum enclosed area, to guard against pickup of electromagnetic interference, and the twisted pair should be shielded against capacitively coupled (electrostatic) interference. A braided wire shield may be satisfactory, but a lapped foil shield is better since it allows only one tenth as much leakage capacitance to ground per foot. A key requirement for the transmission cable is that it presents a balanced line to sources of noise interference. This means an equal series impedance in each conductor plus an equally distributed impedance from each conductor to ground. The result should be signals equal in magnitude but opposite in phase at any transverse plane. Noise will be coupled in phase to both conductors, and may be rejected as common mode voltage by a differential amplifier connected to the multiplexer output.

Coaxial cable is not suitable for low-level signals because the two conductors (center and shield) are unbalanced. Also, ground loops are produced if the shield is grounded at both ends by standard BNC connectors. If coax must be used, carry the signal on the center conductors of two equal-length cables whose shields are terminated only at the transducer end. As a general rule, terminate (ground) the shield at one end only, preferably at the end with greatest noise interference. This is usually the transducer end for both high and low level signals.

TABLE 1.

WIRE GAGE	EQUIVALENT WIDTH OF P.C. CONDUCTOR (2 oz. Cu.)	D.C. RESISTANCE PER FOOT	INDUCTANCE PER FOOT	IMPEDANCE PER FOOT	
				AT 60Hz	AT 10kHz
18	0.47"	0.0064Ω	0.36μH	0.0064Ω	0.0235Ω
20	0.30"	0.0102Ω	0.37μH	0.0102Ω	0.0254Ω
22	0.19"	0.0161Ω	0.37μH	0.0161Ω	0.0288Ω
24	0.12"	0.0257Ω	0.40μH	0.0257Ω	0.0345Ω
26	0.075"	0.041Ω	0.42μH	0.041Ω	0.0488Ω
28	0.047"	0.066Ω	0.45μH	0.066Ω	0.0718Ω
30	0.029"	0.105Ω	0.49μH	0.105Ω	0.110Ω
32	0.018"	0.168Ω	0.53μH	0.168Ω	0.171Ω

Applications (Continued)

WATCH SMALL ΔV ERRORS

Printed circuit traces and short lengths of wire can add substantial error to a signal even after it has traveled hundreds of feet and arrived on a circuit board. Here, the small voltage drops due to current flow through connections of a few milliohms must be considered, especially to meet an accuracy requirement of 12 bits or more.

Table 1 is a useful collection of data for calculating the effect of these short connections. (Proximity to a ground plane will lower the values of inductance.)

As an example, suppose the HI-539 is feeding a 12 bit converter system with an allowable error of ±1/2 LSB (±1.22mV). If the interface logic draws 100mA from the 5V supply, this current will produce 1.28mV across 6 inches of #24 wire; more than the error budget. Obviously, this digital current must not be routed through any portion of the analog ground return network.

PROVIDE PATH FOR I_{BIAS}

The input bias current for any DC-coupled amplifier must have an external path back to the amplifier's power supply. No such path exists in Figure 1A, and consequently the amplifer output will remain in saturation.

A single large resistor (1MΩ to 10MΩ) from either signal line to power supply common will provide the required path, but a resistor on each line is necessary to preserve accuracy. A single pair of these bias current resistors on the HI-539 output may be used if their loading effect can be tolerated (each forms a voltage divider with R_{ON}). Otherwise, a resistor pair on each input channel of the multiplexer is required.

The use of bias current resistors is acceptable only if one is confident that the sum of signal plus common-mode voltage will remain within the input range of the multiplexer/amplifier combination.

Another solution is to simply run a third wire from the low side of the signal source, as in Figure 1B. This wire assures a low common-mode voltage as well as providing the path for bias currents. Making the connection near the multiplexer will save wire, but it will also unbalance the line and reduce the amplifier's common-mode rejection.

DIFFERENTIAL OFFSET, ΔV_{OS}

There are two major sources of ΔV_{OS}. That part, due to the expression (R_{ON} $\Delta I_D(ON) + I_D(ON)$ ΔR_{ON}) becomes significant with increasing temperature, as shown in the Electrical Characteristics section. The other source of offset is the thermocouple effects due to dissimilar materials in the signal path. These include silicon, aluminum, tin, nickel-iron and (often) gold, just to exit the package.

For the thermocouple effects in the package alone, the constraint on ΔV_{OS} may be stated in terms of a limit on the difference in temperature for package pins leading to any channel of the HI-539. For example, a difference of 0.13°C produces a 5μV offset. Obviously, this ΔT effect can dominate the ΔV_{OS} parameter at any temperature unless care is taken in mounting the HI-539 package.

Temperature gradients across the HI-539 package should be held to a minimum in critical applications. Locate the HI-539 far from heat producing components, with any air currents flowing lengthwise across the package.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI4P0539	0°C to +75°C	20-Pin PLCC
HI1-0539-2	-55°C to +125°C	16-Pin CERDIP
HI3-0539-5	0°C to +75°C	16-Pin Plastic DIP
HI1-0539-4	-25°C to +85°C	16-Pin CERDIP
HI1-0539-5	0°C to +75°C	16-Pin CERDIP

Applications (Continued)

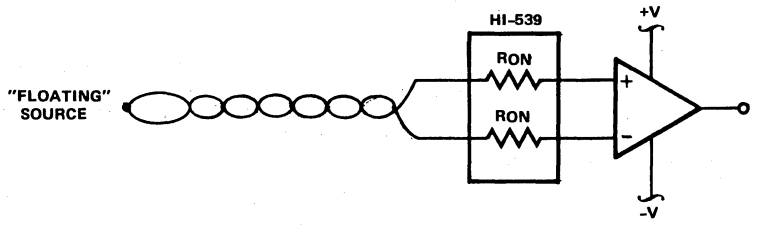


FIGURE 1A

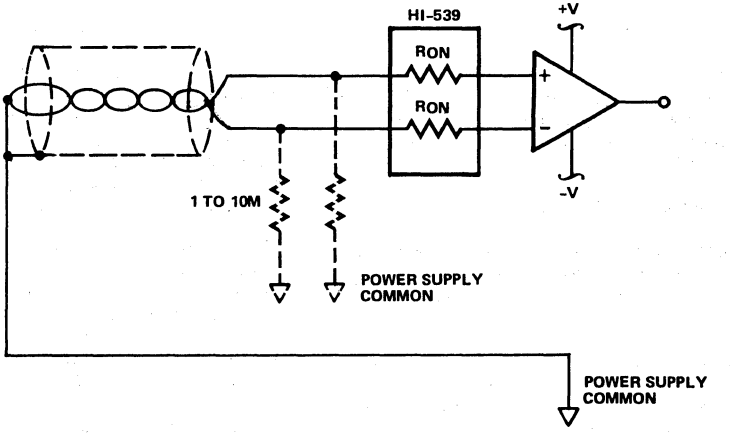


FIGURE 1B

The amplifier in Figure 1A is unusable because its bias currents cannot return to the power supply. Figure 1B shows two alternative paths for these bias currents: either a pair of resistors, or (better) a third wire from the low side of the signal source.

Die Characteristics

Transistor Count 236
Die Dimensions ..... 92 x 100 mils
Substrate Potential* ..... $-V_{SUPPLY}$
Process: ..... CMOS-DI

Thermal Constants ($^oC/W$)	θ_{ja}	θ_{jc}
Ceramic DIP	103	34
Plastic DIP	75	22

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

HARRIS

HI-546/547

Single 16/Differential 8 Channel CMOS Analog Multiplexers with Active Overvoltage Protection

Features

- Analog Overvoltage Protection ..... $70V_{p-p}$
- No Channel Interaction During Overvoltage
- ESD Resistant ..... >4,000V
- Guaranteed R_{ON} Matching
- 44V Maximum Power Supply
- Break-Before-Make Switching
- Analog Signal Range ..... ±15V
- Access Time (Typical) 500ns
- Standby Power (Typical) 7.5mW

Applications

- Data Acquisition
- Industrial Controls
- Telemetry

Description

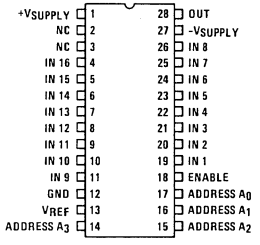
The HI-546 and HI-547 are analog multiplexers with Active Overvoltage Protection and guaranteed R_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. Digital inputs will also sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-546 and HI-547 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The HI-546 is a 16 channel device and the HI-547 is a 8 channel differential version. If input overvoltage protection is not needed, the HI-506 and HI-507 multiplexers are recommended. For further information see Application Notes 520 and 521.

The HI-546/547 are offered in both commercial and military grades. Additional Hi-Rel screening to MIL-STD-883 is available when specified by the "/883" suffix. For details, request the HI-546/883 or HI-547/883 data sheets.

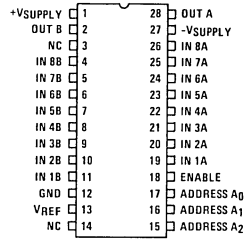
Each device is available in a 28 pin Plastic or Ceramic DIP, and a 28 pin Plastic Leaded Chip Carrier (PLCC).

Pinouts

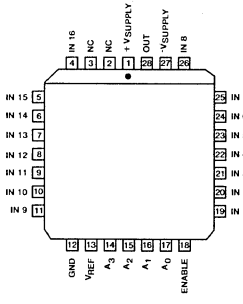
HI1-546 (CERAMIC DIP)
HI3-546 (PLASTIC DIP)
TOP VIEW



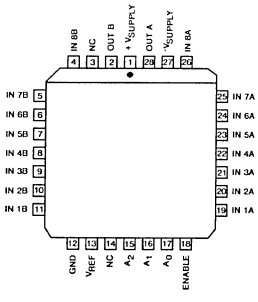
HI1-547 (CERAMIC DIP)
HI3-547 (PLASTIC DIP)
TOP VIEW



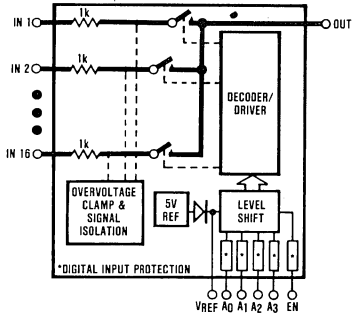
HI4P546 (PLCC)
TOP VIEW



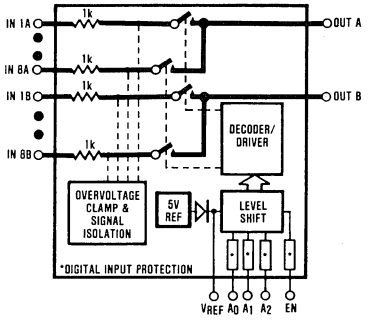
HI4P547 (PLCC)
TOP VIEW



Functional Diagrams



HI-546



HI-547

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Specifications HI-546/547

Absolute Maximum Ratings (Note 1)

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ 44V
$V_{SUPPLY(+)}$ to GND 22V
$V_{SUPPLY(-)}$ to GND 25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first.
Analog Signal Overvoltage (Note 7)
$+V_S$ ..... $+V_{SUPPLY}$ +20V
$-V_S$ ..... $-V_{SUPPLY}$ -20V
Continuous Current, S or D: 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% duty cycle max): 40mA
Junction Temperature ..... +175°C
Operating Temperature Ranges:
HI-546/547-2 ..... -55°C to +125°C
HI-546/547-4 ..... -25°C to +85°C
HI-546/547-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications Unless Otherwise Specified:

Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-546/HI-547 -2 MIN.	HI-546/HI-547 -2 TYP.	HI-546/HI-547 -2 MAX.	HI-546/547 -4, -5 MIN.	HI-546/547 -4, -5 TYP.	HI-546/547 -4, -5 MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
R_{ON}, On Resistance (Note 2)	+25°C		1.2	1.5		1.5	1.8	kΩ
	Full		1.5	1.8		1.8	2.0	kΩ
ΔR_{ON}, Any Two Channels	+25°C			7.0			7.0	%
I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-546	Full			300			300	nA
HI-547	Full			200			200	nA
I_D (OFF), with Input Overvoltage Applied (Note 4)	+25°C		4.0			4.0		nA
	Full			2.0				μA
I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-546	Full			300			300	nA
HI-547	Full			200			200	nA
I_{DIFF}, Differential Off Output Leakage Current (HI-547 Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold TTL Drive	Full			0.8			0.8	V
V_{AH}, Input High Threshold (Note 8)	Full	4.0			4.0			V
V_{AL} MOS Drive (Note 9)	+25°C			0.8			0.8	V
V_{AH} MOS Drive (Note 9)	+25°C	6.0			6.0			V
I_A, Input Leakage Current (High or Low) (Note 5)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5			0.5		μs
	Full			1.0			1.0	μs
t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.01%)	+25°C		3.5			3.5		μs
"Off Isolation" (Note 6)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-546	+25°C		50			50		pF
HI-547	+25°C		25			25		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
I+, Current Pin 1 (Note 7)	Full		0.5	2.0		0.5	2.0	mA
I−, Current Pin 27 (Note 7)	Full		0.02	1.0		0.02	1.0	mA

TRUTH TABLES

HI-546

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-547

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

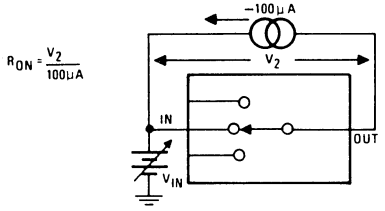
NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = -100μA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Analog Overvoltage = ±33V.
5. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
6. V_{EN} = 0.8V, R_L = 1K, C_L = 15pF, V_S = 7V_{RMS}, f = 100kHz.
7. V_{EN}, V_A = 0V or 4.0V.
8. To drive from DTL/TTL Circuits, 1kΩ pull-up resistors to +5.0V_{SUPPLY} are recommended.
9. V_{REF} = +10V.

Performance Characteristics and Test Circuits

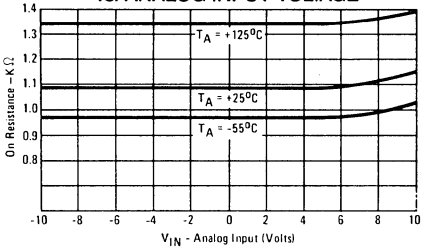
Unless Otherwise Specified: T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = +4 V, V_{AL} = 0.8 V And V_{Ref} = Open.

ON RESISTANCE vs.
INPUT SIGNAL LEVEL, SUPPLY VOLTAGE

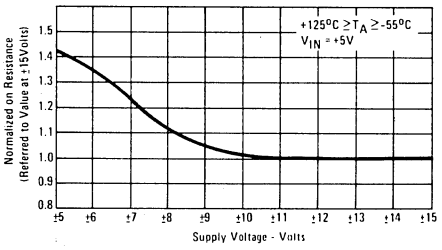
TEST CIRCUIT NO. 1



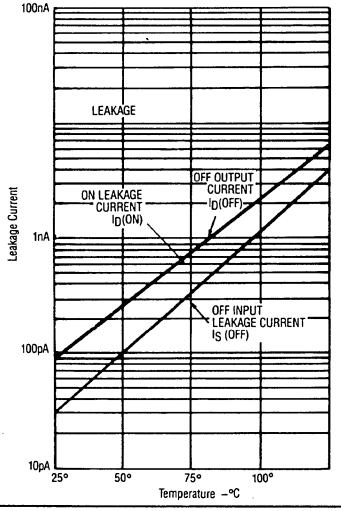
ON RESISTANCE
vs. ANALOG INPUT VOLTAGE



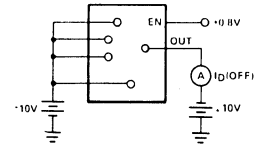
NORMALIZED ON RESISTANCE
vs. SUPPLY VOLTAGE



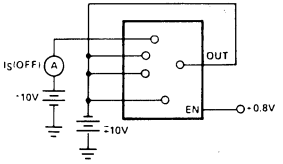
LEAKAGE CURRENT VS. TEMPERATURE



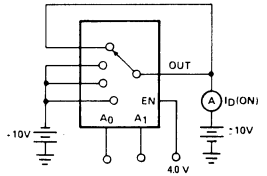
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

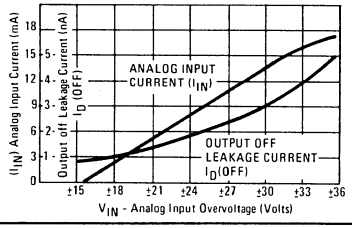


TEST CIRCUIT NO. 4*



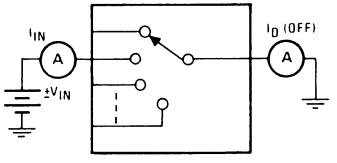
***Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for $I_{D(OFF)}$: +10 V/−10 V and −10 V/+10 V.)**

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



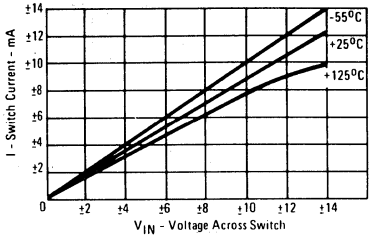
TEST CIRCUIT NO. 5

ANALOG INPUT
OVERVOLTAGE CHARACTERISTICS



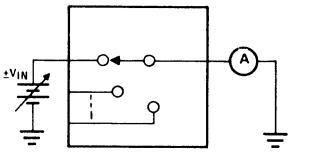
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

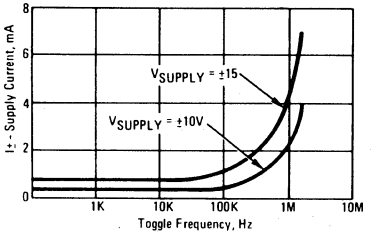


TEST CIRCUIT NO. 6

ON CHANNEL CURRENT vs. VOLTAGE

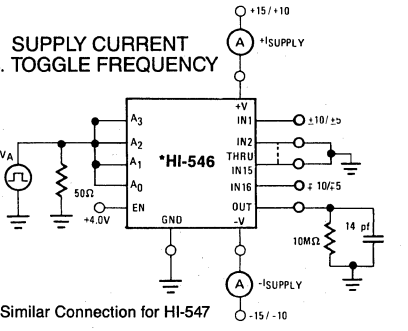


SUPPLY CURRENT vs. TOGGLE FREQUENCY



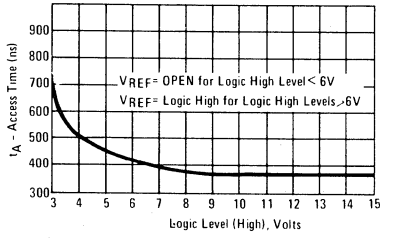
TEST CIRCUIT NO. 7

SUPPLY CURRENT vs. TOGGLE FREQUENCY



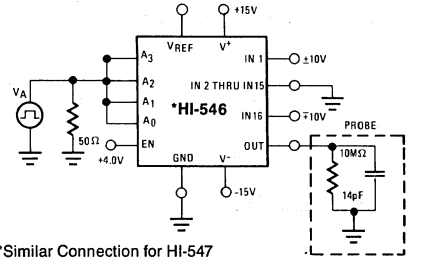
*Similar Connection for HI-547

ACCESS TIME VS. LOGIC LEVEL (HIGH)



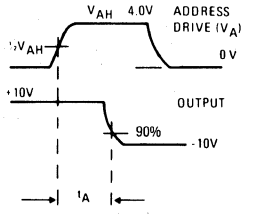
TEST CIRCUIT NO. 8

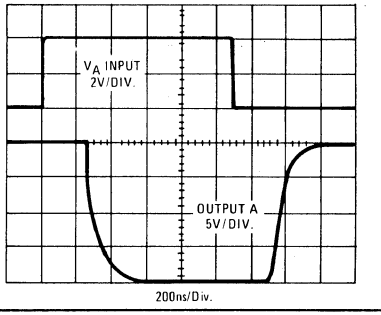
ACCESS TIME vs. LOGIC LEVEL (HIGH)



*Similar Connection for HI-547

Switching Waveforms

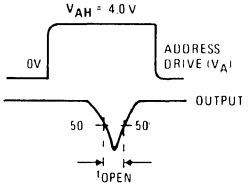


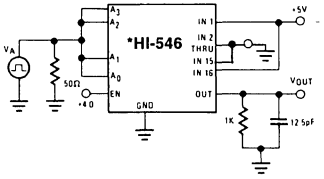


Switching Waveforms (continued)

TEST CIRCUIT NO. 9

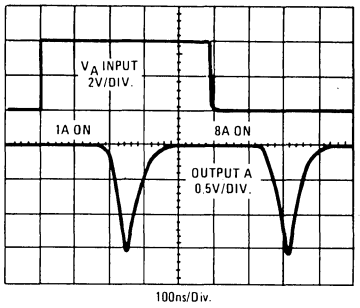
BREAK-BEFORE-MAKE DELAY (tOPEN)





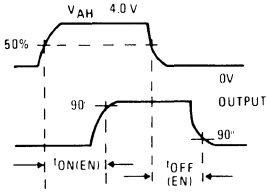
*Similar Connection for HI-547

BREAK-BEFORE-MAKE DELAY(tOPEN)

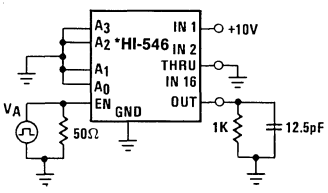


TEST CIRCUIT NO. 10

ENABLE DRIVE

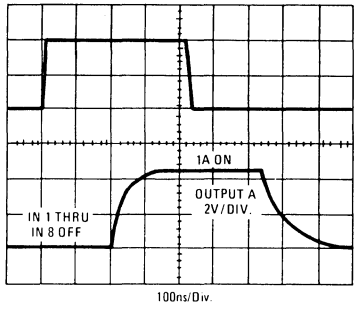


ENABLE DELAY (tON(EN),tOFF(EN))

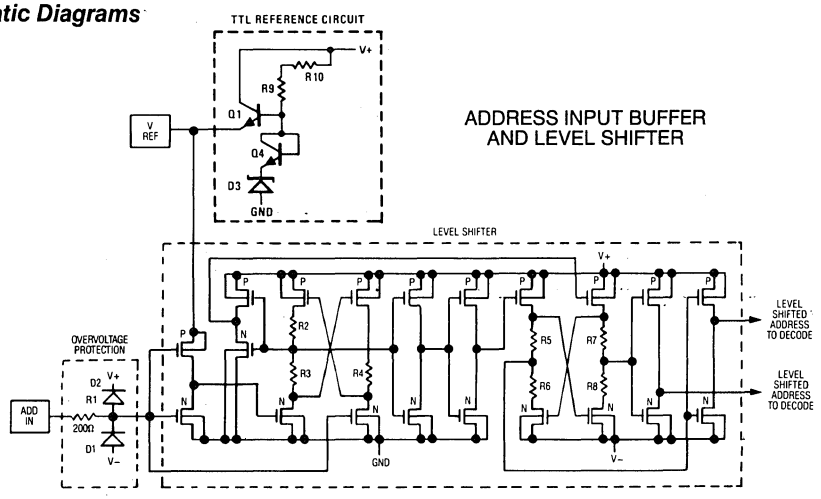


*Similar Connection for HI-547

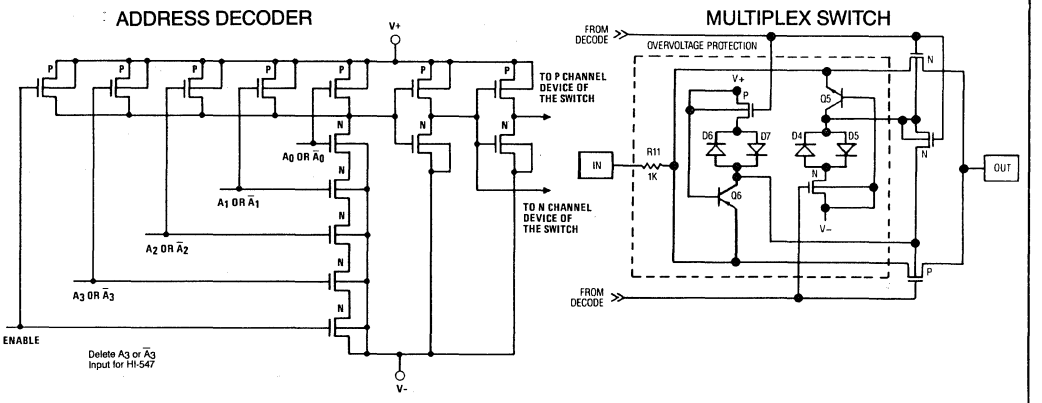
ENABLE DELAY (tON(EN),tOFF(EN))



Schematic Diagrams



Schematic Diagrams (continued)



Die Characteristics

Transistor Count		485
Die Dimensions		159 x 84 mils
Substrate Potential*		$-V_{SUPPLY}$
Process		CMOS-DI
Thermal Constants ($^oC/W$)	θ_{ja}	θ_{jc}
Ceramic DIP	50	18

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0546-4	-25°C to +85°C	28-Pin CERDIP
HI1-0546-5	0°C to +75°C	28-Pin CERDIP
HI1-0546-2	-55°C to +125°C	28-Pin CERDIP
HI3-0546-5	0°C to +75°C	28-Pin Plastic DIP
HI4P0546-5	0°C to +75°C	28-Pin PLCC
HI1-0547-4	-25°C to +85°C	28-Pin CERDIP
HI1-0547-2	-55°C to +125°C	28-Pin CERDIP
HI1-0547-5	0°C to +75°C	28-Pin CERDIP
HI4P0547-5	0°C to +75°C	28-Pin PLCC
HI3-0547-5	0°C to +75°C	28-Pin Plastic

HARRIS

HI-548/549

Single 8/Differential 4 Channel CMOS Analog Multiplexers with Active Overvoltage Protection

Features

- Analog Overvoltage Protection ..... $70V_{p-p}$
- No Channel Interaction During Overvoltage
- ESD Resistant ..... >4,000V
- Guaranteed RON Matching
- 44V Maximum Power Supply
- Break-Before-Make Switching
- Analog Signal Range ..... ±15V
- Access Time (Typical) 500ns
- Standby Power (Typical) 7.5mW

Applications

- Data Acquisition
- Industrial Controls
- Telemetry

Description

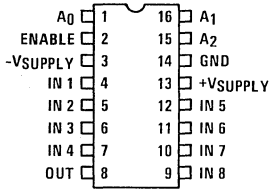
The HI-548 and 549 are analog multiplexers with Active Overvoltage Protection and guaranteed R_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels and typically survive static discharges beyond 4,000 volts. Digital inputs will also sustain continous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents 1kΩ of resistance under this condition. These features make the HI-548 and HI-549 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The HI-548 is an 8 channel device and the HI-549 is a 4 channel differential version. If input overvoltage protection is not needed, the HI-508 and HI-509 multiplexers are recommended. For further information see Application Notes 520 and 521.

The HI-548/549 are offered in both commercial and military grades. Additional Hi-Rel screening to MIL-STD-883 is available, when specified by the "/883" suffix. For details, request the HI-548/883 or HI-549/883 data sheets.

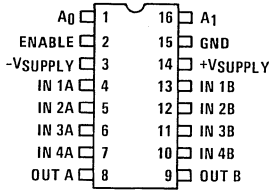
Each device is available in a 16 pin Plastic or Ceramic DIP, and a 20 pin Plastic Leaded Chip Carrier (PLCC).

Pinouts

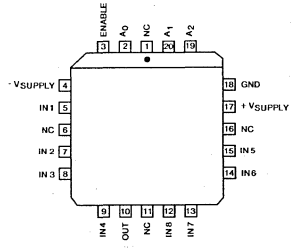
HI1-548 (CERAMIC DIP)
HI3-548 (PLASTIC DIP)
TOP VIEW



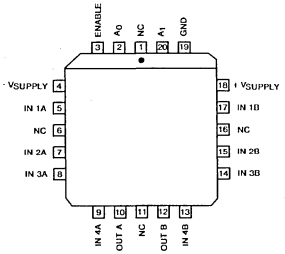
HI1-549 (CERAMIC DIP)
HI3-549 (PLASTIC DIP)
TOP VIEW



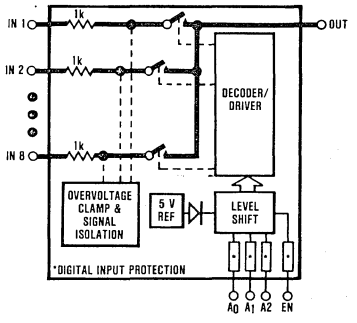
HI4P548 (PLCC)
TOP VIEW



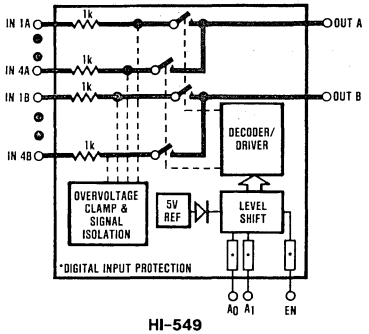
HI4P549 (PLCC)
TOP VIEW



Functional Diagrams



HI-548



HI-549

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Specifications HI-548/549

Absolute Maximum Ratings (Note 1)

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ 44V
$V_{SUPPLY(+)}$ to GND 22V
$V_{SUPPLY(-)}$ to GND 25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first.
Analog Signal Overvoltage (Note 7)
$+V_S$ ..... $+V_{SUPPLY}$ +20V
$-V_S$ ..... $-V_{SUPPLY}$ -20V
Continuous Current, S or D: 20mA
Peak Current, S or D
(Pulsed at 1ms, 10% duty cycle max): 40mA
Junction Temperature ..... +175°C
Operating Temperature Ranges:
HI-548/549-2 ..... -55°C to +125°C
HI-548/549-4 ..... -25°C to +85°C
HI-548/549-5 ..... 0°C to +75°C
Storage Temperature Range ..... -65°C to +150°C

Electrical Specifications Unless Otherwise Specified:

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V;
V_{AL} (Logic Level Low) = +0.8V. For Test Conditions, consult Performance Characteristics Section.

PARAMETER	TEMP.	HI-548/HI-549 -2 MIN.	HI-548/HI-549 -2 TYP.	HI-548/HI-549 -2 MAX.	HI-548/549 -4, -5 MIN.	HI-548/549 -4, -5 TYP.	HI-548/549 -4, -5 MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 2)	+25°C		1.2	1.5		1.5	1.8	kΩ
	Full		1.5	1.8		1.8	2.0	kΩ
$\triangle R_{ON}$, Any Two Channels	+25°C			7.0			7.0	%
I_S (OFF), Off Input Leakage Current (Note 3)	+25°C		0.03			0.03		nA
	Full			50			50	nA
I_D (OFF), Off Output Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-548	Full			200			200	nA
HI-549	Full			100			100	nA
$I_{D(OFF)}$ with Input Overvoltage Applied (Note 4)	+25°C		4.0			4.0		nA
	Full			2.0				μA
I_D (ON), On Channel Leakage Current (Note 3)	+25°C		0.1			0.1		nA
HI-548	Full			200			200	nA
HI-549	Full			100			100	nA
I_{DIFF}, Differential Off Output Leakage Current (HI-549 Only)	Full			50			50	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold (Note 8)	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	4.0			4.0			V
I_A, Input Leakage Current (High or Low) (Note 5)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5			0.5		μs
	Full			1.0			1.0	μs
t_{OPEN}, Break-Before-Make Delay	+25°C	25	80		25	80		ns
t_{ON} (EN), Enable Delay (ON)	+25°C		300	500		300		ns
	Full			1000			1000	ns
t_{OFF} (EN), Enable Delay (OFF)	+25°C		300	500		300		ns
	Full			1000			1000	ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.01%)	+25°C		3.5			3.5		μs
"OFF Isolation" (Note 6)	+25°C	50	68		50	68		dB
C_S (OFF), Channel Input Capacitance	+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance HI-548	+25°C		25			25		pF
HI-549	+25°C		12			12		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
I+, Current (Note 7)	Full		0.5	2.0		0.5	2.0	mA
I−, Current (Note 7)	Full		0.02	1.0		0.02	1.0	mA

TRUTH TABLES

HI-548

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-549

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

NOTES:

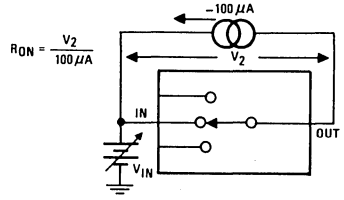
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = -100μA.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Analog Overvoltage = ±33V.
5. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at 25°C.
6. V_{EN} = 0.8V, R_L = 1K, C_L = 15pF, V_S = $7V_{RMS}$, f = 100kHz. Worst case isolation occurs on channel 4 due to proximity of the output pins.
7. V_{EN}, V_A = 0V or 4.0V.
8. To drive from DTL/TTL Circuits, 1kΩ pull-up resistors to $+5.0V_{SUPPLY}$ are recommended.

Performance Characteristics and Test Circuits

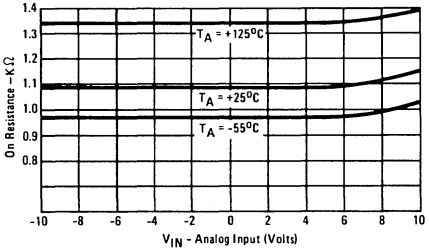
Unless Otherwise Specified T_A = 25°C, V_{Supply} = ±15 V, V_{AH} = +4 V, V_{AL} = 0.8 V

TEST CIRCUIT NO. 1

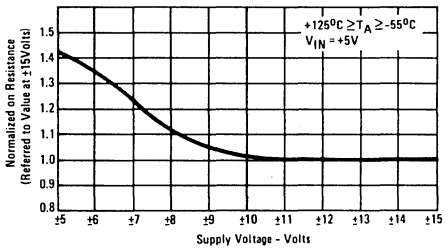
ON RESISTANCE vs. INPUT SIGNAL LEVEL, SUPPLY VOLTAGE



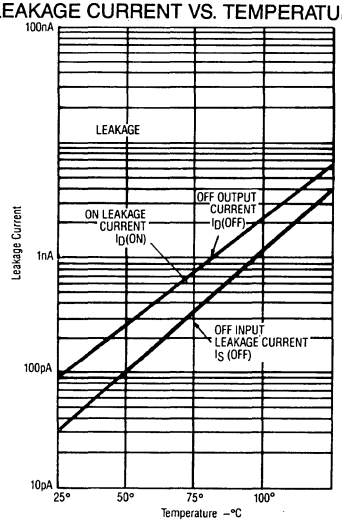
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



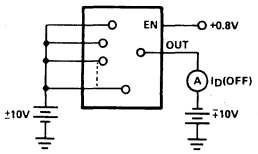
NORMALIZED ON RESISTANCE vs. SUPPLY VOLTAGE



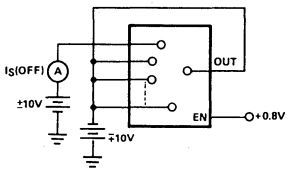
LEAKAGE CURRENT VS. TEMPERATURE



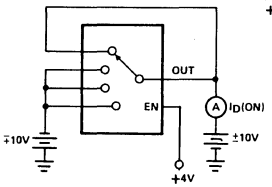
TEST CIRCUIT NO. 2*



TEST CIRCUIT NO. 3*

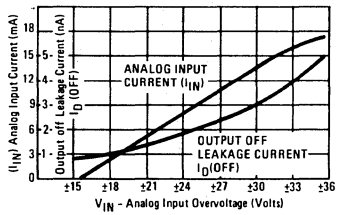


TEST CIRCUIT NO. 4*



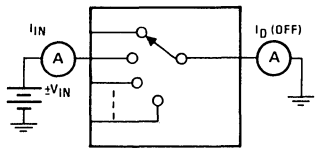
*Two measurements per channel: +10 V/−10 V and −10 V/+10 V. (Two measurements per device for $I_{D(OFF)}$: +10 V/−10 V and −10 V/+10 V.)

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



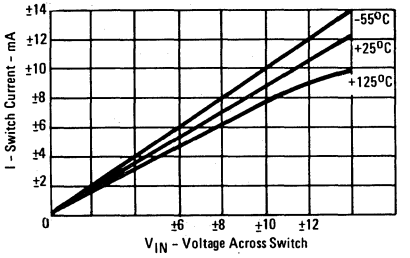
TEST CIRCUIT NO. 5

ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



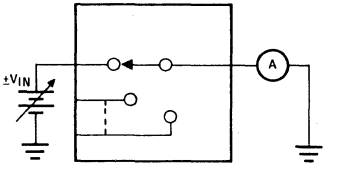
Performance Characteristics and Test Circuits (continued)

ON CHANNEL CURRENT vs. VOLTAGE

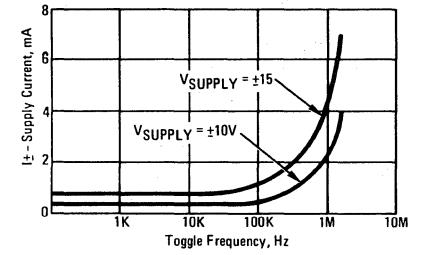


TEST CIRCUIT NO. 6

ON CHANNEL CURRENT vs. VOLTAGE

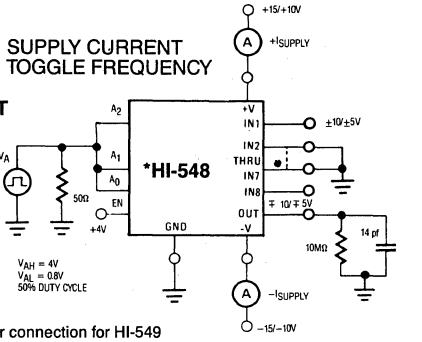


SUPPLY CURRENT vs. TOGGLE FREQUENCY



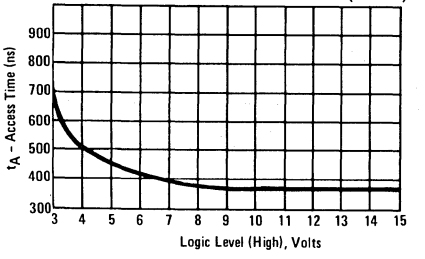
TEST CIRCUIT NO. 7

SUPPLY CURRENT vs. TOGGLE FREQUENCY



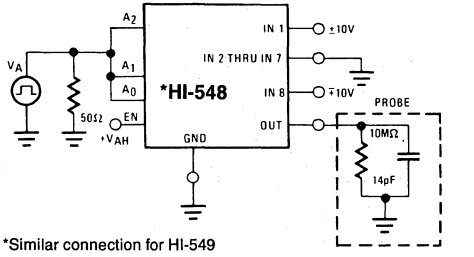
*Similar connection for HI-549

ACCESS TIME VS. LOGIC LEVEL (HIGH)



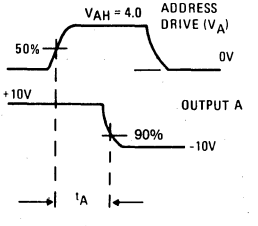
TEST CIRCUIT NO. 8

ACCESS TIME vs. LOGIC LEVEL (HIGH)

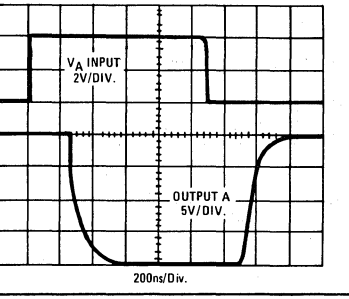


*Similar connection for HI-549

Switching Waveforms



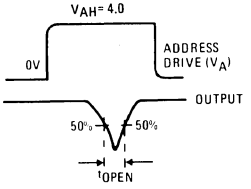
ACCESS TIME

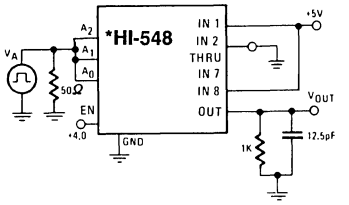


Switching Waveforms (continued)

TEST CIRCUIT NO. 9

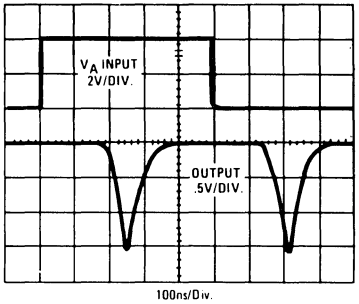
BREAK-BEFORE-MAKE DELAY(tOPEN)





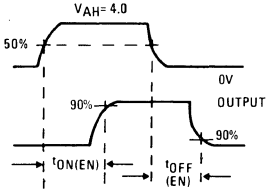
*Similar connection for HI-549

BREAK-BEFORE-MAKE DELAY (tOPEN)

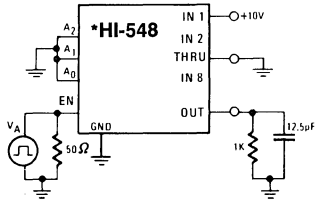


TEST CIRCUIT NO. 10

ENABLE DRIVE

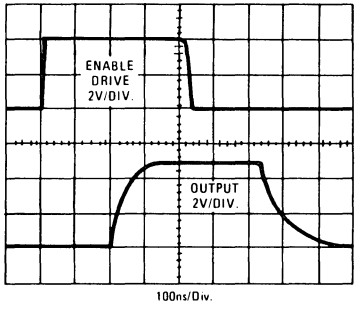


ENABLE DELAY (tON(EN),tOFF(EN))

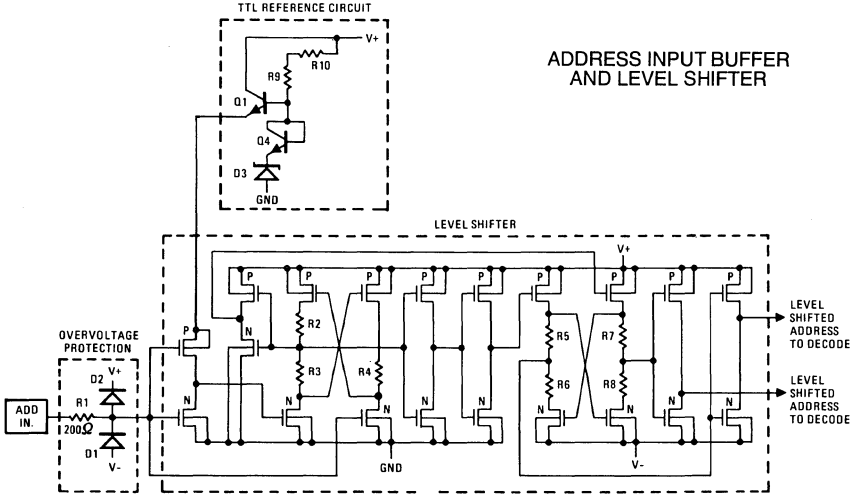


*Similar connection for HI-549

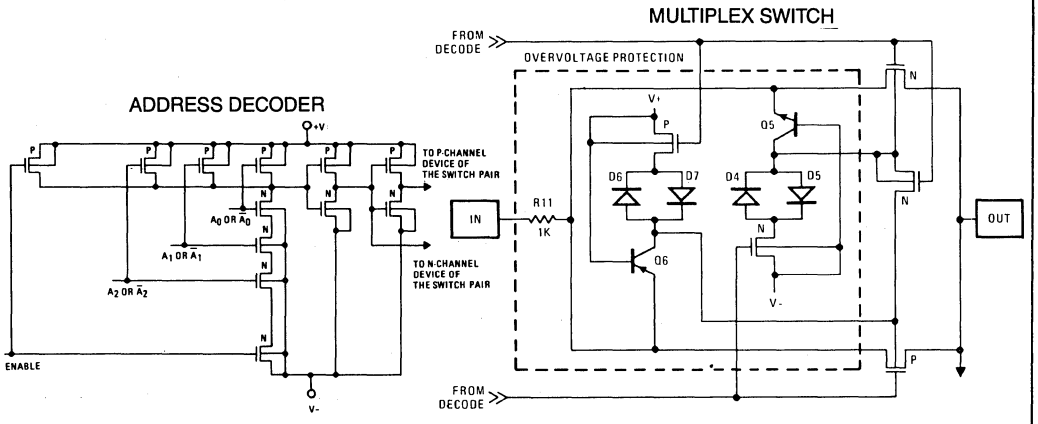
ENABLE DELAY (tON(EN),tOFF(EN))



Schematic Diagrams



Schematic Diagrams (continued)



Die Characteristics

Transistor Count 253
Die Dimensions ..... 108 x 83 mils
Substrate Potential* ..... $-V_{SUPPLY}$
Process ..... CMOS-DI

Thermal Constants (°C/W)	θ_{ja}	θ_{jc}
Ceramic DIP	104	35
Plastic DIP	75	23

*The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI3-0548-5	0°C to +75°C	16-Pin Plastic DIP
HI4P0548-5	0°C to +75°C	20-Pin PLCC
HI1-0548-2	-55°C to +125°C	16-Pin CERDIP
HI1-0548-4	-25°C to +85°C	16-Pin CERDIP
HI1-0548-5	0°C to +75°C	16-Pin CERDIP
HI1-0549-5	0°C to +75°C	16-Pin CERDIP
HI1-0549-4	-25°C to +85°C	16-Pin CERDIP
HI1-0549-2	-55°C to +125°C	16-Pin CERDIP
HI3-0549-5	0°C to +75°C	16-Pin Plastic DIP
HI4P0549-5	0°C to +75°C	20-Pin PLCC

HARRIS SEMICONDUCTOR

IH5108
8-Channel Fault Protected CMOS Analog Multiplexer

GENERAL DESCRIPTION

The IH5108 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the HI548 and similar devices, but adds fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ±25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc.

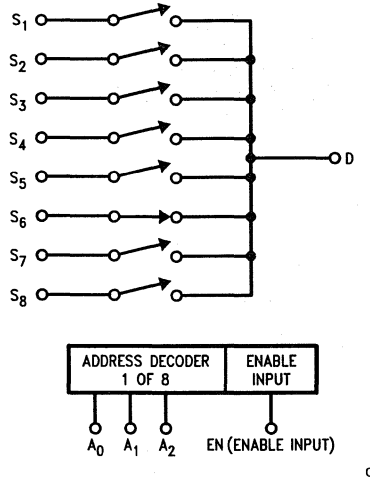
A binary 3-bit address code together with the ENable input allows selection of any one channel, or none at all. These 4 inputs are all TTL compatible for easy logic interface; the ENable input also facilitates MUX expansion and cascading.

FEATURES

- **All Channels OFF When Power OFF, for Analog Signals up to ±25V**
- **Power Supply Quiescent Current Less Than 1mA**
- **±13V Analog Signal Range**
- **No SCR Latchup**
- **Break-Before-Make Switching**
- **Pin Compatible With HI-548**
- **Any Channel Turns OFF if Input Exceeds Supply Rails by Up to ±25V**
- **TTL and CMOS Compatible Binary Address and ENable Inputs**

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH5108MJE	−55°C to +125°C	16 pin CERDIP
IH5108IJE	−25°C to +85°C	16 pin CERDIP
IH5108CPE	0°C to 70°C	16 pin plastic DIP



3 LINE BINARY ADDRESS INPUTS
(1 0 1) AND EN HI
ABOVE EXAMPLE SHOWS CHANNEL 6 TURNED ON

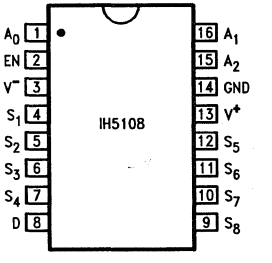
Figure 1: Functional Diagram

TRUTH TABLE

A_2	A_1	A_0	EN	On Switch
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2, EN
Logic "1" = $V_{AH} \geq 2.4V$
Logic "0" = $V_{AL} \leq 0.8V$

(outline dwg JE, PE)



V^+ Common to Substrate

Figure 2: Pin Configuration

304200-004

NOTE: All typical values have been characterized but are not tested.

IH5108

ABSOLUTE MAXIMUM RATINGS

V_{IN}(A, EN) to Ground ..... −15V to 15V
V_S or V_D to V^+ ..... +25V, −40V
V_S or V_D to V^- ..... −25V, +40V
V^+ to Ground 20V
V^- to Ground ..... −20V
Current (Any Terminal) 20mA
Operating Temperature
C Suffix .....0°C to +70°C
I Suffix .....−25°C to +85°C
M Suffix .....−55°C to +125°C

Storage Temperature
C Suffix .....−65°C to +125°C
I & M Suffix .....−65°C to +150°C
Lead Temperature (Soldering, 10 sec).....300°C
Power Dissipation*
CERDIP Package**.....900 mW
Plastic Package*** .....470 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 12 mW/°C above 75°C

***Derate 6.3 mW/°C above 75°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS ($V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.)

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions		Typ 25°C	Max Limits M Suffix −55°C	M Suffix 25°C	M Suffix 125°C	C Suffix −25°C/0°C	C Suffix 25°C	C Suffix 85°C/70°C	Units
SWITCH												
$R_{DS(ON)}$	S to D	8	$V_D = 10V$, $I_S = -100\mu A$	Sequence each switch on	900	1200	1200	1800	1500	1500	2000	Ω
		8	$V_D = -10V$, $I_S = -100\mu A$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$	900	1200	1200	1800	1500	1500	2000	
$\Delta R_{DS(ON)}$			$\Delta R_{DS(on)} = \frac{R_{DS(on)max} - R_{DS(on)min}}{R_{DS(on)avg.}}$, $V_S = \pm 10V$		5							%
$I_{S(off)}$	S	8	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0.8V$	±0.02		±0.5	±50		±1.0	±50	nA
		8	$V_S = -10V$, $V_D = 10V$		±0.02		±0.5	±50		±1.0	±50	
$I_{D(off)}$	D	1	$V_D = 10V$, $V_S = -10V$		±0.02		±1.0	±100		±2.0	±100	
		1	$V_D = -10V$, $V_S = 10V$		±0.05		±1.0	±100		±2.0	±100	
$I_{D(on)}$	D	8	$V_{S(All)} = V_D = 10V$	Sequence each switch on	±0.1		±2.0	±100		±5	±100	
		8	$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$, $V_{EN} = 2.4V$	±0.1		±2.0	±100		±5	±100	
FAULT												
I_S with Power OFF	S	8	$V_{SUPP} = 0V$, $V_{IN} = \pm 25V$, $V_{EN} = V_O = 0V$, $A_0, A_1, A_2 = 0V$		±1.0		±2.0			±5.0		μA
$I_{S(off)}$ with Overvoltage	S	8	$V_{IN} = \pm 25V$, $V_0 = \pm 10V$		±1.0		±5.0			±10		

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

($V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.) (Continued)

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions	Typ 25°C	Max Limits M Suffix −55°C	M Suffix 25°C	M Suffix 125°C	C Suffix −25°C/0°C	C Suffix 25°C	C Suffix 85°C/70°C	Units
INPUT											
$I_{EN(on)}$ $I_{A(on)}$ or $I_{EN(off)}$ $I_{A(off)}$	A_0, A_1, A_2 or EN	4	$V_A = 0V$	0.01		−10	−30		−10	−30	µA
		4	$V_A = 15V$	0.01		10	30		10	30	
DYNAMIC											
$t_{transition}$	D		See Figure 3	0.3		1					µs
t_{open}	D		See Figure 4	0.2							
$t_{on(EN)}$	D		See Figure 5	0.6		1.5					
$t_{off(EN)}$	D			0.4		1					
t_{on}-t_{off} Break-Before-Make Delay Settling Time	D	6	$V_{EN} = +5V$, A_0, A_1, A_2 Strobed $V_{IN} = \pm 10V$, see Figure 6	10							ns
"OFF" Isolation	D		$V_{EN} = 0V$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3$ VRMS, $f = 500kHz$	60							dB
$C_{s(off)}$	S		$V_S = 0V$; $V_{EN} = 0V$, $f = 140kHz$ to 1 MHz	5							pF
$C_{D(off)}$	D		$V_D = 0V$	25							
$C_{DS(off)}$	D to S		$V_S = 0V$, $V_D = 0V$	1							
SUPPLY											
Supply Current	I^+	1	$V_{EN} = 5V$ All $V_A = 0V/5V$	0.5	0.7	0.6	0.5		1.0		mA
	I^-	1		0.02	0.7	0.6	0.5		1.0		

Note 1. Readings taken 400ms after the overvoltage occurs.

SWITCHING TIME TEST CIRCUITS

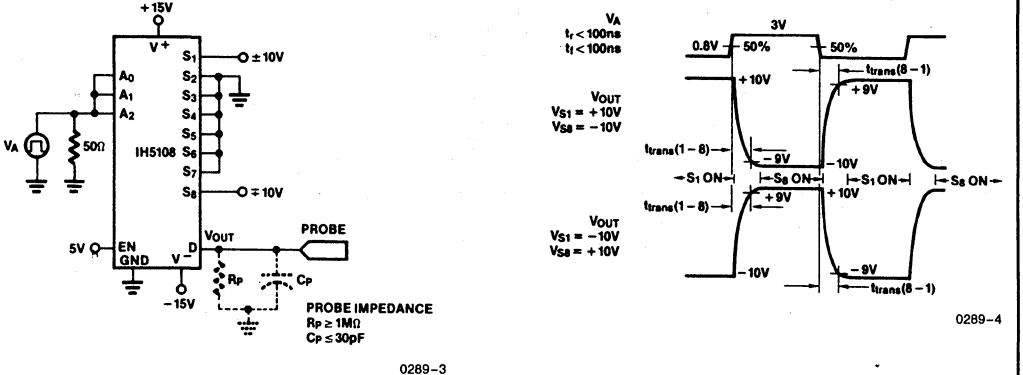


Figure 3: $t_{transition}$ Switching Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

SWITCHING TIME TEST CIRCUITS (Continued)

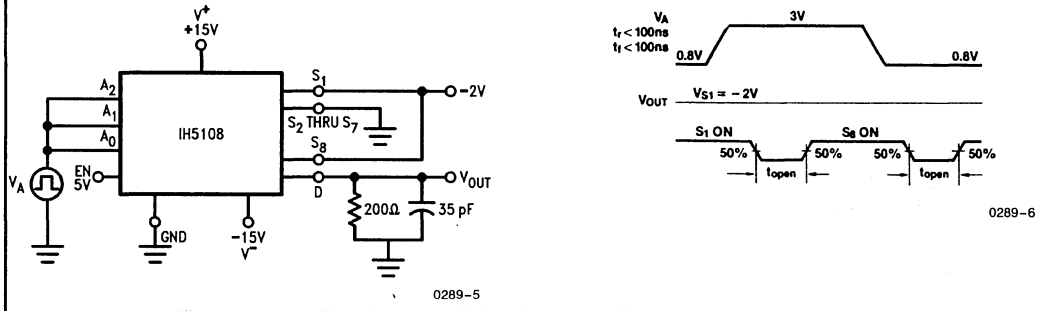


Figure 4: t_{open} (Break-Before-Make) Switching Test Circuit and Waveforms

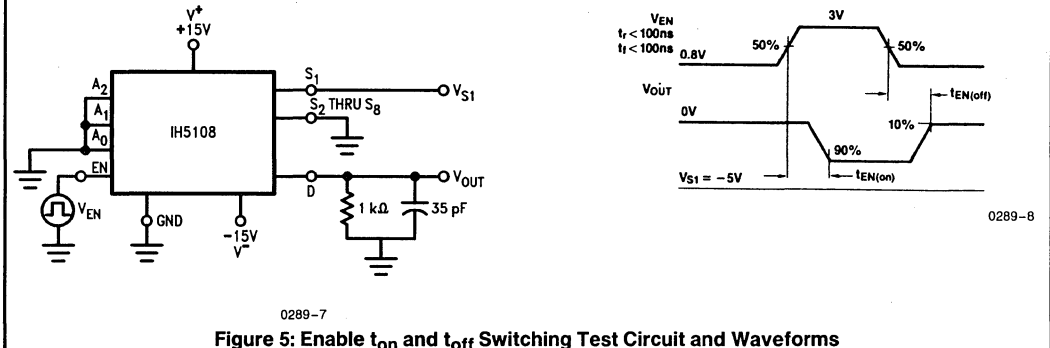


Figure 5: Enable t_{on} and t_{off} Switching Test Circuit and Waveforms

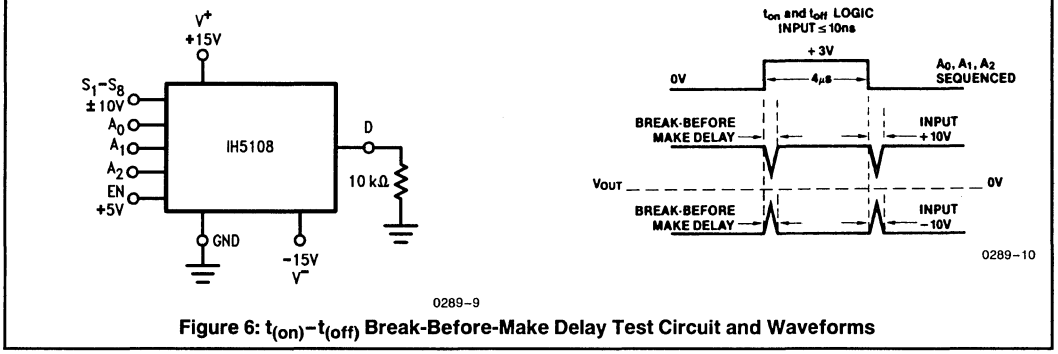


Figure 6: $t_{(on)}$-$t_{(off)}$ Break-Before-Make Delay Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

The IH5108, like all Harris multiplexers, contains a set of CMOS switches that form the channels, and driver and decoder circuitry to control which channel turns ON, if any. In addition, the IH5108 contains an internal regulator which provides a fully TTL compatible ENable input that is identical in operation to the Address inputs. This does away with the special conditions that many multiplexer enable inputs require for proper logic swings. The identical circuit conditions of the ENable and Address lines also helps ensure the extension of break-before-make switching to wider multiplexer systems (see applications section).

Another, and more important difference lies in the switching channel. Previous devices have used parallel n- and p-channel MOSFET switches. While this scheme yields reasonably good ON resistance characteristics and allows the switching of rail-to-rail input signals, it also has a number of drawbacks. The sources and drains of the switch transistors will conduct to the substrate if the input goes outside the supply rails, and even careful use of diodes cannot avoid channel-to-output and channel-to-channel coupling in cases of input overrange. The IH5108 uses a novel series arrangement of the p- and n-channel switches (Figure 7) combined with a dielectrically isolated process to eliminate these problems.

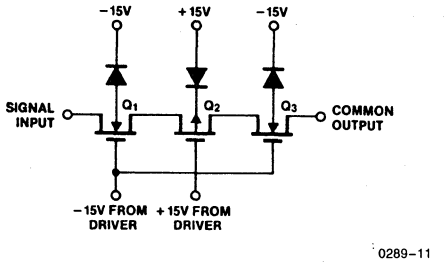
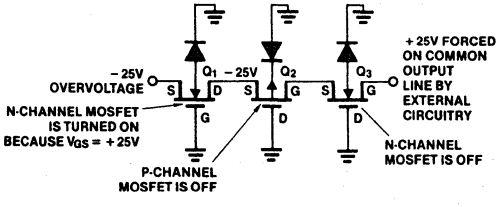
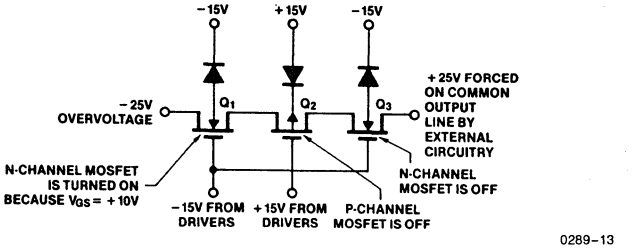


Figure 7: Series Connection of Channel Switches

Within the normal analog signal range, the inherent variation of switch ON resistance will balance out almost as well as the customary parallel configuration, but as the analog signal approaches either supply rail, even for an ON channel, either the p- or the n-channel will become a source follower, disconnecting the channel (Figure 8). Thus protection is provided for any input or output channel against overvoltage, even in the absence of multiplexer supply voltages. This applies up to the breakdown voltage of the respective switches. Figure 9 shows a more detailed schematic of the channel switches, including the back-gate driver devices which ensure optimum channel ON resistances and breakdown voltage under the various conditions.



(a) OVERVOLTAGE WITH MUX POWER OFF



(b) OVERVOLTAGE WITH MUX POWER ON

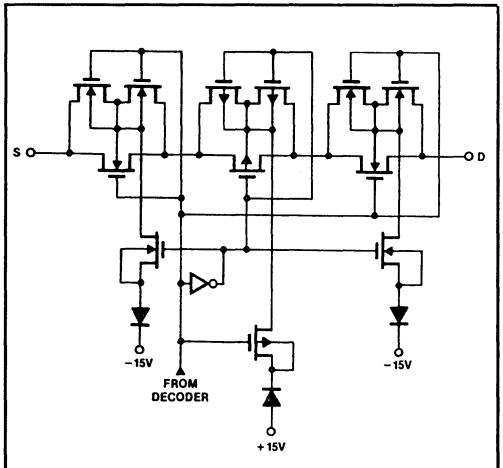
Figure 8: Overvoltage Protection

NOTE: All typical values have been characterized but are not tested.

IH5108

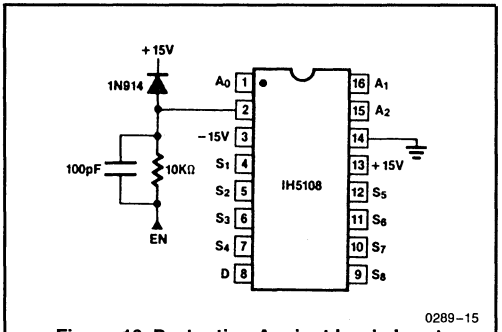
DETAILED DESCRIPTION (Continued)

Under some circumstances, if the logic inputs are present but the multiplexer supplies are not, the circuit will use the logic inputs as a sort of phantom supply; this could result in an output up to that logic level. To prevent this from occurring, simply ensure that the ENable pin is LOW any time the multiplexer supply voltages are missing (Figure 10).



0289-14

Figure 9: Detailed Channel Switch Schematic



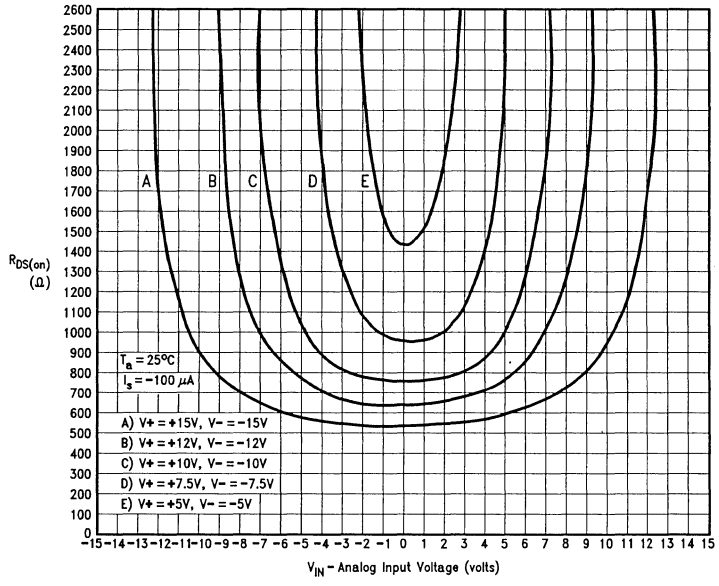
0289-15

Figure 10: Protection Against Logic Input

MAXIMUM SIGNAL HANDLING CAPABILITY

The IH5108 is designed to handle signals in the ±10V range, with a typical $r_{DS(on)}$ of 900Ω; it can successfully handle signals up to ±12V, however, $r_{DS(on)}$ will increase to about 1.8kΩ. Beyond ±12V the device approaches an open circuit, and thus ±12V is about the practical limit, see Figure 11.

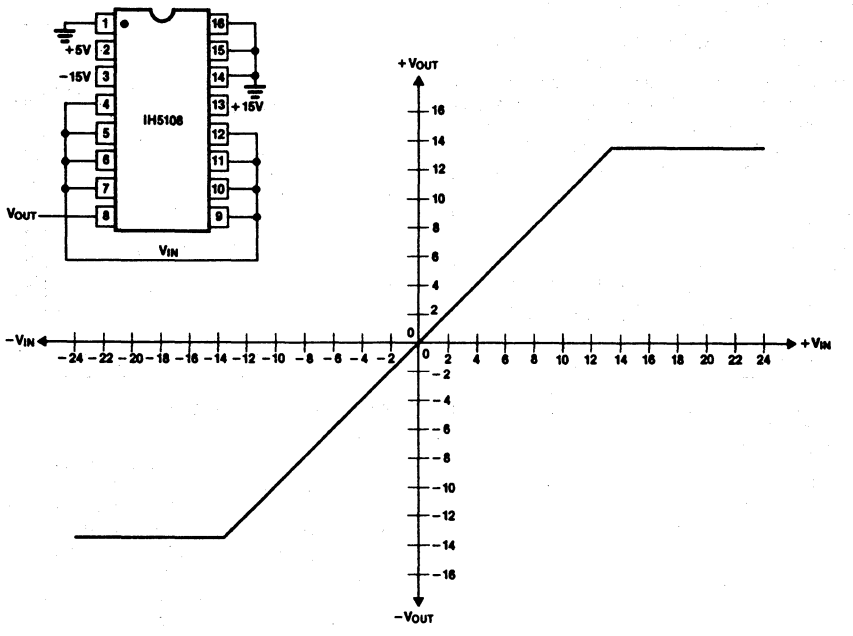
Figure 12 shows the input/output characteristics of an ON channel, illustrating the inherent limiting action of the series switch connection (see Detailed Description), while Figure 13 gives the ON resistance variation with temperature.



0289-16

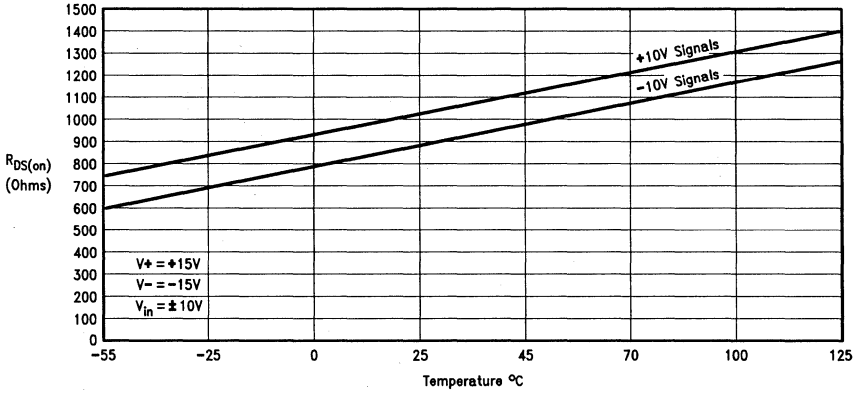
Figure 11: $R_{DS(on)}$ vs Analog Signal Voltage

NOTE: All typical values have been characterized but are not tested.



0289-17

Figure 12: MUX Output Voltage vs Input Voltage (Channel 1 Shown; All Channels Similar)



0289-18

Figure 13: Typical $r_{DS(on)}$ Variation With Temperature

NOTE: All typical values have been characterized but are not tested.

USING THE IH5108 WITH SUPPLIES OTHER THAN ±15V

The IH5108 will operate successfully with supply voltages from ±5V to ±15V, however $r_{DS(on)}$ increases as supply voltage decreases, as shown in Figure 11. Leakage currents, on the other hand, decrease with a lowering of supply voltage, and therefore the error term product of $r_{DS(on)}$ and leakage current remains reasonably constant. $r_{DS(on)}$ also decreases as signal levels decrease. For high system accuracy [acceptable levels of $r_{DS(on)}$] the maximum input signal should be 3V less than the supply voltages. The logic levels remain TTL compatible.

APPLICATION NOTES

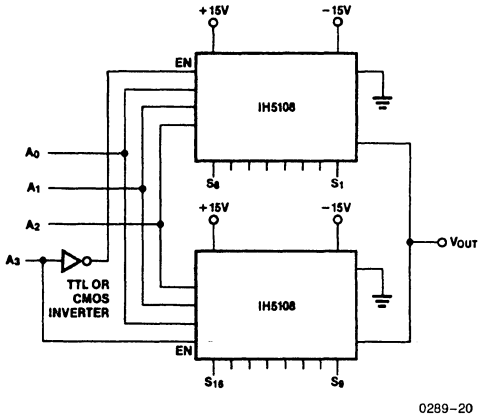
Further information may be found in:

A003 "Understanding and Applying the Analog Switch"

A006 "A New CMOS Analog Gate Technology"

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing"

IH5108 APPLICATIONS INFORMATION



TRUTH TABLE

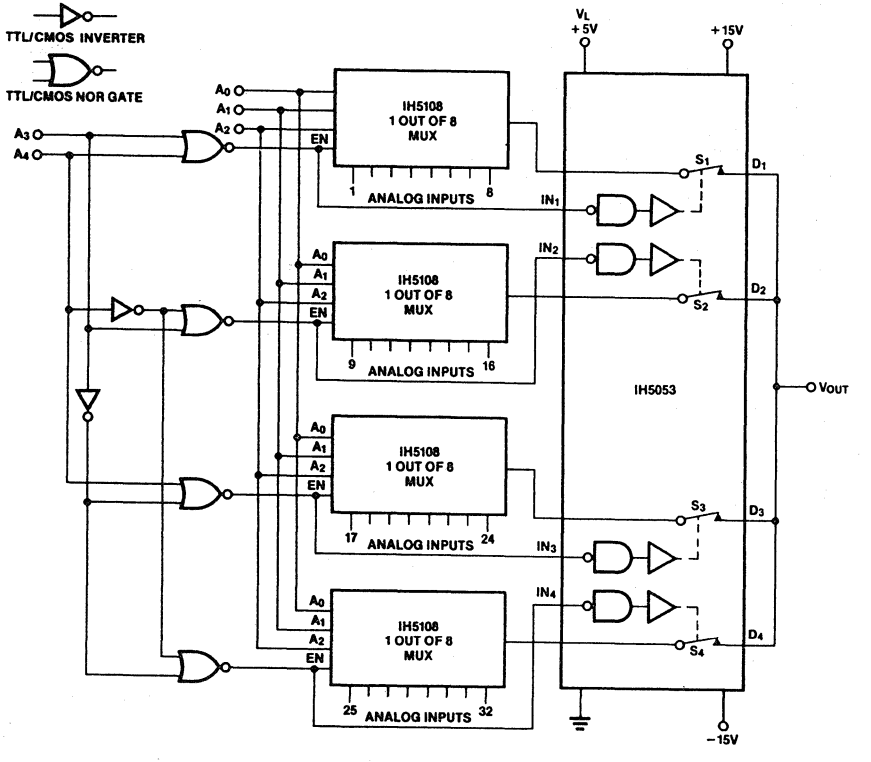
A_3	A_2	A_1	A_0	On Switch
0	0	0	0	S1
0	0	0	1	S2
0	0	1	0	S3
0	0	1	1	S4
0	1	0	0	S5
0	1	0	1	S6
0	1	1	0	S7
0	1	1	1	S8
1	0	0	0	S9
1	0	0	1	S10
1	0	1	0	S11
1	0	1	1	S12
1	1	0	0	S13
1	1	0	1	S14
1	1	1	0	S15
1	1	1	1	S16

Figure 14: 1 of 16 Channel Multiplexer Using Two IH5108s. Overvoltage Protection Is Maintained Between All Channels, As Is Break-Before-Make Switching.

8

NOTE: All typical values have been characterized but are not tested.

IH5108 APPLICATIONS INFORMATION (Continued)



TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	On Switch
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	On Switch
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 15: 1 Of 32 Multiplexer Using 4 IH5108s and An IH5053 As A Submultiplexer. Note That The IH5053 Is Protected Against Overvoltages By The IH5108s. Submultiplexing Reduces Output Leakage and Capacitance.

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

IH5116
16-Channel Fault Protected CMOS Analog Multiplexer

GENERAL DESCRIPTION

The IH5116 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the HI546 and similar devices, but adding fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ±25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc. Cross talk onto "good" channels is also prevented.

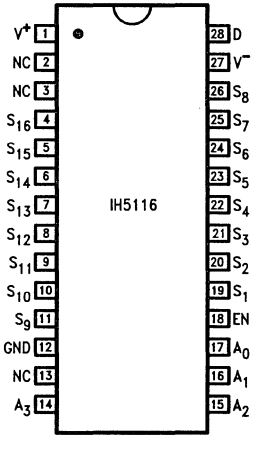
A binary 4-bit address code together with the ENable input allows selection of any channel or none at all. These 5 inputs are all TTL compatible for easy logic interface. The ENable input also facilitates MUX expansion and cascading.

FEATURES

- **All Channels OFF When Power OFF, for Analog Signals Up to ±25V**
- **Power Supply Quiescent Current Less Than 1mA**
- **±13V Analog Signal Range**
- **No SCR Latchup**
- **Break-Before-Make Switching**
- **TTL and CMOS Compatible Strobe Control**
- **Pin Compatible With HI546**
- **Any Channel Turns OFF If Input Exceeds Supply Rails By Up to ±25V**
- **TTL and CMOS Compatible Binary Address and ENable Inputs**

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH5116MJI	−55°C to +125°C	28 pin CERDIP
IH5116CJI	0°C to +70°C	28 pin CERDIP
IH5116CPI	0°C to +70°C	28 pin Plastic DIP



TOP VIEW

V+ COMMON TO SUBTRATE

Figure 1: Pin Configuration (Outline dwg JI, PI)

TRUTH TABLE

A_3	A_2	A_1	A_0	EN	On Switch
X	X	X	X	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Logic "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 2.4V$

Logic "0" = $V_{AL} \leq 0.8V$

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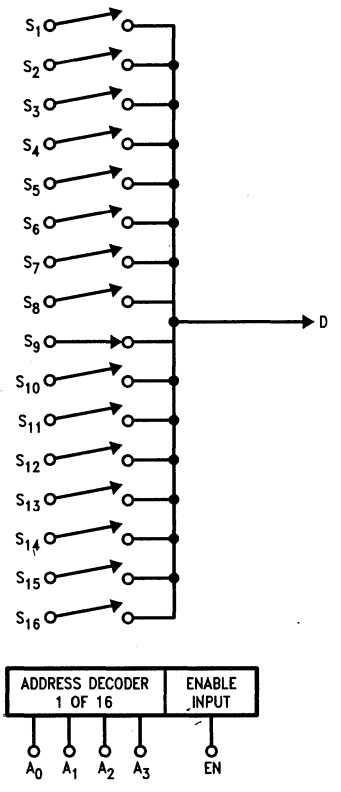
NOTE: All typical values have been characterized but are not tested.



4 LINE BINARY ADDRESS INPUTS
(0001) AND EN = 5V
ABOVE EXAMPLE SHOWS CHANNELS 9
TURNED ON.

Figure 2: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V to +15V
V_S or V_D to V^+ ..... +25V to −40V
V_S or V_D to V^- ..... −25V to +40V
V^+ to Ground 20V
V^- to Ground ..... −20V
Current (Any Terminal) 20mA
Operating Temperature
C Suffix .....0°C to +70°C
M Suffix .....−55°C to +125°C
Storage Temperature ..... −65 to +150°C
Storage Temperature
C Suffix .....−65°C to +125°C
M Suffix .....−65°C to +150°C
Lead Temperature (Soldering, 10 Sec.) .....300°C
Power Dissipation*
28-Pin CERDIP Package** .....1200 mW
28-Pin Plastic Package*** .....625 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 16 mW/°C above 75°C

***Derate 8.3 mW/°C above 75°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS ($V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.)

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions		Typ 25°C	Max Limits M Suffix −55°C	M Suffix 25°C	M Suffix 125°C	C Suffix 0°C	C Suffix 25°C	C Suffix 70°C	Units
SWITCH												
$R_{DS(on)}$	S to D	16	$V_D = 10V$, $I_S = -100\mu A$	Sequence each switch on	900	1200	1200	1800	1500	1500	2000	Ω
		16	$V_D = -10V$ $I_S = -100\mu A$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$	900	1200	1200	1800	1500	1500	2000	
$\Delta R_{DS(on)}$			$\Delta R_{DS(on)} = \frac{R_{DS(on)max} - R_{DS(on)min}}{R_{DS(on)avg.}}$ $V_S = \pm 10V$		5							%
$I_{S(off)}$	S	16	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0.8V$	±0.02		±0.5	±50		±1.0	±50	nA
		16	$V_S = -10V$, $V_D = 10V$		±0.02		±0.5	±50		±1.0	±50	
$I_{D(off)}$	D	1	$V_D = 10V$, $V_S = -10V$		±0.05		±1.0	±100		±2.0	±100	
		1	$V_D = -10V$, $V_S = 10V$		±0.05		±1.0	±100		±2.0	±100	
$I_{D(on)}$	D	16	$V_{S(All)} = V_D = 10V$	Sequence each switch on	±0.1		±2.0	±100		±4.0	±100	
		16	$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$	±0.1		±2.0	±100		±4.0	±100	
FAULT												
I_S with Power OFF	S	16	$V_{SUPP} = 0V$, $V_{IN} = \pm 25V$, $V_{EN} = V_O = 0V$, $A_0, A_1, A_2 = 0V$ or 5V		±1.0		±2.0			±5.0		μA
$I_{S(off)}$ with Overvoltage	S	16	$V_{IN} = \pm 25V$, $V_0 = \pm 10V$		±1.0		±2.0			±5.0		
INPUT												
$I_{EN(on)}$ $I_{A(on)}$ or $I_{EN(off)}$ $I_{A(off)}$	A_0, A_1, A_2, A_3 or EN	4	$V_A = 0V$		0.01		−10	−30		−10	−30	μA
		4	$V_A = 15V$		0.01		10	30		10	30	

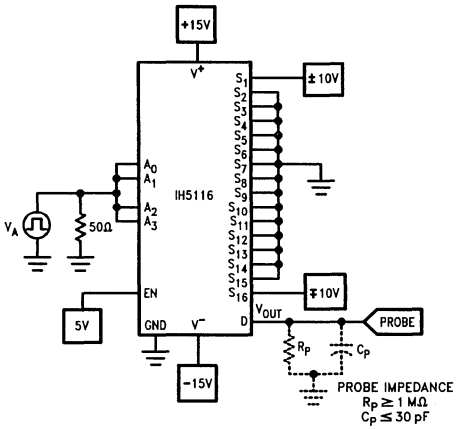
NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

($V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.) (Continued)

Characteristic		Measured Terminal	No Tests Per Temp	Test Conditions		Typ 25°C	Max Limits						Units
							M Suffix			C Suffix			
							−55°C	25°C	125°C	0°C	25°C	70°C	
DYNAMIC													
$t_{transition}$		D		See Figure 3		0.3		1					µs
t_{open}		D		See Figure 4		0.2							
$t_{on(EN)}$		D		See Figure 5		0.6		1.5					
$t_{off(EN)}$		D				0.4		1					
t_{on}-t_{off} Break-Before-Make Delay Settling Time		D		$V_{EN} = +5V$, A_0, A_1, A_2 Strobed $V_{IN} = \pm 10V$, See Figure 6		25							ns
"OFF" Isolation		D		$V_{EN} = 0V$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3VRMS$, $f = 500kHz$		60							dB
$C_{s(off)}$		S		$V_S = 0V$	$V_{EN} = 0V$, $f = 140kHz$ to 1 MHz	5							pF
$C_{D(off)}$		D		$V_D = 0V$		25							
$C_{DS(off)}$		D to S		$V_S = 0V$, $V_D = 0V$		1							
SUPPLY													
Supply Current	+	I^+	1	All $V_A = 0V/5V$ $V_{EN} = 5V$		0.5		0.6			1.0		mA
	−	I^-	1			0.02		0.6			1.0		

NOTE: All typical values have been characterized but are not tested.



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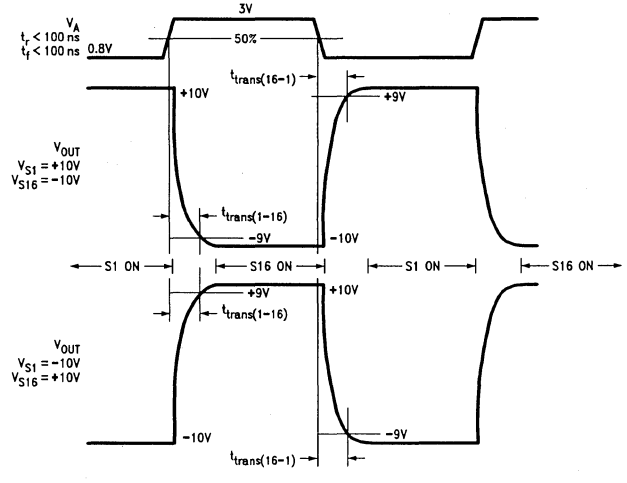

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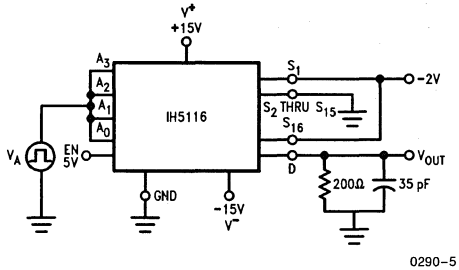
Figure 3: $t_{transition}$ Switching Test Circuit and Waveforms



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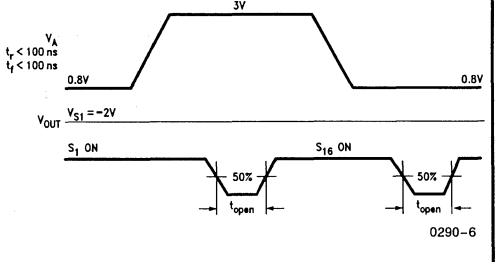

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Figure 4: t_{open} (Break-Before-Make) Switching Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

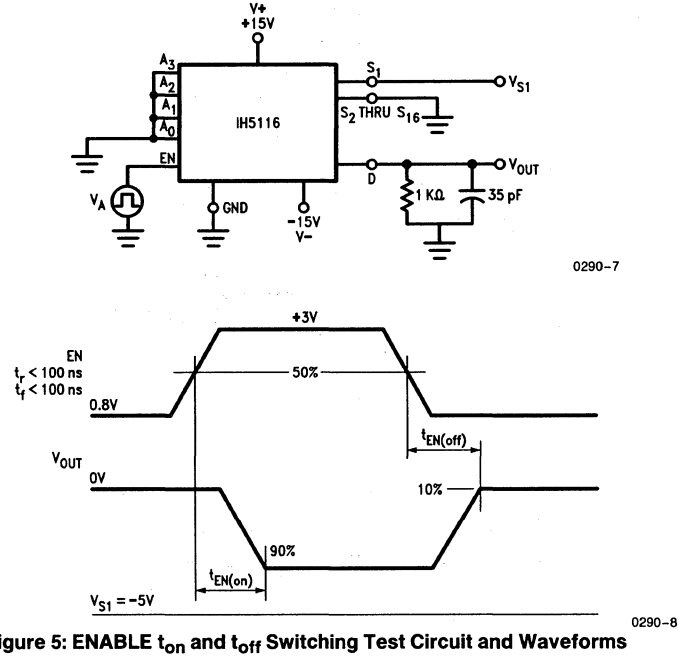


Figure 5: ENABLE t_{on} and t_{off} Switching Test Circuit and Waveforms

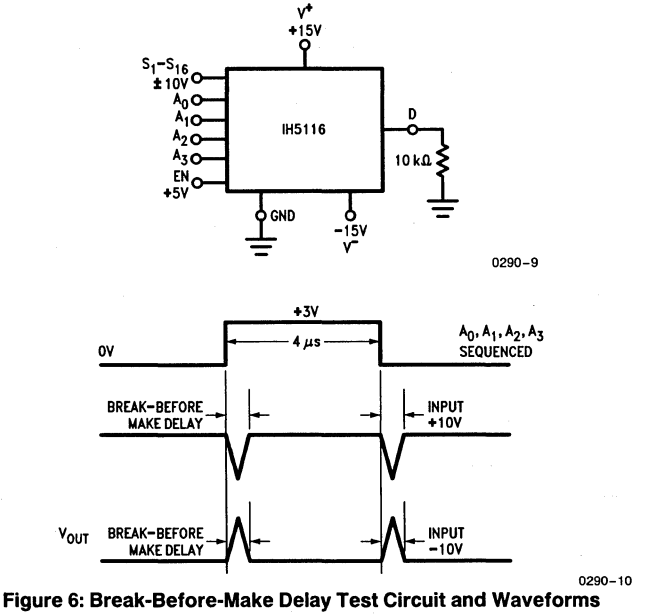


Figure 6: Break-Before-Make Delay Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

The IH5116, like all Harris multiplexers, contains a set of CMOS switches that form the channels, and driver and decoder circuitry to control which channel turns ON, if any. In addition, the IH5116 contains an internal regulator which provides a fully TTL compatible ENable input that is identical in operation to the Address inputs. This does away with the special conditions that many multiplexer enable inputs require for proper logic swings. The identical circuit conditions of the ENable and Address lines also helps ensure the extension of break-before-make switching to wider multiplexer systems (see applications section).

Another, and more important difference lies in the switching channel. Previous devices have used parallel n- and p-channel MOSFET switches. While this scheme yields reasonably good ON resistance characteristics and allows the switching of rail-to-rail input signals, it also has a number of drawbacks. The sources and drains of the switch transistors will conduct to the substrate if the input goes outside the supply rails, and even careful use of diodes cannot avoid channel-to-output and channel-to-channel coupling in cases of input overrange. The IH5116 uses a novel series arrangement of the p- and n-channel switches (Figure 7) combined with a dielectrically isolated process to eliminate these problems.

Within the normal analog signal range, the inherent variation of switch ON resistance will balance out almost as well as the customary parallel configuration, but as the analog signal approaches either supply rail, even for an ON channel, either the p- or the n-channel will become a source

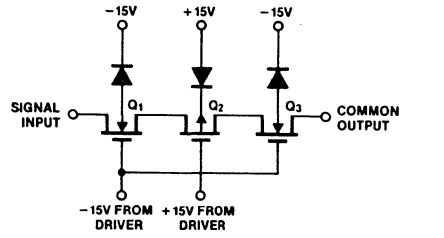
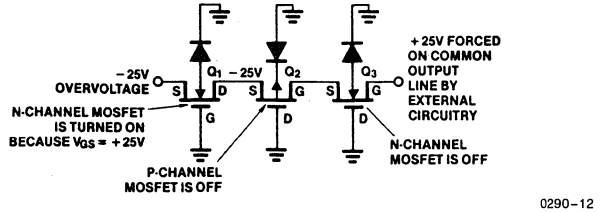


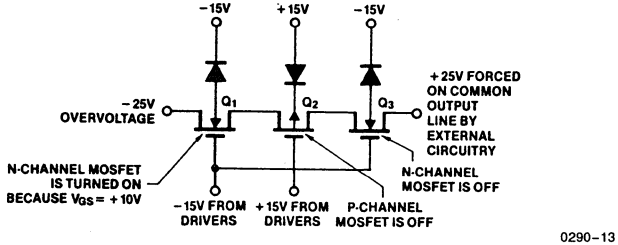
Figure 7: Series Connection of Channel Switches

follower, disconnecting the channel (Figure 8). Thus protection is provided for any input or output channel against overvoltage, even in the absence of multiplexer supply voltages. This applies up to the breakdown voltage of the respective switches. Figure 9 shows a more detailed schematic of the channel switches, including the back-gate driver devices which ensure optimum channel ON resistances and breakdown voltage under the various conditions.

Under some circumstances, if the logic inputs are present but the multiplexer supplies are not, the circuit will use the logic inputs as a sort of phantom supply; this could result in an output up to that logic level. To prevent this from occurring, simply ensure that the ENable pin is LOW any time the multiplexer supply voltages are missing (Figure 10).



(a) OVERVOLTAGE WITH MUX POWER OFF



(b) OVERVOLTAGE WITH MUX POWER ON

Figure 8: Overvoltage Protection

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION (Continued)

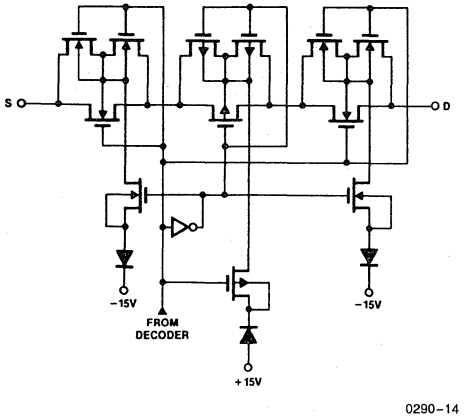


Figure 9: Detailed Channel Switch Schematic

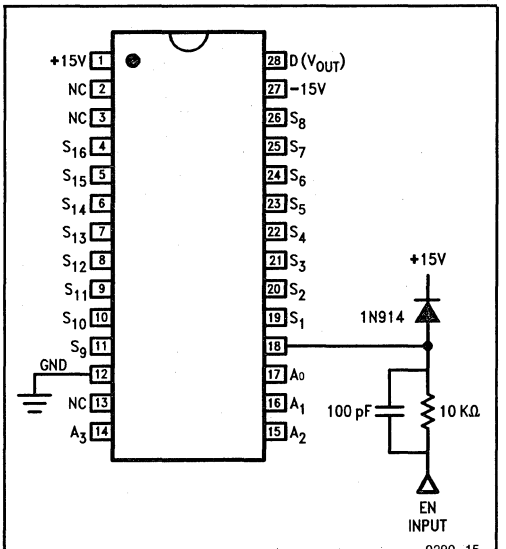


Figure 10: Protection Against Logic Input

MAXIMUM SIGNAL HANDLING CAPABILITY

The IH5116 is designed to handle signals in the ±10V range, with a typical $R_{DS(on)}$ of 900Ω; it can successfully handle signals up to ±12V, however, $R_{DS(on)}$ will increase to about 1.8kΩ. Beyond ±12V the device approaches an open circuit, and thus ±12V is about the practical limit, see Figure 11.

Figure 12 shows the input/output characteristics of an ON channel, illustrating the inherent limiting action of the series switch connection (see Detailed Description), while Figure 13 gives the ON resistance variation with temperature.

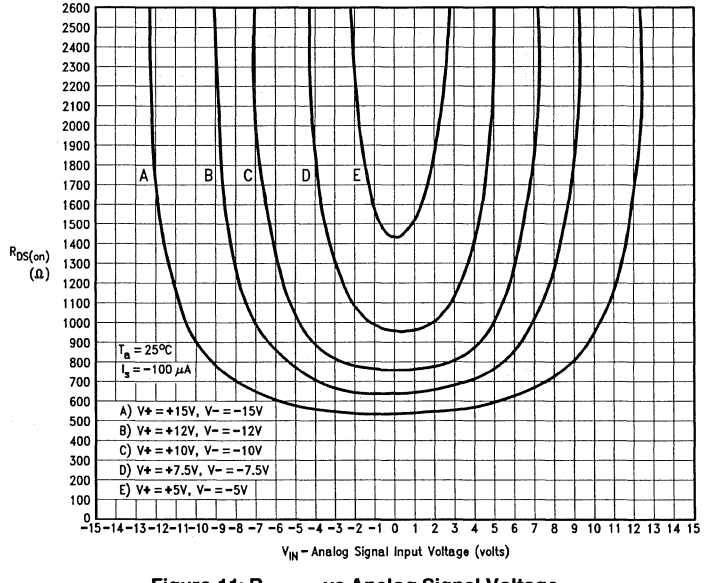
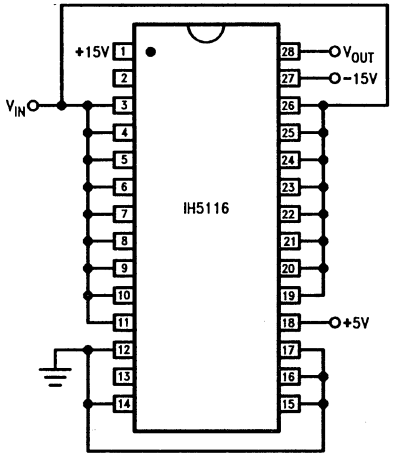


Figure 11: $R_{DS(on)}$ vs Analog Signal Voltage

NOTE: All typical values have been characterized but are not tested.



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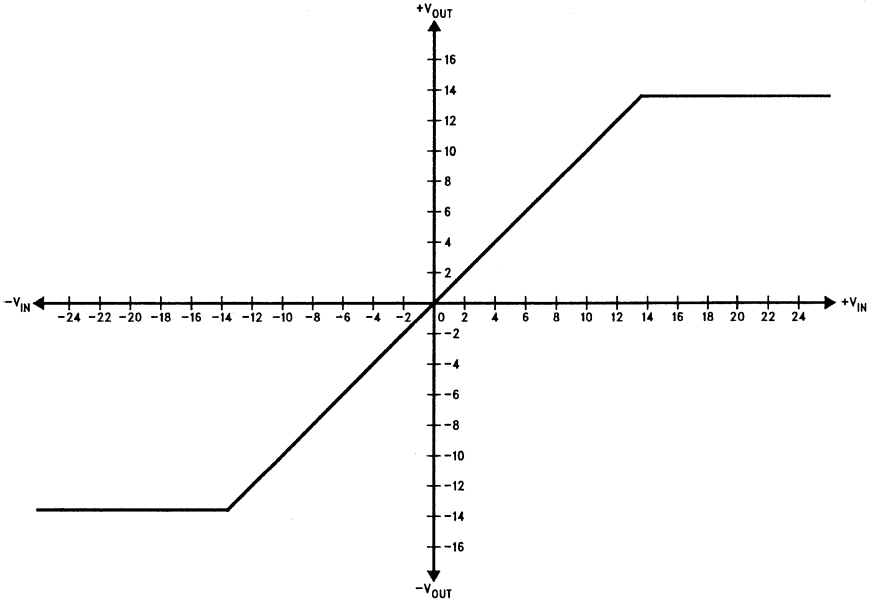

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Figure 12: MUX Output Voltage vs Input Voltage (Channel 1 Shown; All Channels Similar)

NOTE: All typical values have been characterized but are not tested.

IH5116 APPLICATIONS

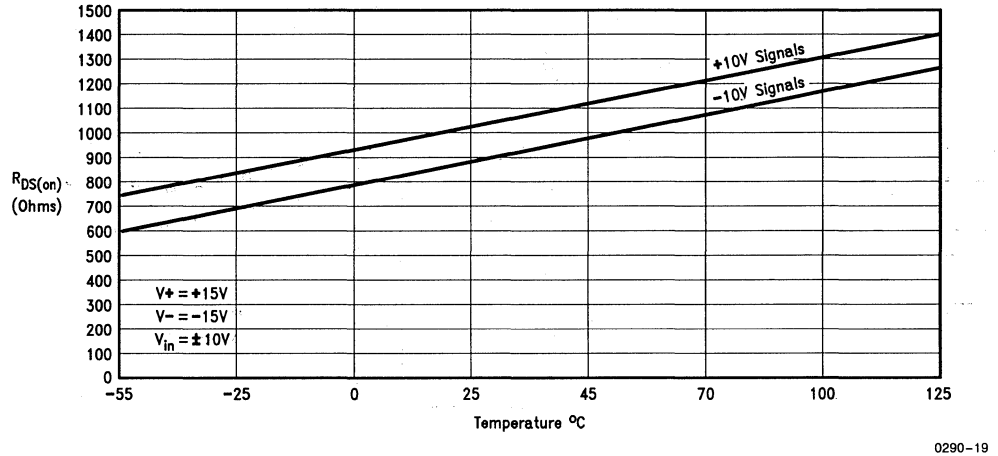
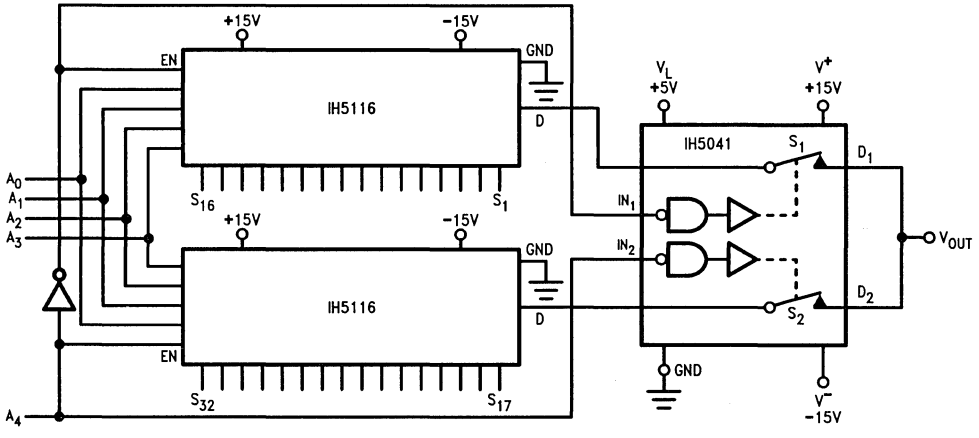


Figure 13: Typical $R_{DS(ON)}$ Variation with Temperature

NOTE: All typical values have been characterized but are not tested.

IH5116 APPLICATIONS (Continued)



TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

TRUTH TABLE

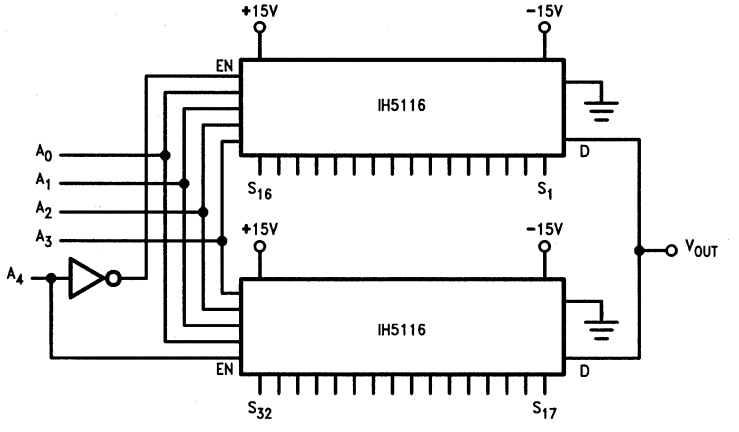
A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 15: 1 of 32 Channel Multiplexer Using 2 IH5116's and an IH5041 for Submultiplexing

8

NOTE: All typical values have been characterized but are not tested.

IH5116 APPLICATIONS (Continued)



TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 16: 1 of 32 Channel Multiplexer Using 2 IH5116's

NOTE: All typical values have been characterized but are not tested.

IH5116 APPLICATIONS (Continued)

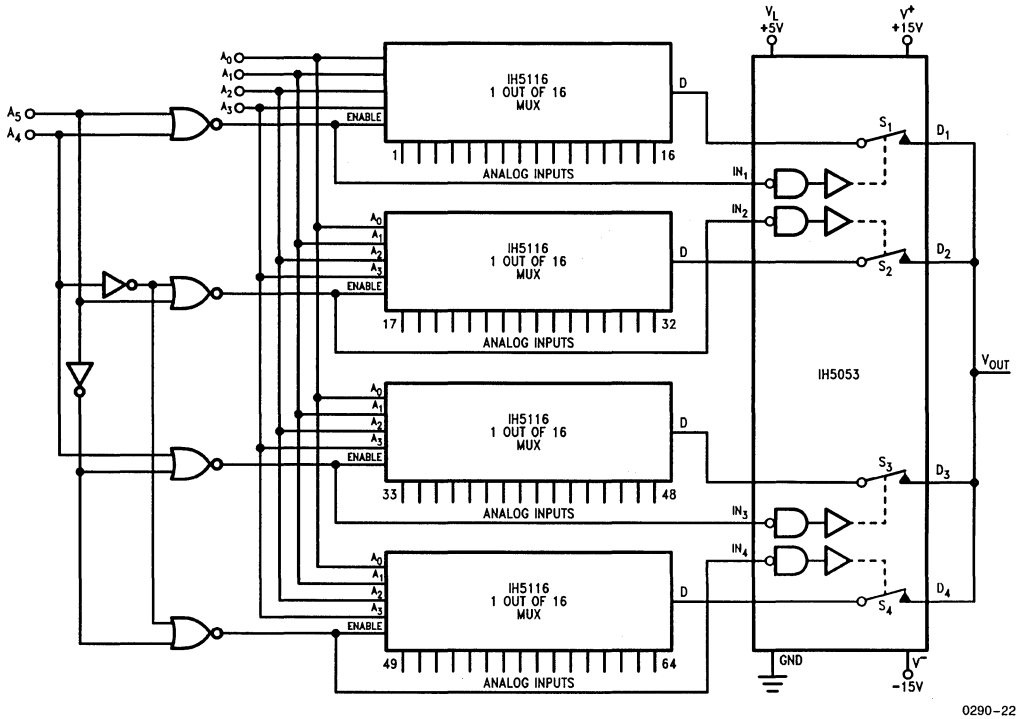


Figure 17: 1 of 64 Multiplexer Using 4 1/16s and IH5053 As Submultiplexer

General note on expandability of IH5116

Figures 15, 16, and 17 show how the IH5116 can be expanded.

Figure 15 shows a 1 of 32 multiplexer, using 2 IH5116s.

Figure 16 shows the 1 of 32 MUX of Figure 15, with a second tier of submultiplexing added to further reduce leakage and output capacitance. The IH5041 has typical ON resistances of 50Ω (max. is 75Ω) so it only increases thruput channel resistance from the 900Ω of Figure 15 to about 950Ω for Figure 16.

Figure 17 shows a 1 of 64 MUX using 2 tier MUXing (similar to Figure 16). The V_{OUT} point will see 15 OFF channels and 1 ON channel at any one time, so that the typical leakages will be about 0.05 nA. Throughput channel resistance will be in the 950Ω range.

USING THE IH5116 WITH SUPPLIES OTHER THAN ±15V

The IH5116 will operate successfully with supply voltages from ±5V to ±15V, however, $r_{DS(on)}$ increases as supply voltage decreases, as shown in Figure 11. Leakage currents, on the other hand, decrease with a lowering of supply voltage, and therefore the error term product of $r_{DS(on)}$ and leadkage current remains reasonably constant. $r_{DS(on)}$ also decreases as signal levels decrease. For high system accuracy [acceptable levels of $r_{DS(on)}$] the maximum input signal should be 3V less than the supply voltages. The logic levels remain TTL compatible.

APPLICATION NOTES

Further information may be found in:

A003 "Understanding and Applying the Analog Switch"

A006 "A New CMOS Analog Gate Technology"

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing"

R009 "Reduce CMOS Multiplexer Troubles Through Proper Device Selection"

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

IH5208
4-Channel Differential Fault Protected CMOS Analog Multiplexer

GENERAL DESCRIPTION

The IH5208 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the HI549 and similar devices, but adds fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ±25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc.

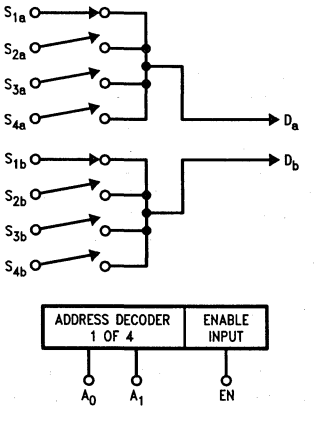
A binary 2-bit address code together with the ENable input allows selection of any channel pair or none at all. These 3 inputs are all TTL compatible for easy logic interface; the ENable input also facilitates MUX expansion and cascading.

FEATURES

- **All Channels OFF When Power OFF, for Analog Signals Up to ±25V**
- **Power Supply Quiescent Current Less Than 1μA**
- **±13V Analog Signal Range**
- **No SCR Latchup**
- **Break-Before-Make Switching**
- **TTL and CMOS Compatible Strobe Control**
- **Pin Compatible With HI549**
- **Any Channel Turns OFF If Input Exceeds Supply Rails by Up to ±25V**
- **TTL and CMOS Compatible Binary Address and ENable Inputs**

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH5208MJE	−55°C to +125°C	16 pin CERDIP
IH5208IJE	−25°C to +85°C	16 pin CERDIP
IH5208CPE	0°C to 70°C	16 pin plastic DIP



0293-1

2 LINE BINARY ADDRESS INPUTS

(0 0) AND EN = 1

ABOVE EXAMPLE SHOWS CHANNELS 1a AND 1b ON

Figure 1. Functional Diagram

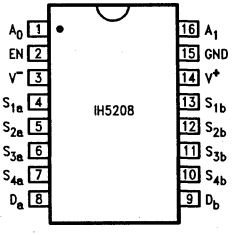
TRUTH TABLE

A_1	A_0	EN	On Switch Pair
X	X	0	NONE
0	0	1	1a, 1b
0	1	1	2a, 2b
1	0	1	3a, 3b
1	1	1	4a, 4b

A_0, A_1, EN

Logic "1" = $V_{AH} \geq 2.4V$

Logic "0" = $V_{AL} \leq 0.8V$



0293-2

V+ Common to Substrate

TOP VIEW

Figure 2: Pin Configuration (Outline dwg JE, PE)

304250-004

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V, +15V
V_S or V_D to V^+ ..... +25V, −40V
V_S or V_D to V^- ..... −25V, +40V
V^+ to Ground 20V
V^- to Ground ..... −20V
Current (Any Terminal) 20mA
Operating Temperature
C Suffix .....0°C to +70°C
I Suffix .....−25°C to +85°C
M Suffix .....−55°C to +125°C

Storage Temperature
C Suffix .....−65°C to +125°C
I & M Suffix .....−65°C to +150°C
Lead Temperature (Soldering, 10 sec).....300°C
Power Dissipation*
CERDIP Package**.....900 mW
Plastic Package***.....470 mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 12 mW/°C above 75°C

***Derate 6.3 mW/°C above 75°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

$V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions		Typ 25°C	Max Limits M Suffix −55°C	M Suffix 25°C	M Suffix 125°C	C Suffix −25°C/0°C	C Suffix 25°C	C Suffix 85°C/70°C	Units
SWITCH												
$R_{DS(on)}$	S to D	8	$V_D = 10V$, $I_S = -100\mu A$	Sequence each switch on	900	1200	1200	1800	1500	1500	2000	Ω
		8	$V_D = -10V$ $I_S = -100\mu A$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$	900	1200	1200	1800	1500	1500	2000	
$\Delta R_{DS(on)}$			$\Delta R_{DS(on)} = \frac{R_{DS(on)max} - R_{DS(on)min}}{R_{DS(on)avg.}}$ $V_S = \pm 10V$		5							%
$I_{S(off)}$	S	8	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0.8V$	±0.02		±0.5	±50		±1.0	±50	nA
		8	$V_S = -10V$, $V_D = 10V$		±0.02		±0.5	±50		±1.0	±50	
$I_{D(off)}$	D	1	$V_D = 10V$, $V_S = -10V$		±0.02		±1.0	±100		±2.0	±100	
		1	$V_D = -10V$, $V_S = 10V$		±0.05		±1.0	±100		±2.0	±100	
$I_{D(on)}$	D	8	$V_{S(All)} = V_D = 10V$	Sequence each switch on	±0.1		±2.0	±100		±5.0	±100	
		8	$V_{S(All)} = V_D = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$	±0.1		±2.0	±100		±5.0	±100	
FAULT												
I_S with Power OFF	S	8	$V_{SUPP} = 0V$, $V_{IN} = \pm 25V$, $V_{EN} = V_O = 0V$, $A_0, A_1, A_2 = 0V$		±1.0		±2			±5		μA
$I_{S(off)}$ with Overvoltage	S	8	$V_{IN} = \pm 25V$, $V_0 = \pm 10V$		±1.0		±5			±10		
INPUT												
$I_{EN(on)}$ $I_{A(on)}$ or $I_{EN(off)}$ $I_{A(off)}$	A_0, A_1, A_{A2} or EN	4	$V_A = 0V$		0.01		−10	−30		−10	−30	μA
		4	$V_A = 15V$		0.01		10	30		10	30	

NOTE: All typical values have been characterized but are not tested.

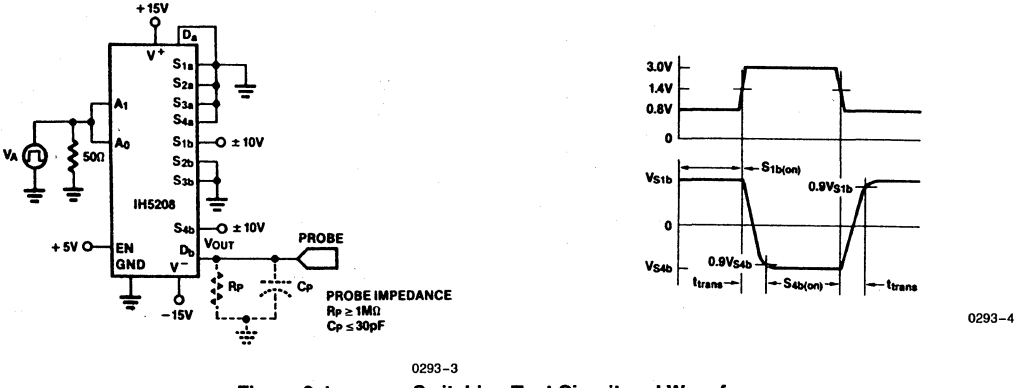
ELECTRICAL CHARACTERISTICS

$V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified. (Continued)

Characteristic		Measured Terminal	No Tests Per Temp	Test Conditions		Typ 25°C	Max Limits M Suffix −55°C	M Suffix 25°C	M Suffix 125°C	C Suffix −20°C/0°C	C Suffix 25°C	C Suffix 85°C/70°C	Units
DYNAMIC													
$t_{transition}$		D		See Figure 3		0.3							µs
t_{open}		D		See Figure 4		0.2							
$t_{on(EN)}$		D		See Figure 5		0.6		1.5					
$t_{off(EN)}$		D				0.4		1					
t_{on}-t_{off} Break-Before-Make Delay Settling Time		D		$V_{EN} = +5V$, A_0, A_1, A_2 Strobed $V_{IN} = \pm 10V$, See Figure 6		10							ns
"OFF" Isolation		D		$V_{EN} = 0V$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3VRMS$, $f = 500kHz$		60							dB
$C_{s(off)}$		S		$V_S = 0V$	$V_{EN} = 0V$, $f = 140kHz$ to 1 MHz	5							pF
$C_{D(off)}$		D		$V_D = 0V$		25							
$C_{DS(off)}$		D to S		$V_S = 0V$, $V_D = 0V$		1							
SUPPLY													
Supply Current	+	I^+	1	$V_{EN} = 5V$ All $V_A = 0V/5V$		0.5	0.7	0.6	0.5		1.0		mA
	−	I^-	1			0.02	0.7	0.6	0.5		1.0		

Note 1. Readings taken 400ms after the overvoltage occurs.

SWITCHING INFORMATION



0293-3

Figure 3: $t_{transition}$ Switching Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

SWITCHING INFORMATION (Continued)

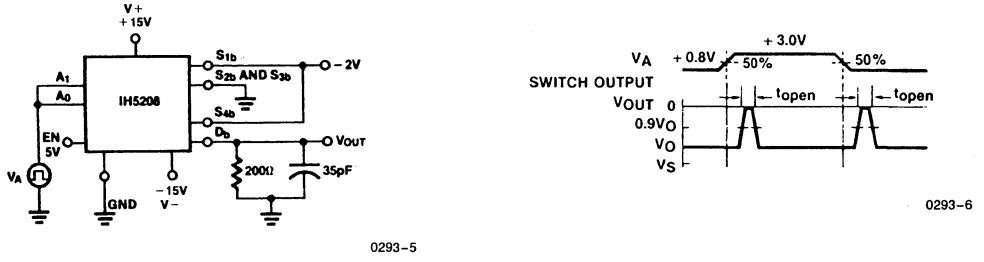


Figure 4: t_{open} (Break-Before-Make) Switching Test Circuit and Waveforms

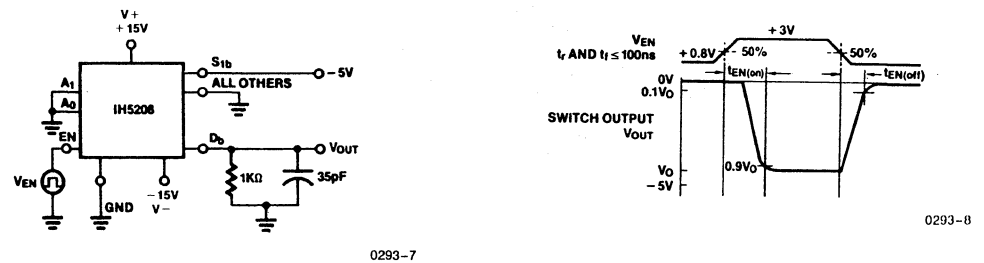


Figure 5: Enable t_{on} and t_{off} Switching Test Circuit and Waveforms

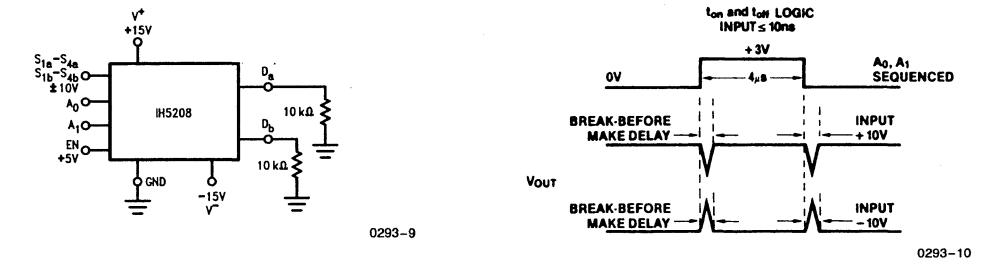


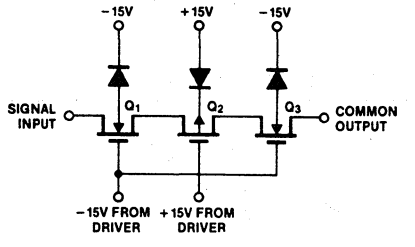
Figure 6: Break-Before-Make Delay Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

The IH5208, like all Harris' multiplexers, contains a set of CMOS switches that form the channels, and driver and decoder circuitry to control which channel turns ON, if any. In addition, the IH5208 contains an internal regulator which provides a fully TTL compatible ENable input that is identical in operation to the Address inputs. This does away with the special conditions that many multiplexer enable inputs require for proper logic swings. The identical circuit conditions of the ENable and Address lines also helps ensure the extension of break-before-make switching to wider multiplexer systems (see applications section).

Another, and more important difference lies in the switching channel. Previous devices have used parallel n- and p-channel MOSFET switches. While this scheme yields reasonably good ON resistance characteristics and allows the switching of rail-to-rail input signals, it also has a number of drawbacks. The sources and drains of the switch transistors will conduct to the substrate if the input goes outside the supply rails, and even careful use of diodes cannot avoid channel-to-output and channel-to-channel coupling in cases of input overrange. The IH5208 uses a novel series arrangement of the p- and n-channel switches (Figure 7) combined with the dielectrically isolated process to eliminate these problems.



0293-11

Figure 7: Series Connection of Channel Switches

Within the normal analog signal range, the inherent variation of switch ON resistance will balance out almost as well as the customary parallel configuration, but as the analog signal approaches either supply rail, even for an ON channel, either the p- or the n-channel will become a source follower, disconnecting the channel (Figure 8). Thus protection is provided for any input or output channel against overvoltage, even in the absence of multiplexer supply voltages. This applies up to the breakdown voltage of the respective switches. Figure 9 shows a more detailed schematic of the channel switches, including the back-gate driver devices which ensure optimum channel ON resistances and breakdown voltage under the various conditions.

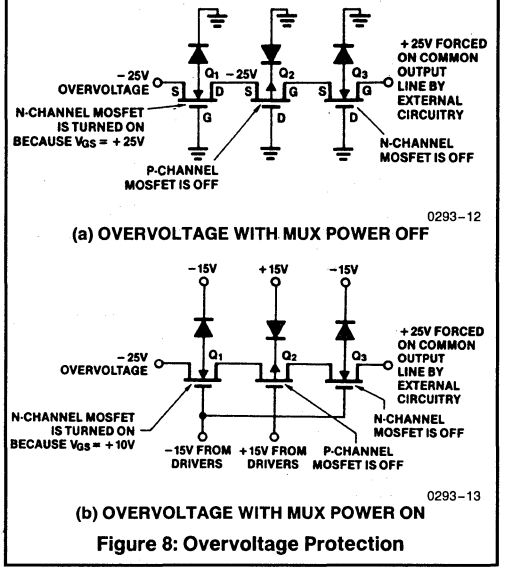
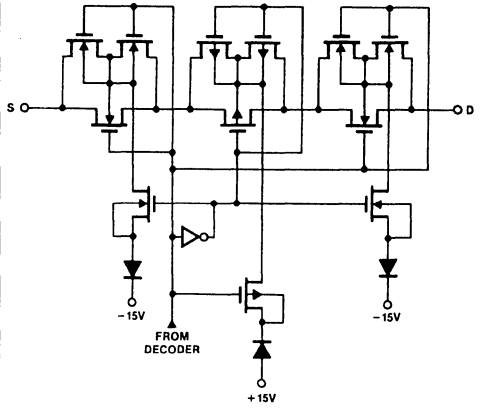


Figure 8: Overvoltage Protection

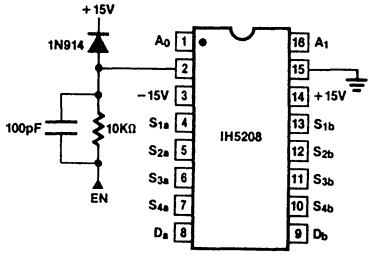
Under some circumstances, if the logic inputs are present but the multiplexer supplies are not, the circuit will use the logic inputs as a sort of phantom supply; this could result in an output up to that logic level. To prevent this from occurring, simply ensure that the ENable pin is LOW any time the multiplexer supply voltages are missing (Figure 10).

NOTE: All typical values have been characterized but are not tested.



0293-14

Figure 9: Detailed Channel Switch Schematic



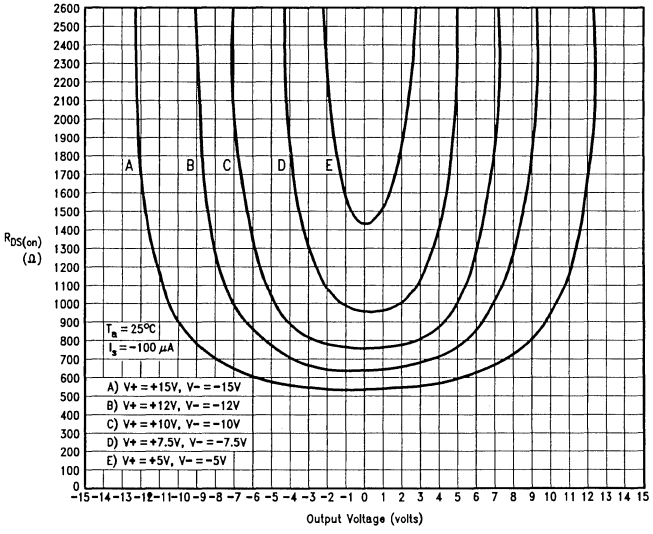
0293-15

Figure 10: Protection Against Logic Input

MAXIMUM SIGNAL HANDLING CAPABILITY

The IH5208 is designed to handle signals in the ±10V range, with a typical $r_{DS(on)}$ of 900Ω; it can successfully handle signals up to ±12V, however, $r_{DS(on)}$ will increase to about 1.8kΩ. Beyond ±12V the device approaches an open circuit, and thus ±12V is about the practical limit, see Figure 11.

Figure 12 shows the input/output characteristics of an ON channel, illustrating the inherent limiting action of the series switch connection (see Detailed Description), while Figure 13 gives the ON resistance variation with temperature.

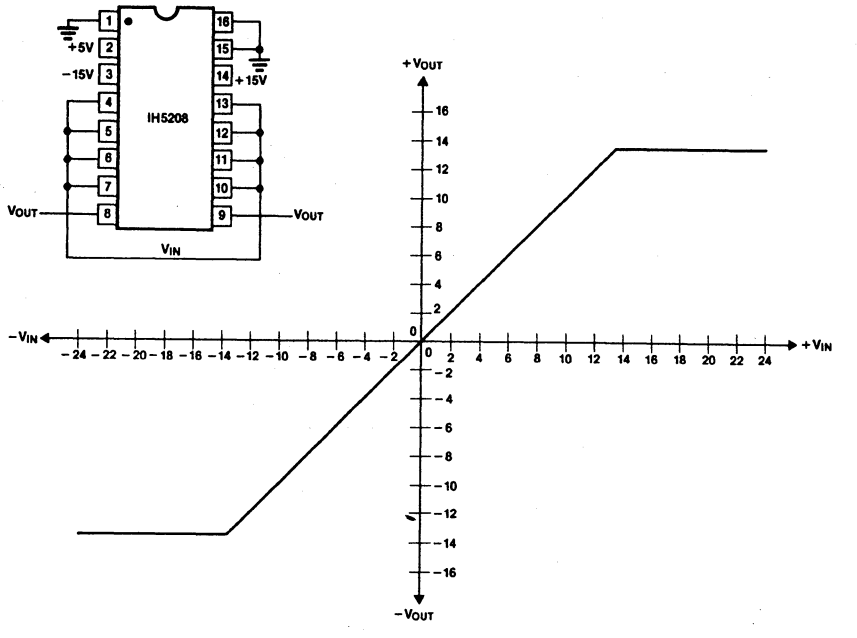


0293-16

Figure 11: $R_{DS(on)}$ vs Analog Signal Voltage

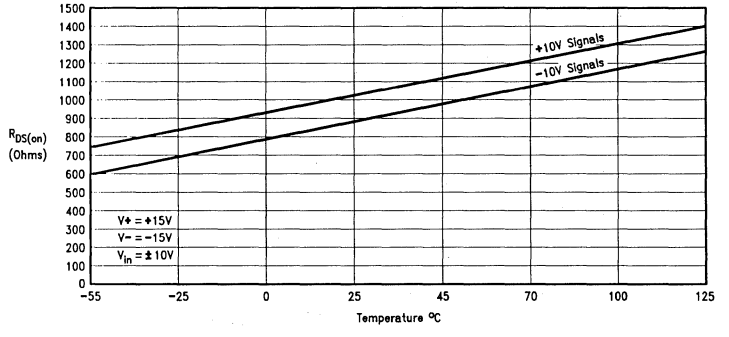
NOTE: All typical values have been characterized but are not tested.

IH5208



0293-17

Figure 12: MUX Output Voltage vs Input Voltage Channel 1 Shown; All Channels Similar



0293-18

Figure 13: Typical $R_{DS(on)}$ Variation with Temperature

NOTE: All typical values have been characterized but are not tested.

USING THE IH5208 WITH SUPPLIES OTHER THAN ±15V

The IH5208 will operate successfully with supply voltages from ±5V to ±15V, however $r_{DS(on)}$ increases as supply voltage decreases, as shown in Figure 11. Leakage currents, on the other hand, decrease with a lowering of supply voltage, and therefore the error term product of $r_{DS(on)}$ and leakage current remains reasonably constant. $r_{DS(on)}$ also decreases as signal levels decrease. For high system accuracy [acceptable levels of $r_{DS(on)}$] the maximum input signal should be 3V less than the supply voltages. The logic thresholds remain TTL compatible.

APPLICATION NOTES

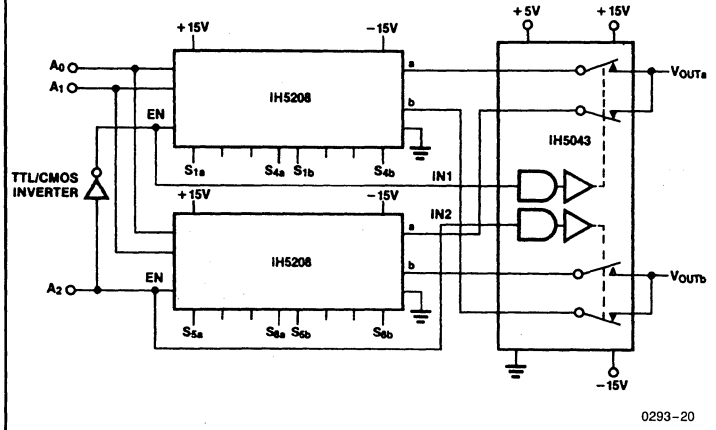
Further information may be found in:

A003 "Understanding and Applying the Analog Switch"

A006 "A New CMOS Analog Gate Technology"

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing"

IH5208 APPLICATIONS INFORMATION



TRUTH TABLE

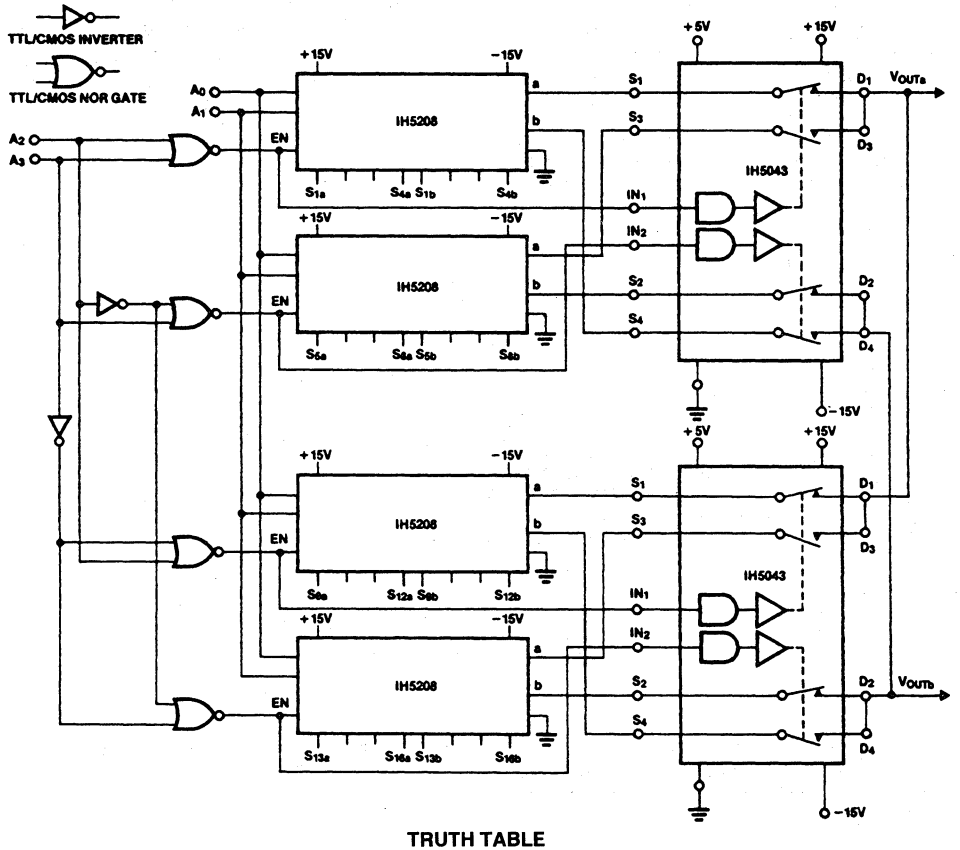
A_2	A_1	A_0	On Switch Pair
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

Figure 14: 2 of 16 Channel Multiplexer Using Two IH5208s. Overvoltage Protection and Break-Before-Make Switching Are Extended to All Channels.

8

NOTE: All typical values have been characterized but are not tested.

IH5208 APPLICATIONS INFORMATION (Continued)



TRUTH TABLE

A_3	A_2	A_1	A_0	On Switch		On Switch	
0	0	0	0	S1a		S1b	
0	0	0	1	S2a		S2b	
0	0	1	0	S3a		S3b	
0	0	1	1	S4a		S4b	
0	1	0	0	S5a		S5b	
0	1	0	1	S6a		S6b	
0	1	1	0	S7a		S7b	
0	1	1	1	S8a	V_{OUTa}	S8b	V_{OUTb}
1	0	0	0	S9a		S9b	
1	0	0	1	S10a		S10b	
1	0	1	0	S11a		S11b	
1	0	1	1	S12a		S12b	
1	1	0	0	S13a		S13b	
1	1	0	1	S14a		S14b	
1	1	1	0	S15a		S15b	
1	1	1	1	S16a		S16b	

Figure 15: Submultiplexed 2 of 32 System. The Two IH5043s Are Overvoltage Protected By The IH5208s. Submultiplexing Reduces Output Capacitance and Leakage Currents.

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

IH5216
8-Channel Differential Fault Protected CMOS Analog Multiplexer

GENERAL DESCRIPTION

The IH5216 is a dielectrically isolated CMOS monolithic analog multiplexer, designed as a plug-in replacement for the HI547 and similar devices, but adding fault protection to the standard performance. A unique serial MOSFET switch ensures that an OFF channel will remain OFF when the input exceeds the supply rails by up to ±25V, even with the supply voltage at zero. Further, an ON channel will be limited to a throughput of about 1.5V less than the supply rails, thus affording protection to any following circuitry such as op amps, D/A converters, etc. Cross talk onto "good" channels is also prevented.

A binary 3-bit address code together with the ENable input allows selection of any channel pair or none at all. These 4 inputs are all TTL compatible for easy logic interface. The ENable input also facilitates MUX expansion and cascading.

FEATURES

- **All Channels OFF When Power OFF, for Analog Signals Up to ±25V**
- **Power Supply Quiescent Current Less Than 1mA**
- **±13V Analog Signal Range**
- **No SCR Latchup**
- **Break-Before-Make Switching**
- **TTL and CMOS Compatible Strobe Control**
- **Pin Compatible With HI547**
- **Any Channel Turns OFF If Input Exceeds Supply Rails By Up to ±25V**
- **TTL and CMOS Compatible Binary Address and ENable Inputs**

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH5216MJI	−55°C to +125°C	28 pin CERDIP
IH5216CJI	0°C to +70°C	28 pin CERDIP
IH5216CPI	0°C to +70°C	28 pin Plastic DIP

TRUTH TABLE

A_2	A_1	A_0	EN	On Switch Pair
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 2.4V$
Logic "0" = $V_{AL} \leq 0.8V$

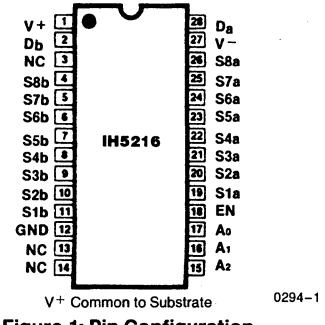
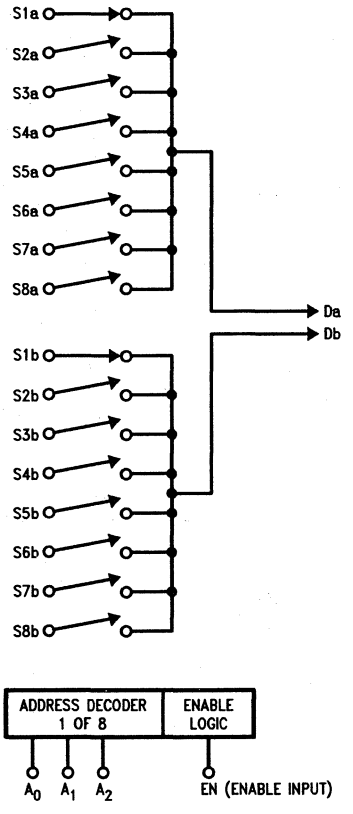


Figure 1: Pin Configuration (Outline dwgs JI, PI)

8

NOTE: All typical values have been characterized but are not tested.



3 LINE BINARY ADDRESS INPUTS
(0 0 0) AND EN = 5V
ABOVE EXAMPLE SHOWS CHANNELS 1a AND 1b ON.

0294-2

Figure 2: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

IH5216

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V to +15V
V_S or V_D to V^+ ..... +25V to −40V
V_S or V_D to V^- ..... −25V to +40V
V^+ to Ground 20V
V^- to Ground ..... −20V
Current (Any Terminal) 20mA
Operating Temperature
C Suffix ..... 0°C to +70°C
M Suffix ..... −55°C to +125°C
Storage Temperature
C Suffix ..... −65°C to +125°C
M Suffix ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C
Power Dissipation*
28-Pin CERDIP Package** 1200mW
28-Pin Plastic Package*** 625mW

*Device mounted with all leads soldered or welded to PC board.

**Derate 16mW/°C above 75°C

***Derate 8.3mV/°C above 75°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS ($V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.)

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions		Typ 25°C	Max Limits M Suffix −55°C	M Suffix 25°C	M Suffix 125°C	C Suffix 0°C	C Suffix 25°C	C Suffix 70°C	Units
SWITCH												
$R_{DS(on)}$	S to D	16	$V_D = 10V$, $I_S = -100\mu A$	Sequence each switch on $V_{AL} = 0.8V$, $V_{AH} = 2.4V$	900	1200	1200	1800	1500	1500	2000	Ω
		16	$V_D = -10V$ $I_S = -100\mu A$		900	1200	1200	1800	1500	1500	2000	
$\Delta R_{DS(on)}$			$\Delta R_{DS(on)} = \frac{R_{DS(on)max} - R_{DS(on)min}}{R_{DS(on)avg.}}$ $V_S = \pm 10V$		5							%
$I_{S(off)}$	S	16	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0.8V$	±0.02		±0.5	±50		±1.0	±50	nA
		16	$V_S = -10V$, $V_D = 10V$		±0.02		±0.5	±50		±1.0	±50	
$I_{D(off)}$	D	1	$V_D = 10V$, $V_S = -10V$		±0.05		±1.0	±100		±2.0	±100	
		1	$V_D = -10V$, $V_S = 10V$		±0.05		±1.0	±100		±2.0	±100	
$I_{D(on)}$	D	16	$V_{S(All)} = V_D = 10V$	Sequence each switch on $V_{AL} = 0.8V$, $V_{AH} = 2.4V$	±0.1		±2.0	±100		±4.0	±100	
		16	$V_{S(All)} = V_D = -10V$		±0.1		±2.0	±100		±4.0	±100	
FAULT												
I_S with Power OFF	S	16	$V_{SUPP} = 0V$, $V_{IN} = \pm 25V$, $V_{EN} = V_O = 0V$, A_0, A_1, $A_2 = 0V$ or $5V$		±1.0		±2.0			±5.0		μA
$I_{S(off)}$ with Overvoltage	S	16	$V_{IN} = \pm 25V$, $V_O = \pm 10V$		±1.0		±2.0			±5.0		

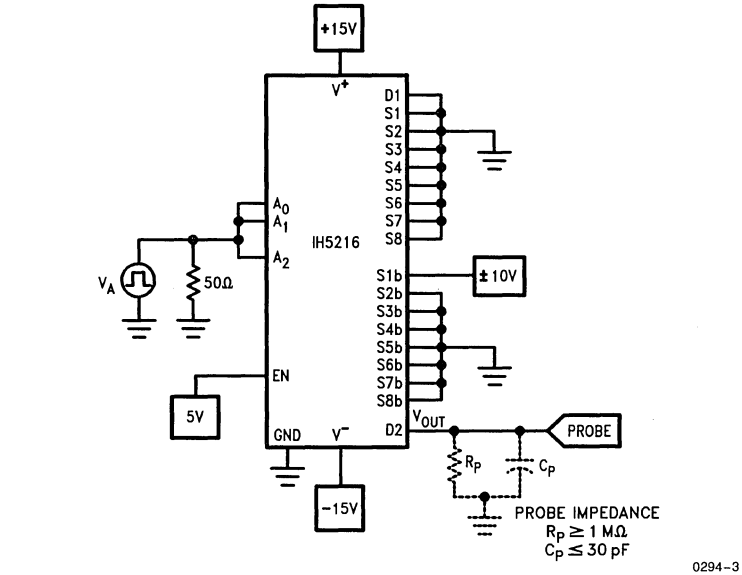
NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

($V^+ = 15V$, $V^- = -15V$, $V_{EN} = 2.4V$, unless otherwise specified.) (Continued)

Characteristic	Measured Terminal	No Tests Per Temp	Test Conditions		Typ 25°C	Max Limits M Suffix −55°C	M Suffix 25°C	M Suffix 125°C	C Suffix 0°C	C Suffix 25°C	C Suffix 70°C	Units
INPUT												
$I_{EN(on)}$ $I_{A(on)}$ or $I_{EN(off)}$ $I_{A(off)}$	A_0, A_1 A_2, A_3 or EN	4	$V_A = 0V$		0.01		−10	−30		−10	−30	µA
		4	$V_A = 15V$		0.01		10	30		10	30	
DYNAMIC												
$t_{transition}$	D		See Figure 3		0.3		1					µs
t_{open}	D		See Figure 4		0.2							
$t_{on(EN)}$	D		See Figure 5		0.6		1.5					
$t_{off(EN)}$	D				0.4		1					
t_{on}-t_{off} Break-Before-Make Delay Settling Time	D		$V_{EN} = +5V$, A_0, A_1, A_2 Strobed $V_{IN} = \pm 10V$. See Figure 6		25							ns
"OFF" Isolation	D		$V_{EN} = 0V$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3VRMS$, $f = 500kHz$		60							dB
$C_{s(off)}$	S		$V_S = 0V$	$V_{EN} = 0V$, $f = 140kHz$ to 1 MHz	5							pF
$C_{D(off)}$	D		$V_D = 0V$		25							
$C_{DS(off)}$	D to S		$V_S = 0V$, $V_D = 0V$		1							
SUPPLY												
Supply Current	+	I^+	1	All $V_A = 0V/5V$ $V_{EN} = 5V$	0.5		0.6			1.0		mA
	−	I^-	1		0.02		0.6			1.0		

NOTE: All typical values have been characterized but are not tested.



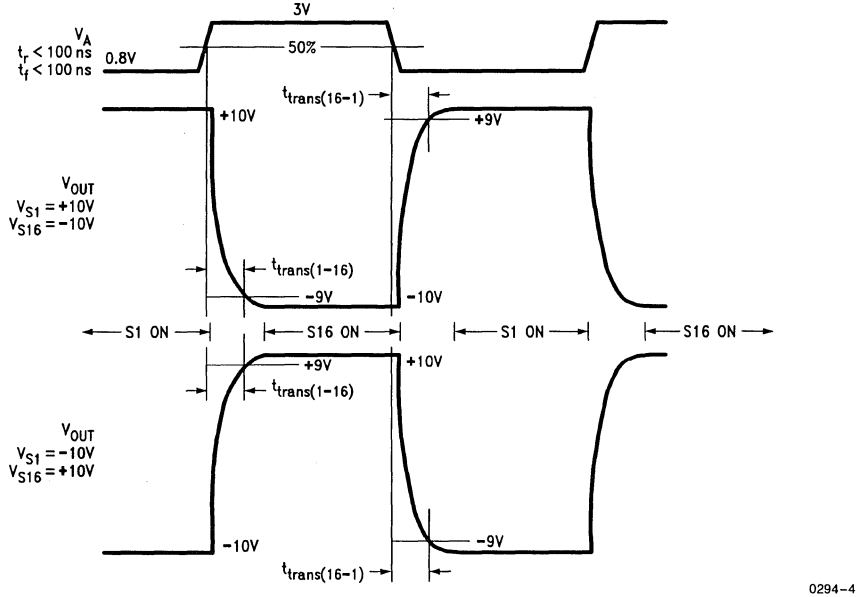


Figure 3: $t_{transition}$ Switching Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

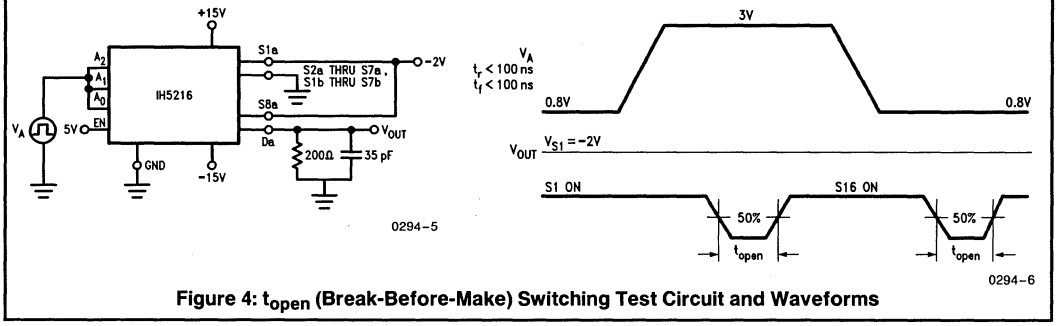


Figure 4: t_{open} (Break-Before-Make) Switching Test Circuit and Waveforms

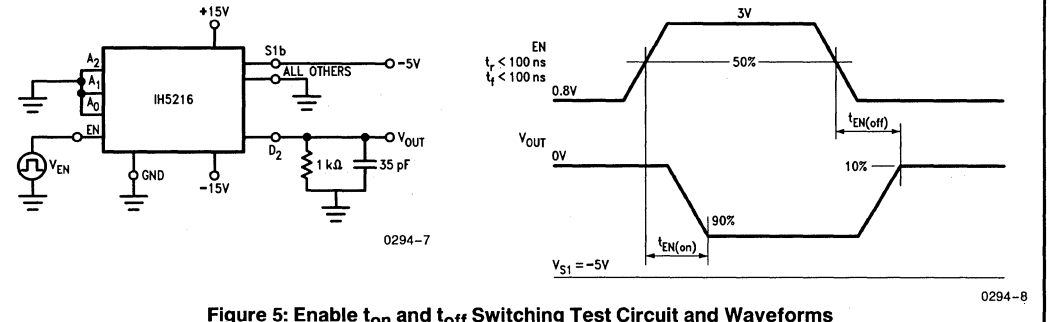


Figure 5: Enable t_{on} and t_{off} Switching Test Circuit and Waveforms

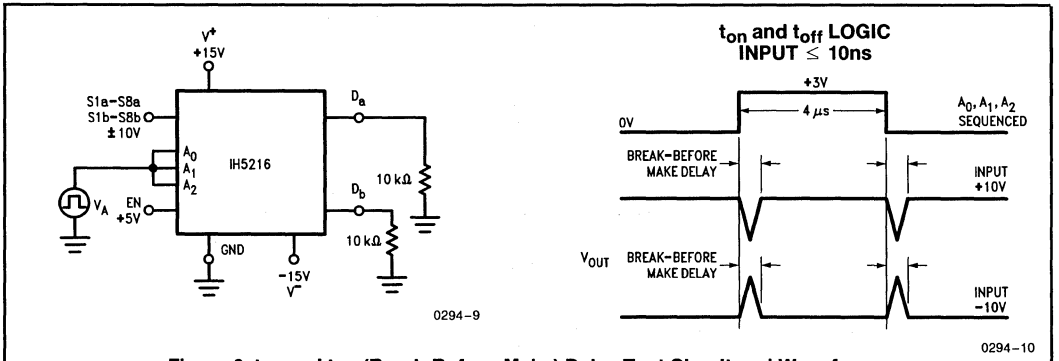


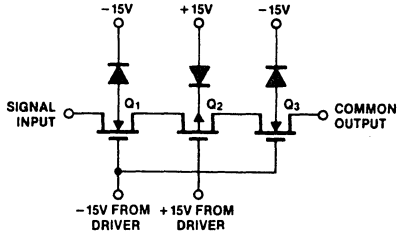
Figure 6: t_{on} and t_{off} (Break-Before-Make) Delay Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

The IH5216, like all Harris' multiplexers, contains a set of CMOS switches that form the channels, and driver and decoder circuitry to control which channel turns ON, if any. In addition, the IH5216 contains an internal regulator which provides a fully TTL compatible ENable input that is identical in operation to the Address inputs. This does away with the special conditions that many multiplexer enable inputs require for proper logic swings. The identical circuit conditions of the ENable and Address lines also helps ensure the extension of break-before-make switching to wider multiplexer systems (see applications section).

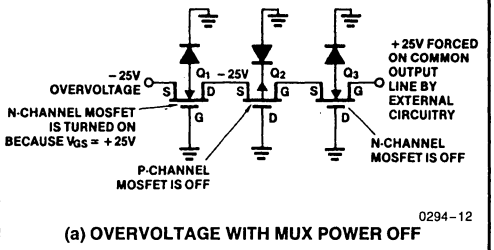
Another, and more important difference lies in the switching channel. Previous devices have used parallel n- and p-channel MOSFET switches. While this scheme yields reasonably good ON resistance characteristics and allows the switching of rail-to-rail input signals, it also has a number of drawbacks. The sources and drains of the switch transistors will conduct to the substrate if the input goes outside the supply rails, and even careful use of diodes cannot avoid channel-to-output and channel-to-channel coupling in cases of input overrange. The IH5216 uses a novel series arrangement of the p- and n-channel switches (Figure 7) combined with the dielectrically isolated process to eliminate these problems.



0294-11

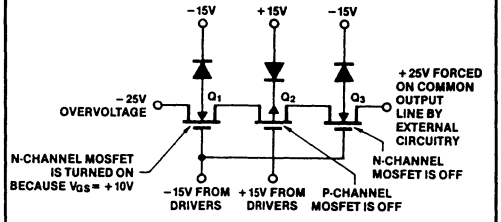
Figure 7: Series Connection of Channel Switches

Within the normal analog signal range, the inherent variation of switch ON resistance will balance out almost as well as the customary parallel configuration, but as the analog signal approaches either supply rail, even for an ON channel, either the p- or the n-channel will become a source follower, disconnecting the channel (Figure 8). Thus protection is provided for any input or output channel against overvoltage, even in the absence of multiplexer supply voltages. This applies up to the breakdown voltage of the respective switches. Figure 9 shows a more detailed schematic of the channel switches, including the back-gate driver devices which ensure optimum channel ON resistances and breakdown voltage under the various conditions.



0294-12

(a) OVERVOLTAGE WITH MUX POWER OFF



0294-13

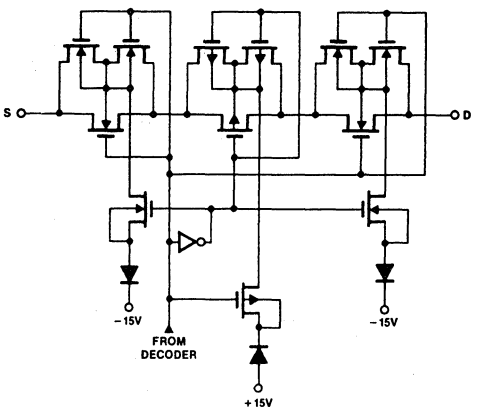
(b) OVERVOLTAGE WITH MUX POWER ON

Figure 8: Overvoltage Protection

Under some circumstances, if the logic inputs are present but the multiplexer supplies are not, the circuit will use the logic inputs as a sort of phantom supply; this could result in an output up to that logic level. To prevent this from occurring, simply ensure that the ENable pin is LOW any time the multiplexer supply voltages are missing (Figure 10).

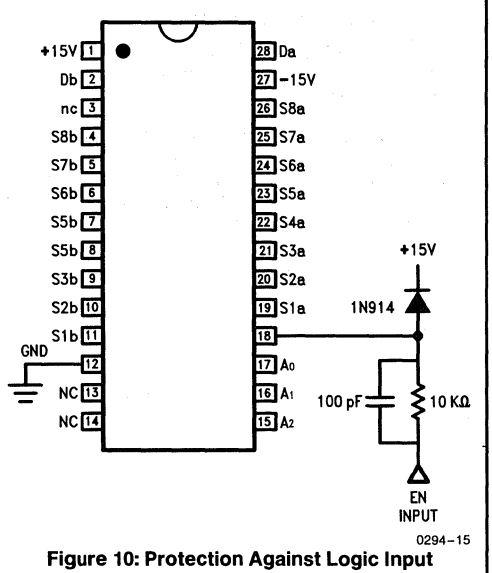
8

NOTE: All typical values have been characterized but are not tested.



0294-14

Figure 9: Detailed Channel Switch Schematic



0294-15

Figure 10: Protection Against Logic Input

MAXIMUM SIGNAL HANDLING CAPABILITY

The IH5216 is designed to handle signals in the ±10V range, with a typical $r_{DS(on)}$ of 900Ω; it can successfully handle signals up to ±12V, however, $r_{DS(on)}$ will increase to about 1.8kΩ. Beyond ±12V the device approaches an open circuit, and thus ±12V is about the practical limit, see Figure 11.

Figure 12 shows the input/output characteristics of an ON channel, illustrating the inherent limiting action of the series switch connection (see Detailed Description), while Figure 13 gives the ON resistance variation with temperature.

USING THE IH5216 WITH SUPPLIES OTHER THAN ±15V

The IH5216 will operate successfully with supply voltages from ±5V to ±15V, however $r_{DS(on)}$ increases as supply voltage decreases, as shown in Figure 11. Leakage currents, on the other hand, decrease with a lowering of supply voltage, and therefore the error term product of $r_{DS(on)}$ and leakage current remains reasonably constant. $r_{DS(on)}$ also decreases as signal levels decrease. For high system accuracy [acceptable levels of $r_{DS(on)}$] the maximum input signal should be 3V less than the supply voltages. The logic thresholds remain TTL compatible.

NOTE: All typical values have been characterized but are not tested.

IH5216

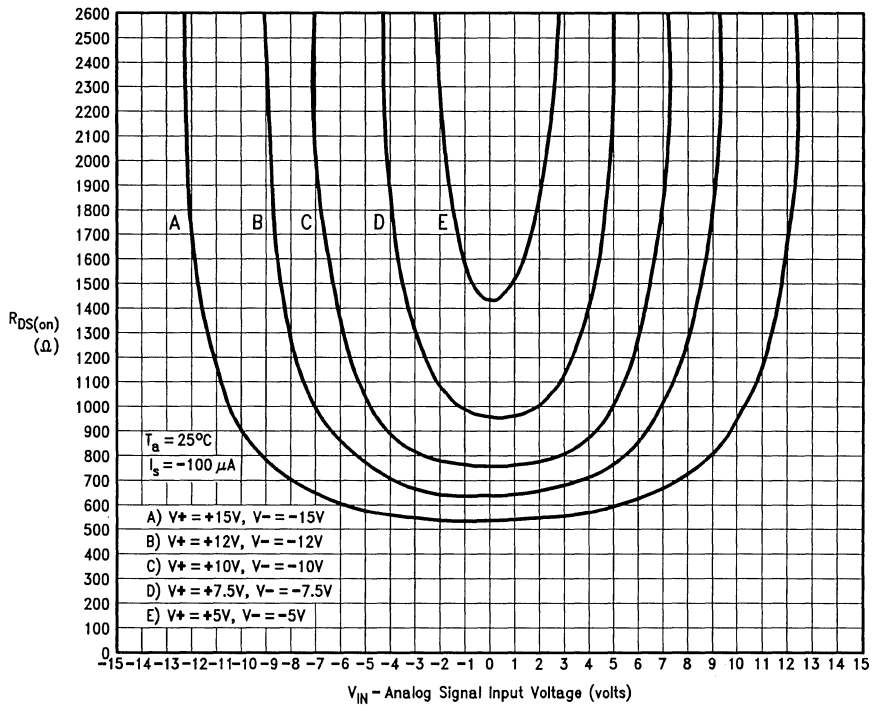


Figure 11: $r_{DS(on)}$ vs Signal Input Voltage @ $T_A = +25°C$

8

NOTE: All typical values have been characterized but are not tested.

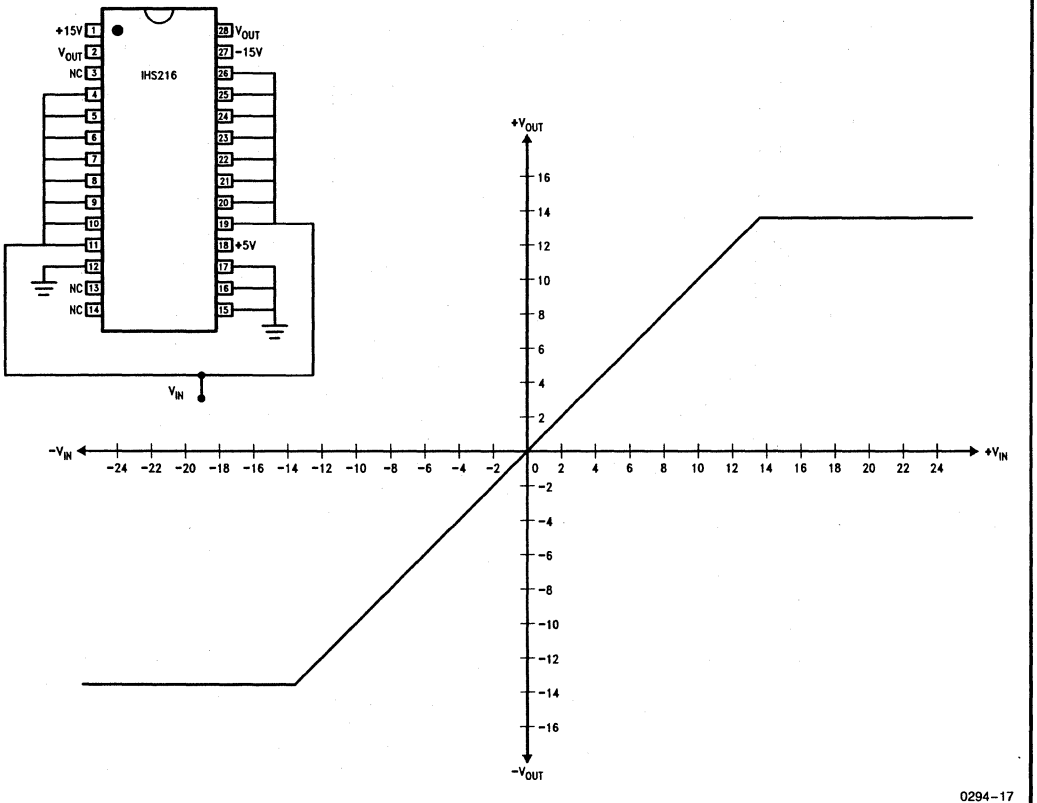


Figure 12: MUX Output Voltage vs Input Voltage Channel 1 Shown; All Channels Similar

NOTE: All typical values have been characterized but are not tested.

IH5216

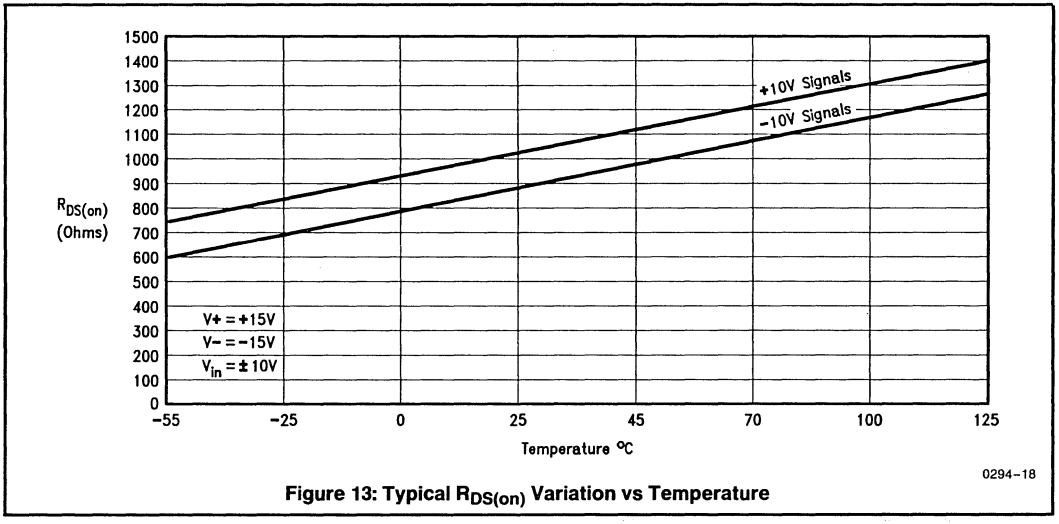


Figure 13: Typical $R_{DS(on)}$ Variation vs Temperature

8

NOTE: All typical values have been characterized but are not tested.

IH5216 APPLICATIONS

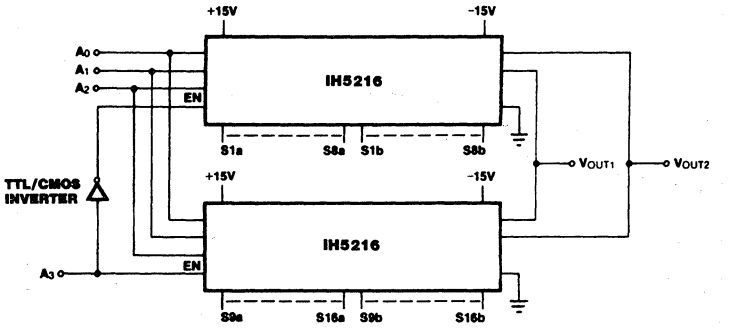


Figure 14: 2 of 32 Channel Multiplexer Using 2 IH5216s

TRUTH TABLE

A_3	A_2	A_1	A_0	On Switch	
0	0	0	0	S1a	
0	0	0	1	S2a	
0	0	1	0	S3a	
0	0	1	1	S4a	
0	1	0	0	S5a	
0	1	0	1	S6a	
0	1	1	0	S7a	
0	1	1	1	S8a	V_{OUT1}
1	0	0	0	S9a	
1	0	0	1	S10a	
1	0	1	0	S11a	
1	0	1	1	S12a	
1	1	0	0	S13a	
1	1	0	1	S14a	
1	1	1	0	S15a	
1	1	1	1	S16a	

TRUTH TABLE

A_3	A_2	A_1	A_0	On Switch	
0	0	0	0	S1b	
0	0	0	1	S2b	
0	0	1	0	S3b	
0	0	1	1	S4b	
0	1	0	0	S5b	
0	1	0	1	S6b	
0	1	1	0	S7b	
0	1	1	1	S8b	V_{OUT2}
1	0	0	0	S9b	
1	0	0	1	S10b	
1	0	1	0	S11b	
1	0	1	1	S12b	
1	1	0	0	S13b	
1	1	0	1	S14b	
1	1	1	0	S15b	
1	1	1	1	S16b	

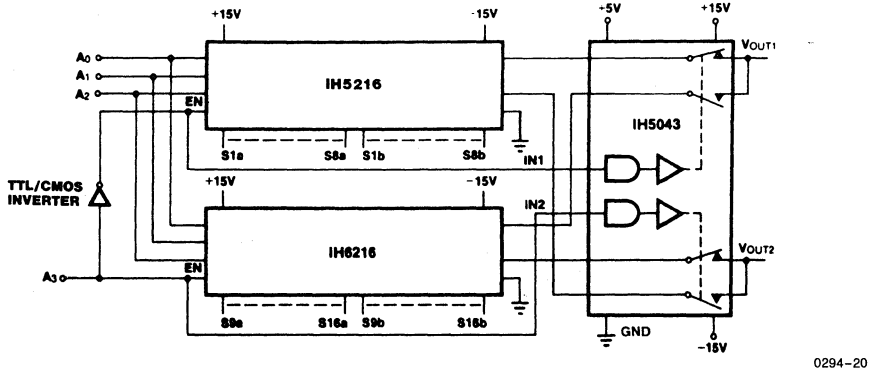


Figure 15: 2 of 32 Multiplexer Using Two IH5216s, and An IH5043 for Submultiplexing

NOTE: All typical values have been characterized but are not tested.

General note on expandability

Figures 14, 15, and 16 show how the IH5216 is expanded. Figure 14 shows a 2 of 32 multiplexer, using 2 IH5216s. Corresponding output points of each of the IH5216s are connected together, and the ENable input strobe is used as the A_3 input. Since each output (pins 2 and 28) corresponds to an "ON" FET and an "OFF" FET, the overall system looks like 1 "ON" FET and 7 "OFF" FETs for each of the V_{out1} and V_{out2} outputs. Thus the output leakage will be 1 $I_{D(on)}$ plus 7 $I_{D(off)}$s or about 0.45nA at room temperature. Throughput speed will be typically 0.6μs for t_{on} and 0.4μs for t_{off}, with throughput channel resistance in the 950Ω area.

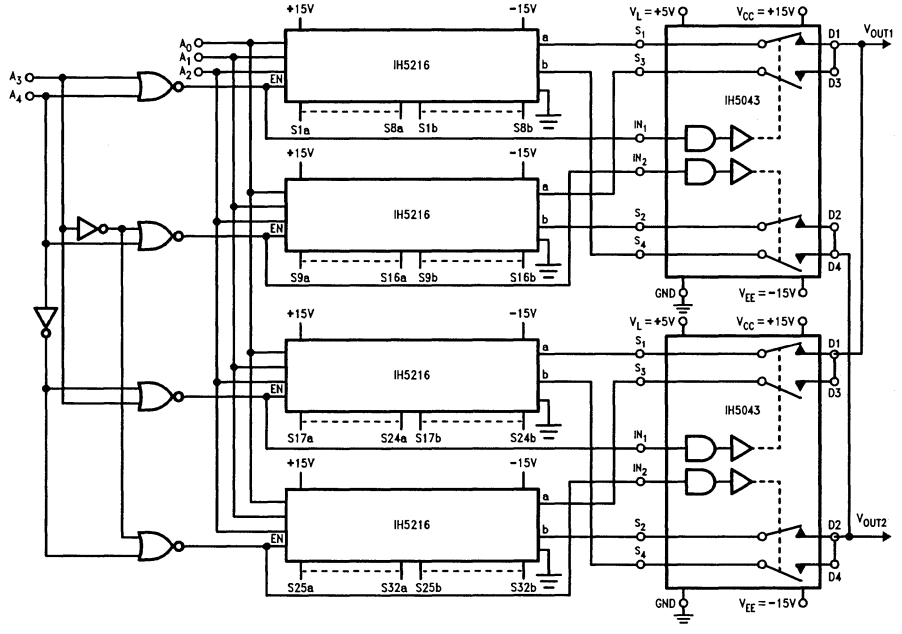


Figure 16: 2 of 64 Multiplexer Using 4 IH5216s and 2 IH5043s as Submultiplexers

NOTE: All typical values have been characterized but are not tested.

Figure 15 shows the 2 of 32 MUX, with a second tier of submultiplexing added to reduce leakage and output capacitance. The IH5043 has typical ON resistance of 50Ω (max. is 75Ω) so it only increases throughput channel resistance from the 900 ohms of Figure 14 to about 950 ohms for Figure 15. Throughput channel speed is a little slower by about 0.5μs for both ON and OFF time, and output leakage is about 0.2nA.

Figure 16 shows a 2 of 64 MUX using 2 tier MUXing (similar to Figure 15). The IH5043 is used for the second tier of MUXing. Each V_{out} point will see 7 OFF channels and 1 ON channel at anytime, so that the typical leakages will be about 0.45nA. Throughput channel resistance will be in the 950Ω area and throughput switching speeds about 1.3μs for ON time and 0.8μs for OFF time.

The IH5043 was chosen as the second tier of the MUX because it will switch the same AC signals as the 5216 (typically plus and minus 15V) and uses break before make switching. Also power supply quiescent currents are typically 1-2μA so that no excessive system power is generated. Note that the logic of the 5043 is such that it can be tied directly to the ENable input (as shown in the figures) with no extra logic being required.

Enable input strobing levels

The ENable input acts as an enabling or disabling pin for the 5216 when used as a 2 out of 16 channel MUX, however when expanding the MUX to more than 16 channels, the EN pin acts as another address input. Figures 14 and 15 show the EN pin used as the A_3 input. TTL and the Enable input is CMOS compatible.

APPLICATION NOTES

Further information may be found in:

A003 "Understanding and Applying the Analog Switch"

A006 "A New CMOS Analog Gate Technology"

A020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing"

R009 "Reduce CMOS Multiplexer Troubles through Proper Device Selection"

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

IH6108
8-Channel CMOS Analog Multiplexer

GENERAL DESCRIPTION

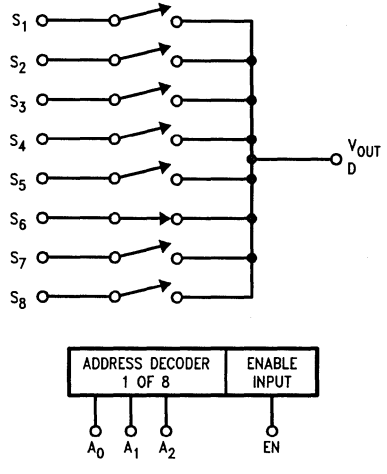
The IH6108 is a CMOS one of 8 multiplexer. The part is a plug-in replacement for the DG508A. Three line decoding is used so that the 8 channels can be controlled by 3 Address inputs; additionally a fourth input is provided for use as a system enable. When the ENable input is high (5V), a channel is selected by the three Address inputs, and when low (0V) all channels are off. The 3 Address inputs are TTL and CMOS logic compatible, with a "1" corresponding to any voltage greater than 2.4V.

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH6108MJE	−55°C to +125°C	16 pin CERDIP
IH6108CJE	0°C to 70°C	16 pin CERDIP
IH6108CPE	0°C to 70°C	16 pin plastic DIP

FEATURES

- **Ultra Low Leakage — $I_{D(off)} \leq 100$pA Typical**
- **$r_{DS(on)} < 400$ Ohms Over Full Signal and Temperature Range**
- **Power Supply Quiescent Current Less Than 100μA**
- **$\pm$14V Analog Signal Range**
- **No SCR Latchup**
- **Break-Before-Make Switching**
- **Binary Address Control (3 Address Inputs Control 8 Channels)**
- **TTL and CMOS Compatible Strobe Control**
- **Pin Compatible With DG508A, HI-508 & ADG508A**
- **Internal Diode In Series With V^+ for Fault Protection**



3 LINE BINARY ADDRESS INPUTS
(1 0 1) AND EN @ 5V
ABOVE EXAMPLE SHOWS CHANNEL 6 TURNED ON.

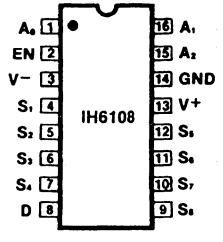
0297-1

Figure 1: Functional Diagram

TRUTH TABLE

A_2	A_1	A_0	EN	On Switch
x	x	x	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2
Logic "1" = $V_{AH} \geq 2.4V$, $V_{ENH} \geq 4.5V$
Logic "0" = $V_{AL} \leq 0.8V$



0297-2

Figure 2: Pin Configuration

8

305530-004

NOTE: All typical values have been characterized but are not tested.

IH6108

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V to 15V
V_S or V_D to V+ ..... 0, −36V
V_S or V_D to V− 0, 36V
V+ to Ground 18V
V− to Ground ..... −18V
Current (Any Terminal) ..... 30 mA
Current (Analog Source or Drain) ..... 20 mA
Operating Temperature
C Suffix ..... 0°C to +70°C
M Suffix ..... −55°C to +125°C
Storage Temperature ..... −65 to 150°C
C Suffix ..... −65°C to +125°C
M Suffix ..... −65°C to +150°C

Lead Temperature (Soldering, 10 sec) ..... 300°C
Power Dissipation*
CERDIP Package** ..... 900 mW
Plastic Package*** ..... 470 mW

* Device mounted with all leads soldered or welded to PC board.
** Derate 12 mW/°C above 75°C
*** Derate 6.3 mW/°C above 75°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

$V^+ = 15V$, $V^- = -15V$, $V_{EN} = +5V$ (Note 1), Ground = 0V, unless otherwise specified.

Characteristic	Measured Terminal	No Tests Per Temp	Typ 25°C	Test Conditions		Max Limits M Suffix −55°C	M Suffix 25°C	M Suffix 125°C	C Suffix 0°C	C Suffix 25°C	C Suffix 70°C	Units
SWITCH												
$R_{DS(on)}$	S to D	8	180	$V_D = +10V$, $I_S = -1.0mA$	Sequence each switch on	300	300	400	350	350	450	Ω
		8	150	$V_D = -10V$, $I_S = -1.0mA$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$	300	300	400	350	350	450	
$\Delta R_{DS(on)}$			20	$R_{DS(on)} = \frac{R_{DS(on)max} - R_{DS(on)min}}{R_{DS(on)avg.}}$, $V_S = \pm 10V$								%
$I_{S(OFF)}$	S	8	0.002	$V_S = 10V$, $V_D = -10V$	$V_{EN} = 0.8V$		±.5	±50		±1	±50	nA
		8	0.002	$V_S = -10V$, $V_D = 10V$			±.5	±50		±1	±50	
$I_{D(OFF)}$	D	1	0.03	$V_D = 10V$, $V_S = -10V$			±2	±100		±5	±100	
		1	0.03	$V_D = -10V$, $V_S = 10V$			±2	±100		±5	±100	
$I_{D(ON)}$	D	8	0.1	$V_{S(ALL)} = V_D = 10V$	Sequence each switch on $V_{AL} = 0.8V$, $V_{AH} = 2.4V$		±2	±100		±5	±100	
		8	0.1	$V_{S(ALL)} = V_D = -10V$			±2	±100		±5	±100	
INPUT												
$I_{AN(ON)}$ or $I_{A(on)}$	A_0, A_1 or A_2 Inputs	3	0.01	$V_A = 0V$			−10	−30		−10	−30	μA
$I_{AN(OFF)}$ $I_{A(off)}$		3	0.01	$V_A = 14V$			10	30		10	30	
I_A	A_0, A_1, A_2	3	0.01	$V_{EN} = 5V$	All $V_A = 0V$ (Address pins)		−10	−30		−10	−30	
	EN	1	0.01	$V_{EN} = 0V$			−10	−30		−10	−30	
DYNAMIC												
$t_{transition}$	D		0.3	See Fig. 3			1					μs
t_{open}	D		0.2	See Fig. 4								
$t_{on(EN)}$	D		0.6	See Fig. 5			1.5					
$t_{off(EN)}$	D		0.4				1					
"OFF" Isolation	D		60	$V_{EN} = 0V$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3VRMS$, $f = 500kHz$								dB
$C_{s(off)}$	S		5	$V_S = 0V$	$V_{EN} = 0V$, f = 140kHz to 1MHz							pF
$C_{d(off)}$	D		25	$V_D = 0V$								
$C_{DS(off)}$	D to S		1	$V_S = 0V$, $V_D = 0V$								

NOTE 1: See "Enable Input Strobing Levels", in Application Section.

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued)

$V^+ = 15V$, $V^- = -15V$, $V_{EN} = +5V$ (Note 1), Ground = 0V, unless otherwise specified.

Characteristic		Measured Terminal	No Tests Per Temp	Typ 25°C	Test Conditions		Max Limits						Units
							M Suffix			C Suffix			
							−55°C	25°C	125°C	0°C	25°C	70°C	
SUPPLY													
Supply Current	+	V^+	1	40	$V_{EN} = 5V$	All $V_A = 0V$ or 5V		200			1000		μA
	−	V^-	1	2				100			1000		
Standby Current	+	V^+	1	1	$V_{EN} = 0V$			100			1000		
	−	V^-	1	1				100			1000		

SWITCHING INFORMATION

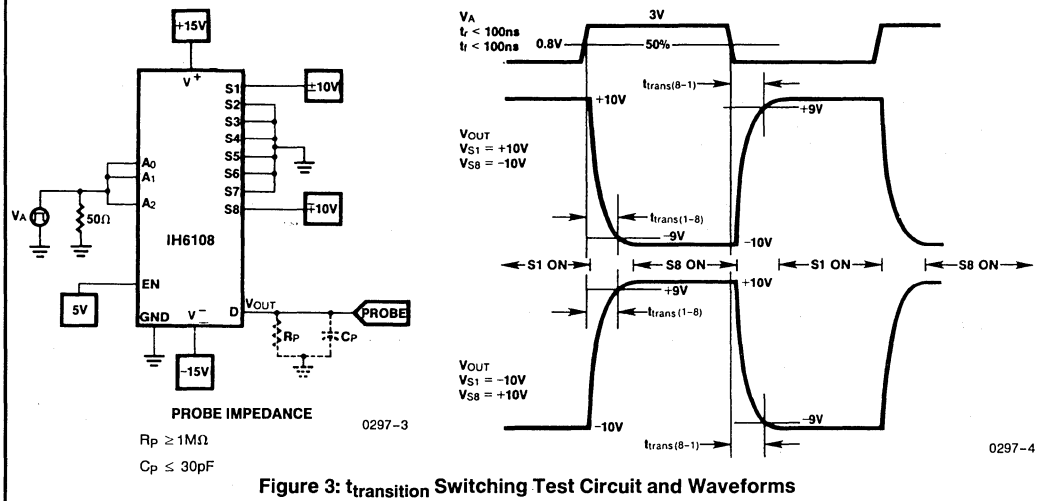


Figure 3: $t_{transition}$ Switching Test Circuit and Waveforms

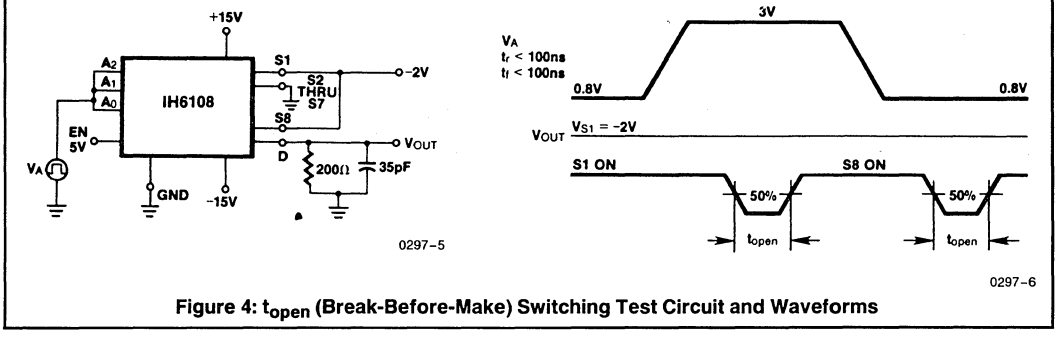


Figure 4: t_{open} (Break-Before-Make) Switching Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

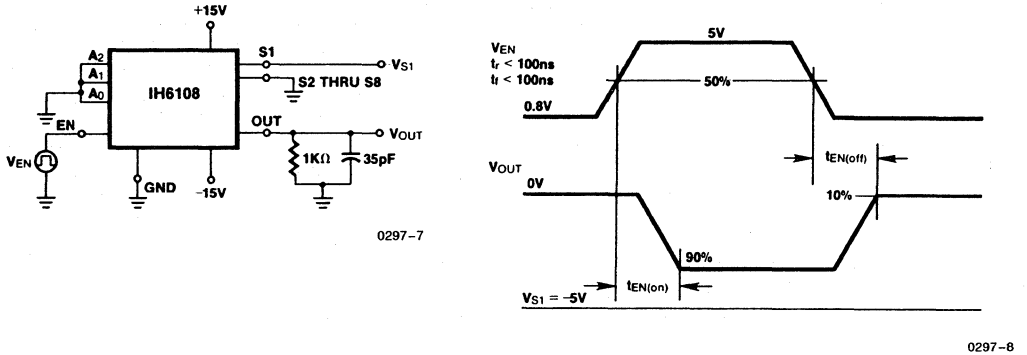


Figure 5: t_{on} and t_{off} Switching Test Circuit and Waveforms

IH6108 APPLICATION INFORMATION

ENable Input Strobing Levels

The ENable input on the IH6108 requires a minimum of +4.5V to trigger to the "1" state and a maximum of +0.8V to trigger to the "0" state. If the ENable input is being driven from TTL logic, a pull-up resistor of 1k to 3kΩ is required from the gate output to +5V supply. (See Figure 6)

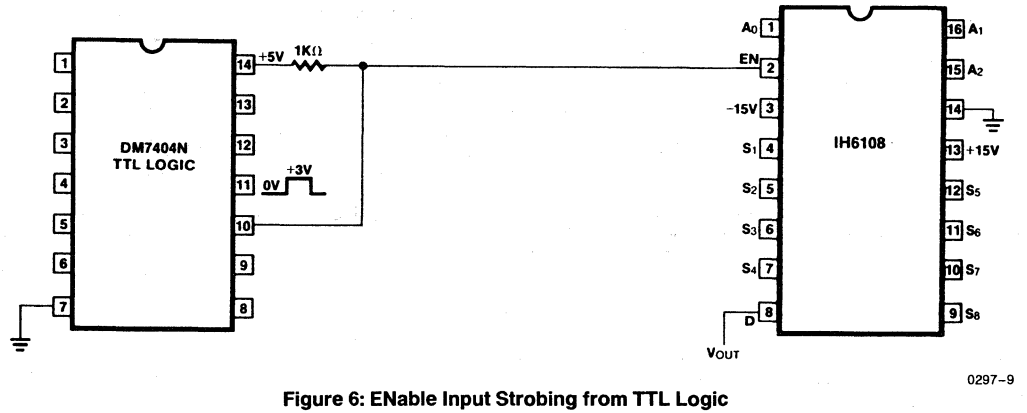


Figure 6: ENable Input Strobing from TTL Logic

When the EN input is driven from CMOS logic, no pullup is necessary, see Fig. 7.

NOTE: All typical values have been characterized but are not tested.

IH6108 APPLICATION INFORMATION (Continued)

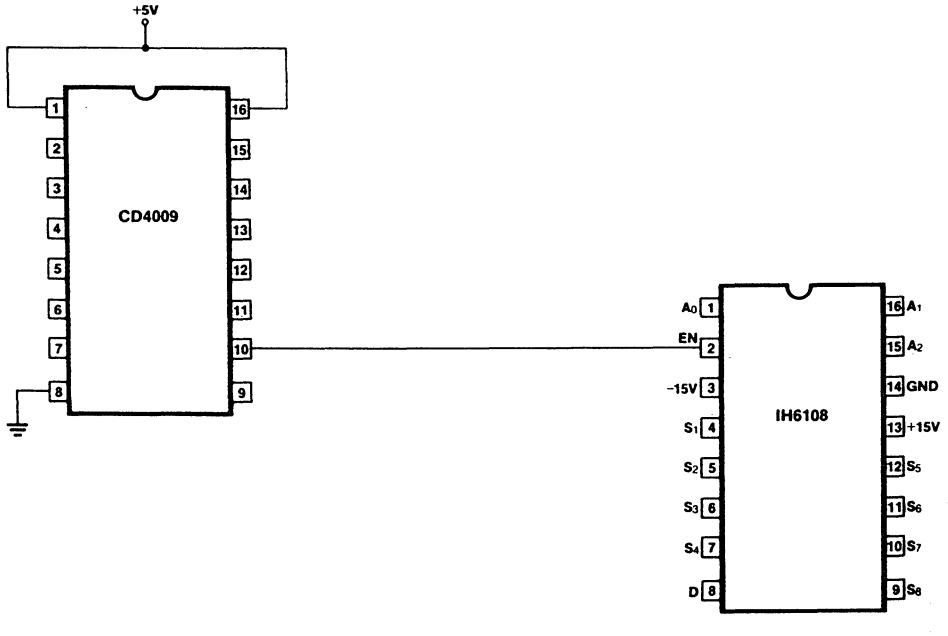


Figure 7: ENable Input Driven from CMOS Logic

The supply voltage of the CD4009 affects the switching speed of the IH6108; the same is true for TTL supply voltage levels. The following chart shows the effect, on t_{trans} for a supply varying from +4.5V to +5.5V.

CMOS or TTL Supply Voltage	Typical t_{trans} @ 25°C
+4.5V	400ns
+4.75V	300ns
+5.00V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the ENable Strobe Logic.

The examples shown in Figures 6 and 7 deal with ENable strobing when expansion to more than eight channels is required. In these cases the EN terminal acts as a fourth address input. If eight channels or less are being multiplexed, the EN terminal can be directly connected to +5V logic supply to enable the IH6108 at all times.

Using the IH6108 with supplies other than ±15V

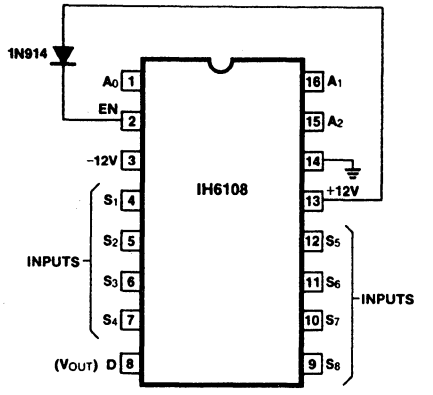
The IH6108 can be used with power supplies ranging from ±6V to ±16V. The switch $r_{DS(on)}$ will increase as the supply voltages decrease, however, the multiplexer error term (the product of leakage times $r_{DS(on)}$) will remain approximately constant since leakage decreases as the supply voltages are reduced.

Caution must be taken to ensure that the enable (EN) voltage is at least 0.7V below V^+ at all times. If this is not done, the Address input strobing levels will not function properly. This may be achieved quite simply by connecting EN (pin 2) to V^+ (pin 13) via a silicon diode as shown in Figure 8. When using this type of configuration, a further requirement must be met: the strobe levels of A0 and A1 must be within 2.5V of the EN voltage in order to define a binary "1" state. For the case shown in Figure 8 the EN voltage is 11.3V which means that logic high at A0 and A1 is = +8.8V (logic low continues to be = 0.8V). In this configuration the IH6108 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the IH6108 have common supplies, the EN pin should again be connected to the supply through a silicon diode. In this case, tying EN to the logic supply directly will not work since it violates the 0.7V differential voltage required between V^+ and EN, (See Figure 9). A 1μF capacitor can be placed across the diode to minimize switching glitches.

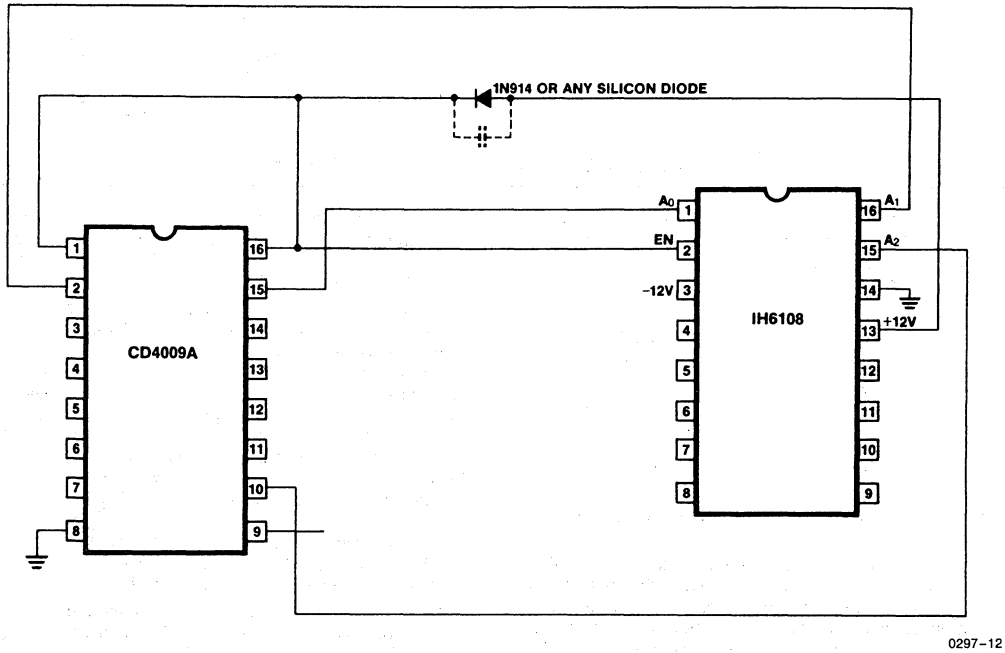
NOTE: All typical values have been characterized but are not tested.

IH6108 APPLICATION INFORMATION (Continued)



0297-11

Figure 8: IH6108 Connection Diagram for less than ±15V Supply Operation



0297-12

Figure 9: IH6108 Connection Diagram with ENable Input Strobing for less than ±15V Supply Operation

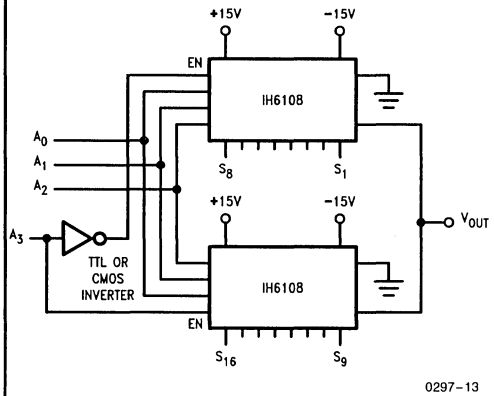
Peak-to-Peak Signal Handling Capability

The IH6108 can handle input signals up to ±14V (actually −15V to +14.3V because of the input protection diode) when using ±15V supplies.

The electrical specifications of the IH6108 are guaranteed for ±10V signals, but the specifications have very minor changes for ±14V signals. The notable changes are slightly lower $r_{DS(on)}$ and slightly higher leakages.

NOTE: All typical values have been characterized but are not tested.

IH6108 APPLICATIONS INFORMATION



NOTE: TTL inverter must have pullup resistor to +5V to drive EN input.

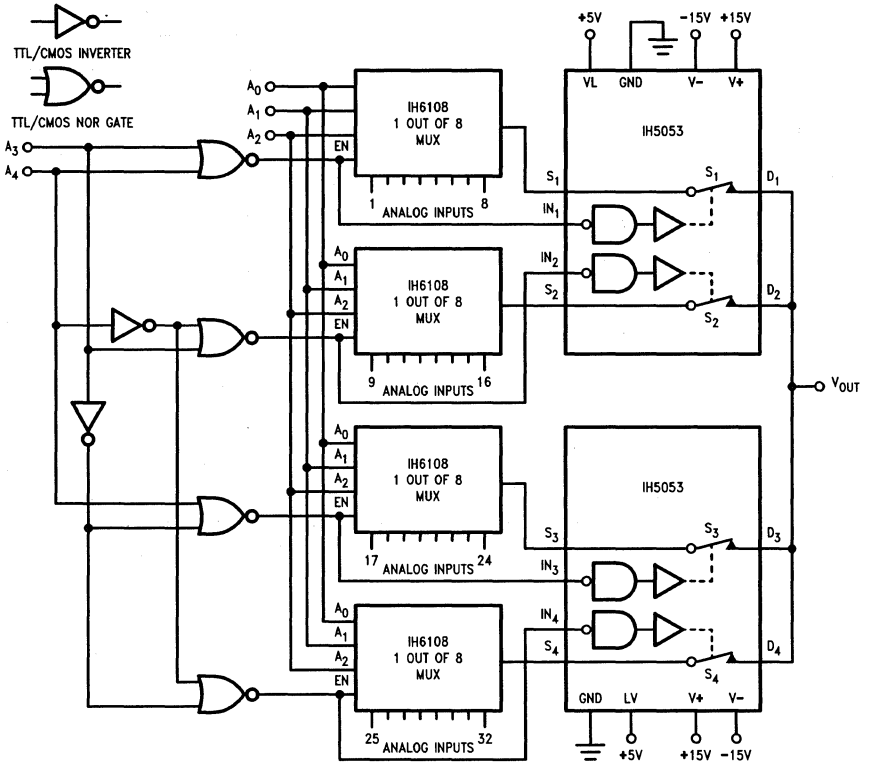
TRUTH TABLE

A_3	A_2	A_1	A_0	On Switch
0	0	0	0	S1
0	0	0	1	S2
0	0	1	0	S3
0	0	1	1	S4
0	1	0	0	S5
0	1	0	1	S6
0	1	1	0	S7
0	1	1	1	S8
1	0	0	0	S9
1	0	0	1	S10
1	0	1	0	S11
1	0	1	1	S12
1	1	0	0	S13
1	1	0	1	S14
1	1	1	0	S15
1	1	1	1	S16

Figure 10: 1 of 16 Channel Multiplexer Using Two IH6108's. Overvoltage Protection Is Maintained Between All Channels, As Is Break-Before-Make Switching.

NOTE: All typical values have been characterized but are not tested.

IH6108 APPLICATIONS INFORMATION



NOTE: TTL NOR gate must have pullup resistor to +5V to drive EN inputs.

TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	On Switch
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	On Switch
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

Figure 11: 1 of 32 Multiplexer Using 4 IH6108s and Two IH5053's As A Submultiplexer

NOTE: All typical values have been characterized but are not tested.

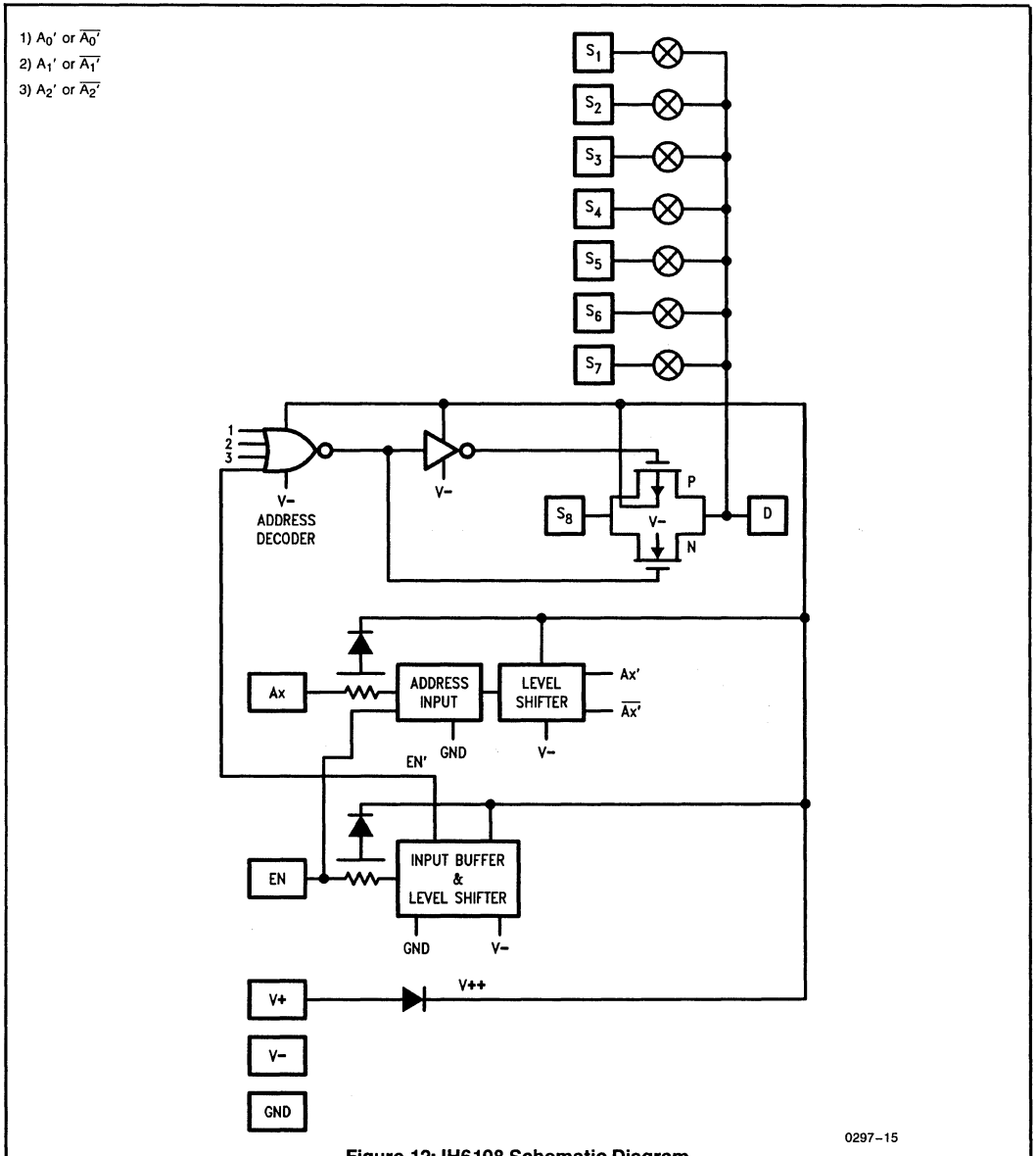


Figure 12: IH6108 Schematic Diagram

NOTE: All typical values have been characterized but are not tested.

IH6108

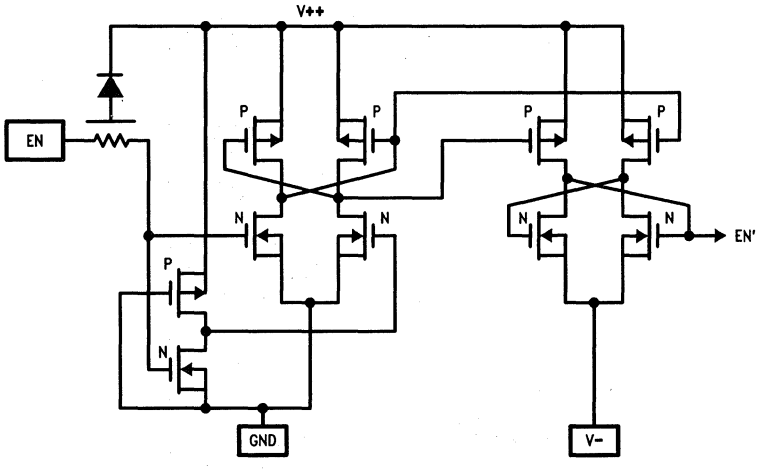


Figure 13: Enable Input and Level Shifter

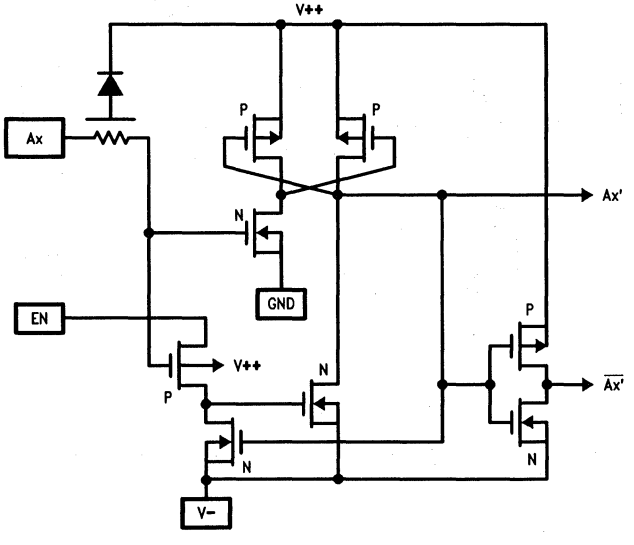


Figure 14: Address Input and Level Shifter

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

IH6208
4-Channel Differential CMOS Analog Multiplexer

GENERAL DESCRIPTION

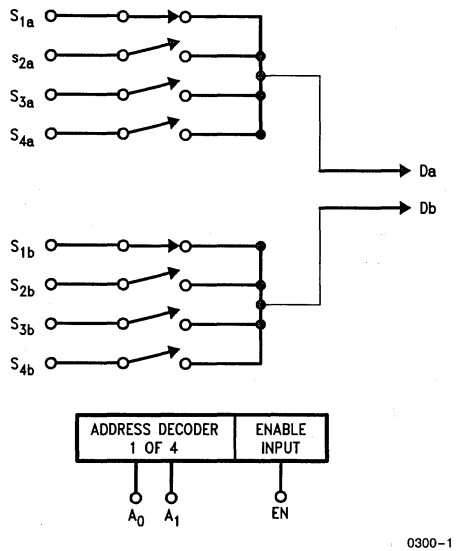
The IH6208 is a 2 of 8 CMOS multiplexer. The part is a plug-in replacement for the DG509A. Two line binary decoding is used so that the 8 channels can be controlled in pairs by the binary inputs; additionally a third input is provided to use as a system enable. When the ENable input is high (5V) the channels are sequenced by the 2 line binary inputs, and when low (0V) all channels are off. The 2 Address inputs are controlled by TTL logic or CMOS logic elements with a "0" corresponding to any voltage less than 0.8V and a "1" corresponding to any voltage greater than 2.4V. Note that the ENable input must be taken to 5V to enable the system, and less than 0.8V to disable the system.

ORDERING INFORMATION

Part Number	Temperature Range	Package
IH6208MJE	−55°C to +125°C	16 pin CERDIP
IH6208CJE	0°C to 70°C	16 pin CERDIP
IH6208CPE	0°C to 70°C	16 pin Plastic DIP

FEATURES

- **Ultra Low Leakage — $I_{D(off)} \leq 100pA$ Typical**
- **$r_{DS(on)} < 400$ Ohms Over Full Signal and Temperature Range**
- **Power Supply Quiescent Current Less Than 100μA**
- **$\pm$14V Analog Signal Range**
- **No SCR Latchup**
- **Break-Before-Make Switching**
- **Binary Address Control (2 Address Inputs Control 2 Out of 8 Channels)**
- **TTL and CMOS Compatible Address Control**
- **Pin Compatible With HI509, DG509A & ADG509A**
- **Internal Diode In Series With V^+ For Fault Protection**



2 LINE BINARY ADDRESS INPUTS
(0 0) AND EN = 5V (EN = "1" FOR +5V, "0" FOR 0V)
ABOVE EXAMPLE SHOWS CHANNELS 1a AND 1b ON

Figure 1: Functional Diagram

TRUTH TABLE

A_1	A_0	EN	On Switch Pair
X	X	0	NONE
0	0	1	1a, 1b
0	1	1	2a, 2b
1	0	1	3a, 3b
1	1	1	4a, 4b

A_0, A_1
LOGIC "1" = $V_{AH} \geq 2.4V$ $V_{ENH} \geq 4.5V$
LOGIC "0" = $V_{AL} \leq 0.8V$

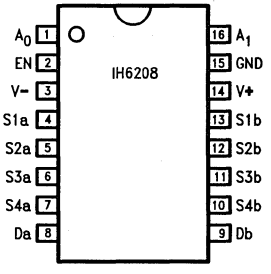


Figure 2: Pin Configuration

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V, 15V
V_S or V_D to V^+ ..... 0, −36V
V_S or V_D to V^- 0, 36V
V^+ to Ground 18V
V^- to Ground ..... −18V
Current (Any Terminal) 30mA
Current (Analog Source or Drain) 20mA
Operating Temperature
C Suffix .....0°C to +70°C
M Suffix .....−55°C to +125°C
Storage Temperature
C Suffix .....−65°C to +125°C
M Suffix .....−65°C to +150°C
Lead Temperature (Soldering, 10 sec).....300°C
Power Dissipation*
CERDIP Package**.....900 mW
Plastic Package*** .....470 mW

*Device mounted with all leads soldered or welded to PC board.
**Derate 12 mW/°C above 75°C
***Derate 6.3 mW/°C above 75°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

$V^+ = 15V$, $V^- = -15V$, $V_{EN} = +5V$ (Note 1), Ground = 0V, unless otherwise specified.

Characteristic		Measured Terminal	No Tests Per Temp	Typ 25°C	Test Conditions		Max Limits M Suffix −55°C	M Suffix 25°C	M Suffix 125°C	C Suffix 0°C	C Suffix 25°C	C Suffix 70°C	Units
SWITCH													
$R_{DS(ON)}$		S to D	8	180	$V_D = +10V$, $I_S = -1.0mA$	Sequence each switch on	300	300	400	350	350	450	Ω
			8	150	$V_D = -10V$, $I_S = -1.0mA$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$	300	300	400	350	350	450	
$\Delta R_{DS(ON)}$				20	$\Delta R_{DS(on)} = \frac{R_{DS(on)max} - R_{DS(on)min}}{R_{DS(on)avg.}}$, $V_S = \pm 10V$								%
$I_{S(OFF)}$		S	8	0.002	$V_S = 10V$, $V_D = -10V$			±.5	±50		±1	±50	nA
			8	0.002	$V_S = -10V$, $V_D = 10V$			±.5	±50		±1	±50	
$I_{D(OFF)}$		D	2	0.03	$V_D = 10V$, $V_S = -10V$	$V_{EN} = 0.8V$		±2	±50		±5	±100	
			2	0.03	$V_D = -10V$, $V_S = 10V$			±2	±50		±5	±100	
$I_{D(ON)}$		D	8	0.1	$V_{S(ALL)} = V_D = 10V$	Sequence each switch on		±2	±50		±5	±100	
			8	0.1	$V_{S(ALL)} = -10V$	$V_{AL} = 0.8V$, $V_{AH} = 2.4V$		±2	±50		±5	±100	
INPUT													
$I_{A(on)}$		A_0, A_1	2	0.01	$V_A = 0V$			−10	−30		−10	−30	μA
$I_{A(off)}$			2	0.01	$V_A = 14V$			10	30		10	30	
I_A		A_0, A_1	2	0.01	$V_{EN} = 5V$	All $V_A = 0V$ (Address Pins)		−10	−30		−10	−30	
		EN	1	0.01	$V_{EN} = 0V$			−10	−30		−10	−30	
DYNAMIC													
$t_{transition}$		D		0.3	See Fig. 3			1					μs
t_{open}		D		0.2	See Fig. 4								
$t_{EN(on)}$		D		0.6	See Fig. 5			1.5					
$t_{EN(off)}$		D		0.4				1					
"OFF" Isolation		D		60	$V_{EN} = 0V$, $R_L = 200\Omega$, $C_L = 3pF$, $V_S = 3VRMS$, $f = 500kHz$								dB
$C_{s(off)}$		S		5	$V_S = 0V$	$V_{EN} = 0V$, $f = 140kHz$ to 1MHz							pF
$C_{d(off)}$		D		12	$V_D = 0V$								
$C_{ds(off)}$		D to S		1	$V_S = 0V$, $V_D = 0V$								
SUPPLY													
Supply	+	V^+	1	40		All $V_A = 0V$ or 5V		200			1000		μA
Current	−	V^-	1	2	$V_{EN} = 5V$			100			1000		
Standby	+	V^+	1	1				100			1000		
Current	−	V^-	1	1	$V_{EN} = 0V$			100			1000		

NOTE 1: See "Enable Input Strobing Levels", in Application Section.

NOTE: All typical values have been characterized but are not tested.

SWITCHING INFORMATION

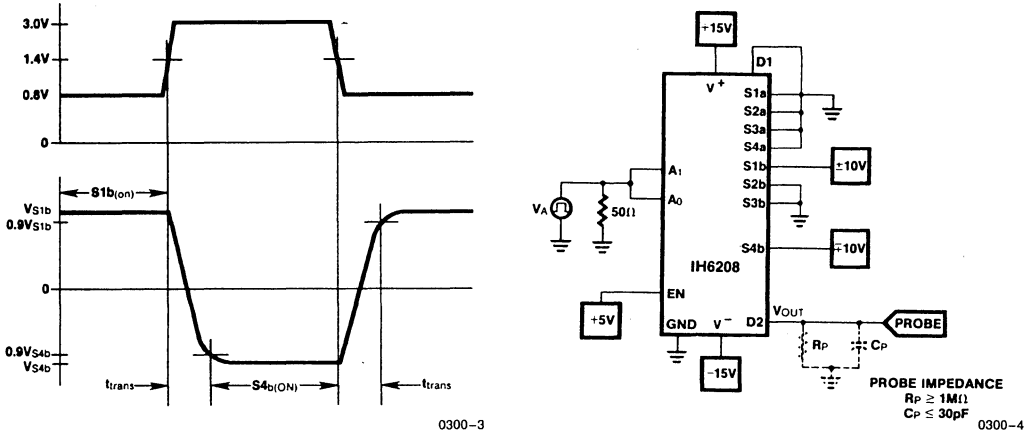


Figure 3: t_{trans} Switching Test Circuit and Waveforms

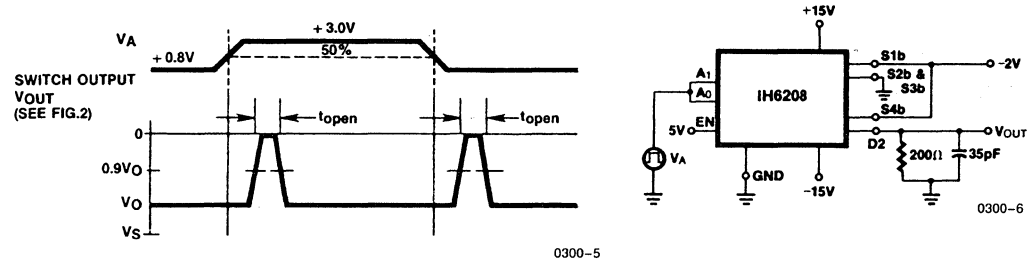


Figure 4: t_{open} (Break-Before-Make) Switching Test Circuit and Waveforms

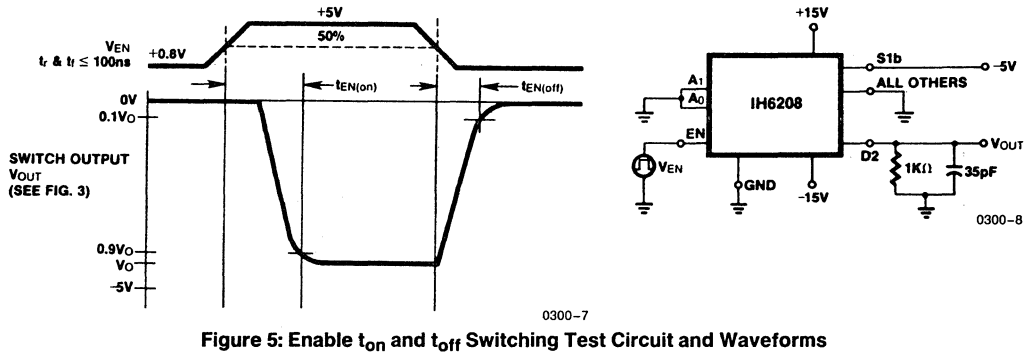


Figure 5: Enable t_{on} and t_{off} Switching Test Circuit and Waveforms

NOTE: All typical values have been characterized but are not tested.

IH6208 APPLICATION INFORMATION

ENable Input Strobing Levels

The ENable input on the IH6208 requires a minimum of +4.5V to trigger it into the "1" state and a maximum of +0.8V to trigger it into the "0" state. If the ENable input is being driven from TTL logic, a pull-up resistor of 1k to 3kΩ is required from the gate output to +5V supply. (See Figure 6).

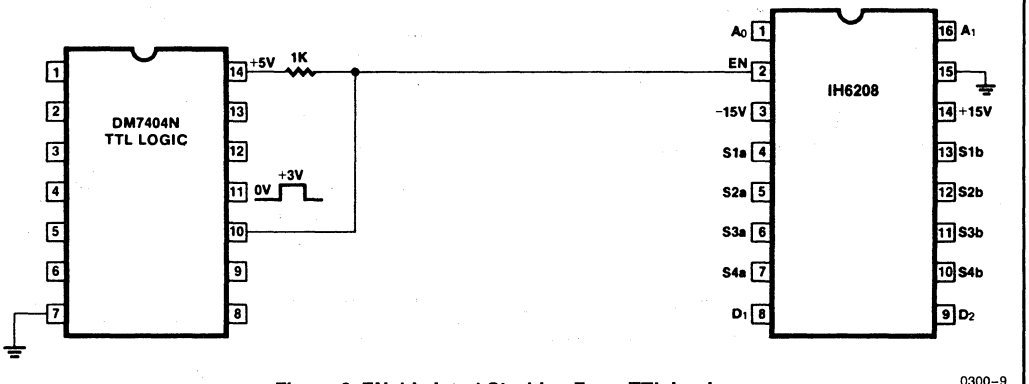


Figure 6: ENable Input Strobing From TTL Logic

When the EN input is driven from CMOS logic, no pullup is necessary. (See Fig. 7)

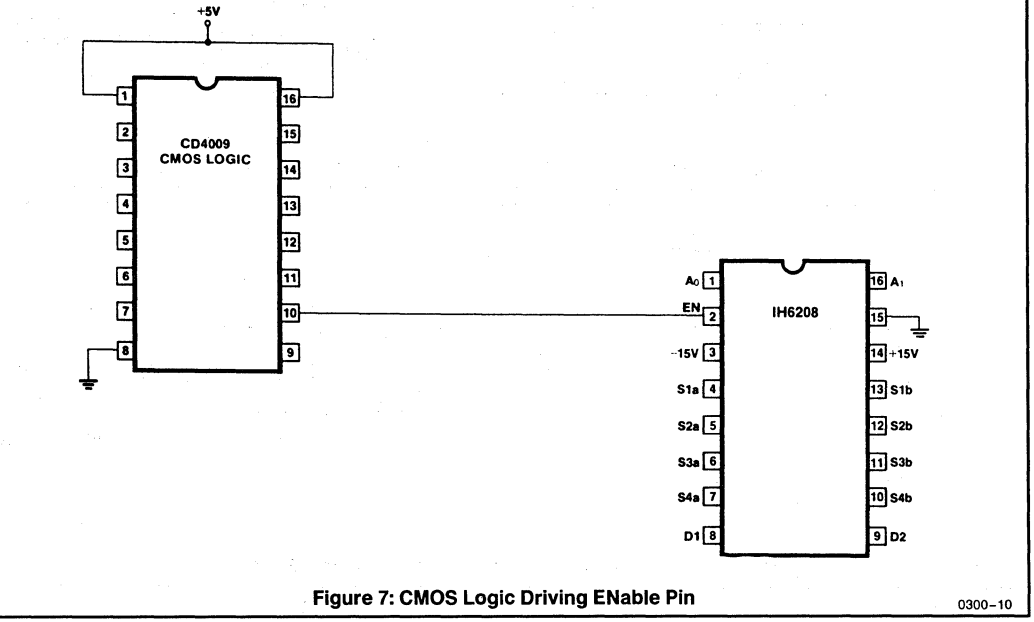


Figure 7: CMOS Logic Driving ENable Pin

NOTE: All typical values have been characterized but are not tested.

IH6208 APPLICATION INFORMATION (Continued)

The supply voltage of the CD4009 affects the switching speed of the IH6208; the same is true for TTL supply voltage levels. The chart below shows the effect on t_{trans} for a supply varying from +4.5V to +5.5V.

CMOS OR TTL SUPPLY	TYPICAL t_{trans} @ 25°C
+4.5V	400ns
+4.75V	300ns
+5.0V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the ENable Strobe Logic.

The examples shown in Figures 6 and 7 deal with ENable strobing when expansion to more than four differential channels is required; in these cases the EN terminal acts as a third address input. If four channel pairs or less are being multiplexed, the EN terminal can be directly connected to +5V to enable the IH6208 at all times.

Using the IH6208 with supplies other than ±15V

The IH6208 can be used with power supplies ranging from ±6V to ±16V. The switch $r_{DS(on)}$ will increase as the supply voltages decrease, however, the multiplexer error term (the product of leakage times $r_{DS(on)}$) will remain approximately constant since leakage decreases as the supply voltages are reduced.

Caution must be taken to ensure that the enable (EN) voltage is at least 0.7V below V^+ at all times. If this is not done the Address Input strobing levels will not function properly. This may be achieved quite simply by connecting EN (pin 2) to V^+ (pin 14) via a silicon diode as shown in Figure 8. A further requirement must be met when using this type of configuration; the strobe levels at A0 and A1 must be within 2.5V of the EN voltage in order to define a binary "1" state. For the case shown in Figure 8 the EN voltage is 11.3V, which means that logic high at A0 and A1 is = +8.8V (logic low continues to be = 0.8V). In this configuration the IH6208 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the IH6208 have common supplies, the EN pin should again be connected to the supply through a silicon diode. In this case, tying EN to the logic supply directly will not work since it violates the 0.7V differential voltage required between V^+ and EN (See Figure 9). A 1μF capacitor can be placed across the diode to minimize switching glitches.

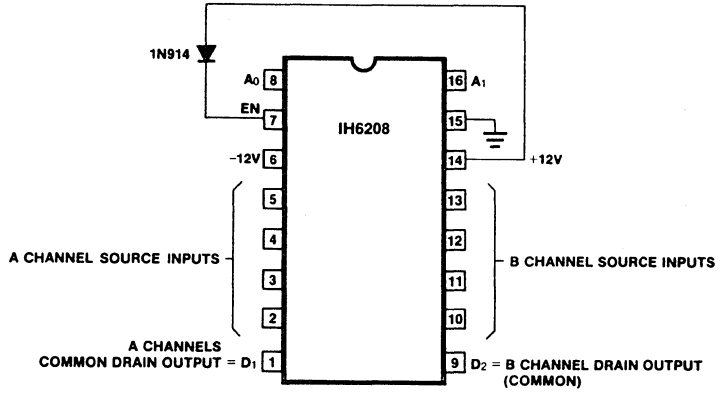


Figure 8: IH6208 Connection Diagram for Less Than ±15V Supply Operation

NOTE: All typical values have been characterized but are not tested.

IH6208 APPLICATION INFORMATION (Continued)

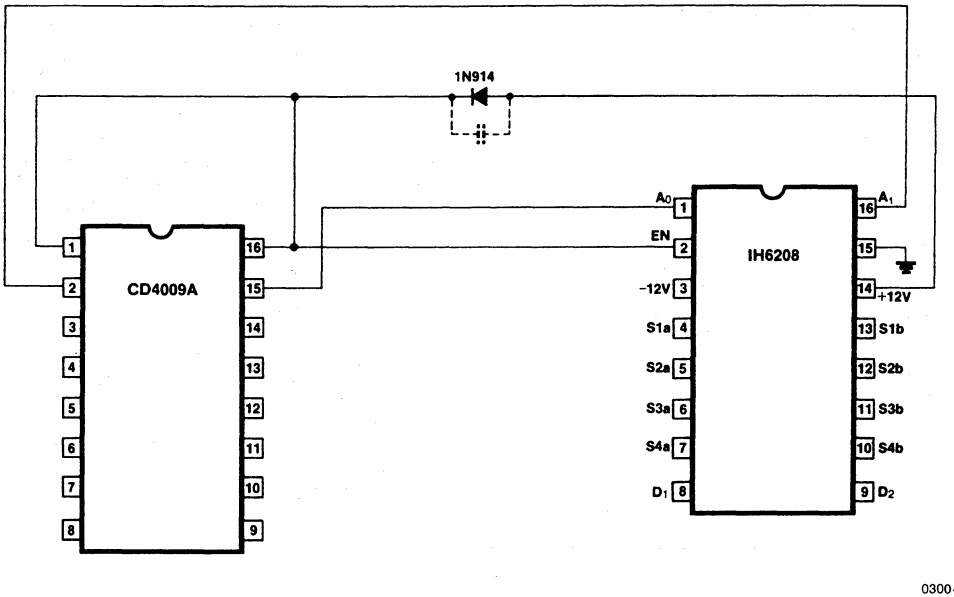


Figure 9: IH6208 Connection Diagram With ENable Input Strobing for Less Than ±15V Supply Operation

Peak-to-Peak Signal Handling Capability

The IH6208 can handle input signals up to ±14V (actually −15V to +14.3V because of the input protection diode) when using ±15V supplies.

The electrical specifications of the IH6208 are guaranteed for ±10V signals, but the specifications have very minor changes for ±14V signals. The notable changes are slightly lower $r_{DS(on)}$ and slightly higher leakages.

NOTE: All typical values have been characterized but are not tested.

IH6208 APPLICATION INFORMATION (Continued)

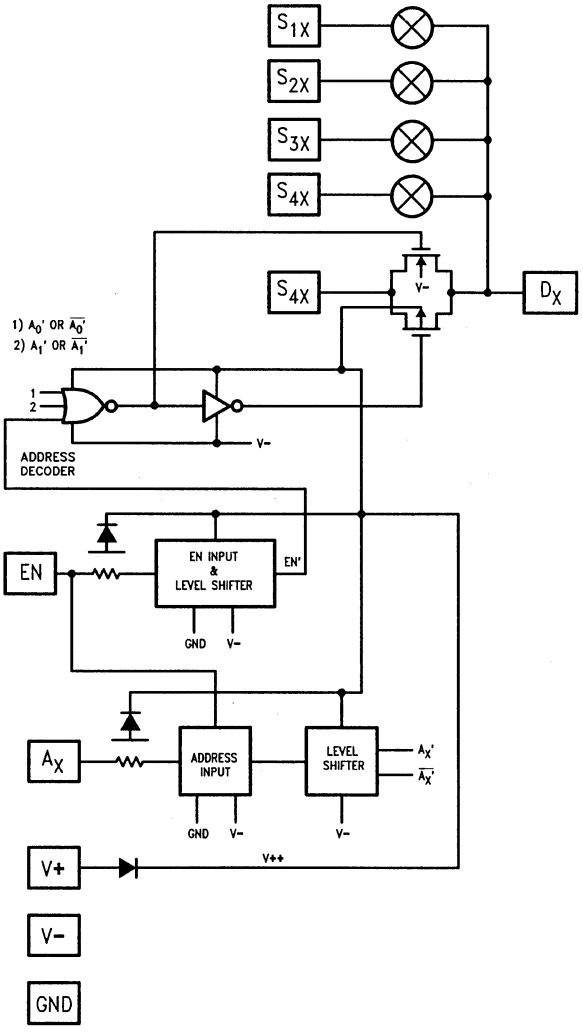


Figure 10: ½ IH6208 Schematic Diagram

NOTE: All typical values have been characterized but are not tested.

IH6208 APPLICATION INFORMATION (Continued)

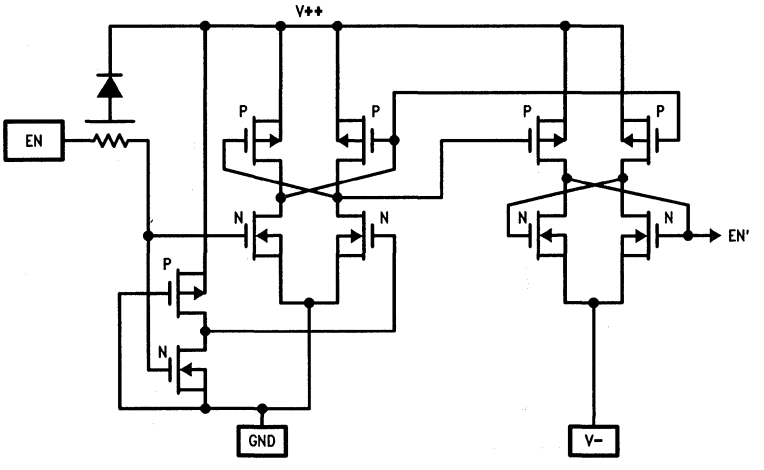


Figure 11: Enable Input and Level Shifter

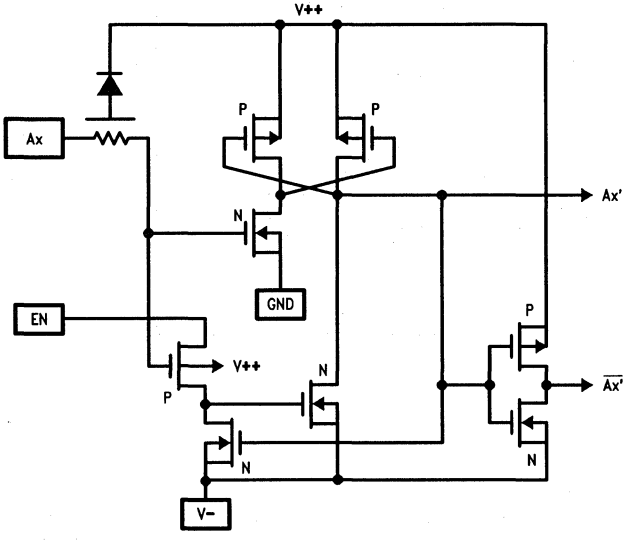


Figure 12: Address Input and Level Shifter

NOTE: All typical values have been characterized but are not tested.

DATA ACQUISITION 9

DISPLAY DRIVERS

HARRIS SEMICONDUCTOR

CA3161

BCD-to-Seven-Segment Decoder/Driver

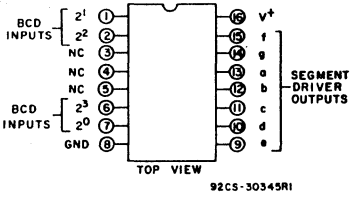
Features:

- *TTL-compatible input logic levels*
- *25-mA [typ.] constant-current segment outputs*
- *Eliminates need for output current-limiting resistors*
- *Pin compatible with other industry standard decoders*
- *Low standby power dissipation - 18 mW (typ.)*

The RCA-CA3161E is a monolithic intergrated circuit that performs the BCD-to-seven-segment decoding function and features constant-current segment drivers. When used with the CA3162E A/D Converter* the CA3161E provides a complete digital readout system with a minimum number of external parts.

The CA3161 is supplied in the 16-lead dual-in-line plastic package (E suffix). The CA3161 is also available in chip form (H suffix).

*The CA3162E is described in RCA data bulletin File No. 1080.



TERMINAL ASSIGNMENT
CA3161E

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (between terminals 1 and 10) ..... +7 V

INPUT VOLTAGE (terminals 1, 2, 6, 7) ..... +5.5 V

OUTPUT VOLTAGE:

Output "Off" ..... +7 V

Output "On" (See note 1) ..... +10 V

DEVICE DISSIPATION:

Up to T_A = +55°C ..... 1 W

Above T_A = +55°C ..... derate linearly at 10.5 mW/°C

AMBIENT TEMPERATURE RANGE:

Operating ..... 0 to +75°C

Storage ..... −65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

NOTE 1: This is the maximum output voltage for any single output. The output voltage must be consistent with the maximum dissipation and derating curve for worst-case conditions. Example: All segments "on", 100% duty cycle.

File Number **1079**

TRUTH TABLE

BINARY STATE	INPUTS				OUTPUTS							DISPLAY
	2^3	2^2	2^1	2^0	a	b	c	d	e	f	g	
0	L	L	L	L	L	L	L	L	L	L	H	0
1	L	L	L	H	H	L	L	H	H	H	H	1
2	L	L	H	L	L	L	H	L	L	H	L	2
3	L	L	H	H	L	L	L	L	H	H	L	3
4	L	H	L	L	H	L	L	H	H	L	L	4
5	L	H	L	H	L	H	L	L	H	L	L	5
6	L	H	H	L	L	H	L	L	L	L	L	6
7	L	H	H	H	L	L	L	H	H	H	H	7
8	H	L	L	L	L	L	L	L	L	L	L	8
9	H	L	L	H	L	L	L	L	H	L	L	9
10	H	L	H	L	H	H	H	H	H	H	L	—
11	H	L	H	H	L	H	H	L	L	L	L	E
12	H	H	L	L	H	L	L	H	L	L	L	H
13	H	H	L	H	H	H	H	L	L	L	H	L
14	H	H	H	L	L	L	H	H	L	L	L	P
15	H	H	H	H	H	H	H	H	H	H	H	BLANK

CA3161

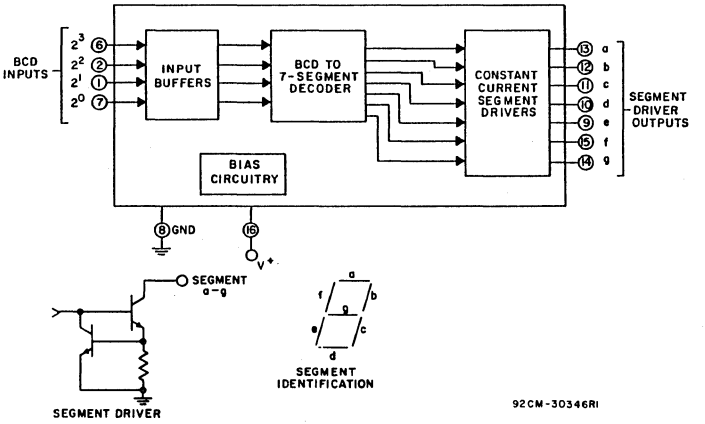
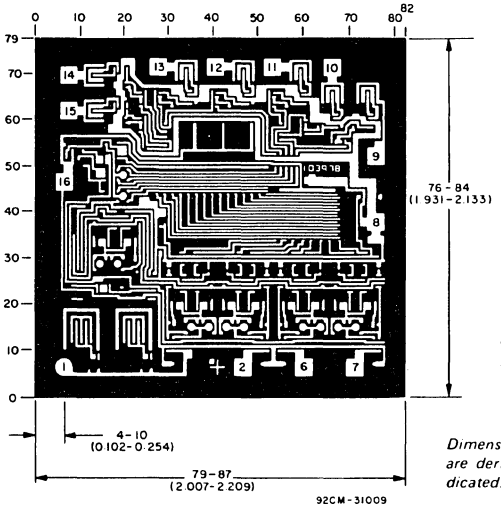


Fig. 1-Functional block diagram of the CA3161E.

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ C$

CHARACTERISTIC		LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Voltage Operating Range, V^+		4.5	5	5.5	V
Supply Current, I^+ (all inputs high)		–	3.5	8	mA
Output Current Low (V_O = 2 V)		18	25	32	mA
Output Current High (V_O = 5.5 V)		–	–	250	μA
Input Voltage High (logic "1" level)		2	–	–	V
Input Voltage Low (logic "0" level)		–	–	0.8	V
Input Current High (logic "1")	2 V	–30	–	–	μA
Input Current Low (logic "0")	0 V	–40	–	–	μA
Propagation Delay Time	t_{PHL}	–	2.6	–	μs
	t_{PLH}	–	1.4	–	



The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for the CA3161H.

ORDERING INFORMATION

Part Number	Temperature Range	Package
CA3161E	0°C to + 70°C	16-Pin Plastic Dip

9

HARRIS SEMICONDUCTOR

CA3168

2-Digit BCD-to-7-Segment Decoder/Driver

For Common-Anode LED Displays

Features

- *Separate BCD inputs and segment outputs for each digit*
- *Input loading less than 15 μA*
- *I^2L logic with buffered inputs and outputs*
- *Internal input overrange protection circuit*
- *5-V supply operation*
- *Internal biasing circuits*
- *Output drive capability of 25 mA per segment*
- *Open collector outputs drive indicators directly*

ORDERING INFORMATION

Part Number	Temperature Range	Package
CA3168	0°C to + 70°C	24-Pin Plastic Dip

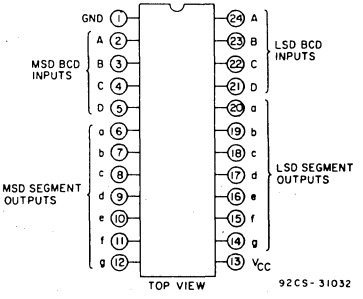
The RCA-CA3168E•is a monolithic integrated circuit intended for 2-digit display such as "numbers" for TV and "CB" channel selection, and other 0-99 numerical or counting for consumer or industrial indicator applications. It consists of two independent BCD-to-7-segment decoder/drivers. Two sets of BCD inputs are buffered with p-n-p differential amplifier stages internally referenced to 1.7 V. Each of the eight input terminals draws less than 15 μA and is provided with an internal protection circuit.

Decoding is accomplished with I^2L ROM's. The fourteen output terminals are buffered with Darlington pairs driving common-emitter output transistors. Each output is capable of sinking 25 mA for an LED common-anode display device. The supply-voltage range (V_{CC}) is intended to be 4.5 V to 6 V. The output voltage (V_O) must not exceed 12 V, which provides for a wide range of common-anode voltage sources.

The CA3168E is supplied in the 24-lead dual-in-line plastic package.

•Formerly RCA Dev. Type No. TA10337

CA3168E
TERMINAL ASSIGNMENT



MAXIMUM RATINGS, *Absolute-Maximum Values:*

SUPPLY-VOLTAGE, V_{CC} ..... 6 V
INPUT-VOLTAGE (MIN./MAX.) ..... $-0.3/V_{CC}$ V
INPUT CURRENT (PROTECTION CIRCUIT) ..... ±10 mA
OUTPUT VOLTAGE, V_O ..... 12 V
OUTPUT SEGMENT CURRENT, $I_{DISPLAY}$ ..... 25 mA
AMBIENT TEMPERATURE RANGE:
  Operating ..... 0 to +70°C
  Storage ..... -55 to +150°C
POWER DISSIPATION:
  Up to +70°C ..... 400 mW
  Above +70°C ..... derate linearly at 8.7 mW/°C
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for
  10 seconds max. ..... +265°C

TYPICAL ELECTRICAL CHARACTERISTICS at V_{CC} = 5 V, V_1 = GND, $V_{DISP.}$ = 12 V, and T_A = 25°C, See Fig. 2
Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		Min.	Typ.	Max.	
Input Voltage High, V_{IH}		2.4	5	V_{CC}	V
Input Voltage Low, V_{IL}		0	–	0.6	V
Input Current High, I_{IH}	All BCD Inputs = 5 V	–	–	15	μA
Input Current Low, I_{IL}	All BCD inputs = 0 V	–10	–	–	μA
On-State Output Voltage, V_{OL}	$I_{O(Sink)}$ = 25 mA	–	–	1	V
Off-State Output Current, I_{OH}		–	5	50	μA
Power Supply Drain Current, I_{CC}	V_{CC} = 6 V	–	17	25	mA
Input Capacitance, C_I		–	5	–	pF

TRUTH TABLES

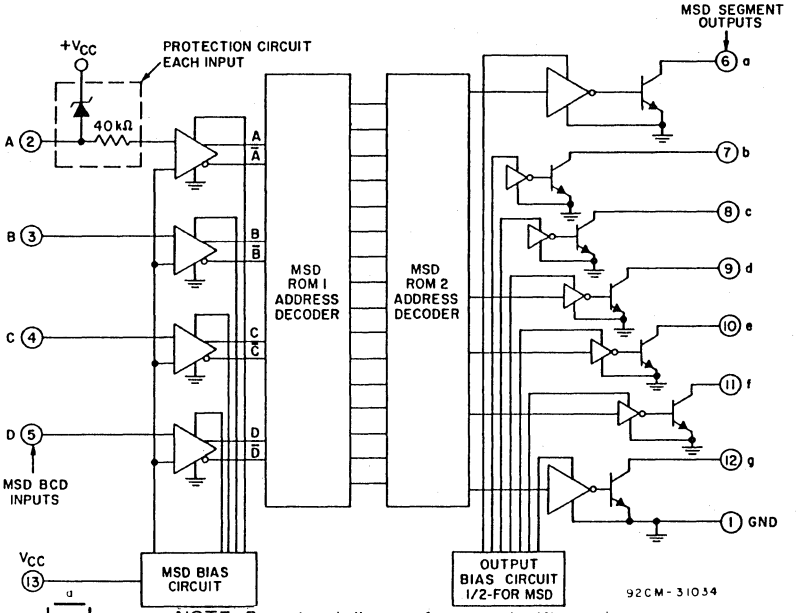
Most Significant Digit (MSD)

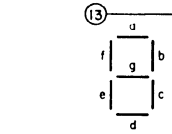
INPUTS				OUTPUTS							DISPLAY
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	2
0	0	1	1	0	0	0	0	1	1	0	3
0	1	0	0	1	0	0	1	1	0	0	4
0	1	0	1	0	1	0	0	1	0	0	5
0	1	1	0	0	1	0	0	0	0	0	6
0	1	1	1	0	0	0	1	1	1	1	7
1	0	0	0	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	0	1	0	0	9
1	0	1	0	0	1	1	0	0	0	1	C
1	0	1	1	0	0	0	1	0	0	0	A
1	1	0	0	0	0	1	1	0	0	0	P
1	1	0	1	0	1	1	0	0	0	0	E
1	1	1	0	1	1	1	1	1	1	0	–
1	1	1	1	1	1	1	1	1	1	1	BLANK

Least Significant Digit (LSD)

INPUTS				OUTPUTS							DISPLAY
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	2
0	0	1	1	0	0	0	0	1	1	0	3
0	1	0	0	1	0	0	1	1	0	0	4
0	1	0	1	0	1	0	0	1	0	0	5
0	1	1	0	0	1	0	0	0	0	0	6
0	1	1	1	0	0	0	1	1	1	1	7
1	0	0	0	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	0	1	0	0	9
1	0	1	0	1	0	0	1	0	0	0	H
1	0	1	1	1	0	0	0	0	1	1	J
1	1	0	0	1	1	1	0	0	0	1	L
1	1	0	1	0	1	1	1	0	0	0	F
1	1	1	0	1	1	1	1	1	1	0	–
1	1	1	1	1	1	1	1	1	1	1	BLANK

CA3168

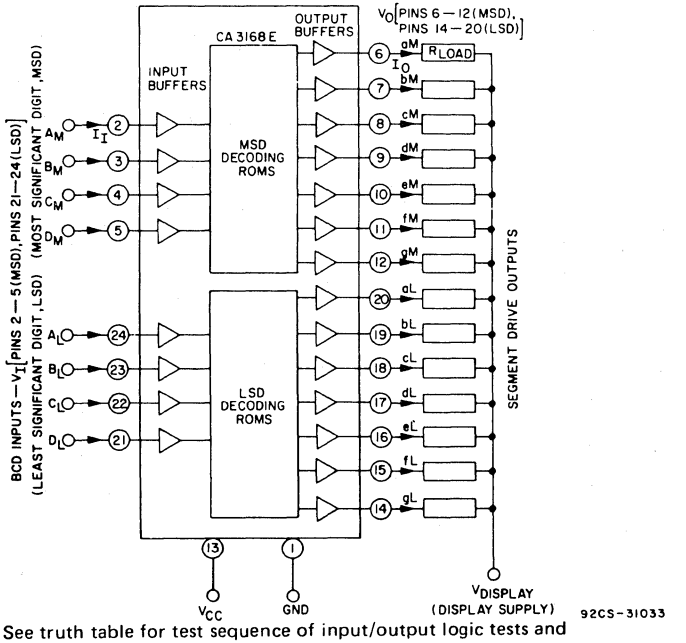




DISPLAY SEGMENT IDENTIFICATION

NOTE: Functional diagram for least significant digit is identical to functional diagram used for MSD with the exception of Terminal Assignments (see Terminal Assignment diagram). A separate LSD Bias circuit, and ½ of the Output Bias Circuit is used for LSD.

Fig. 1 - Functional diagram for Most Significant Digit (MSD).



NOTE: See truth table for test sequence of input/output logic tests and

Minimum $R_{LOAD} = \frac{V_{DISPLAY} - V_{OL}}{\text{Max. } I_{DISPLAY}}$ for each of the 14 segment drive output terminals. (LED is not used in test circuit)

Fig. 2 - Test circuit.

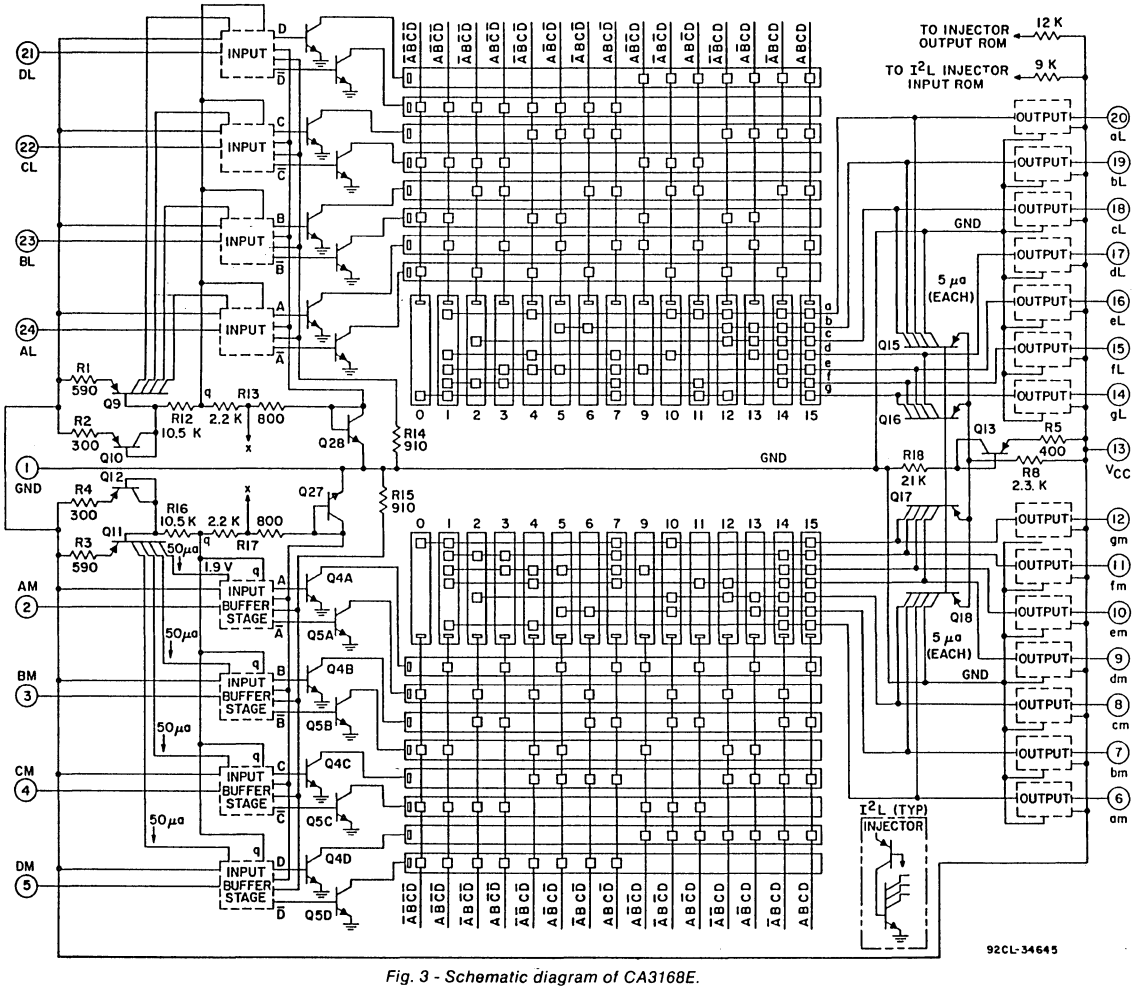


Fig. 3 - Schematic diagram of CA3168E.

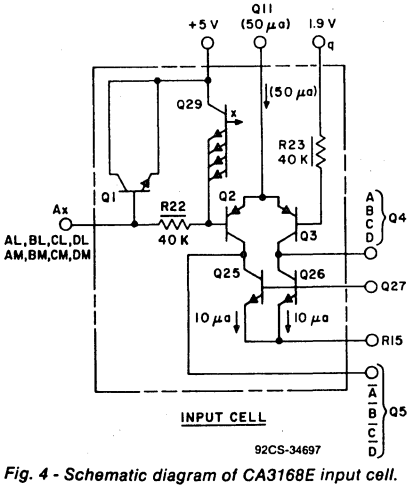


Fig. 4 - Schematic diagram of CA3168E input cell.

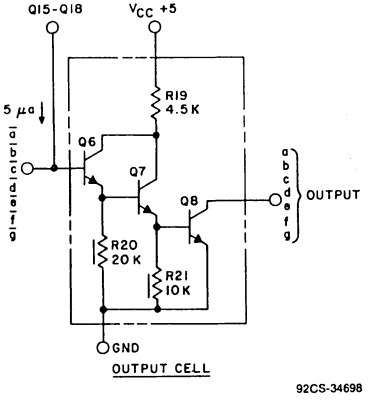


Fig. 5 - Schematic diagram of CA3168E output cell.

HARRIS SEMICONDUCTOR

ICM7211/12
4-Digit LCD/LED Display Driver

GENERAL DESCRIPTION

The ICM7211 (LCD) and ICM7212 (LED) devices constitute a family of non-multiplexed four-digit seven-segment CMOS display decoder-drivers.

The ICM7211 devices are configured to drive conventional LCD displays by providing a complete RC oscillator, divider chain, backplane driver, and 28 segment outputs.

The ICM7212 devices are configured to drive common-anode LED displays, providing 28 current-controlled, low leakage, open-drain n-channel outputs. These devices provide a BRighTness input, which may be used at normal logic levels as a display enable, or with a potentiometer as a continuous display brightness control.

These devices are available with multiplexed or microprocessor input configurations. The multiplexed versions provide four data inputs and four Digit Select inputs. This configuration is suitable for interfacing with multiplexed BCD or binary output devices, such as the ICM7217, ICM7226 and ICL7135. The microprocessor versions provide data input latches and Digit Address latches under control of high-speed Chip Select inputs. These devices simplify the task of implementing a cost-effective alphanumeric seven-segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

The standard devices will provide two different decoder configurations. The basic device will decode the four bit binary inputs into a seven-segment alphanumeric hexadecimal output. The "A" versions will provide the "Code B" output code, i.e., 0-9, dash, E, H, L, P, blank. Either device will correctly decode true BCD to seven-segment decimal outputs.

Devices in the ICM7211/7212 family are packaged in a standard 40 pin plastic dual-in-line and 44 pin plastic surface mount packages and all inputs are fully protected against static discharge.

ICM7211 (LCD) FEATURES

- **Four Digit Non-Multiplexed 7 Segment LCD Display Outputs With Backplane Driver**
- **Complete Onboard RC Oscillator to Generate Backplane Frequency**
- **Backplane Input/Output Allows Simple Synchronization of Slave-Devices to a Master**
- **ICM7211 Devices Provide Separate Digit Select Inputs to Accept Multiplexed BCD Input (Pinout and Functionally Compatible With Siliconix DF411)**
- **ICM7211M Devices Provide Data and Digit Address Latches Controlled by Chip Select Inputs to Provide a Direct High Speed Processor Interface**
- **ICM7211 Decodes Binary to Hexadecimal; ICM7211A Decodes Binary to Code B (0–9, Dash, E, H, L, P, Blank)**
- **ICM7211A Available in Surface Mount Package**

ICM7212AM (LED) FEATURES

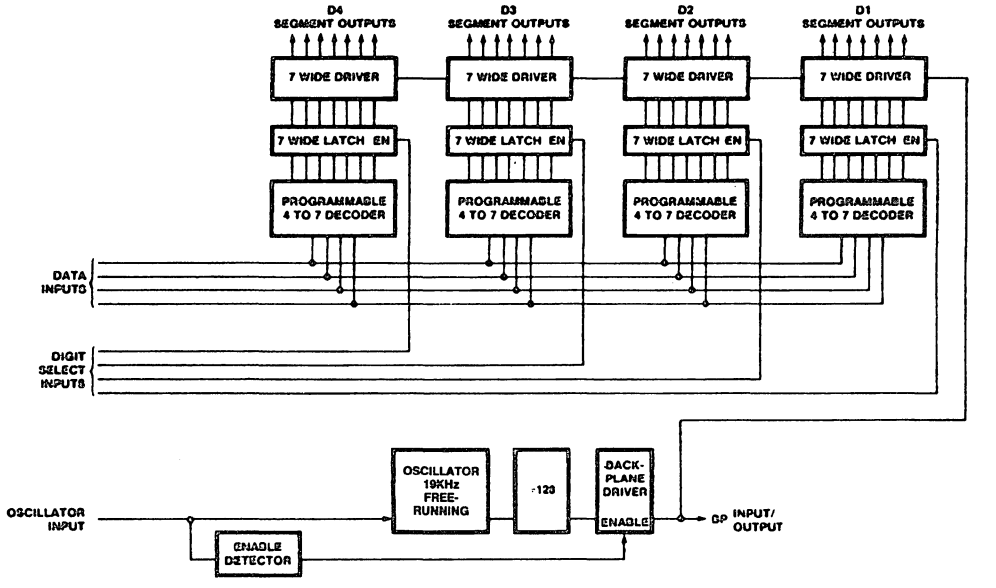
- **28 Current-Limited Segment Outputs Provide 4-Digit Non-Multiplexed Direct LED Drive at > 5mA Per Segment**
- **Brightness Input Allows Direct Control of LED Segment Current With a Single Potentiometer or Digitally as a Display Enable**
- **ICM7212AM Device Provides Same Input Configuration and Output Decoding Options as the ICM7211AM**

ORDERING INFORMATION

Part Number	Temperature Range	Package	Display Type	Display Decoding	Input Interfacing	Display Drive Type
ICM7211IPL	−40°C to +85°C	40-Pin Plastic DIP	LCD	Hexadecimal	Multiplexed	Direct Drive
ICM7211MIPL	−40°C to +85°C	40-Pin Plastic DIP	LCD	Hexadecimal	Microprocessor	Direct Drive
ICM7211AIPL	−40°C to +85°C	40-Pin Plastic DIP	LCD	Code B	Multiplexed	Direct Drive
ICM7211AMIPL	−40°C to +85°C	40-Pin Plastic DIP	LCD	Code B	Microprocessor	Direct Drive
ICM7211AIM44	−40°C to +85°C	44-Pin P. Flatpack	LCD	Code B	Multiplexed	Direct Drive
ICM7211AMIM44	−40°C to +85°C	44-Pin P. Flatpack	LCD	Code B	Microprocessor	Direct Drive
ICM7212AMIPL	−40°C to +85°C	40-Pin Plastic DIP	LED	Code B	Microprocessor	Common Anode

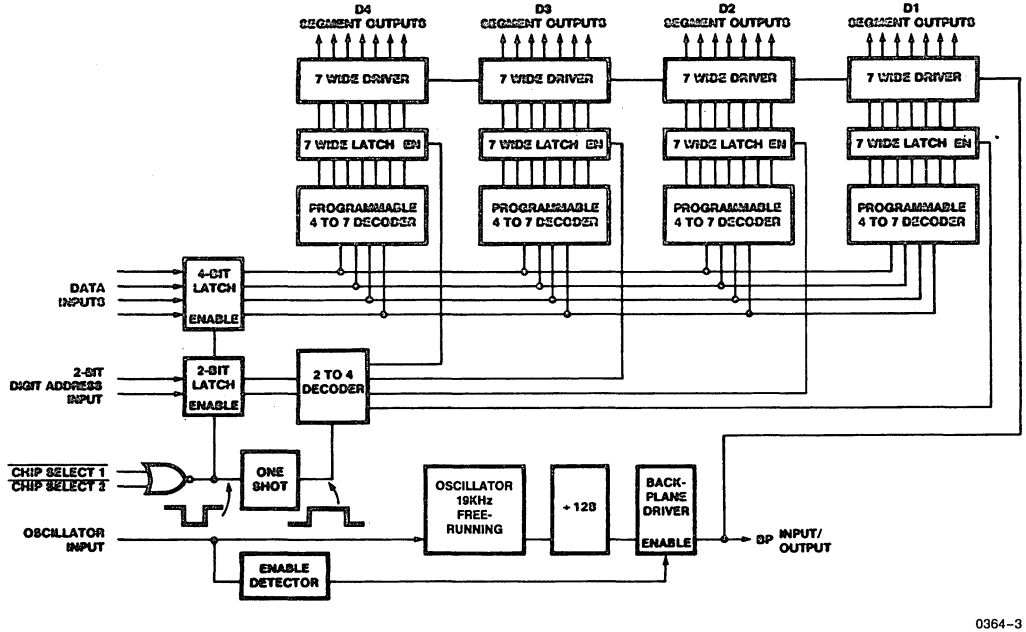
NOTE: All typical values have been characterized but are not tested.

ICM7211 (A)



0364-1

ICM7211(A)M



0364-3

Figure 1: Functional Diagrams

NOTE: All typical values have been characterized but are not tested.

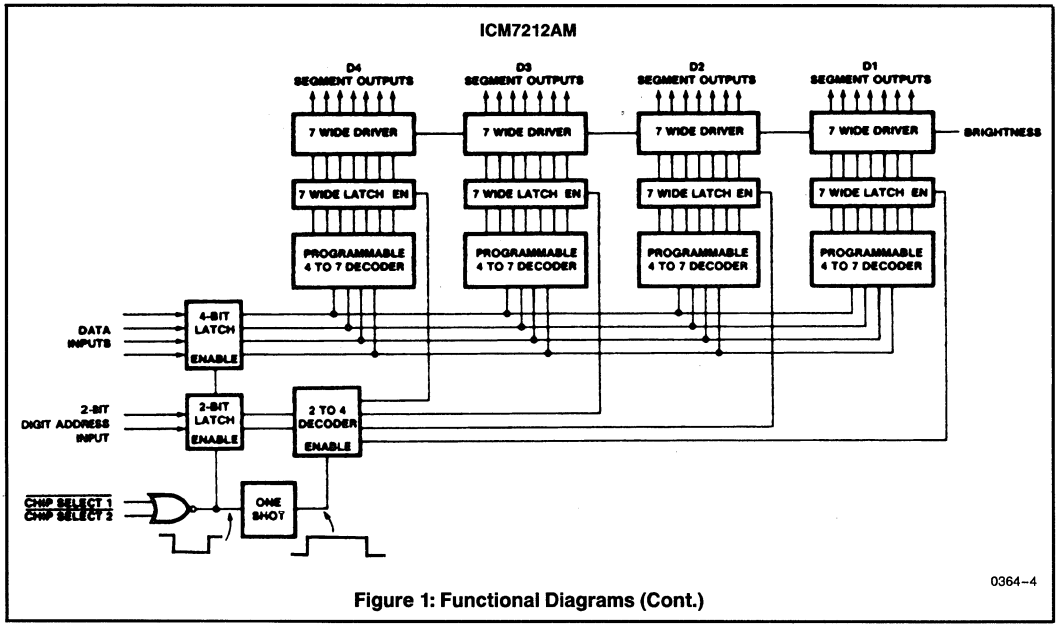
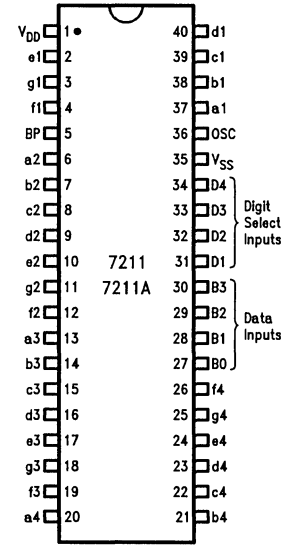
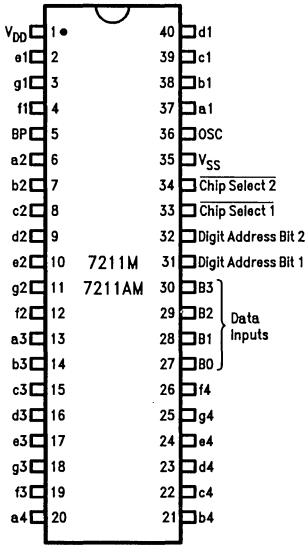


Figure 1: Functional Diagrams (Cont.)

NOTE: All typical values have been characterized but are not tested.



0364-5



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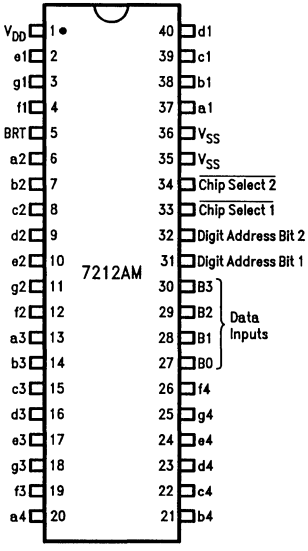

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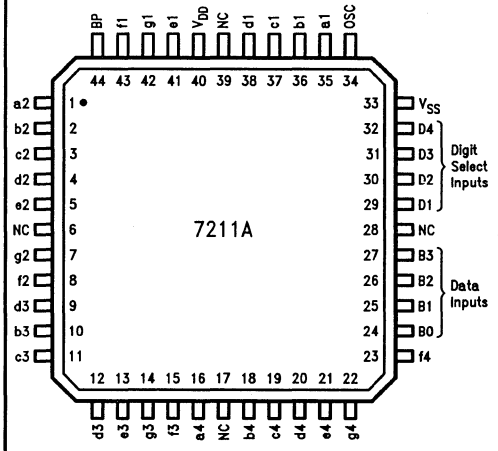
DIP Packages Outline (PL)



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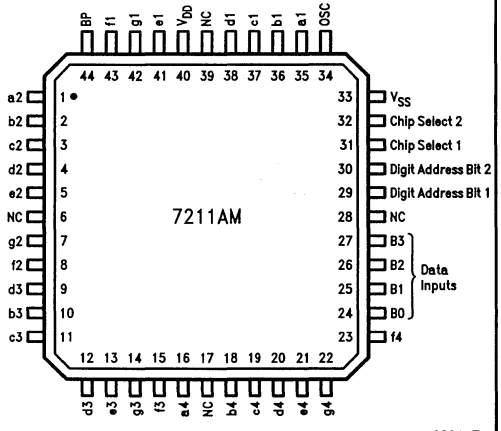


0364-7

Surface Mount Packages (M44)

Figure 2: Pin Configurations (Outline Drawing PL)

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5W@70°C
Supply Voltage ($V_{DD}-V_{SS}$) 6.5V
Input Voltage (Any Terminal) (Note 2)
..... V_{SS} −0.3V to V_{DD}+0.3V

Operating Temperature Range ..... −40°C to +85°C
Storage Temperature Range ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE 1: This limit refers to that of the package and will not be realized during normal operation.

NOTE 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7211/ICM7212 be turned on first.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

ICM7211 CHARACTERISTICS (LCD) $V_{DD}=5V \pm 10\%$, $T_A=25°C$, $V_{SS}=0V$ unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SUPPLY}	Operating Supply Voltage Range ($V_{DD}-V_{SS}$)		3	5	6	V
I_{DD}	Operating Current	Test circuit, Display blank		10	50	µA
I_{OSCI}	Oscillator Input Current	Pin 36		±2	±10	
t_R, t_F	Segment Rise/Fall Time	$C_L=200pF$		0.5		µs
t_R, t_F	Backplane Rise/Fall Time	$C_L=5000pF$		1.5		
f_{OSC}	Oscillator Frequency	Pin 36 Floating		19		kHz
f_{BP}	Backplane Frequency	Pin 36 Floating		150		Hz

ICM7212 CHARACTERISTICS (COMMON ANODE LED)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SUPPLY}	Operating Supply Voltage Range ($V_{DD}-V_{SS}$)		4	5	6	V
I_{STBY}	Operating Current Display Off	Pin 5 (Brightness), Pins 27–34=V_{SS}		10	50	µA
I_{DD}	Operating Current	Pin 5 at V_{DD}, Display all 8's		200		mA
I_{SLK}	Segment Leakage Current	Segment Off		±0.01	±1	µA
I_{SEG}	Segment On Current	Segment On, $V_O=+3V$	5	8		mA

NOTE: All typical values have been characterized but are not tested.

INPUT CHARACTERISTICS (ICM7211 AND ICM7212)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{IH}	Logical "1" input voltage		4			V
V_{IL}	Logical "0" input voltage				1	
I_{ILK}	Input leakage current	Pins 27–34		±.01	±1	μA
C_{IN}	Input capacitance	Pins 27–34		5		pF
I_{BPLK}	BP/Brightness input leakage	Measured at Pin 5 with Pin 36 at V_{SS}		±.01	±1	μA
C_{BPI}	BP/Brightness input capacitance	All Devices		200		pF
AC CHARACTERISTICS — MULTIPLEXED INPUT CONFIGURATION						
t_{WH}	Digit Select Active Pulse Width	Refer to Timing Diagrams	1			μs
t_{DS}	Data Setup Time		500			ns
t_{DH}	Data Hold Time		200			
t_{IDS}	Inter-Digit Select Time		2			μs
AC CHARACTERISTICS — MICROPROCESSOR INTERFACE						
t_{WL}	Chip Select Active Pulse Width	other Chip Select either held active, or both driven together	200			ns
t_{DS}	Data Setup Time		100			
t_{DH}	Data Hold Time		10	0		
t_{ICS}	Inter-Chip Select Time		2			μs

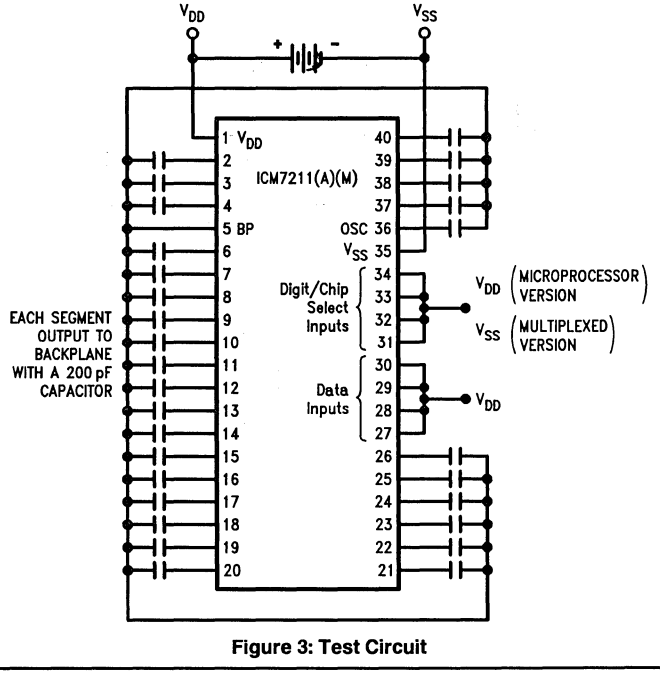
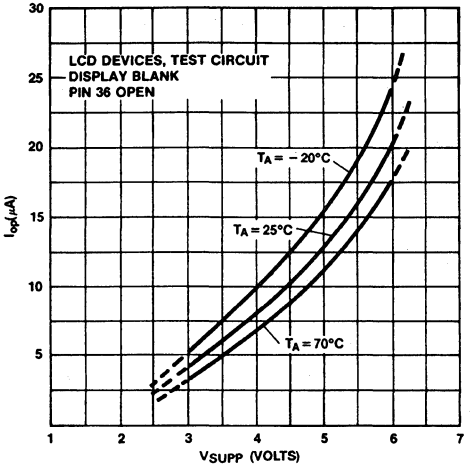


Figure 3: Test Circuit

NOTE: All typical values have been characterized but are not tested.

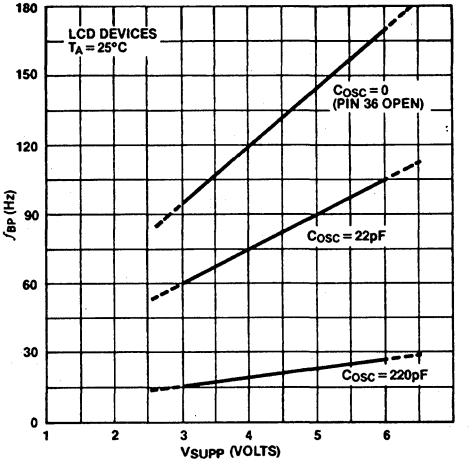
TYPICAL PERFORMANCE CHARACTERISTICS

ICM7211 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



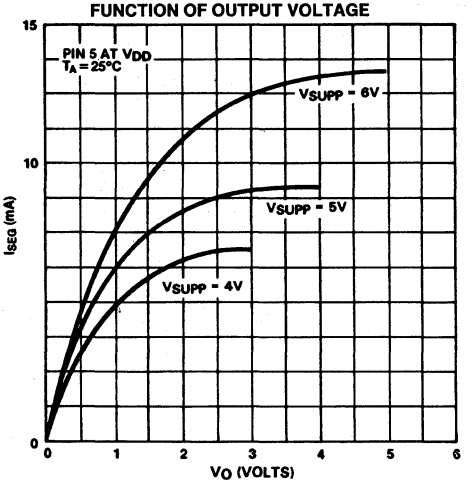
0364-10

ICM7211 BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



0364-11

ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

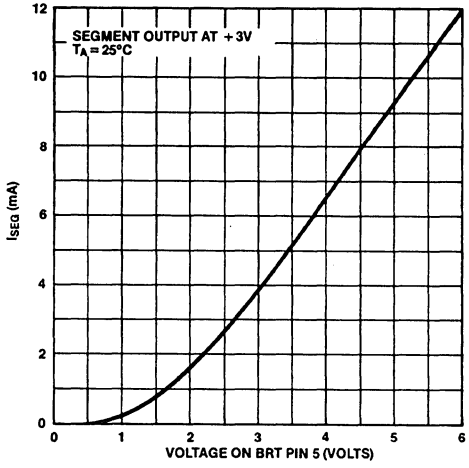


0364-12

NOTE: All typical values have been characterized but are not tested.

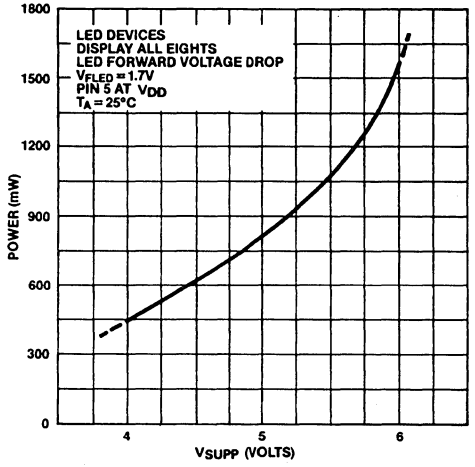
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE



0364-13

ICM7212 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE



0364-14

INPUT DEFINITIONS

In this table, V_{DD} and V_{SS} are considered to be normal operating input logic levels. Actual input low and high levels are specified under Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

Input	Terminal	Conditions	Function	
B0	27	V_{DD} = Logical One V_{SS} = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V_{DD} = Logical One V_{SS} = Logical Zero	Twos	
B2	29	V_{DD} = Logical One V_{SS} = Logical Zero	Fours	
B3	30	V_{DD} = Logical One V_{SS} = Logical Zero	Eights (Most significant)	
OSC (LCD Devices Only)	36	Floating or with external capacitor to V_{DD} V_{SS}	Oscillator input Disables BP output devices, allowing segments to be synchronized to an external signal input at the BP terminal (Pin 5)	

9

NOTE: All typical values have been characterized but are not tested.

ICM7211 MULTIPLEXED-BINARY INPUT CONFIGURATION

Input	Terminal	Conditions	Function
D1	31	V_{DD} = Active V_{SS} = Inactive	D1 Digit Select (Least significant)
D2	32		D2 Digit Select
D3	33		D3 Digit Select
D4	34		D4 Digit Select (Most significant)

ICM7211M/ICM7212M MICROPROCESSOR INTERFACE INPUT CONFIGURATION

Input	Description	Terminal	Conditions	Function
DA1	Digit Address Bit 1 (LSB)	31	V_{DD} = Logical One V_{SS} = Logical Zero	DA1 & DA2 serve as a two bit Digit Address Input DA2, DA1 = 00 selects D4 DA2, DA1 = 01 selects D3 DA2, DA1 = 10 selects D2 DA2, DA1 = 11 selects D1
DA2	Digit Address Bit 2 (MSB)	32		
$\overline{CS1}$	Chip Select 1	33	V_{DD} = Inactive V_{SS} = Active	When **both** $\overline{CS1}$ and $\overline{CS2}$ are taken low, the data at the Data and Digit Select code inputs are written into the input latches. On the rising edge of **either** $\overline{Chip\ Select}$, the data is decoded and written into the output latches.
$\overline{CS2}$	Chip Select 2	34		

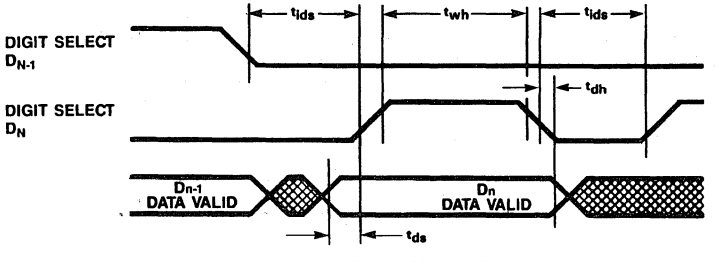


Figure 4: Multiplexed Input Timing Diagram

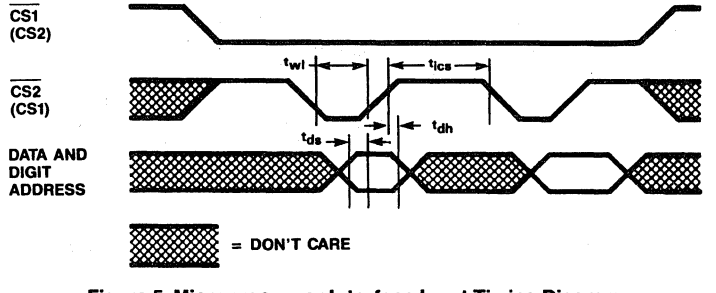


Figure 5: Microprocessor Interface Input Timing Diagram

NOTE: All typical values have been characterized but are not tested.

DESCRIPTION OF OPERATION

LCD DEVICES

The LCD devices in the family (ICM7211, 7211A, 7211M, 7211AM) provide outputs suitable for driving conventional four-digit, seven-segment LCD displays. These devices include 28 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any DC component, which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the OSCillator input (pin 36) to V_{SS}. This allows the 28 segment outputs to be synchronized directly to a signal input at the BP terminal (pin 5). In this manner, several slave devices may be cascaded to the backplane output of one master device, or the backplane may be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device represents a load of approximately 200pF (comparable to one additional segment). Thus the limitation of the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits. A good rule of thumb to observe in order to minimize power consumption is to keep the backplane rise and fall times less than about 5 microseconds. The backplane output driver should handle the backplane to a display of 16 one-half-inch characters. It is recommended, if more than four devices are to be slaved together, the backplane signal be derived externally and all the ICM7211 devices be slaved to it. This external signal should be capable of driving very large capacitive loads with short (1-2μs) rise and fall times. The maximum frequency for a backplane signal should be about 150Hz although this may be too fast for optimum display response at lower display temperatures, depending on the display type.

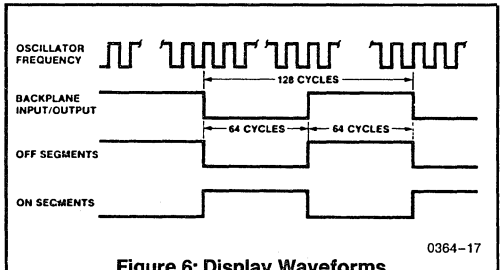


Figure 6: Display Waveforms

The onboard oscillator is designed to free run at approximately 19kHz at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 150Hz with the oscillator free-running; the oscillator frequency may be reduced by connecting an external capacitor between the OSCillator terminal and V_{DD}.

The oscillator may also be overdriven if desired, although care must be taken to ensure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a D.C. component to the display). This can be done by driving the OSCillator input between the positive supply and a level out of the range where the backplane disable is sensed (about one fifth of the supply voltage above V_{SS}). Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

LED DEVICES

The LED device in the family (7212AM) provides outputs suitable for directly driving four-digit, seven-segment common-anode LED displays. These devices include 28 individual segment drivers, each consisting of a low-leakage, current-controlled, open-drain, n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the BRighTness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Figure 7. The potentiometer should be a high value (100KΩ to 1MΩ) to minimize power consumption, which can be significant when the display is off.

The BRighTness input may also be operated digitally as a display enable; when high, the display is fully on, and low fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two voltages at the BRighTness input.

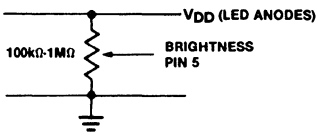
Note that the LED device has two connections for V_{SS}; both of these pins should be connected. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (−15mW/°C above 35°C). Power dissipation for the device is given by:

$$P = (V_{SUPP} - V_{FLED})(I_{SEG})(n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "on" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the BRighTness input to keep power dissipation within the limits described above.

NOTE: All typical values have been characterized but are not tested.



0364-18

Figure 7: Brightness control

INPUT CONFIGURATIONS AND OUTPUT CODES

The standard devices in the ICM7211/12 family accept a four-bit true binary (ie, positive level=logical one) input at pins 27 thru 30, least significant bit at pin 27 ascending to the most significant bit at pin 30. The ICM7211 and ICM7211M devices decode this binary input into a seven-segment alphanumeric hexadecimal output, while the ICM7211A, ICM7211AM, and ICM7212AM decode the binary input into seven-segment alphanumeric "Code B" output, i.e. 0-9, dash, E. H, L, P, blank. These codes are shown explicitly in Table 1. Either decoder option will correctly decode true BCD to a seven-segment decimal output.

TABLE 1: Output Codes

BINARY				HEXADECIMAL ICM7211 ICM7211M	CODE B ICM7211A ICM7212AM
B3	B2	B1	B0		
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(BLANK)

0364-19

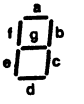
These devices are actually mask-programmable to provide any 16 combinations of the seven segment outputs decoded from the four input bits. For large quantity orders custom decoder options can be arranged. Contact the factory for details.

The ICM7211 and ICM7211A devices are designed to accept multiplexed binary or BCD input. These devices provide four separate digit lines (least significant digit at pin 31 ascending to most significant digit at pin 34), each of which when taken to a positive level decodes and stores in the output latches of its respective digit the character corresponding to the data at the input port, pins 27 through 30.

The ICM7211M, ICM7211AM, and ICM7212AM devices are intended to accept data from a data bus under processor control.

In these devices, the four data input bits and the two-bit digit address (DA1 pin 31, DA2 pin 32) are written into input buffer latches when both chip select inputs ($\overline{CS1}$ pin 33, $\overline{CS2}$ pin 34) are taken low. On the rising edge of either chip select input, the content of the data input latches is decoded and stored in the output latches of the digit selected by the contents of the digit address latches.

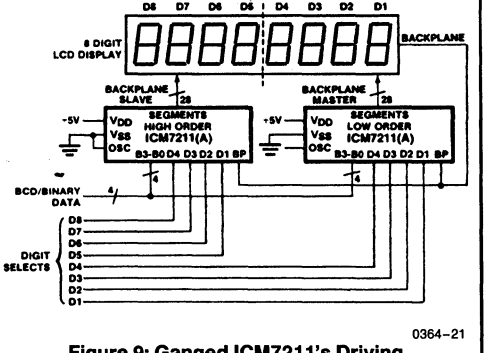
An address of 00 writes into D4, DA2=0, DA1=1 writes into D3, DA2=1, DA1=0 writes into D2, and 11 writes into D1. The timing relationships for inputting data are shown in Figure 5, and the chip select pulse widths and data setup and hold times are specified under Operating Characteristics.



0364-20

Figure 8: Segment Assignment

APPLICATIONS



0364-21

Figure 9: Ganged ICM7211's Driving 8-Digit LCD Display

NOTE: All typical values have been characterized but are not tested.

ICM7211/12

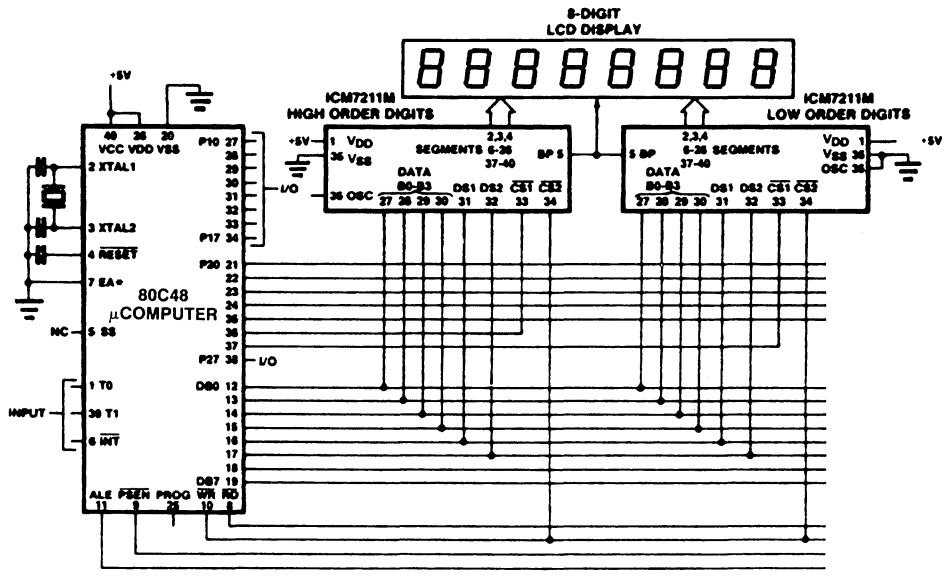


Figure 10: 80C48 Microprocessor Interface

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICM7218
8-Digit LED μP Compatible Multiplexed Display Decoder Driver

GENERAL DESCRIPTION

The ICM7218 series of universal LED driver systems provide, in a single package, all the circuitry necessary to interface most common microprocessors or digital systems to an LED display. Included on chip are an 8-byte static display memory, 2 types of 7-segment decoders, multiplex scan circuitry, and high current digit and segment drivers for either common-cathode or common-anode displays.

The ICM7218A and ICM7218B feature 2 control lines ($\overline{WRITE}$ and MODE) which write either 4 bits of control information (DATA COMING, $\overline{SHUTDOWN}$,$\overline{DECODE}$, and HEXA/$\overline{CODE\ B}$) or 8 bits of display input data. Display data is automatically sequenced into the 8-byte internal memory on successive positive going $\overline{WRITE}$ pulses. Data may be displayed either directly or decoded in Hexadecimal or Code B formats.

The ICM7218C and ICM7218D feature 2 control lines ($\overline{WRITE}$ and HEXA/CODE B/$\overline{SHUTDOWN}$), 4 separate display data input lines, and 3 digit address lines. Display data is written into the internal memory by setting up a digit address and strobing the $\overline{WRITE}$ line low. Only Hexadecimal and Code B formats are available for display outputs.

FEATURES

- **Microprocessor Compatible**
- **Total Circuit Integration On Chip Includes:**
  - **a) Digit and Segment Drivers**
  - **b) All Multiplex Scan Circuitry**
  - **c) 8 Byte Static Display Memory**
  - **d) 7 Segment Hexadecimal and Code B Decoders**
- **Output Drive Suitable for LED Displays Directly**
- **Common Anode and Common Cathode Versions**
- **Single 5 Volt Supply Required**
- **Data Retention to 2 Volts Supply**
- **Shutdown Feature — Turns Off Display and Puts Chip Into Low Power Dissipation Mode**
- **Sequential and Random Access Versions**
- **Decimal Point Drive On Each Digit**

ORDERING INFORMATION

Part Number	Temperature Range	Package	Display Type
ICM7218AIJI	−40°C to +85°C	28-PIN CERDIP	Common Anode
ICM7218BIJI	−40°C to +85°C	28-PIN CERDIP	Common Cathode
ICM7218CIJI	−40°C to +85°C	28-PIN CERDIP	Common Anode
ICM7218DIJI	−40°C to +85°C	28-PIN CERDIP	Common Cathode

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) 6V
Digit Output Current 300mA
Segment Output Current 50mA
Input Voltage
(any terminal) ..... V_{SS} −0.3V to V_{DD} + 0.3V
(Note 1)

Power Dissipation (28 Pin CERDIP) ..... 1 W (Note 2)
Operating Temperature Range ..... −40°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason it is recommended that no inputs from sources operating on a different power supply be applied to the device before its own supply is established, and when using multiple supply systems the supply to the ICM7218 should be turned on first.
2: These limits refer to the package and will not be obtained during normal operation. Derate above 50°C by 25mW per °C.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

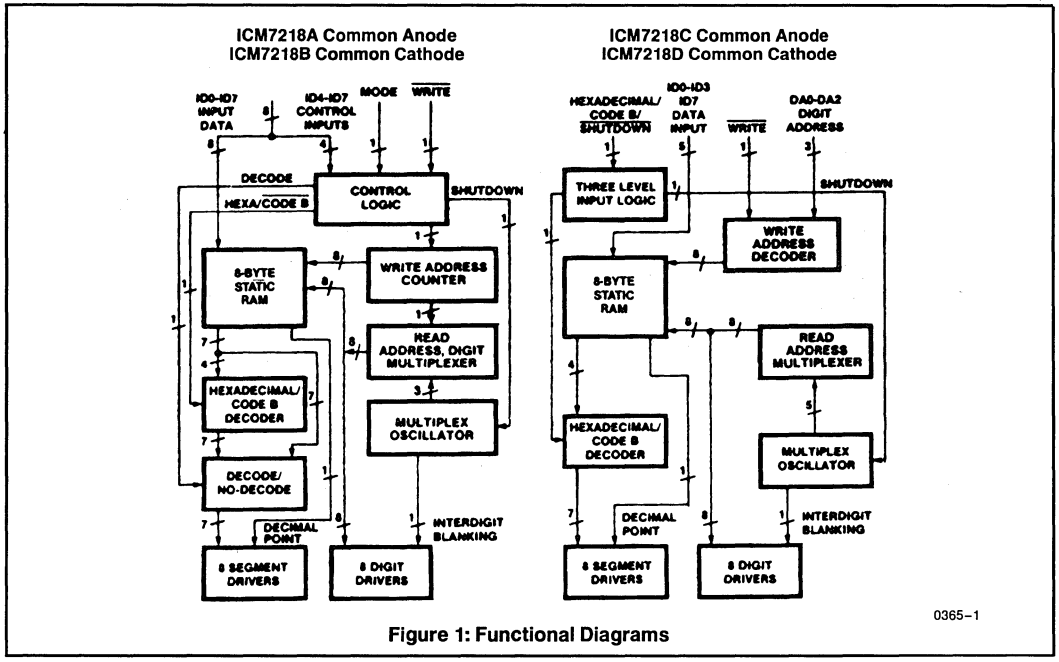
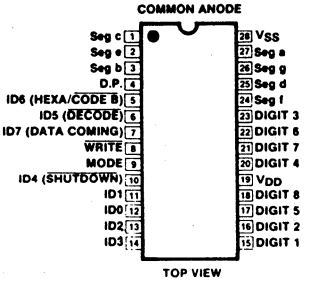


Figure 1: Functional Diagrams

NOTE: All typical values have been characterized but are not tested.

ICM7218A
(OUTLINE DWG JI)



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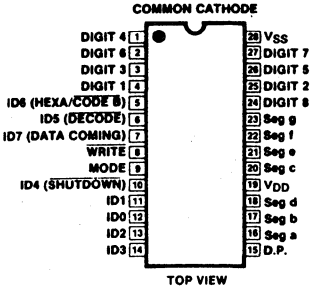
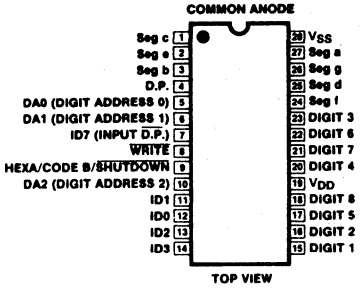
ICM7218B
(OUTLINE DRAWING JI)



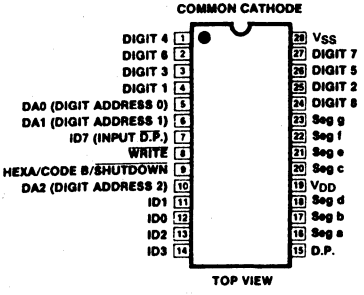
0365-3

ICM7218C
(OUTLINE DRAWING JI)



0365-4

ICM7218D
(OUTLINE DRAWING JI)



0365-5

Figure 2: Pin Configurations

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

$V_{DD}=5V$, $V_{SS}=0V$, $T_A=25°C$, Display Diode drop = 1.7V

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{SUPPLY}	Supply Voltage Range	Operating	4		6	V
		Power Down Mode	2		6	V
I_Q	Quiescent Supply Current	Shutdown (Note 3)	6	10	300	µA
I_{DD}	Operating Supply Current	Common Anode SEGS On (Outputs Open Circuit)			2.5	mA
		SEGS Off (Outputs Open Circuit)			500	µA
		Common Cathode SEGS On (Outputs Open Circuit)			700	µA
		SEGS Off (Outputs Open Circuit)			500	µA
		Note 4				
I_{DIG}	Digit Drive Current	Common Anode $V_{out}=V_{DD}-2.0V$	140	200		mA
		Common Cathode $V_{out}=V_{SS}+1.0V$	50	100		mA
I_{DLK}	Digit Leakage Current	Shutdown Mode				
		Common Anode $V_{out}=2V$			100	µA
		Common Cathode $V_{out}=5V$			100	µA
I_{SEG}	Peak Segment Drive Current	Common Anode $V_{out}=V_{SS}+1.0V$	20	40		mA
		Common Cathode $V_{out}=V_{DD}-2.0V$	−10	−20		mA
I_{SLK}	Segment Leakage Current	Shutdown Mode				
		Common Anode $V_{out}=V_{DD}$			100	µA
		Common Cathode $V_{out}=V_{SS}$			100	µA
f_{MUX}	Display Scan Rate	Per Digit		250		Hz
	Three Level Input: Pin 9 ICM7218C/D					
V_{IH}	Logical "1" Input Voltage	Hexadecimal	4.5			V
V_{IF}	Floating Input	Code B	2.0		3.0	V
V_{IL}	Logical "0" Input Voltage	Shutdown			0.4	V
Z_{IN}	Three Level Input Impedance	Note 3		100		kΩ
V_{IH}	Logical "1" Input Voltage		3.5			V
V_{IL}	Logical "0" Input Voltage				0.8	V
t_{WL}	Write Pulse Width (Low)	7218A, B	550	400		ns
t_{WL}	Write Pulse Width (Low)	7218C, D	400	250		ns
t_{MH}	Mode Hold Time	7218A, B	150			ns
t_{MS}	Mode Set Up Time	7218A, B	500			ns
t_{DS}	Data Set Up Time		500			ns
t_{DH}	Data Hold Time	7218 A, B	50			ns
		7218 C, D	125			ns
t_{AS}	Digit Address Set Up Time	ICM7218C, D	500			ns
t_{AH}	Digital Address Hold Time	ICM7218C, D	0			ns
Z_{IN}	Data Input Impedance	5-10 pF Gate Capacitance		10^{10}		Ohms

NOTE: All typical values have been characterized but are not tested.

TABLE 1: INPUT DEFINITIONS ICM7218A and B

Input		Terminal	Logic Level	Function
$\overline{\text{WRITE}}$		8	High Low	Input Not Loaded Input Loaded
MODE		9	High Low	Load Control bits on Write Pulse Load Input Data on Write Pulse
ID4 $\overline{\text{SHUTDOWN}}$	MODE High	10	High Low	Normal Operation Shutdown (Oscillator, Decoder and Display Disabled)
ID5 ($\overline{\text{DECODE}}$)	MODE High	6	High Low	No Decode Decode
ID6 (HEXA/$\overline{\text{CODE B}}$)	MODE High	5	High Low	Hexadecimal Decoding Code B Decoding
ID7 (DATA COMING)	MODE High	7	High Low	Data Coming No Data Coming } Control Word
ID0-ID7	MODE Low	11,12,13,14, 5,6,10,7		Display Data Inputs (Notes 4, 5)

TABLE 2: INPUT DEFINITIONS ICM7218C and D

Input	Terminal	Logic Level	Function
$\overline{\text{WRITE}}$	8	High Low	Input Not Loaded Into Memory Input Loaded Into Memory
HEXA/CODE B/$\overline{\text{SHUTDOWN}}$	9 (Note 3)	High Floating Low	Hexadecimal Decoding Code B Decoding Shutdown (Oscillator, Decoder and Display Disabled)
DA0 – DA2	10,6,5		Digit Address Inputs
ID0 – ID3 ID (INPUT $\overline{\text{D.P.}}$)	14,13,11,12 7		Display Data Inputs Decimal Point Input

NOTE 3: In the ICM7218C and D (random access versions) the HEXA/CODE B/$\overline{\text{SHUTDOWN}}$ Input (Pin 9) has internal biasing resistors to hold it at $V_{DD}/2$ when Pin 9 is open circuited. These resistors consume power and result in a quiescent supply current (I_Q) of typically 50μA.
The ICM7218A, B, and E devices do not have these biasing resistors and thus are not subject to this condition.

4: ID0-ID3 = Don't care when writing control data
ID4-ID6 = Don't care when writing Hex/Code B data
ID7 = Decimal Point data
(The display blanks on ICM7218A/B versions when writing in data)

5: In the No Decode format, "Ones" represents "on" segments for all inputs except for the Decimal Point, where "Zero" represents an "on" segment, (i.e. segments are positive true, decimal point is negative true).

6: Common Anode segment drivers and Common Cathode Digit Drivers have 20kΩ pullup resistors.

NOTE: All typical values have been characterized but are not tested.

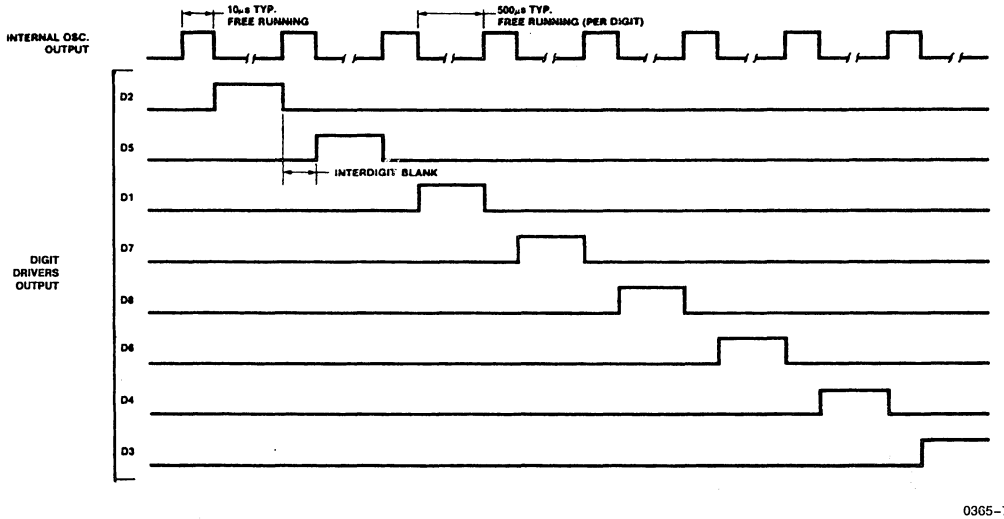


Figure 3: Multiplex Timing (Common Cathode Version)

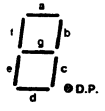


Figure 4: Segment Assignments

DETAILED DESCRIPTION

$\overline{\text{DECODE}}$ Operation

For the ICM7218A/B products, there are 3 input data formats possible; either direct segment and decimal point information (8 bits per digit) or two Binary code plus decimal point information (Hexadecimal/Code B formats with 5 bits per digit).

9

NOTE: All typical values have been characterized but are not tested.

The 7 segment decoder on chip is disabled when direct segment information is to be written. In this format, the inputs directly control the outputs as follows:

Input Data: ID7 ID6 ID5 ID4 ID3 ID2 ID1 ID0

Output Segments: $\overline{D.P.}$ a b c e g f d

Here, "Ones" represent "on" segments for all inputs except the Decimal Point. For the Decimal Point "zero" represents an "on" segment.

HEXAdecimal/CODE B Decoding

For all products, a choice of either HEXA or Code B decoding may be made, HEXA decoding provides 7 segment numeric plus six alpha characters while Code B provides a negative sign (−), a blank (for leading zero blanking), certain useful alpha characters and all numeric formats.

The four bit binary code is set up on inputs ID3-ID0, and decimal point data is set up on ID7.

Decimal	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
HEXA CODE	0 1 2 3 4 5 6 7 8 9 A b C d E F
CODE B	0 1 2 3 4 5 6 7 8 9 - E H L P (BLANK)

$\overline{\text{SHUTDOWN}}$

$\overline{\text{SHUTDOWN}}$ performs several functions: it puts the device into a very low dissipation mode (typically 10μA at $V_{DD}=5V$), turns off both the digit and segment drivers, and stops the multiplex scan oscillator (this is the only way the scan oscillator can be disabled). However, it is still possible to input data to the memory during shutdown — only the display output sections of the device are disabled in this mode.

Powerdown

In the Shutdown Mode, the supply voltage may be reduced to 2 volts without data in memory being lost. However, data should not be written into memory if the supply voltage is less than 4 volts.

Output Drive

The common anode output drive is approximately 200 mA per digit at a 12% duty cycle. With segment peak drive current of 40mA typically, this results in 5mA average drive. The common cathode drive capability is approximately one half that of the common anode drive. If high impedance LED displays are used, the drive current will be correspondingly less.

Inter Digit Blanking

A blanking time of approximately 10μs occurs between digit strobes. This ensures that the segment information is correct before the next digit drive, thereby avoiding display ghosting.

Driving Larger Displays

If a higher average drive current per digit is required, it is possible to connect digit drive outputs together. For example, by paralleling pairs of digit drives together to drive a 4 digit display, 5mA average segment drive current can be obtained.

Power Dissipation Considerations

Assuming common anode drive at $V_{DD}=5$ volts and all digits on with an average of 5 segments driven per digit, the average current would be approximately 200mA. Assuming a 1.8 volt drop across the LED display, there will be a 3.2 volt drop across the ICM7218. The device power dissipation will therefore be 640mW, rising to about 900mW, for all '8' 's displayed. **Caution: Position device in system such that air can flow freely to provide maximum cooling. The common cathode dissipation is approximately one half that of the common anode dissipation.**

Sequential Addressing Considerations (ICM7218A/B)

The control instructions are read from the input bus lines if MODE is high and $\overline{\text{WRITE}}$ low. The instructions occur on 4 lines and are — $\overline{\text{DECODE}}$/no Decode, type of Decode (if desired), $\overline{\text{SHUTDOWN}}$/no Shutdown and DATA COMING/not Coming. After the control word has been written (with the Data Coming instruction), display data can be written into memory with each successive negative going $\overline{\text{WRITE}}$ pulse. After all 8 digit memory locations have been written to, additional transitions of the $\overline{\text{WRITE}}$ input are ignored until a new control word is written. It is not possible to change one individual digit without refreshing the data for all the other digits.

Random Access Input Drive Considerations (ICM7218C/D)

Control instructions are provided to the ICM7218C/D by a single three level input terminal (Pin 9), which operates independently of the $\overline{\text{WRITE}}$ pulse.

Data can be written into memory on the ICM7218C/D by setting up a 3 bit binary code (one of eight) on the digit address inputs and applying a low level to the $\overline{\text{WRITE}}$ pin. For example, it is possible to change only digit 7 without altering the data for the other digits. (See Figure 7).

Supply Capacitor

A 0.1μF plus a 47μF capacitor is recommended between V_{DD} and V_{SS} to bypass display multiplexed noise.

NOTE: All typical values have been characterized but are not tested.

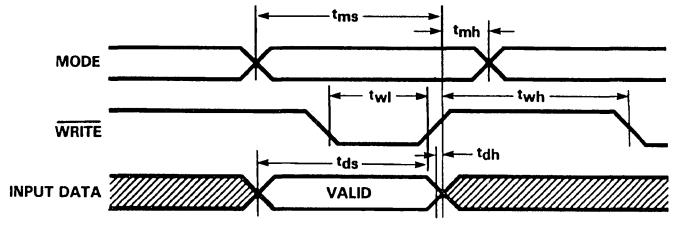


Figure 5: Timing Diagram for ICM7218A/B

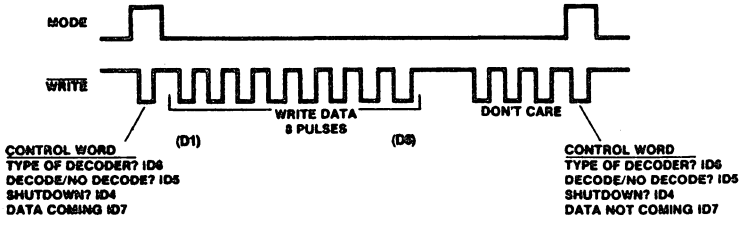


Figure 6: Load Sequence ICM7218A/B

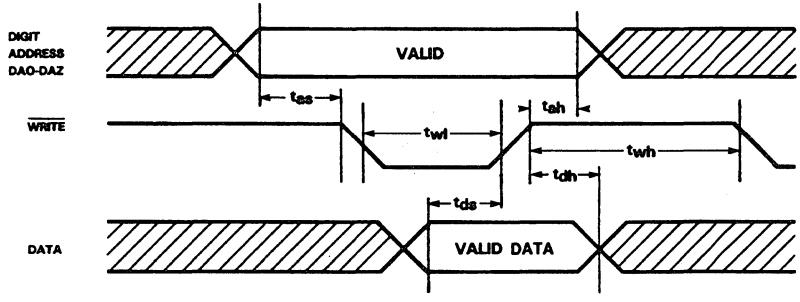


Figure 7: Timing Diagram for ICM7218C/D

NOTE: All typical values have been characterized but are not tested.

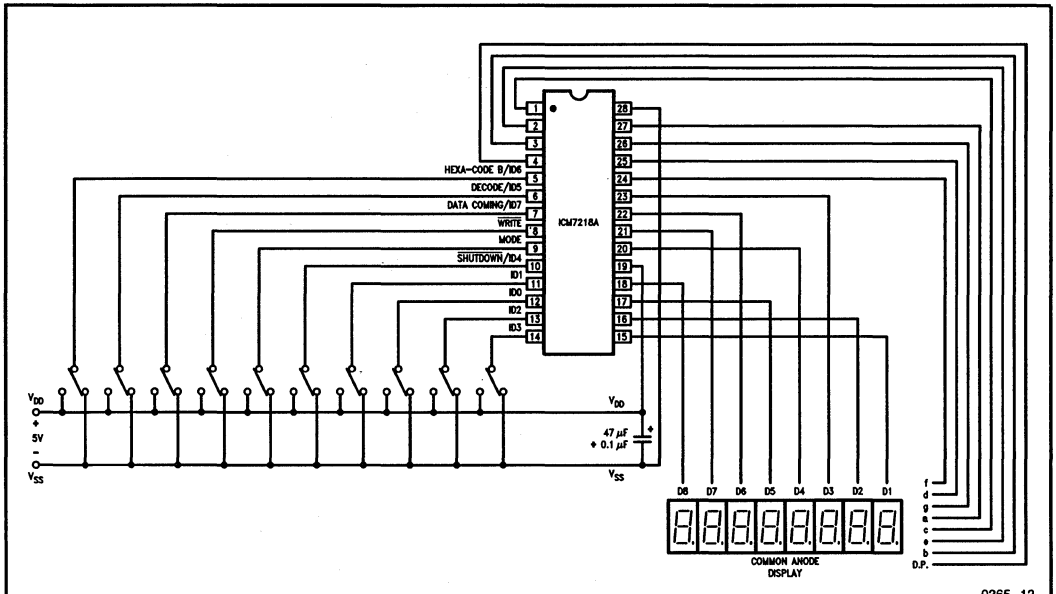


Figure 8: Functional Test Circuit (#1)

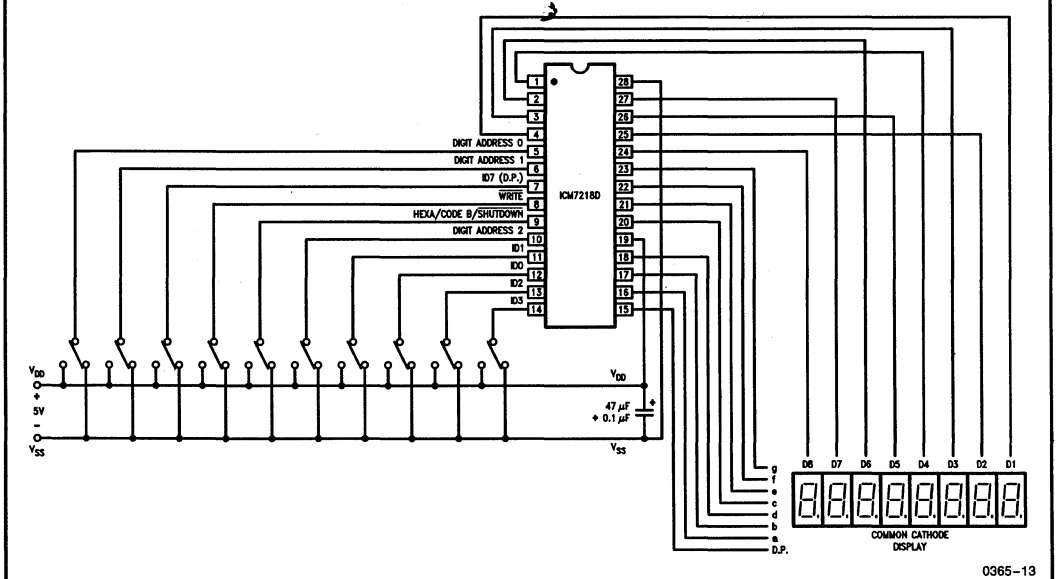
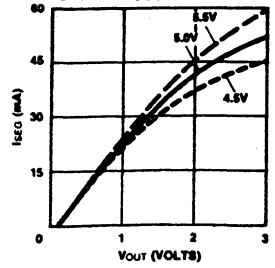


Figure 9: Functional Test Circuit (#2)

NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

COMMON ANODE SEG. DRIVER
I_{SEG} vs. V_{OUT} AT 25°C



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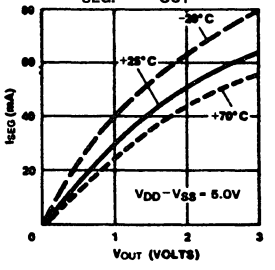
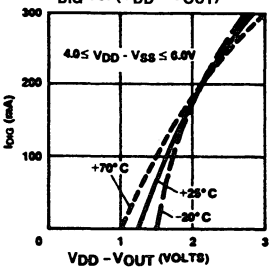
COMMON ANODE SEG. DRIVER
I_{SEG} vs. V_{OUT}



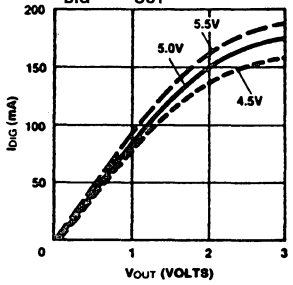
0365-15

COMMON ANODE DIGIT DRIVER
I_{DIG} vs. ($V_{DD} - V_{OUT}$)



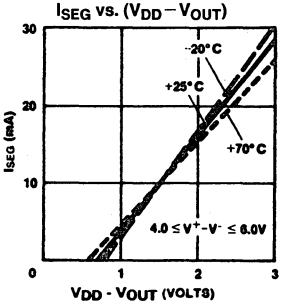
0365-16

COMMON CATHODE DIGIT DRIVER
I_{DIG} vs. V_{OUT} AT 25°C



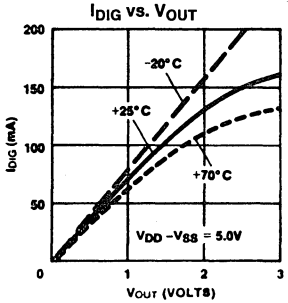
0365-17

COMMON CATHODE SEG. DRIVER
I_{SEG} vs. ($V_{DD} - V_{OUT}$)

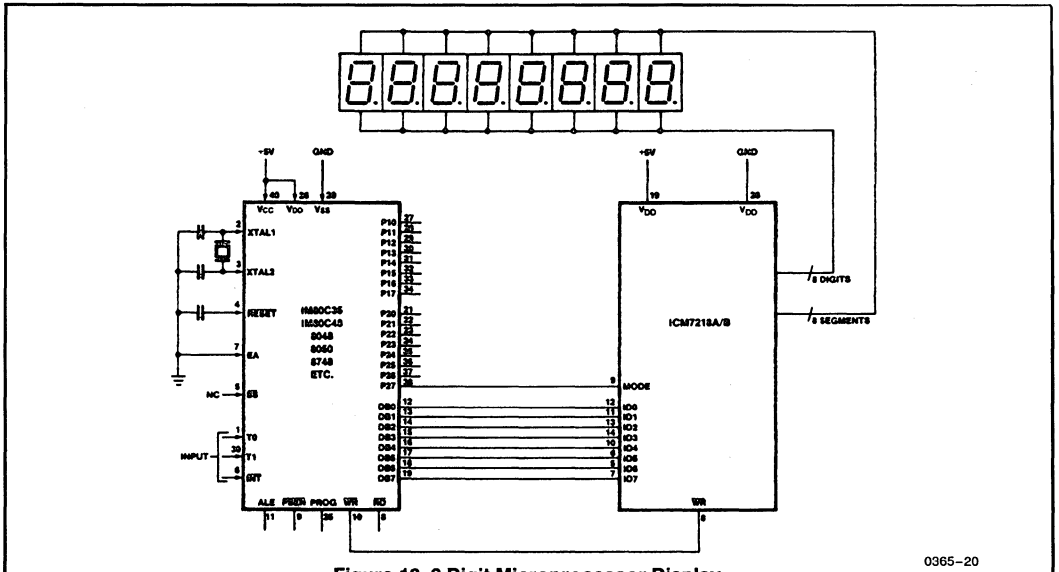


0365-18

COMMON CATHODE DIGIT DRIVER
I_{DIG} vs. V_{OUT}



0365-19



0365-20

Figure 10: 8 Digit Microprocessor Display

NOTE: All typical values have been characterized but are not tested.

APPLICATION EXAMPLES

8 DIGIT MICROPROCESSOR DISPLAY APPLICATION

Figure 10 shows a display interface using the ICM7218A/B with an 8048 family microcontroller. The 8 bit data bus (DB0/DB7-ID0/ID7) transfers control and data information to the 7218 display interface on successive $\overline{\text{WRITE}}$ pulses. The MODE input to the 7218 is connected to one of the I/O port pins on the microcontroller. When MODE is high a control word is transferred; when MODE is low data is transfered. Sequential locations in the 8-byte static memory are automatically loaded on each successive $\overline{\text{WRITE}}$ pulse. After eight $\overline{\text{WRITE}}$ pulses have occurred, further pulses are ignored until a new control word is transferred. (See Figure 6). This also allows writing to other peripheral devices without disturbing the ICM7218A/B.

16 DIGIT MICROPROCESSOR DISPLAY

In this application (see Figure 11), both ICM7218's are addressed simultaneously with a 3 bit word, DA2-DA0. Display data from the 8048 I/O bus (DB7-DB0) is transferred to both ICM7218's simultaneously.

The display digits from both ICM7218's are interleaved to allow adjacent pairs of digits to be loaded simultaneously from a single 8 bit data bus.

Decimal point information is supplied to the ICM7218's from the processor on port lines P26 and P27.

NO DECODE APPLICATION

The ICM7218 can also be used as a microprocessor based LED status panel driver. The microprocessor selected control word must include "No Decode" and "Data Coming". The processor writes "Ones" and "Zeroes" into the ICM7218 which in turn directly drives appropriate discrete LEDs. LED indicators can be red or green (8 segments $\times$8 digits=64 dots $\div$2 per red or green =32 channels).

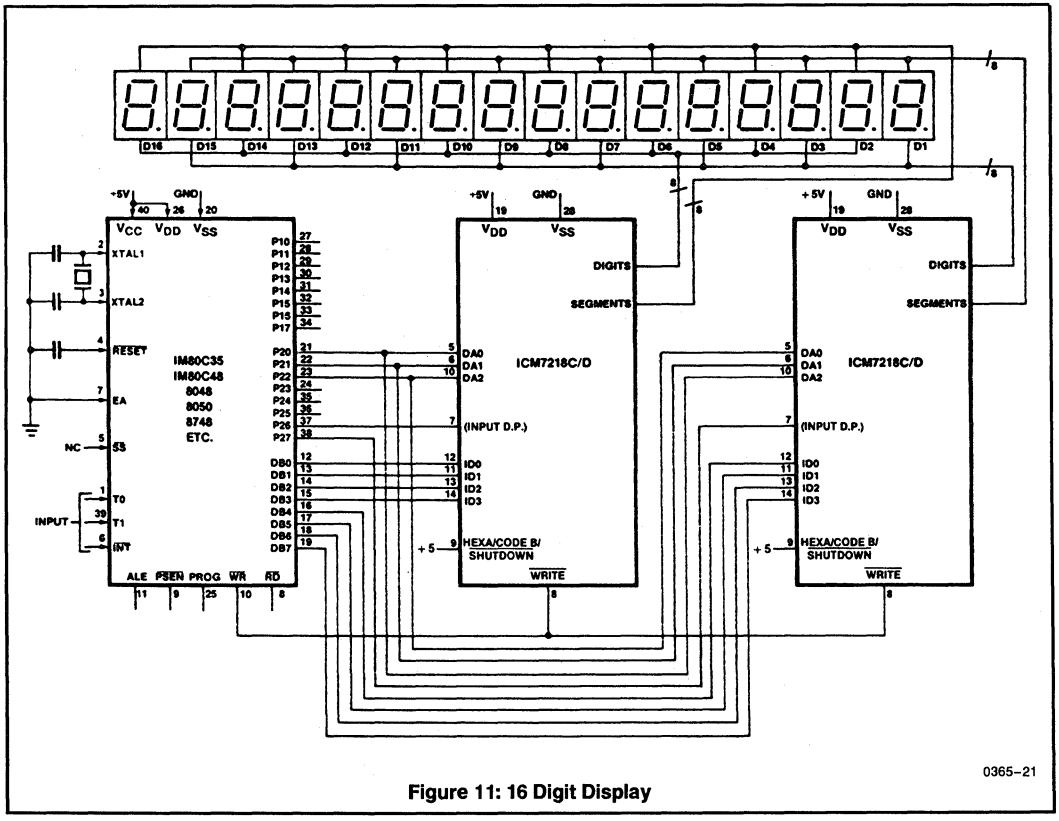


Figure 11: 16 Digit Display

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICM7228
8-Digit μP Compatible LED Display Decoder Driver

GENERAL DESCRIPTION

The Harris ICM7228 display driver interfaces microprocessors to an 8 digit, 7 segment, numeric LED display. Included on chip are two types of 7 segment decoder, multiplex scan circuitry, LED display segment drvers, LED display digit drivers and an 8-byte static memory as display RAM.

Data can be written to the ICM7228A and ICM7228B's display RAM in sequential 8 digit update or in single digit update format. Data is written to the ICM7228C and ICM7228D display RAM in parallel random access format. The ICM7228A and ICM7228C drive common anode displays. The ICM7228B and ICM7228D drive common cathode displays. All versions can display the RAM data as either Hexadecimal or Code B format. The ICM7228A and ICM7228B incorporate a No Decode mode allowing each bit of each digit's RAM word to drive individual display segments resulting in independent control of all display segments. As a result, bargraph and other irregular display segments and formats can be driven directly by this chip.

The Harris ICM7228 is an alternative to both the Maxim ICM7218 and the Harris ICM7218 display drivers. Notice that the ICM7228A/B has an additional single digit access mode. This could make the Harris ICM7218A/B software incompatible with ICM7228A/B operation. As a result, the part is renamed the ICM7228 to eliminate this possible confusion.

All versions of the ICM7228 are offered in both industrial and military temperature ranges.

FEATURES

- **Improved 2nd Source to Maxim ICM7218**
- **Fast Write Access Time of 200 ns**
- **Multiple Microprocessor Compatible Versions**
- **Hexadecimal, Code B and No Decode Modes**
- **Individual Segment Control with "No Decode" Feature**
- **Digit and Segment Drivers On-Chip**
- **Non-Overlapping Digits Drive**
- **Common Anode and Common Cathode LED Versions**
- **Low Power CMOS Architecture**
- **Single 5V Supply**
- **883B/Rev C Compliant**

APPLICATIONS

- **Instrumentation**
- **Test Equipment**
- **Hand Held Instruments**
- **Bargraph Displays**
- **Numeric and Non-Numeric Panel Displays**
- **High and Low Temperature Environments where LCD Display Integrity is Compromised**

ORDERING INFORMATION

Part Number	Tempertaure Range	Package	Data Entry Protocol	Display Type
ICM7228AIPI	−40°C to +85°C	28-Pin Plastic DIP	Sequential	Common Anode
ICM7228BIPI	−40°C to +85°C	28-Pin Plastic DIP	Sequential	Common Cathode
ICM7228CIPI	−40°C to +85°C	28-Pin Plastic DIP	Random	Common Anode
ICM7228DIPI	−40°C to +85°C	28-Pin Plastic DIP	Random	Common Cathode
ICM7228AIJI	−40°C to +85°C	28-Pin CERDIP	Sequential	Common Anode
ICM7228BIJI	−40°C to +85°C	28-Pin CERDIP	Sequential	Common Cathode
ICM7228CIJI	−40°C to +85°C	28-Pin CERDIP	Random	Common Anode
ICM7228DIJI	−40°C to +85°C	28-Pin CERDIP	Random	Common Cathode
ICM7228AIBI	−40°C to +85°C	28-Pin SOIC	Sequential	Common Anode
ICM7228BIBI	−40°C to +85°C	28-Pin SOIC	Sequential	Common Cathode
ICM7228CIBI	−40°C to +85°C	28-Pin SOIC	Random	Common Anode
ICM7228DIBI	−40°C to +85°C	28-Pin SOIC	Random	Common Cathode
ICM7228AMIJI	−55°C to +125°C	28-Pin CERDIP	Sequential	Common Anode
ICM7228BMIJI	−55°C to +125°C	28-Pin CERDIP	Sequential	Common Cathode
ICM7228CMIJI	−55°C to +125°C	28-Pin CERDIP	Random	Common Anode
ICM7228DMIJI	−55°C to +125°C	28-Pin CERDIP	Random	Common Cathode

*All MIJI versions available compliant to 883B/Rev C.

202820-002

NOTE: All typical values have been characterized but are not tested.

ICM7228

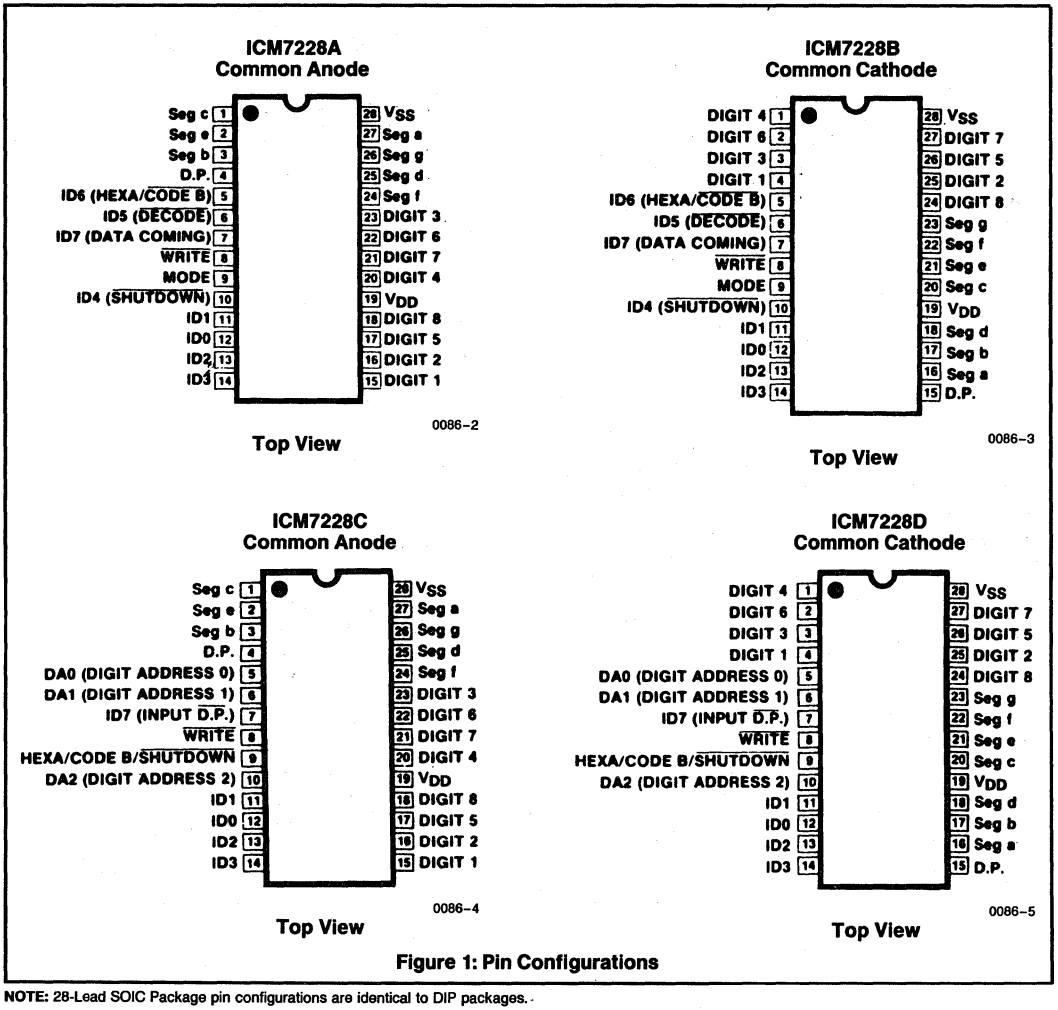


Figure 1: Pin Configurations

NOTE: 28-Lead SOIC Package pin configurations are identical to DIP packages.

NOTE: All typical values have been characterized but are not tested.

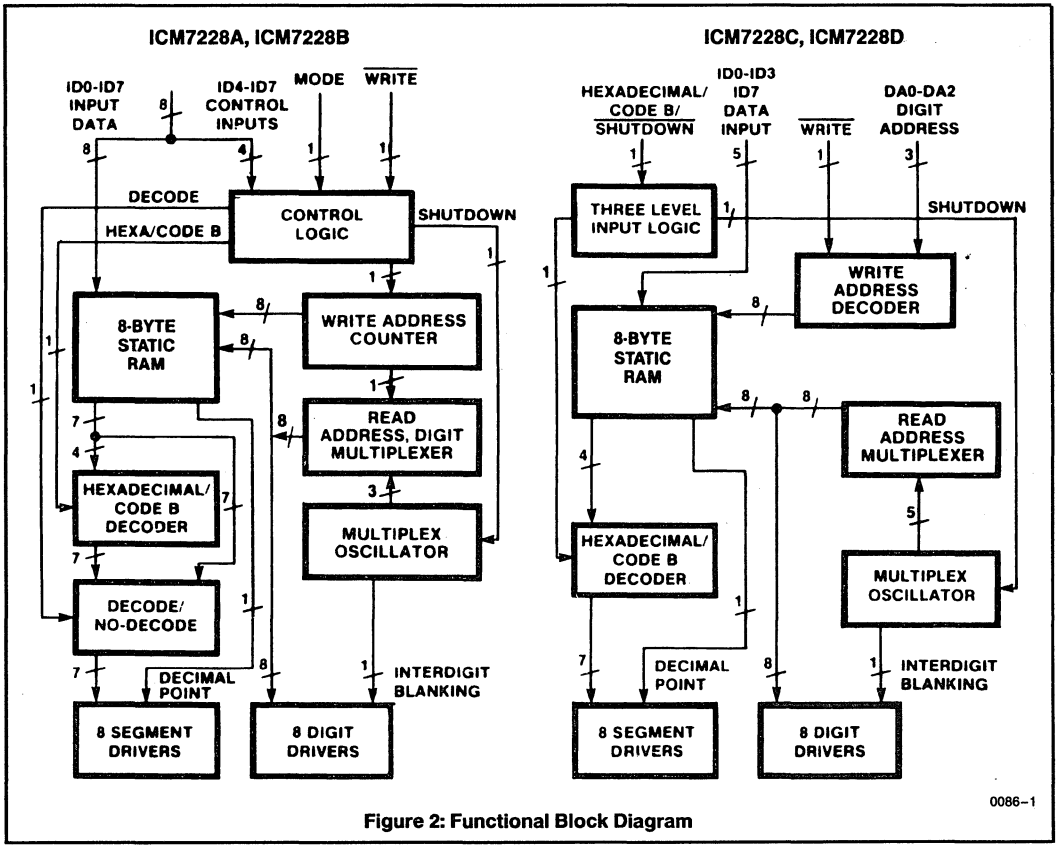


Figure 2: Functional Block Diagram

9

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) 6V
Digit Output Current ..... 500 mA
Segment Output Current ..... 100 mA
Input Voltage (Note 1)
(Any Terminal) ..... $(V_{SS} - 0.3V) < V_{IN} < (V_{DD} + 0.3V)$
Power Dissipation (Note 2)
28-Pin Plastic with Copper Leadframe 1.0W
28-Pin CERDIP 1.0W
28-Pin SOIC 0.7W
Operating Temperature Range
IPI, IJI, IBI Packages ..... $-40°C < T_A < +85°C$
MIJI Package ..... $-55°C < T_A < +125°C$
Storage Temperature Range ..... $-65°C < T_S < +160°C$
Lead Temperature (Soldering 10 sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTE 1: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from sources operating on a different power supply be applied to the device before its own supply is established, and when using multiple supply systems the supply to the ICM7228 should be turned on first.

NOTE 2: These limits refer to the package and will not be obtained during normal operation. Derate above 50°C by 25 mW per °C.

ELECTRICAL CHARACTERISTICS (V_{DD} = +5.0V ±10%, V_{SS} = 0V)

INDUSTRIAL TEMPERATURE RANGE, IPI, IJI, IBI DEVICES

Symbol	Parameter	Test Conditions	T_A = +25°C			−40°C ≤ T_A ≤ +85°C			Units
			Min	Typ	Max	Min	Typ	Max	
V_{SUPPLY}	Supply Voltage Range	Operating	4		6	4		6	V
		Power Down Mode	2			2			
I_Q	Quiescent Supply Current	Shutdown, 7228A, 7228B		1	100		1	100	µA
		Shutdown, 7228C, 7228D		2.5	100		2.5	100	
I_{DD}	Operating Supply Current	Common Anode, 7228A/C Segments = ON Outputs = OPEN		200	450		200	450	µA
		Common Anode, 7228A/C Segments = OFF Outputs = OPEN		100	450		100	450	
		Common Cathode, 7228B/D Segments = ON Outputs = OPEN		250	450		250	450	
		Common Cathode, 7228B/D Segments = OFF Outputs = OPEN		175	450		175	450	
I_{DIG}	Digit Drive Current	Common Anode, 7228A/C $V_{OUT} = V_{DD} - 2.0V$	200			175			mA
		Common Cathode, 7228B/D $V_{OUT} = V_{SS} + 1.0V$	50			40			
I_{DLK}	Digit Leakage Current	Shutdown Mode, V_{OUT} = 2.0V Common Anode, 7228A/C		1	100		1	100	µA
		Shutdown Mode, V_{OUT} = 5.0V Common Cathode, 7228B/D		1	100		1	100	
I_{SEG}	Peak Segment Drive Current	Common Anode, 7228A/C $V_{OUT} = V_{SS} + 1.0V$	20	25		20			mA
		Common Cathode, 7228B/D $V_{OUT} = V_{DD} - 2.0V$	10	12		10			

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (V_{DD} = +5.0V ±10%, V_{SS} = 0V) (Continued)

INDUSTRIAL TEMPERATURE RANGE, IPI, IJI, IBI DEVICES

Symbol	Parameter	Test Conditions	T_A = +25°C			−40°C ≤ T_A ≤ +85°C			Units
			Min	Typ	Max	Min	Typ	Max	
I_{SLK}	Segment Leakage Current	Shutdown Mode, V_{OUT} = V_{DD} Common Anode, 7228A/C		1	50		1	50	µA
		Shutdown Mode, V_{OUT} = V_{SS} Common Cathode, 7228B/D		1	50		1	50	
I_{IL}	Input Leakage Current	All Inputs except Pin 9 7228C, 7228D V_{IN} = V_{SS}			1			1	µA
		All Inputs except Pin 9 7228C, 7228D V_{IN} = 5.0V			−1			−1	
f_{MUX}	Display Scan Rate	Per Digit		390			390		Hz
t_{IDB}	Inter-Digit Blanking Time		2	10		2			µs
V_{INH}	Logical "1" Input Voltage	Three Level Input: Pin 9 7228C, 7228D Hexadecimal V_{DD} = 5V	4.2			4.2			V
V_{INF}	Floating Input	Three Level Input: Pin 9 7228C, 7228D Code B V_{DD} = 5V	2.0		3.0	2.0		3.0	V
V_{INL}	Logical "0" Input Voltage	Three Level Input: Pin 9 7228C, 7228D Shutdown V_{DD} = 5V			0.8			0.8	V
Z_{IN}	Three Level Input Impedance	V_{CC} = 5V Pin 9 of 7228C and 7228D	50			50			kΩ
V_{IH}	Logical "1" Input Voltage	All Inputs except Pin 9 of 7228C, 7228D V_{DD} = 5V	2.0			2.0			V
V_{IL}	Logical "0" Input Voltage				0.8			0.8	

SWITCHING CHARACTERISTICS (V_{DD} = +5.0V ±10%, V_{SS} = 0V, V_{IL} = +0.4V, V_{IH} = +2.4V)

INDUSTRIAL TEMPERATURE RANGE, IPI, IJI, IBI DEVICES

Symbol	Parameter	Test Conditions	T_A = +25°C			−40°C ≤ T_A ≤ +85°C			Units
			Min	Typ	Max	Min	Typ	Max	
t_{WL}	Write Pulsewidth (Low)		200	100		250			ns
t_{WH}	Write Pulsewidth (High)		850	540		1200			ns
t_{MH}	Mold Hold Time	7228A, 7228B	0	−65		0			ns
t_{MS}	Mold Setup Time	7228A, 7228B	250	150		250			ns
t_{DS}	Data Setup Time		250	160		250			ns
t_{DH}	Data Hold Time		0	−60		0			ns
t_{AS}	Digit Address Setup Time	7228C, 7228D	250	110		250			ns
t_{AH}	Digit Address Hold Time	7228C, 7228D	0	−60		0			ns

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (V_{DD} = +5.0V ±10%, V_{SS} = 0V) (Continued)

MILITARY TEMPERATURE RANGE, MIJI DEVICES

Symbol	Parameter	Test Conditions	T_A = +25°C			−55°C ≤ T_A ≤ +125°C			Units
			Min	Typ	Max	Min	Typ	Max	
V_{SUPPLY}	Supply Voltage Range	Operating	4		6	4		6	V
		Power Down Mode	2			2			
I_Q	Quiescent Supply Current	Shutdown, 7228A, 7228B		1	100		1	100	µA
		Shutdown, 7228C, 7228D		2.5	100		2.5	100	
I_{DD}	Operating Supply Current	Common Anode, 7228A/C Segments = ON Outputs = OPEN		200	450		200	550	µA
		Common Anode, 7228A/C Segments = OFF Outputs = OPEN		100	450		100	450	
		Common Cathode, 7228C/D Segments = ON Outputs = OPEN		250	450		250	550	
		Common Cathode, 7228C/D Segments = OFF Outputs = OPEN		175	450		175	450	
I_{DIG}	Digit Drive Current	Common Anode, V_{DD} = 5.0V V_{OUT} = V_{DD} − 2.0V	200			170			mA
		Common Cathode, V_{DD} = 5.0V V_{OUT} = V_{SS} + 1.0V	50			35			
I_{DLK}	Digit Leakage Current	Shutdown Mode Common Anode, , V_{OUT} = 2.0V		1	100		1	100	µA
		Shutdown Mode Common Cathode, V_{OUT} = 5.0V		1	100		1	100	
I_{SEG}	Peak Segment Drive Current	Common Anode, V_{DD} = 5.0V V_{OUT} = V_{SS} + 1.0V	20	25		20	25		mA
		Common Cathode, V_{DD} = 5.0V V_{OUT} = V_{DD} − 2.0V	10	12		10	12		
I_{SLK}	Segment Leakage Current	Shutdown Mode Common Anode, V_{OUT} = V_{DD}		1	50		1	50	µA
		Shutdown Mode Common Cathode, V_{OUT} = V_{SS}		1	50		1	50	
I_{IL}	Input Leakage Current	All Inputs except Pin 9 7228C, 7228D V_{IN} = V_{SS}			1			1	µA
		All Inputs except Pin 9 7228C, 7228D V_{IN} = 5.0V			−1			−1	
f_{MUX}	Display Scan Rate	Per Digit		390			390		Hz
t_{IDB}	Inter-Digit Blanking Time		2	10		2	10		µs

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (V_{DD} = +5.0V ±10%, V_{SS} = 0V) (Continued)

MILITARY TEMPERATURE RANGE, MIJI DEVICES

Symbol	Parameter	Test Conditions	T_A = +25°C			−55°C ≤ T_A ≤ +125°C			Units
			Min	Typ	Max	Min	Typ	Max	
V_{INH}	Logial "1" Input Voltage	Three Level Input: Pin 9 7228C, 7228D Hexadecimal V_{DD} = 5V	4.2			4.2			V
V_{INF}	Floating Input	Three Level Input: Pin 9 7228C, 7228D Code B V_{DD} = 5V	2.0		3.0	2.4		3.0	V
V_{INL}	Logical "0" Input Voltage	Three Level Input: Pin 9 7228C, 7228D Shutdown V_{DD} = 5V			0.8			0.4	V
Z_{IN}	Three Level Input Impedance	V_{CC} = 5V Pin 9 of 7228C and 7228D	50			50			kΩ
V_{IH}	Logical "1" Input Voltage	All Inputs except Pin 9 of 7228C, 7228D V_{DD} = 5V	2.0			2.0			V
V_{IL}	Logical "0" Input Voltage				0.8			0.8	

SWITCHING CHARACTERISTICS (V_{DD} = +5.0V ±10%, V_{SS} = 0V, V_{IL} = +0.4V, V_{IH} = +2.4V)

MILITARY TEMPERATURE RANGE, MIJI DEVICES

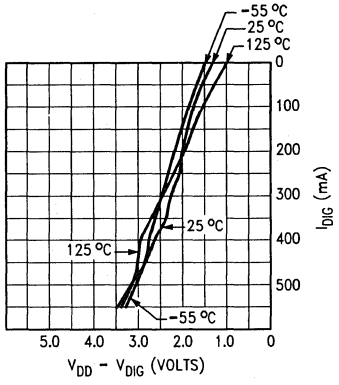
Symbol	Parameter	Test Conditions	T_A = +25°C			−55°C ≤ T_A ≤ +125°C			Units
			Min	Typ	Max	Min	Typ	Max	
t_{WL}	Write Pulsewidth (Low)		200	100		250	115		ns
t_{WH}	Write Pulsewidth (High)		850	540		1200	840		ns
t_{MH}	Mode Hold Time	7228A, 7228B	0	−65		0	−65		ns
t_{MS}	Mode Setup Time	7228A, 7228B	250	150		250	165		ns
t_{DS}	Data Setup Time		250	160		250	160		ns
t_{DH}	Data Hold Time		0	−60		0	−60		ns
t_{AS}	Digit Address Setup Time	7228C, 7228D	250	110		250	100		ns
t_{AH}	Digit Address Hold Time	7228C, 7228D	0	−60		0	−60		ns

NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

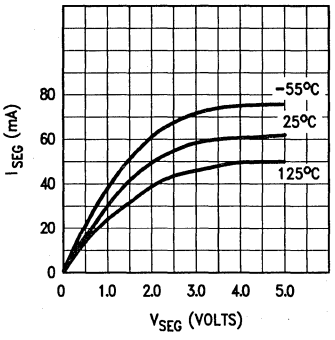
Common Anode Drivers:

Common Anode Digit Driver
I_{DIG} vs (V_{DD} − V_{DIG}) @ T_A°C



0086-12

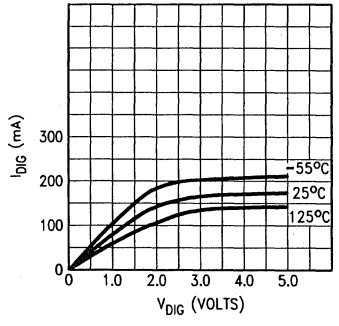
Common Anode Segment Driver
I_{SEG} vs V_{SEG} @ T_A°C



0086-23

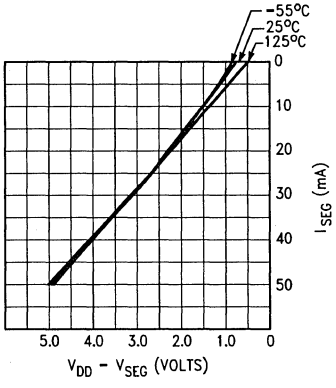
Common Cathode Drivers:

Common Cathode Digit Driver
I_{DIG} vs V_{DIG} @ T_A°C



0086-15

Common Cathode Segment Driver
I_{SEG} vs (V_{DD} − V_{SEG}) @ T_A°C



0086-13

NOTE: All typical values have been characterized but are not tested.

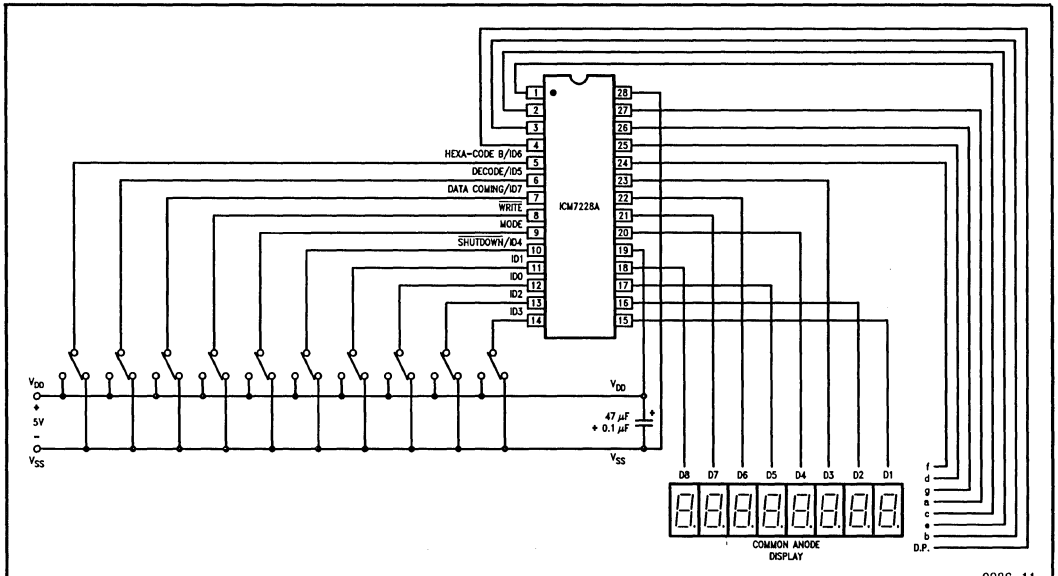


Figure 3: Functional Test Circuit (# 1)

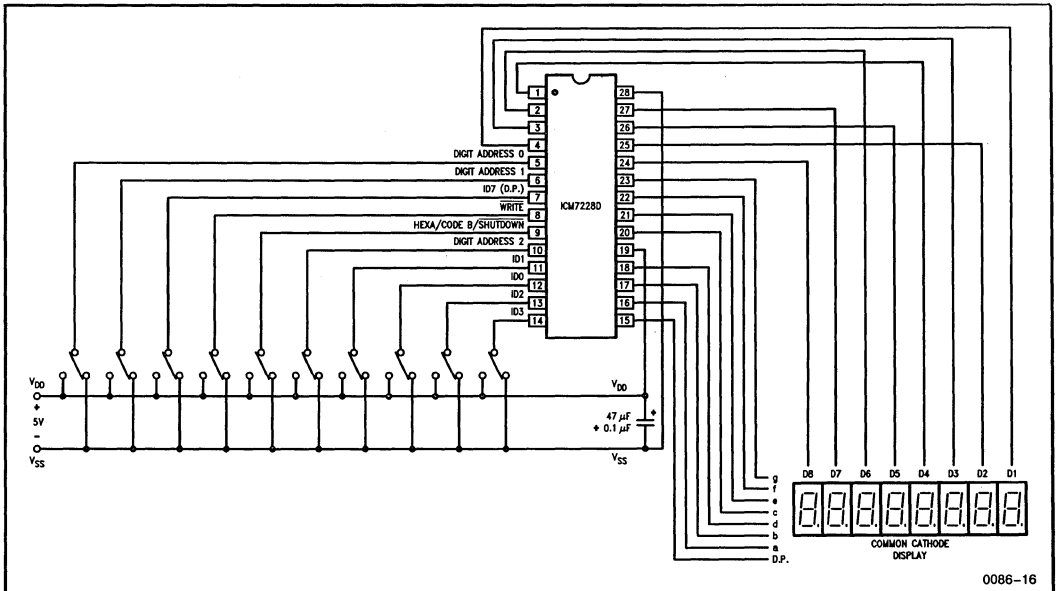


Figure 4: Functional Test Circuit (# 2)

NOTE: All typical values have been characterized but are not tested.

Table 1: ICM7228A Pin Assignments and Descriptions

Pin #	Name	Function	Description
1 2 3 4	Seg c Seg e Seg b D.P.	Output	LED Display Segments c, e, b and Decimal Point Drive Lines.
5	ID6, (HEXA/$\overline{\text{CODE B}}$)	Input	When "MODE" Low: Display Data Input, Bit 7. When "MODE" High: Control Bit, Decoding Scheme Selection: High, Hexadecimal Decoding. Low, Code B Decoding.
6	ID5, ($\overline{\text{DECODE}}$)	Input	When "MODE" Low: Display Data Input, Bit 6. When "MODE" High: Control Bit, Decode/No Decode Selection: High, No Decode. Low, Decode.
7	ID7, (DATA COMING)	Input	When "MODE" Low: Display Data Input, Bit 8, Decimal Point Data. When "MODE" High: Control Bit, Sequential Data Update Select: High, Data Coming. Low, No Data Coming.
8	$\overline{\text{WRITE}}$	Input	Data Input Will Be Written to Control Register or Display RAM on Rising Edge of WRITE.
9	MODE	Input	Selects Data to Be Loaded to Control Register or Display RAM: High, Loads Control Register. Low, Loads Display RAM.
10	ID4, ($\overline{\text{SHUTDOWN}}$)	Input	When "MODE" Low: Display Data Input, Bit 5. When "MODE" High: Control Bit, Low Power Mode Select: High, Normal Operation. Low, Oscillator and Display Disabled.
11	ID1	Input	When "MODE" Low: Display Data Input, Bit 2. When "MODE" High and "ID7 (DATA COMING)" Low: Digit Address, Bit 2, Single Digit Update Mode.
12	ID0	Input	When "MODE" Low: Display Data Input, Bit 1. When "MODE" High and "ID7 (DATA COMING)" Low: Digit Address, LSB, Single Digit Update Mode.
13	ID2	Input	When "MODE" Low: Display Data Input, Bit 3. When "MODE" High and "ID7 (DATA COMING)" Low: Digit Address, MSB, Single Digit Update Mode.
14	ID3	Input	When "MODE" Low: Display Data Input, Bit 4. When "MODE" High: RAM Bank Select (Decode Modes Only): High, RAM Bank A. Low, RAM Bank B.
15 16 17 18	DIGIT 1 DIGIT 2 DIGIT 5 DIGIT 8	Output	LED Display Digits 1, 2, 5 and 8 Drive Lines.
19	V_{DD}	Supply	Device Positive Power Supply Rail.
20 21 22 23	DIGIT 4 DIGIT 7 DIGIT 6 DIGIT 3	Output	LED Display Digits 4, 7, 6 and 3 Drive Lines.
24 25 26 27	Seg f Seg d Seg g Seg a	Output	LED Display Segments f, d, g and a Drive Lines.
28	V_{SS}	Supply	Device Ground or Negative Power Supply Rail.

NOTE: All typical values have been characterized but are not tested.

Table 2: ICM7228B Pin Assignments and Descriptions

Pin #	Name	Function	Description
1 2 3 4	DIGIT 4 DIGIT 6 DIGIT 3 DIGIT 1	Output	LED Display Digits 4, 6, 3 and 1 Drive Lines.
5	ID6, (HEXA/$\overline{\text{CODE B}}$)	Input	When "MODE" Low: Display Data Input, Bit 7. When "MODE" High: Control Bit, Decoding Scheme Selection: High, Hexadecimal Decoding. Low, Code B Decoding.
6	ID5, ($\overline{\text{DECODE}}$)	Input	When "MODE" Low: Display Data Input, Bit 6. When "MODE" High: Control Bit, Decode/No Decode Selection: High, No Decode. Low, Decode.
7	ID7, (DATA COMING)	Input	When "MODE" Low: Display Data Input, Bit 8, Decimal Point Data. When "MODE" High: Control Bit, Sequential Data Update Select: High, Data Coming. Low, No Data Coming.
8	$\overline{\text{WRITE}}$	Input	Data Input Will Be Written to Control Register or Display RAM on Rising Edge of $\overline{\text{WRITE}}$.
9	MODE	Input	Selects Data to Be Loaded to Control Register or Display RAM: High, Loads Control Register. Low, Loads Display RAM.
10	ID4, ($\overline{\text{SHUTDOWN}}$)	Input	When "MODE" Low: Display Data Input, Bit 5. When "MODE" High: Control Bit, Low Power Mode Select: High, Normal Operation. Low, Oscillator and Display Disabled.
11	ID1	Input	When "MODE" Low: Display Data Input, Bit 2. When "MODE" High and "ID7 (DATA COMING)" Low: Digit Address, Bit 2, Single Digit Update Mode.
12	ID0	Input	When "MODE" Low: Display Data Input, Bit 1. When "MODE" High and "ID7 (DATA COMING)" Low: Digit Address, LSB, Single Digit Update Mode.
13	ID2	Input	When "MODE" Low: Display Data Input, Bit 3. When "MODE" High and "ID7 (DATA COMING)" Low: Digit Address, MSB, Single Digit Update Mode.
14	ID3	Input	When "MODE" Low: Display Data Input, Bit 4. When "MODE" High: RAM Bank Select (Decode Modes Only): High, RAM Bank A. Low, RAM Bank B.
15 16 17 18	D.P. Seg a Seg b Seg d	Output	LED Display Segments c, e, b and Decimal Point Drive Lines.
19	V_{DD}	Supply	Device Positive Power Supply Rail.
20 21 22 23	Seg c Seg e Seg f Seg g	Output	LED Display Segments c, e, f and g Drive Lines.
24 25 26 27	DIGIT 8 DIGIT 2 DIGIT 5 DIGIT 7	Output	LED Display Digits 8, 2, 5 and 7 Drive Lines.
28	V_{SS}	Supply	Device Ground or Negative Power Supply Rail.

NOTE: All typical values have been characterized but are not tested.

Table 3: ICM7228C Pin Assignments and Descriptions

Pin #	Name	Function	Description
1 2 3 4	Seg c Seg e Seg b D.P.	Output	LED Display Segments c, e, b and Decimal Point Drive Lines.
5	DA0	Input	Digit Address Input, Bit 1, LSB.
6	DA1	Input	Digit Address Input, Bit 2.
7	ID7, (INPUT $\overline{\text{D.P.}}$)	Input	Display Decimal Point Data Input, Negative True.
8	$\overline{\text{WRITE}}$	Input	Data Input Will Be Written to Display RAM on Rising Edge of $\overline{\text{WRITE}}$.
9	HEXA/CODE B/ $\overline{\text{SHUTDOWN}}$	Input	Three Level Input. Display Function Control: High, Hexadecimal Decoding. Float, Code B Decoding. Low, Oscillator and Display Disabled.
10	DA2	Input	Digit Address Input, Bit 3, MSB.
11 12 13 14	ID1 ID0 ID2 ID3	Input	Display Data Inputs.
15 16 17 18	DIGIT 1 DIGIT 2 DIGIT 5 DIGIT 8	Output	LED Display Digits 1, 2, 5, and 8 Drive Lines.
19	V_{DD}	Supply	Device Positive Power Supply Rail.
20 21 22 23	DIGIT 4 DIGIT 7 DIGIT 6 DIGIT 3	Output	LED Display Digits 4, 7, 6, and 3 Drive Lines.
24 25 26 27	Seg f Seg d Seg g Seg a	Output	LED Display Segments f, d, g and a Drive Lines.
28	V_{SS}	Supply	Device Ground or Negative Power Supply Rail.

NOTE: All typical values have been characterized but are not tested.

Table 4: ICM7228D Pin Assignments and Descriptions

Pin #	Name	Function	Description
1 2 3 4	DIGIT 4 DIGIT 6 DIGIT 3 DIGIT 1	Output	LED Display Digits 4, 6, 3, and 1 Drive Lines.
5	DA0	Input	Digit Address Input, Bit 1, LSB.
6	DA1	Input	Digit Address Input, Bit 2.
7	ID7, (INPUT $\overline{\text{D.P.}}$)	Input	Display Decimal Point Data Input, Negative True.
8	$\overline{\text{WRITE}}$	Input	Data Input Will Be Written to Display RAM on Rising Edge of $\overline{\text{WRITE}}$.
9	HEXA/CODE B/ $\overline{\text{SHUTDOWN}}$	Input	Three Level Input. Display Function Control: High, Hexadecimal Decoding. Float, Code B Decoding. Low, Oscillator and Display Disabled.
10	DA2	Input	Digit Address Input, Bit 3, MSB.
11 12 13 14	ID1 ID0 ID2 ID3	Input	Display Data Inputs.
15 16 17 18	D.P. Seg a Seg b Seg d	Output	LED Display Segments a, b, d and Decimal Point Drive Lines.
19	V_{DD}	Supply	Device Positive Power Supply Rail.
20 21 22 23	Seg c Seg e Seg f Seg g	Output	LED Display Segments c, e, f and g Drive Lines.
24 25 26 27	DIGIT 8 DIGIT 2 DIGIT 5 DIGIT 7	Output	LED Display Digits 8, 2, 5 and 7 Drive Lines.
28	V_{SS}	Supply	Device Ground or Negative Power Supply Rail.

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

System Interfacing and Data Entry Modes, ICM7228A and ICM7228B

The ICM7228A/B devices are compatible with the architectures of most microprocessor systems. Their fast switching characteristics makes it possible to access them as a memory mapped I/O device with no wait state necessary in most microcontroller systems. All the ICM7228A/B inputs, including MODE, feature a 250 ns minimum setup and 0 ns hold time with a 200 ns minimum WRITE pulse. Input logic levels are TTL and CMOS compatible. Figure 7 shows a generic method of driving the ICM7228A/B from a microprocessor bus. To the microprocessor, each device appears to be 2 separate I/O locations; the Control Register and the Display RAM. Selection between the two is accomplished by the MODE input driven by address line A0. Input data is placed on the ID0–ID7 lines. The WRITE input acts as both a device select and write cycle timing pulse. See Figure 5 and Switching Characteristics Table for write cycle timing parameters.

The ICM7228A/B have three data entry modes: Control Register update without RAM update, sequential 8 digit update and single digit update. In all three modes a control word is first written by pulsing the $\overline{\text{WRITE}}$ input while the MODE input is high, thereby latching data into the Control Register. The logic level of individual bits in the Control Register select Shutdown, Decode/No Decode, Hex/Code B, RAM bank A/B and Display RAM digit address as shown in Tables 1 and 2.

The ICM7228A/B Display RAM is divided into 2 banks, called bank A and B. When using the Hexadecimal or code B display modes, these RAM banks can be selected separately. This allows two separate sets of display data to be stored and displayed alternately. Notice that the RAM bank selection is not possible in No-Decode mode, this is because the display data in the No-Decode mode has 8 bits, but in Decoded schemes (Hex/Code B) is only 4 bits (ID0–ID3 data). It should also be mentioned that the decimal point is independent of selected bank, a turned on decimal point will remain on for either banks. Selection of the RAM banks is controlled by ID3 input. The ID3 logic level (during Control Register update) selects which bank of the internal RAM to be written to and/or displayed.

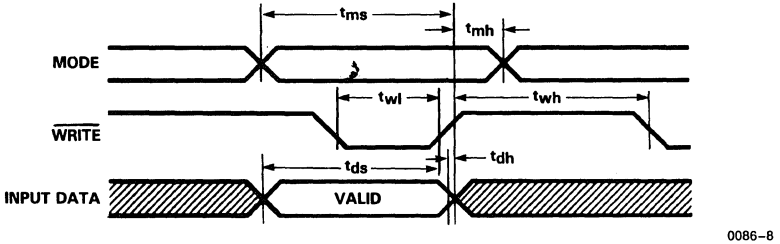


Figure 5: ICM7228A/B Write Cycle Timing Diagram

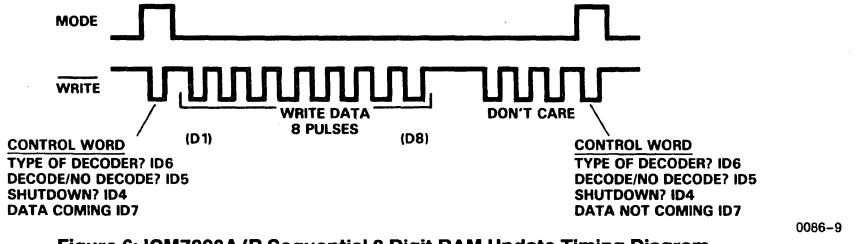


Figure 6: ICM7228A/B Sequential 8 Digit RAM Update Timing Diagram

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTIONS (Continued)

Control Register update without RAM update:

The Control Register can be updated without changing the display data by a single pulse on the $\overline{\text{WRITE}}$ input, with MODE high and DATA COMING low. If the display is being decoded (Hex/Code B), then the value of ID3 determines which RAM bank will be selected and displayed for all eight digits.

Sequential 8 digit update:

The logic state of DATA COMING (ID7) is also latched during a Control Register update. If the latched value of DATA COMING (ID7) is high, the display becomes blanked and a sequential 8 digit update is initiated. Display data can now be written into RAM with 8 successive $\overline{\text{WRITE}}$ pulses, starting with digit 1 and ending with digit 8 (See Figure 6). After all 8 RAM locations have been written to, the display turns on again and the new data is displayed. Additional write pulses are ignored until a new Control Register update is performed. All 8 digits are displayed in the format (Hex/Code B or No Decode) specified by the control word that preceded the 8 digit update. If a decoding scheme (Hex/Code B) is to be used than the value of ID3 during the control word update determines which RAM bank will be written to.

Single Digit update:

In this mode each digit data in the display RAM can be updated individually without changing the other display data. First, with MODE input high, a control word is written to the Control Register carrying the following information; DATA COMING (ID7) low, the desired display format data on ID4–ID6, the RAM bank selected by ID3 (if decoding is selected) and the address of the digit to be updated on data lines ID0–ID2 (See Table 5). A second write to the ICM7228A/B, this time with MODE input low, transfers the data at the ID0-ID7 inputs into the selected digit's RAM location. In single digit update mode, each individual digit's data can be specified independently for being displayed in Decoded or No-Decode mode. For those digits which decoding scheme (Hex/Code B) is selected, only one can be effective at a time. Whenever a control word is written, the specified decoding scheme will be applied to all those digits which selected to be displayed in Decoded mode.

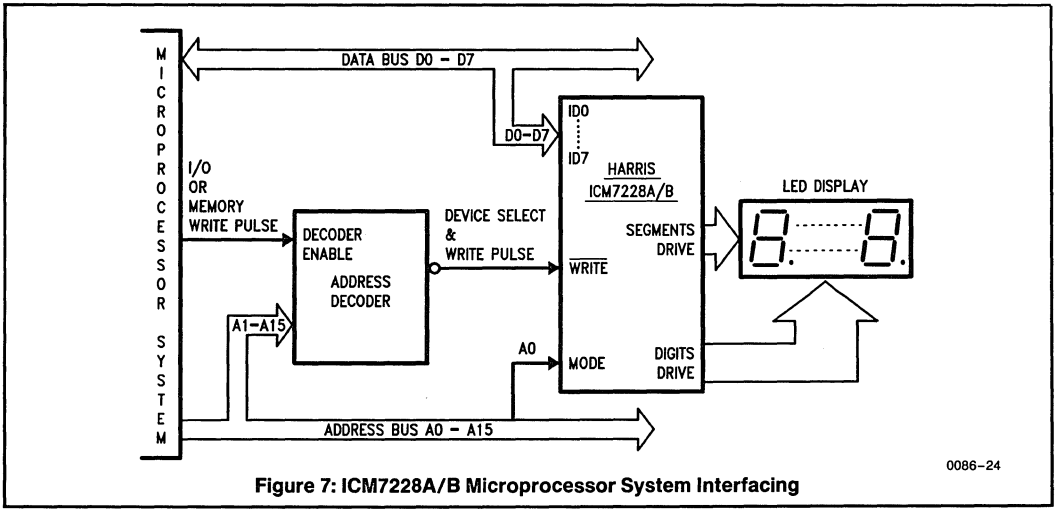


Figure 7: ICM7228A/B Microprocessor System Interfacing

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTIONS (Continued)

Table 5: Digits Address, ICM7228A/B

Input Data Lines			Selected Digit
ID2	ID1	ID0	
0	0	0	DIGIT 1
0	0	1	DIGIT 2
0	1	0	DIGIT 3
0	1	1	DIGIT 4
1	0	0	DIGIT 5
1	0	1	DIGIT 6
1	1	0	DIGIT 7
1	1	1	DIGIT 8

System Interfacing, ICM7228C and ICM7228D

The ICM7228C/D devices are directly compatible with the architecture of most microprocessor systems. Their fast switching characteristics make it possible to access them as a memory mapped I/O device with no wait state necessary in most microcontroller systems. All the ICM7228C/D inputs, excluding HEXA/CODE B/$\overline{\text{SHUTDOWN}}$, feature a 250 ns minimum setup and 0 ns hold time with a 200 ns minimum $\overline{\text{WRITE}}$ pulse. Input logic levels are TTL and CMOS compatible. Figure 9 shows a generic method of driving the ICM7228C/D from a microprocessor bus. To the microprocessor, the 8 bytes of the Display RAM appear to be 8 separate I/O locations. Loading the ICM7228C/D is quite similar to a standard memory write cycle. The address of the digit to be updated is placed on lines DA0–DA2, the data to be written is placed on lines ID0–ID3 and ID7, then a low pulse on $\overline{\text{WRITE}}$ input will transfer the data in. See Figure 8 and Switching Characteristics Table for write cycle timing parameters.

The ICM7228C/D devices do not have any control register, and also they do not provide the No Decode display format. Hexadecimal or Code B character selection and shutdown mode are directly controlled through the three-level input at Pin 9, which is accordingly called HEXA/CODE B/$\overline{\text{SHUTDOWN}}$. See Tables 3 and 4 for input and output definitions of the ICM7228C/D devices.

Compatibility with the ICM7218 Series

The Harris ICM7228 series devices are upwardly compatible with the ICM7218 series. The following are the differences between two series.

1. The ICM7228 versions A and B have two functions which are not available in 7218, the RAM bank select and single digit update. Software written for ICM7218A/B may not be directly compatible with ICM7228A/B operation. ID0–ID3 are "don't cares" when writing a control word to the ICM7218A/B, while for the ICM7228A/B, ID0–ID2 select the digit address for a single digit RAM update and ID3 always selects either bank A or bank B for Hex and Code B data. Considering the ID3 input only, the software is compatible provided all control word updates use a consistent value for ID3, either high or low. The single digit update mode is upwardly compatible, it is an invalid operation with the ICM7218A/B and is unlikely to occur in software originally written for the ICM7218A/B. But depending on system hardware (address decoding and $\overline{\text{WRITE}}$ pulse generation) the software might not function properly if an ICM7228A/B is going to be inserted in the ICM7218A/B socket. Some minor modifications of the software may be necessary.
2. The ICM7228 series has enhanced switching characteristics and is more than twice as fast as the ICM7218 series.
3. The ICM7228 series digit and segment drivers are improved compared to those of the ICM7218 series. Also the Typical display scan rate is increased from 250 Hz to 390 Hz to enhance display performance.
4. The ICM7228 series devices generally draw less current than the ICM7218 series. In the shutdown mode, the ICM7228A/B devices draw $1/10$ the current of the equivalent ICM7218 parts. The ICM7228C/D devices draw $1/4$ the current of the ICM7218 series part.

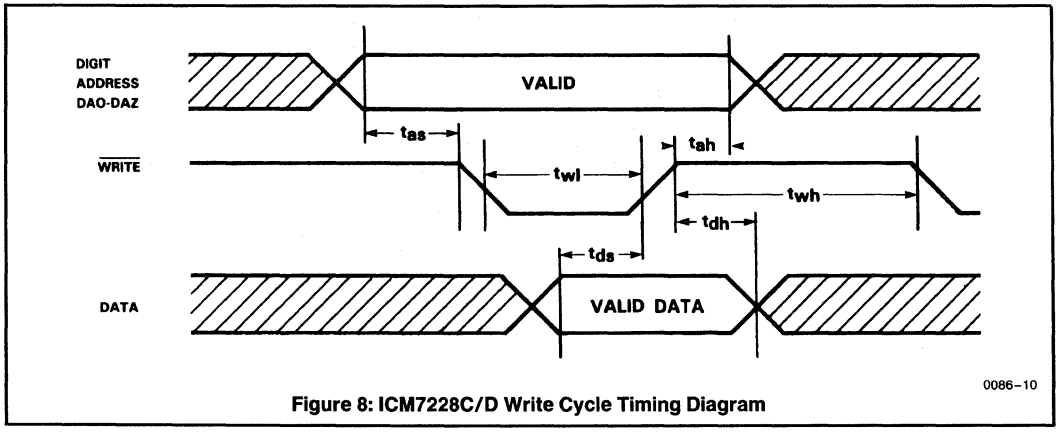


Figure 8: ICM7228C/D Write Cycle Timing Diagram

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTIONS (Continued)

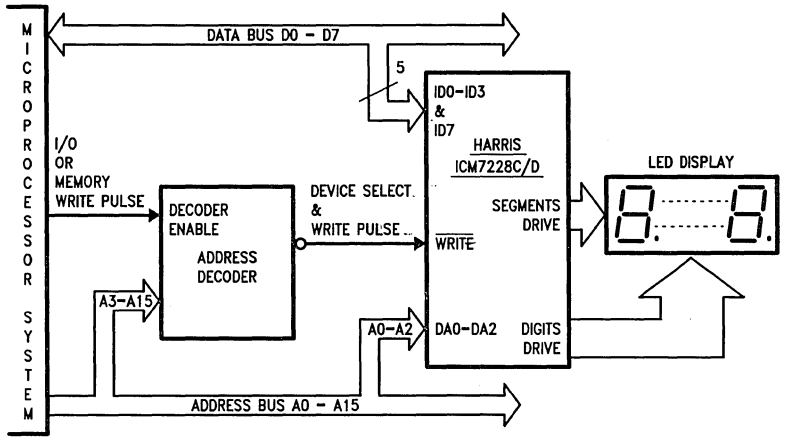


Figure 9: ICM7228C/D Microprocessor System Interfacing

Table 6: Display Character Sets

Input Data Code				Display Characters	
ID3	ID2	ID1	ID0	Hexadecimal	Code B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	—
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(Blank)

Display Formats

The ICM7228A and ICM7228B have three possible display formats; Hexadecimal, Code B and No Decode. Table 6 shows the character sets for the decode modes and their corresponding input code.

The display formats of the ICM7228A/B are selected by writing data to bits ID4, ID5 and ID6 of the Control Register (See Table 1 and 2 for input Definitions). Hexadecimal and Code B data is entered via ID0–ID3 and ID7 controls the decimal point.

Table 7: No Decode Segment Locations

Data Input	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Controlled Segment	Decimal Point	a	b	c	e	g	f	d

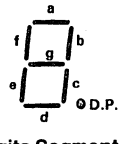


Figure 10: Digits Segment Assignments

The No Decode mode of the ICM7228A and ICM7228B allows the direct segment-by-segment control of all 64 segments driven by the device. In the No Decode mode, the input data directly control the outputs as shown in Table 7.

An input high level turns on the respective segment, except for the decimal point, which is turned on by an input low level on ID7.

The No Decode mode can be used in different applications such as bar graph or status panel driving where each segment controls an individual LED.

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTIONS (Continued)

The ICM7228C and ICM7228D have only the Hexadecimal and Code B character sets. The HEXA/CODE B/$\overline{\text{SHUTDOWN}}$ input, pin 9, requires a three level input. Pin 9 selects the Hexadecimal format when pulled high, the Code B format when floating or driven to mid-supply, and the shutdown mode when pulled low (See Tables 3 and 4). Table 6 also applies to the ICM7228C/D devices.

Shutdown and Display Blanking

When shutdown, the ICM7228 enters a low power standby mode typically consuming only 1 μA of supply current for the ICM7228A/B and 2.5 μA for the ICM7228C/D. In this mode the ICM7228 turns off the multiplex scan oscillator as well as the digit and segment drivers. However, input data can still be entered when in the shutdown mode. Data is retained in memory even with the supply voltage as low as 2V.

The ICM7228A/B is shutdown by writing a control word with Shutdown (ID4) low. The ICM7228C/D is put into shutdown mode by driving pin 9, HEXA/CODE B/$\overline{\text{SHUTDOWN}}$, low.

The ICM7228 operating current with the display blanked is within 100 μA–200 μA for all versions. All versions of the ICM7228 can be blanked by writing Hex FF to all digits and selecting Code B format. The ICM7228A and ICM7228B can also be blanked by selecting No Decode mode and writing Hex 80 to all digits (See Tables 6 and 7).

Common Anode Display Drivers, ICM7228A and ICM7228C

The common anode digit and segment driver output schematics are shown in Figure 11. The common anode digit driver output impedance is approximately 4Ω. This provides a nearly constant voltage to the display digits. Each digit has a minimum of 200 mA drive capability. The N-channel segment driver's output impedance of 50Ω limits the segment current to approximately 25 mA peak current per segment. Both the segment and digit outputs can directly drive the display, current limiting resistors are not required.

Individual segment's current is not significantly affected by whether other segments are on or off. This is because the segment driver output impedance is much higher than that of the digit driver. This feature is important in bar graph applications where each bar graph element should have the same brightness, independent of the number of elements being turned on.

Common Cathode Display Drivers, ICM7228B and ICM7228D

The common cathode digit and segment driver output schematics are shown in Figure 12. The N-channel digit drivers have an output impedance of approximately 15Ω. Each digit has a minimum of 50 mA drive capability. The segment drivers have an output impedance of approximately 100Ω with typically 10 mA peak current drive for each segment. The common cathode display driver output currents are only $\frac{1}{4}$ of the common anode display driver currents. Therefore, the ICM7228A and ICM7228C commn anode display drivers are recommended for those applications where high display brightness is desired. The ICM7228B and ICM7228D common cathode display drivers are suitable for driving bubble-lensed monolithic 7 segment displays. They can also drive individual LED displays up to 0.3" in height when high brightness is not required.

Display Multiplexing

Each digit of the ICM7228 is on for approximately 320 μs, with a multiplexing frequency of approximately 390 Hz. The ICM7228 display drivers provide interdigit blanking. This ensures that the segment information of the previous digit is gone and the information of the next digit is stable before the next digit is driven on. This is necessary to eliminate display ghosting (a faint display of data from previous digit superimposed on the next digit). The interdigit blanking time is 10 μs typical with a guaranteed 2 μs minimum. The ICM7228 turns off both the digit drivers and the segment drivers during the interdigit blanking period. The digit multiplexing sequence is: D2, D5, D1, D7, D8, D6, D4 and D3. A typical digit's drive pulses are shown on Figure 13.

Due to the display multiplexing, the driving duty cycle for each digit is 12% (100 $\times$ $\frac{1}{8}$). This means the average current for each segment is $\frac{1}{8}$ of its peak current. This must be considered while designing and selecting the displays.

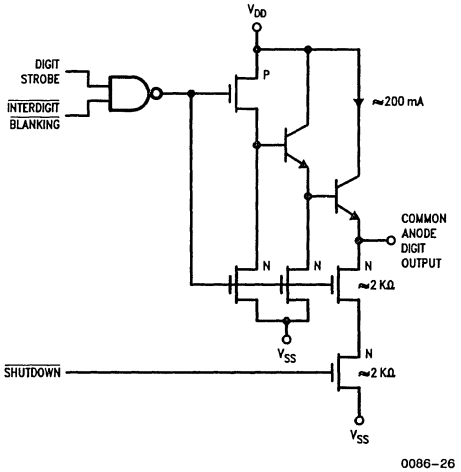
NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTIONS (Continued)

Driving Larger Displays

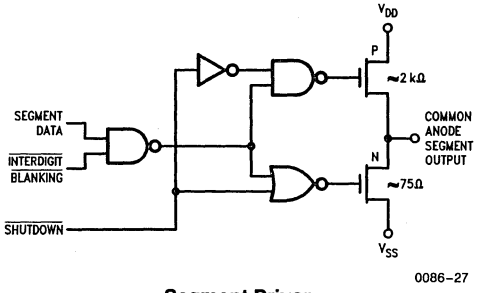
If very high display brightness is desired, the ICM7228 display driver outputs can be externally buffered. Figures 14 thru 16 show how to drive either common anode or common cathode displays using the ICM7228 and external driver circuit for higher current displays.

Another method of increasing display currents is to connect two digit outputs together and load the same data into both digits. This drives the display with the same peak current, but the average current doubles because each digit of the display is on for twice as long, i.e., ¼ duty cycle versus ⅛.



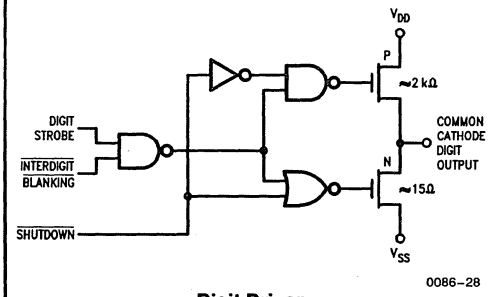
NOTE: When SHUTDOWN goes low INTERDIGIT BLANKING also stays low.

Digit Driver

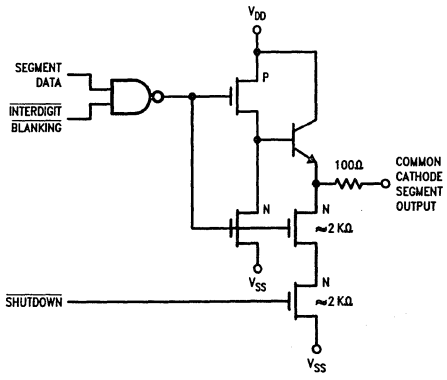


Segment Driver

Figure 11: Common Anode Display Drivers



Digit Driver



NOTE: When SHUTDOWN goes low INTERDIGIT BLANKING also stays low.

Segment Driver

Figure 12: Common Cathode Display Drivers

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTIONS (Continued)

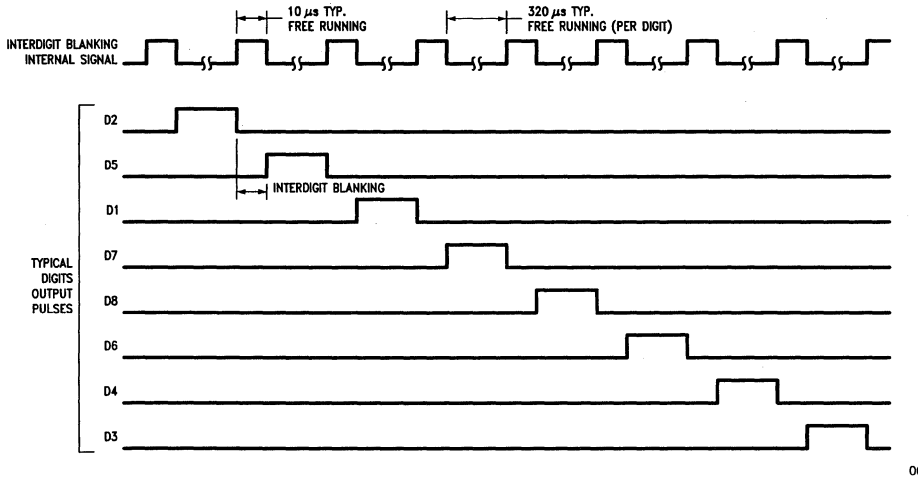


Figure 13: Display Digits Multiplex Timing Diagram (Common Anode Display)

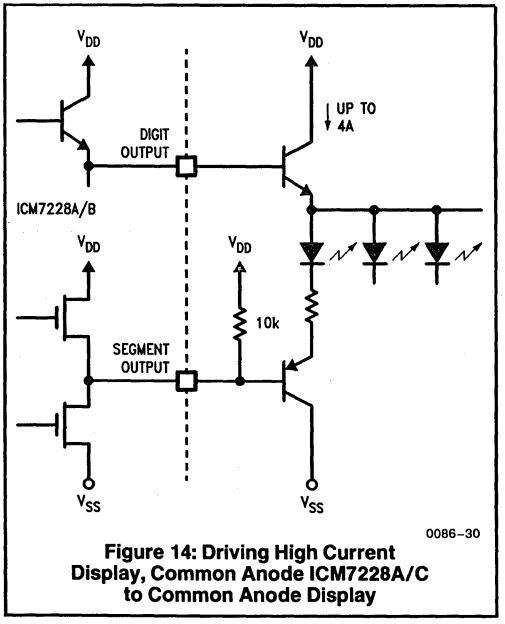


Figure 14: Driving High Current Display, Common Anode ICM7228A/C to Common Anode Display

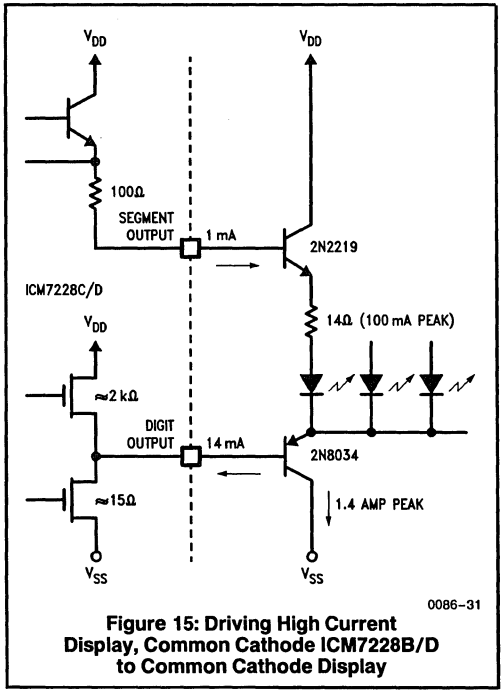


Figure 15: Driving High Current Display, Common Cathode ICM7228B/D to Common Cathode Display

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTIONS (Continued)

Three Level Input, ICM7228C and ICM7228D

As mentioned before, pin 9 is a three level input and controls three functions: Hexadecimal display decoding, Code B display decoding and shutdown mode. In many applications, pin 9 will be left open or permanently wired to one state. When pin 9 can not be permanently left in one state, the circuits illustrated in Figure 17 can be used to drive this three level input.

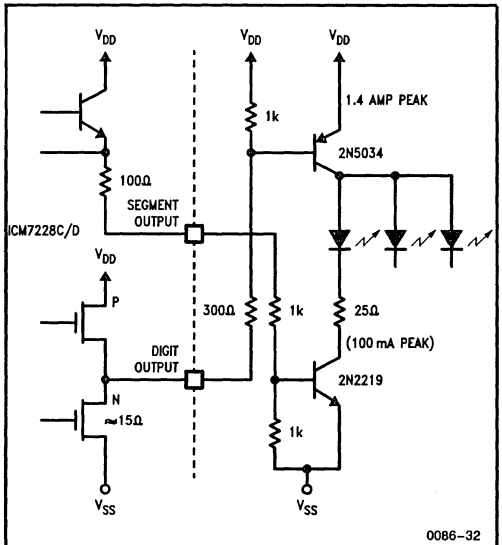


Figure 16: Driving High Current Display Common Cathode ICM7228B/D to Common Anode Display

Power Supply Bypassing

Connect a minimum of 47 μF in parallel with 0.1μF capacitors between V_{DD} and V_{SS} of ICM7228. These capacitors should be placed in close proximity to the device to reduce the power supply ripple caused by the multiplexed LED display drive current pulses.

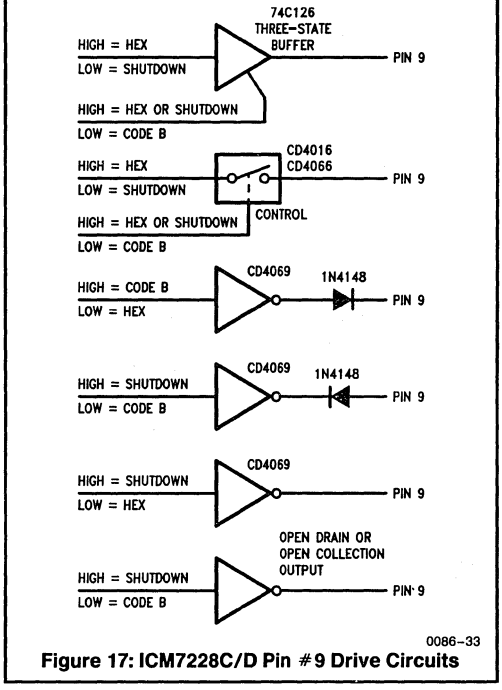


Figure 17: ICM7228C/D Pin #9 Drive Circuits

9

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICM7231-ICM7232
Numeric/Alphanumeric Triplexed LCD Display Driver

GENERAL DESCRIPTION

The ICM7231-7232 family of integrated circuits are designed to generate the voltage levels and switching waveforms required to drive triplexed liquid-crystal displays. These chips also include input buffer and digit address decoding circuitry allowing six bits of input data to be decoded into 64 independent combinations of the output segments of the selected digit.

The family is designed to interface to modern high performance microprocessors and microcomputers and ease system requirements for ROM space and CPU time needed to service a display.

FEATURES

- **ICM7231: Drives 8 Digits of 7 Segments With Two Independent Annunciators Per Digit Address and Data Input in Parallel Format**
- **ICM7232: Drives 10 Digits of 7 Segments With Two Independent Annunciators Per Digit Address and Data Input in Serial Format**
- **All Signals Required to Drive Rows and Columns of Triplexed LCD Display Are Provided**
- **Display Voltage Independent of Power Supply**
- **On-Chip Oscillator Provides All Display Timing**
- **Total Power Consumption Typically 200μW, Maximum 500μW at 5V**
- **Low-Power Shutdown Mode Retains Data With 5μW Typical Power Consumption at 5V, 1μW at 2V**
- **Direct Interface to High-Speed Microprocessors**

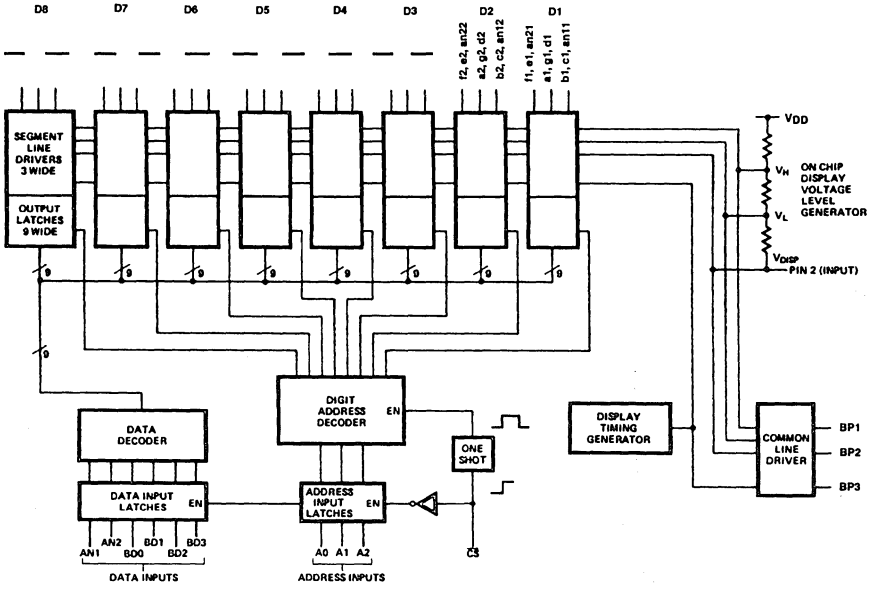
ORDERING INFORMATION

Part Number	Temperature Range	Package	Number of Digits	Input Format
ICM7231BFIPL	-25°C to +85°C	40 Pin Plastic DIP	8 Digit	Parallel
ICM7232AFIPL	-25°C to +85°C	40 Pin Plastic DIP	10 Digit	Serial
ICM7232BFIPL	-25°C to +85°C	40 Pin Plastic DIP	10 Digit	Serial
ICM7232CRIPL	-25°C to +85°C	40 Pin Plastic DIP	10 Digit	Serial

NOTE: All versions intended for triplexed LCD displays

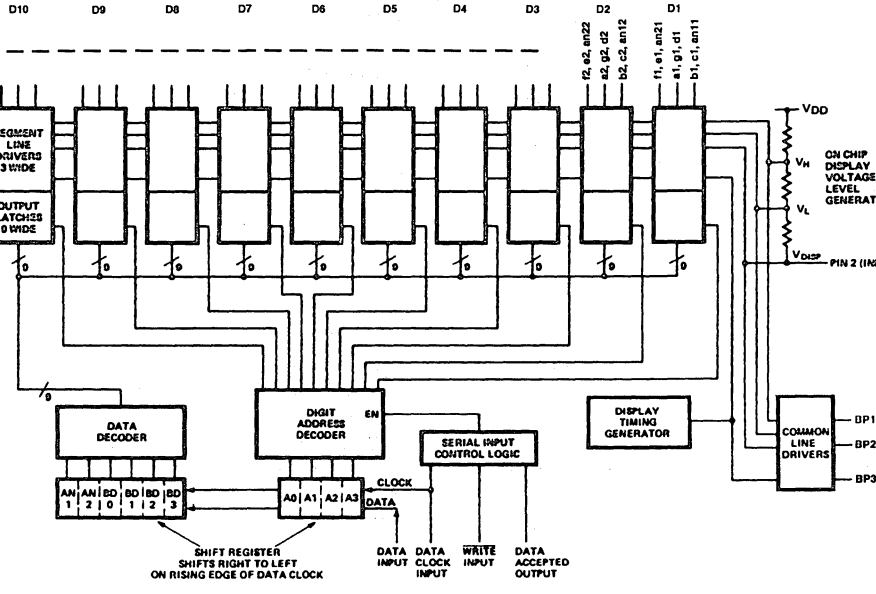
203299-003

NOTE: All typical values have been characterized but are not tested.



NOTE: See Figure 17 for display segment connections.

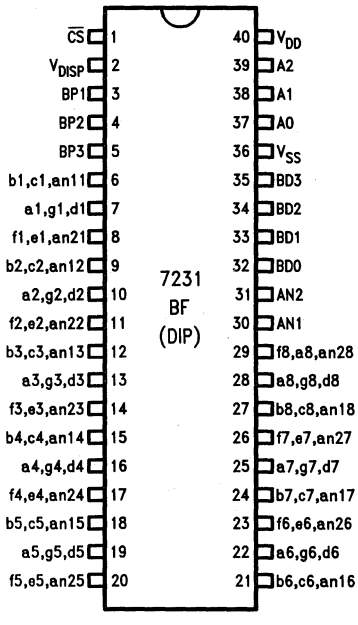
Figure 1: ICM7231 Functional Diagram



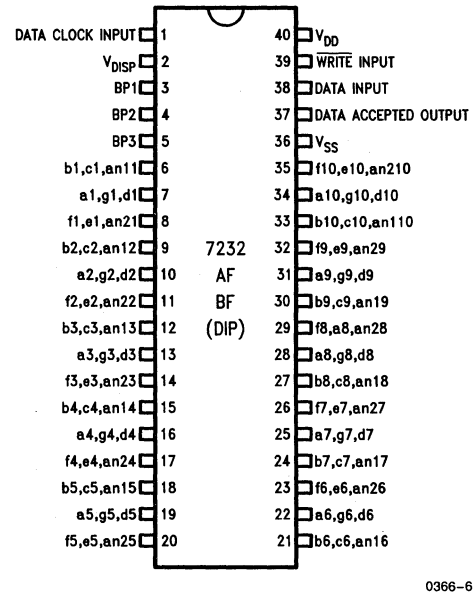
NOTE: See Figures 17 and 18 for display segment connections.

Figure 2: ICM7232 Functional Diagram

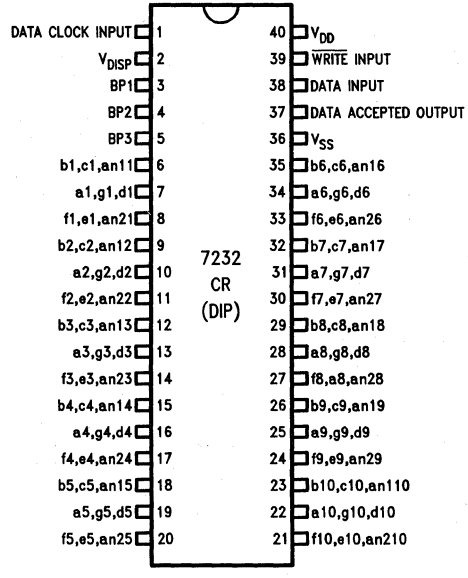
NOTE: All typical values have been characterized but are not tested.



0366-5



0366-6



0366-7

Figure 4: Pin Configuration (Outline dwg PL)

NOTE: All typical values have been characterized but are not tested.

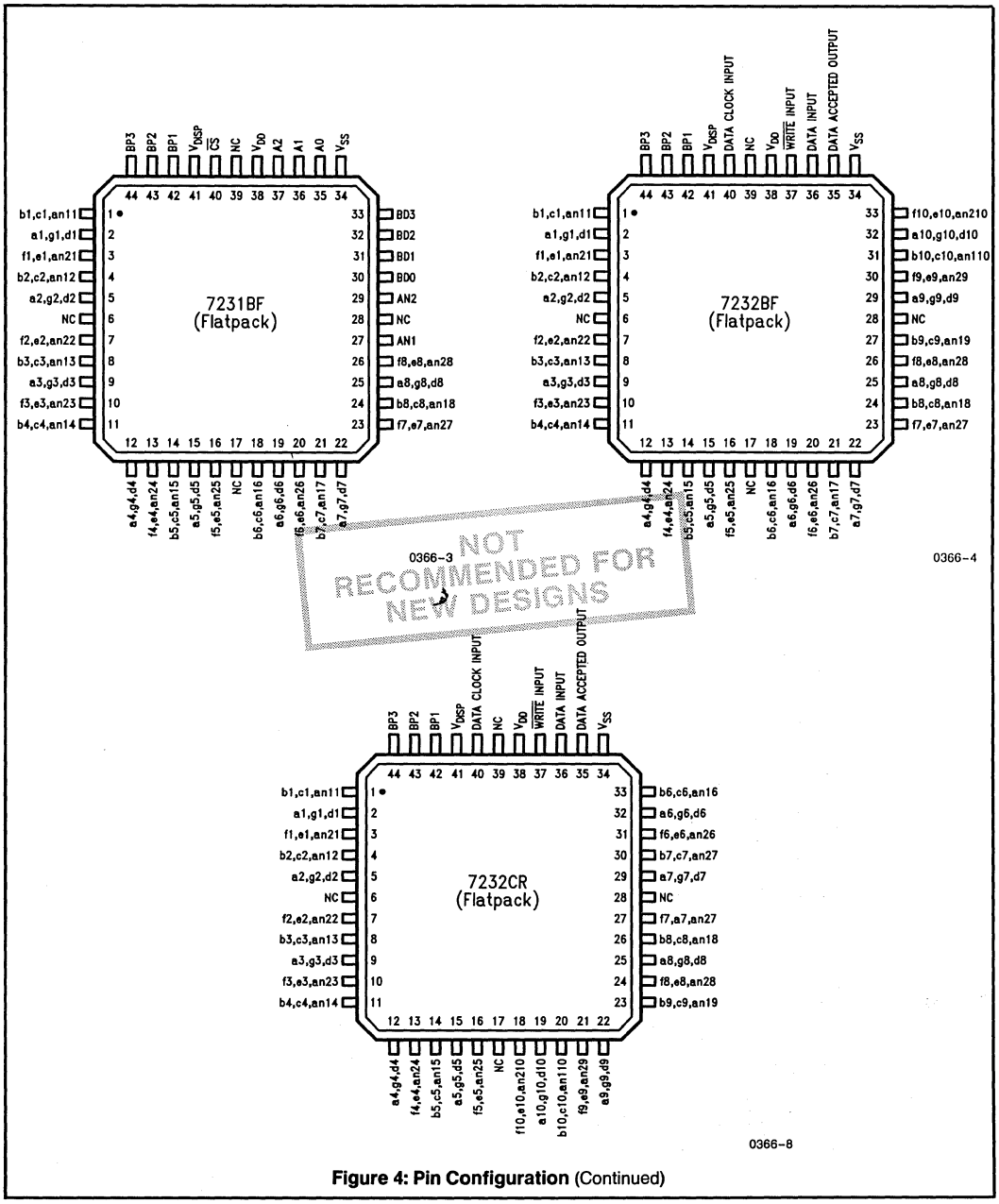


Figure 4: Pin Configuration (Continued)

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) 6.5V
Input Voltage[2] ..... $V_{SS} - 0.3 \le V_{IN} \le 6.5$
Display Voltage[2] ..... $-0.3 \le V_{DISP} \le +0.3$

Power Dissipation[1] ..... 0.5W @ 70°C
Operating Temperature Range ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

Notes: 1. This limit refers to that of the package and will not be obtained during normal operation.

2. Due to the SCR structure inherent in these devices, connecting any display terminal or the display voltage terminal to a voltage outside the power supply to the chip may cause destructive device latchup. The digital inputs should never be connected to a voltage less than −0.3 volts below ground, but may be connected to voltages above V_{DD} but not more than 6.5 volts above V_{SS}.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

($V^+ = 5V \pm 10\%$, $V_{SS} = 0V$, $T_A = -25°C$ to $+85°C$ unless otherwise specified)

Symbol	Parameter	Test Conditions/Description	Min	Typ	Max	Units
V_{DD}	Power Supply Voltage		4.5	>4	5.5	V
V_{DD}	Data Retention Supply Voltage	Guaranteed Retention at 2V	2	1.6		V
I_{DD}	Logic Supply Current	Current from V_{DD} to Ground excluding Display. $V_{DISP} = 2V$		30	100	µA
I_S	Shutdown Total Current	V_{DISP} Pin 2 Open		1	10	µA
V_{DISP}	Display Voltage Range	$V_{SS} \le V_{DISP} \le V_{DD}$	0		V_{DD}	V
I_{DISP}	Display Voltage Setup Current	$V_{DISP} = 2V$ Current from V_{DD} to V_{DISP} On-Chip		15	30	µA
R_{DISP}	Display Voltage Setup Resistor Value	One of Three Identical Resistors in String	40	75		kΩ
	DC Component of Display Signals	(Sample Test only)		¼	1	% ($V_{DD} - V_{DISP}$)
f_{DISP}	Display Frame Rate	See Figure 6	60	90	120	Hz
V_{IL}	Input Low Level	ICM7231 Pins 30-35, 37-39, 1			0.8	V
V_{IH}	Input High Level		2.0			V
I_{ILK}	Input Leakage	ICM7232, Pins 1, 38, 39 (Note 1)		0.1	1	µA
C_{IN}	Input Capacitance			5		pF
V_{OL}	Output Low Level	Pin 37, ICM7232, $I_{OL} = 1mA$,			0.4	V
V_{OH}	Output High Level	$V_{DD} = 4.5V$, $I_{OH} = -500\mu A$	4.1			V
T_{OP}	Operating Temperature Range	Industrial Range	−25		+85	°C

AC CHARACTERISTICS

($V_{DD} = 5V \pm 10\%$ $V_{SS} = 0V$, $-20°C \le T_A \le +85°C$)

PARALLEL INPUT (ICM7231) See Figure 14

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{cs}	$\overline{\text{Chip Select}}$ Pulse Width	(Note 1)	500	350		ns
t_{ds}	Address/Data Setup Time	(Note 1)	200			ns
t_{dh}	Address/Data Hold Time	(Note 1)	0	−20		ns
t_{ics}	Inter-Chip Select Time	(Note 1)	3			µs

SERIAL INPUT (ICM7232) See Figures 15, 16

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$t_{\overline{cl}}$	Data Clock Low Time	(Note 1)	350			ns
t_{cl}	Data Clock High Time	(Note 1)	350			ns
t_{ds}	Data Setup Time	(Note 1)	200			ns
t_{dh}	Data Hold Time	(Note 1)	0	−20		ns
t_{wp}	$\overline{\text{Write}}$ Pulse Width	(Note 1)	500	350		ns
t_{wil}	$\overline{\text{Write}}$ Pulse to Clock at Initialization	(Note 1)	1.5			µs
t_{odl}	Data Accepted Low Output Delay	(Note 1)		200	400	ns
t_{odh}	Data Accepted High Output Delay	(Note 1)		1.5	3	µs
t_{cws}	Write Delay After Last Clock	(Note 1)	350			ns

NOTE 1: For design reference only, not 100% tested.

NOTE: All typical values have been characterized but are not tested.

TABLE OF FEATURES

Type Number	Output Code	Annunciator Locations	Input	Output
ICM7231BF	Code B	Both Annunciators on BP3	Parallel Entry 4 bit Data 2 bit Annunciators 3 bit Address	8 Digits plus 16 Annunciators
ICM7232AF	Hexadecimal	Both Annunciators on BP3	Serial Entry 4 bit Data 2 bit Annunciators 4 bit Address	10 Digits plus 20 Annunciators
ICM7232BF	Code B			
ICM7232CR	Code B	1 Annunciator BP1 1 Annunciator BP3		

TERMINAL DEFINITIONS

ICM7231 PARALLEL INPUT NUMERIC DISPLAY

Terminal	Pin No.	Description	Function	
AN1 AN2	30 31	Annunciator 1 Control Bit Annunciator 2 Control Bit	High = ON Low = OFF	See Table 3
BD0 BD1 BD2 BD3	32 33 34 35	Least Significant Most Significant 4 Bit Binary Data Inputs	Input Data (See Table 1)	HIGH = Logical One (1) LOW = Logical Zero (0)
A0 A1 A2	37 38 39	Least Significant Most Significant 3 Bit Digit Address Inputs	Input Address (See Table 2)	
$\overline{CS}$	1	Data Input Strobe/Chip Select (Note 3)	Trailing (Positive going) edge latches data, causes data input to be decoded and sent out to addressed digit	

NOTE: 3. $\overline{CS}$ has a special "mid-level" sense circuit that establishes a **test** mode if it is held near 3V for several msec. Inadvertent triggering of this mode can be avoided by pulling it high when inactive, or ensuring frequent activity.

ICM7232 SERIAL DATA AND ADDRESS INPUT

Terminal	Pin No.	Description	Function
Data Input	38	Data + Address Shift Register Input	HIGH = Logical One (1) LOW = Logical Zero (0)
$\overline{WRITE}$ Input	39	Decode, Output, and Reset Strobe	When DATA ACCEPTED Output is LOW, positive going edge of WRITE causes data in shift register to be decoded and sent to addressed digit, then shift register and control logic to be reset. When DATA ACCEPTED Output is HIGH, positive going edge of $\overline{WRITE}$ triggers reset only.
Data Clock Input	1	Data Shift Register and Control Logic Clock	Positive going edge advances data in shift register. ICM7232: Eleventh edge resets shift register and control logic.
DATA ACCEPTED Output	37	Handshake Output	Output LOW when correct number of bits entered into shift register; ICM7232 8, 9 or 10 bits

NOTE: All typical values have been characterized but are not tested.

ALL DEVICES

Terminal	Pin No.	Description	Function
Display Voltage V_{DISP}	2	Negative end of on-chip resistor string used to generate intermediate voltage levels for display. Shutdown Input.	Display voltage control. When open (or less than 1V from V_{DD} chip is shutdown; oscillator stops, all display pins to V_{DD}.
Common Line Driver Outputs	3,4,5		Drive display commons, or rows.
Segment Line Driver Outputs	6–29 6–35	(On ICM7231) (On ICM7232)	Drive display segments, or columns.
V_{DD}	40	Chip Positive Supply	
V_{SS}	36	Chip Negative Supply	

ICM7231 FAMILY DESCRIPTION

The ICM7231 drives displays with 8 seven-segment digits with two independent annunciators per digit, accepting six data bits and three digit address bits from parallel inputs controlled by a chip select input. The data bits are subdivided into four binary code bits and two annunciator control bits.

The ICM7232 drives 10 seven-segment digits with two independent annunciators per digit. To write into the display, six bits of data and four bits of digit address are clocked serially into a shift register, then decoded and written to the display.

Input levels are TTL compatible, and the DATA ACCEPTED output on the serial input devices will drive one LSTTL load. The intermediate voltage levels necessary to drive the display properly are generated by an on-chip resistor string, and the output of a totally self-contained on-chip oscillator is used to generate all display timing. All devices in this family have been fabricated using Harris' MAXCMOS® process and all inputs are protected against static discharge.

TRIPLEXED (1/3 MULTIPLEXED) LIQUID CRYSTAL DISPLAYS

Figure 5 shows the connection diagram for a typical 7-segment display with two annunciators such as would be used with an ICM7231 or ICM7232 numeric display driver. Figure 6 shows the voltage waveforms of the common lines and one segment line, chosen for this example to be the "a, g, d" segment line. This line intersects with BP1 to form the "a" segment, BP2 to form the "g" segment and BP3 to form the "d" segment. Figure 6 also shows the waveform of the "a, g, d" segment line for four different ON/OFF combinations of the "a", "g" and "d" segments. Each intersection (segment or annunciator) acts as a capacitance from segment line to common line, shown schematically in Figure 7. Figure 8 shows the voltage across the "g" segment for the same four combinations of ON/OFF segments used in Figure 6.

The degree of polarization of the liquid crystal material and thus the contrast of any intersection depends on the RMS voltage across the intersection capacitance. Note from Figure 8 that the RMS OFF voltage is always $V_P/3$ and that the RMS ON voltage is always 1.92 $V_P/3$.

For a 1/3 multiplexed LCD, the ratio of RMS ON to OFF voltages is fixed at 1.92, achieving adequate display contrast with this ratio of applied RMS voltage makes some demands on the liquid crystal material used.

Figure 9 shows the curve of contrast versus applied RMS voltage for a liquid crystal material tailored for $V_P = 3.1V$, a typical value for 1/3-multiplexed displays in calculators. Note that the RMS OFF voltage $V_P/3 \approx 1V$ is just below the "threshold" voltage where contrast begins to increase. This places the RMS ON voltage at 2.1V, which provides about 85% contrast when viewed straight on.

All members of the ICM7231/ICM7232 family use an internal resistor string of three equal value resistors to generate the voltages used to drive the display. One end of the string is connected on the chip to V_{DD} and the other end (user input) is available at pin 2 (V_{DISP}) on each chip. This allows the display voltage input (V_{DISP}) to be optimized for the particular liquid crystal material used. Remember that $V_P = V_{DD} - V_{DISP}$ and should be three times the threshold voltage of the liquid crystal material used. Also it is very important that pin 2 never be driven below V_{SS}. This can cause device latchup and destruction of the chip.

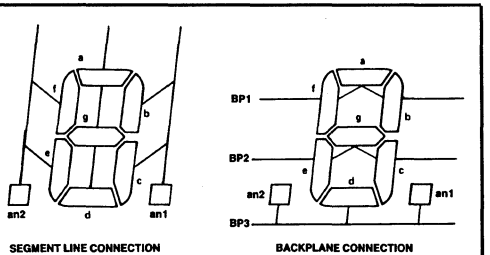
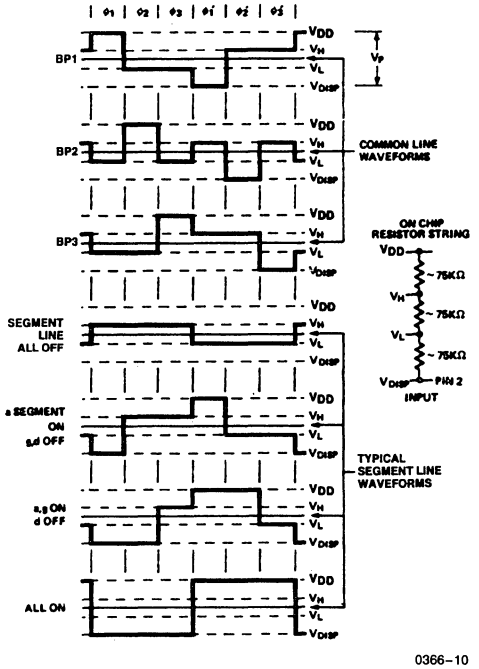


Figure 5: Connection Diagrams for Typical 7-Segment Displays

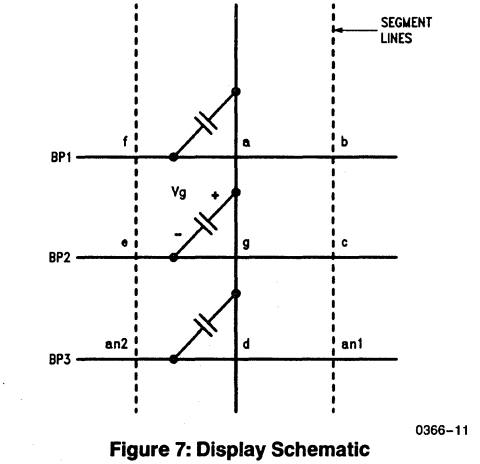
NOTE: All typical values have been characterized but are not tested.



0366-10

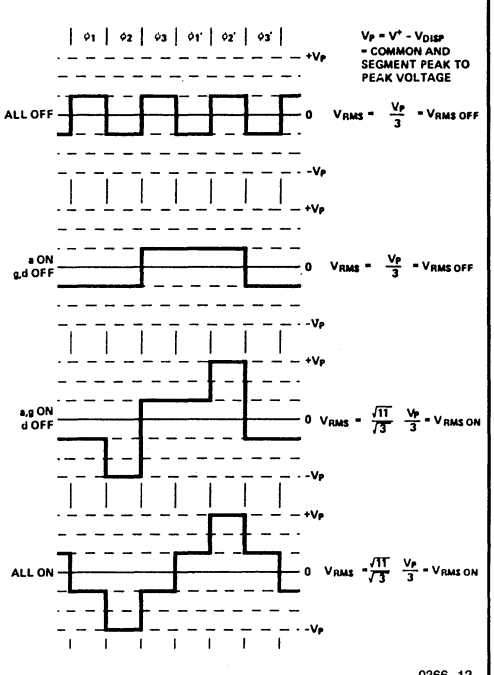
Figure 6: Display Voltage Waveforms

NOTE: ϕ_1, ϕ_2, ϕ_3 — BP HIGH WITH RESPECT TO SEGMENT.
$\phi_{1'}$, $\phi_{2'}$, $\phi_{3'}$ — BP LOW WITH RESPECT TO SEGMENT.
BP1 ACTIVE DURING ϕ_1 AND $\phi_{1'}$
BP2 ACTIVE DURING ϕ_2 AND $\phi_{2'}$
BP3 ACTIVE DURING ϕ_3 AND $\phi_{3'}$



0366-11

Figure 7: Display Schematic



0366-12

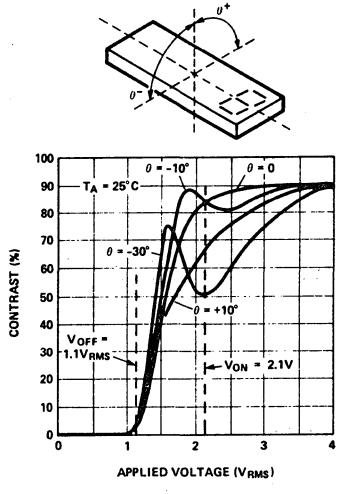
Figure 8: Voltage Waveforms on Segment g(V_g)

$$\text{VOLTAGE CONTRAST RATIO} = \frac{V_{RMS}\ ON}{V_{RMS}\ OFF} = \frac{\sqrt{11}}{\sqrt{3}} = 1.92$$

NOTE: ϕ_1, ϕ_2, ϕ_3 – BP HIGH WITH RESPECT TO SEGMENT.
$\phi_{1'}$, $\phi_{2'}$, $\phi_{3'}$ – BP LOW WITH RESPECT TO SEGMENT.
BP1 ACTIVE DURING ϕ_1 AND $\phi_{1'}$
BP2 ACTIVE DURING ϕ_2 AND $\phi_{2'}$
BP3 ACTIVE DURING ϕ_3 AND $\phi_{3'}$

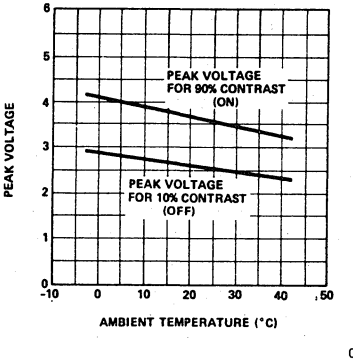
9

NOTE: All typical values have been characterized but are not tested.



0366-13

Figure 9: Contrast vs. Applied RMS Voltage



0366-14

Figure 10: Temperature Dependence of LC Threshold

TEMPERATURE EFFECTS AND TEMPERATURE COMPENSATION

The performance of the LCD material is affected by temperature in two ways. The response time of the display to changes of applied RMS voltage gets longer as the display temperature drops. At very low temperatures (−20°C) some displays may take several seconds to change a new character after the new information appears at the outputs. However, for most applications above 0°C this will not be a problem with available multiplexed LCD materials, and for low-temperature applications, high-speed liquid crystal materials are available. On high temperature, effect to consider deals with plastic materials used to make the polarizer. Some polarizers become soft at high temperatures and permanently lose their polarizing ability, thereby seriously degrading display contrast. Some displays also use sealing materials unsuitable for high temperature use. Thus, when specifying displays the following must be kept in mind: liquid crystal material, polarizer, and seal materials.

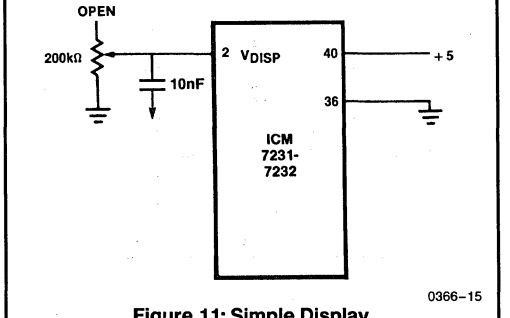
A more important effect of temperature is the variation of threshold voltage. For typical liquid crystal materials suitable for multiplexing, the peak voltage has a temperature coefficient of −7 to −14 mV/°C. This means that as temperature rises, the threshold voltage goes down. Assuming a fixed value for V_P, when the threshold voltage drops below $V_P/3$ OFF segments begin to be visible. Figure 10 shows the temperature dependence of peak voltage for the same liquid crystal material of Figure 9.

For applications where the display temperature does not vary widely, V_P may be set at a fixed voltage chosen to make the RMS OFF voltage, $V_P/3$, just below the threshold voltage at the highest temperature expected. This will prevent OFF segments turning ON at high temperature (this at the cost of reduced contrast for ON segments at low temperatures).

For applications where the display temperature may vary to wider extremes, the display voltage V_{DISP} (and thus V_P) may require temperature compensation to maintain sufficient contrast without OFF segments becoming visible.

DISPLAY VOLTAGE AND TEMPERATURE COMPENSATION

These circuits allow control of the display peak voltage by bringing the bottom of the voltage divider resistor string out at pin 2. The simplest means for generating a display voltage suitable to a particular display is to connect a potentiometer from pin 2 to V_{SS} as shown in Figure 11. A potentiometer with a maximum value of 200 kΩ should give sufficient range of adjustment to suit most displays. This method for generating display voltage should be used only in applications where the temperature of the chip and display won't vary more than ±5°C (±9°F), as the resistors on the chip have a positive temperature coefficient, which will tend to increase the display peak voltage with an increase in temperature. The display voltage also depends on the power supply voltage, leading to tighter tolerances for wider temperature ranges.



0366-15

Figure 11: Simple Display Voltage Adjustment

NOTE: All typical values have been characterized but are not tested.

Figure 12(a) shows another method of setting up a display voltage using five silicon diodes in series. These diodes, 1N914 or equivalent, will each have a forward drop of approximately 0.65V, with approximately 20μA flowing through them at room temperature. Thus, 5 diodes will give 3.25V, suitable for a 3V display using the material properties shown in Figures 9 and 10. For higher voltage displays, more diodes may be added. This circuit provides reasonable temperature compensation, as each diode has a negative temperature coefficient of −2 mV/°C; five in series gives −10 mV/°C, not far from optimum for the material described.

The disadvantage of the diodes in series is that only integral multiples of the diode voltage can be achieved. The diode voltage multiplier circuit shown in Figure 12(b) allows fine-tuning the display voltage by means of the potentiometer; it likewise provides temperature compensation since the temperature coefficient of the transistor base-emitter junction (about −2 mV/°C) is also multipled. The transistor should have a beta of at least 100 with a collector current of 10 μA. The inexpensive 2N2222 shown in the figure is a suitable device.

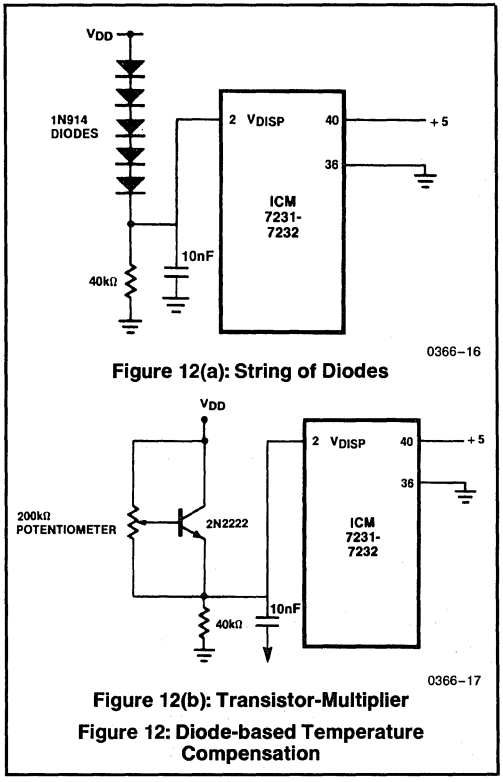


Figure 12(a): String of Diodes

Figure 12(b): Transistor-Multiplier

Figure 12: Diode-based Temperature Compensation

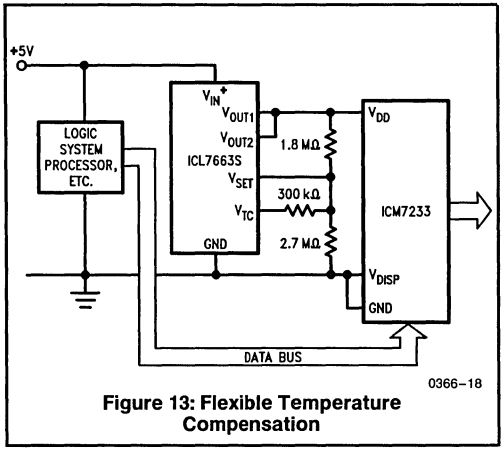


Figure 13: Flexible Temperature Compensation

NOTE: All typical values have been characterized but are not tested.

ICM7231-ICM7232

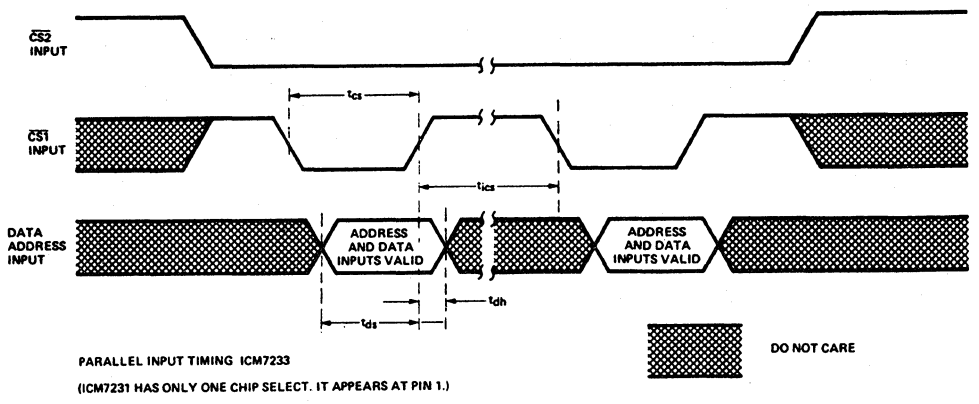


Figure 14: Parallel Input Timing

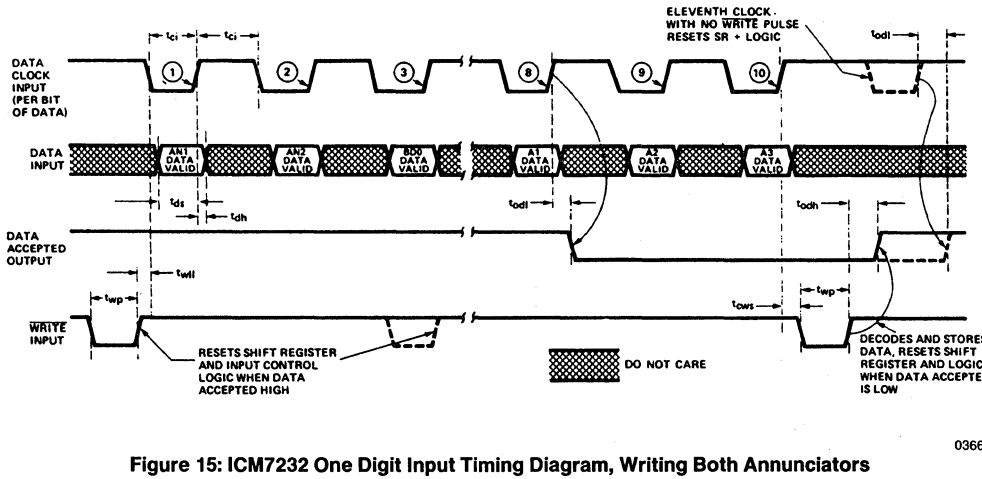


Figure 15: ICM7232 One Digit Input Timing Diagram, Writing Both Annunciators

For battery operation, where the display voltage is generally the same as the battery voltage (usually 3-4.5V), the chip may be operated at the display voltage, with V_{DISP} connected to V_{SS}. The inputs of the chip are designed such that they may be driven above V_{DD} without damaging the chip. This allows, for example, the chip and display to operate at a regulated 3V, and a microprocessor driving its inputs to operate with a less well controlled 5V supply. (The inputs should not be driven more than 6.5V above GND under any circumstances.) This also allows temperature compensation with the ICL76635, as shown in Figure 13. This circuit allows independent adjustment of both voltage and temperature compensation.

DESCRIPTION OF OPERATION

PARALLEL INPUT OF DATA AND ADDRESS (ICM7231)

The parallel input structure of the ICM7231 device is organized to allow simple, direct interfacing to all microprocessors, (see functional diagram Figure 1). In the ICM7231, address and data bits are written into the input latches on the rising edge of the Chip Select input.

NOTE: All typical values have been characterized but are not tested.

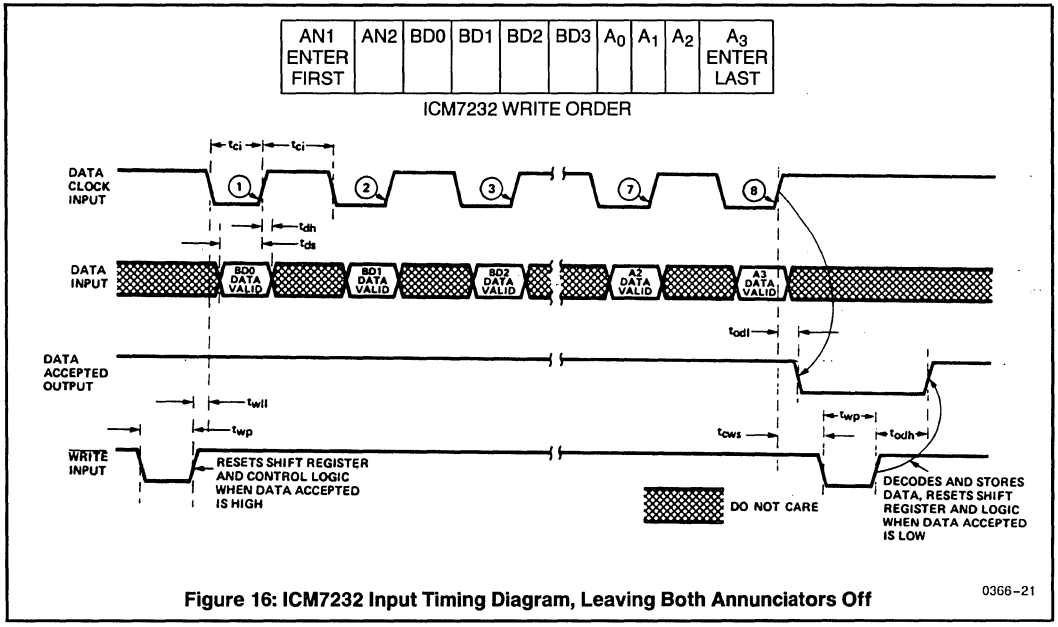


Figure 16: ICM7232 Input Timing Diagram, Leaving Both Annunciators Off

The rising edge of the Chip Select also triggers an on-chip pulse which enables the address decoder and latches the decoded data into the addressed digit/character outputs. The timing requirements for the parallel input device are shown in Figure 14, with the values for setup, hold, and pulse width times shown in the AC Characteristics section. Note that there is a minimum time between Chip Select pulses; this is to allow sufficient time for the on-chip enable pulse to decay, and ensures that new data doesn't appear at the decoder inputs before the decoded data is written to the outputs.

SERIAL INPUT OF DATA AND ADDRESS (ICM7232)

The ICM7232 trades six pins used as data inputs on the ICM7231 for six more segment lines, allowing two more 9-segment digits. This is done at the cost of ease in interfacing, and requires that data and address information be entered serially. Refer to functional diagram, Figure 2 and timing diagrams, Figures 15 and 16. The interface consists of four pins: DATA Input, DATA CLOCK Input, $\overline{\text{WRITE}}$ Input and DATA ACCEPTED Output. The data present at the DATA Input is clocked into a shift register on the rising edge of the DATA CLOCK Input signal, and when the correct number of bits has been shifted into the shift register (8 in the ICM7232), the DATA ACCEPTED Output goes low. Following this, a low-going pulse at the $\overline{\text{WRITE}}$ input will trigger the chip to decode the data and store it in the output latches of the addressed digit/character. After the data is latched at the outputs, the shift register and the control logic are reset, returning the DATA ACCEPTED Output high. After this occurs, a pulse at the $\overline{\text{WRITE}}$ input will not change the outputs, but will reset the control logic and shift register, assuring that each data bit will be entered into the correct position in the shift register depending on subsequent DATA CLOCK inputs.

The shift register and control logic will also be reset if too many DATA CLOCK INPUT edges are received; this prevents incorrect data from being decoded. In the ICM7232, the eleventh clock resets the shift register and control logic.

The recommended procedure for entering data is shown in the serial input timing diagram, Figure 15. First, when DATA ACCEPTED is high, send a $\overline{\text{WRITE}}$ pulse. This resets the shift register and control logic and initializes the chip for the data input sequence. Next clock in the appropriate number of correct data and address bits. The DATA ACCEPTED Output may be monitored if desired, to determine when the chip is ready to output the decoded data. When the correct number of bits has been entered, and the DATA ACCEPTED Output is low, a pulse at $\overline{\text{WRITE}}$ will cause the data to be decoded and stored in the latches of the addressed digit/character. The shift register and control logic are reset, causing DATA ACCEPTED to return high, and leaving the chip ready to accept data for the next digit/character.

Note that for the ICM7232 the eleventh clock resets the shift register and control logic, but the DATA ACCEPTED Output goes low after the eighth clock. This allows the user to abbreviate the data to eight bits, which will write the correct character to the 7-segment display, but will leave the annunciators off, as shown in Figure 16.

If only AN2 is to be turned on, nine bits are clocked in; if AN1 is to be turned on, all ten bits are used.

NOTE: All typical values have been characterized but are not tested.

The DATA ACCEPTED Output will drive one low-power Schottky TTL input, and has equal current drive capability pulling high or low.

Note that in the serial input devices, it is possible to address digits/characters which don't exist. As shown in Tables 2 and 5, when an incorrect address is applied together with a $\overline{\text{WRITE}}$ pulse, none of the outputs will be changed.

DISPLAY FONTS AND OUTPUT CODES

The standard versions of the ICM7231 and ICM7232 chips are programmed to drive a 7-segment display plus two annunciators per digit. See Table 3 for annunciator input controls.

The "A" and "B" suffix chips place both annunciators on BP3. The display connections for one digit of this display are shown in Figure 17. The "A" devices decode the input data into a hexadecimal 7-segment output, while the "B" devices supply Code B outputs (see Table 1).

The "C" devices place the left hand annunciator on BP1 and the right hand annunciator (usually a decimal point) on BP3. (See Figure 18). The "C" devices provide only a "Code B" output for the 7-segments.

TABLE 1. BINARY DATA DECODING (ICM7231/32)

CODE INPUT				DISPLAY OUTPUT	
BD 3	BD 2	BD 1	BD 0	HEX	CODE B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	BLANK

0366-23

TABLE 2. ADDRESS DECODING (ICM7231/32)

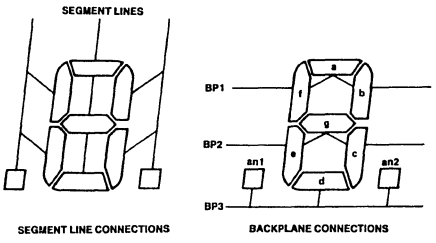
Code Input				Display Output
ICM7232 Only A3	A2	A1	A0	Digit Selected
0	0	0	0	D1
0	0	0	1	D2
0	0	1	0	D3
0	0	1	1	D4
0	1	0	0	D5
0	1	0	1	D6
0	1	1	0	D7
0	1	1	1	D8
1	0	0	0	D9
1	0	0	1	D10
1	0	1	0	NONE
1	0	1	1	NONE
1	1	0	0	NONE
1	1	0	1	NONE
1	1	1	0	NONE
1	1	1	1	NONE

TABLE 3. ANNUNCIATOR DECODING

CODE INPUT		DISPLAY OUTPUT	
AN 2	AN 1	ICM7231 A/B ICM7232 A/B BOTH ANNUNCIATORS ON BP3	ICM7231C ICM7232C an2 ANNUNCIATOR BP1 an1 ANNUNCIATOR BP3
0	0	8	8
0	1	8	8
1	0	8	8
1	1	8	8

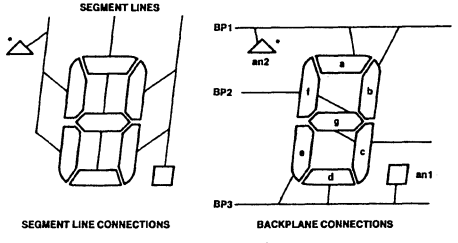
0366-24

NOTE: All typical values have been characterized but are not tested.



0366-25

Figure 17: ICM7231 and ICM7232 Display Fonts ("A" and "B" Suffix Versions)



*ANNUNCIATORS CAN BE: STOP, GO, △, ↑ - ARROWS THAT POINT TO INFORMATION PRINTED AROUND THE DISPLAY OPENING, ETC., WHATEVER THE DESIGNER CHOOSES TO INCORPORATE IN THE LIQUID CRYSTAL DISPLAY.

0366-26

Figure 18: ICM7231 Display Fonts ("C" Suffix Versions)

COMPATIBLE DISPLAYS

Compatible displays are manufactured by:

G.E. Displays Inc., Beechwood, Ohio (216)831-8100 (#356E3R99HJ)

Epson America Inc., Torrance CA (Model Numbers LDB726/7/8).

Seiko Instruments USA Inc., Torrance CA (Custom Displays)

Crystaloid, Hudson, OH

9

NOTE: All typical values have been characterized but are not tested.

APPLICATIONS

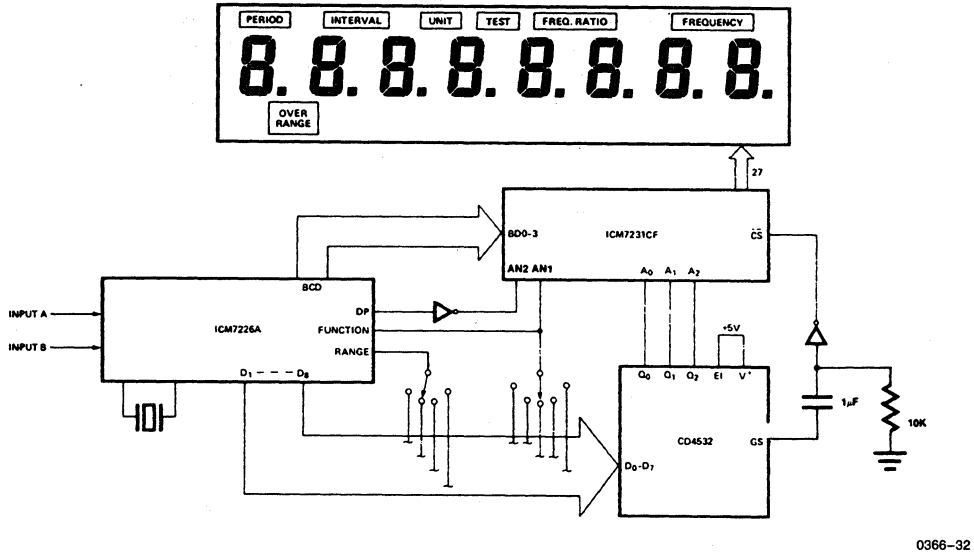


Figure 23: 10MHz Frequency/Period Pointer with LCD Display.
The annunciators show function and the decimal points indicate the range of the current operation. The system can be efficiently battery operated.

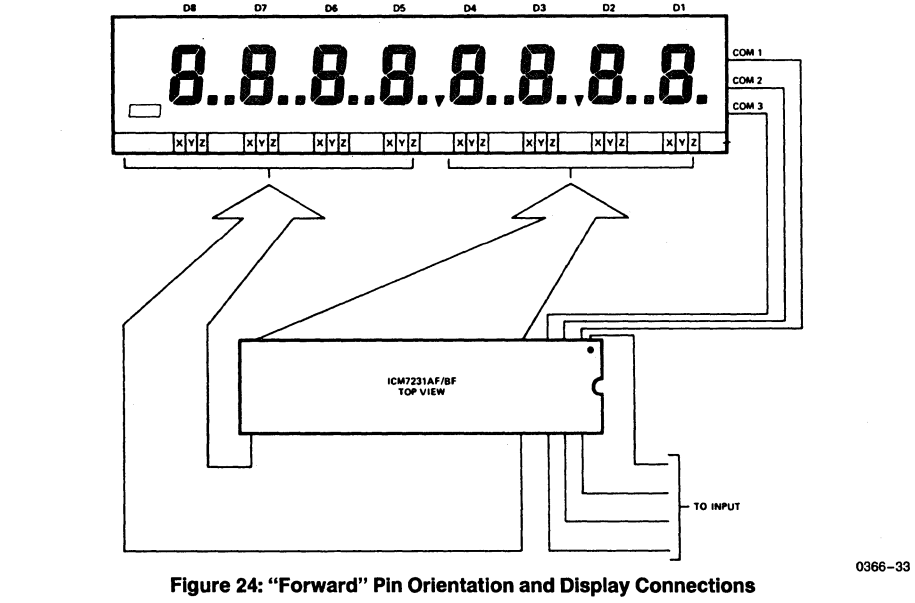


Figure 24: "Forward" Pin Orientation and Display Connections

NOTE: All typical values have been characterized but are not tested.

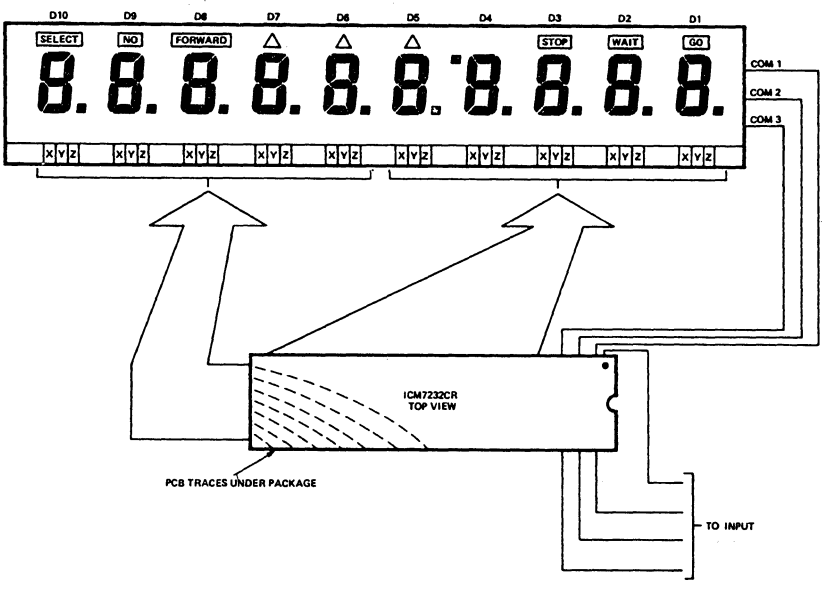


Figure 25: "Reverse" Pin Orientation and Display Connections

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICM7243
8-Character μP-Compatible LED Display Decoder Driver

GENERAL DESCRIPTION

The ICM7243 is an 8-character alphanumeric display driver and controller which provides all the circuitry required to interface a microprocessor or digital system to a 14- or 16-segment display. It is primarily intended for use in microprocessor systems, where it minimizes hardware and software overhead. Incorporated on-chip are a 64-character ASCII decoder, 8×6 memory, high power character and segment drivers, and the multiplex scan circuitry.

Six-bit ASCII data to be displayed is written into the memory directly from the microprocessor data bus. Data location depends upon the selection of either **Sequential** (MODE=1) or **Random** access mode (MODE=0). In the **Sequential Access** mode the first entry is stored in the lowest location and displayed in the "left-most" character position. Each subsequent entry is automatically stored in the next higher location and displayed to the immediate "right" of the previous entry. A DISPlay FULL signal is provided after 8 entries; this signal can be used for cascading devices together. A CLeaR pin is provided to clear the memory and reset the location counter. The **Random Access** mode allows the processor to select the memory address and display digit for each input word.

The character multiplex scan runs whenever data is not being entered. It scans the memory and CHARacter drivers, and ensures that the decoding from memory to display is done in the proper sequence. Intercharacter blanking is provided to avoid display ghosting.

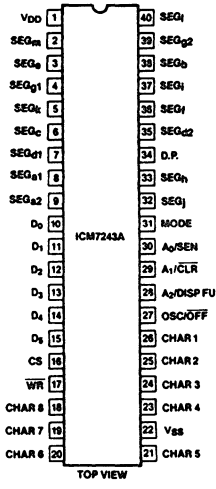
FEATURES

- **14- and 16-Segment Fonts With Decimal Point**
- **Mask Programmable For Other Font-Sets Up to 64 Characters**
- **Microprocessor Compatible**
- **Directly Drives LED Common Cathode Displays**
- **Cascadable Without Additional Hardware**
- **Standby Feature Turns Display Off; Puts Chip in Low Power Mode**
- **Sequential Entry or Random Entry of Data Into Display**
- **Single +5V Operation**
- **Character and Segment Drivers, All MUX Scan Circuitry, 8×6 Static Memory and 64-Character ASCII Font Generator Included On-Chip**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7243AIPL	−20°C to +85°C	40 Pin PLASTIC
ICM7243BIPL	−20°C to +85°C	40 Pin PLASTIC

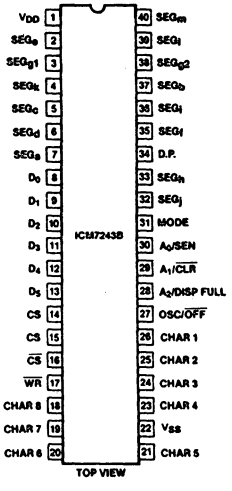
16-Segment Character



0368-1

Common Cathode Display Driver

14-Segment Character



0368-2

Common Cathode Display Driver

Figure 1: Pin Configurations

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD}-V_{SS}$) 6V
CHARacter Output Current 300mA
SEGment Output Current 30mA
Input Voltage (Any Terminal) .. ($V_{DD}+0.3V$) to ($V_{SS}-0.3V$)
Power Dissipation 1W

Operating Temperature Range..... −25°C to +85°C
Storage Temperature Range ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

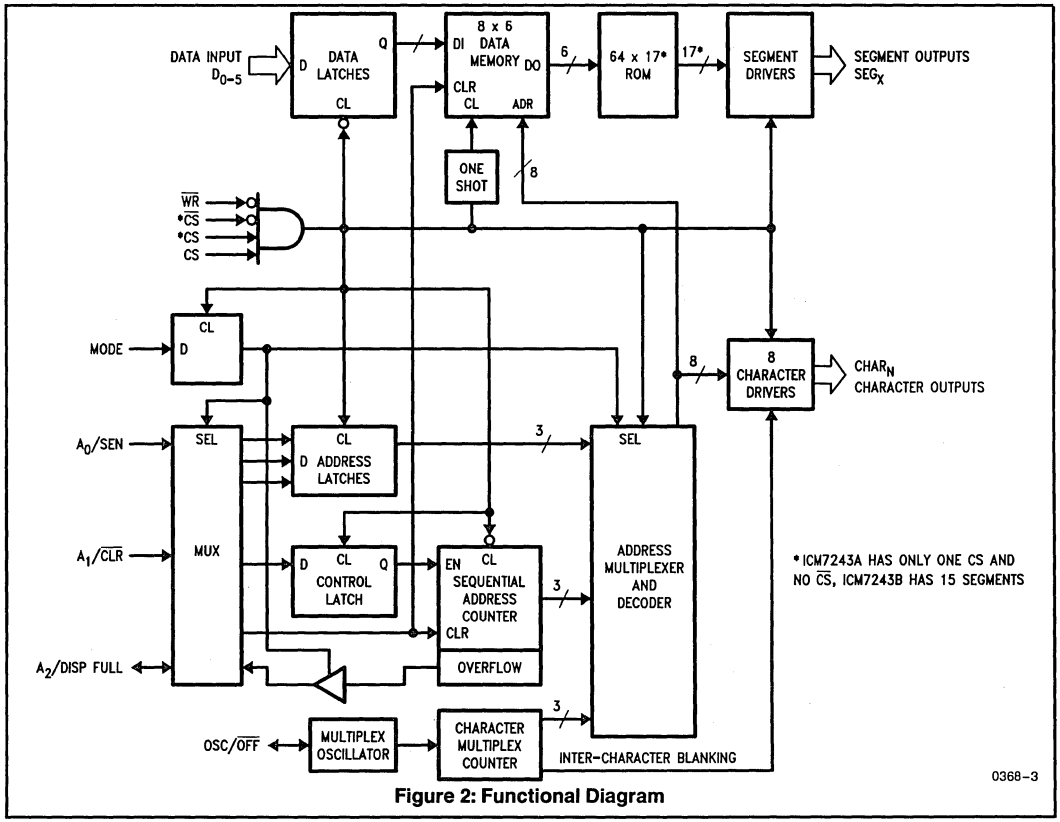


Figure 2: Functional Diagram

DC ELECTRICAL CHARACTERISTICS ($V_{DD}=5V$, $V_{SS}=0V$, $T_A=25°C$ unless otherwise stated)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
V_{SUPP}	Supply Voltage ($V_{DD}-V_{SS}$)		4.75	5.0	5.25	V
I_{DD}	Operating Supply Current	$V_{SUPP}=5.25V$, 10 Segments ON, All 8 Characters		180		mA
I_{STBY}	Quiescent Supply Current	$V_{SUPP}=5.25V$, OSC/$\overline{OFF}$ Pin<0.5V, CS=V_{SS}		30	250	µA
V_{IH}	Input High Voltage		2			V
V_{IL}	Input Low Voltage				0.8	V
I_{IN}	Input Current		−10		+10	µA

NOTE: All typical values have been characterized but are not tested.

DC ELECTRICAL CHARACTERISTICS ($V_{DD}=5V$, $V_{SS}=0V$, $T_A=25°C$ unless otherwise stated)

(Continued)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
I_{CHAR}	CHARacter Drive Current	$V_{SUPP}=5V$, $V_{OUT}=1V$	140	190		mA
I_{CHLK}	CHARacter Leakage Current				100	μA
I_{SEG}	SEGment Drive Current	$V_{SUPP}=5V$, $V_{OUT}=2.5V$	14	19		mA
I_{SLK}	SEGment Leakage Current			0.01	10	μA
V_{OL}	DISPlay FULL Output Low	$I_{OL}=1.6mA$			0.4	V
V_{OH}	DISPlay FULL Output High	$I_{IH}=100\mu A$	2.4			V
f_{ds}	Display Scan Rate			400		Hz

AC ELECTRICAL CHARACTERISTICS (Drive levels 0.4V and 2.4V, timing measured at 0.8V and 2.0V. $V_{DD}=5V$, $T_A=25°C$ unless otherwise stated).

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{WPI}	$\overline{WR}$, $\overline{CLeaR}$ Pulse Width Low		300	250		ns
t_{WPH}	$\overline{WR}$, $\overline{CLeaR}$ Pulse Width High (Note 1)			250		
t_{DH}	Data Hold Time		0	−100		
t_{DS}	Data Setup Time		250	150		
t_{AH}	Address Hold Time		125			
t_{AS}	Address Setup Time		40	15		
t_{CS}	CS, $\overline{CS}$ Setup Time		0			
t_T	Pulse Transition Time				100	
t_{SEN}	SEN Setup Time		0	−25		
t_{WDF}	Display Full Delay		700	480		

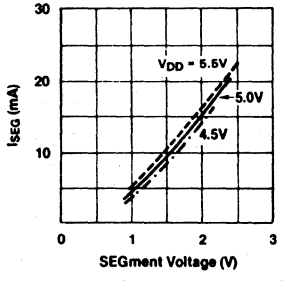
CAPACITANCE

Symbol	Test	Min	Typ	Max	Units
C_{IN}	Input Capacitance (Note 2)		5		pF
C_O	Output Capacitance (Note 2)		5		pF

NOTES: 1. In Sequential mode $\overline{WR}$ high must be $\geq T_{SEN}+T_{WDF}$.
2. For design reference only, not 100% tested.

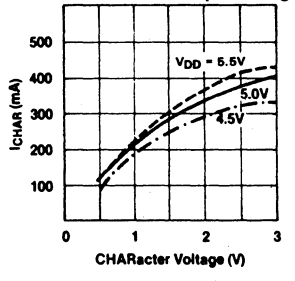
TYPICAL PERFORMANCE CHARACTERISTICS

SEGment Current vs Output Voltage



0368-4

CHARacter Current vs Output Voltage

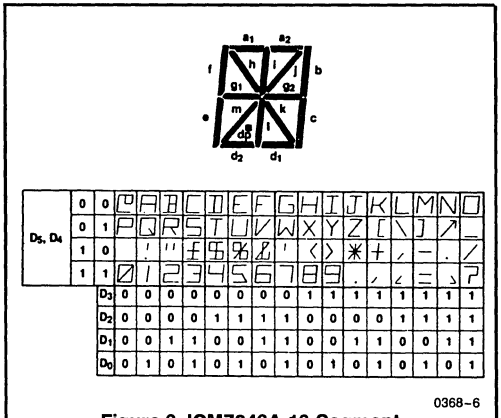


0368-5

NOTE: All typical values have been characterized but are not tested.

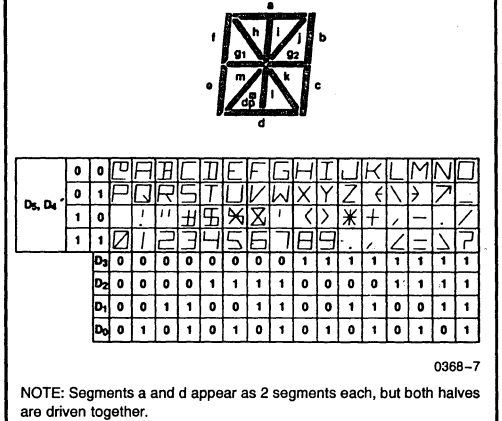
ICM7243A/B DISPLAY FONT AND SEGMENT ASSIGNMENTS

Note: Some display manufacturers use different designations for some of the segments. Check data sheets carefully.



0368-6

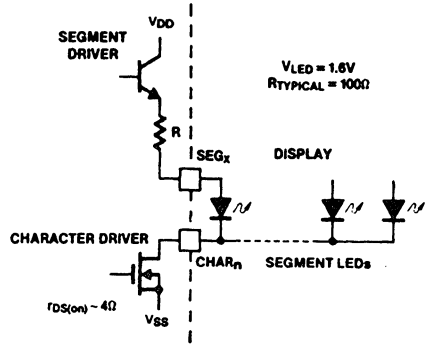
Figure 3: ICM7243A 16-Segment Character Font with Decimal Point



0368-7

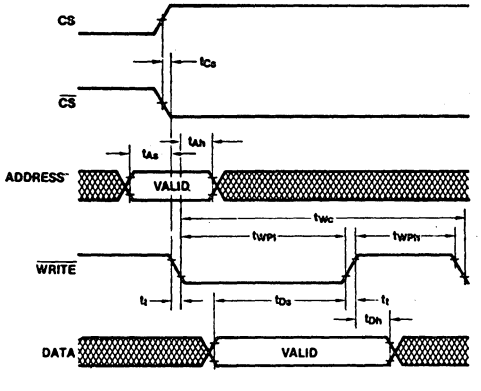
NOTE: Segments a and d appear as 2 segments each, but both halves are driven together.

Figure 4: ICM7243B 14-Segment Character Font with Decimal Point



0368-8

Figure 5: Segment and Character Drivers Output Circuit



0368-9

Figure 6: Random Access Timing

NOTE: All typical values have been characterized but are not tested.

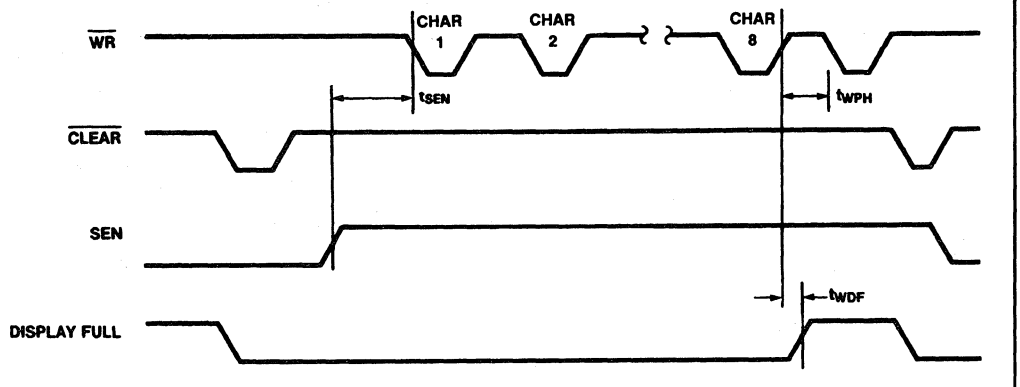


Figure 7: Sequential Access Mode Timing (Mode = 1)

TABLE 1: PIN DESCRIPTIONS, ICM7243A*(B)*

Signal	Pin	Function
$D_0 - D_5$	10 – 15 *(8 – 13)*	Six-Bit ASCII Data input pins (active high).
CS, $\overline{CS}$	16 *(14–16)*	Chip Select from μP address decoder, etc.
$\overline{WR}$	17	WRite pulse input pin (active low). For an active high write pulse, CS can be used, and $\overline{WR}$ can be used as $\overline{CS}$.
MODE	31	Selects data entry MODE. High selects **Sequential Access (SA)** mode where first entry is displayed in "leftmost" character and subsequent entries appear to the "right". Low selects the **Random Access (RA)** mode where data is displayed on the character addressed via A_0–A_2 Address pins.
A_0/SEN	30	In **RA** mode it is the LSB of the character Address. In **SA** mode it is used for cascading devices for displays of more than 8 characters (active high enables device controller).
A_1/$\overline{CLeaR}$	29	In **RA** mode this is the second bit of the address. In **SA** mode, a low input will CLeaR the Serial Address Counter, the Data Memory and the display.
A_2/DISPlay FULL	28	In **RA** mode this is the MSB of the Address. In **SA** mode, the output goes high after eight entries, indicating DISPlay FULL.
OSC/$\overline{OFF}$	27	OSCillator input pin. Adding capacitance to V_{DD} will lower the internal oscillator frequency. An external oscillator can be applied to this pin. A low at this input sets the device into a (shut down) mode, shutting OFF the display and oscillator but retaining data stored in memory.
SEG_a – SEG_m, D.P.	2 – 9, 32 – 40 *(2 – 7), (32 – 40)*	SEGment driver outputs.
CHARacter 1 – 8	18 – 21, 23 – 26	CHARacter driver outputs.

NOTE: All typical values have been characterized but are not tested.

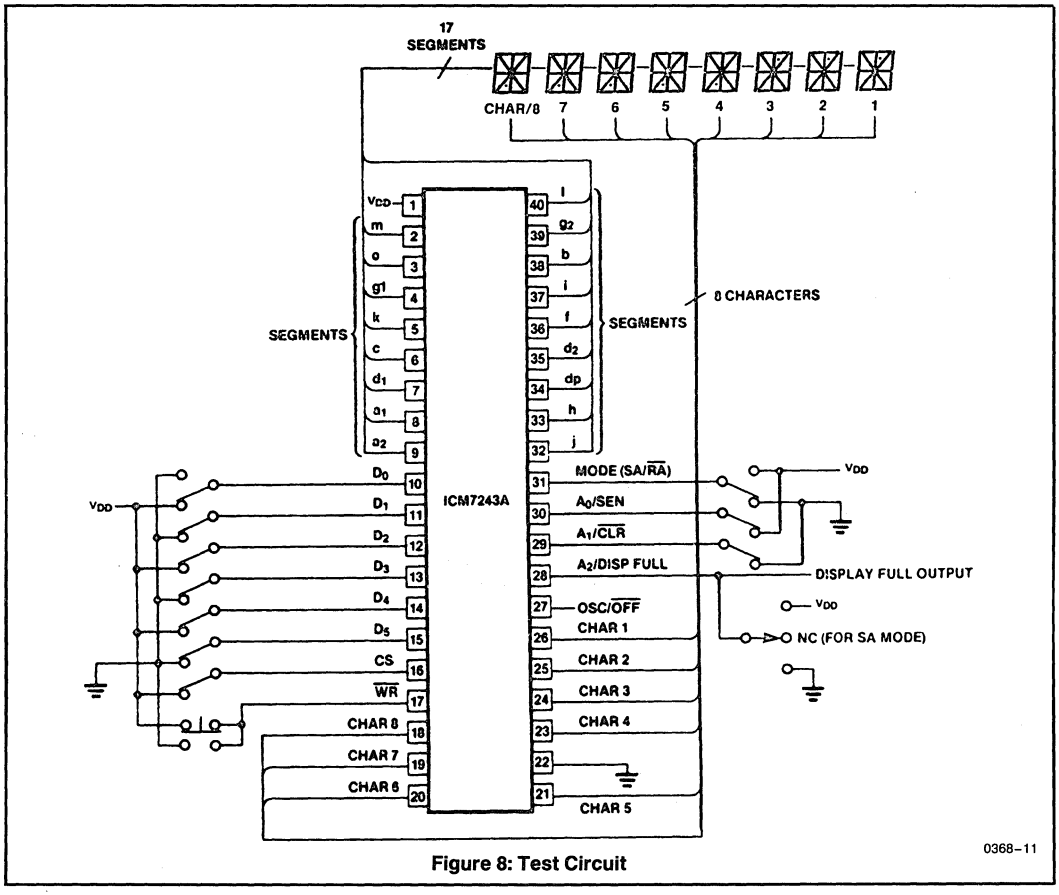


Figure 8: Test Circuit

DETAILED DESCRIPTION

$\overline{WR}$, $\overline{CS}$, CS. These pins are immediately functionally ANDed, so all actions described as occurring on an edge of $\overline{WR}$, with CS and $\overline{CS}$ enabled, will occur on the equivalent (last) enabling or (first) disabling edge of any of these inputs. The delays from CS pins are slightly (about 5ns) greater than from $\overline{WR}$ or $\overline{CS}$ due to the additional inverter required on the former.

MODE. The MODE pin input is latched on the falling edge of $\overline{WR}$ (or its equivalent, see above). The location (in Data Memory) where incoming data will be placed is determined either from the Address pins or the Sequential Address Counter. This is controlled by MODE input. MODE also controls the function of A_0/SEN, $A_1/\overline{CLR}$, and A_2/DISPlay FULL lines.

Random Access Mode. When the internal mode latch is set for **Random Access (RA)** (MODE latched low), the Address input on A_0, A_1 and A_2 will be latched by the falling edge of $\overline{WR}$ (or its equivalent). Subsequent changes on the Address lines will not affect device operation. This allows use of a multiplexed 6-bit bus controlling both address and data, with timing controlled by $\overline{WR}$.

Sequential Access Mode. If the internal latch is set for **Sequential Access (SA),** (MODE latched high), the Serial ENable input or SEN will be latched on the falling edge of $\overline{WR}$ (or its equivalent). The $\overline{CLR}$ input is asynchronous, and will force-clear the Sequential Address Counter to address 000 (CHARacter 1), and set all Data Memory contents to 100000 (blank) at any time. The DISPlay FULL output will be active in **SA** mode to indicate the overflow status of the Sequential Address Counter. If this output is low, and SEN is (latched) high, the contents of the Counter will be used to establish the Data Memory location for the Data input. The Counter is then incremented on the rising edge of $\overline{WR}$. If SEN is low, or DISPlay FULL is high, no action will occur. This allows easy "daisy-chaining" of display drivers for multiple character displays in a **Sequential Access** mode.

NOTE: All typical values have been characterized but are not tested.

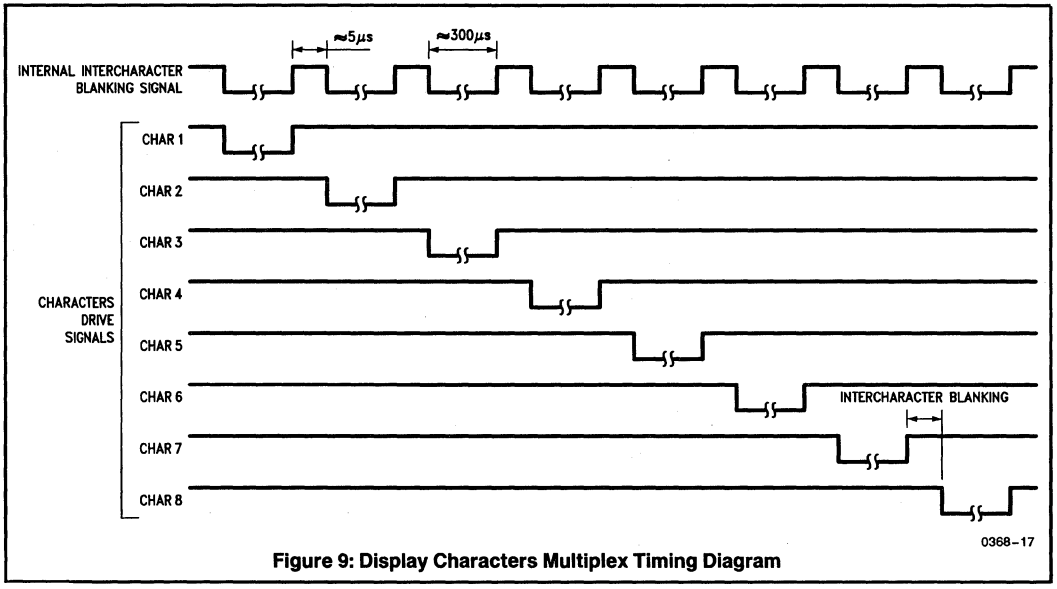


Figure 9: Display Characters Multiplex Timing Diagram

NOTE: All typical values have been characterized but are not tested.

Changing Modes. Care must be exercised in any application involving changing from one mode to another. The change will occur only on a falling edge of $\overline{WR}$ (or its equivalent). When changing mode from **Sequential Access** to **Random Access**, note that A_2/DISPlay FULL will be an output until $\overline{WR}$ has fallen low, and an Address drive here could cause a conflict. When changing from **Random Access** to **Sequential Access**, $A_1/\overline{CLR}$ should be high to avoid inadvertent clearing of the Data Memory and Sequential Address Counter. DISPlay FULL will become active immediately after the rising edge of $\overline{WR}$.

Data Entry. The input Data is latched on the rising edge of $\overline{WR}$ (or its equivalent) and then stored in the Data Memory location determined as described above. The six Data bits can be multiplexed with the Address information on the same lines in **Random Access** mode. Timing is controlled by the $\overline{WR}$ input.

OSC/$\overline{OFF}$. The device includes a relaxation oscillator with an internal capacitor and a nominal frequency of 200kHz. By adding external capacitance to V_{DD} at the OSC/$\overline{OFF}$ pin, this frequency can be reduced as far as desired. Alternatively, an external signal can be injected on this pin. The oscillator (or external) frequency is pre-divided by 64, and then further divided by 8 in the Multiplex Counter, to drive the CHARacter drive lines (see Figure 9). An inter-character blanking signal is derived from the pre-divider. An additional comparator on the OSC/$\overline{OFF}$ input detects a level lower than the relaxation oscillator's range, and blanks the display, disables the DISPlay FULL output (if active), and clears the pre-divider and Mutliplex Counter. This puts the circuit in a low-power-dissipation mode in which all outputs are effectively open circuits, except for parasitic diodes to the supply lines. Thus a display connected to the output may be driven by another circuit (including another ICM7243) without driver conflicts.

Display Output. The output of the Multiplex Counter is decoded and multiplexed into the address input of the Data Memory, except during $\overline{WR}$ operations (in **Sequential Access** mode, with SEN high and DISPlay FULL low), when it scans through the display data. The address decoder also drives the CHARacter outputs, except during the inter-character blanking interval (nominally about 5μs). Each CHARacter output lasts nominally about 300μs, and is repeated nominally every 2.5ms, i.e., at a 400Hz rate (times are based on internal oscillator without external capacitor).

The 6 bits read from the Data Memory are decoded in the ROM to the 17 (15 for ICM7243B) segment signals, which drive the SEGment outputs. Both CHARacter and SEGment outputs are disabled during $\overline{WR}$ operations (with SEN high and DISPlay FULL Low for **Sequential Access** mode). The outputs may also be disabled by pulling OSC/$\overline{OFF}$ low.

The decode pattern from 6 bits to 17 (15) segments is done by a ROM pattern according to the ASCII font shown. Custom decode patterns can be arranged, within these limitations, by consultation with the factory.

APPLICATIONS

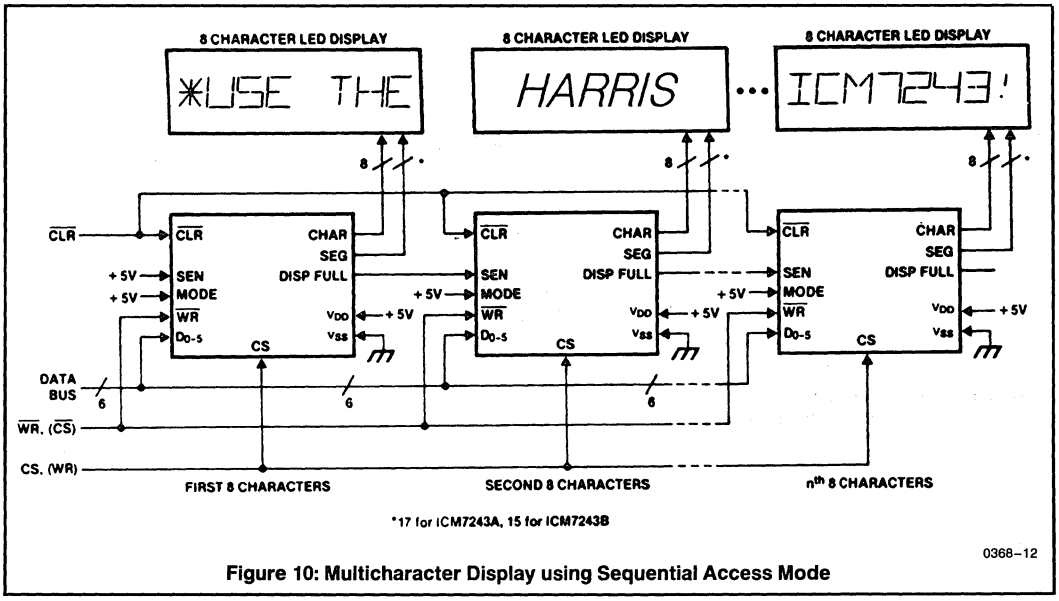
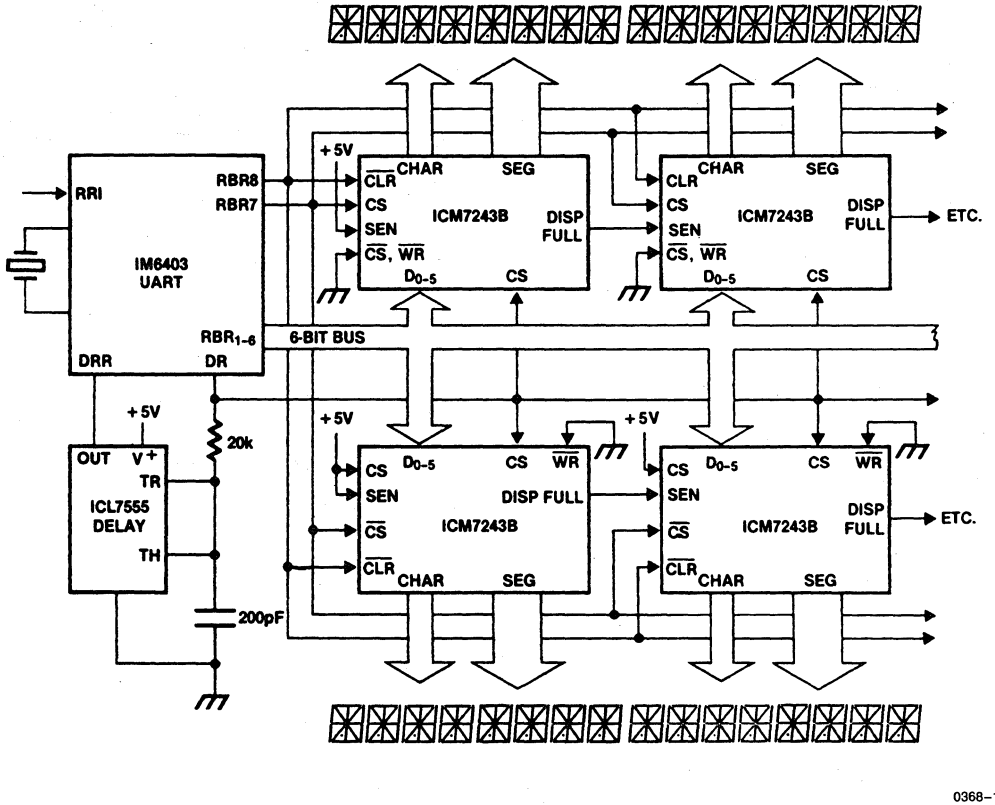


Figure 10: Multicharacter Display using Sequential Access Mode

NOTE: All typical values have been characterized but are not tested.

APPLICATIONS (Continued)



0368-13

Figure 11: Driving Two Rows of Characters from a Serial Input.

UART converts data stream to parallel bytes. Bit 7 of each word sets which row data will be entered into. Bit 8 will blank and reset whole display if low. Each MODE pin should be tied high. ICM7243A can also be used, with inverter on RBR7 for one row.

COMPONENT SELECTION

Displays suitable for use with the ICM7243 may be obtained from the following manufacturers; among others:

Hewlett Packard Components, Palo Alto, California (415) 857-6620 (part #HDSP6508, HDSP6300)

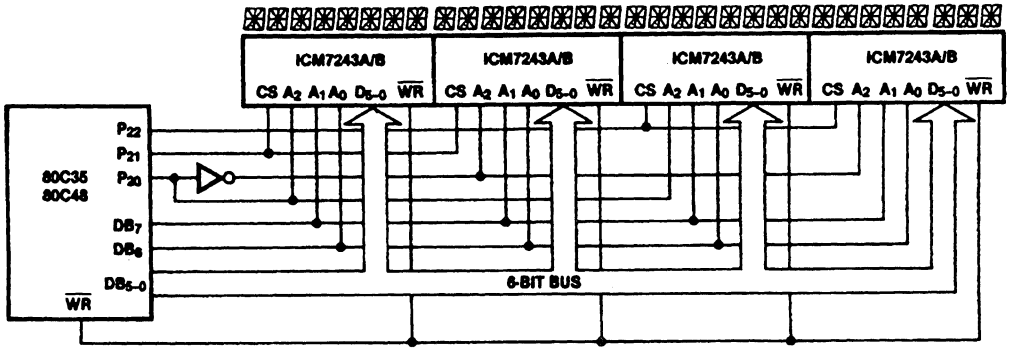
General Instruments Inc., Palo Alto, California (415) 493-0400 (part #MAN2815)

Texas Instruments Inc., Dallas, Texas (214) 995-6611 (part #HDSP6508)

A.N.D., Burlingame, California (415) 347-9916 (part #AND370R)

IEE Inc., Van Nuys, California (213) 787-0311 (part #LR3784R)

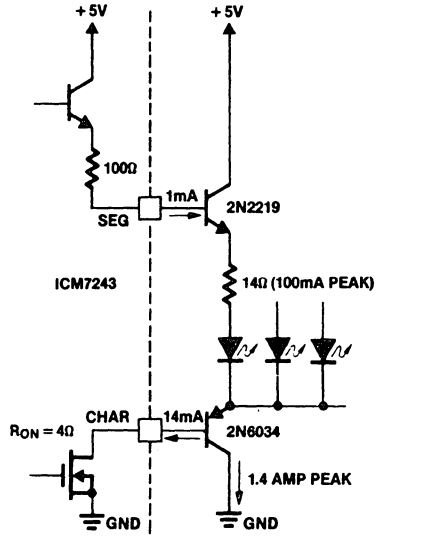
NOTE: All typical values have been characterized but are not tested.



0368-14

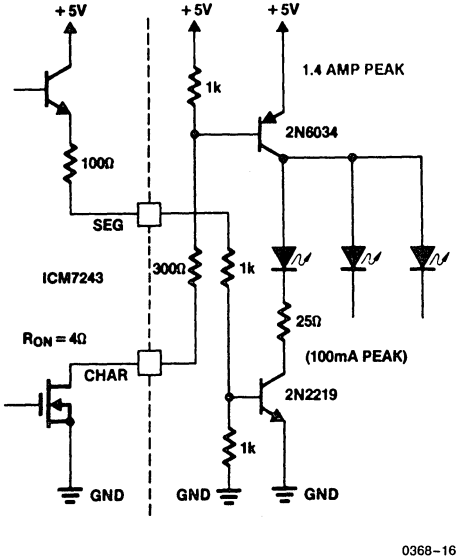
Figure 12: Random Access 32-Character Display in a 80C48 system.

One port line controls A_2, other two are CS lines. 8-bit data bus drives 6 data and 2 address lines. MODE should be GrouNDed on each part.



0368-15

(a)
Common Cathode Displays



0368-16

(b)
Common Anode Displays

Figure 13: Driving Large Displays.

The circuits of Figures 13a and 13b can be used to drive 0.5" or larger alphanumeric displays, either common cathode (13a) or common anode (13b).

NOTE: All typical values have been characterized but are not tested.

DATA ACQUISITION 10

REAL-TIME CLOCK

HARRIS SEMICONDUCTOR

ICM7170
μP-Compatible Real-Time Clock

GENERAL DESCRIPTION

The ICM7170 real time clock is a microprocessor bus compatible peripheral, fabricated using Harris' silicon gate CMOS LSI process. An 8-bit bidirectional bus is used for the data I/O circuitry. The clock is set or read by accessing the 8 internal separately addressable and programmable counters from 1/100 seconds to years. The counters are controlled by a pulse train divided down from a crystal oscillator circuit, and the frequency of the crystal is selectable with the on-chip command register. An extremely stable oscillator frequency is achieved through the use of an on-chip regulated power supply.

The device access time (t_{acc}) of 300ns eliminates the need for wait states or software overhead with most microprocessors. Furthermore, an ALE (Address Latch Enable) input is provided for interfacing to microprocessors with a multiplexed address/data bus. With these two special features, the ICM7170 can be easily interfaced to any available microprocessor.

The ICM7170 generates two types of interrupts, periodic and alarm. The periodic interrupt (100Hz, 10Hz, etc.) can be programmed by the internal interrupt control register to provide 6 different output signals. The alarm interrupt is set by loading an on-chip 51-bit RAM that activates an interrupt output through a comparator. The alarm interrupt occurs when the real time counter and alarm RAM time are equal. A status register is available to indicate the interrupt source.

An on-chip Power-Down Detector eliminates the need for external components to support the battery back-up function. When a power-down or power failure occurs, internal logic switches the on-chip counters to battery back-up operation. Read/write functions become disabled and operation is limited to time-keeping and interrupt generation, resulting in low power consumption.

Internal latches prevent clock roll-over during a read cycle. Counter data is latched on the chip by reading the 100th-seconds counter and is held indefinitely until the counter is read again, assuring a stable and reliable time value.

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7170IPG	−40°C to +85°C	24-Pin Plastic Dip
ICM7170IDG	−40°C to +85°C	24-Pin Ceramic
ICM7170IBG	−40°C to +85°C	24-Pin SOIC
ICM7170MDG	−55°C to +125°C	24-Pin Ceramic
ICM7170AIPG	−40°C to +85°C	24-Pin Plastic Dip
ICM7170AIDG	−40°C to +85°C	24-Pin Ceramic
ICM7170AIBG	−40°C to +85°C	24-Pin SOIC
ICM7170AMDG	−55°C to +125°C	24-Pin Ceramic

"A" Parts Screened to <5 μA I_{STBY} @ 32 KHz

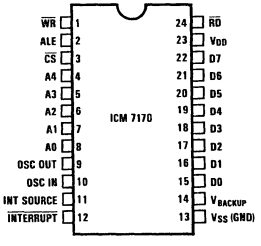
FEATURES

- **8-Bit μP Bus Compatible —Multiplexed or Direct Addressing**
- **Regulated Oscillator Supply Ensures Frequency Stability and Low Power**
- **Time From 1/100 Seconds to 99 Years**
- **Software Selectable 12/24 Hour Format**
- **Latched Time Data Ensures No Roll-Over During Read**
- **Full Calendar With Automatic Leap Year Correction**
- **On-Chip Battery Backup Switchover Circuit**
- **Access Time Less Than 300ns**
- **4 Programmable Crystal Oscillator Frequencies over Industrial Temp Range**
- **3 Programmable Crystal Oscillator Frequencies over Military Temp Range**
- **On-Chip Alarm Comparator and RAM**
- **Interrupts from Alarm and 6 Selectable Periodic Intervals**
- **Standby Micro-Power Operation: 1.2μA Typical at 3.0V and 32kHz Crystal**

APPLICATIONS

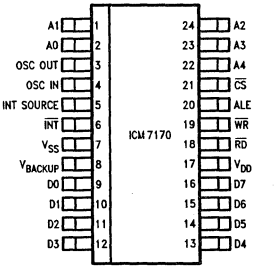
- **Portable and Personal Computers**
- **Data Logging**
- **Industrial Control Systems**
- **Point Of Sale**

Plastic & Ceramic



0372-1

S.O.I.C.



0372-11

Figure 1: Pin Configurations

301680-008

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

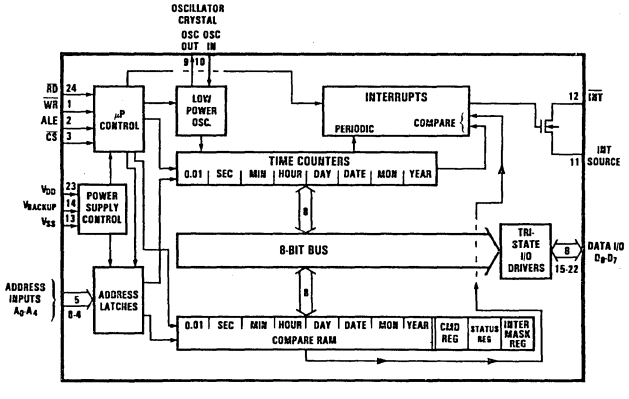
Supply Voltage 8V
Power Dissipation (Note 1) 500mW
Input Voltage (Any Terminal)
(Note 2) ..... V_{DD} +0.3V to V_{SS} −0.3V

Operating Temperature ..... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE 1: T_A = 25°C.

NOTE 2: Due to the SCR structure inherent in the CMOS process, connecting any terminal at voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7170 be turned on first.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*



0372-2

Figure 2: Functional Diagram

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS

(T_A = −40°C to +85°C, V_{DD} = +5V ±10%, V_{BACKUP} = V_{DD}, V_{SS} = 0V unless otherwise specified)
All I_{DD} specifications include all input and output leakages (7170 and 7170A)

Symbol	Parameter	Test Conditions		Specification Min	Specification Typ	Specification Max	Units
V_{DD}	V_{DD} Supply Range	F_{OSC} = 32kHz		1.9		5.5	V
		F_{OSC} = 1, 2, 4MHz		2.6		5.5	
$I_{STBY(1)}$	Standby Current	F_{OSC} = 32kHz Pins 1–8, 15–22 & 24 = V_{DD} V_{DD} = V_{SS}; V_{BACKUP} = V_{DD} − 3.0V For 7170A See General Note (5)	7170		1.2	20.0	µA
			7170A		1.2	5.0	
$I_{STBY(2)}$	Standby Current	F_{OSC} = 4MHz Pins 1–8, 15–22 & 24 = V_{DD} V_{DD} = V_{SS}; V_{BACKUP} = V_{DD} − 3.0V			20	150	µA
$I_{DD(1)}$	Operating Supply Current	F_{OSC} = 32kHz Read/Write Operation at 100Hz			0.3	1.2	mA
$I_{DD(2)}$	Operating Supply Current	F_{OSC} = 32kHz Read/Write Operation at 1MHz			1.0	2.0	mA

"A" Parts Screened to <5 µA I_{STBY} @ 32 KHz

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS
DC CHARACTERISTICS

($T_A = -40°C$ to $+85°C$, $V_{DD} = +5V \pm 10\%$, $V_{BACKUP} = V_{DD}$, $V_{SS} = 0V$ unless otherwise specified) (Continued)
All I_{DD} specifications include all input and output leakages (7170 and 7170A)

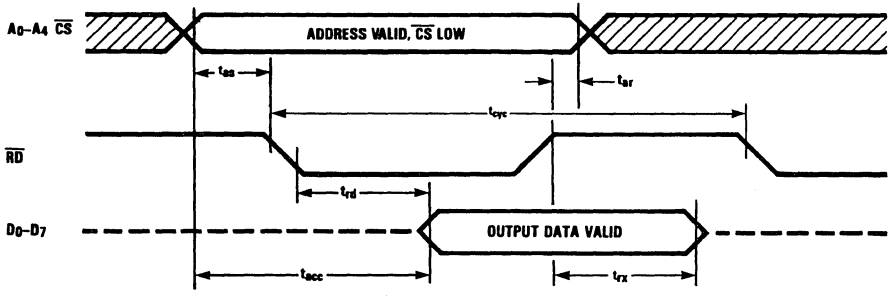
Symbol	Parameter	Test Conditions		Specification			Units
				Min	Typ	Max	
V_{IL}	Input low voltage (Except Osc.)	$V_{DD} = 5.0V$				0.8	V
V_{IH}	Input high voltage (Except Osc.)	$V_{DD} = 5.0V$		2.4			V
V_{OL}	Output low voltage (Except Osc.)	$I_{OL} = 1.6mA$				0.4	V
V_{OH}	Output high voltage except $\overline{INTERRUPT}$ (Except Osc.)	$I_{OH} = -400\mu A$		2.4			V
I_{IL}	Input leakage current	$V_{IN} = V_{DD}$ or V_{SS}		−10	0.5	+10	μA
I_{OL}(1)	Tristate leakage current (D_0–D_7)	$V_0 = V_{DD}$ or V_{SS}		−10	0.5	+10	μA
$V_{BATTERY}$	Backup Battery Voltage	$F_{OSC} = 1, 2, 4MHz$		2.6		$V_{DD} - 1.3$	V
$V_{BATTERY}$	Backup Battery Voltage	$F_{OSC} = 32kHz$		1.9		$V_{DD} - 1.3$	V
I_{OL}(2)	Leakage current $\overline{INTERRUPT}$	$V_0 = V_{DD}$	INT SOURCE connected to V_{SS}		0.5	10	μA
$C_{I/O}$	CAPACITANCE D_0–D_7				8		pF
$C_{ADDRESS}$	CAPACITANCE A_0–A_4				6		pF
$C_{CONTROL}$	CAP. $\overline{RD}$, $\overline{WR}$, $\overline{CS}$ ALE				6		pF
C_{IN} Osc.	Total Osc. Input Cap.				3		pF

AC CHARACTERISTICS ($T_A = -40°C$ to $+85°C$, $V_{DD} = +5V \pm 10\%$, $V_{BACKUP} = V_{DD}$, D_0–D_7 Load Capacitance = 150pF, $V_{IL} = 0.4V$, $V_{IH} = 2.8V$ unless otherwise specified)

Symbol	Parameter	Min	Max	Units
READ CYCLE TIMING				
t_{rd}	READ to DATA valid		250	ns
t_{acc}	ADDRESS valid to DATA valid		300	ns
t_{cyc}	READ cycle time	400		ns
t_{rh}	Read high time	150		ns
t_{rx}	$\overline{RD}$ high to bus tristate		25	ns
t_{as}	ADDRESS to READ set up time	50		ns
t_{ar}	ADDRESS HOLD time after READ	0		ns
WRITE CYCLE TIMING				
t_{ad}	ADDRESS valid to WRITE strobe	50		ns
t_{wa}	ADDRESS hold time for WRITE	0		ns
t_{wl}	WRITE pulse width, low	100		ns
t_{wh}	WRITE high time	300		ns
t_{dw}	DATA IN to WRITE set up time	100		ns
t_{wd}	DATA IN hold time after WRITE	30		ns
t_{cyc}	WRITE cycle time	400		ns
MULTIPLEXED MODE TIMING				
t_{ll}	ALE Pulse Width, High	50		ns
t_{al}	ADDRESS to ALE set up time	30		ns
t_{la}	ADDRESS hold time after ALE	30		ns

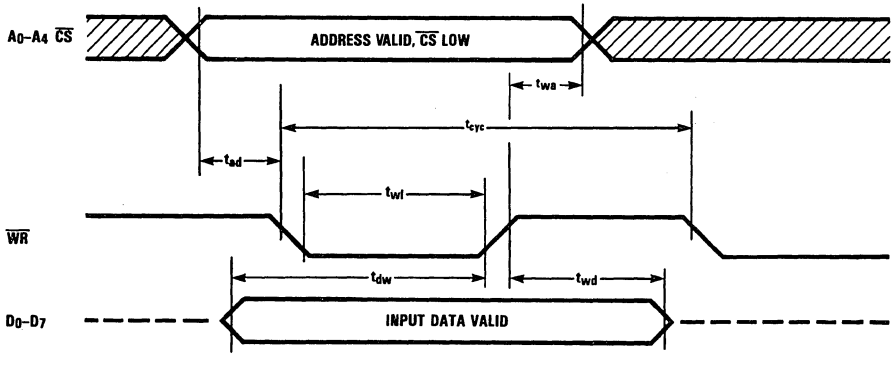
NOTE: All typical values have been characterized but are not tested.

READ CYCLE TIMING FOR NON-MULTIPLEXED BUS (ALE = V_{IH}, $\overline{WR}$ = V_{IH})



0372-3

WRITE CYCLE TIMING FOR NON-MULTIPLEXED BUS (ALE = V_{IH}, $\overline{RD}$ = V_{IH})



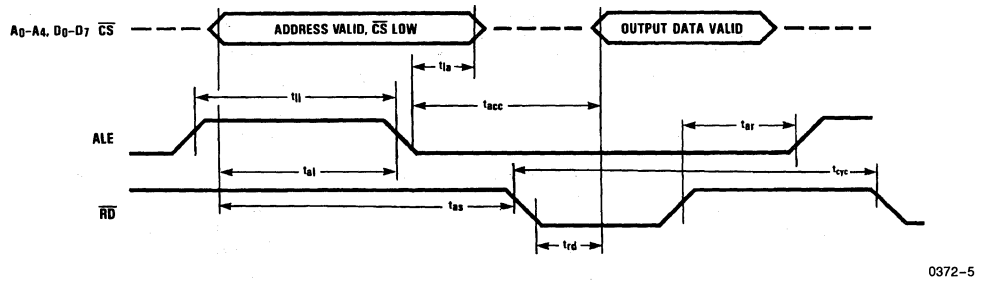
0372-4

Figure 3: Timing Diagrams — Nonmultiplexed Bus

10

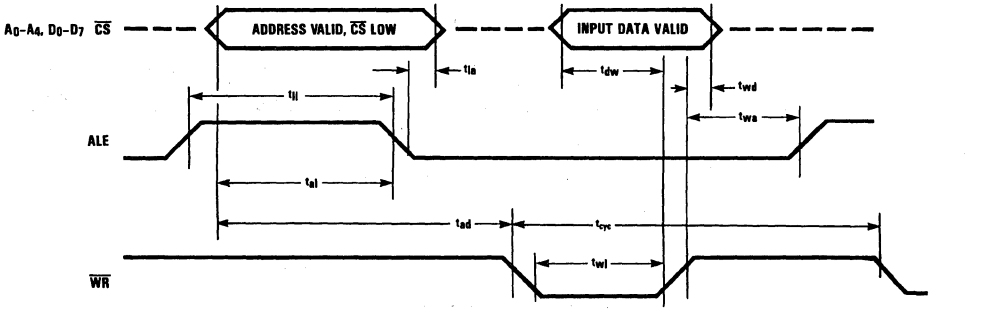
NOTE: All typical values have been characterized but are not tested.

READ CYCLE TIMING FOR MULTIPLEXED BUS ($\overline{WR} = V_{IH}$)



0372-5

WRITE CYCLE TIMING FOR MULTIPLEXED BUS ($\overline{RD} = V_{IH}$)



0372-6

NOTE: The A0 to A4 address inputs may be connected to the D0 to D4 data lines when a multiplexed bus is used.

Figure 4: Timing Diagrams — Multiplexed Bus

Table 1: Pin Description

Signal	Pin#	SOIC Pin#	Description
$\overline{WR}$	1	19	$\overline{Write}$ input
ALE	2	20	Address latch enable input
$\overline{CS}$	3	21	$\overline{Chip\ select}$ input
A4-A0	4-8	22-2	Address inputs
OSC OUT	9	3	Oscillator output
OSC IN	10	4	Oscillator input
INT SOURCE	11	5	Interrupt source
$\overline{INTERRUPT}$	12	6	$\overline{Interrupt}$ output
V_{SS}(GND)	13	7	Digital common
V_{BACKUP}	14	8	Battery negative side
D0-D7	15-22	9-16	Data I/O
V_{DD}	23	17	Positive digital supply
$\overline{RD}$	24	18	$\overline{Read}$ input

DETAILED DESCRIPTION

Oscillator

The ICM7170 has an onboard CMOS Pierce oscillator with an internally regulated voltage supply for maximum accuracy, stability, and low power consumption. It operates at any of four popular crystal frequencies: 32.768kHz, 1.048576MHz, 2.097152MHz, and 4.194304MHz.* The crystal should be designed for the parallel resonant mode of oscillation. In addition to the crystal, 2 or 3 load capacitors are required, depending on the circuit topology used.

The oscillator output is divided down to 4000Hz by one of four divider ratios, determined by the two frequency selection bits in the Command Register (D0 and D1 at address $11). This 4000Hz is then divided down to 100Hz, which is used as the clock for the counters.

Time and calendar information is provided by 8 consecutive, programmable counters: 100ths of seconds, seconds, minutes, hours, day of week, date, month, and year. The data is in binary format with 8 bits per digit. See Table 4 for address information. Any unused bits are held to a logic "0" during a read and ignored during a write operation.

***NOTE:** 4.194304MHz is not available over military temperature range.

NOTE: All typical values have been characterized but are not tested.

Alarm Compare RAM

On the chip are 51 bits of Alarm Compare RAM grouped into words of different lengths. These are used to store the time, ranging from 100ths of seconds to years, for comparison to the real-time counters. Each counter has a corresponding RAM word. In the Alarm Mode an interrupt is generated when the current time is equal to the alarm time. The RAM contents are compared to the counters on a word by word basis. If a comparison to a particular counter is unnecessary, then the appropriate 'M' bit in Compare RAM should be set to logic "1".

The 'M' bit, referring to Mask bit, causes a particular RAM word to be masked off or ignored during a compare. Table 4 shows addresses and Mask bit information.

Periodic Interrupts

The interrupt output can be programmed for 6 periodic signals: 100 Hz, 10 Hz, once per second, once per minute, once per hour, or once per day. The 100 Hz and 10 Hz interrupts have instantaneous errors of ±2.5% and ±0.15% respectively. This is because non-integer divider circuitry is used to generate these signals from the crystal frequency, which is a power of 2. The time average of these errors over a 1 second period, however, is zero. Consequently, the 100 Hz or 10 Hz interrupts are not suitable as an aid in tuning the oscillator; the 1 second interrupt must be used instead.

See General Note (6).

The periodic interrupts can occur concurrently and in addition to alarm interrupts. The periodic interrupts are controlled by bits in the interrupt mask register, and are enabled by setting the appropriate bit to a "1" as shown in Table 5. Bits D1 through D6 in the mask register, in conjunction with bits D1 through D6 of the status register, control the generation of interrupts according to Figure 5.

The interrupt status register, when read, indicates the cause of the interrupt and resets itself on the rising edge of the RD signal. When any of the counters having a corresponding bit in the status register increments, that bit is set to a "1" regardless of whether the corresponding bit in the interrupt mask register is set or not.

Consequently, when the status register is read it will always indicate which counters have increments and if an alarm compare occurred, since the last time it was read. This requires some special software considerations. If a slow interrupt is enabled (i.e. hourly or daily), the program must always check the slowest interrupt that has been enabled first, because all the other lower order bits in the status register will be set to "1" as well.

Bit D7 is the global interrupt bit, and when set to a "1", indicates that the 7170 did indeed generate a hardware interrupt. This is useful when other interrupting devices in addition to the 7170 are attached to the system microprocessor, and all devices must be polled to determine which one generated the interrupt.

See General Note (6).

Table 2: Command Register Format

COMMAND REGISTER ADDRESS (10001b, 11h) WRITE-ONLY							
D7	D6	D5	D4	D3	D2	D1	D0
n/a	n/a	Normal/Test Mode	Interrupt Enable	Run/Stop	12/24 Hour Format	Crystal Frequency	Crystal Frequency

Table 3: Command Register Bit Assignments

D5	Test Bit	D4	Interrupt Enable	D3	Run/Stop	D2	24/12 Hour Format	D1	D0	Crystal Frequency
0	Normal Mode	0	Interrupt disabled	0	Stop	0	12 hour mode	0	0	32.768kHz
1	Test Mode	1	Interrupt enable	1	Run	1	24 hour mode	0	1	1.048576MHz
								1	0	2.097152MHz
								1	1	4.194304MHz

NOTE: All typical values have been characterized but are not tested.

Table 4: Address Codes and Functions

Address						Function	DATA								Value
A4	A3	A2	A1	A0	HEX		D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	00	Counter-1/100 seconds	–	.	.	.	.	.	.	.	0-99
0	0	0	0	1	01	Counter-hours	–	–	–	.	.	.	.	.	0-23
						12 Hour Mode	*	–	–	–	.	.	.	.	1-12
0	0	0	1	0	02	Counter-minutes	–	–	.	.	.	.	.	.	0-59
0	0	0	1	1	03	Counter-seconds	–	–	.	.	.	.	.	.	0-59
0	0	1	0	0	04	Counter-month	–	–	–	–	.	.	.	.	1-12
0	0	1	0	1	05	Counter-date	–	–	–	.	.	.	.	.	1-31
0	0	1	1	0	06	Counter-year	–	.	.	.	.	.	.	.	0-99
0	0	1	1	1	07	Counter-day of week	–	–	–	–	–	.	.	.	0-6
0	1	0	0	0	08	RAM-1/100 seconds	M	.	.	.	.	.	.	.	0-99
0	1	0	0	1	09	RAM-hours	–	M	–	.	.	.	.	.	0-23
						12 hour Mode	*	M	–	–	.	.	.	.	1-12
0	1	0	1	0	0A	RAM-minutes	M	–	.	.	.	.	.	.	0-59
0	1	0	1	1	0B	RAM-seconds	M	–	.	.	.	.	.	.	0-59
0	1	1	0	0	0C	RAM-month	M	–	–	–	.	.	.	.	1-12
0	1	1	0	1	0D	RAM-date	M	–	–	.	.	.	.	.	1-31
0	1	1	1	0	0E	RAM-year	M	.	.	.	.	.	.	.	0-99
0	1	1	1	1	0F	RAM-day of week	M	–	–	–	–	.	.	.	0-6
1	0	0	0	0	10	Interrupt Status and Mask Register	+	.	.	.	.	.	.	.	
1	0	0	0	1	11	Command register	–	–	.	.	.	.	.	.	

NOTES: Addresses 10010 to 11111 (12h to 1Fh) are unused.
'+' Unused bit for Interrupt Mask Register, MSB bit for Interrupt Status Register.
'–' Indicates unused bits.
'*' AM/PM indicator bit in 12 hour format. Logic "0" indicates AM, logic "1" indicates PM.
'M' Alarm compare for particular counter will be enabled if bit is set to logic "0".

Table 5: Interrupt and Status Registers Format

INTERRUPT MASK REGISTER ADDRESS (10000b, 10h) WRITE-ONLY							
D7	D6	D5	D4	D3	D2	D1	D0
Not Used	Day	Hour	Min.	Sec.	1/10 sec.	1/100 sec.	Alarm
	←	Periodic Interrupt Mask Bits				→	Alarm/Compare Mask Bit
INTERRUPT STATUS REGISTER ADDRESS (10000b, 10h) READ-ONLY							
D7	D6	D5	D4	D3	D2	D1	D0
Global Interrupt	Day	Hour	Min.	Sec.	1/10 sec.	1/100 sec.	Alarm
Periodic and Alarm Flags	←	Periodic Interrupt Flags				→	Alarm Compare Flag

NOTE: All typical values have been characterized but are not tested.

Interrupt Operation

The Interrupt Output N-channel MOSFET (Figure 5) is enabled whenever both the Interrupt Enable bit (D4 of the Command Register) and a mask bit (D0-D6 of the Interrupt Mask Register) are set. The transistor is turned ON when a flag bit is set that corresponds to one of the set mask bits. This also sets the Global Interrupt Flag Bit (D7 of the Interrupt Status Register). It is turned OFF when the Interrupt Status Register is read. An interrupt can occur in both the operational and standby modes of operation.

Since system power is usually applied between V_{DD} and V_{SS}, the user can connect the Interrupt Source (pin #11) to V_{SS}. This allows the Interrupt Output to turn on only while system power is applied and will not be pulled to V_{SS} during standby operation. If interrupts are required only during standby operation, then the interrupt source pin should be connected to the battery's negative side (V_{BACKUP}). In this configuration, for example, the interrupt could be used to turn on power for a cold boot.

Power-Down Detector

The ICM7170 contains an on-chip power-down detector that eliminates the need for external components to support the battery-backup switchover function, as shown in Figure 6. Whenever the voltage from the V_{SS} pin to the V_{BACKUP} pin is less than approximately 1.0V (the V_{th} of the N-channel MOSFET), the data bus I/O buffers in the 7170 are automatically disabled and the chip cannot be read or written to. This prevents random data from the microprocessor being written to the clock registers as the power supply is going down.

Actual switchover to battery operation occurs when the voltage on the V_{BACKUP} pin is within ±50 mV of V_{SS}. This switchover uncertainty is due to the offset voltage of the CMOS comparator that is used to sense the battery voltage. During battery backup, device operation is limited to timekeeping and interrupt generation only, thus achieving micropower current drain. If an external battery-backup switchover circuit is being used with the 7170, or if standby battery operation is not required, the V_{BACKUP} pin should be pulled up to V_{DD} through a 2k resistor.

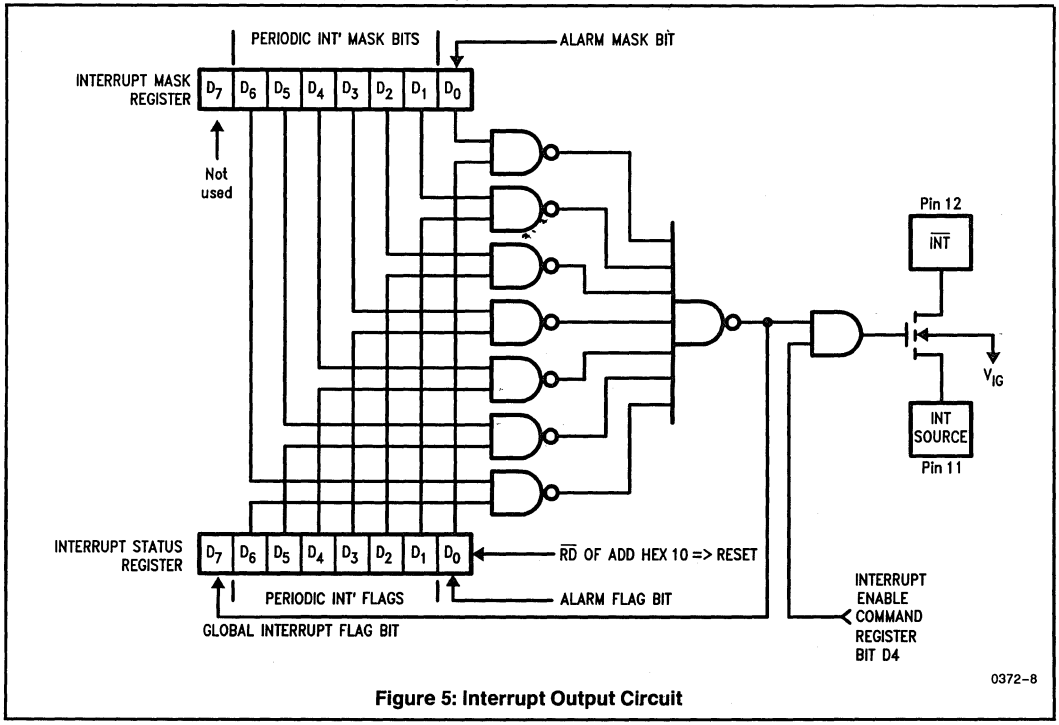


Figure 5: Interrupt Output Circuit

NOTE: All typical values have been characterized but are not tested.

Time Synchronization

Time synchronization is achieved through bit D3 of the Command Register, which is used to enable or disable the 100Hz clock from the counters. A logic "1" allows the counters to function and a logic "0" disables the counters. To accurately set the time, a logic "0" should be written into D3 and then the desired times entered into the appropriate counters. The clock is then started at the proper time by writing a logic "1" into D3 of the Command Register.

Latched Data

To prevent ambiguity while the processor is gathering data from the registers, the ICM7170 incorporates data latches and a transparent transition delay circuit.

By accessing the 100ths of seconds counter an internal store signal is generated and data from all the counters is transferred into a 36-bit latch. A transition delay circuit will delay a 100Hz transition during a READ cycle. The data stored by the latches is then available for further processing until the 100ths of seconds counter is read again. If a $\overline{RD}$ signal is wider than 0.01 sec., 100Hz counts will be ignored.

Control Lines

The $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ signals are active low inputs. Data is placed on the bus from counters or registers when $\overline{RD}$ is a logic "0". Data is transferred to counters or registers when $\overline{WR}$ is a logic "0". $\overline{RD}$ and $\overline{WR}$ must be accompanied by a logical "0" $\overline{CS}$ as shown in Figures 3 and 4. The 7170 will also work satisfactorily with $\overline{CS}$ grounded. In this mode, access to the 7170 is controlled by $\overline{RD}$ and $\overline{WR}$ only.

With the ALE (Address Latch Enable) input, the ICM7170 can be interfaced directly to microprocessors that use a multiplexed address/data bus by connecting the address lines A0-A4 to the data lines D0-D4. To address the chip, the address is placed on the bus and ALE is strobed. On the falling edge, the address and $\overline{CS}$ information is read into the address latch and buffer. $\overline{RD}$ and $\overline{WR}$ are used in the same way as on a non-multiplexed bus. If a non-multiplexed bus is used, ALE should be connected to V_{DD}.

Test Mode

The test mode is entered by setting D5 of the Command Register to a logic "1". This connects the 100Hz counter directly to the oscillator's output.

Oscillator Considerations

Load Design: A new oscillator load configuration, shown in Figure 7, has been found that eliminates startup problems sometimes encountered with 32kHz tuning fork crystals.

Two conditions must be met for best oscillator performance: the capacitive load must be matched to both the inverter and crystal to provide the ideal conditions for oscillation, and the resonant frequency of the oscillator must be adjustable to the desired frequency. In the original design (Figure 8), these two goals were often at odds with each other; either the oscillator was trimmed to frequency by detuning the load circuit, or stability was increased at the expense of absolute frequency accuracy.

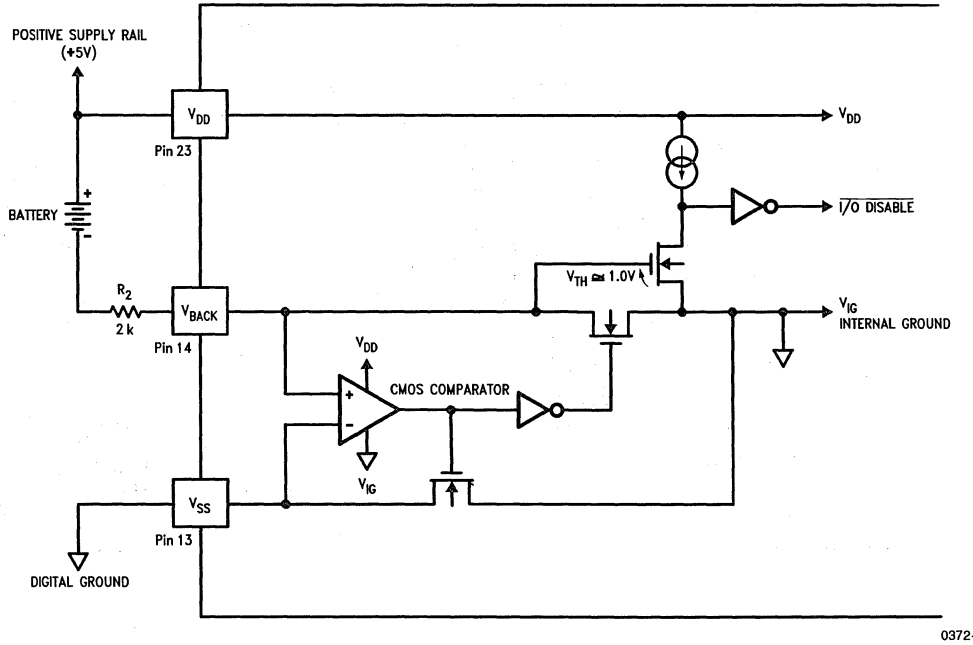


Figure 6: Simplified 7170 Battery Backup Circuit

NOTE: All typical values have been characterized but are not tested.

The new load configuration (Figure 7) allows these two conditions to be met independently. The two load capacitors, C_1 and C_2, provide a fixed load to the oscillator and crystal. C_3 adjusts the frequency that the circuit resonates at by reducing the effective value of the crystal's motional capacitance, C_o. This minute adjustment does not appreciably change the load of the overall system, therefore stability is no longer affected by tuning. Typical values for these capacitors are shown in Table 6. C_1 and C_2 must always be greater than twice the crystal's recommended load capacitance in order for C_3 to be able to trim the frequency. Some experimentation may be necessary to determine the ideal values of C_1 and C_2 for a particular crystal.

This three capacitor tuning method will be more stable than the original design and is mandatory for 32 kHz tuning fork crystals: without it they may leap into an overtone mode when power is initially applied.

The original two-capacitor circuit (Figure 8) will continue to work as well as it always has, and may continue to be used in applications where cost or space is a critical consideration. It is also easier to tune to frequency since one end of the trimmer capacitor is fixed at the AC ground of the circuit (V_{DD}), minimizing the disturbance cause by contact between the adjustment tool and the trimmer capacitor. Note that in both configurations the load capacitors are connected between the oscillator pins and V_{DD}—do not use V_{SS} as an AC ground.

Table 6: Typical Load Capacitor Values

Crystal Frequency	Load Caps (C_1, C_2)	Trimmer Cap (C_3)
32 kHz	33 pF	5–50 pF
1 MHz	33 pF	5–50 pF
2 MHz	25 pF	5–50 pF
4 MHz	22 pF	5–100 pF

Layout: Due to the extremely low current (and therefore high impedance) design of the ICM7170's oscillator, special attention must be given to the layout of this section. Stray capacitance should be minimized. Keep the oscillator traces on a single layer of the PCB. Avoid putting a ground plane above or below this layer. The traces between the crystal, the capacitors, and the 7170 OSC pins should be as short as possible. Completely surround the oscillator components with a thick trace of V_{DD} to minimize coupling with any digital signals. The final assembly must be free from contaminants such as solder flux, moisture, or any other potential sources of leakage. A good solder mask will help keep the traces free of moisture and contamination over time.

Oscillator Tuning

Trimming the oscillator should be done indirectly. Direct monitoring of the oscillator frequency by probing OSC IN or OSC OUT is not accurate due to the capacitive loading of most probes. One way to accurately trim the 7170 is by turning on the 1 second periodic interrupt and trimming the oscillator until the interrupt period is exactly one second. This can be done as follows:

1) Turn on the system. Write a $00 to the Interrupt Mask Register (location $10) to clear all interrupts.
2) Set the Command Register (location $11) for the appropriate crystal frequency, set the Interrupt Enable and Run/Stop bits to 1, and set the Test bit to 0.
3) Write a $08 to the Interrupt Mask Register to turn on the 1 second interrupt.
4) Write an interrupt handler to read the Interrupt Status Register after every interrupt. This resets the interrupt and allows it to be set again. A software loop that reads the Interrupt Status Register several times each second will accomplish this also.
5) Connect a precision period counter capable of measuring 1 second within the accuracy desired to the interrupt output. If the interrupt is configured as active low, trigger on the falling edge. If the interrupt is active high, trigger on the rising edge. Be sure to measure the period between when the transistor turns ON, and when the transistor turns ON a second later.
6) Adjust C_3 (C_2 for the two-capacitor load configuration) for an interrupt period of exactly 1.000000 seconds.

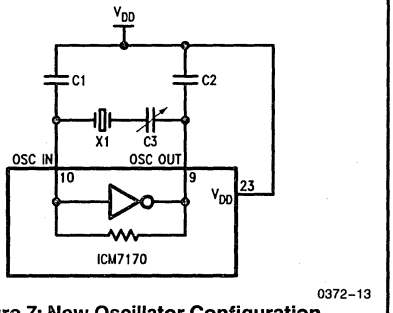


Figure 7: New Oscillator Configuration

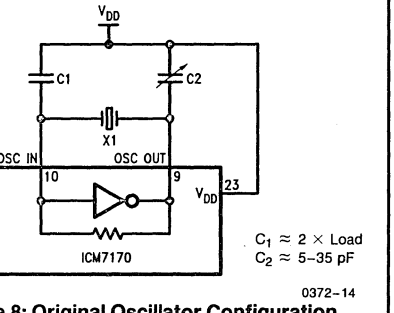


Figure 8: Original Oscillator Configuration

APPLICATION NOTES

Digital Input Termination During Backup

To ensure low current drain during battery backup operation, none of the digital inputs to the 7170 should be allowed to float. This keeps the input logic gates out of their transition region, and prevents crossover current from flowing which will shorten battery life. The address, data, $\overline{CS}$, and ALE pins should be pulled to either V_{DD} or V_{SS}, and the $\overline{RD}$ and $\overline{WR}$ inputs should be pulled to V_{DD}. This is necessary whether the internal battery switchover circuit is used or not.

NOTE: All typical values have been characterized but are not tested.

IBM/PC Evaluation Circuit

Figure 9 shows the schematic of a board that has been designed to plug into an IBM PC/XT* or compatible computer. In this example $\overline{CS}$ is permanently tied low and access to the chip is controlled by the $\overline{RD}$ and $\overline{WR}$ pins. These signals are generated by U1, which gates the IBM's $\overline{IOR}$ and $\overline{IOW}$ with a device select signal from U3, which is functioning as an I/O block address decoder. DS1 selects the interrupt priority.

U5 is used to isolate the ICM7170 from the PC databus for test purposes. It is only required on heavily-loaded TTL databusses—the ICM7170 can drive most TTL and CMOS databusses directly.

Since the IBM PC/XT* requires a positive interrupt transition, the 7170's interrupt output transistor has been configured as a source follower. As a source follower, the interrupt output signal will swing between 0V and 2.5V. When trimming the oscillator, the frequency counter must be triggered on the rising edge of the interrupt signal.

Batteries	Crystals		
Panasonic	Saronix	32kHz	NTF3238
Rayovac	Statek	32kHz	CX-1V
	Seiko	2MHz	GT-38

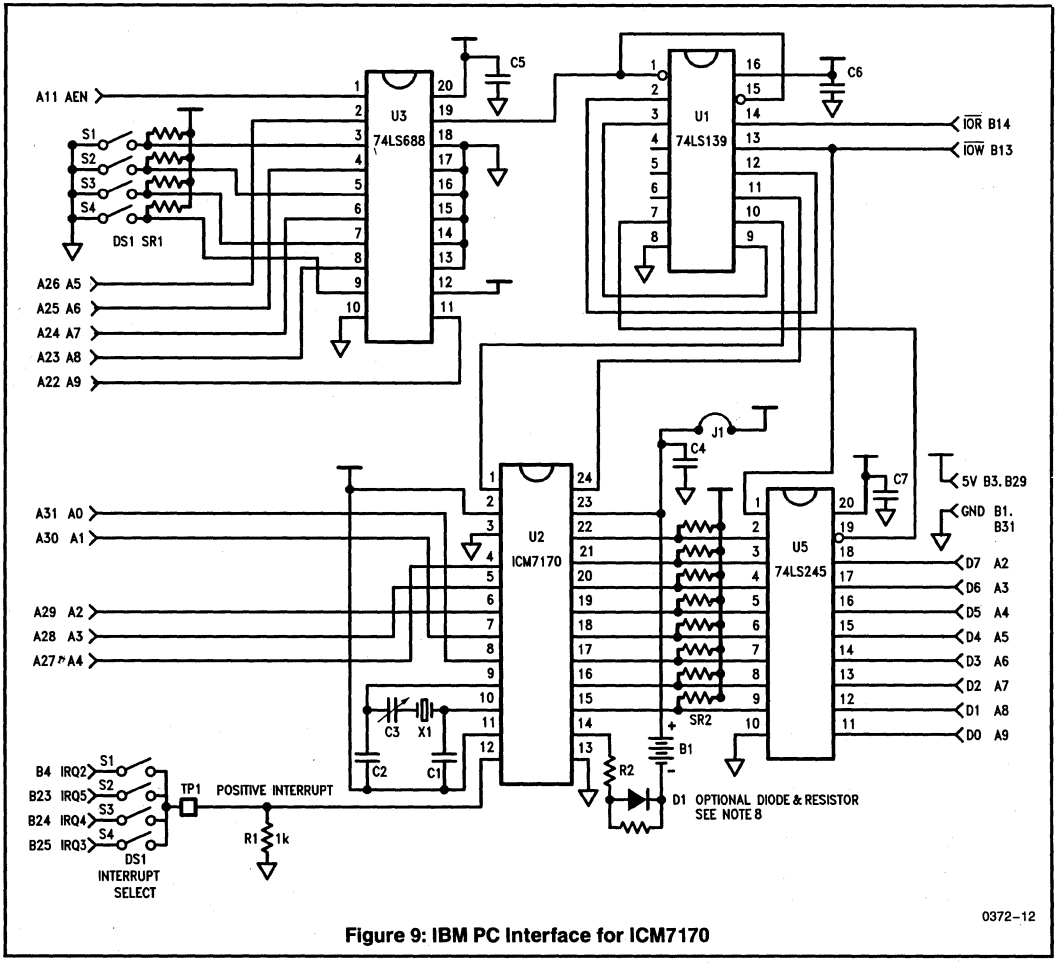


Figure 9: IBM PC Interface for ICM7170

*IBM, IBM PC, and IBM XT are trademarks of IBM Corp.

NOTE: All typical values have been characterized but are not tested.

GENERAL NOTES:

(1) TIME ACCESS

To update the present time registers (Hex 00–07) the 1/100 register must be read first. The 7 real time counter registers (Hours, Minutes, Seconds, Month, Date, Day, and Year) data are latched only if the 1/100 second counter register is read. The 1/100 seconds data itself is not latched. The real time data will be held in the latches until the 1/100 seconds is read again. See the data sheet section on LATCHED DATA. None of the RAM data is latched since it is static by nature.

(2) REGULATED OSCILLATOR

The oscillator's power supply is voltage regulated with respect to V_{dd}. In the 32 kHz mode the regulator's amplitude is $\Sigma Vtn + Vtp$ ($\cong 1.8$). In the 1, 2, and 4 MHz mode the regulator's amplitude is $\Sigma Vtn + Vtn + Vtp$ ($\cong 2.6V$). As a result, signal conditioning is necessary to drive the oscillator with an external signal. In addition, it is also necessary to buffer the oscillator's signal to drive other external clocks because of its reduced amplitude and offset voltage.

(3) INTERNAL BATTERY BACKUP

When the 7170 is using its own internal battery backup circuitry, no other circuitry interfaced to the 7170 should be active during standby operation. When V_{dd} (+5V) is turned off (Standby operation), V_{dd} should equal V_{ss} = 0V. All 7170 I/O should also equal V_{SS}. At this time, the Vbackup pin should be 2.8V to 3.5V below V_{SS} when using a Lithium battery.

(4) EXTERNAL BATTERY BACKUP

The 7170 may be placed on the same power supply as battery-backed up RAM by keeping the 7170 in its operational state and having an external circuit switch between system and backup power for the 7170 and the RAM. In this case V_{BACKUP} should be pulled up to V_{DD} through a 2k resistor. Although the 7170 is always "on" in this configuration, its current consumption will typically be less than a microamp greater than that of standby operation at the same supply voltage. (See Note 9.)

Proper consideration must be given to disabling the 7170's and the RAM's I/O before system power is removed. This is important because many microprocessors can generate spurious write signals when their supply falls below their specified operating voltage limits. NANDing $\overline{CS}$ (or $\overline{WR}$) with a POWERGOOD signal will create a $\overline{CS}$ (or $\overline{WR}$) that is only valid when system power is within specifications. The POWERGOOD signal should be generated by an accurate supply monitor such as the ICL7665 under/over voltage detector.

An alternate method of disabling the 7170's I/O is to pull V_{BACKUP} down to under a volt above V_{SS} ($V_{SS} < V_{BACKUP} < 1.0V$). This will cause the 7170 to internally disable all I/O. Do not allow V_{BACKUP} to equal V_{SS}, since this could cause oscillation of the battery backup comparator (See Figure 6). $V_{BACKUP} = V_{SS} + 0.5V$ will disable the I/O and provide enough overdrive for the comparator.

(5) 7170A PART

The 7170A part is binned at final test for a 32.768 kHz maximum current of 5 μA. All other specifications remain the same.

(6) INTERRUPTS

The Interrupt Status Register (address $10) always indicates which of the real time counters have been incremented since the last time the register was read. NOTE: This is independent of whether or not any mask bits are set.

The status register is always reset immediately after it is read. If an interrupt from the 7170 has occurred since the last time the status register was read, bit D7 of the register will be set. If the source was an alarm interrupt, bit D0 will also be set. If the interrupt transistor has been turned on, reading the Interrupt Status Register will reset it.

To enable the periodic interrupt, both the Command Register's Interrupt Enable bit (D4) and at least one bit in the Interrupt Mask Register (D1–D6) must be set to a 1. The periodic interrupt is triggered when the counter corresponding to a mask bit that has been set is incremented. For example, if you enable the 1 second interrupt when the current value in the 100ths counter is 57, the first interrupt will occur 0.43 seconds later. All subsequent interrupts will be exactly one second apart. The interrupt service routine should then read the Interrupt Status Register to reset the interrupt transistor and, if necessary, determine the cause of the interrupt (periodic, alarm, or non-7170 generated) from the contents of the status register.

To enable the alarm interrupts, both the Command Register's Interrupt Enable bit (D4) and the Interrupt Mask Register's Alarm bit (D0) must be set to a 1. Each time there is an exact match between the values in the alarm register and the values in the real time counters, bits D0 and D7 of the Interrupt Status Register will be set to a 1 and the N-channel interrupt transistor will be turned on. As with a periodic interrupt, the service routine should then read the Interrupt Status Register to reset the interrupt transistor and, since periodic and alarm interrupts may be simultaneously enabled, determine the cause of the interrupt if necessary.

Mask bits: The 7170 alarm interrupt compares the data in the alarm registers with the data in the real time registers, ignoring any registers with the mask bit set. For example, if the alarm register is set to 11-23-95 (Month-Day-Year), 10:59:00:00 (Hour-Minutes-Seconds-Hundredths), and DAY = XX (XX = masked off), the alarm will generate a single interrupt at 10:59 on November 23, 1995. If the alarm register is set to 11-XX-95, 10:XX:00:00, and DAY = 2 (2 = Tuesday); the alarm will generate one interrupt every minute from 10:00–10:59 on every Tuesday in November, 1995.

NOTE: Masking off the 100ths of a second counter has the same effect as setting it to 00.

(7) RESISTOR IN SERIES WITH BATTERY

A 2k resistor (R2) must be placed in series with the battery backup pin of the 7170. The UL laboratories have requested the resistor to limit the charging and discharging current to the battery. The resistor also serves the purpose of degenerating parasitic SCR action. This SCR action may occur if an input is applied to the 7170, outside of its supply voltage range, while it is in the standby mode.

10

NOTE: All typical values have been characterized but are not tested.

GENERAL NOTES: (Continued)

(8) V_{BACKUP} DIODE

Lithium batteries may explode if charged or if discharged at too high a rate. These conditions could occur if the battery was installed backwards or in the case of a gross component failure. A 1N914-type diode placed in series with the battery as shown in Figure 9 will prevent this from occurring. A resistor of 2 MΩ or so should parallel the diode to keep the V_{BACKUP} terminal from drifting toward the V_{SS} terminal and shutting off 7170 I/O during normal operation.

(9) SUPPLY CURRENT

7170 supply current is predominantly a function of oscillator frequency and databus activity. The lower the oscillator frequency, the lower the supply current. When there is little or no activity on the data, address or control lines, the current consumption of the 7170 in its operational mode approaches that of the backup mode.

NOTE: All typical values have been characterized but are not tested.

DATA ACQUISITION 11

COUNTERS WITH DISPLAY DRIVERS/TIMEBASE GENERATORS

HARRIS SEMICONDUCTOR

ICM7207/A
CMOS Timebase Generator

GENERAL DESCRIPTION

The ICM7207/A consist of a high stability oscillator and frequency divider providing 4 control outputs suitable for frequency counter timebases. Specifically, when used as a frequency counter timebase in conjunction with the ICM7208, ICM7224 or ICM7225 display counters, the four outputs provide the gating signals for the count window, store function, reset function and multiplex frequency reference. Additionally, the duration of the count window may be changed by a factor of 10 to provide a 2 decade range counting system.

The normal operating voltage of the ICM7207/A is 5 volts. The typical power dissipation is less than 2mW when using an oscillator frequency of 6.5536MHz with the 7207 and 5.24288MHz with the 7207A.

ORDERING INFORMATION

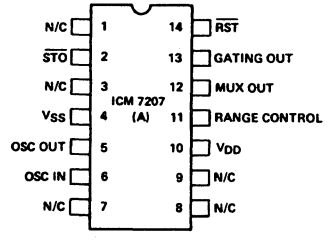
Order Number	Temperature Range	Package
ICM7207IPD	−25°C to +85°C	14-Pin PLASTIC DIP
ICM7207AIPD	−25°C to +85°C	14-Pin PLASTIC DIP

FEATURES

- **Stable HF Oscillator**
- **Low Power Dissipation ≤ 2mW With 5 Volt Supply**
- **Counter Chain Has Outputs at $\div 2^{12}$ and $\div 2^n$ or $\div(2^n \times 10)$; n = 17 for 7207, and 20 for 7207A**
- **Low Impedance Output Drivers ≤ 100 Ohms**
- **Count Windows of 10/100ms (7207 With 6.5536MHz Crystal) or 0.1/1 Sec. (7207A With 5.24288MHz Crystal)**

APPLICATIONS

- **System Timebases**
- **Oscilloscope Calibration Generators**
- **Marker Generator Strobes**
- **Frequency Counter Controllers**



0348-1

Figure 1: Pin Configuration (Outline dwg PD)

202200-004

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD}-V_{SS}$) 6.0V
Input Voltages ..... $V_{SS}-0.3V$ to $V_{DD}+0.3V$
Output Voltages:
7207 ..... V_{SS} to +6V
7207A ..... V_{DD} to V_{SS}

Output Currents 25mA
Power Dissipation @ 25°C Note 1 ..... 200mW
Operating Temperature Range ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE 1: Derate by 2mW/°C above 25°C.

Absolute maximum ratings refer to values which if exceeded may permanently change or destroy the device.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

$f_{osc}=6.5536$MHz(7207), 5.24288MHz(7207A), $V_{DD}=5V$, $T_A=25°C$, $V_{SS}=0V$, test circuit unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{DD}	Operating Voltage Range	−20°C to +85°C	4		5.5	V
I_{DD}	Supply Current	All outputs open circuit		260	1000	μA
$R_{ds}(on)$	Output Low Resistances	Output current = 5mA sink All outputs		50	120	Ω
I_{OLK}	Output Leakage Currents	All outputs ($\overline{STORE}$ only)			50	μA
R_{OUT}	Output High Resistance Terminals 12,13,14	Output current = 50μA source, 7207A only			33K	Ω
I_{pd}	Input Pulldown Current	Terminal 11 connected to V_{DD}		50	200	μA
	Input Noise Immunity		25			% supply voltage
f_{osc}	Oscillator Frequency Range	Note 2	2		10	MHz
f_{STAB}	Oscillator Stability	$C_{IN}=C_{OUT}=22pF$		0.2	1.0	ppm/V
r_{OSC}	Oscillator Feedback Resistance	Quartz crystal open circuit Note 3	3			MΩ

NOTES: 2. Dynamic dividers are used in the initial stages of the divider chain. These dividers have a lower frequency of operation determined by transistor sizes, threshold voltages and leakage currents.
3. The feedback resistor has a non-linear value determined by the oscillator instantaneous input and output voltage voltages and the supply voltage.

NOTE: All typical values have been characterized but are not tested.

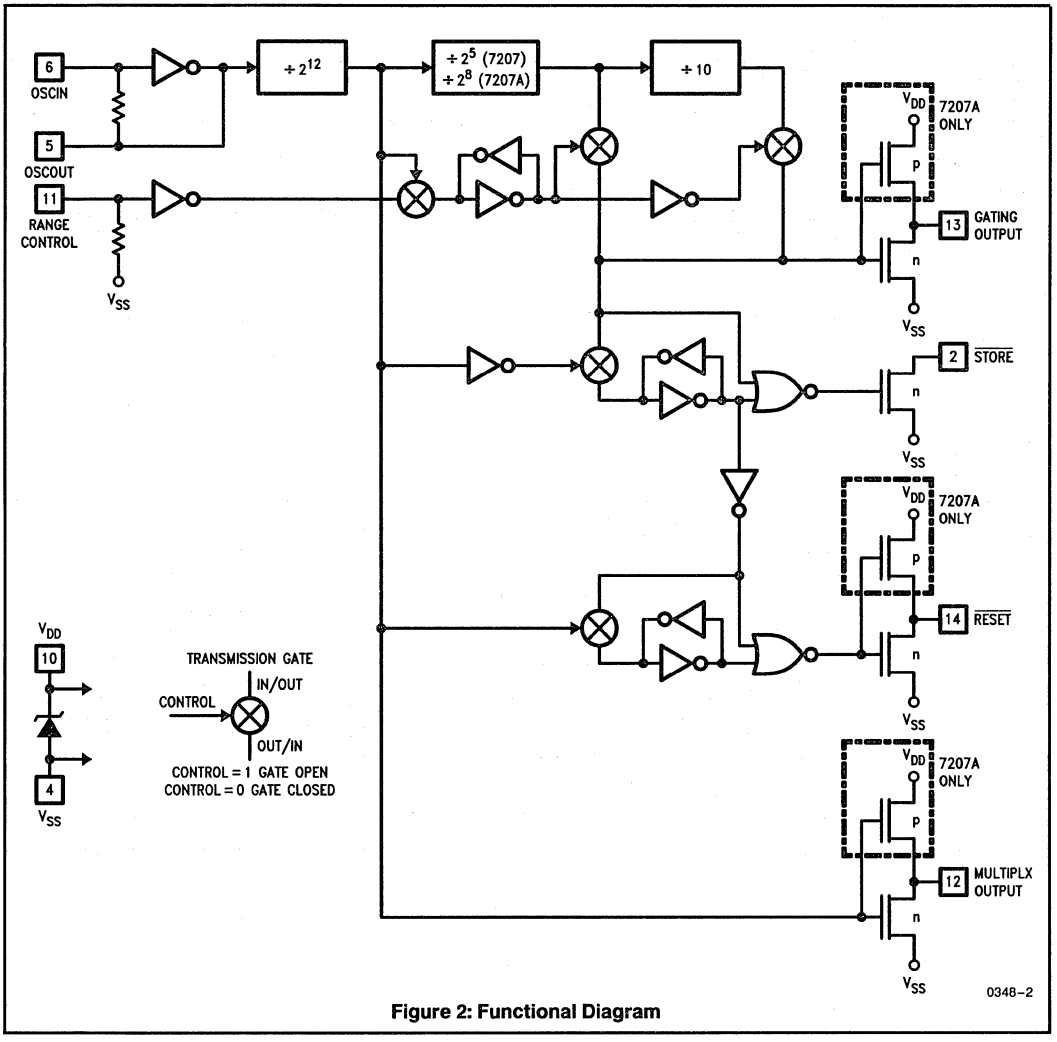
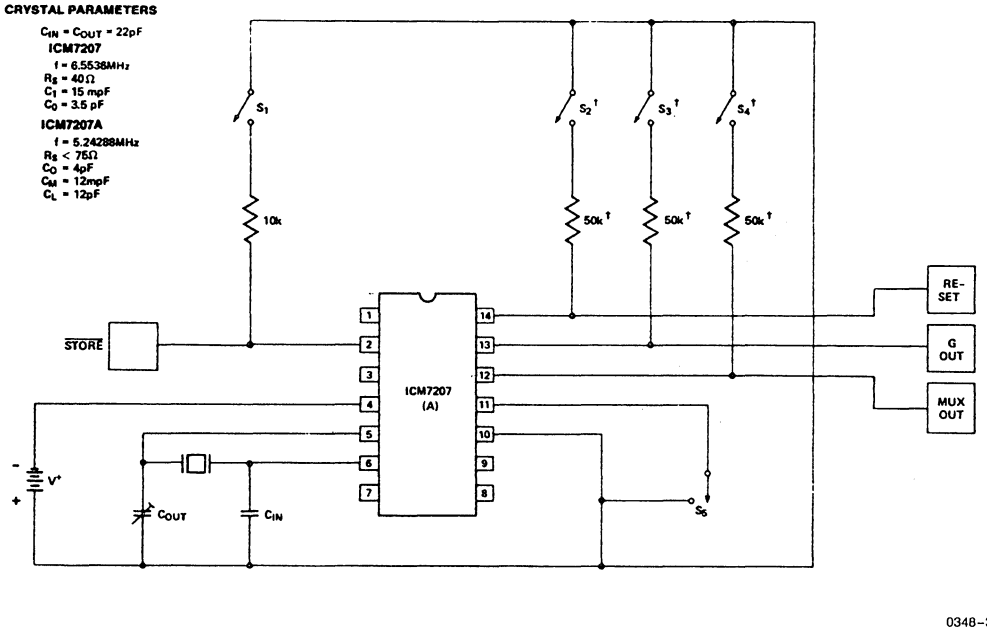


Figure 2: Functional Diagram

NOTE: All typical values have been characterized but are not tested.



SWITCHES S_1, S_2, S_3, S_4 OPEN CIRCUIT FOR SUPPLY CURRENT MEASUREMENT.

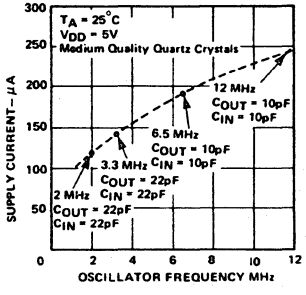
SWITCH S_5 OPEN CIRCUIT FOR SLOW GATING PERIOD.

† SWITCHES S_2, S_3, S_4 and 50k RESISTORS ARE NOT NEEDED WHEN USING THE ICM7207A.

Figure 3: Test Circuit

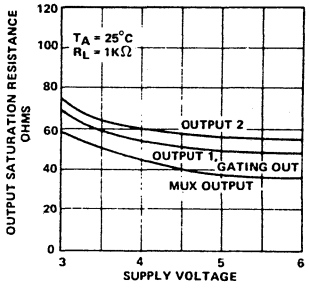
TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY



0348-4

OUTPUT SATURATION RESISTANCES AS A FUNCTION OF SUPPLY VOLTAGE

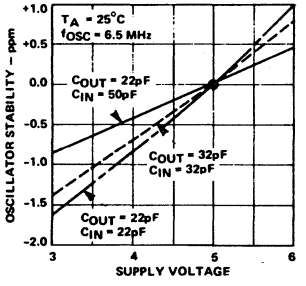


0348-5

NOTE: All typical values have been characterized but are not tested.

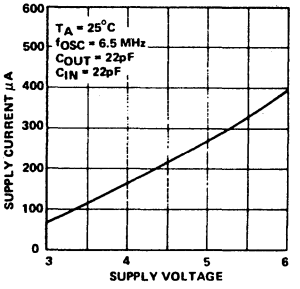
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE



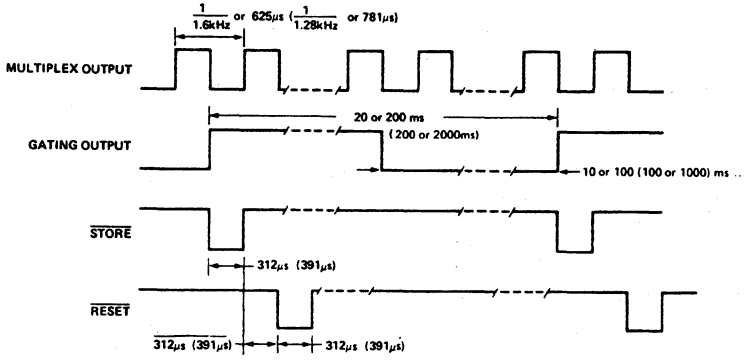
0348-6

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



0348-7

OUTPUT TIMING WAVEFORMS 7207 (7207A)
Crystal Frequency = 6.5536(5.24288)MHz



0348-8

Figure 4: Output Waveform

DETAILED DESCRIPTION

Referring to the Test Circuit, Figure 3, and waveforms, Figure 4, the crystal oscillator frequency is divided by 2^{12} to provide both the multiplex frequency and generate the output pulse widths. The GATING OUTPUT provides a 50% duty cycle signal whose period depends upon whether the RANGE CONTROL terminal is connected to V_{DD} or V_{SS} (open circuit).

OUTPUTS CONSIDERATIONS

In the ICM7207 version all the outputs (MUltipleX, GATING OUT, STOre and ReSeT) are open drain and need pull up resistors as shown in Figure 3.

In the ICM7207A version the MUltipleX, GATING OUT and ReSeT outputs provide both active pull up and pull down, eliminating the need for 3 external resistors, although, buffering is required if interfacing with TTL logic family. See the electrical characteristics for outputs source and sink resistances. The STOre output is still open drain in 7207A version.

OSCILLATOR CONSIDERATIONS

The oscillator consists of a CMOS inverter with a non-linear resistor connected between the input and output terminals to provide biasing. Oscillator stabilities of approximately 0.1 ppm per 0.1 volt change are achievable at a supply voltage of 5 volts, using low cost crystals. The crystal specifications are shown in the TEST CIRCUIT.

It is recommended that the crystal load capacitance (C_L) be no greater than 15pF for a crystal having a series resistance equal to or less than 75Ω, otherwise the output amplitude of the oscillator may be too low to drive the divider reliably.

NOTE: All typical values have been characterized but are not tested.

If a very high quality oscillator is desired, it is recommended that a quartz crystal be used having a tight tuning tolerance ±10ppm, a low series resistance (less than 25Ω), a low motional capacitance of 5fF and a load capacitance of 15pF. The fixed capacitor C_{IN} should be 39pF and the oscillator tuning capacitor should range between approximately 8 and 60pF.

Use of a high quality crystal will result in typical oscillator stabilities of 0.05ppm per 0.1 volt change of supply voltage.

FREQUENCY LIMITATIONS

The ICM7207/A uses dynamic frequency counters in the initial divider sections. Dynamic frequency counters are faster and consume less power than static dividers but suffer from the disadvantage that there is a minimum operating frequency at a given supply voltage.

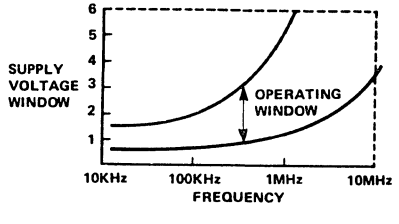


Figure 5

For example, if instead of 6.5MHz, a 1MHz oscillator is required, it is recommended that the supply voltage be reduced to between 2 and 2.5 volts. This may be realized by using a series resistor in series with the 5V positive supply line plus a decoupling capacitor. The quartz crystal parameters, etc., will determine the value of this resistor. NOTE: Except for the output open drain n-channel transistors no other terminal is permitted to exceed the supply voltage limits.

APPLICATION

A PRACTICAL FREQUENCY COUNTER

A complete frequency counter using the ICM7207/A together with the ICM7208 Frequency Counter is described in the ICM7208 data sheet. Other frequency counters using the ICM7207/A can be constructed using the ICM7224 and ICM7225, for LCD and LED displays. The latter are available as EV/Kits also.

QUARTZ CRYSTAL MANUFACTURERS

The following list of possible suppliers is intended to be of assistance in putting a design into production. It should not be interpreted as a comprehensive list of suppliers, nor does it constitute an endorsement by Harris.

a) CTS Knights, Sandwich, Illinois, (815) 786-8411

b) Motorola Inc., Franklin Park, Illinois (708) 451-1000

c) Sentry Manufacturing Co., Chickasaw, Oklahoma (405) 224-6780

d) Tyco Filters Division, Phoenix, Arizona (602) 272-7945

e) M-Tron Inds., Yankton, South Dakota (605) 665-9321

f) Saronix, Palo Alto, California (415) 856-6900

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICM7208
7-Digit LED Display Counter

GENERAL DESCRIPTION

The ICM7208 is a fully integrated seven decade counter-decoder-driver.

Specifically the ICM7208 provides the following on chip functions: a 7 decade counter, multiplexer, 7 segment decoder, digit & segment driver, plus additional logic for display blanking, reset, input inhibit, and display on/off.

For unit counter applications the only additional components are a 7 digit common cathode display, 3 resistors and a capacitor to generate the multiplex frequency reference, and the control switches.

The ICM7208 is intended to operate over a supply voltage of 2 to 6 volts as a medium speed counter, or over a more restricted voltage range for high frequency applications.

As a frequency counter it is recommended that the ICM7208 be used in conjunction with the ICM7207 Oscillator Controller, which provides a stable HF oscillator, and output signals for enable, store and reset.

FEATURES

- **Low Operating Power Dissipation < 10mW**
- **Low Quiescent Power Dissipation < 5mW**
- **Counts and Displays 7 Decades**
- **Wide Operating Supply Voltage Range $2V \leq V_{DD} \leq 6V$**
- **Drives Directly 7 Decade Multiplexed Common Cathode LED Display**
- **Internal Store Capability**
- **Internal Inhibit for Counter Input**
- **Test Speedup Point**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7208IPI	−25°C to +85°C	28 Lead Plastic DIP

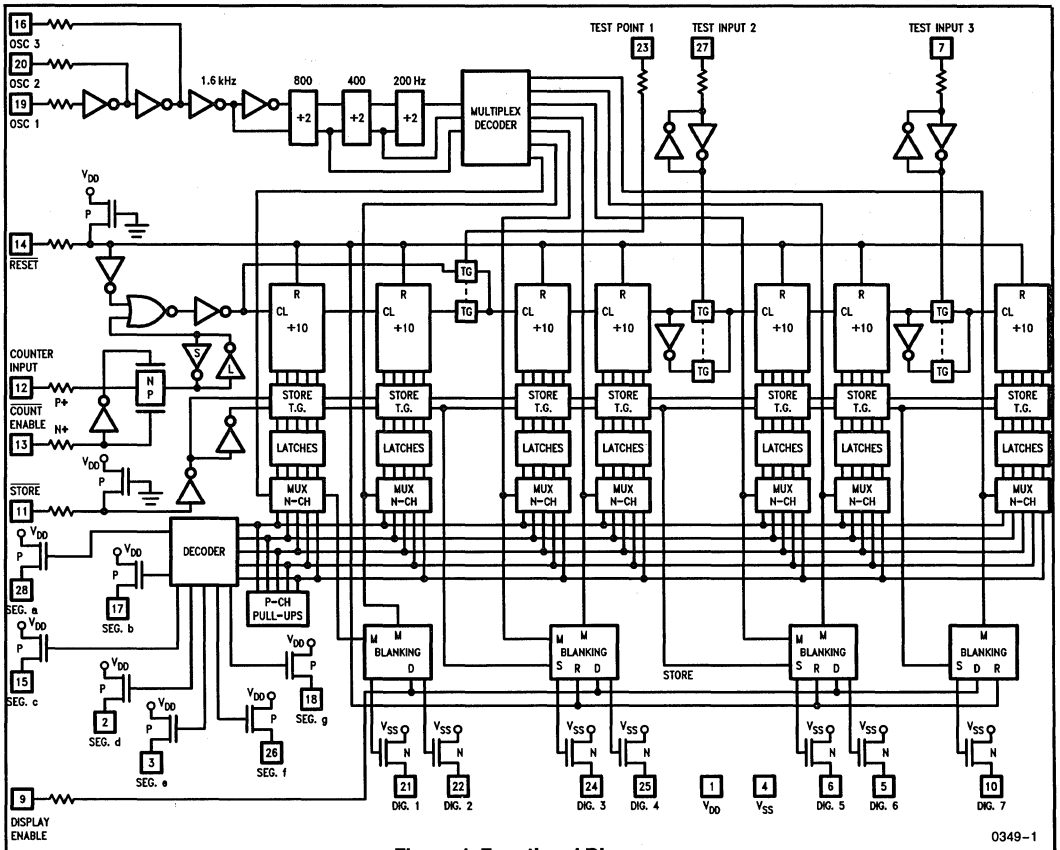


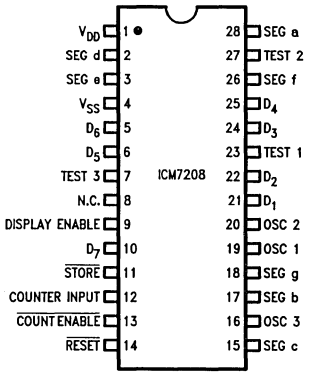
Figure 1: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 2) ($V_{DD}-V_{SS}$) 6V
Input Voltage Range (any input terminal)
(Note 2) ..... $V_{SS}-0.3V$ to $V_{DD}+0.3V$
Output Digit Drive Current (Note 3) 150mA
Output Segment Drive Current 30mA
Power Dissipation (Note 1) 1W
Operating Temperature Range ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*



0349-2

Figure 2: Pin Configuration (Outline Drawing PI)

ELECTRICAL CHARACTERISTICS ($V_{DD}=5V$, $V_{SS}=0V$, $T_A=25°C$, display off, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{Q1}	Quiescent Current	All controls plus terminal 19 connected to V_{DD} No multiplex oscillator		30	300	μA
I_{Q2}	Quiescent Current	All control inputs plus terminal 19 connected to V_{DD} except STORE which is connected to V_{SS}		70	350	
I_{DD1}	Operating Supply Current	All inputs connected to V_{DD}, RC multiplexer osc operating $f_{in}<25kHz$		210	500	
I_{DD2}	Operating Supply Current	$f_{in}=2MHz$			700	
V_{SUPPLY}	Supply Voltage Range	$f_{in}\leq 2MHz$	3.5		5.5	V
R_{DIG}	Digit Driver On Resistance			4	12	Ω
I_{DIG}	Digit Driver Leakage Current				500	μA
r_{SEG}	Segment Driver On Resistance			40		Ω
I_{SLK}	Segment Driver Leakage Current				500	μA
R_p	Pullup Resistance of RESET or STORE Inputs		100	400		kΩ
R_{IN}	COUNTER INPUT Resistance	Terminal 12 either at V_{DD} or V_{SS}			100	
V_{HIN}	COUNTER INPUT Hysteresis Voltage			25	50	mV

NOTES: 1. This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.
2. The supply voltage must be applied before or at the same time as any input voltage. This poses no problems with a single power supply system. If a multiple power supply system is used, it is mandatory that the supply for the ICM7208 is switched on before the other supplies otherwise the device may be permanently damaged.
3. The output digit drive current must be limited to 150mA or less under steady state conditions. (Short term transients up to 250mA will not damage the device.) Therefore, depending upon the LED display and the supply voltage to be used it may be necessary to include additional segment series resistors to limit the digit currents.

NOTE: All typical values have been characterized but are not tested.

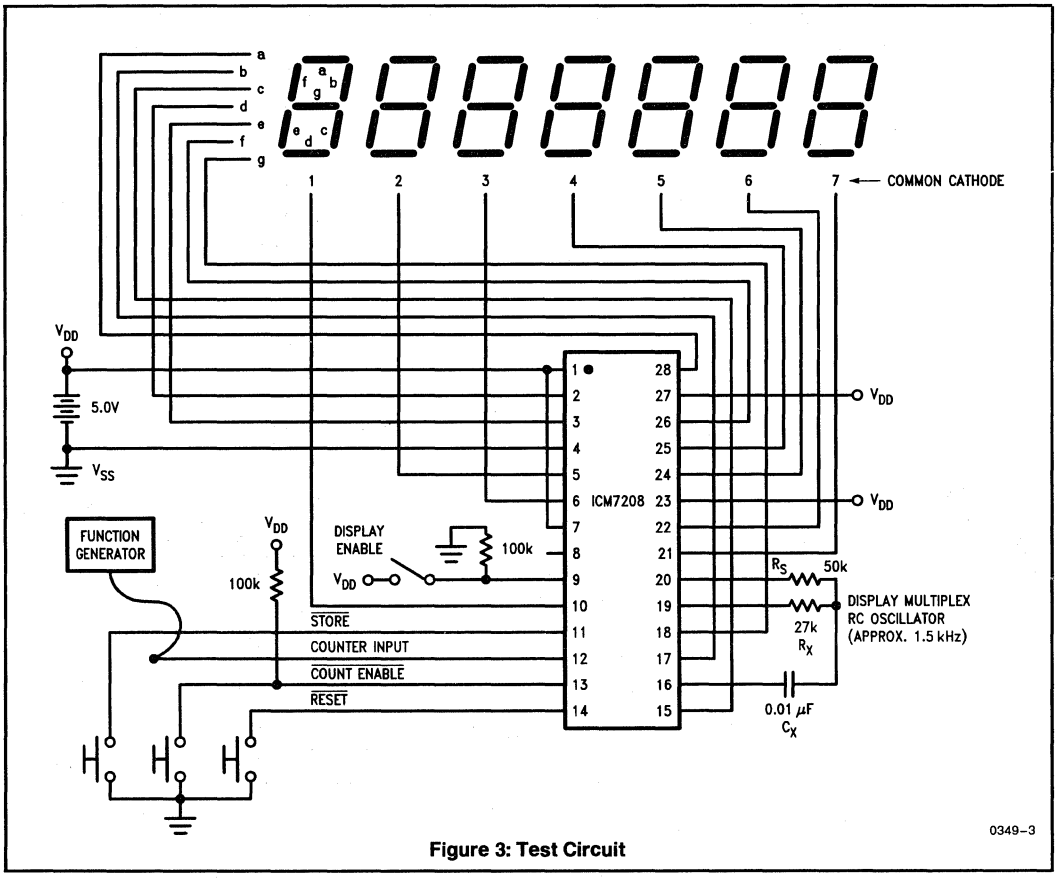
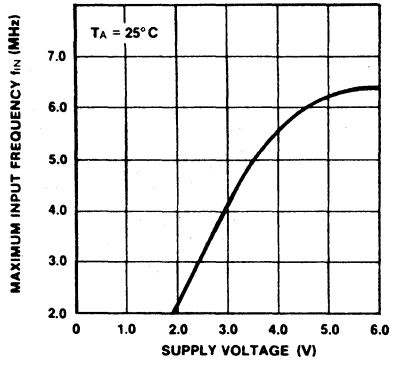


Figure 3: Test Circuit

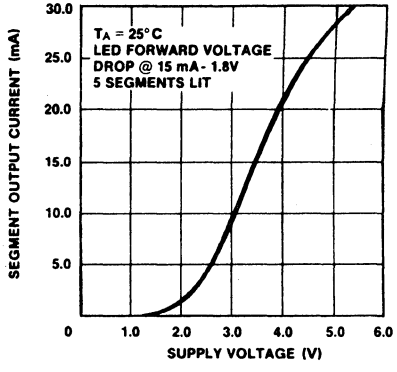
TYPICAL PERFORMANCE CHARACTERISTICS

MAXIMUM COUNTER INPUT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



0349-4

SEGMENT OUTPUT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

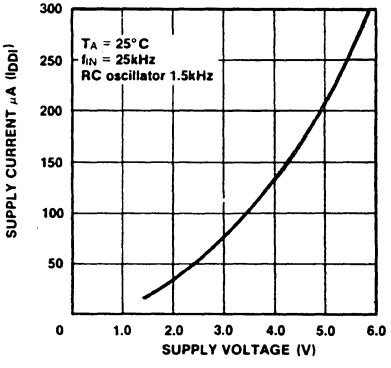


0349-5

NOTE: All typical values have been characterized but are not tested.

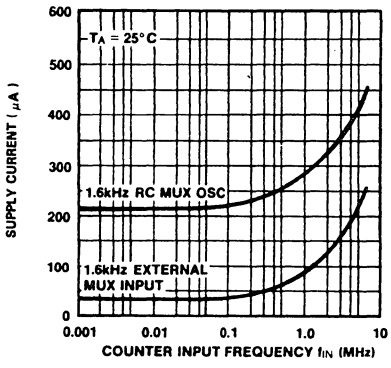
TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



0349-6

SUPPLY CURRENT AS A FUNCTION OF COUNTER INPUT FREQUENCY



0349-7

DETAILED DESCRIPTION

Test Inputs

The ICM7208 is provided with three input terminals 7, 23, 27 which may be used to accelerate testing. The least two significant decade counters may be tested by applying an input to the 'COUNTER INPUT' terminal 12. 'TEST POINT' terminal 23 provides an input which bypasses the 2 least significant decade counters and permits an injection of a signal into the third decade counter. Terminals 7 and 27 permit rapid counter advancing at two points along the string of decade counters. These test inputs must be tied to V_{DD} for normal operation of the device.

CONTROL INPUT DEFINITIONS

Input	Terminal	Voltage	Function
DISPLAY ENABLE	9	V_{DD} V_{SS}	Display On Display Off
$\overline{\text{STORE}}$	11	V_{DD} V_{SS}	Counter Information Latched Counter Information Transferring
$\overline{\text{COUNT}}$ $\overline{\text{ENABLE}}$	13	V_{DD} V_{SS}	Input to Counter Blocked Normal Operation
$\overline{\text{RESET}}$	14	V_{DD} V_{SS}	Normal Operation Counters Reset

COUNTER INPUT

The internal counters of the ICM7208 index on the negative edge of the input signal at terminal #12.

The noise immunity of the COUNTER INPUT Terminal is approximately ⅓ the supply voltage. Consequently, the input signal should be at least 50% of the supply in peak to peak amplitude and preferably equal to the supply.

The optimum input signal is a 50% duty cycle square wave equal in amplitude to the supply. However, as long as the rate of change of voltage is not less than approximately 10^{-4} V/μs, at 50% of the power supply voltage, the input waveshape can be sinusoidal, triangular, etc.

When driving the input of the ICM7208 from TTL, a 1k – 5kΩ pull-up resistor to the positive supply must be used to increase peak to peak input signal amplitude.

Display Considerations

Any common cathode multiplexable LED display may be used. However, if the peak digit current could exceed 150mA for any prolonged time, it is recommended that resistors be included in series with the segment outputs to limit digit current to 150mA.

The ICM7208 is specified with 500μA of possible digit leakage current. With certain new LED displays that are extremely efficient at low currents, it may be necessary to include resistors between the cathode outputs and the positive supply to bleed off this leakage current.

Display Multiplex Rate

The ICM7208 has approximately 0.5μs overlap between display drive signals. Therefore, if the multiplex rate is very fast, digit ghosting will occur. The ghosting determines the upper limit for the multiplex frequency. At very low multiplex rates flicker becomes visible.

NOTE: All typical values have been characterized but are not tested.

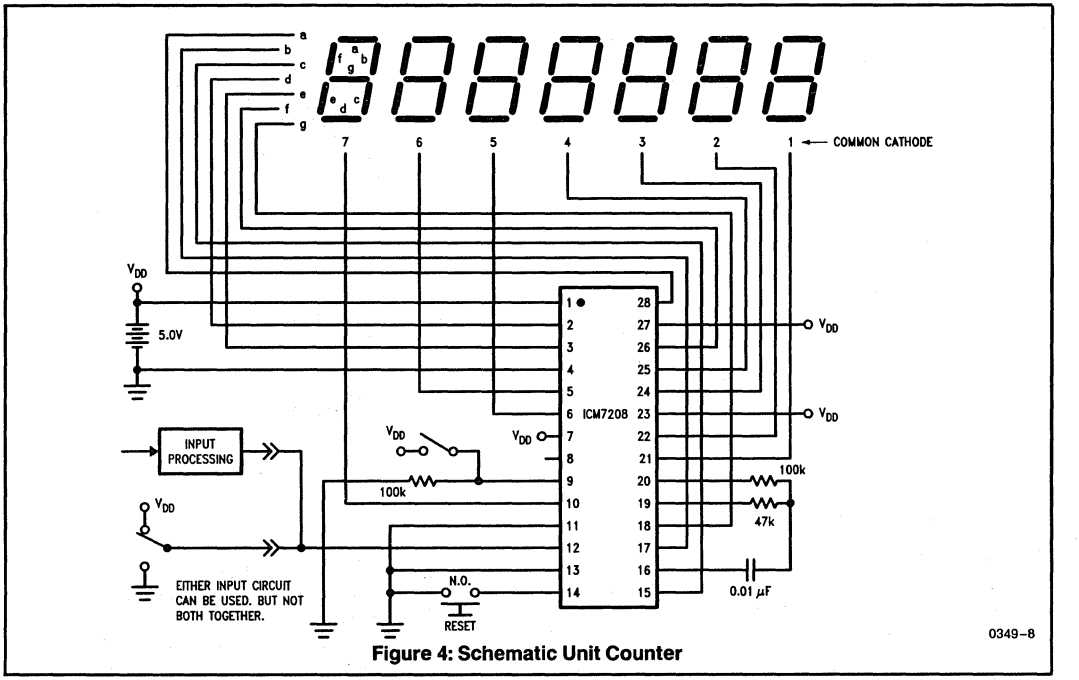


Figure 4: Schematic Unit Counter

It is recommended that the display multiplex rate be within the range of 50Hz to 200Hz, which corresponds to 400Hz to 1600Hz for the multiplex frequency input. For stand alone systems, two inverters are provided so that a simple but stable RC oscillator may be built using only 2 resistors and a capacitor.

The multiplex oscillator is eight times the multiplex rate. The frequency is given using the following formulii:

$$f = \frac{1}{2.2R_xC_x}$$

R_S should always be $\leq 1M\Omega$ and $R_S = kR_X$ where k is in the range 2-10 (See Figure 3).

An external generator may be used to provide the multiplex frequency input. This signal, applied to terminal 19 (terminals 16 and 20 open circuit), should be approximately equal to the supply voltage, and should be a square wave for minimum of power dissipation.

Unit Counter

Figure 4 shows the schematic of an extremely simple unit counter that can be used for remote traffic counting, to name one application. The power cell stack should consist of 3 or 4 nickel cadmium rechargeable cells (nominal 3.6 or 4.8 volts). If 4×1.5 volt cells are used it is recommended that a diode be placed in series with the stack to guarantee that the supply voltage does not exceed 6 volts.

The input switch is shown to be a single pole double throw switch (SPDT). A single pole single throw switch (SPST) could also be used (with a pullup resistor), however, anti-bounce circuitry must be included in series with the counter input. In order to avoid contact bounce problems due to the SPDT switch the ICM7208 contains an input latch on chip.

The unit counter updates the display for each negative transition of the input signal. The information on the display will count, after reset, from 00 to 9,999,999 and then reset to 0000000 and begin to count up again. To blank leading zeros, actuate reset at the beginning of a count. Leading zero blanking affects two digits at a time.

For battery operated systems the display may be switched off to conserve power.

Frequency Counter

The ICM7208 may be used as a frequency counter when used with an external frequency reference and gating logic. This can be achieved using the ICM7207 Oscillator Controller (Figure 5). The ICM7207 uses a crystal controlled oscillator to provide the store and reset pulses together with the counting window. Figure 6 shows the recommended input gating waveforms to the ICM7208. At the end of a counting period (50% duty cycle) the counter input is inhibited. The counter information is then transferred and stored in latches, and can be displayed. Immediately after this information is stored, the counters are cleared and are ready to start a new count when the counter input is enabled.

Using a 6.5536MHz quartz crystal and the ICM7207 driving the ICM7208, two ranges of counting may be obtained, using either 0.01 sec or 0.1 sec counter enable windows.

Previous comments on leading zero blanking, etc., apply as per the unit counter.

The ICM7207 provides the multiplex frequency reference of 1.6kHz.

NOTE: All typical values have been characterized but are not tested.

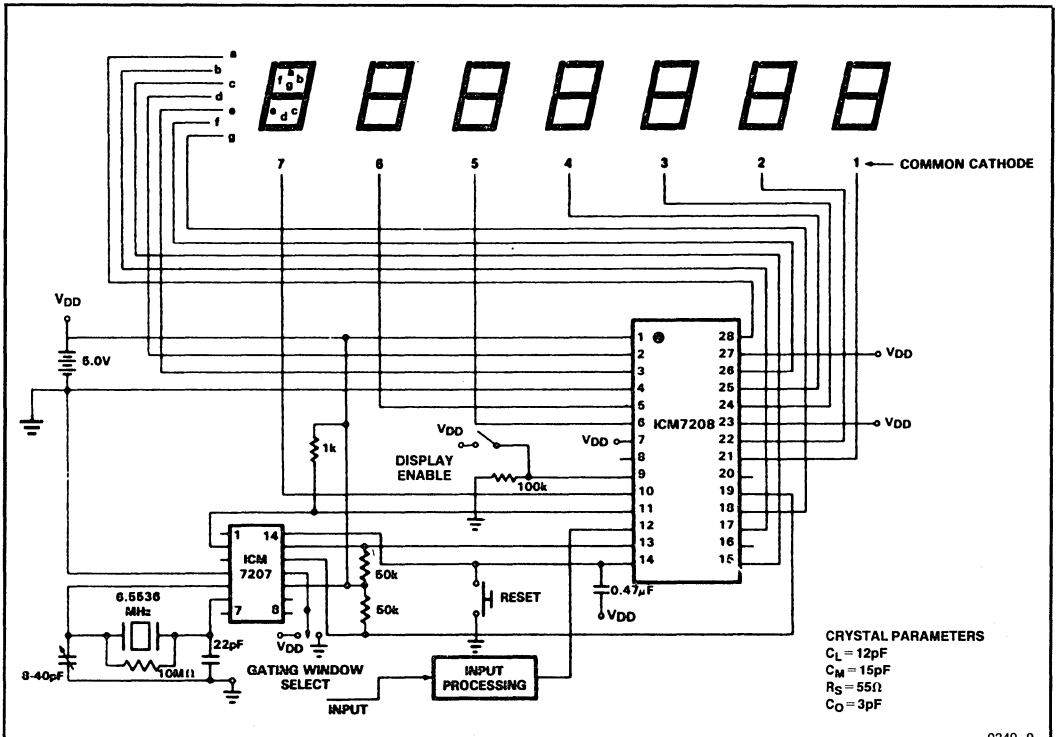


Figure 5: Frequency Counter

Note: For a 1 sec count window which allows all 7 digits to be used with a resolution of 1Hz, the ICM7207 can be replaced with the ICM7207A. Circuit details are given on the 7207A data sheet.

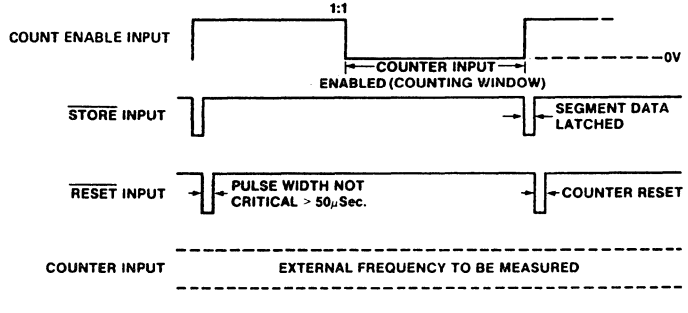


Figure 6: Frequency Counter Input Waveforms

NOTE: All typical values have been characterized but are not tested.

Period Counter

For this application, as opposed to the frequency counter, the gating and the input signal to be measured are reversed compared to the frequency counter. The input period is divided by two to produce a single polarity signal (50% duty cycle) equal to the input period, which is used to gate the frequency reference (1MHz in this case). Figure 8 shows a block schematic of the input waveform generator. The 1MHz frequency reference is generated by the ICM7209 Clock Generator using an 8MHz oscillator frequency and internally dividing this frequency by 8. Alternatively, a 1MHz signal could be applied directly to COUNTER INPUT. Waveforms are shown in Figure 7.

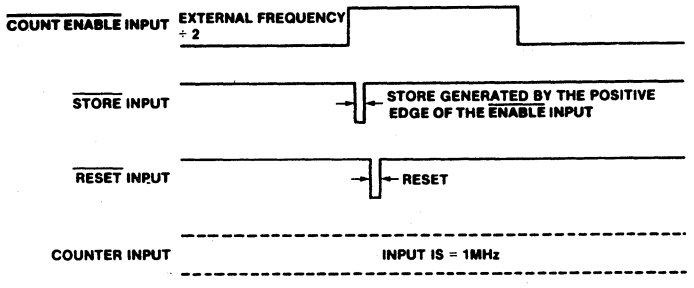


Figure 7: Period Counter Input Waveforms

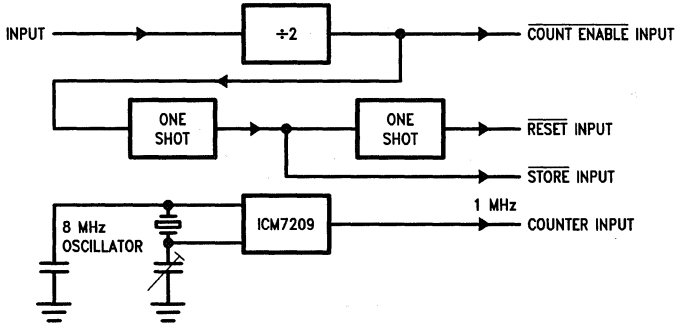


Figure 8: Period Counter Input Generator

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICM7209
Timebase Generator

GENERAL DESCRIPTION

The Harris ICM7209 is a versatile CMOS clock generator capable of driving a number of 5 volt systems with a variety of input requirements. When used to drive up to 5 TTL gates, the typical rise and fall times are 10ns.

The ICM7209 consists of an oscillator, a buffered output equal to the oscillator frequency and a second buffered output having an output frequency one-eighth that of the oscillator. The guaranteed maximum oscillator frequency is 10MHz. Connecting the DISABLE terminal to the negative supply forces the ÷8 output into the '0' state and the OUT1 into the '1' state.

FEATURES

- **High Frequency Operation — 10MHz Guaranteed**
- **Requires Only A Quartz Crystal and Two Capacitors**
- **Bipolar, CMOS Compatibility**
- **High Output Drive Capability — 5×TTL Fanout With 10ns Rise and Fall Times**
- **Low Power — 50mW at 10MHz**
- **Choice of Two Output Frequencies — Osc., and Osc. ÷ 8 Frequencies**
- **Disable Control for Both Outputs**
- **Wide Industrial Temperature Range — 20°C to +85°C**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7209IPA	−20°C to +85°C	8 pin PLASTIC

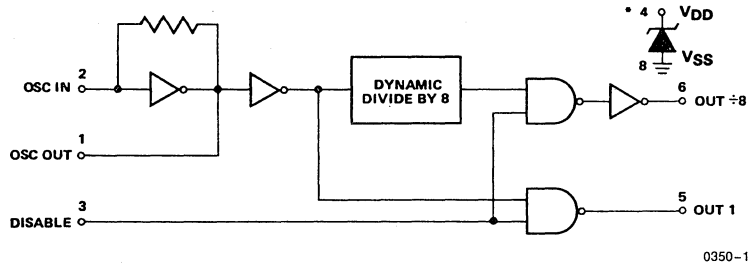


Figure 1: Functional Diagram

*Zener Voltage is Typically 6.3 Volts

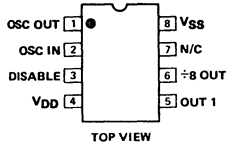


Figure 2: Pin Configuration (Outline dwg PA)

Pin 1 is designated by either a dot or a notch

11

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6V
Output Voltages ..... $V_{SS}-0.3V$ to $V_{DD}+0.3V$
Input Voltages ..... $V_{SS}-0.3V$ to $V_{DD}+0.3V$

Power Dissipation (25°C) 300mW
Storage Temperature ..... −55°C to +125°C
Operating Temperature Range ..... −20°C to +85°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

($V_{DD}-V_{SS}=5V$, test circuit, $f_{osc}=10MHz$, $T_A=25°C$ unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Supply Current	Note 1 No Load		11	20	mA
C_D	Disable Input Capacitance			5		pF
I_{ILK}	Disable Input Leakage	Either '1' or '0' state			±10	μA
V_{OL}	Output Low State	Either OUT 1 or OUT ÷8 simulated 5×TTL loads			0.4	V
V_{OH}	Output High State	Either OUT 1 or OUT ÷8 simulated 5×TTL loads	4.0	4.9		V
t_R	Output Rise Time (Note 3)	Either OUT 1 or OUT ÷8 simulated 5×TTL loads		10		ns
t_F	Output Fall Time (Note 3)	Either OUT 1 or OUT ÷8 simulated 5×TTL loads		10		ns
f_{OSC}	Minimum OSC Frequency for ÷8 Output	Note 2	2			MHz
	Output ÷8 duty cycle	Any operating frequency Low state : High state		7:9		
GM	Oscillator Transconductance		80	200		μS

NOTES: 1. The power dissipation is a function of the oscillator frequency (1st ORDER EFFECT see curve) but is also effected to a small extent by the oscillator tank components.

2. The ÷8 circuitry uses a dynamic scheme. As with any dynamic system, information or data is stored on very small nodal capacitances instead of latches (static systems) and there is a lower cutoff frequency of operation. Dynamic dividers are used in the ICM7209 to significantly improve high frequency performance and to decrease power consumption.

3 Rise and fall times are defined between the output levels of 0.5 and 2.4 volts.

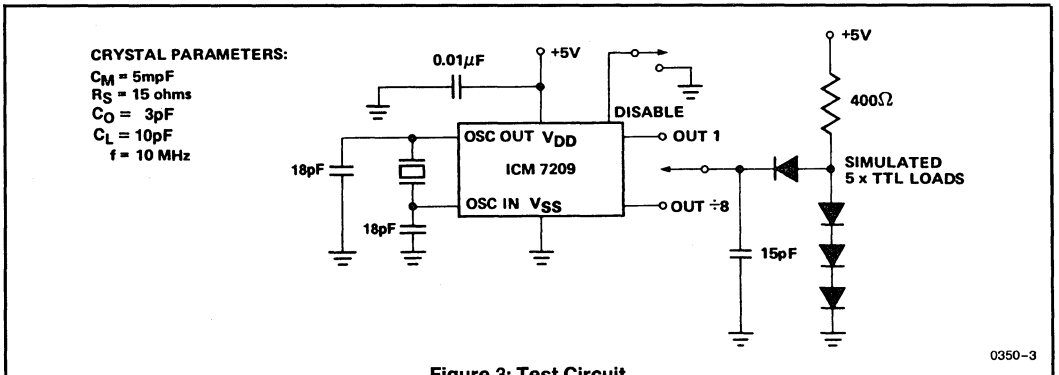
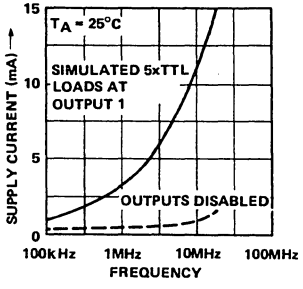


Figure 3: Test Circuit

NOTE: All typical values have been characterized but are not tested.

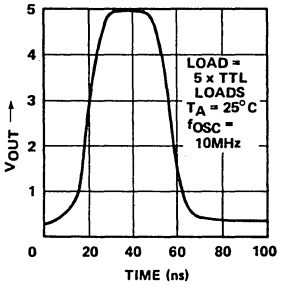
TYPICAL PERFORMANCE CHARACTERISTICS ($V_{DD} - V_{SS} = 5V$)

SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY



0350-4

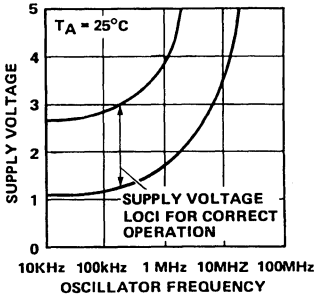
TYPICAL OUT 1 RISE AND FALL TIMES



0350-5

Rise and fall times of OUT ÷ 8 are similar to those of OUT 1.

SUPPLY VOLTAGE RANGE FOR CORRECT OPERATION OF ÷ 8 COUNTER AS A FUNCTION OF OSCILLATOR FREQUENCY.



0350-6

DETAILED DESCRIPTION

OSCILLATOR CONSIDERATIONS

The oscillator consists of a CMOS inverter with a non-linear resistor connected between the oscillator input and output to provide D.C. biasing. Using commercially obtainable quartz crystals the oscillator will operate from low frequencies (10kHz) to 10MHz.

The oscillator circuit consumes about 500μA of current using a 10MHz crystal with a 5 volt supply, and is designed to operate with a high impedance tank circuit. It is therefore necessary that the quartz crystal be specified with a load capacitance (C_L) of 10pF instead of the standard 30pF. To maximize the stability of the oscillator as a function of supply voltage and temperature, the motional capacitance of the crystal should be low (5mpF or less). Using a fixed input capacitor of 18pF and a variable capacitor of nominal value of 18pF on the output will result in oscillator stabilities of typically 1ppm per volt change in supply voltage.

THE ÷ 8 OUTPUT

A dynamic divider is used to divide the oscillator frequency by 8. Dynamic dividers use small nodal capacitances to store voltage levels instead of latches (which are used in static dividers). The dynamic divider has advantages in high speed operation and low power but suffers from limited low frequency operation. This results in a window of operation for any oscillator frequency (see TYPICAL PERFORMANCE CHARACTERISTICS).

OUTPUT DRIVERS

The output drivers consist of CMOS inverters having active pullups and pulldowns. Thus the outputs can be used to directly drive TTL gates, other CMOS gates operating with a 5 volt supply, or TTL compatible MOS gates. The guaranteed fanout is 5 TTL loads although typical fanout capability is at least 10 TTL loads with slightly increased output rise and fall times.

DEVICE POWER CONSUMPTION

At low frequencies the principal component of the power consumption is the oscillator. At high oscillator frequencies the major portion of the power is consumed by the output drivers, thus by disabling the outputs (activating the DISABLE INPUT) the device power consumption can be dramatically reduced.

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICM7213
One Second/One Minute Timebase Generator

GENERAL DESCRIPTION

The ICM7213 is a fully integrated micropower oscillator and frequency divider with four buffered outputs suitable for interfacing with most logic families. The power supply may be either a two battery stack (Ni-cad, alkaline, etc.) or a regular power supply greater than 2 volts. Depending upon the state of the WIDTH, INHIBIT, and TEST inputs, using a 4.194304MHz crystal will produce a variety of output frequencies including 2048Hz, 1024Hz, 34.133Hz, 16Hz, 1Hz, and 1/60Hz (plus composites).

The ICM7213 utilizes a very high speed low power metal gate CMOS technology which uses 6.4 volt zeners between the drains and sources of each transistor and also across the supply terminals. Consequently, the ICM7213 is limited to a 6 volt maximum supply voltage, although a simple dropping network can be used to extend the supply voltage range well above 6 volts (See Figure 7).

FEATURES

- **Guaranteed 2 Volts Operation**
- **Very Low Current Consumption: Typ. 100μA @ 3V**
- **All Outputs TTL Compatible**
- **On Chip Oscillator Feedback Resistor**
- **Oscillator Requires Only 3 External Components: Fixed Capacitor, Trim Capacitor, and A Quartz Crystal**
- **Output Inhibit Function**
- **4 Simultaneous Outputs: One Pulse/Sec, One Pulse/Min, 16Hz and Composite 1024+16+2Hz Outputs**
- **Test Speed-Up Provides Other Frequency Outputs**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7213IPD	−25°C to +85°C	14 pin PLASTIC DIP

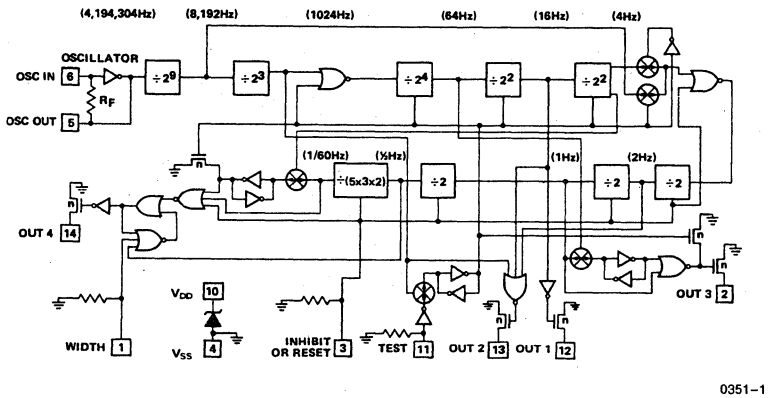


Figure 1: Functional Diagram

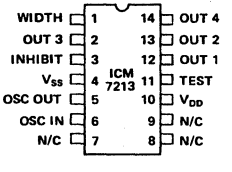


Figure 2: Pin Configuration (Outline drawing PD)

202800-003

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD}-V_{SS}$) 6.0V
Output Current (Any output) 20mA
All Input and Oscillator Voltages
(Note 1) ..... $V_{SS}-0.3V$ to $V_{DD}+0.3V$
All Output Voltages (Note 1) ..... V_{SS} to 6.0V

Operating Temperature Range ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Power Dissipation (Note 2) 200mW
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTE 1: The ICM7213 like most CMOS devices, may enter a destructive latchup mode if an input or output voltage is applied in excess of those defined and there is no supply current limiting:
2: Derate linearly power rating of 200mW at 25°C to 50mW at 70°C.

ELECTRICAL CHARACTERISTICS

($V_{DD}-V_{SS}=3.0V$, $f_{osc}=4.194304MHz$, Test Circuit, $T_A=25°C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD}	Supply Current			100	140	μA
V_{SUPPLY}	Guaranteed Operating Supply Voltage Range ($V_{DD}-V_{SS}$)	$-20°C<T_A<85°C$	2		4	V
I_{OLK}	Output Leakage Current	Any output, $V_{OUT}=6$ Volts			10	μA
R_{OUT}	Output Sat. Resistance	Any output, $I_{OLK}=2.5mA$		120	200	Ω
I_I	Inhibit Input Current	Inhibit terminal connected to V_{DD}		10	40	μA
I_{TP}	Test Point Input Current	Test point terminal connected to V_{DD}		10	40	
I_W	Width Input Current	Width terminal connected to V_{DD}		10	40	
g_m	Oscillator Transconductance	$V_{DD}=2V$	100			μS
f_{OSC}	Oscillator Frequency Range (Note 3)		1		10	MHz
f_{STAB}	Oscillator Stability	$2V<V_{DD}<4V$		1.0		ppm
t_s	Oscillator Start Time			0.1		sec
		$V_{DD}=2.0$ volts		0.2		

NOTE: 3. The ICM7213 uses dynamic dividers for high frequency division. As with any dynamic system, information is stored on very small nodal capacitances instead of latches (static system), therefore there is a lower frequency of operation. Dynamic dividers are used to improve the high frequency performance while at the same time significantly decreasing power consumption. At low supply voltages, operation at less than 1MHz is possible.

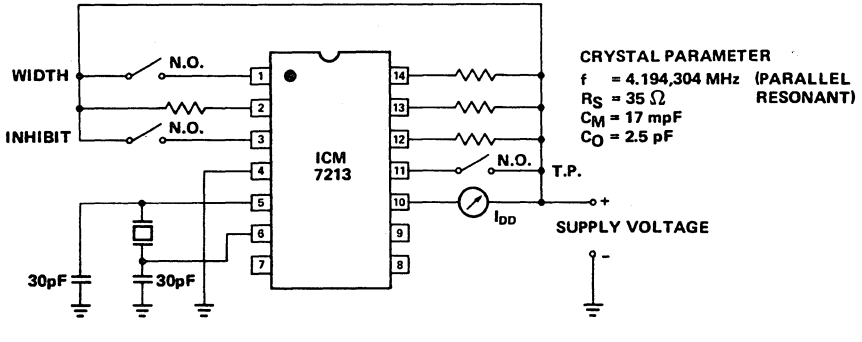
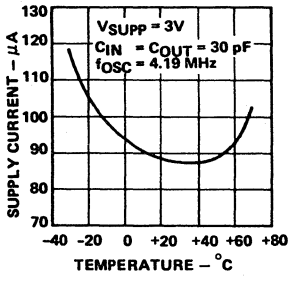


Figure 3: Test Circuit

NOTE: All typical values have been characterized but are not tested.

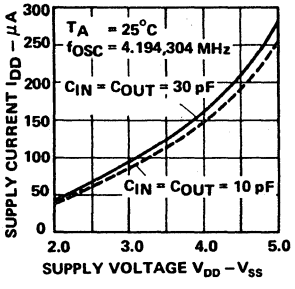
TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



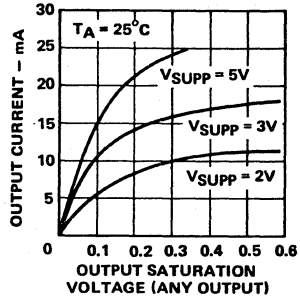
0351-4

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



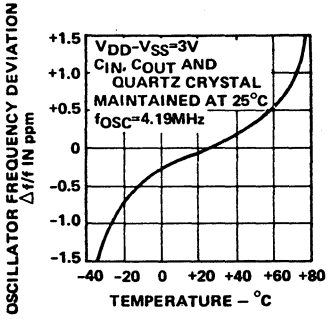
0351-5

OUTPUT CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE



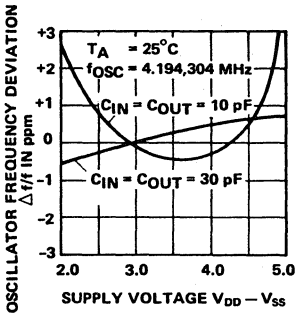
0351-6

OSCILLATOR STABILITY AS A FUNCTION OF DEVICE TEMPERATURE



0351-7

OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE



0351-8

OUTPUT DEFINITIONS

Input States*			Pin 12	Pin 13	Pin 2	Pin 14
Test	Inhibit	Width	Out 1	Out 2	Out 3	Out 4
L	L	L	16Hz $\div 2^{18}$	$\overline{1024+16+2}$Hz ($\div 2^{12} \div 2^{18} \div 2^{21}$) composite	1Hz, 7.8ms $\div 2^{22}$	1/60Hz, 1 Sec. $\div (2^{24} \times 3 \times 5)$
L	L	H	16Hz $\div 2^{18}$	$\overline{1024+16+2}$Hz ($\div 2^{12} \div 2^{18} \div 2^{21}$) composite	1Hz, 7.8ms $\div 2^{22}$	1/60Hz, 125ms
L	H	L	16Hz $\div 2^{18}$	$\overline{1024+16}$Hz ($\div 2^{12} \div 2^{18}$) composite	OFF	OFF
L	H	H	16Hz $\div 2^{18}$	$\overline{1024+16}$Hz ($\div 2^{12} \div 2^{18}$) composite	OFF	SEE WAVEFORMS
H	L	L	ON	$\overline{4096+1024}$Hz ($\div 2^{10} \div 2^{12}$) composite	2048Hz $\div 2^{11}$	34.133Hz, 50% D.C. $\div (2^{13} \times 5 \times 3)$
H	L	H	ON	$\overline{4096+1024}$Hz ($\div 2^{10} \div 2^{12}$) composite	2048Hz $\div 2^{11}$	34.133Hz, 50% D.C. $\div (2^{13} \times 5 \times 3)$
H	H	L	ON	1024Hz $\div 2^{12}$	ON	OFF
H	H	H	ON	1024Hz $\div 2^{12}$	ON	OFF

NOTE: When TEST and RESET are connected to ground, or left open, all outputs except for OUT 3 and OUT 4 have a 50% duty cycle.

NOTE: All typical values have been characterized but are not tested.

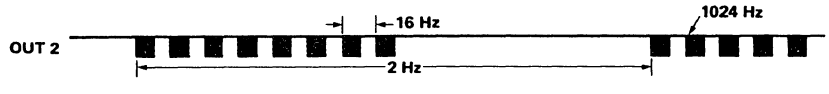


Figure 4: Output Waveform

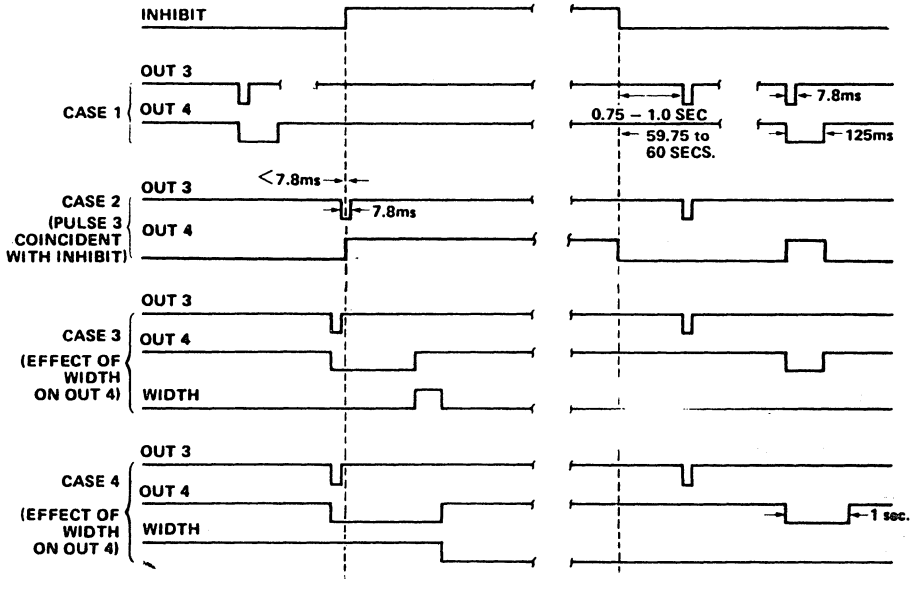


Figure 5: Effect of the Inhibit Input (Test Connected to V_{SS} or Left Open)

NOTE: Refers to Figure 5

All time scales are arbitrary, and in the case of OUT 3 only the pulses coinciding with the negative edge of OUT 4 are shown. Where time intervals are relevant they are clearly shown.

DETAILED DESCRIPTION

Supply Voltage Considerations

The ICM7213 may be used to provide various precision outputs with frequencies from 2048Hz to 1/60Hz using a 4,194,304Hz quartz oscillator, and other output frequencies may be obtained using other quartz crystal frequencies. Since the ICM7213 uses dynamic high frequency dividers for the initial frequency division there are limitations on the supply voltage range depending on the oscillator frequency. If, for example, a low frequency quartz crystal is selected, the supply voltage should be selected in the center of the operating window, or approximately 1.7 volts.

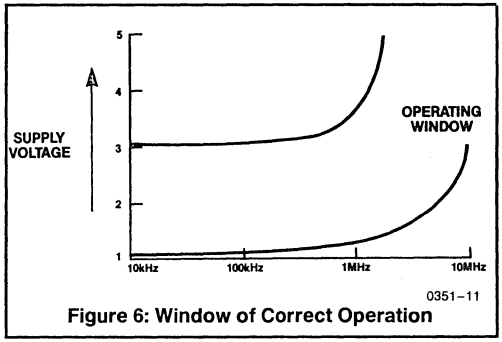


Figure 6: Window of Correct Operation

The supply voltage to the ICM7213 may be derived from a high voltage supply by using a simple resistor divider (if power is of no concern), by using a series resistor for minimum current consumption, or by means of a regulator.

NOTE: All typical values have been characterized but are not tested.

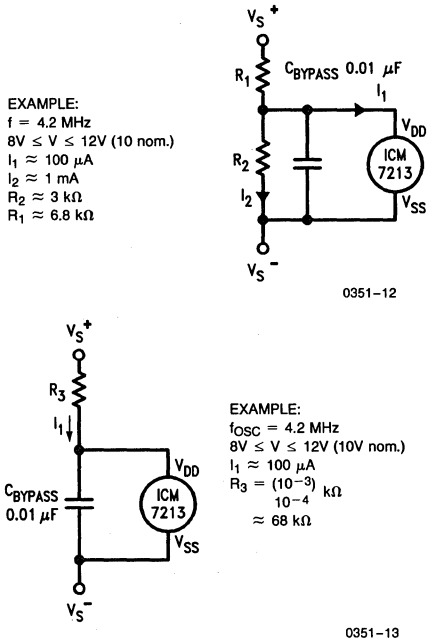


Figure 7: Biasing Schemes with High Voltage Supplies

Outputs

Pull up resistors will generally be required to interface with other logic families. These resistors must be connected between the various outputs and the positive power supply.

Oscillator Considerations

The oscillator consists of a CMOS inverter and a feedback resistor whose value is dependent on the voltage at the oscillator input and output terminals and the supply voltage. Oscillator stabilities of approximately 0.1ppm per 0.1 volt variation are achievable with a nominal supply voltage of 5 volts and a single voltage dropping resistor. The crystal specifications are shown in the TEST CIRCUIT.

It is recommended that the crystal load capacitance (CL) be no greater than 22pF for a crystal having a series resistance equal to or less than 75 ohms, otherwise the output amplitude of the oscillator may be too low to drive the divider reliably.

If a very high quality oscillator is desired, it is recommended that a quartz crystal be used having a tight tuning tolerance ±10ppm, a low series resistance (less than 25 ohms), a low motional capacitance of 5mpF and a load capacitance of 20pF. The fixed capacitor C_{IN} should be 30pF and the oscillator tuning capacitor should range between approximately 16 and 60pF.

Use of a high quality crystal will result in typical stabilities of 0.05ppm per 0.1 volt change of supply voltage.

Control Inputs

The TEST input inhibits the 2^{18} output and applies the 2^9 output to the 2^{21} divider, thereby permitting a speedup of the testing of the ÷60 section by a factor of 2048 times. This also results in alternative output frequencies (see table).

The WIDTH input may be used to change the pulse width of OUT 4 from 125ms to 1 sec, or to change the state of OUT 4 from ON to OFF during INHIBIT.

See Figures 4 and 5 for output waveforms and effect of control inputs.

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICM7216A/B/D
8-Digit Multi-Function Frequency Counter/Timer

GENERAL DESCRIPTION

The ICM7216A and B are fully integrated Timer Counters with LED display drivers. They combine a high frequency oscillator, a decade timebase counter, an 8-decade data counter and latches, a 7-segment decoder, digit multiplexers and 8 segment and 8 digit drivers which directly drive large multiplexed LED displays. The counter inputs have a maximum frequency of 10 MHz in frequency and unit counter modes and 2 MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7216A and B can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or as a totalizing counter. The counter uses either a 10 MHz or 1 MHz quartz crystal timebase. For period and time interval, the 10 MHz timebase gives a 0.1μs resolution. In period average and time interval average, the resolution can be in the nanosecond range. In the frequency mode, the user can select accumulation times of 0.01 sec, 0.1 sec, 1 sec and 10 sec. With a 10 sec accumulation time, the frequency can be displayed to a resolution of 0.1Hz in the least significant digit. There is 0.2 seconds between measurements in all ranges.

The ICM7216D functions as a frequency counter only, as described above.

All versions of the ICM7216 incorporate leading zero blanking. Frequency is displayed in kHz. In the ICM7216A and B, time is displayed in μs. The display is multiplexed at 500Hz with a 12.2% duty cycle for each digit. The ICM7216A is designed for common anode displays with typical peak segment currents of 25 mA. The ICM7216B and D are designed for common cathode displays with typical peak segment currents of 12 mA. In the display off mode, both digit and segment drivers are turned off, enabling the display to be used for other functions.

FEATURES

ALL VERSIONS:

- **Functions as a Frequency Counter (DC to 10 MHz)**
- **Four Internal Gate Times: 0.01 Sec, 0.1 Sec, 1 Sec, 10 Sec in Frequency Counter Mode**
- **Directly Drives Digits and Segments of Large Multiplexed LED Displays (Common Anode and Common Cathode Versions)**
- **Single Nominal 5V Supply Required**
- **Highly Stable Oscillator, Uses 1 MHz or 10 MHz Crystal**
- **Internally Generated Decimal Points, Interdigit Blanking, Leading Zero Blanking and Overflow Indication**
- **Display Off Mode Turns Off Display and Puts Chip Into Low Power Mode**
- **Hold and Reset Inputs for Additional Flexibility**

ICM7216A AND ICM7216B

- **Functions Also as a Period Counter, Unit Counter, Frequency Ratio Counter or Time Interval Counter**
- **1 Cycle, 10 Cycles, 100 Cycles, 1000 Cycles in Period, Frequency Ratio and Time Interval Modes**
- **Measures Period From 0.5μs to 10s**

ICM7216D

- **Decimal Point and Leading Zero Blanking May Be Externally Selected**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7216AIJI	−25°C to +85°C	28 pin CERDIP
ICM7216BIPI	−25°C to +85°C	28 pin PLASTIC DIP
ICM7216DIPI	−25°C to +85°C	28 pin PLASTIC DIP

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NOTE: All typical values have been characterized but are not tested.

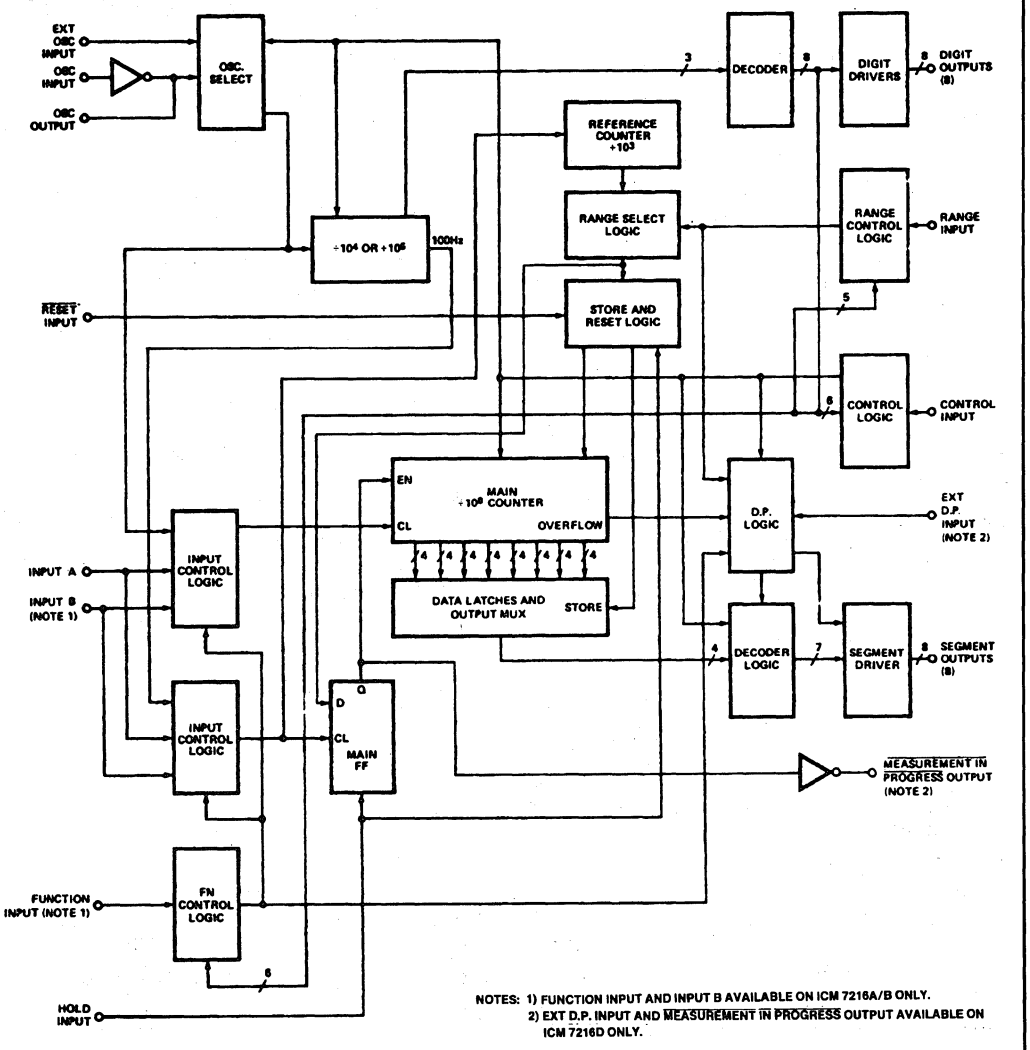


Figure 1: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

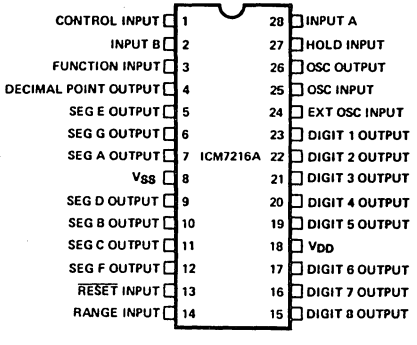
ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage ($V_{DD}-V_{SS}$) 6.5V
Maximum Digit Output Current ..... 400 mA
Maximum Segment Output Current ..... 60 mA
Voltage On Any Input or
Output Terminal[1] ..... ($V_{DD}+0.3V$) to ($V_{SS}-0.3V$)
Maximum Power Dissipation at
70°C 1.0W (ICM7216A)
0.5W (ICM7216B & D)
Operating Temperature Range ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

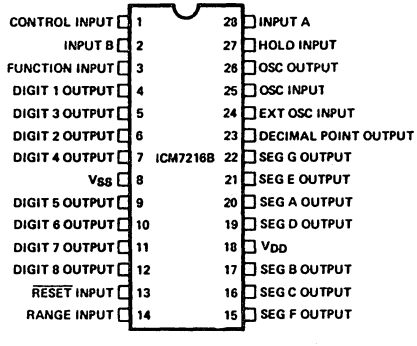
Note: 1. The ICM7216 may be triggered into a destructive latchup mode if either input signals are applied before the power supply is applied or if input or outputs are forced to voltages exceeding V_{DD} to V_{SS} by more than 0.3 volts.

Common Anode



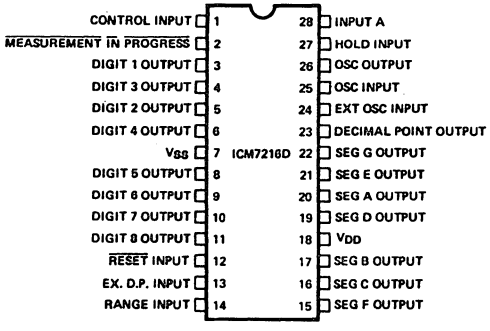
0353-2

Common Cathode



0353-3

Common Cathode



0353-5

Figure 2: Pin Configurations

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (ICM7216A/B)

(V_{DD} = 5.0V, V_{SS} = 0, T_A = 25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
ICM7216A/B						
I_{DD}	Operating Supply Current	Display Off, Unused Inputs to V_{SS}		2	5	mA
V_{SUPPLY}	Supply Voltage Range ($V_{DD}-V_{SS}$)	INPUT A, INPUT B Frequency at f_{max}	4.75		6.0	V
$f_{A(max)}$	Maximum Frequency INPUT A, Pin 28	Figure 3, Function = Frequency, Ratio, Unit Counter Function = Period, Time Interval	 10 2.5			 MHz MHz
$f_{B(max)}$	Maximum Frequency INPUT B, Pin 2	Figure 4	2.5			MHz
	Minimum Separation INPUT A to INPUT B Time Interval Function	Figure 9	250			ns
f_{osc}	Maximum Osc. Freq. and Ext. Osc. Frequency		10			MHz
f_{osc}	Minimum Ext. Osc. Freq.				100	kHz
g_m	Oscillator Transconductance	V_{DD} = 4.75V, T_A = +85°C	2000			µS
f_{mux}	Multiplex Frequency	f_{osc} = 10 MHz		500		Hz
	Time Between Measurements	f_{osc} = 10 MHz		200		ms
 V_{INL} V_{INH}	Input Voltages: Pins 2,13,25,27,28 Input Low Voltage Input High Voltage		 3.5		1.0	 V V
R_{IN}	Input Resistance to V_{DD} Pins 13,24	V_{IN} = V_{DD} − 1.0V	100	400		kΩ
I_{ILK}	Input Leakage Pin 27,28,2				20	µA
dV_{IN}/dt	Input Range of Change	Supplies Well Bypassed		15		mV/µS
ICM7216A						
 I_{OH} I_{OL}	Digit Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Low Output Current	 V_{OUT} = V_{DD} − 2.0V V_{OUT} = V_{SS} + 1.0V	 −140	 −180 0.3		 mA mA
 I_{OL} I_{OH}	Segment Driver: Pins 4,5,6,7,9,10,11,12 Low Output Current High Output Current	 V_{OUT} = V_{SS} + 1.5V V_{OUT} = V_{DD} − 2.5V	 20	 35 −100		 mA µA
 V_{INL} V_{INH} R_{IN}	Multiplex Inputs: Pins 1,3,14 Input Low Voltage Input High Voltage Input Resistance to V_{SS}	 V_{IN} = V_{SS} + 1.0V	 2.0 50	 100	0.8	 V V kΩ

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (ICM7216A/B)

(V_{DD} = 5.0V, V_{SS} = 0, T_A = 25°C, unless otherwise specified.) (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
ICM7216B						
	Digit Driver:					
	Pins 4,5,6,7,9,10,11,12					
I_{OL}	Low Output Current	$V_{OUT} = V_{SS} + 1.3V$	50	75		mA
I_{OH}	High Output Current	$V_{OUT} = V_{DD} - 2.5V$		−100		μA
	Segment Driver:					
	Pins 15,16,17,19,20,21,22,23					
I_{OH}	High Output Current	$V_{OUT} = V_{DD} - 2.0V$	−10			mA
I_{SLK}	Leakage Current	$V_{OUT} = V_{DD} - 2.5V$			10	μA
	Multiplex Inputs:					
	Pins 1,3,14					
V_{INL}	Input Low Voltage				$V_{DD} - 2.0$	V
V_{INH}	Input High Voltage		$V_{DD} - 0.8$			V
R_{IN}	Input Resistance to V_{DD}	$V_{IN} = V_{DD} - 2.5V$	100	360		kΩ

ELECTRICAL CHARACTERISTICS (ICM7216D)

(V_{DD} = 5.0V, V_{SS} = 0, T_A = 25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
ICM7216D						
I_{DD}	Operating Supply Current	Display Off, Unused Inputs to V_{SS}		2	5	mA
V_{SUPPLY}	Supply Voltage Range ($V_{DD} - V_{SS}$)	INPUT A Frequency at f_{max}	4.75		6.0	V
$f_{A(max)}$	Maximum Frequency INPUT A, Pin 28	Figure 3	10			MHz
f_{osc}	Maximum Osc. Freq. and Ext. Osc. Frequency		10			MHz
f_{osc}	Minimum Ext. Osc. Freq.				100	kHz
g_m	Oscillator Transconductance	V_{DD} = 4.75V, T_A = +85°C	2000			μS
f_{mux}	Multiplex Frequency	f_{osc} = 10 MHz		500		Hz
	Time Between Measurements	f_{osc} = 10 MHz		200		ms
	Input Voltages: Pins 12,27,28					
V_{INL}	Input Low Voltage				1.0	V
V_{INH}	Input High Voltage		3.5			V
	Input Resistance to V_{DD}					
R_{IN}	Pins 12,24	$V_{IN} = V_{DD} - 1.0V$	100	400		kΩ
	Input Leakage					
I_{ILK}	Pin 27, Pin 28				20	μA
I_{OL}	Output Current	V_{OL} = +.4V	0.36			mA
I_{OH}	Pin 2	$V_{OH} = V_{DD} - 0.8V$	265			μA
dV_{IN}/dt	Input Rate of Change	Supplies Well Bypassed		15		mV/μS

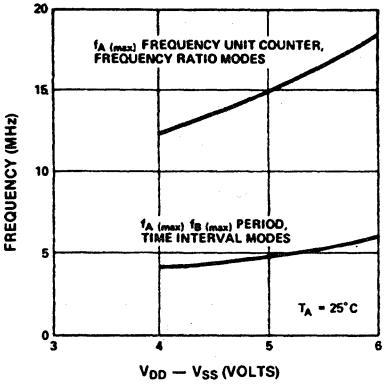
NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (ICM7216D)

(V_{DD} = 5.0V ±5%, V_{SS} = 0, T_A = 25°C, unless otherwise specified.) (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
ICM7216D						
	Digit Driver:					
	Pins 3,4,5,6,8,9,10,11					
I_{OL}	Low Output Current	V_{OUT} = +1.3V	50	75		mA
I_{OH}	High Output Current	V_{OUT} = V_{DD} − 2.5V		100		μA
	Segment Driver:					
	Pins 15,16,17,19,20,21,22,23					
I_{OH}	High Output Current	V_{OUT} = V_{DD} − 2.0V	10	15		mA
I_{SLK}	Leakage Current	V_{OUT} = V_{DD} − 2.5V			10	μA
	Multiplex Inputs:					
	Pins 1,13,14					
V_{INL}	Input Low Voltage				V_{DD} − 2.0	V
V_{INH}	Input High Voltage		V_{DD} − 0.8			V
R_{IN}	Input Resistance to V_{DD}	V_{IN} = V_{DD} − 1.0V	100	360		kΩ

TYPICAL PERFORMANCE CHARACTERISTICS



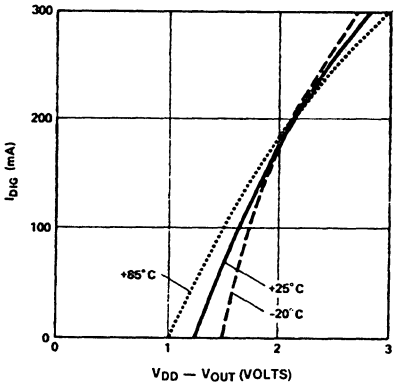
0353-26

f_A(max), f_B(max) as a Function of Supply

NOTE: All typical values have been characterized but are not tested.

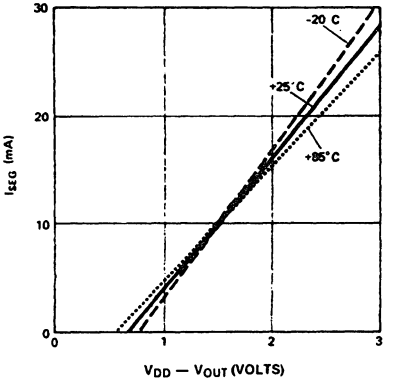
TYPICAL PERFORMANCE CHARACTERISTICS

ICM7216A Typical I_{DIG} vs. $V_{DD} - V_{OUT}$, $4.5 \le V_{DD} \le 6.0V$



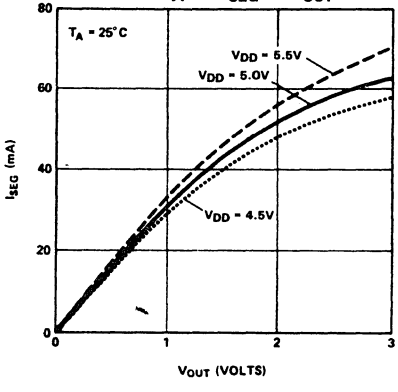
0353-6

ICM7216B & D Typical I_{SEG} vs. $V_{DD} - V_{OUT}$, $4.5 \le V_{DD} \le 6.0V$

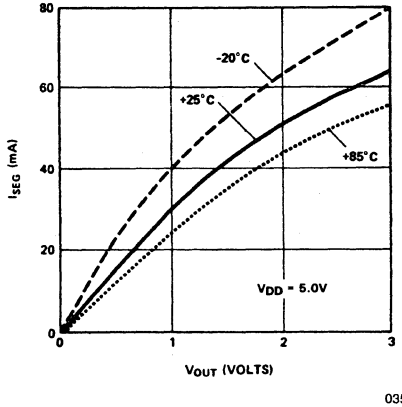


0353-7

ICM7216A Typical I_{SEG} vs. V_{OUT}

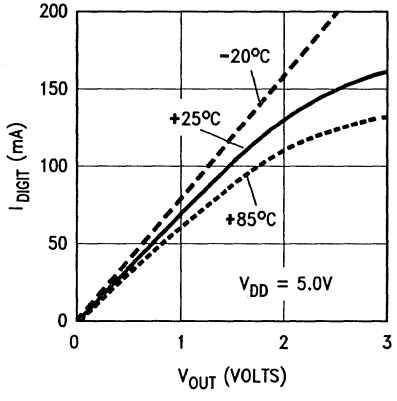


0353-8

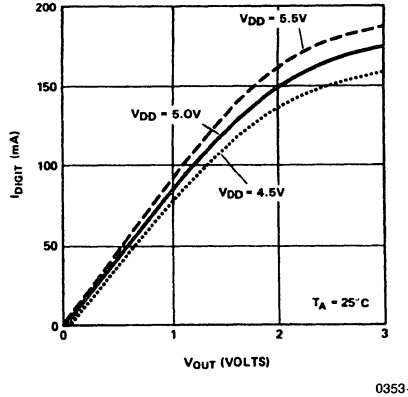


0353-9

ICM7216B & D Typical I_{DIGIT} vs. V_{OUT}



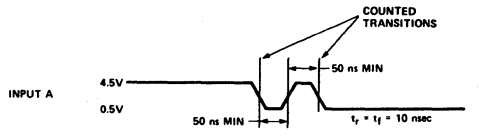
0353-27



0353-10

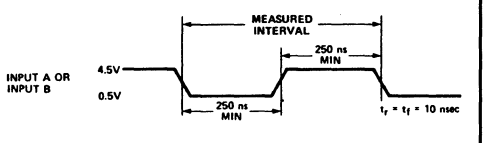
NOTE: All typical values have been characterized but are not tested.

ICM7216A/B/D



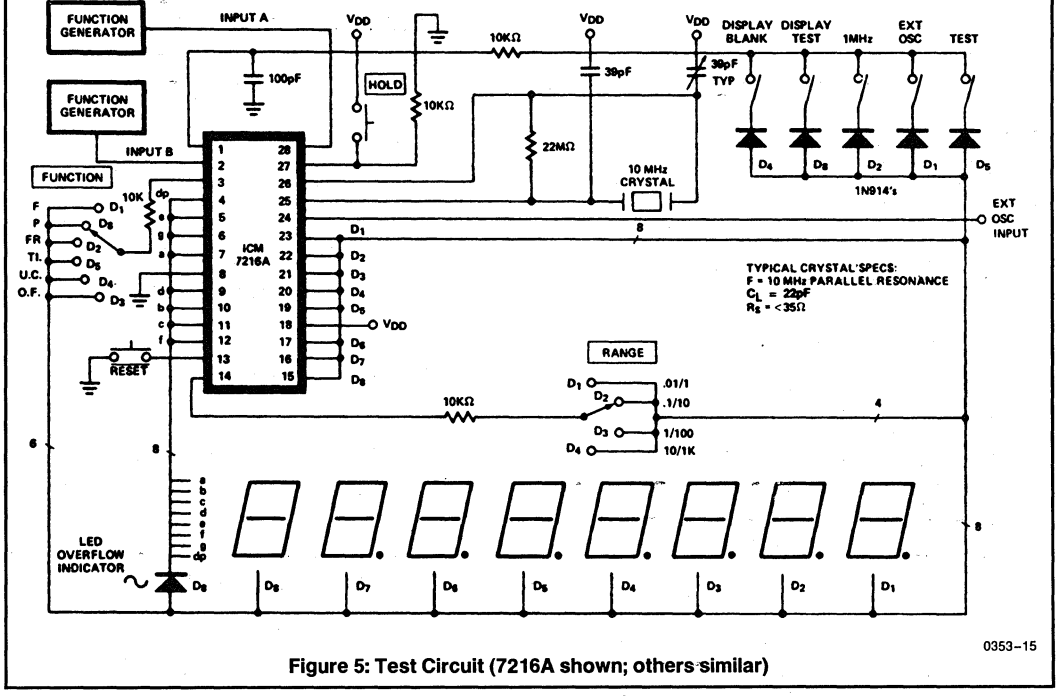
0353-11

Figure 3: Waveform for Guaranteed Minimum f_A(max) Function = Frequency, Frequency Ratio, Unit Counter.



0353-12

Figure 4: Waveform for Guaranteed Minimum f_B(max) and f_A(max) for Function = Period and Time Interval.

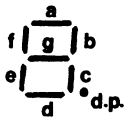


0353-15

Figure 5: Test Circuit (7216A shown; others similar)

NOTE: All typical values have been characterized but are not tested.

ICM7216A/B/D



0353-16

Overflow will be indicated on the decimal point output of digit 8.

A separate LED overflow indicator can be connected as follows:

	Cathode	Anode
ICM7216A	DEC. PT.	D_8
ICM7216B/D	D_8	DEC. PT.

0353-17

Figure 6: Segment Identification and Display Font

DETAILED DESCRIPTION

INPUTS A and B

INPUTS A and B are digital inputs with a typical switching threshold of 2.0V at $V_{DD}=5.0V$. For optimum performance the peak-to-peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from TTL logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs. (INPUT B is available only on ICM7216A/B).

Note that the amplitude of the input should not exceed the device supply (above the V_{DD} and below the V_{SS}) by more than 0.3V, otherwise the device may be damaged.

Multiplexed Inputs

The FUNCTION, RANGE, CONTROL and EXTERNAL DECIMAL POINT inputs are time multiplexed to select the function desired. This is achieved by connecting the appropriate Digit driver output to the inputs. The function, range and control inputs must be stable during the last half of each digit output, (typically 125μs). The multiplexed inputs are active high for the common anode ICM7216A and active low for the common cathode ICM7216B and D.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the **unit counter** mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10kΩ resistor should be placed in series with the multiplexed inputs as shown in the application circuits.

Table 1 shows the functions selected by each digit for these inputs.

Table 1: Multiplexed Input Functions

	Function	Digit
FUNCTION INPUT (Pin 3, ICM7216A & B Only)	Frequency	D_1
	Period	D_8
	Frequency Ratio	D_2
	Time Interval	D_5
	Unit Counter	D_4
	Oscillator Frequency	D_3
RANGE INPUT Pin 14	0.01 sec/1 Cycle	D_1
	0.1 sec/10 Cycles	D_2
	1 sec/100 Cycles	D_3
	10 sec/1K Cycles	D_4
CONTROL INPUT Pin 1	Display Off	D_4 and Hold
	Display Test	D_8
	1 MHz Select	D_2
	External Oscillator Enable	D_1
	External Decimal Point Enable	D_3
EXT. D.P. INPUT (Pin 13, ICM7216D Only)	Decimal point is output for same digit that is connected to this input	

FUNCTION INPUT

The six functions that can be selected are: **Frequency, Period, Time Interval, Unit Counter, Frequency Ratio** and **Oscillator Frequency.** This input is available on the ICM7216A and B only.

11

NOTE: All typical values have been characterized but are not tested.

The implementation of different functions is done by routing the different signals to two counters, called "Main Counter" and "Reference Counter". A simplified block diagram of the device for functions realization is shown in Figure 7. Table 2 shows which signals will be routed to each counter in different cases. The output of the Main Counter if the information which goes to the display. The Reference Counter divides its input to 1, 10, 100 and 1000. One of these outputs will be selected through the range selector and drive the enable input of the Main Counter. This means that the Reference Counter, along with its' associated blocks, directs the Main Counter to begin counting and determines the length of the counting period. Note that Figure 7 does not show the complete functional diagram (See Figure 1). After the end of each counting period, the output of the Main Counter will be latched and displayed, then the counter will be reset and a new measurement cycle will begin. Any change in the FUNCTION INPUT will stop the present measurement without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION INPUT is changed. In all cases, the 1–0 transitions are counted or timed.

Table 2: 7216A/B Input Routing

Function	Main Counter	Reference Counter
Frequency (f_A)	Input A	100 Hz (Oscillator $\div 10^5$ or 10^4)
Period (t_A)	Oscillator	Input A
Ratio (f_A/f_B)	Input A	Input B
Time Interval (A → B)	Oscillator	Input A Input B
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq. (f_{osc})	Oscillator	100 Hz (Oscillator $\div 10^5$ or 10^4)

Frequency—In this mode input A is counted by the Main Counter for a precise period of time. This time is determined by the time base oscillator and the selected range. For the 10 MHz (or 1 MHz) time base, the resolutions are 100, 10, 1 and 0.1 Hz. The decimal point on the display is set for kHz reading.

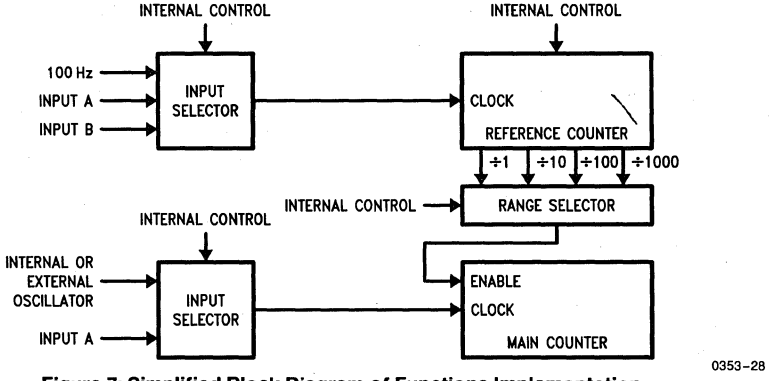


Figure 7: Simplified Block Diagram of Functions Implementation

NOTE: All typical values have been characterized but are not tested.

Period—In this mode, the timebase oscillator is counted by the Main Counter for the duration of 1, 10, 100 or 1000 (range selected) periods of the signal at input A. A 10 MHz timebase gives resolutions of 0.1μs to 0.0001μs for 1000 periods averaging. Note that the maximum input frequency for period measurement is 2.5 MHz.

Frequency Ratio—In this mode, the input A is counted by the Main Counter for the duration of 1, 10, 100 or 1000 (range selected) periods of the signal at input B. The frequency at input A should be higher than input B for meaningful result. The result in this case is unitless and its resolution can go up to 3 digits after decimal point.

Time Interval—In this mode, the timebase oscillator is counted by the Main Counter for the duration of a 1–0 transition of input A until a 1–0 transition of input B. This means input A starts the counting and input B stops it. If other ranges, except 0.01 s/1 cycle are selected the sequence of input A and B transitions must happen 10, 100 or 1000 times until the display becomes updated; note this when measuring long time intervals to give enough time for measurement completion. The resolution in this mode is the same as for period measurement. See the Time Interval Measurement section also.

Unit Counter—In this mode, the Main Counter is always enabled. The input A is counted by the Main Counter and displayed continuously.

Oscillator Frequency—In this mode, the device makes a frequency measurement on its timebase. This is a self test mode for device functionality check. For 10 MHz timebase the display will show 10000.0, 10000.00, 10000.000 and Overflow in different ranges.

RANGE INPUT

The RANGE INPUT selects whether the measurement period is made for 1, 10, 100 or 1000 counts of the Reference Counter. As it is shown in Table 1, this gives different counting windows for frequency measurement and various cycles for other modes of measurement.

In all functional modes except Unit Counter, any change in the RANGE INPUT will stop the present measurement without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the RANGE INPUT is changed.

CONTROL INPUT

Unlike the other multiplexed inputs, to which only one of the digit outputs can be connected at a time, this input can be tied to different digit lines to select combination of controls. In this case, isolation diodes must be used in digit lines to avoid crosstalk between them (see Figure 5). The direction of diodes depends on the device version, common anode or common cathode. For maximum noise immunity at this input, in addition to the 10k resistor which was mentioned before, a 39 to 100 pF capacitor should also be placed between this input and the V_{DD} or V_{SS} (See Figure 5).

Display Off—To disable the display drivers, it is necessary to tie the D_4 line to the CONTROL INPUT and have the HOLD input at V_{DD}. While in Display Off mode, the segments and digit drivers are all off, leaving the display lines floating, so the display can be shared with other devices. In this mode, the oscillator continues to run with a typical supply current of 1.5 mA with a 10 MHz crystal, but no measurements are made and multiplexed inputs are inactive. A new measurement cycle will be initiated when the HOLD input is switched to V_{SS}.

Display Test—Display will turn on with all the digits showing 8s and all decimal points on. The display will be blanked if Display Off is selected at the same time.

NOTE: All typical values have been characterized but are not tested.

1 MHz Select—The 1 MHz select mode allows use of a 1 MHz crystal with the same digit multiplex rate and time between measurement as with a 10 MHz crystal. This is done by dividing the oscillator frequency by 10^4 rather than 10^5. The decimal point is also shifted one digit to the right in period and time interval, since the least significant digit will be in μs increment rather than 0.1μs increment.

External Oscillator Enable—In this mode, the signal at EXT OSC INPUT is used as a timebase instead of the on-board crystal oscillator (built around the OSC INPUT, OSC OUTPUT inputs). This input can be used for an external stable temperature compensated crystal oscillator or for special measurements with any external source. The on-board crystal oscillator continues to work when the external oscillator is selected. This is necessary to avoid hang-up problems, and has no effect on the chip's functional operation. If the on-board oscillator frequency is less than 1 MHz or only the external oscillator is used, THE OSC INPUT MUST BE CONNECTED TO THE EXT OSC INPUT providing the timebase has enough voltage swing for OSC INPUT (See electrical characteristics). If the external timebase is TTL level a pullup resistor must be used for OSC INPUT. The other way is to put a 22 MΩ resistor between OSC INPUT and OSC OUTPUT and capacitively couple the EXT OSC INPUT to OSC INPUT. This will bias the OSC INPUT at its threshold and the drive voltage will need to be only 2 $V_{p\text{-}p}$. The external timebase frequency must be greater than 100 kHz or the chip will reset itself to enable the on-board oscillator.

External Decimal Point Enable—In this mode, the EX D.P. INPUT is enabled (ICM7216D only). A decimal point will be displayed for the digit that its output line is connected to this input (EX D.P. INPUT). Digit 8 should not be used since it will override the overflow output. Leading zero blanking is effective for the digits to the left of selected decimal point.

HOLD INPUT

Except in the **unit counter mode**, when the HOLD input is at V_{DD}, any measurement in progress (before $\overline{\text{STORE}}$ goes low) is stopped, the main counter is reset and the chip is held ready to initiate a new measurement as soon as HOLD goes low. The latches which hold the main counter data are not updated, so the last complete measurement is displayed. In **unit counter** mode when HOLD input is at V_{DD}, the counter is not stopped or reset, but the display is frozen at that instantaneous value. When HOLD goes low the count continues from the new value in the new counter.

$\overline{\text{RESET}}$ INPUT

The $\overline{\text{RESET}}$ input resets the main counter, stops any measurement in progress, and enables the main counter latches, resulting in an all zero output. A capacitor to ground will prevent any hang-ups on power-up.

$\overline{\text{MEASUREMENT IN PROGRESS}}$

This output is provided in ICM7216D. It stays low during measurements and goes high for intervals between measurements. It is provided for system interfacing and can drive a low power Schottky TTL or one ECL load if the ECL device is powered from the same supply as ICM7216D.

Decimal Point Position

Table 3 shows the decimal point position for different modes of ICM7216 operation. Note that the digit 1 is the least significant digit. Table is give for 10 MHz timebase frequency.

Overflow Indication

When overflow happens in any measurement it will be indicated on the decimal point of the digit 8. A separate LED indicator can be used. Figure 6 shows how to connect this indicator.

NOTE: All typical values have been characterized but are not tested.

Table 3: Decimal Point Position

Range	Frequency	Period	Frequency Ratio	Time Interval	Unit Counter	Oscillator Frequency
0.01 s/1 Cycle	D2	D2	D1	D2	D1	D2
0.1 s/10 Cycle	D3	D3	D2	D3	D1	D3
1 s/100 Cycle	D4	D4	D3	D4	D1	D4
10 s/1k Cycle	D5	D5	D4	D5	D1	D5

Time Interval Measurement

When in the **time interval** mode and measuring a single event, the ICM7216A/B must first be "primed" prior to measuring the event of interest. This is done by first generating a negative going edge on Channel A followed by a negative going edge on Channel B to start the "measurement interval". The inputs are then primed ready for the measurement. Positive going edges on A and B, before or after the priming, will be needed to restore the original condition.

Priming can be easily accomplished using the circuit in Figure 8.

Following the priming procedure (when in single event or 1 cycle range) the device is ready to measure one (only) event.

When timing repetitive signals, it is not necessary to "prime" the ICM7216A/B as the first alternating signal states automatically prime the device. See Figure 9.

During any time interval measurement cycle, the ICM7216A/B requires 200 ms following B going low to update all internal logic. A new measurement cycle will not take place until completion of this internal update time.

Oscillator Considerations

The oscillator is a high gain CMOS inverter. An external resistor of 10MΩ to 22MΩ should be connected between the OSCillator INPUT and OUTPUT to provide biasing. The oscillator is designed to work with a parallel resonant 10 MHz quartz crystal with a static capacitance of 22pF and a series resistance of less than 35 ohms.

For a specific crystal and load capacitance, the required g_m can be calculated as follows:

$$g_m = \omega^2 C_{in} C_{out} R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

where $C_L = \left(\frac{C_{in}C_{out}}{C_{in}+C_{out}}\right)$

C_O = Crystal Static Capacitance

R_S = Crystal Series Resistance

C_{in} = Input Capacitance

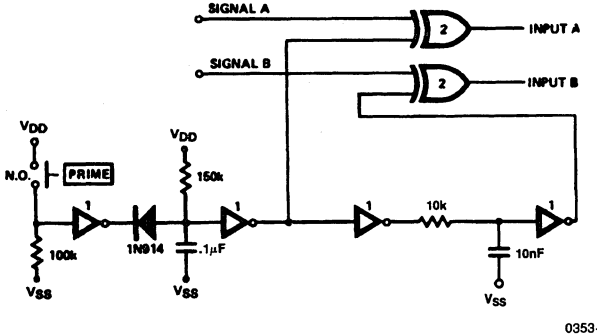
C_{out} = Output Capacitance

$\omega = 2\pi f$

The required g_m should not exceed 50% of the g_m specified for the ICM7216 to insure reliable startup. The OSCillator INPUT and OUTPUT pins each contribute about 5pF to C_{in} and C_{out}. For maximum stability of frequency, C_{in} and C_{out} should be approximately twice the specified crystal static capacitance.

In cases where non decade prescalers are used it may be desirable to use a crystal which is neither 10 MHz or 1 MHz. In that case both the multiplex rate and time between measurements will be different. The multiplex rate is $f_{mux} = \frac{f_{osc}}{2\times10^4}$ for 10 MHz mode and $f_{mux} = \frac{f_{osc}}{2\times10^3}$ for the 1 MHz mode. The time between measurements is $\frac{2\times10^6}{f_{osc}}$ in the 10 MHz mode and $\frac{2\times10^5}{f_{osc}}$ in the 1 MHz mode.

The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. Coupling from the EXTERNAL OSCILLATOR INPUT to the OSCILLATOR OUTPUT or INPUT can cause undesirable shifts in oscillator frequency.



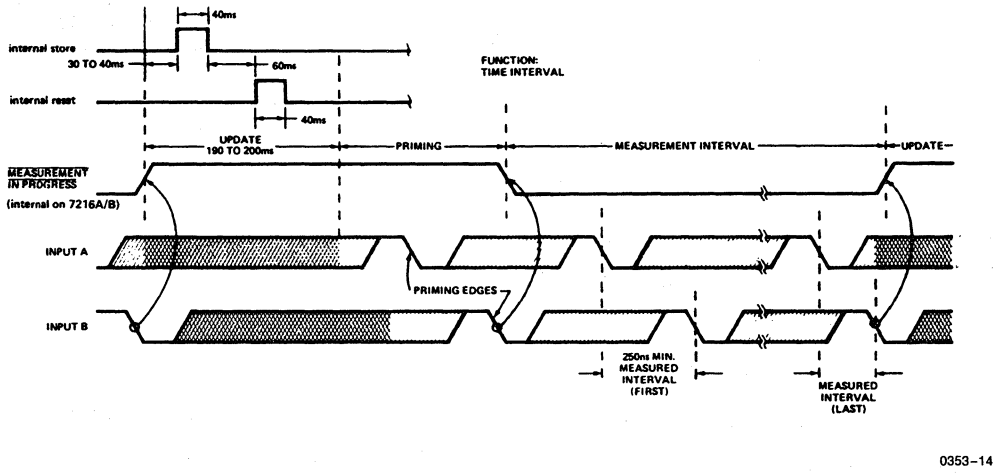
Device	Type
1	CD4049B Inverting Buffer
2	CD4070B Exclusive-OR

0353-29

Figure 8: Priming Circuit, Signals A & B Both High or Low

NOTE: All typical values have been characterized but are not tested.

ICM7216A/B/D



NOTE: IF RANGE IS SET TO 1 EVENT, FIRST AND LAST MEASURED INTERVAL WILL COINCIDE.

Figure 9: Waveforms for Time Interval Measurement (Others are similar, but without priming phase).

Display Considerations

The display is multiplexed at a 500 Hz rate with a digit time of 244 μS. An interdigit blanking time of 6μs is used to prevent display ghosting (faint display of data from previous digit superimposed on the next digit). Leading zero blanking is provided, which blanks the left hand zeroes after decimal point or any non zero digits. Digits to the right of the decimal point are always displayed. The leading zero blanking will be disabled when the Main Counter overflows.

The ICM7216A is designed to drive common anode LED displays at peak current of 25 mA/segment, using displays with $V_F = 1.8V$ at 25 mA. The average DC current will be over 3 mA under these conditions. The ICM7216B and D are designed to drive common cathode displays at peak current of 15 mA/segment using displays with $V_F = 1.8V$ at 15 mA. Resistors can be added in series with the segment drivers to limit the display current in very efficient displays, if required. The Typical Performance Characteristics curves show the digit and segment currents as a function of output voltage.

To get additional brightness out of the displays, V_{DD} may be increased up to 6.0V. However, care should be taken to see that maximum power and current ratings are not exceeded.

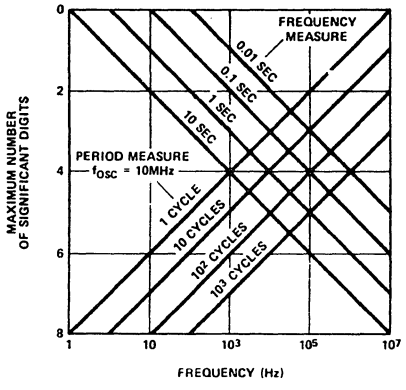
The segment and digit outputs in ICM7216's are not directly compatible with either TTL or CMOS logic when driving LEDs. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals.

ACCURACY

In a Universal Counter crystal drift and quantization effects cause errors. In **frequency, period** and **time interval** modes, a signal derived from the oscillator is used in either the Reference Counter or Main Counter. Therefore, in these modes an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of 20ppm/°C.

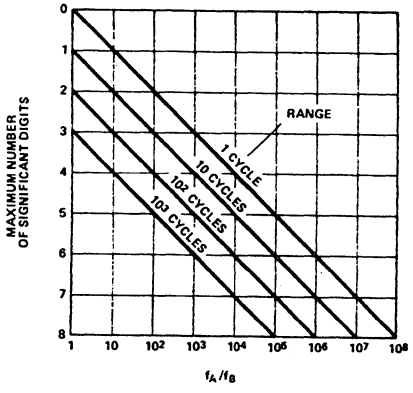
In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the **frequency** mode the maximum accuracy is obtained with high frequency inputs and in **period** mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 10. In **time interval** measurements there can be an error of 1 count per interval. As a result there is the same inherent accuracy in all ranges as shown in Figure 11. In **frequency ratio** measurement can be more accurately obtained by averaging over more cycles of INPUT B as shown in Figure 12.

NOTE: All typical values have been characterized but are not tested.



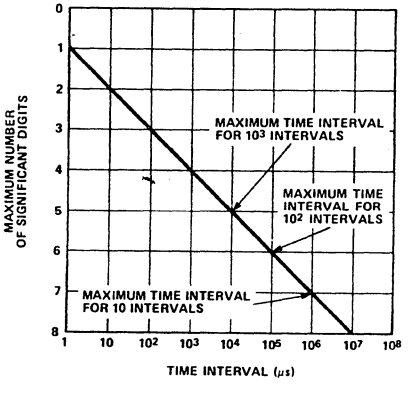
0353-18

Figure 10: Maximum Accuracy of Frequency and Period Measurements Due to Limitations of Quantization Errors



0353-20

Figure 12: Maximum Accuracy for Frequency Ratio Measurement Due to Limitation of Quantization Errors



0353-19

Figure 11: Maximum Accuracy of Time Interval Measurement Due to Limitations of Quantization Errors

NOTE: All typical values have been characterized but are not tested.

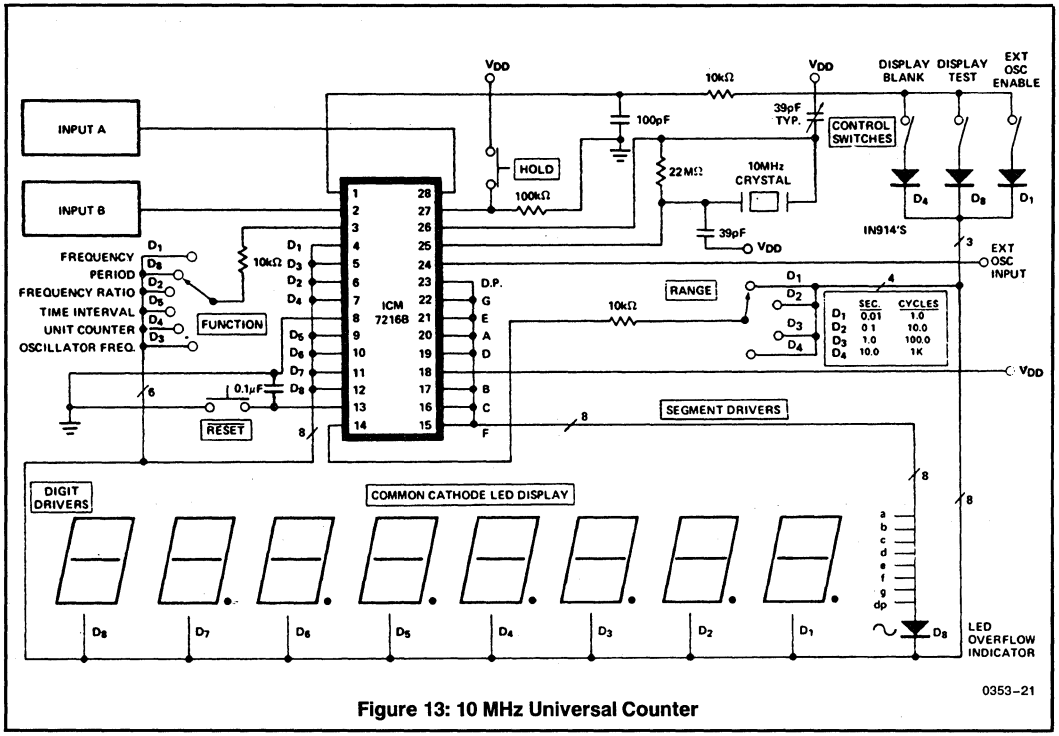


Figure 13: 10 MHz Universal Counter

APPLICATIONS

The ICM7216 has been designed for use in a wide range of Universal and Frequency counters. In many cases, prescalers will be required to reduce the input frequencies to under 10 MHz. Because INPUT A and INPUT B are digital inputs, additional circuitry is often required for input buffering, amplification, hysterisis, and level shifting to obtain a good digital signal.

The ICM7216A or B can be used as a minimum component complete Universal Counter as shown in Figure 13. This circuit can use input frequencies up to 10 MHz at INPUT A and 2 MHz at INPUT B. If the signal at INPUT A has a very low duty cycle it may be necessary to use a 74LS121 monostable multivibrator or similar circuit to stretch the input pulse width to be able to guarantee that it is at least 50 ns in duration.

NOTE: All typical values have been characterized but are not tested.

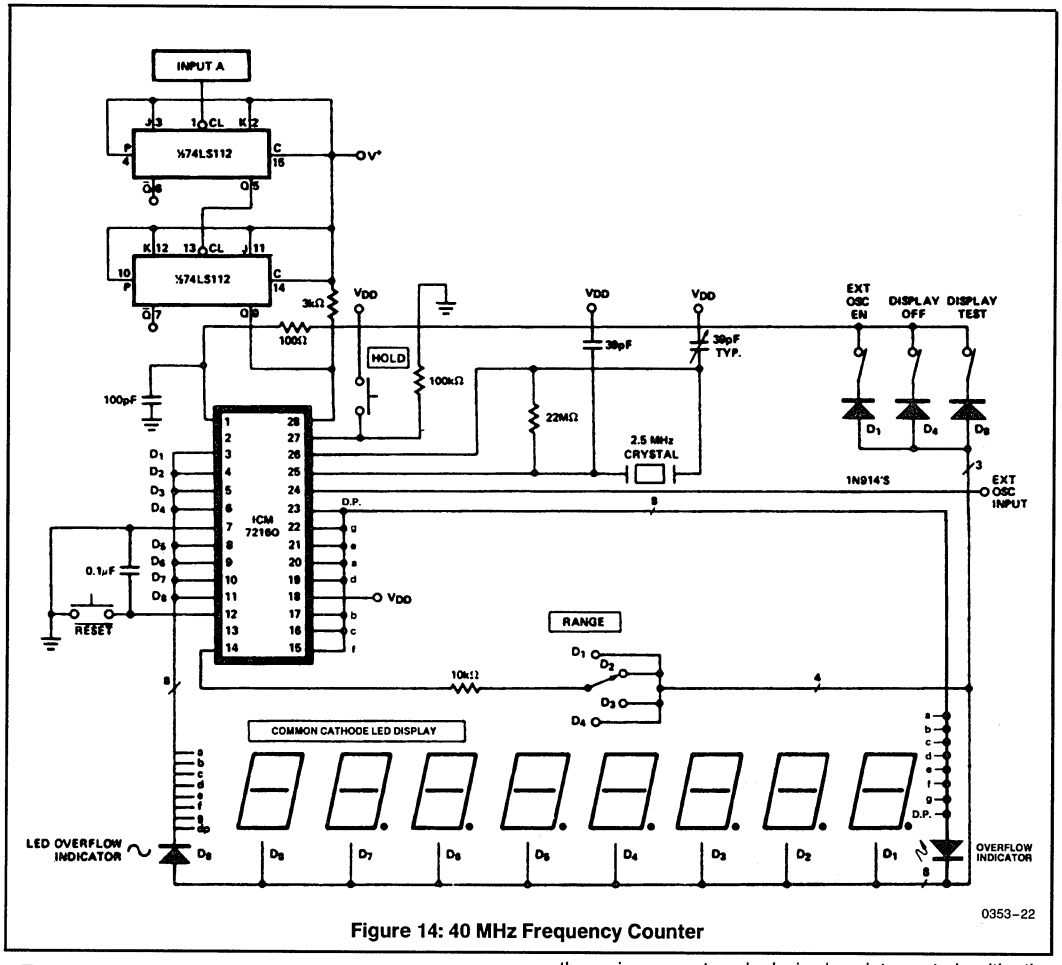


Figure 14: 40 MHz Frequency Counter

To measure frequencies up to 40 MHz the circuit of Figure 14 can be used. To obtain the correct measured value, it is necessary to divide the oscillator frequency by four as well as the input frequency. In doing this the time between measurements is also lengthened to 800 ms and the display multiplex rate is decreased to 125 Hz.

If the input frequency is prescaled by ten, then the oscillator can remain at 10 or 1 MHz, but the decimal point must be moved one digit to the right. Figure 15 shows a frequency counter with a ÷10 prescaler and an ICM7216A. Since there is no external decimal point control with the ICM7216A/B, the decimal point may be controlled externally with additional drivers as shown in Figure 15. Alternatively, if separate anodes are available for the decimal points, they can be wired up to the adjacent digit anodes. Note that there can be one zero to the left of the decimal point since the internal leading zero blanking cannot be changed. In Figure 16 additional logic has been added to count the input directly in **period** mode for maximum accuracy. In Figures 15 and 16, INPUT A comes from Q_C of the prescaler rather than Q_D to obtain an input duty cycle of 40%.

NOTE: All typical values have been characterized but are not tested.

ICM7216A/B/D

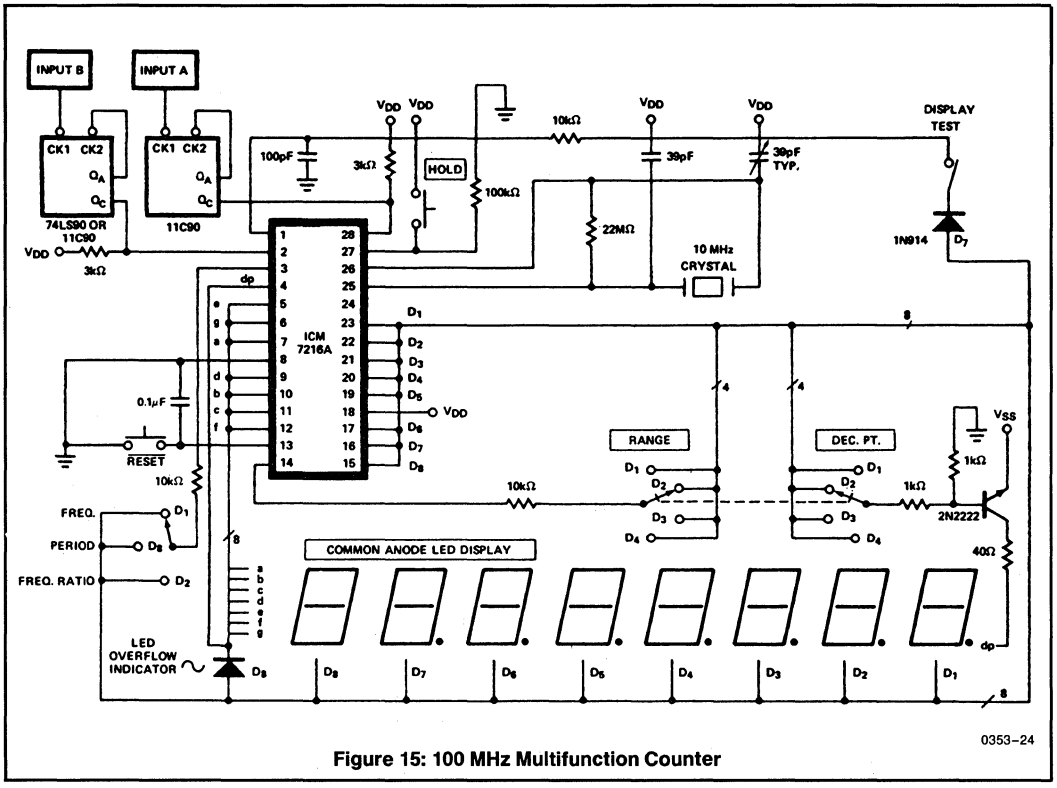
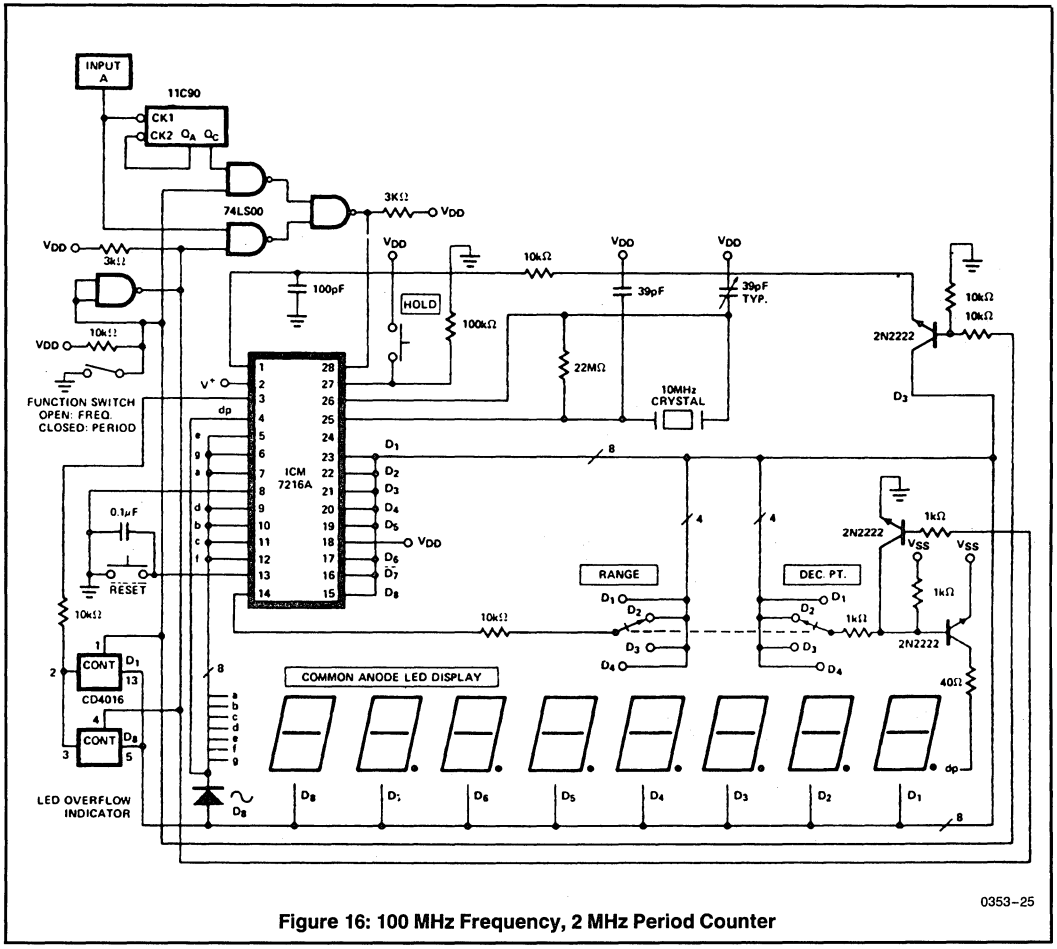


Figure 15: 100 MHz Multifunction Counter

NOTE: All typical values have been characterized but are not tested.



0353-25

Figure 16: 100 MHz Frequency, 2 MHz Period Counter

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICM7217
4-Digit LED Display Programmable Up/Down Counter

GENERAL DESCRIPTION

The ICM7217 is a four digit, presettable up/down counter with an onboard presettable register continuously compared to the counter. The ICM7217 is intended for use in hard-wired applications where thumbwheel switches are used for loading data, and simple SPDT switches are used for chip control.

This circuit provides multiplexed 7 segment LED display outputs, with common anode or common cathode configurations available. Digit and segment drivers are provided to directly drive displays of up to 0.8" character height (common anode) at a 25% duty cycle. The frequency of the on-board multiplex oscillator may be controlled with a single capacitor, or the oscillator may be allowed to free run. Leading zeros can be blanked. The data appearing at the 7 segment and BCD outputs is latched; the content of the counter is transferred into the latches under external control by means of the Store pin.

The ICM7217 (common anode) and ICM7217A (common cathode) versions are decade counters, providing a maximum count of 9999, while the ICM7217B (common anode) and ICM7217C (common cathode) are intended for timing purposes, providing a maximum count of 5959.

This circuit provides 3 main outputs; a CARRY/BORROW output, which allows for direct cascading of counters, a $\overline{\text{ZERO}}$ output, which indicates when the count is zero, and an $\overline{\text{EQUAL}}$ output, which indicates when the count is equal to the value contained in the register. Data is multiplexed to and from the device by means of a three-state BCD I/O port. The CARRY/BORROW, $\overline{\text{EQUAL}}$, $\overline{\text{ZERO}}$ outputs, and the BCD port will each drive one standard TTL load.

To permit operation in noisy environments and to prevent multiple triggering with slowly changing inputs, the count input is provided with a Schmitt trigger.

Input frequency is guaranteed to 2MHz, although the device will typically run with f_{in} as high as 5MHz. Counting and comparing ($\overline{\text{EQUAL}}$ output) will typically run 750kHz maximum.

FEATURES

- **Four Decade, Presettable Up-Down Counter With Parallel Zero Detect**
- **Settable Register With Contents Continuously Compared to Counter**
- **Directly Drives Multiplexed 7 Segment Common Anode or Common Cathode LED Displays**
- **On-Board Multiplex Scan Oscillator**
- **Schmitt Trigger On Count Input**
- **TTL Compatible BCD I/O Port, Carry/Borrow, Equal, and Zero Outputs**
- **Display Blank Control for Lower Power Operation; Quiescent Power Dissipation <5mW**
- **All Terminals Fully Protected Against Static Discharge**
- **Single 5V Supply Operation**

ORDERING INFORMATION

Part Number	Temperature Range	Package	Display Driver Type	Count Option/ Max Count
ICM7217AIPI	-25°C to +85°C	28 Pin Plastic DIP	Common Cathode	Decade/9999
ICM7217CIPI	-25°C to +85°C	28 Pin Plastic DIP	Common Cathode	Timing/5959
ICM7217IJI	-25°C to +85°C	28 Pin CERDIP	Common Anode	Decade/9999
ICM7217BIJI	-25°C to +85°C	28 Pin CERDIP	Common Anode	Timing/5959

202816-004

NOTE: All typical values have been characterized but are not tested.

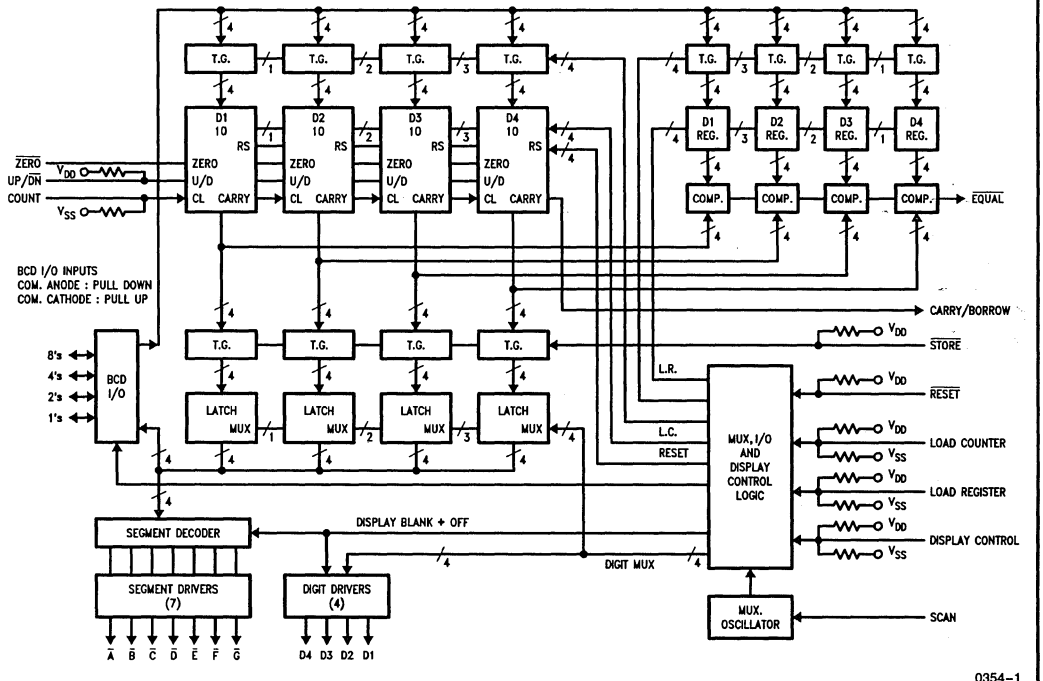


Figure 1: ICM7217 Functional Diagram

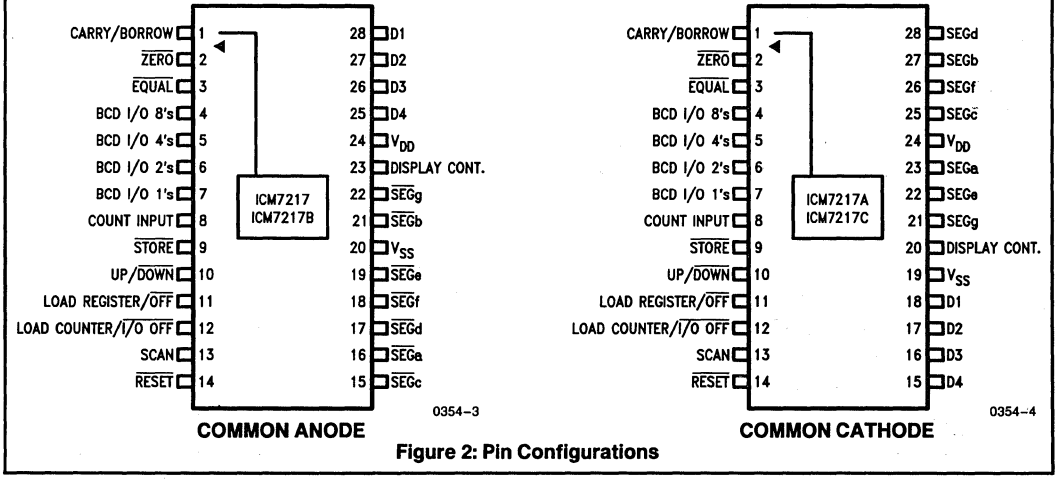


Figure 2: Pin Configurations

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD} - V_{SS}$) 6V
Input Voltage (any terminal) ..... ($V_{SS} - 0.3$)V to ($V_{DD} + 0.3$)V
(Note 2)
Power Dissipation (common anode/Cerdip) 1W
(Note 1)
Power Dissipation (common cathode/Plastic) 0.5W
(Note 1)
Operating Temperature Range ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C, Display Diode Drop 1.7V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{DD} (7217)	Supply Current (Lowest power mode)	Display Off, LC, DC, UP/DN, ST, RS, BCD I/O Floating or at V_{DD} (Note 3)		350	500	μA
I_{OP}	Supply Current OPERATING	Common Anode, Display On, all "8's"	140	200		mA
		Common Cathode, Display On, all "8's"	50	100		mA
V_{DD}	Supply Voltage		4.5	5	5.5	V
I_{DIG}	Digit Driver output current	Common anode, $V_{OUT} = V_{DD} - 2.0V$	140	−200		mA peak
I_{SEG}	SEGment driver output current	Common anode, $V_{OUT} = +1.5V$	20	35		mA peak
I_{DIG}	Digit Driver output current	Common cathode, $V_{OUT} = +1.0V$	−50	−75		mA peak
I_{SEG}	SEGment driver output current	Common cathode $V_{OUT} = V_{DD} - 2V$	−9	−12.5		mA peak
I_P	$\overline{ST}$, $\overline{RS}$, UP/$\overline{DN}$ input pullup current	$V_{IN} = V_{DD} - 2V$ (See Note 3)	5	25		μA
Z_{IN}	3 level input impedance		40		350	kΩ
V_{BIH}	BCD I/O input high voltage	ICM7217 common anode (Note 4)	1.5			V
		ICM7217 common cathode (Note 4)	4.40			V
V_{BIL}	BCD I/O input low voltage	ICM7217 common anode (Note 4)			0.60	V
		ICM7217 common cathode (Note 4)			3.2V	V
I_{BPU}	BCD I/O input pullup current	ICM7217 common cathode $V_{IN} = V_{DD} - 2V$ (Note 3)	5	25		μA
I_{BPD}	BCD I/O input pulldown current	ICM7217 common anode $V_{IN} = +2V$ (Note 3)	5	25		μA
V_{OH}	BCD I/O, $\overline{ZERO}$, $\overline{EQUAL}$ Outputs output high voltage	$I_{OH} = -100\mu A$	3.5			V
V_{OL}	BCD I/O, CARRY/BORROW $\overline{ZERO}$, $\overline{EQUAL}$ Outputs output low voltage	$I_{OL} = 1.6mA$			0.4	V
f_{in}	Count input frequency	$-20°C < T_A < +70°C$		5		MHz
		Guaranteed	0		2	
V_{TH}	Count input threshold	(Note 5)		2		V

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (Continued) (V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C, Display Diode Drop 1.7V, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{HYS}	Count input hysteresis	(Note 5)		0.5		V
V_{CIL}	Count input LO				0.40	V
V_{CIH}	Count Input HI		3.5			V
f_{ds}	Display scan oscillator frequency	Free-running (SCAN terminal open circuit)		2.5	10	kHz

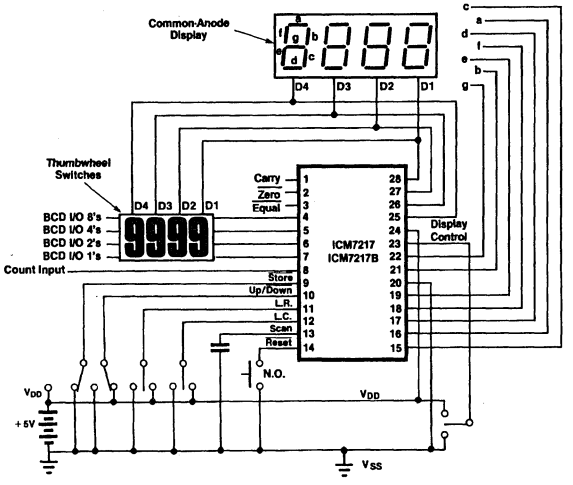
SWITCHING CHARACTERISTICS (V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{UCs}	UP/$\overline{DOWN}$ setup time	300			ns
t_{UCh}	UP/$\overline{DOWN}$ hold time	1500	750		
t_{CWh}	COUNT pulse width high	250	100		
t_{CWl}	COUNT pulse width low	250	100		
t_{CB}	COUNT to CARRY/BORROW delay		750		
t_{Bw}	CARRY/BORROW pulse width		100		
t_{CE}	COUNT to $\overline{EQUAL}$ delay		500		
t_{CZ}	COUNT to $\overline{ZERO}$ delay		300		
t_{RST}	RESET pulse width	1000	500		

NOTES: 1. These limits refer to the package and will not be obtained during normal operation.

2. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason it is recommended that the power supply to the device be established before any inputs are applied and that in multiple systems the supply to the ICM7217 be turned on first.
3. In the ICM7217 the UP/$\overline{DOWN}$, $\overline{STORE}$, $\overline{RESET}$ and the BCD I/O as inputs have pullup or pulldown devices which consume power when connected to the opposite supply. Under these conditions, with the display off, the device will consume typically 750 μA.
4. These voltages are adjusted to allow the use of thumbwheel switches for the ICM7217. Note that a high level is taken as an input logic zero for ICM7217 common-cathode versions.
5. Parameters not tested (Guaranteed by Design).

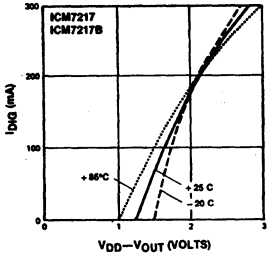
NOTE: All typical values have been characterized but are not tested.



0354-5

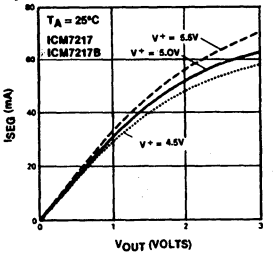
Figure 3: Test Circuits, showing the ICM7217 in the Common-Anode Version

TYPICAL PERFORMANCE CHARACTERISTICS (DIGIT AND SEGMENT DRIVERS)

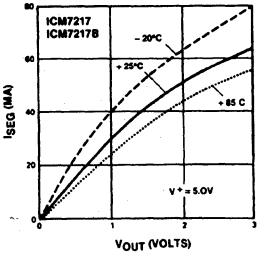


0354-7

Typical I_{DIG} vs. $V_+ - V_{OUT}$, $4.5V \leq V^+ \leq 6.0V$

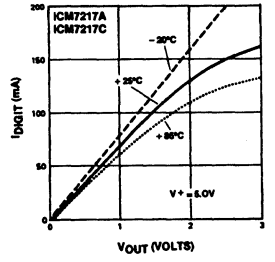


0354-8



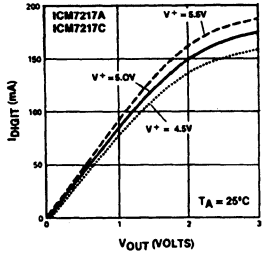
0354-9

Typical I_{SEG} vs. V_{OUT}

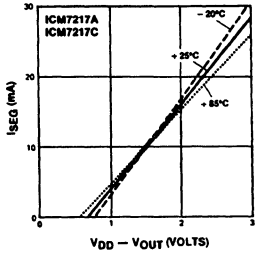


0354-10

Typical I_{DIGIT} vs. V_{OUT}



0354-11



0354-12

Typical I_{SEG} vs. $V_{DD} - V_{OUT}$, $4.5 \leq V_{DD} - V_{SS} \leq 6.0V$

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

Control Outputs

The CARRY/BORROW output is a positive going pulse occurring typically 500ns after the positive going edge of the COUNT INPUT. It occurs when the counter is clocked from 9999 to 0000 when counting up and from 0000 to 9999 when counting down. This output allows direct cascading of counters. The CARRY/BORROW output is not valid during load counter and reset operation. When the count is 6000 or higher, a reset generates a CARRY/BORROW pulse.

The $\overline{\text{EQUAL}}$ output assumes a negative level when the contents of the counter and register are equal.

The $\overline{\text{ZERO}}$ output assumes a negative level when the content of the counter is 0000.

The CARRY/BORROW, $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs will drive a single TTL load over the full range of supply voltage and ambient temperature; for a logic zero, these outputs will sink 1.6mA @ 0.4V and for a logic one, the outputs will source>60μA. A 10kΩ pull-up resistor to V_{DD} on the $\overline{\text{EQUAL}}$ or $\overline{\text{ZERO}}$ outputs is recommended for highest speed operation, and on the CARRY/BORROW output when it is being used for cascading. Figure 5 shows control outputs timing diagram.

Display Outputs and Control

The Digit and SEGment drivers provide a decoded 7 segment display system, capable of directly driving common anode LED displays at typical peak currents of 35mA/seg. This corresponds to average currents of 8mA/seg at a 25% multiplex duty cycle. For the common cathode versions, peak segment currents are 12.5mA, corresponding to average segment currents of 3.1mA. Figure 4 shows the multiplex timing. The DISPLAY pin controls the display output using three level logic. The pin is self-biased to a voltage approximately ½ (V_{DD}); this corresponds to normal operation. When this pin is connected to V_{DD}, the segments are disabled and when connected to V_{SS}, the leading zero blanking feature is inhibited. For normal operation (display on with leading zero blanking) the pin should be left open. The display may be controlled with a 3 position SPDT switch; see Figure 3.

Multiplex SCAN Oscillator

The on-board multiplex scan oscillator has a nominal free-running frequency of 2.5kHz. This may be reduced by the addition of a single capacitor between the SCAN pin and the positive supply. Capacitor values and corresponding nominal oscillator frequencies, digit repetition rates, and loading times are shown in Table 1 below.

Table 1: ICM7217 Multiplexed Rate Control

Scan Capacitor	Nominal Oscillator Frequency	Digit Repetition Rate	Scan Cycle Time (4 digits)
None	2.5kHz	625Hz	1.6ms
20pF	1.25kHz	300Hz	3.2ms
90pF	600Hz	150Hz	8ms

The internal oscillator output has a duty cycle of approximately 25:1, providing a short pulse occurring at the oscillator frequency. This pulse clocks the four-state counter which provides the four multiplex phases. The short pulse width is used to delay the digit driver outputs, thereby providing inter-digit blanking which prevents ghosting. The digits are scanned from MSD (D4) to LSD (D1). See Figure 4 for the display digit multiplex timing.

During **load counter** and **load register** operations, the multiplex oscillator is disconnected from the SCAN input and is allowed to free-run. In all other conditions, the oscillator may be directly overdriven to about 20kHz, however the external oscillator signal should have the same duty cycle as the internal signal, since the digits are blanked during the time the external signal is at a positive level (see Figure 4). To insure proper leading zero blanking, the interdigit blanking time should not be less than about 2μs. Overdriving the oscillator at less than 200Hz may cause display flickering.

The display brightness may be altered by varying the duty cycle. Figure 7 shows several variable-duty-cycle oscillators suitable for brightness control at the ICM7217 SCAN input. The inverters should be CMOS CD4000 series and the diodes may be any inexpensive device such as IN914.

Counting Control, $\overline{\text{STORE}}$, $\overline{\text{RESET}}$

As shown in Figure 5, the counter is incremented by the rising edge of the COUNT INPUT signal when UP/$\overline{\text{DOWN}}$ is high. It is decremented when UP/$\overline{\text{DOWN}}$ is low. A Schmitt trigger on the COUNT INPUT provides hysteresis to prevent double triggering on slow rising edges and permits operation in noisy environments. The COUNT INPUT is inhibited during reset and **load counter** operations.

The $\overline{\text{STORE}}$ pin controls the internal latches and consequently the signals appearing at the 7-segment and BCD outputs. Bringing the $\overline{\text{STORE}}$ pin low transfers the contents of the counter into the latches.

The counter is asynchronously reset to 0000 by bringing the $\overline{\text{RESET}}$ pin low. The circuit performs the reset operation by forcing the BCD input lines to zero, and "presetting" all four decades of counter in parallel. This affects register loading; if LOAD REGISTER is activated when the $\overline{\text{RESET}}$ input is low, the register will also be set to zero. The $\overline{\text{STORE}}$, $\overline{\text{RESET}}$ and UP/$\overline{\text{DOWN}}$ pins are provided with pull-up resistors of approximately 75kΩ.

BCD I/O Pins

The BCD I/O port provides a means of transferring data to and from the device. The ICM7217 versions can multiplex data into the counter or register via thumbwheel switches, depending on inputs to the LOAD COUNTER or LOAD REGISTER pins; (see below). When functioning as outputs, the BCD I/O pins will drive one standard TTL load. Common anode versions have internal pull down resistors and common cathode versions have internal pull up resistors on the four BCD I/O lines when used as inputs.

NOTE: All typical values have been characterized but are not tested.

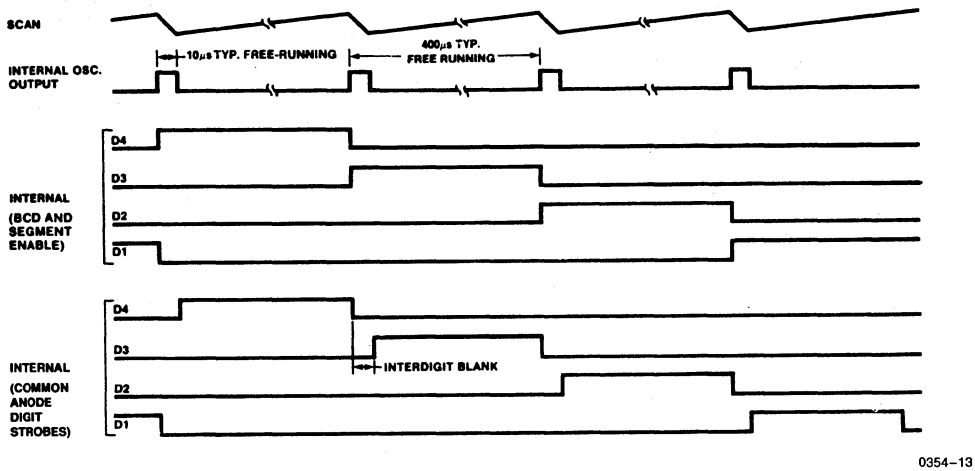


Figure 4: Multiplex Timing

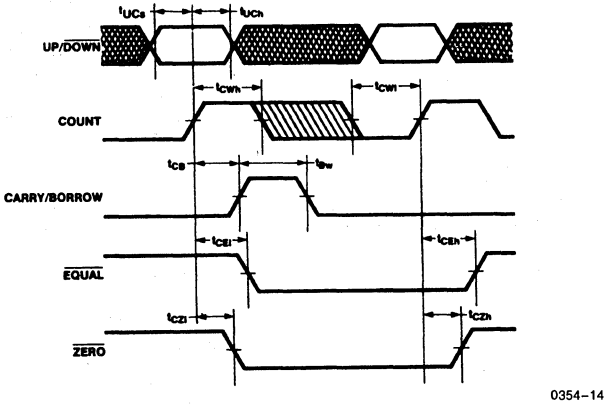


Figure 5: ICM7217 COUNT and Outputs Timing

NOTE: All typical values have been characterized but are not tested.

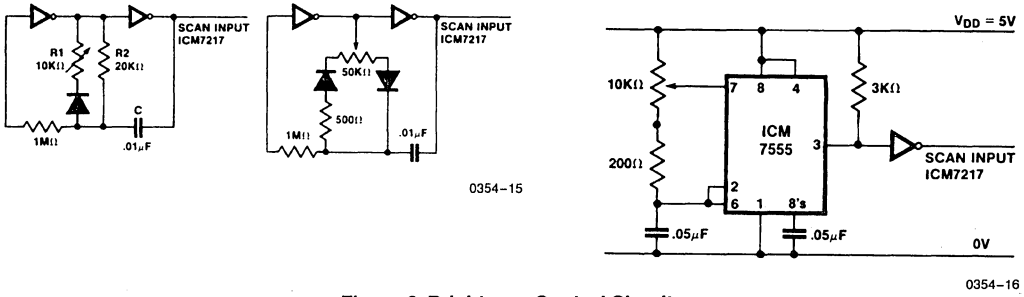


Figure 6: Brightness Control Circuits

LOADing the COUNTER and REGISTER

The BCD I/O pins, the LOAD COUNTER (LC), and LOAD REGISTER (LR) pins combine to provide presetting and compare functions. LC and LR are three-level inputs, being self-biased at approximately $\frac{1}{2}V_{DD}$ for normal operation. With both LC and LR open, the BCD I/O pins provide a multiplexed BCD output of the latch contents, scanned from MSD to LSD by the display multiplex.

When either the LOAD COUNTER (Pin 12) or LOAD REGISTER (Pin 11) is taken low, the drivers are turned off and the BCD pins become high-impedance inputs. When LC is connected to V_{DD}, the count input is inhibited and the levels at the BCD pins are multiplexed into the counter. When LR is connected to V_{DD}, the levels at the BCD pins are multiplexed into the register without disturbing the counter. When both are connected to V_{DD}, the count is inhibited and both register and counter will be loaded.

The LOAD COUNTER and LOAD REGISTER inputs are edge-triggered, and pulsing them high for 500ns at room temperature will initiate a full sequence of data entry cycle operations (see Figure 9). When the circuit recognizes that either or both of the LC or LR pins input is high, the multiplex oscillator and counter are reset (to D4). The internal oscillator is then disconnected from the SCAN pin and the preset circuitry is enabled. The oscillator starts and runs with a frequency determined by its internal capacitor, (which may vary from chip to chip). When the chip finishes a full 4 digit multiplex cycle (loading each digit from D4 to D3 to D2 to D1 in turn), it again samples the LOAD REGISTER and LOAD COUNTER inputs. If either or both is still high, it repeats the load cycle, if both are floating or low, the oscillator is reconnected to the SCAN pin and the chip returns to normal operation. Total load time is digit "on" time multiplied by 4. If the Digit outputs are used to strobe the BCD data into the BCD I/O inputs, the input must be synchronized to the appropriate digit (Figure 9). Input data must be valid at the trailing edge of the digit output.

When LR is connected to GROUND, the oscillator is inhibited, the BCD I/O pins go to the high impedance state, and the segment and digit drivers are turned off. This allows the display to be used for other purposes and minimizes power consumption. In this display off condition, the circuit will continue to count, and the CARRY/BORROW, $\overline{\text{EQUAL}}$, $\overline{\text{ZERO}}$, UP/$\overline{\text{DOWN}}$, $\overline{\text{RESET}}$ and $\overline{\text{STORE}}$ functions operate as normal. When LC is connected to ground, the BCD I/O pins are forced to the high impedance state without disturbing the counter or register. See "Control Input Definitions" (Table 2) for a list of the pins that function as three-state self-biased inputs and their respective operations.

Note that the ICM7217 and 7217B have been designed to drive common anode displays. The BCD inputs are high true, as are the BCD outputs.

The ICM7217A and the 7217C are used to drive common cathode displays, and the BCD inputs are low true. BCD outputs are high true.

Notes on Thumbwheel Switches & Multiplexing

As it was mentioned, the ICM7217 is basically designed to be used with thumbwheel switches for loading the data to the device. See Figures 11 and 14.

The thumbwheel switches used with these circuits (both common anode and common cathode) are TRUE BCD coded; i.e. all switches open corresponds to 0000. Since the thumbwheel switches are connected in parallel, diodes must be provided to prevent crosstalk between digits. In order to maintain reasonable noise margins, these diodes should be specified with low forward voltage drops (IN914). Similarly, if the BCD outputs are to be used, resistors should be inserted in the Digit lines to avoid loading problems.

NOTE: All typical values have been characterized but are not tested.

Table 2: Control Input Definitions ICM7217

Input	Terminal	Voltage	Function
$\overline{\text{STORE}}$	9	V_{DD} (or floating) V_{SS}	Output latches not updated Output latches updated
UP/$\overline{\text{DOWN}}$	10	V_{DD} (or floating) V_{SS}	Counter counts up Counter counts down
$\overline{\text{RESET}}$	14	V_{DD} (or floating) V_{SS}	Normal Operation Counter Reset
LOAD COUNTER/ $\overline{\text{I/O OFF}}$	12	Unconnected V_{DD} V_{SS}	Normal operation Counter loaded with BCD data BCD port forced to Hi Z condition
LOAD REGISTER/ $\overline{\text{OFF}}$	11	Unconnected V_{DD} V_{SS}	Normal operation Register loaded with BCD data Display drivers disabled; BCD port forced to Hi Z condition, mpx counter reset to D4; mpx oscillator inhibited
DISPLAY CONTrol	23 Common Anode 20 Common Cathode	Unconnected V_{DD} V_{SS}	Normal Operation Segment drivers disabled Leading zero blanking inhibited

Output and Input Restrictions

LOAD COUNTER and LOAD REGISTER operations take 1.6ms typical (5ms maximum) after LC or LR are released. During this load period the $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs are not valid (see Figure 9). Since the Counter and register are compared by XOR gates, loading the counter or register can cause erroneous glitches on the $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs when codes cross.

LOAD COUNTER or LOAD REGISTER, and $\overline{\text{RESET}}$ input can not be activated at the same time or within a short period of each other. Operation of each input must be delayed 1.6ms typical (5ms for guaranteed proper operation) relating to the preceding one.

Counter and register can be loaded together with the same value if LC and LR inputs become activated exactly at the same time.

Notice the setup and hold time of UP/$\overline{\text{DOWN}}$ input when it is changing during counting operation. Violation of UP/$\overline{\text{DOWN}}$ hold time will result in incrementing or decrementing the counter by 1000, 100 or 10 where the preceding digit is transitioning from 5 to 6 or 6 to 5.

The $\overline{\text{RESET}}$ input may be susceptible to noise if its input rise time is greater than about 500μs. This will present no problems when this input is driven by active devices (i.e., TTL or CMOS logic) but in hardwired systems adding virtually any capacitance to the $\overline{\text{RESET}}$ input can cause trouble. A simple circuit which provides a reliable power-up reset and a fast rise time on the $\overline{\text{RESET}}$ input is shown on Figure 7.

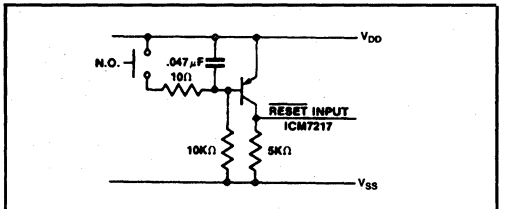


Figure 7

When using the circuit as a programmable divider (÷ by n with equal outputs) a short time delay (about 1μs) is needed from the $\overline{\text{EQUAL}}$ output to the $\overline{\text{RESET}}$ input to establish a pulse of adequate duration. (See Figure 8)

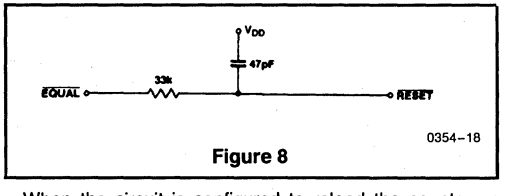


Figure 8

When the circuit is configured to reload the counter or register with a new value from the BCD lines (upon reaching $\overline{\text{EQUAL}}$), loading time will be digit "on" time multiplied by four. If this load time is longer than one period of the input count, a count can be lost. Since the circuit will retain data in the register, the register need only be updated when a new value is to be entered. $\overline{\text{RESET}}$ will not clear the register.

NOTE: All typical values have been characterized but are not tested.

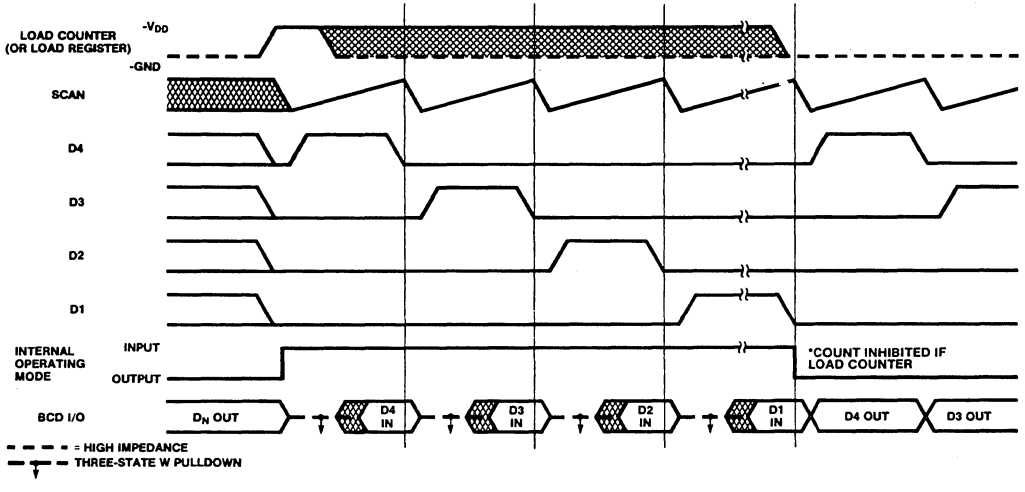


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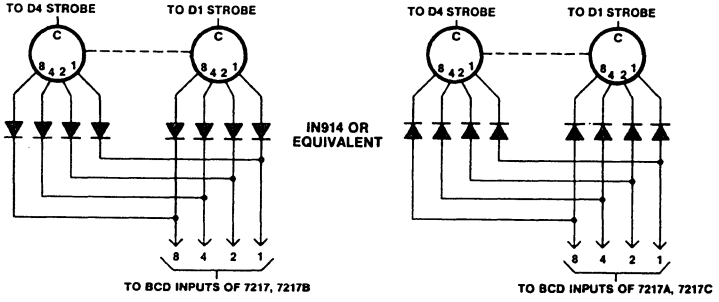
Figure 9: ICM7217 BCD I/O and Loading Timing



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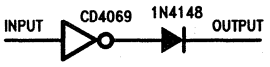
Note: If the BCD pins are to be used for outputs a 10kΩ resistor should be placed in series with each digit line to avoid loading problems through the switches.

Figure 10: Thumbwheel Switch/Diode Connections

11

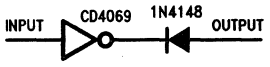
NOTE: All typical values have been characterized but are not tested.

CMOS Inverter



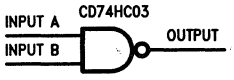
Input	Output
High	High
Low	Disconnected

CMOS Inverter



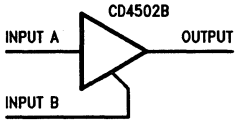
Input	Output
High	Disconnected
Low	Low

CMOS Open Drain



Input B	Input A	Output
High	High	Low
High	Low	Disconnected
Low	High	Disconnected
Low	Low	Disconnected

CMOS 3-State Buffer



Input B	Input A	Output
High	High	Disconnected
High	Low	Disconnected
Low	High	High
Low	Low	Low

Figure 11: Driving 3-Level Inputs of ICM7217

NOTE: All typical values have been characterized but are not tested.

APPLICATIONS

3-LEVEL INPUTS

ICM7217 has three inputs with 3-level logic states; High, Low and Disconnected. These inputs are: LOAD REGISTER/$\overline{\text{OFF}}$, LOAD COUNTER/$\overline{\text{I/O OFF}}$ and DISPLAY CONT.

The circuits illustrated on Figure 11 can be used to drive these inputs in different applications.

FIXED DECIMAL POINT

In the common anode versions, a fixed decimal point may be activated by connecting the D.P. segment lead from the appropriate digit (with separate digit displays) through a 39Ω series resistor to Ground. With common cathode devices, the D.P. segment lead should be connected through a 75Ω series resistor to V_{DD}.

To force the device to display leading zeroes after a fixed decimal point, use a bipolar transistor and base resistor in a configuration like that shown below with the resistor connected to the digit output driving the D.P. for left hand D.P. displays, and to the next least significant digit output for right hand D.P. display.

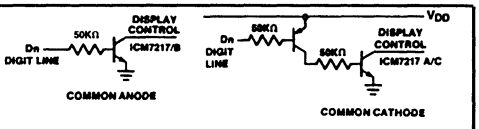


Figure 12: Forcing Leading Zero Display

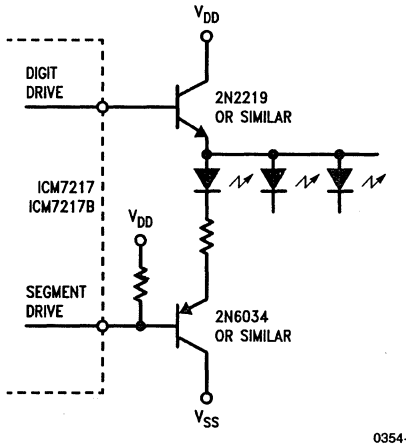
DRIVING LARGER DISPLAYS

For displays requiring more current than the ICM7217 can provide, the circuits of Figure 13 can be used.

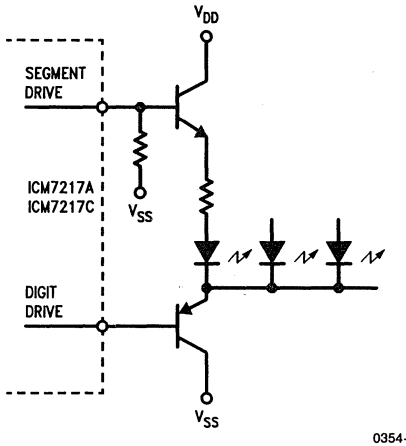
LCD DISPLAY INTERFACE

The low-power operation of the ICM7217 makes an LCD interface desirable. The Harris ICM7211 4 digit BCD to LCD display driver easily interfaces to the ICM7217 as shown in Figure 14. Total system power consumption is less than 5mW. System timing margins can be improved by using capacitance to ground to slow down the BCD lines.

The 10 – 20kΩ resistors on the switch BCD lines serve to isolate the switches during BCD output.



Common Anode Display



Common Cathode Display

Figure 13: Driving High Current Displays

11

NOTE: All typical values have been characterized but are not tested.

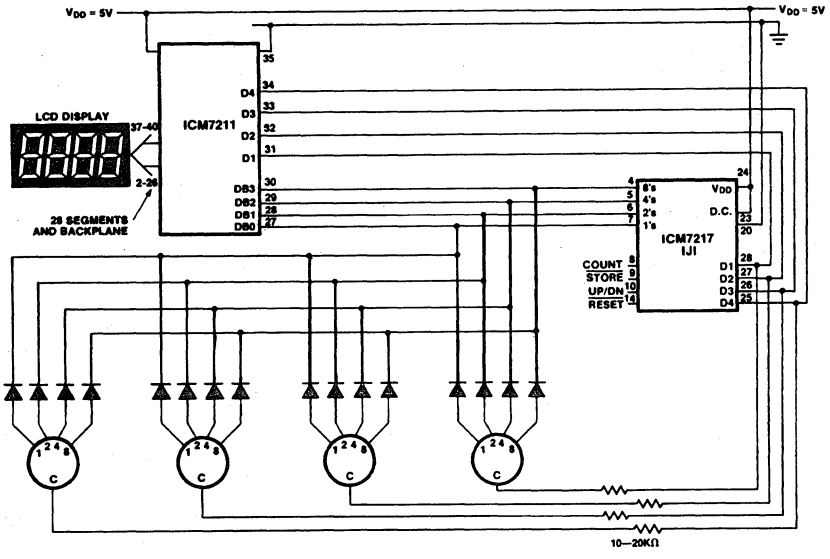


Figure 14: LCD Display Interface (with Thumbwheel Switches)

UNIT COUNTER WITH BCD OUTPUT

The simplest application of the ICM7217 is a 4 digit unit counter (Figure 15). All that is required is an ICM7217, a power supply and a 4 digit display. Add a momentary switch for reset, an SPDT center-off switch to blank the display or view leading zeroes, and one more SPDT switch for up/down control. Using an ICM7217A with a common-cathode calculator-type display results in the least expensive digital counter/display system available.

INEXPENSIVE FREQUENCY COUNTER/ TACHOMETER

This circuit uses the low power ICM7555 (CMOS 555) to generate the gating, $\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ signals as shown in Figure 16. To provide the gating signal, the timer is configured as an astable multivibrator, using R_A, R_B and C to provide an output that is positive for approximately one second and negative for approximately 300 – 500μs. The positive waveform time is given by $t_{wp} = 0.693\ (R_A + R_B)C$ while the negative waveform is given by $t_{wn} = 0.693\ R_BC$. The system is calibrated by using a 5MΩ potentiometer for R_A as a "coarse" control and a 1kΩ potentiometer for R_B as a "fine" control. CD40106B's are used as a monostable multivibrator and reset time delay.

TAPE RECORDER POSITION INDICATOR/CONTROLLER

The circuit in Figure 17 shows an application which uses the up/down counting feature of the ICM7217 to keep track of tape position. This circuit is representative of the many applications of up/down counting in monitoring dimensional position.

In the tape recorder application, the LOAD REGISTER, $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs are used to control the recorder. To make the recorder stop at a particular point on the tape, the register can be set with the stop point and the $\overline{\text{EQUAL}}$ output used to stop the recorder either on fast forward, play or rewind.

To make the recorder stop before the tape comes free of the reel on rewind, a leader should be used. Resetting the counter at the starting point of the tape, a few feet from the end of the leader, allows the $\overline{\text{ZERO}}$ output to be used to stop the recorder on rewind, leaving the leader on the reel.

The 1MΩ resistor and .0047μF capacitor on the COUNT INPUT provide a time constant of about 5ms to debounce the reel switch. The Schmitt trigger on the COUNT INPUT of the ICM7217 squares up the signal before applying it to the counter. This technique may be used to debounce switch-closure inputs in other applications.

PRECISION ELAPSED TIME/ COUNTDOWN TIMER

The circuit in Figure 18 uses an ICM7213 precision one minute/one second timebase generator using a 4.1943MHz crystal for generating pulses counted by an ICM7217B. The thumbwheel switches allow a starting time to be entered into the counter for a preset-countdown type timer, and allow the register to be set for compare functions. For instance, to make a 24-hour clock with BCD output the register can be preset with 2400 and the $\overline{\text{EQUAL}}$ output used to reset the counter. Note the 10k resistor connected between the LOAD COUNTER terminal and Ground. This resistor pulls the LOAD COUNTER input low when not loading, thereby inhibiting the BCD output drivers. This resistor should be eliminated and SW4 replaced with an SPDT center-off switch if the BCD outputs are to be used.

NOTE: All typical values have been characterized but are not tested.

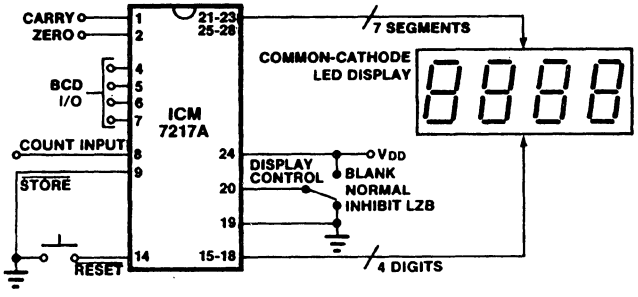


Figure 15: Unit Counter

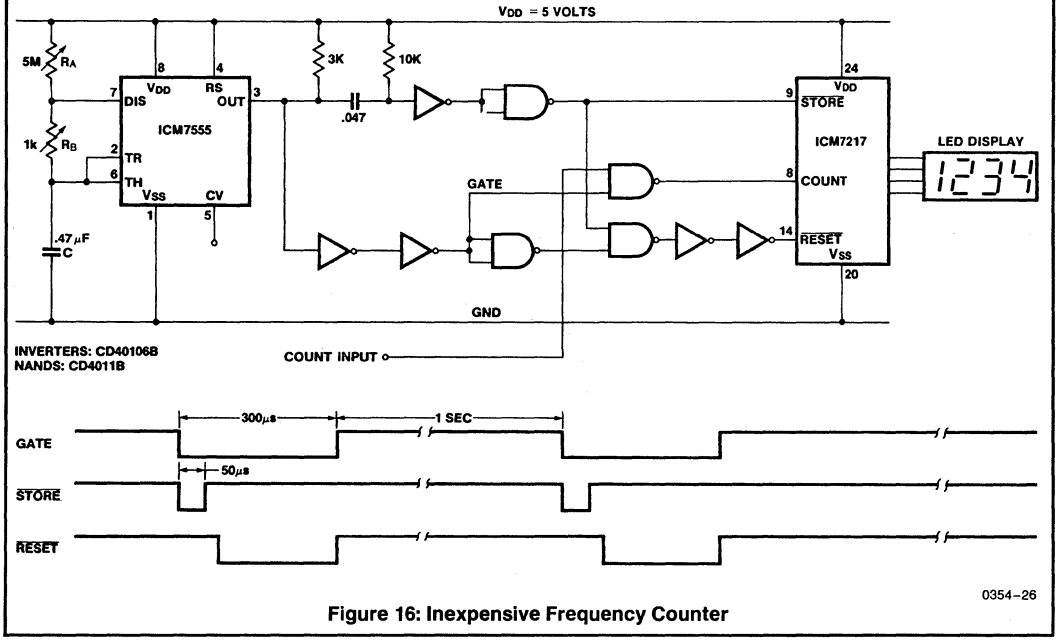


Figure 16: Inexpensive Frequency Counter

11

NOTE: All typical values have been characterized but are not tested.

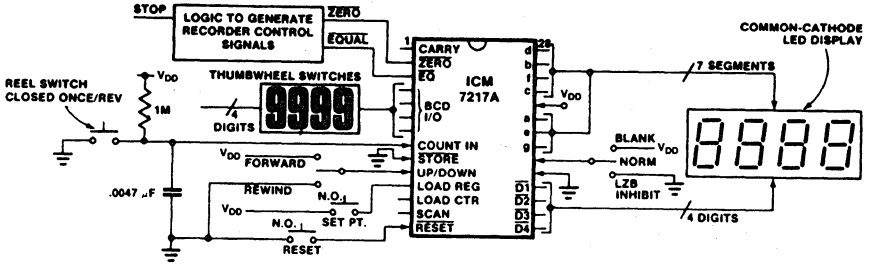


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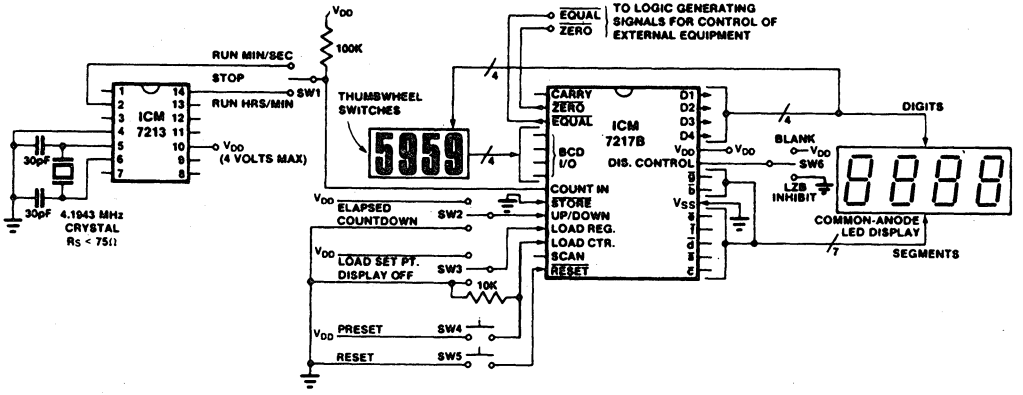
Figure 17: Tape Recorder Position Indicator



0354-28

Figure 18: Precision Timer

NOTE: All typical values have been characterized but are not tested.

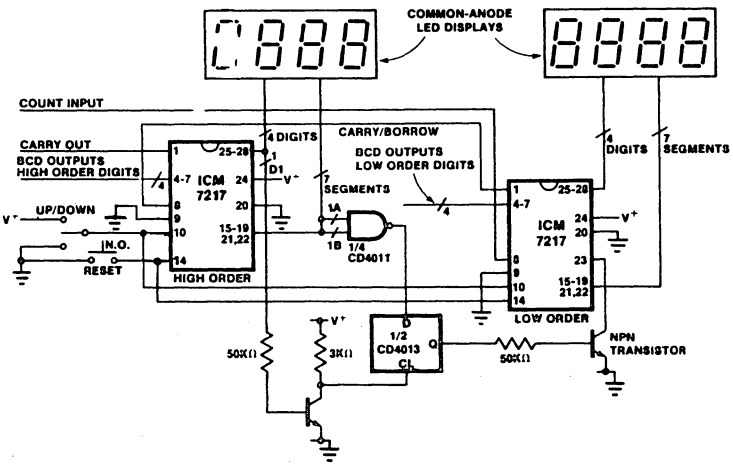


Figure 19: 8 Digit Up/Down Counter

This technique may be used on any 3-level input. The 100kΩ pullup resistor on the count input is used to ensure proper logic voltage swing from the ICM7213. For a less expensive (and less accurate) timebase, an ICM7555 timer may be used in a configuration like that shown in Figure 16 to generate a 1Hz reference.

8-DIGIT UP/DOWN COUNTER

This circuit (Figure 19) shows how to cascade counters and retain correct leading zero blanking. The NAND gate detects whether a digit is active since one of the two segments $\overline{a}$ or $\overline{b}$ is active on any unblanked number. The flip flop is clocked by the least significant digit of the high order counter, and if this digit is not blanked, the Q output of the flip flop goes high and turns on the NPN transistor, thereby inhibiting leading zero blanking on the low order counter.

It is possible to use separate thumbwheel switches for presetting, but since the devices load data with the oscillator free-running, the multiplexing of the two devices is difficult to synchronize.

PRECISION FREQUENCY COUNTER/ TACHOMETER

The circuit shown in Figure 20 is a simple implementation of a four digit frequency counter, using an ICM7207A to provide the one second gating window and the $\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ signals. In this configuration, the display reads hertz directly. With Pin 11 of the ICM7027A connected to V_{DD}, the gating time will be 0.1 second; this will display tons of hertz at the least significant digit. For shorter gating times, an ICM7207 may be used (with a 6.5536MHz crystal), giving a 0.01 second gating with Pin 11 connected to V_{DD}, and a 0.1 second gating with Pin 11 open.

To implement a four digit tachometer, the ICM7207A with one second gating should be used. To get the display to read directly in RPM, the rotational frequency of the object to be measured must be multiplied by 60. This can be done electronically using a phase-locked loop, or mechanically by using a disc rotating with the object with the appropriate number of holes drilled around its edge to interrupt the light from an LED to a photo-dector. For faster updating, use 0.1 second gating, and multiply the rotational frequency by 600.

AUTO-TARE SYSTEM

This circuit uses the count-up and count-down functions of the ICM7217, controlled via the $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs, to count in SYNC with an ICL7109 A/D Converter as shown in Figure 21. By $\overline{\text{RESET}}$ing the ICM7217 on a "tare" value conversion, and $\overline{\text{STORE}}$-ing the result of a true value conversion, an automatic tare subtraction occurs in the result.

The ICM7217 stays in step with the ICL7109 by counting up and down between 0 and 4095, for 8192 total counts, the same number as the ICL7109 cycle. See applications note #A047 for more details.

NOTE: All typical values have been characterized but are not tested.

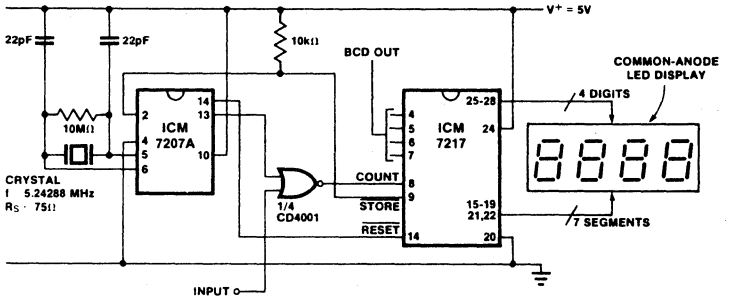


Figure 20: Precision Frequency Counter (MHz Maximum)

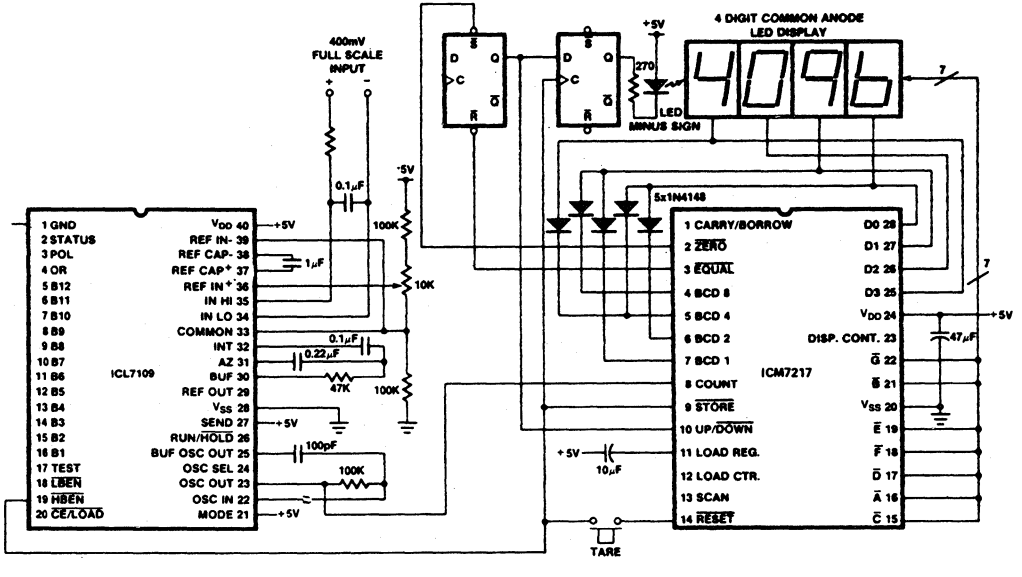


Figure 21: Auto-Tare System for A/D Converter

NOTE: All typical values have been charecterized but are not tested.

HARRIS SEMICONDUCTOR

ICM7224
4½-Digit LCD Display Counter

GENERAL DESCRIPTION

The ICM7224 device is a high-performance CMOS 4½-digit counter, including decoder, output latch, display driver, count inhibit, leading zero blanking, and reset circuitry.

The counter section provides direct static counting, guaranteed from DC to 15 MHz, using a 5V ±10% supply over the operating temperature range. At normal ambient temperatures, the devices will typically count up to 25 MHz. The COUNT input is provided with a Schmitt trigger to allow operation in noisy environments and correct counting with slowly changing inputs. The COUNT INHIBIT, STORE and RESET inputs allow a direct interface with the ICM7207/A to implement a low cost, low power frequency counter with a minimum component count.

These devices also incorporate several features intended to simplify cascading four-digit blocks. The CARRY output allows the counter to be cascaded, while the Leading Zero Blanking INput and OUTput allows correct Leading Zero Blanking between four-decade blocks. The BackPlane driver of the LCD devices may be disabled, allowing the segments to be slaved to another backplane signal, necessary when using an eight or twelve digit, single backplane display.

These devices provide maximum count of 19999. The display drivers are not of the multiplexed type and each display segment has its own individual drive pin, providing high quality display outputs. The ICM7224 drives LCD displays.

The ICM7224 is packaged in a standard 40-pin dual-in-line plastic or CERDIP package, or in dice.

FEATURES

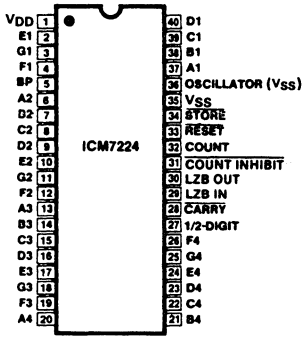
- **High Frequency Counting — Guaranteed 15MHz, Typically 25MHz at 5V**
- **Low Power Operation — Typically Less Than 100μW Quiescent**
- **$\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ Inputs Permit Operation as Frequency or Period Counter**
- **True $\overline{\text{COUNT INHIBIT}}$ Disables First Counter Stage**
- **$\overline{\text{CARRY}}$ Output for Cascading Four-Digit Blocks**
- **Schmitt-Trigger On The COUNT Input Allows Operation in Noisy Environments or With Slowly Changing Inputs**
- **Leading Zero Blanking INput and OUTput for Correct Leading Zero Blanking With Cascaded Devices**
- **LCD Devices Provide Complete Onboard Oscillator and Divider Chain to Generate Backplane Frequency, or Backplane Driver May Be Disabled Allowing Segments to be Slaved to A Master Backplane Signal**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7224IPL	-25°C to +85°C	40 Pin Plastic DIP
ICM7224IJL	-25°C to +85°C	40 Pin CERDIP
ICL7224RIPL*	-25°C to +85°C	40 Pin Plastic DIP

* "R" indicates device with reversed leads configuration.

ICM7224 Direct Drive LCD



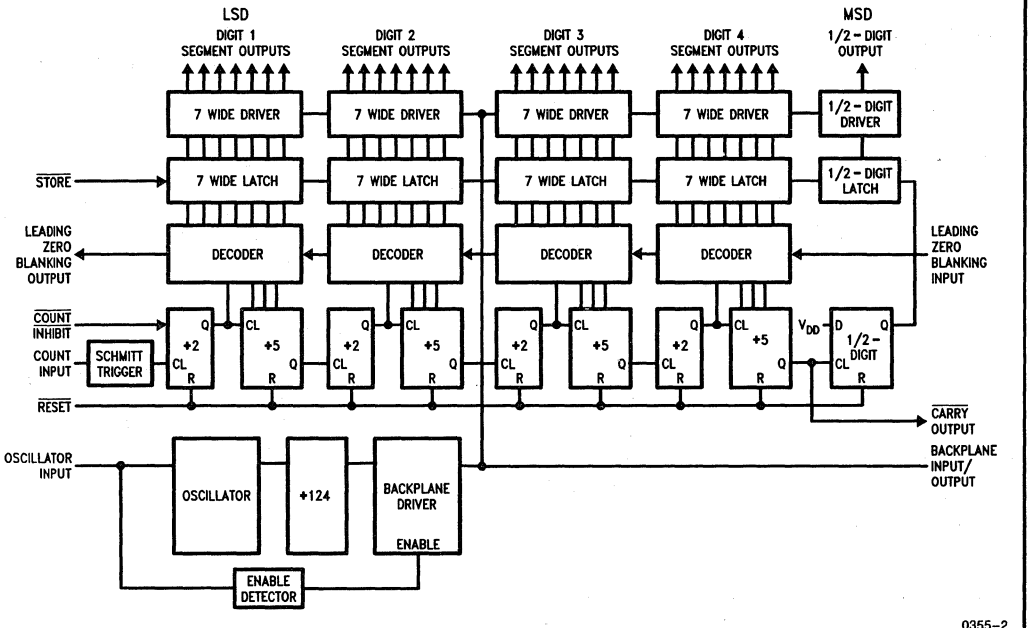
0355-1

Figure 1: Pin Configuration

NOTE: All typical values have been characterized but are not tested.

ICM7224/ICM7225

ICM7224, LCD Display



ICM7225, LED Display

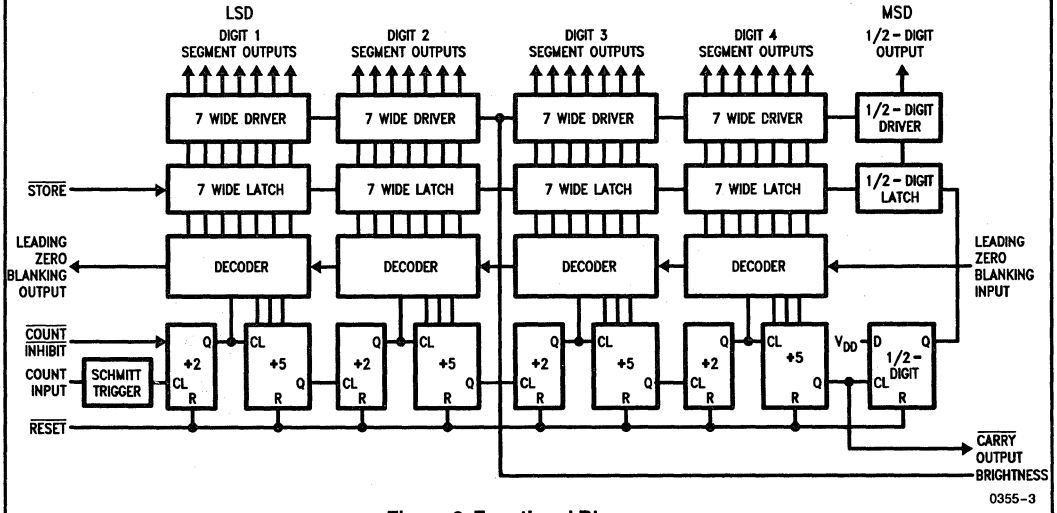


Figure 2: Functional Diagrams

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{DD}-V_{SS}$) 6.5V
Input Voltage (Any Terminal) (Note 2) ..... ($V_{DD}+0.3V$) to ($V_{SS}-0.3V$)
Power Dissipation (Note 1) ..... 0.5W @ 70°C
Operating Temperature Range ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE 1: This limit refers to that of the package and will not be obtained during normal operation.

2: Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from sources operating on a different power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7224/ICM7225 be turned on first.

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS ($V_{DD}=5V$, $V_{SS}=0V$, $T_A=25°C$, unless otherwise indicated)

ICM7224 CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Operating current	Test circuit, Display blank		10	50	µA
V_{SUPPLY}	Operating supply voltage range ($V_{DD}-V_{SS}$)		3		6	V
I_{OSCI}	OSCILLATOR input current	Pin 36		±2	±10	µA
t_R, t_F	Segment rise/fall time	$C_{load}=200pF$		0.5		µs
t_R, t_F	BackPlane rise/fall time	$C_{load}=5000pF$		1.5		
f_{OSC}	Oscillator frequency	Pin 36 Floating		19		kHz
f_{BP}	Backplane frequency	Pin 36 Floating		150		Hz

ICM7225 CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{STBY}	Operating current display off	Pin 5 (BRighTness) at V_{SS} Pins 29, 31-34 at V_{DD}		10	50	µA
V_{SUPP}	Operating supply voltage range ($V_{DD}-V_{SS}$)		4		6	V
I_{DD}	Operating current	Pin 5 at V_{DD}, Display 18888		200		mA
I_{SLK}	Segment leakage current	Segment Off		±0.01	±1	µA
I_{SEG}	Segment on current	Segment On, Vout = +3V	5	8		mA
I_H	Half-digit on current	Half-digit on, Vout = +3V	10	16		

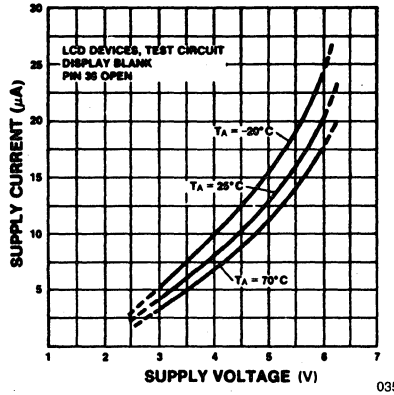
FAMILY CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_P	Input Pullup Currents	Pins 29, 31, 33, 34 Vin = $V_{DD}-3V$		10		µA
V_{IH}	Input High Voltage	Pins 29, 31, 33, 34	3			V
V_{IL}	Input Low Voltage	Pins 29, 31, 33, 34			1	
V_{CT}	$\overline{COUNT}$ Input Threshold			2		
V_{CH}	$\overline{COUNT}$ Input Hysteresis			0.5		
I_{OH}	Output High Current	$\overline{CARRY}$ Pin 28 Leading Zero Blanking OUT Pin 30 Vout = $V_{DD}-3V$	−350	−500		µA
I_{OL}	Output Low Current	$\overline{CARRY}$ Pin 28 Leading Zero Blanking OUT Pin 30 Vout = +3V	350	500		
f_{COUNT}	Count Frequency	$4.5V<V_{DD}<6V$	0		15	MHz
t_S,t_R	$\overline{STORE}$, $\overline{RESET}$ Minimum Pulse Width		3			µs

NOTE: All typical values have been characterized but are not tested.

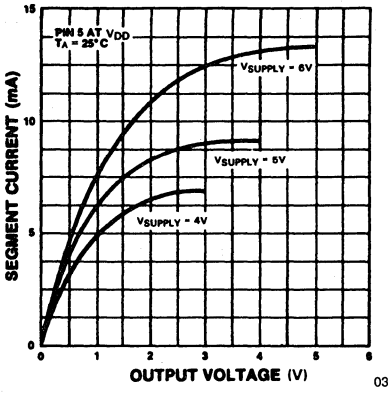
TYPICAL PERFORMANCE CHARACTERISTICS

7224 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



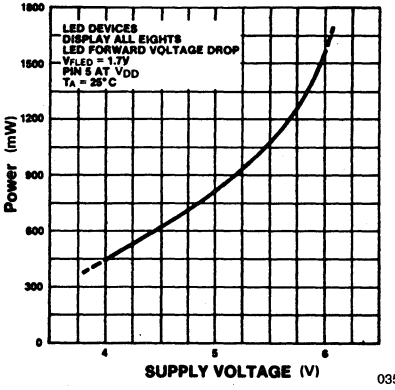
0355-4

7225 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



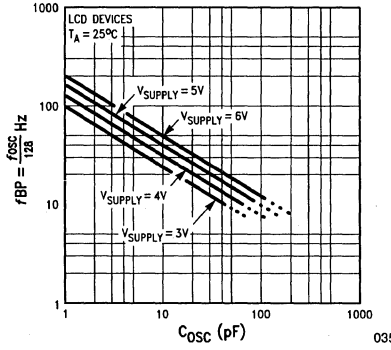
0355-5

7225 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE



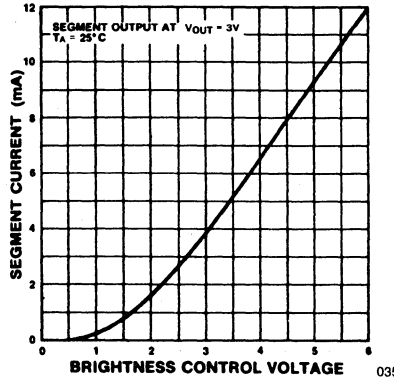
0355-7

7224 BACKPLANE FREQUENCY AS A FUNCTION OF OSCILLATOR CAPACITOR C_{OSC}



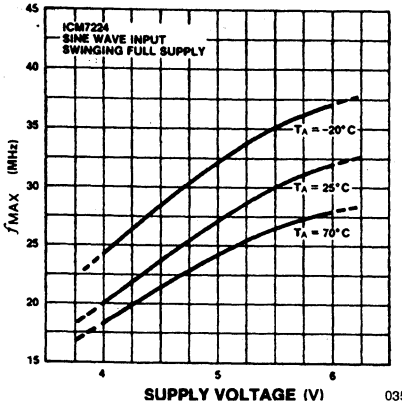
0355-8

7225 LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE



0355-9

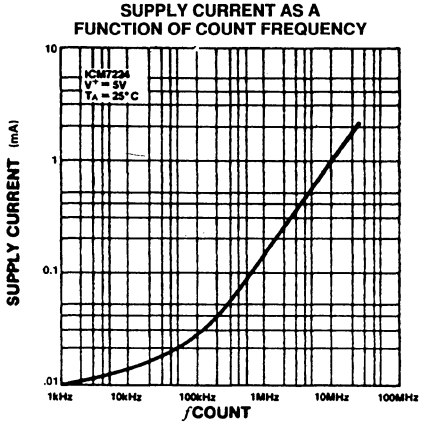
MAXIMUM COUNT FREQUENCY (TYPICAL) AS A FUNCTION OF SUPPLY VOLTAGE



0355-10

NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)



0355-11

TABLE I: Control Input Definitions

INPUT	TERMINAL	VOLTAGE	FUNCTION
Leading Zero Blanking INput	29	V_{DD} or Floating V_{SS}	Leading Zero Blanking Enabled Leading Zeroes Displayed
$\overline{\text{COUNT INHIBIT}}$	31	V_{DD} or Floating V_{SS}	Counter Enabled Counter Disabled
$\overline{\text{RESET}}$	33	V_{DD} or Floating V_{SS}	Inactive Counter Reset to 0000
$\overline{\text{STORE}}$	34	V_{DD} or Floating V_{SS}	Output Latches not Updated Output Latches Updated

CONTROL INPUT DEFINITIONS

In Table I, V_{DD} and V_{SS} are considered to be normal operating input logic levels. Actual input low and high levels are specified in the Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

DETAILED DESCRIPTION

LCD Device

The LCD device provides outputs suitable for driving conventional 4½-digit by seven segment LCD displays. They include 29 individual segment drivers, a backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency (See Figure 4).

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any D.C. component which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output can be disabled by connecting the OSCILLATOR input (pin 36) to V_{SS}. This synchronizes the 29 segment outputs directly with a signal input at the BP terminal (pin 5) and allows cascading of several slave devices to the backplane output of one master device. The backplane may also be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device will represent a load of approximately 200pF (comparable to one additional segment). The limitation on the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits, and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimize power consumption, is to keep the rise and fall times less than about 5 microseconds. The backplane driver of one device should handle the backplane to a display of 16 one-half-inch characters without the rise and fall times exceeding 5μs (ie, 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM7224 devices be slaved to it.

This external backplane signal should be capable of driving very large capacitive loads with short (1-2μs) rise and fall times. The maximum frequency for a backplane signal should be about 150Hz, although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 19kHz, at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 150Hz with the oscilla-

11

NOTE: All typical values have been characterized but are not tested.

tor free-running. The oscillator frequency may be reduced by connecting an external capacitor between the OSCillator terminal (pin 36) and V_{DD}; see the plot of oscillator/backplane frequency in "Typical Characteristics" for detailed information.

The oscillator may also be overdriven if desired, although care must be taken to insure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a D.C. component to the display). This can be done by driving the OSCILLATOR input between the positive supply and a level out of the range where the backplane disable is sensed, about one fifth of the supply voltage above the negative supply. Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

LED Device

The LED device provides outputs suitable for directly driving 4½-digit by seven segment common-anode LED displays. They include 28 individual segment drivers and one half-digit driver, each consisting of a low-leakage current-controlled open-drain n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the BRighTness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Figure 3. The potentiometer should be a high value (100kΩ to 1MΩ) to minimize power consumption, which can be significant when the display is off.

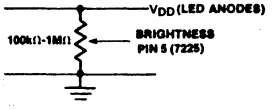
The BRighTness input may also be operated digitally as a display enable; when at V_{DD}, the display is fully on, and at V_{SS}, fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two supplies at the BRighTness input.

Note that the LED devices have two connections for V_{SS}; both should be connected. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating the LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (15mW/°C above 35°C). Power dissipation for the device is given by:

$$P = (V_{DD} - V_{FLED}) \times (I_{SEG}) \times (n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "ON" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the BRighTness input to keep power dissipation within the limits described above.



0355-12

Figure 3: Brightness Control

COUNTER SECTION

The devices in the ICM7224/ICM7225 family implement a four-digit ripple carry resettable counter, including a Schmitt trigger on the COUNT input and a $\overline{\text{CARRY}}$ output. Also included is an extra D-type flip-flop, clocked by the $\overline{\text{CARRY}}$ signal which controls the half-digit segment driver. This output driver can be used as either a true half-digit or as an overflow indicator. The counter will increment on the negative-going edge of the signal at the COUNT input, while the $\overline{\text{CARRY}}$ output provides a negative-going edge following the count which increments the counter from 9999 to 10000. Once the half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the $\overline{\text{RESET}}$ terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half-digit is set, and subsequent $\overline{\text{CARRY}}$ outputs will not be affected.

A negative level at the $\overline{\text{COUNT INHIBIT}}$ input disables the first divide-by-two in the counter chain without affecting its clock. This provides a true inhibit, not sensitive to the state of the COUNT input, which prevents false counts that can result from using a normal logic gate to prevent counting.

Each decade of the counter directly drives a four-to-seven segment decoder which develops the required output data. The output data is latched at the driver. When the $\overline{\text{STORE}}$ pin is low, these latches are updated, and when it is high or floating, the latches hold their contents.

The decoders also include zero detect and blanking logic to provide leading zero blanking. When the Leading Zero Blanking INput is floating or at a positive level, this circuitry is enabled and the device will blank leading zeroes. When it is low, or the half-digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The Leading Zero Blanking OUTput is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked; this can only occur when the Leading Zero Blanking INput is at a positive level and the half-digit is not set.

For example, in an eight-decade counter with overflow using two ICM7224/ICM7225 devices, the Leading Zero Blanking OUTput of the high order digit would be connected to the Leading Zero Blanking INput of the low order digit device. This will assure correct leading zero blanking for all eight digits.

NOTE: All typical values have been characterized but are not tested.

The $\overline{\text{STORE}}$, $\overline{\text{RESET}}$, $\overline{\text{COUNT INHIBIT}}$, and Leading Zero Blanking INputs are provided with pullup devices, so that they may be left open when a positive level is desired. The $\overline{\text{CARRY}}$ and Leading Zero Blanking OUTputs are suitable for interfacing to CMOS logic in general, and are specifically designed to allow cascading of ICM7224 to ICM7225 devices in four-digit blocks.

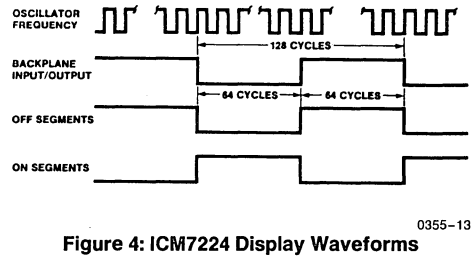


Figure 4: ICM7224 Display Waveforms

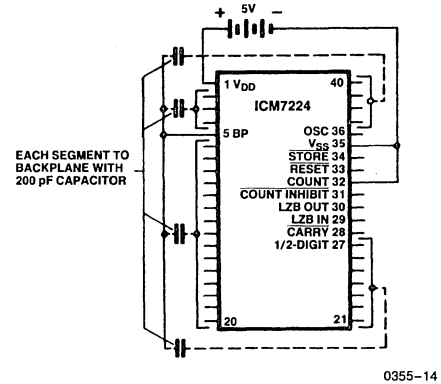


Figure 5: Test Circuit

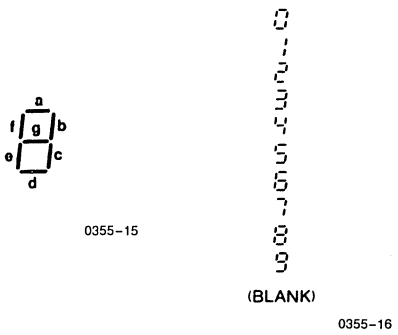


Figure 6: Segment Assignment and Display Font

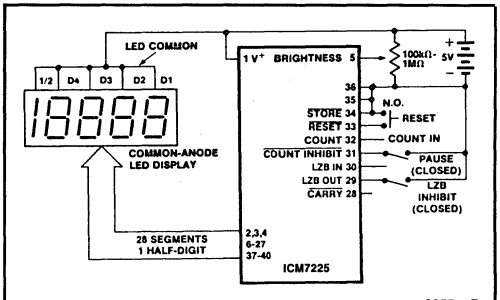


Figure 7: Typical Application (Unit Counter)

APPLICATIONS

Figures 7 and 8 show two typical applications for ICM7224/25 devices.

In Figure 7 an ICM7225, LED display and a few passive components form a unit counter. The device counts and totals the input pulses. Since the $\overline{\text{STORE}}$ input is tied to V_{SS} the display simultaneously updates the counts. The circuit has switches for pause operation, leading zero blanking control, and a pushbutton for resetting the counter.

Figure 8 shows an 8-digit precision frequency counter. The circuit uses two ICM7224s cascaded to provide an 8-digit display. Backplane output of the second device is disabled and is driven by the first device. The ½ digit output of the second device is used for overflow indication. The input signal is fed to the first device and the COUNT input of the second is driven by the $\overline{\text{CARRY}}$ output of the first. Notice that leading zero blanking is controlled on the second device and the LZB OUT of the second one is tied to LZB IN of the first one. An ICM7207A device is used as a timebase generator and frequency counter controller. It generates count window, store and reset signals which are directly compatible with ICM7224 inputs (notice the need for an inverter at $\overline{\text{COUNT INHIBIT}}$ input). The ICM7207A provides two count window signals (1s and 0.1s gating) for displaying frequencies in Hz or tens of Hz (×10 Hz).

NOTE: All typical values have been characterized but are not tested.

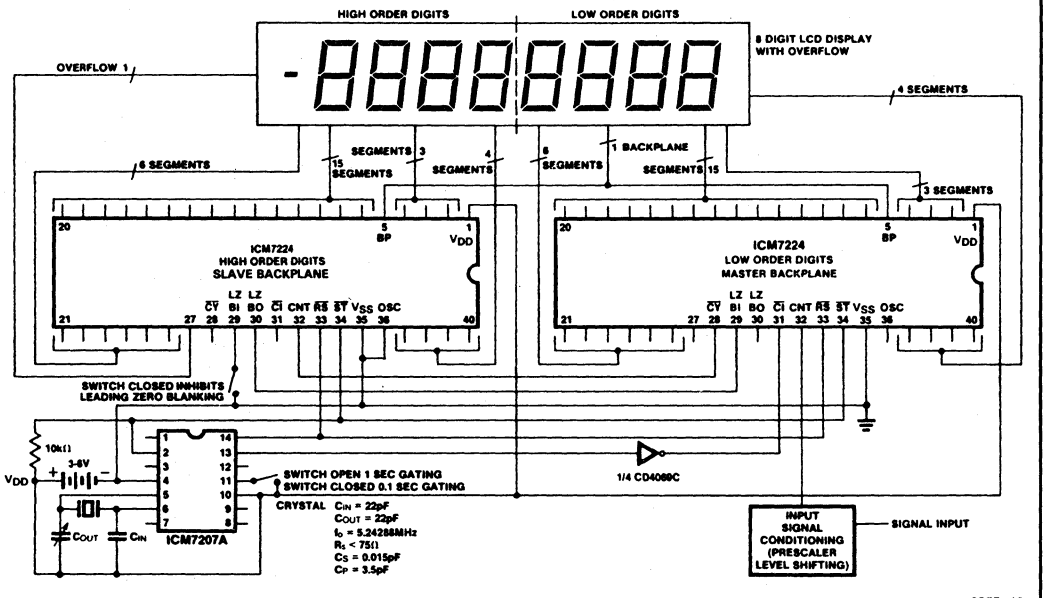


Figure 8: Eight-Digit Precision Frequency Counter

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICM7226A/B
8-Digit Multi-Function Frequency Counter/Timer

GENERAL DESCRIPTION

The ICM7226 is a fully integrated Universal Counter and LED display driver. It combines a high frequency oscillator, a decade timebase counter, an 8 decade data counter and latches, a 7 segment decoder, digit multiplexer, and segment and digit drivers which can directly drive large LED displays. The counter inputs accept a maximum frequency of 10 MHz in **frequency** and **unit counter** modes and 2 MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7226 can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or a totalizing counter. The devices require either a 10 MHz or 1 MHz crystal timebase, or if desired an external timebase can also be used. For **period** and **time interval,** the 10 MHz timebase gives a 0.1μs resolution. In **period average** and **time interval average,** the resolution can be in the nanosecond range. In the **frequency** mode, the user can select accumulation time of 10ms, 100ms, 1s and 10s. With a 10s accumulation time, the frequency can be displayed to a resolution of 0.1 Hz. There is a 0.2s interval between measurements in all ranges. Control signals are provided to enable gating and storing of prescaler data.

Leading zero blanking has been incorporated with frequency display in kHz and time in μs. The display is multiplexed at a 500 Hz rate with a 12.2% duty cycle for each digit. The ICM7226A is designed for common anode displays with typical peak segment currents of 25 mA, and the ICM7226B is designed for common cathode displays with typical segment currents of 12 mA. In the **display off** mode, both digit drivers & segment drivers are turned off, allowing the display to be used for other functions.

FEATURES

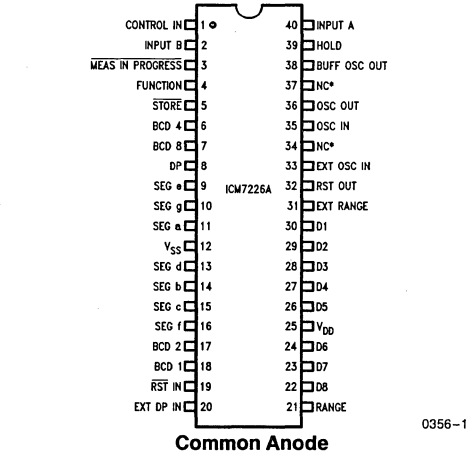
- **CMOS Design for Very Low Power**
- **Output Drivers Directly Drive Both Digits and Segments of Large 8 Digit LED Displays. Both Common Anode and Common Cathode Versions Are Available**
- **Measures Frequencies From DC to 10 MHz; Periods From 0.5μs to 10s**
- **Stable High Frequency Oscillator Uses Either 1 MHz or 10 MHz Crystal**
- **Control Signals Available for External Systems Interfacing**
- **Multiplexed BCD Outputs**

APPLICATIONS

- **Frequency Counter**
- **Period Counter**
- **Unit Counter**
- **Frequency Ratio Counter**
- **Time Interval Counter**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7226AIJL	−25°C to 85°C	40 pin CERDIP
ICM7226BIPL	−25°C to 85°C	40 pin PLASTIC DIP



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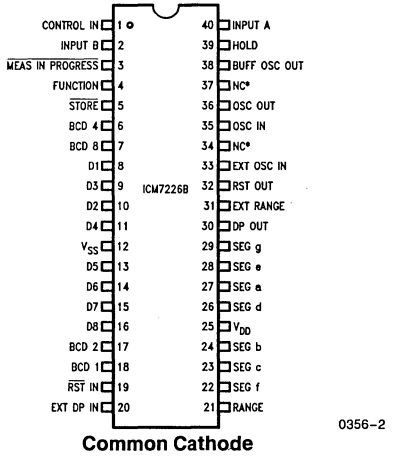
Common Anode



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Common Cathode

*For maximum frequency stability, connect to V_{DD} or V_{SS}

Figure 1: Pin Configurations

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage ($V_{DD}-V_{SS}$) 6.5V
Maximum Digit Output Current ..... 400 mA
Maximum Segment Output Current ..... 60 mA
Voltage on any Input or Output Terminal (Note 1) .....
($V_{SS}-0.3V$) to ($V_{DD}+0.3V$)
Maximum Power Dissipation at 70°C (Note 2)
ICM7226A 1.0W
ICM7226B 0.5W
Operating Temperature Range ..... −25°C to +85°C
Storage Temperature Range ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Note 1: Destructive latchup may occur if input signals are applied before the power supply is established or if inputs or outputs are forced to voltages exceeding V_{DD} or V_{SS} by 0.3V.
2: Assumes all leads soldered or welded to PC board and free air flow.

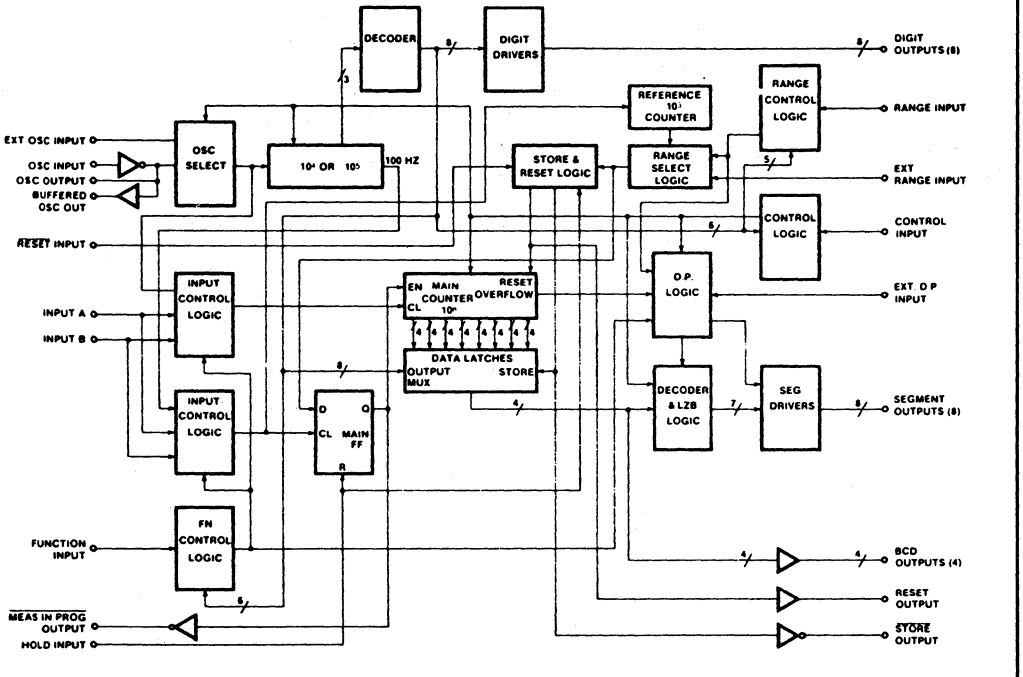


Figure 2: Functional Diagram

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V, T_A = 25°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{DD}	Operating Supply Current	Display Off Unused inputs to V_{SS}		2	5	mA
V_{SUPPLY}	Supply Voltage Range $V_{DD}-V_{SS}$	$-25°C<T_A<85°C$ Input A, Input B Frequency at f_{MAX}	4.75		6.0	V
$f_{A(max)}$	Maximum Guaranteed Frequency Input A, Pin 40	$-25°C<T_A<85°C$ $4.75V<V_{DD}<6.0V$ Figure 3 Function = Frequency, Ratio, Unit Counter Function = Period, Time Interval	 10 2.5	 14		MHz
$f_{B(max)}$	Maximum Frequency Input B, Pin 2	$-25°C<T_A<85°C$ $4.75V<V_{DD}<6.0V$ Figure 4	2.5			
	Minimum Separation Input A to Input B Time Interval Function	$-25°C<T_A<85°C$ $4.75V<V_{DD}<6.0V$ Figure 11	250			ns
f_{OSC}	Osc. freq. and ext. osc. freq. (minimum ext. osc. freq.)	$-25°C<T_A<85°C$ $4.75V<V_{DD}<6.0V$	10 (0.1)			MHz
g_m	Oscillator Transconductance	V_{DD} = 4.75V T_A = +85°C	2000			μS
f_{mux}	Multiplex Frequency	f_{osc} = 10 MHz		500		Hz
	Time Between Measurements	f_{osc} = 10 MHz		200		ms
dV_{in}/dt	Input Rate of Charge	Inputs A, B		15		mV/μs
V_{IL}	INPUT VOLTAGES PINS 2, 19, 33, 39, 40, 35 input low voltage	$-25°C<T_A<+85°C$			1.0	V
V_{IH}	input high voltage		3.5			
I_{ILK}	PIN 2, 39, 40 INPUT LEAKAGE, A, B				20	μA
R_{IN}	Input resistance to V_{DD} PINS 19,33	$V_{IN}=V_{DD}-1.0V$	100	400		kΩ
R_{IN}	Input resistance to V_{SS} PIN 31	$V_{IN}=+1.0V$	50	100		
I_{OL}	Output Current PINS 3,5,6,7,17,18,32,38	$V_{OL}=+0.4V$	400			μA
I_{OH}	PINS 5,6,7,17,18,32	$V_{OH}=+2.4V$	100			μA
I_{OH}	PINS 3,38	$V_{OH}=V_{DD}-0.8V$	265			
I_{OH}	**ICM7226A** PINS 22,23,24,26,27,28,29,30 DIGIT DRIVER high output current	$V_O=V_{DD}-2.0V$	150	180		mA
I_{OL}	low output current	$V_O=+1.0V$		−0.3		
I_{OL}	SEGMENT DRIVER PINS 8,9,10,11,13,14,15,16 low output current	$V_O=+1.5V$	25	35		mA
I_{OH}	high output current	$V_O=V_{DD}-1.0V$		100		μA

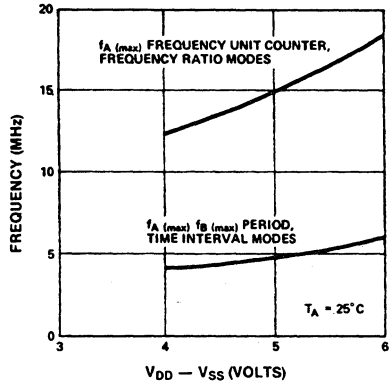
NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V, T_A = 25°C, unless otherwise specified.) (Continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
	MULTIPLEX INPUTS PINS 1,4,20,21					
V_{IL}	input low voltage				0.8	V
V_{IH}	input high voltage		2.0			
R_{IN}	input resistance to V_{SS}	V_{IN} = +1.0V	50	100		kΩ
	ICM7226B DIGIT DRIVER PINS 8,9,10,11,13,14,15,16					
I_{OL}	low output current	V_O = +1.0V	50	75		mA
I_{OH}	high output current	$V_O = V_{DD} - 2.5V$		100		μA
	SEGMENT DRIVER PINS 22,23,24,26,27,28,29,30					
I_{OH}	high output current	$V_O = V_{DD} - 2.0V$	10	15		mA
I_L	leakage current	$V_O = V_{SS}$			10	μA
	MULTIPLEX INPUTS PINS 1,4,20,21					
V_{IL}	input low voltage				$V_{DD} - 2.0$	V
V_{IH}	input high voltage		$V_{DD} - 0.8$			
R_{IN}	input resistance to V_{DD}	$V_{IN} = V_{DD} - 1.0V$	100	360		kΩ

NOTE: Typical values are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS



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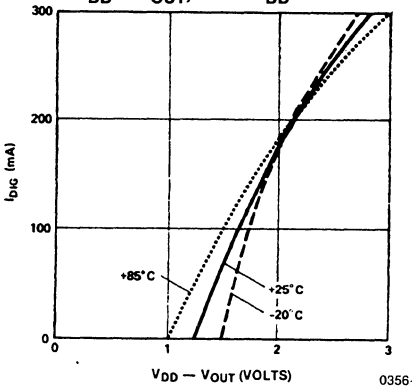
f_A(max), f_B(max) as a Function of Supply Voltage

NOTE: All typical values have been characterized but are not tested.

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

ICM7226A Typical I_{DIG} vs $V_{DD} - V_{OUT}$, $4.5 \le V_{DD} \le 6.0V$



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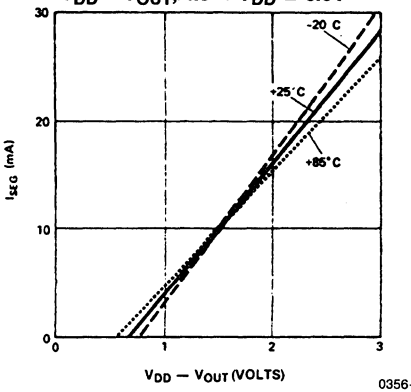
ICM7226B Typical I_{SEG} vs $V_{DD} - V_{OUT}$, $4.5 \le V_{DD} \le 6.0V$



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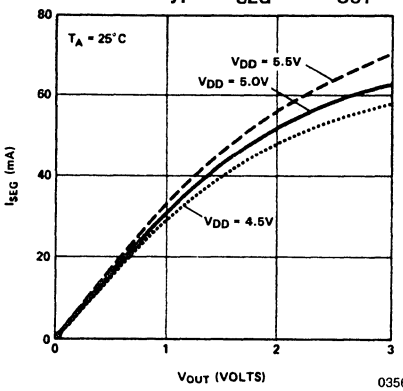
ICM7226A Typical I_{SEG} vs $-V_{OUT}$



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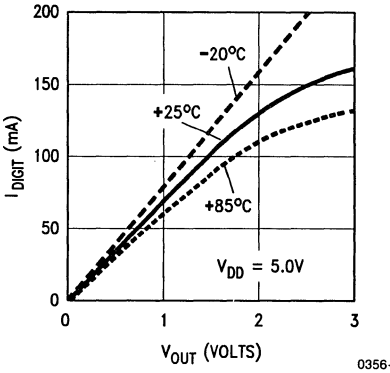
ICM7226B Typical I_{DIGIT} vs $-V_{OUT}$



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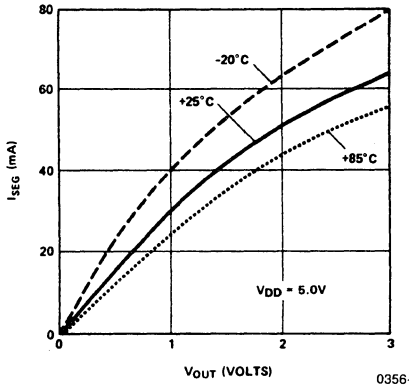

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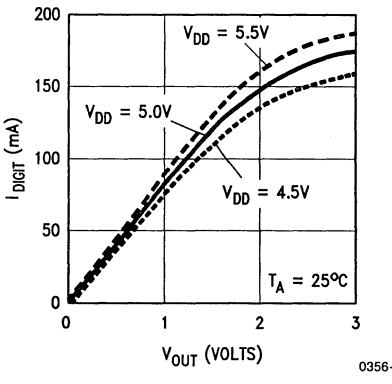

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NOTE: All typical values have been characterized but are not tested.

ICM7226A/B

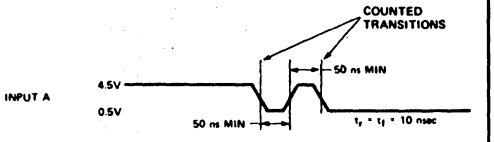

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Figure 3: Waveform for Guaranteed Minimum f_A(max) Function = Frequency, Frequency Ratio, Unit Counter

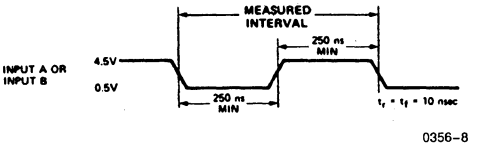

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Figure 4: Waveform for Guaranteed Minimum f_B(max) and f_A(max) for Function = Period and Time Interval

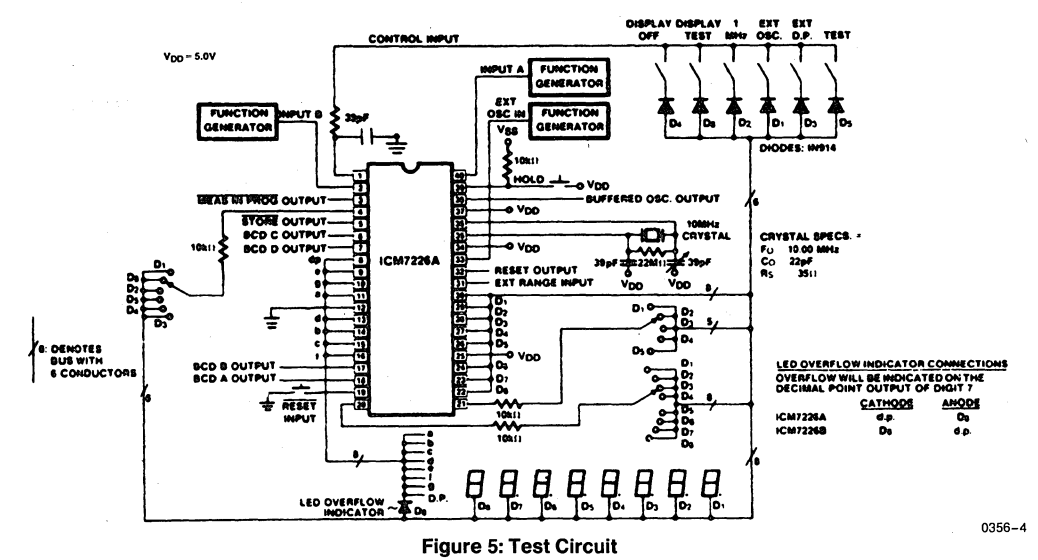

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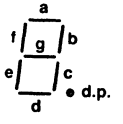
Figure 5: Test Circuit



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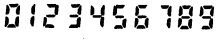

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LED overflow indicator connections:
Overflow will be indicated on the decimal point output of digit 8.

	CATHODE	ANODE
ICM7226A	d.p.	D_8
ICM7226B	D_8	d.p.

Figure 6: Segment Identification and Display Font

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

INPUTS A & B

The signal to be measured is applied to INPUT A in **frequency period, unit counter, frequency ratio** and **time interval** modes. The other input signal to be measured is applied to INPUT B in **frequency ratio** and **time interval.** f_A should be higher than f_B during **frequency ratio**.

Both inputs are digital inputs with a typical switching threshold of 2.0V at $V_{DD}=5.0V$ and input impedance of 250 kΩ. For optimum performance, the peak to peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from TTL logic, it is desirable to use a pull-up resistor. The circuit counts high to low transitions at both inputs.

Note that the amplitude of the input should not exceed the device supply (above the V_{DD} and below the V_{SS}) by more than 0.3V, otherwise the device may be damaged.

MULTIPLEXED INPUTS

The FUNCTION, RANGE, CONTROL and EXTERNAL DECIMAL POINT inputs are time multiplexed to select the function desired. This is achieved by connecting the appropriate digit driver output to the inputs. The function, range and control inputs must be stable during the last half of each digit output, (typically 125μs). The multiplex inputs are active high for the common anode ICM7226A, and active low for the common cathode ICM7226B.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the **unit counter** mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10 kΩ resistor should be placed in series with the multiplex inputs as shown in the application notes.

Table 1 shows the functions selected by each digit for these inputs.

Table 1: Multiple Input Control

	Function	Digit
FUNCTION INPUT PIN 4	Frequency	D_1
	Period	D_8
	Frequency Ratio	D_2
	Time Interval	D_5
	Unit Counter	D_4
	Oscillator Frequency	D_3
RANGE INPUT PIN 21	0.01 Sec/1 Cycle	D_1
	0.1 Sec/10 Cycles	D_2
	1 Sec/100 Cycles	D_3
	10 Sec/1k Cycles	D_4
	Enable External Range Input	D_5
CONTROL INPUT PIN 1	Display Off	D_4 & Hold
	Display Test	D_8
	1 MHz Select	D_2
	External Oscillator Enable	D_1
	External Decimal Point Enable	D_3
EXTERNAL DECIMAL POINT INPUT, PIN 20	Decimal Point is Output for Same Digit That is Connected to This Input	

FUNCTION INPUT

The ICM7226 has six modes of operation to be selected by FUNCTION input. These are: Frequency, Period, Frequency Ratio, Time Interval, Unit Counter and Oscillator Frequency.

The implementation of different functions is done by routing the different signals to two counters, called "Main Counter" and "Reference Counter". A simplified block diagram of the device for functions realization is shown in Figure 7. Table 2 shows which signals will be routed to each counter in different cases. The output of the Main Counter is the information which goes to the display. The Reference Counter divides its input to 1, 10, 100 and 1000. One of these outputs will be selected through the range selector and drive the enable input of the Main Counter. This means that the Reference Counter, along with its' associated blocks, directs the Main Counter to begin counting and determines the length of the counting period. Note that Figure 7 does not show the complete functional diagram (See Figure 1). After the end of each counting period, the output of the Main Counter will be latched and displayed, then the counter will be reset and a new measurement cycle will begin. Any change in the FUNCTION INPUT will stop the present measurement without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION INPUT is changed. In all cases, the 1 → 0 transitions are counted or timed.

Table 2: Input Routing

Function	Main Counter	Reference Counter
Frequency (f_A)	Input A	100 Hz (Oscillator ÷ 10^5 or 10^4)
Period (t_A)	Oscillator	Input A
Ratio (f_A/f_B)	Input A	Input B
Time Interval (A → B)	Oscillator	Input A Input B
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq. (f_{osc})	Oscillator	100 Hz (Oscillator ÷ 10^5 or 10^4)

Frequency—In this mode input A is counted by the Main Counter for a precise period of time. This time is determined by the time base oscillator and the selected range. For the 10 MHz (or 1 MHz) timebase, the resolutions are 100, 10, 1 and 0.1 Hz. The decimal point on the display is set for kHz reading.

NOTE: All typical values have been characterized but are not tested.

ICM7226A/B

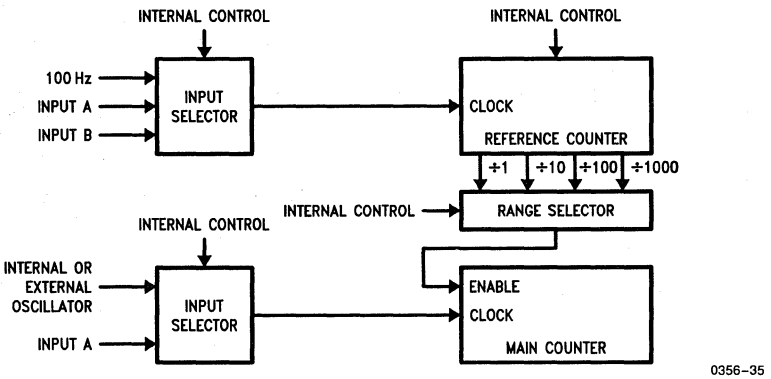


Figure 7: Simplified Block Diagram of Functions Implementation

Period—In this mode the timebase oscillator is counted by the Main counter for the duration of 1, 10, 100 or 1000 (range selected) periods of the signal at input A. A 10 MHz timebase gives resolutions of 0.1μs to 0.0001μs for 1000 periods averaging. Note that the maximum input frequency for period measurement is 2.5 MHz.

Frequency Ratio—In this mode the input A is counted by the Main Counter for the duration of 1, 10, 100 or 1000 (range selected) periods of the signal at input B. The frequency at input A should be higher than input B for meaningful result. The result in this case is unitless and its resolutions can go up to 3 digits after decimal point.

Time Interval—In this mode, the timebase oscillator is counted by the Main Counter for the duration of a 1 $\rightarrow$ 0 transition of input A until a 1 $\rightarrow$ 0 transition of input B. This means input A starts the counting and input B stops it. If other ranges, except 0.01 s/1 cycle are selected the sequence of input A and B transitions must happen 10, 100 or 1000 times until the display becomes updated; note this when measuring long time intervals to give enough time for measurement completion. The resolution in this mode is the same as for period measurement. See the Time Interval Measurement section also.

Unit Counter—In this mode the Main Counter is always enabled, the input A is counted by the Main Counter and displayed continuously.

Oscillator Frequency—In this mode the device makes a frequency measurement on its timebase. This is a self test mode for device functionality check. For 10 MHz timebase the display will show 10000.0, 10000.00, 10000.000 and Overflow in different ranges.

RANGE Input

The RANGE input selects whether the measurement period is made for 1, 10, 100 or 1000 counts of the Reference Counter or it is controlled by EXT RANGE input. As it is shown in Table 1, this gives different counting windows for frequency measurement and various cycles for other modes of measurement.

In all functional modes except Unit Counter any change in the RANGE INPUT will stop the present measurement without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the RANGE INPUT is changed.

CONTROL Input

Unlike the other multiplexed inputs, to which only one of the digit outputs can be connected at a time, this input can be tied to different digit lines to select combination of controls. In this case, isolation diodes must be used in digit lines to avoid crosstalk between them (see Figure 5). The direction of diodes depends on the device version, common anode or common cathode. For maximum noise immunity at this input, in addition to the 10k resistor which was mentioned before, a 39 pF to 100 pF capacitor should also be placed between this input and the V_{DD} or V_{SS} (See Figure 5).

Display Off—To disable the display drivers, it is necessary to tie the D4 line to the CONTROL INPUT and have the HOLD input at V_{DD}. While in Display Off mode, the segments and digit drivers are all off, leaving the display lines floating, so the display can be shared with other devices. In this mode, the oscillator continues to run with a typical supply current of 1.5 mA with a 10 MHz crystal, but no measurements are made and multiplexed inputs are inactive. A new measurement cycle will be initiated when the HOLD input is switched to V_{SS}.

Display Test —Display will turn on with all the digits showing 8s and all decimal points also on. The display will be blanked if Display Off is selected at the same time.

1 MHz Select—The 1 MHz select mode allows use of a 1 MHz crystal with the same digit multiplex rate and time between measurements as with a 10 MHz crystal. This is done by dividing the oscillator frequency by 10^4 rather than 10^5. The decimal point is also shifted one digit to the right in period and time interval, since the least significant digit will be in μs increment rather than 0.1μs increment.

NOTE: All typical values have been characterized but are not tested.

External Oscillator Enable—In this mode, the signal at EXT OSC INPUT is used as a timebase instead of the on-board crystal oscillator (built around the OSC INPUT, OSC OUTPUT inputs). This input can be used for an external stable temperature compensated crystal oscillator or for special measurements with any external source. The on-board crystal oscillator continues to work when the external oscillator is selected. This is necessary to avoid hang-up problems, and has no effect on the chip's functional operation. If the on-board oscillator frequency is less than 1 MHz or only the external oscillator is used, THE OSC INPUT MUST BE CONNECTED TO THE EXT OSC INPUT providing the timebase has enough voltage swing for OSC INPUT (See electrical characteristics). If the external timebase is TTL level a pullup resistor must be used for OSC INPUT. The other way is to put a 22 MΩ resistor between OSC INPUT and OSC OUTPUT and capacitively couple the EXT OSC INPUT to OSC INPUT. This will bias the OSC INPUT at its threshold and the drive voltage will need to be only 2 V_{p-p}. The external timebase frequency must be greater than 100 kHz or the chip will reset itself to enable the on-board oscillator.

External Decimal Point Enable—In this mode the EX D.P. INPUT is enabled. A decimal point will be displayed for the digit that its output line is connected to this input (EX D.P. INPUT). Digit 8 should not be used since it will override the overflow output. Leading zero blanking is effective for the digits to the left of selected decimal point.

HOLD Input

Except in the **unit counter** mode, when the HOLD input is at V_{DD}, any measurement in progress (before $\overline{\text{STORE}}$ goes low) is stopped, the main counter is reset and the chip is held ready to initiate a new measurement as soon as HOLD goes low. The latches which hold the main counter data are not updated, so the last complete measurement is displayed. In **unit counter** mode when HOLD input is at V_{DD}, the counter is not stopped or reset, but the display is frozen at that instantaneous value. When HOLD goes low the count continues from the new value in the counter.

$\overline{\text{RST}}$ IN Input

The RST IN is provided to reset the Main Counter, stop any measurement in progress, and enable the display latches, resulting in the all zero display. It is suggested to have a capacitor at this input to V_{SS} to prevent any hang-up problem on power up. See application circuits.

EXT RANGE Input

This input is provided to select ranges other than those provided in the chip. In any mode of measurement the duration of measurement is determined by the EXT RANGE if this input is enabled. This input is sampled at 10ms intervals by the 100 Hz reference derived from the timebase. Figure 8 shows the relationship between this input, 100 Hz reference signal and MEAS IN PROGRESS. EXT RANGE can change state anywhere during the period of 100 Hz reference but will be sampled at the trailing edge of the period to start or stop measurement.

This input should not be used for short arbitrary ranges (because of its sampling period), it is provided for very long gating purposes. A way of using the 7226 for a short arbitrary range is to feed the gating signal into the INPUT B and run the device in the Frequency Ratio mode. Note that the gating period will be from one positive edge until the next positie edge of INPUT B (0.01 s/1 cycle range).

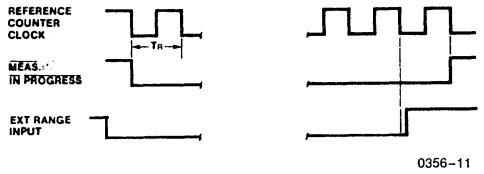


Figure 8: External Range Input to End of $\overline{\text{MEASUREMENT IN PROGRESS}}$

$\overline{\text{MEAS IN PROGRESS}}$, $\overline{\text{STORE}}$, RST OUT Outputs

These outputs are provided for external system interfacing. MEAS IN PROGRESS stays low during measurements and goes high for intervals between measurements. Figure 9 shows the relationship between these outputs for intervals between measurements. All these outputs can drive a low power Schottky TTL. The MEAS IN PROGRESS can drive one ECL load if the ECL device is powered from the same power supply as the ICM7226.

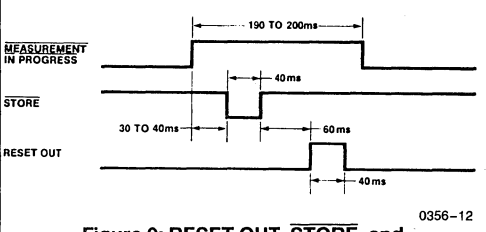


Figure 9: RESET OUT, $\overline{\text{STORE}}$, and $\overline{\text{MEASUREMENT IN PROGRESS}}$ Outputs between Measurements

BCD Outputs

The BCD representation of each display digit is available at the BCD outputs in a multiplexed fashion. See Table 3 for digits truth table. The BCD output of each digit is available when its corresponding digit output is activated. Note that the digit outputs are multiplexed from D8 (MSD) to D1 (LSD). The positive going (ICM7226A, common anode) or the negative going (ICM7226B, common cathode) digit drive signals lag the BCD data by 2μs to 6μs. This starting edge of each digit drive signal should be used to externally latch the BCD data. Each BCD output drives one low power Schottky TTL load. Leading zero blanking has no effect on the BCD outputs.

NOTE: All typical values have been characterized but are not tested.

Table 3: Truth Table BCD Outputs

Number	BCD 8 Pin 7	BCD 4 Pin 6	BCD 2 Pin 17	BCD 1 Pin 18
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

BUFF OSC OUT Output

The BUFFered OSCillator OUTput is provided for use of the on-board oscillator signal, without loading the oscillator itself. This output can drive one low power Schottky TTL load. Care should be taken to minimize capacitive loading on this pin.

Decimal Point Position

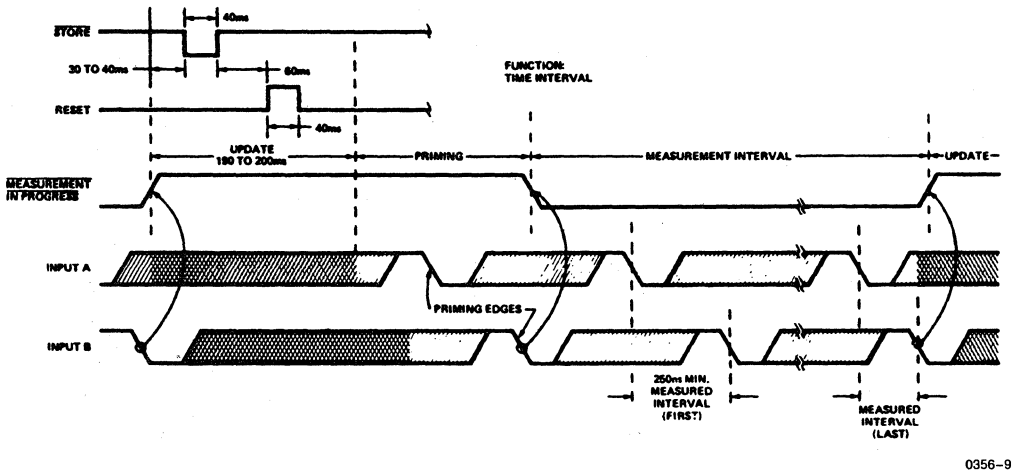
Table 4 shows the decimal point position for different modes of ICM7216 operation. Note that the digit 1 is the least significant digit. Table is given for 10 MHz timebase frequency.

Overflow Indication

When overflow happens in any measurement it will be indicated on the decimal point of the digit 8. A separate LED indicator can be used. Figure 6 shows how to connect this indicator.

Table 4: Decimal Point Position

Range	Frequency	Period	Frequency Ratio	Time Interval	Unit Counter	Oscillator Frequency
0.01 s/1 Cycle	D2	D2	D1	D2	D1	D2
0.1 s/10 Cycle	D3	D3	D2	D3	D1	D3
1 s/100 Cycle	D4	D4	D3	D4	D1	D4
10 s/1k Cycle	D5	D5	D4	D5	D1	D5
External	N/A	N/A	N/A	N/A	N/A	N/A



Note: If range is set to 1 event, first and last measured interval will coincide.

Figure 11: Waveforms for Time Interval Measurement (Others are similar, without priming phase)

NOTE: All typical values have been characterized but are not tested.

Time Interval Measurement

When in the time interval mode and measuring a single event, the ICM7226A/B must first be "primed" prior to measuring the event of interest. This is done by first generating a negative going edge on Channel A followed by a negative going edge on Channel B to start the "measurement interval." The inputs are then primed ready for the measurement. Positive going edges on A and B, before or after the priming, will be needed to restore the original condition.

Priming can be easily accomplished using the circuit in Figure 10.

Following the priming procedure (when in single event or 1 cycle range input) the device is ready to measure one (only) event.

When timing repetitive signals, it is not necessary to "prime" the ICM7226A/B as the first alternating signal states automatically prime the device. See Figure 11.

During any time interval measurement cycle, the ICM7226A/B requires 200ms following B going low to update all internal logic. A new measurement cycle will not take place until completion of this internal update time.

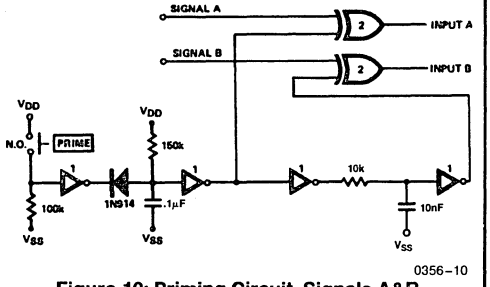


Figure 10: Priming Circuit, Signals A&B Both High or Low

Device	Type
1	CD4049B Inverting Buffer
2	CD4070B Exclusive-OR

Oscillator Consideration

The oscillator is a high gain complementary FET inverter. An external resistor of 10 MΩ or 22 MΩ should be connected between the oscillator input and output to provide biasing. The oscillator is designed to work with a parallel resonant 10 MHz quartz crystal with a load capacitance of 22 pF and a series resistance of less than 35Ω. Among suitable crystals is the 10 MHz CTS KNIGHTS ISI-002.

For a specific crystal and load capacitance, the required g_m can be calculated as follows:

$$g_m = \omega^2 C_{IN} C_{OUT} Rs \left(1 + \frac{C_O}{C_L}\right)^2$$

where $C_L = \left(\frac{C_{IN}C_{OUT}}{C_{IN}+C_{OUT}}\right)$

C_O = Crystal Static Capacitance

R_S = Crystal Series Resistance

C_{IN} = Input Capacitance

C_{OUT} = Output Capacitance

$\omega = 2\pi f$

The required g_m should not exceed 50% of the g_m specified for the ICM7226 to insure reliable startup. The oscillator input and output pins each contribute about 4 pF to C_{IN} and C_{OUT}. For maximum frequency stability, C_{IN} and C_{OUT} should be approximately twice the specified crystal load capacitance.

In cases where nondecade prescalers are used, it may be desirable to use a crystal which is neither 10 MHz nor 1 MHz. In this case both the multiplex rate and the time between measurements will be different. The multiplex rate is $f_{mux} = \frac{f_{osc}}{2\times10^4}$ for 10 MHz mode and $f_{mux} = \frac{f_{osc}}{2\times10^3}$ for the 1 MHz mode. The time between measurements is $\frac{2\times10^6}{f_{osc}}$ in the 10 MHz mode and $\frac{2\times10^5}{f_{osc}}$ in the 1 MHz mode. The buffered oscillator output should be used as an oscillator test point or to drive additional logic; this output will drive one low power Schottky TTL load. When the buffered oscillator output is used to drive CMOS or the external oscillator input, a 10 kΩ resistor should be added from the buffered oscillator output to V_{DD}.

The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. In particular, coupling from the BUFFered OSCillator OUTput and EXTernal OSCillator INput to the OSCillator OUTput or OSCillator INput can cause undesirable shifts in oscillator frequency. To minimize this coupling, pins 34 and 37 should be connected to V_{DD} or V_{SS} and these two signals should be kept away from the oscillator circuit.

Display Considerations

The display is multiplexed at a 500Hz rate with a digit time of 244μs. An interdigit blanking time of 6μs is used to prevent display ghosting (faint display of data from previous digit superimposed on the next digit). Leading zero blanking is provided, which blanks the left hand zeros after decimal point or any non-zero digits. Digits to the right of the decimal point are always displayed. The leading zero blanking will be disabled when the Main Counter overflows.

The ICM7226A is designed to drive common anode LED displays at a peak current of 25 mA/segment, using displays with $V_F = 1.8V$ at 25 mA. The average DC current will

11

NOTE: All typical values have been characterized but are not tested.

be greater than 3 mA under these conditions. The ICM7226B is designed to drive common cathode displays at a peak current of 15 mA/segment, using displays with $V_F = 1.8V$ at 15 mA. Resistors can be added in series with the segment drivers to limit the display current, if required. The Typical Performance Characteristics curves show the digit and segment currents as a function of output voltage for common anode and common cathode drivers.

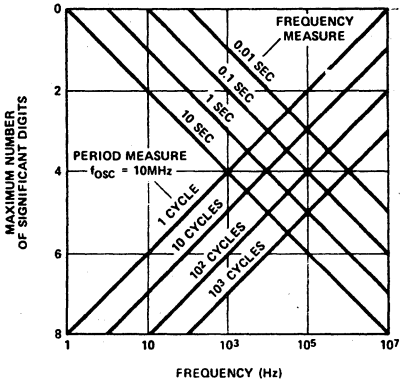
To increase the light output from the displays, V_{DD} may be increased to 6.0V, however care should be taken to see that maximum power and current ratings are not exceeded.

The SEGment and Digit outputs in both the 7226A and B are not directly compatible with either TTL or CMOS logic. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals. External latching should be done on the leading edge of the digit signal.

ACCURACY

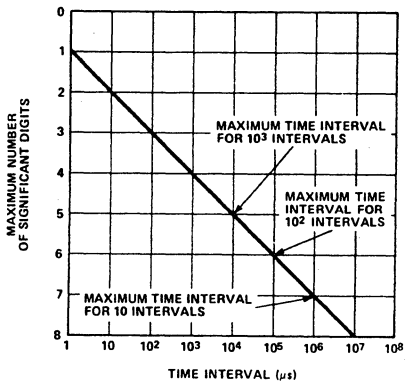
In a Universal Counter, crystal drift and quantization errors cause errors. In **frequency, period** and **time interval** modes, a signal derived from the oscillator is used either in the Reference Counter or Main Counter, and in these modes, an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of 20ppm/°C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the **frequency** mode, maximum accuracy is obtained with high frequency inputs, and in **period** mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 12. In **time interval** measurements there is a maximum error of 1 count per interval. As a result there is the same inherent accuracy in all ranges, as shown in Figure 13. In **frequency ratio** measurement more accuracy can be obtained by averaging over more cycles of INPUT B as shown in Figure 14.



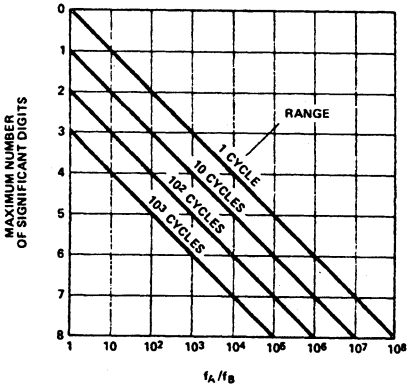
0356-36

Figure 12: Maximum Accuracy of Frequency and Period Measurements Due to Limitations of Quantization Errors



0356-38

Figure 13: Maximum Accuracy of Time Interval Measurements Due to Limitations of Quantization Errors



0356-37

Figure 14: Maximum Accuracy of Frequency Ratio Measurement Due to Limitation of Quantization Errors

APPLICATIONS

The ICM7226 has been designed as a complete stand alone Universal Counter, or used with prescalers and other circuitry in a variety of applications. Since INPUT A and INPUT B are digital inputs, additional circuitry will be required in many applications, for input buffering, amplification, hysteresis, and level shifting to obtain the required digital voltages. For many applications a FET source follower can be used for input buffering, and an ECL 10116 line receiver can be used for amplification and hysteresis to obtain high impedance input, sensitivity and bandwidth. However, cost and complexity of this circuitry can vary widely, depending

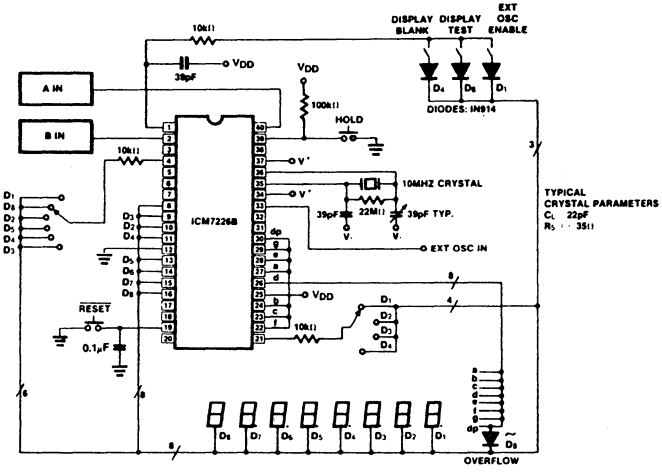
NOTE: All typical values have been characterized but are not tested.

upon the sensitivity and bandwidth required. When TTL prescalers or input buffers are used, a pull up resistors to V_{DD} should be used to obtain optimal voltage swing at INPUTS A and B.

If prescalers aren't required, the ICM7226 can be used to implement a minimum component Universal Counter as shown in Figure 15.

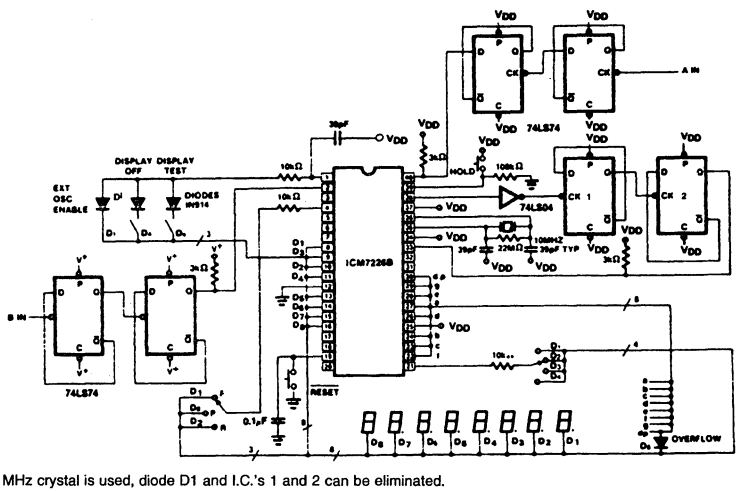
For input frequencies up to 40 MHz, the circuit shown in Figure 16 can be used to implement a **frequency and period counter.** To obtain the correct value when measuring frequency and period, it is necessary to divide the 10 MHz oscillator frequency down to 2.5 MHz. In doing this the time between measurements is lengthened to 800ms and the display multiplex rate is decreased to 125 Hz.

If the input frequency is prescaled by ten, the oscillator frequency can remain at either 10 MHz or 1 MHz, but the decimal point must be moved. Figure 17 shows use of a ÷ 10 prescaler in **frequency counter** mode. Additional logic has been added to enable the 7226 to count the input directly in **period** mode for maximum accuracy.



0356-20

Figure 15: 10 MHz Universal Counter



0356-21

Note 1: If a 2.5 MHz crystal is used, diode D1 and I.C.'s 1 and 2 can be eliminated.

Figure 16: 40 MHz Frequency, Period Counter

NOTE: All typical values have been characterized but are not tested.

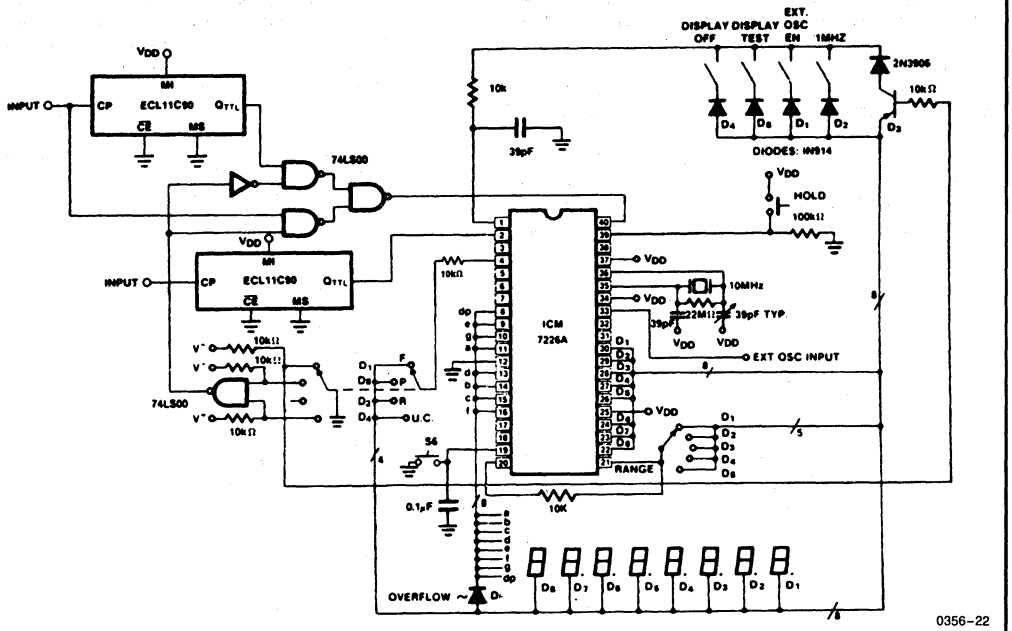


Figure 17: 100 MHz Multi Function Counter

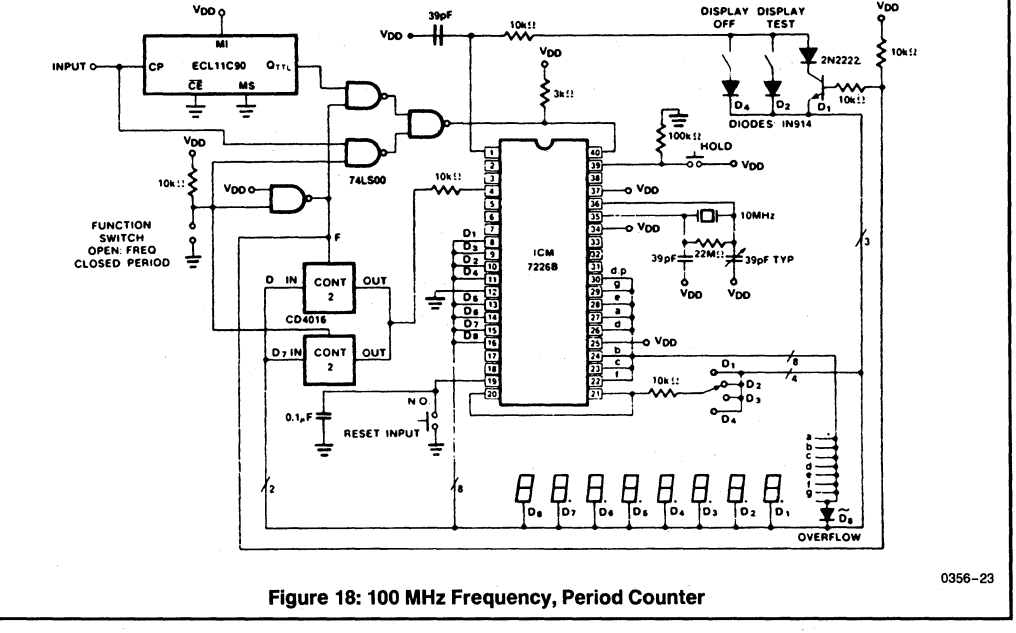
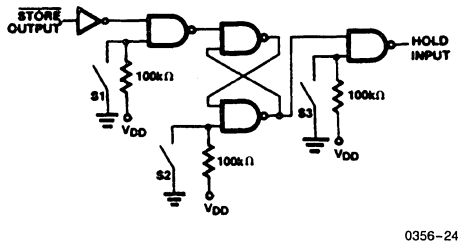


Figure 18: 100 MHz Frequency, Period Counter

NOTE: All typical values have been characterized but are not tested.

Figure 18 shows the use of a CD4016 analog multiplexer to multiplex the digital outputs back to the FUNCTION Input. Since the CD4016 is a digitally controlled analog transmission gate, no level shifting of the digit output is required. CD4051's or CD4052's could also be used to select the proper inputs for the multiplexed input on the ICM7226 from 2 or 3 bit digital inputs. These analog multiplexers may also be used in systems in which the mode of operation is controlled by a microprocessor rather than directly from front panel switches. TTL multiplexers such as the 74LS153 or 74LS251 may also be used, but some additional circuitry will be required to convert the digit output to TTL compatible logic levels.

The circuit shown in Figure 19 can be used in any of the circuit applications shown to implement a single measurement mode of operation. This circuit uses the $\overline{\text{STORE}}$ output to put the ICM7226 into a hold mode. The HOLD input can also be used to reduce the time between measurements. The circuit shown in Figure 20 puts a short pulse into the HOLD input a short time after STORE goes low. A new measurement will be initiated at the end of the pulse on the HOLD Input. This circuit reduces the time between measurements to about 40ms from 200ms; use of the circuit shown in Figure 20 on the circuit shown in Figure 16 will reduce the time between measurements from 800ms to about 160ms.



0356-24

Switch	Function
S1	OPEN-SINGLE MEAS MODE ENABLED
S2	CLOSED-INITIATE NEW MEASUREMENT
S3	CLOSED-HOLD INPUT

Figure 19: Single Measurement Circuit for Use with ICM7226

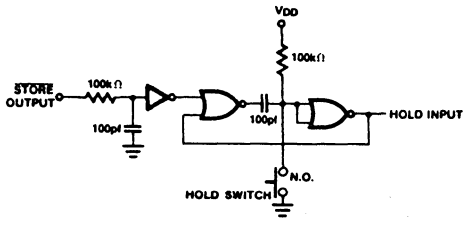


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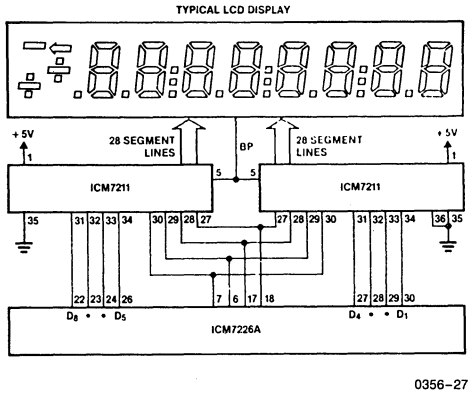
Figure 20: Circuit for Reducing Time between Measurements

Using LCD Display

Figure 21 shows the ICM7226 being interfaced to LCD displays, by using its BCD outputs and 8 digit lines to drive two ICM7211 display drivers.



0356-27

Figure 21: 10 MHz Universal Counter System with LCD Display

11

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICM7249
5½ Digit LCD μ-Power Event/Hour Meter

GENERAL DESCRIPTION

The ICM7249 Timer/Counter is intended for long-term battery-supported industrial applications. The ICM7249 typically draws 1μA during active timing or counting, due to Harris' special low-power design techniques. This allows more than 10 years of continuous operation without battery replacement. The chip offers four timing modes, eight counting modes and four test modes.

The ICM7249 is a 48-lead device, powered by a single DC voltage source and controlled by a 32.768kHz quartz crystal. No other external components are required. Inputs to the chip are TTL-compatible and outputs drive standard direct drive LCD segments. The chip is available in dice and in Plastic DIP package forms.

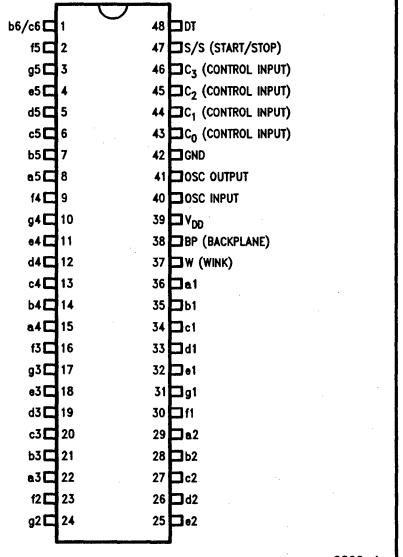


Figure 1: Pin Configuration

FEATURES

- **Hour Meter Requires Only 4 Parts Total**
- **Micropower Operation: <1μA at 2.8V Typical**
- **10 Year Operation On One Lithium Cell**
  2½ Year Battery Life With Display Connected
- **Directly drives 5½ Digit LCD**
- **14 Programmable Modes of Operation**
- **Times Hrs., 0.1 Hrs., .01 Hrs., .1 Mins.**
- **Counts 1's, 10's, 100's, 1000's**
- **Dual Funtion Input Circuit:**
  —Selectable Debounce for Counter
  —High-Pass Filter for Timer
- **Direct AC Line Triggering With Input Resistor**
- **Winking "Timer Active" Display Output**
- **Display Test Feature**

APPLICATIONS

- **AC or DC Hour Meters**
- **AC or DC Totalizers**
- **Portable Battery Powered Equipment**
- **Long Range Service Meters**

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICM7249IPM	−40°C to +85°C	48-Pin Plastic DIP

203500-005

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6V
Input Voltage
Pins 43-48 (Note 1) ..... (V_{SS} −0.3V) to (V_{DD} +0.3V)
Power Dissipation (Note 2) 200mW
Operating Temperature Range ..... −40°C to 85°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

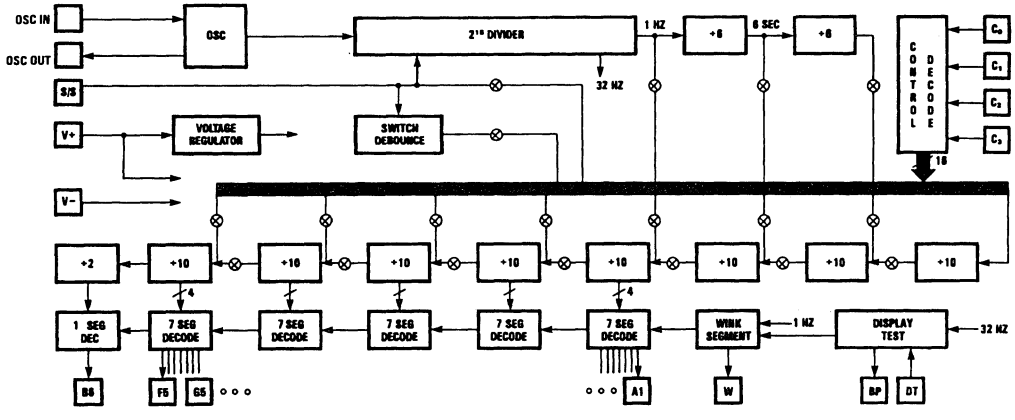


Figure 2: Functional Diagram

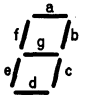


Figure 3: Digits Segment Assignment

NOTE: All typical values have been characterized but are not tested.

ELECTRICAL CHARACTERISTICS

Temperature = −40°C to +85°C, V_{DD} = 2.5V to 5.5V, V_{SS} = 0V, unless otherwise noted. Typical specifications measured at temperature = 25°C and V_{DD} = 2.8V unless otherwise noted.

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
V_{DD}	Operating Voltage	Note 3	2.5		5.5	V
I_{DD}	Operating Current	Note 4, All inputs = V_{DD} or GND				
		V_{DD} = 2.8V		1.0	10.0	µA
		V_{DD} = 5.5V		4.0	20.0	µA
	Input Current:	All Inputs V_{DD} or GND				
I_{IN}	C_0-C_3,	V_{DD} = 2.8V	0.0		1	µA
I_{SS}	S/S	Note 5	0.5	1.5	3.0	µA
I_{DT}	DT		40.0		110	µA
	Input Voltage:					
V_{IL}	C_0-C_3, DT, S/S				0.3 V_{DD}	V
V_{IH}			0.7 V_{DD}			V
V_{OL}	Segment Output Voltage	I_{OL} = 1µA			0.8	V
V_{OH}		I_{OH} = 1µA	V_{DD} − 0.8			
V_{OL}	Backplane Output Voltage	I_{OL} = 10µA			0.8	V
V_{OH}		I_{OH} = 10µA	V_{DD} − 0.8			
—	**Oscillator Stability:**					
	Temp. = 25°C, V_{DD} = 2.5V to 5.5V			0.1		ppm
	Temp. = −40°C to +85°C,					
	V_{DD} = 2.5V to 5.5V			5		ppm
	S/S Pulse Width:					
T_{HP}	High-pass Filter (Modes 0-3)		5		10,000	µs
T_{DE}	Debounce (Modes 4, 6, 8, 10)		10,000			µs
T_{DE}	w/o Debounce (Modes 5, 7, 9, 11)		5			µs

NOTES: 1. Due to the SCR structure inherent in junction-isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs or outputs before power is applied. If only inputs are affected, latchup also can be prevented by limiting the current into the input terminal to less than 1mA.

2. This limit refers to that of the package and will not occur during normal operation.
3. Internal reset to 00000 requires a maximum V_{DD} rise time of 1µs. Longer rise times at power-up may cause improper reset.
4. Operating current is measured with the LCD disconnected, and input current I_{SS} and I_{DT} supplied externally.
5. Inputs C_0-C_3 are latched internally and draw no DC current after switching. During switching, a 90µA peak current may be drawn for 10 nanoseconds.

NOTE: All typical values have been characterized but are not tested.

Table 1. Pin Assignment and Function

Pin	Name	Description
1	b_6/c_6	Half-digit LCD segment output.
2	f_5	Seven-segment LCD outputs.
3	g_5	
4	e_5	
5	d_5	
6	c_5	
7	b_5	
8	a_5	
9	f_4	
10	g_4	
11	e_4	
12	d_4	
13	c_4	
14	b_4	
15	a_4	
16	f_3	
17	g_3	
18	e_3	
19	d_3	
20	c_3	
21	b_3	
22	a_3	
23	f_2	
24	g_2	
25	e_2	
26	d_2	
27	c_2	
28	b_2	
29	a_2	
30	f_1	
31	g_1	
32	e_1	
33	d_1	
34	c_1	
35	b_1	
36	a_1	

Table 1. Pin Assignment and Function (Continued)

Pin	Name	Description
37	W	Wink-segment output.
38	BP	Backplane for LCD reference.
39	V_{DD}	Positive supply voltage.
40	OSC IN	Quartz Crystal connections
41	OSC OUT	
42	GND	Supply GRounD.
43	C_0	Mode-select control inputs.
44	C_1	
45	C_2	
46	C_3	
47	S/S	Start / Stop Input
48	DT	Display Test Input

Table 2. Mode Select Table

Mode	Control Pin Inputs				Function
	C_3	C_2	C_1	C_0	
0	0	0	0	0	1 hour interval timer
1	0	0	0	1	0.1 hour interval timer
2	0	0	1	0	0.01 hour interval timer
3	0	0	1	1	0.1 minute interval timer
4	0	1	0	0	1's counter with debounce
5	0	1	0	1	1's counter
6	0	1	1	0	10's counter with debounce
7	0	1	1	1	10's counter
8	1	0	0	0	100's counter with debounce
9	1	0	0	1	100's counter
10	1	0	1	0	1000's counter with debounce
11	1	0	1	1	1000's counter
12	1	1	0	0	Test display digits
13	1	1	0	1	Internal test
14	1	1	1	0	Internal test
15	1	1	1	1	Reset

NOTE: All typical values have been characterized but are not tested.

DETAILED DESCRIPTION

As Figure 2 shows the device consists of the following building blocks:

- A 32.768 kHz crystal oscillator with the associated dividers to generate timebase signals for periods of 1s (frequency of 1 Hz), 6s (1/10 min) and 36s (1/100 hour), and 32 Hz signal for LCD drivers.
- A debounce/high-pass detect circuit for the S/S (Start/Stop) input.
- A chain of cascaded decade counters, 3 decade counters for prescaling and 5½ BCD decade counters for display driving.
- Display control circuitry and BCD to 7-segment decoder/drivers.
- A control decoder to select different modes of operation. This is done by routing different signals to the different points in the chain of decade counters.

The control decoder has 4 inputs for selecting 16 possible modes of operation, numbered 0 to 15. The 16 modes are selected by placing the binary equivalent of the mode number on inputs C_0 to C_3. Table 2 shows the control inputs and the modes of operation.

After applying power, the ICM7249 requires a rise time of T_R to become active and for oscillation to begin, as shown in Figure 4. The BP (backplane) output changes state once every 512 cycles of the crystal oscillator, resulting in a square wave of 32 Hz. The display segments drive signal has the same level and frequency as BP. Segments are off when in phase with BP and are on when out of phase with BP.

A non-multiplexed LCD display is used because it is more stable over temperature and allows many standard LCD displays to be used.

Timer Mode of Operation

In modes 0 to 3 the device functions as an interval timer. In this mode, one of the timebase signals will be routed to the decade counters at a proper point in the chain. Depending on the selected mode the display will be incremented at 0.1 min, 0.01 hour, 0.1 hour or 1 hour rates.

Control of timing function is handled by the S/S input. There is a high-pass filtering effect on the S/S input in timer modes. Referring to Figure 5, timing is active when either S/S is held high for more than 12.5 ms, or if input frequency is 50 Hz to 120 kHz. Driving S/S with a frequency between 40 Hz to 50 Hz has an indeterminate effect on timing and should be avoided. Note that the T_{hp} intervals shown on Figure 4 are also applied to the intervals when the S/S input is low.

Counter Mode of Operation

In modes 4 to 11 the device functions as an event counter or totalizer. In this mode the S/S input will be routed to the decade counters at a proper point in the chain. Each positive transition of the S/S will be registered as one count. Depending on the selected mode, the display will be incremented by each pulse, every 10 pulses, every 100 pulses or every 1000 pulses.

In counter modes 4, 6, 8 and 10 the S/S input is subjected to debounce filtering. Referring to Figure 7, only the pulses with a frequency of less than 40 Hz are valid and

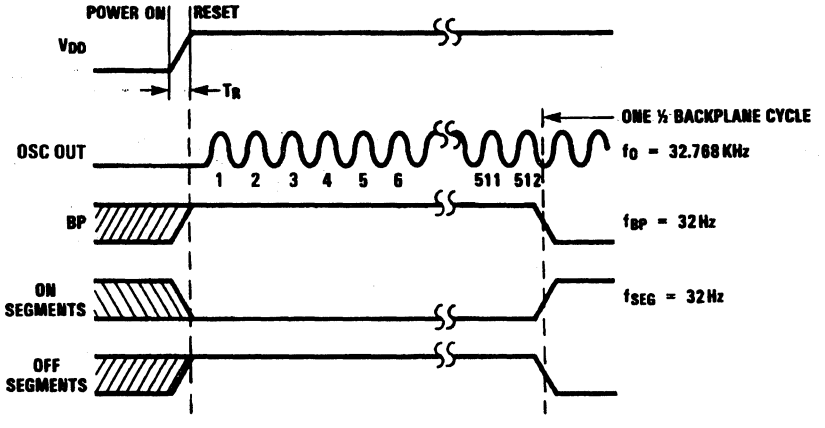


Figure 4: Power ON/Reset Waveforms

NOTE: All typical values have been characterized but are not tested.

will be counted. Input pulses with a frequency of 50 Hz to 120 kHz are not counted indivdually, but each burst of input pulses will be counted as one pulse if it lasts at least 12.5ms. Driving S/S with a frequency between 40 Hz to 50 Hz has an indeterminate result and should be avoided.

In counter modes 5, 7, 9 and 11 the S/S input is not subjected to any debouncing action and input pulses will be counted up to a frequency of 120 kHz.

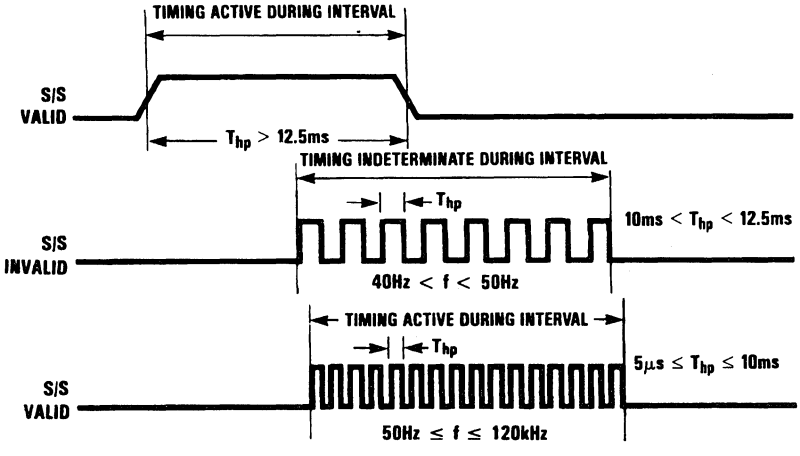


Figure 5: Start/Stop Input High-Pass Filtering in Timing Modes

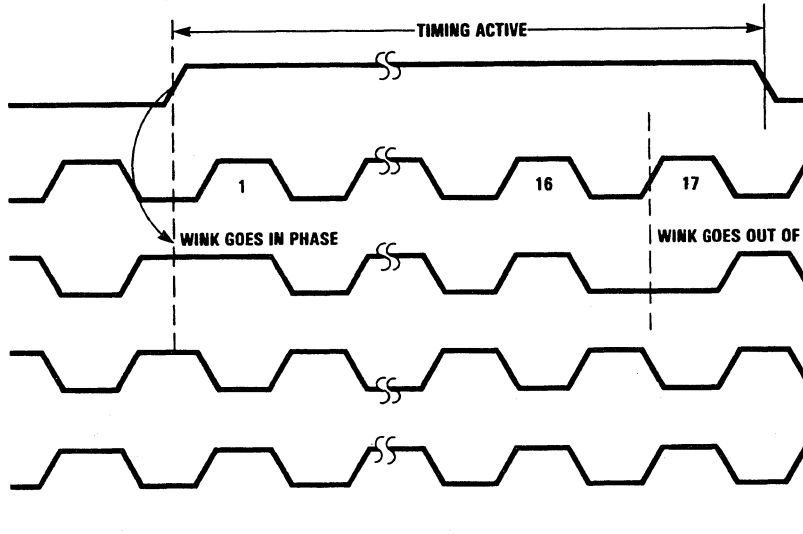


Figure 6: Wink Waveforms in Timing Modes

NOTE: All typical values have been characterized but are not tested.

Wink Segment

The wink segment is provided as an annunciator to indicate the 7249 is working. It can be connected to any kind of annunciator on an LCD, like the flashing colons in a clock type LCD.

In the timer modes, the wink segment flashes while timing is taking place. The wink segment waveform is shown on Figure 6 for timer modes. On the positive transition of S/S, the wink output turns off. It remains off for 16 BP cycles and turns back on for another 16 cycles. If timing is still active, this will be repeated, giving a wink flash rate of 1 Hz; otherwise, the wink segment remains on while timing is not active.

In the counter modes, the wink segment stays on until a pulse occurs on S/S input, then it winks off indicating a pulse is counted. This will happen regardless of whether the display is incremented. Figure 8 shows the wink waveform for counter modes. When a count occurs, the wink segment turns off at the end of the 16th BP cycle and turns back on at the end of the 32nd BP cycle, giving a half-second wink. If counting occurs more frequently than once a second, the wink output will continue to flash at the constant rate of 1 Hz.

Display Test and Reset

The display may be tested at any time without disturbing operation by pulsing DT high, as seen in Figure 8. On the next positive transition of BP, all the segments turn on and remain on until the end of the 16th BP cycle. This takes a half-second or less. All the segments then turn off for an additional 48 BP cycles (the end of the 64th cycle), after which valid data returns to the display. As long as DT is held high, the segments will remain on.

Additional display testing is provided by using mode 12. In this mode each displayed decade is incremented on each positive transition of S/S. Modes 13 and 14 are manufacturer testing only.

Mode 15 resets all the decades and internal counters to zero, essentially bringing everything back to power-up status.

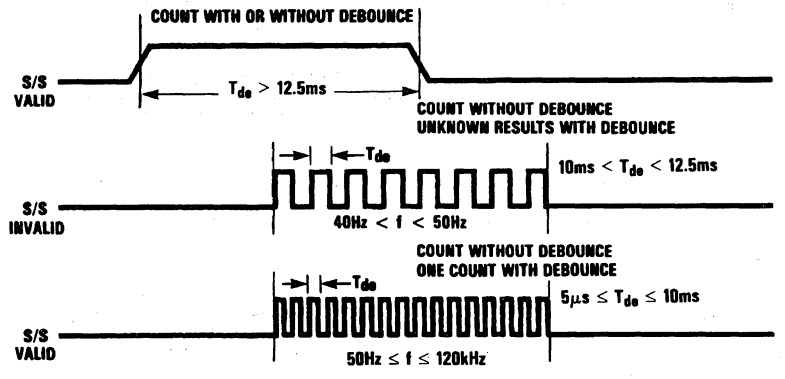


Figure 7: Start/Stop Input Debounce Filtering In Counting Modes

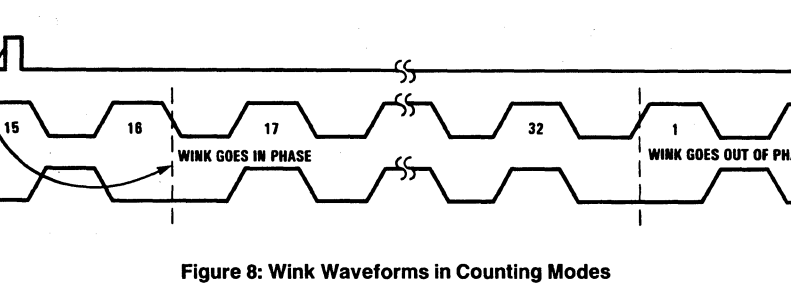


Figure 8: Wink Waveforms in Counting Modes

NOTE: All typical values have been characterized but are not tested.

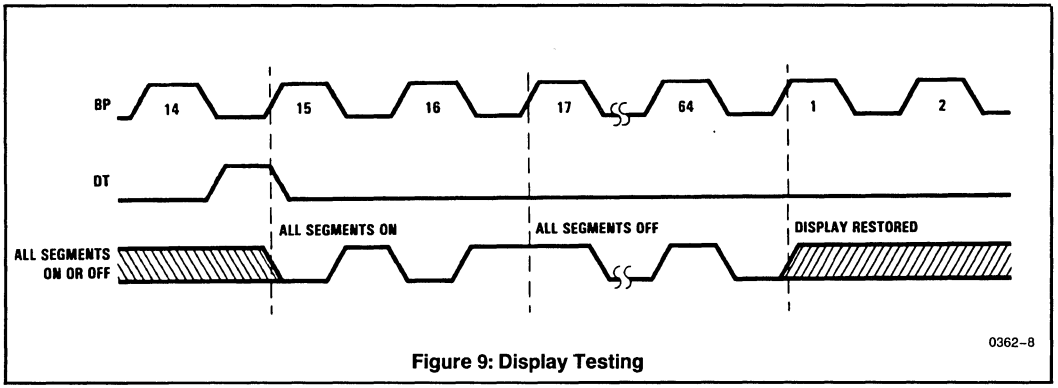


Figure 9: Display Testing

APPLICATIONS

A typical use of the ICM7249 is seen in Figure 10, the Motor Hour Meter. In this application the ICM7249 is configured as an hours-in-use meter and shows how many whole hours of line voltage have been applied. The 20MΩ resistor and high-pass filtering allow AC line activation of the S/S input. This configuration, which is powered by a 3V lithium cell, will operate continuously for 2½ years. Without the display, which only needs to be connected when a reading is required, the span of operation is extended to 10 years.

When the ICM7249 is configured as an attendance counter, as shown in Figure 11, the display shows each increment. By using mode 2, external debouncing of the gate switch is unnecessary, provided the switch bounce is less than 10 ms.

The 3V lithium battery can be replaced without disturbing operation if a suitable capacitor is connected in parallel with it. The display should be disconnected, if possible, during the procedure to minimize current drain. The capacitor should be large enough to store charge for the amount of time needed to physically replace the battery ($\Delta t = \Delta VC/I$). A 100μF capacitor initially charged to 3V will supply a current of 1.0μA for 50 seconds before its voltage drops to 2.5V, which is the minimum operating voltage for the ICM7249.

Before the battery is removed, the capacitor should be placed in parallel, across the V_{DD} and GND terminals. After the battery is replaced, the capacitor can be removed and the display reconnected.

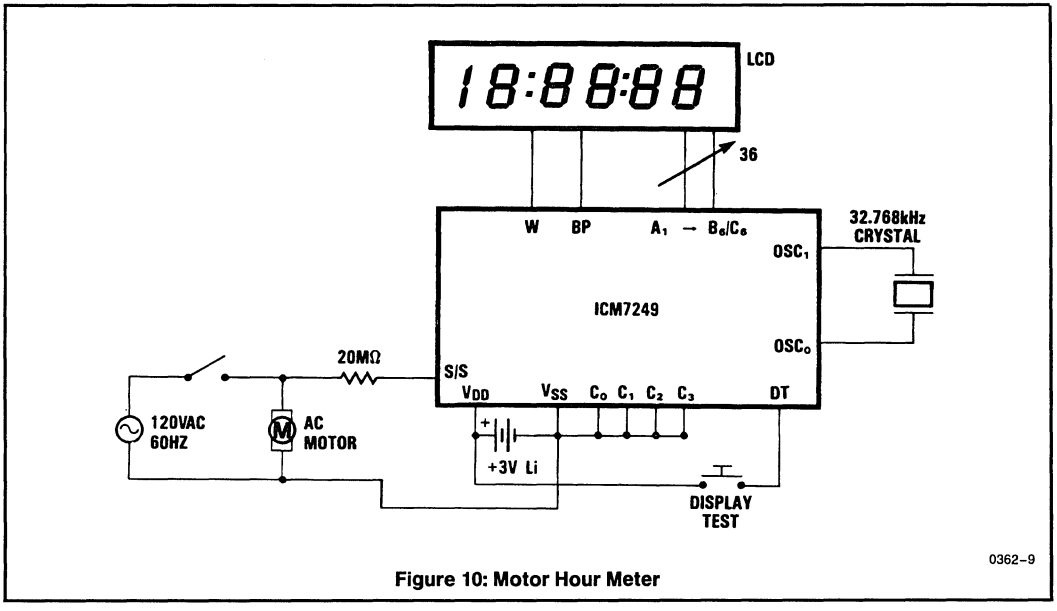


Figure 10: Motor Hour Meter

NOTE: All typical values have been characterized but are not tested.

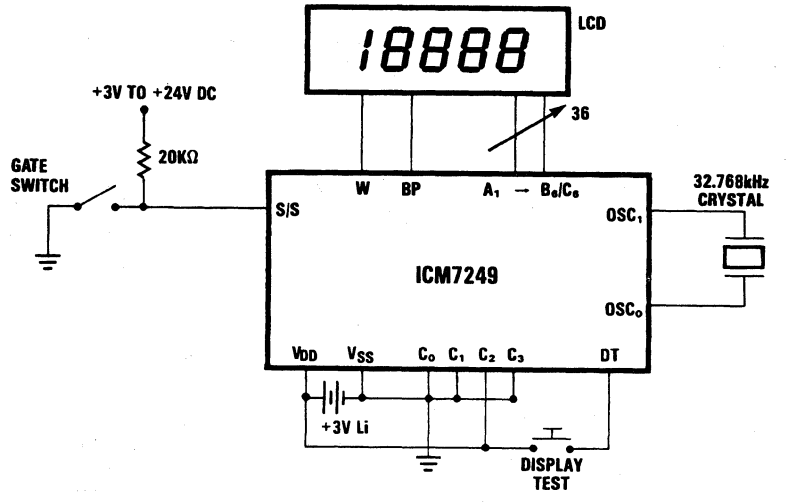


Figure 11: Attendance Counter

NOTE: All typical values have been characterized but are not tested.

DATA ACQUISITION 12

SPECIAL PURPOSE

HARRIS SEMICONDUCTOR

AD590
2-Wire Current Output Temperature Transducer

GENERAL DESCRIPTION

The AD590 is an integrated-circuit temperature transducer which produces an output current proportional to absolute temperature. The device acts as a high impedance constant current regulator, passing 1μA/°K for supply voltages between +4V and +30V. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2μA output at 298.2°K (+25°C).

The AD590 should be used in any temperature-sensing application between −55°C and +150°C in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance- measuring circuitry and cold-junction compensation are not needed in applying the AD590. In the simplest application, a resistor, a power source and any voltmeter can be used to measure temperature.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, and biasing proportional to absolute temperature. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

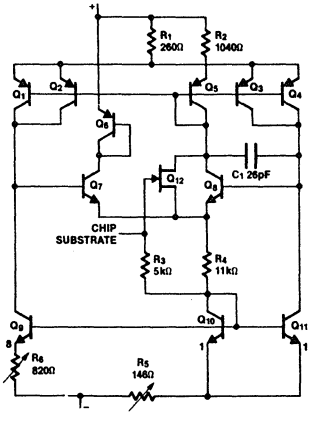
The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high-impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

FEATURES

- **Linear Current Output: 1μA/°K**
- **Wide Range: −55°C to +150°C**
- **Two-Terminal Device: Voltage In/Current Out**
- **Wide Power Supply Range: +4V to +30V**
- **Sensor Isolation From Case**
- **Low Cost**

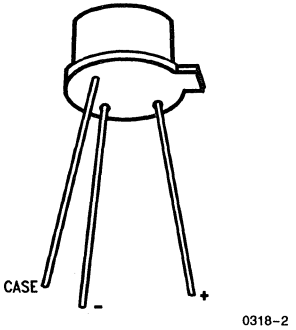
ORDERING INFORMATION

Non-Linearity (°C)	Part Number	Temperature Range	Package
±3.0	AD590IH	−55°C to +150°C	TO-52
±1.5	AD590JH	−55°C to +150°C	TO-52



0318-1

Figure 1: Functional Diagram



0318-2

Figure 2: Pin Configurations

300106-003

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Forward Voltage (V^+ to V^-) ..... +44V
Reverse Voltage (V^+ to V^-) ..... −20V
Breakdown Voltage (Case to V^+ or V^-) ..... ±200V
Storage Temperature Range ..... −65°C to +150°C
Rated Performance Temperature Range
TO-52 ..... −55°C to +150°C
Lead Temperature (Soldering, 10sec) ..... +300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

SPECIFICATIONS (Typical values at T_A = +25°C, V^+ = 5V unless otherwise noted)

Characteristics	AD590I	AD590J	Units
Output			
Nominal Output Current @ +25°C(298.2°K)	298.2	298.2	μA
Nominal Temperature Coefficient	1.0	1.0	μA/°K
Calibration Error @ +25°C (Notes 1, 5)	±10.0 max	±5.0 max	°C
Absolute Error (−55°C to +150°C) (Note 7)			
Without External Calibration Adjustment	±20.0 max	±10.0 max	°C
With External Calibration Adjustment	±5.8 max	±3.0 max	°C
Non-Linearity (Note 6)	±3.0 max	±1.5 max	°C
Repeatability (Notes 2, 6)	±0.1 max	±0.1 max	°C
Long Term Drift (Notes 3, 6)	±0.1 max	±0.1 max	°C/month
Current Noise	40	40	pA/$\sqrt{Hz}$
Power Supply Rejection:			
$+4V < V^+ < +5V$	0.5	0.5	μA/V
$+5V < V^+ < +15V$	0.2	0.2	μA/V
$+15V < V^+ < +30V$	0.1	0.1	μA/V
Case Isolation to Either Lead	10^{10}	10^{10}	Ω
Effective Shunt Capacitance	100	100	pF
Electrical Turn-On Time (Note 1)	20	20	μs
Reverse Bias Leakage Current (Note 4)	10	10	pA
Power Supply Range	+4 to +30	+4 to +30	V

NOTES: 1. Does not include self heating effects.
2. Maximum deviation between +25°C reading after temperature cycling between −55°C and +150°C.
3. Conditions: Constant +5V, constant +125°C.
4. Leakage current doubles every +10°C.
5. Mechanical strain on package may disturb calibration of device.
6. Guaranteed. But not tested.
7. −55°C Guaranteed by testing @ +25°C and @ +150°C.

TRIMMING OUT ERRORS

The ideal graph of current versus temperature for the AD590 is a straight line, but as Figure 3 shows, the actual shape is slightly different. Since the sensor is limited to the range of −55°C to +150°C, it is possible to optimize the accuracy by trimming. Trimming also permits extracting maximum performance from the lower-cost sensors.

The circuit of Figure 4 trims the slope of the AD590 output. The effect of this is shown in Figure 5.

The circuit of Figure 6 trims both the slope and the offset. This is shown in Figure 7. The diagrams are exaggerated to show effects, but it should be clear that these trims can be used to minimize errors over the whole range, or over any selected part of the range. In fact, it is possible to adjust the I-grade device to give less than 0.1°C error over the range 0°C to 90°C and less than 0.05°C error from 25°C to 60°C.

NOTE: All typical values have been characterized but are not tested.

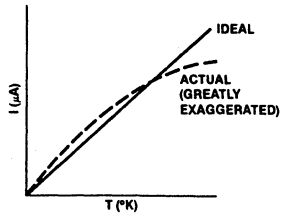


Figure 3: Trimming Out Errors

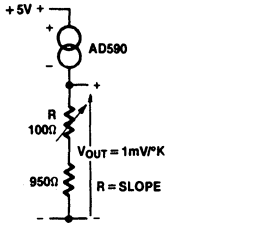


Figure 4: Slope Trimming

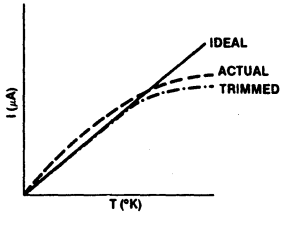


Figure 5: Effect of Slope Trim

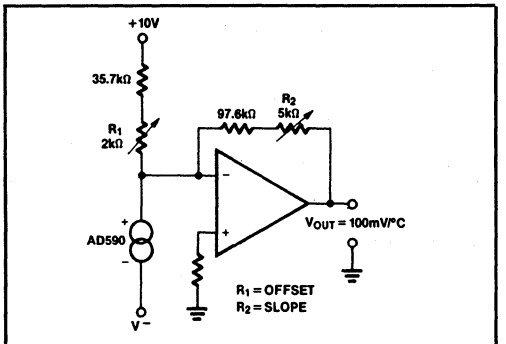


Figure 6: Slope and Offset Trimming

ACCURACY

Maximum errors over limited temperature spans, with $V_S = +5V$, are listed by device grade in the following tables. The tables reflect the worst-case linearities, which invariably occur at the extremities of the specified temperature range. The trimming conditions for the data in the tables are shown in Figures 4 and 6.

All errors listed in the tables are ±°C. For example, if ±1°C maximum error is required over the +25°C to +75°C range (i.e., lowest temperature of +25°C and span of 50°C), then the trimming of a J-grade device, using the single-trim circuit (Figure 4), will result in output having the required accuracy over the stated range. An I-grade device with two trims (Figure 6) will have less than ±0.2°C error. If the requirement is for less than ±1.4°C maximum error, from −25°C to +75°C (100° span from −25°C), it can be satisfied by an I-grade device with two trims.

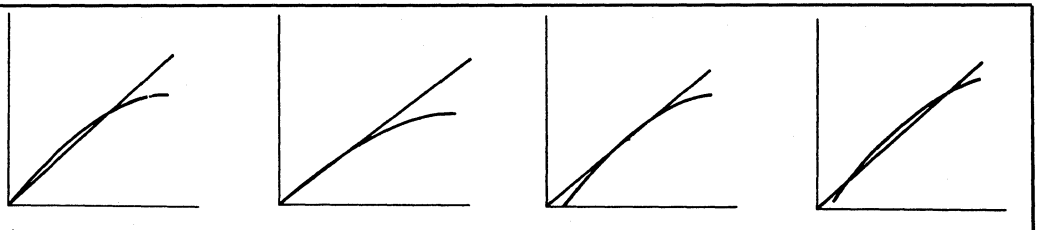


Figure 7: Effect of Slope and Offset Trimming

NOTE: All typical values have been characterized but are not tested.

I GRADE — MAXIMUM ERRORS, °C

Number of Trims	Temperature Span—°C	Lowest Temperature in Span—°C							
		−55	−25	0	+25	+50	+75	+100	+125
None	10	8.4	9.2	10.0	10.8	11.6	12.4	13.2	14.4
None	25	10.0	10.4	11.0	11.8	12.0	13.8	15.0	16.0
None	50	13.0	13.0	12.8	13.8	14.6	16.4	18.0	
None	100	15.2	16.0	16.6	17.4	18.8			
None	150	18.4	19.0	19.2					
None	205	20.0							
One	10	0.6	0.4	0.4	0.4	0.4	0.4	0.4	0.6
One	25	1.8	1.2	1.0	1.0	1.0	1.2	1.6	1.8
One	50	3.8	3.0	2.0	2.0	2.0	3.0	3.8	
One	100	4.8	4.5	4.2	4.2	5.0			
One	150	5.5	4.8	5.5					
One	205	5.8							
Two	10	0.3	0.2	0.1	*	*	0.1	0.2	0.3
Two	25	0.5	0.3	0.2	*	0.1	0.2	0.3	0.5
Two	50	1.2	0.6	0.4	0.2	0.2	0.3	0.7	
Two	100	1.8	1.4	1.0	2.0	2.5			
Two	150	2.6	2.0	2.8					
Two	205	3.0							

* Less than 0.05°C.

J GRADE — MAXIMUM ERRORS, °C

Number of Trims	Temperature Span—°C	Lowest Temperature in Span—°C							
		−55	−25	0	+25	+50	+75	+100	+125
None	10	4.2	4.6	5.0	5.4	5.8	6.2	6.6	7.2
None	25	5.0	5.2	5.5	5.9	6.0	6.9	7.5	8.0
None	50	6.5	6.5	6.4	6.9	7.3	8.2	9.0	
None	100	7.7	8.0	8.3	8.7	9.4			
None	150	9.2	9.5	9.6					
None	205	10.0							
One	10	0.3	0.2	0.2	0.2	0.2	0.2	0.2	0.3
One	25	0.9	0.6	0.5	0.5	0.5	0.6	0.8	0.9
One	50	1.9	1.5	1.0	1.0	1.0	1.5	1.9	
One	100	2.3	2.2	2.0	2.0	2.3			
One	150	2.5	2.4	2.5					
One	205	3.0							
Two	10	0.1	*	*	*	*	*	*	0.1
Two	25	0.2	0.1	*	*	*	*	0.1	0.2
Two	50	0.4	0.2	0.1	*	*	0.1	0.2	*
Two	100	0.7	0.5	0.3	0.7	1.0			
Two	150	1.0	0.7	1.2					
Two	205	1.6							

* Less than ±0.05°C.

NOTE: All typical values have been characterized but are not tested.

NOTES

1. Maximum errors over all ranges are guaranteed based on the known behavior characteristic of the AD590.
2. For one-trim accuracy specifications, the 205°C span is assumed to be trimmed at +25°C; for all other spans, it is assumed that the device is trimmed at the midpoint.
3. For the 205°C span, it is assumed that the two-trim temperatures are in the vicinity of 0°C and +140°C; for all other spans, the specified trims are at the endpoints.
4. In precision applications, the actual errors encountered are usually dependent upon sources of error which are often overlooked in error budgets. These typically include:
   a. Trim error in the calibration technique used
   b. Repeatability error
   c. Long-term drift errors

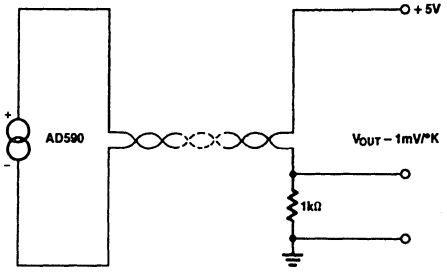
Trim error is usually the largest error source. This error arises from such causes as poor thermal coupling between the device to be calibrated and the reference sensor; reference sensor errors; lack of adequate time for the device being calibrated to settle to the final temperature; radically different thermal resistances between the case and the surroundings ($R_{\theta CA}$) when trimming and when applying the device.

Repeatability errors arise from a strain hysteresis of the package. The magnitude of this error is solely a function of the magnitude of the temperature span over which the device is used. For example, thermal shocks between 0°C and 100°C involve extremely low hysteresis and result in repeatability errors of less than ±0.05°C. When the thermal-shock excursion is widened to −55°C to +150°C, the device will typically exhibit a repeatability error of ±0.05°C (±0.10 guaranteed maximum).

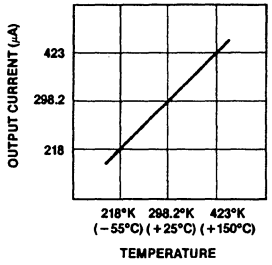
Long-term drift errors are related to the average operating temperature and the magnitude of the thermal shocks experienced by the device. Extended use of the AD590 at temperatures above 100°C typically results in long-term drift of ±0.03°C per month; the guaranteed maximum is ±0.10°C per month. Continuous operation at temperatures below 100°C induces no measurable drifts in the device. Besides the effects of operating temperature, the severity of thermal shocks incurred will also affect absolute stability. For thermal-shock excursions less than 100°C, the drift is difficult to measure (<0.03°C). However, for 200°C excursions, the device may drift by as much as ±0.10°C after twenty such shocks. If severe, quick shocks are necessary in the application of the device, realistic simulated life tests are recommended for a thorough evaluation of the error introduced by such shocks.

NOTE: All typical values have been characterized but are not tested.

TYPICAL APPLICATIONS

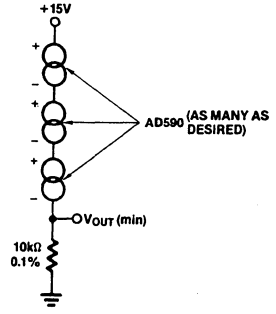


0318-11



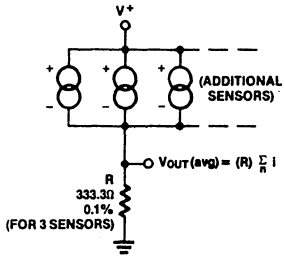
0318-12

Figure 8: Simple connection. Output is proportional to absolute temperature.



0318-13

Figure 9: Lowest-temperature sensing scheme. Available current is that of the "coldest" sensor.



0318-14

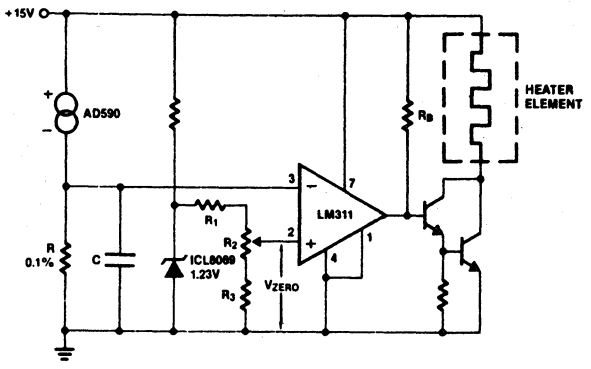
Figure 10: Average-temperature sensing scheme. The sum of the AD590 currents appears across R, which is chosen by the formula:

$$R = \frac{10k\Omega}{n}$$

n being the number of sensors.

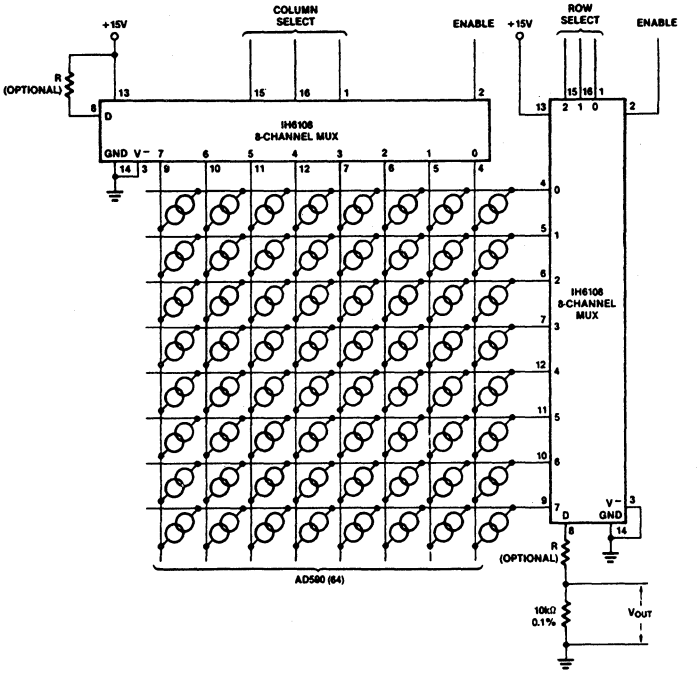
12

NOTE: All typical values have been characterized but are not tested.



0318-15

Figure 11: Single-setpoint temperature controller. The AD590 produces a temperature-dependent voltage across R (C is for filtering noise). Setting R_2 produces a scale-zero voltage. For the Celsius scale, make $R = 1k\Omega$ and $V_{ZERO} = 0.273$ volts. For Fahrenheit, $R = 1.8k\Omega$ and $V_{ZERO} = 0.460$ volts.



0318-16

Figure 12: Multiplexing sensors. If shorted sensors are possible, a series resistor in series with the D line will limit the current (shown as R, above: only one is needed). A six-bit digital word will select one of 64 sensors.

NOTE: All typical values have been characterized but are not tested.

AD590

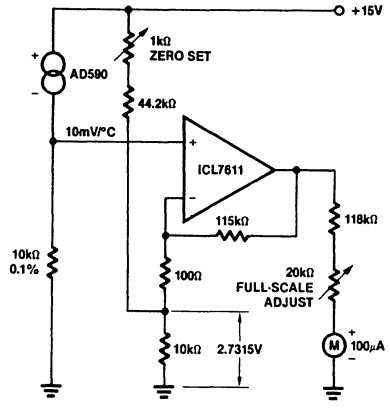


Figure 13: Centigrade thermometer (0°C – 100°C) . the ultra-low bias current of the ICL7611 allows the use of large-value gain-resistors, keeping meter-current error under ½%, and therefore saving the expense of an extra meter-driving amplifier.

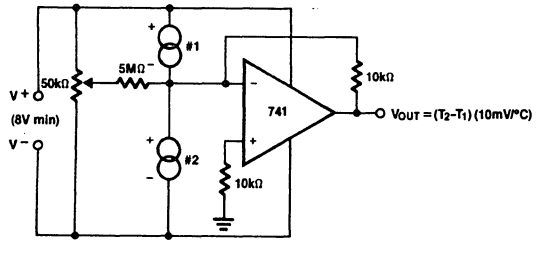


Figure 14: Differential thermometer. The 50kΩ pot trims offsets in the devices whether internal or external, so it can be used to set the size of the difference interval. This also makes it useful for liquid-level detection (where there will be a measurable temperature difference).

12

NOTE: All typical values have been characterized but are not tested.

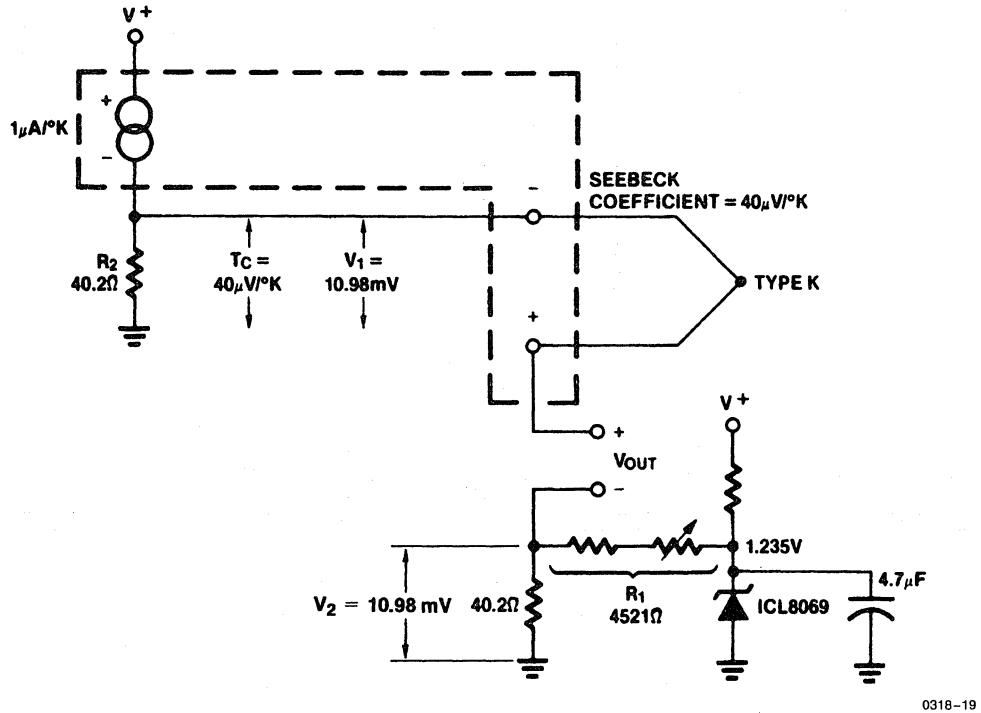


Figure 15: Cold-junction compensation for type K thermocouple. The reference junction(s) should be in close thermal contact with the AD590 case. V^+ must be at least 4V, while ICL8069 current should be set at 1mA − 2mA. Calibration does not require shorting or removal of the thermocouple: set R_1 for $V_2 = 10.98mV$. If very precise measurements are needed, adjust R_2 to the exact Seebeck coefficient for the thermocouple used (measured or from table) note V_1, and set R_1 to buck out this voltage (i.e., set $V_2 = V_1$). For other thermocouple types, adjust values to the appropriate Seebeck coefficient.

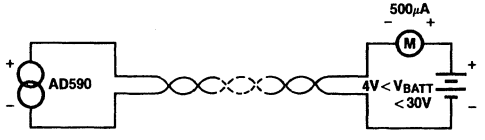
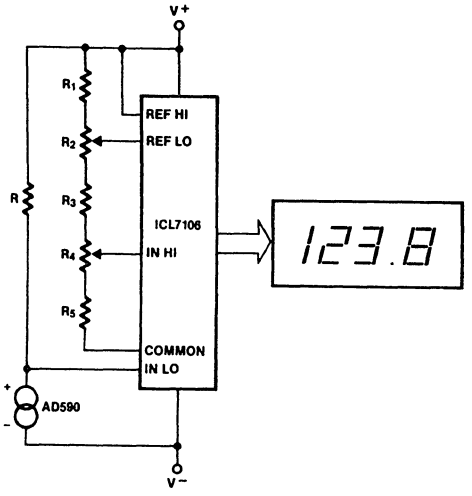


Figure 16: Simplest thermometer. Meter displays current output directly in degrees Kelvin. Using the AD590J, sensor output is within ± 10 degrees over the entire range.

NOTE: All typical values have been characterized but are not tested.



0318-21

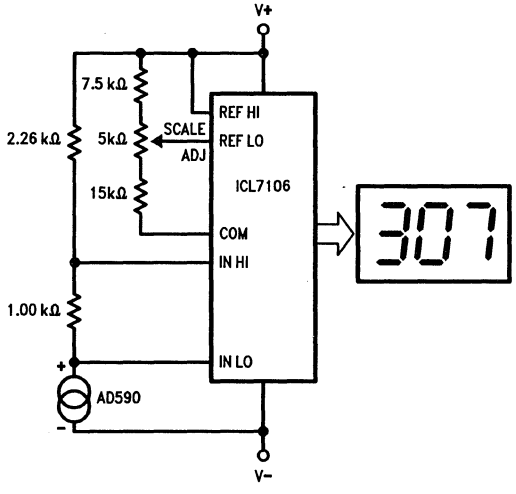
	R	R_1	R_2	R_3	R_4	R_5
°F	9.00	4.02	2.0	12.4	10.0	0
°C	5.00	4.02	2.0	5.11	5.0	11.8

$\sum_{n=1}^{5} R_n = 28k\Omega$ nominal

All values in kΩ

The ICL7106 has a V_{IN} span of ±2.0V, and a V_{CM} range of ($V^+ - 0.5$) Volts to ($V^- + 1$) Volts; R is scaled to bring each range within V_{CM} while not exceeding V_{IN}. V_{REF} for both scales is 500mV. Maximum reading on the Celsius range is 199.9°C, limited by the (short-term) maximum allowable sensor temperature. Maximum reading on the Fahrenheit range is 199.9°F (93.3°C), limited by the number of display digits. See note next page.

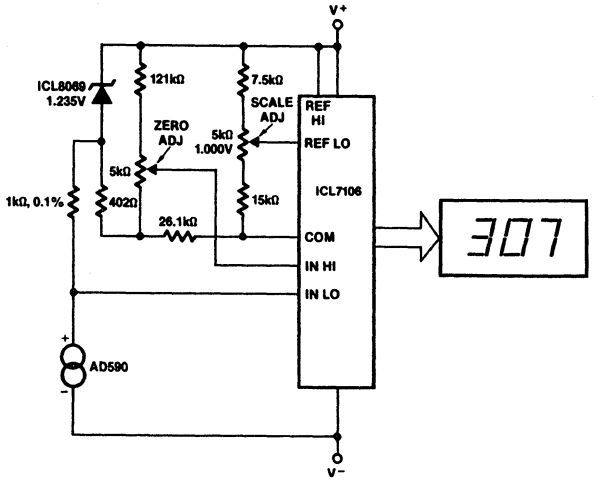
Figure 17: Basic digital thermometer, Celsius and Fahrenheit scales



0318-22

Figure 18: Basic digital thermometer, Kelvin scale. The Kelvin scale version reads from 0 to 1999°K theoretically, and from 223°K to 473°K actually. The 2.26kΩ resistor brings the input within the ICL7106 V_{CM} range: 2 general-purpose silicon diodes or an LED may be substituted.

NOTE: All typical values have been characterized but are not tested.



0318-23

Figure 19: Basic digital thermometer, Kelvin scale with zero adjust. This circuit allows "zero adjustment" as well as slope adjustment. The ICL8069 brings the input within the common-mode range, while the 5kΩ pots trim any offset at 218°K (−55°C), and set the scale factor.

Note on Figure 17, Figure 18 and Figure 19: Since all 3 scales have narrow V_{IN} spans, some optimization of ICL7106 components can be made to lower noise and preserve CMR. The table below shows the suggested values. Similar scaling can be used with the ICL7126/36.

Scale	V_{IN} Range (V)	R_{INT}(kΩ)	C_{AZ}(μF)
K	0.223 to 0.473	220	0.47
C	−0.25 to +1.0	220	0.1
F	−0.29 to +0.996	220	0.1

For all:

$C_{REF} = 0.1\mu F$ $C_{OSC} = 100pF$

$C_{INT} = 0.22\mu F$ $R_{OSC} = 100k\Omega$

NOTE: All typical values have been characterized but are not tested.

HARRIS SEMICONDUCTOR

ICL8069
Low Voltage Reference

GENERAL DESCRIPTION

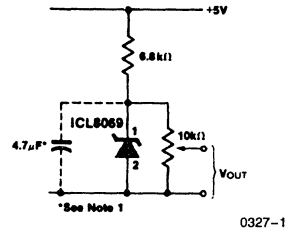
The ICL8069 is a 1.2V temperature compensated voltage reference. It uses the band-gap principle to achieve excellent stability and low noise at reverse currents down to 50μA. Applications include analog-to-digital converters, digital-to-analog converters, threshold detectors, and voltage regulators. Its low power consumption makes it especially suitable for battery operated equipment.

FEATURES

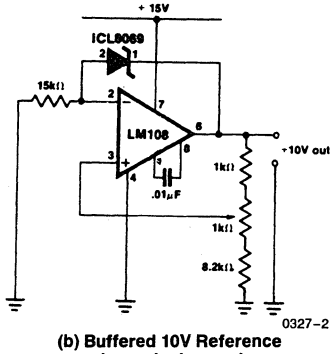
- **Low Bias Current — 50μA Min**
- **Low Dynamic Impedance**
- **Low Reverse Voltage**
- **Low Cost**

ORDERING INFORMATION

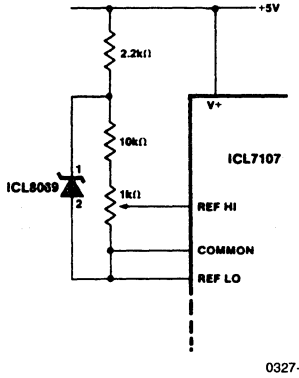
Part Number	Maximum Tempco	Temperature Range	Package
ICL8069CCZR	0.005%/°C	0°C to +70°C	TO-92
ICL8069CCSQ	0.005%/°C	0°C to +70°C	TO-52
ICL8069DCZR	0.01%/°C	0°C to +70°C	TO-92
ICL8069DCSQ	0.01%/°C	0°C to +70°C	TO-52
ICL8069DCBA	0.01%/°C	0°C to +70°C	8 Lead SOIC
ICL8069CMSQ	0.005%/°C	−55°C to +125°C	TO-52
ICL8069DMSQ	0.01%/°C	−55°C to +125°C	TO-52



(a) Simple Reference (1.2 volts or less)



(b) Buffered 10V Reference using a single supply.



(c) Double regulated 100mV reference for ICL7107 one-chip DPM circuit.

Figure 1: Functional Diagrams

12

303120-004

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

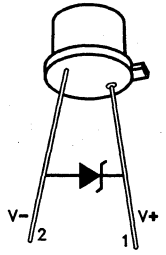
Reverse Voltage ..... See Note 2
Forward Current 10mA
Reverse Current 10mA
Power Dissipation ..... Limited by max forward/reverse current

Storage Temperature ..... −65°C to +150°C
Operating Temperature
ICL8069C ..... 0°C to +70°C
ICL8069M ..... −55°C to +125°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

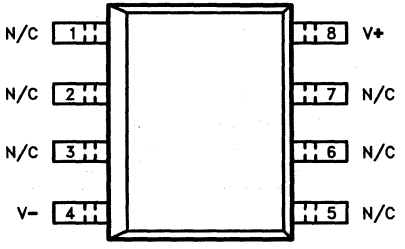
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristics	Test Conditions	Min	Typ	Max	Units
Reverse breakdown Voltage	I_R = 500µA	1.20	1.23	1.25	V
Reverse breakdown Voltage change	50µA ≤ I_R ≤ 5mA		15	20	mV
Reverse dynamic impedance	I_R = 50µA I_R = 500µA		1 1	2 2	Ω
Forward Voltage Drop	I_F = 500µA		0.7	1	V
RMS Noise Voltage	10Hz ≤ f ≤ 10kHz I_R = 500µA		5		µV
Long Term Stability	I_R = 4.75mA T_A = 25°C		1		ppm/kHR
Breakdown voltage Temperature coefficient ICL8069C ICL8069D	I_R = 500µA T_A = operating Temperature range (Note 3)			 .005 .01	%/°C
Reverse Current Range	1.18V to 1.27V	0.050		5	mA



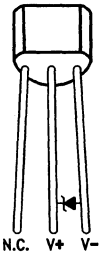
0327-4

TO-52



0327-9

8-Lead SOIC Package



0327-5

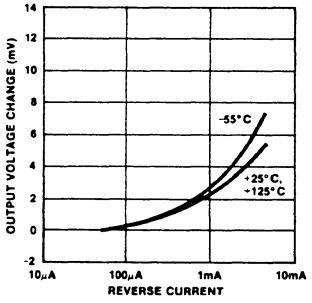
TO-92

Figure 2: Pin Configurations

NOTE: All typical values have been characterized but are not tested.

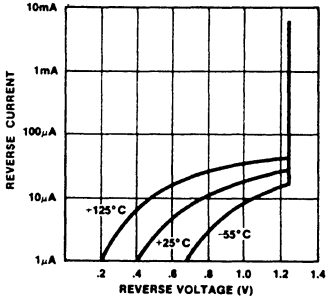
TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE CHANGE AS A FUNCTION OF REVERSE CURRENT



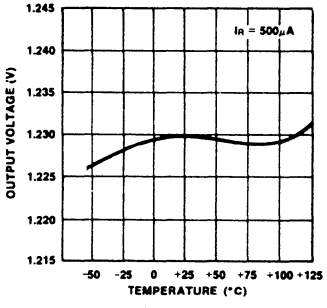
0327-6

REVERSE VOLTAGE AS A FUNCTION OF CURRENT



0327-7

REVERSE VOLTAGE AS A FUNCTION OF TEMPERATURE



0327-8

Notes: 1) If circuit strays in excess of 200pF are anticipated, a 4.7μF shunt capacitor will ensure stability under all operating conditions.
2) In normal use, the reverse voltage cannot exceed the reference voltage. However when plugging units into a powered-up test fixture, an instantaneous voltage equal to the compliance of the test circuit will be seen. This should not exceed 20V.
3) For the military part, measurements are made at 25°C, −55°C, and +125°C. The unit is then classified as a function of the worst case T.C. from 25°C to −55°C, or 25°C to +125°C.

12

NOTE: All typical values have been characterized but are not tested.

DATA ACQUISITION 13

DATA COMMUNICATIONS

HARRIS SEMICONDUCTOR

ICL232
+5 Volt Powered Dual RS-232 Transmitter/Receiver

GENERAL DESCRIPTION

The ICL232 is a dual RS-232 transmitter/receiver interface circuit that meets all EIA RS-232C specifications. It requires a single +5V power supply, and features two onboard charge pump voltage converters which generate +10V and −10V supplies from the 5V supply.

The drivers feature true TTL/CMOS input compatibility, slew-rate-limited output, and 300 ohms power-off source impedance. The receivers can handle up to ±30 volts, and have a 3 to 7 kilohms input impedance. The receivers also have hysteresis to improve noise rejection.

Typical Applications

Any System Requiring RS-232 Communications Port:

- **Computers—Portable and Mainframe**
- **Peripherals—Printers and Terminals**
- **Portable Instrumentation**
- **Modems**
- **Dataloggers**

ORDERING INFORMATION

Part	Temperature Range	Package
ICL232CPE	0°C to + 70°C	16 Pin Plastic DIP
ICL232CJE		16 Pin CERDIP
ICL232CBE		16 Pin SOIC (WB)
ICL232IPE	−40°C to +85°C	16 Pin Plastic DIP
ICL232IJE		16 Pin CERDIP
ICL232IBE		16 Pin SOIC (WB)
ICL232MJE	−55°C to +125°C	16 Pin CERDIP

FEATURES

- **Meets All RS-232C Specifications**
- **Requires Only Single +5V Power Supply**
- **Onboard Voltage Quadrupler**
- **Low Power Consumption**
- **2 Drivers**
  - **—±9V Output Swing for +5V Input**
  - **—300 Ohms Power-off Source Impedance**
  - **—Output Current Limiting**
  - **—TTL/CMOS Compatible**
  - **—30 V/us Maximum Slew Rate**
- **2 Receivers**
  - **—±30V Input Voltage Range**
  - **—3 to 7 kohms Input Impedance**
  - **—0.5V Hysteresis to Improve Noise Rejection**
- **All Critical Parameters are Guaranteed Over the Entire Commercial, Industrial and Military Temperature Ranges**

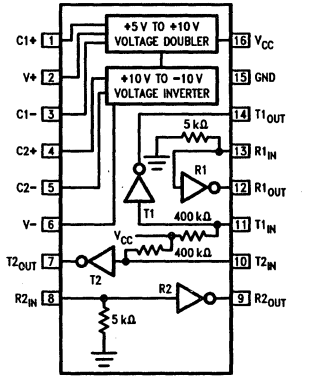
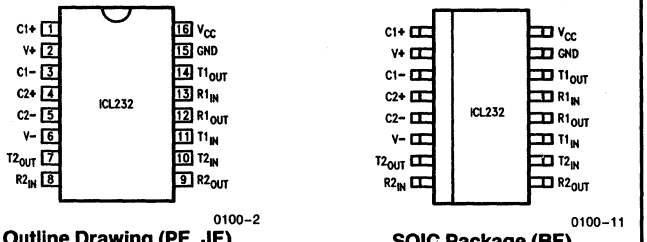


Figure 2: ICL232 Functional Diagram



Outline Drawing (PE, JE) **SOIC Package (BE)**

Figure 1: Pin Configurations

301600-003

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to ground .....(GND − 0.3V) < V_{CC} < 6V
V^+ to ground .....(V_{CC} − 0.3V) < V^+ < 12V
V^- to ground.....−12V < V^- < (GND + 0.3V)
Input Voltages
$T1_{in}$, $T2_{in}$ .....(V^- − 0.3V) < V_{in} < (V^+ + 0.3V)
$R1_{in}$, $R2_{in}$ .....±30V
Output Voltages
$T1_{OUT}$, $T2_{OUT}$ ..(V^- − 0.3V) < V_{TXOUT} < (V^+ + 0.3V)
$R1_{OUT}$, $R2_{OUT}$ .....
.....(GND − 0.3V) < V_{RXOUT} < (V^+ + 0.3V)
Short Circuit Duration
$T1_{OUT}$, $T2_{OUT}$.....Continuous
$R1_{OUT}$, $R2_{OUT}$ .....Continuous
Continuous Total Power Dissipation (T_a = 25°C)
CERDIP Package 500mW
derate −9.5 mW/°C above 70°C
Plastic Package.....375mW
derate −7.0 mW/°C above 70°C
SO Package .....375 mW
derate −7.0 mW/°C above 70°C
Storage Temperature Range .....−65°C to +150°C
Lead Temperature (Soldering, 10 sec).....+300°C
Operating Temperature Range
ICL232C.....0°C to +70°C
ICL232I .....−40°C to +85°C
ICL232M .....−55°C to +125°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{CC} = +5V ±10%, T_a = operating temperature range, Test Circuit as in Figure 3 (unless otherwise specified)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ	Max	
T_{OUT}	Transmitter Output Voltage Swing	$T1_{OUT}$ and $T2_{OUT}$ loaded with 3 kΩ to ground	±5	±9	±10	V
I_{CC}	Power Supply Current	Outputs Unloaded, T_a = 25°C		5	10	mA
V_{IL}	Tin, Input Logic Low				0.8	V
V_{IH}	Tin, Input Logic High		2.0			V
I_p	Logic Pullup Current	$T1_{in}$, $T2_{in}$ = 0V		15	200	µA
V_{in}	RS-232 Input Voltage Range		−30		+30	V
R_{in}	Receiver Input Impedance	V_{in} = ±3V	3.0	5.0	7.0	kΩ
V_{IN} (H−L)	Receiver Input Low Threshold	V_{cc} = 5.0V, T_a = 25°C	0.8	1.2		V
V_{IN} (L−H)	Receiver Input High Threshold	V_{cc} = 5.0V, T_a = 25°C		1.7	2.4	V
V_{hyst}	Receiver Input Hysteresis		0.2	0.5	1.0	V
V_{OL}	TTL/CMOS Receiver Output Voltage Low	I_{out} = 3.2mA		0.1	0.4	V
V_{OH}	TTL/CMOS Receiver Output Voltage High	I_{out} = −1.0mA	3.5	4.6		V
t_{pd}	Propagation Delay	RS-232 to TTL or TTL to RS-232		0.5		µs
SR	Instantaneous Slew Rate	C_L = 10 pF, R_L = 3 kΩ, T_a = 25°C (Note 1, 2)			30	V/µs
SR_t	Transition Region Slew Rate	R_L = 3 kΩ, C_L = 2500 pF Measured from +3V to −3V or −3V to +3V		3		V/µs
R_{out}	Output Resistance	V_{cc} = V+ = V− = 0V, V_{out} = ±2V	300			Ω
I_{SC}	RS-232 Output Short Circuit Current	$T1_{out}$ or $T2_{out}$ shorted to GND		±10		mA

NOTE 1: Guaranteed by design.
2: See Figure 5 for definition.

NOTE: All typical values have been characterized but are not tested.

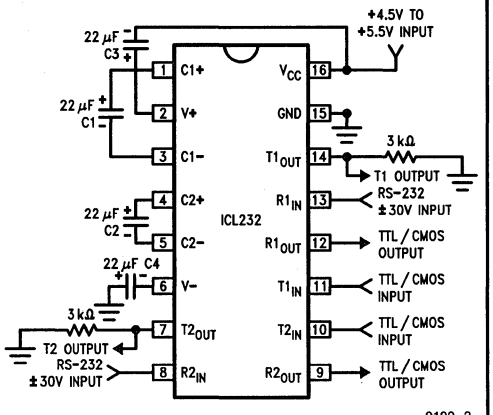


Figure 3: General Test Circuit

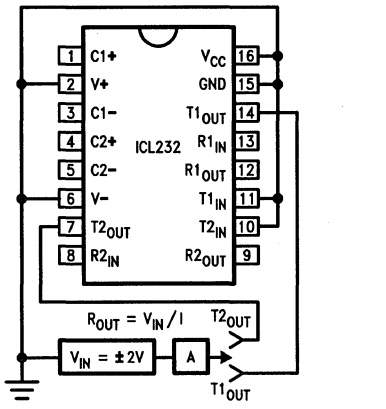
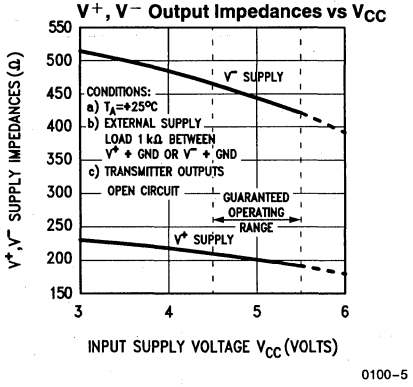
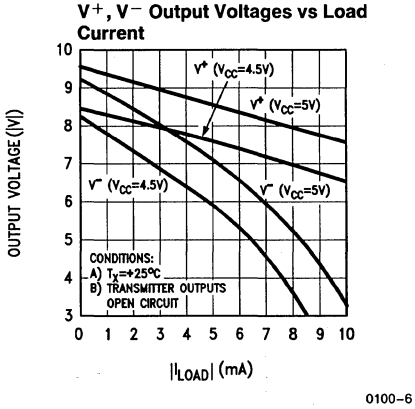


Figure 4: Power-Off Source Resistance Configuration

TYPICAL PERFORMANCE CHARACTERISTICS





NOTE: All typical values have been characterized but are not tested.

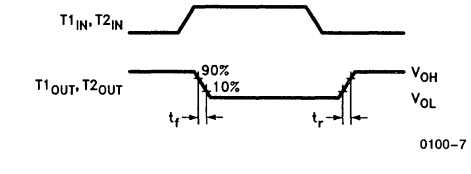
DETAILED DESCRIPTION

The ICL232 is a dual RS-232 transmitter/receiver powered by a single +5V power supply which meets all EIA RS-232C specifications and features low power consumption. The functional diagram (Figure 2) illustrates the major elements of the ICL232. The circuit is divided into three sections: a voltage quadrupler, dual transmitters, and dual receivers.

Voltage Converter

An equivalent circuit of the dual charge pump is illustrated in Figure 5.

The voltage quadrupler contains two charge pumps which use two phases of an internally generated clock to generate +10V and −10V. The nominal clock frequency is 16 kHz. During phase one of the clock, capacitor C1 is charged to V_{CC}. During phase two, the voltage on C1 is added to V_{CC}, producing a signal across C2 equal to twice V_{CC}. At the same time, C3 is also charged to $2V_{CC}$, and then during phase one, it is inverted with respect to ground to produce a signal across C4 equal to $-2V_{CC}$. The voltage converter accepts input voltages up to 5.5V. The output impedance of the doubler (V^+) is approximately 200 ohms, and the output impedance of the inverter (V^-) is approximately 450 ohms. Typical graphs are presented which show the voltage converters output vs input voltage and output voltages vs load characteristics. The test circuit (Figure 3) uses 22 uF capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the output impedance of the voltage doubler and inverter, and increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the V^+ and V^- supplies.



Instantaneous Slew Rate (SR) = $\frac{(0.8)(V_{oh} - V_{ol})}{t_r}$ or $\frac{(0.8)(V_{ol} - V_{oh})}{t_f}$

Figure 6: Slew Rate Definition

Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of V_{CC}, or 1.3V for V_{CC} = 5V. A logic 1 at the input results in a voltage of between −5V and V^- at the output, and a logic 0 results in a voltage between +5V and (V^+ −0.6V). Each transmitter input has an internal 400 kilohm pullup resistor so any unused input can be left unconnected and its output remains in its low state. The output voltage swing meets the RS-232C specification of ±5V minimum with the worst case conditions of: both transmitters driving 3kohm minimum load impedance, V_{CC} = 4.5V, and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than 30V/us. The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of 300 ohms with ±2V applied to the outputs and V_{CC} = 0V.

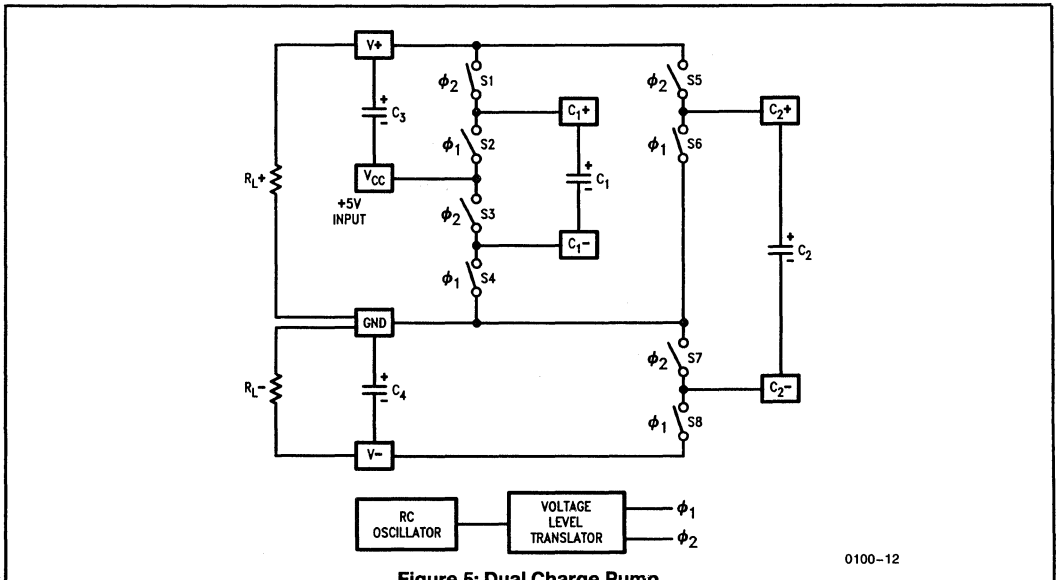


Figure 5: Dual Charge Pump

NOTE: All typical values have been characterized but are not tested.

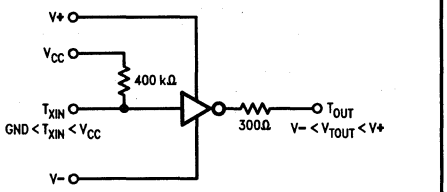


Figure 7: Transmitter

Receivers

The receiver inputs accept up to ±30V while presenting the required 3 to 7 kilohms input impedance even if the power is off (V_{CC}=0V). The receivers have a typical input threshold of 1.3V which is within the ±3V limits, known as the transition region, of the RS-232 specification. The receiver output is 0V to V_{CC}. The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and −30V. The receivers feature 0.5V hysteresis to improve noise rejection.

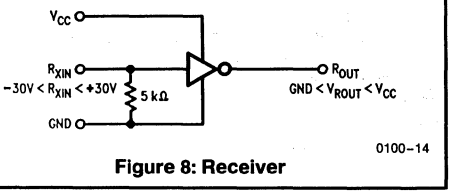
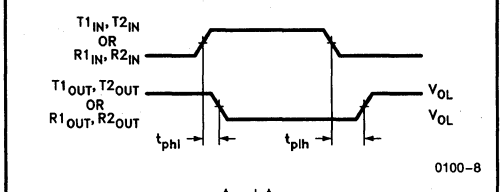


Figure 8: Receiver



Average Propagation Delay = $\frac{t_{phl} + t_{plh}}{2}$

Figure 9: Propagation Delay Definition

APPLICATIONS

The ICL232 may be used for all RS-232 data terminal and communication links. It is particularly useful in applications where ±12V power supplies are not available for conventional RS-232 interface circuits. The applications presented represent typical interface configurations.

A simple duplex RS-232 port with CTS/RTS handshaking is illustrated in Figure 10. Fixed output signals such as DTR (data terminal ready) and DSRS (data signaling rate select) is generated by driving them through a 5 kΩ resistor connected to V^+.

In applications requiring four RS-232 inputs and outputs (Figure 11), note that each circuit requires two charge pump capacitors (C1 and C2) but can share common reservoir capacitors (C3 and C4). The benefit of sharing common reservoir capacitors is the elimination of two capacitors and the reduction of the charge pump source impedance which effectively increases the output swing of the transmitters.

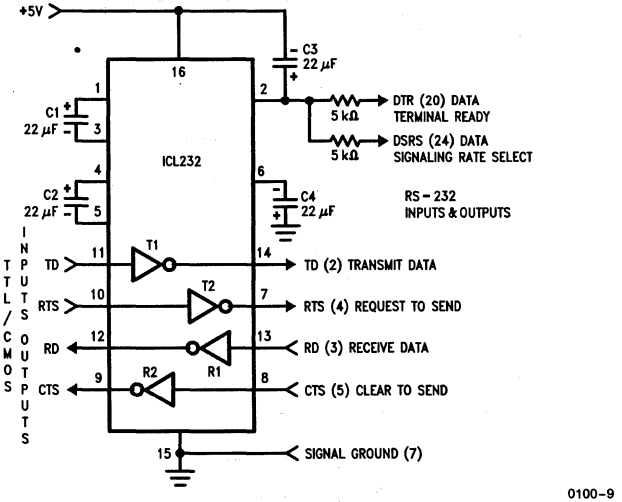


Figure 10: Simple Duplex RS-232 Port with CTS/RTS Handshaking

NOTE: All typical values have been characterized but are not tested.

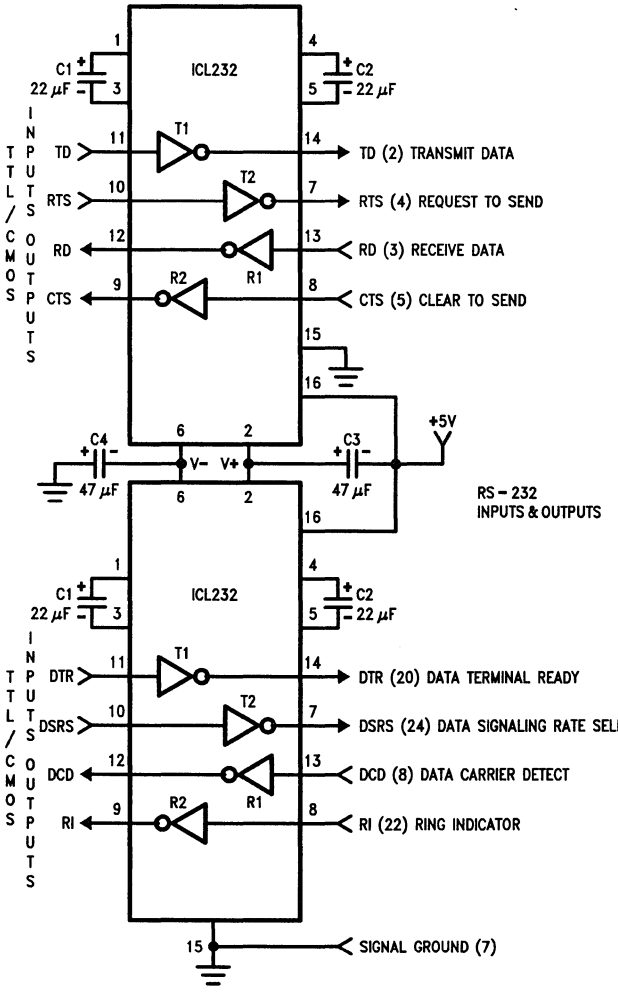


Figure 11: Combining Two ICL232's for 4 Pairs of RS-232 Inputs and Outputs

13

NOTE: All typical values have been characterized but are not tested.

DATA ACQUISITION 14

MEMORY

HARRIS SEMICONDUCTOR

IM6653/IM6654
4096-Bit CMOS UV EPROM

GENERAL DESCRIPTION

The Harris IM6653 and IM6654 are fully decoded 4096 bit CMOS electrically programmable ROMs (EPROMs) fabricated with Harris' advanced CMOS processing technology. In all static states these devices exhibit the microwatt power dissipation typical of CMOS. Inputs and three-state outputs are TTL compatible and allow for direct interface with common system bus structures. On-chip address registers and chip select functions simplify system interfacing requirements.

The IM6653 and IM6654 are specifically designed for program development applications where rapid turn-around for program changes is required. The devices may be erased by exposing their transparent lids to ultra-violet light, and then re-programmed.

FEATURES

- **Organization — IM6653: 1024×4**
  IM6654: 512×8
- **Low Power — 770μW Maximum Standby**
- **High Speed**
  —300ns 10V Access Time For IM6653/54 AI
  —450ns 5V Access Time For IM6653/54-1I
- **Single +5V Supply Operation**
- **UV Erasable**
- **Synchronous Operation For Low Power Dissipation**
- **Three-State Outputs and Chip Select for Easy System Expansion**

ORDERING INFORMATION

Part Number	Temperature Range	Package
IM6653/4IJG	−40°C to +85°C	24-Pin CERDIP
IM6653/4-1IJG	−40°C to +85°C	24-Pin CERDIP
IM6653/4AIJG	−40°C to +85°C	24-Pin CERDIP
IM6653/4MJG*	−55°C to +125°C	24-Pin CERDIP
IM6653/4AMJG*	−55°C to +125°C	24-Pin CERDIP

* Add /HR for HiRel processing

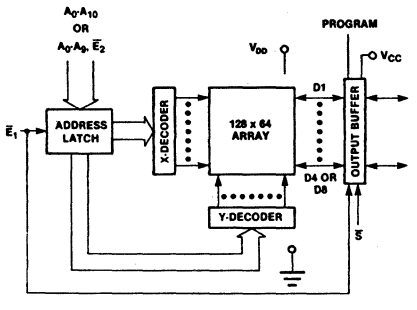


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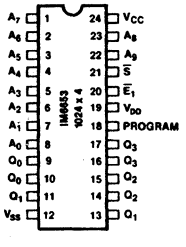
Figure 1: Functional Diagram



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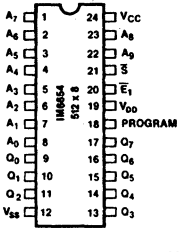

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Figure 2: Pin Configurations

16002

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS (IM6653/54 I, -1I, M)

Supply Voltages
$V_{DD}-V_{SS}$ ..... +8.0V
$V_{CC}-V_{SS}$ ..... +8.0V
Input or Output Voltage ..... (V_{SS} −0.3V) to (V_{DD} +0.3V)
Operating Range Range (T_A)
Industrial ..... −40°C to +85°C
Military ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC ELECTRICAL CHARACTERISTICS

($V_{CC}=V_{DD}=5V \pm 10\%$ $V_{SS}=0V$, T_A = Operating Temperature Range)

Symbol	Parameter	Test Conditions	IM6653/54I, -1I, M		Units
			Min	Max	
V_{IH}	Logical "1" Input Voltage	$\overline{E}_1$, $\overline{S}$	$V_{DD}-2.0$		V
V_{IH}		Address Pins	2.7		
V_{IL}	Logical "0" Input Voltage			0.8	
I_I	Input Leakage	$GND \le V_{IN} \le V_{DD}$	−1.0	1.0	μA
V_{OH}	Logical "1" Output Voltage	$I_{OH}=-0.2mA$	2.4		V
V_{OL}	Logical "0" Output Voltage	$I_{OL}=2.0mA$		0.45	
I_{OLK}	Output Leakage	$GND \le V_O \le V_{CC}$	−1.0	1.0	μA
I_{STBY}	Standby Supply Current	$V_{IN}=V_{DD}$		100	
I_{CC}		$V_{IN}=V_{DD}$		40	
I_{DD}	Operating Supply Current (1)	f=1MHz		6	mA
C_I	Input Capacitance	Note 1		7.0	pF
C_O	Output Capacitance	Note 1		10.0	

Note: 1. For design reference only, not 100% tested.

AC ELECTRICAL CHARACTERISTICS

($V_{CC}=V_{DD}=5V \pm 10\%$ $V_{SS}=0V$, $C_L=50pf$, T_A = Operating Temperature Range)

Symbol	Parameter	IM6653/54-1I		IM6653/54 I		IIM6653/54 M		Units
		Min	Max	Min	Max	Min	Max	
TE_1LQV	Access Time From $\overline{E}_1$		450		550		600	ns
TSLQV	Output Enable Time		110		140		150	
TE_1HQZ	Output Disable Time		110		140		150	
TE_1HE_1L	$\overline{E}_1$ Pulse Width (Positive)	130		150		150		
TE_1LE_1H	$\overline{E}_1$ Pulse Width (Negative)	450		550		600		
$TAVE_1L$	Address Setup Time	0		0		0		
TE_1LAX	Address Hold Time	80		100		100		
TE_2VE_1L	Chip Enable Setup Time (6654)	0		0		0		
TE_1LE_2X	Chip Enable Hold Time (6654)	80		100		100		

14

NOTE: All typical values have been characterized but are not tested.

ABSOLUTE MAXIMUM RATINGS (IM6653/54AI, AM)

Supply Voltages
- $V_{DD}-V_{SS}$ ..... +11.0V
- $V_{CC}-V_{SS}$ ..... +11.0V

Input or Output Voltage ..... (V_{SS} −0.3V) to (V_{DD} +0.3V)

Operating Temperature Range
- Industrial ..... −40°C to +85°C
- Military ..... −55°C to +125°C

Storage Temperature Range ..... −65°C to +150°C

Lead Temperature (Soldering, 10sec) ..... 300°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC ELECTRICAL CHARACTERISTICS

($V_{CC}=V_{DD}=4.5V$ to 10.5V $V_{SS}=0V$, T_A=Operational Temperature Range)

Symbol	Parameter	Test Conditions	IM6653/54AI, AM		Units
			Min	Max	
V_{IH}	Logical "1" Input Voltage	$\overline{E}_1$, $\overline{S}$	$V_{DD}-2.0$		V
V_{IH}		Address Pins	$V_{DD}-2.0$		
V_{IL}	Logical "0" Input Voltage			0.8	
I_I	Input Leakage	$GND \le V_{IN} \le V_{DD}$	−1.0	1.0	μA
V_{OH}	Logical "1" Output Voltage	$I_{OUT}=0$ (Note 1)	$V_{CC}-0.01$		V
V_{OL}	Logical "0" Output Voltage	$I_{OUT}=0$ (Note 1)		$V_{SS}+0.01$	
I_{OLK}	Output Leakage	$V_{SS} \le V_O \le V_{CC}$	−1.0	1.0	μA
I_{STBY}	Standby Supply Current	$V_{IN}=V_{DD}$		100	
I_{CC}		$V_{IN}=V_{DD}$		40	
I_{DD}	Operating Supply Current	f=1MHz		12	mA
C_I	Input Capacitance	Note 1		7.0	pF
C_O	Output Capacitance	Note 1		10.0	

Note: 1. For design reference only, not 100% tested.

AC ELECTRICAL CHARACTERISTICS

($V_{CC}=V_{DD}=10V \pm 5\%$ $V_{SS}=0V$, $C_L=50pf$, T_A=Operating Temperature Range)

Symbol	Parameter	IM6653/54 AI		IM6653/54 AM		Units
		Min	Max	Min	Max	
TE_1LQV	Access Time From $\overline{E}_1$		300		350	ns
TSLQV	Output Enable Time		60		70	
TE_1HQZ	Output Disable Time		60		70	
TE_1HE_1L	$\overline{E}_1$ Pulse Width (Positive)	125		125		
TE_1LE_1H	$\overline{E}_1$ Pulse Width (Negative)	300		350		
$TAVE_1L$	Address Setup Time	0		0		
TE_1LAX	Address Hold Time	60		60		
TE_2VE_1L	Chip Enable Setup Time (6654)	0		0		
TE_1LE_2X	Chip Enable Hold Time (6654)	60		60		

NOTE: All typical values have been characterized but are not tested.

PIN ASSIGNMENTS

Pin	Symbol	Active Level	Description
1-8,23	A_0-A_7,A_8	–	Address Lines
9-11, 13-17	Q_0-Q_7 Q_0-Q_3	– –	Data Out lines, 6654 Data Out lines, 6653
12	V_{SS}	–	Negative Supply
18	Program	–	Programming pulse input
19	V_{DD}	–	Chip positive supply, normally tied to V_{CC}
20	$\overline{E}_1$	L	Strobe line, latches both address lines and, for 6654, Chip enable $\overline{E}_2$
21	$\overline{S}$	L	Chip select line, must be low for valid data out
22	Ag $\overline{E}_2$	– L	Additional address line for 6653 Chip enable line, latched by Chip enable $\overline{E}_1$ on 6654
24[1]	V_{CC}	–	Output buffer positive supply

READ MODE OPERATION

In a typical READ operation address lines and chip enable $\overline{E}_2$* are latched by the falling edge of chip enable $\overline{E}_1$ (T=0). Valid data appears at the outputs one access time (TELQV) later, provided level-sensitive chip select line $\overline{S}$ is low (T=3). Data remains valid until either $\overline{E}_1$ or $\overline{S}$ returns to a high level (T=4). Outputs are then forced to a high-Z state.

Address lines and $\overline{E}_2$ must be valid one setup time before (TAVEL), and one hold time after (TELAX), the falling edge of $\overline{E}_1$ starting the read cycle. Before becoming valid, Q output lines become active (T=2). The Q output lines return to a high-Z state one output disable time (TE_1HQZ) after any rising edge on $\overline{E}_1$ or $\overline{S}$.

The program line remains high throughout the READ cycle.

Chip enable line $\overline{E}_1$ must remain high one minimum positive pulse width (TEHEL) before the next cycle can begin.

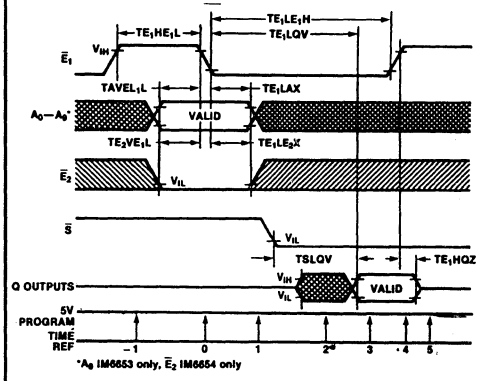

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Figure 3: Read Cycle Timing

FUNCTION TABLE

Time Ref	Inputs				Outputs Q	Notes
	$\overline{E}1$	$\overline{E}2$	$\overline{S}$	A		
–1	H	X	X	X	Z	DEVICE INACTIVE
0	↘	L	X	V	Z	CYCLE BEGINS; ADDRESSES, $\overline{E}_2$ LATCHED*
1	L	X	X	X	Z	INTERNAL OPERATIONS ONLY
2	L	X	L	X	A	OUTPUTS ACTIVE UNDER CONTROL OF $\overline{E}_1$, $\overline{S}$
3	L	X	L	X	V	OUTPUTS VALID AFTER ACCESS TIME
4	↗	X	L	X	V	READ COMPLETE
5	H	X	X	X	Z	CYCLE ENDS (SAME AS –1)

NOTE: All typical values have been characterized but are not tested.

IM6653/IM6654

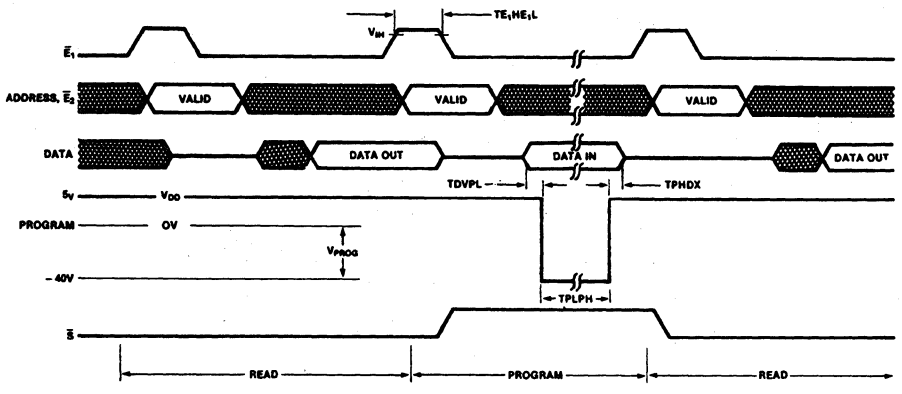


Figure 4: Read and Program Cycle Timing

DC CHARACTERISTICS FOR PROGRAMMING OPERATION

($V_{CC}=V_{DD}=5V \pm 5\%$ $V_{SS}=0V$, $T_A=25°C$)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{PROG}	Program Pin Load Current			80	100	mA
V_{PROG}	Programming Pulse Amplitude		−38	−40	−42	V
I_{CC}	V_{CC} Current			0.1	5	mA
I_{DD}	V_{DD} Current			40	100	
V_{IHA}	Address Input High Voltage		$V_{DD}-2.0$			V
V_{ILA}	Address Input Low Voltage				0.8	
V_{IH}	Data Input High Voltage		$V_{DD}-2.0$			
V_{IL}	Data Input Low Voltage				0.8	

AC CHARACTERISTICS FOR PROGRAMMING OPERATION

($V_{CC}=V_{DD}=5V \pm 5\%$ $V_{SS}=0V$, $T_A=25°$)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
TPLPH	Program Pulse Width	$t_{rise}=t_{fall}=5\mu s$	18	20	22	ms
	Program Pulse Duty Cycle				75%	
TDVPL	Data Setup Time		9			μs
TPHDX	Data Hold Time		9			
TE_1HE_1L	Strobe Pulse Width		150			ns
$TAVE_1L$	Address Setup Time		0			
TE_1LE_1X	Address Hold Time		100			
TE_1LQV	Access Time				1000	

NOTE: All typical values have been characterized but are not tested.

PROGRAM MODE OPERATION

Initially, all 4096 bits of the EPROM are in the logic one (output high) state. Selective programming of proper bit locations to "0"s is performed electrically.

In the PROGRAM mode for all EPROMs, V_{CC} and V_{DD} are tied together to a +5V operating supply. High logic levels at all of the appropriate chip inputs and outputs must be set at V_{DD} −2V minimum. Low logic levels must be set at V_{SS} +0.8V maximum. Addressing of the desired location in PROGRAM mode is done as in the READ mode. Address and data lines are set at the desired logic levels, and PROGRAM and chip select ($\overline{S}$) pins are set high. The address is latched by the downward edge on the strobe line ($\overline{E}_1$). During valid DATA IN time, the PROGRAM pin is pulsed from V_{DD} to −40V. This pulse initiates the programming of the device to the levels set on the data outputs. Duty cycle limitations are specified from chip heat dissipation considerations. PULSE RISE AND FALL TIMES MUST NOT BE FASTER THAN 5μs.

Intelligent programmer equipment with successive READ/PROGRAM/VERIFY sequences is recommended.

PROGRAMMING SYSTEM CHARACTERISTICS

1. During programming the power supply should be capable of limiting peak instantaneous current to 100mA.
2. The programming pin is driven from V_{DD} to −40 volts (±2V) by pulses of 20 milliseconds duration. These pulses should be applied in the sequence shown in the flow chart. Pulse rise and fall times of 10 microseconds are recommended. Note that any individual location may be programmed at any time.
3. Addresses and data should be presented to the device within the recommended setup/hold time and high/low logic level margins. Both "A" (10V) and non "A" EPROMs are programmed at V_{CC}, V_{DD} of 5V ±5%.
4. Programming is to be done at room temperature.

ERASING PROCEDURE

The IM6653/54 are erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537Å. The recommended integrated dose (i.e., UV intensity × exposure time) is 10W sec/cm^2. The lamps should be used without short-wave filters, and the IM6653/54 to be erased should be placed about one inch away from the lamp tubes. For best results it is recommended that the device remain inactive for 5 minutes after erasure, before reprogramming.

The erasing effect of UV light is cumulative. Care should be taken to protect EPROMs from exposure to direct sunlight or fluorescent lamps radiating UV light in the 2000Å to 4000Å range.

NOTE: All typical values have been characterized but are not tested.

IM6653/IM6654

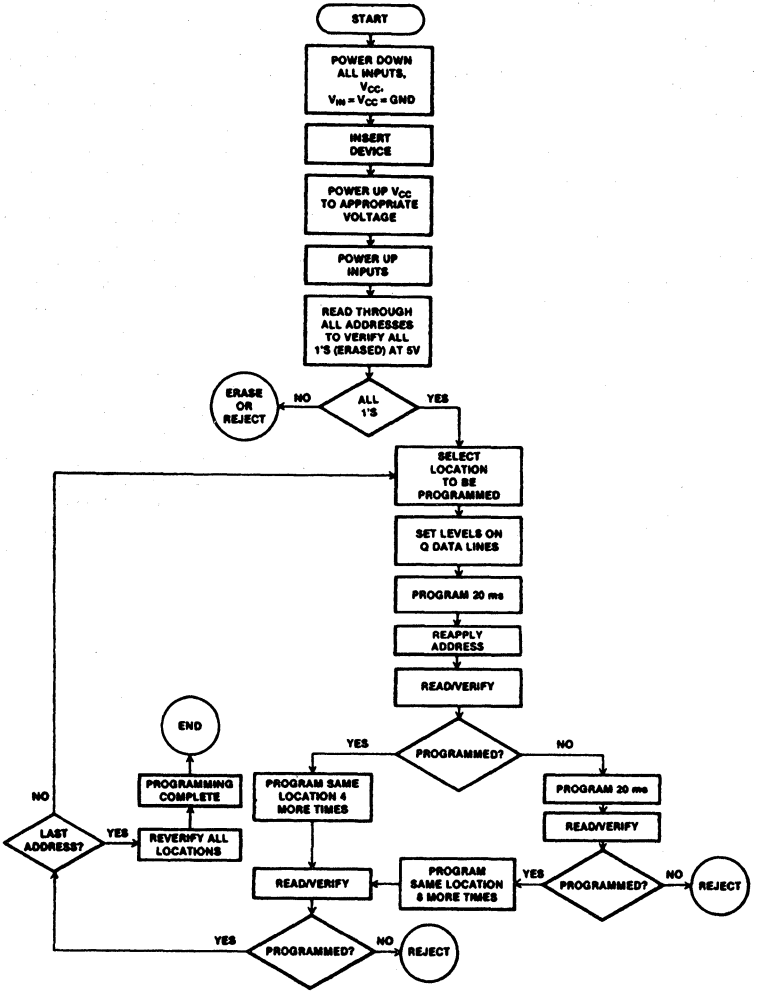


Figure 5: Programming Flow Chart

NOTE: All typical values have been characterized but are not tested.

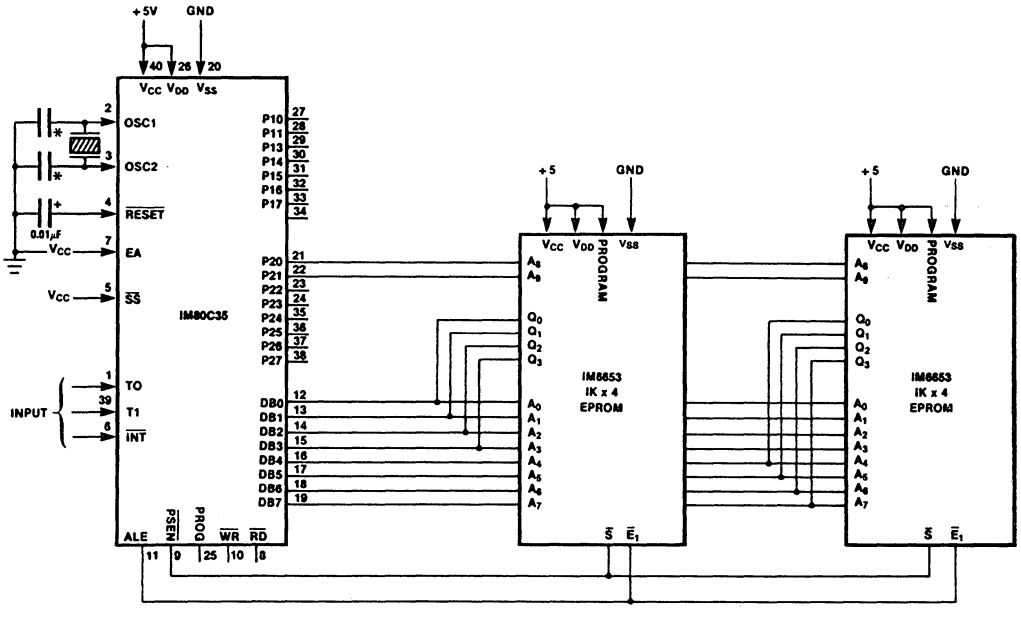


Figure 6: IM6653 CMOS EPROMS as External Program Memory with the IM80C35

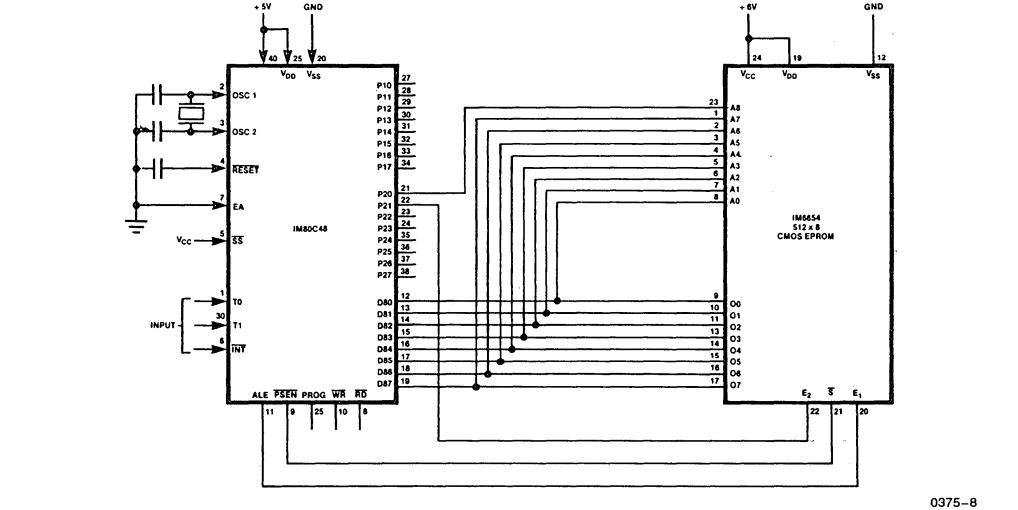


Figure 7: Using IM6654 CMOS EPROM To Extend Program Memory

14

NOTE: All typical values have been characterized but are not tested.

DATA ACQUISITION 15

PACKAGING INFORMATION

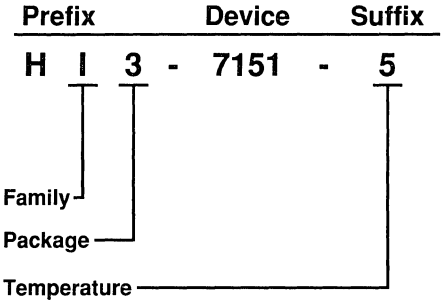
Part Number Descriptions

In December 1988, Harris acquired the General Electric Solid State division thereby adding former RCA, Intersil, and GE products to the total Harris Semiconductor portfolio. The three which apply to Data Acquisition products are shown below.

Part number descriptions are on the following pages.

HARRIS SEMICONDUCTOR PART NUMBER DESCRIPTIONS	
PART ORIGIN/GROUP	**PART NUMBER DESCRIPTION**
Harris-Origin Devices	A
RCA-Origin Devices	B
Intersil-Origin Devices	C

Part Number Description A



Family:

- A: Analog
- C: Communications
- D: Digital
- I: Interface
- M: Memory
- PL: Programmable Logic
- S: Military/Aerospace
- V: High Voltage

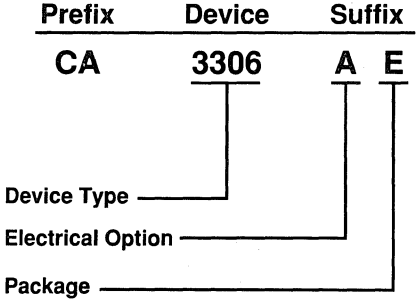
Package:

- 1: Ceramic DIP
- 1B: Brazed Seal
- 2: TO-5
- 3: Epoxy DIP
- 4: Leadless Carriers
- 4P: Plastic Leaded Chip Carrier
- 5: Ceramic Substrate
- 7: Mini DIP
- 9: Flat Pack
- 9P: Small Outline
- 0: Chip Form

Temperature:

- 1: -55°C to +200°C
- 2: -55°C to +125°C
- 4: -25°C to +85°C
- 5: 0°C to +75°C
- 6: 100% 25°C Probe (Dice Only)
- 7: 0°C to +75°C with 96 hour burn-in
- 8: Dash 8 Program; hi-rel processing with burn-in
- 9: -40°C to +85°C
- 9+: -40°C to +85°C with burn-in

Part Number Description B



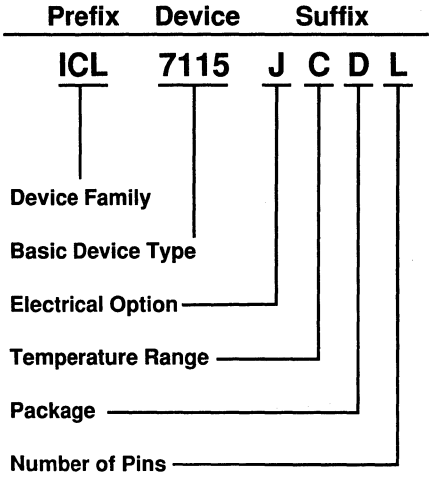
Prefix:

- CA: Linear ICs

Package:

- D: Ceramic DIP
- E: Plastic DIP
- F: CERDIP
- H: Chip
- J: 3-Layer Ceramic Leadless Chip Carrier
- K: Ceramic Flat Package
- L: Single Layer Ceramic Leadless Chip Carrier
- M: Small-Outline Plastic Package
- Q: Plastic-Chip-Carrier Package

Part Number Description C



Prefix:

- AD: Analog Devices Alternate Source
- ADC: National Semiconductor Alternate Source
- DG: Siliconix Alternate Source
- ICL: Linear IC
- ICM: Microperipheral IC
- IH: Analog Switch Family
- IM: Microcontroller IC

Temperature Range:

- C: Commercial: 0°C to 70°C
- I: Industrial: -25°C to 85°C or -40°C to 85°C (Specified on Datasheet)
- M: Military: -55°C to +125°C

Package:

- B: SOIC
- D: Ceramic (Side-Brazed) Dual-In-Line
- F: Ceramic Flat-Pack
- I: 16-Pin (.6 x .7 Pin Spacing) Hermetic Hybrid DIP
- J: CERDIP Dual-In-Line
- L: Leadless Ceramic Quad-Pack
- M: Plastic Quad-Pack (PQFP)
- P: Plastic Dual-In-Line
- S: TO-52
- T: TO-5 (Also TO-78, TO-99, TO-100)
- U: TO-72 (Also TO-18, TO-71)
- Z: TO-92
- /W: Wafer
- /D: Dice

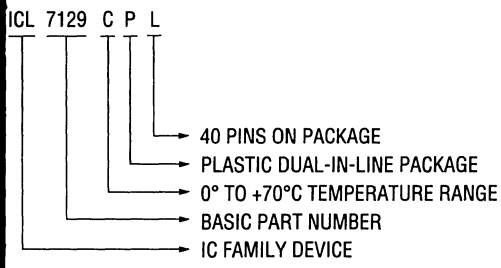
Pin-Count Designators

Suffix	Number of Pins
A	8
B	10
C	12
D	14
E	16
F	22
G	24
H	42
I	28
J	32
K	35
L	40
N	18
P	20
R	3
W	10 (0.230" pin circle, isolated case)
44	44

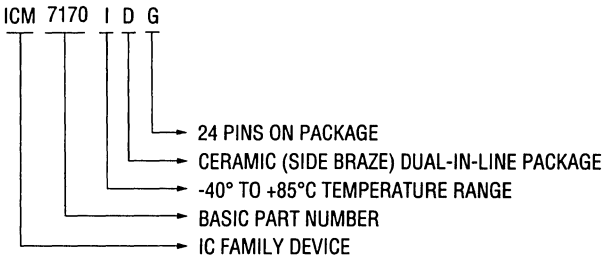
Exceptions to Package-Type Designators	
	DG (Analog Switch & MUX) Series
A	10-Pin Metal Can
L	14-Pin Flat Pack
P	Ceramic (Dual-In-Line Package (Special Order Only)
K	CERDIP
Y	SOIC
	AD (D/A Converter) Series
H	TO-52
D	CERDIP Ceramic Dual-In-Line Package
N	Epoxy Dual-In-Line Package
R	TO-92

ORDERING INFORMATION

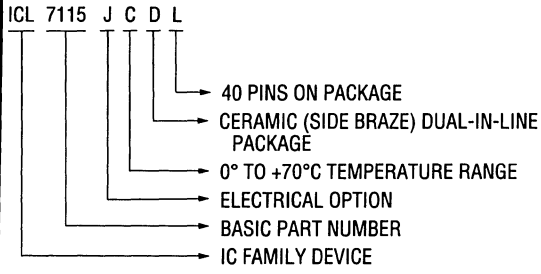
Part Number Systems Examples



Example 1



Example 2



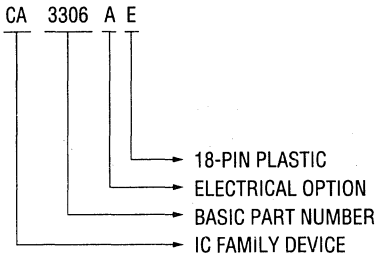
Example 3

Example 4

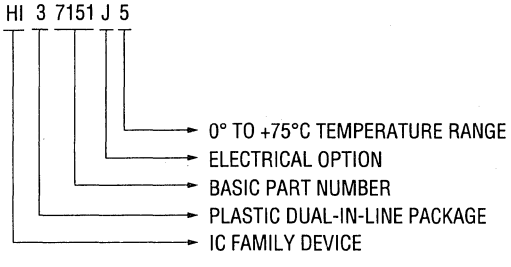
15

ORDERING INFORMATION

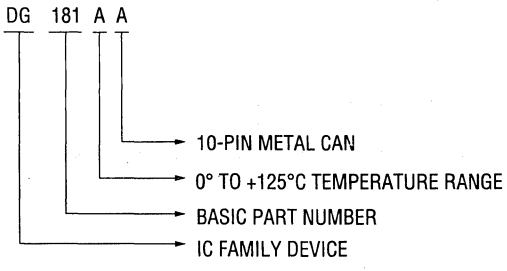
Part Number Systems Examples (Continued)



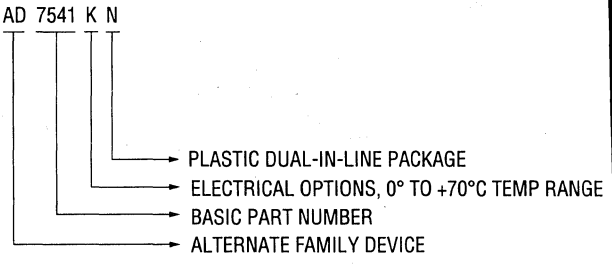
Example 5



Example 6

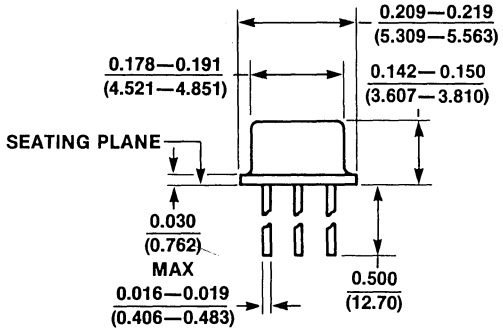


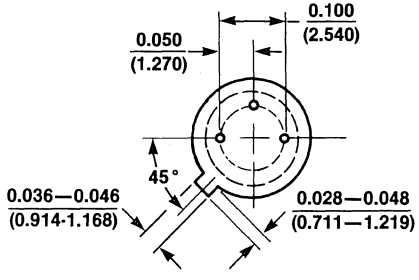
Example 7



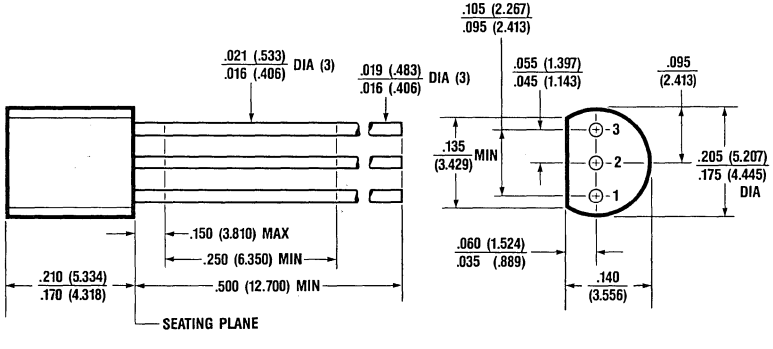
Example 8

PACKAGE OUTLINES All dimensions given in inches and (millimeters).





TO-52 (SQ*, SR)

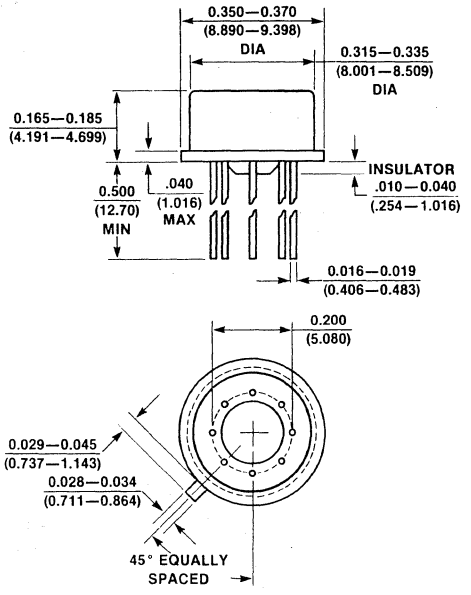


TO-92 (ZR)

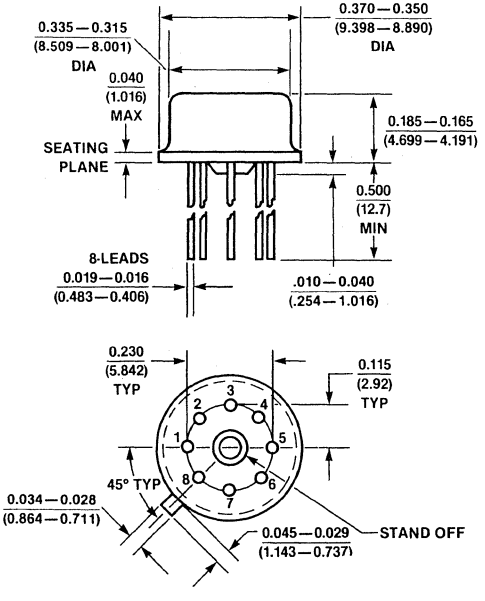
*SQ denotes a two lead package; center lead missing.

15

PACKAGE OUTLINES All dimensions given in inches and (millimeters).



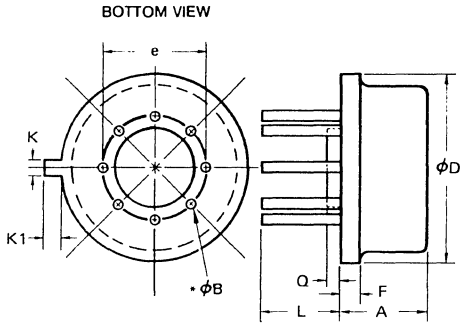
TO-99 (TV, TY)



.230 PCD TO-99 (TZ)

PACKAGE OUTLINES All dimensions given in inches and (millimeters).

Figure A

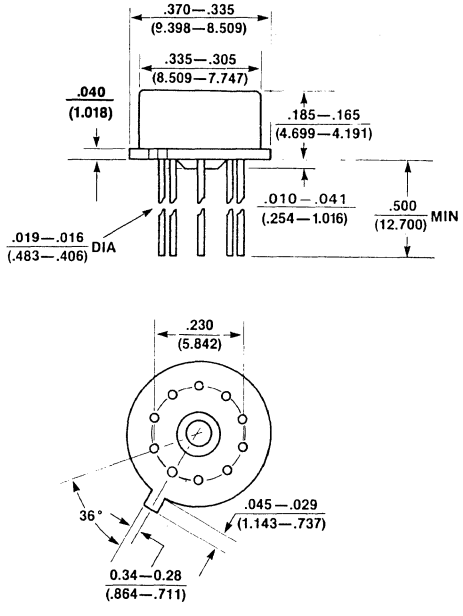


PKG. CODE	LEAD COUNT	DIM. A	DIM. ϕB	DIM. ϕD	DIM. e	DIM. F	DIM. K	DIM. K1	DIM. L	DIM. Q
X	10 TO-100	.165 / .185	.016 / .018	.345 / .365	.220 / .240	.020 / .040	.028 / .034	.028 / .040	.505 / .550	.015 / .040

TO-100 METAL CAN

* Solder dip finish add +0.003 inches.

Figure B



TO-100 (TW, TX)

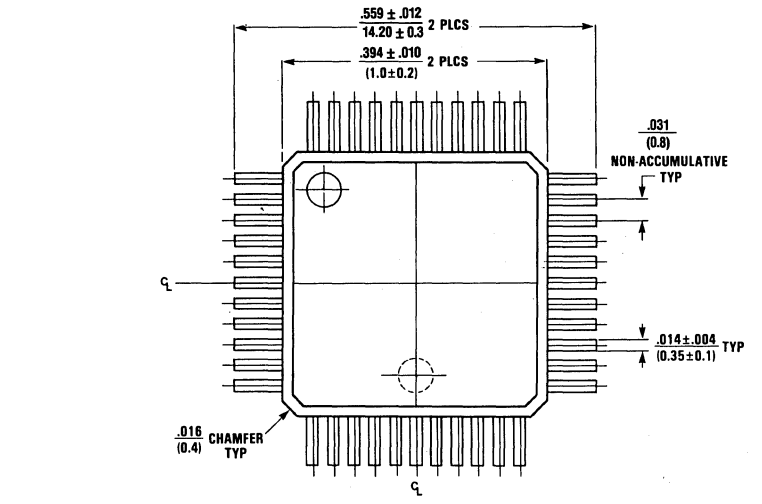
TO-100 METAL CAN LIST

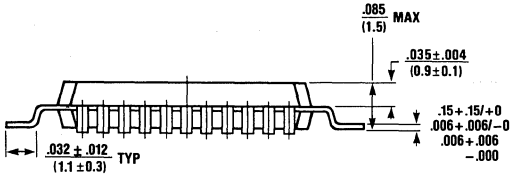
HI-200	TO-100	Figure A
HI-300	TO-100	Figure A
HI-301	TO-100	Figure A
HI-304	TO-100	Figure A
HI-305	TO-100	Figure A
HI-381	TO-100	Figure A
HI-387	TO-100	Figure A
DG180,181,182, 186,187,188	TO-100	Figure B
DG200	TO-100	Figure B
DG300-301	TO-100	Figure B
IH5341	TO-100	Figure B

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

15

PACKAGE OUTLINES All dimensions given in inches and (millimeters).





NOTES:
1. PART MUST COMPLY TO SPECIFICATION.
2. DIMENSIONS IN PARENTHESIS ARE IN MILLIMETERS.
3. PART IS SYMMETRICAL ABOUT THE CENTERLINES (℄) SHOWN.

44 LEAD PLASTIC FLATPACK (M44, PQFP)

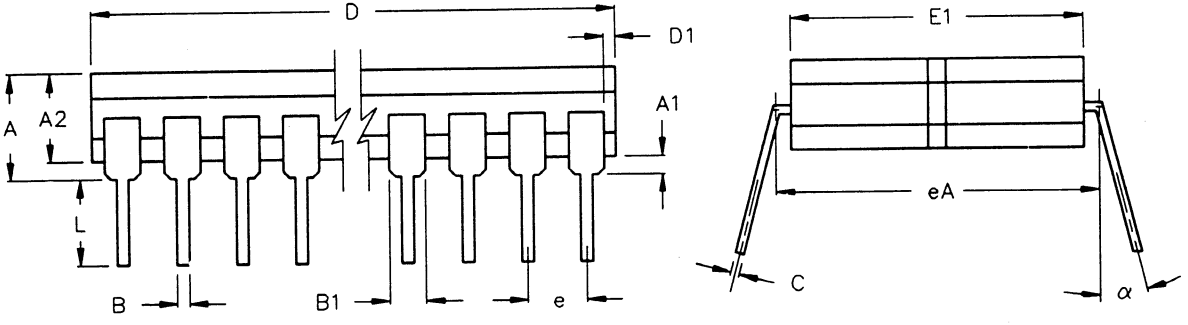
14, 16, and 20 Pin CERDIP Packages (only)

Package Designator by MSI, SSI, LSI

AD7520	MSI	16-PIN	CERDIP
AD7523	MSI	16-PIN	CERDIP
AD7530	MSI	16-PIN	CERDIP
ADC0802	MSI	20-PIN	CERDIP
ADC0803	MSI	20-PIN	CERDIP
ADC0804	MSI	20-PIN	CERDIP
DG200	LSI	14-PIN	CERDIP
DG201	LSI	16-PIN	CERDIP
DG201A	MSI	16-PIN	CERDIP
DG202	MSI	16-PIN	CERDIP
DG300	LSI	14-PIN	CERDIP
DG301	LSI	14-PIN	CERDIP
DG302	LSI	14-PIN	CERDIP
DG303	LSI	14-PIN	CERDIP
DG308A	MSI	16-PIN	CERDIP
DG309	MSI	16-PIN	CERDIP
DG508A	MSI	16-PIN	CERDIP
DG509A	MSI	16-PIN	CERDIP
HI-200	SSI	14-PIN	CERDIP
HI-201	SSI	16-PIN	CERDIP
HI-222	SSI	16-PIN	CERDIP
HI-304	SSI	14-PIN	CERDIP
HI-305	SSI	14-PIN	CERDIP
HI-306	SSI	14-PIN	CERDIP
HI-307	SSI	14-PIN	CERDIP
HI-381	SSI	14-PIN	CERDIP
HI-384	SSI	16-PIN	CERDIP
HI-387	SSI	16-PIN	CERDIP
HI-390	SSI	16-PIN	CERDIP
HI-508	SSI	16-PIN	CERDIP
HI-508A	SSI	16-PIN	CERDIP
HI-509	SSI	16-PIN	CERDIP
HI-509A	SSI	16-PIN	CERDIP
HI-539	SSI	16-PIN	CERDIP
HI-548	SSI	16-PIN	CERDIP
HI-549	SSI	16-PIN	CERDIP
HI-1818A	SSI	16-PIN	CERDIP
HI-1828A	SSI	16-PIN	CERDIP
HI-5040	SSI	16-PIN	CERDIP
HI-5041	SSI	16-PIN	CERDIP
HI-5042	SSI	16-PIN	CERDIP
HI-5043	SSI	16-PIN	CERDIP
HI-5044	SSI	16-PIN	CERDIP
HI-5045	SSI	16-PIN	CERDIP
HI-5046	SSI	16-PIN	CERDIP
HI-5046A	SSI	16-PIN	CERDIP
HI-5047	SSI	16-PIN	CERDIP
HI-5047A	SSI	16-PIN	CERDIP
HI-5048	SSI	16-PIN	CERDIP
HI-5049	SSI	16-PIN	CERDIP
HI-5050	SSI	16-PIN	CERDIP
HI-5051	SSI	16-PIN	CERDIP
HI-201HS	MSI	16-PIN	CERDIP
ICL232	MSI	16-PIN	CERDIP
ICL8052	LSI	14-PIN	CERDIP
ICL8068	LSI	14-PIN	CERDIP
ICM7207	LSI	14-PIN	CERDIP
IH5040	MSI	16-PIN	CERDIP
IH5041	MSI	16-PIN	CERDIP
IH5042	MSI	16-PIN	CERDIP
IH5043	MSI	16-PIN	CERDIP
IH5044	MSI	16-PIN	CERDIP
IH5045	MSI	16-PIN	CERDIP
IH5046	MSI	16-PIN	CERDIP
IH5047	MSI	16-PIN	CERDIP
IH5108	LSI	16-PIN	CERDIP
IH5140	MSI	16-PIN	CERDIP
IH5141	MSI	16-PIN	CERDIP
IH5142	MSI	16-PIN	CERDIP
IH5143	MSI	16-PIN	CERDIP
IH5144	MSI	16-PIN	CERDIP
IH5145	MSI	16-PIN	CERDIP
IH5148	LSI	16-PIN	CERDIP
IH5149	LSI	16-PIN	CERDIP
IH5150	LSI	16-PIN	CERDIP
IH5151	LSI	16-PIN	CERDIP
IH5208	LSI	16-PIN	CERDIP
IH5352	MSI	16-PIN	CERDIP
IH6108	MSI	16-PIN	CERDIP
IH6201	MSI	16-PIN	CERDIP
IH6208	MSI	16-PIN	CERDIP

Packaging

OUTLINE DIMENSIONS-FRIT (CERDIP) PACKAGES

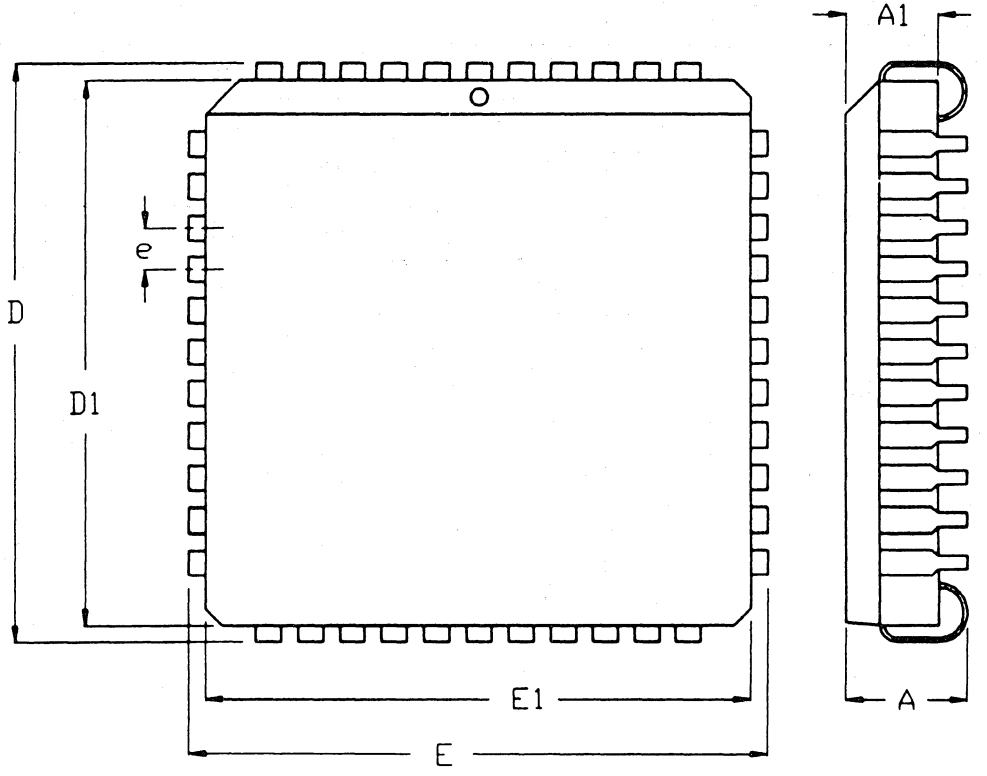


OUTLINE DIMENSIONS-FRIT (CERDIP) PACKAGES

LEADS	A	A2	B	B1	C	D	E1	e_A	e	L	D1	A1	α
8	.200 MAX	.140 .170	.015 .023	.040 .065	.008 .015	.375 .395	.245 .265	.290 .310	.100 BSC	.125 MIN	.005 MIN	.015 .060	0° 15°
14 SSI	.200 MAX	.140 .170	.015 .023	.040 .065	.008 .015	.750 .785	.245 .265	.290 .310	.100 BSC	.125 MIN	.005 MIN	.015 .060	0° 15°
14 MSI	.200 MAX	.140 .170	.015 .023	.040 .065	.008 .015	.750 .785	.265 .285	.290 .310	.100 BSC	.125 MIN	.005 MIN	.015 .060	0° 15°
14 LSI	.200 MAX	.140 .170	.015 .023	.040 .065	.008 .015	.750 .785	.285 .305	.300 .320	.100 BSC	.125 MIN	.005 MIN	.015 .060	0° 15°
16 SSI	.200 MAX	.140 .170	.015 .023	.040 .065	.008 .015	.750 .785	.245 .265	.290 .310	.100 BSC	.125 MIN	.005 MIN	.015 .060	0° 15°
16 MSI	.200 MAX	.140 .170	.015 .023	.040 .065	.008 .015	.750 .785	.265 .285	.290 .310	.100 BSC	.125 MIN	.005 MIN	.015 .060	0° 15°
16 LSI	.200 MAX	.140 .170	.015 .023	.040 .065	.008 .015	.750 .785	.285 .305	.300 .320	.100 BSC	.125 MIN	.005 MIN	.015 .060	0° 15°
18	.200 MAX	.140 .170	.015 .023	.040 .065	.008 .015	.880 .915	.285 .305	.300 .320	.100 BSC	.125 MIN	.005 MIN	.015 .060	0° 15°
20 MSI	.200 MAX	.140 .170	.015 .023	.040 .065	.008 .015	.940 1.000	.265 .285	.290 .310	.100 BSC	.125 MIN	.005 MIN	.015 .060	0° 15°
20 LSI	.200 MAX	.140 .170	.015 .023	.040 .065	.008 .015	.940 1.000	.285 .305	.300 .320	.100 BSC	.125 MIN	.005 MIN	.015 .060	0° 15°
22	.225 MAX	.150 .180	.015 .023	.040 .065	.008 .015	1.055 1.100	.375 .395	.400 .420	.100 BSC	.125 MIN	.005 MIN	.015 .060	0° 15°
24 SKNY	.200 MAX	.150 .180	.015 .023	.040 .065	.008 .015	1.240 1.280	.285 .305	.300 .320	.100 BSC	.125 MIN	.005 MIN	.015 .060	0° 15°
24	.225 MAX	.150 .180	.015 .023	.040 .065	.008 .015	1.240 1.270	.515 .535	.595 .615	.100 BSC	.125 MIN	.005 MIN	.015 .060	0° 15°
28	.225 MAX	.150 .180	.015 .023	.040 .065	.008 .015	1.440 1.480	.515 .535	.595 .615	.100 BSC	.125 MIN	.005 MIN	.015 .060	0° 15°
40	.225 MAX	.160 .200	.015 .023	.040 .065	.008 .015	2.035 2.095	.515 .535	.595 .615	.100 BSC	.125 MIN	.005 MIN	.015 .060	0° 15°

Packaging

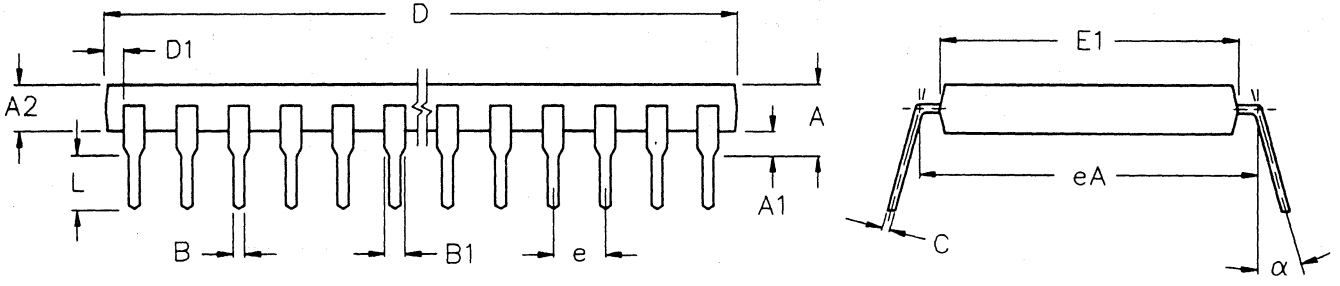
OUTLINE DIMENSIONS-PLCC (PLASTIC LEADED CHIP CARRIERS)



OUTLINE DIMENSIONS-PLCC (PLASTIC LEADED CHIP CARRIERS)

LEADS	A	A1	D	D1	E	E1	e
28	.165 .180	.090 .120	.485 .495	.450 .456	.485 .495	.450 .456	.050 .050
44	.165 .180	.090 .120	.685 .695	.650 .656	.685 .695	.650 .656	.050 .050
68	.165 .200	.090 .130	.985 .995	.950 .958	.985 .995	.950 .958	.050 .050

Packaging
OUTLINE DIMENSIONS-PLASTIC DIPS

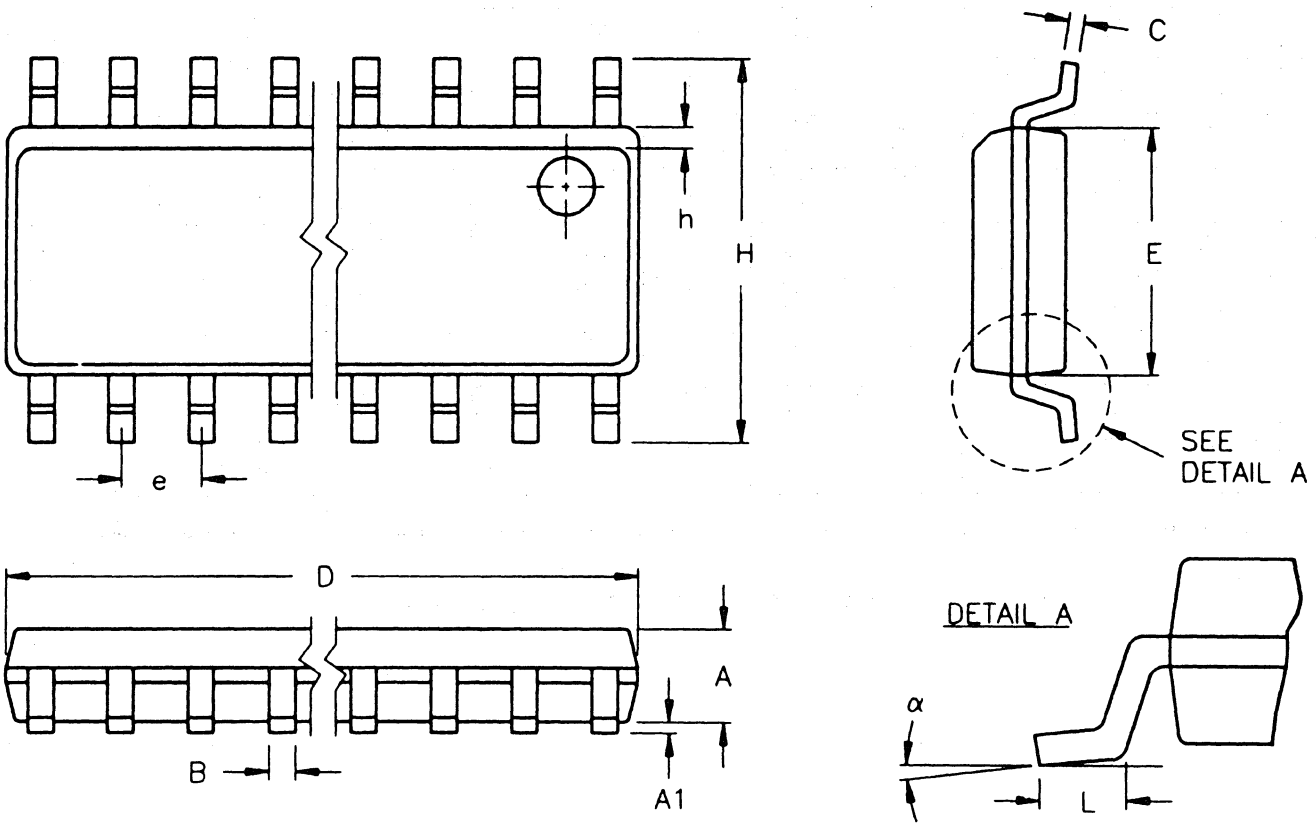


OUTLINE DIMENSIONS-PLASTIC DIPS

LEADS	A	A2	B	B1	C	D	E1	e_A	e	L	D1	A1	α
8	.200 MAX	.125 .135	.015 .022	.040 .070	.008 .015	.370 .390	.240 .260	.290 .310	.100 BSC	.115 MIN	.005 MIN	.015 MIN	0^o 15^o
14	.200 MAX	.125 .135	.015 .022	.040 .070	.008 .015	.745 .770	.240 .260	.290 .310	.100 BSC	.115 MIN	.005 MIN	.015 MIN	0^o 15^o
16	.200 MAX	.125 .135	.015 .022	.040 .070	.008 .015	.745 .770	.240 .260	.290 .310	.100 BSC	.115 MIN	.005 MIN	.015 MIN	0^o 15^o
18	.200 MAX	.125 .135	.015 .022	.040 .070	.008 .015	.845 .900	.240 .260	.290 .310	.100 BSC	.115 MIN	.005 MIN	.015 MIN	0^o 15^o
20	.200 MAX	.125 .135	.015 .022	.040 .070	.008 .015	1.010 1.040	.240 .260	.290 .310	.100 BSC	.115 MIN	.005 MIN	.015 MIN	0^o 15^o
22	.200 MAX	.145 .165	.015 .022	.040 .070	.008 .015	1.090 1.120	.335 .355	.390 .410	.100 BSC	.115 MIN	.005 MIN	.015 MIN	0^o 15^o
24 SKNY	.200 MAX	.125 .135	.015 .022	.040 .070	.008 .015	1.240 MAX	.240 .260	.290 .310	.100 BSC	.100 MIN	.005 MIN	.015 MIN	0^o 15^o
24	.225 MAX	.145 .165	.015 .022	.040 .070	.008 .015	1.240 1.270	.535 .560	.590 .610	.100 BSC	.100 .160	.005 MIN	.015 MIN	0^o 15^o
28	.225 MAX	.145 .165	.015 .022	.040 .070	.008 .015	1.440 1.470	.535 .560	.590 .610	.100 BSC	.100 .160	.005 MIN	.015 MIN	0^o 15^o
40	.225 MAX	.145 .165	.015 .022	.040 .070	.008 .015	2.030 2.070	.535 .560	.590 .610	.100 BSC	.100 .160	.005 MIN	.015 MIN	0^o 15^o

Packaging

OUTLINE DIMENSIONS-SMALL OUTLINE PACKAGES (SOP)

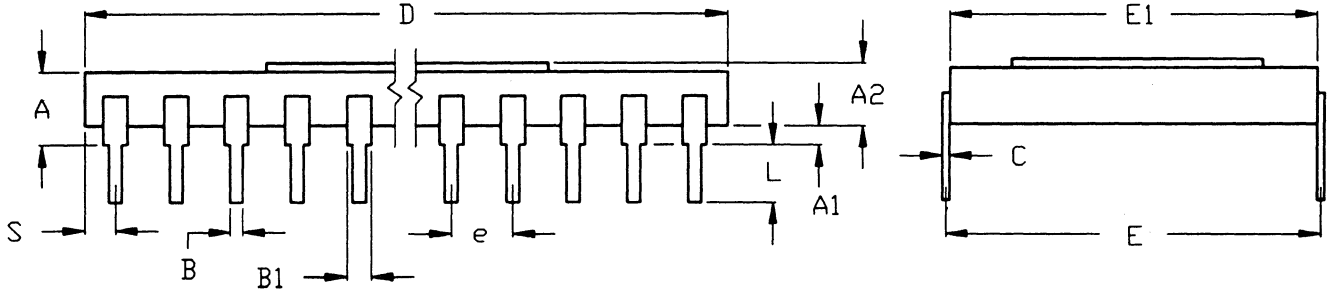


OUTLINE DIMENSIONS-SMALL OUTLINE PACKAGES (SOP)

LEADS	A	A1	B	C	D	E	e	H	h	L	α
8 (N)	.054 .068	.004 .009	.014 .019	.0075 .0098	.189 .196	.150 .157	.050 BSC	.229 .244	.010 .019	.016 .050	0° 8°
14 (N)	.054 .068	.004 .009	.014 .019	.0075 .0098	.337 .344	.150 .157	.050 BSC	.229 .244	.010 .019	.016 .050	0° 8°
16 (N)	.054 .068	.004 .009	.014 .019	.0075 .0098	.386 .393	.150 .157	.050 BSC	.229 .244	.010 .019	.016 .050	0° 8°
16 (W)	.093 .104	.004 .011	.014 .019	.0091 .0125	.398 .413	.292 .299	.050 BSC	.394 .419	.010 .029	.016 .050	0° 8°
20 (W)	.093 .104	.004 .011	.014 .019	.0091 .0125	.497 .511	.292 .299	.050 BSC	.394 .419	.010 .029	.016 .050	0° 8°
24 (W)	.093 .104	.004 .011	.014 .019	.0091 .0125	.599 .614	.292 .299	.050 BSC	.394 .419	.010 .029	.016 .050	0° 8°
28 (W)	.093 .104	.004 .011	.014 .019	.0091 .0125	.697 .712	.292 .299	.050 BSC	.394 .419	.010 .029	.016 .050	0° 8°

Packaging

OUTLINE DIMENSIONS-CERAMIC DIPS (SIDE BRAZE)

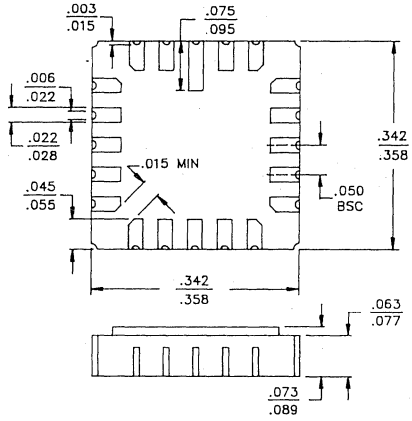


OUTLINE DIMENSIONS-CERAMIC DIPS (SIDE BRAZE)

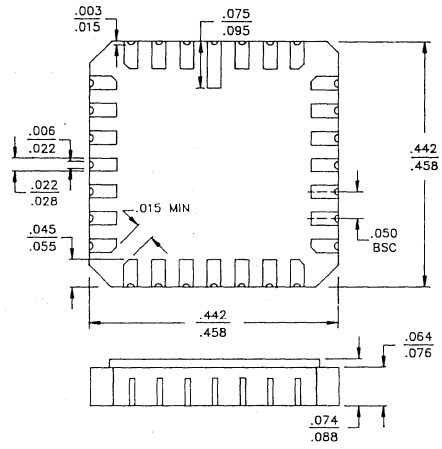
LEADS	A	A2	B	B1	C	D	E1	E	e	L	S	A1
8	.200 MAX	.080 .110	.015 .023	.040 .070	.008 .015	.380 .400	.280 .310	.290 .310	.100 BSC	.125 MIN	.055 MAX	.015 .060
14	.200 MAX	.080 .110	.015 .023	.040 .070	.008 .015	.735 .770	.280 .310	.290 .310	.100 BSC	.125 MIN	.098 MAX	.015 .060
16	.200 MAX	.080 .110	.015 .023	.040 .065	.008 .015	.790 .820	.280 .310	.290 .310	.100 BSC	.125 MIN	.080 MAX	.015 .060
18	.200 MAX	.080 .110	.015 .023	.040 .065	.008 .015	.890 .910	.280 .310	.290 .310	.100 BSC	.125 MIN	.098 MAX	.015 .060
20	.200 MAX	.080 .110	.015 .023	.040 .065	.008 .015	.990 1.010	.280 .310	.290 .310	.100 BSC	.125 MIN	.080 MAX	.015 .060
22	.200 MAX	.080 .110	.015 .023	.040 .065	.008 .015	1.060 1.090	.380 .410	.390 .420	.100 BSC	.125 MIN	.080 MAX	.015 .060
24	.225 MAX	.080 .110	.015 .023	.040 .065	.008 .015	1.185 1.215	.570 .610	.590 .620	.100 BSC	.125 MIN	.080 MAX	.015 .060
28	.225 MAX	.080 .110	.015 .023	.040 .065	.008 .015	1.385 1.415	.570 .610	.590 .620	.100 BSC	.125 MIN	.080 MAX	.015 .060
40	.225 MAX	.080 .110	.015 .023	.040 .065	.008 .015	1.980 2.020	.570 .610	.590 .620	.100 BSC	.125 MIN	.080 MAX	.015 .060

Packaging

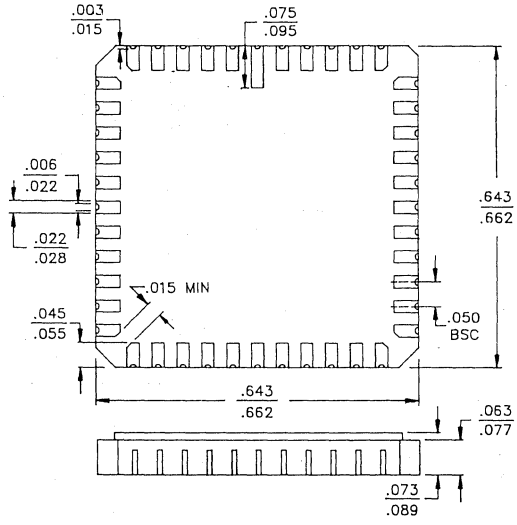
20 PAD CERAMIC LEADLESS CHIP CARRIER



28 PAD CERAMIC LEADLESS CHIP CARRIER



44 PAD CERAMIC LEADLESS CHIP CARRIER



DATA ACQUISITION 16

NEW PRODUCTS

Harris Semiconductor Data Acquisition

High Reliability/Military Specification/883B Products
Analog Switches

NUMERIC DEVICE LIST	DESCRIPTION	LDS	PKG CODE	PACKAGE
DG180AA/883B DG180AL/883B DG180AP/883B	Dual SPST Analog Switch, 10 OHM	10 14 14	L5 A2 AA	Can Flat Pack SB CerDIP
DG181AA/883B DG181AL/883B DG181AP/883B	Dual SPST Analog Switch, 30 OHM	10 14 14	L5 A2 AA	Can Flat Pack SB CerDIP
DG182AA/883B DG182AP/883B	Dual SPST Analog Switch, 75 OHM	10 14	L5 AA	Can SB CerDIP
DG183AL/883B DG183AP/883B	Dual DPST Analog Switch, 10 OHM	14 16	A2 AA	Flat Pack SB CerDIP
DG184AL/883B DG184AP/883B	Dual DPST Analog Switch, 30 OHM	14 16	A2 AA	Flat Pack SB CerDIP
DG185AP/883B	Dual DPST Analog Switch, 75 OHM	16	AA	SB CerDIP
DG186AA/883B DG186AL/883B DG186AP/883B	SPDT Analog Switch, 10 OHM	10 14 14	L5 A2 AA	Can Flat Pack SB CerDIP
DG187AA/883B DG187AL/883B DG187AP/883B	SPDT Analog Switch, 30 OHM	10 14 14	L5 A2 AA	Can Flat Pack SB CerDIP
DG188AA/883B DG188AP/883B	SPDT Analog Switch, 75 OHM	10 14	L5 AA	Can SB CerDIP
DG189AP/883B	Dual SPDT Analog Switch, 10 OHM	16	AA	SB CerDIP
DG190AL/883B DG190AP/883B	Dual SPDT Analog Switch, 30 OHM	14 16	A2 AA	Flat Pack SB CerDIP
DG191AL/883B DG191AP/883B	Dual SPDT Analog Switch, 75 OHM	14 16	A2 AA	Flat Pack SB CerDIP
DG200AA/883B DG200AK/883B	Dual SPST Analog Switch 100 OHM	10 14	L5 CY	Can CerDIP
HI1-0200/883, -8 HI2-0200/883	Dual SPST Analog Switch 80 OHM	14 10	CY NX	CerDIP Can
DG201AK/883B	Quad SPST Analog Switch, 125 OHM	16	CY	CerDIP
DG201AAK/883B	Quad SPST Analog Switch, 75 OHM	16	CY	CerDIP
HI1-0201/883, -8 HI4-0201/883	Quad SPST Analog Switch	16 20	CY CE	CerDIP LCC
HI1-0201HS/883, -8 HI4-0201HS/883, -8	Quad SPST High Speed Analog Switch	16 20	CY CE	CerDIP LCC
DG202AK/883B	Quad SPST Analog Switch 175 OHMS	16	CY	CerDIP
HI1-0222/883	Dual SPST Analog Switch 50 OHM	14	CY	CerDIP
DG300AAA/883B DG300AAK/883B	Dual SPST Analog Switch, 50 OHM	10 14	L5 CY	Can CerDIP
DG301AAA/883B DG301AAK/883B	SDPT Analog Switch, 50 OHM	10 14	L5 CY	Can CerDIP
DG302AAK/883B	Dual DPST Analog Switch, 50 OHM	14	CY	CerDIP
DG303AAK/883B	Dual SPDT Analog Switch	14	CY	CerDIP
HI1-0304/883	Dual DPST Analog Switch, 50 OHM	14	CY	CerDIP
HI1-0305/883	SDPT Analog Switch, 50 OHM	14	CY	CerDIP
HI1-0306/883	Dual DPST Analog Switch, 50 OHM	14	CY	CerDIP
DG308AAK/883B	Quad SPST Analog Switch 100 OHMS	16	CY	CerDIP
DG309AK/883B	Quad SPST Analog Switch 100 OHMS	16	CY	CerDIP
HI1-0381/883 HI2-0381/883	Dual DPST Analog Switch, 50 OHM	14 10	CY A2	CerDIP Can
HI1-0384/883	Dual DPST Analog Switch, 50 OHM	14	CY	CerDIP

High Reliability/Military Specification/883B Products
Analog Switches:Continued

NUMERIC DEVICE LIST	DESCRIPTION	LDS	PKG CODE	PACKAGE
HI1-0390/883	Dual SPDT Analog Switch 50 OHM	16	CY	CerDIP
HI1-5040/883	SPST Analog Switch 50 OHM Type	16	CY	CerDIP
HI1-5041/883, -8	Dual DPST Analog Switch, 50 OHM Type	16 20	CY CE	CerDIP LCC
HI1-5042/883	SPDT Analog Switch 50 OHM Type	16	CY	CerDIP
HI1-5043/883, -8 HI4-5043/883, -8	Dual SPDT Analog Switch	16	CY	CerDIP
IH5043MJE/883B	Dual SPDT Analog Switch 75 OHM	16 20	CY CE	CerDIP LCC
HI1-5044/883B	Double Pole Single Throw (DPST) Analog Switch 50 OHM Type	16	CY	CerDIP
HI1-5045/883 HI4-5045/883	Dual DPST Analog Switch	16 20	CY CE	CerDIP LCC
HI1-5046/883	Double Pole Double Throw (DPDT) Analog Switch 50 OHM	16	CY	CerDIP
HI1-5046A/883	Double Pole Double Throw (DPDT) Analog Switch 25 OHM	16	CY	CerDIP
HI1-5047/883	Four Pole Single Throw (4PST) Analog Switch 50 OHM	16	CY	CerDIP
HI1-5047A/883	Four Pole Single Throw (4PST) Analog Switch 25 OHM Type	16	CY	CerDIP
HI1-5048/883	Dual DPST Analog Switch, 25 OHM Type	16	CY	CerDIP
HI1-5049/883 HI4-5049/883	Dual DPST Analog Switch	16 20	CY CE	CerDIP LCC
HI1-5050/883	SPDT Analog Switch 25 OHM Type	16	CY	CerDIP
HI1-5051/883, -8 HI4-5051/883, -8	Dual SPDT Analog Switch	16 20	CY CE	Cerdip LCC
IH5012MDE/883B	4 Channel Virtual Ground FET Switch	16	AA	SB CerDIP
IH5053MDE/883B	Quad SPST Analog Switch 80 OHMS	16	CY	CerDIP
IH5140MJE/883B	SPST Analog Switch 50 OHM	16	CY	CerDIP
IH5141MJE/883B	Dual SPST Analog Switch 75 OHM	16	CY	CerDIP
IH5142MJE/883B	SPDT Analog Switch 75 OHM Type	16	CY	CerDIP
IH5143MJE/883B	Dual SPDT Analog Switch 75 OHM	16	CY	CerDIP
IH5144MJE/883B	Double Pole Single Throw (DPST) Analog Switch 75 OHM	16	CY	CerDIP
IH5145MJE/883B	Dual DPST Analog Switch 75 OHM	16	CY	CerDIP
IH5151MJE/883B	Dual SPDT Analog Switch 30 OHM	16	CY	CerDIP
IH5341MTW/883B	Dual SPST Analog Switch 75 OHM	10	TO-100	Can
IH5352MJE/883B	Quad SPST Analog Switch 75 OHM	16	CY	CerDIP
IH6201MJE/883B	Dual CMOS Driver/Translator - Drive IH401A	16	CY	CerDIP

High Reliability/Military Specification/883B Products
Ancillary Devices

NUMERIC DEVICE LIST	DESCRIPTION	LEADS	PKG CODE	PACKAGE
ICL232MJE883B	+5 VDC RS 232 Transceiver/Power Converter	16	CY	CerDIP
ICL8069CMSQ/883B	50 PPM Bandgap Voltage Reference	2	TO-52	Can
ICL8069DMSQ/883B	100 PPM Bandgap Voltage Reference	2	TO-52	Can
ICM7170AMDG/883B	Real Time Clock	24	AA	SB CerDIP
ICM7170MDG/883B	Real Time Clock	24	AA	SB CerDIP

Harris Semiconductor Data Acquisition

High Reliability/Military Specification/883B Products
Analog to Digital Converters

NUMERIC DEVICE LIST	DESCRIPTION	LDS	PKG CODE	PACKAGE
HI1-574ASD/883 HI4-574ASE/883	12 Bit 25 µSec A to D	24 44	AA CE	SB CerDIP LCC
HI1-574ATD/883 HI4-574ATE/883	12 Bit 25 µSec A to D	28 44	AA CE	SB CerDIP LCC
HI1-574AUD/883 HI4-574AUE/883	12 Bit 25 µSec A to D	28 44	AA CE	SB CerDIP LCC
HI1-674ASD/883 HI4-674ASE/883	12 Bit 12 µSec A to D	28 44	AA CE	SB CerDIP LCC
HI1-674ATD/883 HI4-674ATE/883	12 Bit 12 µSec A to D	28 44	AA CE	SB CerDIP LCC
HI1-674AUD/883 HI4-674AUE/883	12 Bit 12 µSec A to D	28 44	AA CE	SB CerDIP LCC
HI1-774S/883 HI4-774S/883	12 Bit 8 µSec A to D	28 44	AA CE	SB CerDIP LCC
HI1-774T/883 HI4-774T/883	12 Bit 8 µSec A to D	28 44	AA CE	SB CerDIP LCC
HI1-774U/883 HI4-774U/883	12 Bit 8 µSec A to D	28 44	AA CE	SB CerDIP LCC
HI1-5701T/883	6 bIT 30 MSPS Flash A to D	18	AA	SB CerDIP
ICL7109MDL/883	12 Bit 133 µSec A to D	18	AA	SB CerDIP
HI1-7153S/883	10 Bit 8 Input MUX 5 µSec A to D	40	AA	SB CerDIP

High Reliability/Military Specification/883B Products
Digital to Analog Converters

NUMERIC DEVICE LIST	DESCRIPTION	LEADS	PKG CODE	PACKAGE
AD7520SD/883B	10 Bit D to A Converter 500 nsec	16	CY	CerDIP
AD7520UD/883B	10 Bit D to A Converter 500 nsec	16	CY	CerDIP
AD7541TD/883B	12 Bit D to A Converter 1 µsec	18	CY	CerDIP
AD7545SO/883B	12 Bit D to A Converter 2 µsec	20	CY	CerDIP
HI1-565ASD/883	12 Bit D to A Converter 500 nsec w/Int Reference	20	CY	CerDIP
HI1-565ATD/883	12 Bit D to A Converter 500 nsec w/Int Reference	24	CY	CerDIP

High Reliability/Military Specification/883B Products
Display Drivers

NUMERIC DEVICE LIST	DESCRIPTION	LEADS	PKG CODE	PACKAGE
ICM7228AMJI883B	8 Digit Common Anode LED Driver	28	CY	CerDIP
ICM7228BMJI883B	8 Digit Common Cathode LED Driver	28	CY	CerDIP
ICM7228CMJI883B	8 Digit Common Anode LED Driver	28	CY	CerDIP
ICM7228DMJI883B	8 Digit Common Cathode LED Driver	28	CY	CerDIP

High Reliability/Military Specification/883B Products
Analog Multiplexers

NUMERIC DEVICE LIST	DESCRIPTION	LEADS	PKG CODE	PACKAGE
HI1-0506/883 HI4-0506/883	16 Channel Analog Multiplexer (MUX)	28 28	CY CE	CerDIP LCC
DG506AAK/883B	16 Channel Analog Multiplexer (MUX)	28	CY	
HI1-0506A-8 HI4-0506A-8	16 Channel OVP Analog Multiplexer (MUX)	28 28	CY CE	CerDIP LCC
HI1-0507/883 HI4-0507/883	Diff 8 Channel Analog Multiplexer (MUX)	28 28	CY CE	CerDIP LCC
DG507AAK/883B	Diff 8 Channel Analog Multiplexer (MUX)	28	CY	CerDIP
HI1-0507A-8 HI4-0507A-8	Diff 8 Channel OVP Analog Multiplexer (MUX)	28 28	CY CE	CerDIP LCC
HI1-0508/883 HI4-0508/883	8 Channel Analog Multiplexer (MUX)	16 20	CY CE	CerDIP LCC
DG508AAK/883B	8 Channel Analog Multiplexer (MUX)	16	CY	
HI1-0508A-8 HI4-0508A-8	8 Channel OVP Analog Multiplexer (MUX)	16 20	CY CE	CerDIP LCC
HI1-0509/883 HI4-0509/883		16 20	CY CE	CerDIP LCC
DG509AAK/883B	Dual 4 Channel Analog Multiplexer (MUX)	16	CY	CerDIP
HI1-0509A-8 HI4-0509A-8	Diff 4 Channel OVP Analog Multiplexer (MUX)	16 20	CY CE	CerDIP LCC
HI1-0516-8 HI4-0516-8	Programmable 16/Diff 8 Channel Analog Multiplexer (MUX)	28 28	CY CE	CerDIP LCC
HI1-0518-8 HI4-0518-8	Programmable 8/Diff 4 Channel Analog Multiplexer (MUX)	18 20	CY CE	CerDIP LCC
HI1-0524-8 HI4-0524-8	4 Channel Wideband Analog Multiplexer (MUX)	18 20	CY CE	CerDIP LCC
DG526AK/883B	16 Channel Analog Multiplexer (MUX)	28	CY	CerDIP
DG527AK/883B	Diff 8 Channel Analog Multiplexer (MUX)	28	CY	CerDIP
DG528AK/883B	8 Channel Analog Multiplexer (MUX)	18	CY	CerDIP
DG529AK/883B	Diff 4 Channel Analog Multiplexer (MUX)	18	CY	CerDIP
HI1-0546/883 HI4-0546/883	16 Channel 70V PK RON-Match Analog Multiplexer (MUX)	28 28	CY CE	CerDIP LCC
HI1-0547/883 HI4-0547/883	Diff 8 Channel 70V PK RON-Match Analog Multiplexer (MUX)	28 28	CY CE	CerDIP LCC
HI-0548/883 HI4-0548/883	8 Channel 70V PK RON-Match Analog Multiplexer (MUX)	16 20	CY CE	CerDIP LCC
HI1-0549/883 HI4-0549/883	Diff 4 Channel 70V PK RON-Match Analog Multiplexer (MUX)	16 20	CY CE	CerDIP LCC
HI1-1818A/883 HI4-1818A-8	8 Channel Analog Multiplexer (MUX) 400 OHM	16 20	CY CE	CerDIP LCC
HI1-1828A/883 HI4-1828A/883 HI4-1828A-8	Dual 4 Channel Analog Multiplexer (MUX) 400 OHM	16 20 20	CY CE CE	CerDIP LCC LCC
IH5108MJE/883B	8 Channel Analog Multiplexer (MUX) 1200 OHM	16	CY	CerDIP
IH5116MJI/883B	16 Channel Analog Multiplexer (MUX) 1200 OHM	28	CY	CerDIP
IH5208MJE/883B	Dual 4 Channel Analog Multiplexer (MUX) 1200 OHM	16	CY	CerDIP
IH5216MJI/883B	Dual 8 Channel Analog Multiplexer (MUX) 1200 OHM	28	CY	CerDIP
IH6108MJE/883B	8 Channel Analog Multiplexer (MUX) 350 OHM	16	CY	Cerdip
IH6208MJE/883B IH6208MFE/883B	Dual 4 Channel Analog Multiplexer (MUX) 300 OHM	16 16	CY A2	CerDIP Flat Pack

Harris Semiconductor Data Acquisition

Surface Mount Products

ALPHANUMERIC DEVICE LIST	DESCRIPTION CERAMIC LEADLESS CHIP CARRIER PACKAGES (LCC)	LEADS
CA3306CJ3	6 Bit Flash A to D Converter	20 *
CA3306J3	6 Bit Flash A to D Converter	20 *
HI4-0201/883	Quad SPST Analog Switch	20
HI4-0201HS/883	Quad SPST High Speed Analog Switch	20
HI4-0506/883, -8	16 Channel Analog Multiplexer (MUX)	28
HI4-0506A-8	16 Channel Over Voltage Protected Analog Multiplexer (MUX)	28
HI4-0507/883	Differential 8 Channel Analog Multiplexer (MUX)	28
HI4-0507A-8	Differential 8 Channel Over Voltage Protected Analog Multiplexer (MUX)	28
HI4-0508/883	8 Channel Analog Multiplexer (MUX)	20
HI4-0508A-8	8 Channel Over Voltage Protected Analog Multiplexer (MUX)	20
HI4-0509/883, -8	Differential 4 Channel Analog Multiplexer (MUX)	20
HI4-0509A-8	Differential 4 Channel Over Voltage Protected Analog Multiplexer (MUX)	20
HI4-0516-8	Programmable 16/Differential 8 Channel Analog Multiplexer (MUX)	28
HI4-0518-8	Programmable 8/Differential 4 Channel Analog Multiplexer (MUX)	20
HI4-0524-8	4 Channel Wideband Analog Multiplexer (MUX)	20
HI4-0546/883	16 Channel 70V PK RON-Match Analog Multiplexer (MUX)	28
HI4-0547/883	Differential 8 Channel 70V PK RON-Match Analog Multiplexer (MUX)	28
HI4-0548/883	8 Channel 70V PK RON-Match Analog Multiplexer (MUX)	20
HI4-0549/883	Differential 4 Channel 70V PK RON-Match Analog Multiplexer (MUX)	20
HI4-1818A/883, -8	8 Channel 400 OHM RON CMOS Level Analog Multiplexer (MUX)	20
HI4-1828A/883, -8	Differential 4 Channel 400 OHM RON CMOS Level Analog Multpilexer (MUX)	20
HI4-5043/883	Dual SPDT Analog Switch	20
HI4-5045/883	Dual DPST Analog Switch	20
HI4-5049/883	Dual DPST Analog Switch	20
HI4-5051/883	Dual SPDT Analog Switch	20
HI4-574ASE/883	12 Bit 25 µSec A to D Converter	44
HI4-574ATE/883	12 Bit 25 µSec A to D Converter	44
HI4-574AUE/883	12 Bit 25 µSec A to D Converter	44
HI4-674ASE/883	12 Bit 12 µSec A to D Converter	44
HI4-674ATE/883	12 Bit 12 µSec A to D Converter	44
HI4-674AUE/883	12 Bit 12 µSec A to D Converter	44
HI4-774S/883	12 Bit 8 µSec A to D Converter	44
HI4-774T/883	12 Bit 8 µSec A to D Converter	44
HI4-774U/883	12 Bit 8 µSec A to D Converter	44
ICL7115JMLL	14 Bit 40 µSec µProcess A to D Converter	40
ICL7115KMLL	14 Bit 40 µSec µProcess A to D Converter	40

Surface Mount Products: Continued

ALPHANUMERIC DEVICE LIST	DESCRIPTION PLASTIC SMALL OUTLINE INTEGRATED CIRCUIT (GULL-WING) (SOIC)	LEADS
CA3304AM	4 Bit Flash A to D Converter	16
CA3304M	4 Bit Flash A to D Converter	16
CA3306CM	6 Bit Flash A to D Converter	20
CA3306M	6 Bit Flash A to D Converter	20
CA3310AM	10 Bit A to D Converter with T/H	24
CA3310M	10 Bit A to D Converter with T/H	24
CA3318CM	8 Bit Flash CMOS Video Speed A to D Converter	24
CA3338AM	8 Bit CMOS Video Speed D to A Converter	16
CA3338M	8 Bit CMOS Video Speed D to A Converter	16
DG201ACY	Quad SPST Analog Switch	16
DG211CY	Quad SPST Analog Switch	16
DG212CY	Quad SPST Analog Switch	16
DG303ABY, ACY	Dual SPDT Analog Switch	16
DG308ACY	Quad SPST Analog Switch	16
DG309CY	Quad SPST Analog Switch	16
DG506ABY, ACY	Low Cost 16 Channel Analog Multiplexer (MUX)	28
DG507ABY, ACY	Low Cost Differential 8 Channel Analog Multiplexer (MUX)	28
DG508ABY, ACY	Low Cost 8 Channel Analog Multiplexer (MUX)	16
DG509ABY, ACY	Low Cost Differential 4 Channel Analog Multiplexer (MUX)	16
DG526BY, CY	16 Channel µProcess Compatible Analog Multiplexer (MUX)	28
DG527BY, CY	Differential 8 Channel µProcess Compatible Analog Multiplexer (MUX)	28
DG528CY	8 Channel µProcess Compatible Analog Multiplexer (MUX)	18
DG529CY	Differential 4 Channel µProcess Compatible Analog Multiplexer (MUX)	18
HI9P0200-5, -9	Dual SPST Analog Switch	14 *
HI9P0201-5, -9	Quad SPST Analog Switch	16
HI9P0201HS-5, -9	High Speed Quad SPST Analog Switch	16
HI9P0506-5, -9	16 Channel D.I. Analog Multiplexer (MUX)	28
HI9P0507-5, -9	Differential 8 Channel D.I. Analog Multiplexer (MUX)	28
HI9P0508-5, -9	8 Channel d.I. Analog Multiplexer (MUX)	16
HI9P0509-5, -9	Differential 4 Channel D.I. Analog Multiplexer (MUX)	16
HI9p0516-5, -9	Programmable 16/Differential 8 Channel Analog Multiplexer (MUX)	28
HI9P0546-5, -9	16 Channel RDS Match Over Voltage Protected Analog Multiplexer (MUX)	28
HI9P0547-5, -9	Differential 8 Channel Over Voltage Protected Analog Multiplexer	28
HI9P0548-5, -9	8 Channel RDS Match Over Voltage Protected Analog Multiplexer (MUX)	16
HI9P0549-5, -9	Differential 4 Channel Over Voltage Protected Analog Multiplexer	16
HI9P565AAR-9, AJR-5	12 Bit 500 NSEC D to A Converter with INT REF 1/2 LSB INL	24
HI9P565ABR-9, AKR-5	12 Bit 500 NSEC D to A Converter with INT REF 1/4 LSB INL	24
HI9P5701B-9, K-5	6 Bit 30 MSPS Flash A to D Converter	18
HI9P5043-5, -9	Dual SPDT Analog Analog Switch	16
HI9P5045-5, -9	Dual DPST Analog Analog Switch	16
HI9P5049-5, -9	Dual DPST Analog Analog Switch	16
HI9P5051-5, -9	Dual SPDT Analog Analog Switch	16
ICL232CBE, IBE	+5V RS232 Transmit/Receive with Power Converter	16
ICL8069CCBA	50 PPM Band-Gap Voltage Reference	8
ICL8069DCBA	100 PPM Band-Gap Voltage Reference	8
ICM7170AIBG	µP Compatible Real Time Clock	24
ICM7170IBG	µP Compatible Real Time Clock	24
ICM7228AIBI	8 Digit Universal Driver COM Anode	28
ICM7228BIBI	8 Digit Universal Driver COM Cathode	28

Surface Mount Products: Continued

ALPHANUMERIC DEVICE LIST	DESCRIPTION PLASTIC SMALL OUTLINE INTEGRATED CIRCUIT (GULL-WING) (SOIC)	LEADS
ICM7228CIBI	8 Digit Universal Driver COM Anode	28
ICM7228DIBI	8 Digit Universal Driver COM Cathode	28
IH5043CY	Dual SPST Video Analog Switch	16
IH5352CBP, IBP	Quad SPST Video Analog Switch	20

ALPHANUMERIC DEVICE LIST	DESCRIPTION PLASTIC LEADED CHIP CARRIER PACKAGE (J-LEAD) (PLCC)	LEADS
HI4P0201-5	Quad SPST Analog Switch	20
HI4P0201HS-5	Quad SPST HI-Speed Analog Switch	20
HI4P0222-5	200 MHZ Dual SPST Analog Switch	20
HI4P0506-5	16 Channel Analog Multiplexer (MUX)	28
HI4P0507-5	Differential 8 Channel Analog Multiplexer (MUX)	28
HI4P0508-5	8 Channel Analog Multiplexer (MUX)	20
HI4P0509-5	16 Channel Analog Multiplexer (MUX)	20
HI4P0516-5	Programmable 16/Differential 8 Channel Analog Multiplexer (MUX)	28
HI4P0518-5	Programmable 8/Differential 4 Channel Analog Multiplexer (MUX)	20
HI4P0524-5	4 Channel Video "T" Analog Multiplexer (MUX)	20
HI4P0539-5	Differential 4 Channel Low Level Analog Multiplexer (MUX)	20
HI4P0546-5	16 Channel RDS-ON Match Over Voltage Protected Analog Multiplexer (MUX)	28
HI4P0547-5	Differential 8 Channel RDS-ON Match Over Voltage Protected Analog Multiplexer (MUX)	28
HI4P0548-5	8 Channel RDS-ON Match Over Voltage Protected Analog Multiplexer (MUX)	20
HI4P0549-5	Differential 4 Channel Over Voltage Protected Analog Multiplexer (MUX)	20
HI4P1818A-5	8 Channel Analog Multiplexer (MUX)	20
HI4P1828A-5	Differential 4 Channel Analog Multiplexer (MUX)	20
HI4P5043-5	Dual SPDT Analog Switch	20
HI4P5045-5	Dual DPST Analog Switch	20
HI4P5049-5	Dual DPST 30-OHM Analog Switch	20
HI4P5051-5	Dual SPDT 30-OHM Analog Switch	20

ALPHANUMERIC DEVICE LIST	DESCRIPTION PLASTIC LEADED QUAD FLAT-PACK (GULL-WING) (PQFP)	LEADS
ICL7106CM44	3 1/2 Digit DVM LCD	44
ICL7107CM44	3 1/2 Digit DVM COM Anode LED	44
ICL7116CM44	3 1/2 Digit DISPL Hold DVM LCD	44
ICL7129CM44	4 1/2 Digit DVM LCD	44
ICL7136CM44	3 1/2 Digit Low Power DVM LCD	44
ICL7149CM44	3 3/4 Digit Autorange DMM LCD	44
ICL7182CM44	101 SEG Bar Graph DVM LCD	44
ICM7211AIM44	4 Digit Decoder Driver LCD	44
ICM7211AMIM44	4 Digit Decoder Driver LCD µp Bus	44

HARRIS

HI-5701

ADVANCED INFORMATION

September 1991

6 Bit, 30 MSPS Flash A/D Converter

Features

- 30 MSPS Conversion Rate
- No Missing Codes
- Sample and Hold Not Required
- Differential Linearity Error ..... ±0.35 LSB
- Integral Linearity Error..... ±0.5 LSB
- CMOS/TTL Compatible
- Single +5V Supply Voltage
- Low Power CMOS 250mW

Applications

- Video Digitizing
- Radar Systems
- Communication Systems
- High Speed Data Acquisition Systems

Description

The HI-5701 is a monolithic, 6 bit, CMOS flash Analog-to-Digital Converter. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 30 MSPS speed is made possible by a parallel architecture which also eliminates the need for an external sample and hold circuit. The HI-5701 delivers ±0.35 LSB differential nonlinearity while consuming only 250mW. Latched outputs are provided which present valid data to the output bus 1½ clock cycles after the convert command is received. An overflow bit is provided to allow the series connection of two converters, thus achieving 7 bit resolution.

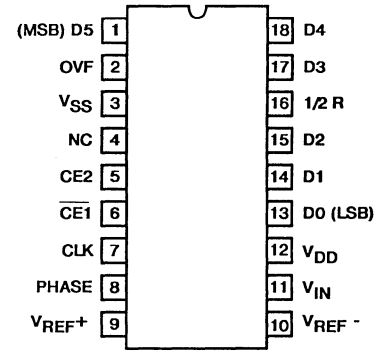
The HI-5701 is available in commercial and industrial temperature ranges. It is available in 18 pin plastic DIP and SOIC packages.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI3-5701K-5	$0^oC \leq T_A \leq +75^oC$	18 Pin Plastic DIP
HI9P-5701K-5	$0^oC \leq T_A \leq +75^oC$	18 Pin SOIC
HI3-5701B-9	$-40^oC \leq T_A \leq +85^oC$	18 Pin Plastic DIP
HI9P-5701B-5	$-40^oC \leq T_A \leq +85^oC$	18 Pin SOIC

Pinouts

18 PIN PLASTIC DIP
18 PIN SOIC
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **2937**

HARRIS

HI-7153

8-Channel 10 Bit High Speed Sampling A/D Converter

September 1991

Features

- 5μs Conversion Time
- 8-Channel Multiplexer
- 200,000 Channels/Second Throughput Rate
- Over 9 Effective Bits at 20kHz
- No Offset or Gain Adjustments Necessary
- Analog and Reference Inputs Fully Buffered
- On-Chip Track and Hold Amplifier
- μP Compatible Interface
- 2's Complement Data Output
- 150mW Power Consumption
- Only a Single 2.5V Reference Required for a ±2.5V Input Range
- Out-of-Range Flag

Applications

- μP Controlled Data Acquisition Systems
- DSP
  - ▸ Avionics
  - ▸ Sonar
- Process Control
  - ▸ Automotive Transducer Sensing
  - ▸ Industrial
- Robotics
- Digital Communications

General Description

The HI-7153 is an 8-channel high speed 10 bit A/D converter which uses a Two Step Flash algorithm to achieve through-put rates of 200kHz. The converter features an 8-channel CMOS analog multiplexer with random channel addressing. A unique switched capacitor technique allows a new input voltage to be sampled while a conversion is taking place.

Internal high speed CMOS buffers at both the analog and reference inputs simplifies interface requirements.

A Track and Hold amplifier is included on the chip, consisting of two high speed amplifiers and an internal hold capacitor, reducing external circuitry.

Microprocessor bus interfacing is simplified by the use of standard Chip Select, Read, and Write control signals. The digital three-state outputs are byte organized for bus interface to 8 or 16 bit systems. An Out-of-Range pin, together with the MSB bit, can be used to indicate an under or over-range condition.

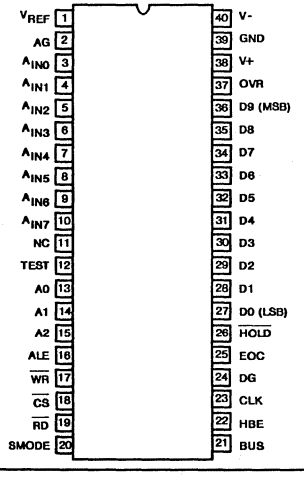
The HI-7153 operates with ±5V supplies. Only a single +2.5V reference is required to provide a bipolar input range from -2.5V to +2.5V.

Ordering Information

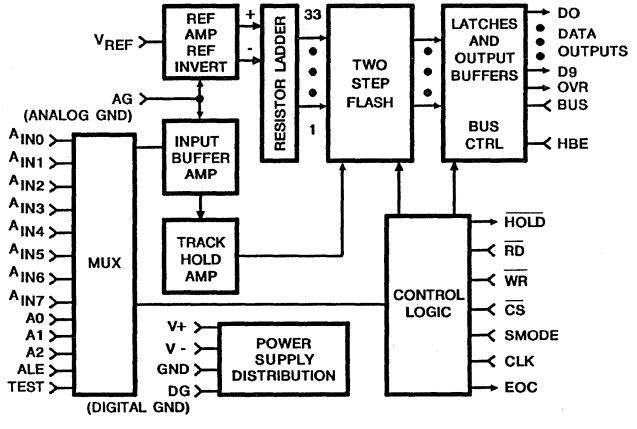
PART NO.	LINEARITY (MAX. ILE)	TEMPERATURE RANGE	PACKAGE
HI3-7153J-5	±1.0 LSB	0°C to +75°C	40 Pin Plastic DIP
HI3-7153A-9	±1.0 LSB	-40°C to +85°C	40 Pin Plastic DIP
HI1-7153S-2	±1.0 LSB	-55°C to +125°C	40 Pin Ceramic DIP
HI1-7153S/883	±1.0 LSB	-55°C to +125°C	40 Pin Ceramic DIP

Pinout

HI-7153
TOP VIEW



Functional Diagram



File Number **2787.2**

Absolute Maximum Ratings

Supply Voltage
V+ to Gnd (DG/AG/GND) ..... -0.3V < V+ <+5.7V
V- to Gnd (DG/AG/GND) ..... -5.7V < V- <+0.3V

Analog Input Pins (Note 1)
(A_{IN0}-A_{IN7}, V_{REF}) ..... V- -0.3V < V_{INA} < V+ +0.3V

Digital I/O Pins (Note 1) ..... DG -0.3V < $V_{I/O}$ < V+ +0.3V
(D0-D9, OVR, CLK, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, ALE, SMODE, $\overline{HOLD}$, EOC, HBE, BUS, A0-A2, TEST)

Power Dissipation (Note 2) 500mW
Derate above +70°C at 10mW/°C

Operating Temperature Range
HI3-7153X-5 ..... 0°C to +75°C
HI3-7153X-9 ..... -40°C to +85°C
HI1-7153X-2 ..... -55°C to +125°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (soldering, 10s) ..... 300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics (Note 4), V+ = +5V, V- = -5V, V_{REF} = +2.50V, f_{clk} = 600kHz, $t_R = t_F \leq$ 25ns, 50% duty cycle. All typical values have been characterized but are not tested.

SYMBOL	PARAMETER	(Note 3) TEMPERATURE	J, A, S GRADE MIN	J, A, S GRADE TYP	J, A, S GRADE MAX	UNITS
ACCURACY						
RES	Resolution (Note 5)	$T_A = +25°C$	10	-	-	Bits
		$T_{MIN} \leq T_A \leq T_{MAX}$	10	-	-	Bits
ILE	Integral Linearity Error	$T_A = +25°C$	-	±0.5	±1.0	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±0.75	±1.0	LSB
DLE	Differential Linearity Error	$T_A = +25°C$	-	±0.5	±1.0	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±0.75	±1.0	LSB
V_{OS}	Bipolar Offset Error	$T_A = +25°C$	-	±1.0	±2.5	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±1.5	±3.0	LSB
FSE	Unadjusted Gain Error	$T_A = +25°C$	-	±1.0	±2.5	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±1.5	±3.0	LSB
	Channel to Channel Mismatch	$T_A = +25°C$	-	±0.02	-	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±0.02	-	LSB

NOTES:
1. Input voltages may exceed the supply voltage, one input or channel at a time, provided the input current is limited to ±10mA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. See Ordering Information Table
4. FSR (Full Scale Range) = 2 x V_{REF} (5.00V at V_{REF} = 2.50V). LSB (Least Significant Bit) = FSR/1024 (4.88mV at V_{REF} = 2.50V).
5. Parameter Not tested. Parameter guaranteed by design, simulation, or characterization.

Electrical Characteristics (Continued) (Note 4), V+ = +5V, V- = -5V, V_{REF} = +2.50V, T_A = +25°C, f_{clk} = 600kHz, $t_R = t_F \leq 25$ns, 50% duty cycle. All typical values have been characterized but are not tested.

SYMBOL	PARAMETER	CONDITIONS	+25°C TYP	UNITS
DYNAMIC CHARACTERISTICS				
SNR	Signal to Noise Ratio	f_{IN} = 4.932kHz, ±2.5V	59	dB
		f_{IN} = 14.697kHz, ±2.5V	59	dB
		f_{IN} = 24.462kHz, ±2.5V	58	dB
		f_{IN} = 43.994kHz, ±2.5V	56	dB
SINAD	Signal to Noise + Distortion	f_{IN} = 4.932kHz, ±2.5V	59	dB
		f_{IN} = 14.697kHz, ±2.5V	58	dB
		f_{IN} = 24.462kHz, ±2.5V	55	dB
		f_{IN} = 43.994kHz, ±2.5V	48	dB
THD	Total Harmonic Distortion	f_{IN} = 4.932kHz, ±2.5V	-66	dBc
		f_{IN} = 14.697kHz, ±2.5V	-61	dBc
		f_{IN} = 24.462kHz, ±2.5V	-56	dBc
		f_{IN} = 43.994kHz, ±2.5V	-48	dBc
SFDR	Spurious-Free Dynamic Range	f_{IN} = 4.932kHz, ±2.5V	-76	dB
		f_{IN} = 14.697kHz, ±2.5V	-77	dB
		f_{IN} = 24.462kHz, ±2.5V	-77	dB
		f_{IN} = 43.994kHz, ±2.5V	-74	dB

DC Electrical Characteristics (Note 4), V+ = +5V, V- = -5V, V_{REF} = +2.50V, T_A = +25°C, f_{clk} = 600kHz, $t_R = t_F \leq 25$ns, 50% duty cycle, unless otherwise specified. All typical values have been characterized but are not tested.

			+25°C			0°C to +75°C		-40 to +85°C		-55 to +125°C		
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
ANALOG MULTIPLEXER INPUT												
VIR	Input Range		$-V_{REF}$	-	$+V_{REF}$	$-V_{REF}$	$+V_{REF}$	$-V_{REF}$	$+V_{REF}$	$-V_{REF}$	$+V_{REF}$	V
R_{IN}	Input Resistance		-	10	-	-						MΩ
IBI	Input Leak. Current	A_{IN} = 0V	-	0.01	100	-	100	-	100	-	100	nA
$CA_{IN(ON)}$	On Channel Input Capacitance	A_{IN} = 0V, Note 5	-	10	30	-	30	-	30	-	30	pF
$CA_{IN(OFF)}$	Off Channel Input Capacitance	A_{IN} = 0V, Note 5	-	8	20	-	20	-	20	-	20	pF
$R_{DS(ON)}$	MUX On-Resistance	A_{IN} = ±2.5V, I_{IN} = 100μA	-	1.1	2.5	-	2.5	-	2.5	-	2.5	KΩ
$\Delta R_{DS(ON)}$	Greatest Change in $R_{DS(ON)}$ Between Any Two Channels	-2.5V ≤ A_{IN} ≤ +2.5V	-	2.5	-	-	-	-	-	-	-	%
OIRR	Off-Channel Isolation	F_{IN} = 100kHz, Note 7	-	-96	-	-	-	-	-	-	-	dB
CCRR	Channel to Channel Isolation	F_{IN} = 100kHz, Note 7	-	-83	-	-	-	-	-	-	-	dB

NOTES:

4. FSR (Full Scale Range) = 2 x V_{REF} (5.00V at V_{REF} = 2.50V). LSB (Least Significant Bit) = FSR/1024 (4.88mV at V_{REF} = 2.50V).
5. Parameter Not tested. Parameter guaranteed by design, simulation, or characterization.
6. Functionality is guaranteed by negative GAIN ERROR test.
7. Channel Isolation is tested with an input signal of ±2.5Vp-p, 100kHz and the measured pin is loaded with 100Ω to GND.

DC Electrical Characteristics (Continued) (Note 4), V+ = +5V, V- = -5V, V_{REF} = +2.50V, T_A = +25°C, f_{clk} = 600kHz, $t_R = t_F \leq 25ns$, 50% duty cycle, unless otherwise specified. All typical values have been characterized but are not tested.

SYMBOL	PARAMETER	CONDITIONS	+25°C			0°C to +75°C		-40 to +85°C		-55 to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
REFERENCE INPUT												
VRR	Reference Input Range	Note 6	2.2	-	2.6	2.2	2.6	2.2	2.6	2.2	2.6	V
IBR	Reference Input Bias Current	V_{REF} = +2.50V	-	0.01	100	-	100	-	100	-	100	nA
CV_R	Reference Input Capacitance	Note 5	-	8	20	-	-	-	-	-	-	pF
LOGIC INPUTS												
V_{IH}	Input High Voltage		2.4	-	-	2.4	-	2.4	-	2.4	-	V
V_{IL}	Input Low Voltage		-	-	0.8	-	0.8	-	0.8	-	0.8	V
I_{IL}	Logic Input Current	V_{IN} = 0V, +5V	-	0.05	1	-	1	-	1	-	1	µA
C_{IN}	Input Capacitance	Note 5	-	7	17	-	-	-	-	-	-	pF
LOGIC OUTPUTS												
V_{OH}	Output High Volt.	I_{OH} = -200µA	2.4	-	-	2.4	-	2.4	-	2.4	-	V
V_{OL}	Output Low Volt.	I_{OL} = 1.6mA	-	-	0.4	-	0.4	-	0.4	-	0.4	V
I_{OL}	Output Leakage Current	$\overline{RD}$ = +5V, V_{OUT} = +5V	-	0.04	1	-	10	-	10	-	10	µA
		$\overline{RD}$ = +5V, V_{OUT} = 0V	-1	-0.01	-	-10	-	-10	-	-10	-	µA
C_{OUT}	Output Capacitance	High-Z state, Note 5	-	7	15	-	-	-	-	-	-	pF
POWER SUPPLY VOLTAGE RANGE												
V+		Func'l Operation Only, Note 6	4.5	5.0	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
V-			-4.5	-5.0	-5.5	-4.5	-5.5	-4.5	-5.5	-4.5	-5.5	V
POWER SUPPLY REJECTION												
ΔFSE	V+, V- Gain Error	V+ = 5V, V- = -4.75V, -5.25V	-	0.1	0.5	-	0.6	-	0.6	-	0.8	LSB
		V- = -5V, V+ = 4.75V, 5.25V	-	0.1	0.5	-	0.6	-	0.6	-	0.8	LSB
ΔVOS	V+, V- Offset Error	V+ = 5V, V- = -4.75V, -5.25V	-	0.15	0.5	-	0.6	-	0.6	-	0.8	LSB
		V- = -5V, V+ = 4.75V, 5.25V	-	0.15	0.5	-	0.6	-	0.6	-	0.8	LSB
SUPPLY CURRENTS												
I+	V+ Supply Current	V+ = 5V, V- = -5V V_{IN} = 0V, Digital Outputs Are Unloaded	-	20	30	-	30	-	30	-	30	mA
I-	V- Supply Current		-	-10	-15	-	-15	-	-15	-	-15	mA
IGND	GND Current		-	-8	-	-	-	-	-	-	-	mA
IDG	DG Current		-	-2	-	-	-	-	-	-	-	mA
IAG	AG Current		-	0.02	-	-	-	-	-	-	-	µA

4. FSR (Full Scale Range) = 2 x V_{REF} (5.00V at V_{REF} = 2.50V). LSB (Least Significant Bit) = FSR/1024 (4.88mV at V_{REF} = 2.50V).
5. Parameter Not tested. Parameter guaranteed by design, simulation, or characterization.
6. Functionality is guaranteed by negative GAIN ERROR test.
7. Channel Isolation is tested with an input signal of 5Vp-p, 100kHz and the measured pin is loaded with 100Ω to GND.

Electrical Characteristics (Continued) (Note 11) V+ = 5V ± 10%, V- = -5V, V_{REF} = 2.50V, T_A = +25°C, f_{clk} = 600kHz, $t_R = t_F \leq 25$ns, 50% duty cycle, C_L = 100pF (Including stray for D0-D9, OVR, $\overline{HOLD}$), unless otherwise specified. All typical values have been characterized but are not tested.

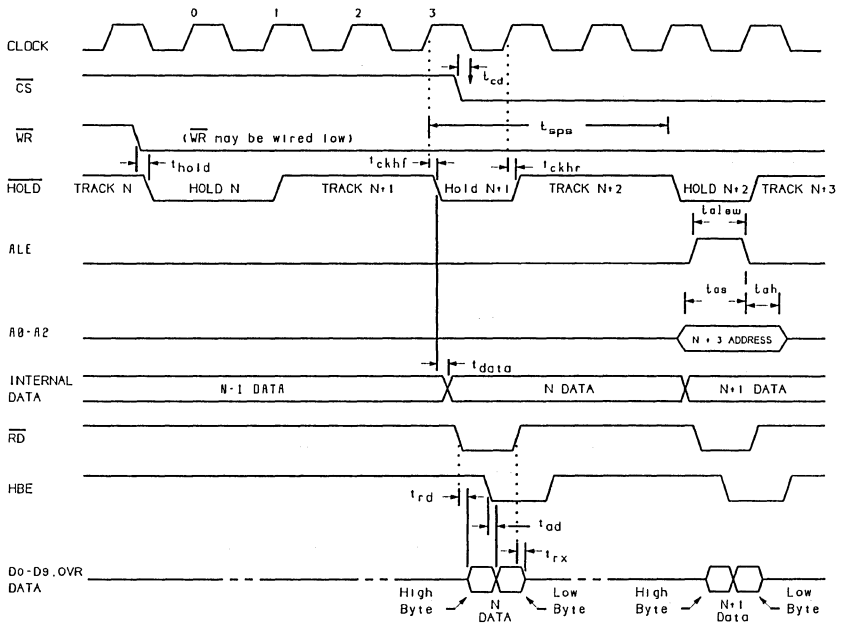
SYMBOL	PARAMETER		+25°C MIN	+25°C TYP	+25°C MAX	0°C to +75°C MIN	0°C to +75°C MAX	-40°C to +85°C MIN	-40°C to +85°C MAX	-55°C to+125°C MIN	-55°C to+125°C MAX	UNITS
TIMING CHARACTERISTICS												
t_{sps}	Continuous Conversion Time	Note 9	-	-	5	-	5	-	5	-	5	µs
		Note 5	60	-	-	60	-	60	-	60	-	µs
		Notes 9, 15	-	-	$3t_{clk}$	-	$3t_{clk}$	-	$3t_{clk}$	-	$3t_{clk}$	µs
t_{conv}	Conversion Time, First Conversion	Notes 5, 8	-	-	$4t_{clk}$+ 0.63	-	$4t_{clk}$+ 0.75	-	$4t_{clk}$+ 0.75	-	$4t_{clk}$+ 0.8	µs
t_{cyc}	Continuous Throughput	Note 9	-	-	$t_{clk}/3$	-	$t_{clk}/3$	-	$t_{clk}/3$	-	$t_{clk}/3$	CPS
t_{clk}	Clock Period		-	$1/f_{clk}$	-	-	-	-	-	-	-	-
D	Clock Input Duty Cycle	Note 5	45	50	55	45	55	45	55	45	55	%
t_{alew}	ALE Pulse Width	Note 5	30	15	-	40	-	40	-	50	-	ns
t_{as}	Address Setup Time	Note 5	40	15	-	80	-	80	-	80	-	ns
t_{ah}	Address Hold Time		0	-16	-	0	-	0	-	0	-	ns
t_{wrl}	$\overline{WR}$ Pulse Width	Notes 5,8,10	100	20	$t_{clk}/2$	100	$t_{clk}/2$	100	$t_{clk}/2$	100	$t_{clk}/2$	ns
t_{wreoc}	$\overline{WR}$ to EOC Low	Notes 5, 8	-	80	130	-	160	-	160	-	160	ns
t_{hold}	$\overline{WR}$ to $\overline{HOLD}$ Delay	Notes 5, 8	-	80	150	-	170	-	170	-	170	ns
t_{ckhr}	Clock to $\overline{HOLD}$ Rise Delay	Note 5	150	265	450	140	500	120	500	120	500	ns
t_{ckhf}	Clock to $\overline{HOLD}$ Fall Delay	Notes 5, 9	50	95	200	40	225	40	225	40	225	ns
t_{ckeoc}	Clock to EOC High	Notes 5, 8	-	460	630	-	750	-	750	-	800	ns
t_{data}	$\overline{HOLD}$ to DATA Change	Notes 5, 9	100	200	350	90	400	90	400	90	400	ns
t_{cd}	$\overline{CS}$ to DATA	Note 5	-	40	70	-	85	-	85	-	85	ns
t_{ad}	HBE to DATA	Note 5	-	30	50	-	70	-	70	-	70	ns
t_{rd}	$\overline{RD}$ LOW to Active	Notes 5, 13	-	70	100	-	125	-	125	-	125	ns
t_{rx}	$\overline{RD}$ HIGH to Inactive	Notes 5, 14	-	30	60	-	70	-	70	-	70	ns
t_r	Output Rise Time	Notes 5, 12	-	20	40	-	60	-	60	-	60	ns
t_f	Output Fall Time	Notes 5, 12	-	15	30	-	50	-	50	-	50	ns

NOTES:

8. Slow memory mode timing.
9. Fast memory or DMA mode of operation, except the first conversion which is equal to t_{CONV}.
10. Maximum specification to prevent multiple triggering with $\overline{WR}$.
11. All input drive signals are specified with $t_R = t_F \leq 10$ns and shall swing from 0.4V to 2.4V for all timing specifications. A signal is considered to change state as it crosses a 1.4V threshold (except t_{RD} & t_{RX}).
12. t_R and t_F load is C_L = 100pF (including stray capacitance) to DG and is measured from the 10%-90% point.
13. t_{RD} is the time required for the data output level to change by 10% in response to $\overline{RD}$ crossing a voltage level of 1.4V. High-Z to V_{OH} is measured with R_L = 2.5KΩ and C_L = 100pF (including stray) to DG. High-Z to V_{OL} is measured with R_L = 2.5KΩ to V+ and C_L = 100pF (including stray) to DG.
14. t_{RX} is the time required for the data output level to change by 10% in response to $\overline{RD}$ crossing a voltage level of 1.4V. V_{OH} to High-Z is measured with R_L = 2.5KΩ and C_L = 10pF (including stray) to DG. V_{OL} to High-Z is measured with R_L = 2.5KΩ to V+ and C_L = 10pF (including stray) to DG.
15. For clock frequencies other than 600kHz.

Timing Diagrams

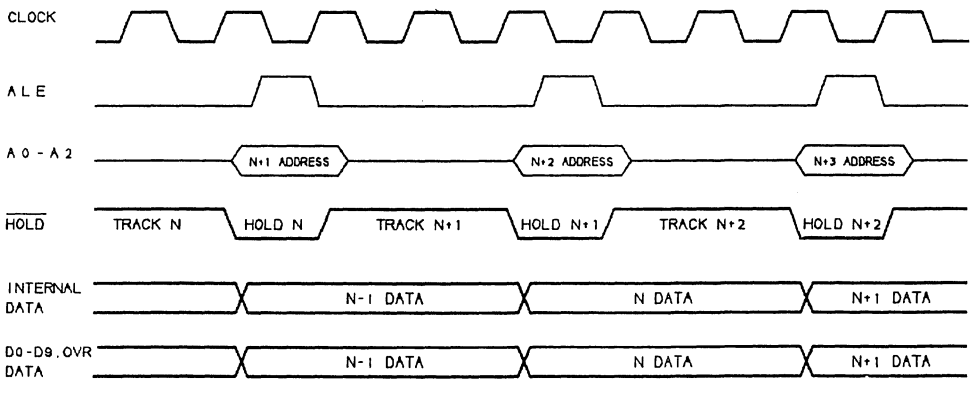
FAST MEMORY MODE (8 BIT DATA BUS)



CONDITIONS: SMODE = DG. Bus = DG.

NOTE: With SMODE = DG, the internal logic disables the output latches from being updated during a read. The EOC output is LOW continuosly.

DMA MODE (16-BIT DATA BUS)

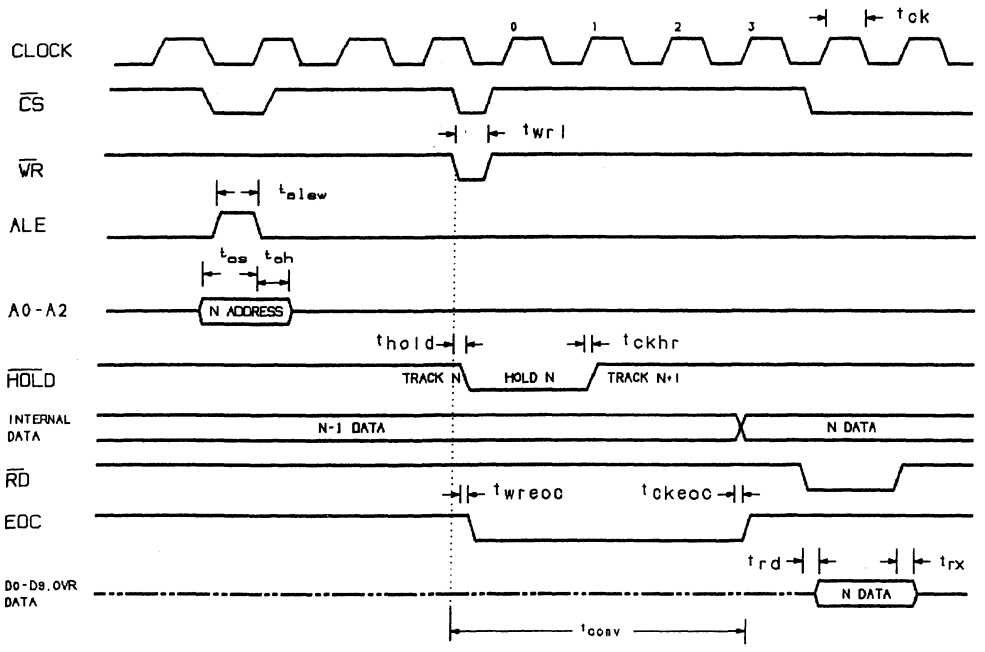


CONDITIONS: SMODE = V+, CS = WR = RD = DG, Bus = V+, HBE = DG or V+

NOTE: EOC output is low continuosly.

Timing Diagrams (Continued)

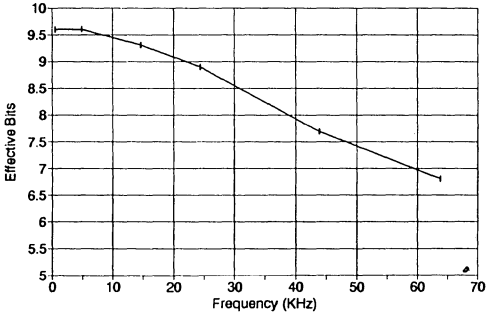
SLOW MEMORY MODE (16 BIT DATA BUS)



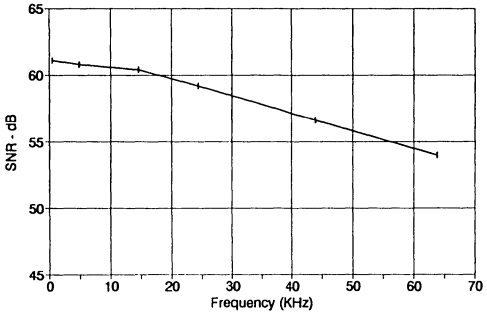
CONDITIONS: SMODE = V+, Bus = V+, HBE = DG or V+

Typical Dynamic Performance Characteristics

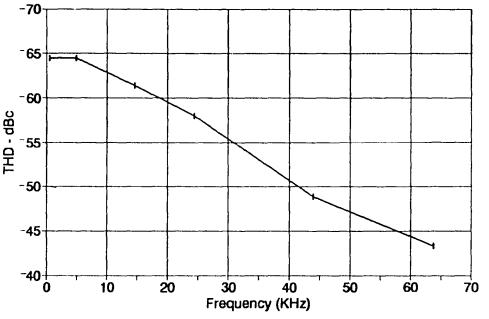
EFFECTIVE NUMBER OF BITS



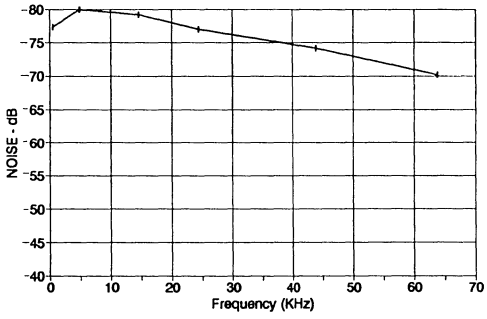
SIGNAL-TO-NOISE RATIO



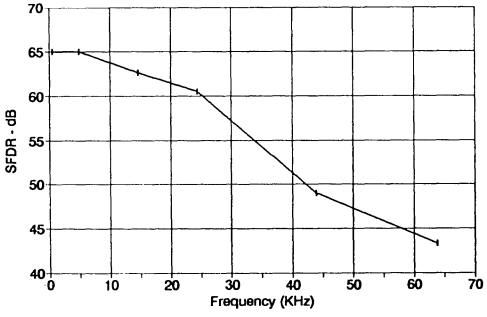
TOTAL HARMONIC DISTORTION



PEAK NOISE

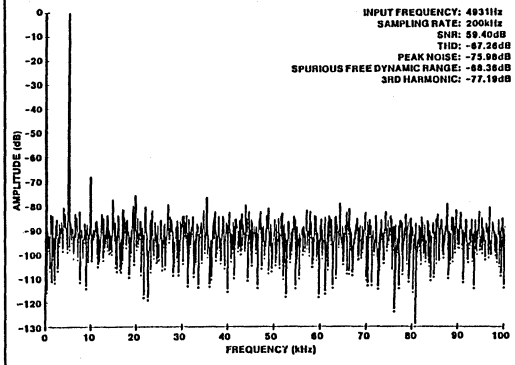


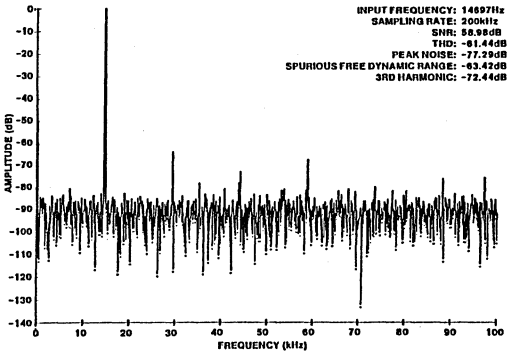
SPURIOUS-FREE DYNAMIC RANGE

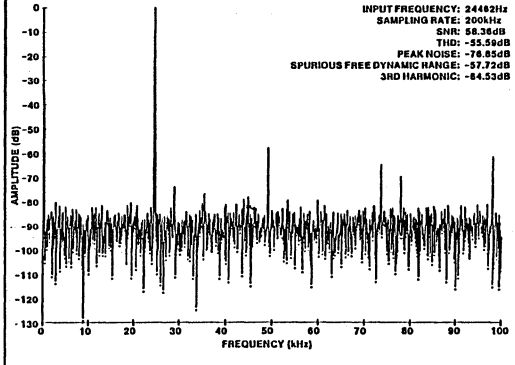


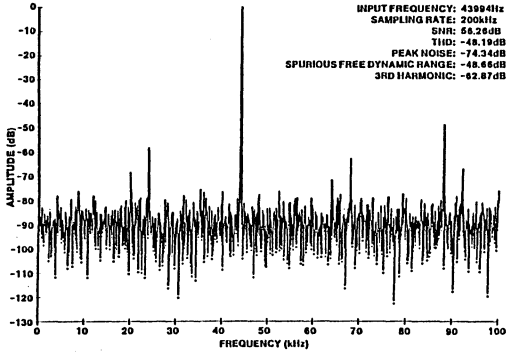
Typical Dynamic Performance Characteristics (Continued)

FFT SPECTRUMS









Pin Descriptions

PIN	SYMBOL	DESCRIPTION
1	V_{REF}	Reference voltage input (+2.50V)
2	AG	Analog ground reference (0V)
3	A_{IN0}	Analog input channel 0
4	A_{IN1}	Analog input channel 1
5	A_{IN2}	Analog input channel 2
6	A_{IN3}	Analog input channel 3
7	A_{IN4}	Analog input channel 4
8	A_{IN5}	Analog input channel 5
9	A_{IN6}	Analog input channel 6
10	A_{IN7}	Analog input channel 7
11	NC	No connect or tie to V+ only.
12	TEST	Test pin. Connect to DG for normal operation
13	A0	Mux address input. (LSB) Active high.
14	A1	Mux address input. (LSB) Active high.
15	A2	Mux address input. (MSB) Active high.
16	ALE	Mux address enable. When high, the latch is transparent. Address data is latched on the falling edge.
17	$\overline{WR}$	Write input. With CS low, starts conversion when pulsed low; continuous conversions when kept low.
18	$\overline{CS}$	Chip select input. Active low.
19	$\overline{RD}$	Read input. With CS low, enables output buffers when pulsed low; outputs updated at the end of conversion.
20	SMODE	Slow memory mode input. Active high.

PIN	SYMBOL	DESCRIPTION
21	BUS	Bus select input. High = all outputs enabled together D0-D9, OVR Low = Outputs enabled by HBE
22	HBE	Byte select (HBE/LBE) input for 8-bit bus. High = High byte select, D8 - D9, OVR Low = Low byte select, D0 - D7
23	CLK	Clock input. TTL compatible.
24	DG	Digital ground (0V)
25	EOC	End-of-conversion status. Pulses high at the end-of-conversion.
26	$\overline{HOLD}$	Start of conversion status. Pulses low at the start-of-conversion.
27	D0	Bit 0 (LSB)
28	D1	Bit 1
29	D2	Bit 2 Output
30	D3	Bit 3 Data
31	D4	Bit 4 Bits
32	D5	Bit 5 (See Table 2)
33	D6	Bit 6
34	D7	Bit 7
35	D8	Bit 8
36	D9	Bit 9 (MSB)
37	OVR	Out of Range flag. Valid at end of conversion when output exceeds full scale.
38	V+	Positive supply voltage input (+5.0V)
39	GND	Ground return for comparators (0V)
40	V-	Negative supply voltage input (-5.0V)

Detailed Description

The HI-7153 is an 8 channel high speed 10 bit A/D converter which achieves throughput rates of 200kHz by use of a Two Step Flash algorithm. A pipelined operation has been achieved through the use of switched capacitor techniques which allows the device to sample a new input voltage while a conversion is taking place. The 8-channel multiplexer can be randomly addressed. The HI-7153 requires a single reference input of +2.5V, which is internally inverted to -2.5V, thereby allowing an input range of -2.5V to +2.5V. The ten bits are two's complement coded. The analog and reference inputs are internally buffered by high speed CMOS buffers, which greatly simplifies the external analog drive requirements for the device.

Analog to Digital Section

The HI-7153 uses a conversion technique which is generally called a "Two Step Flash" algorithm. This algorithm enables very fast conversion rates without the penalty of high power dissipation or high cost. A detailed functional diagram is presented in Figure 1.

The reference input to the HI-7153 is buffered by a high speed CMOS amplifier which is used to drive one end of the resistor string. Another high speed amplifier configured in the inverting unity gain mode inverts the reference voltage with respect to analog ground and forces it onto the other end of the resistor string. Both reference amplifiers are offset trimmed during manufacturing in order to increase the accuracy of the HI-7153 and to simplify its usage.

The input voltage is first converted into a 5 bit result (plus Out of Range information) by the flash converter. This flash converter consists of an array of 33 auto-zeroed comparators which perform a comparison between the input voltage and subdivisions of the reference voltage. These subdivisions of the reference voltage are formed by forcing the reference voltage and its negative on the two ends of a string of 32 resistors.

The 5 bit result of the first flash conversion is latched into the upper five bits of double buffered latches. It is also converted back into an analog signal by choosing the ladder voltage which is closest to but less than the input voltage.

The selected voltage (VTAP) is then subtracted from the input voltage. The residual is then amplified by a factor of 32 and referenced to the negative reference voltage (VSCA = $32(V_{IN} - VTAP) + V_{REF-}$). This subtraction and amplification operation is performed by a Switched Capacitor amplifier (SCA). The output of the SCA amplifier is between the positive and negative reference voltages and can therefore be digitized by the original 5 bit flash converter (second flash conversion).

The 5 bit result of the second flash conversion is latched into the lower five bits of double buffered latches. At the end of a conversion, 10 bits of data plus an Out of Range bit are latched into the second level of latches and can then be put on the digital output pins.

The conversion takes place in three clock cycles and is illustrated in Figure 2. When the conversion begins, the track and hold goes into its hold mode for 1 clock cycle. During the first half clock cycle the comparator array is in its auto-zero mode and it samples the input voltage. During the second half clock cycle, the comparators make a comparison between the input voltage and the ladder voltages. At the beginning of the third half clock cycle, the first most significant 5-bit result becomes available. During the first clock cycle, the SCA was sampling the input voltage. After the first flash result becomes available and a ladder tap voltage has been selected the SCA amplifies the residue between the input and ladder tap voltages. During the next three half clock cycles, while the SCA output is settling to its required accuracy, the comparators go into their auto-zero mode and sample this voltage. During the sixth half clock cycle, the comparators perform another comparison whose 5 bit result becomes available on the next clock edge.

Reference Input

The reference input to the HI-7153 is buffered by a high speed CMOS amplifier. The reference input range is 2.2V to 2.6V. The reference input voltage should be applied following the application of V+ and V- supplies.

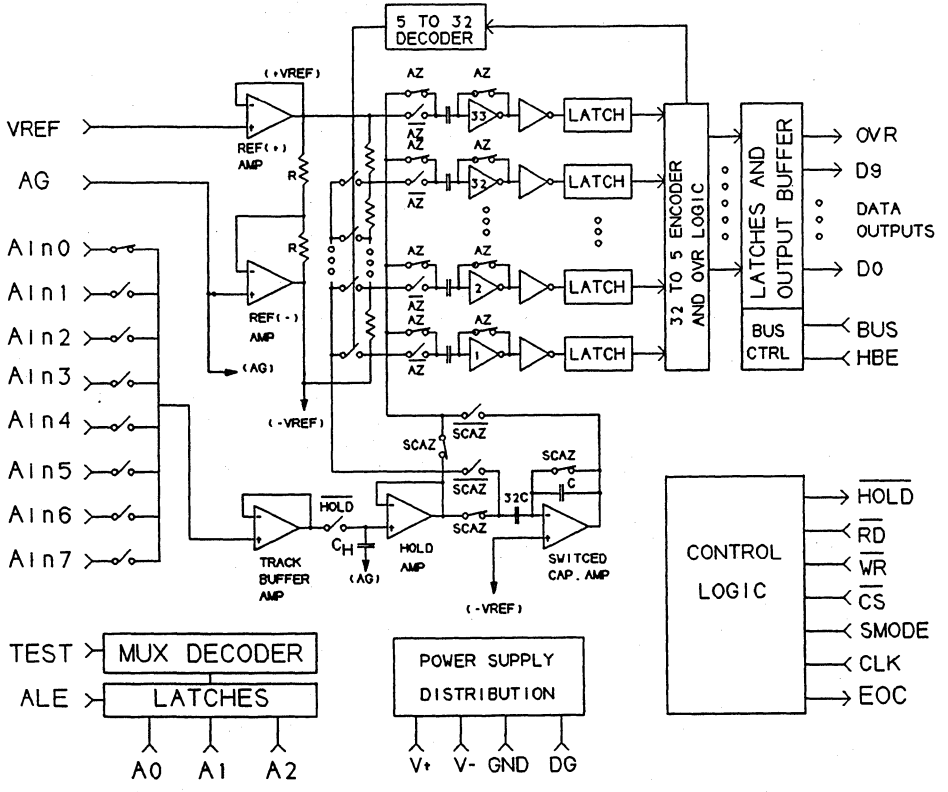


FIGURE 1. DETAILED BLOCK DIAGRAM

Analog Multiplexer

The multiplexer channel assignments are shown in Table 1 and can be randomly addressed. Address inputs A0-A2 are binary coded and are TTL/CMOS compatible. During power-up the circuit is initialized and multiplexer channel A_{IN0} is selected. The multiplexer address is transparent when ALE is high and $\overline{CS}$ is low. The address data is latched on the falling edge of the ALE signal. The multiplexer channel acquisition timing (Timing Diagrams, Slow Memory Mode) occurs approximately 500ns after the rising edge of HOLD. The multiplexer features a typical break-before-make switch action of 44ns.

Track And Hold

A Track and Hold amplifier has been fully integrated on the front end of the A/D converter. Because of the sampling nature of this A/D converter, the input is required to stay constant only during the first clock cycle. Therefore, the Track and Hold (T/H) amplifier "holds" the input voltage only during the first clock cycle and it acquires the input voltage for the next conversion during the remaining two clock cycles. The high input impedance of the T/H input amplifier simplifies analog interfacing. Input signals up to $\pm V_{REF}$ can be directly connected to the A/D without buffering. The T/H amplifier typically settles to within 1/4 LSB in 1.5µs. The A/D output code table is presented in Table 2.

The timing signals for the Track and Hold amplifier are generated internally, and are also provided externally (HOLD) for synchronization purposes.

All of the internal amplifiers are offset trimmed during manufacturing to give improved accuracy and to minimize the number of external components. If necessary, offset error can be adjusted by using digital post correction.

TABLE 1. MULTIPLEXER CHANNEL SELECTION

ADDRESS & CONTROL INPUTS					ANALOG CHANNEL SELECTED
A2	A1	A0	$\overline{CS}$	ALE	
0	0	0	0	1	A_{IN0}
0	0	1	0	1	A_{IN1}
0	1	0	0	1	A_{IN2}
0	1	1	0	1	A_{IN3}
1	0	0	0	1	A_{IN4}
1	0	1	0	1	A_{IN5}
1	1	0	0	1	A_{IN6}
1	1	1	0	1	A_{IN7}

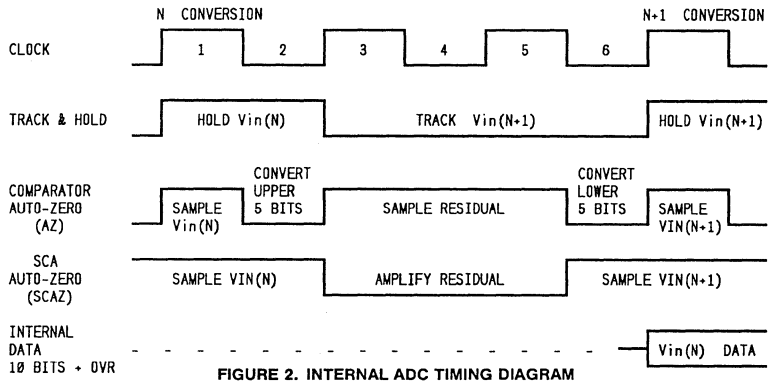


FIGURE 2. INTERNAL ADC TIMING DIAGRAM

TABLE 2. A/D OUTPUT CODE TABLE

ANALOG INPUT*		OUTPUT DATA (2'S COMPLEMENT)										
LSB = $2(V_{REF})/1024$	V_{REF} = 2.500 VOLTS	OVR	MSB 9	8	7	6	5	4	3	2	1	LSB 0
$\geq +V_{REF}$	2.500 to V+ (+OVR)	1	0	0	0	0	0	0	0	0	0	0
$+V_{REF}$-1LSB	2.49512 (+Full Scale)	0	0	1	1	1	1	1	1	1	1	1
+1LSB	0.00488	0	0	0	0	0	0	0	0	0	0	1
0	0.000	0	0	0	0	0	0	0	0	0	0	0
-1LSB	-0.00488	0	1	1	1	1	1	1	1	1	1	1
$-V_{REF}$	-2.500 (-Full Scale)	0	1	0	0	0	0	0	0	0	0	0
$\leq -V_{REF}$-1LSB	2.50488 to V- (-OVR)	1	1	0	0	0	0	0	0	0	0	0

* The voltages listed above are the ideal centers of each output code shown as a function of its associated reference voltage.

Dynamic Performance

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance for one channel of the A/D system. A low distortion sine wave is applied to the input of the A/D converter. The input is sampled by the A/D and its output stored in RAM. The data is then transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the converters dynamic performance such as SNR and THD. See typical performance characteristics.

Signal-To-Noise Ratio

The signal to noise ratio (SNR) is the measured rms signal to rms sum of noise at a specified input and sampling frequency. The noise is the rms sum of all except the fundamental and the first five harmonic signals. The SNR is dependent on the number of quantization levels used in the converter. The theoretical SNR for an N-bit converter with no differential or integral linearity error is: SNR = (6.02N + 1.76) dB. For an ideal 10 bit converter the SNR is 62dB. Differential and integral linearity errors will degrade SNR.

$$SNR = 10 \log \frac{\text{Sinewave signal power}}{\text{Total noise power}}$$

Signal-To-Noise + Distortion Ratio

SINAD is the measured rms signal to rms sum of noise plus harmonic power and is expressed by the following.

$$SINAD = 10 \log \frac{\text{Sinewave signal power}}{\text{Noise + harmonic power (2nd thru 6th)}}$$

Effective Number of Bits

The effective number of bits (ENOB) is derived from the SINAD data;

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

The total harmonic distortion (THD) is the ratio of the rms sum of the second through sixth harmonic components to the fundamental rms signal for a specified input and sampling frequency.

$$THD = 10 \log \frac{\text{Total harmonic power (2nd - 6th harmonics}}{\text{Sinewave signal power}}$$

Spurious-Free Dynamic Range

The spurious-free dynamic range (SFDR) is the ratio of the fundamental rms amplitude to the rms amplitude of the next largest spur or spectral component. It is usually determined by the largest harmonic. However, if the harmonics are buried in the noise floor it is the largest peak.

$$SFDR = 10 \log \frac{\text{Sinewave signal power}}{\text{Highest spurious signal power}}$$

Clock

The clock input is TTL compatible. The converter will function with clock inputs between 10kHz and 800kHz.

Microprocessor Interface

The HI-7153 can be interfaced to microprocessors through the use of standard Write, Read, Chip Select, and HBE control pins. The digital outputs are two's complement coded, three-state gated, and byte organized for bus interface with 8 and 16 bit systems. The digital outputs (D0 - D9, OVR) may be accessed under control of BUS, byte enable input HBE, chip select, and read inputs for a simple parallel bus interface. The microprocessor can read the current data in the output latches in typically 60ns/byte (t_{rd}). An over-range pin (OVR) together with the MSB (D9) pin set to either a logic 0 or 1 will indicate a positive or negative over-range condition respectively. All digital output buffers are capable of driving one TTL load. The multiplexer can be interfaced to either multiplexed or separate address and data bus systems.

The HI-7153 can be interfaced to a microprocessor using one of three modes: slow memory, fast memory, or DMA mode.

Slow Memory Mode

In slow memory mode, the conversion will be initiated by the microprocessor by selecting the chip ($\overline{CS}$) and pulsing $\overline{WR}$ low. This mode is selected by hardwiring the SMODE pin to V+. Note that the converter will change to the DMA interface mode if the $\overline{WR}$ to $\overline{RD}$ active timing is less than 100ns. The end-of-conversion (EOC) output signals an interrupt for the microprocessor to jump to a read subroutine at the end of conversion. When the 8-bit bus operation is selected, high and low byte data may be accessed in either order. An I/O truth table is presented in Table 3 for the slow memory mode of operation.

Fast Memory Mode

The fast memory mode of operation is selected by tying the SMODE and $\overline{WR}$ pins to DG. In this mode, the chip performs continuous conversions and only $\overline{CS}$ and $\overline{RD}$ are required to read the data. Whenever the SMODE pin is low, $\overline{WR}$ is independent of $\overline{CS}$ in starting a conversion cycle. During the first conversion cycle, $\overline{HOLD}$ follows $\overline{WR}$ going low. HOLD will be one clock period wide for subsequent conversion cycles.

Data can be read a byte at a time or all 11 bits at once. When the 8-bit bus operation is selected, high and low byte data may be accessed in either order. EOC is continuously low in this mode of operation. The conversion data can be read after $\overline{HOLD}$ has gone low. An I/O truth table is presented in Table 4 for the fast memory mode of operation.

DMA Mode

This is a hardwired mode where the HI-7153 continuously converts. The user implements hardware to store the results in memory, bypassing the microprocessor. This mode is recognized by the chip when SMODE is connected to V+ and $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ are connected to DG. When 8-bit bus operation is selected, high and low byte data may be accessed in either order. EOC is continuously low in this mode. The conversion data can be read approximately 300ns after $\overline{HOLD}$ has gone low. An I/O truth table is presented in Table 5 for the DMA mode of operation.

TABLE 3. SLOW MEMORY MODE I/O TRUTH TABLE (SMODE = V+)

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	BUS	HBE	ALE	FUNCTION
0	0	X	X	X	X	Initiates a conversion.
0	X	X	X	X	1	Selects mux channel. Address data is latched on falling edge of ALE. Latch is transparent when ALE is high.
1	X	X	X	X	X	Disables all chip commands.
0	X	0	1	X	X	Enables D0 - D9 & OVR.
0	X	0	0	0	X	Low byte enable: D0 - D7
0	X	0	0	1	X	High byte enable: D8 - D9, OVR
X	X	1	X	X	X	Disables all outputs (high impedance).

X = don't care

TABLE 4. FAST MEMORY MODE I/O TRUTH TABLE (SMODE = DG)

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	BUS	HBE	ALE	FUNCTION
0	0	X	X	X	X	Continuous conversion, WR may be tied to DG.
0	X	X	X	X	1	Selects mux channel. Address data is latched on falling edge of ALE. Latch is transparent when ALE is high.
1	X	X	X	X	X	Disables all chip commands.
0	X	0	1	X	X	Enables D0 - D9 & OVR.
0	X	0	0	0	X	Low byte enable: D0 - D7
0	X	0	0	1	X	High byte enable: D8 - D9, OVR
X	X	1	X	X	X	Disables all outputs (high impedance).

X = don't care

TABLE 5. DMA MODE I/O TRUTH TABLE (SMODE = V+, $\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = DG)

BUS	HBE	ALE	FUNCTION
X	X	1	Selects mux channel. Address data is latched on falling edge of ALE. Latch is transparent when ALE is high.
1	X	X	Enables D0 - D9 & OVR.
0	0	X	Low byte enable: D0 - D7
0	1	X	High byte enable: D8 - D9, OVR

X = don't care

Optimizing System Performance

The HI-7153 has three ground pins (AG, DG, GND) for improved system accuracy. Proper grounding and bypassing is illustrated in Figure 3. The AG pin is a ground pin and is used internally as a reference ground. The reference input and analog input should be referenced to the analog ground (AG) pin. The digital inputs and outputs should be referenced to the digital ground (DG) pin. The GND pin is a return point for the supply current of the comparator array. The comparator array is designed such that this current is approximately constant at all times and does not vary with input voltage. By virtue of the switched capacitor nature of the comparators, it is necessary to hold GND firmly at zero volts at all times. Therefore, the system ground star connection should be located as close to this pin as possible.

As in any analog system, good supply bypassing is necessary in order to achieve optimum system performance. The power supplies should be bypassed with at least a 20µF tantalum and a 0.1µF ceramic capacitor to GND. The reference input should be bypassed with a 0.1µF ceramic capacitor to AG. The capacitor leads should be as short as possible.

The pins on the HI-7153 are arranged such that the analog pins are well isolated from the digital pins. In spite of this arrangement, there is always some pin-to-pin coupling. Therefore the analog inputs to the device should not be driven from very high output impedance sources. PC board layout should screen the analog and reference inputs with guard rings on both sides of the PC board, connected to AG. Using a solder mask is good practice and helps reduce leakage due to moisture contamination on the PC board.

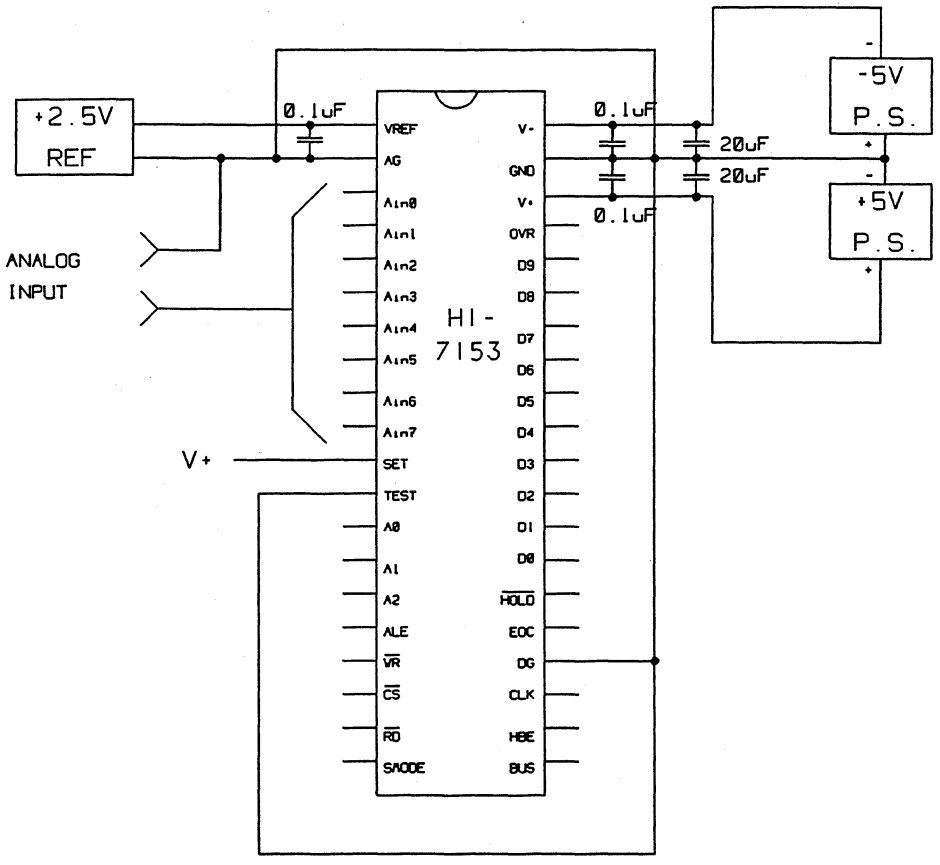


FIGURE 3. GROUND AND POWER SUPPLY DECOUPLING

Applications

Figure 4 illustrates an application where the HI-7153 is used to form a multi-channel data acquisition system. Either slow memory or fast memory modes of operation can be selected. Fast memory mode should be selected for maximum throughput. The output data is configured for 16 bit bus operation in these applications. By tying BUS to DG and connecting the HBE input to the system address decoder, the output data can be configured for 8-bit bus systems.

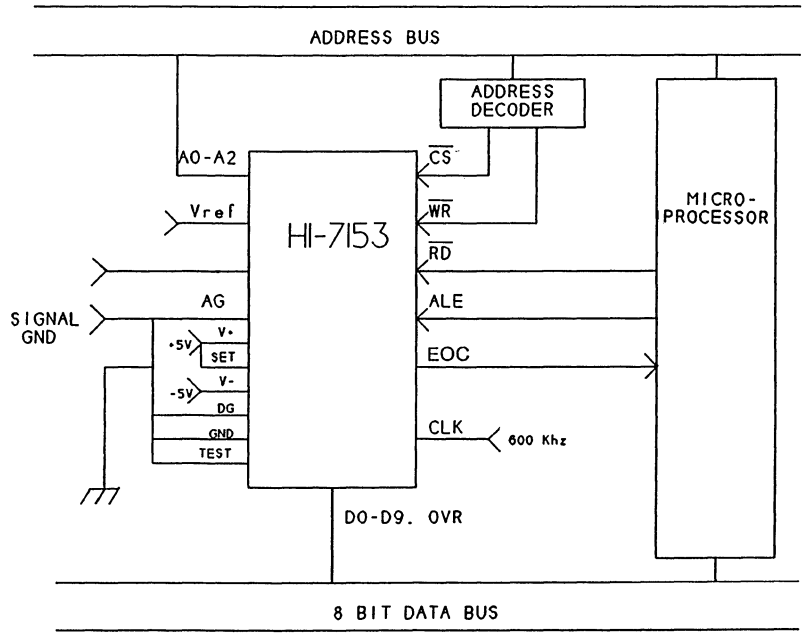


FIGURE 4. MULTI-CHANNEL DATA ACQUISITION SYSTEM

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