MOTOROLA

M68EBS(D1)

EXORbus

SPECIFICATION MANUAL

MICROSYSTEMS

M68EBS(D1)

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EXORbus

SPECIFICATION MANUAL

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CHAPTER 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

Microprocessor technology has gone through a tremendous learning curve in the recent past, and this curve has not yet peaked. As a result, some ideas which were conceived during the earliest phases of this learning curve have been modified and expanded as new developments occurred. One of the concepts that has seen significant growth is that of the microprocessor bus. Early bus designs were aimed very closely at the physical hardware design of a particular chip. As replacement devices became available, this necessitated changes in the bus architecture itself. Such a process occurred as the Motorola EXORbus evolved from the earliest forms of the MC6800 to the much more powerful MC6809 varieties.

Because of the changes that have occurred in EXORbus, and as a support to users who desire to develop new applications based on the Motorola M6800 family, it becomes necessary to document the Motorola EXORbus as it is visualized today.

The purpose of this document is not to define all of the various forms of EXORbus which have been used in the past. Rather, it is intended to provide M6800 guidelines for the development of future EXORbus modules. This does not mean that this document ignores the past. Careful consideration has been given to past design and to future needs, to develop a specification which combines maximum flexibility for the future with minimum incompatibility with the past. As a particular aid to those who are concerned with compatibility between new designs and present products, this document will give some recommendations that will minimize difficulties. Appendix E also provides material on presently-known compatibility problems and their recommended resolution.

At the same time, new designs based on this specification will have greater freedom in terms of timing differences between modules. A synchronous bus may always be viewed as a subset of a broader asynchronous bus. By defining such a view in this document, the user is allowed to use the synchronous designs of the past, and to add asynchronous higher-speed designs as need may dictate.

This increased flexibility of design should extend the life of current M6800 family-based products, and provide a continuing positive climate for future applications.

CHAPTER 2

EXORbus SIGNAL LINES

2.1 NOMENCLATURE AND ABBREVIATIONS

All abbreviations shown in Figure 2-1 and Tables 2-1 and 2-2 (as well as in the discussion) use uppercase characters with no subscript. The initial character is the letter T, followed by a six-character descriptor. This descriptor is used to identify the to/from measurement points. The first two letters of the descriptor identify the signal name. The next letter identifies the transition ending level for the measurement starting point, while the last three characters identify the signal name and transition level for the ending point. The descriptor format is illustrated in Table 2-1, while Table 2-2 lists the measurement abbreviations and the waveforms.

For full understanding of this document, certain definitions are required.

MASTER - A module capable of initiating data transfers and selecting address and direction by driving the address lines, the address validator lines, and the read/write line.

SYSTEM MASTER - The MASTER that drives the system clocking signal BE, monitors bus request and drives bus grant, and monitors refresh request and drives refresh grant.

SECONDARY MASTER - The MASTER that takes its clocking from the SYSTEM MASTER, petitions for use of the bus via bus request, and initiates data transfers only when it has been given a bus grant.

BUS MASTER - The MASTER currently driving the bus, whether SYSTEM or SECONDARY MASTER.

2.2 EXORbus CLOCKS

All systems require timing or strobe signals to specify when certain actions must occur. In synchronous systems, they are the clock signals.

In the past, EXORbus has used several different clocks. For future use, EXORbus defines one clock -- BE (BUS ENABLE). The BE clock is similar to the Phase 2 and the E clock of earlier EXORbus systems. The rising edge of BE signals the bus to begin read or write operations.

Any board designed for EXORbus may define its timing requirements in terms of four parameters. This allows maximum flexibility in the design of EXORbus modules, as well as simplifying the description of many timing constraints. To understand this clearly, consider the oscillating signal BE. The constraints imposed on this signal are:

a. The interval from one fall of BE until the next fall of BE may not exceed 10.0 microseconds. This interval is identified as TBELBEL. (See Figure 2-1).

b. BE will remain low long enough to allow the BUS MASTER to provide the required address setup time. This interval is identified as TBELBEH. (See Figure 2-1.)

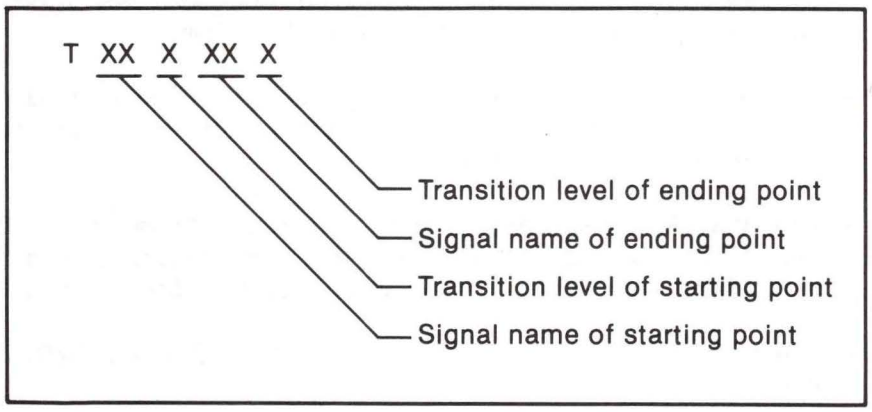
c. BE will then go high and remain high long enough for either the READ DATA or WRITE DATA setup time requirement to be met. This interval is identified as TBEHBEL. (See Figure 2-1.)

d. BE is inhibited from falling by intervention of the peripheral device. This allows a slow peripheral to extend data-access time. (See Figure 2-1.)

NOTE

The asterisk denotes an active low signal.

TABLE 2-1. Descriptor Format



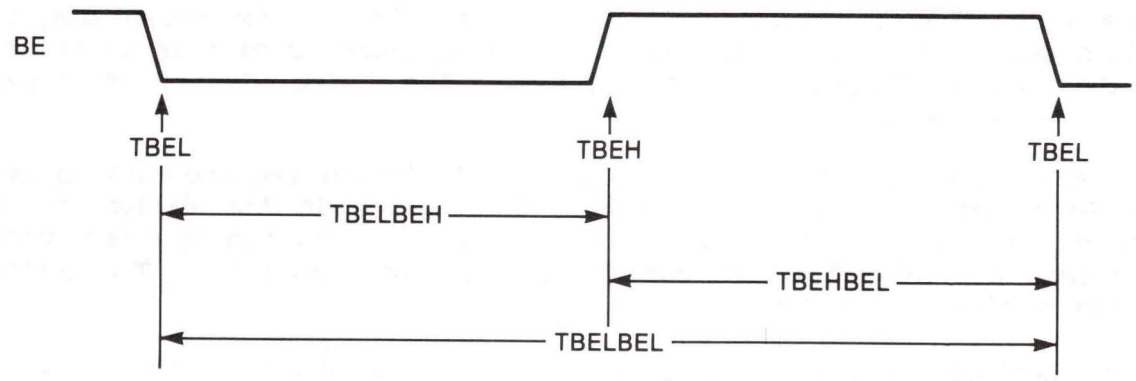


FIGURE 2-1. Time Interval Definitions

This BE signal now represents the timing edges on which all events except interrupt requests occur. By controlling this signal in such a way that each interval is minimized for the task required, the maximum system thruput is obtained. As an example, the interval for address setup (which is explained in Appendix A as TADVBEH) should be adjusted to the minimum safe interval which guarantees that the address lines are stable on the bus prior to the rise of BE. As each such interval is referenced, its optimization criteria and limits will be easily visible.

Because previous boards also used a signal called MEMCLK, it is recommended that new processor designs which need to be compatible with old peripherals also provide the signal BE on EXORbus pin L.

TABLE 2-2. Measurement Abbreviations

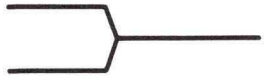
ABBREVIATIONS (Signal Names)

AD = Bus Address, R/W*, VMA, VUA, VXA
DW = Write data from MPU to peripheral module
DR = Read data from peripheral module to MPU
BE = Bus E clock signal

ABBREVIATIONS (Transition Levels)

H = Low-To-High Transition
L = High-To-Low Transition
V = Transition to Valid State
X = Transition to Invalid or Don't Care State
Z = Transition to Off (High Impedance State)

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	Must be Valid	Will be Valid
	Change from High-To-Low	Will change from High-To-Low
	Change from Low-To-High	Will change from Low-To-High
	Don't Care (Any change)	Changing State
		High Impedance (Off)

2.3 ADDRESS LINES

The address lines in the system provide the primary means by which memory and peripheral devices are accessed. These 16 address lines provide the user with 65,536 possible addresses. In addition, this address range may be extended by the use of additional signals to provide three separate address maps. The normal use of these maps is to provide one system or executive map space, a second user map space, and a third memory map. By allocating all device addresses within the system space, it is possible to protect all device activities from inadvertent misuse by applications software. This particular multi-map design is not a requirement for EXORbus compatibility, but is provided as an example for the user. See Figure 2-2.

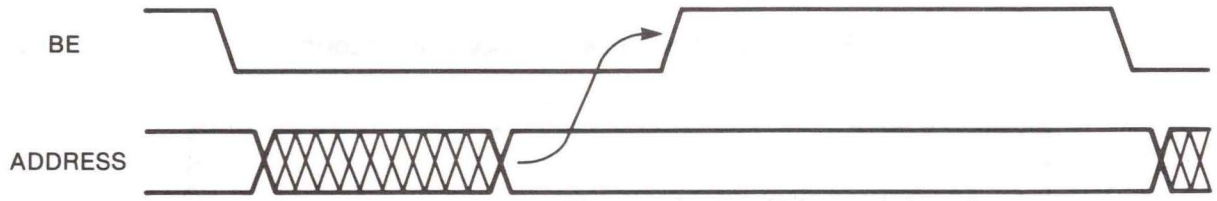


FIGURE 2-2. Address Bus Setup

2.4 DATA LINES

The data lines provide the means by which data is transferred between the various components of an EXORbus system. These eight lines provide for the transfer of one byte of information between the current BUS MASTER and the addressed device. Since the data lines are driven by three-state devices, some synchronization is necessary to ensure that no two drivers are active at the same time. This is accomplished by defining two requirements. First, no device may be active while BE is low. This provides a broad window between devices. Second, addresses must be stable for the time TADVBEH (see Appendix A) before the selected device is allowed to drive the lines. This should provide adequate decode time to guarantee that no device is still in doubt as to the validity of its address. Since each address in the system is allowed to be assigned to only one device, only one device will respond to that address. See Figure 2-3.

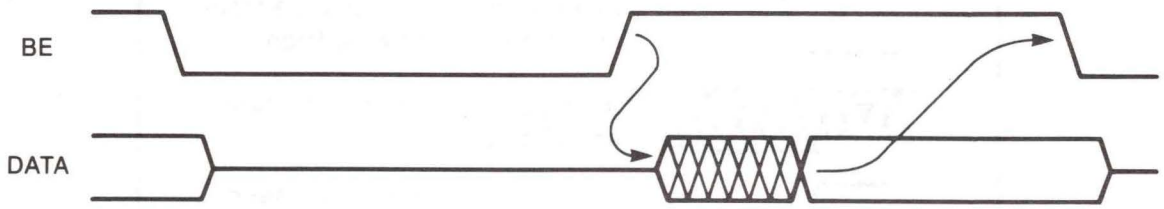


FIGURE 2-3. Data Bus Setup

2.5 CONTROL LINES

2.5.1 Interrupt Lines

Interrupts are the means by which peripheral devices notify the processor of asynchronous needs for attention. There are three major uses for interrupts.

a. The first is to inform the processor of unexpected system or device failures. Examples are bad parity in a memory board, seek failure on a disk drive, or anticipated loss of AC power.

b. The second is to request service for devices which will lose data if not serviced in some minimum time interval. One such example would be an Asynchronous Communications Interface Adapter (ACIA), which will lose data after it has received two bytes.

c. The third is to inform the system of the completion of a task which requires a long time in system terms. This eliminates the need for the system to keep polling the device and asking "Task completed?". The time saved may be utilized by the processor for other tasks.

There are three interrupt lines defined for EXORbus -- NMI*, FIRQ*, and IRQ*. Each generates an interrupt request to the processor board. These lines must be prioritized in such a way that any simultaneous detection of multiple lines will service NMI* first, FIRQ* second (see paragraph 2.5.1.2), and IRQ* last.

2.5.1.1 NMI* (Non-Maskable Interrupt). NMI* is the non-maskable interrupt. It is recommended that this signal be used only to inform the processor of emergency conditions which must be serviced immediately.

2.5.1.2 FIRQ* (Fast Interrupt Request -- M6809- and M6809E-based systems only). FIRQ* is the fast interrupt request, and should be used only for time-critical interrupts.

2.5.1.3 IRQ* (Interrupt Request). IRQ* is the normal interrupt request, and should be used for most system interrupts.

2.5.2 Data Transfer Control

The design of the EXORbus allows non-data transfer cycles to occur. In addition, the EXORbus specification provides for three unique address spaces. Several control signals have been defined to inform the peripheral devices on the bus as to the current validity and applicability of the address lines.

A legal transfer cycle is a cycle where the current BUS MASTER controls data transfers by means of the address lines, VMA, VUA, or VXA lines, and the R/W* line.

2.5.2.1 Address Validators (VMA, VUA, VXA). EXORbus provides for extensions of the basic address space defined by the 16 address lines. Auxiliary lines allow up to three separate and distinct address maps for partitioning various peripheral boards into one or more memory maps. The three address validator lines are: Valid Memory Address (VMA), Valid User Address (VUA), and Valid Executive Address (VXA).

2.5.2.1.1 VMA (Valid Memory Address) - The first of these signals is Valid Memory Address (VMA). If VMA is high at the rising edge of BE, it indicates that the address on the bus is a "valid memory address". This line should be high only during a legal transfer cycle.

2.5.2.1.2 VUA (Valid User Address) - If the device or memory in question is intended to be used only in the user map, the address validator to be used is Valid User Address (VUA). This line should be high only during a legal transfer cycle.

2.5.2.1.3 VXA (Valid Executive Address) - If the device in question is intended to be used only in the executive map, the address validator to be used is Valid Executive Address (VXA). This line should be high only during a legal transfer cycle.

2.5.2.1.4 Design Considerations - Peripheral boards, which may be used in multi-map configurations, should provide a means to select any one of the three signals -- VMA, VUA, or VXA -- as the address validator. Boards intended for only single map applications should always use VUA.

For EXORciser applications, refer to Appendix E.

2.5.2.2 R/W* (Read/Write). In addition to ensuring the validity of the address, any peripheral being addressed must know the direction of data transfer being performed. This control is provided by the Read/Write line. Driven by the current BUS MASTER, the transfer is a read if the line is high at the rise of BE, and the data will be clocked from the peripheral to the processor on the fall of BE. The transfer is a write if the line is low at the rise of BE, and the data should be valid for the peripheral to accept for the WRITE DATA setup time (TDWVBEL).

2.5.2.3 MNRDY* (Memory Not Ready). In some cases, a peripheral may not be able to react to the processor in the minimum allotted time. This is particularly true when the bus is running at its maximum specified rate of 2 MHz. The MNRDY* signal provides the ability to make the system wait on a slow device. As mentioned in the earlier discussion of clocks, the requirements on the clock circuit provide that this signal may be used to stretch the time BE remains high. Because of timing constraints in dynamic systems, this stretch time is limited to 9.5 microseconds. To avoid system difficulties, it is recommended that clock circuits be designed to override the MNRDY* signal before this time elapses. Since this means that the transfer cycle in process will not be completed, such an override should also generate a non-maskable interrupt (NMI*) to the processor. This allows the user to attempt diagnostics and/or recovery operations.

2.5.2.4 PARERR* (Parity Error). PARERR* indicates a data fetch malfunction, and could be used to generate a non-maskable interrupt (NMI*). The PARERR* signal may be generated by any peripheral which incorporates error detection. The detection of this signal and its handling should be located on the processor board. The user may choose from a variety of approaches to servicing this type of system malfunction.

2.5.3 Bus Allocation and Control

To allow multiple devices to control the bus -- whether processors or Direct Memory Access (DMA) controllers -- requires a procedure by which bus control may be transferred from one device to another. The EXORbus has two signal lines which perform this function.

2.5.3.1 BUSREQ* (Bus Request). BUSREQ* is a signal line which, when low, indicates to the SYSTEM MASTER that another device is requesting the bus. On some future falling edge of BE, the SYSTEM MASTER will release (three-state, high impedance) the address lines, VMA, VXA, and/or VUA, and R/W*. The data lines will be released as a natural consequence of BE going low, thus allowing the SECONDARY MASTER to operate the bus.

2.5.3.2 BUSGNT (Bus Grant). To inform the SECONDARY MASTER that the bus has been transferred, the SYSTEM MASTER will drive BUSGNT high after the fall of BE, but before the next rise of BE. This avoids any contention for the system control lines.

2.5.3.3 BA (Bus Available). The state of the system is indicated by the BA and BS lines. When high, BA indicates that the system is in the sync acknowledge, halt, or bus grant state. Sync acknowledge indicates that the SYSTEM MASTER is waiting for an interrupt to continue operation from a specific operating point.

2.5.3.4 BS (Bus Status -- M6809, M6809E systems only). When high, BS indicates that the system is in the halt, interrupt acknowledge, or bus grant state. Thus, the combination of BA and BS high indicates that the SYSTEM MASTER is in the halt or bus grant state. This will be the condition when the SYSTEM MASTER relinquishes control of the bus to the SECONDARY MASTER.

When the SECONDARY MASTER releases the BUSREQ* signal, the SYSTEM MASTER will take control of the bus again after the next fall of BE.

BA	BS	STATE
0	0	Normal (running)
0	1	Interrupt Acknowledge
1	0	Sync Acknowledge
1	1	Halt or Bus Grant

NOTE

If the bus request is released totally asynchronously, it is possible to have one full cycle without a device in charge of the bus. To eliminate invalid address operations, the SECONDARY MASTER must hold VMA low until BUSGNT goes low.

2.5.4 System Status and Control

The system status and control lines are those used to monitor or control major system conditions. These lines will usually involve switches or indicators, although they may also have other sources.

2.5.4.1 PWRFAIL* (Power Fail). PWRFAIL* indicates loss of AC power, and that loss of system DC power may be imminent. It is recommended that the processor board convert this signal to a non-maskable interrupt. It may also be used by memory boards to trigger conversion to standby power. This signal may be generated on any one peripheral board of the user's choice, or by the system power supply.

2.5.4.2 HALT* (System Halt). HALT* is the control line which directs all processors and peripherals to stop their current activity when they detect this line low. This signal is usually generated from a switch. While all normal processing will cease upon detection of this signal, certain system activities will proceed. In particular, BE will continue to run, and refresh request and grant will continue so that memory refresh cycles will be performed to ensure that contents of memory are not lost during the halt. The use of HALT* makes it possible to halt the system without destroying any of the data which might help to identify the source of the problem.

2.5.4.3 RESET* (System Reset). RESET* is the control line which directs all processors and peripherals to re-initialize all necessary status and command registers to provide a known starting point for system operation.

2.5.4.4 BQ (Bus Quadrature -- M6809, M6809E systems only). BQ is a special signal generated by the M6809 MPU and required by the M6809E MPU. It is not currently used by most EXORbus designs, and it must not be used by any future designs. Since no other microprocessors generate or require this signal, any use of it makes the design unique to a limited subset of the EXORbus.

2.5.4.5 LIC (Last Instruction Cycle -- M6809E systems only). LIC is a special signal generated by the M6809E microprocessor. It is not currently used by most EXORbus designs, and it must not be used by any future designs. Since no other microprocessor generates this signal, any use of it makes the design unique to a very limited subset of the EXORbus.

2.5.4.6 DEBUG* (Debug Module Indicator). This optional signal is used to indicate the presence of a debug module in the system. A debug module may be used to modify the system memory map to provide alternate vectors for interrupts, thus allowing the system to function with two sets of ROM memory -- one for normal use and another during the debug process.

This line is grounded by the DEbug II Module and is used by other modules to determine the presence of the DEbug II Module. In some cases, the line is connected into the address decoders so that the module map is reconfigured automatically when a debug module is installed for system debugging.

2.5.5 Memory Refresh

Because the EXORbus allows the use of dynamic memory, it must make provision for refresh cycles. It does this by utilizing two signals -- REFREQ* and REFGNT.

2.5.5.1 REFREQ* (Refresh Request). REFREQ* is the signal from memory to the SYSTEM MASTER, requesting a refresh cycle. Because memory does not know the state of the system, it cannot make the determination of when to take such a cycle, but must allow the SYSTEM MASTER to grant the cycle.

2.5.5.2 REFGNT (Refresh Grant). REFGNT is the SYSTEM MASTER'S response to the REFREQ* signal. The SYSTEM MASTER provides this signal at the appropriate system time, which may be at the end of an instruction or upon completion of a DMA data transfer. Because the memory does not actually drive any lines on the bus, no timing is imposed on the driving of address, data, or control lines. The memory releases REFREQ* upon receipt of REFGNT. One cycle is provided for memory refresh. The SYSTEM MASTER, in turn, will release REFGNT, and the system will continue its normal operation.

2.6 RESERVED

Certain lines in EXORbus are defined as reserved. Some of these have had uses in the past, but it is now desirable to free up these pins. Others have always been defined as reserved, but may have been used by some applications in the past. One of the goals of this document is to ensure that any future use of such pins is done only in a coordinated manner.

2.6.1 Always Reserved (Used for Address Selection)

Certain pins in the EXORbus have always been defined as reserved. These pins have been used in the past for a variety of different uses, so it is recommended that no new use be made of these pins.

2.6.2 GROUND's Redefined

In an effort to free pins for future use, a large number of pins which had previously been defined as GROUND have now been moved to the reserved category. It is recommended that no use of these pins be made at this time.

2.6.3 Other Redefinitions

Some additional pins, which have been defined in the past, have also now been transferred to the reserved category. Because of the high probability of conflict, these pins should not be used in any new design.

CHAPTER 3

EXORbus TIMING

3.1 INTRODUCTION

This chapter describes the basic operation and sequencing of the EXORbus. Table A-3 in Appendix A shows two sets of specific timings -- one for 1-MHz rated products and a second for 2-MHz rated products. Compatibility between 1-MHz and 2-MHz rated products cannot be guaranteed.

3.2 DATA TRANSFER OPERATION

A data transfer occurs during one cycle of BE. After the falling edge of BE, the BUS MASTER places the address on A00-A15. The BUS MASTER then signals the peripheral that this cycle will be a valid transfer by driving VMA, VUA, and/or VXA high. If any one or a combination of the three signals is driven high, the cycle is valid. (See Figure 3-1.) The BUS MASTER will also drive Read/Write high if the cycle is a read cycle, or low if it is a write cycle.

On the rising edge of BE, all the addressing information is guaranteed to be valid and may be latched. After the rising edge of BE, the MASTER will drive the data bus on a write cycle, and the peripheral will drive the data bus on a read cycle.

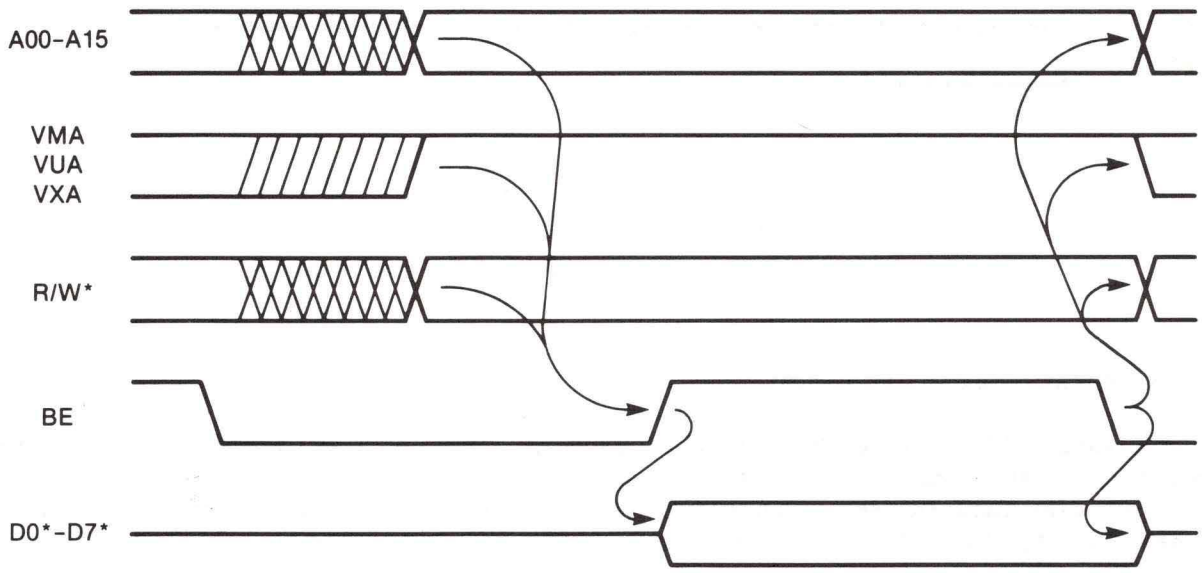


FIGURE 3-1. EXORbus Data Transfer Sequence

3.2.1 Memory Not Ready (MNRDY*)

Timing design is easy because EXORbus provides a clock delaying signal for the use of peripheral boards. The timing requirements which apply here are that the peripheral must have either latched (on write) or provided stable data (on read) prior to the fall of BE. The delaying signal which inhibits the fall of BE is MNRDY*, and it may make the high-to-low (assertion) or low-to-high (negation) transition only during the interval from the fall of BE to 30 nanoseconds prior to the next rise of BE. (See Figure 3-2.) The peripheral is restricted to a maximum hold time on MNRDY*. The SYSTEM MASTER will abort the cycle by driving BE low after a minimum of 5 microseconds from the previous BE low. Since this is much longer than any reasonable access time, it should serve only to extricate the EXORbus from system malfunctions.

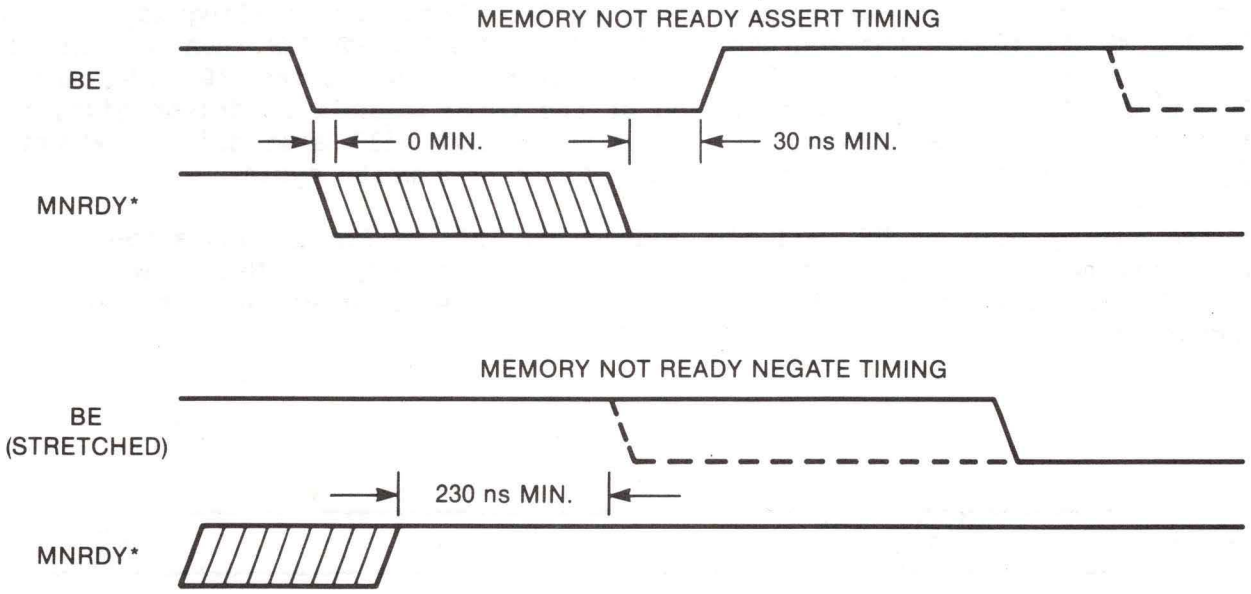


FIGURE 3-2. MNRDY* Timing

3.2.2 Parity Error (PARERR*)

In designs which incorporate the use of the signal PARERR*, the timing constraints are exactly the same as for valid data -- i.e., the signal must be valid at the fall of BE. Since the peripheral is already controlling the fall of BE (through MNRDY*), this imposes no additional complexity.

3.3 BUS EXCHANGE

EXORbus makes provision for SECONDARY MASTERS which require control of the bus at certain times. They request this control by driving BUSREQ* low. When the SYSTEM MASTER is prepared to grant the bus, it does so by driving BUSGNT high. Care must be taken during the exchange of bus control to ensure that no board misinterprets the bus signals during this transition. To provide proper timing and control, two constraints are applied. BUSGNT will go high only during the interval from the fall of BE to 30 nanoseconds prior to the address setup time of the SYSTEM MASTER. If the SECONDARY MASTER is prepared to have all of the address lines stable within the address setup time prior to the next rise of BE, the system can proceed at maximum speed. If the SECONDARY MASTER is not capable of meeting this requirement, it must drive VMA, VUA, and VXA low within 50 nanoseconds of receipt of BUSGNT, and hold them low until the next fall of BE. This provides a "dead" cycle during which no board will interpret any address because no authorization signal has been provided. Operation is similar to the procedure discussed in the data transfer section for providing dead cycles when a SECONDARY MASTER does not run at the speed of the primary. See Figure 3-3.

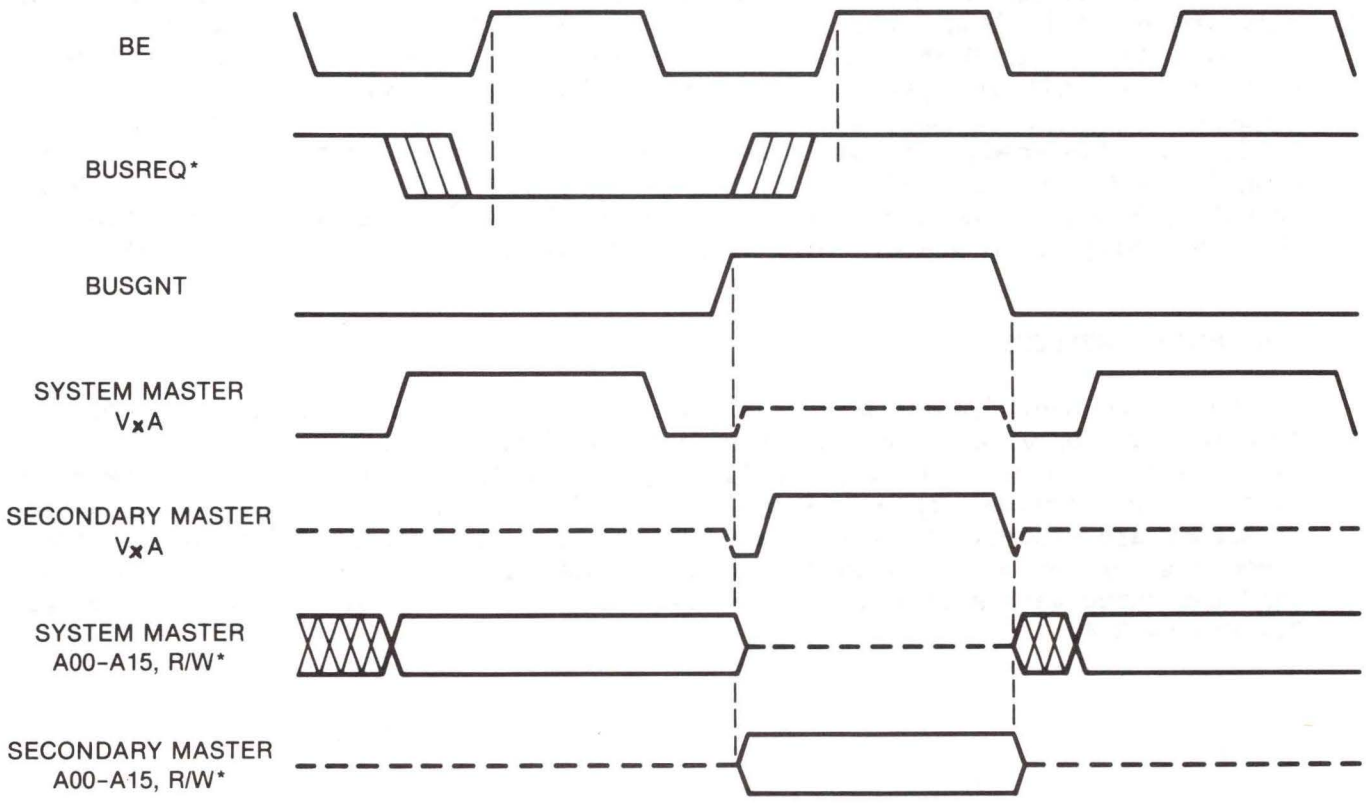


FIGURE 3-3. EXORbus Exchange of Mastership Sequence

3.3.1 Bus Arbitration

NOTE

VxA refers to any valid memory line -- i.e., VMA, VUA, or VXA.

Let us now consider how a transfer of bus mastership occurs. At the start of this example, the SYSTEM MASTER is driving the bus. Now a SECONDARY MASTER drives BUSREQ* low. The SYSTEM MASTER may elect to complete several more bus cycles, but on some future fall of BE, the SYSTEM MASTER will, within 50 nanoseconds, set its address, VxA, and R/W* lines to their high impedance state and drive BUSGNT high. Upon detecting BUSGNT high on its BUSGNT input pin, the SECONDARY MASTER drives all VxA lines to their low state. If sufficient time exists for the SECONDARY MASTER, it may present an address and drive the appropriate VxA signal(s) high. If the SECONDARY MASTER cannot present its address in the minimum address setup time prior to the next rise of BE, the SECONDARY MASTER will initiate the logic to present the desired address while holding all VxA lines low. This prohibits any board from accepting the possibly invalid address. Upon detecting the next fall of BE, the SECONDARY MASTER will drive the appropriate VxA line(s) high and initiate a data transfer. The SECONDARY MASTER will continue operating in this manner until either it loses bus grant or it has completed its transfer needs. BUSGNT may make a transition only while BE is low. When it goes low, the SECONDARY MASTER will set its address, VxA, and R/W* drivers to the high-impedance state, but will hold BUSREQ* low until it again gets the bus. The most common occurrence of this sequence is when a memory refresh cycle is being granted. When the SECONDARY MASTER is finished, it will set the address and R/W* lines to their high-impedance state, release BUSREQ*, and hold all VxA lines low. Upon detecting BUSGNT going low, the SECONDARY MASTER will release all VxA lines to their high-impedance state. This will return control to the SYSTEM MASTER.

3.4 MEMORY REFRESH

If the system uses dynamic memory but does not use hidden refresh, it may become necessary to provide a memory refresh cycle during system operation. Such a cycle is requested by driving REFREQ* low. When the SYSTEM MASTER is prepared to allow this refresh cycle, it will drive REFGNT high. The timing constraints on REFGNT are exactly the same as on BUSGNT. The significant difference is that since the refresh cycle does not actually use the bus, the SYSTEM MASTER must hold the three validator signals -- VMA, VUA, and VXA -- low during the cycle. See Figure 3-4.

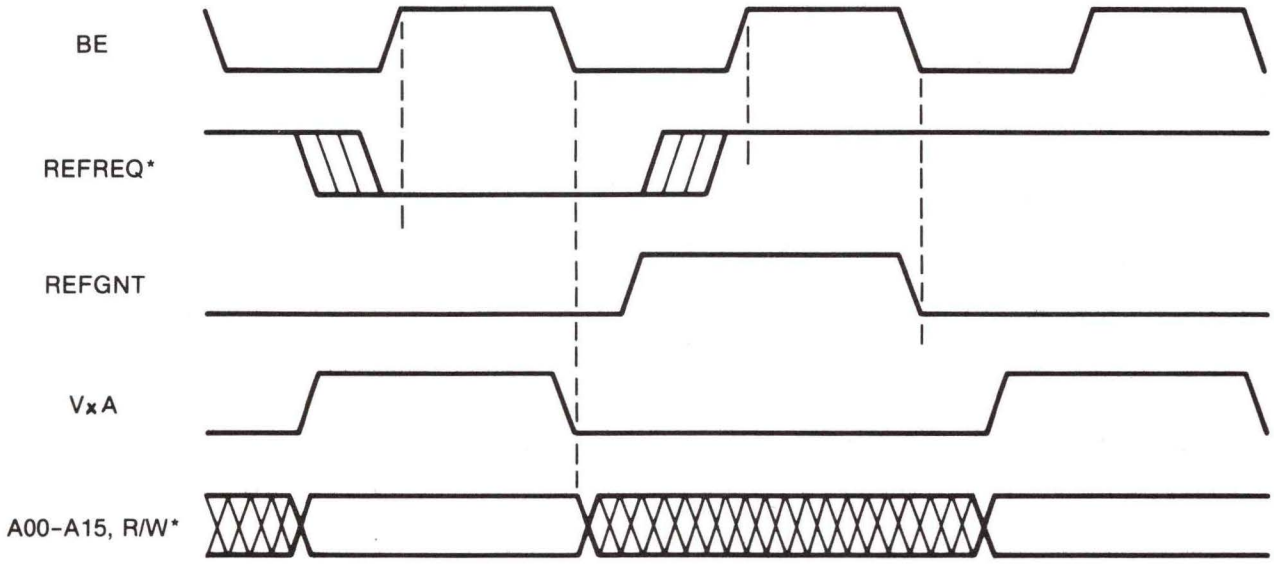


FIGURE 3-4. EXORbus Refresh Request/Grant Sequence

3.5 INTERRUPTS

Interrupts occur asynchronously to all other processes within the system. At the end of an instruction, the processor will recognize the pending request, if not masked, by executing an interrupt acknowledge sequence, which may be decoded from the state of BS and BA. BS and BA timing is the same as that for address and VxA lines. Further processing will depend on the software/firmware implementation.

CHAPTER 4

EXORbus ELECTRICAL SPECIFICATIONS

4.1 INTRODUCTION

In this chapter, the EXORbus specification defines the DC voltages supplied, maximum current drain, and signal requirements and limitations upon the user.

4.2 POWER

The EXORbus specification itself does not define current requirements for the system power supply. It does define maximum current draw per card and percent voltage regulation. Users are responsible for ensuring that the supply chosen is capable of meeting the current requirements of the configuration selected. All voltages discussed must be maintained at each card slot to the tolerances given in Table 4-1.

NOTE

> The user should ensure that the power supply tolerances guarantee these voltages at the slot, even with possible drop in the motherboard.

4.2.1 +5 Volts

+5 Vdc is the main logic level and normally has the largest associated current requirement. The bulk of the system circuitry -- including TTL logic, MOS microprocessors, and memories -- requires this voltage.

4.2.2 STANDBY +5 Volts (+12 Vdc on Earlier EXORcisers)

+5 Vdc Standby is used for distributing battery backup power. The standby voltage is maintained during system power loss to sustain memory and time-of-day clocks. If battery backup power is not required, the standby line is not used.

4.2.3 ±12 Volts

±12 Vdc represents the auxiliary digital logic supplies. These voltages supply the needs of MOS memories and I/O circuitry requiring multiple voltages. They may also be used for analog purposes. A -5 Vdc bias voltage and a -5.2 Vdc ECL voltage may also be derived from -12 Vdc, as needed. These supplies normally have lower current requirements than the +5 Vdc.

4.2.4 Bus Voltage/Current Specifications

Table 4-1 summarizes the bus voltage/current specifications. The listed specifications are the maximum allowed variance as measured at the edge connector of any card plugged into the motherboard.

The percentage listed under VARIATION is the total DC tolerance allowed at the EXORboard edge connector. This percentage is the sum expressed as:

VARIATION = DISTRIBUTION + LINE-REGULATION + LOAD-REGULATION

where:

DISTRIBUTION — Is defined as the percent variation caused by motherboard effects (resistive losses and differences from power supply sense point).

LINE-REGULATION — Is defined as provided in the vendor's power supply specification.

LOAD-REGULATION — Is defined as provided in the vendor's power supply specification.

The voltage tolerances listed apply to steady state conditions in the system. If very high current fluctuations occur due to system operation (such as might be caused by memory refresh), the response time of the voltage distribution system becomes important. Sufficient bypass capacitance and adequate power supply response time must be provided for such cases.

TABLE 4-1. Bus Voltage Specifications

MNEMONIC	DESCRIPTION	VARIATION (see NOTE)	RIPPLE & NOISE (PK-PK)	MAXIMUM CURRENT DRAW PER SLOT
+5V	+5 Vdc power	+5.0%/-2.5%	50 mV	2.5 amps
+12V	+12 Vdc power	+5.0%/-3.0%	120 mV	2 amps
-12V	-12 Vdc power	+3.0%/-5.0%	120 mV	2 amps
+5V STDBY	+5 Vdc standby	+5.0%/-2.5%	50 mV	1 amp
GND	ground	Ref.	Ref.	

NOTE:

The non-symmetric variation spec is given to ensure that the DC power will remain within the ±5% tolerance required by most IC's despite any drops resulting from power distribution on individual EXORboards.

4.2.5 Ground Distribution

The main ground distribution (mnemonic "GND") is the system return for all +5 Vdc and ±12 Vdc current.

Other than power supply lines, all EXORbus signals are limited to positive levels between 0 and 5.0 volts. These signal levels are:

a. 0.0 V $\leq$ Low level $\leq$ 0.8 V

b. 2.0 V $\leq$ High level $\leq$ 5.0 V

Figure 4-1 gives a simple graphic representation of these levels.

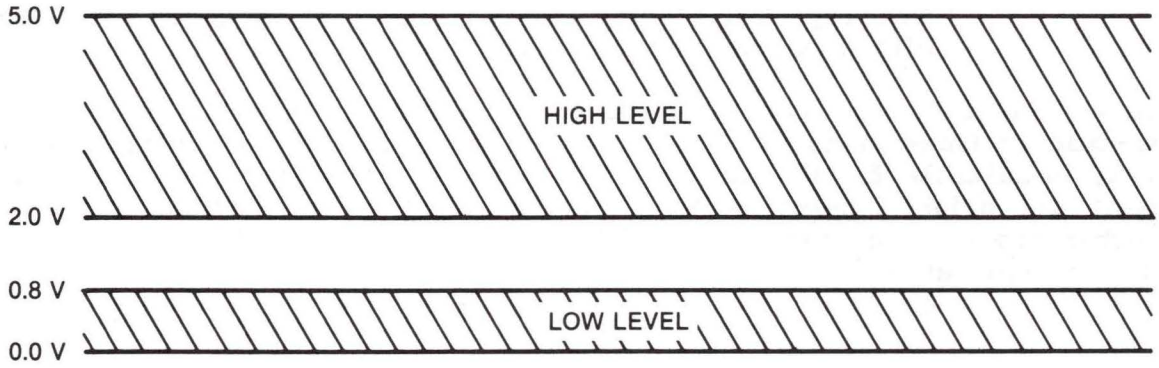


FIGURE 4-1. EXORbus Signal Levels

Depending on the function required, EXORbus uses three-state, open-collector, or totem-pole drivers. The drivers are specified in paragraph 4.3, and the receivers are specified in paragraph 4.4.

4.3 DRIVER SPECIFICATIONS

Totem-pole, three-state, and open-collector drivers are defined as follows:

Totem-pole - An active driver in both states which sinks current in the low state and sources current in the high state. Totem-pole drivers are used on signals having only a single driver per line (e.g., BUSGNT and REFGNT).

Three-state - Similar to a totem-pole driver except that it can go to a high impedance state (drivers turned off) in addition to the low and high logic states. Three-state drivers are used for lines that can be driven by several devices at different points on the bus. Only one driver can be active at any one time (e.g., address and data buses).

Open collector - Sinks current in the low state but sources no current in the high state. Open-collector drivers are used for signal lines which can be driven by several devices simultaneously (e.g., interrupt and refresh request lines) in wired-OR configuration with a common pull-up resistor.

Table 4-2 lists driver specifications. The MC8T28 or SN74S241 can be used for totem-pole or three-state drivers requiring 48 mA current sink capability. The MC8T26A is suitable for the bidirectional data bus interface. All standard 74xx outputs can drive totem-pole applications using 16 mA current sink. Open collector applications can use the 7406 or 7407. Table 4-3 lists signal lines by driver application.

TABLE 4-2. Bus Driver Specifications

DRIVER TYPE	PARAMETERS	MIN.	MAX.	UNIT	TEST CONDITION
Totem-pole	Low state (V_{OL})		0.5	V	Sink 48 mA
(High current)	High state (V_{OH})	2.4		V	Source 5 mA
Totem-pole	Low state (V_{OL})		0.5	V	Sink 16 mA
(Low current)	High state (V_{OH})	2.4		V	Source 400 uA
Three-state	Low state (V_{OL})		0.5	V	Sink 48 mA
	High state (V_{OH})	2.4		V	Source 5 mA
	Off-state output current (I_{OZ})		$\pm$100	uA	2.4V or 0.5V applied
Open-Collector	Low state (V_{OL})		0.7	V	Sink 40 mA
	High state output current (I_{OH})		50	uA	5.0V applied

NOTE: For output current, a positive value indicates current flow into the driver. A negative value indicates current flow out of the driver.

TABLE 4-3. Driver Applications

THREE-STATE	HIGH CURRENT TOTEM-POLE	LOW CURRENT TOTEM-POLE	OPEN-COLLECTOR
ADDRESS bus (A00-A15) DATA bus (D0*-D7*) R/W* VMA VUA VXA	BA BE BS MEMCLK	BUSGNT REFGNT	BUSREQ* (see NOTE) DEBUG* (see NOTE) FIRQ* HALT* IRQ* MNRDY* NMI* PARERR* PWRFAIL* (see NOTE) REFREQ* RESET*

NOTE: This signal may be driven by either an open-collector or totem-pole driver. (This allows the board designer to minimize device count.)

4.4 RECEIVER SPECIFICATIONS

Table 4-4 lists the standard receiver specification. Bus receivers should have input diode clamp circuits (SN74LS240, SN74LS244, SN74S240, SN74S244) to prevent excessive negative voltage excursions. The standard specification of 40 uA can be met by using devices with standard PNP inputs. The MC8T28, MC8T97, or MC8T98 is suitable for use as a receiver, as well as types SN74LS240, SN74LS244, or SN74S240.

TABLE 4-4. Bus Receiver Specifications

PARAMETER	MIN.	MAX.	UNIT	INPUT VOLTAGE
Low state input voltage (V_{IL})		0.8	V	
High state input voltage (V_{IH})	2.0		V	
Low state input current (I_{IL})		-400	uA	0 V $\leq$ V $\leq$ 0.4 V
High state input current (I_{IH})		100	uA	5.0 V $\geq$ V $\geq$ 2.4 V

4.5 MOTHERBOARD SIGNAL LINE INTERCONNECTIONS

EXORbus is intended for high performance systems. The signal line distance on the motherboard will be short (18" maximum) and signal line noise will be low. The following paragraphs specify and describe signal line characteristics and elements that influence signals on the motherboard.

4.6 ELECTRICAL LOADING

4.6.1 Board Level Loading

For any EXORbus resident board, the following rules apply:

a. Total capacitive load on any EXORbus line shall not exceed 15 picofarads. Typically, a driver or receiver has 3 to 5 picofarads capacitive load.

b. Each signal line input must not source more than 1.5 mA at 0.5V nor sink more than 140 uA at 2.4 volts.

4.6.2 System Level Loading

a. Total capacitive load on any EXORbus line must not exceed 250 picofards. This includes the total of all board capacitive loads plus the motherboard capacitive load.

b. Total DC load on any high current totem-pole or three-state EXORbus line must not exceed 30 mA source current at 0.5V, or 3 mA sink current at 2.4 volts.

c. Total DC load on any low current totem-pole EXORbus line must not exceed 10 mA source current at 0.5V, or 1.5 mA sink current at 2.4 volts.

d. Total DC load on any open-collector EXORbus line must not exceed 20 mA source current at 0.7V.

CHAPTER 5

MECHANICAL SPECIFICATIONS

5.1 INTRODUCTION

Information in this chapter is provided to ensure that EXORbus motherboards, card racks, and PCB's are mechanically compatible. This chapter supplies part numbers for specific vendor parts that may be used to meet the requirements of this specification. As long as the specifications given in this chapter are complied with, any compatible vendor part may be substituted.

Throughout this chapter, the following terminology is used:

Motherboard - A PC board (backplane) into which one or more EXORboards are installed. This PC board interconnects the pins of the various connectors to provide buses between connectors.

EXORboard - A PC board which is plugged into the motherboard and communicates with other EXORboards installed in the same motherboard.

The "front" of a motherboard is the side into which the EXORboards are inserted into the edge connectors.

The "front" of an EXORboard is the side on which the components are mounted.

The "bottom edge" of an EXORboard is the edge which provides the PC fingers for insertion into the edge connector on the motherboard.

5.2 EXORbus MOTHERBOARD

This portion of text provides the following EXORbus motherboard information:

a. Reference designations and pin numbering standards
b. Motherboard/EXORboard dimensional requirements
c. Connector sockets

5.2.1 Reference Designations and Pin Numbering Standards

The following standards are <u>recommended</u> for motherboard identification purposes (see Figure 5-1):

a. Card slot locations are designated A1, A2, A3, etc. The numbering technique is illustrated in Figure 5-1.

b. Connector sockets on the motherboard will be designated J1. J1 is the 86-pin socket.

c. Numbering of the 86-pin socket is depicted in Figure 5-1.

d. An additional connector (e.g., for power) located on the motherboard will be designated P1.

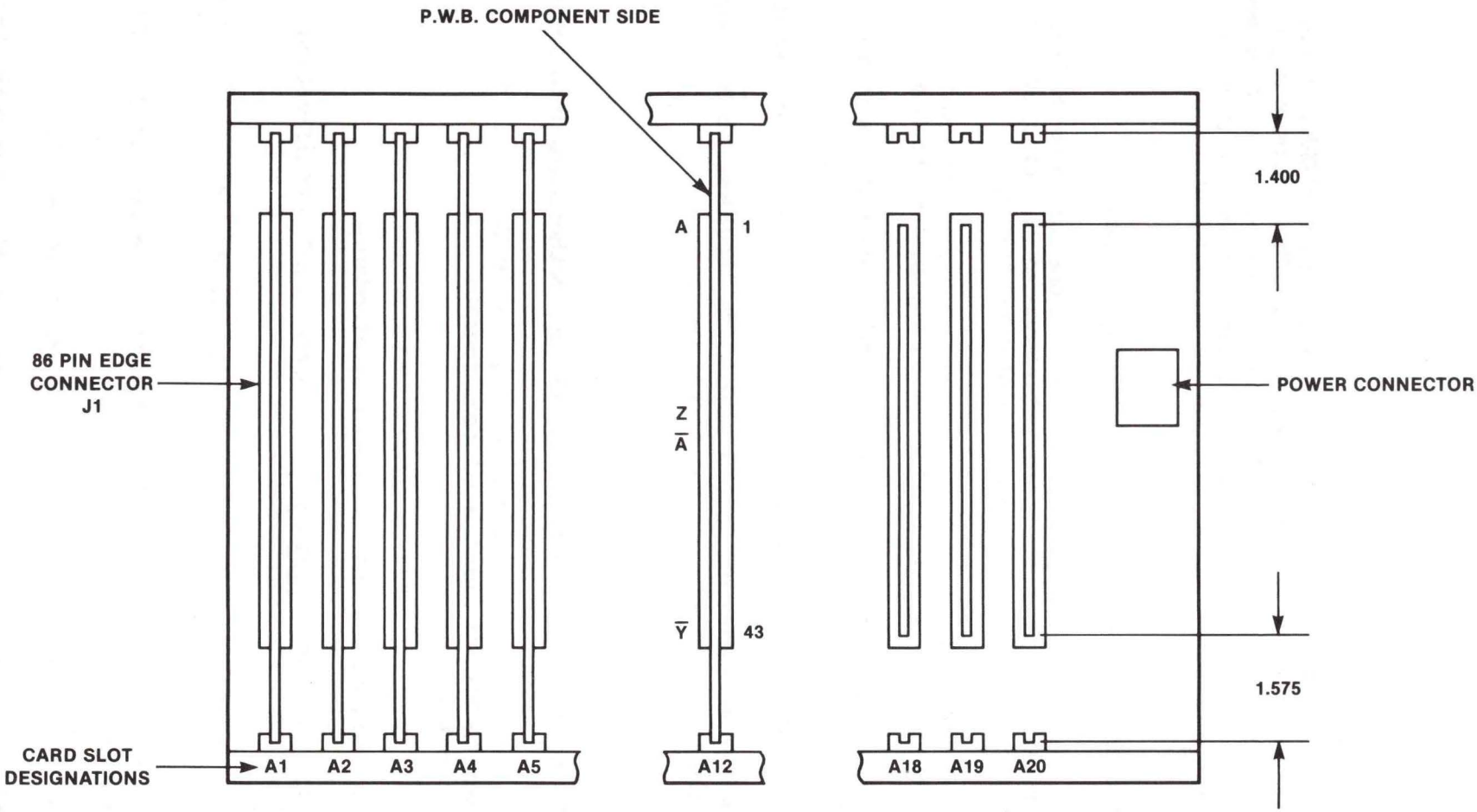


FIGURE 5-1. Motherboard Reference Designations and Pin Numbering Standard (front view)

5.2.2 Motherboard/EXORboard Dimensional Requirements

Certain specifications must be adhered to when designing an EXORbus motherboard and compatible EXORboards. Figure 5-2 illustrates the following relationships:

a. Board Spacing (BS) - center-to-center spacing of the boards is as follows:

   1. Printed Circuit Board spacing - .75 minimum (.80 recommended)
   2. Wire Wrap Board spacing - 1.4 minimum

b. Board Thickness (BT)- board thickness is 0.062 $\pm$ .005 inch.

c. Component Lead Length (LL) - length of the component leads protruding through the back of the EXORboards must not exceed .100 inch.

d. Component Height (CH) - height of the components on the front of each EXORboards must not exceed dimensions shown in Figure 5-3.

e. Board Warpage (BW) - maximum allowable EXORboard warpage is .062 inch.

f. Wire Wrap Pin Height (WW) - length of the wire wrap pins protruding through the back of the EXORboards must not exceed .650 inch.

5.2.3 Connector Sockets

The P1 edge connectors on the EXORboard are inserted into the connector sockets mounted to the motherboard.

Prefabricated connector sockets are inserted into the motherboard in a one-step operation. The socket contacts and socket insulator construction is of a one-piece design. Recommended vendors are SAE, AMP, and VIKING. (Standard Applied Engineering part number SAC-43D/1-2.)

CAUTION

Connectors from various vendors are not necessarily interchangeable dimensionally, and may affect the design of the card cage.

5.3 EXORboards

This portion of text provides the following EXORboard information:

a. Construction techniques
b. Reference designations and pin numbering standards
c. Overall dimensions
d. Bus edge connector
e. Non-bus edge connectors
f. Ejectors

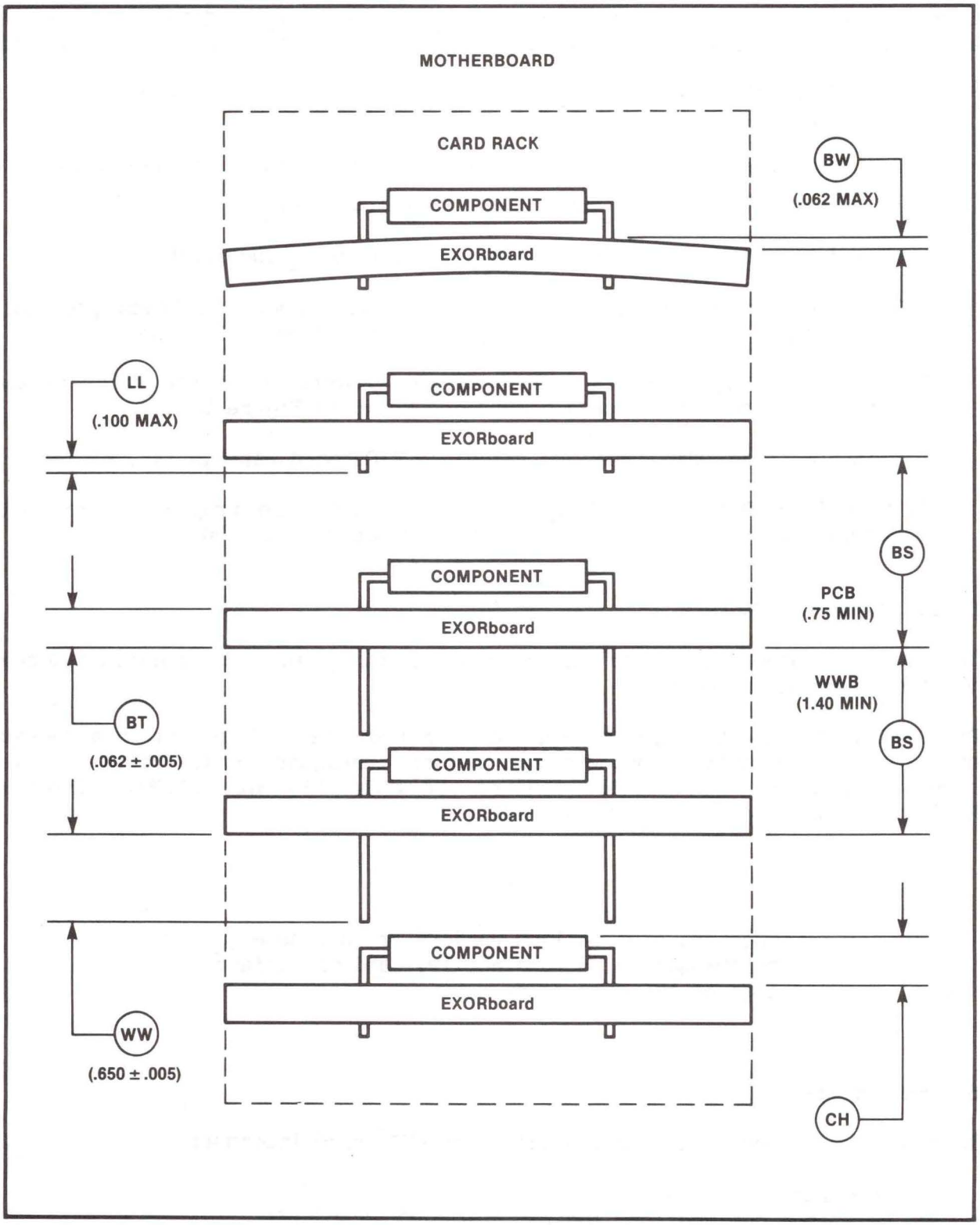


FIGURE 5-2. Motherboard/EXORboard Dimensional Requirements

5.3.1 Construction Techniques

Many PCB construction techniques are available to the designer. Care should be taken to ensure that an adequate ground grid is provided on the board.

5.3.2 Reference Designations and Pin Numbering Standards

Refer to Figures 5-3 and 5-4. The following standards are recommended for PCB identification purposes:

a. The card edge finger on the bottom edge of the EXORboard is designated P1, and mates with an 86-pin edge connector. Its pin numbers are labeled A through Z and $\overline{A}$ through $\overline{Y}$ from left to right on the component side of the EXORboard, and 1 through 43 from right to left on the solder side.

b. Edge connectors on the top edge of the PCB are designated J1, J2, J3, etc.

5.3.3 Overall Dimensions

Figure 5-3 shows the physical dimensions of a standard EXORboard.

All EXORboards to be mounted on the standard motherboard have an 86-pin edge connector that mates with a card edge connector (Stanford Applied Engineering SAC-43D/1-2 or equivalent) in an EXORboard chassis, card cage, or EXORciser chassis.

5.3.4 Bus Edge Connector

Figure 5-3 defines the EXORboard bus edge connector requirements. All information contained in Figure 5-3 must be adhered to for EXORbus compatibility.

5.3.5 Non-Bus Edge Connectors

Figure 5-4 illustrates the PCB non-bus edge connector type and spacing information. There is no prescribed limit to the number or type of I/O connections which may be made off the top edge of the board as long as they do not exceed the allowed dimensional restrictions given in Figure 5-4.

NOTE

It is recommended that the use of cable connections to the top edge of the board be minimized, since it makes the job of installing and removing EXORboards more difficult.

5.3.6 Ejectors

Ejectors facilitate the insertion and removal of EXORboards within a card rack environment. The card ejectors used on EXORboards are either Scanbe part number S-203 or Birtcher part number 82-2.

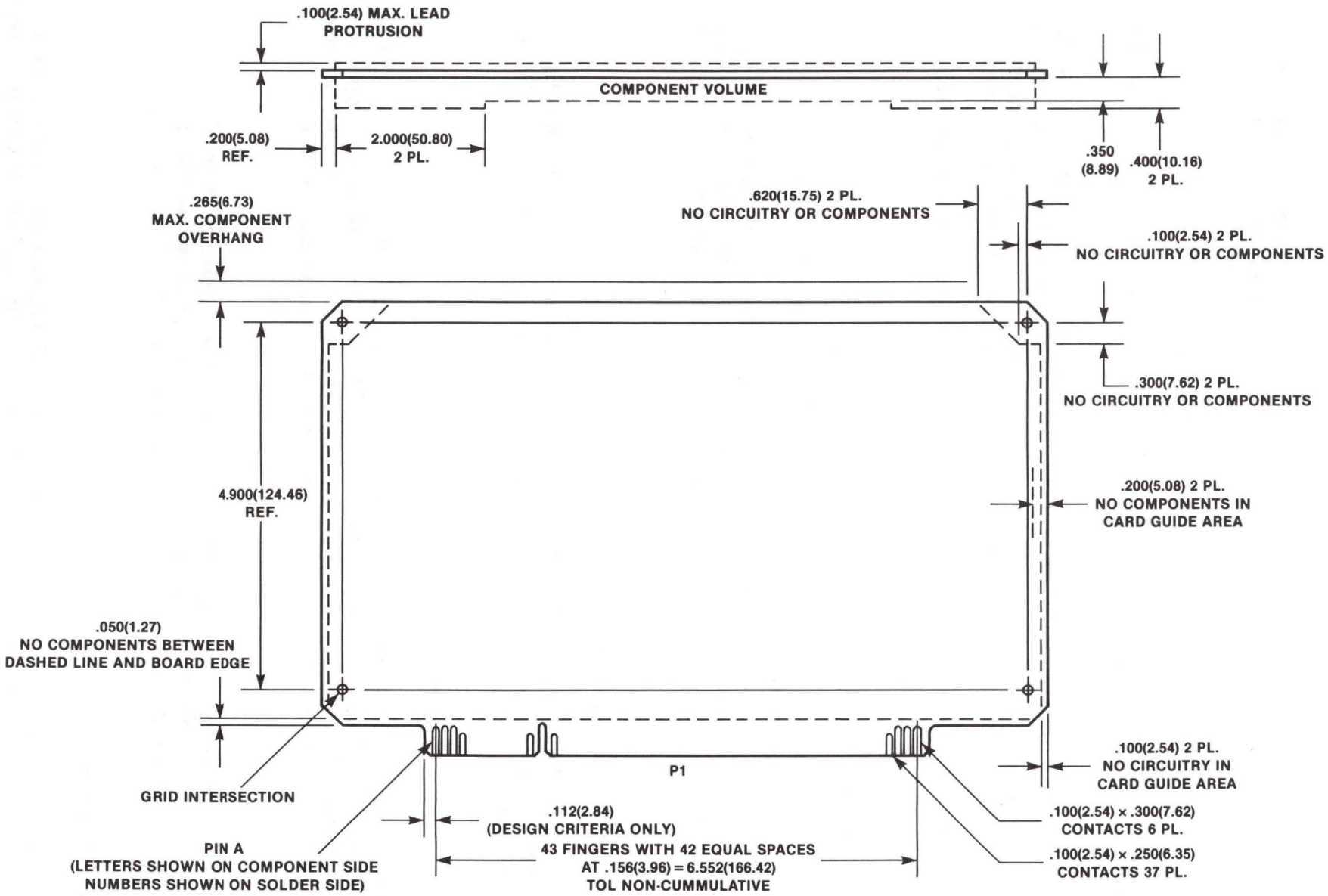


FIGURE 5-3. EXORboard PCB Standards (Sheet 1 of 2)

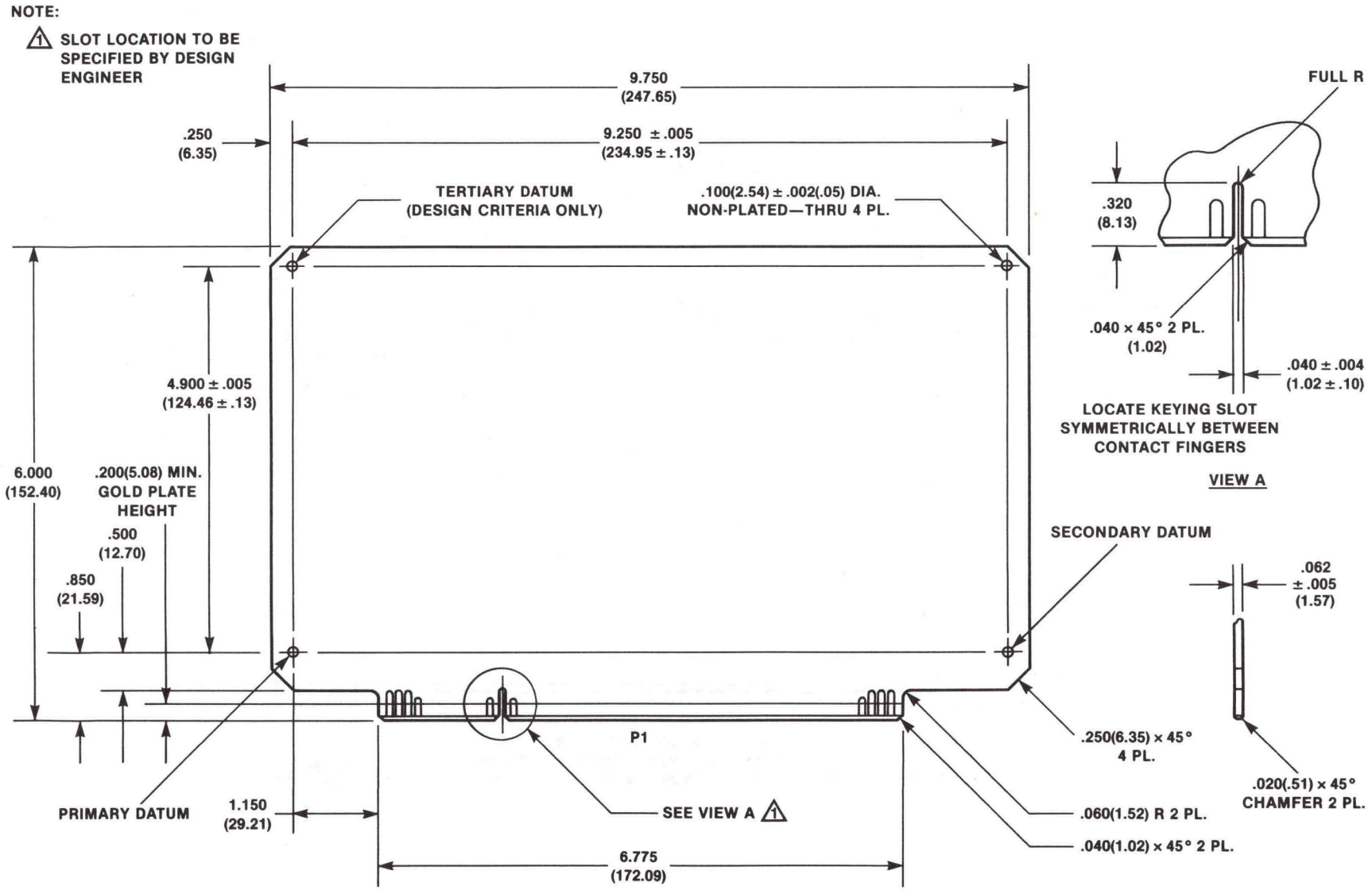


FIGURE 5-3. EXORboard PCB Standards (Sheet 2 of 2)

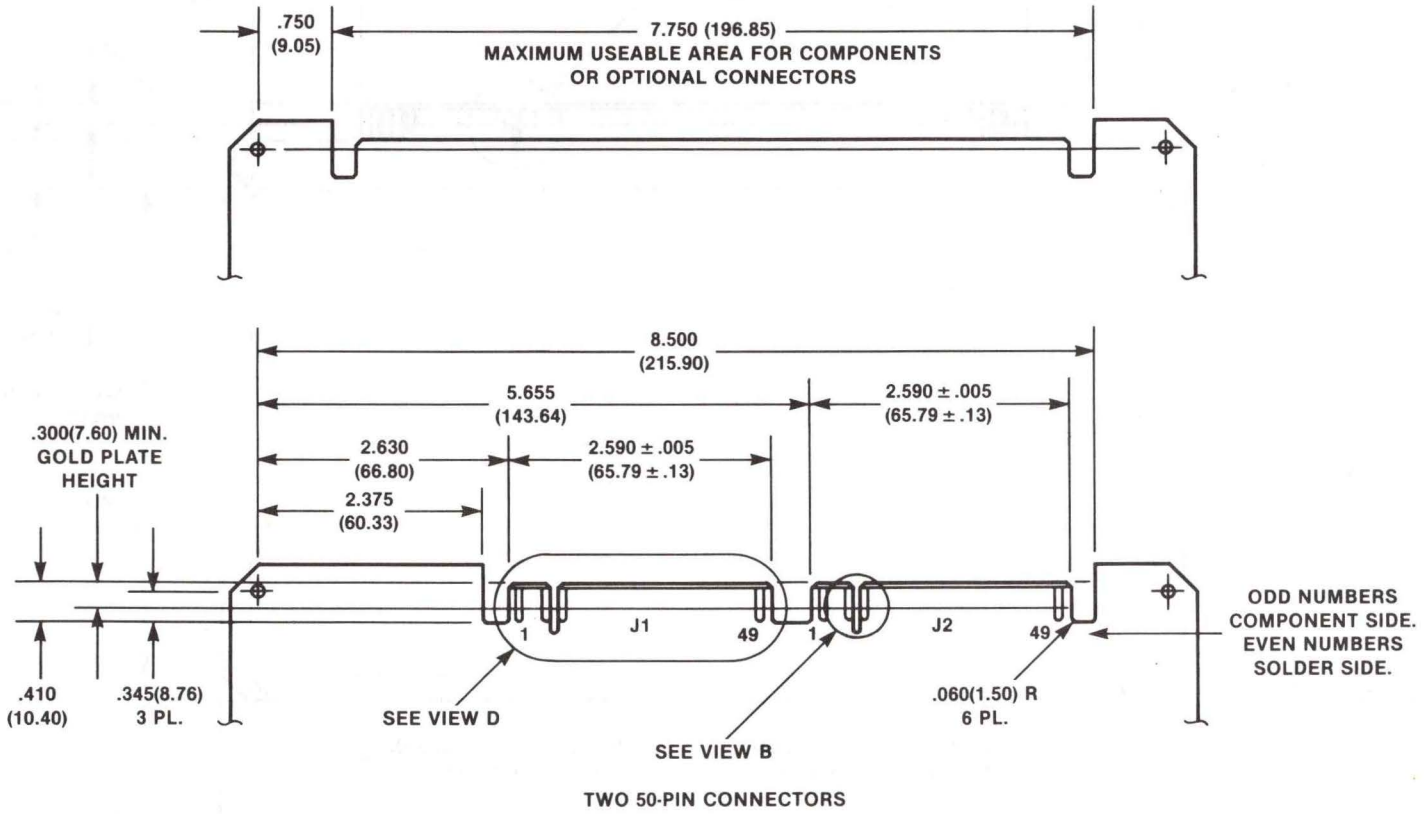


FIGURE 5-4. Typical EXORboard Non-Bus Edge Connectors (Sheet 1 of 2)

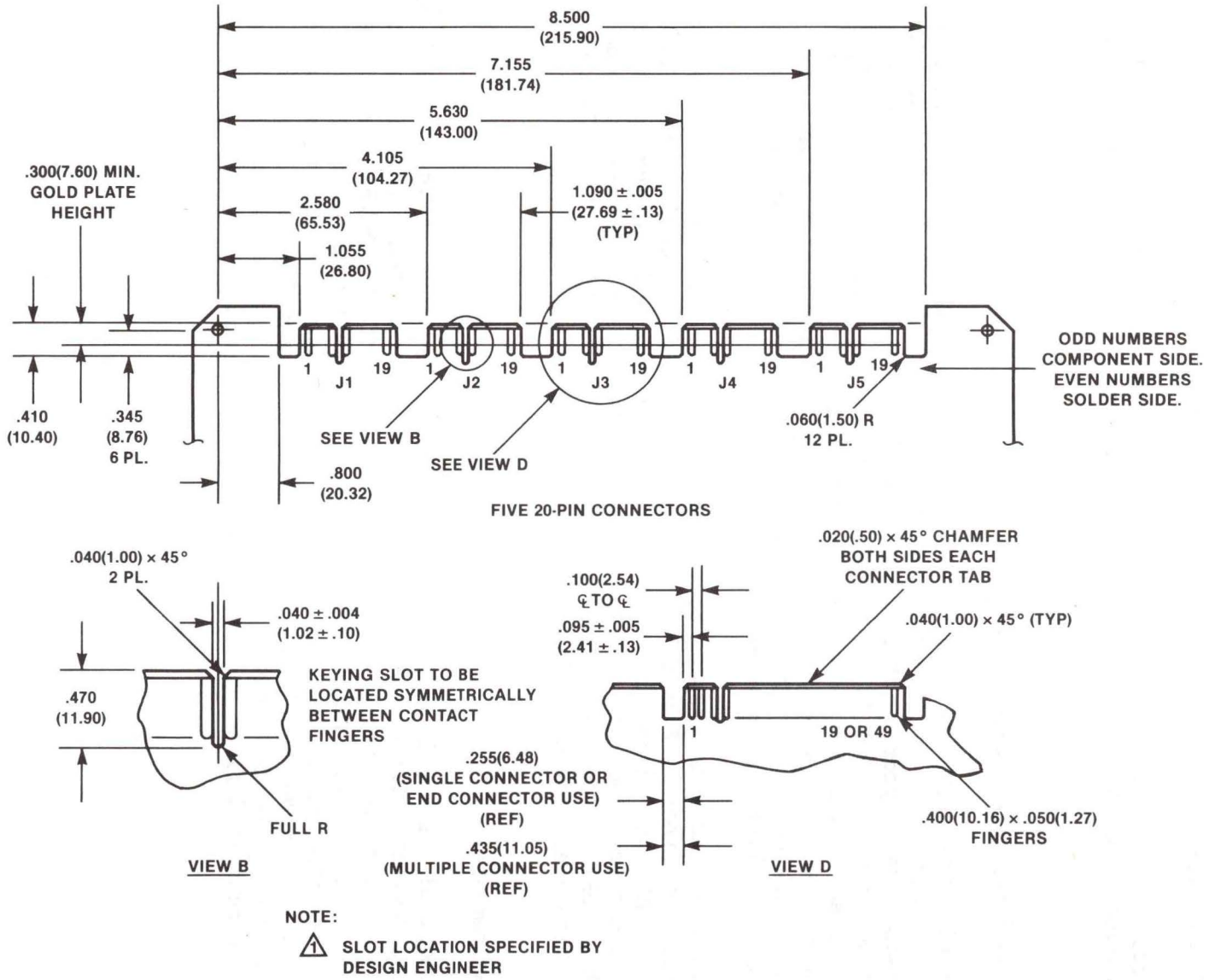


FIGURE 5-4. Typical EXORboard Non-Bus Edge Connectors (Sheet 2 of 2)

APPENDIX A

MOTOROLA STANDARD EXORbus TIMING

A.0 INTRODUCTION

The purpose of this appendix is to provide standard EXORbus timing specifications that may be used by the prospective peripheral or MPU board designer.

A.1 Nomenclature and Abbreviations

All abbreviations shown in Tables A-1, A-2, and A-3 use uppercase characters with no subscripts. The initial character is the letter T, followed by a six-character descriptor. This descriptor is used to identify the to/from measurement points. The first three letters of the descriptor identify the signal name and transition level for the measurement starting point, while the last three letters identify the signal name and transition level for the measurement ending point. The descriptor format is illustrated in Table A-1, while Table A-2 lists the measurement abbreviations.

Timing is presented with respect to the bus. The time relationship between the bus signals is shown in Figure A-1, while the minimum and maximum time values for the signals are listed in Table A-3 (for 1.0 MHz and 2.0 MHz operation). All of these time values are referenced to the leading edge or trailing edge of Bus Enable (BE). Time relationships not specified within this table can be readily calculated from the information provided.

A.2 Requirements

It is required that all interfacing to the bus be buffered with MC8T28 or equivalent devices. Timing data on each signal is based upon a capacitive load (C_L) of 250 picofarads and a maximum device loading of 10 MC8T28 or equivalent devices (-4.0 mA @ 0.5V and 400 uA @ 2.4V). Bus skew time is assumed to be 10 ns. Skew time is to be equally shared by the source and destination unit specification. Driver requirement is 48 mA @ 0.5V and 5 mA @ 2.4V. V_{CC} is always assumed to be 5.0 volts. Ground is 0 volts and is logic zero (low). Positive current is defined as into the terminal referenced.

TABLE A-1. Descriptor Format

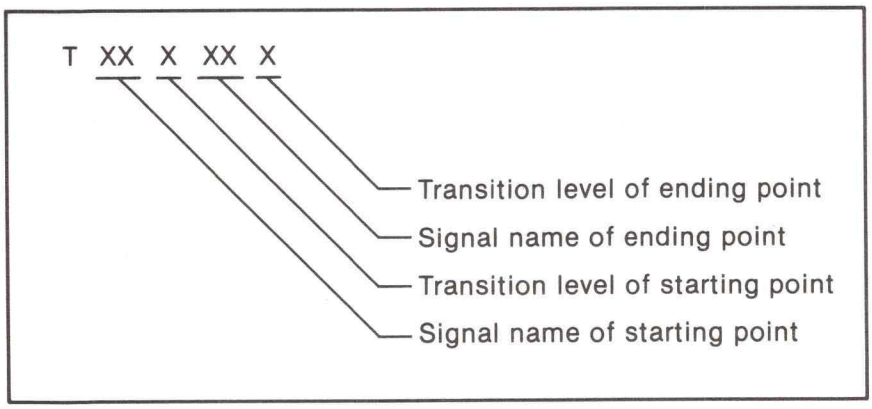


TABLE A-2. Measurement Abbreviations

ABBREVIATIONS (Signal Names)

AD = Bus Address, R/W*, VMA, VUA, VXA
DW = Write data from MPU to peripheral module
DR = Read data from peripheral module to MPU
BE = Bus E clock signal

ABBREVIATIONS (Transition Levels)

H = Low-To-High Transition
L = High-To-Low Transition
V = Transition to Valid State
X = Transition to Invalid or Don't Care State
Z = Transition to Off (High Impedance State)

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	Must be Valid	Will be Valid
	Change from High-To-Low	Will change from High-To-Low
	Change from Low-To-High	Will change from Low-To-High
	Don't Care (Any change)	Changing State
		High Impedance (Off)

TABLE A-3. EXORbus Specifications

DESCRIPTION	NUMBER	SYMBOL	1.0 MHz		2.0 MHz	
			MIN	MAX	MIN	MAX
CYCLE TIME	(1)	TBELBEL	1000 ns	10 us	500 ns	10 us
RISE or FALL TIME	(2)	Tr, Tf	5 ns	25 ns	5 ns	25 ns
BUS E HIGH TIME	(3)	TBEHBEL	470 ns	9.5 us	240 ns	9.75 us
ADDRESS SET-UP TIME	(4)	TADVBEH	175 ns		120 ns	
ADDRESS HOLD TIME	(5)	TBELADX	15 ns		15 ns	
DATA BUS ACTIVE	(6)	TBEHDWX	0 ns		0 ns	
WRITE DATA SET-UP TIME	(7)	TDWVBEL	185 ns		80 ns	
WRITE DATA HOLD TIME	(8)	TBELDWZ	15 ns		15 ns	
READ DATA BUFFER ON	(9)	TBEHDRX	0 ns		0 ns	
READ DATA SET-UP TIME	(10)	TDRVBEL	100 ns		60 ns	
READ DATA BUFFER OFF	(11)	TBELDRZ	0 ns	50 ns	0 ns	50 ns

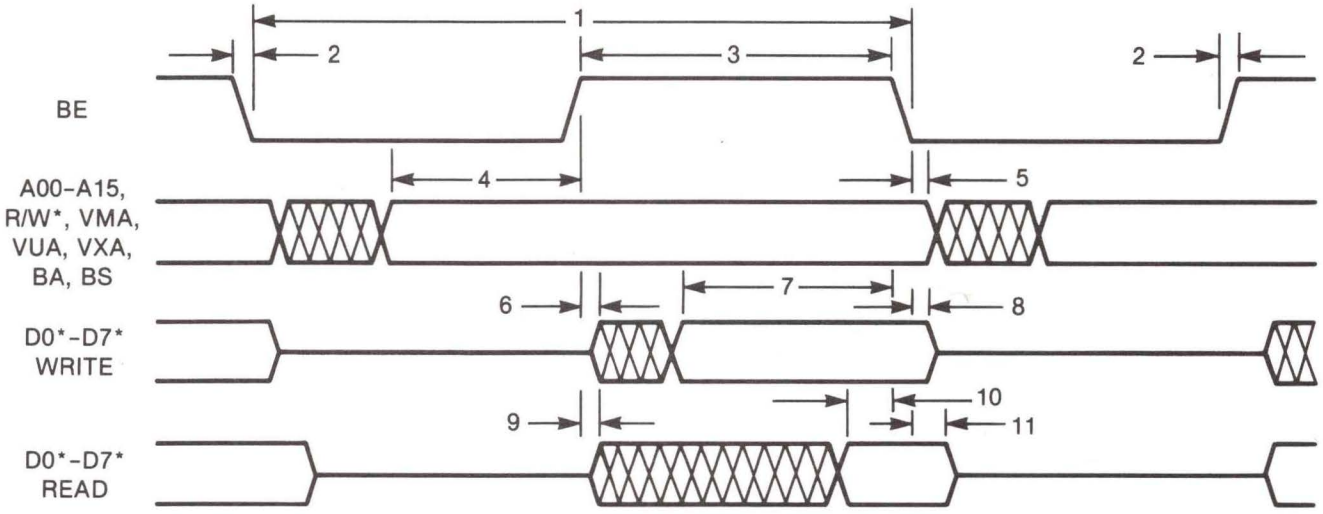


FIGURE A-1. EXORbus Specification Timing Diagram

APPENDIX B

EXORbus INTERFACE CONNECTOR PINOUTS

ALPHANUMERIC PIN SEQUENCE

This list contains all currently authorized uses for EXORbus pins. It is intended to control the future use of these pins, rather than being a guide to the past.

PINS	SIGNAL	SIGNAL DEFINITION
A-C	+5 VDC	+5 Vdc Power - Used by the system logic circuitry.
D	IRQ*	INTERRUPT REQUEST - An active low, wired-OR, level-sensitive signal that requests the generation of an interrupt sequence by the SYSTEM MASTER. The SYSTEM MASTER will continue normal operation until it completes the current instruction before it recognizes the request. At that time, if the SYSTEM MASTER is accepting interrupts, it will start executing the interrupt sequence.
E	NMI*	NONMASKABLE INTERRUPT - An active low, wired-OR, edge-sensitive signal that requests the generation of a nonmaskable interrupt sequence by the SYSTEM MASTER. The SYSTEM MASTER will continue normal operation until it completes the current instruction before it recognizes the request. At that time, regardless of the state of any interrupt masks, the SYSTEM MASTER will begin executing the nonmaskable interrupt sequence.
F	VMA	VALID MEMORY ADDRESS - An active high signal generated by the current BUS MASTER to indicate the presence of a valid memory address on the bus. The SYSTEM MASTER must maintain this line in the high impedance state while BUSGNT (pin 15) is active (high).
H	-	RESERVED - ($\pm$12V RETURN in earlier system designs.)
J	BE	BUS ENABLE - (E or Phase 2 in earlier system designs.) An active high clock signal generated by the SYSTEM MASTER. This signal is stretched in the high state while MNRDY* (pin R) is active (low).
K	-	RESERVED - ($\pm$12V RETURN in earlier system designs.)
L	MEMCLK	MEMORY CLOCK - This pin should not be used in any new peripheral board designs. Any new processor board design should provide BE on this pin as well as pin J if compatibility with older Micromodules within the system is desired.
M	-12 VDC	-12 VDC Power - Used by system logic circuitry.

PINS	SIGNAL	SIGNAL DEFINITION
N	BUSREQ*	BUS REQUEST - (TSC* in earlier M6800 systems.) An active low, wired-OR signal that requests access to the system bus. An active (low) state on this line will cause the SYSTEM MASTER to release the data, address, VMA, VUA, VXA, and R/W lines. A BUSGNT signal (pin 15) will also be generated after the fall of BE.
P	BA	BUS AVAILABLE - An active high signal generated by the SYSTEM MASTER which, along with BS, indicates the current state of the SYSTEM MASTER but does not reflect the status of the system bus (this is done via BUSGNT, pin 15). NOTE: BA, BS states unique to M6809 systems.

BA	BS	STATE
0	0	Normal (Running)
0	1	Interrupt Acknowledge
1	0	Sync Acknowledge
1	1	Halt or Bus Grant

R	MNRDY*	MEMORY NOT READY (MEMRDY in early EXORcisers) - An active low, wired-OR signal that permits the system to work with slow memory modules. When this signal is low, the clocks will be stretched with BE active (high) and BQ (if provided) inactive (low).
S	LIC	LAST INSTRUCTION CYCLE (M6809E systems only) - An active high signal produced by the M6809E microprocessor during the last cycle of each instruction. This line will be in the high impedance state during the BUSGNT state. Not recommended for new design.
T	+12 VDC	+12 Vdc Power - Used by system logic circuitry.
U	STANDBY	+5 Vdc STANDBY Power (+12V in early EXORcisers) - This line is used with battery backup memory modules. If battery backup is not required, the STANDBY line should not be used for any other purpose.
V	PWRFAIL*	POWER FAIL - This active low, wired-OR signal is used by battery backup memory modules. When this signal goes active (low), it disables the write function of the protected memory module.
W	PARERR*	PARITY ERROR - This active low, wired-OR signal is normally held high. If a memory module that incorporates a parity check circuit is used within the system and a parity error is detected, this signal will be forced low.
X-Z	GND	GROUND

PINS	SIGNAL	SIGNAL DEFINITION
$\overline{A}$	FIRQ*	FAST INTERRUPT REQUEST (M6809, M6809E systems only) - An active low, wired-OR, level-sensitive signal that requests the generation of a SYSTEM MASTER fast interrupt sequence. The SYSTEM MASTER will wait until the instruction being executed is completed before recognizing the request. At that time, if the interrupt is not masked, the SYSTEM MASTER will begin the interrupt sequence. This sequence is fast in the sense that it stacks only the return address and condition codes.
$\overline{B}$	-	RESERVED - (Reference GND in earlier system designs.)
$\overline{C}$-$\overline{F}$	-	RESERVED - These signal lines and their counterpart pin numbers (25, 26, 27, and 28) are reserved by Motorola. However, some earlier Micromodules used these lines for address selection.
$\overline{H}$	D3*	DATA bus (bit 3) - One of eight bidirectional data lines which provide a two-way data transfer path between the BUS MASTER and all modules in the system. The data bus drivers on various modules are in the off or high impedance state except when selected during a data transfer operation. Data bus drivers should drive the data bus coincident with BE (phase 2) asserted.
$\overline{J}$	D7*	DATA bus (bit 7) - Same as D3* on pin $\overline{H}$.
$\overline{K}$	D2*	DATA bus (bit 2) - Same as D3* on pin $\overline{H}$.
$\overline{L}$	D6*	DATA bus (bit 6) - Same as D3* on pin $\overline{H}$.
$\overline{M}$	A14	ADDRESS bus (bit 14) - One of 16 address lines driven by the current BUS MASTER that permits selection of any addressable memory location or peripheral in the system.
$\overline{N}$	A13	ADDRESS bus (bit 13) - Same as A14 on pin $\overline{M}$.
$\overline{P}$	A10	ADDRESS bus (bit 10) - Same as A14 on pin $\overline{M}$.
$\overline{R}$	A9	ADDRESS bus (bit 9) - Same as A14 on pin $\overline{M}$.
$\overline{S}$	A6	ADDRESS bus (bit 6) - Same as A14 on pin $\overline{M}$.
$\overline{T}$	A5	ADDRESS bus (bit 5) - Same as A14 on pin $\overline{M}$.
$\overline{U}$	A2	ADDRESS bus (bit 2) - Same as A14 on pin $\overline{M}$.
$\overline{V}$	A1	ADDRESS bus (bit 1) - Same as A14 on pin $\overline{M}$.
$\overline{W}$-$\overline{Y}$	GND	GROUND

PINS	SIGNAL	SIGNAL DEFINITION
1-3	+5 VDC	+5 Vdc Power - Used by system logic circuitry.
4	HALT*	HALT - An active low, wired-OR signal which halts the SYSTEM MASTER at the end of the present instruction. The halt condition, indicated through BA (pin P) and BS (pin 23), does not grant access to the system bus. Refer to BUSREQ* (pin N) and BUSGNT (pin 15).
5	RESET*	RESET - An active low, wired-OR signal used to reset the SYSTEM MASTER and other peripheral devices and system modules. This signal starts the initialization of the system when power is initially applied. Depressing any RESET pushbutton switch while the system is operating will generate a RESET* signal and cause the SYSTEM MASTER to execute the restart routine.
6	R/W*	READ/WRITE - An active high (read operation) or active low (write operation) signal generated by the current BUS MASTER, which indicates to modules in the system the action the current BUS MASTER is taking and the direction of data transfer.
7	BQ	BUS QUADRATURE - (M6809, M6809E systems only) (Q or Phase 1 in earlier system designs.) A timing signal which leads BE.
8,9	-	RESERVED - (±12V RETURN in earlier system designs.)
10	VUA	VALID USER ADDRESS - An active high signal generated by the current BUS MASTER to indicate the presence of a valid user address on the bus. The SYSTEM MASTER must maintain this line in the high-impedance state while BUSGNT (pin 15) is active (high). On-board memory and I/O may be placed in the user memory map through strap selection.
11	-12 VDC	-12 Vdc Power - Used by system logic circuitry.
12	REFREQ*	REFRESH REQUEST - An active low, wired-OR signal which requests a bus cycle for the refresh of dynamic memory modules. Refer to REFGNT (pin 13).
13	REFGNT	REFRESH GRANT - An active high signal which acknowledges the request for a refresh cycle and indicates the refresh grant cycle. While REFGNT is active (high), BUSGNT is to be held inactive (low). The SYSTEM MASTER is inactive during the REFGNT cycle.
14	DEBUG*	DEBUG - A static, active low signal which indicates that a debug module is in the system.

PINS	SIGNAL	SIGNAL DEFINITION
15	BUSGNT	BUS GRANT - An active high signal generated by the SYSTEM MASTER, which acknowledges the request for the system bus, generated via BUSREQ*, and indicates the granting of bus access. This signal tightly controls access to the system bus. The signal is held inactive (low) during refresh grant cycles.
16	+12 VDC	+12 Vdc Power - Used by system logic circuitry.
17	STANDBY	+5 Vdc STANDBY Power - (+12V in early EXORcisers) - This line is used with battery backup memory modules and is identical to pin U.
18	-	RESERVED - (In earlier systems, this was CLOCK, a free-running, symmetrical clock signal generated by the SYSTEM MASTER and available to peripheral modules that require a clock not affected by the processor and/or memory timings. When internally-clocked devices became available, the ungated clock signal previously used became unnecessary.)
19	VXA	VALID EXECUTIVE ADDRESS - An active high signal generated by the current BUS MASTER when the system is operating in the multi-map mode and the program is addressing the executive portion of the memory map. Additionally, all peripheral modules (such as memories) must be set to respond to the VXA signal if the user wants to operate those modules in the executive portion of the map.
20-22	GND	GROUND
23	BS	BUS STATUS - This signal, in conjunction with the BA signal (pin P), reflects the SYSTEM MASTER halt, interrupt, and sync states.
24	-	RESERVED - (Reference GND in earlier systems.)
25-28	-	RESERVED - These signal lines and their counterpart pin numbers ($\overline{C}$, $\overline{D}$, $\overline{E}$, $\overline{F}$) are reserved by Motorola.
29	D1*	DATA bus (bit 1) - Same as D3* on pin $\overline{H}$.
30	D5*	DATA bus (bit 5) - Same as D3* on pin $\overline{H}$.
31	D0*	DATA bus (bit 0) - Same as D3* on pin $\overline{H}$.
32	D4*	DATA bus (bit 4) - Same as D3* on pin $\overline{H}$.
33	A15	ADDRESS bus (bit 15) - Same as A14 on pin $\overline{M}$.
34	A12	ADDRESS bus (bit 12) - Same as A14 on pin $\overline{M}$.

PINS	SIGNAL	SIGNAL DEFINITION
35	A11	ADDRESS bus (bit 11) - Same as A14 on pin $\overline{M}$.
36	A8	ADDRESS bus (bit 8) - Same as A14 on pin $\overline{M}$.
37	A7	ADDRESS bus (bit 7) - Same as A14 on pin $\overline{M}$.
38	A4	ADDRESS bus (bit 4) - Same as A14 on pin $\overline{M}$.
39	A3	ADDRESS bus (bit 3) - Same as A14 on pin $\overline{M}$.
40	A0	ADDRESS bus (bit 0) - Same as A14 on pin $\overline{M}$.
41-43	GND	GROUND

NOTE: Overscore pin letters denote lower case letters (i.e., $\overline{A}$ = a).

APPENDIX C

EXORbus INTERFACE CONNECTOR PINOUTS

MNEMONIC SIGNAL SEQUENCE

This list contains all currently authorized uses for EXORbus pins. It is intended to control the future use of these pins, rather than being a guide to the past.

SIGNAL	PINS	SIGNAL DEFINITION
-	H,K, 8,9	RESERVED - (±12V RETURN in earlier system designs.)
-	$\overline{B}$,24	RESERVED - (Reference GND in earlier system designs.)
-	$\overline{C}$-$\overline{F}$, 25-28	RESERVED - These signal lines are reserved by Motorola. However, some earlier Micromodules used these lines for address selection.
-	18	RESERVED - (In earlier systems, this was CLOCK, a free-running, symmetrical clock signal generated by the SYSTEM MASTER and available to peripheral modules that require a clock not affected by the processor and/or memory timings. When internally-clocked devices became available, the ungated clock signal previously used became unnecessary.)
+5 VDC	A-C, 1-3	+5 Vdc Power - Used by system logic circuitry.
+12 VDC	T,16	+12 Vdc Power - Used by system logic circuitry.
-12 VDC	M, 11	-12 VDC Power - Used by system logic circuitry.
A0	40	ADDRESS bus (bit 0) - One of 16 address lines driven by the current BUS MASTER that permits selection of any addressable memory location or peripheral in the system.
A1	$\overline{V}$	ADDRESS bus (bit 1) - Same as A0 on pin 40.
A2	$\overline{U}$	ADDRESS bus (bit 2) - Same as A0 on pin 40.
A3	39	ADDRESS bus (bit 3) - Same as A0 on pin 40.
A4	38	ADDRESS bus (bit 4) - Same as A0 on pin 40.
A5	$\overline{T}$	ADDRESS bus (bit 5) - Same as A0 on pin 40.
A6	$\overline{S}$	ADDRESS bus (bit 6) - Same as A0 on pin 40.
A7	37	ADDRESS bus (bit 7) - Same as A0 on pin 40.
A8	36	ADDRESS bus (bit 8) - Same as A0 on pin 40.

SIGNAL	PINS	SIGNAL DEFINITION
A9	$\overline{R}$	ADDRESS bus (bit 9) - Same as A0 on pin 40.
A10	$\overline{P}$	ADDRESS bus (bit 10) - Same as A0 on pin 40.
A11	35	ADDRESS bus (bit 11) - Same as A0 on pin 40.
A12	34	ADDRESS bus (bit 12) - Same as A0 on pin 40.
A13	$\overline{N}$	ADDRESS bus (bit 13) - Same as A0 on pin 40.
A14	$\overline{M}$	ADDRESS bus (bit 14) - Same as A0 on pin 40.
A15	33	ADDRESS bus (bit 15) - Same as A0 on pin 40.
BA	P	BUS AVAILABLE - An active high signal generated by the SYSTEM MASTER which, along with BS, indicates the current state of the SYSTEM MASTER but does not reflect the status of the system bus (this is done via BUSGNT, pin 15). NOTE: BA, BS states unique to M6809 systems.
BE	J	BUS ENABLE - (E or Phase 2 in earlier system designs.) - An active high clock signal generated by the SYSTEM MASTER. This signal is stretched in the high state while MNRDY* (pin R) is active (low).
BQ	7	BUS QUADRATURE - (M6809, M6809E systems only) (Q or Phase 1 in earlier system designs.) A timing signal which leads BE.
BS	23	BUS STATUS - This signal, in conjunction with the BA signal (pin P), reflects the SYSTEM MASTER halt, interrupt, and sync states.
BUSGNT	15	BUS GRANT - An active high signal generated by the SYSTEM MASTER, which acknowledges the request for the system bus, generated via BUSREQ*, and indicates the granting of bus access. This signal tightly controls access to the system bus. The signal is held inactive (low) during refresh grant cycles.

BA	BS	STATE
0	0	Normal (Running)
0	1	Interrupt Acknowledge
1	0	Sync Acknowledge
1	1	Halt or Bus Grant

SIGNAL	PINS	SIGNAL DEFINITION
BUSREQ*	N	BUS REQUEST - (TSC* in earlier M6800 systems.) An active low, wired-OR signal that requests access to the system bus. An active (low) state on this line will cause the SYSTEM MASTER to release the data, address, VMA, VUA, VXA, and R/W lines. A BUSGNT signal (pin 15) will also be generated after the fall of BE.
D0*	31	DATA bus (bit 0) - One of eight bidirectional data lines which provide a two-way data transfer path between the BUS MASTER and all modules in the system. The data bus drivers on various modules are in the off or high impedance state except when selected during a data transfer operation. Data bus drivers should drive the data bus coincident with BE (phase 2) asserted.
D1*	29	DATA bus (bit 1) - Same as D0* on pin 31.
D2*	$\overline{K}$	DATA bus (bit 2) - Same as D0* on pin 31.
D3*	$\overline{H}$	DATA bus (bit 3) - Same as D0* on pin 31.
D4*	32	DATA bus (bit 4) - Same as D0* on pin 31.
D5*	30	DATA bus (bit 5) - Same as D0* on pin 31.
D6*	$\overline{L}$	DATA bus (bit 6) - Same as D0* on pin 31.
D7*	$\overline{J}$	DATA bus (bit 7) - Same as D0* on pin 31.
DEBUG*	14	DEBUG - A static, active low signal which indicates that a debug module is in the system.
FIRQ*	$\overline{A}$	FAST INTERRUPT REQUEST (M6809, M6809E systems only) - An active low, wired-OR, level-sensitive signal that requests the generation of a SYSTEM MASTER fast interrupt sequence. The SYSTEM MASTER will wait until the instruction being executed is completed before recognizing the request. At that time, if the interrupt is not masked, the SYSTEM MASTER will begin the interrupt sequence. This sequence is fast in the sense that it stacks only the return address and condition codes.
GND	X-Z,$\overline{W}$-$\overline{Y}$, 20-22,41-43	GROUND
4	HALT*	HALT - An active low, wired-OR signal which halts the SYSTEM MASTER at the end of the present instruction. The halt condition, indicated through BA (pin P) and BS (pin 23), does not grant access to the system bus. Refer to BUSREQ* (pin N) and BUSGNT (pin 15).

SIGNAL	PINS	SIGNAL DEFINITION
IRQ*	D	INTERRUPT REQUEST - An active low, wired-OR, level-sensitive signal that requests the generation of an interrupt sequence by the SYSTEM MASTER. The SYSTEM MASTER will continue normal operation until it completes the current instruction before it recognizes the request. At that time, if the SYSTEM MASTER is accepting interrupts, it will start executing the interrupt sequence.
LIC	S	LAST INSTRUCTION CYCLE (M6809E systems only) - An active high signal produced by the M6809E microprocessor during the last cycle of each instruction. This line will be in the high impedance state during the BUSGNT state. Not recommended for new design.
MEMCLK	L	MEMORY CLOCK - This pin should not be used in any new peripheral board designs. Any new processor board design should provide BE on this pin as well as pin J if compatibility with older Micromodules within the system is desired.
MNRDY*	R	MEMORY NOT READY (MEMRDY in early EXORcisers) - An active low, wired-OR signal that permits the system to work with slow memory modules. When this signal is low, the clocks will be stretched with BE active (high) and BQ (if provided) inactive (low).
NMI*	E	NONMASKABLE INTERRUPT - An active low, wired-OR, edge-sensitive signal that requests the generation of a nonmaskable interrupt sequence by the SYSTEM MASTER. The SYSTEM MASTER will continue normal operation until it completes the current instruction before it recognizes the request. At that time, regardless of the state of any interrupt masks, the SYSTEM MASTER will begin executing the nonmaskable interrupt sequence.
PARERR*	W	PARITY ERROR - This active low, wired-OR signal is normally held high. If a memory module that incorporates a parity check circuit is used within the system and a parity error is detected, this signal will be forced low.
PWRFAIL*	V	POWER FAIL - This active low, wired-OR signal is used by battery backup memory modules. When this signal goes active (low), it disables the write function of the protected memory module.
R/W*	6	READ/WRITE - An active high (read operation) or active low (write operation) signal generated by the current BUS MASTER, which indicates to modules in the system the action the current BUS MASTER is taking and the direction of data transfer.

SIGNAL	PINS	SIGNAL DEFINITION
REFGNT	13	REFRESH GRANT - An active high signal which acknowledges the request for a refresh cycle and indicates the refresh grant cycle. While REFGNT is active (high), BUSGNT is to be held inactive (low). The SYSTEM MASTER is inactive during the REFGNT cycle.
REFREQ*	12	REFRESH REQUEST - An active low, wired-OR signal which requests a bus cycle for the refresh of dynamic memory modules. Refer to REFGNT (pin 13).
RESET*	5	RESET - An active low, wired-OR signal used to reset the SYSTEM MASTER and other peripheral devices and system modules. This signal starts the initialization of the system when power is initially applied. Depressing any RESET pushbutton switch while the system is operating will generate a RESET* signal and cause the SYSTEM MASTER to execute the restart routine.
STANDBY	U,17	+5 Vdc STANDBY Power (+12V in early EXORcisers) - This line is used with battery backup memory modules. If battery backup is not required, the STANDBY line should not be used for any other purpose.
VMA	F	VALID MEMORY ADDRESS - An active high signal generated by the current BUS MASTER to indicate the presence of a valid memory address on the bus. The SYSTEM MASTER must maintain this line in the high impedance state while BUSGNT (pin 15) is active (high).
VUA	10	VALID USER ADDRESS - An active high signal generated by the current BUS MASTER to indicate the presence of a valid user address on the bus. The SYSTEM MASTER must maintain this line in the high-impedance state while BUSGNT (pin 15) is active (high). On-board memory and I/O may be placed in the user memory map through strap selection.
VXA	19	VALID EXECUTIVE ADDRESS - An active high signal generated by the current BUS MASTER when the system is operating in the multi-map mode and the program is addressing the executive portion of the memory map. Additionally, all peripheral modules (such as memories) must be set to respond to the VXA signal if the user wants to operate those modules in the executive portion of the map.

NOTE: Overscore pin letters denote lower case letters (i.e., $\overline{A}$ = a).

APPENDIX D

STANDARD I/O CONNECTOR PINOUTS

D.0 INTRODUCTION

Micromodules allow the user to connect up to five I/O connectors to the top edge of the Micromodule PC board. Five standard I/O connectors are identified in this appendix. Tables D-1 through D-5 show the pinouts for these connectors. NOTE: Refer to specific product manual for specific signals supported.

D.1 SERIAL I/O PORT

The serial port is basically configured for an RS-232C interface. On some Micromodules, the serial port is also configurable for user-selected RS-422 and RS-423 interfaces. The EXORbus specification calls for a 20-conductor, card edge connector with the keying slot between pins 7 and 9. Table D-1 and Figure D-1 list the signal names and pinouts for an RS-232C interface. Table D-2 and Figure D-2 list the signal names and pinouts for an RS-422/RS-423 interface. These pinouts allow for differential drivers and receivers. For single-ended drivers, such as RS-232C, use the positive pin.

D.2 TIMER PORT

The timer port I/O connector allows the various inputs and outputs of the MC6840 triple-timer to be brought out through a cable to front panel controls or to a chassis mounted connector for external access. The timer port is also a 20-conductor, card edge connector, but differs from the serial port in that the keying slot is between pins 3 and 5. This prevents inadvertent interchanging of the serial port and timer port connectors. Refer to Table D-3 for signal names and pin numbers.

D.3 PARALLEL PRINTER PORT

The printer port is a 50-conductor, card edge connector that has a pin configuration compatible with the Centronics type parallel printer interface. Pin identification and inputs/outputs correspond to this printer interface requirement. Table D-4 gives specific pin numbers and signal descriptions. The EXORbus specification calls for the keying slot in this 50-conductor, card edge connector to be between positions 7 and 9.

D.4 PARALLEL INDUSTRIAL I/O PORT

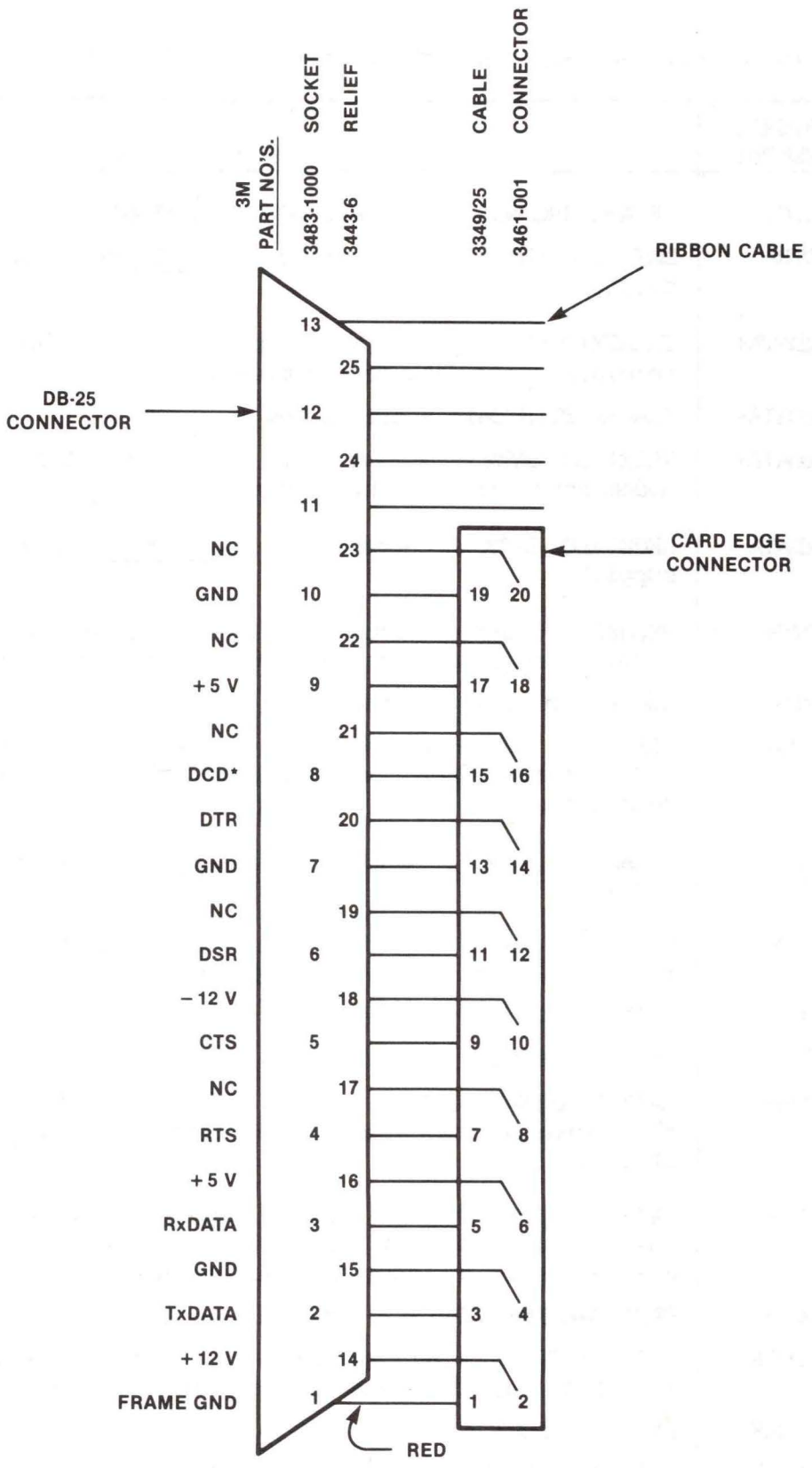
The parallel industrial I/O port is a 50-conductor, card edge connector. Its pinouts are such that a mass terminated ribbon cable may be used to interconnect this port with the industrial standard parallel I/O boards (Crydom model MS-16 or Opto 22 model PB-16). These boards contain up to 16 input or output channels of optically isolated interface. The keying slot for this 50-conductor, card edge connector is between positions 3 and 5. Refer to Table D-5 for signal names and pin numbers.

TABLE D-1. RS-232C Serial Interface Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1	N.C.	(FRAME GROUND ONLY - MAKE NO CONNECTION).
2	+12V	OPTIONAL jumper to +12 VDC supply (see NOTE).
3	TxDATA	TRANSMITTED DATA - The line through which the terminal sends data to the modem.
4	GND	GROUND - Signal and power return.
5	RxDATA	RECEIVED DATA - The line through which the modem sends data to the terminal.
6	+5V	OPTIONAL jumper to +5 VDC supply (see NOTE).
7	RTS	REQUEST TO SEND - The line through which the terminal requests permission to transmit data to the modem.
9	CTS	CLEAR TO SEND - The line through which the modem acknowledges the acceptance of a terminal request to send data.
10	-12V	OPTIONAL jumper to -12 VDC supply (see NOTE).
11	DSR	DATA SET READY - The line through which the modem indicates its on-line, in-service, or active status.
13	GND	GROUND - Signal and power return.
14	DTR	DATA TERMINAL READY - The line through which the terminal indicates its on-line, in-service, or active status.
15	DCD	DATA CARRIER DETECT - The line through which the modem indicates that its interfacing communications channel is in an acceptable active state.
17	+5V	OPTIONAL jumper to +5 VDC supply (see NOTE).
19	GND	GROUND - Signal and power return.
8,12,16, 18,20	N.C.	NO CONNECTION

NOTE: OPTIONAL jumpers, normally not connected, to be connected upon specific requirement.

CAUTION: DO NOT CONNECT A STANDARD RS-232 DEVICE WITH OPTIONAL POWER CONNECTIONS INSTALLED, SINCE SYSTEM COMPONENTS COULD BE DAMAGED.



KEY: RS232 TERMINOLOGY

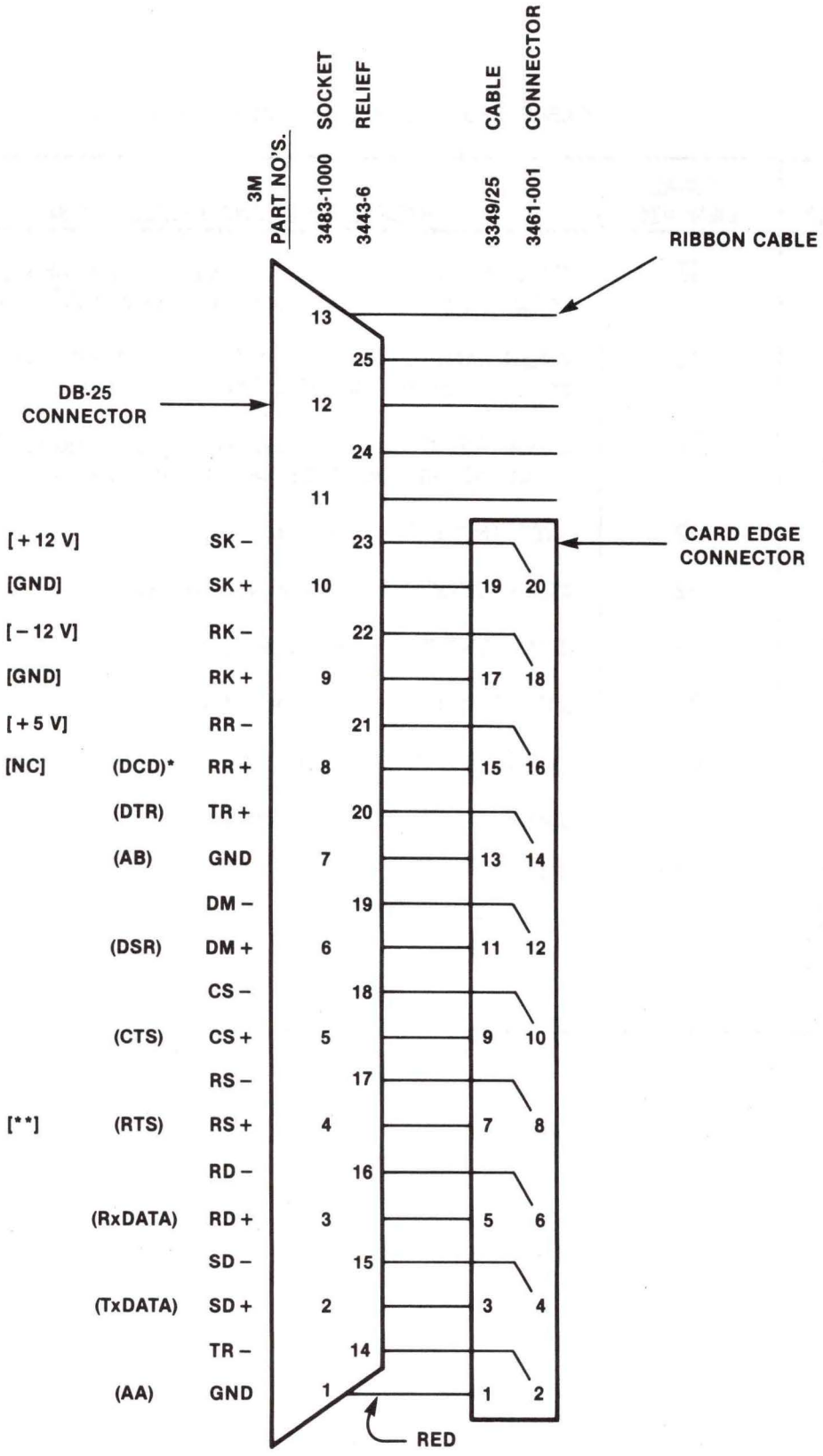
NOTES: *DCD IS A BELL 202 MODEM TERM.
NC - NO CONNECTION IS TO BE MADE.

FIGURE D-1. RS-232C Serial Interface Cabling Diagram

TABLE D-2. RS-449/RS-422/RS-423 Serial Interface Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1	N.C.	(FRAME GROUND ONLY - MAKE NO CONNECTION)
2	DTR-	DATA TERMINAL READY - active low (OPTIONAL jumper to +12 VDC supply)
3	TxDATA+	TRANSMITTED DATA - active high - the line through which the terminal sends data to the modem.
4	TxDATA-	TRANSMITTED DATA - active low
5	RxDATA+	RECEIVED DATA - active high - the line through which the modem sends data to the terminal.
6	RxDATA-	RECEIVED DATA - active low (OPTIONAL jumper to +5 VDC supply)
7	RTS+	REQUEST TO SEND - active high - the line through which the terminal requests permission to transmit data to the modem.
8	RTS-	REQUEST TO SEND - active low
9	CTS+	CLEAR TO SEND - active high - the line through which the modem acknowledges the acceptance of a terminal request to send data.
10	CTS-	CLEAR TO SEND - active low (OPTIONAL jumper to -12 VDC supply)
11	DSR+	DATA SET READY - active high - the line through which the modem indicates its on-line, in-service, or active status.
12	DSR-	DATA SET READY - active low
13	GND	GROUND - signal return
14	DTR+	DATA TERMINAL READY - active high - the line through which the terminal indicates its on-line, in-service, or active status.
15	DCD+	DATA CARRIER DETECT - active high - the line through which the modem indicates that its interfacing communications channel is in an acceptable active state.
16	DCD-	DATA CARRIER DETECT - active low
17	RDCLK+	RECEIVE CLOCK - active high - the line to be used to clock in and synchronize data into the terminal.
18	RDCLK-	RECEIVE CLOCK - active low
19	TDCLK+	TRANSMIT CLOCK - active high - the line to be used to clock in and synchronize data into the modem.
20	TDCLK-	TRANSMIT CLOCK - active low

NOTE: Mnemonics reflect RS-232 signal name abbreviations. Correspondence between RS-449 and RS-232C signal mnemonics are those given in EIA Bulletin No. 12, "Application Notes on Interconnection Between Interface Circuits using RS-449 and RS-232C", dated November 1977.



KEY: RS-449 TERMINOLOGY (RS-232C INITIALS) [MM11 CURRENT LOOP INTERFACE CONNECTION]

NOTES: *DCD IS A BELL 202 MODEM TERM.
NC - NO CONNECTION IS TO BE MADE.

'+'-SIGNAL VOLTAGE HIGH WHEN ACTIVE. '–'-SIGNAL VOLTAGE LOW WHEN ACTIVE.
**THIS SIGNAL IS USED TO CONTROL THE TTY READER WHEN USING MM11 AND IS THUS INCOMPATIBLE WITH THE RS-232C STANDARD (AN OUTPUT WHICH IS DEFINED AS AN INPUT).

FIGURE D-2. RS-449/RS-422/RS-423 Serial Interface Cabling Diagram

TABLE D-3. Timer Interface Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
1	$\overline{G1}$	GATE INPUT 1 - Low level asynchronous TTL compatible input signal as trigger or clock gating to Timer.
3	01	TIMER OUTPUT 1 - High level output from PTM capable of driving up to two TTL loads.
5	$\overline{C1}$	CLOCK INPUT 1 - Low level asynchronous TTL voltage level input signal used to decrement Timer.
7	$\overline{G2}$	GATE INPUT 2 - Same as pin 1.
9	02	TIMER OUTPUT 2 - Same as pin 3.
11	$\overline{C2}$	CLOCK INPUT 2 - Same as pin 5.
13	$\overline{G3}$	GATE INPUT 3 - Same as pin 1.
15	03	TIMER OUTPUT 3 - Same as pin 3.
17	$\overline{C3}$	CLOCK INPUT 3 - Same as pin 5.
2,4,6, 8,10, 12,14, 16,18, 19,20	GND	GROUND

TABLE D-4. Parallel Printer Interface Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
All even pins plus pins 3,7, 41,45, & 49	GND	GROUND - Signal return line.
1	INPUT PRIME*	INPUT PRIME - Output used for priming printer (normally in high state). (This is CB2 signal from the PIA.)
5	FAULT*	Printer FAULT signal - This low-going, edge-sensitive input indicates a printer fault. (This is signal CB1 to the PIA.)
9	PB7	PERIPHERAL DATA line, Section B, bit 7 - Input or output. A logic 0 in bit 7 of the B data direction register makes this line function as an input, while a 1 makes it function as an output.
11	PB6	PERIPHERAL DATA line, Section B, bit 6 - Same as PB7 except controlled by bit 6 of the B data direction register.
13	PB5	PERIPHERAL DATA line, Section B, bit 5 - Same as PB7 except controlled by bit 5 of the B data direction register.
15	PB4	PERIPHERAL DATA line, Section B, bit 4 - Same as PB7 except controlled by bit 4 of the B data direction register.
17	PB3	PERIPHERAL DATA line, Section B, bit 3 - Same as PB7 except controlled by bit 3 of the B data direction register.
19	BUSY	Printer BUSY input signal. (This is signal PB2 of the PIA.)
21	PAPER OUT	PAPER OUT - This input signal indicates the printer is out of paper. (This is signal PB1 of the PIA.)
23	SEL	Printer SELECTED input signal. (This is signal PB0 of the PIA.)
25	PD7	PERIPHERAL DATA line, bit 7 - Input or output. A logic 0 in bit 7 of the A data direction register makes this line function as an input, while a 1 makes it function as an output.
27	PD6	PERIPHERAL DATA line, bit 6 - Same as PD7 except controlled by bit 6 of the A data direction register.

TABLE D-4. Parallel Printer Interface Signals (cont'd)

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
29	PD5	PERIPHERAL DATA line, bit 5 - Same as PD7 except controlled by bit 5 of the A data direction register.
31	PD4	PERIPHERAL DATA line, bit 4 - Same as PD7 except controlled by bit 4 of the A data direction register.
33	PD3	PERIPHERAL DATA line, bit 3 - Same as PD7 except controlled by bit 3 of the A data direction register.
35	PD2	PERIPHERAL DATA line, bit 2 - Same as PD7 except controlled by bit 2 of the A data direction register.
37	PD1	PERIPHERAL DATA line, bit 1 - Same as PD7 except controlled by bit 1 of the A data direction register.
39	PD0	PERIPHERAL DATA line, bit 0 - Same as PD7 except controlled by bit 0 of the A data direction register.
43	DATASTB*	DATA STROBE - This output signal, used to strobe the printer, is a negative pulse at least 1 microsecond long. (This is signal CA2 from the PIA.)
47	ACK*	ACKNOWLEDGE - Data accepted input signal. (This is signal CA1 to the PIA.)

TABLE D-5. 50-Conductor Parallel Industrial I/O Port Interface Signals

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME AND DESCRIPTION
All even pins	GND	GROUND - Signal and power return line
1,49	+5V	+5 Vdc
47	IO0	I/O line #0
45	IO1	I/O line #1
43	IO2	I/O line #2
41	IO3	I/O line #3
39	IO4	I/O line #4
37	IO5	I/O line #5
35	IO6	I/O line #6
33	IO7	I/O line #7
31	IO8	I/O line #8
29	IO9	I/O line #9
27	IO10	I/O line #10
25	IO11	I/O line #11
23	IO12	I/O line #12
21	IO13	I/O line #13
19	IO14	I/O line #14
17	IO15	I/O line #15
15	CA1	Buffered PIA CA1 input
13	CA2	Buffered PIA CA2 input/output
11	CB1	Buffered PIA CB1 input
9	CB2	Buffered PIA CB2 input/output
7,5,3	NC	Not used

APPENDIX E

EXORbus APPLICATIONS INFORMATION

E.1 INTRODUCTION

Due to the growth in microprocessor development and theory, EXORbus has gone through an evolutionary process. Because of this, some of the older designs are not perfectly compatible with the newest developments. To aid the user in building systems that use a broad mix of such designs, this appendix documents some minor modifications which will bring various boards into compliance with each other.

E.1.1 Design Consideration and Caution

Designers of new peripheral boards that are to be compatible with older, MC6800- or MC6802-based processor boards are reminded that these early MPU boards are not necessarily EXORbus Specification compatible. Some early M6802-based Micromodules may not respond to MNRDY*, and may not meet other specification requirements pertaining to address and data setup times.

E.1.2 The EXORciser Systems

The basic components of an EXORciser are the MPU and DEbug modules, which are augmented by numerous memory and I/O modules. The design concept of the MPU module is to provide the same signals to the EXORbus that an MC6800 microprocessor provides, but with sufficient drive to operate with a full complement of modules.

A number of mechanical and electronic standards are as follows:

a. Any EXORbus module can be used in any chassis slot.

b. TTL-level signals are used.

c. Three-state bus concepts are used with an 8-bit bidirectional data bus and a 16-bit address bus. The data bus uses inverting drivers.

d. A two-phase clock is used, with both phases provided on the bus at TTL levels.

e. Refresh circuitry is provided for cycle-stealing dynamic RAM's, as well as a similar memory-ready circuit for use with slow memory. A continuous clock signal (MEMCLK) is supplied, which leads phase 2 by about 40 nanoseconds.

E.1.2.1 EXORciser I. The DEbug module provides several unique features which must be understood to design compatible modules. To permit evaluation of any M6800 system, RAM is at the top of the memory map, with circuitry to work with less than fully decoded devices. The EXbug monitor program provides intelligent debugging features. All of the memory and I/O addressable locations

on the DEbug module are above $F000 in the map, leaving over 60,000 bytes for the user system. One of the features is that the VMA signal from the MPU is routed through the DEbug module and becomes VUA for use by all other modules. Logic on the DEbug module inhibits the VUA signal whenever EXbug is addressed. This allows less than full decoding to be used on any user-designed module.

The concept depends on redundant addressing, as typically done in most simple M6800 systems, which allows accessing the vectors even though the program reside and runs at some address below $F000. If fully decoded RAM modules are used, a means is provided to move the vectors up to the RAM at $FFF8 and above.

E.1.2.2 EXORciser II. Because some users start their designs and actually have hardware built before they realize they need a development system (or possibly because they do not understand how the EXORciser can be used), the concepts are expanded in EXORciser II to provide a dual map. The DEbug II Module provides the ability to address two separate 64K-maps, as illustrated in Figure E-1. The DEbug II module uses the Valid Memory Address (VMA) signal from the MPU II modue and converts it to two signals -- Valid User Address (VUA) and Valid Executive Address (VXA). The memory and I/O modules for this system have jumpers which allow them to be used with either signal, thus providing two complete maps. EXbug resides in the executive map, along with the floppy disk controller and printer interface, leaving the entire user map available. A switch is provided on the DEbug II module to select single map mode and can be used in the same way as EXORciser I. All memory above $F000 is enabled by VXA; all memory below $F000 is enabled by VUA.

E.1.2.3 Micromodules. When a Micromodule system is assembled, it is necessary to test and develop the control program and verify its operation with the I/O circuits of the modules. This could be done with a separate EXORciser and a User System Evaluator (USE), but it can also be done much more economically by plugging a DEbug I or II module into the same chassis. Micromodules operate as MPU's with a DEbug I or II module. If used without the EXORciser II MPU module, EXORbus pin 15 must be grounded.

Micromodules have been designed to use the single map mode of the EXORciser for system development. This is accomplished by setting up the Micromodule memory map so that it does not interfere with EXbug or the other devices on the DEbug I or II module. Some Micromodules do not occupy the map above $F000, but others are arranged so that the map is switched when a DEbug module is used on the bus. EXORbus pin 14 (DEBUG*) is grounded on the DEbug II module and is used by the address decoders of other modules to automatically switch ROM sockets out of the map.

Modules designed to be used on an EXORbus should be enabled by the VMA, VUA, or VXA signal. Modules should not be designed to use VMA only, since that would prohibit the use of the DEbug module.

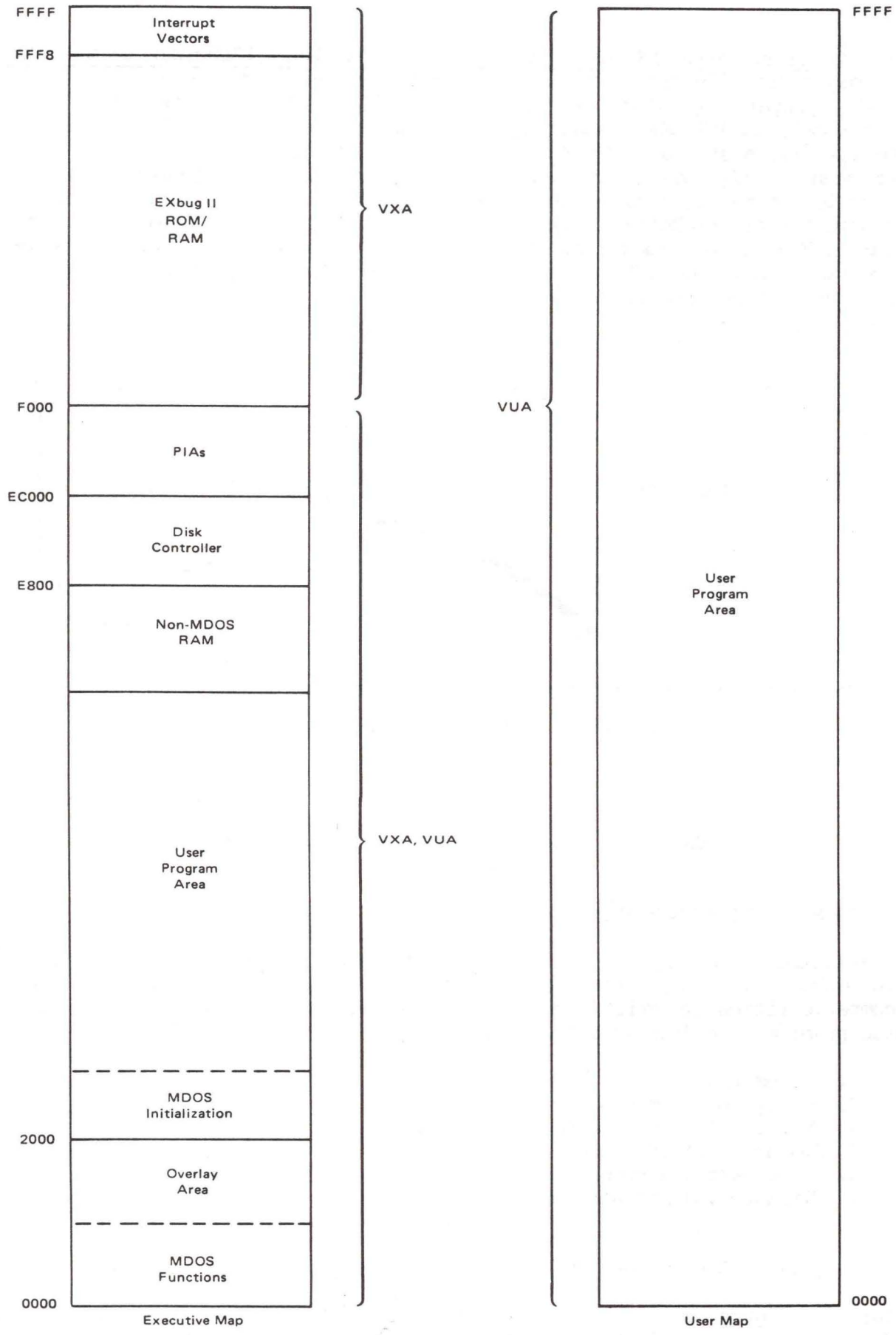


FIGURE E-1. Dual Memory Map for User System

E.1.2.4 Using M6800 EXORciser I Modules in the M6809 EXORciser or with MM19. Dual map capability requires that all peripherals and memories must be assigned to the proper map (VUA or VXA). All EXORciser I modules will respond automaticaly to VUA when operating at 1 MHz or less in an M6809 EXORciser (or EXORciser II) system or with MM19. In order to assign these modules to VXA, the user must modify the individual modules by cutting and jumpering a single connection at the edge connector of the EXORciser I module. The modification is the same for all EXORciser I modules, and is illustrated in Figure E-2. Cut the incoming VUA signal track from pin 10 near the edge connector finger. Solder a jumper wire from the VXA signal track (pin 19) to the circuitry side of the track cut just performed.

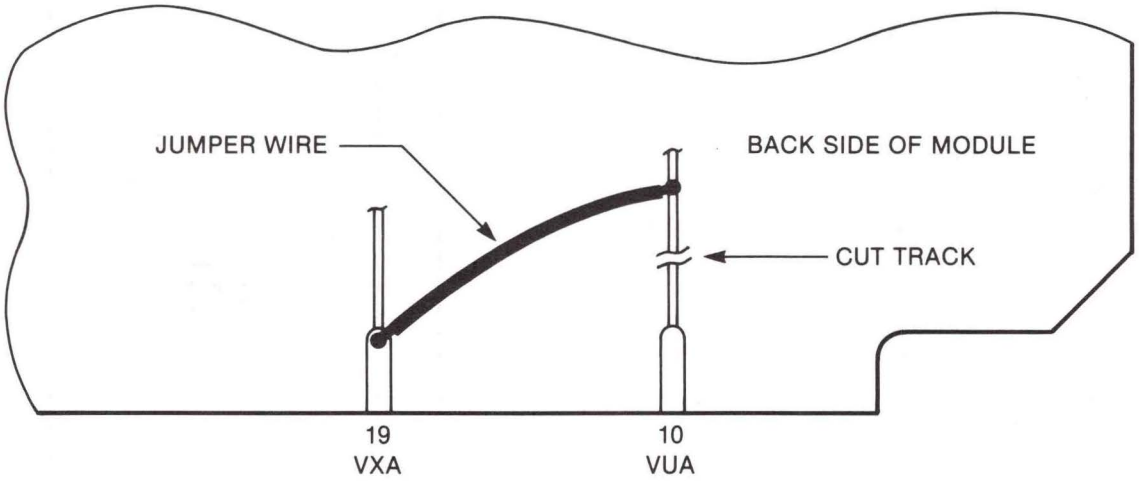


FIGURE E-2. Assigning EXORciser I Modules to VXA

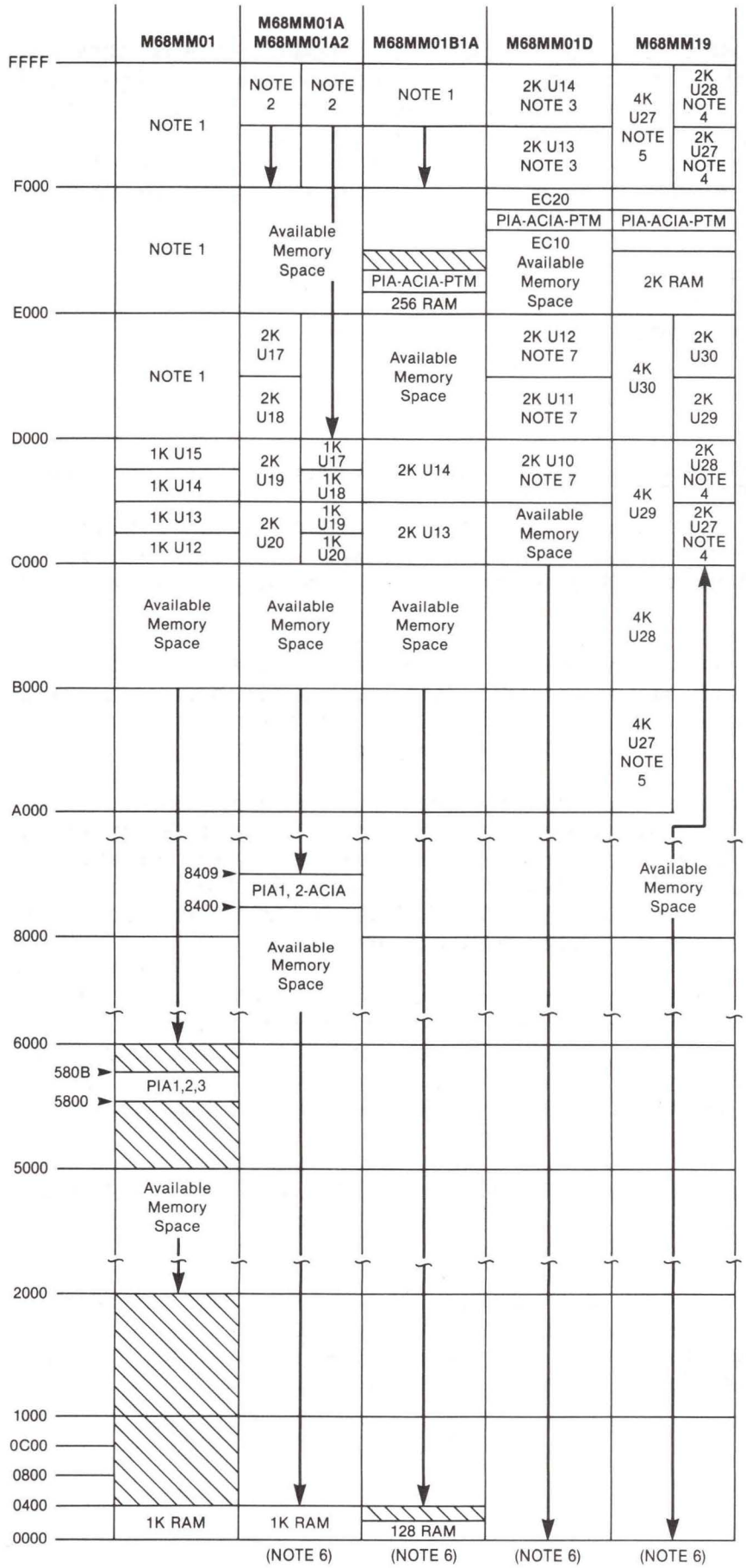
E.2 COMPATIBILITY PROBLEMS

The Micromodule family of products were designed to be fully compatible with each other and with development systems such as the EXORciser. A few incompatibilities do exist, and may be handled as described in this chapter. These problems are discussed in six categories:

1. System I/O
2. Memory requirements
3. Type of MPU and related bus signals
4. System operating speed
5. Other hardware problems
6. Firmware and software problems

E.2.1 System I/O Problems

Refer to Figure E-3 for memory map locations of I/O ports on various Micromodules (MM). Following are additional specific I/O problems.



M68MM--	As Shipped Base Addr.	Size	Modulo (Base)
03	9FFC	4	4 (9E00)
			4 (8E00)
04	A000	8K	8K (0000)
	C000	8K	8K (2000)
04A	8000	8K	8K/16K
	C000	8K	
05A	EF00	16	16 (0000)
05B	EF00	32	32 (0000)
05C	EF00	8	8 (0000)
06	7800	2K	2K (0000)
07	EC20	8	8 (8C00)
09	0000	4K	4K (0000)
10RTC	EC40	64	64 (0000)
12	B800	2K	2K (0000)
12A	—	8	8 (0000)
13A	91FE	2	2 (0000)
13B	91FC	4	4 (0000)
13C,D	90FC	4	4 (0000)
14	EC30	4	4 (0000)
15A,A1	9D00	4	4 (0500)
15B	9D10	4	4 (0500)
15C	9D08	8	8 (0500)
DISK	E800	1K+6	—
PROM PR.	EC08		—
SYST. AN.		528	—
MACE	EE10	8	—

NOTES

1. Ambiguous ROM Addresses
2. Ambiguous ROM Addresses if NOT used with DEbug board
3. Removed from map when used with DEbug board
4. U27 & U28 moved from F000 to C000 when used with DEbug board
5. U27 moved from F000 to A000 when used with DEbug board
6. Address Map may be modified by a reprogrammed device as follows:
   MM1A, A2 — 82S129 PROM
   MM1B1A — 2ea 82S129 PROMs
   MM1D — 82S103 FPGA
   MM19 — 82S100 FPLA
7. Sockets U10, 11 & 12 may be disabled to extend Available Memory Space

▨ Not available

FIGURE E-3. Micromodule Composite Memory Map

E.2.1.1 MM03 I/O Module. MM03, the 32/32 input/output module, has no inherent data readback capability, since the outputs of the module are not physically connected to the inputs. Therefore, when using any software routine with a readback capability (i.e., EXbug, MINIbug, MIKbug, etc.), no readback is possible unless the user connects the outputs to the inputs. If the outputs are jumpered to the input, the simple program loop provided below can be used to provide the readback operation.

```
LDAA #(some data pattern)
STAA (desired output location)
LDAB (corresponding input location)
CBA
BNE FAIL
```

E.2.1.2 MM12 and MM12A GPIB Modules. MM12 and MM12A are a Listener/Talker/Controller and a Listener/Talker conforming to the GPIB (IEEE-488 bus). The GPIB standard is intended to allow the interconnection of independently-manufactured apparatus into a single functional system. The user should be aware of the following problems that may be encountered when attempting to build a system.

PROBLEM #1 - The IEEE-488 bus is designed to allow instruments on it to talk directly to one another without having to route data through the bus controller. The specification provides a means for doing this, but it does not define what the format of the data will be. This could lead to problems.

When purchasing instruments for his system, the user should obtain vendor documentation which defines the data format used by the device. In many cases, the vendor will be willing to provide the instrument with a custom format. If the format is found to be incompatible, it is still possible to use the controller's companion talker and listener interfaces to translate from one format to another. However, this will slow down bus operation.

PROBLEM #2 - Although the GPIB standard defines a very broad spectrum of capabilities, many devices will implement only a subset of these. The user may purchase two devices which utilize different subsets and are thus incompatible to some degree. At best, this might mean that some function of a given device could not be utilized. At worst, it might prevent the bus from functioning at all.

Avoid purchasing instruments which work only in the TALK ONLY or LISTEN ONLY modes, unless you intend to use them only in systems with no controller.

Purchase a controller with complete capability, if possible (C1, C2, C3, C4, and C5 subsets). See the IEEE-488-1978 bus specification. MM12 implements this fully. This will minimize incompatibility problems between the controller and each device. If some incompatibility is then encountered between two devices, the controller may be used as a go-between, as in Problem #1.

E.2.1.3 MM11 Interface Module. MM11 converts an RS-232C serial data port to a 20-mA current loop serial data port. This will require that the ±12 Vdc power at the appropriate pins on the system bus be routed to the serial data port edge connector(s). (See Appendix D.) MM11 is intended to be used with the RS-232C serial data port on an M6800 or M6809 DEbug II Module, Micromodules 01A, 01A2, 01B1A, 01D, or 19, or other board that has been properly modified. Refer to the appropriate user's guide for modification instructions. MM11 can be connected to the TTY by using a connector (Cinch 50-6A-20, or equivalent) on P2, or by soldering the cable to the plated-through holes provided on the board. See also the MM11 User's Guide for the required TTY modifications.

NOTE

The TTY or other 20-mA device connected to P2 of MM11 must have a -12 Vdc return to P2 pin 5. The 20-mA device must be passive, and will use the power provided by MM11.

E.2.1.4 MC68000 Design Module with Micromodule Boards, Chassis, and/or Card Cages. The MC68000 Design Module (MEX68KDM) uses system bus pins C, D, E, F, 25, 26, 27, and 28 for its upper data bits, D08 through D15. Some or all of these pins are used as external address select lines by Micromodules 03, 04, 04A, 06, and 09. Similarly, Micromodules 05A, 05B, and 05C use pin C as a test point. Finally, Micromodules 10B, 10C, and 12A have MEMRDY on pin R, and the MEX68KDM has Bus Grant Acknowledge (BGACK) on pin R. These boards and enclosures can be used together as follows:

a. When Micromodules 03, 04, 04A, 06, and/or 09 are used with the MEX68KDM in an EXORciser or a Front Loading Chassis, remove the isolation diodes associated with the address select pins on the Micromodule. (See the schematics in the individual board user's guide for address select details.) To use Micromodules 05A, 05B, and/or 05C in such a system, cut the track connecting to pin C.

b. Micromodules 03, 04, 04A, 05A, 05B, 05C, 06, and/or 09 may be used with the MEX68KDM in a Long Chassis, Short Chassis, or 5- or 10-card Card Cage without any modification, because these chassis and card cages do not bus the address select pins together.

c. If additional memory boards are used with the MEX68KDM in a Micromodule Long or Short chassis or card cage, the pins associated with the eight additional data lines must be bussed between the slots containing the Design Module and the memory board associated with the upper eight data bits.

   One slot must be assigned to the MEX68KDM, and the required number of slots assigned to the memory board and their bus adapter modules. Jumper wires must then be installed on the motherboard to bus together the eight lines C, D, E, F, 25, 26, 27, and 28 for these assigned slots. If the motherboard does not have a header installed in the address select locations, these jumpers can be soldered into the eight feed-through holes connected to the bus connector. If headers have been installed, they should be removed and jumper wires installed.

d. Micromodules 10B, 10C, and 12A can be used with the MEX68KDM only if the signal track is cut above pin R on the MM10B, 10C, or MM12A edge connector to disable the MEMRDY signal. This must be done because the MEX68KDM uses pin R for a BGACK. In addition, MM10B and 10C interrupt output must be connected to NMI or IRQ, rather than FIRQ, because the MEX68KDM has AS on pin A, while MM10B and MM10C has FIRQ.

E.2.2 Memory Requirement Problems

Refer to Figure E-3 for general memory map considerations for Micromodules. Following are additional specific memory board problems.

E.2.2.1 MM04A ROM/EPROM Module. Micromodule 4A, a ROM/EPROM module, may operate at higher system speeds (1.5 MHz and 2.0 MHz) even when it uses slow memory chips, if it is modified as described in its User's Guide. MM04A has provisions for working at 1.5 MHz or 2.0 MHz with either MM19A or the MEX6800-2 MPU II Module or a system that uses an MC6871 clock chip.

E.2.2.2 8K Dynamic RAM Module MEX6815-1. The early 8K Dynamic RAM Module (MEX6815-1) requires some precaution, as well as modification, before use in an M6809 system or with Micromodule 19, 09, 10B, or 10C. This module transfers data asynchronously. The 8K Dynamic RAM Module (MEX6815-1) may be used in the M6809 EXORciser or with MM19, MM09, MM10B, or MM10C if the following precautions are taken and changes made.

If any difficulty is encountered using MEX6815-1 memories with newer memories, a quick check should be made of the refresh time. Sixty-microsecond timing cannot be used with newer modules, and a a few early versions of the 8K Dynamic RAM Modules (MEX6815-1) used a 60-microsecond refresh cycle. (This was changed to 30 microseconds on later MEX6815-1 modules by changing R25 to 110K ohms, 1%.)

Also important when mixing dynamic RAM's is the early MEX6815-1 requirement to provide +12 Vdc to the battery backup signal (pin U on EXORciser I bus). On EXORciser I, this bus signal was normally jumpered to +12 Vdc (pin T) when the product was manufactured. In the M6809 EXORciser and in MM19, MM09, MM10B, and MM10C, pin U is still designated as STANDBY, but is not jumpered to +12 Vdc at the factory (since the application is more general). When using MEX6815-1 dynamic RAM's with MM19, MM09, MM10B, or MM10C, or in an M6809 EXORciser chassis, the user must re-arrange the module +12 Vdc track connections, as illustrated in Figure E-4, and perform the following modifications:

a. If jumper wires exist between pins T and U (front side of module) or pins 16 and 17 (back side of module), cut or remove the applicable jumper wire.

b. Cut the incoming +12 Vdc track from pin 17 near the edge connector finger.

c. Solder a jumper wire from pin 16 to the +12 Vdc feed-through terminal on the back side of the module.

d. Solder a jumper wire from pin T to the same +12 Vdc feed-through terminal on the front side of the module.

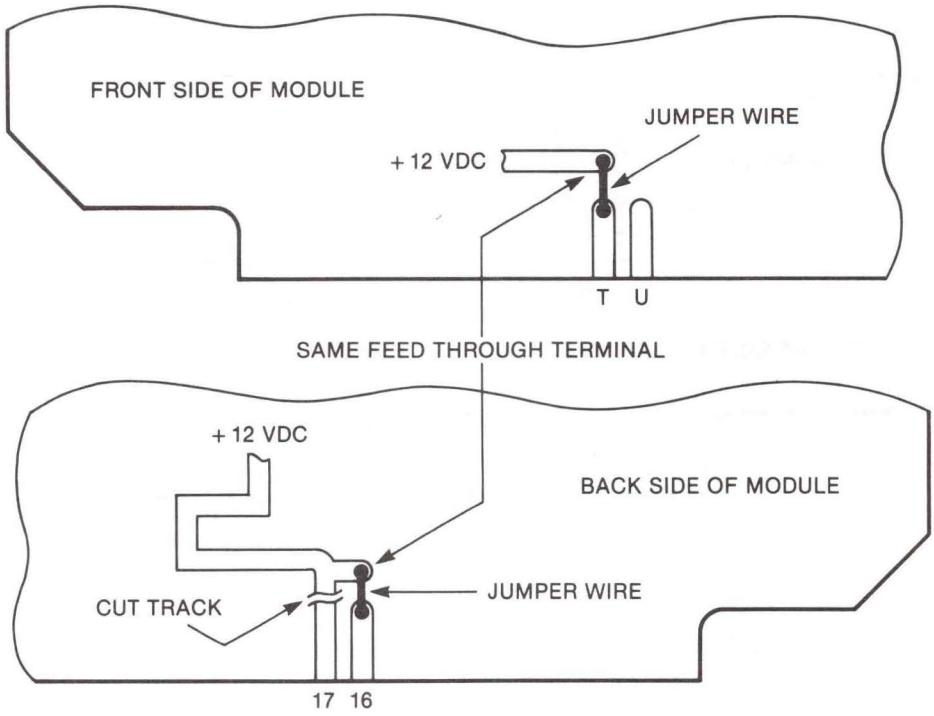


FIGURE E-4. +12 Vdc Modification to 8K Dynamic RAM Module (MEX6815-1)

When using MEX6815-1 modules with other dynamic RAM's (including Series II RAM modules), the MEX6815-1 module must be assigned as the master in the system.

Pin S on the M6809 EXORciser bus has been redefined as the M6809E Last Instruction Cycle (LIC) signal. Previously, this line was used by the MEX6815-1 modules, and was identified as a Refresh Clock (REF CLK) signal. The MEX6815-1 module is the only module which uses this signal. To avoid multi-signal conflicts on this line, simply disable the LIC line from the M6809 MPU Module by removing jumper connection K8 on the MPU Module.

When working with the MC68B09E MPU, the user has two options to avoid multi-signal conflicts. First, the user can use the method explained above. Make sure there are no modules in the system requiring the LIC signal, then disable the LIC signal from the M6809E MPU Module by removing jumper connection K8. The second option is to remove the REF CLK signal from the M6809 EXORciser bus.

As long as there is only one MEX6815-1 module in the system, this is possible. If there is more than one MEX6815-1 module in the system, the REF CLK signal is required to synchronize the module refresh circuitry. In this case, only the first option can be used.

The REF CLK signal can be disabled from the MEX6815-1 module by inserting a jumper connection at POS1 on jumper platform JA, and ensuring that there is no jumper at POS2. Refer to Figure E-5.

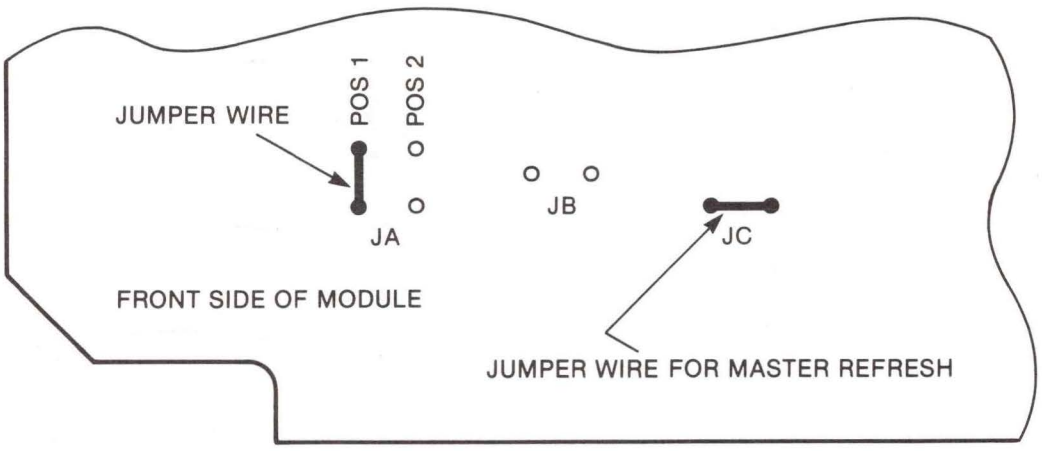


FIGURE E-5. REF CLK Signal Disabled on 8K Dynamic RAM Module (MEX6815-1)

E.2.2.3 MM09 Static RAM Module Parity Circuits. The MM09 Static RAM Module may have optional parity generation/detection circuitry installed by the user. The error output can be sent out as either NMI on bus pin E or as PARITY ERROR on bus pin W by installing a jumper at K6 pins 1 and 2 (for NMI) or at K6 pins 3 and 4 (for PARITY-ERROR).

The parity circuit can be used with EXORciser I or any M6800 system if NMI is connected at K6. However, in this case, it would be necessary to write special routines and replace the usual NMI vector at FFFC and FFFD to use it.

On the other hand, EXORciser II and the M6809 EXORciser have circuitry and EXbug routines provided to recognize this parity error signal. In this case, pin W on the bus is used to activate the circuit, and the DEbug Module will interrupt its task in order to print the parity message, followed by the register display. Refer to the sections on parity control in the EXORciser II or M6809 EXORciser User's Guide for instructions on initializing memory and using this parity.

MM09 with a parity circuit can be used with the MEX68KDM only if the error output is jumpered to pin E. This pin is called IRQ7 on the MEX68KDM, and that board auto-vectors the signal.

E.2.2.4 16K Dynamic RAM Modules (MEX6816-1). The early 16K Dynamic RAM Module (MEX6816-1) requires modification before use in an M6809 EXORciser. These modules generate an Activate (ACT) signal on pin 23. This signal has been redefined in the M6809 EXORciser as Bus Status (BS). It is necessary to disable one of these signals in order to avoid damage to either module. The recommended modification is to disable the ACT signal on the 16K Dynamic RAM Module because it is used on only the MEX68RR EROM/RAM Module. To disable the ACT signal, cut the ACT signal track (pin 23) above the finger on the module edge connector (Figure E-6).

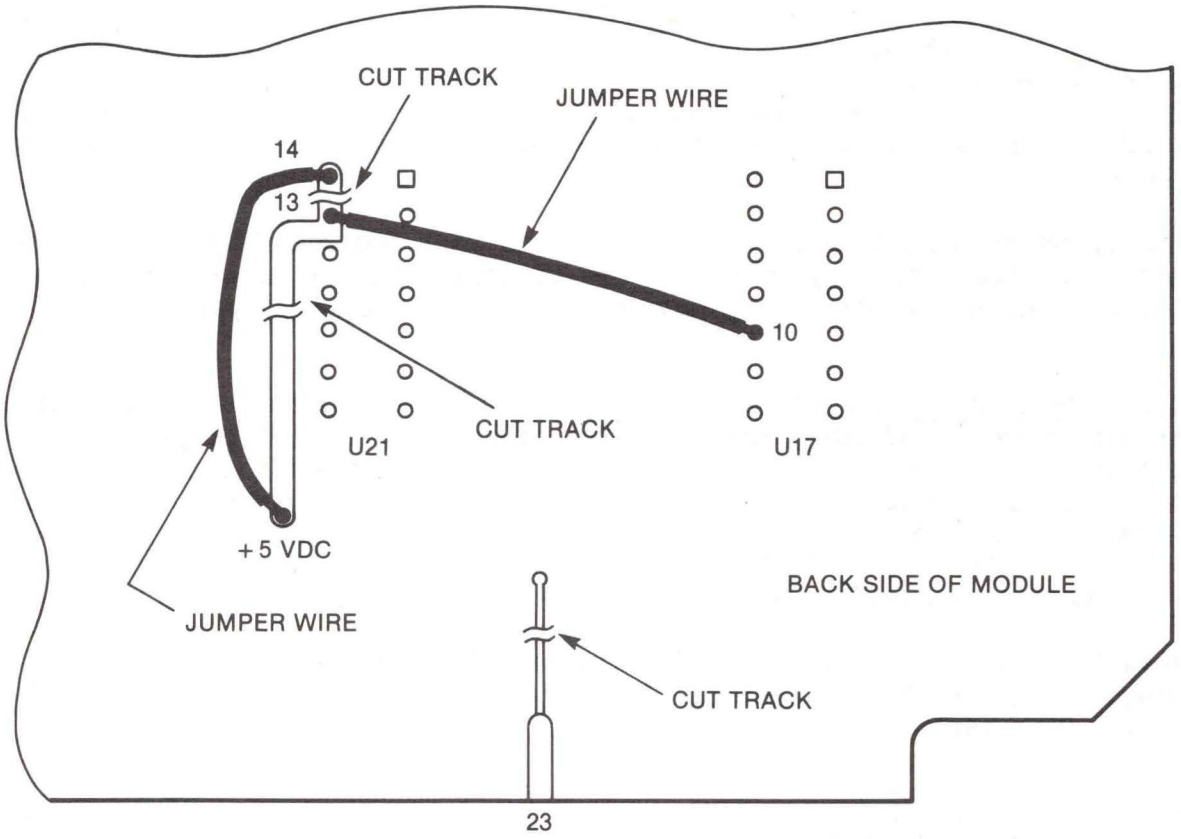


FIGURE E-6. USE Modification for 16K Dynamic RAM Module (MEX6816-1)

It is also possible to disable the BS signal from the M6809 MPU Module by removing the jumper connection at K2 of the MPU Module. Prior to performing this modification, the user must make sure that none of the modules in the system requires the BS signal.

The 16K Dynamic RAM Module (MEX6816-1) transfers data on the bus asynchronously. This causes a timing problem when operating with the M6809 USE Module. In order to enable the RAM module to transfer data synchronously, perform the following modifications on the back side of the RAM module:

a. Remove +5 Vdc connection from U21 pin 13 by cutting the tracks between pins 13 and 14 and between +5 Vdc and pin 13, as illustrated in Figure E-6.

b. Restore +5 Vdc connection to U21 by soldering a jumper wire between +5 Vdc and U21 pin 14.

c. Connect a delayed Clock (CLK) signal to U21 pin 13 by soldering a jumper wire between U17 pin 10 and U21 pin 13, as illustrated.

E.2.2.5 MM09 Static RAM Module, MM10B, or MM10C Power Fail with RAM and Clock Module with High-Speed MPU's. MM09, MM10B, and MM10C are rated to operate at 1.0 MHz. By using built-in circuitry, they will also work in systems with a 1.5 MHz or 2.0 MHz clock by stretching the Ø2 and Ø1 signals with MNRDY. To use MM09, MM10B, or MM10C with the MPU II Module (MC6800 EXORciser II MPU) at 1.5 MHz or 2.0 MHz, the MPU II Module must be modified. Cut pin 12 of U2 (74S74 chip) where it connects to the board. Then install a jumper wire between U2 pin 12 and U19 pin 4. This provides a 100-nsec delay in the Ø2 signal on the MPU II board.

If MM09, MM10B, or MM10C is used in a system that includes MDOS, the system can run only at 1.0 MHz. Trying to use the Ø2 stretch circuits of MM09, MM10B, or MM10C will alter the disk timing cycle of MDOS and stop the system.

E.2.2.6 MM09 Static RAM Module with USE. For proper operation of MM09 with the User System Evaluator (USE) module, a pullup resistor R19 (4.7K ohms, 5%, 1/4 W) has been added to MM09. This resistor pulls up the data bit zero (D0) input to data buffer U24, thus allowing the three-state detector logic on the USE module to assume that a valid logic level on this data bit exists early enough in the cycle at 2 MHz. This is necessary so that the USE module will enable the "development system side" buffers to read the MM09 data.

Issues G and later of MM09 have R19 installed. Users of modules of issues E through F may add R19 if needed. Do not attempt to install R19 on any modules of issue D or earlier.

E.2.2.7 MM02 CPU Module Operation with Debug Module. If the MM02 CPU Module is used in place of an MPU Module in an EXORciser having the Debug or Debug II Module installed, two different modifications are required to the Debug Module. The first modification is required to prevent the Debug or Debug II Module from generating a VUA signal. This modification consists of removing resistor R7 (10 ohms) on the Debug Module; or cutting the trace at connector P1 pin 10 on the Debug II Module (in a way that can be repaired later) to disable the VUA output at P1 pin 10. When the original MPU Module is used with the EXORciser, this modification must not be used. The second modification is required to enable the CPU Module to recognize the existence of the Debug Module in the EXORciser. This modification consists of grounding P1-14 on the Debug Module only. (This pin is already grounded on the Debug II Module.) Since this modification does not affect normal operation of the EXORciser with the MPU Module installed, it does not have to be removed when the CPU Module is replaced by the MPU Module.

When an M6800 system is being designed and tested, it is usual for the control program to be placed in RAM for final debugging. An EXORciser is usually used, and since its EXbug control program occupies the memory range above $F000, the control program must reside at some lower address such as $7000. Typically, the user program will have its interrupt vectors at its "top of memory" which, in this case, could be $7FFF.

Since the EXORciser modules are fully decoded, the techniques provided in EXbug allow the "top of memory" to be adjusted (by setting $FF00) so that the IRQ and RST vectors are usable. (See the EXORciser User's Guide.) However, with fully decoded memories and the Debug Module is not used, it is necessary that the program be relocated so its "top of memory" is at $FFFF. The vectors will then be properly fetched. To avoid relocation, a feature has been added to MM02 which allows the IRQ vector to be fetched even though it is at a lower address. All that is necessary to implement this feature is to install jumpers as shown in the MM02 User's Guide. If the memories for the final system (presumably ROM's) are not fully decoded, and are therefore redundant at $7000 and $F000, for example, this feature is not needed, and no jumpers are required.

E.2.2.8 Power Fail Output and Memories. The PWR FAIL output from Micromodule 10B/10C is on pin V of the bus. Only boards such as Micromodules 9 and 19 or EXORciser II static RAM boards MEX6808-21, MEX6808-22, MEX6816-21, and MEX6816-22S (which have a connection to pin V) can use this signal to disable the write function of their on-board RAM's.

E.2.3 Type of MPU and Related Bus Problems

Micromodule boards have been designed with the following MPU chips on them:

MPU Chip	Micromodules
MC6800	MM01, MM01A, MM01A2, MM01D, MM02
MC6802	MM01B, MM01B1A
MC6809	MM19, MM19A

MC6800-, MC6801-, and MC6802-based systems use the M6800 bus; MC6809-based systems use the M6809 bus. Refer to Appendix B for the bus signals. However, all memory and standard I/O modules designed for use in EXORciser II can be used in the M6809 EXORciser.

Any module designed with an MPU chip other than an MC6809 or MC6809E installed in it, (such as M6800, M6801, M6802 MPU modules; M6800, M6802 USE modules; or M6800 micromodules), will not function in an M6809 system.

Following are additional specific MPU type problems.

E.2.3.1 DEbug Boards in M6809 Systems. Only the M6809 DEbug Module will work in an M6809 system or with MM19. DEbug I and DEbug II Modules will not work properly with M6809 EXORcisers or MM19. DEbug II can be modified to work with M6809 systems; DEbug I cannot.

E.2.3.2 System Analyzers with MM19, MM19A, and M6809 Systems. The M6800 Systems Analyzer I can work at 1 MHz with MM19, MM19A, or in an M6809 system if the M6809 PROM's are installed and the M6809 Systems Analyzer Intercept Module is used. The M6800 Systems Analyzer II Module can be used with MM19 or MM19A or in an M6809 system at 2 MHz when used with the M6809 Systems Analyzer Intercept Module and M6809 PROM's installed.

E.2.3.3 EXORdisks with MM19, MM19A, and M6809 Systems. EXORdisk I used the MEMCLK signal to clock data in or out. EXORdisk I can work with a 1-MHz MM19, MM19A, or M6809 system as long as slow memories are not installed. (Slow memories are ones that require the MNRDY signal to stretch the system clock signals.) Using slow memories with EXORdisk I will cause read/write errors. In addition, the M6800 PROM's on the Floppy Disk Controller Module must be replaced with M6809 PROM's.

When working with EXORdisk II or III, it is necessary to replace the M6800 PROM's with M6809 PROM's on the Floppy Disk Controller Module. A low on the MNRDY line will cause the system clocks to be stretched. For this reason, it is necessary for the disk drivers to operate off the 1 MHz controller clock if the drivers are to function properly when slow memories are installed in the system. All Floppy Disk Controller modules built in recent years have their own clock.

E.2.3.4 MM10B, MM10C FIRQ Output. The FIRQ optional output from Micromodules 10B and 10C on pin A of the bus is usable only with systems having an MC6809 type MPU.

E.2.4 System Operating Speed Problems

EXORciser I systems were designed to run at 1 MHz; EXORciser II and M6809 EXORciser systems at up to 2 MHz. Their boards and all micromodule boards are coded for operating speed by the color of the card ejectors; white for 1 MHz and red for 2 MHz. (M6809 boards have green card ejectors.) Micromodules specifically-assigned operating speeds are:

System Speed	Ejectors	Micromodules
1 MHz	white	MM01, MM01A, MM01A2, MM01B, MM01B1A, MM01D, MM02, MM04, MM04A, MM09, MM10, MM12, MM14, MM23
2 MHz	red	MM07, MM12A, MM14A
1 MHz	green	MM19
2 MHz	green	MM19A

NOTE: For new products from Motorola Microsystems, card ejector color coding has been discontinued.

Following are additional specific speed problems.

E.2.4.1 MM04A ROM/EPROM Module. Refer to paragraph E.2.2.1 for instructions on operating MM04A (with slow memory chips) at 1.5 or 2.0 MHz.

E.2.4.2 MM14 and MM14A APU Modules. MM14 and MM14A are identical except for their operating frequencies. MM14 has a 2 MHz on-board clock, and operates only in a 1 MHz system. MM14A has a 3 MHz on-board clock, and operates in a 1, 1.5, or 2.0 MHz system.

E.2.4.3 EXORciser I Modules with MM19 or M6809 Systems. Most EXORciser I modules are not rated to operate above 1 MHz. The system speed is limited to the maximum clock rate specified for the slowest module in the system. Therefore, when using EXORciser I modules, it is necessary to configure MM19 or the M6809 system to 1 MHz.

E.2.4.4 System Analyzer I and/or EXORdisk I with MM19, MM19A, and M6809 Systems. Refer to paragraphs E.2.3.2 and E.2.3.3, respectively.

E.2.4.5 MM09 Static RAM Module or MM10 Power Fail with RAM and Clock Module. Refer to paragraph E.2.2.5 for instructions on operating MM09 or MM10 with 1.5 MHz or 2.0 MHz systems.

E.2.5 Other Hardware Problems

E.2.5.1 MM01 with MM23. If monoboard MM01 is to be used with the MM23 relay module, IC's U31 and U33 on MM01 should be 7403 or 7409 quad open-collector AND gates.

E.2.5.2 Isolated Ground on Bus. In the EXORciser II and M6809 EXORciser systems, the chassis is wired such that pins 24 and B are an isolated ground signal not connected to the regular system ground. This is not done on the micromodule long chassis, short chassis, and front loading chassis (or on the EXORciser I and IA chassis).

E.2.6 Micromodule Software and Firmware Problems

E.2.6.1 MM03 I/O Module and Debugging Readback. Refer to paragraph E.2.1.1 for instructions on using MM03 with debugging programs (such as EXbug, MINIbug, MIKbug) that have readback features.

E.2.6.2 MM01B1A and MIKbug. An optional MC6846 (ROM, Timer, and I/O combo chip) containing 2K bytes of masked ROM can be installed as U16 on the board. The 2K of ROM may contain either a user custom firmware program, or possibly the MIKbug 2.0 monitor/debug program (on chip MC6846P1).

CAUTION

UNLESS THE BOARD IS MODIFIED AS DESCRIBED IN THE MM01B1A USER'S GUIDE, THE MC6846P1 WITH THE MASK-PROGRAMMED MIKbug 2.0 MONITOR WILL NOT WORK DIRECTLY WITH MICROMODULE 1B1A, DUE TO THE PTM BAUD RATE GENERATOR.

With the address ROM's (U29 and U30) as supplied on the board, the MC6846 ROM may be addressed at C800 or F800 (or ambiguous at C800 and F800), and the available two 2K EPROM's may be addressed at C000 or F000 (or ambiguous at C000 and F000).

E.2.6.3 SUPERbug (M68MM19SB). The SUPERbug firmware contains a monitor, linker, and loader, all designed to operate with MM19. SUPERbug relies on MC6809 features and will operate only with an M6809 system. For the use of SUPERbug with MDOS and EXbug, see the SUPERbug User's Guide.

NOTE

SUPERbug, as delivered, is compatible only with the 1-MHz MM19, and must be programmed into high-speed PROM's for use with the 2-MHz MM19A.

E.2.6.4 MM08 and MM08A MICRObug Firmware with MPU and CPU Micromodules. Micromodule 8/8A MICRObug monitor firmware may be used in systems based on Micromodule 1, 1A, 1A2, or 2. Refer to the MM08/08A User's Guide for details of how to prepare the boards and firmware for use.

MM08 consists of one MEX6850 Asynchronous Communications Interface Adapter (ACIA) Module and one MICRObug ROM. This version is intended to be used specifically with MM01- or MM02-based systems, thus adding both a debugging capability and a serial communications port to them.

MM08A is comprised of only the MICRObug ROM, offering users the option of adding a debugging capability to systems built around MM01A or MM01A2, both of which already have a serial communications port.

NOTE

MICROMODULES 08 AND 08A ARE NOT DESIGNED FOR USE WITH MPU BOARDS MM01B, MM01B1A, MM01D, OR MM19.

E.2.6.7 MM04, MM01, and Editor/Assembler/BASIC Firmware. The M68EAM1 and M68EAB1 or M68EAB2 modules, respectively, contain an editor/assembler program or an editor/assembler program and a BASIC program. Each program is installed in seven 1K-byte ROM's, which are installed in sockets on a Micromodule 4 16K EPROM/ROM module. The ROM sets are also available separately. The M68EAB1 firmware is MINIbug II compatible, while the M68EAB2 firmware is MICRObug compatible. Because the M68EAM1 module is compatible with the EXbug, MINIbug II and III, and MICRObug monitor/debug firmware, this module may be used with the M68ADS2A, EXORciser/EXORterm, and MICRObug-based systems.

NOTE

Due to address conflicts, the firmware BASIC program, version 1.3 and earlier, may not be used in a Micromodule 1-based system.

These modules are supplied with their seven or 14 ROM's installed in the proper sockets and the base addresses of the bottom ROM's set by jumper arrangement to hexadecimal 6400 (editor/assembler) and hexadecimal 4000 (BASIC). Refer to the Micromodule 4 User's Guide for installation, addressing, and interconnection details.