Designing with the DP8462

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Kern Wong
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GENERAL DESCRIPTION

This literature assumes the reader has thoroughly read the DP8462 datasheet and is familiar with the basic circuit operation discussed therein. The objective of this note is to give the customer comprehensive application information for the design and testing of the device. It also offers detailed guidance in the selection of appropriate component values, use of optional device features, and considerations for system configuration. The following is a brief description of key features of the device.

The DP8462 is one of National Semiconductor's second generation disc data synchronizers designed for application in disc drive memory storage systems. It features 3T (1-0-0) or 4T (1-0-0-0) preamble detection circuitry which makes it especially convenient for systems employing run-length-limited codes such as the popular 2, 7 code. Of course, it may also be used as a data synchronizer for other conventional coding methods such as MFM, (1, 7), (1, 8), etc., but the internal (3T/4T) preamble detector function will then be bypassed.

This Phase-Locked-Loop (PLL) chip contains three customer programmable input control pins (TLL logic levels) to offer significant design flexibility. The PREAMBLE SELECT programming input determines whether the preamble detector looks for a 3T or 4T preamble pattern. The 4T preamble has been the most widely chosen pattern because of its ability to attain phase-sync naturally (refer to DP8463B (2, 7) ENDEC datasheet for detailed discussion). The LOCK-CONTROL input pin can be set to allow the phase comparator to function in one of two modes of operation: Phase and Frequency comparison or Phase-Only comparison. During non-read mode, phase and frequency comparison is employed within the DP8462 to lock onto the 2F reference clock. However, in the read mode the phase-frequency detection circuitry changes to phase-only comparison. Via the LOCK CONTROL input, the user may select when this mode change occurs, either immediately after Read Gate is asserted or after preamble detection has occurred. The charge pump also has two modes of operation: high track rate is used for fast acquisition to the 2F reference clock in the non-read mode and to the preamble in the read mode; low track rate is used in the read mode to allow smooth, stable lock to the data field. Both track rates are selectable by the customer via the I-BOOST ENABLE input. In a typical design the PREAMBLE DETECTED output may be directly connected to the I-BOOST ENABLE input to accomplish the desired track rate switch-over.

PHASE-ONLY OR PHASE-FREQUENCY COMPARISON

Depending on system characteristics and sector formats employed, such as soft or hard sectoring, encoding method, acquisition time requirement, etc., the system designers may be required to select only one of the two modes of comparison during read (preamble acquisition) or they may be free to choose either comparison mode to achieve optimum system performance. The following discussion illustrates the differences between the harmonic phase detector and the non-harmonic phase detector techniques incorporated in the DP8462 PLL chip.

In the non-read mode the PLL is always set to Phase-Frequency comparison mode (non-harmonic) to guarantee that it will attain frequency lock to the 2F Clock reference signal; thus, the possibility of a false lock occurrence is eliminated. In the read mode, if the Phase-Only comparison mode is chosen (via LOCK CTL: L0), then the phase detector will engage in phase comparison (harmonic mode) between ENCODED DATA and VCO gated by data pulses immediately upon Read Gate assertion. This must be done in a true soft-sectored system where there is no guarantee of Read Gate assertion occurring only within preamble field. Furthermore, the maximum phase step seen by the PLL at the assertion of Read Gate is at most one-half of one decode window period since the Pulse Gate allows the incoming data pulse to be compared with the nearest occurring VCO pulse. However, there is always a probabilistic condition that an initial burst of pulses can occur at the input during Read Gate switching which may violate normal coding methods or nominal pulse width specifications, resulting in synchronization errors. To avoid false lock possibility with Phase-Only mode in synchronization field when Lock Control is set "LO", it is recommended that the loop's natural frequency bandwidth, Wn, be low. Normally the loop filter component values for C1 and R1 will need to be recalculated in accordance with the lower Wn value selected. Optimizing the selection of the Pulse Gate network (RPG2 and RPG4) may also improve the loop's performance as this allows better centering of the data bit position with respect to its decode window and optimizes accurate locking to the data frequency.

The customer may also configure a soft-sectored write, and pseudo-hard sectored read system, which retains the advantages of formatting flexibility while capitalizing on the Phase-Frequency comparison feature in the read mode (with LOCK CTL: HI). Such a system configuration is realized with a Read Gate qualifying technique which ensures Read Gate is asserted only within the preamble field, thus removing any lock problems associated with reading through write-splice gaps or data field induced false address mark (AM) or false preamble patterns. With this method of operation, the PLL remains in the Phase-Frequency comparison mode in the preamble field until 16 consecutive preamble pulses have been successfully detected; then, it switches to Phase-Only mode. Employing a Phase-Frequency comparator during preamble acquisition ensures that the possibility of Quadrature Lock, a form of false lock due to pulse pairing in the read channel, is eliminated. Similarly, a true hard-sectored system will utilize these same techniques to avoid all the potential lock problems mentioned above.

The user should be aware of the fact that when employing frequency lock, the VCO divided by either 3 or 4 is compared with the data pulse. Therefore, depending on the initial logic state of the divider (which is random) and the initial phase difference incurred at the time of Read Gate assertion, the maximum phase error can be 3 or 4 VCO cycles long (depending on whether 3T or 4T preamble is selected) which is 6 or 8 times greater than when the Phase-Only mode is employed. This requires the PLL synchronization

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bandwidth to be set adequately high in order to guarantee the phase error has settled to less than one-half of one decode window before the PLL switches out of frequency lock mode. Otherwise, a second phase step is introduced when the device switches out of frequency lock mode which lengthens lock times and may result in synchronization errors.

BANDWIDTH CONSIDERATIONS AND LOOP FILTER SELECTION

The DP8462 PLL is a frequency selective feedback circuit that can synchronize with a selected input signal and track the frequency and/or phase changes associated with it. A finite phase error is necessary to generate a corrective voltage to shift the VCO output frequency in compliance with the input signal variation. Once locked, the synchronizer can track a slowly changing input signal. It rejects transient changes (via loop filter) which tend to disturb the PLL. The phase detector (a bi-directional charge pump) generates a proportional error correction current pulse and is followed by a passive low-pass filter network generally with a sufficiently narrow bandwidth to suppress any noise and high frequency components from the phase-detector and charge pump stages. More importantly, the filter network determines the dynamic performance of the loop which includes capture and lock ranges, bandwidth, and transient response time. Of equal significance, the passive filter also yields the characteristic poles and zeroes for stability. There are numerous approaches to calculate a suitable set of filter component values; they may be estimated from a capture range point of view, from the required time and dynamic response profile of the loop, or from noise bandwidth considerations, etc.

LOOP FILTER COMPONENT VALUE SELECTION

The first step when selecting component values is to determine an appropriate value for the natural angular frequency, Wn, of the PLL. (Wn, commonly referred to as the loop's natural frequency should not be confused with the center frequency, Wo or Fo, of the VCO.) Wn is related to the loop gain and the RC time constants imposed by the low-pass loop filter. It should be noted that if the available loop gain is high and a relatively low natural frequency required, very large time constants will result. The size or value of the passive components for the loop filter may become impractical if not difficult to obtain. Therefore, judicious choice of Wn and filter components is necessary to allow good performance while at the same time using only standard component values. Optimum filter design may involve an iterative engineering effort from empirical data to arrive at the desired results. Recommended values in the datasheet are all valid suggestions but may not be the optimized values for every system.

As suggested in the datasheet, a (degenerated) 2nd order passive filter is quite adequate for most applications. The filter network consists of C1 connected in series with R1 and C2 connected in parallel with R1 and C1. The characteristic equation is 3rd order by inclusion of C2 in the highest order term. In practice, if the pole determined by R1 and C2 is more than a decade above the zero, the 3rd order term can be ignored and the equation can be rewritten as a 2nd order loop (refer to the DP8462 datasheet for details).

Two approaches for the determination of Wn are illustrated; component calculations are the same in each case. These examples allow digital designers to start estimating a loop filter without having to derive its poles/zero, and centroid, or construct Bode plots.

Example #1: 10 Mb/s data rate, (2, 7) encoding, 4T preamble

Assume it is desired to track the information recorded on a rotating or travelling medium being modulated by the spindle or capstan velocity, and assume there will be a 1.5% offset in the motor speed. It has been shown that a capture range greater than the input frequency offset, ΔW, will ensure that lock will occur quickly. Choose Rrate $= 820\Omega$ (an optimal value for the charge pump).

The initial frequency offset is then:

$$\Delta W = (1.5\%)\ (10\ \text{Mb/s})\ (2\pi) = 942\ \text{krad/s}$$

In most system designs, an optimally flat frequency-transfer function of the loop is the objective. The Bode diagram of such a transfer characteristic shows this can be achieved with $\zeta = 0.707$ (see reference: F. Gardner). The expression of capture range $\cong 2\ \zeta Wn$ is a reasonable approximation also found in reference materials (i.e., R. Best). A damping of $\zeta = 0.7$ is chosen as a design criterion for optimal response during the 4T pattern acquisition.

By equating capture range and ΔW for acquisition of 4T data pattern, (that is, one data pulse present within 4 VCO periods):

$2\ \zeta Wn\ (4T) \geq \Delta W$

$Wn\ (4T) \geq \Delta W/(2\zeta) = (942\ \text{krad/s})/(2)\ (0.7) = 666\ \text{krad/s}$

This is defined as Wn(max) during preamble or Xtal acquisition, where the PLL is locking onto the 4T preamble or the Xtal divided by 4 signal.

Wn is proportional to the square root of the data frequency (Refer to the datasheet:

$Wn = \sqrt{(2.5)\ (Fvco)/(C1)\ (R)\ (N)}$,

where N is defined as Fvco/Fdata (i.e., N = 8/1). R is the effective gain setting resistor which determines the charge pump reference current.)

For minimum data frequency tracking, for example the 8T pattern (which is the lowest allowed data frequency for the 2, 7 RLL code where one data pulse occurs within an 8 VCO clock period span),

$Wn(min) \equiv Wn(8T) = \sqrt{4T/8T}\ [Wn(4T)] = 471\ \text{krad/s}$

Similarly at maximum data frequency, as in a 3T pattern, Wn(max) in data field becomes 769 krad/s.

To calculate for the loop filter component values, the above general expression for Wn is transposed to obtain the following equation:

1. $C1 = (2.5)(Fvco)/[(Rrate)(N)(Wn(4T))^2]$
   $= (2.5)(Fvco)/[(820)(4)(666E3)^2]$
   $= 0.034E\text{-}6$
   $C1 = 0.03\ \mu F$, which is a standard capacitor value.
2. $R1 = 2\ \zeta/(C1)(Wn) = 2[\zeta(4T)]/(C1)[Wn(4T)]$
   $= 2(0.7)/(0.03E-6)(666E3)$
   $= 70.07$
   $R1 = 68\Omega$, is a standard resistor value.
3. Choose $C2 \cong C1/50$. In general, selecting $C1/50 < C2 < C1/10$ will yield non-dominant parasitic pole and still allows C2 to integrate the current pulses. (Capacitor may be film or monolithic ceramic.)
   $C2 = 560\ pF$

4. Recalculate Wn(8T) at minimum data frequency with standard component values: (For loop stability ζ(min) should not be allowed to be less than 0.5. ζ(min) occurs when Wn is at a minimum.)

   $Wn(8T) = \sqrt{(2.5)(20E6)/(820)(8)(0.03E-6)}$
   $= 504$ krad/s

   $\zeta(8T) = (504E3)(68)(0.03E-6)/2$
   $= 0.51$

5. Recalculate Wn(4T) for data frequency in preamble acquisition with standard component values:

   $Wn(4T) = \sqrt{(2.5)(20E6)/(820)(4)(0.03E-6)}$
   $= 713$ krad/s
   $\zeta(4T) = (713E3)\ (68)\ (0.03E-6)/2$
   $= 0.73$

6. Calculate the loop parameters for locking to the crystal frequency divided by 4 signal (N = 4). Normally a higher loop gain is employed. With the use of an additional charge pump current setting resistor (Rb) to boost loop gain during non-read mode, the damping factor may be chosen with $\zeta(4T-Xtal) \cong 1.0$ for critical damping during crystal acquisition.

   $Wn(4T-Xtal) = \zeta(4T-Xtal)(2)/(R1)(C1)$
   $= (1.0)(2)/(68)(0.03E-6)$
   $= 980$ krad/s

7. Calculate Rb from Wn(4T − Xtal):

   $Wn(4T-Xtal) = \sqrt{(2.5)(Fvco)/(Rr//Rb)(C1)(N)}$
   $980E3 = \sqrt{(2.5)(20E6)/(820//Rb)(0.03E-6)(4)}$
   $820//Rb = (2.5)(20E6)/(0.03E-6)(4)(980E3)^2$
   $= 433.8$
   $= (820)(Rb)/(820 + Rb)$
   $Rb = 921.2$

   choose Rb = 910Ω, a standard resistor value.

   Rp = 820//910 = 431.33, the effective charge pump current setting resistor value.

8. Recalculate Wn(4T − Xtal) with standard component values:

   $Wn(4T-Xtal) = \sqrt{(2.5)(20E6)/(431.33)(0.03E-6)(4)}$
   $= 983$ krad/s

   $\zeta(4T-Xtal) = Wn(4T-Xtal)(Rp)(C1)/2 = 1.02$

In general the customer may choose any suitable gain ratio between fast lock and stable data tracking. A 2:1 ratio is a popular choice; for example, Rr = Rb = 820Ω. In the above example this will make the damping factor and Wn(max) at crystal reference lock slightly larger. Note that we have chosen zeta, ζ, to be between 0.5 and 1.0 as a general guideline such that the system will not be excessively underdamped nor subject to excessive acquisition times. However, an experienced designer can choose other appropriate design values to tailor toward a specific system's requirements.

Note: There is a minimum value for Rr//Rb (parallel combination value) allowed for the DP8462. A maximum reference current limit for the charge pump is imposed such that Vbe/(Rr//Rb) ≤ 2 mA. This translates to Rr//Rb ≥ Vbe/2 mA ≅ 350Ω, typically, for Vbe ≡ 0.7V.

Hence, the above calculations yield the loop filter component values and their corresponding loop parameters for example #1 as follows:

10 Mb/s (2,7) Code	Rr	Rb	R1	C1	C2
	820Ω	910Ω	68Ω	0.03 μF	560 pF

Wn(8T)	ζ(8T)	Wn(4T)	ζ(4T)	Wn(4T − Xtal)	ζ(4T − Xtal)
504 krad/s	0.51	713 krad/s	0.73	983 krad/s	1.02

Another frequently used method for Wn determination is by graphical means. If damping ratio, ζ, and lock time are given, Wn can be arrived at via the normalized phase error versus Wnt plots. Alternatively, if the desired system response has been defined as specified in the example given below, Wn can also be readily determined.

Example #2: 7.5 Mb/s data rate with (2, 7) encoding and 4T preamble

Maximum peak overshoot $< 30\%$

Settling time $\cong$ 11 μs with phase error $\leq \pm 5\%$

VCO capture range within $\pm 20\%$ of 15 MHz and follow excursion of $\pm 5\%$ of Fo

Charge pump gain ratio = 2:1 between non-read and read modes, (Rr = Rb = 820Ω).

It is helpful to know the initial frequency offset for the derivation of Wn. But this information may be available to the customer and the exact value is not necessary to make a trial estimate for Wn. Fortunately, the maximum velocity variation of commercial drive mechanisms are well within 2% and current disc drives have guaranteed rotational tolerance of less than 1%. Hence, initial frequency step between non-read and read modes in normal operation does not contribute appreciably to the total phase-error transient resulting from a maximum phase step assumed in the calculation.

Wn can be derived from the Wnt vs. θe(t) curves due to a phase step. *Figure 1* shows that the $\zeta = 0.5$ parametric curve meets the above requirement of maximum peak overshoot less than 30%. The residual phase error will be approximately -5% at Wnt = 6 rad. Therefore, settling to $\pm 5\%$ (or about 3 ns) in t = 11 μs yields:

Wnt = 6.0 rad

Wn(4T) = 6.0 rad/11 μs = 545E3 rad/s

This is the computed BW for preamble acquisition, which is then used to calculate the loop filter component values as in the previous example. The loop filter and parameter values are presented below:

Transient Response of 2nd Order Loop due to a Step in Phase

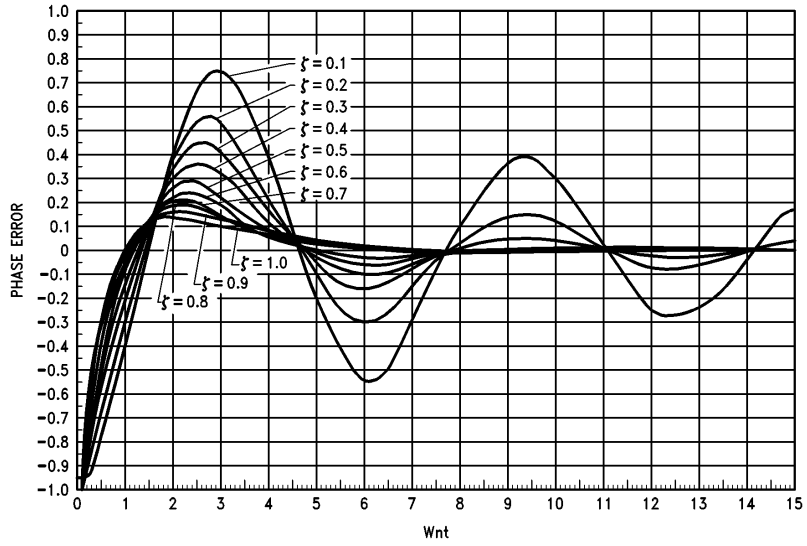

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FIGURE 1

7.5 Mb/s	Rr	Rb	R1	C1	C2
(2, 7) Code	820Ω	820Ω	68Ω	0.039 μF	820 pF
Wn(8T)	ζ(8T)	Wn(4T)	ζ(4T)	Wn(4T−Xtal)	ζ(4T−Xtal)
383 krad/s	0.51	541 krad/s	0.72	766 krad/s	1.01

Note: The derived Wn value may be checked to verify for adequate capture range in the read mode. The value chosen does satisfy the expression $2\zeta(4T)Wn(4T) > \Delta W$(of 1.5%).

The above techniques are useful in estimating suitable loop filters which satisfy basic capture and lock conditions in non-read mode and read mode in preamble field. The conservatively derived component values should allow good performance in most applications. However, there are situations where significant improvement in system performance may be gained if the loop bandwidth is optimized with respect to a particular system. For example, to accommodate certain sensitivities to cylinder formats, media imperfections, or noise in gaps, etc., it may be necessary to raise or lower Wn considerably from the suggested values used in the above computations. In addition to the NSC suggested values in the datasheet and this note, the customer is strongly encouraged to modify those values or tailor a filter to achieve minimum error-rate.

The following table lists additional sets of loop filter component values which have performed well in the field or have been designed into systems:

LOOP BANDWIDTH OPTIMIZATION AND DESIGN CONSIDERATIONS

Numerous ''optimized'' loops have long been derived for various types and orders of PLL systems. Optimum loop transfer functions were formulated for different types of input stimuli. It is practically impossible to make a perfect loop as this will require continuous adaptation of the filter to compensate for the input changes as a function of time. The 2nd order loop (due to its ease of analysis) is by far the most popular and of the greatest interest to design engineers. The following list presents some design trade-off issues and several frequently encountered design and device evaluation considerations.

1. Narrow Bandwidth: Most designers will wish to keep loop BW low to improve noise rejection. This will decrease the loop's response to input jitter at the expense of having a smaller capture range. This can be very helpful in soft-sectored reading to desensitize the effect of write-splice induced perturbations.

2. Wide Bandwidth: If capture range exceeds frequency range within which the input signal is expected to vary, it increases the probability of spontaneous lock. Raising the loop's BW is recommended if the input frequency offset is sufficiently large.

3. Damping Factor: It is suggested that this should be set approximately equal to:

   0.5 for Wn(min) in read mode,
   0.7 for Wn(max) in read mode, and
   1.0 for Wn(Xtal) in non-read mode.

   (If a 4T preamble is employed, then Wn(max) in data field of 3T pattern is larger and the damping factor becomes slightly greater than 0.7.)

   A larger damping factor increases capture range which improves the probability of acquiring lock. It also increases total acquisition time.

   A smaller damping factor minimizes response to bit shift, but excessive underdamping will cause instability.

4. The open loop response of the chip can be modelled as a 2nd order PLL (highest power of $s=2$ in the denominator of the loop transfer function) with a parasitic 3rd pole.

$$G(s) = \frac{2.5(Fvco)\,(1+sR1C1)}{(N)(s^2)(Rr)(C1)(1+sR1C2)}$$

   where Fvco = center frequency and N = Fvco/Fdata.

   If the chosen physical parameters and component values are faithfully modelled by such an expression, phase-margin of the loop can be reasonably predicted. Phase-margin should be between 30° and 70° at unity gain. 45° is good compromise in general; this is the criterion for loop stability. Larger phase-margin produces a more stable loop, but it slows the response, increases VCO output unwanted sidebands, and reduces loop VCO-noise suppression capability.

TABLE I. Loop Filter Component Values

Data Rate (NRZ)	Rr	Rb	R1	C1	C2
5 Mb/s	820Ω	1.5 KΩ	75Ω	0.056 μF	820 pF
	820	2.2K	95	0.047	820
	370	∞	42	0.10	1600
7.5 Mb/s	820Ω	820Ω	62Ω	0.047 μF	1000 pF
10 Mb/s	820Ω	1.2 KΩ	82Ω	0.020 μF	510 pF
	820	820	62	0.039	820
	910	910	51	0.056	820

5. The effects of the loop filter component values can be summarized as follows for component optimization considerations:

   Increasing C1: (Lowers BW) desensitizes PLL from input bit jitter or frequency shift.

   Reduces possibility of spontaneous transient response to spurious signals in read/write gaps. Slows down loop response time. Reduces capture range.

   Increases loop sensitivity to VCO noise.

   Increasing C2: Reduces the rippling effect of the charge pump switching current which allows less loop response to shifted bits. Reduces stability margin.

   Increases (slightly) loop response to VCO noise. Increases response to write splice perturbation.

   Increasing R1: Increases stability margin. Decreases loop response to VCO noise.

6. An often asked question on PLL design parameters regards lock-up time. There is no simple expression that will adequately predict acquisition or lock times because of many factors that influence them and ambiguity of definition of lock. Lock time may be estimated roughly from ''Wnt vs. phase-error'' normalized curves if loop parameters are defined or known (see *Figure 1*). The following lists several factors that contribute most to the variation in lock times. This information offers some insight into lock time interaction with respect to the DP8462 PLL and its environment. Customer should be aware of them in order to realize good designs.

   a) Initial phase difference between input & VCO comparison pulses.

   b) Initial state of the VCO divided by 3 or 4 counter.

   c) Initial input frequency offset.

   d) Low pass loop filter characteristics (BW and damping).

   e) Center frequency (VCO) accuracy and symmetry.

   f) VCO noise and sideband signals.

   Note: Although customer has no control over a) and b), their impact can be minimized through loop filter design.

7. Another frequently asked question is how to measure lock ranges and capture ranges. A few methods are suggested below:

   Lock range is the maximum input frequency-ramp excursion (upper and lower bound) permissible while the loop still maintains lock. To measure lock range, apply a square wave pulse train of known frequency to the ENCODED DATA input of the PLL chip. Allow the PLL to be stably locked onto the periodic input waveform. While in read mode measure either the SYNCHRONIZED DATA or VCO output for good synchronization to the input as its frequency varies until lock is lost. It is recommended to set Read Gate low momentarily after each measurement.

   For the capture range determination, continuously cycle Read Gate as in above (always allow sufficient time for the PLL to lock to the 2F reference clock). Start with the PLL in lock, gradually increase the frequency of the input data stream until the PLL will not lock, then readjust the frequency towards the center frequency until locking is achieved again at a particular frequency. This frequency is the upper capture frequency. Repeat this procedure for the lower boundary to determine the lower capture frequency.

   Note: A noisy analog instrumentation tuning mechanism may produce undersirable transients that disturb the PLL and give false data. Always make very slow and gradual adjustments. Improper toggling of the Read Gate or insufficient deassertion time may result in lock problems during read mode.

OPTIMIZING THE DECODE WINDOW:

In the past, the Twindow A.C. specification in the datasheet was not well understood and has caused misinterpretation by some customers. This specification simply indicates the maximum truncation of the available half decode-window width (one side of nominal window). For a given data rate, an ideal window boundary is defined for the data bit. The entire (ideal) window width can rarely be made available due to noise, device tolerance, and process or other related physical imperfections. The PLL chip, therefore, contributes a total window loss equal to twice the Twindow time stated in the Twindow specification. Basically, there are two mechanisms that are responsible for this loss. First, is the dynamic uncertainty arising from the superposition or modulation of noise and phase movement from internal and external sources that effectively narrows the usable window size. The second, and dominant mechanism, is the deviation of chip produced window center from the theoretical center of the data window. This is caused by non-ideal on-chip device matching due to process related variations during device fabrication. This deviation is sometimes called ''window-margin''. Our Twindow specification, in effect, lumps all contributing factors of window jitter and displacement within the PLL data synchronizer into a single specification which corresponds to the amount of maximum half-window loss. This figure can be determined empirically using a specific set of external passive components and test conditions following complete PLL lock and stabilization. (This will be explained in the next section.)

As suggested in the datasheet, bit jitter tolerance can be improved by adjusting the window center via the PG2 and PG4 pins. There have been no fewer than 3 different current splitting networks employed to adjust the internal silicon delay line to improve the phase margin. (The adjustments are internally compensated for Vcc and temperature variations.) The various network configurations, whether chosen for test convenience or for layout topolgy reasons, are fundamentally equivalent and achieve the necessary bias. They should yield the same final result of centering the data bits within their respective windows. It should be pointed out that we are by no means requiring the user to employ the extra task of trimming during manufacturing to accomplish margin improvements as may be misinterpreted from drawings depicted in the datasheet. Our intention is to illustrate to the users the fact that by selecting an appropriate resistor (fixed) value for RPG4, as in *Figures 2a* and *2b*, one can obtain better Twindow tolerance than specified in the datasheet. For example, the DP8462-3 part type guarantees at most 6 ns of static window loss at each window boundary. But, via an RPG4 of approximately 2.2k to 3.4 kΩ, the window loss can be significantly reduced by 60% or more.

We do see customers who must regain as much margin as possible from up-stream erosions that may be hard to control or correct. This is particularly the case for OEM customers whose electrical and/or mechanical recording compo-

nents in the read channel are usually off-the-shelf items and their integrated spec may not be as optimal as desired. To alleviate such constraint, an extra, but simple, step is added to perform a fine RPG4 selection. For 10 Mb/s operation, 1.5 ns or less of static window loss from each side (from a 50 ns window width) can be achieved with data bits perfectly centered around the expected data window. The graph in *Figure 3* is a plot (represents several lots of DP8462-3 units) of typical RPG4 values vs. the amount of bit shift allowable. The data rate is 10 Mb/s and (2, 7) code with 4T preamble is used. The chip operates under a specific set of operating conditions and support components. The curves show that the absolute value of the average decode window width is 47 ns (sum of T-early and T-late times for any RPG4 value shown.) The cross-over point indicates where T-early equals T-late. The RPG4 value at this point will allow the data bit to be symmetrically centered about its decoding window.

Note that only the phase-shift is being gauged, that is, the actual deviation of the data pulse under test from the theoretical center of the data window. Hence, the plot also indicates that the customer may ''program'' (via an external current source or resistors and switches) a wide range of bias conditions on PG4 pin to perform margin tests on the read channel for final test in manufacturing or for Early/Late strobing techniques used in certain data recovery procedures.

In general the RPG configuration for window deskewing as depicted by *Figure 2C* is preferred. RPG2 is fixed at 1.5 kΩ and RPG3 may be selected proximately between 300Ω to 500Ω. This configuration offers optimum component tracking between the RPG resistors.

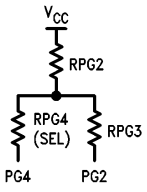

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FIGURE 2a

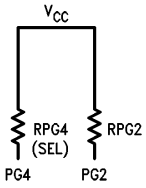

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FIGURE 2b

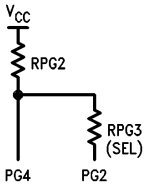

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FIGURE 2c

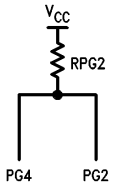

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FIGURE 2d

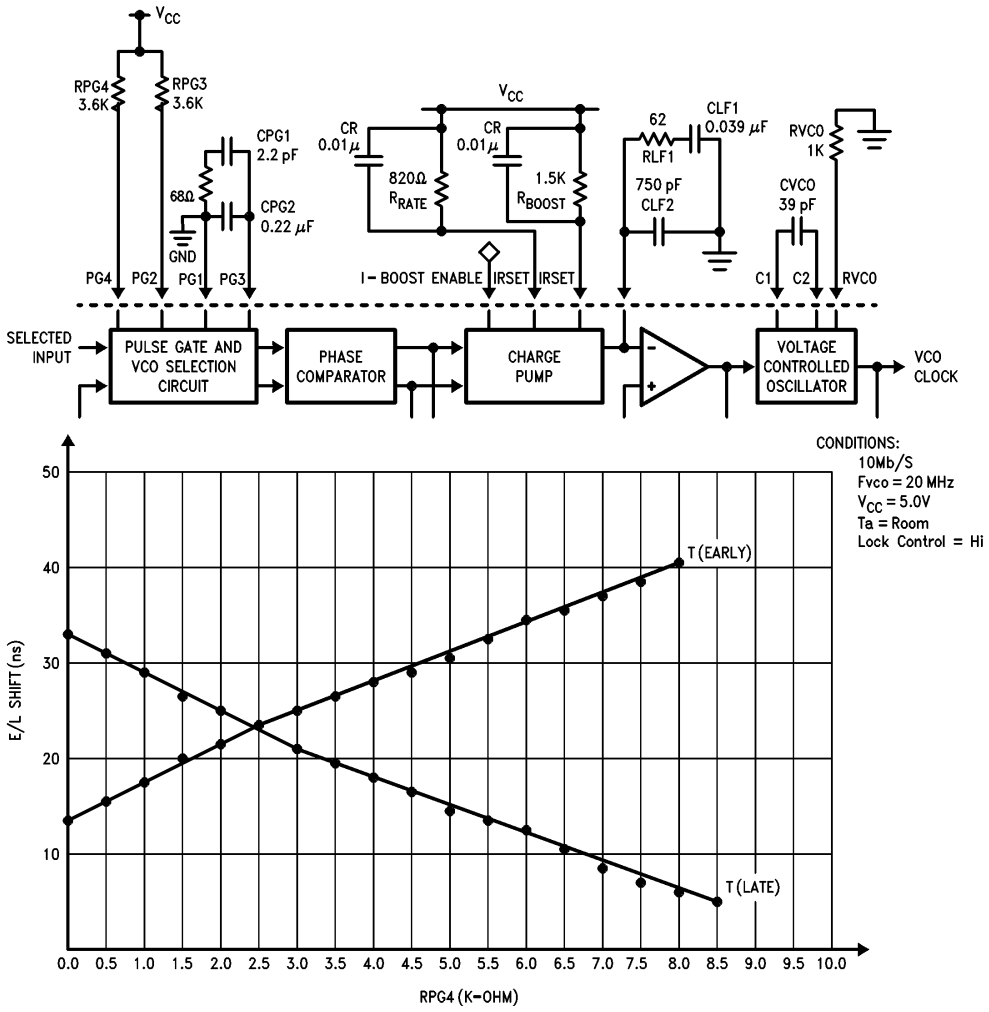

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FIGURE 3. DP8462 Early/Late Window Shift vs RPG4

Note: There is a datasheet change to the DP8462-3 part type (Aug. 1, 1986) which pertains to the test method used to qualify the Twindow spec. The parametric value which appears in the AC Electrical Characteristics table of the datasheet has not been changed. For testing the window, the original configuration required the PG2 and PG4 pins to be tied together and connected to a 1.8 kΩ, RPG2, resistor to Vcc *(Figure 2d).* This configuration is still used for testing the DP8462-4. For testing the DP8462-3, one 300Ω resistor will be palced between the PG2 and PG4 pins and PG4 will be tied to Vcc through a 1.5 kΩ resistor *(Figure 2c).* Note 6 in the datasheet will now read:

"This specification is guaranteed only for the conditions under which the parts were tested. However, significant variation from formula is not expected for other data rates and filters. The DP8462-4 specification is for the condition when PG2 and PG4 are tied together. The DP8462-3 specification is for the condition when a 300Ω resistor is tied from PG2 to PG4 and a 1.5 kΩ resistor is tied from PG4 to Vcc. External adjustment can be used to optimize Twindow as described . . . "

PRINTED CIRCUIT BOARD LAYOUT GUIDELINES:

Other than a true Digital Phase Locked Loop (DPLL), any type of analog PLL is inherently a sensitive device. Hence, the environment in which it is operated should be optimized wherever possible to improve reliability. The following is a list of PCB layout recommendations that should help to minimize the effects of VCO jitter or mislock ocurrence that can be caused by various external sources of disturbance:

1. Establish a local Vcc island or net, separate from the main Vcc plane, to which the device and its associated passive components can be connected to remove unwanted noise coupling. Vcc supply filtering should be liberal and in very close proximity to the PLL chip. The device is sensitive to inadequately filtered switching supply noise. All lead lengths of the filter capacitors between Vcc and ground pins should be as short as possible to minimize lead inductance. Inclusion of a quality high-frequency capacitor, such as a 1000 pF silver mica capacitor, in parallel with a 0.1 μF ceramic capacitor is recommended.
2. Effective capacitive bypassing of the Rrate and Rboost pins (#2 and #3) directly to the Vcc pin is very important. Again, use quality high-frequency capacitors and maintain the shortest possible electrical lead length.
3. Use the main digital ground plane for all grounding associated with the device. The ground pins and the PG1 pin should tie directly to this plane.
4. Do not locate the chip in a region of the PC board where large ground plane currents are expected.
5. Locate all passive components associated with the chip as close to their respective device pins as possible.
6. Orient the chip's external passive components so as to minimize the length of the ground-return path between each component's ground plane tie point and the chip's ground pin.
   Note: Ground noise at the loop filter components, R1, C1, and C2 which is not identically present at the ground pin (common mode), is coupled through the filter components into the VCO control voltage pin.
7. Include no planing whatsover (Vccc or ground) directly between adjacent pins. This will minimize parasitic capacitance at each pin. Planing between the two pin rows, however, is recommended (directly beneath the package).
8. Avoid running signal traces between pins to avoid unwanted noise coupling.
9. Run no digital signal lines between or adjacent to the analog pins or signals traces (pins #1 to #7 and PG3) in order to avoid capacitive coupling of digital transients.
10. Minimize the total lead length of the Cvco capacitor. Inductance in the path degrades VCO performance, as does parasitic pin capacitance.
11. Do not place any bypass filtering at the Rvco pin (minor coupling of the VCO waveform into this pin is normal and acceptable).
12. Eliminate negative-going voltage transients (undershoot) at the digital input pins (pre-termination of driving lines may be necessary) to avoid drawing transient input-clamp-diode current from the device pins. Negative undershoot at the 2F Clock and the Encoded Data inputs should be removed to avoid excess VCO phase movement and window margin degradation. A damping resistor in series from the driving circuitry is recommended (typically 200Ω will be sufficient depending on the characteristic impedance of the path).
13. Minimize digital output loading (VCO, Phase Comparator Test, and Synchronized Data); i.e., if such outputs must drive large loads or long lines, employ buffers.
14. Allow unused digital output pins to float, unconnected to any net.
15. Avoid locating the chip within strong electromagnetic fields. If possible, choose the ''quietest'' region of the PC board.
16. If chip socketing is desired, use a low-profile, low mutual capacitance, low resistance, forced-insertion type (gold plated socket-strips are recommended). In general, avoid the use of ''ZIP-DIP'', zero-insertion-pressure sockets. If there is a need for them such as in batch testing of devices, the new low-profile ''ZIP'' sockets may still be used with acceptable results. The supporting passive components must be soldered directly under the socket pins with virtually zero lead length allowed.
17. Do not use wire-wrap interconnect, even in an evaluation set-up. Point-to-point wiring is acceptable, but the prototype board must have (or improvise) a decent ground plane or strips and Vcc nets.
18. Make allowance for pin-to-pin capacitance when determining Cvco (typically 4 pF to 5 pF) from datasheet formula.
19. When using PCC (plastic chip carrier) package, space for passive component connection to the device will be considerably tighter. It is acceptable to have axial-lead resistors (not capacitors) standing upright, but, the shorter lead must be connected to the device pins to obviate noise induction to sensitive nodes.
20. In multi-layer PCB layout, as in miniature board designs for small drive systems, do not allow any power planes to run into the device region to prevent introducing unwanted noise into the chip.
21. The crystal oscillators may be designed with CMOS inverters such as the 74HC04. If the device gain is too high for the circuit, proper oscillation may not occur. As an alternative, use National's unbuffered 74HCU04 instead (which may require different capacitor values for the oscillator).

EVALUATION BOARD FOR THE DP8462

An example of a good PCB layout is portrayed by the artwork for the DP8462 evaluation PC board in *Figure 4*. This hardware simplifies the task wherein customers evaluate and correlate devices. This evaluation/demonstration board is a compact, convenient, self-contained test set-up with the following features:

— Housed in a compact, pocket-sized PCB

— On-Board programmable data pattern generator

— Self-contained movable-bit generator with continuous adjustable bit delay time and pulse width. Operates to 25 Mb/s data rate.

— Two (2) independent 2F frequency oscillator sources on board for 2F Reference Clock and for clocking the data pulses.

— Four (4) selectable Early/Late strobe settings for window shifting tests; one range is made variable for fine tuning experiments.

— Programmable Lock-Control and Preamble-Select (3T/4T) selections.

— Reference bit and sync-bit pulse output for convenient measurement and triggering needs.

— Direct outputs to ratio counter for monitoring during window margin tests.

First, within the following discussion the method used by National for window testing (manufacturing) will be explained. Secondly, it will be shown how this compact hardware has the ability to perform similar evaluations in a laboratory bench set-up.

WINDOW TEST PHILOSOPHY

The test method used to determine the data synchronizer's tolerance to bit shift is explained below. Test procedures and test hardware have been developed to measure the device A.C. performance. These can easily be ascertained and correlated by any customer regardless of their application specifics. In customers' applications, signal sources may be quite different; they can range from magnetic or optical media, to transmission lines (as in token rings). In each case, the method of pulse detection requires different techniques. Therefore, in order for every customer to be able to agree upon a representative figure of merit, we stipulate a ''Static Window Margin Test'' method. Consequently, for correlation purposes, the window margin test of the PLL chip must not be tested in the system environment. Furthermore, the input signals to the PLL should be supplied from a stable word generator or equivalent source and not from the read outputs of any disc or tape drive system (the PLL chip, not the signal source, is under investigation). In addition, a fixed set of passive components is used for each data rate of interest. In this manner, a controlled condition is established which removes any ambiguity; correlation of Twindow data can thus be performed confidently.

Refer to the timing and test sequence flow diagrams in *Figures 5* and *6*. The A.C. screening test is as follows: The device under test is first powered-on and set in the non-read mode. It will remain in this mode for 200 VCO cycles to allow the PLL to acquire a stable lock to a crystal 2F reference source. The device is then switched to the read mode by asserting the Read Gate input to a logic high level. This causes the internal input multiplexer to switch the PLL input from the crystal 2F reference source to the encoded preamble data pattern which is asynchronously derived from a signal pattern generator. (The preamble pattern is a string of 1-0-0-0 . . . , 4T preamble.) The PLL usually can lock onto the encoded data in less than two bytes of sync pattern. When 16 consecutive preamble bits are validated by the internal detection circuitry, the Preamble-Detected output becomes active-low, indicating lock has been achieved. The preamble continues for a minimum of 200 VCO cycle times after Read Gate assertion to ensure the device will be very stable prior to the window margin test.

When inserting the movable test bits following the last preamble bit, it is necessary to suppress at least as many data pulses (missing bits) as the coding scheme requires before inserting either the Early or Late test bit to avoid interference from an adjacent pulse. The code must not be violated even if the movable bit is allowed to be shifted into an adjacent window. In the 5 Mb/s example, in *Figure 6*, the amount of decode-window loss is determined by shifting a test bit toward the window center starting from 10 ns outside the nominal window boundary. The bit will be moved across the window boundary toward the nominal window center in incremental steps until it resides in a position where it will be recognized by the device under test as being in the appropriate window for a large number of sequential read operations. For a device which passes specification, the movable bit will move no closer to the nominal window center than 40 ns (the ideal half-window width (50 ns) minus the Twindow spec. (10 ns)), before the bit falls into the proper decode window. Hence, the Early test bit begins at 10 ns away from (outside) the left side of the nominal window boundary and moves toward the center of the window by 1 ns increments until the corresponding Synchronized Data output is found at its expected location. Similarly, the Late test bit approaches from the right hand side of the nominal window boundary starting at 10 ns outside the boundary and shifts toward the window center. An automated tester used in manufacturing verifies that the Synchronized Data output and the shifted test bit input waveforms are in their respective valid locations for 100 consecutive successful operations (a test time versus confidence compromise). Parts that exhibit less than 6 ns of window loss from both the front (Early bit) and the back (Late bit) window tests at a 10 Mb/s data rate are designated −3 graded parts. Devices with window truncation of less than 10 ns at 5 Mb/s data rate are designated as the −4 grade part-type.

Device specifications are:

DP8462-4 → Twindow Tolerance = 10.0 ns
DP8462-3 → Twindow Tolerance = 6.0 ns

DP8462 Evaluation PC Board Layout

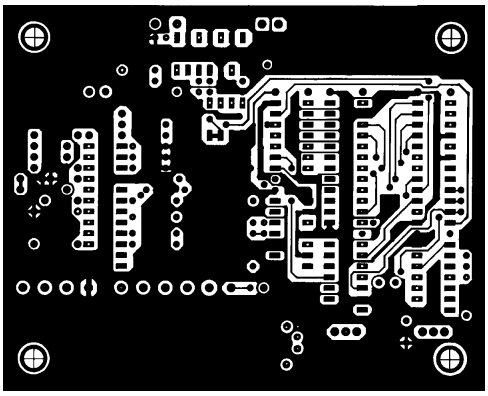

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FIGURE 4a. Component Side with Ground-Plane

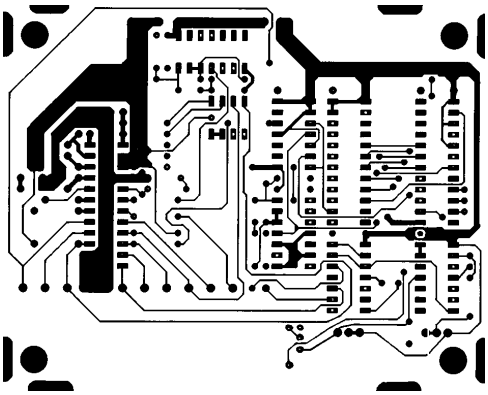

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FIGURE 4b. Trace Side, Bottom View

AC Test Sequence Flow Diagram

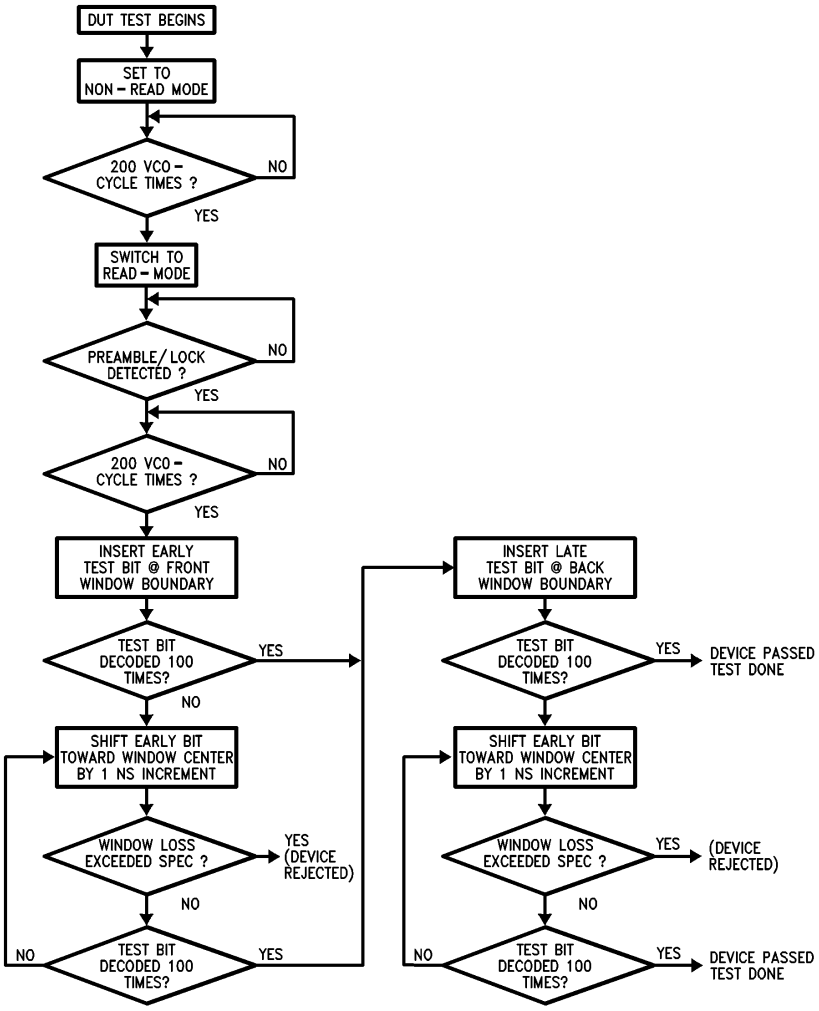

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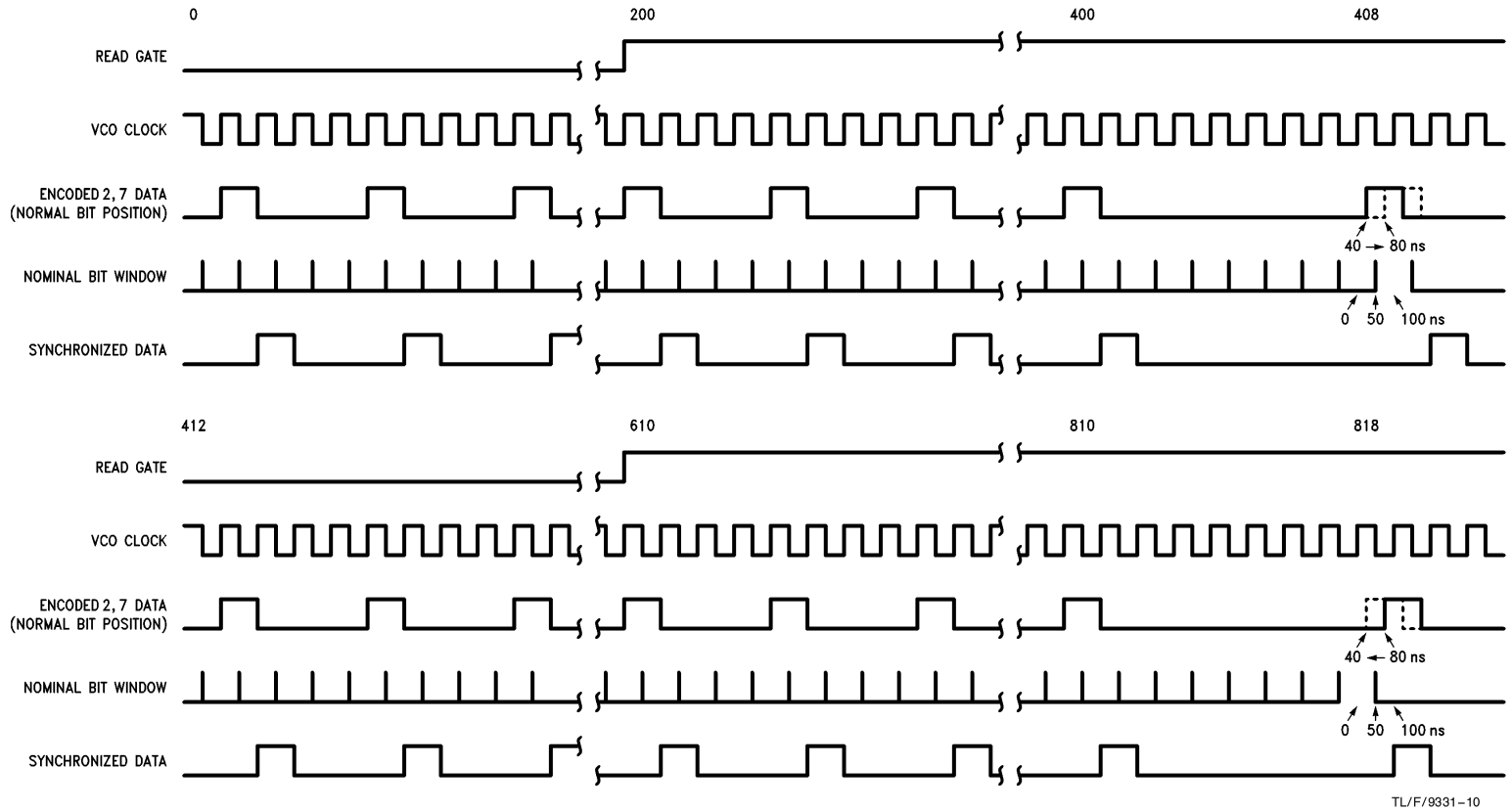
FIGURE 5



***** DP8462 AC TEST TIMING DIAGRAM (5 Mbit/s) *****

VCO = 10 MHz, Preamble is 4T
Rr = 750 Rb = 1600 R1 = 200
C1 = 0.02 μF C2 = 150 pF

FIGURE 6

DP8462 EVALUATION BOARD CIRCUIT OPERATION

The DP8462 evaluation board mentioned above performs the equivalent test sequence as in automatic testers. However, it does not require elaborate pattern generators and measurement systems, or a software contorlled sequencer. Only a calibrated oscilloscope and possibly a digital ratio counter are needed to monitor the device under test. Refer to the schematic diagram in *Figure 7* and the timing diagram in *Figure 8*.

One half of U4 and U6 together form a 9-bit synchronous binary counter to cycle the address lines of U8, a read-only memory that contains all the appropriate test patterns for the Twindow test. U7 is a high speed AS (Advanced Schottky) gate used to buffer and gate the U8 ouputs to the PLL chip. U2 and U5 are CMOS inverters used to construct two crystal oscillators. One oscillator generates the 2F Reference Clock while the other sequences the rest of the logic chips. U9, a monostable multivibrator, is used to set the pulse width of a single movable bit within the Encoded Data pattern string. Q1 and its associated passive components realize a linearly variable threshold adjustment that is capable of continuously skewing the movable bit about its window center position. The other half of U4, with an ''OR'' gate of U7 and together witth U8, set up a detection window for the synchronized bit associated with the corresponding movable test bit. If the test bit is within the correct decode window position, pin #6 of U7 will yield 2 pulses in every read cycle. If the test bit falls out of its expected window only a single pulse is produced from this output of U7. Hence, this output and Read Gate can be connected to the ratio counter inputs for an accurate display of when the bit is within or outside of its expected window. The time measurement system in a laboratory oscilloscope can provide accurate Twindow readings.

DP8462 Evaluation Board

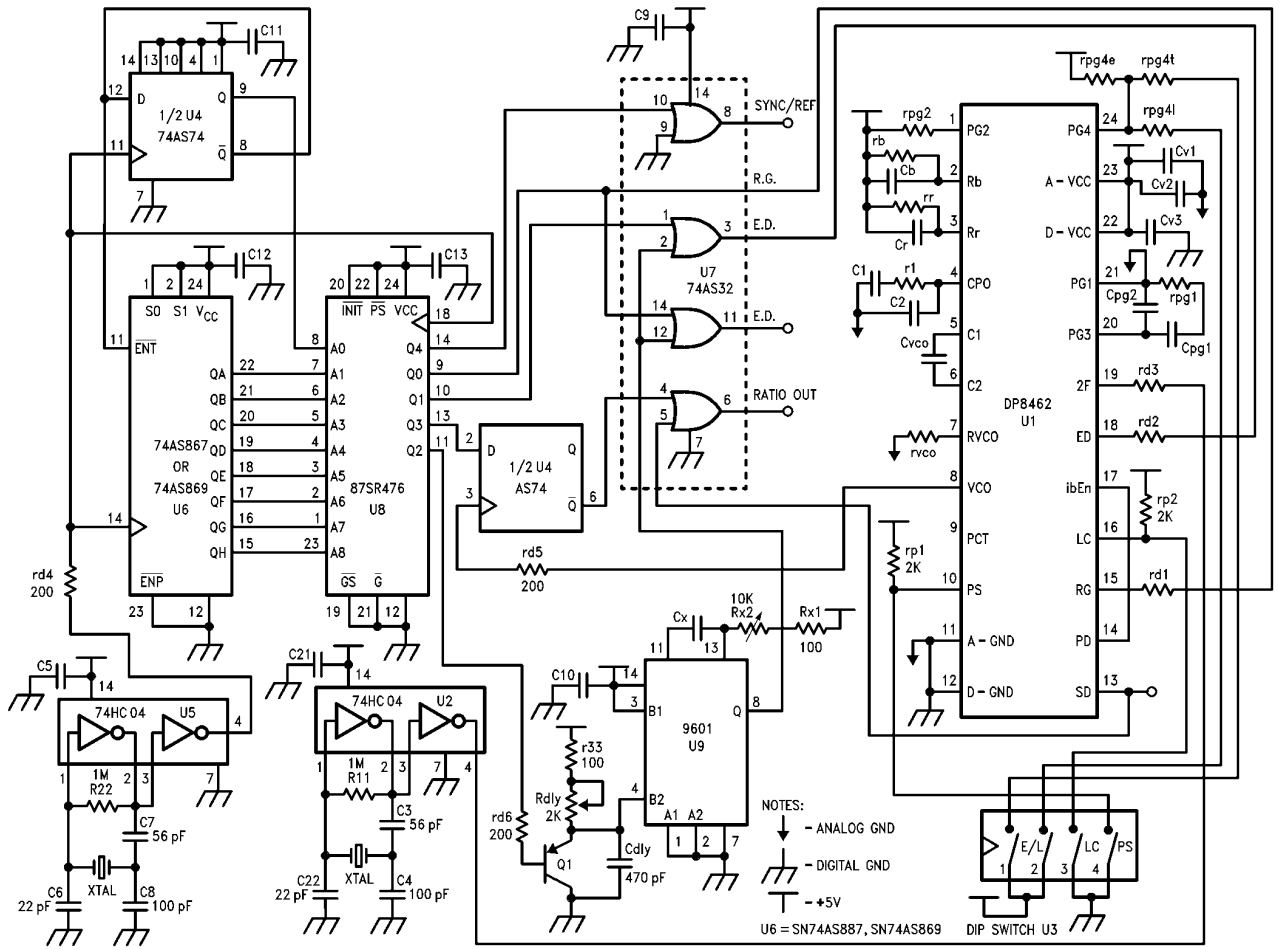


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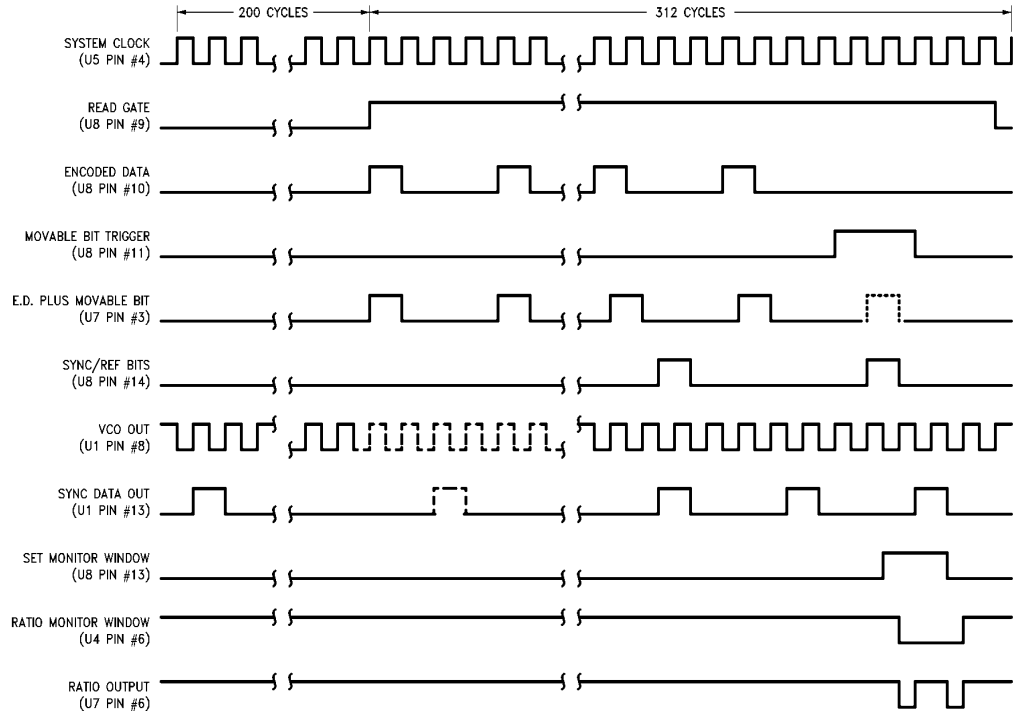
FIGURE 7



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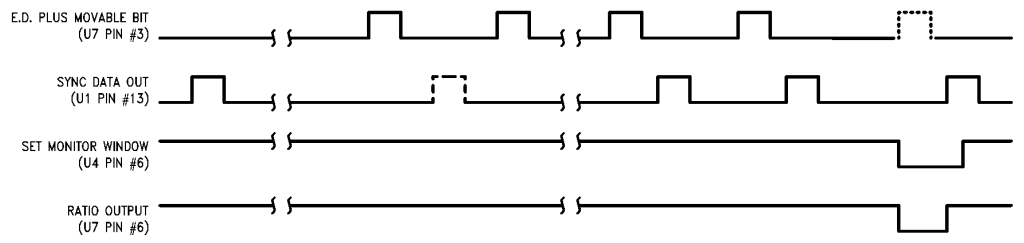
If movable bit is shifted outside of its expected decode window position:



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*__Note:__ Dotted waveforms depict movable bit signal positions; broken waveforms indicate outputs not yet stabilized after read gate assertion.

FIGURE 8. Essential Waveform Diagramatic Representation of the DP8462 Evaluation Board

The variable resistor, ''Rdly'', is used to shift the test bit about its window center. ''Rx2'' is used to adjust the pulse width of the movable bit, which should be set equal to the width of the Encoded Data pulses from the pattern generator ROM. U3 consists of 4 switches used to set Lock Control, Preamble Select, and to select different currents supplied to PG4 to control window centering or to introduce a predetermined amount of early or late shift of the window.

EVALUATION BOARD PREPARATION

Below are listed the component values currently being used by NSC for production testing at 10 Mb/s. (Values may change without notice.)

Rvco	= 1.00 kΩ	Rr	= 800Ω
Cvco	= 39 pF	Rb	= 1.8 kΩ
Cv1	= 0.1 μF	R1	= 82Ω
Cv2	= 1000 pF (Silver Mica)	C1	= 0.02 μF
Cv3	= 1000 pF (Silver Mica)	C2	= 510 pF
CPG1	= 2.2 μF	Cr	= 0.01 μF
CPG2	= 0.22 μF	Cb	= 0.01 μF
RPG1	= 68Ω		
RPG2	= 1.8 kΩ (DP8462-4), = 1.5 kΩ (DP8462-3)	(See *Figures 2c* & *d*)	
RPG3	= 0.0Ω (DP8462-4), = 300Ω (DP8462-3)		
RPG4	= 0.0Ω		

The circuit described in *Figure 7*, for evaluation of the DP8462 PLL, uses the same components as above except for RPG2 = 3.6k, RPG3 = 0, and RPG4 = Rselect. Refer to *Figure 2b*.

The center frequency of the VCO may be checked according to the datasheet (under VCO section description). It can also be conveniently confirmed by another simple technique. First, set CPO (pin #4) at ground potential and measure the VCO frequency (minimum frequency). Then apply approximately 3V to pin #4 and again measure the VCO frequency (maximum frequency). The arithmetic mean of these two measured frequency values yields the equivalent center freqency (choose appropriate Cvco value to ensure proper VCO center frequency).

Before powering up the evaluation board, notice that the circuit has been designed so that it is possible to provide each section of the test circuit, the DP8462 (via Vcc1), the 2F Clock oscillator (Vcc2), and the rest of the digital circuitry (Vcc3), with an independent +5V regulated supply. After power(s) has been on, first check U2 and U5 for proper 2F frequency outputs. If either one or both crystal oscillators appear to exhibit excessive jitter, abnormal oscillation or is being perturbed by the other oscillator, it is possible that the gain of the inverters used is too high. Replace the 74HCO4 device or use the unbuffered device, the 74HCU04, instead; (may require new capacitor values). Next monitor U8 to make certain that all the test patterns are present (refer to *Figure 8*). Trigger an oscilloscope with the SYNC/REF BITS output and display this waveform on the CRT also. Pin #8 of U7 should present two pulses, a sync bit followed by a reference bit from Q4 of U8. Q0 of U8 is the Read Gate sequence, which should be high for 312 2F Clock cycles and low for 200 2F Clock cycles. Pin #3 of U7 outputs the Encoded Data pattern from Q1 of U8. Q1 of U8 consists of a train of 4T patterns starting when Read Gate is asserted. At the end of the 4T patterns there should be an isolated pulse (movable bit). Adjust the Rx2 potentiometer so that the width of this isolated pulse matches those of the 4T pattern (or the reference bit). Also adjusting ''Rdly'' should be able to shift this pulse. Position this bit such that its leading edge aligns perfectly with the leading edge of the reference bit (refer to *Figure 8*). This alignment procedure puts the movable bit in the nominal center of its decode window. Q5 and Q6 (pins #15 and #16) of U8 are optional sync signals for triggering the oscilloscope to monitor other areas of the test sequence.

TEST PROCEDURES

Set ''DIP'' switches: SW-3 for LOCK CTL to (H) for phase-frequency mode during preamble acquisition; SW-4 for Preamble Select to (H) for 4T preamble; SW-1 and SW-2 both set to (L), this selects RPG4E = 3 kΩ on the board (or whatever value the user chooses in testing). Check SYNCHRONIZED DATA and VCO outputs, they should be stable and in lock by the arrival of the SYNC/REF bits (at least 200+ VCO cycles after Read Gate assertion).

To test the available half-window width (complement of the half-window loss), begin turning 'Rdly'' slowly while monitoring ENCODED DATA, SYNC/REF BITS, SYNCHRONIZED DATA or RATIO OUT. (It is recommended to connect READ GATE and RATIO OUT to a digital ratio counter). The ratio counter normally reads a perfect 2.0000 ratio when the test bit is within its proper decode window. Move the test bit away from its centered position (with respect to the Reference Bit positive edge) in either direction. As long as the test bit remains inside the available decode window, a ratio of two is displayed on the counter. When the test bit begins to fall outside of its decode window even occasionally, the ratio count will deviate from a perfect two ratio, indicating the window boundary has been reached. Measure the time span between the leading edge of the movable bit and that of the reference bit which corresponds to the available half-window width. Subtracting this figure from 25 ns (for 10 Mb/s data rate) yields the Twindow number (half-window truncation). Repeat the same procedure for the other half of the decode window. If a ratio counter is not used one can monitor the SYNCHRONIZED DATA or RATIO OUT node on the oscilloscope screen. As the pulse is shifted towards the adjacent window position it will begin to fade; this is the point where the window measurement should be made. This alternate test also gives a reasonably accurate estimate of the Twindow specification.

Switches #1 and #2 of U3 along with the various RPG4 components have been selected for the user who desires to experiment with early/late strobe or select RPG4 in a system design for minimum window offset. To experiment with these different options this procedure is as follows (for 10 Mb/s transfer rate): Refer to *Figure 9*.

1. Choose RPG4E ≅ 6.2 kΩ, RPG4T ≅ 620Ω, and for RPG4L select a 5.0 kΩ potentiometer. (These values may be slightly different for other data rates.)
2. Set switches #1 and #2 to (H), this selects RPG4E only. With a relatively large resistor value, a low level bias current is allowed to the PG4 pin. This produces a wider LATE window (w.r.t. nominal bit position) and a correspondingly smaller EARLY window.

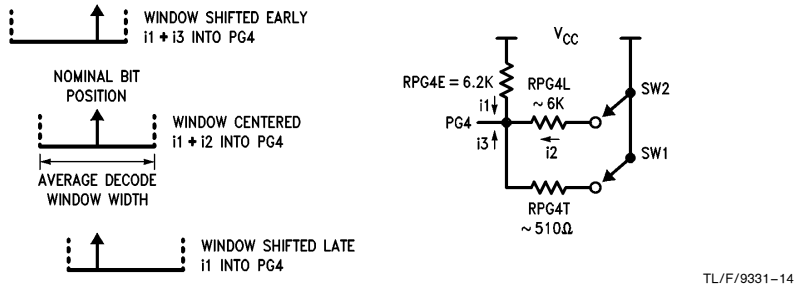

FIGURE 9

3. Set switches #1 to (L) and #2 to (H), this selects RPG4E and RPG4T in parallel. The effective RPG4 value will be the smallest of all the combinations of RPG4 resistors, hence, a larger bias current into PG4. This yields a wider EARLY window and a narrower LATE window (w.r.t. nominal bit position).
4. Set switches #1 to (H) and #2 to (L), this will select RPG4E and RPG4L; the combined value nulls out the window offset (on-time). For an easier set-up, one can utilize a single potentiometer for RPG4L (delete RPG4E and RPG4T) to determine an optimum RPG4 resistor value to nullify any inherent window offset.

SUMMARY

The DP8462 PLL chip is the third circuit in the family of National's second generation high performance data synchronizers. It combines the features of the DP8461 and DP8465 for non-harmonic phase detection in the non-read mode (DP8461 and DP8465) and in read mode during preamble acquisition (DP8461), and harmonic phase detection in read mode. Furthermore, in the DP8462, these mode selections are user controlled. Analog and digital Vcc and ground are brought out to separate device pins which further minimizes phase jitter and internal interference. Window center offset is also reduced or can be nulled out in design with a fixed external resistor. These improvements have significantly eased the task of design and volume production of higher transfer rate systems (data rates of 10 Mb/s to 15 Mb/s), where the data windows are proportionally smaller. The DP8462 device is part of National Semiconductor's DP8460 Series Disc System Data Path Chip Set. It has been designed into many disc drives and controller systems worldwide in conjunction with other members of this family such as the DP8464B pulse detector, the DP8463B (2, 7) ENDEC CHIP; the DP8466 DDC, and the DP8475 SCSI controller.

For further information regarding the DP8462 and the DISK DATA PATH chip set, please refer to National's ''APPS Handbook Volume 1: Mass Storage''.

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408