National Semiconductor Corporation

MOS INTEGRATED CIRCUITS

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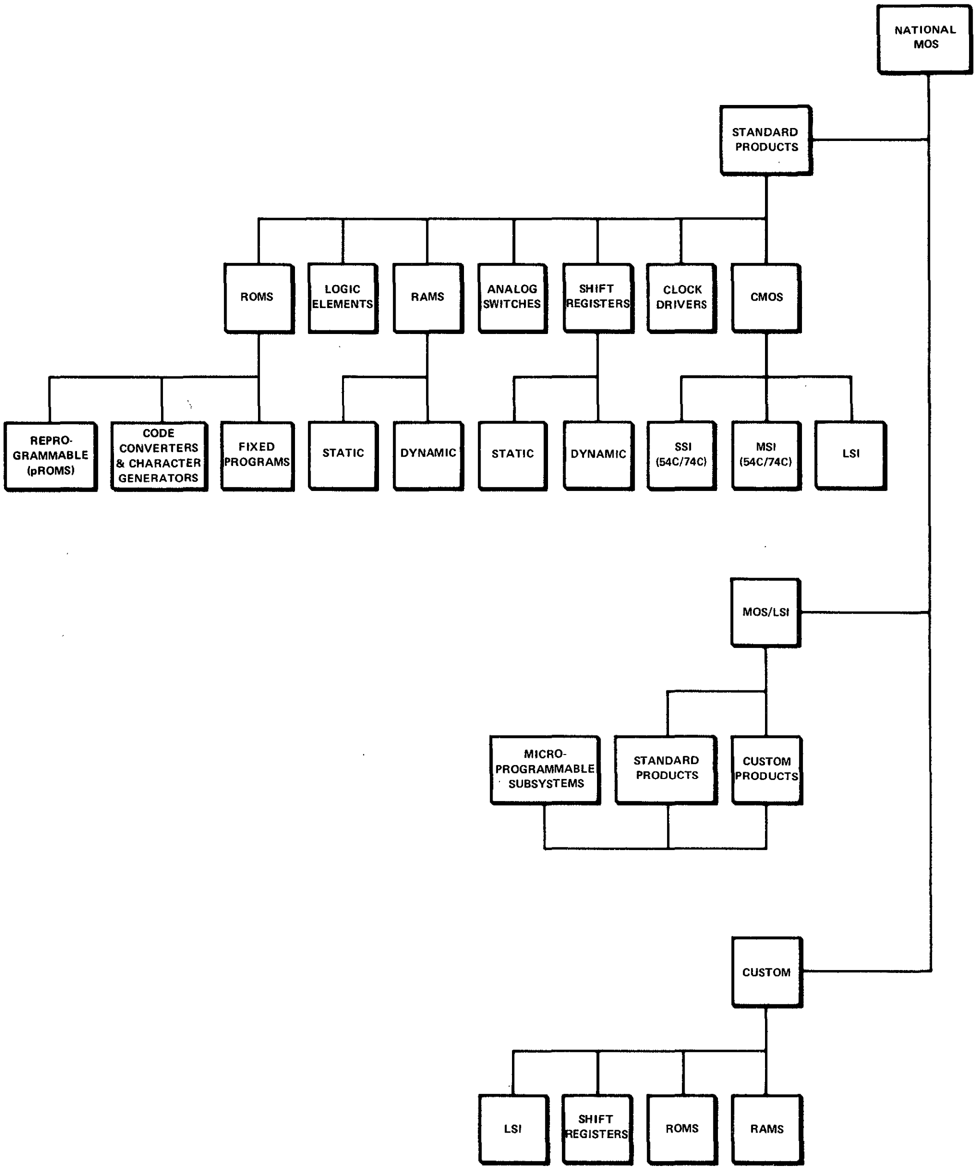
Introduction

Here is National's newest handbook on MOS products. Extra copies of this handbook, plus those on our other major product lines — digital, linear and transistors — are also available. To receive our handbooks, contact a National sales office, representative or distributor; to keep current on our growing product lines ask to be placed on our mailing list.



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Dynamic Shift Registers

Static Shift Registers

ROMs

RAMs

Clock Drivers

Analog Switches

Logic Elements

ROM Character Generators

For information on the following character generators contact National,Santa Clara:
- MM4240AD/MM5240AD Katakana Alphabet Character Generator
- MM4240AF/MM5240AF 5x7 ASCII-6 with Low True Outputs Character Generator
- MM4240AH/MM5240AH 5x7 ASCII-6 with High True Outputs Character Generator
- MM4240AK/MM5240AK 5x7 ECMA-6 (French, British, Italian) Character Generator
- MM4241AAN/MM5241AAN ASCII Vertical Scan Character Generator

ROM Code Converters

For information on the following code converters contact National, Santa Clara:
- MM3501TL ASCII to Baudot, Baudot to ASCII Code Converter
- MM4213UW/MM5213UW EBCDIC-8 to Hollerith Code Converter
- MM4221TM/MM5221TM ASCII to Baudot, Baudot to ASCII Code Converter
- MM4230JC/MM5230JC ASCII to Hollerith Code Converter*
- MM4230JP/MM5230JP ASCII to MDS Code Converter
- MM4230JQ/MM5230JQ Hollerith to EBCDIC Code Converter*
- MM4230JR/MM5230JR Selectric to EBCDIC Code Converter*
- MM4230JS/MM5230JS EBCDIC to Selectric Code Converter*
- MM4230SQ/MM5230SQ ASCII-8 to Hollerith Code Converter

Application Notes

MOS Briefs

*Not recommended for new designs. TBA — To Be Announced

MOS Selection Guide

	PRODUCT TYPE NO. MIL/COM	DESCRIPTION	MAX FREQ OR MIN ACCESS TIME	V_{SS}	V_{DD}	V_{DD2} OR V_{GG}	CLOCK SWING
Dynamic S/R	MM400/MM500	Dual 25 Bit	1.0 MHz	+10	GND	None	16
	MM401/MM501	Dual 25 Bit	1.0 MHz	+10	GND	None	16
	MM402/MM502	Dual 50 Bit	1.0 MHz	+10	GND	None	16
	MM403/MM503	Dual 50 Bit	1.0 MHz	+10	GND	None	16
	MM406/MM506	Dual 100 Bit	1.0 MHz	+10	GND	None	16
	MM407/MM507	Dual 100 Bit	1.0 MHz	+10	GND	None	16
	MM4001A/MM5001A	Dual 64 Bit Split Clock	2.5 MHz	+5	None	–12	17
	MM4006A/MM5006A	Dual 100 Bit	2.5 MHz	+5	None	–12	17
	MM4007/MM5007	Dual 100 Bit Mask Programmable	2.5 MHz	+5	None	–12	17
	MM4010A/MM5010A	Dual 64 Bit Accumulator	2.5 MHz	+5	None	–12	17
	MM4011A/MM5011A	Dual 64 Bit Common Clock	2.5 MHz	+5	None	–12	17
	MM4012/MM5012	Dual 256 Bit Accumulator	2.5 MHz	+5	None	–12	17
	MM4013/MM5013	1024 Bit Accumulator	2.5 MHz	+5	None	–12	17
	MM4015A/MM5015A	Triple 60 + 4 Accumulator	2.5 MHz	+5	None	–12	17
	MM4016/MM5016	500/512 Bit	2.5 MHz	+5	None	–12	17
	MM4017/MM5017	Dual 500/512 Bit	2.5 MHz	+5	None	–12	17
	MM4018/MM5018	Triple 64 Bit	2.5 MHz	+5	None	–12	17
	MM4019/MM5019	Dual 256 Mask Programmable	2.5 MHz	+5	None	–12	17
	MM4020/MM5020	Quad 80 Bit	2.5 MHz	+5	None	–12	17
	MM4021/MM5021	Triple 80 Bit	2.5 MHz	+5	None	–12	17
	MM4100/MM5100	144/156 Bit	1.0 MHz	+5	None	–12	17
	MM4104/MM5104	360/359 + 288/287, 40/32 Bit	2.5 MHz	+5	None	–12	17
	MM4105/MM5105	Quad 64 Accumulator	2.2 MHz	+5	None	–12	17
	MM1402A	Quad 256 Bit	5.0 MHz	+5	–9	None	14
	MM1403A	Dual 512 Bit	5.0 MHz	+5	–9	None	14
	MM1404A	Single 1024 Bit	5.0 MHz	+5	–9	None	14
	MM5024A	Single 1024 Bit with Internal Pullup Resistor	5.0 MHz	+5	–9	None	14
Static S/R	MM404/MM504	Dual 16 Bit	1.0 MHz	+10	GND	–6	16
	MM405/MM505	Dual 32 Bit	1.0 MHz	+10	GND	–6	16
	MM4040/MM5040	Dual 16 Bit	2.2 MHz	+5	GND	–12	17
	MM4050/MM5050	Dual 32 Bit Common Clock	1.6 MHz	+5	GND	–12	17
	MM4051/MM5051	Dual 32 Bit Split Clock	1.6 MHz	+5	GND	–12	17
	MM4052/MM5052	Dual 80 Bit	1.6 MHz	+5	GND	–12	17
	MM4053/MM5053	Dual 100 Bit	1.6 MHz	+5	GND	–12	17
	MM4054/MM5054	Dual 64/72/80 On Chip Clock	2.2 MHz	+5	GND	–12	TTL
	MM5081	High Voltage (V_L=–55V) MM413	250 kHz	GND	–20	–20	–20
ROMs	MM4203/MM5203	2048 Bit ROM (Pin Compatible MM4213) TSL	1.0 μs	+5	–12	–12	None
	MM4210/MM5210	1024 Bit (256 x 4)	650 ns	+12	–12	–12	None
	MM4211/MM5211	1024 Bit (256 x 4)	950 ns	+5	–12	–12	None
	MM4213/MM5213	2048 Bit ROM (Pin Compatible MM4203) TSL	750 ns	+5	–12	–12	None
	MM4220/MM5220	1024 Bit (256x4 or 128x8)	650 ns	+12	–12	–12	None
	MM4221/MM5221	1024 Bit (256x4 or 128x8)	950 ns	+5	–12	–12	None
	MM4230/MM5230	2048 Bit (512x4 or 256x8)	725 ns	+12	–12	–12	None
	MM4231/MM5231	2048 Bit (512x4 or 256x8)	950 ns	+5	–12	–12	None
	MM4232/MM5232	4096 Bit (1024x4 or 512x8) TSL	1.0 μs	+5	–12	–12	None
	MM4240/MM5240	2560 Bit Character Generator	600 ns	+12	–12	–12	None
	MM4241/MM5241	3072 Bit Character Generator	900 ns	+5	–12	–12	None
	SK0003	Sine Look-Up Table	1.0 MHz	+12	–12	–12	None
RAMs	MM1101	256 Bit Static (256 x 1)	1.5 μs	+5	–7	–10	None
	MM11011	256 Bit Static (256 x 1)	1.0 μs	+5	–7	–10	None
	MM1101A	256 Bit Static (256 x 1)	1.5 μs	+5	–9	–9	None
	MM1101A1	256 Bit Static (256 x 1)	1.0 μs	+5	–9	–9	None
	MM1101A2	256 Bit Static (256 x 1)	500 ns	+5	–9	–9	None
	MM5260	1024 Bit Dynamic (1024x1)	350 ns	+5		–12	15
	MM5262	2048 Bit Dynamic (2048x1)	360 ns	+5		–15	18
	MM5263	2048 Bit Dynamic with TSL Output (On Chip Sense Amp)	390 ns	+5		–15	18
	MM1103	1024 Bit Dynamic (1024x1)		+16	GND	12	19
Logic	MM480/MM580	Dual 3 Input NOR Gate	200 ns	+10	GND	None	None
	MM481/MM581	Dual Exclusive OR Gate	400 ns	+10	GND	None	None
	MM482/MM582	Dual Digital MUX Switch	400 ns	+10	GND	None	None
	MM483/MM583	JK Flip Flop	2.4 MHz	+10	GND	None	10V

MAPS

microprogrammable arithmetic processor system

general description

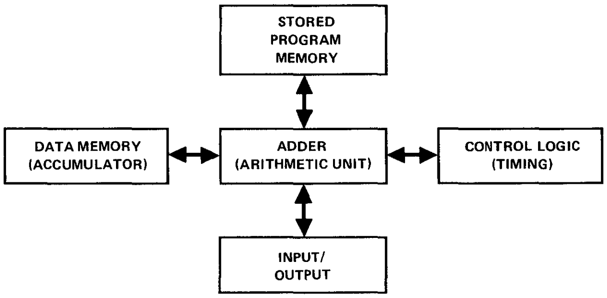
Microprogrammable Arithmetic Processor System devices (MAPS) are MOS/LSI elements that represents a general purpose serial data processor (see Figure 1). The system can be programmed to operate in binary or BCD up to a 76 bit one cycle data word. The system provides a wide variety of data word formating and is applicable to any serial arithmetic control system from machine and process control to business machines.

The basic system is comprised of five MOS/LSI sub-system elements:

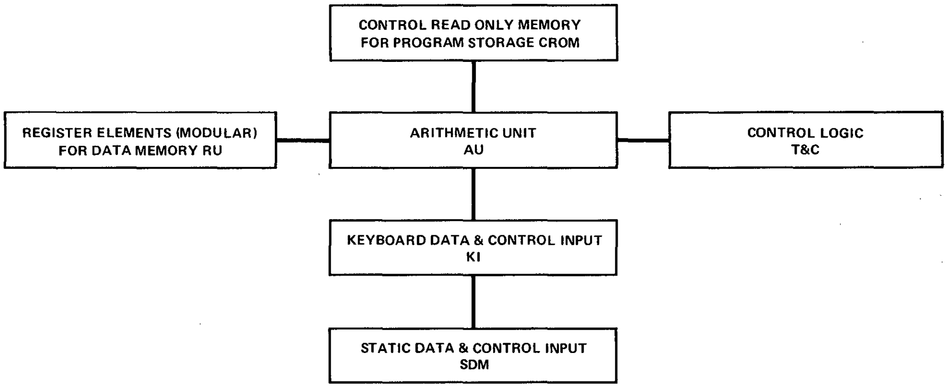
- MM5700 Arithmetic Unit
- MM5701 Register Unit
- MM5702 Timing and Control Unit
- MM5704 Keyboard Interface Unit
- MM5705 Control Read Only Memory

Additional elements for system expansion are:

- MM5703 Control Read Only Memory
- MM5706 Static Data Monitor



1a. General Computer Organization



1b. MAPS Organization

FIGURE 1. General Purpose Computer Organization Compared to MAPS

The five basic elements are interconnected by a serial bit bus-organized distribution system with three data buses, and three command buses (see block diagram Figure 2). The basic cycle of the system is 76 bits, controlled by a set of 32 data micro-instructions stored in the arithmetic and register unit.

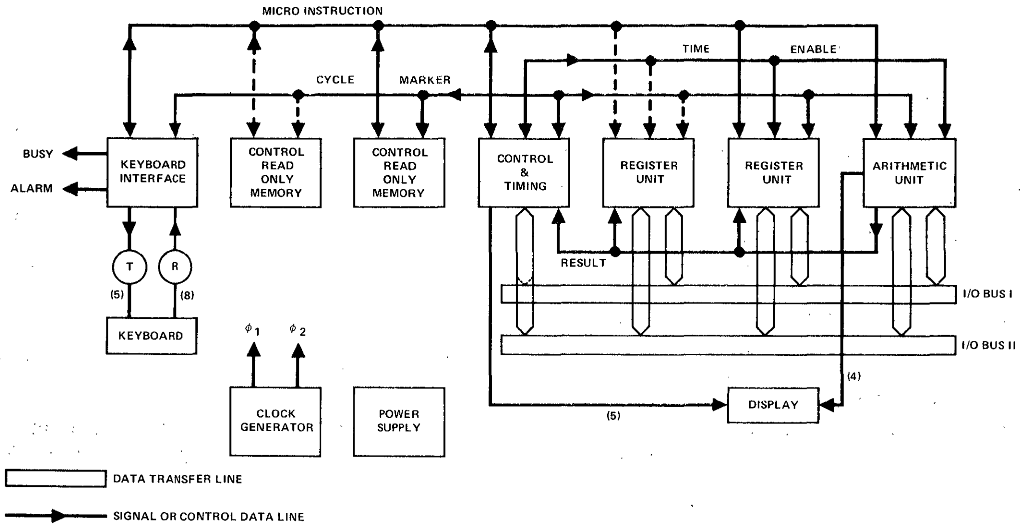


FIGURE 2. MAPS Block Diagram

Data between these elements is passed serial over the three data buses. The logic sequence of data handling is programmed in the CROM element, each CROM provides the system 256 words of a 10-bit command. The T&C element interpolates each command and generates proper time synchronization and time enable signals for performing the command, thus allowing the data in the AU and RU elements to be acted upon. To perform data result tests and control operations, 32 command microinstructions are stored in the T&C element. The format and function performed by each command instruction is programmable by storing the proper bit pattern for the op-code in CROM storage. This allows the same basic command instruction to be programmed differently for a wide variety of machine applications. The keyboard encoder will accept up to 32 dynamic keys and 8 static switch inputs and the static data monitor will scan two banks of 8 data points.

The specific system configuration is expandable since additional RU, CROM, KI and SDM elements can be added on the data and command bus system. The system will accommodate up to 32 CROMs or a total of 8192 microprogrammed instructions. Access from microprogrammed instructions in RAM and mass storage can be performed and controlled. This allows the MAPS elements to function as mini-processors within a larger system.

The system is dynamic two phase logic fabricated with National's bipolar compatible, P-channel enhancement mode, low threshold technology. All elements are in small 16 and 24 pin dual-in-line packages for easy handling and test. Compatibility with the keyboard, data codes, timing and programs required for the system application is obtained during wafer fabrication by mask programming. A preprogrammed calculator kit with 14-digit display outputs is available for evaluation and general use.

features

- Bus-organized for easy expansion and interface with external systems
- Keyboard input
- Static data monitor binary or BCD input
- Error-free keyboard decoding (see MM5704AA data sheet)
- Data and display control outputs
- Clock rates to 750 kHz two phase logic
- DTL/TTL compatible on output for display
- Standard +5V and −12V supplies
- Standard 16-pin and 24-pin DIPs

applications

- General purpose serial computers
- "Smart" data terminals
- Numerical controls
- Electronic business machines
- Point of sales equipment
- Electronic scales
- Electronic calculators
- Traffic controls
- Medical electronics (analyzers, patient monitoring, etc.)

MAPS

MM5704AA MOS/LSI keyboard interface subsystem

general decription

The MM5704AA keyboard interface subsystem is a monolithic MOS/LSI circuit utilizing P-Channel enhancement mode low threshold voltage technology. It self-scans 32 dynamic keys (4 x 8 matrix) and 8 static keys for switch closure. The dynamic key positions are encoded into a 9-bit code that is transmitted bit serial. The static keys are encoded into an 8-bit code. A read-only memory allows customer programming of the character code for the 9-bit code. Control logic provides programmable delay times to match the switch bounce characteristics and key matrix capacitance for a wide selection of keyboard elements. Two "busy" lines are provided so several keyboard interface chips can be paralleled to decode larger key matrixes. Two key "roll over" is provided along with positive lock-out for ambiguous key depressions.

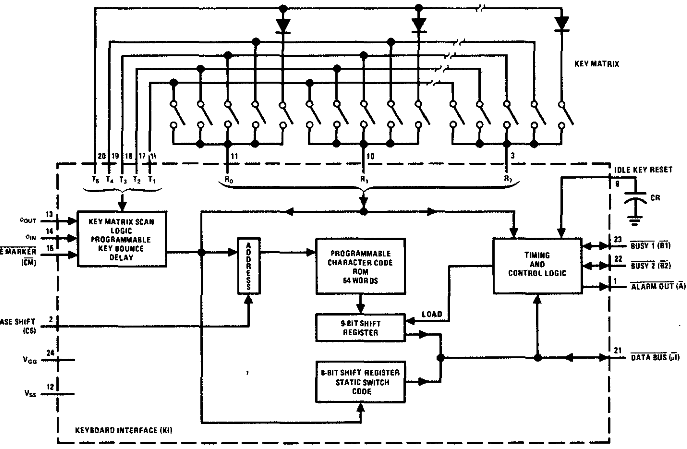
features

■ Bipolar compatibility	Minimum external components required
■ Standard supplies	+5V, −12V
■ Bit serial data transmission	Up to a 9-bit code
■ Character code selection	Programmable character code ROM
■ Error-free decode	Provides two key "roll over" multiple key lock-out by an alarm busy line for active decode indication
■ High speed	0.75 MHz
■ Keyboard element flexibility	Programmable key bounce delay Programmable key matrix capacitance delay Programmable keys for alarm clear Programmable idle key reset delay
■ Large keyboard	32 dynamic keys 8 static keys
■ Expandable	Busy line ORed output (expandable in multiples of 32 dynamic — 8 static keys)
■ Timing control	Provides "character ready" command and responds on "transmit" command
■ Standard package	24-pin dual-in-line package

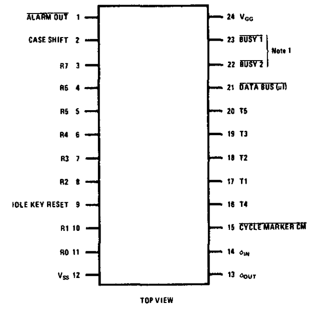
applications

■ Keyboard decode	Terminal interface Calculator Accounting machine Typewriter
■ Binary multiplexer/encoder	Binary remote sensing

block and connection diagrams



Dual-In-Line Package



Note 1: Busy 1 and Busy 2 are connected only when required on custom keyboard interface units. Busy 1 and Busy 2 are connected on MM5704-AA.

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} – 20.0V	Operating Temperature Range	0°C to +70°C
Bulk Reference (substrate)	V_{SS}	Storage Temperature Range	-55°C to +125°C
Package Power Dissipation at 70°C	500 mW		

electrical characteristics

T_A = 25°C; V_{SS} = +5V, V_{GG} = –12V; or V_{SS} = 0V, V_{GG} = –17V; all supplies ±5%, unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clocks (ϕ_{IN} ϕ_{OUT})					
Repetition Rate (ϕ_f)	Min. ϕ_{pw}	0.02		0.75	MHz
Pulse Width (ϕ_{pw})					
1 Min (90%)	Min. ϕ_f	0.3	0.5		μs
0 Min (10%)		0.4	0.6		
Amplitude					
Logic Level "0"	With Respect to V_{SS}	0		-1.5	V
Logic Level "1"		-16	-17	-19	V
Delay Times					
ϕ_d	Min. ϕ_f and	0.35			μs
ϕ_d	Min. ϕ_{pw}	0.35			
Input Capacitance					
ϕ_{IN}	V_{IN} = 0.0V		125	175	pF
ϕ_{OUT}	f = 1.0 MHz		125	175	
Leakage Current					
ϕ_{IN}	@ 25°C		0.1	2.0	μA
ϕ_{OUT}	V_{IN} = –18V		0.1	2.0	
Data Inputs					
Amplitude					
Logic Level "0"	With Respect to V_{SS}	0	-0.7	2.0	V
Logic Level "1"		-6	-8		V
Setup Time (t_{ds})		50	100		ns
Hold Time (t_{dh})		25			ns
Capacitance	V_{IN} = 0.0 V f = 1.0 MHz		15		pF
Leakage Current	V_{IN} = –18V @ 25°C All pins are grounded except data input pin under test.		0.1	2	μA
Data Outputs	With Respect to V_{SS}				
Amplitude	MOS Load				
Logic Level "0"	(1.0 MΩ and 50 pF)	0	-1.0	-1.5	V
Logic Level "1"	μl and Alarm	-7	-10		V
Transition Times	MOS Load				
T_{pd0}	(1.0 MΩ and		150	350	ns
T_{pd1}	50 pF)		150	350	
		(Measured from ϕ_{IN} "one to zero" transition)			
Amplitude	TTL Load @				
(Alarm Outputs)	V_{GG} = –12V; V_{SS} = +5V				
TTL	I_L = 0.5 mA				
Logic Level "1"	I_L = 1.6 mA			2.4	V
Logic Level "0"	Ambient Temp. 25°C	0.4			V
Transition Times	TTL Load @				
T_{pd0}	I_L = 1.6 mA		150	350	ns
T_{pd1}	I_L = 0.5 mA		150	350	
Power Consumption					
DC Supply Current Drain					
I_{GG}	Average current at ϕ_f = 0.75 MHz V_{GG} = –20V ϕ_{IN} ϕ_{OUT} = 20V		15	20	mA
Key Matrix Lines					
R_0 through R_7 Lines					
Amplitude					
Logic Level "0"	With Respect to V_{SS}	V_{SS}		-1.5	V
Logic Level "1"			-8		V
T_1 through T_5 Lines					
Amplitude					
Logic Level "0"	With Respect to V_{SS}	V_{SS}		-2.0	V
Logic Level "1"		-7	-10		V
PROGRAMMABLE FEATURES					
Key Bounce Delay	E counter programmed for modulus = 6 (Note 1)				ms
Key Matrix Capacitance Delay	D counter programmed for modulus = 4 (Note 2)				pF
Character Code	ASCII 8th bit odd parity	See code pattern			
Control Features					
Keyboard Clear Switches	T_4R_7 & T_1R_7; T_4R_5 Note 3				
Key Rollover	Programmed for two key rollover				
Idle Key Reset Capacitor CR	External Capacitor tied from Pin 9 (Note 4)				pF
Static Switch Form	Normally Open (No) (Note 5)				
Static Transmit Bit Interval	Bit Time 5 (Note 6)				
Static Key Form	Normally Closed (NC) (Note 5)				

Note 1: Key bounce delay is total delay defined as D counter programmed modulus = 4 driven from cycle marker (CM) and E counter programmed modulus = 6. See programming section and typical application.

Note 2: Key matrix capacitance is the total lead capacitance from the "T" and "R" lines excluding keyboard package capacitance. This is the total capacitance that must be charged before scanning starts. D counter is programmed for this delay.

Note 3: Three keys on the keyboard have been programmed to clear on "alarm" condition if present. These are (T_4R_7), & (T_1R_7) and (T_4R_5) keys. This programming does not affect normal key operation.

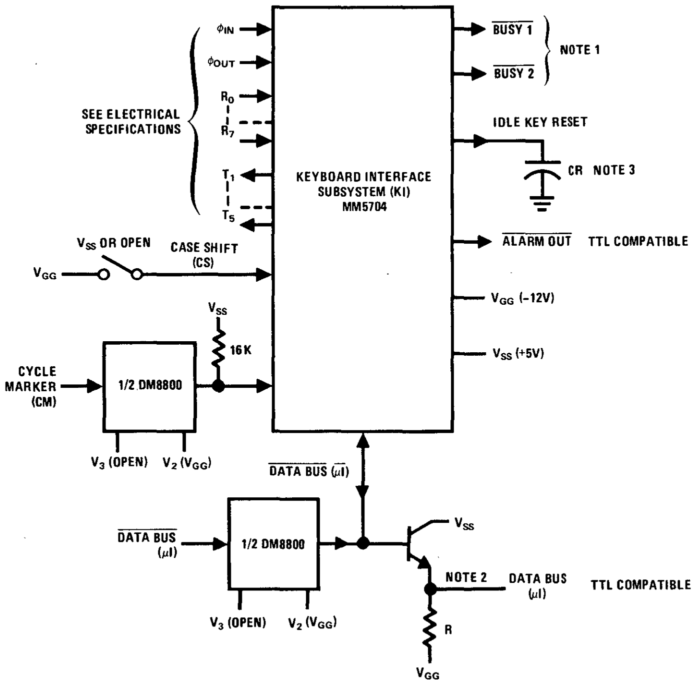
Note 4: Idle Key Reset is programmable by an external capacitor CR. This reset is applied only during the idle mode to enable control logic for first key detection.

Note 5: Shift and static switches can be programmed as normally open or normally closed. (NO) gives logic "1" out on μl bus (NC) gives logic "0" out on μl bus.

Note 6: Static Xmit signal duration is one bit time. This is programmable for each keyboard chip to accrue at a unit bit interval between bit times 5 through 8.

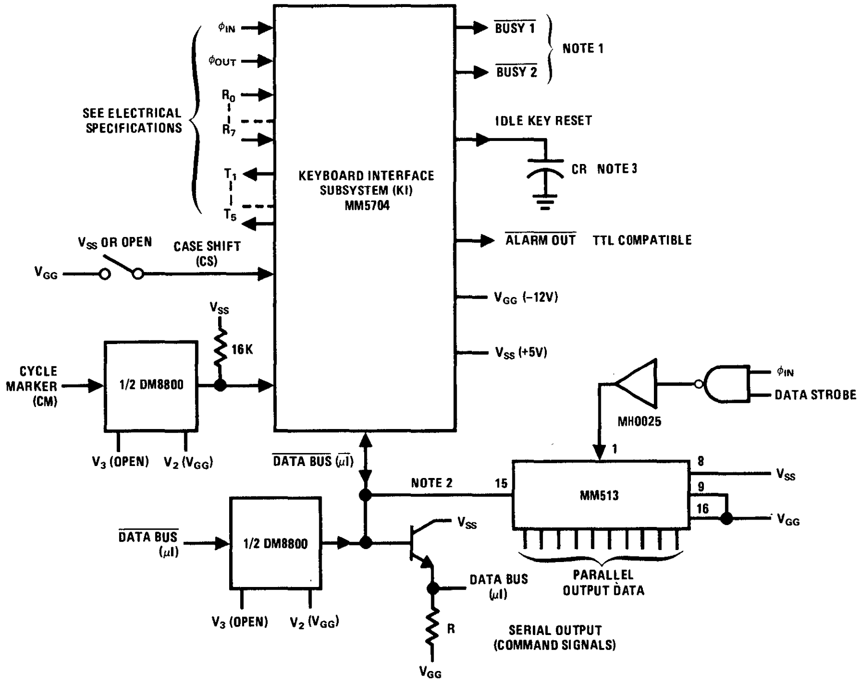
typical applications

TTL/DTL Logic Compatible – Bit Serial Data Output



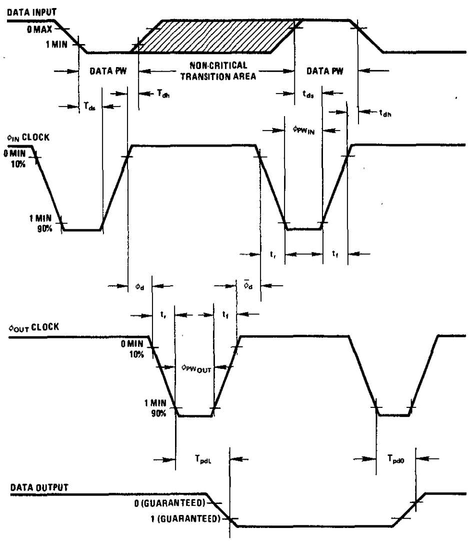
Note 1: With single keyboard interface application, if busy lines are not used in system, leave open. If system will use busy signal, it will require MOS to TTL interface. In multiple (KI) subsystem applications, busy lines are connected busy 1 to busy 1 and busy 2 to busy 2.
Note 2: Data on data bus is in RZ format. Data should be strobed at ϕ_{OUT}.
Note 3: CR value dependent on keyboard scan frequency.

TTL/DTL Compatible – Output Bit Parallel

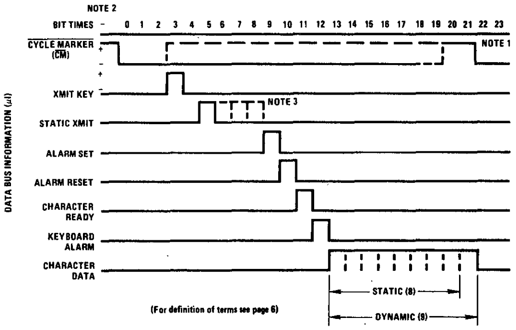


Note 1: With single keyboard interface application, if busy lines are not used in system, leave open. If system will use busy signal, it will require MOS to TTL interface. In multiple (KI) subsystem applications, busy lines are connected busy 1 to busy 1 and busy2 to busy 2.
Note 2: Data on data bus is in RZ format. Data should be strobed at ϕ_{OUT}.
Note 3: CR value dependent on keyboard scan frequency.

timing diagrams



Sequence of Command and Data Transfer



Note 1: Cycle Marker cannot occur sooner than 22 Bit Times.
Note 2: Bit Time = 1/ϕf −Level = V_{SS} − 6V minimum: + Level = V_{SS}.
Note 3: Static Xmit Signal is one Bit Time – Programmed for Bit Time 5 in MM5704-AA.

code pattern

Keyboard Interface ASCII Code Program

Case Shift Control (CS)	No	X	NC		Upper Case Logic Level [✓ +] −		Counter Program	Modulo	Driving Function	Timing	Units
Static Key Form	No	X	NC		Device No.	1 ☒ 2 ☐ 3 ☐ 4 ☐	D Counter	4	CM		
							E Counter	6			

Key Identity	Scan Line		Pin No. 2(+) (Alpha)									Key Identity	Pin No. 2(−) (Numeric)								
	T	R	8	7	6	5	4	3	2	1	0		8	7	6	5	4	3	2	1	0
Q	T1	R0	1	1	1	0	1	0	0	0	1	1	1	1	0	1	1	0	0	0	1
W	T1	R1	1	1	1	0	1	0	1	1	1	7	1	1	0	1	1	0	1	1	1
E	T1	R2	1	1	1	0	0	0	1	0	1	%	1	1	0	1	0	0	1	0	1
R	T1	R3	1	1	1	0	1	0	0	1	0	2	1	1	0	1	1	0	0	1	0
T	T1	R4	1	1	1	0	1	0	1	0	0	4	1	1	0	1	1	0	1	0	0
Y	T1	R5	1	0	1	0	1	1	0	0	1	9	1	0	0	1	1	1	0	0	1
U	T1	R6	1	0	1	0	1	0	1	0	1	5	1	0	0	1	1	0	1	0	1
(5)I	T1	R7	1	1	1	0	0	1	0	0	1	)	1	1	0	1	0	1	0	0	1
A	T2	R0	1	0	1	0	0	0	0	0	1	!	1	0	0	1	0	0	0	0	1
S	T2	R1	1	0	1	0	1	0	0	1	1	3	1	0	0	1	1	0	0	1	1
D	T2	R2	1	0	1	0	0	0	1	0	0	$	1	0	0	1	0	0	1	0	0
F	T2	R3	1	1	1	0	0	0	1	1	0	&	1	1	0	1	0	0	1	1	0
G	T2	R4	1	0	1	0	0	0	1	1	1	'	1	0	0	1	0	0	1	1	1
H	T2	R5	1	0	1	0	0	1	0	0	0	(	1	0	0	1	0	1	0	0	0
J	T2	R6	1	1	1	0	0	1	0	1	0	*	1	1	0	1	0	1	0	1	0
K	T2	R7	1	0	1	0	0	1	0	1	1	+	1	0	0	1	0	1	0	1	1
Z	T3	R0	1	0	1	0	1	1	0	1	0	:	1	0	0	1	1	1	0	1	0
X	T3	R1	1	1	1	0	1	1	0	0	0	8	1	1	0	1	1	1	0	0	0
C	T3	R2	1	1	1	0	0	0	0	1	1	#	1	1	0	1	0	0	0	1	1
V	T3	R3	1	0	1	0	1	0	1	1	0	6	1	0	0	1	1	0	1	1	0
B	T3	R4	1	0	1	0	0	0	0	1	0	"	1	0	0	1	0	0	0	1	0
N	T3	R5	1	0	1	0	0	1	1	1	0	.	1	0	0	1	0	1	1	1	0
M	T3	R6	1	0	1	0	0	1	1	0	1	–	1	0	0	1	0	1	1	0	1
L	T3	R7	1	1	1	0	0	1	1	0	0	,	1	1	0	1	0	1	1	0	0
O	T4	R0	1	1	1	0	0	1	1	1	1	/	1	1	0	1	0	1	1	1	1
P	T4	R1	1	0	1	0	1	0	0	0	0	0	1	0	0	1	1	0	0	0	0
[	T4	R2	1	1	1	0	1	1	0	1	1	;	1	1	0	1	1	1	0	1	1
\	T4	R3	1	0	1	0	1	1	1	0	0	<	1	0	0	1	1	1	1	0	0
]	T4	R4	1	1	1	0	1	1	1	0	1	=	1	1	0	1	1	1	1	0	1
(5)⌒	T4	R5	1	1	1	0	1	1	1	1	0	>	1	1	0	1	1	1	1	1	0
@	T4	R6	1	1	1	0	0	0	0	0	0	SP	1	1	0	1	0	0	0	0	0
(5)–	T4	R7	1	0	1	0	1	1	1	1	1	?	1	0	0	1	1	1	1	1	1

Note 1: A logic "1" or "X" = "most negative voltage".
Note 2: A logic "0" = "most positive voltage".
Note 3: All "Don't Care" cases must be defined as a "1" or "0".
Note 4: If less than 9 bits are used unused bits will be programmed logic "1".
Note 5: These locations are programmed for clearing the keyboard alarm.
Note 6: Bit eight (column 7) is odd parity bit for ASCII code shown.

programming of MM5704

Keyboard Scan Cycle

The matrix scan cycle includes:

1 Counter advancing through each "T" quadrant line T_1 through T_5 each with D counter delay to charge "T" line capacitance.

2 Counter advancing through eight switches in each "T" quadrant except for T_5 static switch quandrant.

3 D counter advances on either system clock ϕ_{IN} or Cycle Marker (programmable feature).

The keyboard scan frequency

$$f_{scan} = Kd + \frac{r}{\phi_f}$$

where

K = 5 (five T quandrants)

d = D counter delay time $= \left(\text{D counter modulus x } \frac{1}{\phi_s}\right)$

r = 33 (Four quandrants times eight switch scans + 1 bit time for T_5 static switch transfer).

ϕ_f = The frequency at which the clock ϕ_{IN} is shifting data through the device.

ϕ_s = ϕ_f when D counter driven by ϕ_f or ϕ_f/x when x is bit times between Cycle Markers.

Key Bounce Delay Time

Since the M counter advances the E counter once each complete keyboard scan the modulo of the E counter determines the key bounce delay

$$E \cdot (Kd + \frac{r}{\phi_f})$$

E = modulus of E counter

The key bounce delay time is the total time elapsed from the first detected key depression until the load flip-flop signals transfer of the character code from ROM to the 9 bit shift register. The E counter controls the number of times the entire keyboard is scanned before a valid key depression is accepted. Variations in timing are obtained from programming of the D counter, E counter, ϕ_f (system operating frequency) and Cycle Marker rep rate provide flexibility for the keyboard interface element to interface with a wide variety of key switch elements.

Idle Key Reset

During an idle key mode (power on) an automatic reset signal is generated by charging an external capacitor C_R which enables the control logic to detect first key depression. This reset prevents keyboard lock-up by mass depression of keys or any attempt to void the integrity of the keyboard encoding. As an example, if a person attempts to hold down three or more keys to force an alarm condition to repeat, in hopes of voiding the keyboard logic, as soon as the keys are released and bounce delay timed out the idle key reset enables the control logic. The value of the reset capacitor is dependent on the keyboard scan cycle. The value of the external capacitor is:

$$C_R = \frac{i_1 \times t_c}{V_1}$$

i_1 = average charging current = 1 mA

V_1 = reset voltage = 3.0V

t_c = charging time interval $t_c = \frac{E + n}{\phi_f}$

E = modulo of E counter

n = number of scan cycles beyond bounce out delay

ϕ_f = frequency of clock ϕ_{IN}

Standard Keyboard Timing

National has programmed a keyboard interface element with the following conditions:

Static Switch Form Normally Open (NO)
Device Number one: static Xmit during bit time 5
Case shift form Normally Open (NO) (alpha characters)
Character Code ASCII (8 bits with 9th bit odd parity)
E counter modulus = 6
D counter modulus = 4
D counter driven by Cycle Marker $\overline{CM}$

Identified as MM5704-AA (see code pattern)

Typical Application

The two main questions in most applications are:

a. How much key matrix capacitance can be charged?
b. What is the key bounce delay time?
c. What is value of idle key reset capacitor?

Using MM5704-AA in system with following characteristics

ϕ_f = 200 kHz $\phi_{OUT(PW)}$ = 0.5 μs

Cycle Marker frequency = $\phi_{f/21}$ (maximum data transfer case)

Key bounce delay

$$E \cdot (Kd + \frac{r}{\phi_f})$$

$$6 \cdot [5(4 \times \frac{1}{\phi_s}) + \frac{33}{\phi_f}]$$

$$6 \cdot [5(4 \times \frac{21}{200 \times 10^3}) + \frac{33}{200 \times 10^3}] =$$

13.5 ms

programming of MM5704 (con't)

D counter is programmed to charge key matrix capacitance

D counter delay

$$d = 4 \times \frac{1}{\phi_s} = 4 \times \frac{21}{200 \times 10^3} = 420\ \mu s$$

There are 84 clock pulses ϕ_{IN} during this 420 μs interval. The output on the "T" lines is charged only during ϕ_{pw}. The total charging time is 42 μs. Using linear approximation

$$C = \frac{Q}{V} = \frac{i \times t}{V}$$

i = average charging current of T lines = 0.5 mA

V = voltage swing 10V across "T" lines for logic "1"

$$C = \frac{0.5 \times 10^{-3} \times 42 \times 10^{-6}}{10} = 2100\ pF$$

Idle Key Reset

Value of C_R is

$$C_R = \frac{i_1 \times t_c}{V_1}$$

$$C_R = \frac{1 \times 10^{-3} \times \frac{6+2}{200 \times 10^3}}{3} = 0.013\ \mu F$$

definition of terms

XMIT Key: Causes KIC to transmit 9 bit dynamic key code at the next data time.

Static XMIT: Transmission on static key information at very next data time. (8 bits)

Alarm Set: Sets KIC alarm.

Alarm Reset: Resets alarm on keyboard.

Character Ready: Indicates that keyboard has 9 bit code stored in shift register and is able to transmit upon command.

Keyboard Alarm: Indication on μI at bit time 12 that alarm is on.

Dynamic Shift Registers

*MM400/MM500 series dynamic shift registers

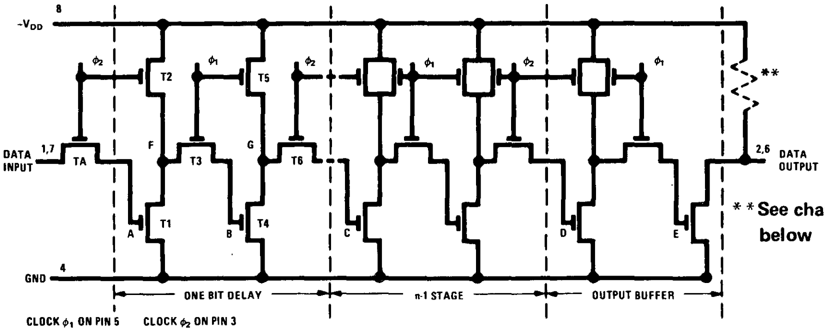
general description

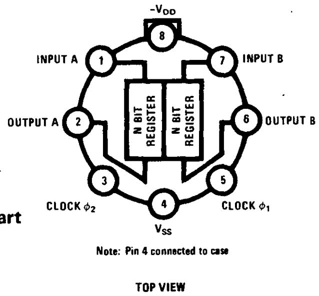
The National Semiconductor line of dynamic shift registers are built on a single silicon chip utilizing MOS P channel enhancement mode transistors. Designed to operate over a wide frequency spectrum, these devices can be used in any sequential digital system that employs a two phase clocking system. The low threshold transistors used permit operation with a V_{DD} supply voltage of –10V and a –16V clock amplitude to obtain these device features:

- Direct DTL or TTL compatibility
- High Frequency Operation — 1 MHz guaranteed
- Low Power Consumption — 0.8 mW/bit @ 1 MHz
- Minimum Operating Frequency Guarantee — 600Hz @ 25°C
- Military and Commercial Temperature Ranges
  - MM400 Series — –55°C to +125°C
  - MM500 Series — –25°C to +70°C
- Low Output Impedance (V_{OH}) — 500 ohms
- Clock inputs directly compatible with MH0009, two phase clock driver

The power dissipation of the device decreases as the operating frequency is decreased; at 10 kHz typical dissipation is 6 μW/bit. The minimum operating frequency is also reduced substantially at lower temperatures; typical minimum frequency of operation at 25°C is 100 Hz.

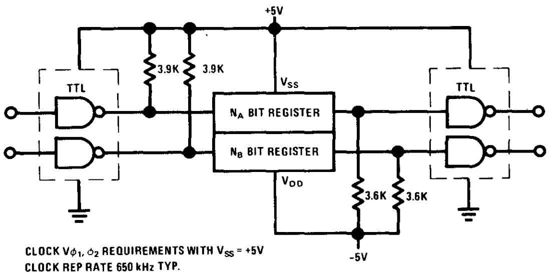
schematic and connection diagrams





typical applications

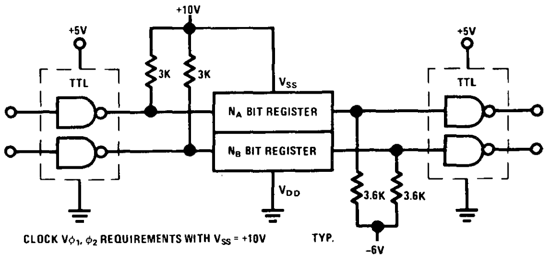
FIGURE 1 – TTL/MOS Interface—Low Frequency
(see clock timing graph for detail)



CLOCK $V\phi_1, \phi_2$ REQUIREMENTS WITH V_{SS} = +5V
CLOCK REP RATE 650 kHz TYP.

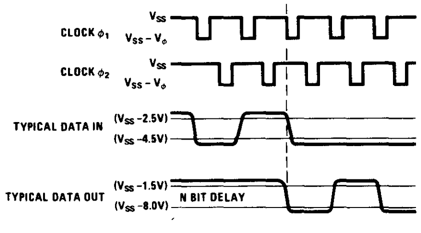
LOGIC "0" (V_{SS})	+4.5V
LOGIC "1" ($V_{SS} - V_{\phi L}$)	–10V

FIGURE 2 – TTL/MOS Interfaces



CLOCK $V\phi_1, \phi_2$ REQUIREMENTS WITH V_{SS} = +10V	TYP.
LOGIC "0" (V_{SS})	+9.5V
LOGIC "1" ($V_{SS} - V_{\phi L}$)	–6.0V

Waveforms for Applications
(complete timing diagrams on page 11)



Standard Register Configurations †

CONFIGURATION	OPEN DRAIN OUTPUT		20 KΩ OUTPUT	
	–55°C to +125°C	–25°C to +70°C	–55°C to +125°C	–25°C to +70°C
Dual 25 bit	MM400	MM500	MM401	MM501
Dual 50 bit	MM402	MM502	MM403	MM503
* Dual 100 bit	MM406	MM506	MM407	MM507

† For other length registers consult your National representative.

* For New Designs, See MM4006A/MM5006A Data Sheet

absolute maximum ratings

Drain Voltage ($-V_{DD}$)	+0.5V to −25V
Clock Inputs ($V\phi_1$, $V\phi_2$)	+0.5V to −25V
Data Inputs	+0.5V to −25V
Power Dissipation (Note 1)	500 mW
Operating Temperature MM400 Series	−55°C to +125°C
MM500 Series	−25°C to + 70°C
Storage Temperature	−65°C to +150°C

electrical drive requirements

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Pulse Width	See Timing Diagram, Page 3				
ϕ_1 Clock pw		0.4		10.0	µs
ϕ_2 Clock pw		0.2		10.0	µs
Clock Delay, ϕ_d	See Definition	0.1			µs
Clock Pulse Transition $t_{r\phi}$, $t_{f\phi}$	1 MHz, ϕ_{pw} = 0.2 µs			0.05	µs
	100 kHz, ϕ_{pw} = 0.2 µs			0.5	µs
	10 kHz, ϕ_{pw} = 10 µs			5.0	µs
Clock Input Level (V_ϕ)					
Logic "0" ($V_{\phi H}$)			V_{SS} −0.5	V_{SS} −1.5	V
Logic "1" ($V_{\phi L}$)		V_{SS} −14.5	V_{SS} −16.0	V_{SS} −18.0	V
Data Pulse Width t_{dw}		0.4			µs
Data Setup Time t_{ds}		0.1			µs
Data Input Voltage Levels					
MOS to MOS					
Logic "0" (V_{IH})	V_{DD} = −10V, V_{SS} = GND			2.0	V
Logic "1" (V_{IL})	freq = 1 MHz max.	−7.0			V
TTL to MOS (Fig. 1)					
Logic "0" (V_{IH})	V_{DD} = GND, V_{SS} = +10V			V_{SS} − 2.0	V
Logic "1" (V_{IL})	freq = 1 MHz max.	V_{SS} −7.0			V
TTL to MOS (Fig. 2)					
Logic "0" (V_{IH})	V_{DD} = −5V, V_{SS} = +5V			V_{SS} − 1.5	V
Logic "1" (V_{IL})	(V_{SS} = 4.75 min)				
	freq = 0.5 MHz max.	V_{SS} −4.2			V

electrical characteristics (Note 2)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Repetition Rate	See Fig. 2	See Note 5		1.0	MHz
	See Fig. 1	See Note 5		0.5	MHz
Clock Input Capacitance	f = 1.0 MHz, 0V Bias				
(Pins 3 & 5)	MM400, 401, 500, 501		22	40	pF
	MM402, 403, 502, 503		40	60	pF
	MM406, 407, 506, 507		85	100	pF
	−20V Bias				
	MM400, 401, 500, 501		18	25	pF
	MM402, 403, 502, 503		32	40	pF
	MM406, 407, 506, 507		55	65	pF
Data Output Voltage Levels					
MOS to MOS	V_{DD} = −10V, V_{SS} = GND				
Logic "0" (V_{OH})	freq = 1 MHz max.			V_{SS} −1.5	V
	Input (d.c.)				
Logic "1" (V_{OL})		V_{SS} −8.0V			V
MOS to TTL (Fig. 1)	V_{DD} = GND, V_{SS} = +10V freq = 1 MHz max. Input (d.c.)				
Logic "0" (V_{OH})	I_L = 2.5 mA } See Note 6	2.5			V
Logic "1" (V_{OL})	I_L = −1.6 mA } See Note 6			0.4	V
MOS to TTL (Fig. 2)	V_{DD} = −5V, V_{SS} = +5V (V_{SS} = 4.75 min) freq = 0.5 MHz max.				
Logic "0" (V_{OH})	I_L = 2.5 mA } See Note 6	2.5			V
Logic "1" (V_{OL})	I_L = −1.6 mA } See Note 6			0.4	V
Breakdown Voltage	1.0 µA Test Current T_A = 25°C				
On Pin 1	GND on Pins 2, 3, 4, 5, 6, 7 −8V on Pin 8	−25			V
On Pin 2 (Note 3)	GND on Pins 1, 4, 6, 7, 8 −8V on Pins 3, 5	−25			V
On Pin 6 (Note 3)	GND on Pins 1, 2, 4, 7, 8 −8V on Pins 3, 5	−25			V
On Pin 7	GND on Pins 1, 2, 3, 4, 5, 6 −8V on Pin 8	−25			V
Leakage Current	T_A = 25°C				
Pin 1	V_1 = −18V, V_8 = −8V All Other Pins at GND			0.5	µA
Pin 2 (Note 4)	V_2 = −18V, V_3 = V_5 = −8V All Other Pins at GND			0.5	µA
Pin 6 (Note 4)	V_6 = −18V, V_3 = V_5 = −8V All Other Pins at GND			0.5	µA
Pin 7	V_7 = −18V, V_8 = −8V All Other Pins at GND			0.5	µA
Pin 8 (Note 4)	V_8 = −8V All Other Pins at GND			0.5	µA
Power Supply Current Drain	Outputs at Logic "1" 1 MHz Operations, T_A = 25°C (ϕ_1 = 0.4 µs, ϕ_2 = 0.2 µs)				
	MM400,401,500,501		4.5	9.0	mA
	MM402,403,502,503		9.0	14.0	(Average)
	MM406,407,506,507		18.0	30.0	

Note 1: For operating at elevated temperatures; the device must be derated based on +150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient. The full rating applies for case temperatures to +125°C for MM400 Series and +70°C for MM500 Series units.

Note 2: These specifications apply over the indicated operating temperature ranges for V_{SS} = 0V and $-11V < V_{DD} < -9.5V$ and 20 kΩ connected between Pins 2 and 8 and between Pins 6 and 8 with output measurement load of less than 10 pF in parallel with 10 MΩ to ground unless otherwise specified. On the 401/501, 403/503, and 407/507 optional versions which include 20 kΩ pull-up resistors internal to package, the external 20 kΩ resistors are not used in measurement circuits.

Note 3: For the odd number devices, MM401, 403 & 407, the output on Pins 2 and 6 will exhibit a resistance when measured with the following bias conditions: Pins: 1, 6 and 8 = GND; Pins 3 and 5 = −16V; Pin: 4 = Open; Measure Pins 2 and 6 = $25k \geq R_{OUT} \geq 15$ kΩ.

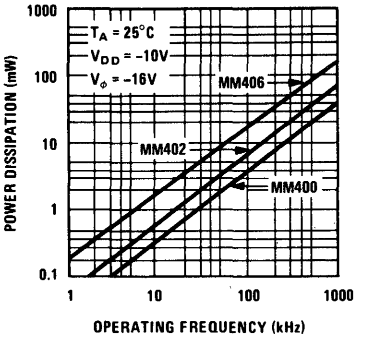
Note 4: Not for internal resistor devices.

Note 5: See minimum operating frequency graph.

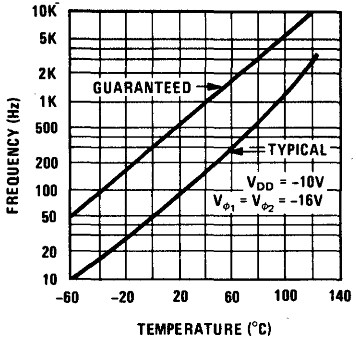
Note 6: In the Logic "0" (V_{OH}) level the MOS register output will be sourcing 2.5 mA into the load Combination of the Pull down resistors and the gate leakage current. In the Logic "1" V_{OL} level I_L represents the current that the pull down resistor and the internal 20K resistor Combination will sink in order to insure Current Sinking Capability for one gate.

performance characteristics

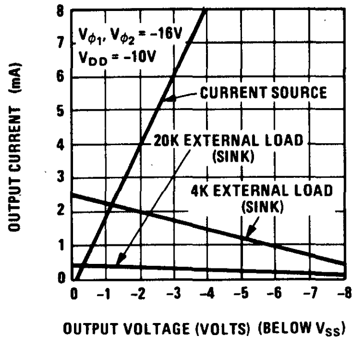
Power Dissipation vs Maximum Frequency



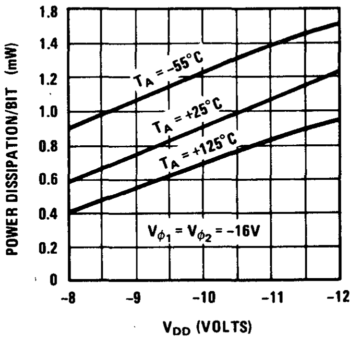
Minimum Operating Frequency



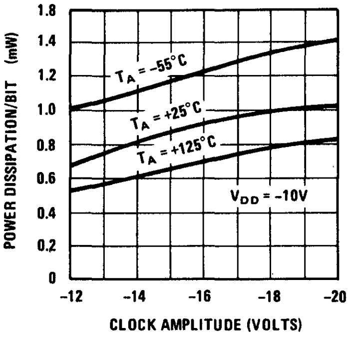
Output Sink/Source Current



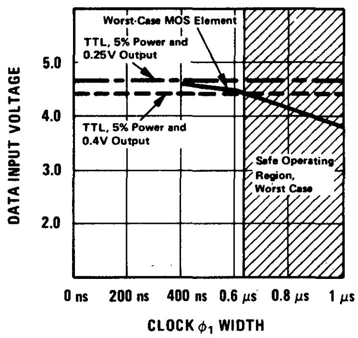
Power Dissipation/Bit vs. Supply Voltage



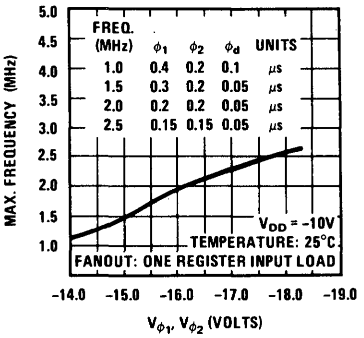
Power Dissipation/Bit vs. Clock Amplitude



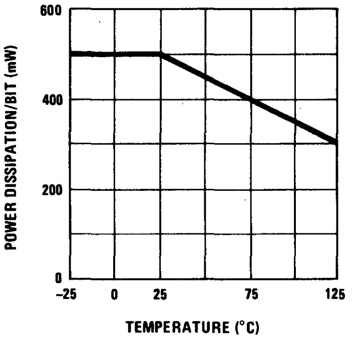
Clock Timing, Direct-Coupled TTL or DTL



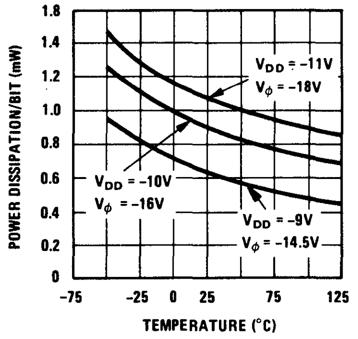
Clock Amplitude V_{ϕ_1}, V_{ϕ_2} vs. Maximum Frequency



Maximum Package Power Dissipation



Power Dissipation/Bit vs. Temperature

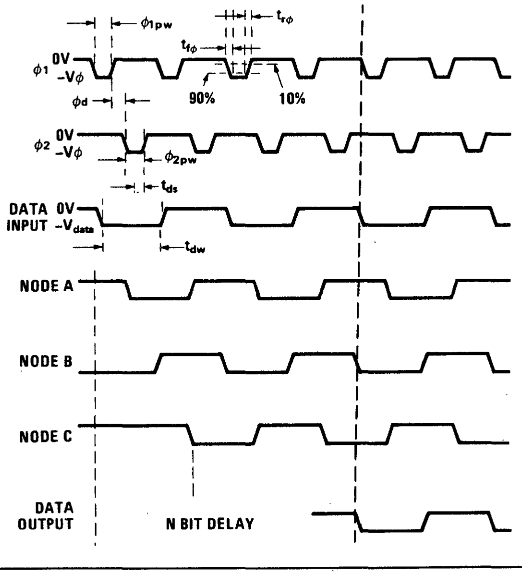


Note: All typical performance data is gathered with $\phi_{pw} = 0.4\ \mu$; $\phi_{2pw} = 0.2\ \mu s$; $\phi_d = 0.1\ \mu s$; f = 1 MHz; except as otherwise noted.

operation

Each bit of delay shown in the circuit schematic consists of two inverters T1 and T4 accompanied by clocked load resistors T2 and T5 and two coupling devices T3 and T6. The circuit functions as follows: When ϕ_2 goes negative (one state) the coupling unit TA and the load resistor T2 are clocked ON allowing information at the input to be transferred to node A turning T1 ON or OFF depending on the state of the input. For example, if a negative potential (near $-V_{DD}$ level) is transferred from the input to the gate to source capacitance at node A, then T1 turns ON allowing node F to be at $\frac{-V_{DD}}{2}$. When ϕ_2 returns to its zero state (ground level) T2 turns OFF allowing node F to discharge to zero volts. When ϕ_1 goes negative (one state) the coupling unit T3 and the load resistor T5 are clocked ON allowing information at node F to be transferred to node B. T4 is held OFF if node F was at ground potential and is turned ON if node F had been at $-V_{DD}$ potential. Continuing the example above, T4 is held OFF and node G is at $-V_{DD}$ since T5 is ON during ϕ_1 clock pulse. When ϕ_1 returns to its zero state, node G maintains a $-V_{DD}$ voltage level. This voltage level is maintained at node G until the ϕ_2 clock appears. The bit delay demonstrated in this example is repeated through each half of the dual register.

timing diagram



Dynamic Shift Registers

MM1402A/MM1403A/MM1404A/MM5024A 1024-bit dynamic shift register

general description

The MM1402A/MM1403A/MM1404A/MM5024A 1024-bit dynamic shift registers are MOS monolithic integrated circuits using silicon gate technology to achieve bipolar compatibility. 5 MHz data rates are achieved by on-chip multiplexing. The clock rate is one-half the data rate; i.e., one data bit is entered for each ϕ_1 and ϕ_2 clock pulse.

All devices in the family can operate from +5V, −5V, or +5V, −9V power supplies.

features

- Guaranteed 5 MHz operation
- Low power dissipation .1 mW/bit at 1 MHz
- DTL/TTL compatible
- Low clock capacitance 125 pF
- Low clock leakage ≤ 1 μA
- Inputs protected against static charge
- Operation from +5V, −5V or +5V, −9V power supplies
- Four standard configurations

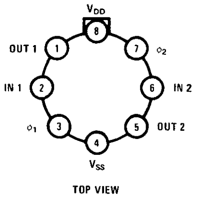
MM1402A	Quad 256-bit
MM1403A	Dual 512-bit
MM1404A	Single 1024-bit
MM5024A	Single 1024-bit with internal 4.7k pull-down resistor

applications

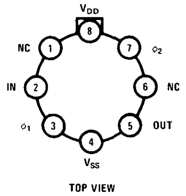
- Radar and sonar processors
- CRT displays
- Terminals
- Desk top calculators
- Disk and drum replacement
- Computer peripherals
- Buffer memory
- Special purpose computers—signal processors, digital filtering and correlators, receivers, spectral compressors and digital differential analyzers
- Telephone equipment
- Medical equipment

connection diagrams

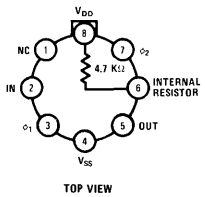
Metal Can Packages



MM1403A

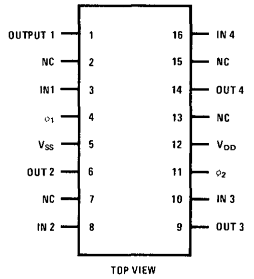


MM1404A



MM5024A

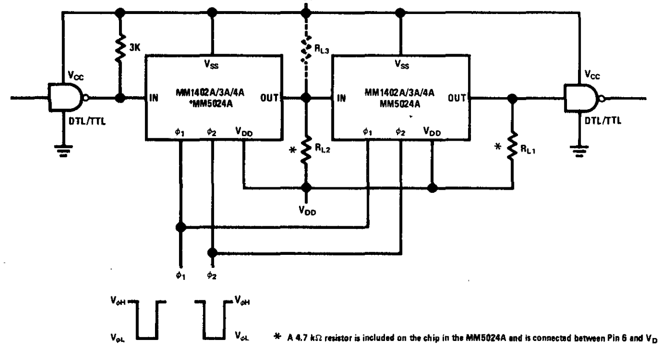
Dual-In-Line Package



MM1402A

typical application

DTL/TTL to MOS Interface



* A 4.7 kΩ resistor is included on the chip in the MM5024A and is connected between Pin 6 and V_{DD}.

R_L Load Resistor Value for Different V_{DD} Supplies

	V_{SS} = 5V V_{DD} = −5V	V_{SS} = 5V V_{DD} = −9V
R_{L1}	3.0k	4.7k
R_{L2}	4.7k	6.2k
R_{L3}	Not required	3.9k

absolute maximum ratings

Data and Clock Input Voltages and Supply Voltages with Respect to V_{SS}	+ 0.3V to -20V
Power Dissipation	600 mW at T_A = 25°C
Operating Temperature Range	-25°C to +70°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A = –25°C to +70°C, V_{SS} = 5V ±5%, V_{DD} = –5V ±5% or –9V ±5%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical LOW Level (V_{IL})		V_{SS} - 10.0		V_{SS} - 4.2	V
Logical HIGH Level (V_{IH})		V_{SS} - 1.7		V_{SS} + 0.3	V
Data Input Leakage Current	V_{IN} = –15V, T_A = 25°C, All Other Pins GND		<10	500	nA
Input Capacitance	V_{IN} = V_{SS}		5	10	pF
Clock Input Levels	V_{DD} = -5V ± 5%				
Logical LOW Level ($V_{\phi L}$)		V_{SS} - 17		V_{SS} - 15	V
Logical HIGH Level ($V_{\phi H}$)		V_{SS} - 1		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)	V_{DD} = -9V ± 5%	V_{SS} - 14.7		V_{SS} - 12.6	V
Logical HIGH Level ($V_{\phi H}$)		V_{SS} - 1		V_{SS} + 0.3	V
Clock Leakage Current	Min $V_{\phi L,}$ T_A = 25°C		10	1000	nA
Clock Capacitance	V_ϕ = V_{SS}		90	125	pF
Data Output Levels					
Logical LOW Level (V_{OL})	R_{L1} = 3k to V_{DD}, I_{OL} = 1.6 mA, V_{DD} = -5V ± 5%		-0.3	0.5	V
Logical HIGH Level (V_{OH})	R_{L1} = 3k to V_{DD}, I_{OH} = 100 μA	2.4	3.5		V
Logical LOW Level (V_{OL})	R_{L1} = 4.7k to V_{DD}, I_{OL} = 1.6 mA, V_{DD} = -9V ± 5%		-0.3	0.5	V
Logical HIGH Level (V_{OH})	R_{L1} = 4.7k to V_{DD}, I_{OH} = 100 μA	2.4	3.5		V
Logical HIGH Level (V_{OH})	R_{L2} = 4.7k to V_{DD}, V_{DD} = -5V ± 5%	V_{SS} - 1.6	V_{SS} - 1		V
Logical HIGH Level (V_{OH})	R_{L2} = 6.2k to V_{DD}, V_{DD} = -9V ± 5%	V_{SS} - 1.6	V_{SS} - 1		V
	R_{L3} = 3.9k to V_{SS}				
Power Supply Current (I_{DD})	T_A = 25°C, V_{DD} = -5V ± 5% Output Logic "0", 5 MHz Data Rate; 33% Duty Cycle, Continuous Operation, $V_{\phi L}$ = V_{SS} – 17V		35	50	mA
	T_A = 0°C			56	mA
	T_A = 25°C, V_{DD} = -9V ± 5% Output at Logic "0", 3 MHz Data Rate, 26% Duty Cycle, Continuous Operation, $V_{\phi L}$ = V_{SS} – 14.7V		30	40	mA
	T_A = 0°C			45	mA
Data Output Leakage Current	V_{OUT} = 0.0V, T_A = 25°C, $V_{\phi 1}$ = $V_{\phi 2}$ = V_{SS} - 10V, All Other Pins +5V		<10	1000	nA
Internal Resistor (MM5024A)	T_A = 25°C	3.7	4.7	5.2	kΩ
Output Capacitance	V_{OUT} = V_{SS}, f = 1 MHz		5	10	pF

ac characteristics T_A = –25°C to +70°C, V_{SS} = 5V ± 5%

PARAMETER	V_{DD} = -5V ± 5%		V_{DD} = -9V ± 5%		UNITS
	MIN	MAX	MIN	MAX	
Clock Frequency (ϕ_f)	Note 1	2.5	Note 1	1.5	MHz
Data Frequency		5.0		3.0	MHz
Clock Pulse Width (ϕ_{PW})	0.130	10	0.170	10	μs
Clock Phase Delay Times (ϕ_d, $\overline{\phi}_d$)	10	Note 1	10	Note 1	ns
Clock Transition Times (ϕt_r, ϕt_f)		1000		1000	ns
Data Input Delay Time (t_{ds})	30		60		ns
Data Input Hold Time (t_{dH})	20		20		ns
Data Output Propagation Delay		90		110	ns

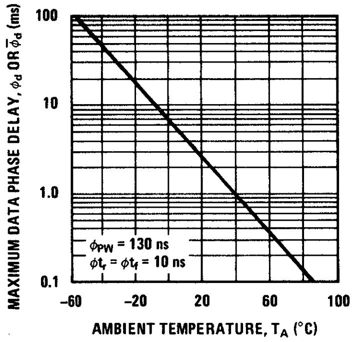
Note 1: Minimum clock frequency is a function of temperature and clock phase delay times, ϕ_d and $\overline{\phi}_d$ as shown by the ϕ_f versus temperature and ϕ_d, $\overline{\phi}_d$ versus temperature curves. The lowest guaranteed clock frequency can be attained by making ϕ_d equal to $\overline{\phi}_d$. The minimum guaranteed clock frequency is:

$\phi_f(\text{min}) \cong \dfrac{1}{\phi_d + \overline{\phi}_d}$ for the condition ($\phi t_r = \phi t_f << \phi_{PW} << \phi_d$ or $\overline{\phi}_d$), where the variables may not exceed the guaranteed maximums.

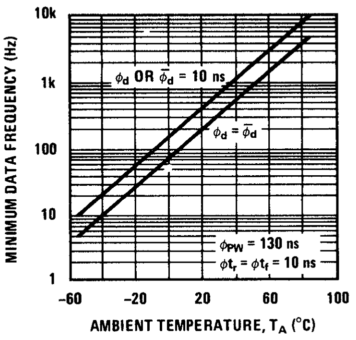
Note 2: Capacitance is guaranteed by periodic testing.

performance characteristics

Guaranteed Maximum Data Phase Delay Times vs Temperature (Note 1)

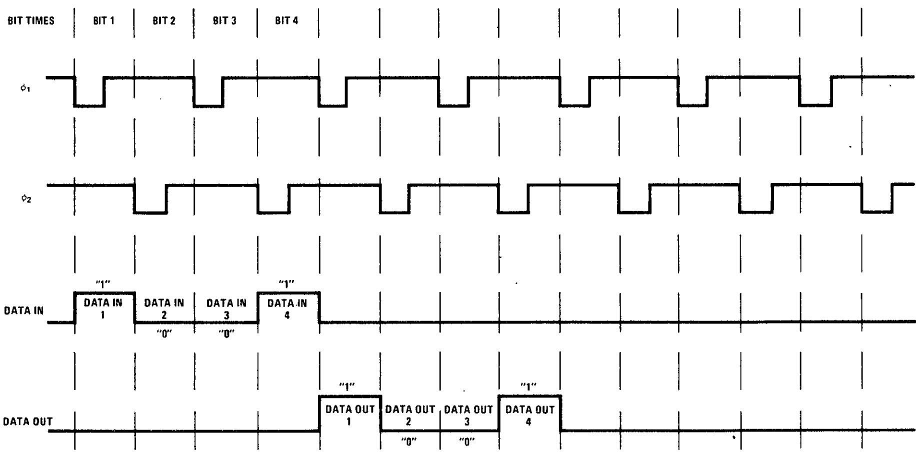


Guaranteed Minimum Data Frequency vs Temperature (Note 1)



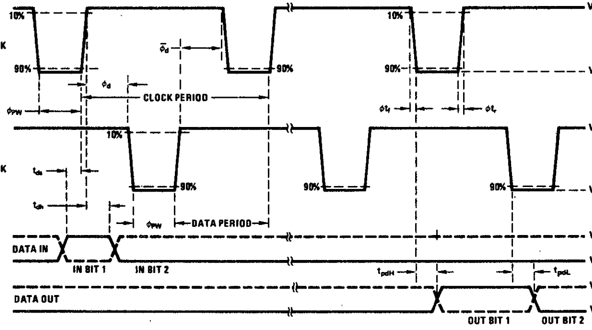
switching time waveforms

Multiplexed 4-Bit MOS Shift Register



Shown is a simplified illustration of the timing of a 4-bit multiplexed register showing input output relationships with respect to the clock. If data enters the register at ϕ_1 time, it exits at ϕ_1 time. (Beginning on $\phi_{1's}$ negative going edge and ending on the succeeding $\phi_{2's}$ negative going edge.)

timing diagram



Dynamic Shift Registers

MM4001A/MM5001A dual 64-bit dynamic shift register
MM4010A/MM5010A dual 64-bit accumulator

general description

The MM4001A/MM5001A dual 64-bit dynamic shift register is a monolithic MOS integrated circuit utilizing P-channel enhancement mode low threshold technology. The device consists of two 64-bit registers with independent two phase clocks and is guaranteed to operate at a 2.5 MHz operating frequency for CRT display applications.

The MM4010A/MM5010A is a dual accumulator function capable of operating at very high frequency. The device is also constructed on a single silicon chip utilizing MOS P-channel enhancement transistors. With the recirculate control line at an MOS logic "0" state, the device functions as an accumulator. A logic "1" state at the recirculate control line allows external information to enter the register serially. It is important to note that recirculation of data is performed internally, independent of the output circuit thus making it insensitive to output loading.

features

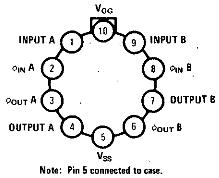
- High frequency operation 3.3 MHz typ
- Low power consumption 0.4 mW/bit at 1 MHz
- DTL/TTL compatibility +5V, −12V power supplies, push-pull output stage
- Minimum operating frequency guaranteed 250 Hz at 25°C
- Application versatility "Split clock" operation, independent control of each register for MM4001A/MM5001A

applications

- Business machine
- CRT refresh memory
- Delay line memory
- Arithmetic operations

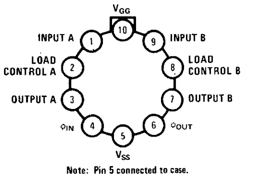
connection diagrams

MM4001A/MM5001A



Note: Pin 5 connected to case.
TOP VIEW

MM4010A/MM5010A



Note: Pin 5 connected to case.
TOP VIEW

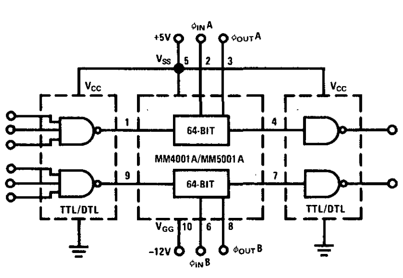
load control truth table

MM4010A/MM5010A

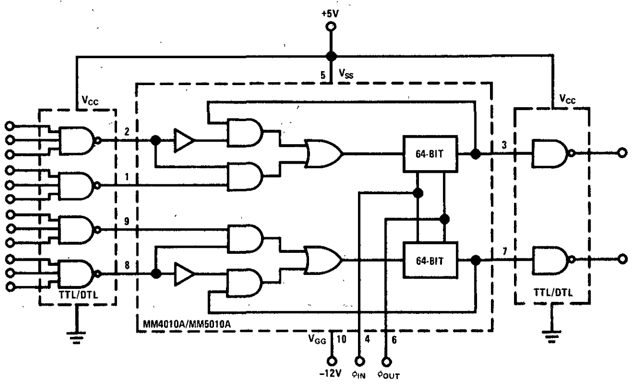
LOGICAL HIGH LEVEL (V_{LCH})	LOGICAL LOW LEVEL (V_{LCL})
Recirculates "old" data	Loads "new" data

typical applications

MM4001A/MM5001A TTL/MOS Interface



MM4010A/MM5010A TTL/MOS Interface



absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} – 22V
Operating Temperature Range	
MM4010A/MM4001A	–55°C to +125°C
MM5010A/MM5001A	–25°C to +70°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = –12.0V ±10%, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} – 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} – 18.5		V_{SS} – 4.2	V
Data Input Leakage	V_{IN} = –20V, T_A = 25°C All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND Note 2		3.0	5.0	pF
Load Control Input Levels					
Logical HIGH Level (V_{LCH})		V_{SS} – 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{LCL})		V_{SS} – 18.5		V_{SS} – 4.2	V
Load Control Input Leakage	V_{IN} = –20V, T_A = 25°C All Other Pins GND		0.01	0.5	μA
Load Control Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND Note 2		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} – 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} – 18.5		V_{SS} – 14.5	V
Clock Input Leakage	V_ϕ = –20V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND				
	MM4001A/MM5001A Note 2		17	20	pF
	MM4010A/MM5010A		34	40	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = –0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = –12V, ϕ_{PW} = 150 ns, V_{SS} = 5.0V, $V_{\phi L}$ = –12V, Data=0-1-0-1				
	0.01 MHz $\leq \phi_f \leq$ 0.1 MHz		2.0	3.0	mA
	ϕ_f = 1 MHz		3.0	4.5	mA
	ϕ_f = 2.5 MHz		5.0	7.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, Note 1	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq$ 10.5 μs	0.15		10	μs
Clock Phase Delay Times ($\phi_d, \overline{\phi}_d$)	Note 1	10			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq$ 10.5 μs			1	μs
Partial Bit Times (T)	Note 1				
Input Partial Bit Time (T_{IN})		0.20		100	μs
Output Partial Bit Time (T_{OUT})		0.20		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Load Control Input Setup Time (t_{LCS})		80	30		ns
Load Control Input Hold Time (t_{LCh})		20	0		ns
Data Output Propagation Delay					
From ϕ_{OUT}	See ac test circuit				
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

Note 1: Minimum clock frequency is a function of temperature and partial bit times, T_{IN} and T_{OUT}, as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

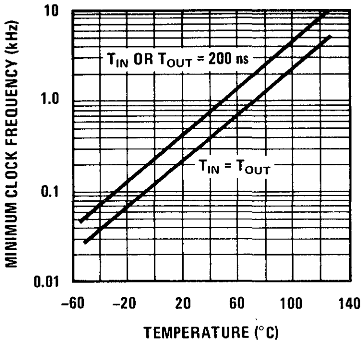
$$\phi_{f(min)} = \frac{1}{T_{IN} + T_{OUT}}$$

where T_{IN} and T_{OUT} may not exceed the guaranteed maximums.

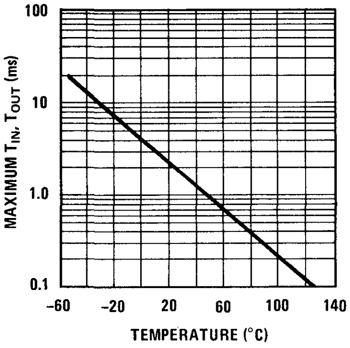
Note 2: Capacitance is guaranteed by lot sample testing.

performance characteristics

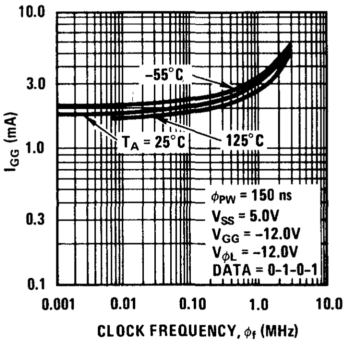
Guaranteed Minimum Clock Frequency vs Temperature (Note 1)



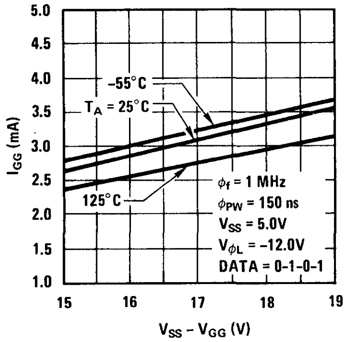
Guaranteed Maximum T_{IN} and T_{OUT} vs Temperature (Note 1)



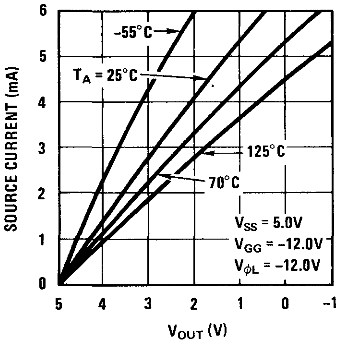
Typical Power Supply Current vs Clock Frequency



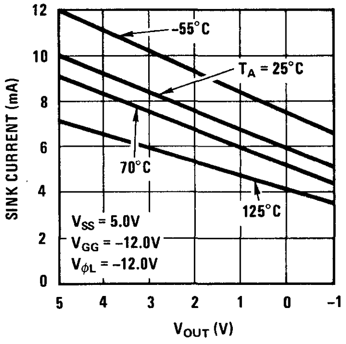
Typical Power Supply Current vs Voltage



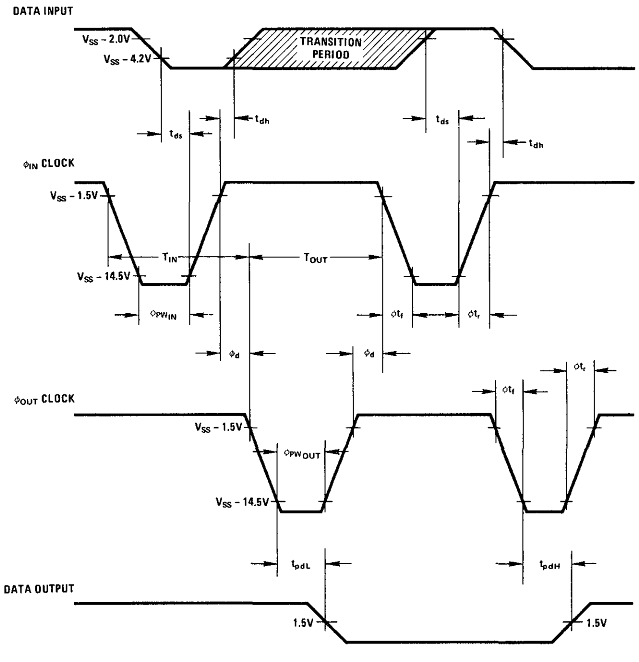
Typical Data Output Source Current vs Data Output Voltage



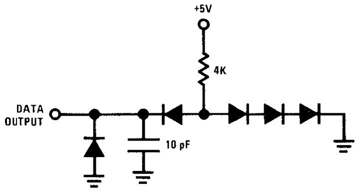
Typical Data Output Sink Current vs Data Output Voltage



switching time waveforms



ac test circuit



Dynamic Shift Registers

MM4007/MM5007 dual 100-bit mask programmable shift register
MM4019/MM5019 dual 256-bit mask programmable shift register
MM4006A/MM5006A dual 100-bit shift register

general description

The MM4007/MM5007 and MM4019/MM5019 are monolithic dual 100-bit and dual 256-bit dynamic shift registers utilizing P-channel enhancement mode technology to achieve bipolar compatibility. The length of the registers may be varied at manufacture by the altering of the metal mask providing custom length of both registers. Additional connection between registers may be accomplished at the metal mask to provide single shift register lengths of up to 200 or 512-bits, with or without an appropriate tap provided at the juncture. The MM5006A is an MM5007 programmed as a dual 100-bit shift register.

For the MM4007/MM5007 N = 20 to 100 bits
For the MM4019/MM5019 N = 40 to 256 bits

STANDARD LENGTHS:

MM4006A	Dual 100-bit
MM4007/AA	Dual 80-bit
MM4019	Dual 256-bit

CUSTOM LENGTHS:

The programmed shift registers are assigned a letter code for each option. These are designated by a pair of letters after the number code but before the package designation such as

MM5007/AA/H

which is a −25°C to +70°C dual 80-bit dynamic shift register in the TO-99 package. Pattern codes are assigned by National upon initial order entry. See MOS Brief 14 for a more detailed description of the custom mask.

features

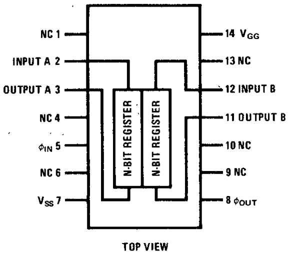
■ Bipolar compatibility	Standard +5V, −12V power supplies
■ Mask programmable length	
MM4007/MM5007	dual 20-100 bits
MM4019/MM5019	dual 40-256 bits
■ Low clock capacitance	
MM4007/MM5007	65 pF max
MM4019/MM5019	125 pF max
■ Standard clock frequency	250 Hz min — typical at 25°C 2.5 MHz max — guaranteed over temp
■ Full temperature range	
MM4007,MM4019	−55°C to +125°C
MM5007,MM5019	−25°C to +70°C

applications

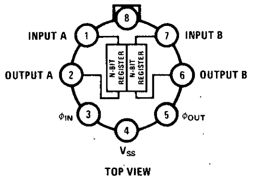
- Custom shift registers
- CRT recirculate display

connection diagrams

Dual-In-Line Package



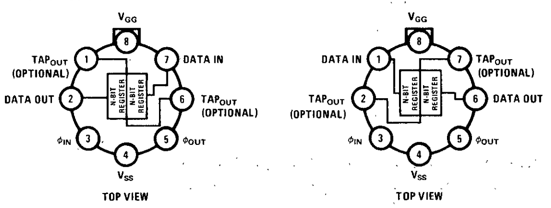
Note: Pin 7 connected to case.



Note: Pin 4 connected to case.

Standard Connection

Metal Can Packages


OPTION A: OUTPUT B CONNECTED TO INPUT A

OPTION B: OUTPUT A CONNECTED TO INPUT B

Note: Pin 4 connected to case.

Note: Pin 4 connected to case.

Optional Connections

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} - 22V
Operating Temperature Range	
MM4006A,MM4007,MM4019	-55°C to +125°C
MM5006A,MM5007,MM5019	-25°C to +70°C
Storage Temperature Range	-65°C to +150°C

electrical characteristics

T_A within operating temperature range, V_{SS} = 5.0V ±5%, V_{GG} = −12.0V ±10%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} - 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} - 18.5		V_{SS} - 4.2	V
Data Input Leakage	V_{IN} = -20V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} - 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} - 18.5		V_{SS} - 14.5	V
Clock Input Leakage	V_{ϕ} = -2.0V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_{ϕ} = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)				
MM4006A/MM5006A & MM4007/MM5007			50	65	pF
MM4019/MM5019			95	125	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = -0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = -12V, ϕ_{PW} = 150 ns V_{SS} = 5.0V, $V_{\phi L}$ = -12V, Data = 0-1-0-1				
MM4006A/MM5006A & MM4007/MM5007	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		2.0	3.0	mA
MM4019/MM5019			2.5	3.5	mA
MM4006A/MM5006A & MM4007/MM5007	ϕ_f = 1.0 MHz		4.0	6.0	mA
MM4019/MM5019			5.0	7.0	mA
MM4006A/MM5006A & MM4007/MM5007	ϕ_f = 2.5 MHz		6.0	9.0	mA
MM4019/MM5019			9.0	12.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns	.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq$ 10.5 μs	0.15		10	μs
Clock Phase Delay Times (ϕ_d, $\bar{\phi}_d$)	(Note 2)	10			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq$ 10.5 μs			1.0	μs
Partial Bit Times (T)	(Note 2)				
Input Partial Bit Time (T_{IN})		0.20		100	μs
Output Partial Bit Time (T_{OUT})		0.20		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay from ϕ_{OUT}	(See ac test circuit)				
Delay to High Level (t_{pdH})			150	200	ns
Delay to Low Level (t_{pdL})			150	200	ns

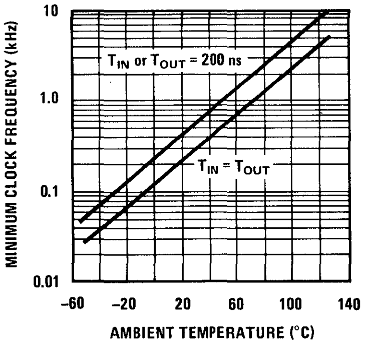
Note 1: Capacitance is guaranteed by periodic testing.

Note 2: Minimum clock frequency is a function of temperature and partial bit times (T_{IN} and T_{OUT}) as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency:

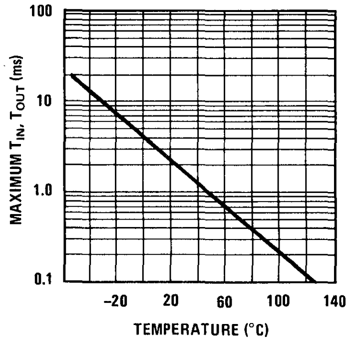
$$\phi_{f(min)} = \frac{1}{T_{IN} + T_{OUT}}$$, where T_{IN} and T_{OUT} do not exceed the guaranteed maximums.

performance characteristics

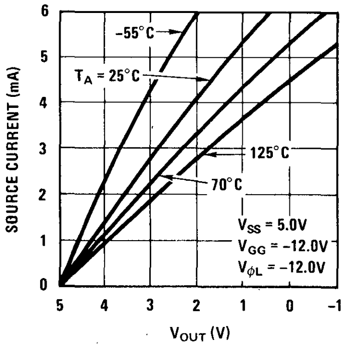
Guaranteed Minimum Clock Frequency vs Temperature (Note 2)



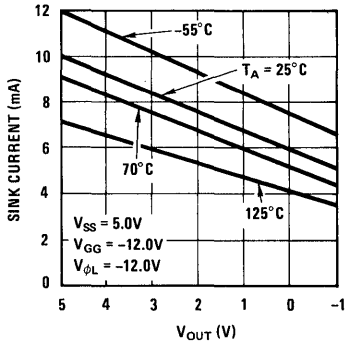
Guaranteed Maximum T_{IN} and T_{OUT} vs Temperature (Note 2)



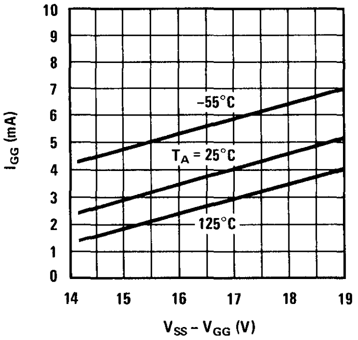
Typical Data Output Source Current vs Voltage



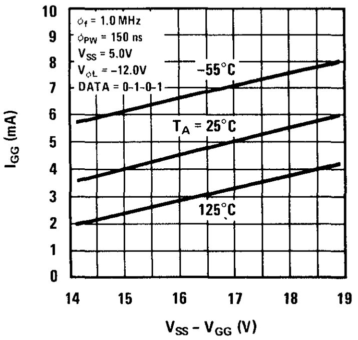
Typical Data Output Sink Current vs Voltage



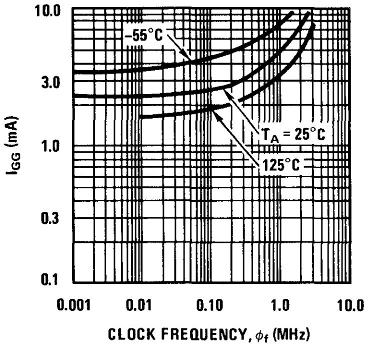
Typical Power Supply Current vs Voltage MM4006A/MM5006A MM4007/MM5007



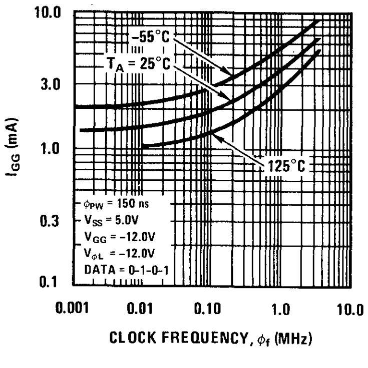
Typical Power Supply Current vs Voltage MM4019/MM5019



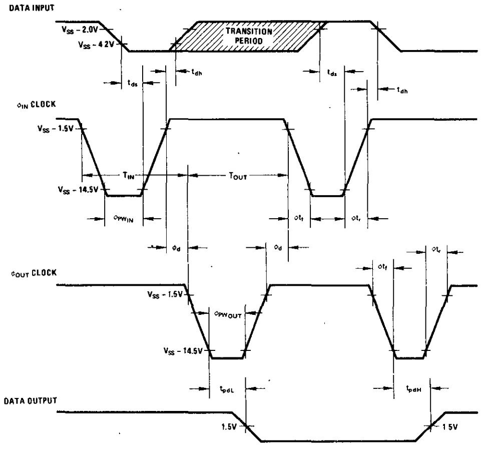
Typical Power Supply Current vs Clock Frequency MM4019/MM5019



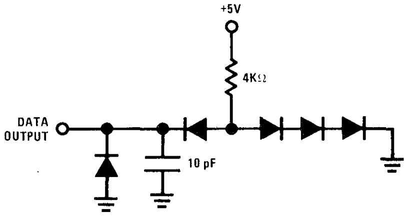
Typical Power Supply Current vs Clock Frequency MM4006A/MM5006A/MM4007/MM5007



switching waveforms



ac test circuit



Dynamic Shift Registers

MM4012/MM5012 dual 256-bit dynamic shift register

general description

The MM4012/MM5012 dual 256-bit dynamic shift register is a monolithic MOS integrated circuit using P-channel enhancement mode technology to achieve bipolar compatibility. The device provides full read/write control, recirculate logic and an independent wire-OR-able TRI-STATE™ output which allows a common output bus-line to be connected between several registers.

The input logic allows recirculating both registers or recirculating either register while loading the other from the data bus input, which along with the TRI-STATE bus output, is enabled by a 2-input NOR gate which allows multiple address decoding. N-bits may be added to the recirculate loop by connecting additional shift registers between outputs A or B and data inputs A or B.

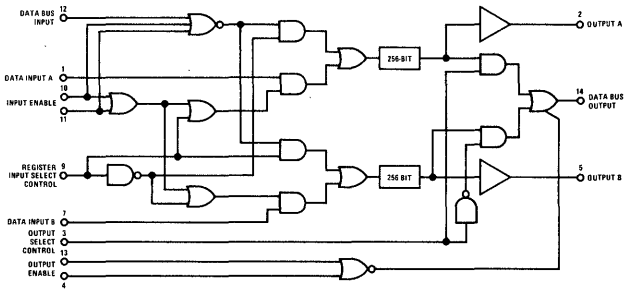
features

■ Bipolar compatibility	+5V, −12V operation No pull-up or pull-down resistors required
■ Wide frequency range	f_{min} = 400 Hz at 25°C f_{max} = 2.5 MHz over temperature guaranteed
■ TRI-STATE output	Common bus systems may be built using wire-OR output
■ System flexibility	Chip contains all recirculate logic, control logic and shift register for disc and drum replacement memories

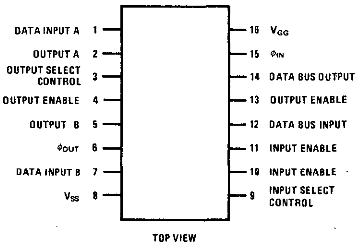
applications

- Disc and drum memory replacement
- CRT refresh memory
- Serial and parallel data storage

logic and connection diagrams

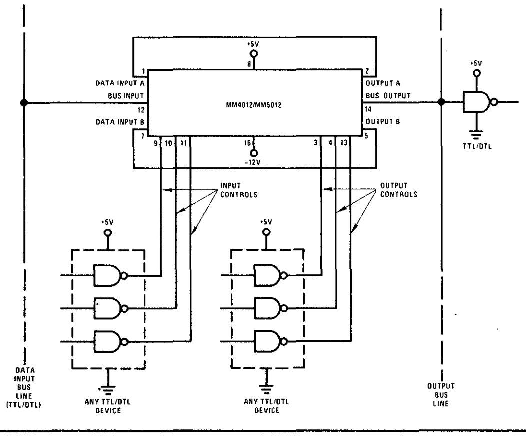


Dual-In-Line Package



typical application

TTL/MOS Interface



absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3 to V_{SS} – 22
Operating Temperature MM4012	–55°C to +125°C
MM5012	–25°C to +70°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = –12.0V ±10%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} – 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})				V_{SS} – 4.2	V
Data Input Leakage	V_{IN} = –20.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND Note 2			5.0	pF
Control Input Levels					
Logical HIGH Level (V_{CH})		V_{SS} – 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{CL})				V_{SS} – 4.2	V
Control Input Leakage	V_{IN} = –20.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Control Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND Note 2		7.0	10.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} – 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} – 18.5		V_{SS} – 14.5	V
Clock Input Leakage	V_ϕ = –20V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND Note 2		110	125	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = –0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Data Bus Output Leakage	$V_{SS} - 5V \leq$ Bus $V_{OUT} \leq V_{SS}$ Bus Output Disabled, T_A = 25°C			10	μA
Power Supply Current					
I_{GG}	T_A = +25°C, V_{GG} = –12V, ϕ_{PW} = 150 ns, V_{SS} = +5.0V, $V_{\phi L}$ = –12V, Data = 0-1-0-1				
	0.01 MHz $\leq \phi_f \leq$ 0.1 MHz		4.0	5.0	mA
	ϕ_f = 1.0 MHz		7.5	9.5	mA
	ϕ_f = 2.5 MHz		13.0	16.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, Note 1	0.01		2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_r = \phi t_f$ = 20 ns	150		10.0	μs
Clock Phase Delay Times (ϕ_d, $\overline{\phi}_d$)		10.0			ns
Clock Transition Times (ϕt_r, ϕt_f)				1.0	μs
Partial Bit Times (T)	Note 1				
Input Partial Bit Time (T_{IN})		0.2		100	μs
Output Partial Bit Time (T_{OUT})		0.2		100	μs
Data Input Setup Time (t_{ds})	Note 4	80	30		ns
Data Input Hold Time (t_{dh})	Note 4	20	0		ns
Output Controls Setup Time (t_{OCS})	Note 3 and 4	50	20		ns
Output Controls Hold Time (t_{OCH})	Note 3 and 4	20	0		ns
Data Output Propagation Delay from ϕ_{OUT}					
Delay to HIGH Level (t_{pdH})			180	250	ns
Delay to LOW Level (t_{pdL})			180	250	ns
Bus Output Propagation Delay from ϕ_{OUT}					
Delay to HIGH Impedance State from LOW Level (t_{0H})			150	200	ns
from HIGH Level (t_{1H})			150	200	ns
Delay to HIGH Level (t_{pdH})			180	250	ns
Delay to LOW Level (t_{pdL})			180	250	ns

Note 1: Minimum clock frequency is a function of temperature and partial bit times, T_{IN} and T_{OUT}, as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guranteed clock frequency is:

$$\phi_f(\text{min}) = \frac{1}{T_{IN} + T_{OUT}},$$ where T_{IN} and T_{OUT} may not exceed the guaranteed maximums.

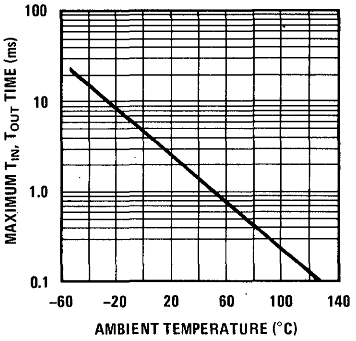
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: The output controls are sampled by ϕ_{IN}. The TRI-STATE output must be enabled or disabled during the ϕ_{IN} clock time prior to the ϕ_{OUT} clock time at which the output is expected to be true or in the high impedance state. See timing diagram. Two bus-connected devices may be in opposite low impedance states simultaneously without damaging either.

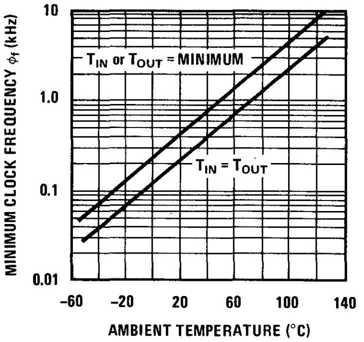
Note 4: Data Input and Input Control Setup and Hold Times are referenced to the trailing edge of ϕ_{IN}, whereas the Output Control Timing is referenced to the leading edge of ϕ_{IN}. See timing diagram.

performance characteristics

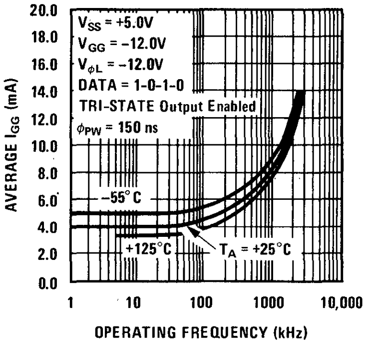
Guaranteed Maximum Partial Bit Times vs Temperature (Note 1)



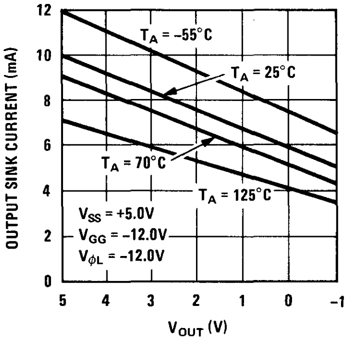
Guaranteed Minimum Clock Frequency vs Temperature (Note 1)



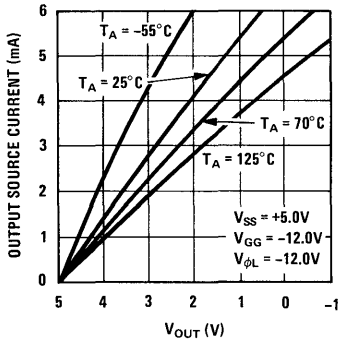
Typical Power Supply Current vs Clock Frequency



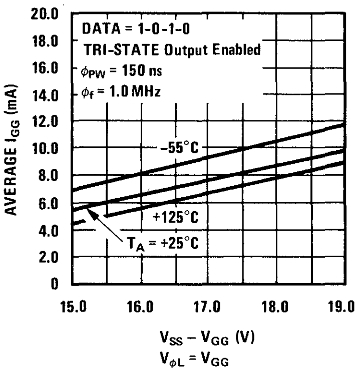
Typical Data Output Sink Current vs Voltage



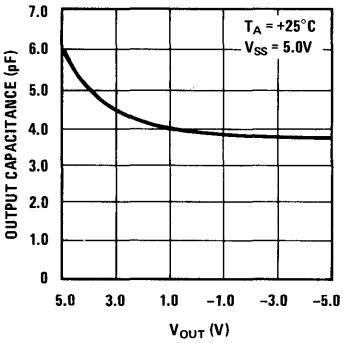
Typical Data Output Source Current vs Voltage



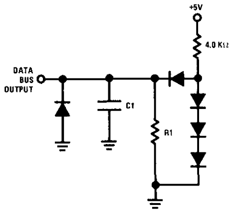
Typical Power Supply Current vs Voltage



Typical Bus Output Capacitance vs Voltage



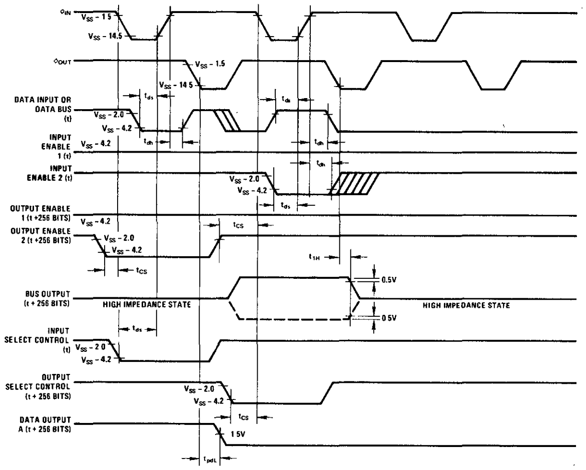
ac test circuit



DELAY	R1	C1
t_{pdL}	35k	20 pF
t_{pdH}	35k	20 pF
t_{0H}*	2.5k	5.0 pF
t_{1H}*	2.5k	5.0 pF

*t_{0H} and t_{1H} only tested on TRI-STATE bus output.

timing diagram



logic table (Notes 3, 4)

MODE	REGISTER SELECT CONTROL	ENABLE CONTROLS		FUNCTION
	PIN 9	PIN 10	PIN 11	
INPUT SELECTION	1	1	1	A Register to A input, B Register to B input
	0	1	1	A Register to A input, B Register to B input
	1	0	1	A Register to A input, B Register to B input
	0	0	1	A Register to A input, B Register to B input
	1	1	0	A Register to A input, B Register to B input
	0	1	0	A Register to A input, B Register to B input
	1	0	0	B Register to Data Bus input, A Register to A input
	0	0	0	A Register to Data Bus input, B Register to B input
	PIN 3	PIN 4	PIN 13	
OUTPUT SELECTION	1	1	1	TRI-STATE™ output in high impedance state
	0	1	1	TRI-STATE output in high impedance state
	1	0	1	TRI-STATE output in high impedance state
	0	0	1	TRI-STATE output in high impedance state
	1	1	0	TRI-STATE output in high impedance state
	0	1	0	TRI-STATE output in high impedance state
	1	0	0	TRI-STATE output connected to A Register
	0	0	0	TRI-STATE output connected to B Register

Note 3: The output controls are sampled by ϕ_{IN}. The TRI-STATE output must be enabled or disabled during the ϕ_{IN} clock time prior to the ϕ_{OUT} clock time at which the output is expected to be true or in the high impedance state. See timing diagram. Two bus-connected devices may be in opposite low impedance states simultaneously without damaging either.

Note 4: Data Input and Input Control Setup and Hold Times are referenced to the trailing edge of ϕ_{IN}, whereas the Output Control Timing is referenced to the leading edge of ϕ_{IN}. See timing diagram.

Dynamic Shift Registers

MM4013/MM5013 1024-bit dynamic shift register/accumulator

general description

The MM4013/MM5013 1024-bit dynamic shift register/accumulator is an MOS monolithic integrated circuit using P-channel enhancement mode low threshold technology to achieve direct bipolar compatibility. There is on-chip logic to load and recirculate data, and a read control for enabling the bus-ORable TRI-STATE™ push pull output stage.

features

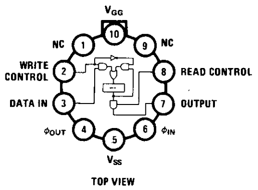
■ Bipolar compatibility	Standard +5V, −12V power supplies No pull down or pull up resistors required
■ Package option	TO-99 or molded 8-pin mini-DIP
■ Low clock capacitance	160 pF max
■ Wide frequency range	ϕ_f min = 400 Hz @ 25°C typ ϕ_f max = 2.5 MHz over temp. guaranteed
■ Built-in recirculate	Exclusive-OR and recirculate loop on-chip
■ TRI-STATE output	Allows wire-OR bus structure on output
■ Full temperature operation	
MM4013	−55°C to +125°C
MM5013	−25°C to +70°C

applications

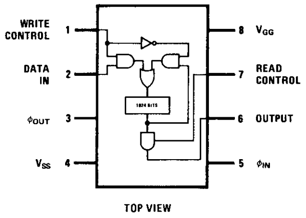
- "Silicon Store" replacement for drum and disc memories
- File memories
- CRT refresh

connection diagrams

TO-100 Package

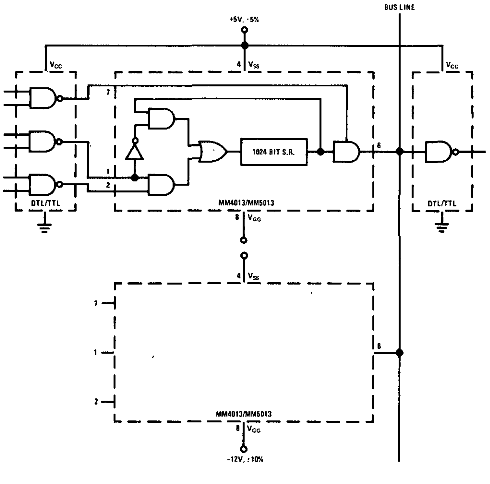


Dual-In-Line Package



typical applications

TTL/MOS Interface



truth table

(Positive Logic)
Logic "1" = V_{IH} = Logical HIGH Level
Logic "0" = V_{IL} = Logical LOW Level

WRITE	READ	FUNCTION
0	0	Recirculate Output Disabled
0	1	Recirculate Output Enabled
1	0	Write Mode Output Disabled
1	1	Write Mode Output Enabled

absolute maximum ratings

Voltage at Any Pin		$V_{SS} + 0.3$ to $V_{SS} - 22$
Operating Temperature Range	MM4013	−55°C to +125°C
	MM5013	−25°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

T_A within operating temperature range, $V_{SS} = +5.0V \pm 5\%$, $V_{GG} = -12.0V \pm 10\%$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		$V_{SS} - 2.0$		$V_{SS} + 0.3$	V
Logical LOW Level (V_{IL})		$V_{SS} - 18.5$		$V_{SS} - 4.2$	V
Data Input Leakage	$V_{IN} = -20.0V$, $T_A = 25°C$, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	$V_{IN} = 0.0V$, f = 1 MHz, All Other Pins GND (Note 1)		3.0	5.0	pF
Control Input Levels					
Logical HIGH Level (V_H)		$V_{SS} - 2.0$		$V_{SS} + 0.3$	V
Logical LOW Level (V_L)		$V_{SS} - 18.5$		$V_{SS} - 4.2$	V
Control Input Leakage	$V_{IN} = -20.0V$, $T_A = 25°C$, All Other Pins GND		0.01	0.5	μA
Control Input Capacitance	$V_{IN} = 0.0V$, f = 1 MHz, All Other Pins GND (Note 1)		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		$V_{SS} - 1.5$		$V_{SS} + 0.3$	V
Logical LOW Level ($V_{\phi L}$)		$V_{SS} - 18.5$		$V_{SS} - 14.5$	V
Clock Input Leakage	$V_\phi = -20.0V$, $T_A = 25°C$, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	$V_\phi = 0.0V$, f = 1 MHz All Other Pins GND (Note 1)		140	160	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	$I_{SOURCE} = -0.5$ mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	$I_{SINK} = 1.6$ mA			0.4	V
Data Output Leakage	$V_{OUT} = -5.0V$, $T_A = 25°C$ Output in High Impedance State			10.0	μA
Power Supply Current I_{GG}	$T_A = 25°C$, $V_{GG} = -12V$, $\phi_{PW} = 150$ ns, $V_{SS} = 5.0V$, $V_{\phi L} = -12V$, Data = 0-1-0-1				
	$0.01\ MHz \leq \phi_f \leq 0.1\ MHz$		1.60	3.0	mA
	$\phi_f = 1.0$ MHz		5.3	8.0	mA
	$\phi_f = 2.5$ MHz		10.3	15.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f = 20$ ns, (Note 2)	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$	0.15		10	μs
Clock Phase Delay Times (ϕ_d, $\overline{\phi}_d$)	(Note 2)	10.0			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			1.0	μs
Partial Bit Times (T)	(Note 2)				
Input Partial Bit Time (T_{IN})		0.2		100	μs
Output Partial Bit Time (T_{OUT})		0.2		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Write Setup Time (t_{ds})		80	30		ns
Write Hold Time (t_{dh})		20	0		ns
Read Setup Time (t_{RS})		0			ns
Read Hold Time (t_{Rh})		0			ns
Data Output Propagation Delay from ϕ_{OUT}	(see ac test circuit)				
Delay to HIGH Level (t_{pd1})			150	200	ns
Delay to LOW Level (t_{pd0})			150	200	ns
Propagation Delay From Read Control Disable to HIGH Impedance State:					
Delay From HIGH Level (t_{1H})			150	200	ns
Delay From LOW Level (t_{0H})			150	200	ns
Propagation Delay From Read Control Enable to LOW Impedance State:					
Delay to HIGH Level (t_{H1})			150	200	ns
Delay to LOW Level (t_{H0})			150	200	ns

Note 1: Capacitance is guaranteed by periodic testing.

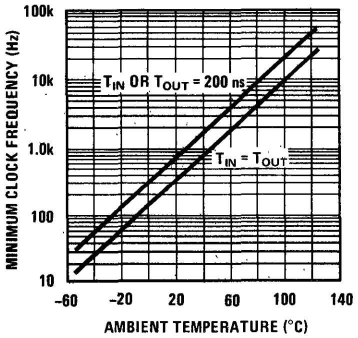
Note 2: Minimum clock frequency is a function of temperature and partial bit times (T_{IN} and T_{OUT}) as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency:

$$\phi_{f(min)} = \frac{1}{T_{IN} + T_{OUT}}$$ where T_{IN} and T_{OUT} do not exceed the guaranteed maximums.

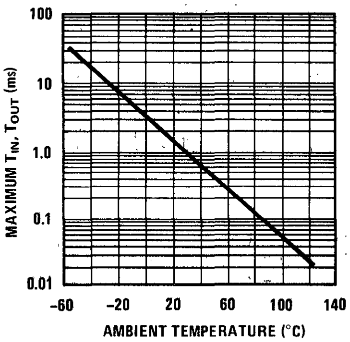
Note 3: Minimum clock frequency and partial bit time curves are guaranteed by testing at a high temperature point.

performance characteristics

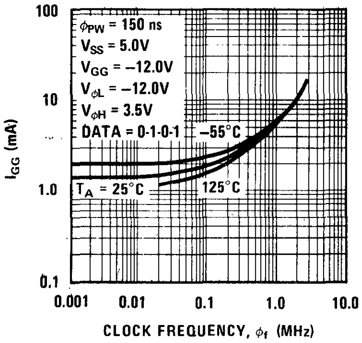
Guaranteed Minimum Clock Frequency vs Temperature (Note 2)



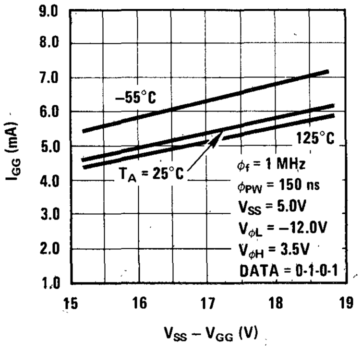
Guaranteed Maximum T_{IN} and T_{OUT} vs Temperature (Note 2)



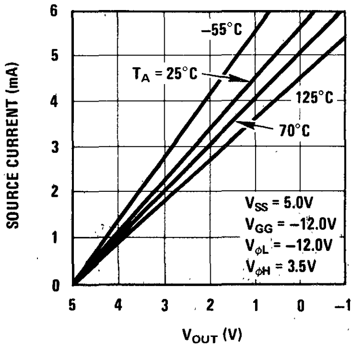
Typical Power Supply Current vs Clock Frequency



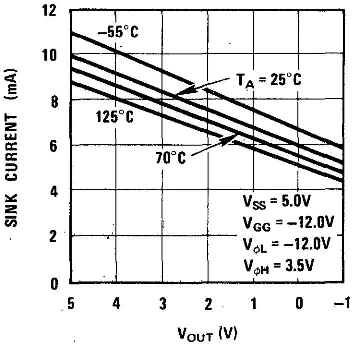
Typical Power Supply Current vs Voltage



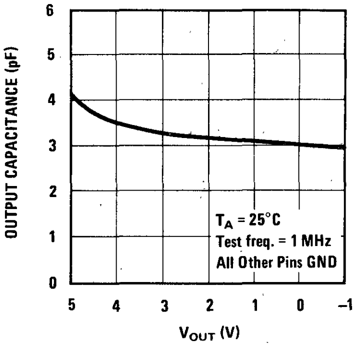
Typical Data Output Source Current vs Data Output Voltage



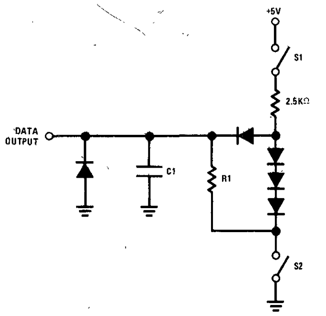
Typical Data Output Sink Current vs Data Output Voltage



Typical Tri-State Data Output Capacitance vs Voltage



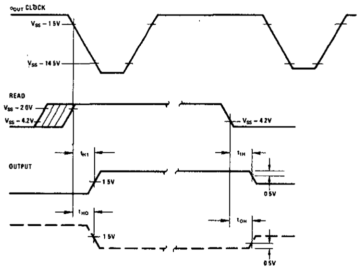
ac test circuit



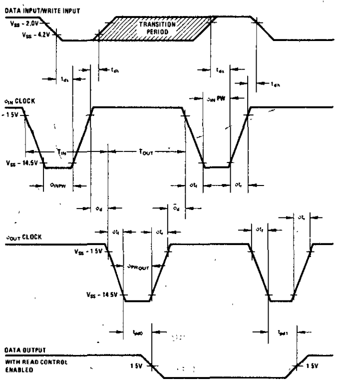
truth table

DELAY	S1	S2	R1	C1
t_{pd0}	Closed	Closed	35K	20 pF
t_{pd1}	Closed	Closed	35K	20 pF
t_{0H}	Closed	Closed	2 5K	5 pF
t_{1H}	Closed	Closed	2 5K	5 pF
t_{H0}	Closed	Open	35K	20 pF
t_{H1}	Open	Closed	35K	20 pF

switching time waveforms



The level of the output when it is in the high impedance state is determined by the external circuitry. The correct data will always appear, after some propagation delay, when the read control is enabled. The guaranteed delay from the high impedance state to the low impedance state requires that the read control is enabled on or before the leading edge of ϕ_{OUT}.



Dynamic Shift Registers

MM4015A/MM5015A triple 60+4 bit accumulator/register

general description

The MM4015A/MM5015A triple 60+4 bit dynamic accumulator is a monolithic MOS integrated circuit utilizing P-channel enhancement mode low threshold technology. The device consists of three independent shift registers with logic to control the entry of external data or to recirculate the data stored in that register. A common two phase clock is required to operate the device.

features

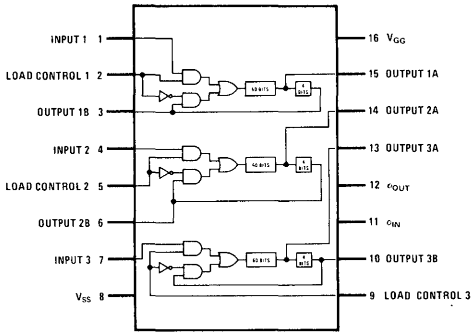
- Direct DTL and TTL compatibility No pull-up or pull-down resistors required
- High frequency operation 2.5 MHz guaranteed
- Low frequency operation 250 Hz at 25°C guaranteed
- Low power consumption 0.4 mW/bit typically at 1 MHz
- Recirculate logic on-chip
- BCD correction look ahead tap

applications

- Data storage registers in BCD arithmetic applications
- Basic accumulator functions
- Business machine memory applications
- Recirculating delay line

connection diagram

Dual-In-Line Package

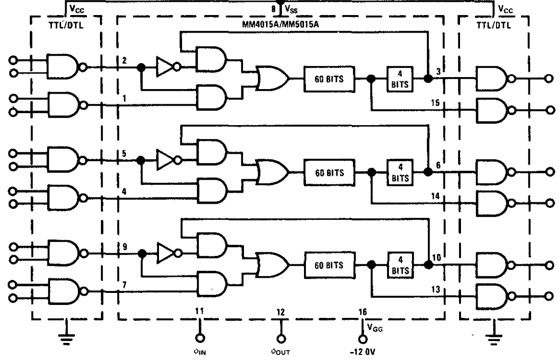


Note Pin 8 connected to case.

TOP VIEW

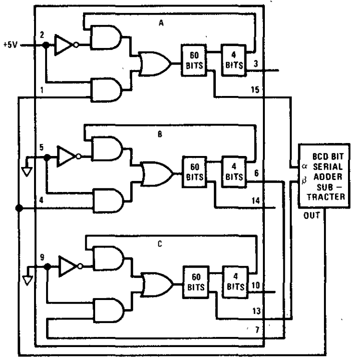
typical applications

TTL/MOS Interface



Load Control } Logical Low – Data is Loaded
} Logical High – Data is Recirculated

Typical Arithmetic Configuration



THE ABOVE CIRCUIT WILL GENERATE THE FUNCTION: A + C → B
B → C
A → A

absolute maximum ratings

Voltage at Any Pin		V_{SS} + 0.3V to V_{SS} – 22.0V
Operating Temperature Range	MM4015A	-55°C to +125°C
	MM5015A	-25°C to +70°C
Storage Temperature Range		-65°C to +150°C

electrical characteristics

T_A within operating temperature range, V_{SS} = 5.0V ±5%, V_{GG} = –12.0V ±10%, unless otherwise stated

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} – 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} – 18.5		V_{SS} – 4.2	V
Data Input Leakage	V_{IN} = –20.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	µA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND See Note 2		3.0	5.0	pF
Load Control Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} – 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} – 18.5		V_{SS} – 4.2	V
Load Control Input Leakage	V_{IN} = –20.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	µA
Load Control Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND See Note 2		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level($V_{\phi H}$)		V_{SS} – 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} – 18.5		V_{SS} – 14.5	V
Clock Input Leakage	$V\phi$ = –20V, T_A = 25°C, All Other Pins GND		0.05	1.0	µA
Clock Input Capacitance	$V\phi$ = 0.0V, f = 1 MHz, All Other Pins GND See Note 2		45.0	60.0	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = –0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = –12V, ϕ_{PW} = 150 ns, V_{SS} = +5.0V, $V_{\phi L}$ = –12V, Data = 0-1-0-1				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		2.2	3.0	mA
	ϕ_f = 1 MHz		4.5	5.5	mA
	ϕ_f = 2.5 MHz		7.0	8.5	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, Note 1	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$	0.15		10.0	µs
Clock Phase Delay Times (ϕ_d, $\overline{\phi}_d$)	Note 1	10			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			1.0	µs
Partial Bit Times (T)	Note 1				
Input Partial Bit Time (T_{IN})		0.20		100	µs
Output Partial Bit Time (T_{OUT})		0.20		100	µs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Load Input Setup Time (t_{ls})		80	30		ns
Load Input Hold Time (t_{lh})		20	0		ns
Data Output Propagation Delay From ϕ_{OUT}					
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

Note 1: Minimum clock frequency is a function of temperature and partial bit times, T_{IN} and T_{OUT}, as shown by the ϕf versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

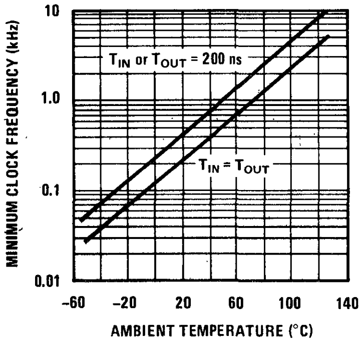
$$\phi f(\min) = \frac{1}{T_{IN} + T_{OUT}}$$

where T_{IN} and T_{OUT} may not exceed the guaranteed maximums.

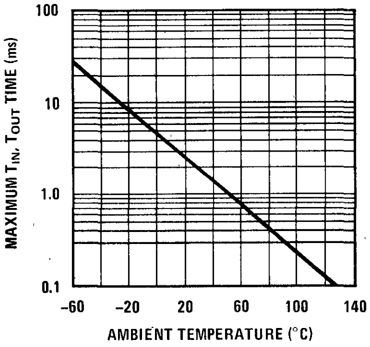
Note 2: Capacitance is guaranteed by periodic testing.

performance characteristics

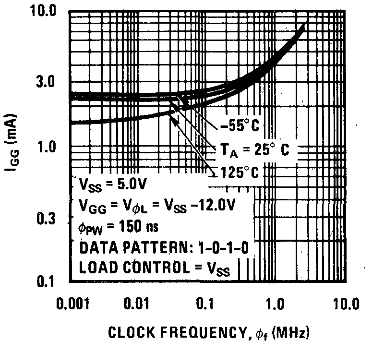
Guaranteed Minimum Clock Frequency vs Temperature (Note 1)



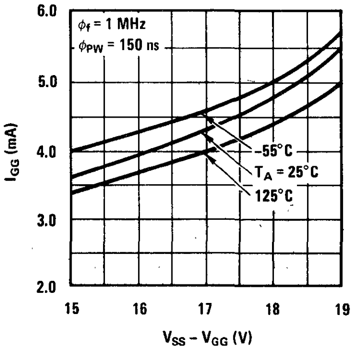
Guaranteed Maximum Partial Bit Times vs Temperature (Note 1)



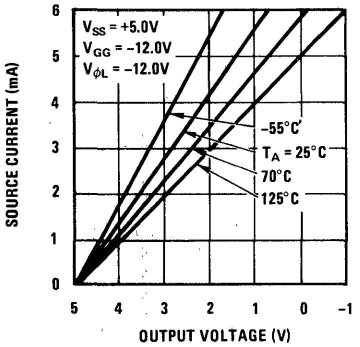
Power Supply Current vs Clock Frequency



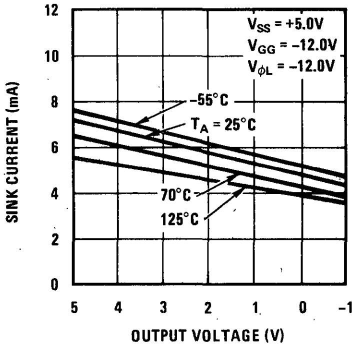
Power Supply Current vs Voltage



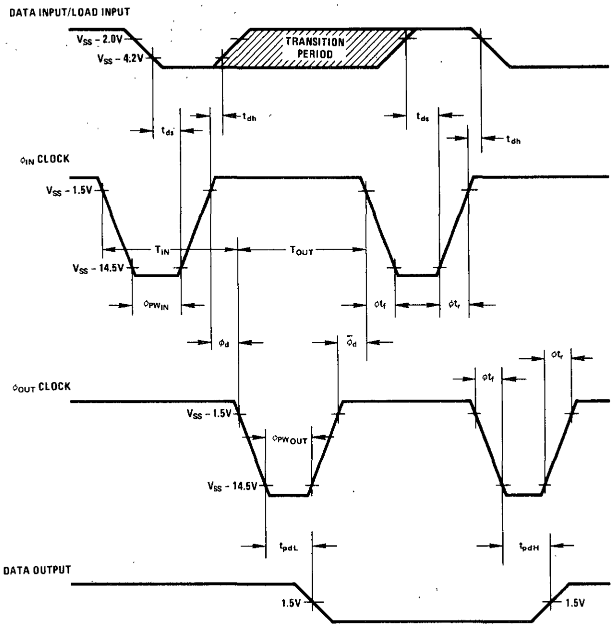
Data Output Source Current vs Voltage



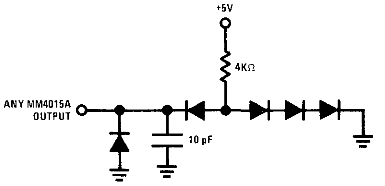
Data Output Sink Current vs Voltage



switching time waveforms



ac test circuit



Dynamic Shift Registers

MM4016/MM5016 512-bit dynamic shift register

general description

The MM4016/MM5016 512-bit dynamic shift register is a monolithic MOS integrated circuit utilizing P channel enhancement mode low threshold technology to achieve bipolar compatibility. An input tap provides the option of using the device as either a 500 or 512-bit register.

features

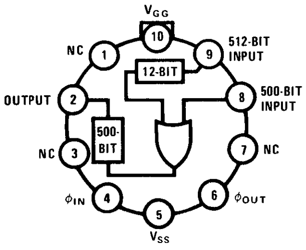
- Bipolar compatibility — +5V, −12V operation. No pull-up or pull-down resistors required.
- Package option — TO-100 or choice of two Dual-In-Line Packages
- Fewer clock drivers required — Clock line capacitance of 100 pF typ
- System flexibility — 300 Hz guaranteed min. operating frequency at 25°C. 500 or 512-bit register length.
- Military and Commercial Temperature Ranges
  - MM4016 −55°C to +125°C
  - MM5016 −25°C to +70°C
- Low power dissipation — < 0.17 mW/bit at 1 MHz max. < 30 μW/bit at 100 kHz typ.

applications

- Glass and magnetostrictive delay line replacement.
- CRT refresh memory.
- Radar delay line.
- Drum memory storage (silicon store)
- Long serial memory.

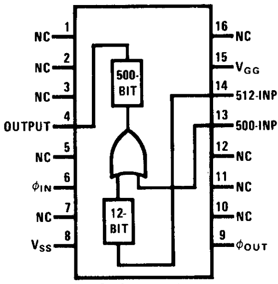
connection diagrams

Metal Can Package



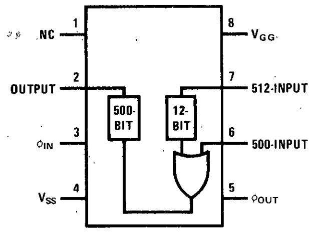
Note: Pin 5 connected to case.
TOP VIEW

Dual-In-Line Package



Note: Pin 8 connected to case.
TOP VIEW

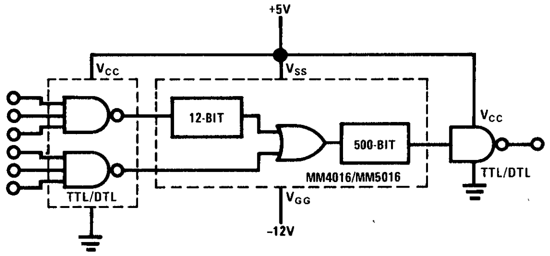
Dual-In-Line Package



TOP VIEW

typical application

TTL/MOS Interface



Note: The unused input pin must be connected to V_{SS}.

absolute maximum ratings

Voltage at Any Pin		V_{SS} + 0.3V to V_{SS} −22V
Operating Temperature Range	MM4016	−55°C to +125°C
	MM5016	−25°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = −12.0V ±10%, unless otherwise specified.

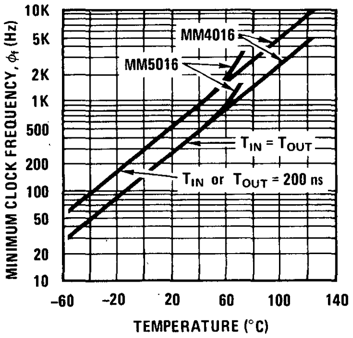
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = − 20V, T_A = 25°C, All Other Pins GND		0.01	0.5	µA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND, (Note 2)		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_ϕ = −20V, T_A = 25°C, All Other Pins GND		0.05	1.0	µA
Clock Input Capacitance	V_ϕ = 0.0V, f = 1 MHz, All Other Pins GND, (Note 2)		100	120	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 150 ns, V_{SS} = 5.0V, $V_{\phi L}$ = −12V, Data = 0-1-0-1				
	0.01 MHz $\leq \phi_f \leq$ 0.1 MHz		1.0	2.0	mA
	ϕ_f = 1 MHz		3.5	5.0	mA
	ϕ_f = 2.5 MHz		7.0	10.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, (Note 1)	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f = \phi_{PW} + \phi t_r \leq$ 10.5 µs	0.15		10	µs
Clock Phase Delay Times (ϕ_d, $\bar{\phi}_d$)	(Note 1)	10			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq$ 10.5 µs			1	µs
Partial Bit Times (T)	(Note 1)				
Input Partial Bit Time (T_{IN})		0.20		100	µs
Output Partial Bit Time (T_{OUT})		0.20		100	µs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay from ϕ_{OUT}	See ac test circuit.				
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

Note 1: Minimum clock frequency is a function of temperature and partial bit times, T_{IN} and T_{OUT}, as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is: $\phi_f(\text{min}) = \frac{1}{T_{IN} + T_{OUT}}$, where T_{IN} and T_{OUT} may not exceed the guaranteed maximums.

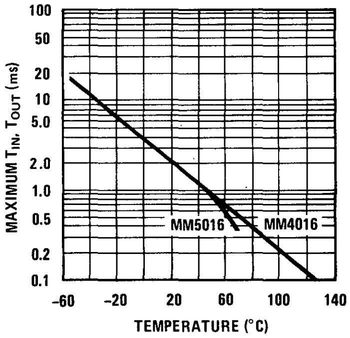
Note 2: Capacitance is guaranteed by statistical lot sample testing.

performance characteristics

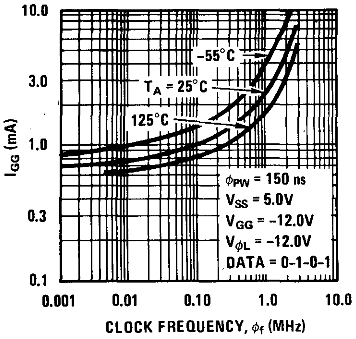
Guaranteed Minimum Clock Frequency vs Temperature (Note 1)



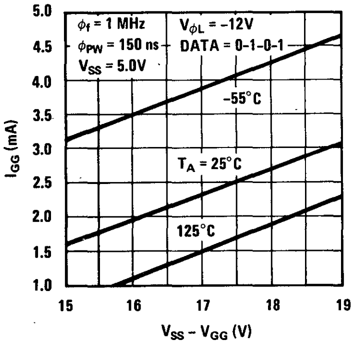
Guaranteed Maximum T_{IN} and T_{OUT} vs Temperature (Note 1)



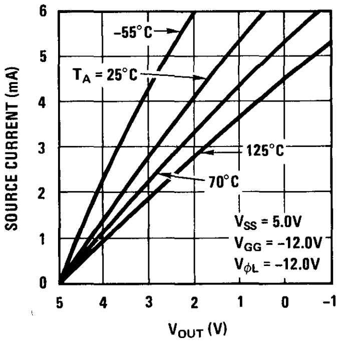
Typical Power Supply Current vs Clock Frequency



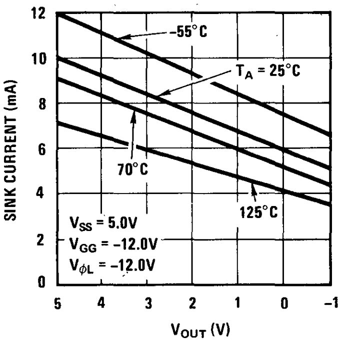
Typical Power Supply Current vs Voltage



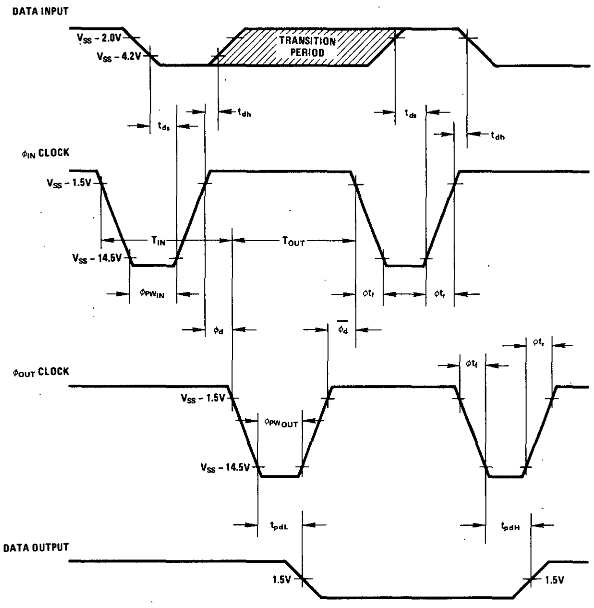
Typical Data Output Source Current vs Voltage



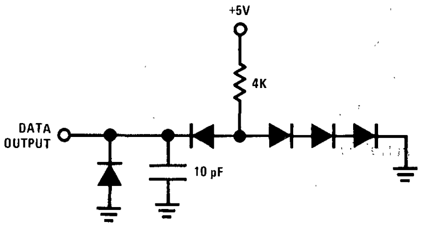
Typical Data Output Sink Current vs Voltage



switching time waveforms



ac test circuit



Dynamic Shift Registers

MM4017/MM5017 dual 512-bit dynamic shift register

general description

The MM4017/MM5017 dual 512-bit dynamic shift register is a monolithic MOS integrated circuit utilizing P channel enhancement mode low threshold technology to achieve bipolar compatibility. An input tap provides the option of using either register in a 500-bit or 512-bit configuration.

features

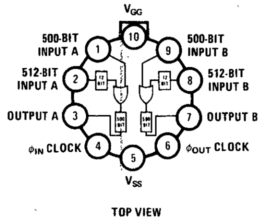
- Standard +5V, −12V supplies Bipolar compatibility. No pull-up or pull-down resistors required.
- Package option TO-100 or Dual-In-Line Package.
- Fewer clock drivers required Clock line capacitance of 140 pF typ.
- System flexibility 400 Hz guaranteed min. operating frequency at 25°C. 500 or 512-bit register length.
- Military and Commercial Temperature Ranges
  - MM4017 −55°C to +125°C
  - MM5017 −25°C to +70°C
- Low power dissipation <0.17 mW/bit at 1 MHz max. < 30 μW/bit at 100 kHz typ.

applications

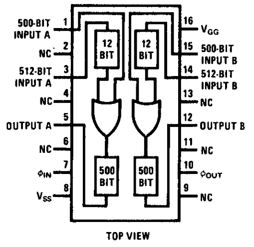
- Glass and magnetostrictive delay line replacement
- CRT refresh memory
- Radar delay line
- Drum memory storage (silicon store)
- Long serial memory

connection diagrams

Metal Can Package

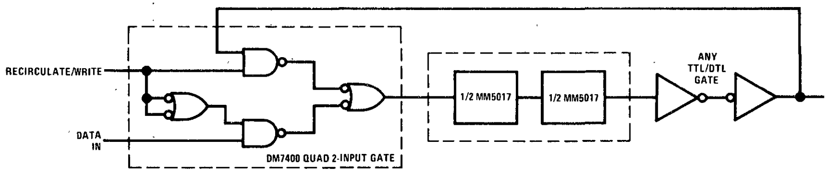


Dual-In-Line Package

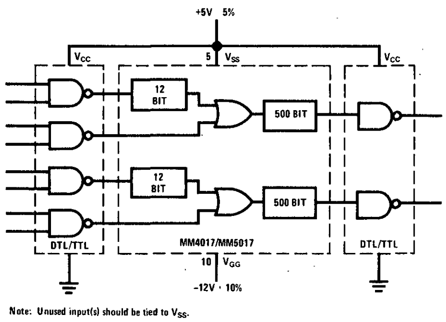


typical applications

1000 or 1024 Bit Accumulator



TTL/MOS Interface



Note: Unused input(s) should be tied to V_{SS}.

absolute maximum ratings

Voltage at Any Pin		$V_{SS} + 0.3$ to $V_{SS} - 22$
Operating Temperature	MM4017	-55°C to +125°C
	MM5017	-25°C to +70°C
Storage Temperature		-65°C to 150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = −12.0V ±10%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		$V_{SS} - 2.0$		$V_{SS} + 0.3$	V
Logical LOW Level (V_{IL})		$V_{SS} - 18.5$		$V_{SS} - 4.2$	V
Data Input Leakage	$V_{IN} = -20V$, $T_A = 25°C$, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	$V_{IN} = 0V$, f = 1 MHz, All Other Pins GND		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		$V_{SS} - 1.5$		$V_{SS} + 0.3$	V
Logical LOW Level ($V_{\phi L}$)		$V_{SS} - 18.5$		$V_{SS} - 14.5$	V
Clock Input Leakage	$V_{\phi} = -20V$, $T_A = 25°C$, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	$V_{\phi} = 0V$, f = 1 MHz, All Other Pins GND		140	160	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	$I_{SOURCE} = -0.5$ mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	$I_{SINK} = 1.6$ mA			0.4	V
Power Supply Current					
I_{GG}	$T_A = 25°C$, $V_{GG} = -12V$, $\phi_{PW} = 150$ ns $V_{SS} = 5.0V$, $V_{\phi L} = -12V$, Data = 0-1-0-1				
	$0.01\text{ MHz} \leq \phi_f \leq 0.1\text{ MHz}$		2.1	3.2	mA
	$\phi_f = 1$ MHz		7.0	10.5	mA
	$\phi_f = 2.5$ MHz		10.0	14.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f = 20$ ns, Note 1	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\,\mu s$	0.15		10	μs
Clock Phase Delay Times (ϕ_d, $\overline{\phi}_d$)	Note 1	10			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\,\mu s$			1.0	μs
Partial Bit Times (T)					
Input Partial Bit Time (T_{IN})		0.20		Note 1	μs
Output Partial Bit Time (T_{OUT})		0.20		Note 1	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay from ϕ_{OUT}	See ac test circuit				
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

Note 1: Minimum clock frequency is a function of temperature and partial bit time, T_{IN} and T_{OUT}, as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

$$\phi f(\text{min}) = \frac{1}{T_{IN} + T_{OUT}}$$

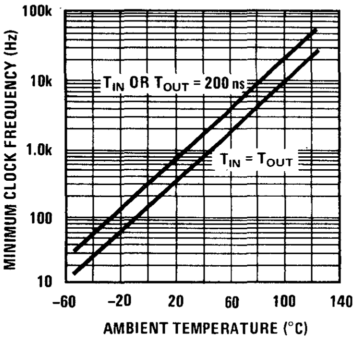
where T_{IN} and T_{OUT} may not exceed the guaranteed maximums.

Note 2: The curves are guaranteed by testing at a high temperature point.

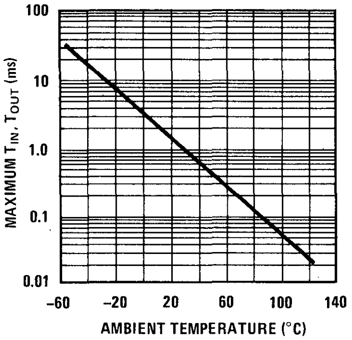
Note 3: Capacitance is guaranteed by periodic testing.

performance characteristics

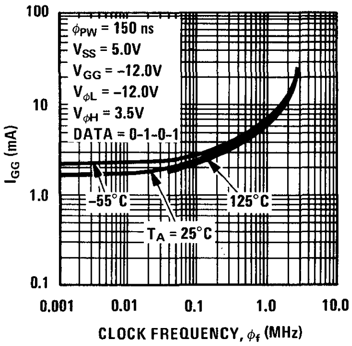
Guaranteed Minimum Clock Frequency vs Temperature (Notes 1 and 2)



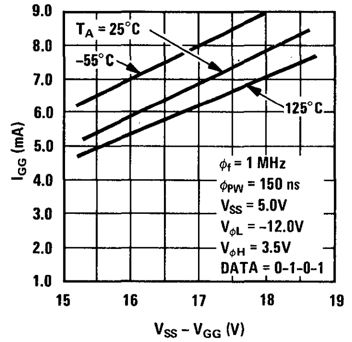
Guaranteed Maximum T_{IN} and T_{OUT} (Notes 1 and 2)



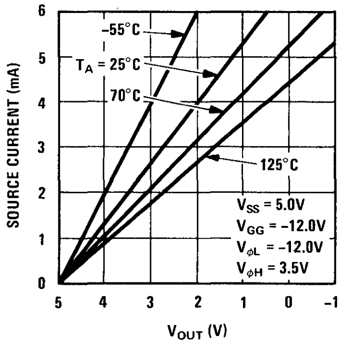
Typical Power Supply Current vs Clock Frequency



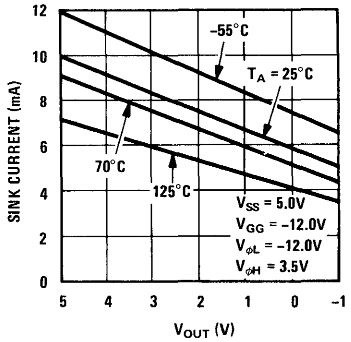
Typical Power Supply Current vs Voltage



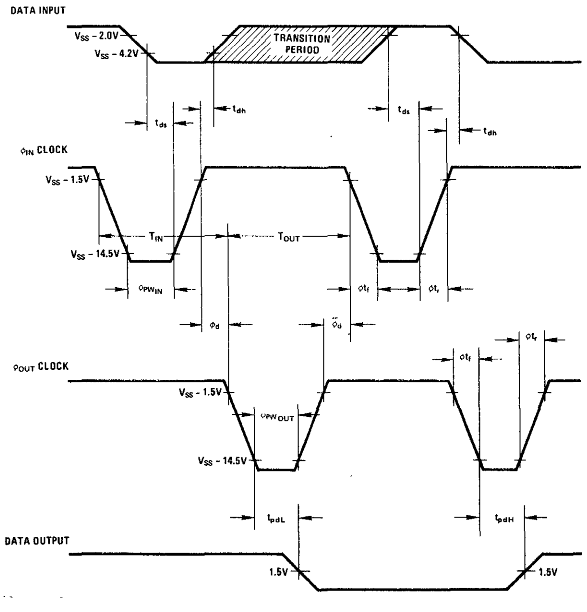
Typical Data Output Source Current vs Data Output Voltage



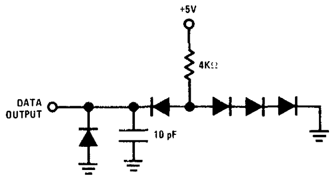
Typical Data Output Sink Current vs Data Output Voltage



switching time waveforms



ac test circuit



Dynamic Shift Registers

MM4018/MM5018 triple 64-bit dynamic shift register

general description

The MM4018/MM5018 triple 64-bit dynamic shift register is a monolithic MOS integrated circuit utilizing P-channel enhancement mode low threshold technology to achieve bipolar compatibility.

features

- Bipolar compatibility — +5V, −12V operation
  No pull-up or pull-down resistors required
- System flexibility — Guaranteed minimum operating frequency of 600 Hz at 25°C
- Military and commercial temperature ranges

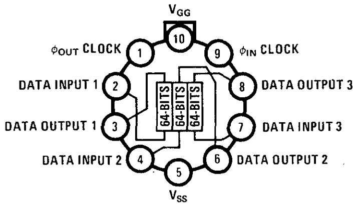
MM4018	−55°C to +125°C
MM5018	−25°C to +70°C

applications

- Calculator storage register
- CRT refresh memory
- Serial data storage.

connection diagram

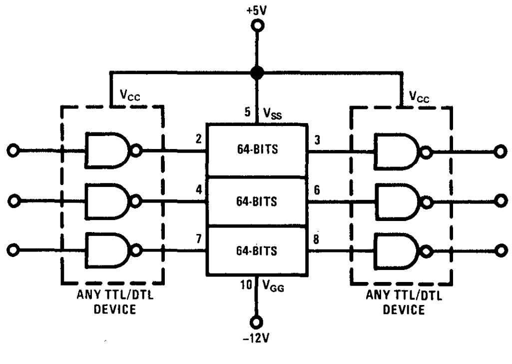
Metal Can Package



TOP VIEW

typical application

TTL/MOS Interface



absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} - 22.0V
Operating Temperature Range MM4018	-55°C to +125°C
MM5018	-25°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

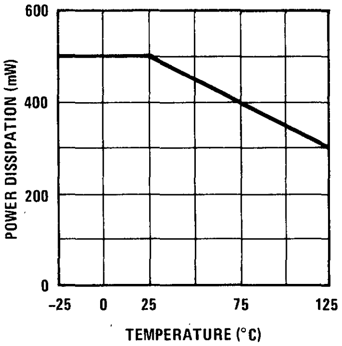
(T_A within operating temperature range, V_{SS} = +5.0V ±5% and V_{GG} = −12.0V ±10%, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical High Level (V_{IH})		V_{SS} - 2.0		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} - 18.5		V_{SS} - 4.2	V
Data Input Leakage	V_{IN} = −20V, T_A = 25°C, All other pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All other pins GND		3.0	5.0	pF
Clock Input Levels					
Logical High Level ($V_{\phi H}$)		V_{SS} - 1.5		V_{SS} + 0.3	V
Logical Low Level ($V_{\phi L}$)		V_{SS} - 18.5		V_{SS} - 14.5	V
Clock Input Leakage	V_I = −20V, T_A = 25°C, All other pins GND		0.05	1.0	μA
Clock Input Capacitance	V_I = 0.0V, f = 1 MHz, All other pins GND		45	60	pF
Data Output Levels					
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current (I_{GG})	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 0.15 μs, $V_{\phi L}$ = −12V				
	0.01 MHz $\leq \phi_f \leq$ 0.1 MHz		2.9	4.5	mA
	ϕ_f = 1 MHz		3.8	5.5	mA
	ϕ_f = 2.5 MHz		5.8	7.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns (Note 1)	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq$ 10.5 μs	0.15		10	μs
Clock Phase Delay Times (ϕ_d or ϕ_d)	Note 1	10			ns
Clock Transition Times					
Risetime (ϕt_r)	$\phi t_f + \phi_{PW} + \phi t_r \leq$ 10.5 μs			2	μs
Falltime (ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq$ 10.5 μs			2	μ
Partial Bit Times					
Input Partial Bit Time (T_{IN})	Note 1	0.20		100	μs
Output Partial Bit Time (T_{OUT})		0.20		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation					
Delay from ϕ_{OUT}	See AC Test Circuit				
Delay to Output High Level (t_{pdH})			150	200	ns
Delay to Output Low Level (t_{pdL})			150	200	ns

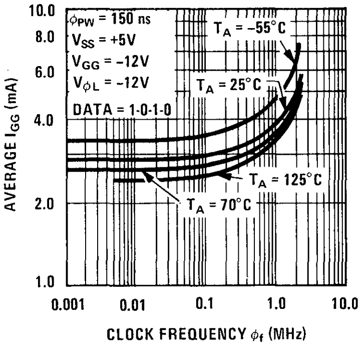
Note 1: Minimum clock frequency is a function of temperature and partial bit times (T_{IN} and T_{OUT}) as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency: $\phi_f(\text{min}) = \frac{1}{T_{IN} + T_{OUT}}$, where T_{IN} and T_{OUT} do not exceed the guaranteed maximums.

performance characteristics

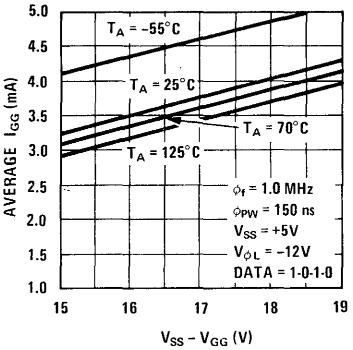
Maximum Power Dissipation



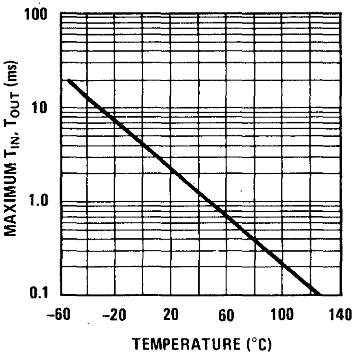
Power Supply Current vs Clock Frequency



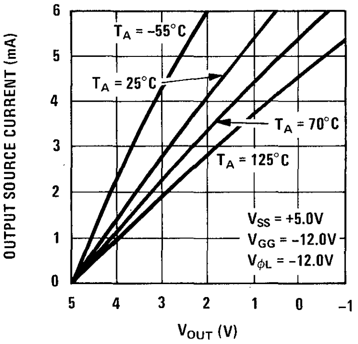
Power Supply Current vs V_{GG}



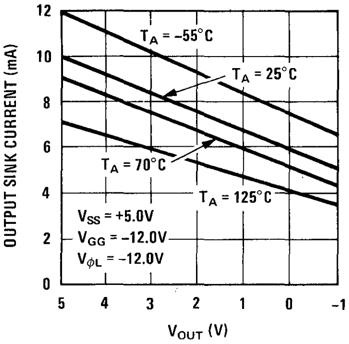
Guaranteed Maximum T_{IN} and T_{OUT} vs Temperature



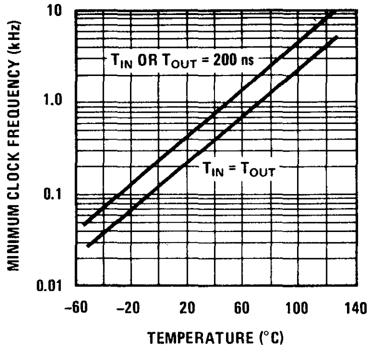
Data Output Source Current vs Data Output Voltage



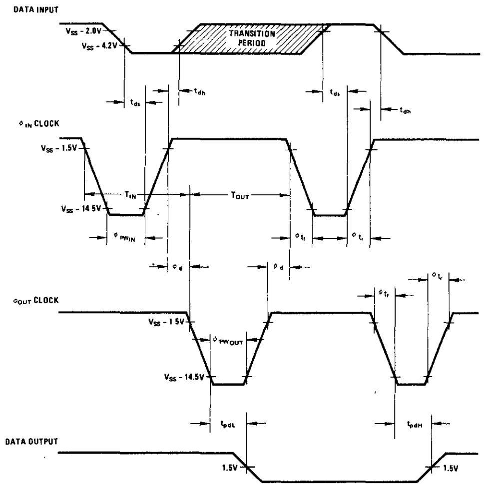
Data Output Sink Current vs Data Output Voltage



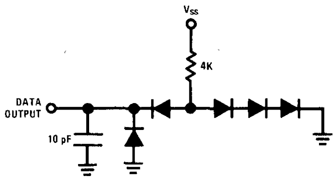
Guaranteed Minimum Clock Frequency vs Temperature



timing diagram



ac test circuit



Dynamic Shift Registers

MM4020/MM5020 quad 80-bit dynamic shift register
MM4021/MM5021 triple 80-bit dynamic shift register

general description

The MM4020/MM5020, and MM4021/MM5021 shift registers are monolithic MOS integrated circuits utilizing P-channel enhancement mode low threshold technology to achieve bipolar compatibility. The MM4021/MM5021 is a metal mask option of the MM4020/MM5020 which eliminates one of the 80-bit registers. Power and clock capacitance are reduced proportionally.

features

- Bipolar compatibility — +5V, −12V operation
No pull-up or pull-down resistors required
- System flexibility — Guaranteed minimum operating frequency of 250 Hz at 25°C
- Military and commercial temperature ranges

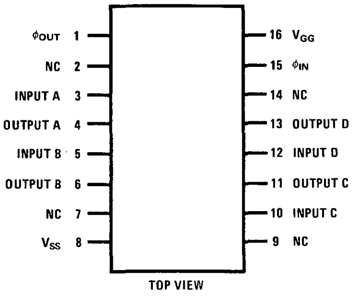
MM4020, MM4021	−55°C to +125°C
MM5020, MM5021	−25°C to +70°C

applications

- Calculator storage register
- CRT refresh memory
- Serial data storage

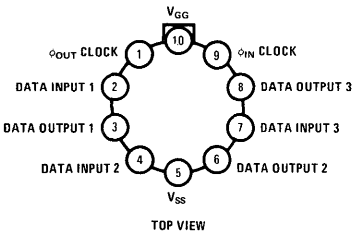
connection diagrams

Dual-In-Line Package



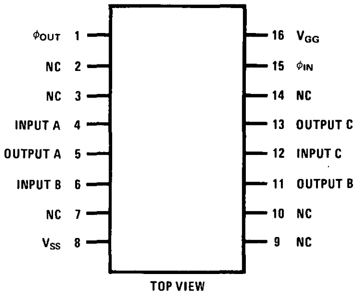
MM4020/MM5020

Metal Can Package



MM4021/MM5021

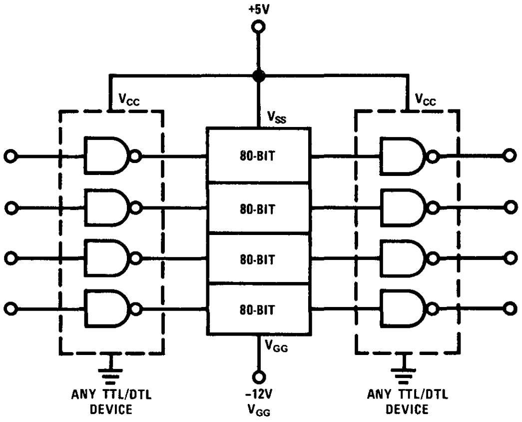
Dual-In-Line Package



MM4021/MM5021

typical applications

TTL/MOS/TTL Interface



absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} - 22.0V
Operating Temperature Range	
MM4020, MM4021	-55°C to +125°C
MM5020, MM5021	-25°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = −12.0V ±10%, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} - 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} - 18.5		V_{SS} - 4.2	V
Data Input Leakage	V_{IN} = −20V, T_A = 25°C, All Other Pins GND		0.01	0.5	µA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND (Note 2)		3.0	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} - 2.0		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} - 18.5		V_{SS} - 14.5	V
Clock Input Leakage	V_{ϕ} = −20V, T_A = 25°C, All Other Pins GND		0.05	1.0	µA
Clock Input Capacitance	V_{ϕ} = 0.0V, f = 1 MHz,				
	All Other Pins GND MM4020		70	90	pF
	(Note 2) MM4021		55	70	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = +25°C, V_{GG} = −12.0V, ϕ_{PW} = 150 ns, V_{SS} = +5.0V, $V_{\phi L}$ = V_{SS} - 17.0V, Data = 0-1-0-1				
MM4020/MM5020	0.01 MHz $\leq \phi_f \leq$ 0.1 MHz		2.9	4.4	mA
	ϕ_f = 1.0 MHz		6.4	8.0	mA
	ϕ_f = 2.5 MHz		10.1	12.5	mA
MM4021/MM5021	0.01 MHz $\leq \phi_f \leq$ 0.01 MHz		2.2	2.75	mA
	ϕ_f = 1.0 MHz		4.8	6.0	mA
	ϕ_f = 2.5 MHz		7.7	9.6	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns (Note 1)	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_r = \phi t_f$ = 20 ns	0.15		10.0	µs
Clock Phase Delay Times (ϕ_d, $\bar{\phi}_d$)	(Note 1)	10			ns
Clock Transition Times (ϕt_r, ϕt_f)				1.0	µs
Partial Bit Times (T)	(Note 1)				
Input Partial Bit Time (T_{IN})		0.2		100	µs
Output Partial Bit Time (T_{OUT})		0.2		100	µs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay from ϕ_{OUT}					
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

Note 1: Minimum clock frequency is a function of temperature and partial bit time, T_{IN} and T_{OUT}, as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

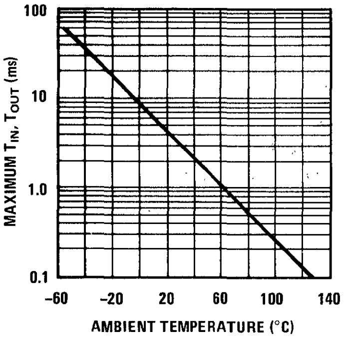
$$\phi_{f(min)} = \frac{1}{T_{IN} + T_{OUT}}$$

where T_{IN} and T_{OUT} may not exceed the guaranteed maximums.

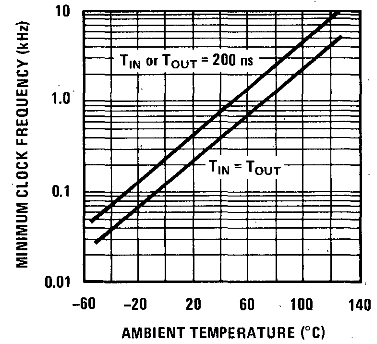
Note 2: Capacitance is guaranteed by periodic testing.

performance characteristics

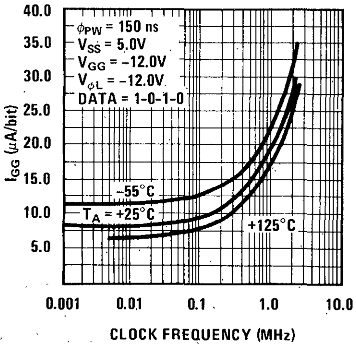
Guaranteed Maximum Partial Bit Times vs Temperature (Note 1)



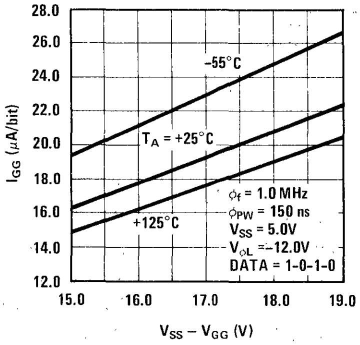
Guaranteed Minimum Clock Frequency vs Temperature (Note 1)



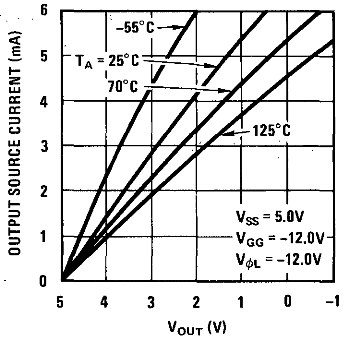
Typical Power Supply Current vs Clock Frequency



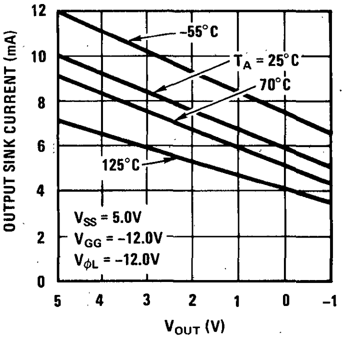
Typical Power Supply Current vs Voltage



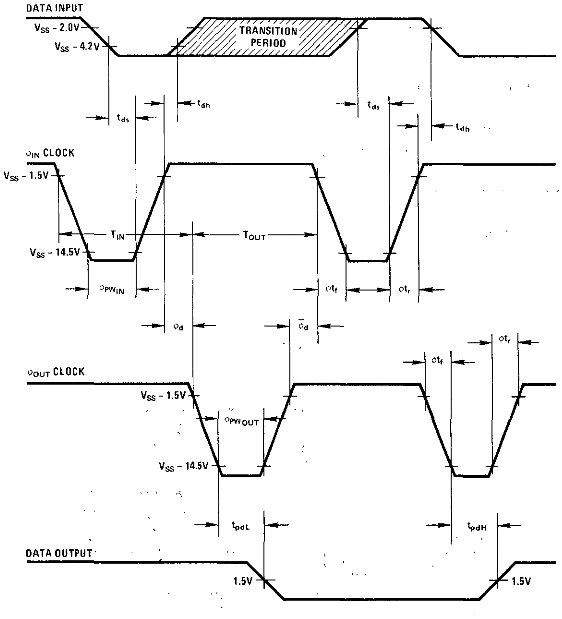
Typical Data Output Source Current vs Data Output Voltage



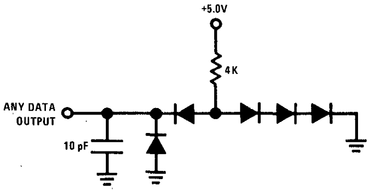
Typical Data Output Sink Current vs Data Output Voltage



switching time waveforms



ac test circuit



Dynamic Shift Registers

MM5081 10-bit serial in-parallel out lamp driver/register

general description

The MM5081 is a 10-bit serial in-parallel out static shift register. It is a monolithic MOS P-channel enhancement mode device utilizing a low threshold manufacturing process. The output circuits were designed to interface directly with gas tubes and other high voltage applications and will withstand 100V transient voltages and will hold off 55V. A serial output is provided for cascading of the registers without additional circuitry. This device utilizes a single phase clock to control the operation of data manipulation.

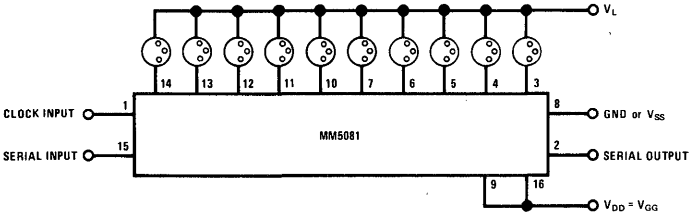
features

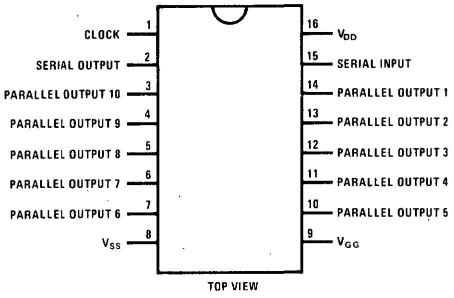
- High voltage output — –55V guaranteed
- Direct control of neon tubes
- Dual-In-Line Package
- Single phase clock
- Serial output for package cascading
- Data output — 10 bits in parallel

applications

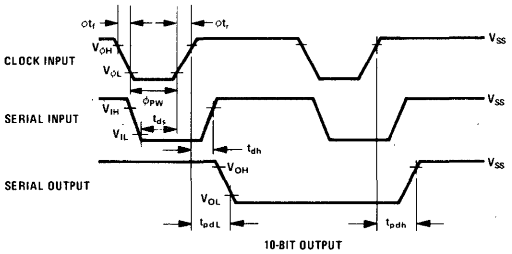
- Electric Sign Boards
- Neon Lamp Displays
- Test Equipment Displays

block and connection diagrams



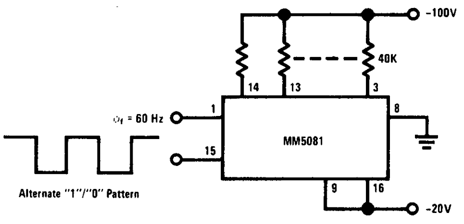


timing diagram

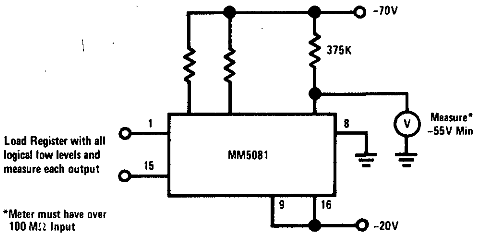


output junction tests

Stress Test



Leakage Test



absolute maximum ratings

Gate Voltage (V_{GG})	−25V to +0.3V
Drain Voltage (V_{DD})	−25V to +0.3V
Clock Input Voltage (V_{ϕ})	−25V to +0.3V
Data Input Voltage (V_{IN})	−25V to +0.3V
Storage Temperature	−55°C to +125°C
Operating Temperature	−25°C to +70°C
Output Stress (Parallel Output Lines)	−100V (see stress test)

electrical characteristics (−25°C to +70°C) (V_{SS} = 0V)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITION
V_{OH}	Parallel Output Voltage	5		V	
$V_{GG} = V_{DD}$	Supply Voltage	−20.0	−16.0	V	
I_{GG}	Supply Current		6.0	mA	$V_{DD} = V_{GG}$ = −20.0V register loaded all logical high levels. V_{SS} = GND
	Serial Input				
V_{IH}	Logical HIGH Level	V_{SS} − 2.5	V_{SS}	V	
V_{IL}	Logical LOW Level	V_{GG}	V_{SS} − 7.0	V	
t_{ds}	Data Setup Time	400		ns	
t_{dh}	Data Hold Time	50		ns	
	Serial Output				
V_{OH}	Logical HIGH Level	V_{SS} − 1.5	V_{SS}	V	
V_{OL}	Logical LOW Level	V_{GG}	V_{SS} − 8.0	V	
	Clock Amplitude				
$V_{\phi H}$	Logical HIGH Level	V_{SS} − 1.5	V_{SS}	V	
$V_{\phi L}$	Logical LOW Level	V_{SS} − 20	V_{SS} − 16	V	
I_L	Clock Leakage Current		5	μA	V_{ϕ} = −20.0V All other pins GND. T_A = 25°C
ϕ_f	Clock Pulse Frequency				
	For Serial Output	dc	250	kHz	
	For Parallel Output	dc	50	kHz	
ϕ_{pw}	Clock Pulse Width	2	10	μs	
ϕt_r	Clock Rise Time		2	μs	
ϕt_f	& Fall Time		2	μs	
	Trigger Method of F.F.	Trailing edge			
	Propagation Delay				
$t_{pd\ L}$	Serial		2	μs	
$t_{pd\ H}$	Parallel		2	μs	
I_{IL}	Input Leakage Current		5.0	μA	
C_{IS}	Input Capacitance (Data)		7	pF	
C_{ISC}	Input Capacitance (Clock)		18	pF	
	Parallel Output Leakage Current		40	μA	V_L = −55V V_{SS} = GND

Dynamic Shift Registers

MM4104/MM5104 dynamic shift register

general description

The MM4104/MM5104 360/359, 228/287, 40/32 bit dynamic shift register is a monolithic MOS integrated circuit utilizing p-channel enhancement mode low threshold technology to achieve bipolar compatibility. The register lengths are lengthened or shortened by hard wiring the length select line to V_{GG} or V_{SS}. The lengths available are: 40, 288, 328, 360, 400, 560, 688; or 32, 287, 319, 359, 391, 446, 678.

features

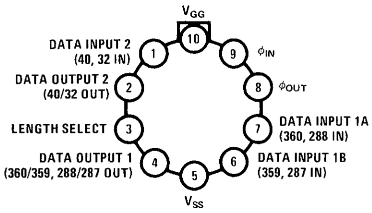
■ DTL/TTL compatibility	+5V, −12V power supply. No pull-up or pull-down resistors required
■ Multiple length registers	Electrically adjustable 360/359, 288/287, 40/32 bit registers
■ Wide frequency range	250 Hz min. guar. at 25°C 2.5 MHz max. guar. over temp.

applications

- Data store
- CRT displays
- Business machine

connection diagram

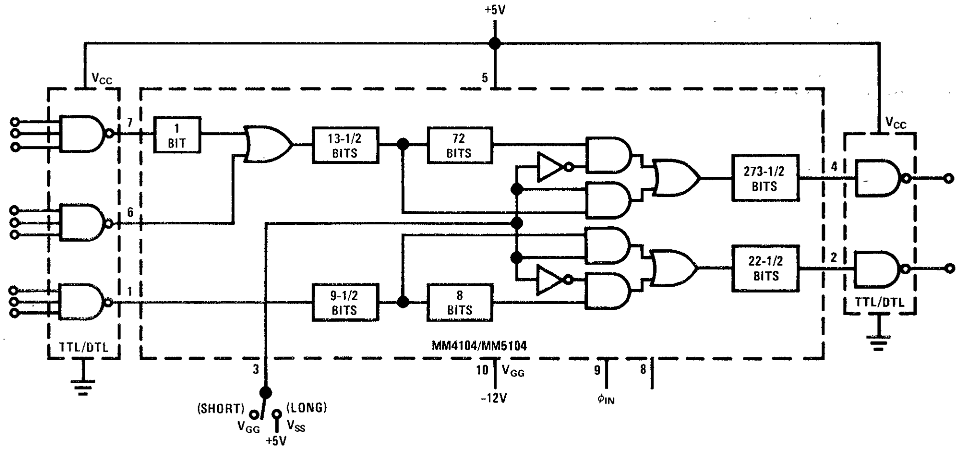
Metal Can Package



TOP VIEW

typical applications

TTL/MOS Interface



NOTE:

V_{GG} on pin 3 results in a 288-bit register between pin 7 and pin 4 and a 287-bit register between pins 6 and 4. The unused input (6 or 7) must be returned to V_{SS}. Also, there is a 32-bit register between pins 1 and 2.

V_{SS} on pin 3 results in a 360-bit register between pin 7 and pin 4 and a 359-bit register between pins 6 and 4. The unused input (6 or 7) must be returned to V_{SS}. Also, there is a 40-bit register between pins 1 and 2.

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} - 22V
Operating Temperature Range MM4104	-55°C to 125°C
MM5104	-25°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

(T_A within operating temperature range, V_{SS} = +5.0V, ±5%, V_{GG} = −12.0V ±10%, unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} - 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} - 18.5		V_{SS} -4.2	V
Data Input Leakage	V_{IN} = -20.0V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND, (Note 3)		3.0	5.0	pF
Length Select Input Levels					
Logical HIGH Level (V_{LSH})		V_{SS}		V_{SS} + 0.3	V
Logical LOW Level (V_{LSL})		V_{SS} - 18.5		V_{GG}	V
Length Select Input Leakage	V_{IN} = -20V, T_A = 25°C, All Other Pins GND		0.01	0.5	μA
Length Select Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND, (Note 3)		6.0	9.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} - 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} -18.5		V_{SS} - 14.5	V
Clock Input Leakage	V_{ϕ} = -20V, T_A = 25°C, All Other Pins GND		0.05	1.0	μA
Clock Input Capacitance	V_{ϕ} = 0.0V, f = 1 MHz, All Other Pins GND, (Note 3)		85	100	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = 25°C, V_{GG} = −12V, ϕ_{PW} = 150 ns V_{SS} = 5.0V, $V_{\phi L}$ = −12V, Data = 0-1-0-1				
	0.01 MHz ≤ ϕ_f ≤ 0.1 MHz		1.5	2.5	mA
	ϕ_f = 1 MHz		3.5	5.0	mA
	ϕ_f = 2.5 MHz		7.0	10.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, (Note 1)	0.01	3.3	2.5	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq$ 10.5 μs	0.15		10	μs
Clock Phase Delay Times (ϕ_d, $\overline{\phi}_d$)	(Note 1)	10			ns
Clock Transition Time (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq$ 10.5 μs			1	μs
Partial Bit Times (T)	(Note 1)				
Input Partial Bit Time (T_{IN})		0.20		100	μs
Output Partial Bit Time (T_{OUT})		0.20		100	μs
Data Input Setup Time (t_{ds})		80	30		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay from ϕ_{OUT}	See ac test circuit.				
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

Note 1: Minimum clock frequency is a function of temperature and partial bit times, T_{IN} and T_{OUT}, as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The least guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency is:

$$\phi_f\,(\text{min}) = \frac{1}{T_{IN} + T_{OUT}}$$

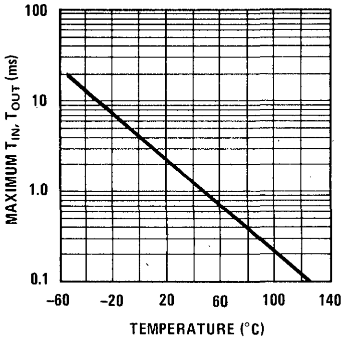
where T_{IN} and T_{OUT} may not exceed the guaranteed maximum.

Note 2: The curves are guaranteed by testing at a high temperature point.

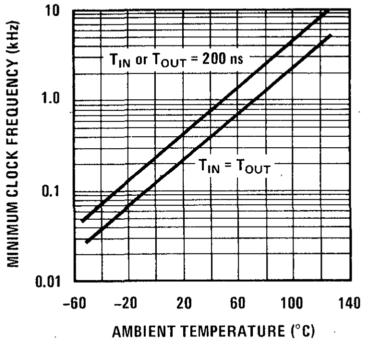
Note 3: Capacitance is guaranteed by periodic testing.

performance characteristics

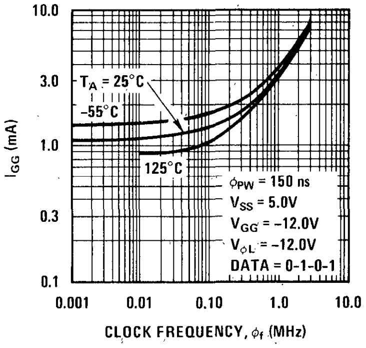
Guaranteed Maximum T_{IN} and T_{OUT} vs Temperature (Notes 1, 2)



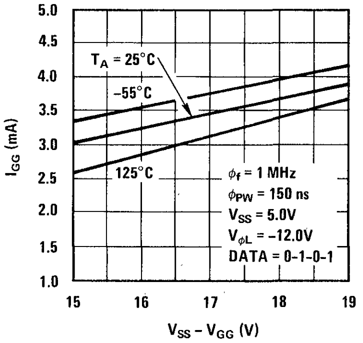
Guaranteed Minimum Clock Frequency vs Temperature (Notes 1, 2)



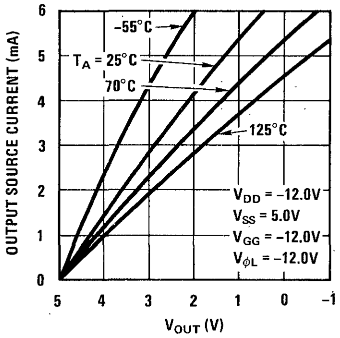
Typical Power Supply Current vs Clock Frequency



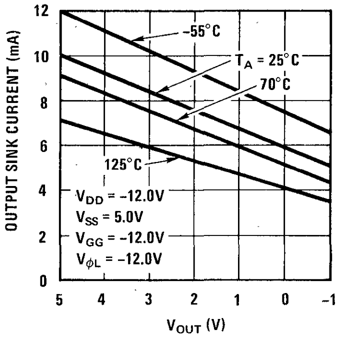
Typical Power Supply Current vs V_{GG}



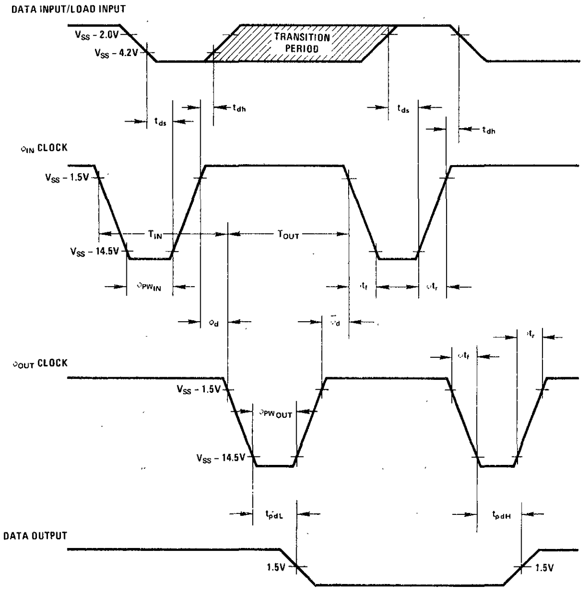
Typical Output Source Current vs Voltage



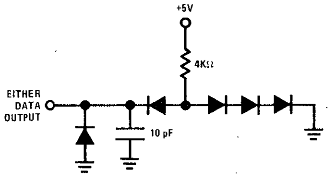
Typical Output Sink Current vs Voltage



switching time waveforms



ac test circuit



Dynamic Shift Registers

MM4105/MM5105 quad 64-bit dynamic shift register/accumulator

general description

The MM4105/MM5105 quad 64-bit dynamic shift register/accumulator is a monolithic MOS integrated circuit utilizing P-channel enhancement mode low threshold technology to achieve bipolar compatability on input/output and control lines. Any one of four recirculating shift registers may be selected, by external logic control, for interrogation at the single common output or for writing in new data at the common input data line.

features

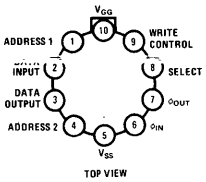
■ TTL compatability	+5, −12V power supplies no pull up or pull down resistors required internal pull up resistors on inputs
■ Input bus capability	chip select allows control of data entry from common bus line
■ Versatile operation	recirculation and register select logic on-chip

applications

- ■ Data buffers
- ■ Disc/drum memory replacement
- ■ Register for arithmetic units

connection diagram

Metal Can Package



TOP VIEW

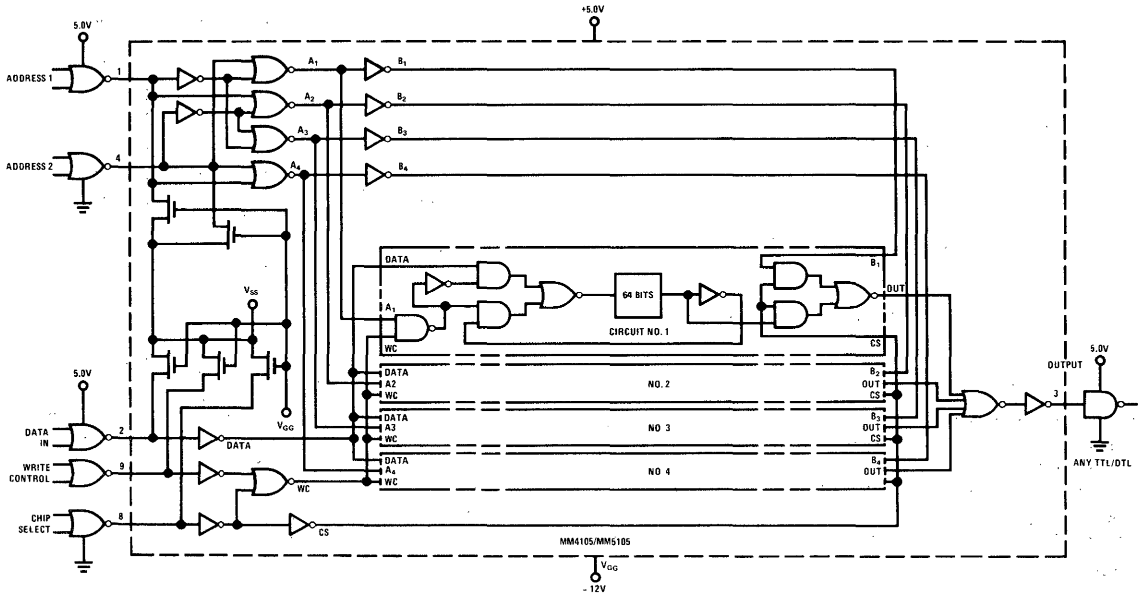
truth table

Logic Definition
"1" Logical HIGH Level
"0" Logical LOW Level

CODING AND MODE TABLE

Address		Write Control		Chip Select		Output Level		
1	2	Write	Recir	Active	Inactive	Chip Select	Input	Output
0	0	0	1	0	1	1	0	0
0	1	0	1	0	1	1	1	1
1	0	0	1	0	1	0	0	1
1	1	0	1	0	1	0	1	1

typical application



absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 22V
Operating Temperature Range MM4105	−55°C to +125°C
MM5105	−25°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{GG} = −12.0V ±10%, unless otherwise specified.

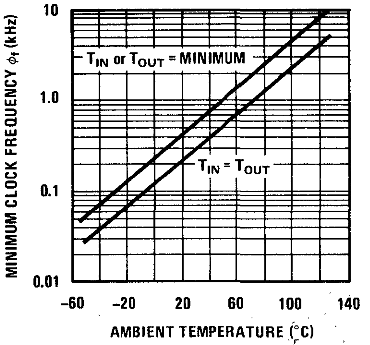
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} −18.5		V_{SS} − 4.2	V
Data Input Leakage (V_{IL})	V_{IN} = −20V, T_A = 25°C, All Other Pins GND		.01	0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND Note 2		3.0	5.0	pF
Chip Select, Write Control and Address 2 Input Levels					
Logical HIGH Level (V_{CH})		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level (V_{CL})		V_{SS} −18.5		V_{SS} − 4.2	V
Chip Select, Write Control and Address 2 Input Leakage	V_{IN} = −20V, T_A = 25°C, All Other Pins GND		0.1	1.0	μA
Chip Select, Write Control and Address 2 Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND Note 2		15	20	pF
Data, Chip Select, Write Control and Address 2 Input Pull-up Resistance	V_{SS} = 5.0V V_{GG} = −12.0V V_{IN} = 0.5V T_A = 25°C	3.0	6.0	9.0	kΩ
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} −18.5		V_{SS} −14.5	V
Clock Input Leakage	V_{ϕ} = −20V, T_A = 25°C, All Other Pins GND		0.5	1.0	μA
Clock Input Capacitance	V_{ϕ} = 0.0V, f = 1 MHz, All Other Pins GND Note 2			100	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current I_{GG}	T_A = 25°C, V_{GG} = −12.0V, ϕ_{PW} = 300 ns, V_{SS} = +5.0V, $V_{\phi L}$ = −120V, Data = 0-1-0-1 0.01 MHz $\leq \phi_f \leq$ 0.1 MHz		3.2	5.0	mA
	ϕ_f = 1.0 MHz		5.0	8.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns, Note 1	0.01	1.5	1.4	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$	0.30		10.0	μs
Clock Phase Delay Times (ϕ_d, $\overline{\phi}_d$)	Note 1	10			ns
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			1.0	μs
Partial Bit Times (T)					
Input Partial Bit Time (T_{IN})	Note 1	0.35		100	μs
Output Partial Bit Time (T_{OUT})		0.35		100	μs
Data Input Setup Time (t_{ds})		300	200		ns
Data Input Hold Time (t_{dh})		20	0		ns
Chip Select, Write Control and Address Setup Time (t_{ds})		300	200		ns
Chip Select, Write Control and Address Hold Time (t_{dh})		20	0		ns
Data Output Propogation Delay from ϕ_{OUT}					
Delay to HIGH Level (t_{pdH})			150	200	ns
Delay to LOW Level (t_{pdL})			150	200	ns

Note 1: Minimum clock frequency is a function of temperature and partial bit times (T_{IN} and T_{OUT}) as shown by the ϕ_f versus temperature and T_{IN}, T_{OUT} versus temperature curves. The lowest guaranteed clock frequency for any temperature can be attained by making T_{IN} equal to T_{OUT}. The minimum guaranteed clock frequency: $\phi_f(\text{min}) = \dfrac{1}{T_{IN} + T_{OUT}}$ where T_{IN} and T_{OUT} do not exceed the guaranteed maximums.

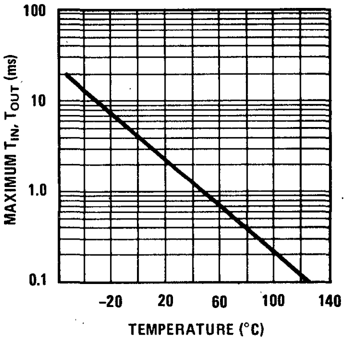
Note 2: Capacitance is guaranteed by periodic testing.

performance characteristics

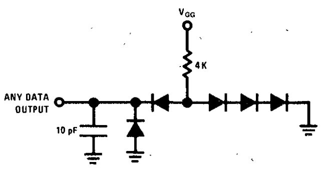
Guaranteed Minimum Clock Frequency vs Temperature (Note 1)



Guaranteed Maximum Partial Bit Times vs Temperature

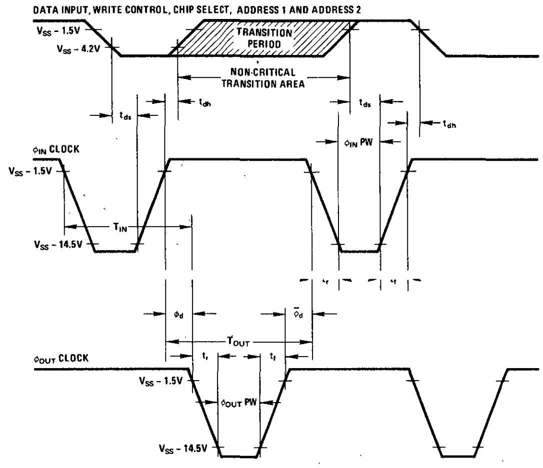


ac test circuit

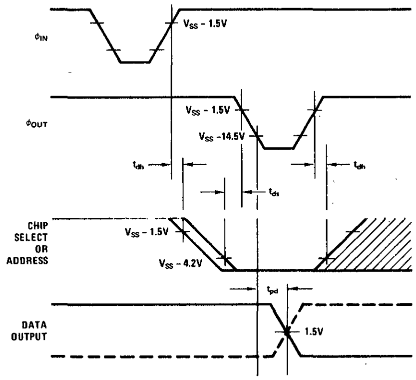


timing diagrams

For Writing Data



For Reading Data



Explanation of Timing Diagrams

In order to write-in or read-out of the MM4105/MM5105, the chip select line must be low during the appropriate clock cycle. If the chip select line is held high during the ϕ_{OUT} clock pulse the output will go high. If it is high during ϕ_{IN} time, data may not be written in. The timing diagram shows that in order to read from a register all inputs must be stable during ϕ_{IN} time. To write information, the write control and chip select must be held low. The address lines and data will depend on what register is to be selected and what information is to be stored. When the write control line is high the information stored in the registers is recirculated.

To read information out chip select must be low and address lines stable during the ϕ_{OUT} clock. Information is always recirculated in the four registers unless chip select and the write control are low. Then, depending on which address is selected, only three registers are recirculating while the selected register is receiving new data.

It is possible to write into and read out of the same register during one clock period. To write information into the register, chip select and write control are held low during the ϕ_{IN} clock. Data and the address lines must be stable during the same ϕ_{IN} clock. During the next ϕ_{OUT} clock time, chip select is held low with the address unchanged. An output will appear from the same register.

To write information into one register and read out of a second register during one clock period similar timing can be used. The address can be changed between the ϕ_{IN} and ϕ_{OUT} clocks to select either of the other three registers.

Static Shift Registers

*MM404/MM504 dual 16 bit static register
*MM405/MM505 dual 32 bit static register

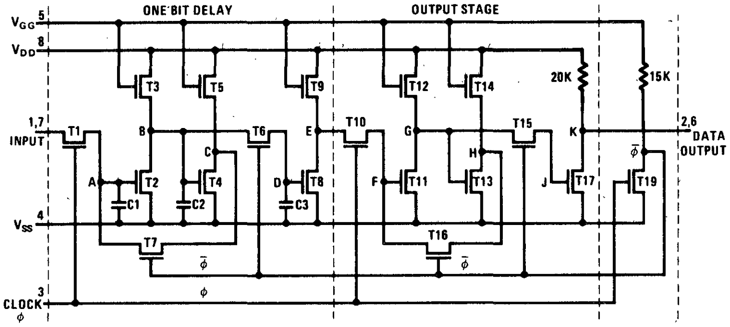
general description

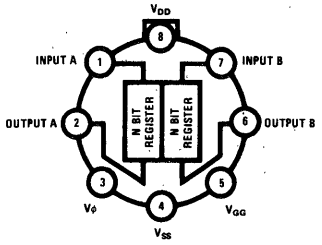
The National Semiconductor line of MOS static shift registers are monolithic integrated circuits utilizing P-channel enhancement mode transistors. The use of a low threshold technology permits operation with a V_{DD} supply voltage of −10 volts and a V_{GG} supply and clock amplitude voltage of less than −16 volts. These registers require only a single clock input to operate from DC to 1 MHz in either synchronous or asynchronous systems. Each register cell is designed specifically to avoid race conditions during latching, thus insuring operation under all conditions specified in the electrical characteristics.

Additional features include:

■ Bipolar compatibility	
■ Single phase clock input	
■ High frequency operation	1.0 MHz
■ Low power consumption	1.7 mW/bit typ
■ Output impedance (V_{OH})	500Ω typ
■ Military and commercial temperature ranges	
MM404, MM405	−55°C to +125°C
MM504, MM505	−25°C to +70°C

schematic and connection diagrams



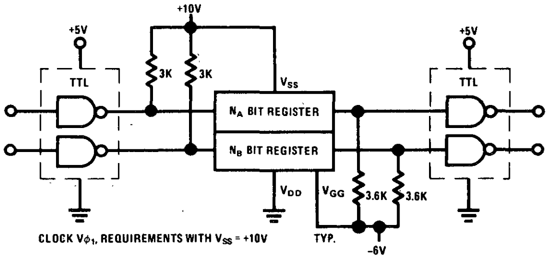


Note: Pin 4 connected to case

Top View

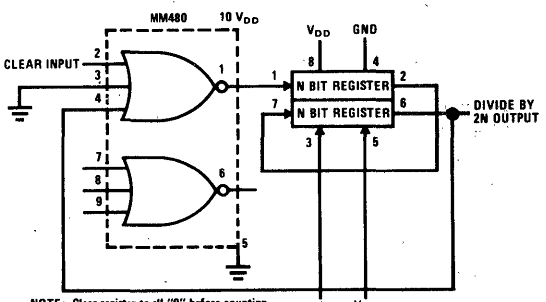
typical applications

TTL/MOS Interface



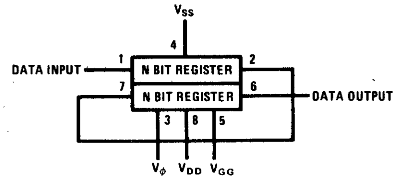
CLOCK $V\phi_1$, REQUIREMENTS WITH V_{SS} = +10V — TYP.
LOGIC "0" — V_{SS} −1.5V
LOGIC "1" — V_{SS} −16V

2N Bit Johnson Counter

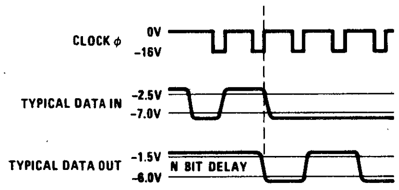


NOTE: Clear register to all "0" before counting by applying "1" to clear input and clocking through 2N clock cycles.

Single 2N Bit Register



Waveforms for Applications
(complete timing diagrams on page 53)



*For New Designs, see MM4040/MM5040, MM4050A/MM5050A.

absolute maximum ratings

Drain Voltage (V_{DD})		+0.5V to −25V
Gate Voltage (V_{GG})		+0.5V to −25V
Clock Input ($V_{\phi 1}$)		+0.5V to −25V
Data Inputs		+0.5V to −25V
Power Dissipation (Note 1)		300 mW
Operating Temperature	MM404, MM504	−55°C to +125°C
	MM405, MM505	−25°C to +70°C
Storage Temperature		−65°C to +150°C

electrical drive requirements (Note 1)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Clock pulse Width ϕ_1 Clock, ϕ_{1pw}		0.4		10	μs
Clock Pulse Risetime, $t_{r\phi}$	1 MHz with ϕ_{pw} = 0.4 μs			0.05	μs
Falltime, $t_{f\phi}$	100 kHz with ϕ_{pw} = 2 μs			0.6	μs
	10 kHz with ϕ_{pw} = 10 μs			2.0	μs
Clock Input Level					
Logic "$V_{\phi H}$"			V_{SS} −0.5	V_{SS} −1.5	V
Logic "$V_{\phi L}$"		V_{SS} −14.5	V_{SS} −16.0	V_{SS} −18.0	V
Data Input Voltage Levels					
Logic "V_{IH}"				V_{SS} −2.5	V
Logic "V_{IL}"		V_{SS} −7.0			V
Data Setup Time, t_{ds}		0.2			μs
Data Hold Time, t_{dh}		0.03			μs

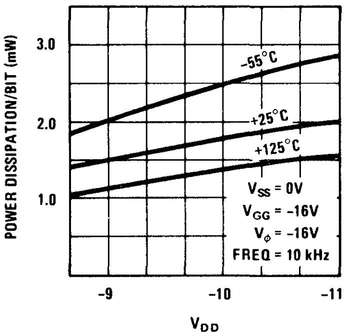
electrical characteristics (Note 2)

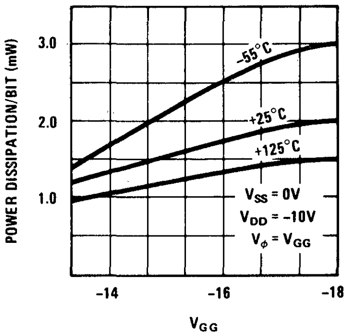
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Clock Repetition Rate	Fan-Out "1"	dc		1.0	MHz
Data Output Voltage Levels					
Logic "V_{OH}"				V_{SS} −1.5	V
Logic "V_{OL}"		V_{SS} −8.0			V
Data Input Capacitance (Each Input)	f = 1 MHz V_{IN} = 0V		1.5	3.0	pF
Clock Line Capacitance	f = 1 MHz, −20V Bias MM404, MM504		9.5	15	pF
	MM405, MM505		18	30	pF
	0V Bias MM404, MM504		15.0	20	pF
	MM405, MM505		25	40	pF
Output Impedance	Outputs at Logic "0"		0.5	1.0	kΩ
Output Impedance Pins 2 & 6	Outputs at Logic "1"	15	20	25	kΩ
Impedance Pin 8	All Other Pins at GND	7.5	10	12.5	kΩ
Breakdown Voltage	1.0 μA Test Current T_A = 25°C				
On Pin 1	GND on Pins 2, 3, 4, 5, 6, 7 −11V on Pin 8	−25			V
On Pin 7	GND on Pins 1, 2, 3, 4, 5, 6 −11V on Pin 8	−25			V
Leakage Current	T_A = 25°C				
Pin 1	V_{IN} = −18V, V_8 = −11V All Other Pins at GND			0.5	μA
Pin 7	V_{IN} = 18V, V_8 = −11V All Other Pins at GND			0.5	μA
Pin 8	V_{IN} = −8V All Other Pins at GND			0.5	μA
Power Supply Current Drain (V_{DD})	Outputs at Logic "0" 1 MHz Operation T_A = 25°C				
	MM404, MM504		5.5	10.0	mA
	MM405, MM505		10.0	15.0	mA

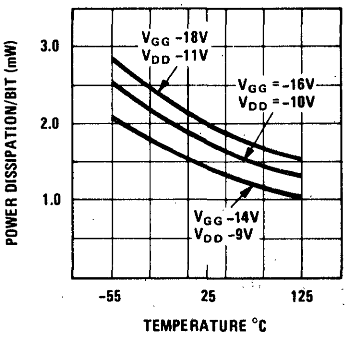
Note 1: For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient. The full rating applies for case temperatures to +125°C.

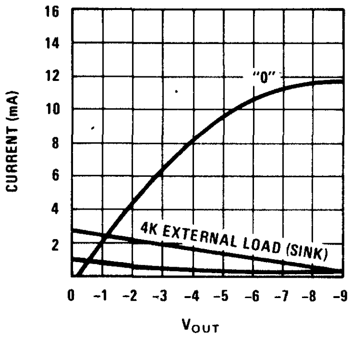
Note 2: These specifications apply over the specified temperature ranges for $-11V < V_{DD} < -9.5V$, and $-18V < V_{GG} < -14.5V$ and clock repetition rate of 10 kHz with output measurement load of less than 10 pF in parallel with 10 MΩ to ground unless otherwise specified.

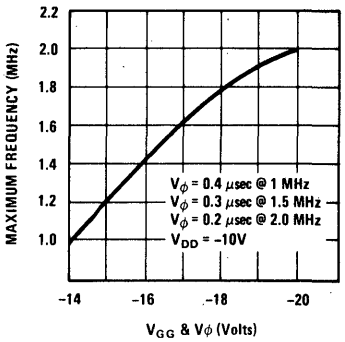
performance characteristics


Power Dissipation vs V_{DD}


Power Dissipation vs V_{GG}


Power Dissipation vs Temp.


V_{OUT} vs Load Current


Max. Frequency vs Supply Voltages

operation

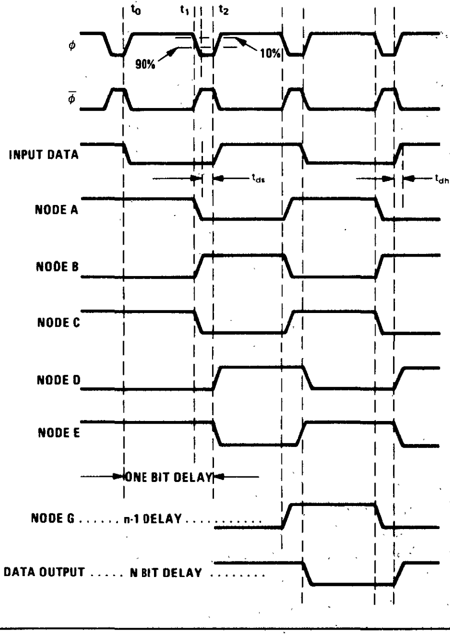
A diagram of a one-bit static register employing two clock phases (ϕ, $\bar{\phi}$) is shown in the schematic. The register requires only one external clock phase (ϕ) since the second clock ($\bar{\phi}$) is generated internally by T_{19} and 15K; this configuration simplifies the input drive requirements.

The basic cell functions as follows. Each bit of delay consists of three inverters T_2, T_4, and T_8 in conjunction with three MOS load resistors T_3, T_5, and T_9 followed by three coupling devices T_1, T_6, and T_7. The timing diagram shows the sequence of operation. Assume the input is at a logic "1" level during t_1 time. When the clock (ϕ) goes to a logic "1" level, two operations take place simultaneously. First, transistor T_1 turns "ON", transferring the input data (logic "1" level) to the gate to source capacitance (C_1) of T_2. The voltage stored on C_1 is sufficient to turn T_2 "ON" discharging node B. With the gate to source capacitance (C_2) of T_4 discharged, T_4 turns "OFF" placing a logic "1" level at node C. Concurrently ϕ turns T_{19} "ON" generating the complement of ϕ, that is ϕ and in turn $\bar{\phi}$ is used to turn T_6 and T_7 "OFF". This action allows the register's previous information to be temporarily stored on the gate to source capacitance C_3 of T_8. The output at node E during this timing sequence remains unchanged. However, during t_2 time, clock ϕ returns to ground; concurrently $\bar{\phi}$ goes to a logic "1" level turning T_1 "OFF" allowing T_6 and T_7 to turn "ON". The information which was previously stored on the gate of T_8 discharges to a logic "0" level causing the output at node E to switch to a logic "1" level thereby obtaining the required one-bit of delay.

Likewise the information at node C is fed back to node A latching T_2 in the "ON" state.

When a logic "0" level is presented at the register input, the sequence is once again repeated. The bit delay demonstrated in this example is repeated for each half of the dual static register.

timing diagram



Static Shift Registers

MM4040/MM5040 dual 16-bit static shift register

general description

The MM4040/MM5040 dual 16-bit static shift register is a monolithic integrated circuit utilizing P channel enhancement mode low threshold technology to achieve direct bipolar compatibility on the inputs and outputs. The device requires only a single phase clock.

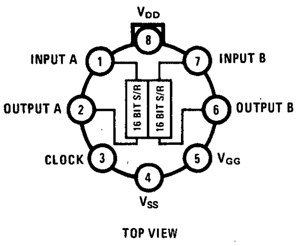
features

- Bipolar compatibility +5, −12V operation No pull-up or pull-down resistors needed
- High frequency operation 2.2 MHz guaranteed
- Single phase clock

applications

- Static data buffer
- Serial memory storage
- Printer memory
- Telemetry systems and data sampling

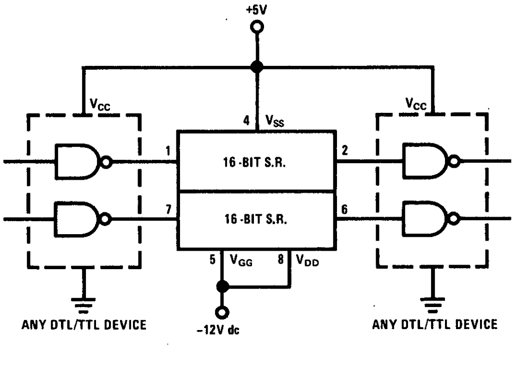
connection diagram



Metal Can Package

TOP VIEW

typical application



absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} – 22
Operating Temperature Range MM4040	-55°C to +125°C
MM5040	-25°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

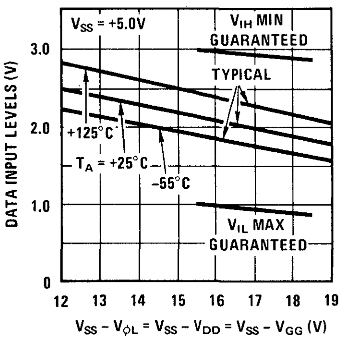
T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{SS} – V_{DD} = 9V to 18.5V, V_{GG} = –12V ±10%, unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical High Level (V_{IH})		V_{SS} – 2.0		V_{SS} + 0.3	V
Logical Low Level (V_{IL})		V_{SS} – 18.5		V_{SS} – 4.2	V
Data Input Leakage	V_{IN} = – 20V, T_A = 25°C, All Other Pins GND			0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)		2.5	5.0	pF
Clock Input Levels					
Logical High Level ($V_{\phi H}$)		V_{SS} – 1.5		V_{SS} + 0.3	V
Logical Low Level ($V_{\phi L}$)		V_{SS} – 18.5		V_{SS} – 14.5	V
Clock Input Leakage	V_{ϕ} = –20V, T_A = 25°C, All Other Pins GND			1.0	μA
Clock Input Capacitance	V_{ϕ} = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)		19	22	pF
Data Output Levels					
Logical High Level (V_{OH})	I_{SOURCE} = –0.5 mA	2.4			V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current	T_A = +25°C, V_{GG} = –12V, ϕ_{PW} = 200 ns, V_{SS} = 5V, V_{DD} = –12V, $V_{\phi L}$ = –12V, Data = 0–1–0–1				
I_{GG}	0.01 MHz $\leq \phi_f \leq$ 0.1 MHz		1.0	2.0	mA
	ϕ_f = 1.0 MHz		1.8	3.0	mA
	ϕ_f = 2.0 MHz		3.0	4.0	mA
I_{DD}	0.01 MHz $\leq \phi_f \leq$ 0.1 MHz		5.0	9.0	mA
	ϕ_f = 1.0 MHz		5.1	9.0	mA
	ϕ_f = 2.0 MHz		5.2	9.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns	DC	3.0	2.2	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_r + \phi t_f + \phi_{PW} \leq$ 10.5 ns	.200	.100	10.0	μs
Clock Transition Times ($\phi t_r + \phi t_f$)	$\phi t_r + \phi t_f + \phi_{PW} \leq$ 10.5 ns			1.0	μs
Data Input Setup Time (t_{ds})		120	60		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay from ϕ	See test circuit				
Delay to High Level (t_{pdH})			200	300	ns
Delay to Low Level (t_{pdL})			200	300	ns

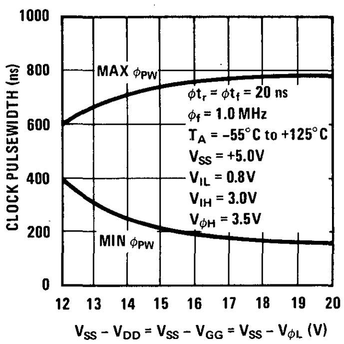
Note 1: Capacitance values are guaranteed by statistical lot sample testing.

guaranteed performance characteristics

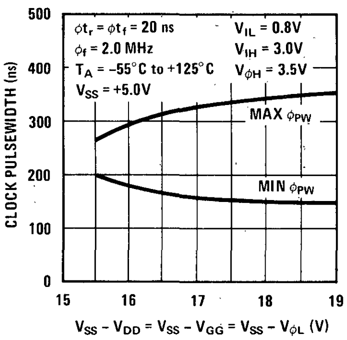
Data Input Levels vs Supply Voltage



1.0 MHz Operating Curve

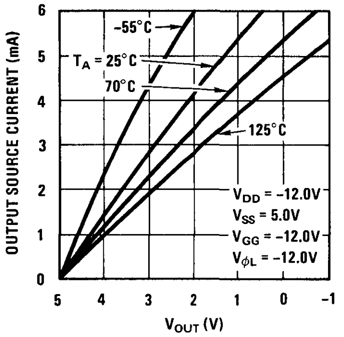


2.0 MHz Operating Curve

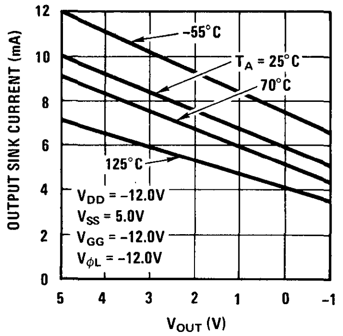


typical performance characteristics

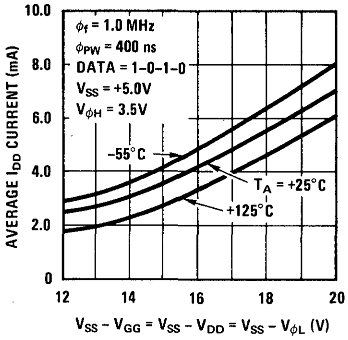
Data Output Source Current vs Voltage



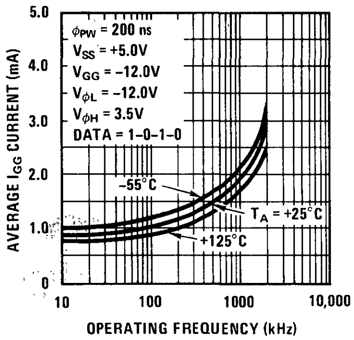
Data Output Sink Current vs Voltage



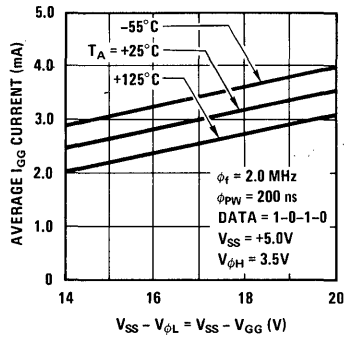
Power Supply Current vs Voltage



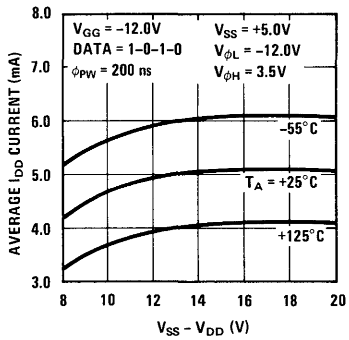
Power Supply Current vs Operating Frequency



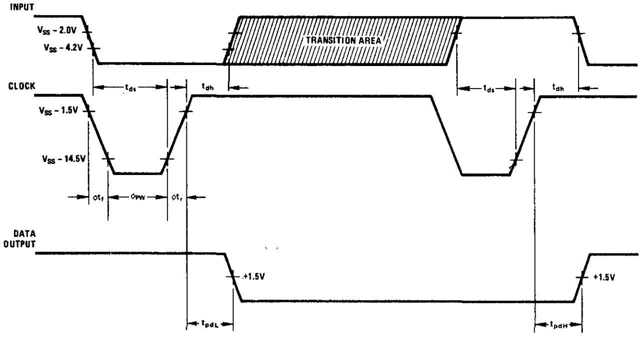
Power Supply Current



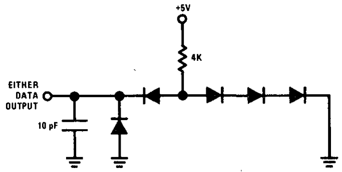
Power Supply Current



switching time waveforms



test circuit



Static Shift Registers

MM4050A/MM5050A dual 32-bit static shift register
MM4051A/MM5051A dual 32-bit static shift register–split clock

general description

The MM4050A/MM5050A and MM4051A/MM5051A dual 32-bit static shift registers are monolithic MOS integrated circuits utilizing P channel enhancement mode low threshold technology to achieve bipolar compatibility. Operation to 2.2 MHz is achieved with a single phase clock. The MM4051A/MM5051A is a bonding option of the MM4050A/MM5050A to provide independent clock control of each register.

features

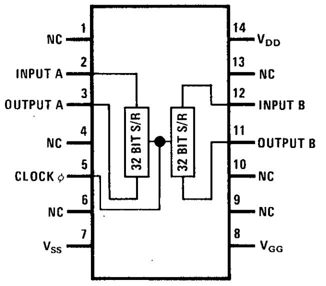
■ Bipolar compatibility	+5V, −12V operation No pull-up or pull-down resistors needed
■ High frequency operation	dc to 2.2 MHz
■ Single phase clock	
■ Improved drive capability	Push-pull outputs
■ Military and commercial temperature ranges	
MM4050A, MM4051A	−55°C to +125°C
MM5050A, MM5051A	−25°C to +70°C

applications

- Serial memory storage
- Printer memory
- Telemetry systems and data sampling

logic and connection diagrams

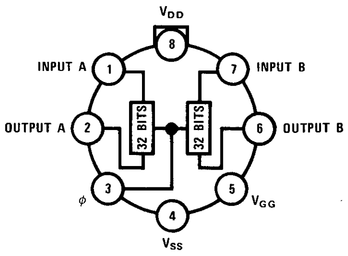
Dual-In-Line Package



TOP VIEW

MM5050A

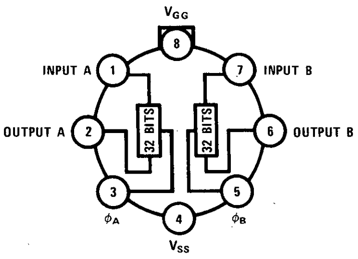
Metal Can Package



TOP VIEW

MM4050A/MM5050A

Metal Can Package

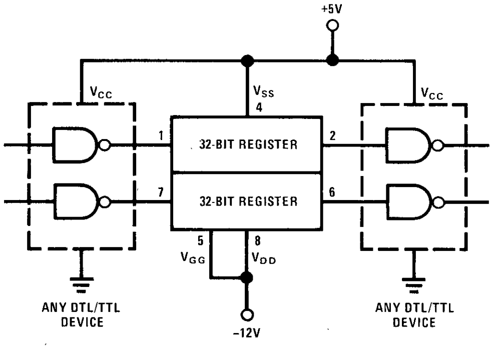


TOP VIEW

MM4051A/MM5051A

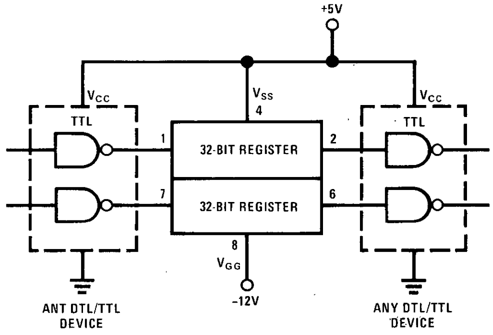
typical applications

TTL/MOS Interface



MM4050A/MM5050A

TTL/MOS Interface



MM4051A/MM5051A

absolute maximum ratings

Voltage at Any Pin		V_{SS} + 0.3V to V_{SS} - 22V
Operating Temperature Range	MM4050A/MM4051A	-55°C to +125°C
	MM5050A/MM5051A	-25°C to +70°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

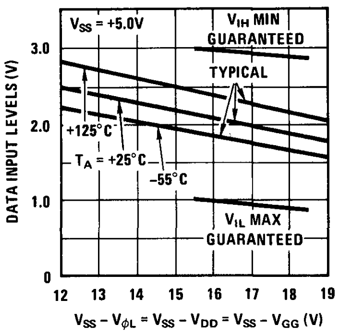
T_A within operating temperature range, V_{SS} = +5.0V ±5%, V_{SS} – V_{DD} = 9V to 18.5V, V_{GG} = –12V ±10%, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical HIGH Level (V_{IH})		V_{SS} - 2.0		V_{SS} + 0.3	V
Logical LOW Level (V_{IL})		V_{SS} - 18.5		V_{SS} - 4.2	V
Data Input Leakage	V_{IN} = –20V, T_A = 25°C, All Other Pins GND			0.5	μA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)		2.5	5.0	pF
Clock Input Levels					
Logical HIGH Level ($V_{\phi H}$)		V_{SS} - 1.5		V_{SS} + 0.3	V
Logical LOW Level ($V_{\phi L}$)		V_{SS} - 18.5		V_{SS} -14.5	V
Clock Input Leakage	V_{ϕ} = –20V, T_A = 25°C, All Other Pins GND			1.0	μA
Clock Input Capacitance	V_{ϕ} = 0.0V, f = 1 MHz, All Other Pins GND (Note 1)		25	35	pF
Data Output Levels					
Logical HIGH Level (V_{OH})	I_{SOURCE} = –0.5 mA	2.4			V
Logical LOW Level (V_{OL})	I_{SINK} = 1.6 mA			0.4	V
Power Supply Current					
I_{GG}	T_A = +25°C, V_{GG} = –12.0V, ϕ_{PW} = 200 ns V_{SS} = +5.0V, $V_{\phi L}$ = –12.0V, Data = 0-1-0-1 V_{DD} = –12.0V				
	0.01 MHz $\leq \phi_f \leq$ 0.1 MHz		1.6	3.5	mA
	ϕ_f = 1.0 MHz		3.8	8	mA
	ϕ_f = 2.0 MHz		4.6	11.0	mA
I_{DD}	0.01 MHz $\leq \phi_f \leq$ 0.1 MHz		2.7	5.0	mA
	$\phi_f \leq$ 1.0 MHz		2.9	5.0	mA
	$\phi_f \leq$ 2.0 MHz		3.1	5.0	mA
Clock Frequency (ϕ_f)	$\phi t_r = \phi t_f$ = 20 ns	DC	3.0	2.2	MHz
Clock Pulsewidth (ϕ_{PW})	$\phi t_r + \phi t_f + \phi_{PW} \leq$ 10.5 μs	0.2	0.100	10.0	μs
Clock Transition Times (ϕt_r, ϕt_f)	$\phi t_r + \phi t_f + \phi_{PW} \leq$ 10.5 μs			1.0	μs
Data Input Setup Time (t_{ds})		80	50		ns
Data Input Hold Time (t_{dh})		20	0		ns
Data Output Propagation Delay From ϕ					
Delay to HIGH Level (t_{pdH})	See ac test circuit		150	300	ns
Delay to LOW Level (t_{pdL})			150	300	ns

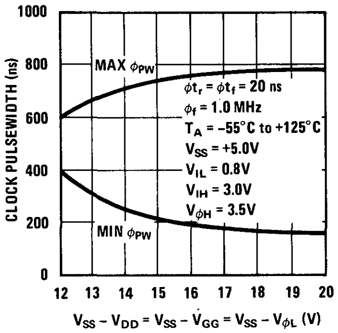
Note 1: Capacitance values are guaranteed by periodic testing.

guaranteed performance characteristics

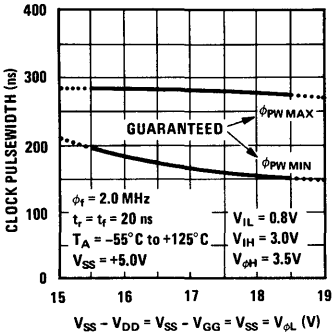
Data Input Voltage vs Supply



1.0 MHz Operating Curve

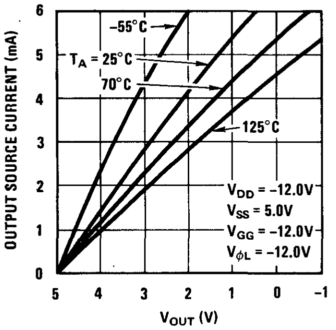


2.0 MHz Operating Curve

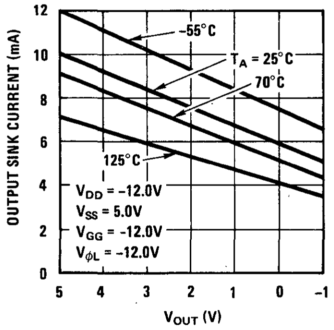


typical performance characteristics

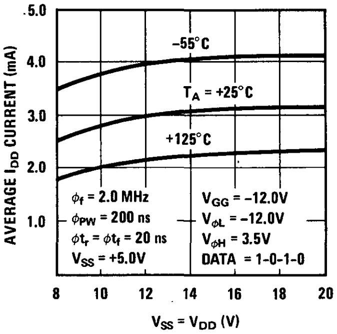
Data Output Source Current vs Voltage



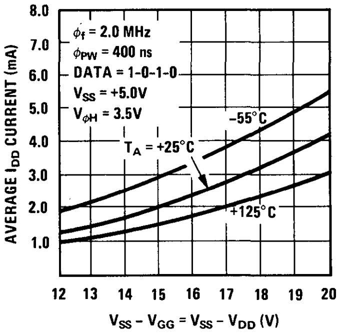
Output Sink Current vs Voltage



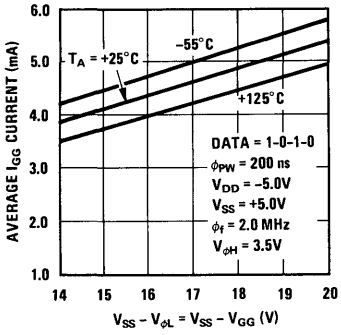
Power Supply Current



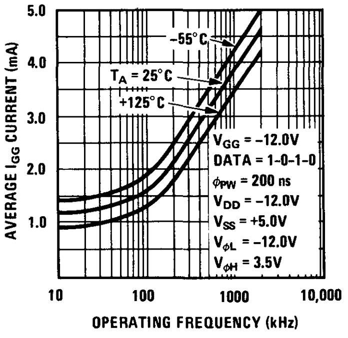
Power Supply Current vs Voltage



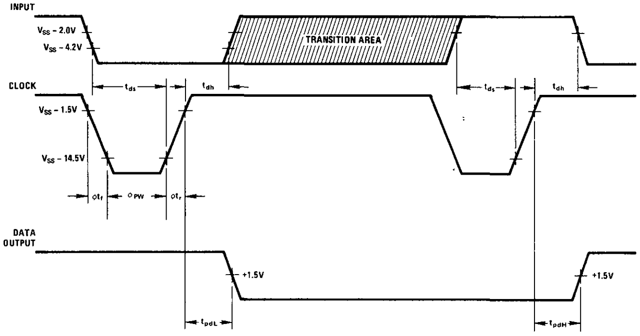
Power Supply Current



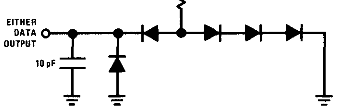
Power Supply Current vs Operating Frequency



switching time waveforms



ac test circuit



Static Shift Registers

MM4052/MM5052 dual 80 bit static shift register
MM4053/MM5053 dual 100-bit static shift register

general description

The MM4052/MM5052 dual 80-bit and MM4053/MM5053 dual 100-bit static shift registers are monolithic integrated circuits utilizing P channel enhancement mode low threshold technology to achieve direct bipolar compatibility on the inputs and outputs. The devices require only a single phase clock.

features

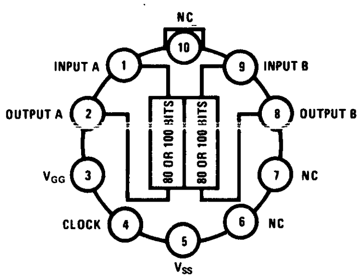
- Bipolar compatibility — +5, −12V operation; No pull-up or pull-down resistors needed
- High frequency operation — 1.6 MHz guarantee
- Single phase clock
- Improved drive capability — push-pull outputs

applications

- Static data buffer
- Serial memory storage
- Printer memory
- Telemetry systems and data sampling

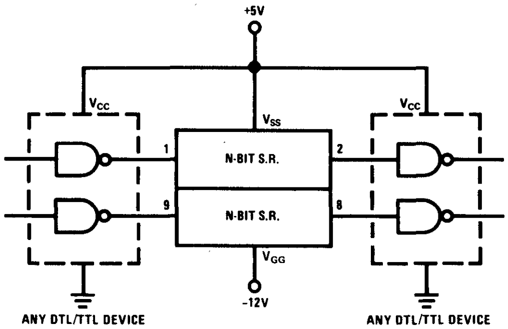
connection diagram

Metal Can Package



TOP VIEW

typical application



absolute maximum ratings

Voltage @ Any Pin	V_{SS} +0.3V to V_{SS} −22V
Operating Temperature Range	
MM4052/MM4053	−55°C to +85°C (Ambient) −55°C to +125°C (Case)
MM5052/MM5053	−25°C to +70°C (Ambient)
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

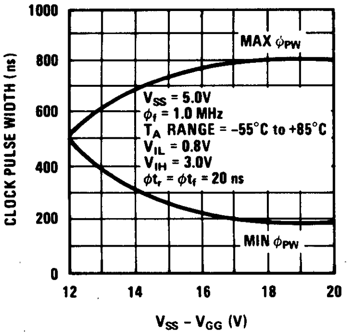
electrical characteristics

T_A within operating temperature range, V_{SS} = +5.0V ±5% and V_{GG} = −12V ±10%, unless otherwise specified.

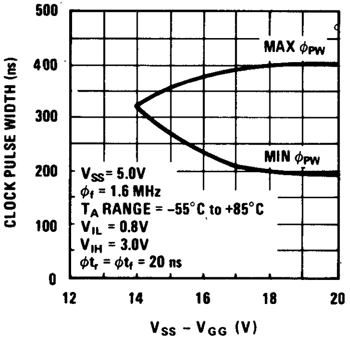
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data Input Levels					
Logical High Level (V_{IH})		V_{SS} − 2.0			V
Logical Low Level (V_{IL})		V_{SS} − 18.5		V_{SS} − 4.2	V
Data Input Leakage	V_{IN} = −20V, T_A = 25°C All other pins GND		.01	0.5	µA
Data Input Capacitance	V_{IN} = 0.0V, f = 1.0 MHz All other pins GND		3.0	5.0	pF
Clock Input Levels					
Logical High Level ($V_{\phi H}$)		V_{SS} − 1.5		V_{SS}	V
Logical Low Level ($V_{\phi L}$)		V_{SS} − 18.5		V_{SS} − 14.5	V
Clock Input Leakage	V_{IN} = −20V, T_A = 25°C All other pins GND			1.0	µA
Clock Input Capacitance	V_{IN} = 0.0V, f = 1.0 MHz All other pins GND		22	28	pF
Data Output Levels					
Logical High Level (V_{OH})	I_{SOURCE} = −500 µA	2.4V	4.8	V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA		−3.0	0.4	V
Logical High Level (V_{OH})	I_{SOURCE} = −10 µA	V_{SS} − 1.0	V_{SS}	V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 10 µA		V_{SS} − 12.0	V_{SS} − 7.0	V
Power Supply Current	T_A = 25°C ϕ_f = 1.6 MHz				
(I_{GG}) MM4052/MM5052	V_{GG} = V_{SS} − 17V $V_{\phi L}$ = V_{SS} − 17V		9.5	12.5	mA
(I_{GG}) MM4053/MM5053			12.0	16.0	mA
Propagation Delays from Clock					
Propagation Delay to a High (t_{pdH})	See waveform		200	300	ns
Propagation Delay to a Low (t_{pdL})	See waveform		200	300	ns
Clock Frequency (ϕ_f)	See operating curves	0		1.6	MHz
Clock Pulse Width (ϕ_{PW})	See operating curves $\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$	0.25		10	µs
Clock Transition Times					
Risetime (ϕt_r)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			5	µs
Falltime (ϕt_f)	$\phi t_f + \phi_{PW} + \phi t_r \leq 10.5\ \mu s$			5	µs
Data Input Setup Time (t_{ds})		80	50		ns
Data Input Hold Time (t_{dh})		20	0		ns

guaranteed performance characteristics

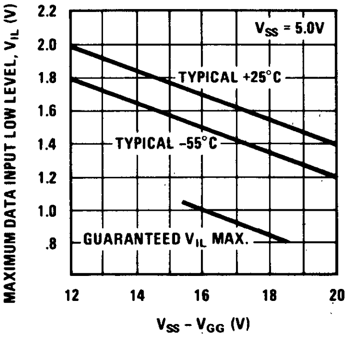
1.0 MHz Operating Curve



1.6 MHz Operating Curve

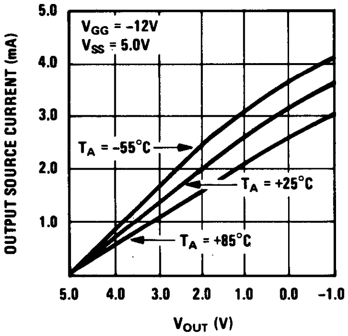


Maximum Data Input Low Level vs Supply Voltage

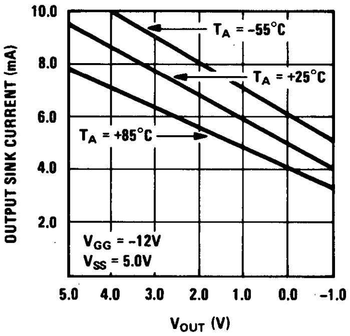


typical performance characteristics

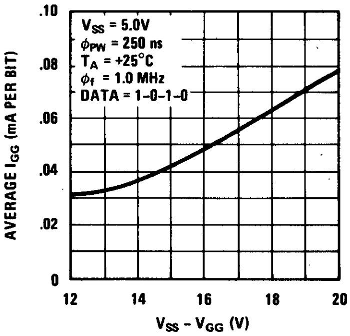
Data Output Source Current vs Data Output Voltage



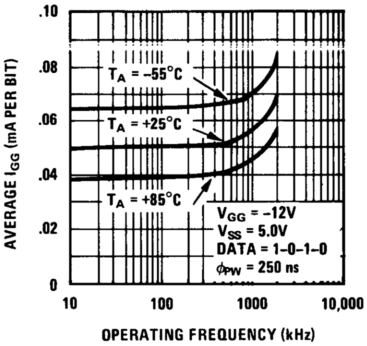
Data Output Sink Current vs Data Output Voltage



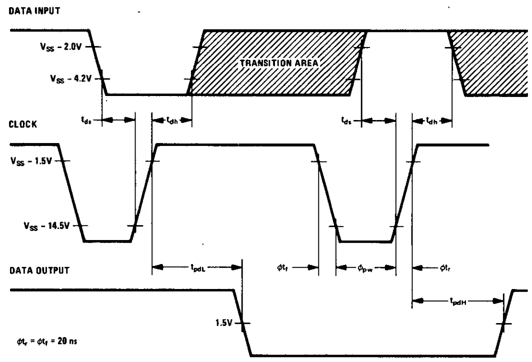
Power Supply Current



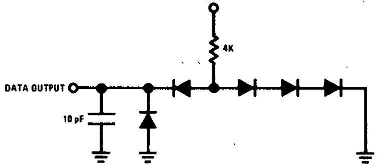
Power Supply Current



switching time waveforms



ac test circuit



Static Shift Registers

MM5054 dual 64/72/80 bit static shift register

general description

The MM5054 dual 80-bit static shift register is a monolithic MOS integrated circuit utilizing silicon gate low threshold technology to achieve complete bipolar compatibility. The device has input and output taps that also provide register lengths of 64 or 72 bits.

The single phase bipolar compatible clock lines may be driven by any conventional DTL or TTL circuit. The registers may be operated as a dual register by connecting the clock lines A and B together, or as two independent registers. Two clock control lines provide independent logical control of the shift register clock lines.

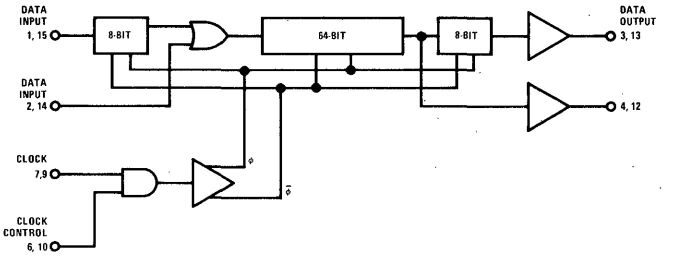
features

■ Complete bipolar compatibility	DTL/TTL input/output and clock line compatibility without additional components
■ Standard supplies	+5V, −12V
■ High freq operation	DC to 3.0 MHz typ
■ Single phase clock	DTL/TTL compatible on-chip clock driver
■ Low clock line capacitance	8 pF max
■ System flexibility	Split clock or common clock operation. Logical control of clock lines
■ Low power dissipation	<600 μW/bit typ

applications

- Teletype data buffers
- Printer memory – 80, 128, 136, 144 bit lengths
- Telemetry and data sampling systems
- Serial memory storage.

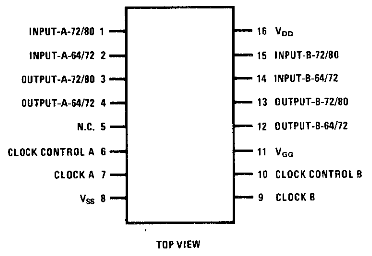
logic and connection diagrams



The unused data inputs and clock controls should be connected to V_{SS} to ensure proper operation.

Logic diagram shows 1/2 of the unit.

Dual-In-Line Package



truth table

CLOCK CONTROL	CLOCK
Low	Inhibited
High	Active

Positive Logic

absolute maximum ratings

Voltage at Any Pin	V_{SS} + 0.3V to V_{SS} − 20.0V
Operating Ambient Temperature Range	−25°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

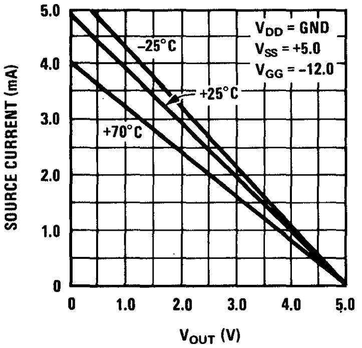
T_A within operating range, V_{GG} = −12V ±10%, V_{DD} = GND, V_{SS} = 5V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Data, Clock Control, and Clock Levels					
Logical High Level (V_{IH})	See Input Level vs V_{GG} Curve	V_{SS} − 2.0		V_{SS} + 0.3	V
Logical Low Level (V_{IL})				V_{SS} − 4.2	V
Input Leakages	V_{IN} = −10V, T_A = 25°C All Other Pins GND			0.5	µA
Data Input Capacitance	V_{IN} = 0.0V, f = 1 MHz All Other Pins GND (Note 1)		4.5	6.0	pF
Clock & Clock Control Capacitance	V_{IN} = 0.0V, f = 1 MHz (Note 1)		6.0	8.0	pF
Data Output Levels	See Figure 1				
Logical High Level (V_{OH})	I_{SOURCE} = −0.5 mA	2.4		V_{SS}	V
Logical Low Level (V_{OL})	I_{SINK} = 1.6 mA		0.15	0.4	V
Power Supply Current	ϕ_f = 2.0 MHz, T_A = 25°C				
(I_{GG} + I_{DD} = I_{SS}) I_{GG}	V_{SS} = 5V, V_{DD} = GND		7.0	10.0	mA
I_{DD}	V_{GG} = −12V		5.0	8.0	mA
Clock Frequency (ϕ_f)	See Operating Curves	DC	3.0	2.2	MHz
Clock Pulsewidth (ϕ_{PW})	See Operating Curves and Figure 1				
Clock Pulsewidth	ϕt_r = ϕt_f = 10 ns	0.25		10	µs
Clock Transition Times					
Clock Risetime (ϕt_r)				500	ns
Clock Falltime (ϕt_f)				500	ns
Clock Control Setup Time (t_{CS})	See Figure 1, ϕt_r = ϕt_f = 10 ns	0			ns
Clock Control Hold Time (t_{ch})	See Figure 1, ϕt_r = ϕt_f = 10 ns	0			ns
Data Input Setup Time (t_{ds})	See Figure 1, ϕt_r = ϕt_f = 10 ns	60	30		ns
Data Input Hold Time (t_{dh})	See Figure 1, ϕt_r = ϕt_f = 10 ns	40	20		ns
Data Output Propagation Delay From Clock	See Figures 1 & 2, ϕt_r = ϕt_f = 10 ns				
Delay to Output High Level (t_{pdH})			200	300	ns
Delay to Output Low Level (t_{pdL})			200	300	ns

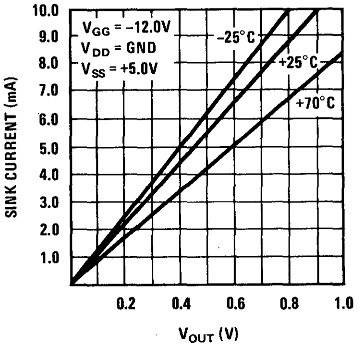
Note 1: Capacitance is guaranteed by periodic testing.

performance characteristics

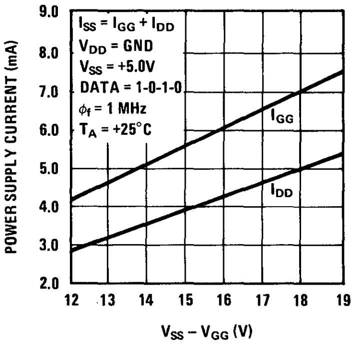
Typical Data Output Source Current vs Data Output Voltage



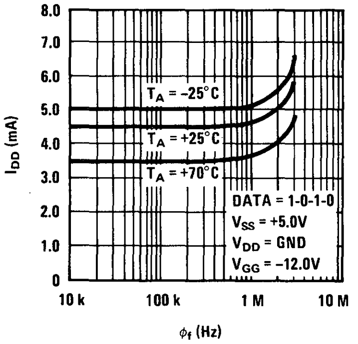
Typical Data Output Sink Current vs Data Output Voltage



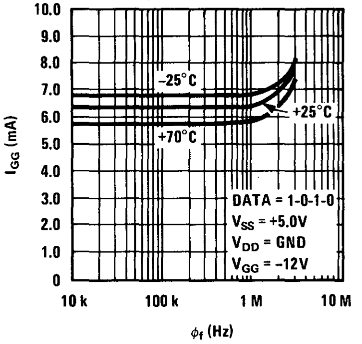
Typical Power Supply Current vs V_{GG}



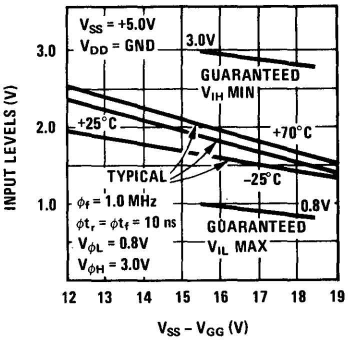
Typical I_{DD} vs Clock Frequency



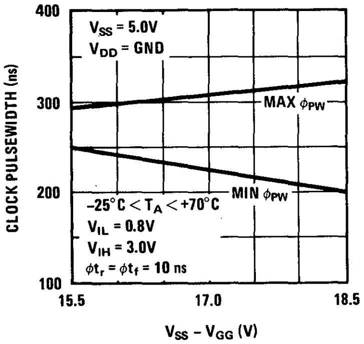
Typical I_{GG} vs Clock Frequency



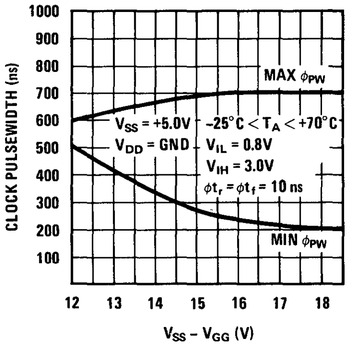
Guaranteed Input Levels vs V_{GG}



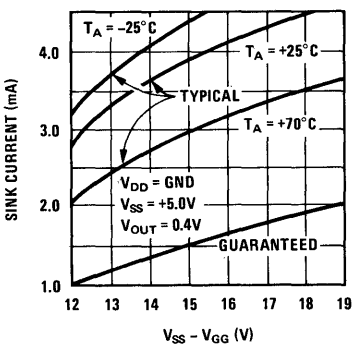
Guaranteed 2.2 MHz Operating Curve



Guaranteed 1.0 MHz Operating Curve



Guaranteed Data Output Sink Current vs V_{GG}



switching waveforms

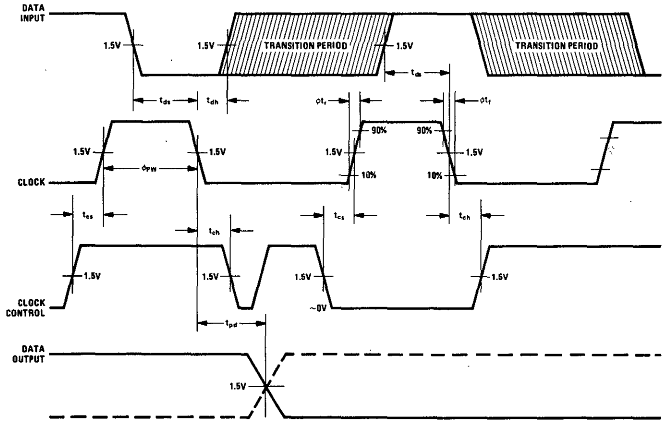


FIGURE 1

test circuit

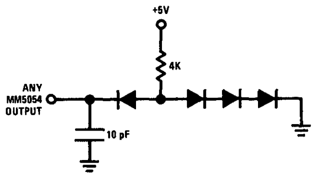


FIGURE 2

MM4203/MM5203 electrically programmable 2048-bit read only memory (pROM)

general description

The MM4203/MM5203 is a 2048-bit static read-only memory which is electrically programmable and uses silicon gate technology to achieve bipolar compatibility. The device is a non-volatile memory organized as a 256-8-bit words or 512-4-bit words. Programming of the memory contents is accomplished by storing a charge in a cell location by programming that location with a 45 volt pulse. Separate output supply lead is provided to reduce internal power dissipation in the output stage (V_{LL}).

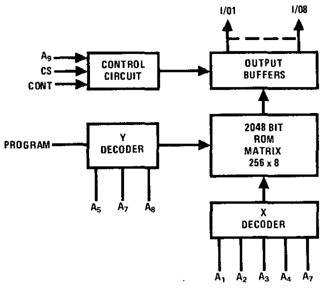
features

- Field programmable
- Bipolar compatibility — +5V, −12V operation
- High speed operation — 1 μs max access time
- Pin compatible with MM5213, MM5231 mask programmable ROMs
- Static operation — no clocks required
- Common data busing (TRI-STATE™ output)
- "Q" quartz lid version erasable with ultra-violet light
- Chip enable output control
- 256 x 8 or 512 x 4 organization

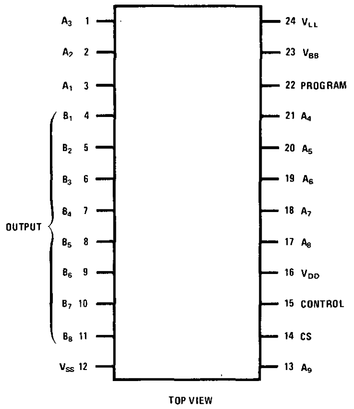
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Micro-programming

block and connection diagrams

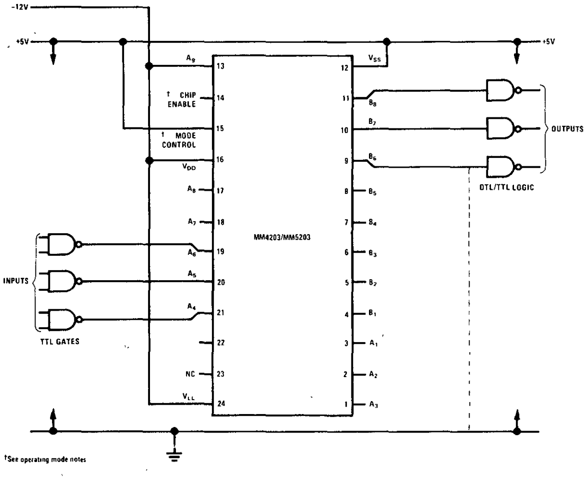


Dual-In-Line Package



typical applications

256 x 8 PROM Showing TTL Interface



†See operating mode notes

Operating Modes

256 x 8 ROM connection (shown)
Mode Control — HIGH
A_9 — LOW
512 x 4 ROM connections
Mode Control — LOW
A_9 — Logic HIGH enables the odd (B_1, B_3..B_7) outputs
— Logic LOW enables the even (B_2, B_4.. B_8) outputs outputs

The outputs are enabled when a logic LOW is applied to the Chip Enable line.

Mode Control should be "hard wired" to V_{DD} (LOW) or V_{SS} (HIGH).

Programming is accomplished in 256 x 8 mode only.

Pin 23 is connected to V_{SS} except when programming when it is connected to V_{BB}.

Program pin is connected to V_{SS} except when programming program pulse is applied.

In the programming mode, data inputs 1–8 are Pins 4–11 respectively. Chip Enable should be disabled (HIGH).

absolute maximum ratings

All Input or Output Voltages with Respect to V_{BB}	+.3 to −20V
Power Dissipation	1W
Operating Temperature Range MM4203	−55°C to 85°C
MM5203	−25°C to 70°C
Storage Temperature Range	−65°C to 125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, $V_{SS} = +5V \pm 5\%$, $V_{DD} = V_{LL} = 12V$, ±5% unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current, I_{L1}	$V_{IN} = 0V$			1	μA
Output Leakage, I_{LO}	$V_{OUT} = 0V$ Output in 3rd State			1	μA
Power Supply Current, I_{DD1}	$T_A = 25°C$		35	55	mA
Input LOW Voltage, V_{IL}				$V_{SS} - 4.0$	V
Input HIGH Voltage, V_{IH}		$V_{SS} - 2.0$			V
Output LOW Voltage, V_{OL}	1.6 mA sink			.40	V
Output HIGH Voltage, V_{OH}	100 μA source	2.4			V
Data Hold Time, T_{OH}	(Min Access Time) Figures 1 & 2			100	ns
Access Time, T_{ACC}	$T_A = 25°C$ Figures 1 & 2		.700	1	μs
Chip Enable Time, T_{CE}	Figures 1 & 3			500	ns
Chip Disable Time, T_{CD}	Figures 1 & 3			500	ns
Allowable Chip Select Delay, t_{CS}	Figures 1 & 2 Allowable delay in selecting chip after change of address without affecting access time.			100	ns
Input Capacitance, C_{IN}	$V_{IN} = V_{SS}$ f = 1.0 MHz Guaranteed by design (Note 2)		8	15	pF
Output Capacitance, C_{OUT}	$V_{OUT} = V_{SS}$ (Chip deselected)		8	15	pF

operating characteristics for programming operations

$T_A = 25°C$, $V_{SS} = 0V$, $V_{BB} = +12V \pm 10\%$ unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Address and Data Input Load Current, I_{L12P}	$V_{IN} = -40V$	10			mA
Program V_{LL} Load Current, I_{L12P}	$V_{IN} = -50V$	10			mA
V_{BB} Supply Load Current, I_{BB}				100	μA
Peak I_{DD} Supply Load Current, I_{DDP} (Note 3)	$V_{LL} = V_{DD} = V_{program} = -50V$		750		mA
Input High Voltage, V_{ILP}				+.3	V
Pulsed Data Input Low Voltage, V_{IH1P}		−48		−40	V
Address Input Low Voltage, V_{IH2P}		−48		−40	V
Pulsed Input Low Voltage: V_{LL}, V_{DD}, and Program, V_{IH3P}		−50		−48	V

Note 1: During programming, data is always applied in the 256 x 8 mode, regardless of the logic state of A_9 and mode control.

Note 2: Capacitances are not tested on a production basis but are periodically sampled.

Note 3: I_{DDP} flows only during program period $t_{\phi PWP}$. Average power supply current I_{DDP} is typically 15 mA at 2% duty cycle.

Note 4: Maximum duty cycle of $t_{\phi PW}$ should not be greater than 2% of cycle time so that power dissipation is minimized. To guarantee long term memory retention the program cycle should be repeated five times with $t_{\phi PW}$ = 20 ms or the equivalent thereof, i.e. 10 cycles of $t_{\phi PW}$ = 10 ms.

operating characteristics (con't) for programming operations

(see Figure 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Duty Cycle				2	%
Program Pulse Width, $t_{\phi PW}$ (Note 4)	$V_{DD} = V_{LL} = V_{program} = -48V$			20	ms
Data Set Up Time, t_{DW}		1			μs
Data Hold Time, t_{DH}		1			μs
Pulsed V_{LL} and V_{DD} Supply Overlap, t_{VD}				3	ms

Operation of the MM4203/MM5203 in Program Mode

Initially, all 2048 bits of the MM4203/MM5203 are in the HIGH state. Information is introduced by selectively programming LOWS in the proper bit locations.

Word address selection is done by the same decoding circuitry used in the Read mode. The eight output terminals are used as data inputs to determine the information pattern in the eight bits of each word. A LOW data input level (–50V) will leave a HIGH and a HIGH data input level will allow programming of a LOW. All eight bits of one word are programmed simultaneously by setting the desired bit information patterns on the data input terminals. The duty cycle of the Program pulse (amplitude and width as specified on page 4). should be limited to 2%. The address should be applied for at least 1 μs before application of the Program pulse.

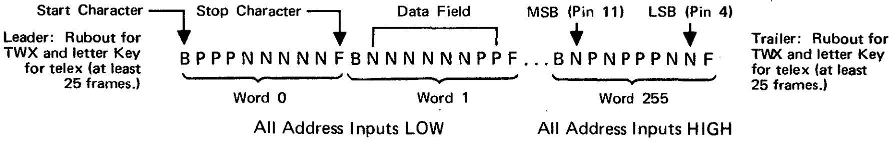
During programming, all inputs are pulsed signals.

MODE	DATA AND ADDRESS LINES LOGIC "1"	 LOGIC "0"	V_{SS}	V_{BB}	V_{DD}	PROGRAM
Read (Data Out)	V_{SS} - 2.0	V_{SS} - 4.0	+5	+5	-12	+5
Program (Data In)	V_{SS} -2.0	V_{SS} - 40 (Pulse)	GND	+12	-48 (Pulse)	-48 (Pulse)

Tape Format

The custom patterns may be sent in on a Telex or submitted as a paper tape in a 7 bit ASCII code from model 33 teletype or TWX. The paper tape should be as the following example:

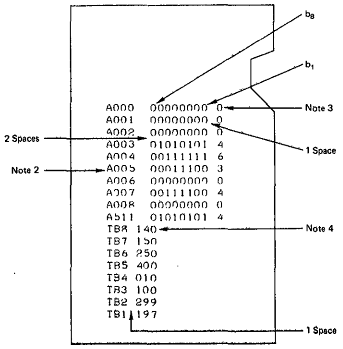
A programmer specifically designed for the MM4203/MM5203 is available from: Spectrum Dynamics, Inc., 2300 East Oakland Park Boulevard, Fort Lauderdale, Florida 33306.



An output HIGH corresponds to a P on the paper tape; an output LOW corresponds to an N.

During programming, word 0 will cause –40V to be applied to all eight address inputs and word 255_{10} would cause 0 volts to be applied to all eight address inputs.

punch tape format



```
A000  00000000 0
A001  00000000 0
A002  00000000 0
A003  01010101 4
A004  00111111 6
A005  00011100 3
A006  00000000 0
A007  00111100 4
A008  00000000 0
A511  01010101 4
TB8 140
TB7 150
TB6 250
TB5 400
TB4 010
TB3 100
TB2 299
TB1 197
```

Note 1: The code is a 7 bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1's" bits in the output word.

Note 4: The total number of "1's" bits in each output column or bit position.

Note 5: Specify whether tape is positive true or negative true logic. Negative true is always assumed when not specified.

The tape would print out as shown for the 256 x 8 code.

access time diagrams

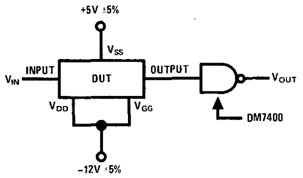


Figure 1

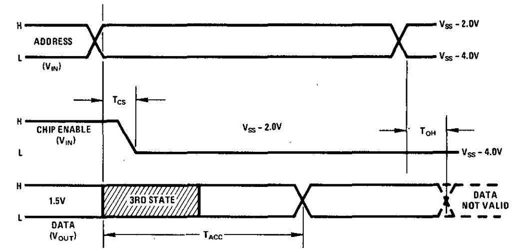


Figure 2

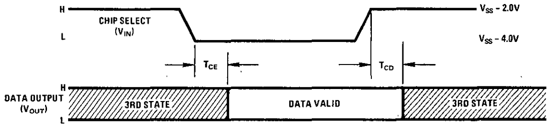


Figure 3

program waveforms

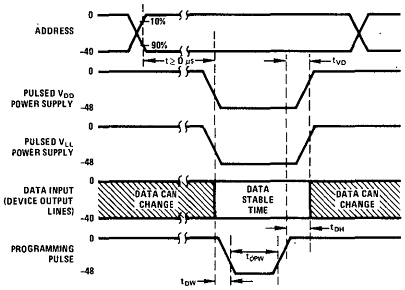


Figure 4

Conditions of Test:

Address and Data Input Pulse Amplitudes: 0 to −40V, Input pulse rise and fall times ≤250 ns V_{LL}, V_{DD}, and Program Input pulse Amplitudes: 0 to −48V.

MM4210/MM5210 1024-bit read only memory

general description

The MM4210/MM5210 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold technology. The device is a non-volatile memory organized as 256-4 bit words. Programming of the memory contents is accomplished by changing one mask during device fabrication. Customer programs may be supplied in a tape, card, or pattern selection format.

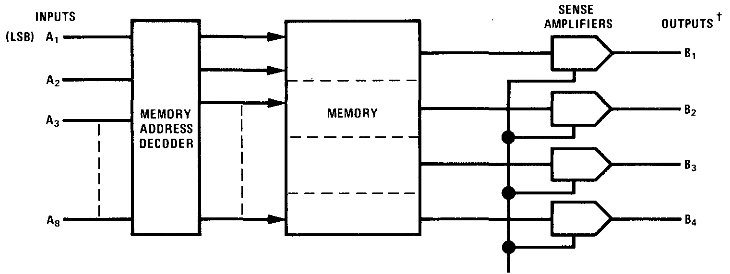
features

- Bipolar compatibility
- High speed operation 500 ns typ
- Static operation no clocks required
- Common data busing output wire AND capability
- Chip enable output control.

applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Micro-programming.

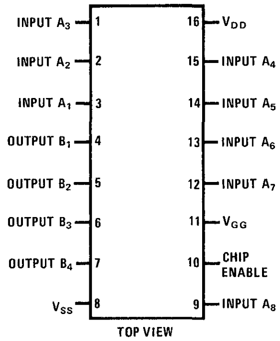
block and connection diagrams



*The output is Enabled by applying a logic "1" to the Chip Enable line.

†The outputs are connected to V_{DD} through an internal MOS resistor when Disabled.

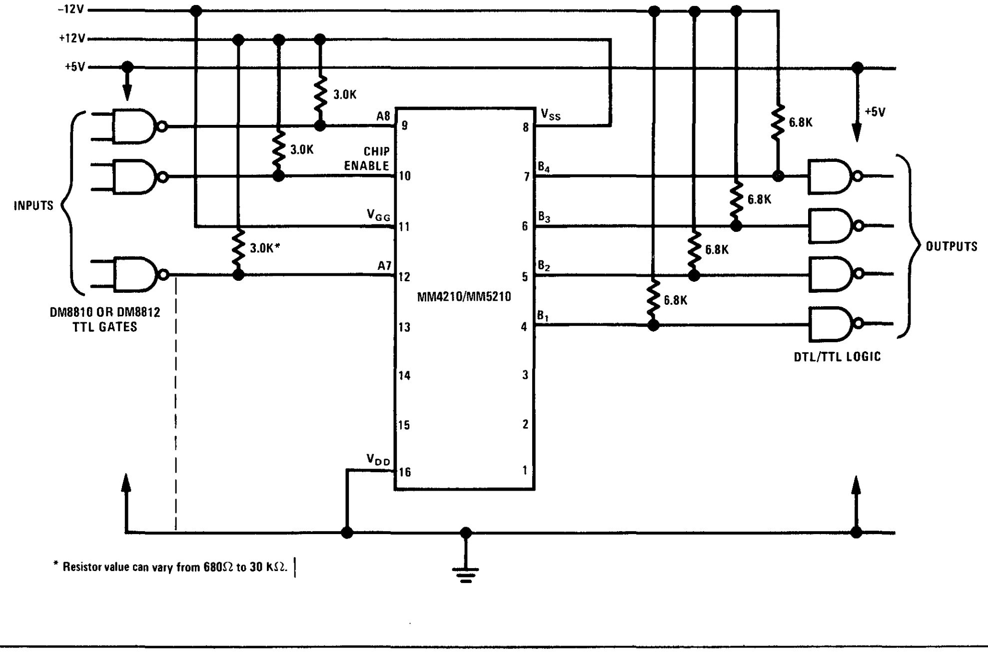
Dual-In-Line Package



TOP VIEW

typical application

256 x 4 Bit ROM Showing TTL Interface



* Resistor value can vary from 680Ω to 30 KΩ.

absolute maximum ratings

V_{GG} Supply Voltage	$V_{SS}-30V$
V_{DD} Supply Voltage	$V_{SS}-15V$
Input Voltage	$(V_{SS} -20)V < V_{IN} < (V_{SS} +0.3)$
Storage Temperature	-65°C to +150°C
Operating Temperature MM4210	-55°C to +125°C
MM5210	-25°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, $V_{SS} = +12V \pm 5\%$ and $V_{GG} = -12V \pm 5\%$, unless otherwise specified.

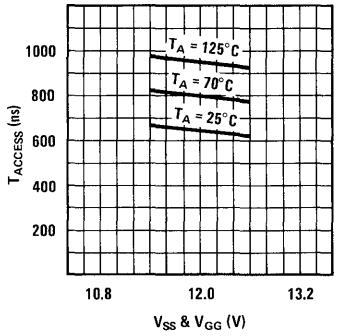
PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	1 MΩ to GND Load (Note 1)			V_{SS} -9.0	V
Logical "0"		V_{SS} -1.0			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate Input	+2.4			V
Input Voltage Levels					
Logical "1"				V_{SS} -8.0	V
Logical "0"		V_{SS} -2.0			V
Power Supply Current	T_A = 25°C				
V_{SS}			19	25	mA
V_{GG} (Note 1)				1	μA
Input Leakage	$V_{IN} = V_{SS} - 12V$			1	μA
Input Capacitance	f = 1.0 MHz V_{IN} = 0V		5		pF
Access Time (Notes 2, 3)	T_A = 25°C				
T_{ACCESS}	(See Timing Diagram) $V_{SS} = +12V$ $V_{GG} = -12V$	150	500	650	ns
Output AND Connection	MOS Load			3	
	TTL Load			8	

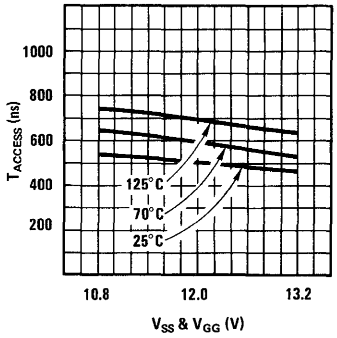
Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

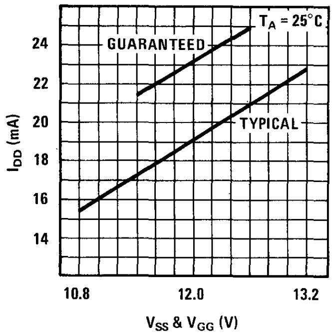
Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.)

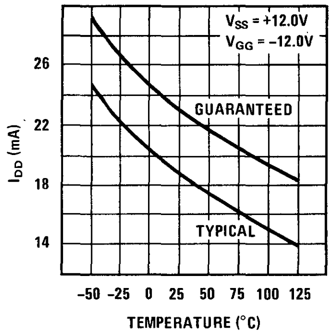
Note 3: The access time in the TTL load configuration follows the equation: T_{ACCESS} = the specified time + (N–1) (50) ns where N = number of AND connections. The number of AND ties in the MOS load configuration can be increased at the expense of MOS "0" level.

performance characteristics

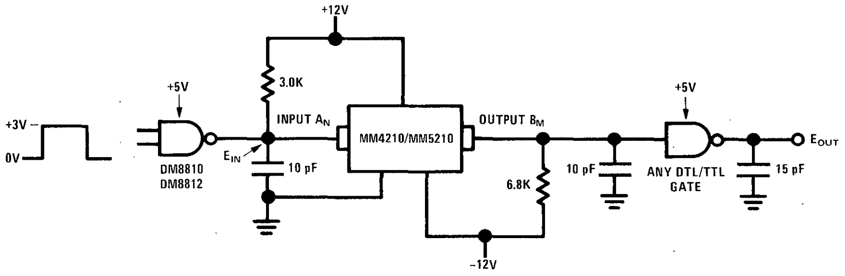

Guaranteed Access Time vs Supply Voltages

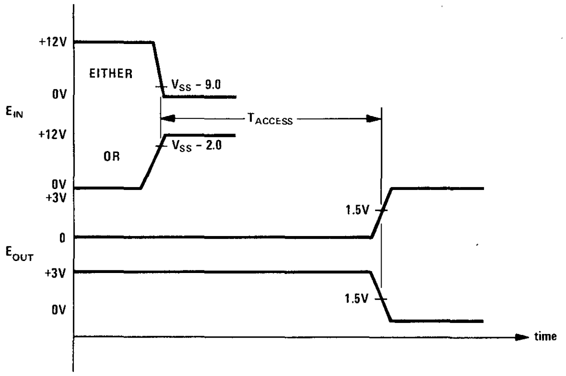

Typical Access Time vs Supply Voltages


Power Supply Current vs Voltage


Power Supply Current vs Temperature

timing diagram/address time





MOS ROM program format

The memory contents for individual requirements must be submitted on a tape or card format as shown below. An 8-1/2" X 11" size pattern selection form is also acceptable. For copies of the MM4210/MM5210 selection form, write or call any National sales office or National, Santa Clara.

Punched Paper Tape or Cards. (See Note 5.)

COLUMN NO.													
1	2	3	4	5	6	7	8	9	10	11	12	13	14
						B4	B3	B2	B1				
A	0	0	0	Space Code	Space Code	1	0	1	0	Space Code	2	Carriage Return	Line Feed
A	0	0	1			1	1	0	0		2		
A	0	0	2			0	0	1	0		1		
|	|	|	|										
|	|	|	|										
|	|	|	|										
|	|	|	|										
|	|	|	|										
A	2	5	5			1	1	0	0		2		
T	B	4	Space Code	0	0	8	(Note 4)				(Note 3)		
T	B	3		1	7	1							
T	B	2		1	6	2							
T	B	1		0	3	0							

Note 1: The code is a 7 bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1's" bits in the output word.

Note 4: The total number of "1's" bits in each output column or bit position.

Note 5: Program one address per card. All columns beyond those specified may be used by the customer.

ROMs

MM4211/MM5211 1024-bit read only memory

general description

The MM4211/MM5211 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold technology. The device is a non-volatile memory organized as 256-4 bit words. Programming of the memory contents is accomplished by changing one mask during device fabrication.

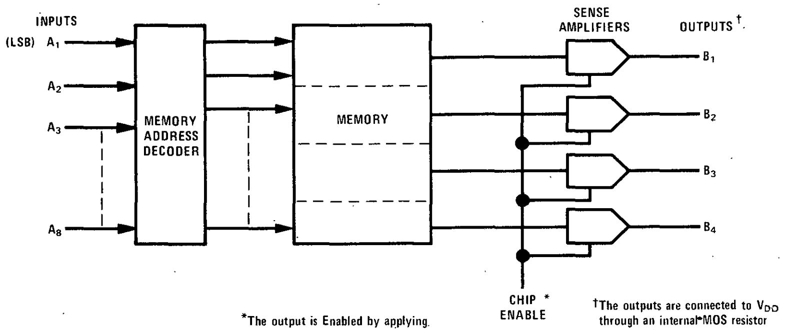
features

■ Bipolar compatibility	+5V, −12V operation
■ High speed operation	< 700 ns typ
■ Static operation	no clocks required
■ Common data busing	output wire AND capability
■ Chip enable output control	

applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Micro-programming

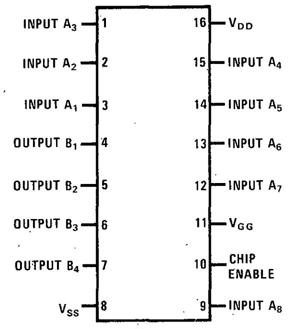
block and connection diagrams



*The output is Enabled by applying a Logic "1" to the Chip Enable line.

†The outputs are connected to V_{DD} through an internal MOS resistor when Disabled.

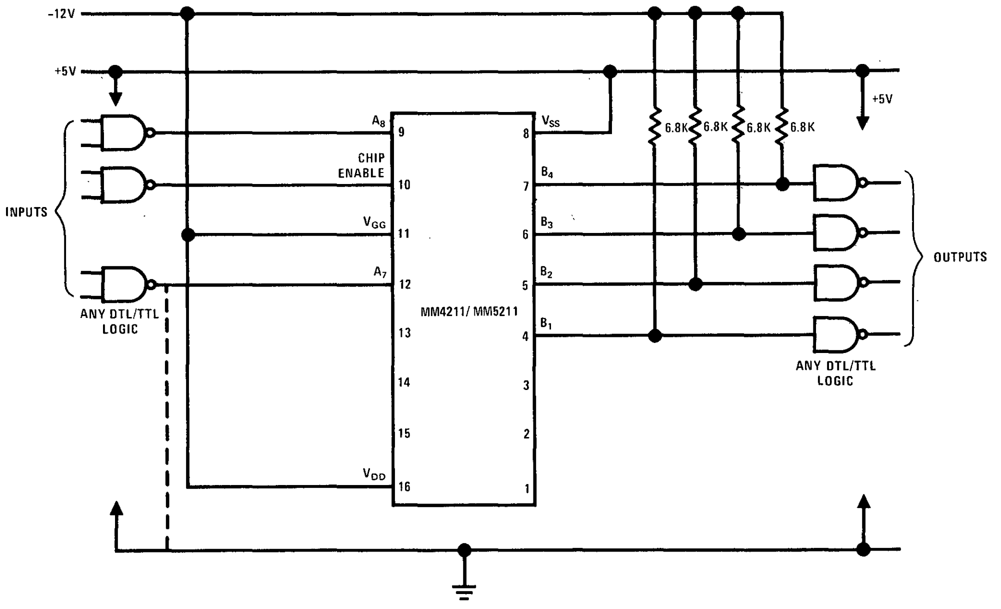
Dual-In-Line Package



TOP VIEW

typical application

256 x 4 Bit ROM Showing TTL Interface



absolute maximum ratings

V_{GG} Supply Voltage	V_{SS} - 20V
V_{DD} Supply Voltage	V_{SS} - 20V
Input Voltage	$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature	-65°C to +150°C
Operating Temperature MM4211	-55°C to +125°C
MM5211	-25°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5V ±5%, $V_{GG} = V_{DD}$ = −12V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to TTL					
Logical "1"	6.8K ±5% to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	+2.4			V
Output Current Capability					
Logical "0"	V_{OUT} = 2.4V	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} - 4.2	V
Logical "0"		V_{SS} - 2.0			V
Power Supply Current	T_A = 25°C				
I_{DD}	V_{SS} = +5V		6.5	12.0	mA
I_{GG} (Note 1)	$V_{GG} = V_{DD}$ = −12V			1	µA
Input Leakage	$V_{IN} = V_{SS}$ - 12V			1	µA
Input Capacitance	f = 1.0 MHz, V_{IN} = 0V		5		pF
V_{GG} Capacitance	f = 1.0 MHz, V_{IN} = 0V		15	25	pF
Address Time (Note 2)	See Timing Diagram				
T_{ACCESS}	T_A = 25°C, V_{SS} = 5V $V_{GG} = V_{DD}$ = −12V		700	950	ns
Output AND Connection (Note 3)	6.8K ±5% to V_{GG} Plus One Standard Series 54/74 Gate			8	

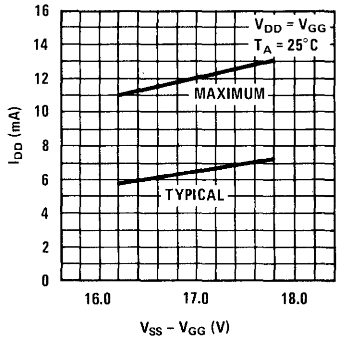
Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.) See curves for guaranteed limit over temperature.

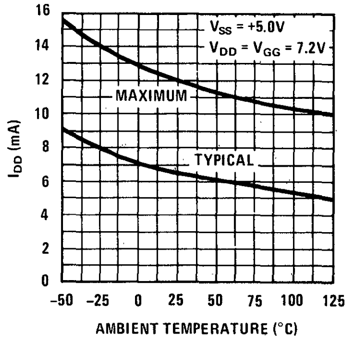
Note 3: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N −1) (50) ns
Where N = Number of AND connections.

performance characteristics

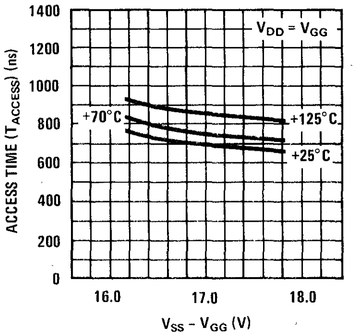
Power Supply Current vs Power Supply Voltages



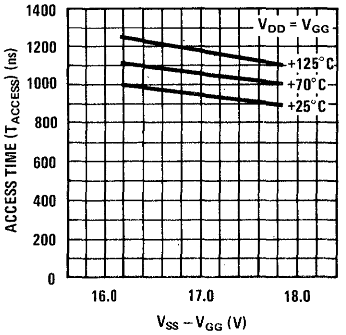
Power Supply Current vs Ambient Temperature



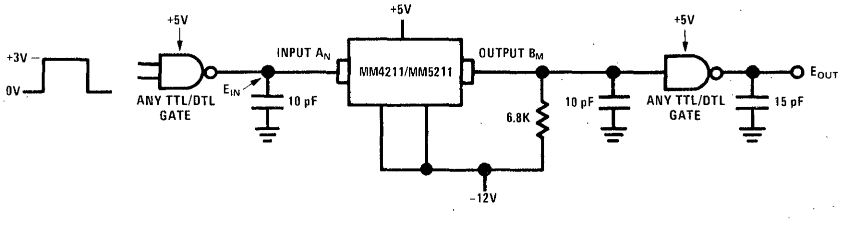
Typical Access Time vs Power Supply Voltages

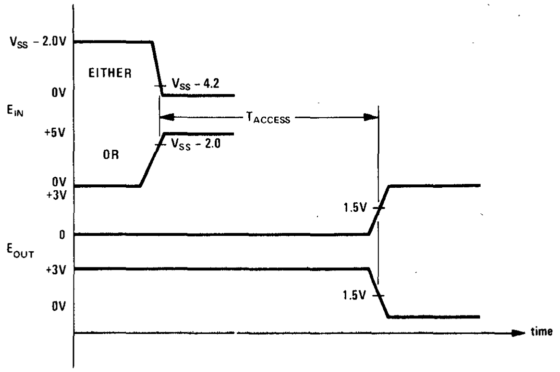


Guaranteed Access Time vs Power Supply Voltages



timing diagram/address time





MOS ROM program format

The memory contents for individual requirements must be submitted on a tape or card format as shown below. An 8-1/2" x 11" size pattern selection form is also acceptable. For copies of the MM4211/MM5211 selection form, write or call any National sales office or National, Santa Clara.

Punched Paper Tape or Cards. (See Note 5.)

COLUMN NO.													
1	2	3	4	5	6	7	8	9	10	11	12	13	14
						B4	B3	B2	B1				
A	0	0	0	Space Code	Space Code	1	0	1	0	Space Code	2	Carriage Return	Line Feed
A	0	0	1			1	1	0	0		2		
A	0	0	2			0	0	1	0		1		
|	|	|	|										
|	|	|	|										
|	|	|	|										
|	|	|	|										
|	|	|	|										
A	2	5	5			1	1	0	0		2		
T	B	4	Space Code	0	0	8	(Note 4)				(Note 3)		
T	B	3		1	7	1							
T	B	2		1	6	2							
T	B	1		0	3	0							

Note 1: The code is a 7 bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1's" bits in the output word.

Note 4: The total number of "1's" bits in each output column or bit position.

Note 5: Program one address per card. All columns beyond those specified may be used by the customer.

MM4220/MM5220 1024-bit read only memory

general description

The MM4220/MM5220 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as 128-8-bit words or 256-4-bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication. Customer programs may be supplied in a tape, card, or pattern selection format.

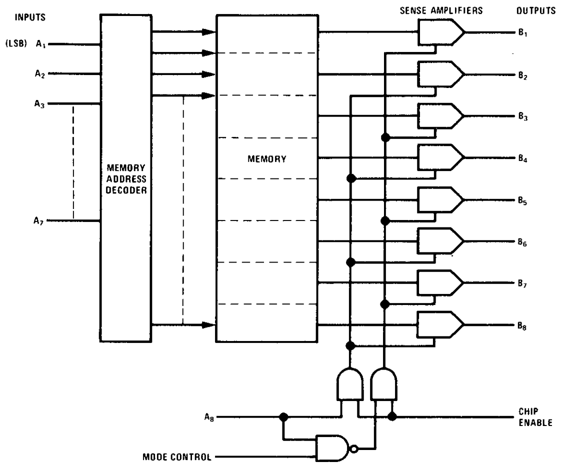
features

■ Bipolar compatibility	
■ High speed operation	500 ns typ
■ Static operation	no clocks required
■ Common data busing	output wire AND capability
■ Chip enable output control.	

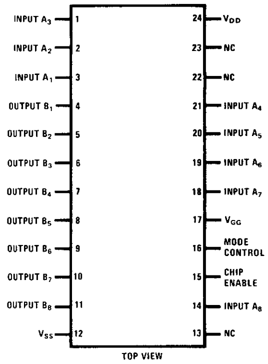
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Micro-programming.

block and connection diagrams

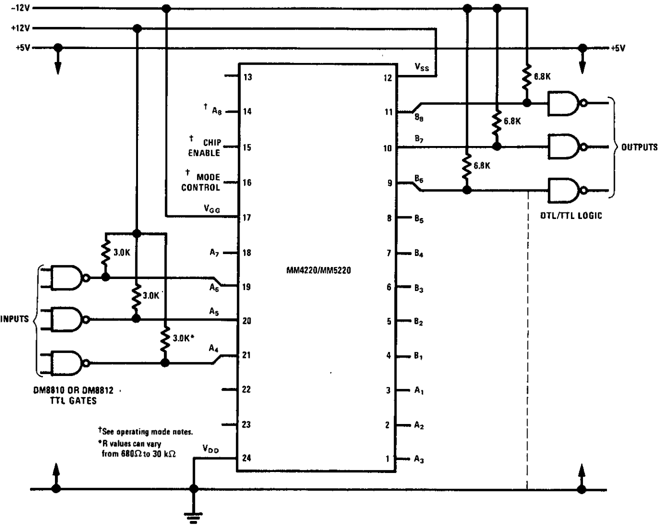


Dual-In-Line Package



typical application

128-8 Bit ROM Showing TTL Interface



†See operating mode notes.

*R values can vary from 680Ω to 30 kΩ

Operating Modes

128x8 ROM connection
Mode Control – Logic "0"
A_8 – Logic "1"

256x4 ROM connection
Mode Control – Logic "1"
A_8 – Logic "0" Enables the odd ($B_1 \ldots B_7$) outputs
– Logic "1" Enables the even ($B_2 \ldots B_8$) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

The outputs are connected to V_{DD} through an internal MOS resistor when "Disabled."

absolute maximum ratings

V_{GG} Supply Voltage	V_{SS}−30V
V_{DD} Supply Voltage	V_{SS}−15V
Input Voltage	$(V_{SS}\ -20)V < V_{IN} < (V_{SS}\ +0.3)V$
Storage Temperature	-65°C to +150°C
Operating Temperature MM4220	-55°C to +125°C
MM5220	-25°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +12V ±5% and V_{GG} = −12V ±5%, unless otherwise specified.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	1 MΩ to GND Load (Note 1)			V_{SS} -9.0	V
Logical "0"		V_{SS} -1.0			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate Input	+2.4			V
Input Voltage Levels					
Logical "1"				V_{SS} -8.0	V
Logical "0"		V_{SS} -2.0			V
Power Supply Current	T_A = 25°C				
V_{SS}			19	25	mA
V_{GG} (Note 1)				1	µA
Input Leakage	V_{IN} = V_{SS} -12V			1	µA
Input Capacitance	f = 1.0 MHz V_{IN} = 0V		5		pF
Access Time (Notes 2, 3)	T_A = 25°C				
T_{ACCESS}	(See Timing Diagram)	150	500	650	ns
	V_{SS} = +12V V_{GG} = -12V				
Output AND Connection	MOS Load			3	
	TTL Load			8	

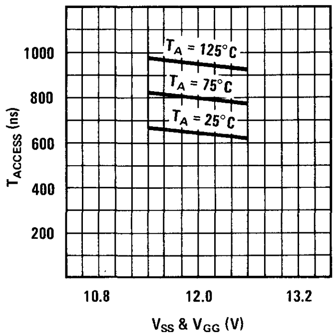
Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.)

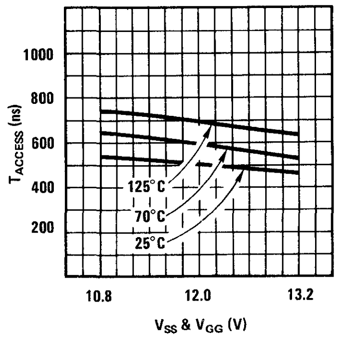
Note 3: The access time in the TTL load configuration follows the equation: T_{ACCESS} = the specified time + (N−1) (50) ns where N = number of AND connections. The number of AND ties in the MOS load configuration can be increased at the expense of MOS "0" level.

performance characteristics

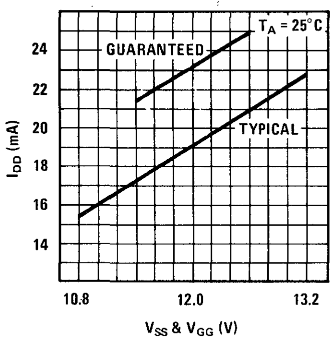
Guaranteed Access Time vs Supply Voltages



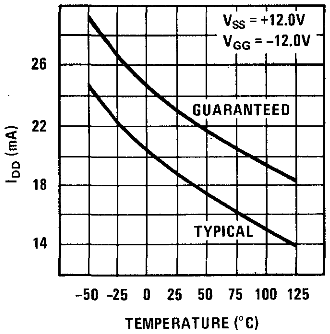
Typical Access Time vs Supply Voltages



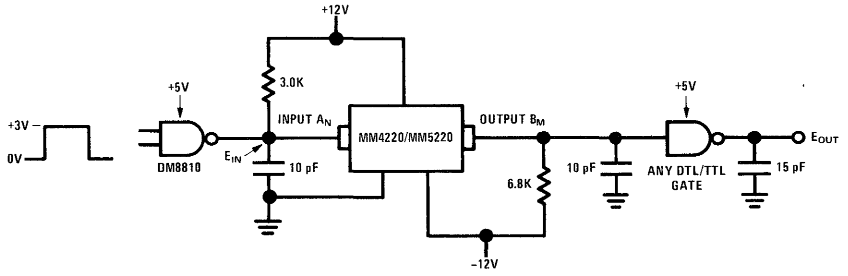
Power Supply Current vs Voltage

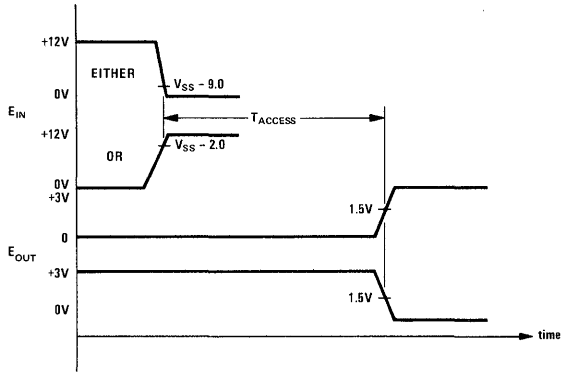


Power Supply Current vs Temperature



timing diagram/address time





MOS ROM program format

The memory contents for individual requirements must be submitted on a tape or card format as shown below. An 8-1/2" X 11" size pattern selection form is also acceptable. For copies of the MM4220/MM5220 selection form, write or call any National sales office or National, Santa Clara.

Punched Paper Tape or Cards. (See Note 5.)

COLUMN NO.																	
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
						B8	B7	B6	B5	B4	B3	B2	B1				
A	0	0	0	Space Code	Space Code	1	0	1	0	1	0	1	0	Space Code	4	Carriage Return	Line Feed
A	0	0	1			1	1	1	1	1	1	0	0		6		
A	0	0	2			1	0	1	1	0	0	1	0		4		
|	|	|	|														
|	|	|	|														
|	|	|	|														
|	|	|	|														
A	1	2	7			0	1	1	1	1	1	0			5 (Note 3)		
T	B	8		0	0	8			(NOTE 4)								
T	B	7		1	7	1											
T	B	6		1	6	2											
|	|	|	Space Code	|	|	|											
|	|	|		|	|	|											
|	|	|		|	|	|											
|	|	|		|	|	|											
T	B	1		0	3	0											

Note 1: The code is a 7 bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1's" bits in the output word.

Note 4: The total number of "1's" bits in each output column or bit position.

Note 5: The punched card format is as shown except that columns 17 and 18 are not necessary. Program one address per card. All columns beyond those specified may be used by the customer.

ROMs

MM4221/MM5221 1024-bit read only memory

general description

The MM4221/MM5221 is a 1024-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as 128-8-bit words or 256-4-bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

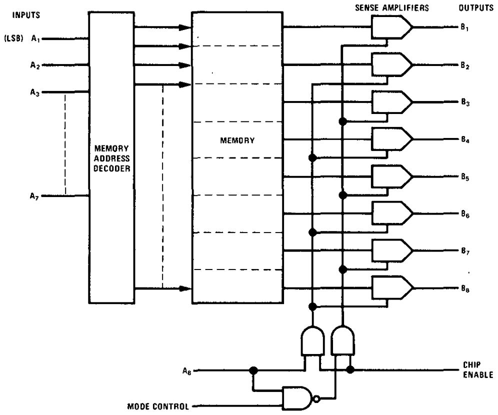
features

■ Bipolar compatibility	+5V, −12V operation
■ High speed operation	<700 ns typ
■ Static operation	no clocks required
■ Common data busing	output wire AND capability
■ Chip enable output control	

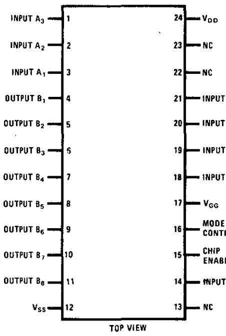
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Micro-programming.

block and connection diagrams

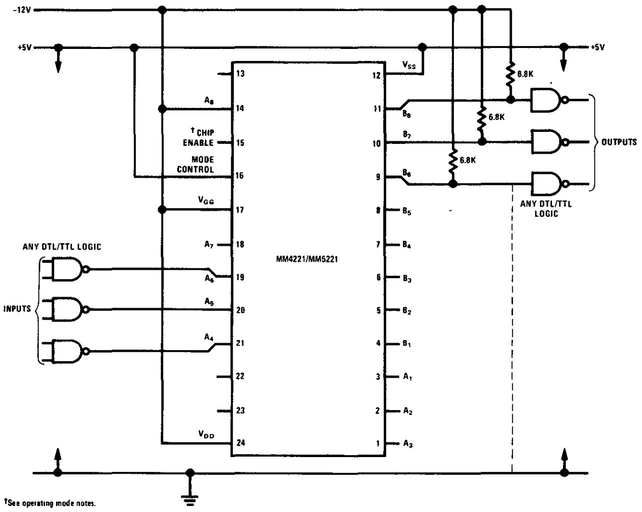


Dual-In-Line Package



typical application

128-8 Bit ROM Showing TTL Interface



†See operating mode notes.

Operating Modes

128x8 ROM connection
Control – Logic "0"
A_8 – Logic "1"

256x4 ROM connection
Control – Logic "1"
A_8 – Enables the odd ($B_1 \ldots B_7$) or even ($B_2 \ldots B_8$) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

The outputs are connected to ground through an internal MOS resistor when "Disabled."

Logic levels are negative true MOS logic.

Mode control should be "hard-wired" to either V_{DD} (logical "1") or V_{SS} (logical "0").

absolute maximum ratings

V_{GG} Supply Voltage	V_{SS} - 20V
V_{DD} Supply Voltage	V_{SS} - 20V
Input Voltage	$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature	-65°C to +150°C
Operating Temperature MM4221	-55°C to +125°C
MM5221	-25°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, $V_{SS} = +5V \pm 5\%$, $V_{GG} = V_{DD} = -12V \pm 5\%$, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels MOS to TTL					
Logical "1"	6.8 kΩ ±5% to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	+2.4			V
Output Current Capability Logical "0"	V_{OUT} = 2.4V	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} - 4.2	V
Logical "0"		V_{SS} - 2.0			V
Power Supply Current	T_A = 25°C				
I_{DD}	V_{SS} = +5V		6.5	12.0	mA
I_{GG} (Note 1)	$V_{GG} = V_{DD}$ = −12V			1	μA
Input Leakage	$V_{IN} = V_{SS}$ - 12V			1	μA
Input Capacitance	f = 1.0 MHz, V_{IN} = 0V		5		pF
V_{GG} Capacitance	f = 1.0 MHz, V_{IN} = 0V		15	25	pF
Address Time (Note 2) T_{ACCESS}	See Timing Diagram T_A = 25°C, V_{SS} = 5V $V_{GG} = V_{DD}$ = −12V		700	950	ns
Output AND Connections (Note 3)	6.8 kΩ ±5% to V_{GG} Plus One Standard Series 54/74 Gate			8	

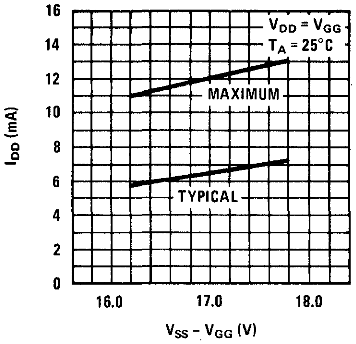
Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 2: Address time is measured from the change of data on any input except mode control or Chip Enable line to the output of a TTL gate. (See Timing Diagram). See curves for guaranteed limit over temperature.

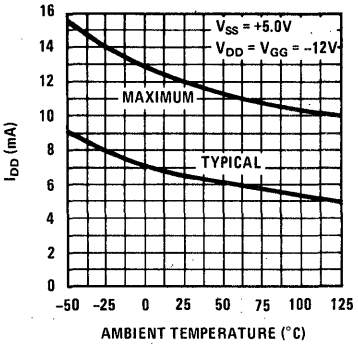
Note 3: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N – 1) (50) ns
Where N = Number of AND connections.

performance characteristics

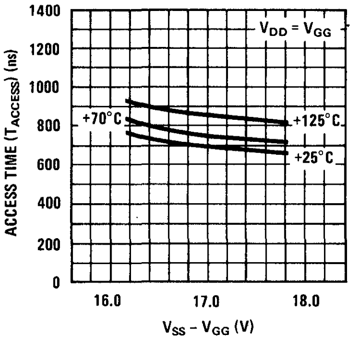
Power Supply Current vs Power Supply Voltages



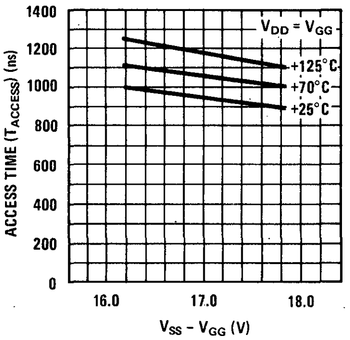
Power Supply Current vs Ambient Temperature



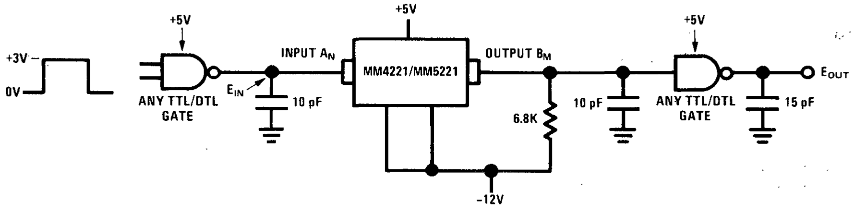
Typical Access Time vs Power Supply Voltages

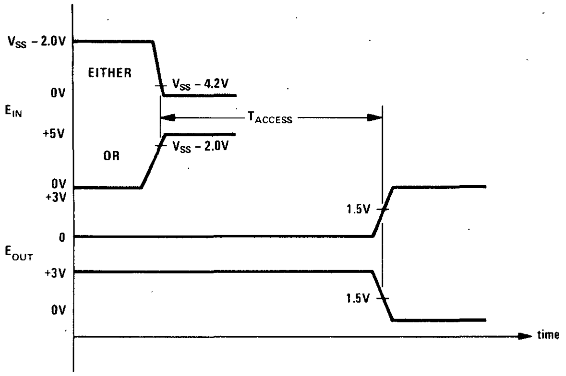


Guaranteed Access Time vs Power Supply Voltages



timing diagram/address time





MOS ROM program format

The memory contents for individual requirements must be submitted on a tape or card format as shown below. An 8-1/2" X 11" size pattern selection form is also acceptable. For copies of the MM4221/MM5221 selection form, write or call any National sales office or National, Santa Clara.

Punched Paper Tape or Cards. (See Note 5.)

COLUMN NO.																	
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
						B8	B7	B6	B5	B4	B3	B2	B1				
A	0	0	0	Space Code	Space Code	1	0	1	0	1	0	1	0	Space Code	4	Carriage Return	Line Feed
A	0	0	1			1	1	1	1	1	1	0	0		6		
A	0	0	2			1	0	1	1	0	0	1	0		4		
|	|	|	|														
|	|	|	|														
|	|	|	|														
|	|	|	|														
A	1	2	7			0	1	1	1	1	1	0			5 (Note 3)		
T	B	8		0	0	8			(NOTE 4)								
T	B	7		1	7	1											
T	B	6		1	6	2											
|	|	|	Space Code	|	|	|											
|	|	|		|	|	|											
|	|	|		|	|	|											
|	|	|		|	|	|											
T	B	1		0	3	0											

Note 1: The code is a 7 bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1's" bits in the output word.

Note 4: The total number of "1's" bits in each output column or bit position.

Note 5: The punched card format is as shown except that columns 17 and 18 are not necessary. Program one address per card. All columns beyond those specified may be used by the customer.

ROMs

MM4230/MM5230 2048-bit read only memory

general description

The MM4230/MM5230 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a nonvolatile memory organized as 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication. Customer programs may be supplied in a tape, card, or pattern selection format.

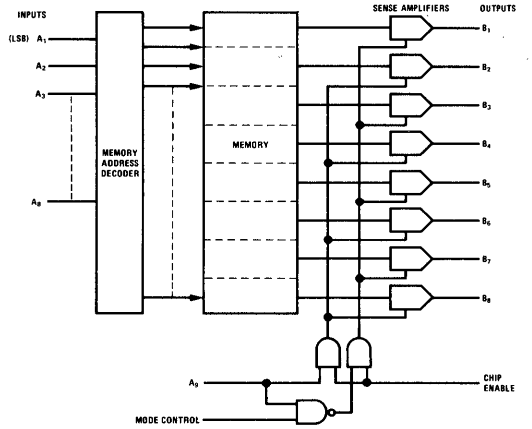
features

- Bipolar compatibility
- High speed operation 500 ns typ
- Static operation no clocks required
- Common data busing output wire AND capability
- Chip enable output control.

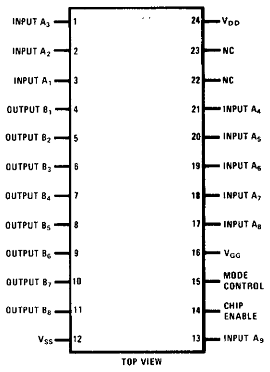
applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generators
- Micro-programming.

block and connection diagrams

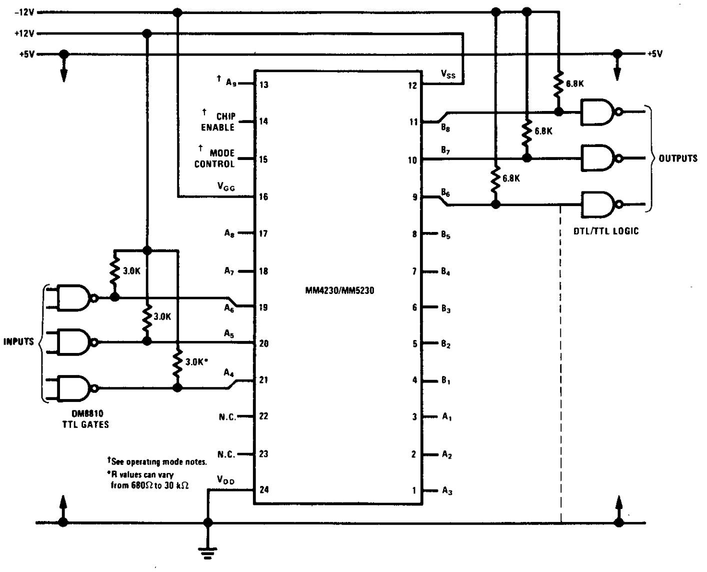


Dual-In-Line Package



typical application

256 x 8 Bit ROM Showing TTL Interface



†See operating mode notes.
*R values can vary from 680Ω to 30 kΩ

Operating Modes

256x8 ROM connection
Mode Control – Logic "0"
A_9 – Logic "1"

512x4 ROM connection
Mode Control – Logic "1"
A_9 – Logic "0" Enables the odd (B_1, B_3 . . . B_9) outputs
– Logic "1" Enables the even (B_2, B_4 . . . B_8) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

The outputs are connected to V_{DD} through an internal MOS resistor when "Disabled."

absolute maximum ratings

V_{GG} Supply Voltage	$V_{SS}-30V$
V_{DD} Supply Voltage	$V_{SS}-15V$
Input Voltage	$(V_{SS}-20)V < V_{IN} < (V_{SS}+0.3)V$
Storage Temperature	-65°C to +150°C
Operating Temperature MM4230	-55°C to +125°C
MM5230	-25°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

T_A within operating temperature range, $V_{SS} = +12V \pm 5\%$ and $V_{GG} = -12V \pm 5\%$, unless otherwise specified.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	1 MΩ to GND Load (Note 1)			V_{SS} -9.0	V
Logical "0"		V_{SS} -1.0			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate Input	+2.4			V
Input Voltage Levels					
Logical "1"				V_{SS} -8.0	V
Logical "0"		V_{SS} -2.0			V
Power Supply Current	T_A = 25°C				
V_{SS}			24	40	mA
V_{GG} (Note 1)				1	μA
Input Leakage	$V_{IN} = V_{SS} -12V$			1	μA
Input Capacitance	f = 1.0 MHz V_{IN} = 0V		5		pF
Access Time (Notes 2, 3)	T_A = 25°C				
T_{ACCESS}	(See Timing Diagram)	150	500	725	ns
	$V_{SS} = +12V$ $V_{GG} = -12V$				
Output AND Connection	MOS Load			3	
	TTL Load			8	

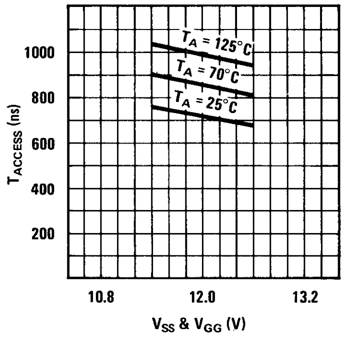
Note 1: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 2: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.)

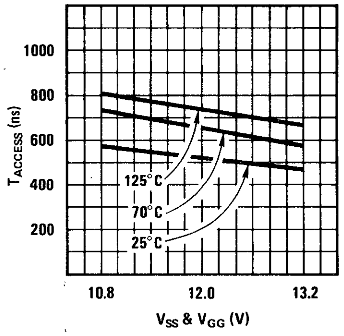
Note 3: The access time in the TTL load configuration follows the equation: T_{ACCESS} = the specified time + (N-1) (50) ns where N = number of AND connections. The number of AND ties in the MOS load configuration can be increased at the expense of MOS "0" level.

performance characteristics

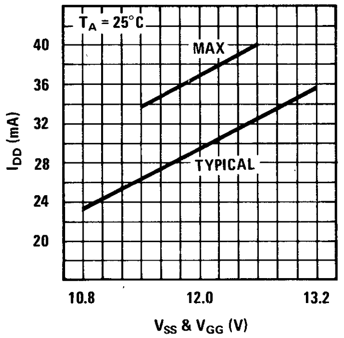
Guaranteed Access Time vs Supply Voltages



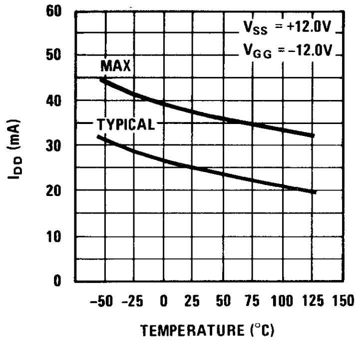
Typical Access Time vs Supply Voltages



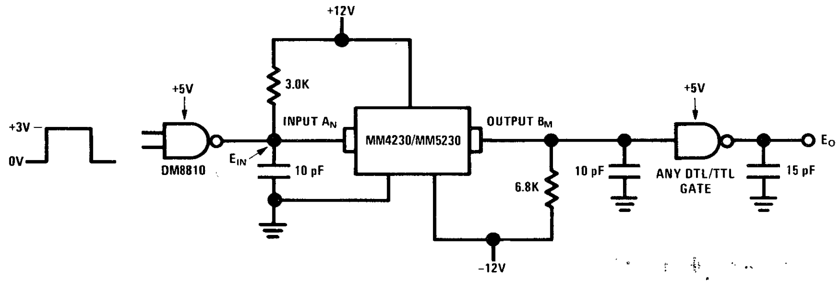
Power Supply Current vs Voltages

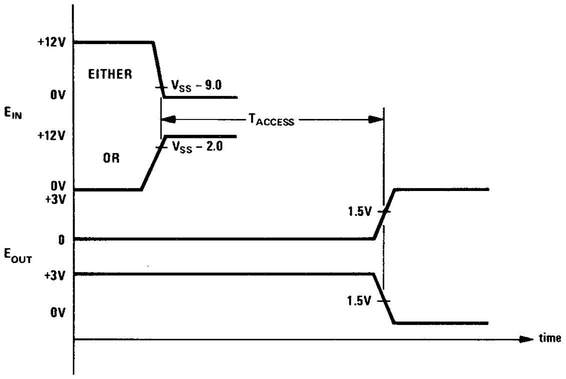


Power Supply Current vs Temperature



timing diagram/address time





MOS ROM program format

The memory contents for individual requirements must be submitted on a tape or card format as shown below. An 8-1/2" X 11" size pattern selection form is also acceptable. For copies of the MM4230/MM5230 selection form, write or call any National sales office or National, Santa Clara.

Punched Paper Tape or Cards. (See Note 5.)

COLUMN NO																	
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
						B8	B7	B6	B5	B4	B3	B2	B1				
A	0	0	0	Space Code	Space Code	1	0	1	0	1	0	1	0	Space Code	4	Carriage Return	Line Feed
A	0	0	1			1	1	1	1	1	1	0	0		6		
A	0	0	2			1	0	1	1	0	0	1	0		4		
|	|	|	|														
|	|	|	|														
|	|	|	|														
|	|	|	|														
A	2	5	5			0	1	1	1	1	1	0			5		
T	B	8		0	0	8			(NOTE 4)						(Note 3)		
T	B	7		1	7	1											
T	B	6		1	6	2											
|	|	|	Space Code	|	|	|											
|	|	|		|	|	|											
|	|	|		|	|	|											
|	|	|		|	|	|											
T	B	1		0	3	0											

Note 1: The code is a 7 bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1's" bits in the output word.

Note 4: The total number of "1's" bits in each output column or bit position.

Note 5: The punched card format is as shown except that columns 17 and 18 are not necessary. Program one address per card. All columns beyond those specified may be used by the customer.

ROMs

MM4231/MM5231 2048-bit read only memory

general description

The MM4231/MM5231 is a 2048-bit static read only memory. It is a P-channel enhancement mode monolithic MOS integrated circuit utilizing low threshold voltage technology. The device is a non-volatile memory organized as a 256-8 bit words or 512-4 bit words. Programming of the memory contents is accomplished by changing one mask during the device fabrication.

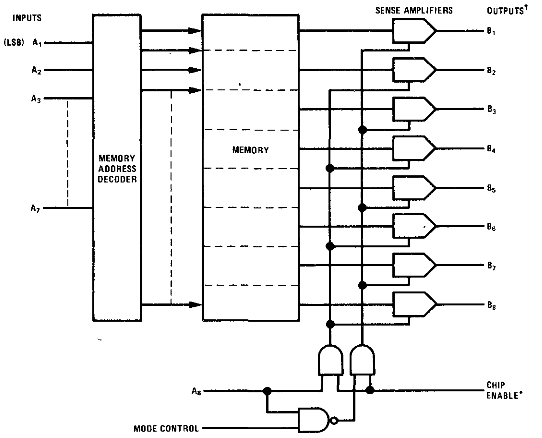
features

■ Bipolar compatibility	+5V, −12V operation
■ High speed operation	640 ns typ.
■ Static operation	No clocks required
■ Common data busing	Output wire AND capability
■ Chip enable output control	

applications

- Code conversion
- Random logic synthesis
- Table look-up
- Character generator
- Micro-programming

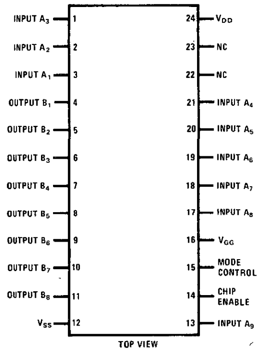
block and connection diagrams



†The outputs are connected to V_{DD} through an internal MOS resistor when Disabled.

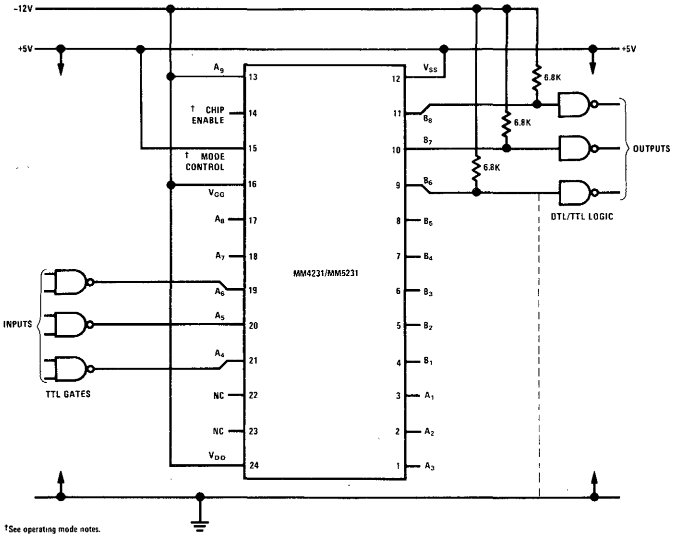
*The output is Enabled by applying a Logic "1" to the Chip Enable line.

Dual-In-Line Package



typical application

256 x 8 Bit ROM Showing TTL Interface



†See operating mode notes.

Operating Modes

256x8 ROM connection (shown)
Mode Control – Logic "0"
A_9 – Logic "1"

512x4 ROM connection
Mode Control – Logic "1"
A_9 – Logic "0" Enables the odd (B_1, B_3 . . . B_9) outputs
– Logic "1" Enables the even (B_2, B_4 . . . B_8) outputs.

The outputs are "Enabled" when a logic "1" is applied to the Chip Enable line.

Logic levels are negative true MOS logic.

Mode Control should be "hard wired" to V_{DD} (Logical "1") or V_{SS} (Logical "0").

absolute maximum ratings

V_{GG} Supply Voltage		V_{SS} - 20V
V_{DD} Supply Voltage		V_{SS} - 20V
Input Voltage		$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature		-65°C to +150°C
Operating Temperature	MM4231	-55°C to +125°C
	MM5231	-25°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to TTL					
Logical "1"	6.8 kΩ ±5% to V_{DD} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	2.4			V
Output Current Capability					
Logical "0"	V_{OUT} = 2.4V	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} - 4.2	V
Logical "0"		V_{SS} - 2.0			V
Power Supply Current	T_A = 25°C				
I_{DD}	V_{SS} = +5V		15	30	mA
I_{GG} (Note 1)	$V_{GG} = V_{DD} = -12V$			1	μA
Input Leakage	V_{IN} = -12V			1	μA
Input Capacitance	f = 1.0 MHz, V_{IN} = 0V		5		pF
V_{GG} Capacitance	f = 1.0 MHz, V_{IN} = 0V		15		pF
Address Time (Note 2)	See Timing Diagram				
T_{ACCESS}	T_A = 25°C V_{SS} = +5.0V $V_{GG} = V_{DD} = -12.0V$		640	950	ns
Output AND Connections (Note 3)	6.8 kΩ ±5% to V_{DD} Plus One Standard Series 54/74 Gate			8	

Note 1: These specifications apply for V_{SS} = +5V ±5%, $V_{GG} = V_{DD} = -12V$, ±5%, and T_A = -55°C to +125°C (MM4231), T_A = -25°C to +70°C (MM5231) unless otherwise specified.

Note 2: The V_{GG} supply may be clocked to reduce device power without affecting access time.

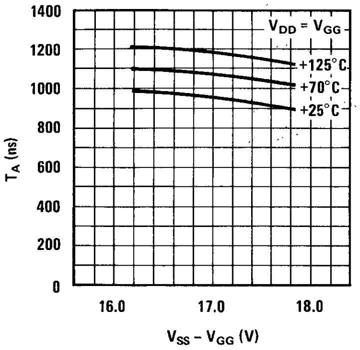
Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram.) See curves for guaranteed limit over temperature.

Note 4: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N - 1) (50) ns.
Where N = Number of AND connections.

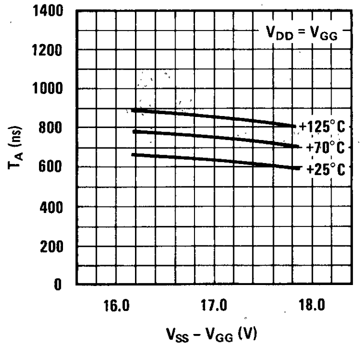
Note 5: Capacitances are measured on a lot sample basis only.

performance characteristics

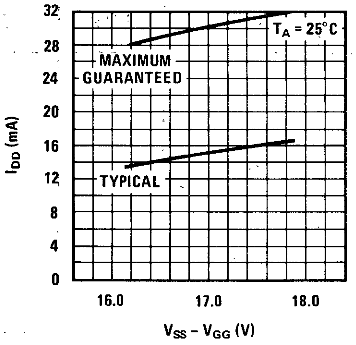
Guaranteed Access Time (T_A) vs Power Supply Voltage



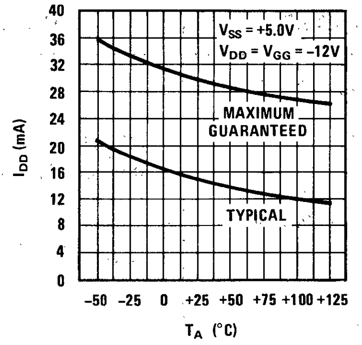
Typical Access Time (T_A) vs Power Supply Voltage



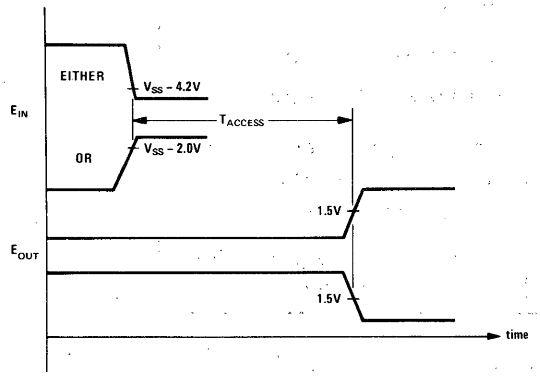
Power Supply Current vs Power Supply Voltage

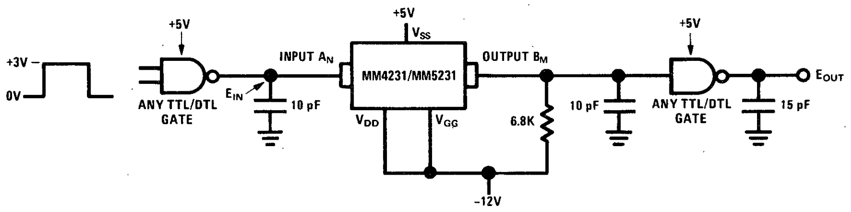


Power Supply Current vs Ambient Temperature



timing diagram/address time





MOS ROM program format

The memory contents for individual requirements must be submitted on a tape or card format as shown below. An 8-1/2" x 11" size pattern selection form is also acceptable. For copies of the MM4231/MM5231 selection form, write or call any National sales office or National, Santa Clara.

Punched Paper Tape or Cards. (See Note 5.)

COLUMN NO.																	
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
						B8	B7	B6	B5	B4	B3	B2	B1				
A	0	0	0	Space Code	Space Code	1	0	1	0	1	0	1	0	Space Code	4	Carriage Return	Line Feed
A	0	0	1			1	1	1	1	1	1	0	0		6		
A	0	0	2			1	0	1	1	0	0	1	0		4		
|	|	|	|														
|	|	|	|														
|	|	|	|														
|	|	|	|														
A	1	2	7			0	1	1	1	1	1	0			5 (Note 3)		
T	B	8		0	0	8			(NOTE 4)								
T	B	7		1	7	1											
T	B	6		1	6	2											
|	|	|	Space Code	|	|	|											
|	|	|		|	|	|											
|	|	|		|	|	|											
|	|	|		|	|	|											
T	B	1		0	3	0											

Note 1: The code is a 7 bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1's" bits in the output word.

Note 4: The total number of "1's" bits in each output column or bit position.

Note 5: The punched card format is as shown except that columns 17 and 18 are not necessary. Program one address per card. All columns beyond those specified may be used by the customer.

MM4232/MM5232 4096-bit static read-only memory

general description

The MM4232/MM5232 4096-bit static read-only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE™ outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 512 word x 8-bit or 1024 word x 4-bit memory organization that is controlled by the mode control input. Programmable Chip Enables (CE_1 and CE_2) provide logic control of up to 16K bits without external logic. A separate output supply lead is provided to reduce internal power dissipation in the output stages.

Customer programs may be submitted for production in a paper tape or punched card format.

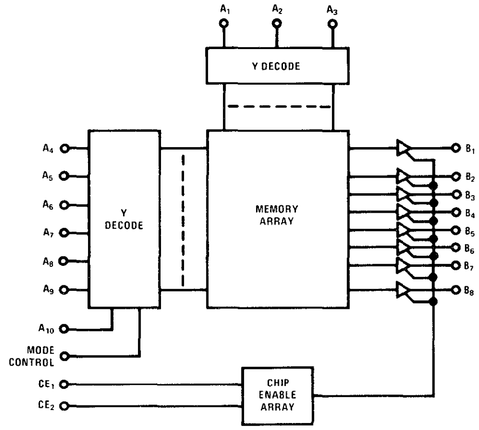
features

■ Bipolar compatibility	No external components required
■ Standard supplies	+5V, −12V
■ Bus ORable output	TRI-STATE outputs
■ Static operation	No clocks required
■ Multiple ROM control	Two-programmable Chip Enable lines

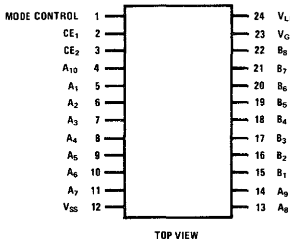
applications

- Character generator
- Random logic synthesis
- Micro-programming
- Table look-up

logic and connection diagrams



Dual-In-Line Package



typical applications

TTL/MOS Interface

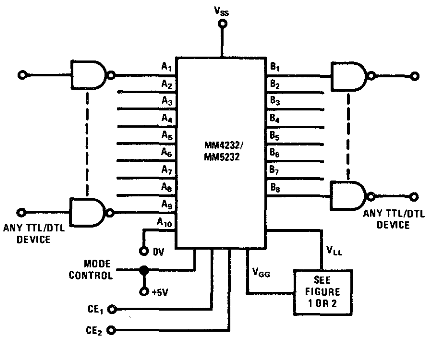


FIGURE 1. Power Saver for Small Memory Arrays

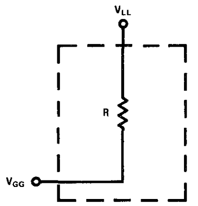
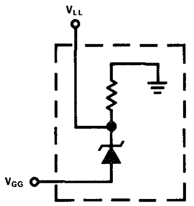


FIGURE 2. Power Saver for Large Memory Arrays



ASSUME $|V_{LL}|MIN = |-3V|$

$V_{GG} - V_{LL}$ MIN = R (1.6 mA) (N) where N = 4 for 1024 x 4 organization
N = 8 for 512 x 8 organization

Operating Modes

512 x 8 ROM connection
Mode Control – Logic HIGH
A_{10} – Logic LOW

1024 x 4 ROM connection
Mode Control – Logic LOW
A_{10} – Logic HIGH enables the odd ($B_1 \ldots B_7$) outputs
Logic LOW enables the even ($B_2 \ldots B_8$) outputs

When $CE_1 = 1$, $CE_2 = 1$ the outputs are enabled when a logic LOW is applied to the chip enable line. The outputs are in the third state when disabled. The logic states of the chip enables are specified on the program tape. Mode Control must be hard wired to V_{GG} or V_{LL} for a logic LOW or to V_{SS} for a logic HIGH.

absolute maximum ratings

V_{GG} Supply Voltage		$V_{SS} - 20V$
V_{LL} Supply Voltage		$V_{SS} - 20V$
Input Voltage		$(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + .03)V$
Storage Temperature Range		-65°C to +150°C
Operating Temperature Range	MM4232	-55°C to +125°C
	MM5232	-25°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

T_A within operating temperature range, $V_{SS} = +5V \pm 5\%$, $V_{GG} = V_{DD} = -12V \pm 5\%$, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
Logical LOW	$I_L = 1.6$ mA Sink			.4	V
Logical HIGH	$I_L = 100\ \mu A$ Source	2.4			V
Input Voltage Levels					
Logical LOW				$V_{SS} - 4.0$	V
Logical HIGH		$V_{SS} - 2.0$			V
Power Supply Current					
I_{SS} (Note 4)	$V_{SS} = 5$, $V_{GG} = -12$, $V_{LL} = -12$, $T_A = 25°C$		23	37	mA
I_{SS} (Note 4)	$V_{SS} = 5$, $V_{GG} = -12$, $V_{LL} = -3$, $T_A = 125°C$		12	20	mA
Input Leakage	$V_{IN} = V_{SS} - 10V$			1	μA
Input Capacitance (Note 2)	$f = 1.0$ MHz, $V_{IN} = 0V$		5	10	pF
Output Capacitance (Note 2)	$f = 1.0$ MHz, $V_{IN} = 0V$		4	10	pF
Address Time (Note 1) T_{ACCESS}	$T_A = 25°C$, $V_{SS} = 5$ $V_{GG} = V_{LL} = -12V$	150		1000	ns
Output AND Connections (Note 3)				20	

Note 1: Capacitances are measured periodically only.

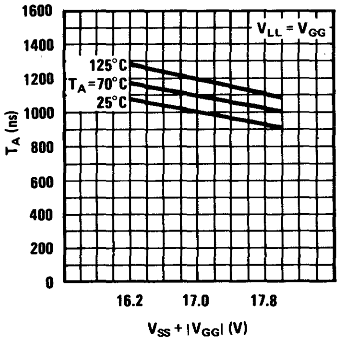
Note 2: Address is measured from the change of data on any input or chip enable line to the output of a TTL gate. (See Timing Diagram.)

Note 3: The address time follows the following equation: T_{ACCESS} = The specified limit + (N−1) x 25 ns where N = Number of AND connections.

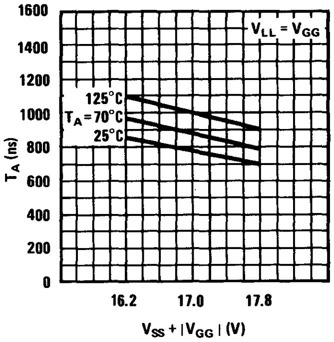
Note 4: Outputs open.

performance characteristics

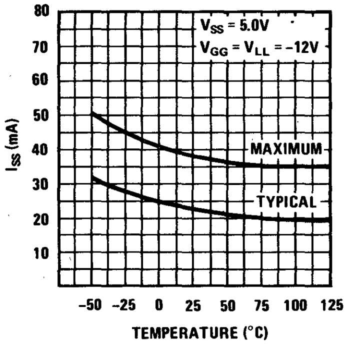
Guaranteed Access Time vs Supply Voltage



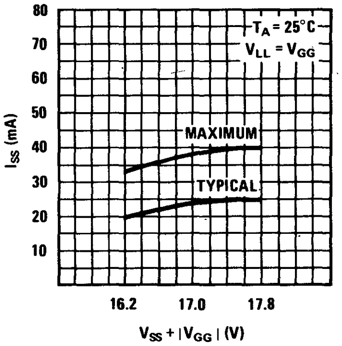
Typical Access Time vs Supply Voltage



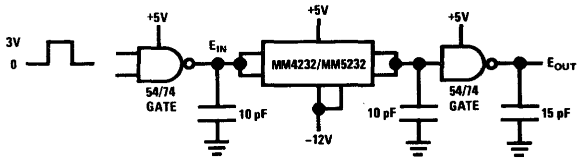
Power Supply Current vs Temperature

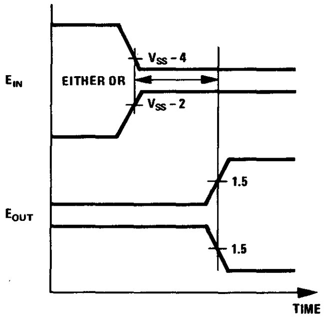


Power Supply Current vs Voltage

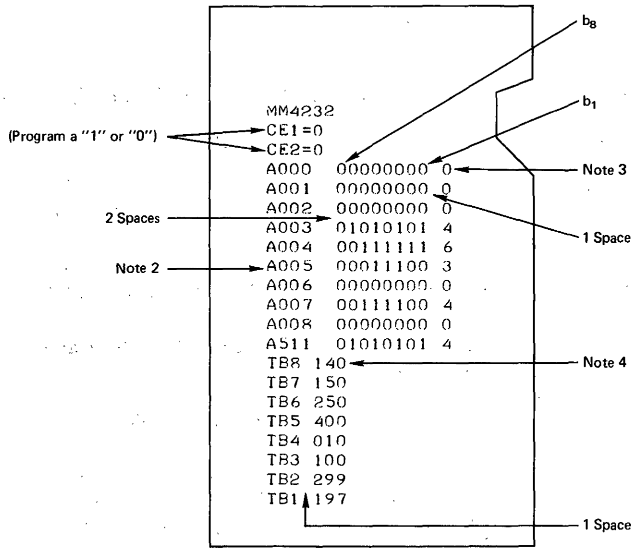


timing diagram/address time





punch tape format



```
MM4232
CE1=0
CE2=0
A000  00000000 0
A001  00000000 0
A002  00000000 0
A003  01010101 4
A004  00111111 6
A005  00011100 3
A006  00000000 0
A007  00111100 4
A008  00000000 0
A511  01010101 4
TB8 140
TB7 150
TB6 250
TB5 400
TB4 010
TB3 100
TB2 299
TB1 197
```

Note 1: The code is a 7 bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in decimal form and is preceded by the letter A.

Note 3: The total number of "1's" bits in the output word.

Note 4: The total number of "1's" bits in each output column or bit position.

The MM5232 can be programmed as a 512 x 8 or a 1024 x 4. The tape would print out as shown for the 512 x 8 code.

MM4240/MM5240 2560-bit static character generator

general description

The MM4240/MM5240 2560-bit static character generator is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology. Six character address and three row address input lines provide access to 64–8 x 5 characters. Customer-generated single or multiple package character fonts are easily programmed by completing a pattern selection form. A standard 7 x 5 raster scan font is available by ordering the MM4240AA/MM5240AA. (See page 102.)

The MM4240/MM5240 may be used as a 512 x 5-bit read only memory for applications other than character generation.

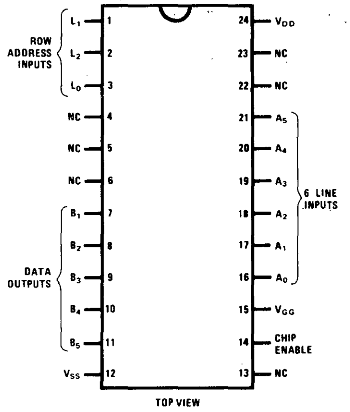
features

- Bipolar compatibility
- High speed operation—600 ns max.
- ±12 volt power supplies
- Static operation—no clocks required
- Multiple ROM logic application—chip enable output control
- Standard fonts available—off-the-shelf delivery

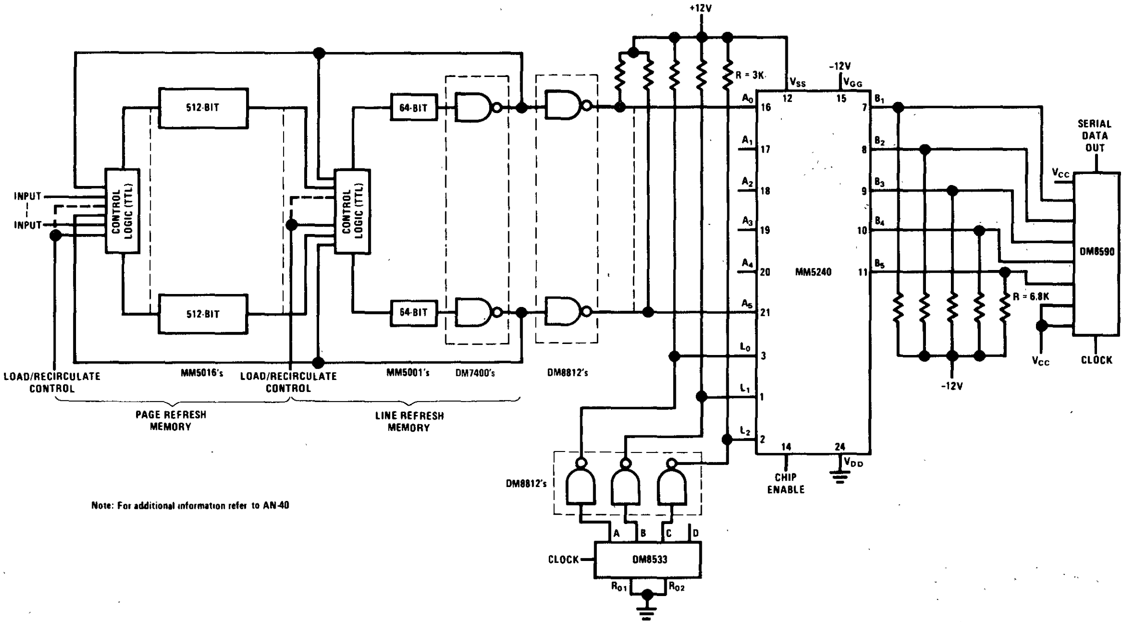
applications

- Character generation
- Random logic synthesis
- Micro-programming
- Table look-up

connection diagram



typical application



Note: For additional information refer to AN-40

absolute maximum ratings

V_{GG} Supply Voltage		V_{SS} - 30V
V_{DD} Supply Voltage		V_{SS} - 15V
Input Voltage		$(V_{SS} - 20)V < V_{IN} < (V_{SS} + 0.3)V$
Storage Temperature		-65°C to +150°C
Operating Temperature	MM4240	-55°C to +125°C
	MM5240	-25°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
MOS to MOS					
Logical "1"	IMΩ to GND			V_{SS} - 9.0	V
Logical "0"		V_{SS} - 1.0			V
MOS to TTL					
Logical "1"	6.8 kΩ to V_{GG} Plus One			+0.4	V
Logical "0"	Standard Series 54/74 Gate	+2.5			V
Output Current Capability					
Logical "0"	$V_{OUT} = V_{SS} - 6.0V$	2.5			mA
Input Voltage Levels					
Logical "1"				V_{SS} - 8.0	V
Logical "0"		V_{SS} - 2.0			V
Power Supply Current	T_A = 25°C				
I_{DD}	MOS Load		25	40	mA
I_{GG} (Note 2)				1	μA
Input Leakage	$V_{IN} = V_{SS} - 12V$			1	μA
Input Capacitance	f = 1.0 MHz, V_{IN} = 0V		5	8	pF
V_{GG} Capacitance	f = 1.0 MHz, V_{IN} = 0V		25	40	pF
Address Time (Note 3)	See Timing Diagram				
T_{ACCESS}	T_A = 25°C	150	450	600	ns
Output AND Connection	MOS Load			4	
(Note 4)	TTL Load			10	

Note 1: These specifications apply for V_{SS} = +12V ±5%, V_{GG} = −12V ±5%, and T_A = −55°C to +125°C (MM4240), T_A = −25°C to +70°C (MM5240) unless otherwise specified.

Note 2: The V_{GG} supply may be clocked to reduce device power without affecting access time.

Note 3: Address time is measured from the change of data on any input or Chip Enable line to the output of a TTL gate. (See Timing Diagram). See curves for guaranteed limit over temperature.

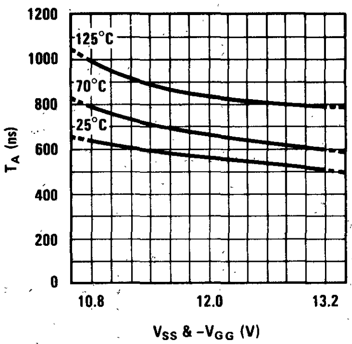
Note 4: The address time in the TTL load configuration follows the equation:
T_{ACCESS} = The specified limit + (N − 1) (50) ns

Where N = Number of AND connections.

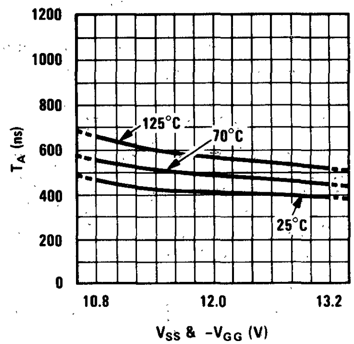
The number of AND ties in the MOS load configuration can be increased at the expense of MOS "0" level.

performance characteristics

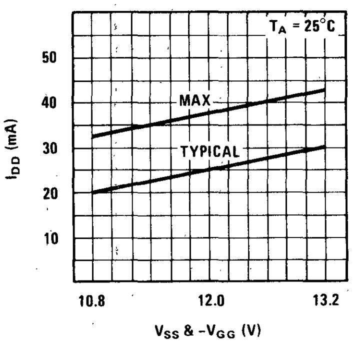
Guaranteed Access Time (T_A) vs Supply Voltage



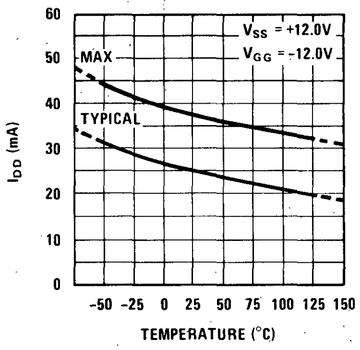
Typical Access Time (T_A) vs Supply Voltage



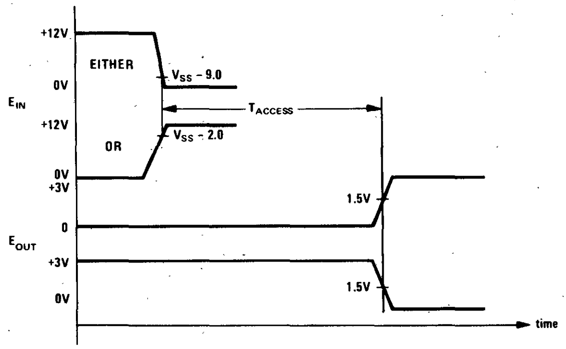
Power Supply Current vs Voltage

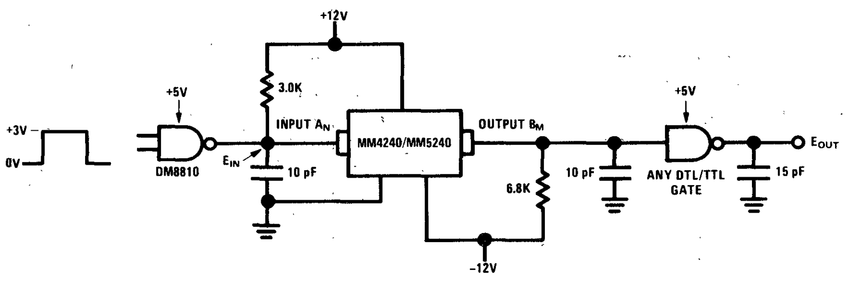


V_{DD} Power Supply Current vs Temperature

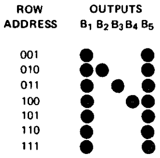


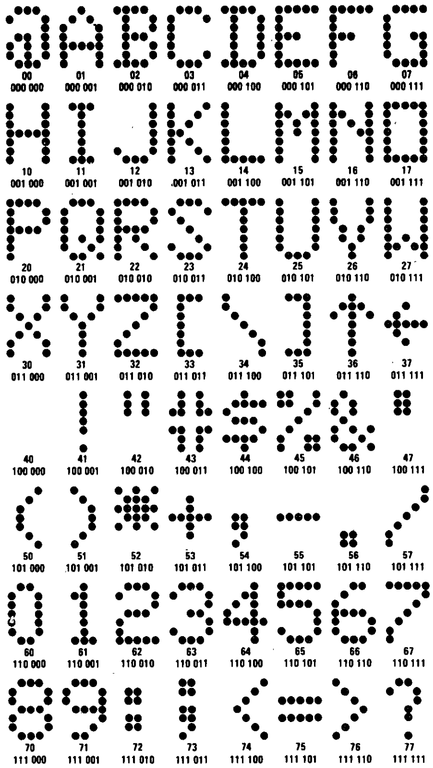
timing diagram/address time





MM4240AA/MM5240AA character font





Input addresses are in six bit ASCII code and are shown in the sequence A_5, A_4, . . . A_0; the octal equivalent is also shown for reference.

ROMs

MM4241/MM5241 3072-bit static read-only memory

general description

The MM4241/MM5241 3072-bit static read-only memory is a P-channel enhancement mode monolithic MOS integrated circuit utilizing a low threshold voltage technology to achieve bipolar compatibility. TRI-STATE™ outputs provide wire ORed capability without loading common data lines or reducing system access times. The ROM is organized in a 64 x 6 word by 8-bit memory organization. Programmable Chip Enables (CE_1 and CE_2) provide logic control of multiple packages without external logic. A separate output supply lead is provided to reduce internal power dissipation in the output stages.

Customer programs may be submitted for production in a paper tape or punched card format.

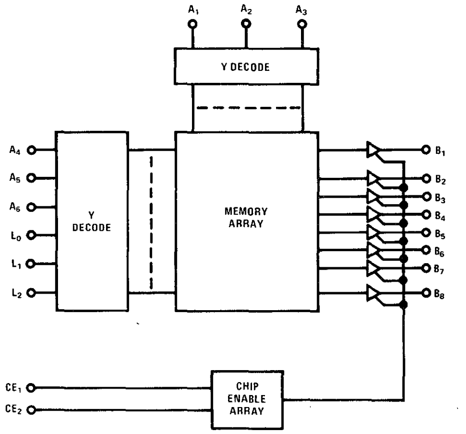
features

■ Bipolar compatibility	No external components required
■ Standard supplies	+5V, −12V
■ Bus ORable output	TRI-STATE outputs
■ Static operation	No clocks required
■ Multiple ROM control	Two programmable Chip Enable lines

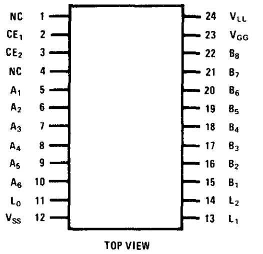
applications

- Character generator
- Random logic synthesis
- Micro-programming
- Table look-up

logic and connection diagrams



Dual-In-Line Package



typical applications

TTL/MOS Interface

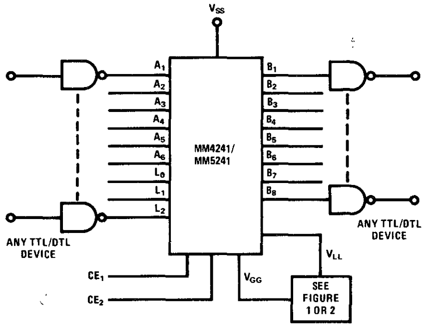


FIGURE 1. Power Saver for Small Memory Arrays

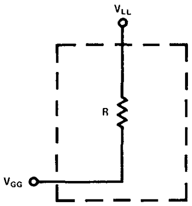
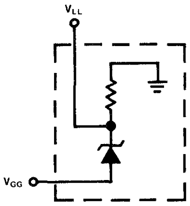


FIGURE 2. Power Saver for Large Memory Arrays



ASSUME $|V_{LL}|MIN = |-3V|$
$V_{GG} - V_{LL}$ MIN = R (1.6 mA) (N) where N = 7 for 5 x 7 font.
N = 8 for 6 x 8 font.

When $CE_1 = 1$, $CE_2 = 1$ the outputs are enabled when a logic LOW is applied to the chip enable line. The outputs are in the third state when disabled. The logic states of the chip enables are specified on the program tape.

absolute maximum ratings

V_{GG} Supply Voltage		V_{SS} - 20V
V_{LL} Supply Voltage		V_{SS} - 20V
Input Voltage		$(V_{SS} - 20)\ V < V_{IN} < (V_{SS} + .03)V$
Storage Temperature Range		-65°C to +150°C
Operating Temperature Range	MM4241	-55°C to +125°C
	MM5241	-25°C to +70°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

T_A within operating temperature range, V_{SS} = +5V ±5%, $V_{GG} = V_{DD}$ = −12V ±5%, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage Levels					
Logical LOW	I_L = 1.6 mA sink			.4	V
Logical HIGH	I_L = 100 µA source	2.4			V
Input Voltage Levels					
Logical LOW				V_{SS} - 4.0	V
Logical HIGH		V_{SS} - 2.0			V
Power Supply Current					
I_{SS} (Note 4)	$V_{SS} = 5$, $V_{GG} = -12$, $V_{LL} = -12$, T_A = 25°C		23	37	mA
I_{SS} (Note 4)	$V_{SS} = 5$, $V_{GG} = -12$, $V_{LL} = -3$, T_A = 125°C			20	mA
Input Leakage	$V_{IN} = V_{SS} - 10V$			1	µA
Input Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		5	10	pF
Output Capacitance (Note 1)	f = 1.0 MHz, V_{IN} = 0V		4	10	pF
Address Time (Note 2) T_{ACCESS}	T_A = 25°C, V_{SS} = 5 $V_{GG} = V_{LL}$ = −12V	150	700	900	ns
Output AND Connections (Note 3)				20	

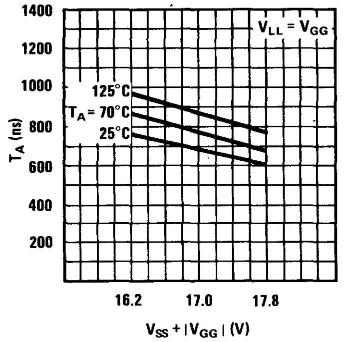
Note 1: Address is measured from the change of data on any input or chip enable line to the output of a TTL gate. (See Timing Diagram.) See curves for guaranteed limit over temperature.

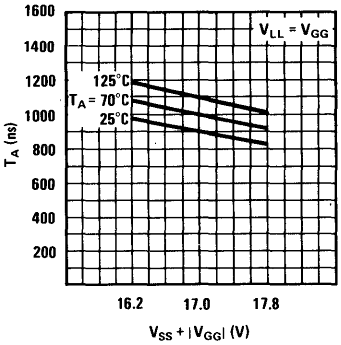
Note 2: Capacitances are measured periodically only.

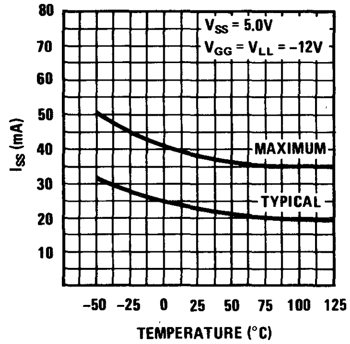
Note 3: The address time follows the following equation: T_{ACCESS} = The specified limit + (N–1) x 25 ns where N = Number of AND connections.

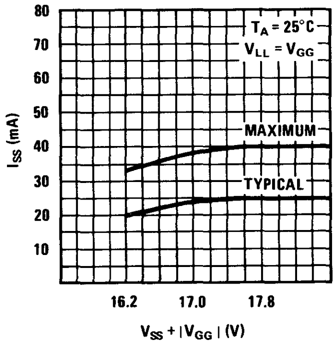
Note 4: Outputs open.

performance characteristics

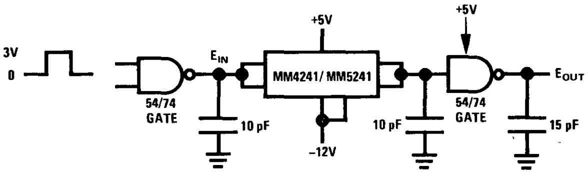

Typical Access Time vs Supply Voltage

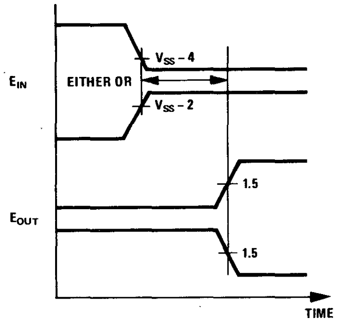

Guaranteed Access Time vs Supply Voltage


Power Supply Current vs Temperature

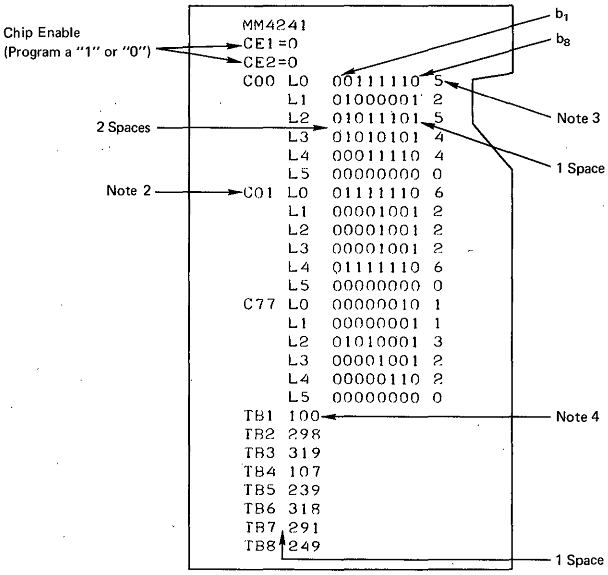

Power Supply Current vs Voltage

timing diagram/address time





punch tape format



```
MM4241
CE1=0
CE2=0
C00 L0  00111110 5
    L1  01000001 2
    L2  01011101 5
    L3  01010101 4
    L4  00011110 4
    L5  00000000 0
C01 L0  01111110 6
    L1  00001001 2
    L2  00001001 2
    L3  00001001 2
    L4  01111110 6
    L5  00000000 0
C77 L0  00000010 1
    L1  00000001 1
    L2  01010001 3
    L3  00001001 2
    L4  00000110 2
    L5  00000000 0
TB1 100
TB2 298
TB3 319
TB4 107
TB5 239
TB6 318
TB7 291
TB8 249
```

Note 1: The code is a 7 bit ASCII code on 8 punch tape. The tape should begin and end with 25 or more "RUBOUT" punches.

Note 2: The ROM input address is expressed in octal form and is preceded by the letter C, the row or line is expressed in decimal form and is preceded by the letter L. There are 78 octal (64 decimal) locations.

Note 3: The total number of "1's" bits in the output word.

Note 4: The total number of "1's" bits in each output column or bit position.

MM1101/MM11011/MM1101A/MM1101A1/MM1101A2
256-bit fully decoded static random access memory

general description

The MM1101 family of fully decoded 256 word x 1-bit random access memories are monolithic MOS integrated circuits using silicon gate low threshold technology to achieve bipolar compatibility. They are static, require no clocks, and hold information indefinitely, subject to the integrity of the power supply to the RAM plane.

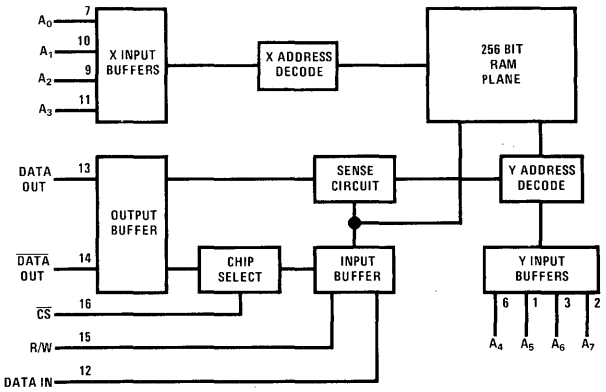
features

- Fast access times MM1101A2 500 ns max
  MM11011, MM1101A1 1.0 µs max
  MM1101, MM1101A 1.5 µs max
- Improved speed/power product MM1101A2 1/3 of 1101A
- Low power operation 1.5 mW/bit
- Fewer system components bipolar compatible input and output
- Second source flexibility 1101, 1101A, 11011, 1101A1 second sources available
- TRI-STATE™ output wired OR capability
- Specified ambient temperature −25°C to +70°C

applications

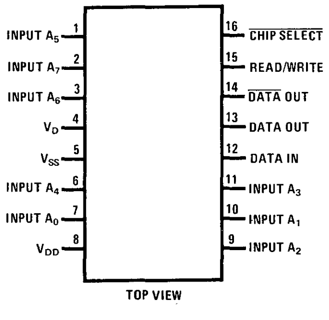
- High speed buffer memories
- Local memory store

block and connection diagrams



V_D = Power to buffers, decoders, and sense circuit
V_{DD} = RAM plane power only. See Note 5.

Dual-In-Line Package



absolute maximum ratings

All Input or Output Voltages with Respect to the Most Positive Supply Voltage, V_{SS}	+.3V to −20V
Supply Voltages V_{DD} and V_D with Respect to V_{SS}	−16V
Power Dissipation at Room Temperature	700 mW
Operating Temperature	−25°C to +70°C ambient
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

dc characteristics (Note 1)

$T_A = -25°C$ to $70°C$, $V_{SS} = +5V \pm 5\%$, $V_{DD} = -9V \pm 5\%$, unless otherwise specified.
$V_{SS} = +5V \pm 5\%$, $V_D = -10V \pm 5\%$, $V_{DD} = -7V \pm 5\%$ (for MM1101 and MM11011)

SYMBOL	TEST	CONDITIONS	MIN	TYP (NOTE 2)	MAX	UNITS
I_{LI}	Input Load Current (All Input Pins)	$V_{IN} = 0.0V$		1.0	500	nA
I_{LO}	Output Leakage Current	$V_{OUT} = 0.0V$, $CS = V_{SS} - 2.0V$		1.0	500	nA
I_{DD}	Power Supply Current, V_{DD}	$T_A = 25°C$ Continuous Operation		13.0	19	mA
I_D	Power Supply Current, V_D	$T_A = 25°C$ $I_{OL} = 0.0$ mA		12.0	18	mA
V_{IL}	Input LOW Voltage		−10		$V_{SS} - 4.2$	V
V_{IH}	Input HIGH Voltage		$V_{SS} - 2.0$		$V_{SS} + 0.3$	V
I_{OL}	Output Sink Current	$V_{OUT} = +0.45V$	2.0			mA
I_{CF}	Output Sink Current	$V_{OUT} = -1.0V$		6.0		mA
V_{OH}	Output HIGH Voltage	$I_{OH} = -100\mu A$	+2.4	3.5		V
C_{IN}	Input Capacitance (Note 3) (All Input Pins)	$V_{IN} = V_{SS}$		7	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = V_{SS}$ f = 1 MHz		7	10	pF
C_V	V_D Power Supply Capacitance	$V_D = V_{SS}$		20	35	pF

ac characteristics

READ CYCLE

SYMBOL	TEST	MIN	TYP (NOTE 2)	MAX	UNITS
t_{rc}	Read Cycle MM1101, MM1101A	1.5			µs
	MM11011, MM1101A1	1.0			µs
	MM1101A2	500			ns
t_a	Access Time MM1101, MM1101A To Either Output		0.85	1.5	µs
	MM11011, MM1101A1		0.65	1.0	µs
	MM1101A2		400	500	ns
t_t	Chip Select to Third State Delay		30	150	ns

WRITE CYCLE

SYMBOL	TEST	MIN	TYP (NOTE 2)	MAX	UNITS
t_{wc}	Write Cycle	0.8			µs
t_{wd}	Address to Write Pulse Delay	0.3			µs
t_{wp}	Write Pulse Width	0.4			µs
t_{dw}	Data Set-up Time	0.3			µs
t_{dh}	Data Hold Time	0.1			µs

Note 1: All voltage measurements are referenced to ground.

Note 2: Typical values are at $T_A = +25°C$ and nominal supply voltages.

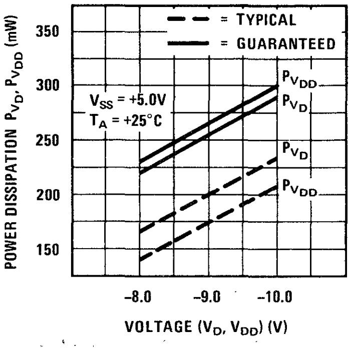
Note 3: Capacitances are measured periodically only.

Note 4: Devices specified for full mil (−55°C to +125°C) temperature range are available. Consult your local sales office or the factory.

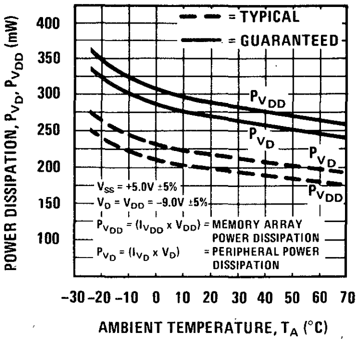
Note 5: For minimum power data retention, turn off V_D, and pulse V_{DD} on for 2 µs every 1 ms or hold 6V min at 2 mA max.

performance curves (MM1101A/MM1101A1/MM1101A2)

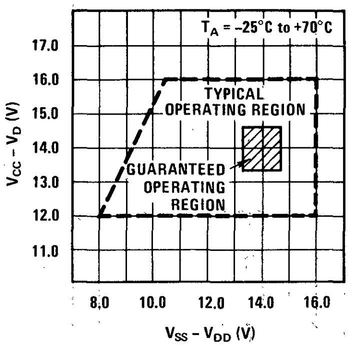
Power Dissipation vs Voltage



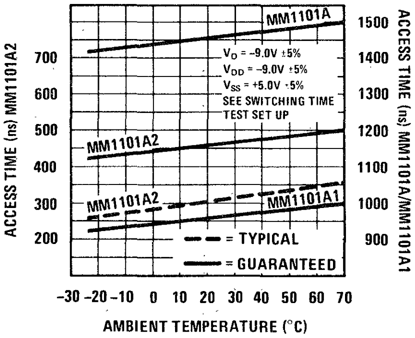
Power Dissipation vs Ambient Temperature



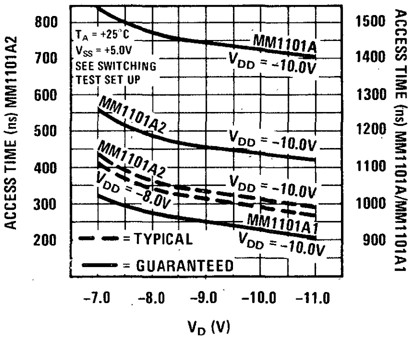
Operating Region



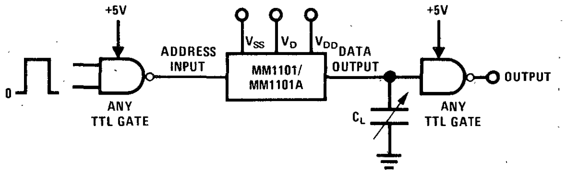
Access Time vs Ambient Temperature



Access Time vs Supply Voltage



test circuit



CONDITIONS OF TEST

Input pulse amplitudes: 0V to +5.0V

Input pulse rise and fall times $\leq$ 10 ns

Speed measurements are referenced to the 1.5V level (unless otherwise noted), at the output of the TTL gate ($t_{pd} \leq 10$ ns) $C_L \leq 20$ pF.

Test Setup for MM1101 and MM1101A Speed Measurement

Note 1: All inputs of the MM1101A accept standard TTL outputs with V_{CC} = +5.0V ±5%.

Note 2: Access time degradation as a function of load capacitance may be determined from the following equations:

a) $t_a\ (T_A = +25°C) = t_{0_1} + 0.32\ C_L$ ns

b) $t_a\ (T_A = +70°C) = t_{0_2} + 0.35\ C_L$ ns

Where t_{0_1}, t_{0_2} = access time in ns for 1 TTL load at T_A = +25°C, and T_A = +70°C respectively.

and C_L = pF

definition of timing parameters

t_a Access Time: The time required for the output to be valid from the initiation of an address change.

t_{wd} Address Input to Write Pulse Delay: The minimum time required after the initiation of an address change and the start of the Write mode of operation.

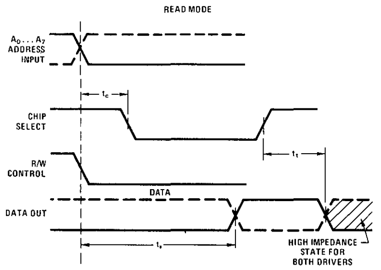
t_{wp} Write Pulse Width: The minimum pulse width required for writing.

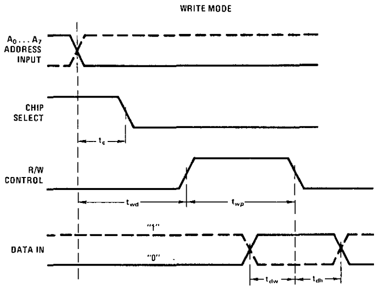
t_{dh} Data-Write Overlap: The minimum overlap between the R/W and the data-in pulse.

t_t Chip Select to TRI-STATE Delay: The maximum delay from Chip Select to the attainment of the high impedance state at the output during chip deselect operation.

t_c Chip Select to Address Bit Overlap: The maximum overlap between the initiation of address change and the transition of the Chip Select to the select mode.

switching time waveforms





Note 1: t_C must be less than 50 ns for minimum access times.

Note 2: While reading, data is guaranteed to remain true for a further 50 ns after the address is changed if chip select is kept low.

MM1103 1024-bit fully decoded dynamic random access read/write memory

general description

The MM1103 fully decoded dynamic 1024 word x 1-bit per word read/write random access memory is a monolithic MOS integrated circuit using silicon gate low threshold technology. This device provides a non-destructive read out memory cell with chip enable for easy selection when many outputs are "OR"ed. Low power is achieved by the use of dynamic logic and power dissipation occurs primarily during precharge. The MM1103 is used for main memory applications where large bit storage, high performance and low cost are important.

features

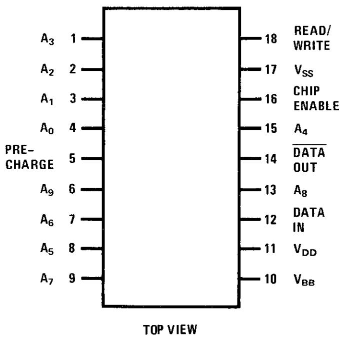
■ Fast access time	300 ns max
■ Fast cycle time	480 ns read cycle 580 ns write cycle
■ Refresh cycle	2 ms
■ Fully decoded	
■ Easy memory expansion	Chip enable input
■ Device protection	All I/O lines have protection against static charge
■ "OR"ing output capability	
■ Low power dissipation	250 mW
■ Small package size	18 pin DIP

applications

- ■ Mainframe memory
- ■ Large buffer memory

connection diagram

Dual-In-Line Package



TOP VIEW

absolute maximum ratings

All Input or Output Voltages With Respect to the Most Positive Supply Voltage V_{SS}	+0.3V to -25V
Supply Voltage V_{DD} and V_{BB} With Respect to V_{SS}	+0.3V to -25V
Power Dissipation at Room Temperature	500 mW
Operating Temperature Range	-25°C to +70°C
Storage Temperature Range	-65°C to +160°C
Lead Temperature (Soldering, 10 sec)	300°C

dc operating characteristics

T_A within operating temperature range, V_{SS} = 16 ± 1V; (V_{BB} −V_{SS}) = 3V to 4V, V_{DD} = 0V unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Load Current (All Input Pins) (I_{L1})	V_{IN} = 0V			1	μA
Output Leakage Current (I_{LO})	V_{OUT} = 0V			1	μA
V_{BB} Supply Current (I_{BB})				100	μA
Average Supply Current ($I_{DD\ AV}$)	Cycle Time = 580 ns precharge width = 240 ns, T_A = 25°C			20	mA
Standby Supply Current	Precharge = V_{SS}, Chip Enable = V_{SS}, T_A = 25°C			100	μA
Input LOW Voltage (V_{IL})		V_{SS} − 17		V_{SS} − 15	V
Input HIGH Voltage (V_{IH})		V_{SS} − 1		V_{SS} + 1	V
Output HIGH Current (I_{OH})	T_A = 25°C R_L = 100Ω	600		4000	μA
Output HIGH Voltage (V_{OH})	T_A = 25°C R_L = 100Ω	60		400	mV

ac operating characteristics T_A = 0°C to 70°C, V_{SS} = 16 ± 5%, (V_{BB} − V_{SS}) = 3.0V to 4.0V, V_{DD} = 0V

READ, WRITE, AND READ/WRITE CYCLE

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Time Between Refresh (t_{REF})				2	ms
Address to Cenable Set Up Time (t_{AC}) Note 1		115			ns
Cenable to Address Hold Time (t_{CA})		20			ns
Precharge to Cenable Delay (t_{PC}) Note 1		125			ns
Precharge & Cenable Overlap, LOW (t_{OVL})		25		75	ns
Cenable to Precharge Delay (t_{CP})		85			ns
Precharge & Cenable Overlap, HIGH (t_{OVH})				140	

READ CYCLE

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Read Cycle (t_{RC}) Note 1	$t_{ACmin} + t_{OVLmin} + t_{POmax} + 2\ t_T$ $t_{PCmin} + t_{OVLmin} + t_{POmax} + 2\ t_T$ t_T = 20 ns C_{LOAD} = 100 pF R_{LOAD} = 100Ω V_{REF} = 40 mV	480			ns
Precharge to End of Cenable (t_{POV})		165		500	ns
End of Precharge to Output Delay (t_{PO})				120	ns
Address to Output Access (t_{ACC1}) Note 1		300			ns
Precharge to Output Access (t_{ACC2}) Note 1		310			ns

WRITE OR READ/WRITE CYCLE

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Write Cycle (t_{WC}) Note 1	t_T = 20 ns	580			ns
Read/Write Cycle (t_{RWC}) Note 1	t_T = 20 ns	580			ns
Precharge to Read/Write Delay (t_{PW})		165		500	ns
Read/Write Pulse Width (t_{WP})		80			ns
Read/Write Set Up Time (t_W)		80			ns
Data Set Up Time (t_{DW})		105			ns
Data Hold Time (t_{DH})		10			ns
End of Precharge to Output Delay (t_{PO})	C_{LOAD} = 100 pF R_{LOAD} = 100Ω			120	ns
Time to Next Precharge (t_P)	V_{REF} = 40 mV	0			

Note 1: These times will degrade by 40 ns (worst case) if the maximum values for V_{IL} (for precharge, cenable and read/write inputs) go to V_{SS} − 14.2V @ 0°C and V_{SS} − 14.5V @ 70°C.

ac operating characteristics (con't)

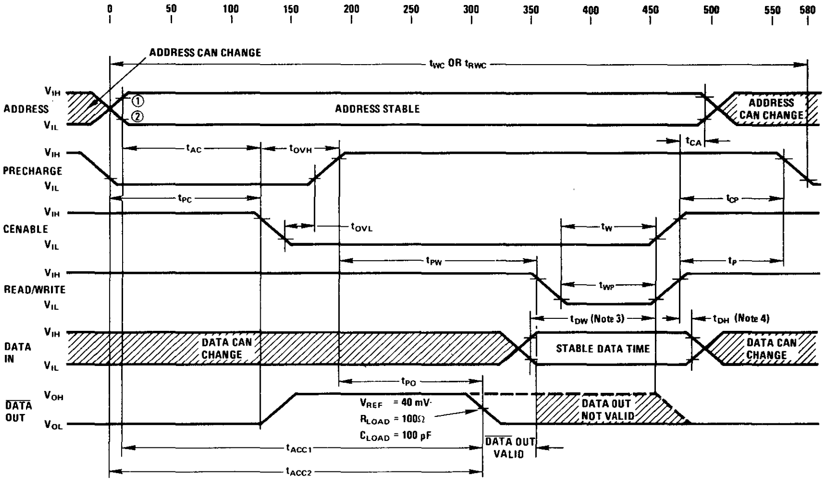
*CAPACITANCE

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Address Capacitance (C_{AD})	$V_{IN} = V_{SS}$	f = 1 MHz All Unused Pins Are at AC GND		5	7	pF
Precharge Capacitance (C_{PR})	$V_{IN} = V_{SS}$			15	18	pF
Cenable Capacitance (C_{CE})	$V_{IN} = V_{SS}$			15	25	pF
Read/Write Capacitance (C_{RW})	$V_{IN} = V_{SS}$			11	15	pF
Data Input Capacitance (C_{IN1})	Cenable = 0V $V_{IN} = V_{SS}$			4	5	pF
Data Input Capacitance (C_{IN2})	Cenable = V_{SS} $V_{IN} = V_{SS}$			2	4	pF
Data Output Capacitance (C_{OUT})	V_{OUT} = 0V			2	3	pF

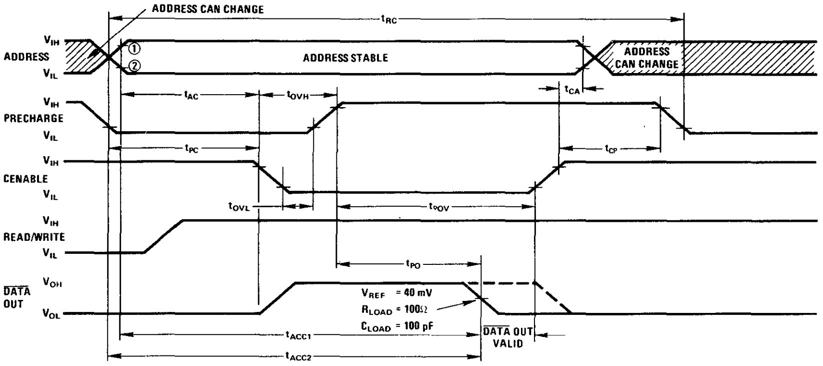
*This parameter is periodically sampled and is not 100% tested. They are measured at worst case operating conditions. Capacitance are for plastic packages only.

switching time waveforms

WRITE CYCLE OR READ/WRITE CYCLE
TIMING ILLUSTRATED FOR MINIMUM CYCLE



READ CYCLE



Note ① $V_{DD} + 2V$ }
Note ② $V_{SS} - 2V$ } t_T is defined as the transitions between these two points.
Note 3 t_{DW} is referenced to point ② of the rising edge of cenable or read/write whichever occurs first
Note 4 t_{DH} is referenced to point ① of the rising edge of cenable or read/write whichever occurs first

MM5260 1024-bit fully decoded dynamic random access memory

general description

The MM5260 fully decoded dynamic 1024 word x 1-bit word read/write random access memory is a monolithic MOS integrated circuit using silicon gate low threshold technology to achieve bipolar compatibility on all I/O lines except the precharge and read/write lines. This provides an efficient approach to memory design using this systems oriented device. The MM5260 is used for main memory applications where large bit storage and improved operating performance are important. A TRI-STATE™ output is utilized to allow wired "OR" capability and common I/O data busing in memory applications.

features

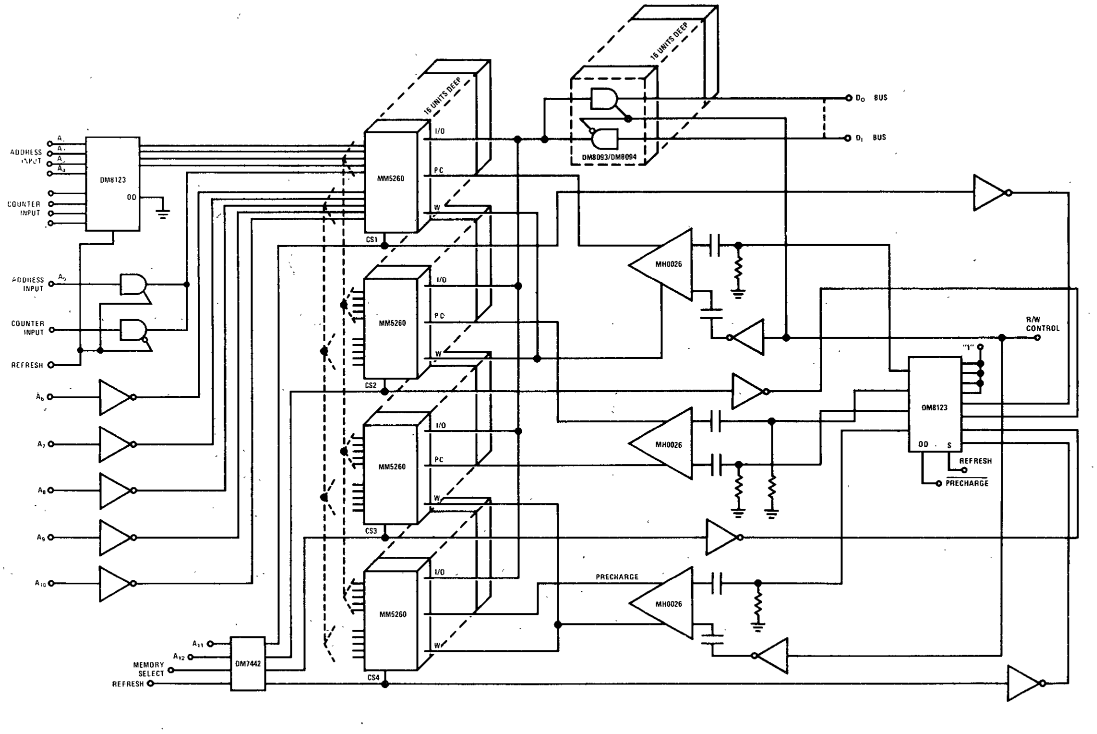
■ Fast access time	350 ns
■ Fast cycle time	450 ns read cycle min 600 ns write cycle min
■ Low overhead circuit count	Fully decoded
■ Systems-oriented design	Bipolar compatible (address lines, chip enable data I/O) Common data I/O line TRI-STATE output
■ Refresh cycle	2.0 ms
■ Easy memory expansion	Chip enable
■ Device protection	All I/O lines have protection against static charge
■ Standard power supplies	+5V, −12V
■ Low power dissipation	400 mW
■ Small package size	16 pin dual-in-line package

applications

- ■ High speed mainframe memory
- ■ Mass memory storage

typical application

Main Memory Module Storing 4096 16-Bit Words



absolute maximum ratings

All Input or Output Voltages with Respect to Most Positive Supply Voltage V_{SS}	+0.3V to −20V
Power Dissipation	600 mW
Operating Temperature Range	−25°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

dc operating characteristics

T_A within operating temperature range, V_{SS} = +5V ±5%, V_{DD} = −12V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage (Address input, chip enable and data input)					
Logic "0" (V_{IH})		$V_{SS} - 2.0$			V
Logic "1" (V_{IL})				$V_{SS} - 4.0$	V
Input voltage (Precharge and Read/Write)					
Logic "0" (V_{IH})		$V_{SS} - 1.5$			V
Logic "1" (V_{IL})				$V_{SS} - 15$	V
Output Voltage Data Output					
Logic "0" (V_{OH})	I_L = 200 μA Source	2.4			V
Logic "1" (V_{OL})	I_L = 1.6 mA Sink			0.4	V
Average Supply Current (I_{DD}) t cycle = 450 ns and t_{pc} = 300 ns			20		mA

ac operating characteristics

T_A within operating temperature range, V_{SS} = +5V ±5V%, V_{DD} = −12V ±5%, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Read Cycle (T_{RC})		450			ns
Write Cycle (T_{WC})		600			ns
Read/Write Cycle (T_{RWC})		(600 + T_D See Note 1)			ns
Access Time (T_A)			350		ns
Address to Chip Enable (T_{AC}) Note 2		0		50	ns
Address to Precharge Delay (T_{APL}) Note 2		0		50	ns
Address to Write Pulse Delay (T_{AWD})		350			ns
Write Pulse Width (T_{WP})		250			ns
Precharge Off Time (T_{PP})		150			ns
Read Write to Precharge Delay (T_{WRP})		50			ns
Refresh Interval (T_{REF})				2	ms
Address to Precharge Trailing Edge (T_{APT})		350			ns

capacitance characteristics

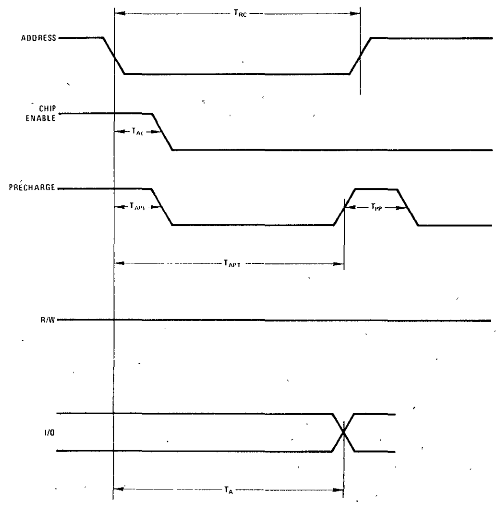
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Address Capacitance (C_A)	$V_{IN} = V_{SS}$	f = 1 MHz All unused inputs are at AC Ground		5		pF
Chip Enable Capacitance (C_{CE})	$V_{IN} = V_{SS}$			5		pF
Precharge Capacitance (C_{PC})	$V_{IN} = V_{SS}$			25		pF
Read/Write Capacitance (C_{RW})	$V_{IN} = V_{SS}$			10		pF
Data Input/Output Capacitance ($C_{IN/OUT}$)	$V_{IN} = V_{SS}$			7		pF

Note 1: T_D = Output data to input data delay in read-modify-write cycle.

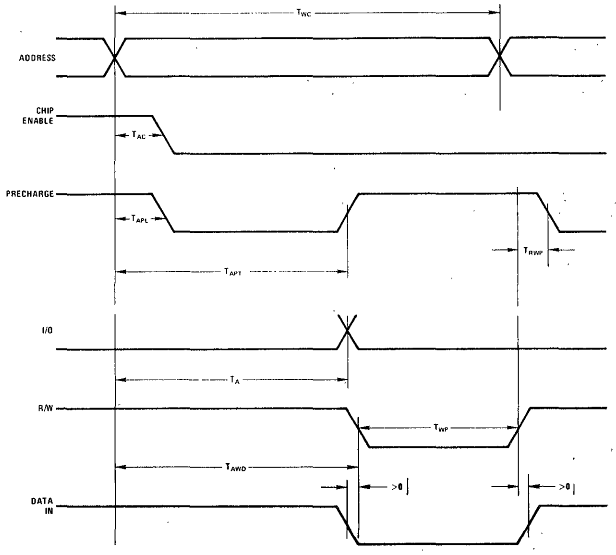
Note 2: Characteristic max limits to achieve T_A specifications. An increase in these times will cause T_A to increase directly.

switching time waveforms

READ CYCLE



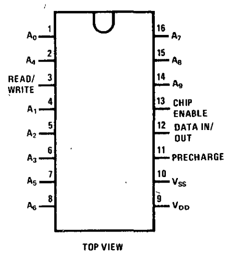
WRITE CYCLE



Note: Precharge and read/write signals should not overlap.

connection diagram

Dual-In-Line Package



Clock Drivers

MH0007/MH0007C dc coupled MOS clock driver

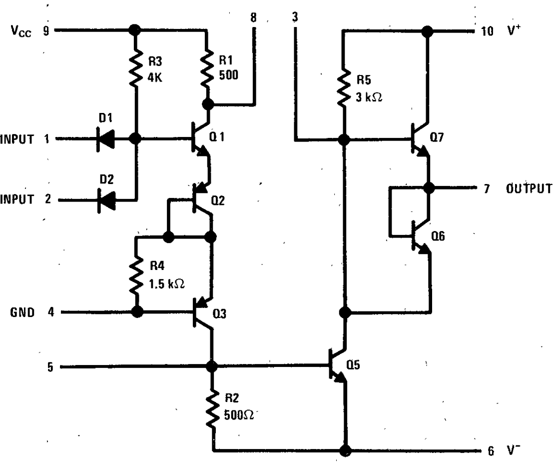
general description

The MH0007 is a voltage translator and power booster designed for interfacing between conventional TTL or DTL voltage levels and those levels associated with inputs or clocks of MOS FET type devices. The design allows the user a wide latitude in selection of supply voltages, and is especially useful in normally "off" applications, since power dissipation is typically only 5 milliwatts in the "off" state.

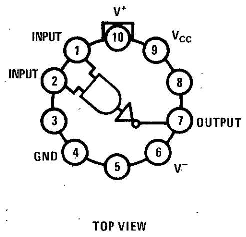
features

- 30 volts (max) output swing
- Standard 5V power supply
- Peak currents in excess of ±300 mA available
- Compatible with all MOS devices
- High speed: 5 MHz with nominal load
- External trimming possible for increased performance

schematic and connection diagram

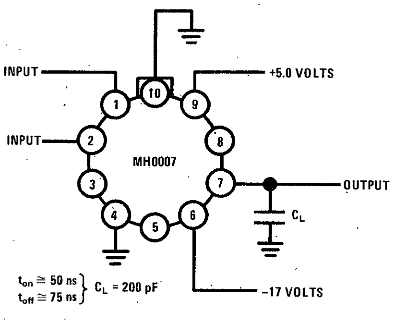


10 Pin TO-100 Package



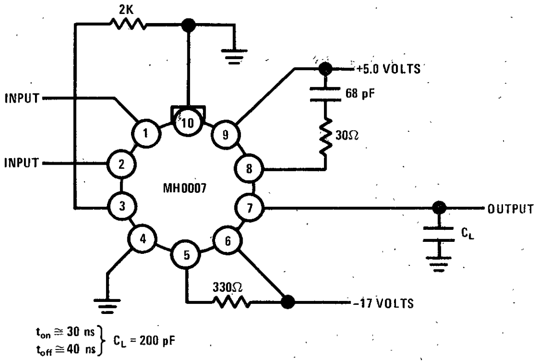
typical applications

Switching Time Test Configuration



$t_{on} \cong 50$ ns, $t_{off} \cong 75$ ns; $C_L = 200$ pF

High Speed Operation



$t_{on} \cong 30$ ns, $t_{off} \cong 40$ ns; $C_L = 200$ pF

absolute maximum ratings

V_{CC} Supply Voltage	8V
V^- Supply Voltage	-40V
V^+ Supply Voltage	+28V
$(V^+ - V^-)$ Voltage Differential	30V
Input Voltage	5.5V
Power Dissipation ($T_A = 25°C$)	800 mW
Peak Output Current	±500 mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range MH0007	-55°C to +125°C
MH0007C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

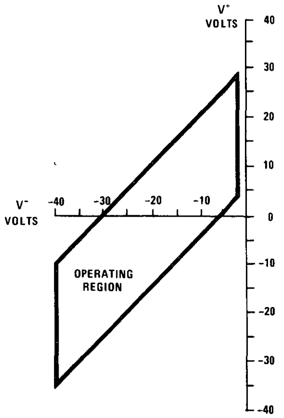
PARAMETER	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
Logical "1" Input Voltage	$V_{CC} = 4.5V$	2.2			V
Logical "0" Input Voltage	$V_{CC} = 4.5V$			0.8	V
Logical "1" Input Current	$V_{CC} = 5.5V$, $V_{IN} = 5.5V$			100	μA
Logical "0" Input Current	$V_{CC} = 5.5V$, $V_{IN} = 0.4V$		1.0	1.5	mA
Logical "1" Output Voltage	$V_{CC} = 5.5V$, $I_{OUT} = 30$ mA, $V_{IN} = 0.8V$	$V^+ - 4.0$			V
	$V_{CC} = 5.5V$, $I_{OUT} = 1$ mA, $V_{IN} = 0.8V$	$V^+ - 2.0$			V
Logical "0" Output Voltage	$V_{CC} = 4.5V$, $I_{OUT} = 30$ mA, $V_{IN} = 2.2V$			$V^- + 2.0$	V
Transition Time to Logical "0" Output	$C_L = 200$ pF (Note 3)		50		ns
Transition Time to Logical "1" Output	$C_L = 200$ pF (Note 3)		75		ns

Note 1: Min/max limits apply across the guaranteed range of -55°C to +125°C for the MH0007, and from 0°C to +85°C for the MH0007C, for all allowable values of V^- and V^+

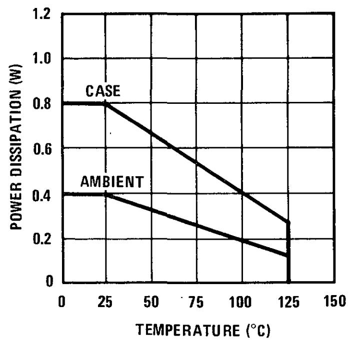
Note 2: All typical values measured at $T_A = 25°C$ with $V_{CC} = 5.0$ volts, $V^- = -25$ volts, $V^+ = 0$ volts.

Note 3: Transition time measured from time V_{IN} = 50% value until V_{OUT} has reached 80% of final value.

Allowable Values for V^- and V^+



Maximum Power Dissipation



Clock Drivers

MH0009/MH0009C dc coupled two phase MOS clock driver

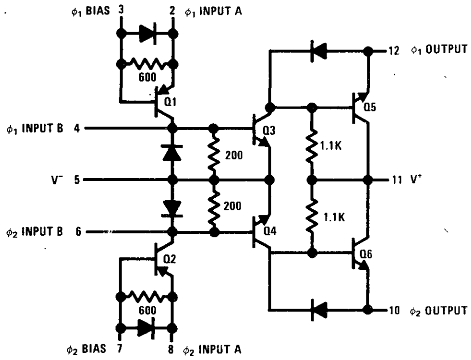
general description

The MH0009/MH0009C is high speed, DC coupled, dual MOS clock driver designed to operate in conjunction with high speed line drivers such as the DM8830, DM7440, or DM7093. The transition from TTL/DTL to MOS logic level is accomplished by PNP input transistors which also assure accurate control of the output pulse width.

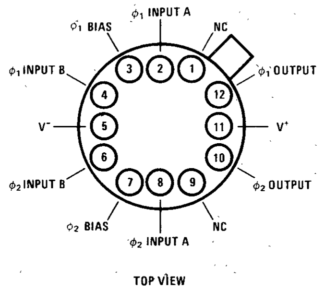
features

- DC logically controlled operation
- Output Swings – to 30V
- Output Currents – in excess of ±500 nA
- High rep rate – in excess of 2 MHz
- Low standby power

schematic and connection diagrams



12-Lead TO-8 Package



typical application

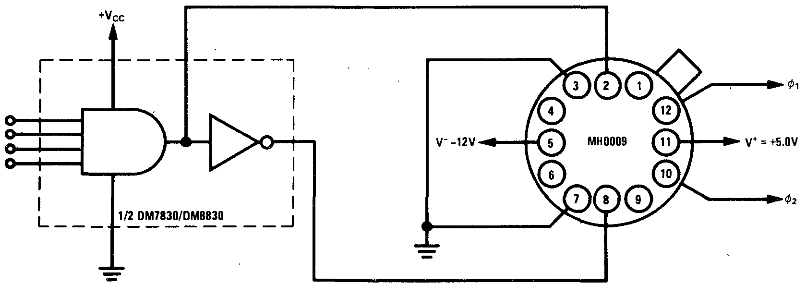


FIGURE 1

absolute maximum ratings

V^- Supply Voltage: Differential (Pin 5 to Pin 3) or (Pin 5 to Pin 7)	−40V
V^+ Supply Voltage: Differential (Pin 11 to Pin 5)	30V
Input Current: (Pin 2, 4, 6 or 8)	±75 mA
Peak Output Current	±500 mA
Power Dissipation (Note 2 and Figure 2)	1.5W
Storage Temperature	−65°C to +150°C
Operating Temperature: MH0009	−55°C to +125°C
MH0009C	0°C to 85°C
Lead Temperature (Soldering, 10 Sec.)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{ON}	C_{IN} = .0022 μF C_L = .001 μF		10	35	ns
t_{rise}	C_{IN} = .0022 μF C_L = .001 μF		40	50	ns
Pulse Width (50% to 50%)	C_{IN} = .0022 μF C_L = .001 μF	340	400	440	ns
t_{fall}	C_{IN} = .0022 μF C_L = .001 μF		80	120	ns
t_{delay}	C_{IN} = 600 pF C_L = 200 pF		10		ns
t_{rise}	C_{IN} = 600 pF C_L = 200 pF		15		ns
Pulse Width (50% to 50%)	C_{IN} = 600 pF C_L = 200 pF	40	70	120	ns
t_{fall}	C_{IN} = 600 pF C_L = 200 pF		40		ns

Note 1: Characteristics apply for circuit of Figure 1. With V^- = −20 volts; V^+ = 0 volts; V_{CC} = 5.0 volts. Minimum and maximum limits apply from −55°C to +125°C for the MH0009 and from 0°C to +85°C for the MH0009C. Typical values are for T_A = 25°C.

Note 2: Transient power is given by $P = fC_L (V^+ - V^-)^2$ watts, where: f = repetition rate, C_L = load capacitance, and $(V^+ - V^-)$ = output swing.

Note 3: For typical performance data see the MH0013/MH0013C data sheet.

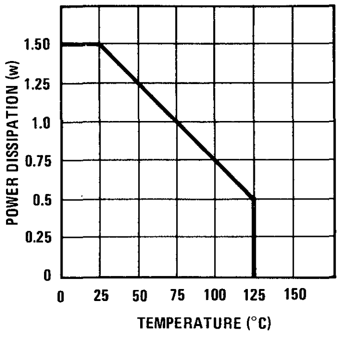


FIGURE 2. Maximum Power Dissipation

Clock Drivers

MH0012/MH0012C high speed MOS clock driver

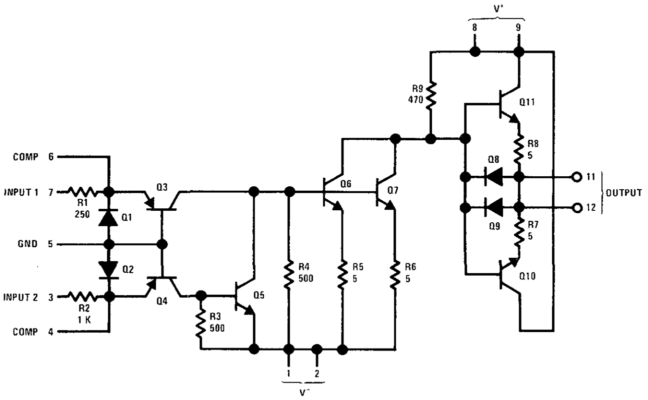
general description

The MH0012/MH0012C is a high performance clock driver that is designed to be driven by the DM7830/DM8830 or other line drivers or buffers with high output current capability. It will provide a fixed width pulse suitable for driving MOS shift registers and other clocked MOS devices.

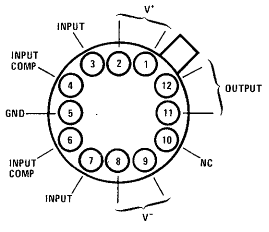
features

- High output voltage swings—12 to 30 volts
- High output current drive capability—1000 mA peak
- High repetition rate—10 MHz at 18 volts into 100 pF
- Low standby power—less than 30 mW

schematic and connection diagrams

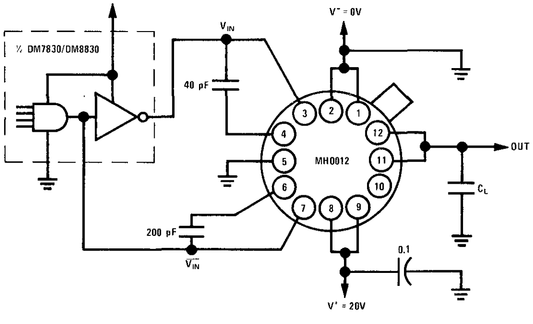


12-lead TO-8 Package

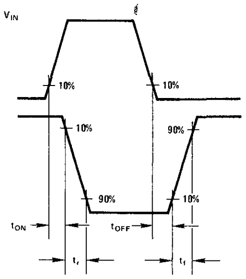


TOP VIEW

typical application (ac test circuit)



timing diagram



absolute maximum ratings

V^- Supply Voltage: Differential (Pin 1 or 2 to Pin 5)	−40V
V^+ Supply Voltage: Differential (Pin 8 or 9 to Pin 1 or 2)	30V
Input Current: (Pin 3 or 7)	±75 mA
Peak Output Current	±1000 mA
Maximum Output Load—See Figure 2	
Power Dissipation—See Figure 1	1.5W
Storage Temperature	−65°C to +150°C
Operating Temperature: MH0012	−55°C to +125°C
MH0012C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

dc electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logic "1" Input Voltage (Pins 7 and 3)	$V^+ - V^- = 20V$, $V_{OUT} \leq V^- + 2V$		1.0	2.0	V
Logic "0" Input Voltage (Pins 7 and 3)	$V^+ - V^- = 20V$, $V_{OUT} \geq V^+ - 1.5V$	0.4	0.6		V
Logic "1" Output Voltage	$V^+ - V^- = 20V$, $I_{OUT} = 1mA$, $V_{IN} = 2.0V$		$V^- + 1.0$	$V^- + 2.0$	V
Logic "0" Output Voltage	$V^+ - V^- = 20V$, $I_{OUT} = -1mA$, $V_{IN} = 0.4V$	$V^+ - 1.5$	$V^+ - 0.7$		V
I_{DC} (V^- Supply)	$V^+ - V^- = 20V$, $V_{IN} = 2.0V$		34	60	mA

ac electrical characteristics

PARAMETER	CONDITIONS (Note 3)	MIN	TYP	MAX	UNITS
Turn-On Delay (t_{ON})	$V^+ - V^- = 20V$, $V_{CC} = 5.0V$ $C_L = 200$ pF, f = 1.0 MHz $T_A = 25°C$		10	15	ns
Rise Time (t_r)			5	10	ns
Turn-Off Delay (t_{OFF})			35	50	ns
Fall Time (t_f)			35	45	ns

Note 1: Characteristics apply for circuit of Figure 1. Min and max limits apply from −55°C to +125°C for the MH0012 and from 0°C to +85°C for the MH0012C. Typical values are for $T_A = 25°C$.

Note 2: Due to the very fast rise and fall times, and the high currents involved, extremely short connections and good by passing techniques are required.

Note 3: All conditions apply for each parameter.

Power Dissipation

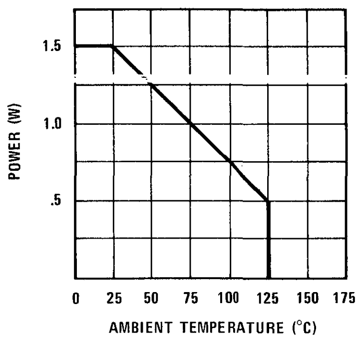


Figure 1.

Maximum Output Load vs Voltage Swing vs Rise Times

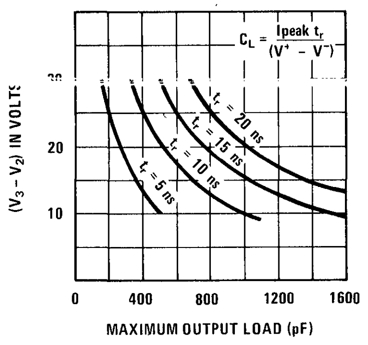
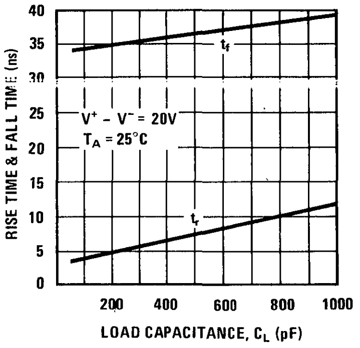


Figure 2.

Rise and Fall Times vs Load Capacitance



applications information

Power Dissipation Considerations

The power dissipated by the MH0012 may be divided into three areas of operation = ON, OFF and switching. The OFF power is approximately 30 mW and is dissipated by R_2 when Pin 3 is in the logic "1" state. The OFF power is neglible and will be ignored in the subsequent discussion. The ON power is dissipated primarily by Q_3 and R_9 and is given by:

$$P_{ON} \cong [|V^-| I_{IN} + \frac{(V^+ - V^-)^2}{R_9}]\ DC \quad (1)$$

Where:

$$DC = \text{Duty Cycle} = \frac{\text{ON Time}}{\text{ON Time \& OFF Time}}$$

I_{IN} is given by $\frac{V_{IN} - V_{BE3}}{R_1}$ and equation (1) becomes:

$$P_{ON} = \left[\frac{(V_{IN} - V_{BE3})|V^-|}{R_1} + \frac{(V^+ - V^-)^2}{R_9}\right] DC \quad (2)$$

For $V_{IN} = 2.5V$, $V_{BE3} = 0.7V$, $V^+ = 0V$, $V^- = -20V$, and DC = 20%, $P_{ON} \cong 200$ mW.

The transient power incurred during switching is given by:

$$P_{AC} = (V^+ - V^-)^2 C_L f \quad (3)$$

For $V^+ = 0V$, $V^- = -20V$, $C_L = 200$ pF, and f = 5.0 MHz, $P_{AC} = 400$ mW.

The total power is given by:

$$P_T = P_{AC} + P_{ON} \quad (4)$$

$$P_T \leq P_{MAX}$$

For the above example, $P_T = 600$ mW.

Clock Drivers

MH0013/MH0013C two phase MOS clock driver

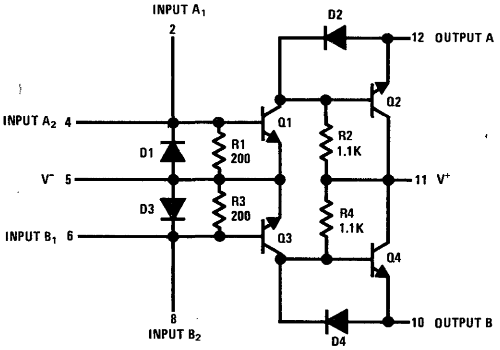
general description

The MH0013/MH0013C is a general purpose clock driver that is designed to be driven by DTL or TTL line drivers or buffers with high output current capability. It will provide fixed width clock pulses for both high threshold and low threshold MOS devices. Two external input coupling capacitors set the pulse width maximum, below which the output pulse width will closely follow the input pulse width or logic control of output pulse width may be obtained by using larger value input capacitors and no input resistors.

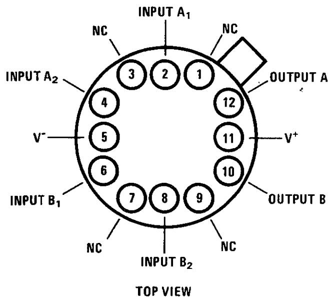
features

- High Output Voltage Swings—up to 30V
- High Output Current Drive Capability—up to 500 mA
- High Repetition Rate—up to 5.0 MHz
- Pin Compatible with the MH0009/MH0009C
- "Zero" Quiescent Power

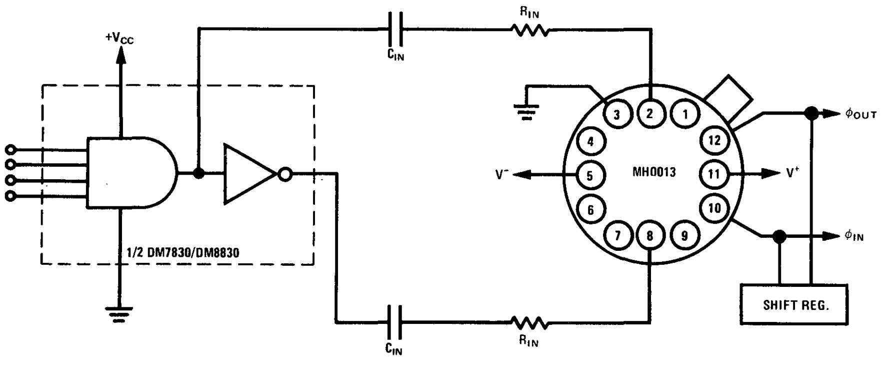
schematic and connection diagrams

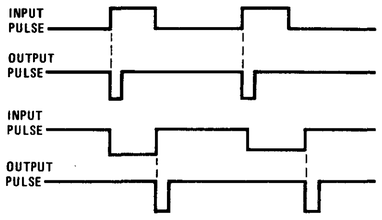


12-Lead TO-8 Package



typical applications





absolute maximum ratings

$(V^+ - V^-)$ Voltage Differential	30V
Input Current (Pin 2, 4, 6 or 8)	±75 mA
Peak Output Current	±600 mA
Power Dissipation (Figure 7)	1.5W
Storage Temperature	−65°C to +150°C
Operating Temperature MH0013	−55°C to +125°C
MH0013C	0°C to +85°C
Lead Temperature (Soldering, 60 sec 1/16" from Case)	300°C

electrical characteristics (Note 1 and Figure 8)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "0" Output Voltage	I_{OUT} = −50 mA I_{IN} = 1.0 mA	$V^+ - 3.0$	$V^+ - 1.0$		V
	I_{OUT} = −10 mA I_{IN} = 1.0 mA		$V^+ - 0.7$	$V^+ - 0.5$	V
Logical "1" Output Voltage	I_{OUT} = 50 mA I_{IN} = 10 mA		$V^- + 1.5$	$V^- + 2.0$	V V
Power Supply Leakage Current	$(V^+ - V^-)$ = 30V $I_{OUT} = I_{IN}$ = 0 mA		1.0	100	µA
Negative Input Voltage Clamp	I_{IN} = − 10 mA	$V^- - 1.2$	$V^- - 0.8$		V
$t_{d\,ON}$			20	35	ns
t_{rise}	C_{IN} = 0.0022 µF		35	50	ns
$t_{d\,OFF}$ (Note 2)	R_{IN} = 0Ω		30	60	ns
t_{fall} (Note 2)	C_L = 0.001 µF	40	50	80	ns
t_{fall} (Note 3)		40	70	120	ns
Pulse Width (50% to 50%) (Note 3)		340	420	490	ns
t_{rise}	C_{IN} = 500 pF		15		ns
t_{fall}	R_{IN} = 0Ω		20		ns
Pulse Width (50% to 50%) (Note 3)	C_L = 200 pF		110		ns
Positive Output Voltage Swing			$V^+ - 0.7V$		V
Negative Output Voltage Swing			$V^- + 0.7V$		V

Note 1: Min/Max limits apply over guaranteed operating temperature range of −55°C to +125°C for MH0013 and 0°C to +85°C for MH0013C, with $V^- = -20V$ and $V^+ = 0V$ unless otherwise specified. Typical values are for 25°C.

Note 2: Parameter values apply for clock pulse width determined by input pulse width.

Note 3: Parameter values apply for input pulse width greater than output clock pulse width.

TABLE I. Typical Drive Capability of One Half MH0013 at 70°C Ambient

$(V^+ - V^-)$ VOLTS	FREQUENCY MHz	PULSE WIDTH ns	TYPICAL R_{IN} Ω	TYPICAL C_{IN} pF	OUTPUT DRIVE CAPABILITY IN pF[1]	RISE TIME LIMIT ns[2]
28					50	–
20	4.0	100	0	750	200	7
16					350	10
28					100	5
20	2.0	200	10	1600	400	14
16					700	19
28					400	19
20	1.0	200	0	2300	1000	34
16					1700	45
28					2800	130
20	0.5	500	10	4000	5500	183
16					9300	248

Note 1: Output load is the maximum load that can be driven at 70°C without exceeding the package rating under the given conditions.

Note 2: The rise time given is the minimum that can be used without exceeding the peak transient output current for the full rated output load.

performance characteristics

FIGURE 1. Output Load vs Voltage Swing

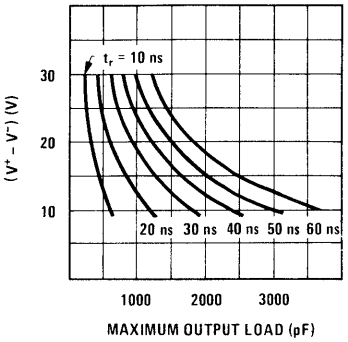


FIGURE 2. Transient Power vs Rep. Rate vs C_L

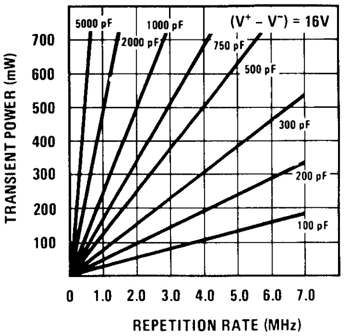
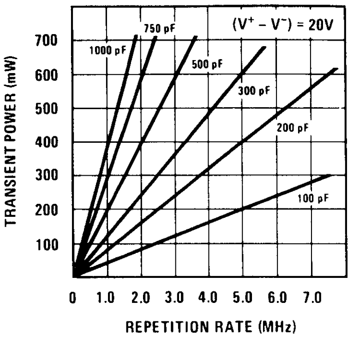


FIGURE 3. Transient Power vs Rep. Rate vs C_L



typical performance (cont.)

FIGURE 4. Average Internal Power vs Output Swing vs Duty Cycle

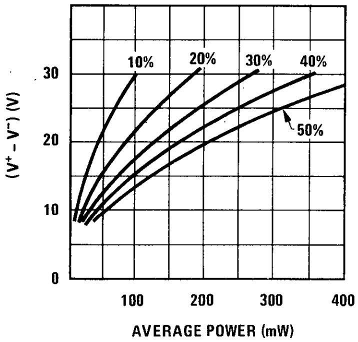


FIGURE 5. Typical Clock Pulse Variations vs Ambient Temperature

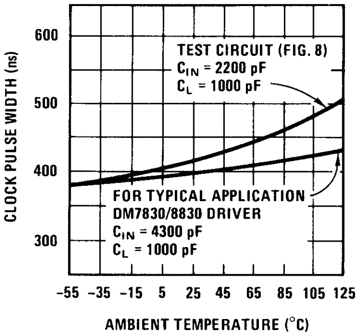


FIGURE 6. R_{IN} vs C_{IN} vs Pulse Width

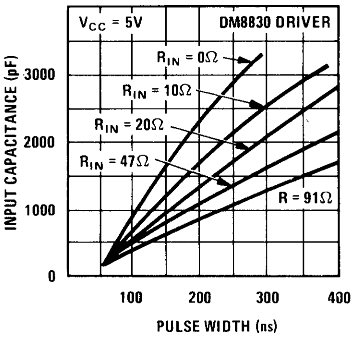
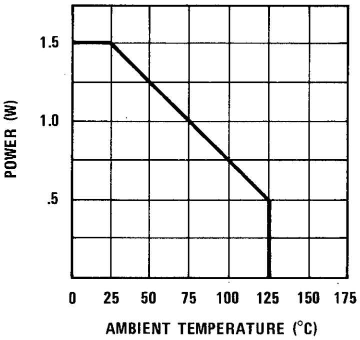


FIGURE 7. Package Power Derating



circuit operation

Input current forced into the base of Q1 through the coupling capacitor C_{IN} causes Q1 to be driven into saturation, swinging the output to $V^- + V_{CE}(SAT) + V_{DIODE}$.

When the input current has decayed, or has been switched, such that Q1 turns off, Q2 receives base drive through R2, turning Q2 on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.

It may be noted that Q1 always switches off before Q2 begins to supply current; hence, high internal transient currents from V^+ to V^- cannot occur.

pulse width

Maximum output pulse width is a function of the input driver characteristics and the coupling capacitance and resistance. After being turned on, the input current must fall from its initial value I_{IN} peak to below the input threshold current I_{IN} min $\simeq V_{BE}/R1$ for the clock driver to turn off. For example, referring to the test circuit of Figure 8, the output pulse width, 50% to 50%, is given by

$$pw_{OUT} \cong \frac{1}{2}(t_{rise} + t_{fall})$$

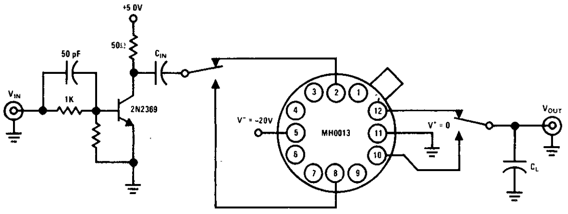
$$+ R_O C_{IN} \ln \frac{I_{IN}\ \text{peak}}{I_{IN}\ \text{min}} \cong 400\ \text{ns}.$$

For operation with the input pulse shorter than the above maximum pulse width, the output pulse width will be directly determined by the input pulse width.

$$pw_{OUT} = pw_{IN} + t_{d\,OFF} + t_{d\,ON} + \frac{1}{2}(t_{fall} + t_{rise})$$

Typical maximum pulse width for various C_{IN} and R_{IN} values are given in Figure 6.

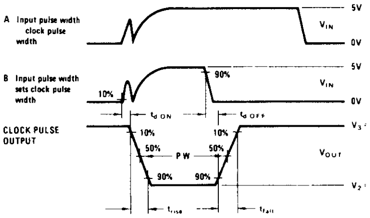
ac test circuit



V_{IN} = 0 to 5V pulse, f = 500 kHz, DC = 50%, t_r and t_f ≲ 10 ns

Figure 8

timing diagram



fan-out calculation

The drive capability of the MH0013 is a function of system requirements, i.e., speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition. Some typical fan-outs for conditions are given in Table 1.

Transient Current

The maximum peak output current of the MH0013 is given as 600 mA. Average transient current required from the driver can be calculated from:

$$I = \frac{C_L\,(V^+ - V^-)}{T_R} \qquad (1)$$

This can give a maximum limit to the load.

Figure 1 shows maximum voltage swing and capacitive load for various rise times.

1. *Transient Output Power*

The average transient power (P_{AC}) dissipated is equal to the energy needed to charge and discharge the output capacitive load (C_L) multiplied by the frequency of operation (F).

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times F \qquad (2)$$

Figures 2 and 3 show transient power for two different values of ($V^+ - V^-$) versus output load and frequency.

2. *Internal Power*

"0" State

Negligible (<3 mW)

"1" State

$$P_{INT} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle.} \qquad (3)$$

Figure 4 gives various values of internal power versus ouptut voltage and duty cycle.

3. *Input Power*

The average input power is a function of the input current and duty cycle. Due to input voltage clamping, this power contribution is small and can therefore be neglected. At maximum duty cycle of 50%, at 25°C, the average input power is less than 10 mW per phase for $R_{IN}C_{IN}$ controlled pulse widths. For pulse widths much shorter than $R_{IN}C_{IN}$, and maximum duty cycle of 50%, input power could be as high as 30 mW, since I_{IN} peak is maintained for the full duration of the pulse width.

4. *Package Power Dissipation*

Total Average Power = Transient Output Power + Internal Power + Input Power

Typical Example *Calculation for One Half MH0013C*

How many MM506 shift registers can be driven by an MH0013C driver at 1 MHz using a clock pulse width of 400 ns, rise time 30–50 ns and 16 volts amplitude over the temperature range 0–70°C?

Power Dissipation

From the graph of power dissipation versus temperature, Figure 7, it can be seen that an MH0013C at 70°C can dissipate 1W without a heat sink; therefore, each half can dissipate 500 mW.

Transient Peak Current Limitation

From Figure 1 (equation 1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 1140 pF.

Average Internal Power

Figure 4 (equation 3) gives an average power of 102 mW at 16V 40% duty cycle.

Input power will be a maximum of 8 mW.

Transient Output Power

For one half of the MH0013C

500 mW = 102 mW + 8 mW
+ transient output power

390 mW = transient output power

Using Figure 2 (equation 2) at 16V, 1 MHz and 390 mW, each half of the MH0013C can drive a 1520 pF load. This is, however, in excess of the load derived from the transient current limitation (Figure 1, equation 1), and so a maximum load of 1140 pF would prevail.

From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is $\frac{1140}{80}$ or 14 registers.

For nonsymmetrical clock widths, drive capability is improved.

Clock Drivers

MH0025/MH0025C two phase MOS clock driver

general description

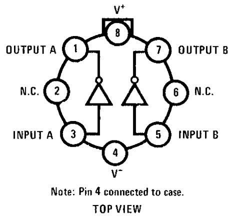
The MH0025/MH0025C is monolithic, low cost, two phase MOS clock driver that is designed to be driven by TTL/DTL line drivers or buffers such as the DM932, DM8830, or DM7440. Two input coupling capacitors are used to perform the level shift from TTL/DTL to MOS logic levels. Optimum performance in turn-off delay and fall time are obtained when the output pulse is logically controlled by the input. However, output pulse widths may be set by selection of the input capacitors eliminating the need for tight input pulse control.

features

- 8-lead TO-5 or 8-lead dual-in-line package
- High Output Voltage Swings—up to 30V
- High Output Current Drive Capability—up to 1.5A
- Rep. Rate: 1.0 MHz into > 1000 pF
- Driven by DM932, DM8830, DM7440(SN7440)
- "Zero" Quiescent Power

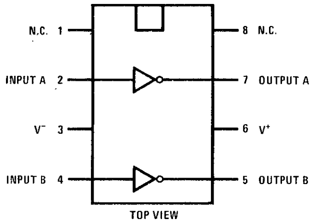
connection diagrams

Metal Can Package



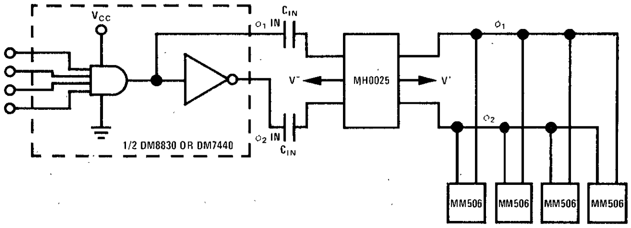
MH0025H, MH0025CH

Dual-In-Line Package

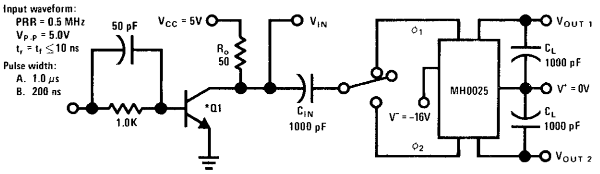


MH0025CN

typical application

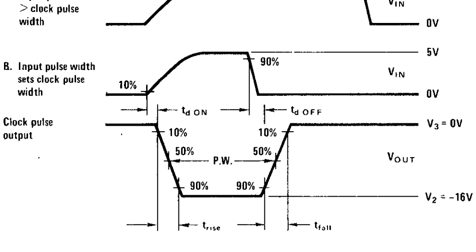


ac test circuit



*Q1 is a selected high speed NPN switching transistor.

timing diagram



absolute maximum ratings

($V^+ - V^-$) Voltage Differential	30V
Input Current	100 mA
Peak Output Current	1.5A
Power Dissipation	See Curves
Storage Temperature	-65°C to +150°C
Operating Temperature MH0025	-55°C to +125°C
MH0025C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1) See test circuit.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$T_{d_{ON}}$	C_{IN} = .001 µF R_{IN} = 0Ω C_L = .001 µF		15	30	ns
T_{rise}			25	50	ns
$T_{d_{OFF}}$ (Note 2)			30	60	ns
T_{fall} (Note 2)		60	90	120	ns
T_{fall} (Note 3)		100	150	250	ns
P.W. (50% to 50%) (Note 3)			500		ns
Positive Output Voltage Swing	V_{IN} = 0V, I_{OUT} = −1 mA	$V^+ - 1.0$	$V^+ - 0.7V$		V
Negative Output Voltage Swing	I_{IN} = 10 mA, I_{OUT} = 1 mA		$V^- + 0.7V$	$V^- + 1.5V$	V

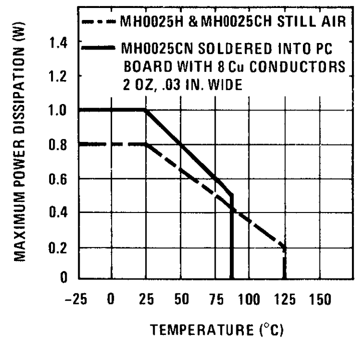
Note 1. Min/Max limits apply across the guaranteed operating temperature range of −55°C to +125°C for MH0025 and 0°C to 85°C for MH0025C. Typical values are for +25°C.

Note 2. Parameter values apply for clock pulse width determined by input pulse width.

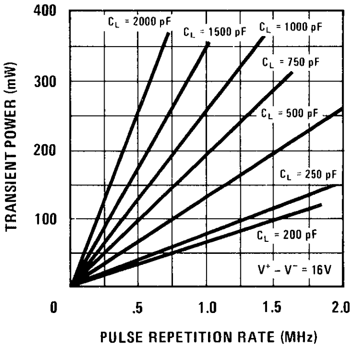
Note 3. Parameter values apply for input pulse width greater than output clock pulse width.

performance characteristics

Package Power Derating

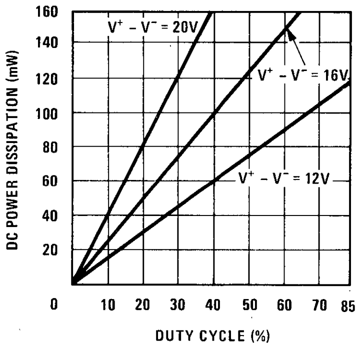


Transient Power vs Rep. Rate



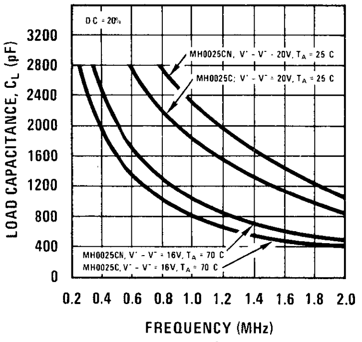
$P_{AC} = (V^+ - V^-)^2 f C_L$

DC Power (P_{DC}) vs Duty Cycle



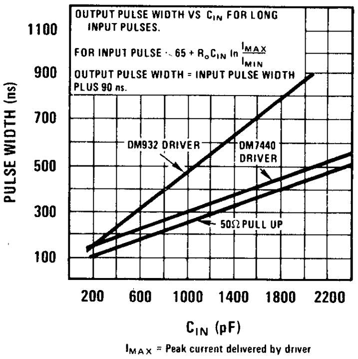
$P_{DC} = \frac{(V^+ - V^-)^2 (DC)}{1k}$

Maximum Load Capacitance



$$C_L \leq \frac{(P_{MAX})(1k) - (V^+ - V^-)^2 (DC)}{(f)(1k)(V^+ - V^-)^2} \leq \frac{(I_{pk})(t_r)}{V^+ - V^-}$$

Output P.W. Controlled by C_{IN}



I_{MAX} = Peak current delivered by driver

$I_{MIN} \geq \frac{V_{BE}}{R_1} = \frac{0.6}{1k}$

applications information

Circuit Operation

Input current forced into the base of Q_1 through the coupling capacitor C_{IN} causes Q_1 to be driven into saturation, swinging the output to $V^- + V_{CE}(sat) + V_{Diode}$.

When the input current has decayed, or has been switched, such that Q_1 turns off, Q_2 receives base drive through R_2, turning Q_2 on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.

It may be noted that Q_1 must switch off before Q_2 begins to supply current, hence high internal transients currents form V^- to V^+ cannot occur.

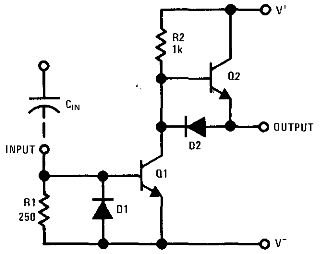


FIGURE 1. MH0025 Schematic (One-Half Circuit)

Fan-Out Calculation

The drive capability of the MH0025 is a function of system requirements, i.e. speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition.

Transient Current

The maximum peak output current of the MH0025 is given as 1.5A. Average transient current required from the driver can be calculated from:

$$I = \frac{C_L\,(V^+ - V^-)}{t_r} \qquad (1)$$

Typical rise times into 1000 pF load is 25 ns For $V^+ - V^- = 20V$, $I = 0.8A$.

Transient Output Power

The average transient power (P_{ac}) dissipated, is equal to the energy needed to charge and discharge the output capacitive load (C_L) multiplied by the frequency of operation (f).

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times f \qquad (2)$$

For $V^+ - V^- = 20V$, f = 1.0 MHz, C_L = 1000 pF, P_{AC} = 400 mW.

Internal Power

"0" State Negligible (<3 mW)

"1" State

$$P_{int} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle} \qquad (3)$$

$$= 80\text{ mW for } V^+ - V^- = 20V,\ DC = 20\%$$

Package Power Dissipation

Total average power = transient output power + internal power

example calculation

How many MM506 shift registers can be driven by an MH0025CN driver at 1 MHz using a clock pulse width of 200 ns, rise time 30-50 ns and 16V amplitude over the temperature range 0-70°C?

Power Dissipation:

At 70°C the MH0025CN can dissipate 630 mW when soldered into printed circuit board.

Transient Peak Current Limitation:

From equation (1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 2800 pF.

Average Internal Power:

Equation (3), gives an average power of 50 mW at 16V and a 20% duty cycle.

For one half of the MH0025C, 630 mW ÷ 2 can be dissipated.

315 mW = 50 mW + transient output power

265 mW = transient output power

Using equation (2) at 16V, 1 MHz and 250 mW, each half of the MH0025CN can drive a 975 pF load. This is, less than the load imposed by the transient current limitation of equation (1) and so a maximum load of 975 pF would prevail.

From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is $\frac{975}{80}$ or 12 registers.

Clock Drivers

MH0026/MH0026C 5 MHz two phase MOS clock driver

general description

The MH0026/MH0026C is a low cost monolithic high speed two phase MOS clock driver and interface circuit. Unique circuit design along with advanced processing provide both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. It may be driven from standard 54/74 series gates and flip-flops or from drivers such as the DM8830 or DM7440. The MH0026 is intended for applications in which the output pulse width is logically controlled: i.e., the output pulse width is equal to the input pulse width.

features

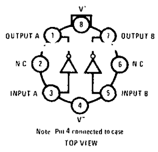
- Fast rise and fall times—20 ns with 1000 pF load
- High output swing—20V
- High output current drive—±1.5 amps
- TTL/DTL compatible inputs
- High rep rate—5 to 10 MHz depending on load
- Low power consumption in MOS "O" state—2 mW
- Drives to 0.4V of GND for RAM address drive

The MH0026 is intended to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for a 8k by 16 bit MM1103 RAM memory system. Information on the correct usage of the MH0026 in these as well as other systems is included in the application section starting on page 134. A thorough understanding of its usage will insure optimum performance of the device.

The device is available in 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, and one and a half watt TO-8 packages.

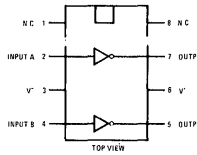
connection diagrams

8-Lead TO-5



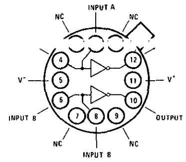
MH0026H/MH0026CH

8-Lead Dual-In-Line Package



MH0026CN

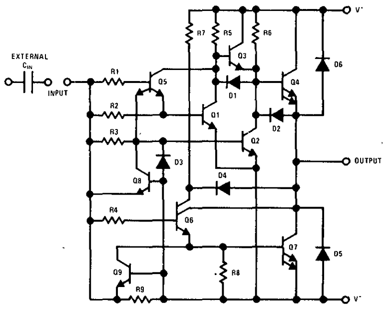
12-Lead TO-8



MH0026G/MH0026CG

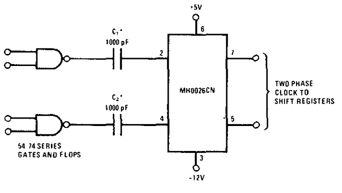
schematic diagram

(1/2 of Circuit Shown)



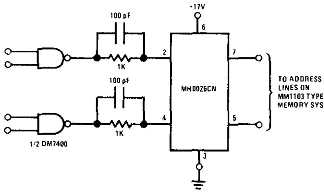
typical applications

AC Coupled MOS Clock Driver



*See applications section on page 134 or detailed information on input/output design criterior.

DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)



absolute maximum ratings (Notes 1 & 2)

$V^+ - V^-$ Differential Voltage		22V
Input Current		100 mA
Input Voltage ($V_{IN} - V^-$)		5.5V
Peak Output Current		1.5A
Power Dissipation		See curves
Operating Temperature Range	MH0026	-55°C to +125°C
	MH0026C	0°C to 85°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

dc electrical characteristics

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Logic "1" Input Voltage	$V_{OUT} = V^- + 1.0V$	2.5	1.5		V
Logic "1" Input Current	$V_{IN} - V^- = 2.5V$, $V_{OUT} = V^- + 1.0V$		10	15	mA
Logic "0" Input Voltage	$V_{OUT} = V^+ - 1.0V$		0.6	0.4	V
Logic "0" Input Current	$V_{IN} - V^- = 0V$, $V_{OUT} = V^+ - 1.0V$		-0.005	-10	μA
Logic "0" Output Voltage	$V^+ = +5.0V$, $V^- = -12.0V$ $V_{IN} = -11.6$	4.0	4.3		V
Logic "0" Output Voltage	$V_{IN} - V^- = 0.4V$	$V^+ - 1.0$	$V^+ - 0.7$		V
Logic "1" Output Voltage	$V^+ = +5.0V$, $V^- = -12.0V$ $V_{IN} = -9.5V$		-11.5	-11.0	V
Logic "1" Output Voltage	$V_{IN} - V^- = 2.5V$		$V^- + 0.5$	$V^- + 1.0$	V
"ON" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 2.5V$		30	40	mA
"OFF" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 0.0V$		10	100	μA

ac electrical characteristics (Notes 1 & 2, AC test circuit)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Turn-On Delay (t_{ON})		5.0	7.5	12	ns
Turn-Off Delay (t_{OFF})		5.0	12	15	ns
Rise time (t_r) – Note 3	$V^+ - V^- = 17V$, $C_L = 250$ pF		12		ns
	$V^+ - V^- = 17V$, $C_L = 500$ pF		15	18	ns
	$C_L = 1000$ pF		20	35	ns
Falltime (t_f) – Note 3	$V^+ - V^- = 17V$, $C_L = 250$ pF		10		ns
	$V^+ - V^- = 17V$, $C_L = 500$ pF		12	16	ns
	$C_L = 1000$ pF		17	25	ns

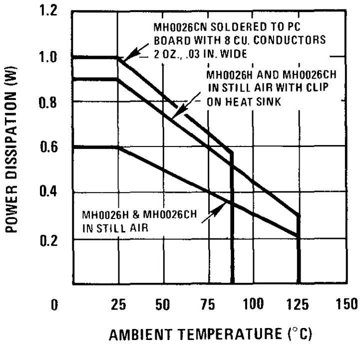
Note 1: These specifications apply for $V^+ - V^- = 10V$ to 20V, $C_L = 1000$ pF, over the temperature range -55°C to +125°C for the MH0026 and 0°C to +85°C for the MH0026C.

Note 2: All typical values for the $T_A = 25°C$.

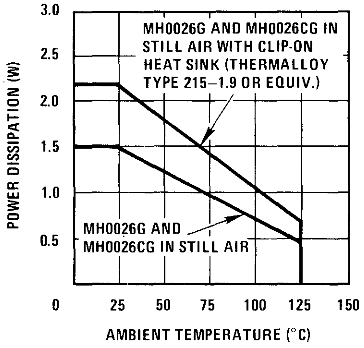
Note 3: Rise and fall time are given for MOS logic levels; i.e., rise time is transistion from logic "0" to logic "1" which is voltage fall. See waveforms on page 133.

typical performance characteristics

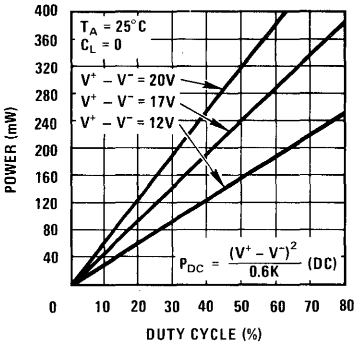
TO-5 & DIP Power Ratings



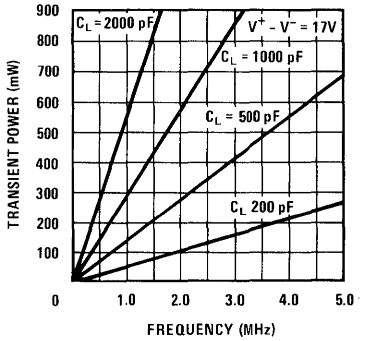
TO-8 Package Power Rating



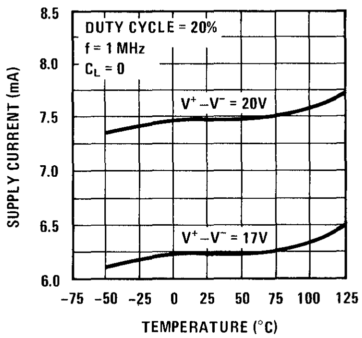
DC Power (P_{DC}) vs Duty Cycle



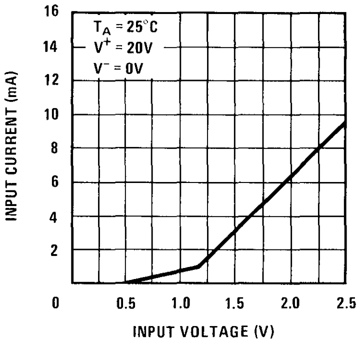
Transient Power (P_{AC}) vs Frequency



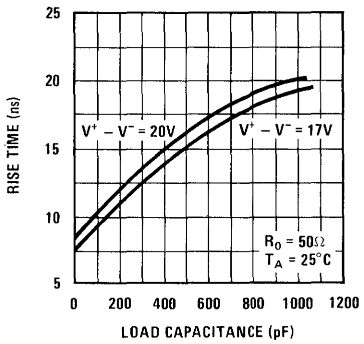
Supply Current vs Temperature



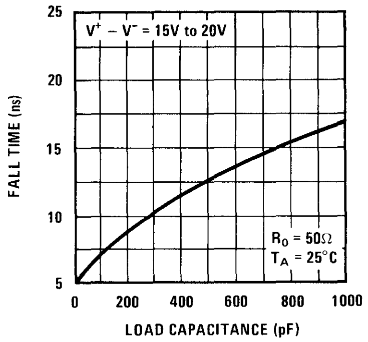
Input Current vs Input Voltage



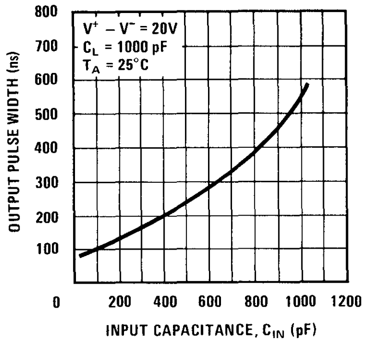
Rise Time vs Load Capacitance



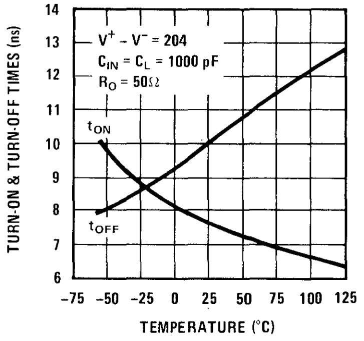
Fall Time vs Load Capacitance



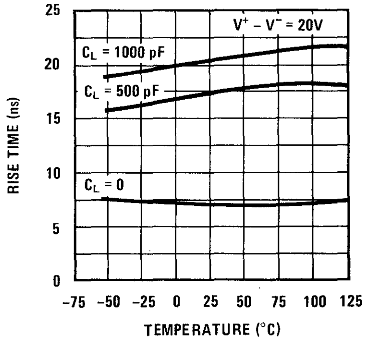
Optimum Input Capacitance vs Output Pulse Width



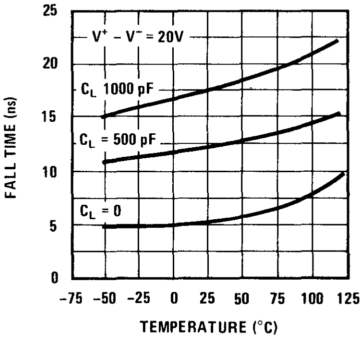
Turn-On & Turn-Off Time vs Temperature



Rise Time vs Temperature

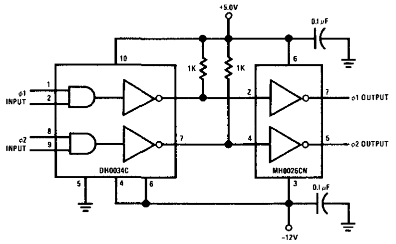


Fall Time vs Temperature

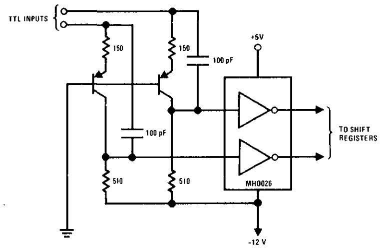


typical applications

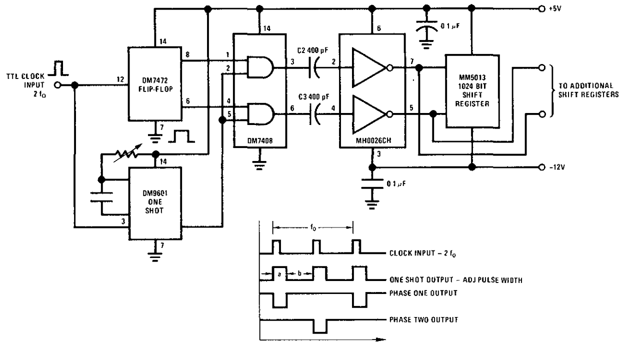
DC Coupled MOS Clock Driver



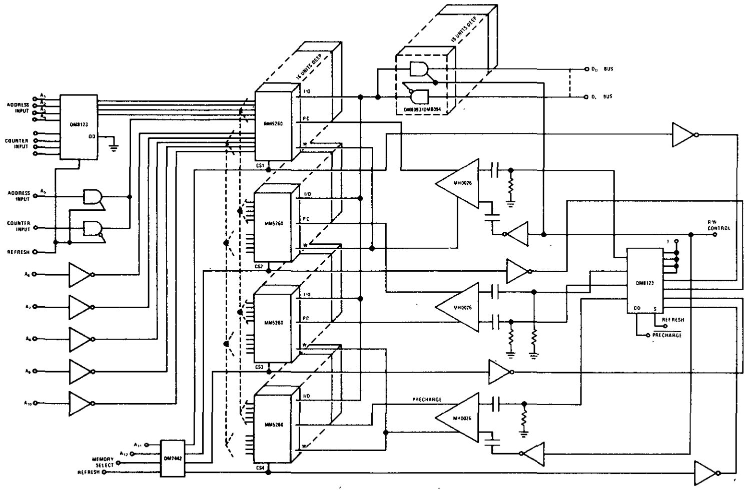
Transistor Coupled MOS Clock Driver



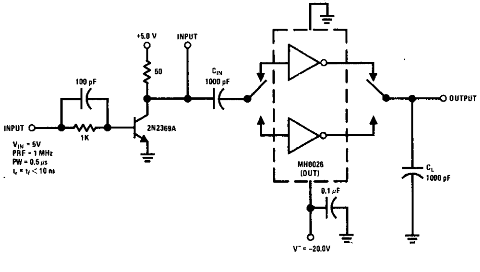
Logically Controlled AC Coupled Clock Driver



Precharge Driver for MOS RAM Memories

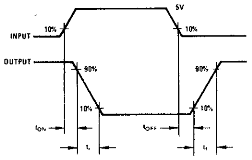


ac test circuit



$V_{IN} = 5V$
PRF = 1 MHz
PW = 0.5 μs
$t_r = t_f < 10$ ns

switching time waveforms



application information

1.0 Introduction

The MH0026 is capable of delivering 30 watts peak power (1.5 amps at 20V needed to rapidly charge large capacitative loads) while its package is limited to the watt range. This section describes the operation of the circuit and how to obtain optimum system performance. If additional design information is required, please contact your local National field application engineer.

2.0 Theory of Operation

Conventional MOS clock drivers like the MH0013 and similar devices have relied on the circuit configuration in Figure 1. The AC coupling of an input pulse allows the device to work over a wide range of supplies while the output pulse width may be controlled by the time constant – $R_1 \times C_1$.

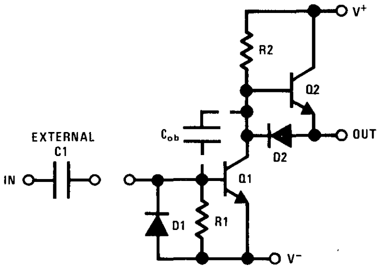


FIGURE 1. Conventional MOS Clock Drive

D_2 provides 0.7V of dead-zone thus preventing Q_1 and Q_2 from conducting at the same time. In order to drive large capacitive loads, Q_1 and Q_2 are large geometry devices but C_{ob} now limits useful output rise time. A high voltage TTL output stage (Figure 2) could be used; however, during switching until the stored charge is removed from Q_1, both output devices conduct at the same time. This is familiar in TTL with supply line glitches in the order of 60 to 100 mA. A clock driver built this way would introduce 1.5 amp spikes into the supply lines.

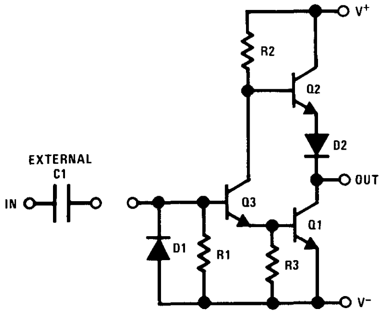


FIGURE 2. Alternate MOS Clock Drive

Unique circuit design and advanced semiconductor processing overcome these clasic problems allowing the high volume manufacture of a device, the MH0026, that delivers 1.5A peak output currents with 20ns rise and fall times into 1000pF loads. In a simplified diagram, D_1 (Figure 3) provides 0.7V dead zone so that Q_3 is turned ON for a rising input pulse and Q_2 OFF prior to Q_1 turning ON a few nanoseconds later. D_2 prevents zenering of the emitter-base junction of Q_2 and provides an initial discharge path for the load via Q_3. During a falling input, the stored charge in Q_3 is used beneficially to keep Q_3 ON thus preventing Q_2 from conducting until Q_1 is OFF. Q_1 stored charge is quickly discharged by means of common-base transistor Q_4.

The complete circuit of the MH0026 (see schematic on page 130 basically makes Darlingtons out of each of the transistors in Figure 3.

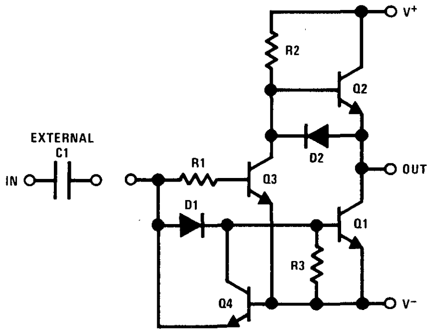


FIGURE 3. Simplified MH0026

When the output of the TTL input element (not shown) goes to the logic "1" state, current is supplied through C_{IN} to the base of Q_1 and Q_2 turning them ON, and Q_3 and Q_4 OFF when the input voltages reaches 0.7V. Initial discharge of the load as well as E-B protection for Q_3 and Q_4 are provided by D_1 and D_2. When the input voltage reaches about 1.5V, Q_6 and Q_7 begin to conduct and the load is rapidly discharged by Q_7. As the input goes low, the input side of C_{IN} goes negative with respect to V^- causing Q_8 and Q_9 to conduct momentarily to assure rapid turn-off of Q_2 and Q_7 respectively. When Q_1 and Q_2 turn OFF, Darlington connected Q_3 and Q_4 rapidly charge the load toward V^+ volts. R_6 assures that the output will reach to within one V_{BE} of the V^+ supply.

The real secret of the device's performance is proper selection of transistor geometries and resistor values so that Q_4 and Q_7 do not conduct at the same time while minimizing delay from input to output.

3.0 Power Dissipation Considerations

There are four considerations in determining power dissipations.

1. Average DC power
2. Average AC power
3. Package and heat sink selection
4. Remember—2 drivers per package

application information (con't)

The total average power dissipated by the MH0026 is the sum of the DC power and AC transient power. The total must be less than given package power ratings.

$$P_{DISS} = P_{AC} + P_{DC} \leq P_{MAX}$$

Since the device dissipates only 2mW with output voltage high (MOS logic "0"), the dominating factor in average DC power is duty cycle or the percent of time in output voltage low state (MOS logic "1"). Percent of total power contributed by P_{DC} is usually neglible in shift register applications where duty cycle is less than 25%. P_{DC} dominates in RAM address line driver applications where duty cycle can exceed 50%.

3.1 DC Power (per driver)

DC Power is given by:

$$P_{DC} = (V^+ - V^-) \times (I_{S(Low)}) \times$$

$$\left(\frac{\text{ON time}}{\text{OFF time—ON time}}\right)$$

or P_{DC} = (Output Low Power) X (Duty Cycle)

where: $I_{S(Low)} = I_S @ V^+ - V^- = \frac{V_S}{20V}$

Example 1: $(V^+ = +5V,\ V^- = -12V)$

a) Duty cycle = 25%, therefore

P_{DC} = 17V X 40mA X 17/20 X 25%

P_{DC} = 145mW worst-case, each side

P_{DC} = 109mW typically

b) Duty cycle = 5%

P_{DC} = 21mW

c) See graph on page 132

The above illustrates that for shift register applications, the minimum clock width allowable for the given type of shift register should be used in order to drive the largest number of registers per clock driver.

Example 2: $(V^+ = +17V,\ V^- = GND)$:

a) Duty cycle = 50%

P_{DC} = 290mW worst-case

P_{DC} = 218mW typically

b) Duty cycle = 100%

P_{DC} = 580mW

Thus for RAM address line applications, package type and heat sink technique will limit drive capability rather than AC power.

3.2 AC Transient Power (per driver)

AC Transient power is given by:

$$P_{AC} = (V^+ - V^-)^2 \times f \times C_L$$

where: f = frequency of operation

C_L = Load capacitance (including all strays and wiring)

Example 3: $(V^+ = +5V,\ V^- = -12V)$

$$P_{AC} = 17 \times 17 \times f(\text{MHz}) \times 10^6 \times$$

$$C_L(\text{nF}) \times 10^{-9}$$

P_{AC} = 290mW per MHz per 1000pF

Thus at 5MHz, a 1000pF load will cause any driver to dissipate one and one half watts. For long shift registers, a driver with the highest package power rating will drive the largest number of bits for the lowest cost per bit.

3.3 Package Selection

Power ratings are based on a maximum junction rating of 175°C. The following guidelines are suggested for package selection. Graphs on page 132 illustrate derating for various operating temperatures.

3.31 TO-5 ("H") Package: Rated at 600mW still air (derate at 4.0mW/°C above 25°C) and 900mW with clip on heat sink (derate at 6.0mW/°C above 25°C). This popular hermetic package is recommended for small systems. Low cost (about 10¢) clip-on-heat sink increases driving capability by 50%.

3.32 8-Pin ("N") Molded Mini-DIP: Rated at 600mW still air (derate at 4.0mW/°C above 25°C) and 1.0 watt soldered to PC board (derate at 6.6mW/°C). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600mW when mounted in a socket and not one watt until it is soldered down.)

3.33 TO-8 ("G") Package: Rated at 1.5 watts still air (derate at 10mW/°C above 25°C) and 2.3 watts with clip on heat sink (Thermalloy type 215-1.9 or equivalent—derate at 15mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

application information (con't)

3.4 Summary—Package Power Considerations

The maximum capacitative load that the MH0026 can drive is thus determined by package type, heat sink technique, ambient temperature, AC power (which is proportional to frequency and capacitive load) and DC power (which is principally determined by duty cycle). Combining equations previously given, the following formula is valid for any clock driver with negligible input power and negligible power in output high state:

$$C_L \text{ (max in pF)} = \frac{10^{-3}}{n} \times \frac{P_{max(mW)}(T_A, pkg) \times R_{eq} - (V^+ - V^-)^2 \times (Dc) \times 10^3}{(V^+ - V^-)^2 \times R_{eq} \times f(MHz)}$$

$$C_L \text{ (max in pF)} = .5 \times 10^{-3} \times \frac{P_{max}(mW) \times 500 - V_S{}^2 \times Dc \times 10^3}{V_S{}^2 \times 500 \times f(MHz)}$$

Where: n = number of drivers per pkg. (2 for the MH0026)

$P_{max(mW)}(T_A, \text{pkg})$ = Package power rating in milliwatts for given package, heat sink, and max, ambient temperature (See graphs)

R_{eq} = equivalent internal resistance

$R_{eq} = (V^+ - V^-)/I_{S(Low)}$ = 500 ohms (worst case over temperature for the MH0026 or 660 ohms typically)

$V_S = (V^+ - V^-)$ = total supply voltage across device

Dc = Duty Cycle =

$$\frac{\text{Time in output low state}}{\text{Time in output low + Time in output high state}}$$

Table I illustrates MH0026 drive capability under various system conditions.

4.0 Pulse Width Control

The MH0026 is intended for applications in which the input pulse width sets the output pulse width; i.e., the output pulse width is logically controlled by the input pulse. The output pulse width is given by:

$$(PW)_{OUT} = (PW)_{IN} + t_r + t_f = PW_{IN} + 25ns$$

Two external input coupling capacitors are required to perform the level translation between TTL/DTL and MOS logic levels. Selection of the capacitor size is determined by the desired output pulse width. Minimum delay and optimum performance is attained when the voltage at the input of the MH0026 discharges to just above the devices threshold (about 1.5V). If the input is allowed to discharge below the threshold, t_{OFF} and t_f will be degraded. The graph on page 132 shows optimum values for C_{IN} vs desired output pulse width. The value for C_{IN} may be roughly predicted by:

$$C_{IN} = (2 \times 10^{-3})\,(PW)_{OUT}$$

For an output pulse width of 500ns, the optimum value for C_{IN} is:

$$C_{IN} = (2 \times 10^{-3})(500 \times 10^{-9}) \cong 1000pF$$

5.0 Rise & Fall Time Considerations(Note 3)

The MH0026's peak output current is limited to 1.5A. The peak current limitation restricts the maximum load capacitance which the device is capable of driving and is given by:

$$I = C_L \frac{dv}{dt} \leqslant 1.5A$$

The rise time, t_r, for various loads may be predicted by:

$$t_r = (\Delta V)(250 \times 10^{-12} + C_L)$$

Where: ΔV = The change in voltage across C_L

$\cong V^+ - V^-$

C_L = The load capacitance

For $V^+ - V^- = 20V$, $C_L = 1000pF$, t_r is:

$$t_r \cong (20V)(250 \times 10^{-12} + 10^{-12}) = 25ns$$

TABLE 1. Worst Case Maximum Drive Capability for MH0026*

PACKAGE TYPE		TO-8 WITH HEAT SINK		TO-8 FREE AIR		MINI-DIP SOLDERED DOWN		TO-5 AND MINI-DIP FREE AIR	
Max. Operating Frequency ↓	Max. Ambient Temp. → Duty Cycle	60°C	85°C	60°C	85°C	60°C	85°C	60°C	85°C
100kHz	5%	30 k	24 k	19 k	15 k	13 k	10k	7.5k	5.8k
500kHz	10%	6.5k	5.1k	4.1k	3.2k	2.7k	2k	1.5k	1.1k
1MHz	20%	2.9k	2.2k	1.8k	1.4k	1.1k	840	600	430
2MHz	25%	1.4k	1.1k	850	650	550	400	280	190
5MHz	25%	620	470	380	290	240	170	120	80
10MHz	25%	280	220	170	130	110	79	–	–

***NOTE:** Values in pF and assume both sides in use as non-overlaping 2 phase driver; each side operating at same frequency and duty cycle with $(V^+ - V^-) = 17V$

application information (con't)

For small values of C_L, equation above predicts optimistic values for t_r. The graph on page 132 shows typical rise times for various load capacitances.

The output fall time (see Graph) may be predicted by:

$$t_f \cong 2.2R\left(C_S + \frac{C_L}{h_{FE} + 1}\right)$$

6.0 Clock Overshoot

The output waveform of the MH0026 can overshoot. The overshoot is due to finite inductance of the clock lines. It occurs on the negative going edge when Q_7 saturates, and on the positive edge when Q_3 turns OFF as the output goes through $V^+ - V_{be}$. The problem can be eliminated by placing a small series resistor in the ouput of the MH0026. The critical valve for $R_s = 2\sqrt{LCL}$ where L is the self-inductance of the clock line. In practice, determination of a value for L is rather difficult. However,R_s is readily determined emperically, and values typically range between 10 and 51 ohms. R_s does reduce rise and fall times as given by:

$$t_r = t_f \cong 2.2R_SC_L$$

7.0 Clock Line Cross Talk

At the system level,voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice-versa) during the transition of ϕ_1 to MOS logic "1". The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. Transistors Q_3 and Q_4 on the ϕ_2 side of the MH0026 are essentially "OFF" when ϕ_2 is in the MOS logic "0" state since only micro-amperes are drawn from the device. When the spike is coupled to ϕ_2, the output has to drop at least 2 V_{BE} before Q_3 and Q_4 come on and pull the output back to V^+. A simple method for eliminating or minimizing this effect is to add bleed resistors between the MH0026 outputs and ground causing a current of a few milliamps to flow in Q_4. When a spike is coupled to the clock line Q_4 is already "ON" with a finite h_{fe}. The spike is quickly clamped by Q_4. Values for R depend on layout and the number of registers being driven and vary typically between 2k and 10k ohms.

8.0 Power Supply Decoupling

Power supply decoupling is a widespread and accepted practice. Decoupling of V^+ to V^- supply lines with at least 0.1 μF noninductive capacitors as close as possible to each MH0026 is strongly recommended. This decoupling is necessary because otherwise 1.5 ampere currents flow during logic transition in order to rapidly charge clock lines.

MH0027C dual high speed MOS interface driver

general description

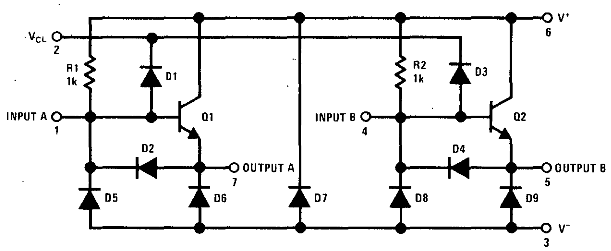
The MH0027C is a dual high current active pull-up designed to operate with a high current sink such as the DH0034 or LM7541A and thus provides fully TTL compatible DC coupled inputs. The partitioning of current sinks and sources into separate packages provides higher overall power drive capability while minimizing system cost. The device is intended for use as a driver for MOS RAM memories such as the MM1103. The MH0027C is capable of sourcing over 1 ampere peak current with a rise-time of 25 ns into 600 pF loads.

features

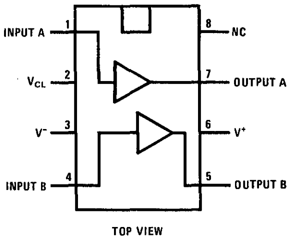
- Fast rise times – 25 ns into 600 pF load
- Peak output current in excess of 1 ampere
- Fully compatible with DH0034 dual level shifter and LM75450 series peripheral drivers.
- Wide operating supply range – 5V to 25V
- Output voltage clamp
- Low power dissipation – 1 mW typical in logic "1" state

The MH0027C operates over an ambient temperature range of 0°C to +85°C and is supplied in a miniature 8-pin molded dual-in-line package.

schematic and connection diagrams

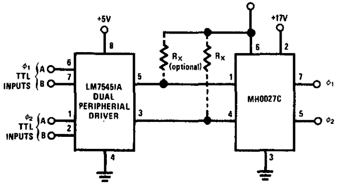


Dual-In-Line Package



typical applications

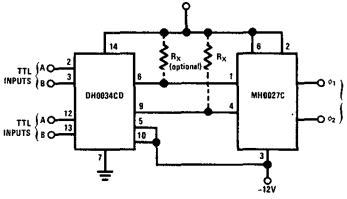
TTL to MM1103 High Speed Memory Interface



To MM1103 4k by 16 bit memory array. Rise and fall time are 25 ns typ into 600 pF load

Note: Minimize stray board capacitance on interconnections between LM75451A and MH0027CN Optional external pull-up resistors (R_X = 1k) may be added to improve rise time by about a factor of 2.

TTL to Negative Level Interface
(DC Coupled MOS Clock)



Output swing – -11V to 4V, delay time – 20 ns
Rise and fall time – 25 ns for C_L = 600 pF

Note: R_X (1k) Optional to decrease rise time

absolute maximum ratings

Continuous Supply Voltage	25V
Peak Supply Voltage (10 ms)	30V
Input Voltage	25V
Output Voltage	V_{CC}
Peak Output Current (each side)	1.2A
Power Dissipation (Note 1)	1.0W
Operating Temperature Range	0°C to 85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (T_A = +25°C, V^+ = 24V, V_{CL} = 21V; unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Low Level Input Current (I_{IL})	V_{IN} = 0V	18	25	32	mA
High Level Output Voltage (V_{OH})	I_{OH} = 4 mA	20.75	21.0	21.25	V
Low Level Output Voltage (V_{OL})	I_{OL} = 100 mA		0.7	1.0	V
Turn-On Time (t_{dON})	C_L = 600 pF		5	15	ns
Turn-Off Time (t_{dOFF})	C_L = 600 pF		5	15	ns
Rise Time (t_r)	C_L = 600 pF		20	45	ns
Fall Time (t_f)	C_L = 600 pF		15	35	ns

Note 1: Rating applies for device soldered to a printed circuit board with 8 copper conductors .03 inches wide. For ambient temperatures above 25°C, derate linearly at 6.7 mW/°C.

For specifications on other National MOS clock drivers and interface circuits, see the following data sheets:

MOS Clock Drivers

Single Phase, TTL Input DC Coupled – MH0007
Two Phase DC Coupled – MH0009
Single Phase, High Speed DC Coupled – MH0012
Two Phase AC Coupled – MH0013
Two Phase Low Cost – MH0025
Two Phase High Speed AC Coupled – MH0026

MOS Interface Circuits

Dual Voltage Translator – DM7800/DM8800
Dual High Speed Translator – DH0034/DH0034C
Quad 2-Input NAND TTL/MOS Interface – DM8810,DM8811
Quad 2-Input AND TTL/MOS Interface – DM8810
Hex Inverter TTL/MOS Interface – DM8812
Dual Peripherial Drivers – LM350,LM351/LM75450A,LM75451A
Analog Comparator to MOS – LM111 series
Dual Analog Comparator to MOS – LH2111 series

Analog Switches

MM450/MM550, MM451/MM551 MM452/MM552, MM455/MM555 MOS analog switches

general description

The MM450, and MM550 series each contain four p channel MOS enhancement mode transistors built on a single monolithic chip. The four transistors are arranged as follows:

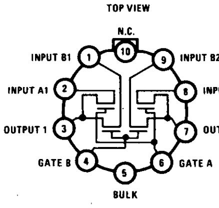
MM450, MM550	Dual Differential Switch
MM451, MM551	Four Channel Switch
MM452, MM552	Four MOS Transistor Package
MM455, MM555	Three MOS Transistor Package

These devices are useful in many airborne and ground support systems requiring multiplexing, analog transmission, and numerous signal routing applications. The use of low threshold transistors (V_{TH} = 2 volts) permits operations with large analog input swings (± 10 volts) at low gate voltages (−20 volts). Significant features, then, include:

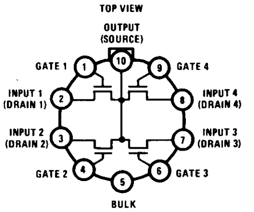
- Large Analog Input Swing ±10 Volts
- Low Supply Voltage V_{BULK} = +10 Volts, V_{GG} = −20 Volts
- Low ON Resistance V_{IN} = −10V 150Ω, V_{IN} = +10V 75Ω
- Low Leakage Current 200 pA @ 25°C
- Input Gate Protection
- Zero Offset Voltage

Each gate input is protected from static charge build-up by the incorporation of zener diode protective devices connected between the gate input and device bulk.

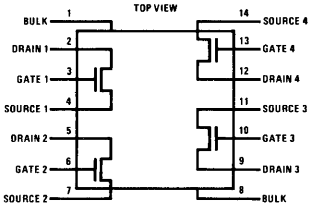
schematic and connection diagrams



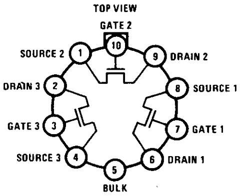
NOTE: Pin 5 connected to case and device bulk.
MM450, MM550



NOTE: Pin 5 connected to case and device bulk.
MM451, MM551

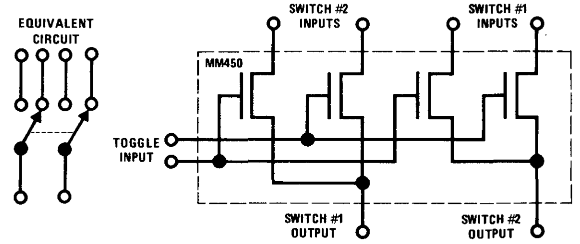


NOTE 1: Pins 1 and 8 connected to case and device bulk. Drain and Source may be interchanged. MM452F, MM552F.
NOTE 2: MM452D and MM552D (dual-in-line packages) have same pin connections as MM452F and MM552F shown above.

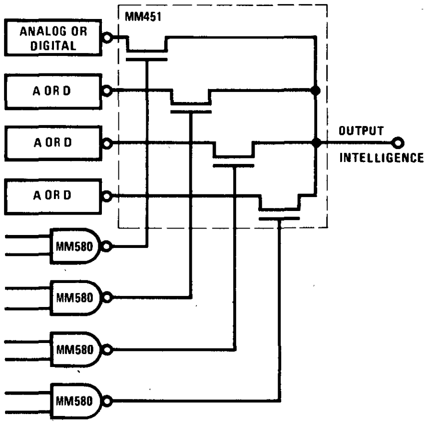


NOTE: Pin 5 connected to case and device bulk.
Drain and Source may be interchanged.
MM455, MM555

typical applications

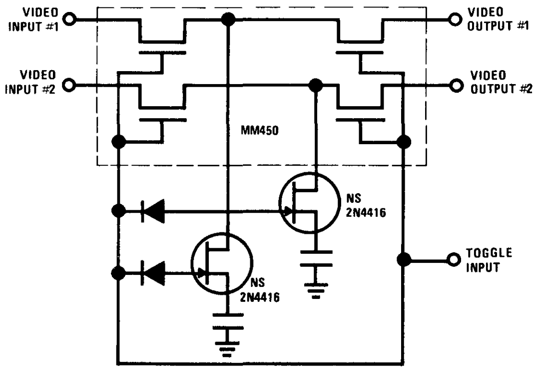


DPDT Analog Switch



4-Channel Multiplexer*

*Expansion in the number of data input lines is possible by using multiple level series switches allowing the same decode gates to be used for all lower rank decoding.



DPST High-Frequency Switch

absolute maximum ratings

	MM450, MM451, MM452, MM455	MM550, MM551, MM552, MM555
Gate Voltage (V_{GG})	+10V to -30V	+10V to -30V
Bulk Voltage (V_{BULK})	+10V	+10V
Analong Input (V_{IN})	+10V to -20V	+10V to -20V
Power Dissipation	200 mW	200 mW
Operating Temperature	-55°C to +125°C	-25°C to 70°C
Storage Temperature	-65°C to +150°C	-65°C to +150°C

electrical characteristics

STATIC CHARACTERISTICS (Note 1)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Analog Input Voltage				±10	V
Threshold Voltage ($V_{GS(T)}$)	V_{DG} = 0, I_D = 1 μA	1.0	2.2	3.0	V
ON Resistance	V_{IN} = -10V		150	600	Ω
ON Resistance	V_{IN} = V_{SS}		75	200	Ω
OFF Resistance			10^{10}		Ω
Gate Leakage Current (I_{GSB})	V_{GS} = -25V, V_{BS} = 0, T_A = 25°C		20		pA
Input (Drain) Leakage Current MM450, MM451, MM452, MM455	T_A = 25°C		.025	100	nA
	T_A = 85°C		.002	1.0	μA
	T_A = 125°C		.025	1.0	μA
Input (Drain) Leakage Current MM550, MM551, MM552, MM555	T_A = 25°C		0.1	100	nA
	T_A = 70°C		.030	1.0	μA
Output (Source) Leakage Current MM450, MM451, MM452, MM455	T_A = 25°C		.040	100	nA
Output (Source) Leakage Current					
MM450	T_A = 85°C			1.0	μA
MM451	T_A = 85°C			1.0	μA
MM452, MM455	T_A = 85°C			1.0	μA
MM450, MM451, MM452, MM455	T_A = 125°C			1.0	μA
Output (Source) Leakage Current					
MM550	T_A = 70°C			1.0	μA
MM551	T_A = 70°C			1.0	μA
MM552, MM555	T_A = 70°C			1.0	μA

DYNAMIC CHARACTERISTICS

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Large Signal Transconductance	V_{DS} = -10V, I_D = 10 mA f = 1 kHz		4000		μmhos

CAPACITANCE CHARACTERISTICS (Note 2)

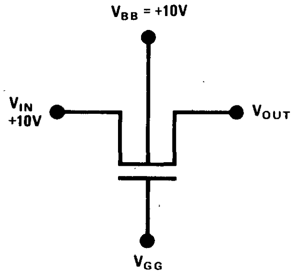
PARAMETER	DEVICE TYPE	MIN	TYP	MAX	UNITS
Analog Input (Drain) Capacitance (C_{DB})	ALL		8	10	pF
Output (Source) Capacitance (C_{SB})	MM450, MM550		11	14	pF
	MM451, MM551		20	24	pF
	MM452, MM552		7.5	11	pF
	MM455, MM555		7.5	11	pF
Gate Input Capacitance (C_{GB})	MM450, MM550		10	13	pF
	MM451, MM551		5.5	8	pF
	MM452, MM552		5.5	9	pF
	MM455, MM555		5.5	9	pF
Gate to Output Capacitance (C_{GS})	ALL		3.0	5	pF

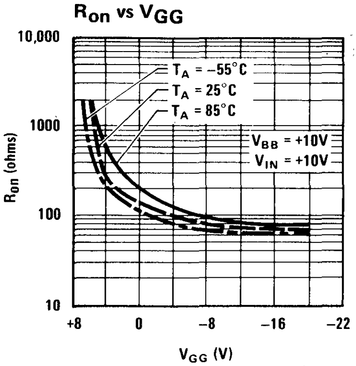
Note 1: The resistance specifications apply for $-55°C \leq T_A \leq +85°C$, V_{GG} = -20V, V_{BULK} = +10V, and a test current of 1 mA. Leakage current is measured with all pins held at ground except the pin being measured which is biased at -25V.

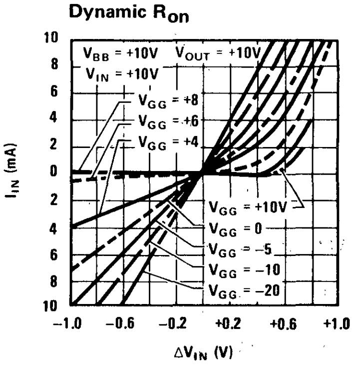
Note 2: All capacitance measurements are made at 0 volts bias at 1 MHz.

typical dynamic input characteristics (T_A = 25°C Unless Otherwise Noted)

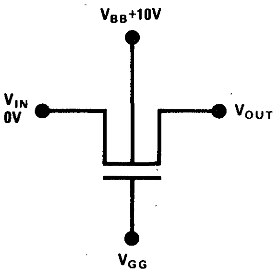
CONDITION 1:
ANALOG INPUT VOLTAGE
AT +10 VOLTS

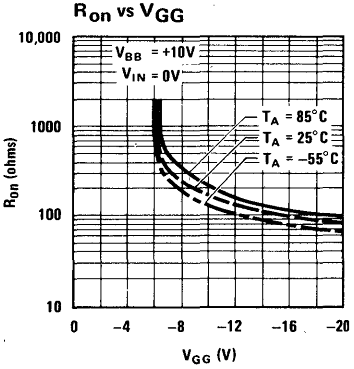


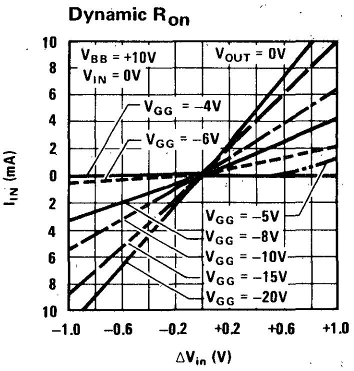

Ron vs VGG


Dynamic Ron

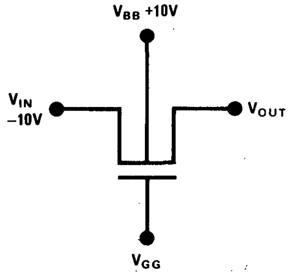
CONDITION 2:
ANALOG INPUT VOLTAGE
AT 0 VOLTS

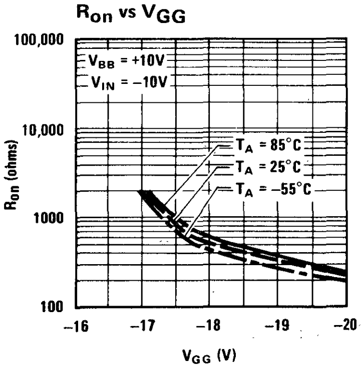


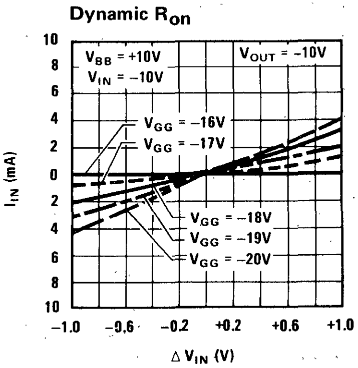

Ron vs VGG

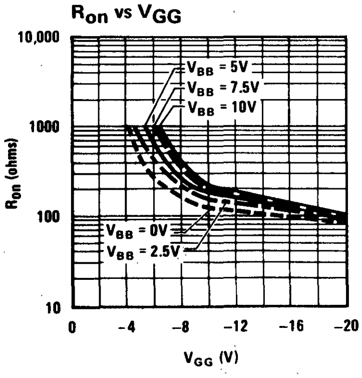

Dynamic Ron

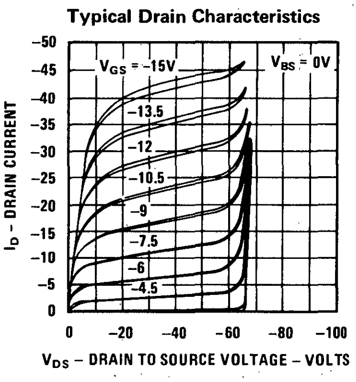
CONDITION 3:
ANALOG INPUT VOLTAGE
AT −10 VOLTS

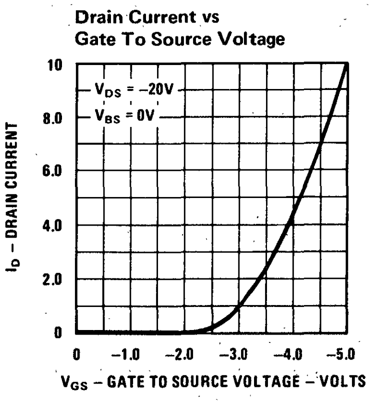



Ron vs VGG


Dynamic Ron

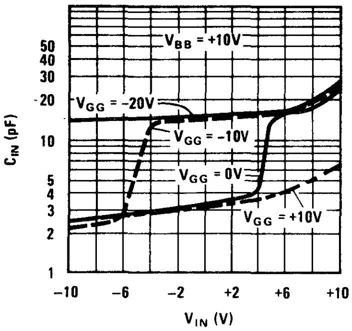

Ron vs VGG


Typical Drain Characteristics

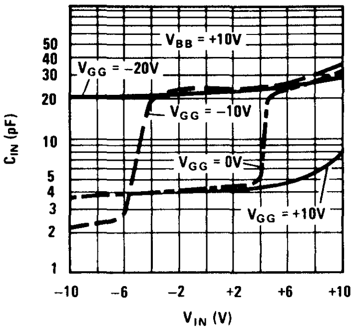

Drain Current vs
Gate To Source Voltage

typical input capacitances

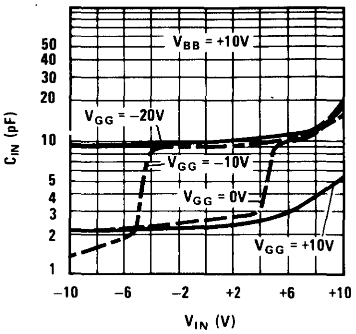
MM450, MM550
C_{IN} vs V_{IN}



MM451, MM551
C_{IN} vs V_{IN}



MM452, MM552 , MM455, MM555
C_{IN} vs V_{IN}



Analog Switches

MM454/MM554 four-channel commutator

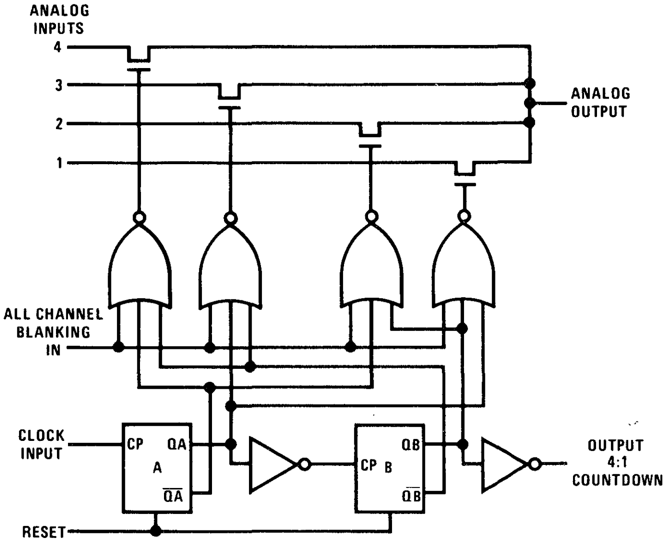
general description

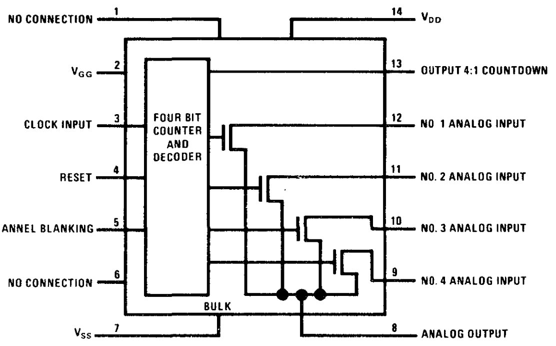
The MM454/MM554 is a four-channel analog commutator capable of switching four analog input channels sequentially onto an output line. The device is constructed on a single silicon chip using MOS P Channel enhancement transistors; it contains all the digital circuitry necessary to sequentially turn ON the four analog switch transistors permitting multiplexing of the analog input data. The device features:

■ High Analog Voltage Handling	±10V
■ High Commutating Rate	500 kHz
■ Low Leakage Current ($T_A = 25°C$)	200 pA
($T_A = 85°C$)	50 nA
■ All Channel Blanking input provided	
■ Reset capability provided	
■ Low ON Resistance	200Ω

In addition, the MM454/MM554 can easily be applied where submultiplexing is required since a 4:1 clock countdown signal is provided which can drive the clock input of subsequent MM454/MM554 units.

schematic and connection diagrams





NOTE: Pin 7 connected to case and to device bulk. Nominal Operating Voltages: $V_{GG} = -24V$; $V_{DD} = 0V$; $V_{SS} = +12V$, RESET BIAS = +12V (0V for RESET), ALL CHANNEL BLANKING BIAS = +12V (0V for BLANKING)

absolute maximum ratings (Note 1)

Gate Voltage (V_{GG})	+10V to −30V
Bulk Voltage (V_{SS})	+10V
Analog Input (V_{IN})	+10V to −20V
Power Dissipation	200 mW
Operating Temperature MM454	−55°C to +125°C
MM554	−25°C to +70°C
Storage Temperature	−65°C to +150°C

static characteristics (Note 2)

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
Analog Input Voltage					±10	V
ON Resistance		$V_{IN} = -10V$		170	600	Ω
ON Resistance		$V_{IN} = V_{SS}$		90	200	Ω
OFF Resistance				10^{10}		Ω
Analog Input Leakage Current	MM454	$T_A = 25°C$		.050	100	nA
	MM454	$T_A = 85°C$		.006	1.0	μA
	MM554	$T_A = 25°C$		.0001	100	nA
	MM554	$T_A = 70°C$		.030	1.0	μA
Analog Output Leakage Current	MM454	$T_A = 25°C$		0.100	100	nA
	MM454	$T_A = 85°C$		30	1.0	μA
	MM554	$T_A = 25°C$		.0001	100	nA
	MM554	$T_A = 70°C$		.030	1.0	μA
V_{SS} Supply Current Drain		$V_{SS} = +12V$		3.8	5.5	mA
V_{GG} Supply Current Drain		$V_{GG} = -24V$		2.4	3.5	mA

capacitance characteristics

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Analog Input Capacitance Channel OFF	$I_{IN} = 0$		4	6	pF
Analog Input Capacitance Channel ON	$I_{IN} = 0$		20	24	pF
Analog Output Capacitance	$I_{IN} = 0$		20	24	pF
Clock Input	$V_{CL} = +12V$		2.0		pF
Reset Input	$V_{RESET} = +12V$		2.0		pF
Blanking Input	$V_{BLANK} = +12V$		2.0		pF

clock characteristics (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Clock Input (HIGH)$^{(4)}$		$V_{SS} - 2$		V_{SS}	V
Clock Input (LOW)		−5	0	+5	V
Clock Input Rise Time (POS GOING)			No requirement		
Clock Input Fall Time (NEG GOING)				20	μsec
Countdown Output (POS) V_{OH}		$V_{SS} - 2$		V_{SS}	V
Countdown Output (NEG) V_{OL}			0		V
Maximum Commutation Rate		0.5	2.0		MHz
V_{SS}		+10.0	+12	+14	V

Note 1: Maximum ratings are limiting values above which the device may be damaged. All voltages referenced to $V_{DD} = 0$.

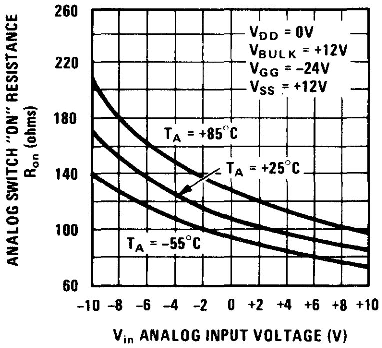
Note 2: These specifications apply over the indicated operating temperature range for $V_{GG} = -24V$, $V_{DD} = 0V$, $V_{SS} = +12V$, $V_{RESET} = +12V$, $V_{BLANK} = +12V$. ON resistance measured at 1 mA, OFF resistance and leakage measured with all analog inputs and output common. Capacitance measured at 1 MHz.

Note 3: Operating conditions in Note 2 apply. V_{SS} to V_{DD} (0V) voltage is applied to counting and gating circuits. V_{GG} is required only for analog switch biasing. All logic inputs are high resistance and are essentially capacitive.

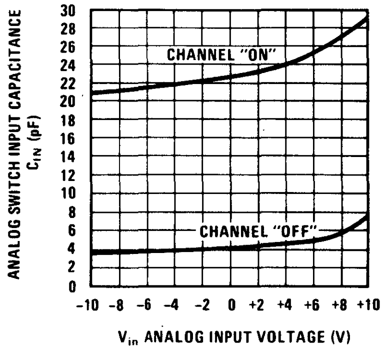
Note 4: Logic input voltage must not be more positive than V_{SS}.

typical performance characteristics

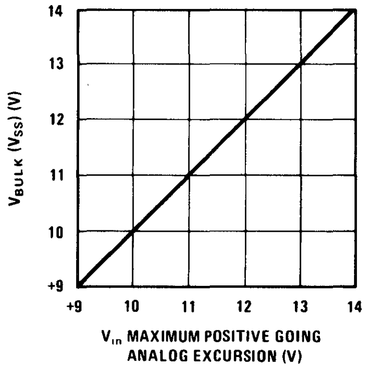
R_{ON} vs Analog Voltage



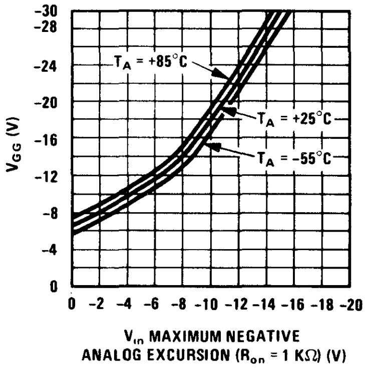
C_{IN} vs V_{IN}



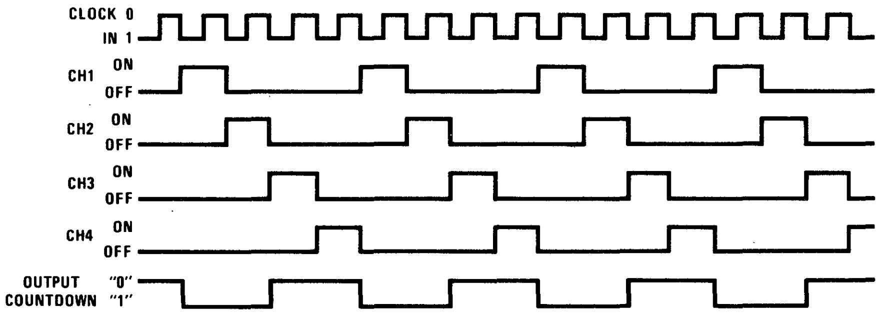
Plus V_{IN} (max) vs V_{BULK}



Minus V_{IN} (max) vs V_{GG}



timing diagram



NOTE: "0" LEVEL = +12V
"1" LEVEL = 0V (GND)

Analog Switches

AH0120/AH0130/AH0140/AH0150/AH0160 series analog switches

general description

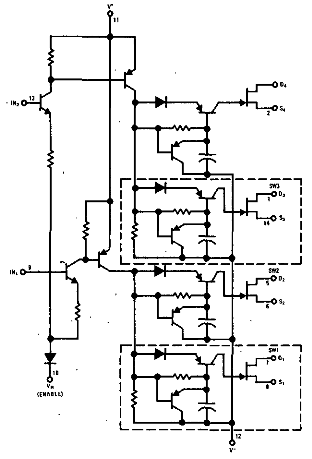
The AH0100 series represents a complete family of junction FET analog switches. The inherent flexibility of the family allows the designer to tailor the device selection to the particular application. Switch configurations available include dual DPST, dual SPST, DPDT, and SPDT. $r_{ds(ON)}$ ranges from 10 ohms through 100 ohms. The series is available in both 14 lead flat pack and 14 lead cavity DIP. Important design features include:

- TTL/DTL and RTL compatible logic inputs
- Up to 20V p-p analog input signal
- $r_{ds(ON)}$ less than 10Ω (AH0140, AH0141, AH0145, AH0146)
- Analog signals in excess of 1 MHz
- "OFF" power less than 1 mW
- Gate to drain bleed resistors eliminated
- Fast switching, t_{ON} is typically .4 μs, t_{OFF} is 1.0 μs
- Operation from standard op amp supply voltages, ±15V, available (AH0150/AH0160 series)
- Pin compatible with the popular DG 100 series.

The AH0100 series is designed to fulfill a wide variety of analog switching applications including commutators, multiplexers, D/A converters, sample and hold circuits, and modulators/demodulators. The AH0100 series is guaranteed over the temperature range −55°C to +125°C; whereas, the AH0100C series is guaranteed over the temperature range −25°C to +85°C.

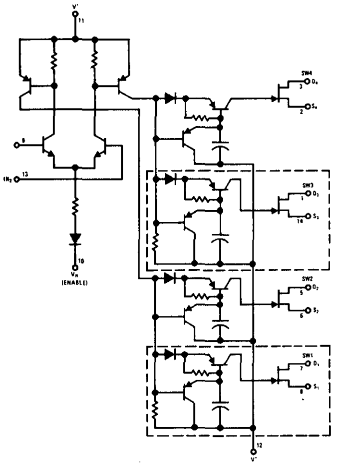
schematic diagrams

DUAL DPST and DUAL SPST



Note: Dotted line portions are not applicable to the dual SPST.

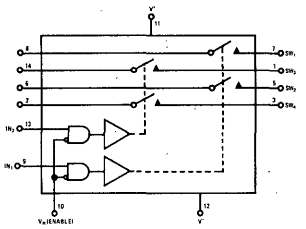
DPDT (diff.) and SPDT (diff.)



Note: Dotted line portions are not applicable to the SPDT (differential).

logic and connection diagrams

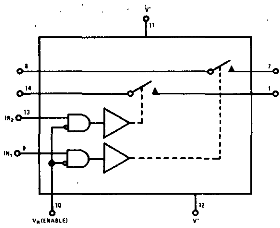
DUAL DPST



HIGH LEVEL (±10V)
AH0140 (10Ω)
AH0129 (30Ω)
AH0126 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0153 (15Ω)
AH0154 (50Ω)

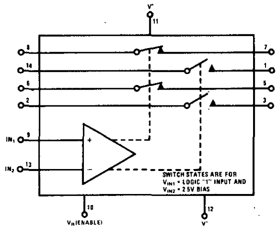
DUAL SPST



HIGH LEVEL (±10V)
AH0141 (10Ω)
AH0133 (30Ω)
AH0134 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0151 (15Ω)
AH0152 (50Ω)

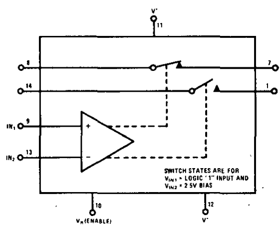
DPDT (Diff)



HIGH LEVEL (±10V)
AH0145 (10Ω)
AH0139 (30Ω)
AH0142 (80Ω)

MEDIUM LEVEL (±7.5)
AH0163 (15Ω)
AH0164 (50Ω)

SPDT (Diff)



HIGH LEVEL (±10V)
AH0146 (10Ω)
AH0144 (30Ω)
AH0143 (80Ω)

MEDIUM LEVEL (±7.5V)
AH0161 (15Ω)
AH0162 (50Ω)

absolute maximum ratings

		High Level	Medium Level
Total Supply Voltage ($V^+ - V^-$)		36V	34V
Analog Signal Voltage ($V^+ - V_A$ or $V_A - V^-$)		30V	25V
Positive Supply Voltage to Reference ($V^+ - V_R$)		25V	25V
Negative Supply Voltage to Reference ($V_R - V^-$)		22V	22V
Positive Supply Voltage to Input ($V^+ - V_{IN}$)		25V	25V
Input Voltage to Reference ($V_{IN} - V_R$)		±6V	±6V
Differential Input Voltage ($V_{IN} - V_{IN2}$)		±6V	±6V
Input Current, Any Terminal		30 mA	30 mA
Power Dissipation		See Curve	
Operating Temperature Range	AH0100 Series	-55°C to +125°C	
	AH0100C Series	-25°C to +85°C	
Storage Temperature Range		-65°C to +150°C	
Lead Temperature (Soldering, 10 sec)		300°C	

electrical characteristics for "HIGH LEVEL" Switches (Note 1)

PARAMETER	SYMBOL	DEVICE TYPE				CONDITIONS		LIMITS		UNITS
		DUAL DPST	DUAL SPST	DPDT (DIFF)	SPDT (DIFF)	$V^+ = 12.0V, V^- = -18.0V, V_R = 0.0V$		TYP	MAX	
Logic "1" Input Current	$I_{IN(ON)}$	All Circuits				Note 2	$T_A = 25°C$	2.0	60	µA
							Over Temp. Range		120	µA
Logic "0" Input Current	$I_{IN(OFF)}$	All Circuits				Note 2	$T_A = 25°C$	.01	.1	µA
							Over Temp. Range		2.0	µA
Positive Supply Current Switch ON	$I^+_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	2.2	3.0	mA
							Over Temp. Range		3.3	mA
Negative Supply Current Switch ON	$I^-_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	-1.0	-1.8	mA
							Over Temp. Range		-2.0	mA
Reference Input (Enable) ON Current	$I_{R(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	-1.0	-1.4	mA
							Over Temp. Range		-1.6	mA
Positive Supply Current Switch OFF	$I^+_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	1.0	10	µA
							Over Temp. Range		25	µA
Negative Supply Current Switch OFF	$I^-_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	-1.0	-10	µA
							Over Temp. Range		-25	µA
Reference Input (Enable) OFF Current	$I_{R(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	-1.0	-10	µA
							Over Temp. Range		-25	µA
Switch ON Resistance	$r_{ds(ON)}$	AH0126	AH0134	AH0142	AH0143	$V_D = 10V$	$T_A = 25°C$	45	80	Ω
						$I_D = 1\ mA$	Over Temp. Range		150	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0129	AH0133	AH0139	AH0144	$V_D = 10V$	$T_A = 25°C$	25	30	Ω
						$I_D = 1\ mA$	Over Temp. Range		60	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0140	AH0141	AH0145	AH0146	$V_D = 10V$	$T_A = 25°C$	8	10	Ω
						$I_F = 1\ mA$	Over Temp. Range		20	Ω
Driver Leakage Current	$(I_D + I_S)_{ON}$	All Circuits				$V_D = V_S = -10V$	$T_A = 25°C$	.01	1	nA
							Over Temp. Range		100	nA
Switch Leakage Current	$I_{S(OFF)}$ OR $I_{D(OFF)}$	AH0126 AH0129	AH0134 AH0133	AH0142 AH0139	AH0143 AH0144	$V_{DS} = ±20V$	$T_A = 25°C$	0.8	1	nA
							Over Temp. Range		100	nA
Switch Leakage Current	$I_{S(OFF)}$ OR $I_{D(OFF)}$	AH0140	AH0141	AH0145	AH0146	$V_{DS} = ±20V$	$T_A = 25°C$	4	10	nA
							Over Temp. Range		1.0	µA
Switch Turn-ON Time	t_{ON}	AH0126 AH0129	AH0134 AH0133	AH0142 AH0139	AH0143 AH0144	See Test Circuit $V_A = ±10V$	$T_A = 25°C$	0.5	0.8	µs
Switch Turn-ON Time	t_{ON}	AH0140	AH0141	AH0145	AH0146	See Test Circuit $V_A = ±10V$	$T_A = 25°C$	0.8	1.0	µs
Switch Turn-OFF Time	t_{OFF}	AH0126 AH0129	AH0134 AH0133	AH0142 AH0139	AH0143 AH0144	See Test Circuit $V_A = ±10V$	$T_A = 25°C$	0.9	1.6	µs
Switch Turn-OFF Time	t_{OFF}	AH0140	AH0141	AH0145	AH0146	See Test Circuit $V_A = ±10V$	$T_A = 25°C$	1.1	2.5	µs

Note 1: Unless otherwise specified these limits apply for -55°C to +125°C for the AH0100 series and -25°C to +85°C for the AH0100C series. All typical values are for $T_A = 25°C$.

Note 2: For the DPST and Dual DPST, the ON condition is for $V_{IN} = 2.5V$; the OFF condition is for $V_{IN} = 0.8V$. For the differential switches and SW1 and 2 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 3.0V$. For SW3 and 4 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 2.0V$.

electrical characteristics for "MEDIUM LEVEL" Switches (Note 1)

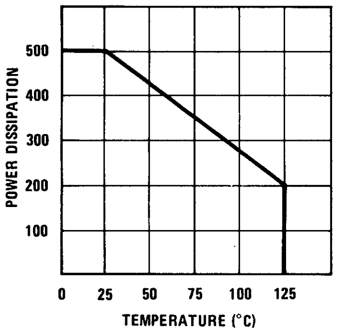
PARAMETER	SYMBOL	DEVICE TYPE				CONDITIONS		LIMITS		UNITS
		DUAL DPST	DUAL SPST	DUAL DPDT	SPDT (DIFF)	$V^+ = +15.0V$, $V^- = -15V$, $V_R = 0V$		TYP	MAX	
Logic "1" Input Current	$I_{IN(ON)}$	All Circuits				Note 2	$T_A = 25°C$	20	60	μA
							Over Temp. Range		120	μA
Logic "0" Input Current	$I_{IN(OFF)}$	All Circuits				Note 2	$T_A = 25°C$	.01	0.1	μA
							Over Temp. Range		2	μA
Positive Supply Current Switch ON	$I^+_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	2.2	3.0	mA
							Over Temp. Range		3.3	mA
Negative Supply Current Switch ON	$I^-_{(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	−1.0	−1.8	mA
							Over Temp. Range		−2.0	mA
Reference Input (Enable) ON Current	$I_{R(ON)}$	All Circuits				One Driver ON Note 2	$T_A = 25°C$	−1.0	−1.4	mA
							Over Temp. Range		−1.6	mA
Positive Supply Current Switch OFF	$I^+_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	1.0	10	μA
							Over Temp. Range		25	μA
Negative Supply Current Switch OFF	$I^-_{(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	−1.0	−10	μA
							Over Temp. Range		−25	μA
Reference Input (Enable) OFF Current	$I_{R(OFF)}$	All Circuits				$V_{IN1} = V_{IN2} = 0.8V$	$T_A = 25°C$	−1.0	−10	μA
							Over Temp. Range		−25	μA
Switch ON Resistance	$r_{ds(ON)}$	AH0153	AH0151	AH0163	AH0161	$V_D = 7.5V$ $I_D = 1\ mA$	$T_A = 25°C$	10	15	Ω
							Over Temp. Range		30	Ω
Switch ON Resistance	$r_{ds(ON)}$	AH0154	AH0152	AH0164	AH0162	$V_D = 7.5V$ $I_D = 1\ mA$	$T_A = 25°C$	45	50	Ω
							Over Temp. Range		100	Ω
Driver Leakage Current	$(I_D + I_S)_{ON}$	All Circuits				$V_D = V_S = -7.5V$	$T_A = 25°C$	.01	2	nA
							Over Temp. Range		500	nA
Switch Leakage Current	$I_{D(OFF)}$ OR $I_{S(OFF)}$	AH0153	AH0151	AH0163	AH0161	$V_{DS} = \pm 15V$	$T_A = 25°C$	5	10	nA
							Over Temp. Range		1.0	μA
Switch Leakage Current	$I_{D(OFF)}$ OR $I_{S(OFF)}$	AH0154	AH0152	AH0164	AH0162	$V_{DS} = \pm 15.0V$	$T_A = 25°C$	1.0	2.0	nA
							Over Temp. Range		200	nA
Switch Turn-ON Time	t_{ON}	AH0153	AH0151	AH0163	AH0161	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		0.8	1.0	μs
Switch Turn-ON Time	t_{ON}	AH0154	AH0152	AH0164	AH0162	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		0.5	0.8	μs
Switch Turn-OFF Time	t_{OFF}	AH0153	AH0151	AH0163	AH0161	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		1.1	2.5	μs
Switch Turn-OFF Time	t_{OFF}	AH0154	AH0152	AH0164	AH0162	See Test Circuit $V_A = \pm 7.5V$ $T_A = 25°C$		0.9	1.5	μs

Note 1: Unless otherwise specified, these limits apply for −55°C to +125°C for the AH0100 series and −25°C to +85°C for the AH0100C series. All typical values are for $T_A = 25°C$.

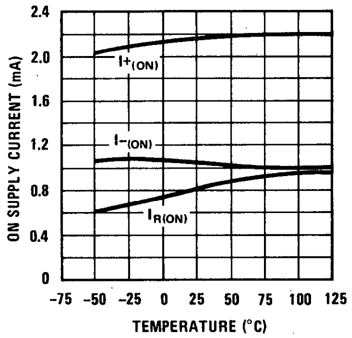
Note 2: For the DPST and Dual DPST, the ON condition is for $V_{IN} = 2.5V$; the OFF condition is for $V_{IN} = 0.8V$. For the differential switches and SW1 and 2 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 3.0V$. For SW3 and 4 ON, $V_{IN2} = 2.5V$, $V_{IN1} = 2.0V$.

typical performance characteristics

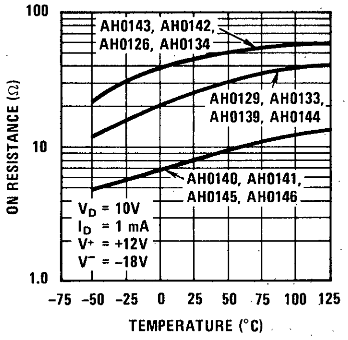
Power Dissipation vs Temperature



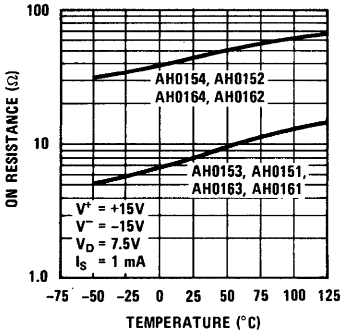
ON Supply Current vs Temperature



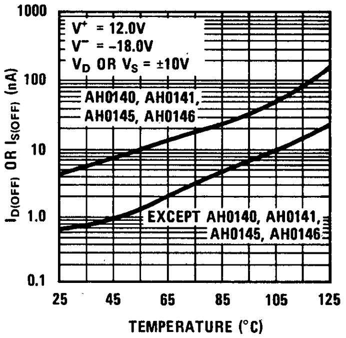
$r_{ds(ON)}$ vs Temperature AH0120 thru AH0140 Series



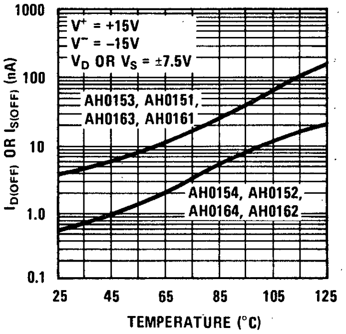
$r_{ds(ON)}$ vs Temperature AH0150/AH0160 Series



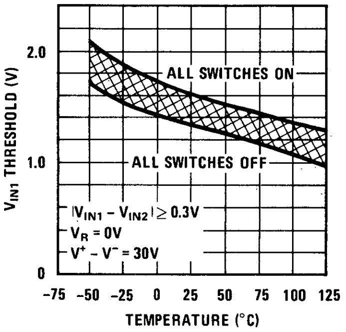
Leakage Current vs Temperature AH0120, AH0130, & AH0140



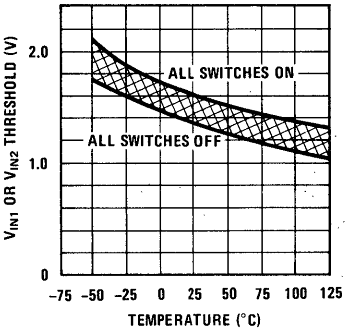
Leakage Current vs Temperature AH0150 & AH0160



Single Ended Switch Input Threshold vs Temperature

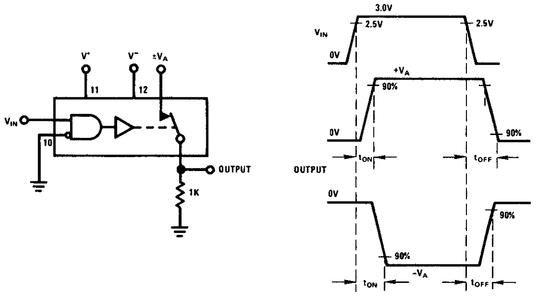


Differential Switch Input Threshold vs Temperature

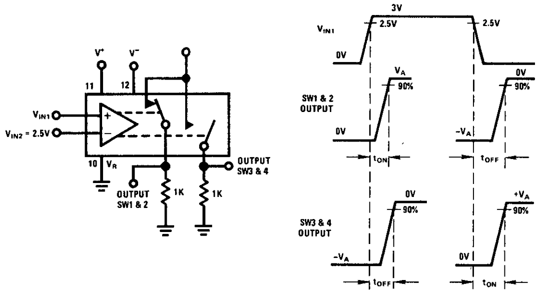


switching time test circuits

Single Ended Input



Differential Input



applications information

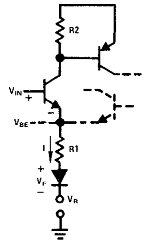
1. INPUT LOGIC COMPATIBILITY

A. Voltage Considerations

In general, the AH0100 series is compatible with most DTL, TTL, and RTL logic families. The ON-input threshold is determined by the V_{BE} of the input transistor plus the V_f of the diode in the emitter leg, plus I x R_1, plus V_R. At room temperature and $V_R = 0V$, the nominal ON threshold is: 0.7V+0.7V+0.2V,=1.6V.Over temperature and manufacturing tolerances, the threshold may be as high as 2.5V and as low as 0.8V. The rules for proper operation are:

$V_{IN} - V_R \geq 2.5V$ All switches ON

$V_{IN} - V_R \leq 0.8V$ All switches OFF



B. Input Current Considerations

$I_{IN(ON)}$, the current drawn by the driver with $V_{IN} = 2.5V$ is typically 20 μA at 25°C and is guaranteed less than 120 μA over temperature. DTL, such as the DM930 series can supply 180 μA at logic "1" voltages in excess of 2.5V. TTL output levels are comparable at 400 μA. The DTL and TTL can drive the AH0100 series directly. However, at low temperature, DC noise margin in the logic "1" state is eroded with DTL. A pull-up resistor of 10 kΩ is recommended when using DTL over military temperature range.

If more than one driver is to be driven by a DM930 series (6K) gate, an external pull-up resistor should be added. The value is given by:

$$R_P = \frac{11}{N-1} \text{ for } N > 2$$

where:

R_P = value of the pull-up resistor in kΩ

N = number of drivers.

C. Input Slew Rate

The slew rate of the logic input must be in excess of 0.3V/μs in order to assure proper operation of the analog switch. DTL, TTL, and RTL output rise times are far in excess of the minimum slew rate requirements. Discrete logic designs, however, should include consideration of input rise time.

2. ENABLE CONTROL

The application of a positive signal at the V_R terminal will open all switches. The V_R (ENABLE) signal must be capable of rising to within 0.8V of $V_{IN(ON)}$ in the OFF state and of sinking $I_{R(ON)}$ milliamps in the ON state (at $V_{IN(ON)} - V_R > 2.5V$). The V_R terminal can be driven from most TTL and DTL gates.

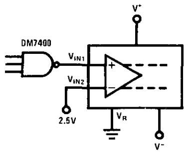
3. DIFFERENTIAL INPUT CONSIDERATIONS

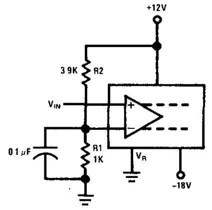
The differential switch driver is essentially a differential amplifier. The input requirements for proper operation are:

$|V_{IN1} - V_{IN2}| \geq 0.3V$

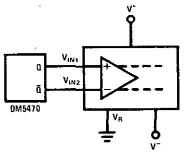
$2.5 \leq (V_{IN1} \text{ or } V_{IN2}) - V_R \leq 5V$

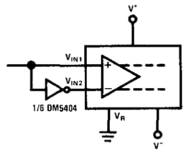
The differential driver may be furnished by a DC level as shown below. The level may be derived from a voltage divider to V^+ or the 5V V_{CC} of the DTL logic. In order to assure proper operation, the divider should be "stiff" with respect to I_{IN2}. Bypassing R1 with a 0.1 μF disc capacitor will prevent degradation of t_{ON} and t_{OFF}.



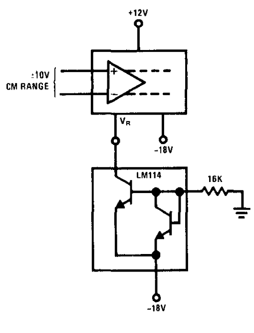


Alternatively, the differential driver may be driven from a TTL flip-flop or inverter.





Connection of a 1 mA current source between V_R and V^- will allow operation over a ±10V common mode range. Differential input voltage must be less than the 6V breakdown, and input threshold of 2.5V and 300mV differential overdrive still prevail.



4. ANALOG VOLTAGE CONSIDERATIONS

The rules for operating the AH0100 series at supply voltages other than those specified essentially breakdown into OFF and ON considerations. The OFF considerations are dictated by the maximum negative swing of the analog signal and the pinch off of the JFET switch. In the OFF state, the gate of the FET is at $V^- + V_{BE} + V_{SAT}$ or about 1.0V above the V^- potential. The maximum V_P of the FET switches is 7V. The most negative analog voltage, V_A, swing which can be accomodated for any given supply voltage is:

$$|V_A| \leq |V^-| - V_P - V_{BE} - V_{SAT} \text{ or}$$

$$|V_A| \leq |V^-| - 8.0 \text{ or } |V^-| \geq |V_A| + 8.0V$$

For the standard high level switches, $V_A \leq |-18| + 8 = -10V$. The value for V^+ is dictated by the maximum positive swing of the analog input voltage. Essentially the collector to base junction of the turn-on PNP must remain reversed biased for all positive value of analog input voltage. The base of the PNP is at $V^+ - V_{SAT} - V_{BE}$ or $V^+ - 1.0V$. The PNP's collector base junction should have at least 1.0V reverse bias. Hence, the most positive analog voltage swing which may be accommodated for a given value of V^+ is:

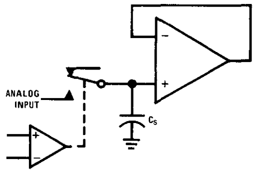
$$V_A \leq V^+ - V_{SAT} - V_{BE} - 1.0V \text{ or}$$

$$V_A \leq V^+ - 2.0V \text{ or } V^+ \geq V_A + 2.0V$$

For the standard high level switches, $V_A = 12 - 2.0V = +10V$.

5. SWITCHING TRANSIENTS

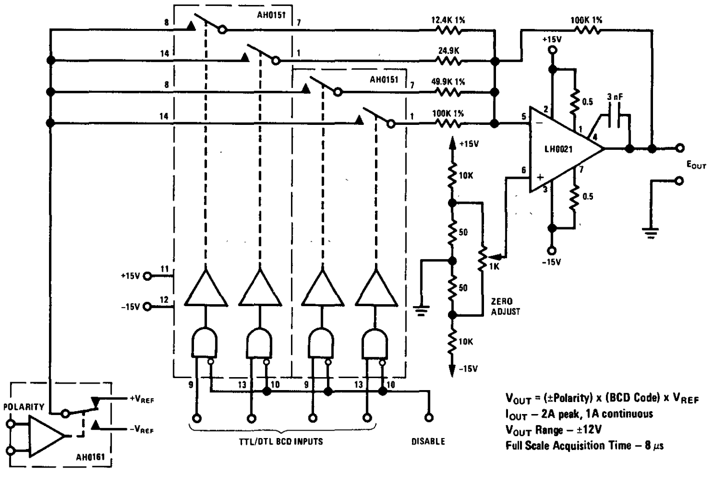
Due to charge stored in the gate-to-source and gate-to-drain capacitances of the FET switch, transients may appear in the output during switching. This is particularly true during the OFF to ON transition. The magnitude and duration of the transient may be minimized by making source and load impedance levels as small as practical.



Furthermore, transients may be minimized by operating the switches in the differential mode; i.e., the charge delivered to the load during the ON to OFF transition is, to a large extent, cancelled by the OFF to ON transition.

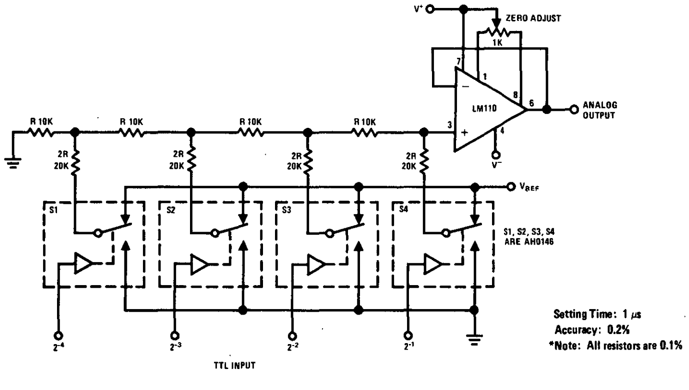
typical applications

Programmable One Amp Power Supply



V_{OUT} = (±Polarity) x (BCD Code) x V_{REF}
I_{OUT} – 2A peak, 1A continuous
V_{OUT} Range – ±12V
Full Scale Acquisition Time – 8 μs

Four to Ten Bit D to A Converter (4 Bits Shown)

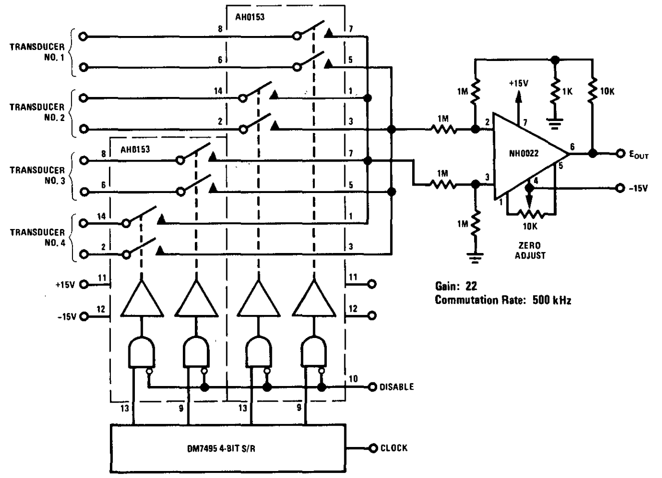


S1, S2, S3, S4 ARE AH0146

Setting Time: 1 μs
Accuracy: 0.2%
*Note: All resistors are 0.1%

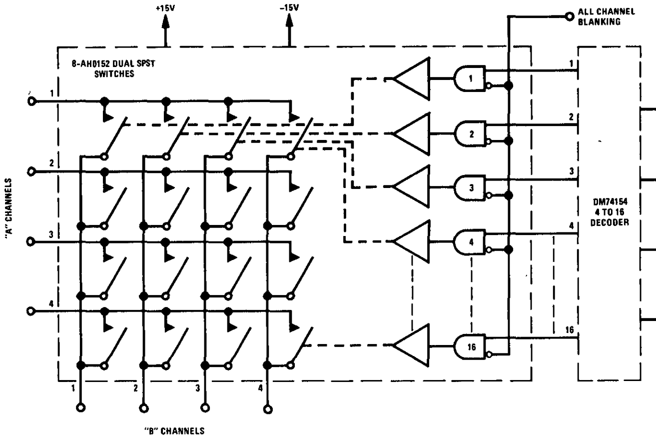
typical applications (con't)

Four Channel Differential Transducer Commutator



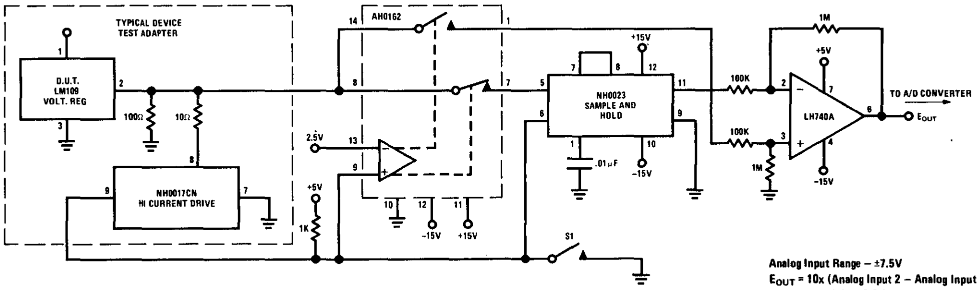
Gain: 22
Commutation Rate: 500 kHz

4 x 4 Cross Point Analog Switch



Switching Time – 800 ns
"ON" Resistance – 45Ω
"OFF" Resistance – 10^{10}Ω

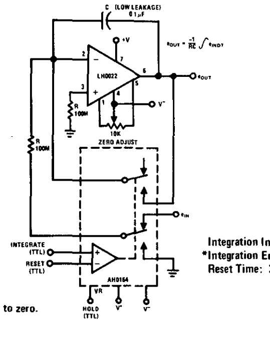
Delta Measurement System for Automatic Linear Circuit Tester



Analog Input Range – ±7.5V
E_{OUT} = 10x (Analog Input 2 – Analog Input 1)
Error Rate – 0.01% F.S./sec

Note: S1 must be open for 50 μs min to take frist reading with I_L = 50 mA. Second reading is taken with S2 closed. With S1 and other set-up forcing functions under computer control, system will measure line and load regulation on voltage regulators, voltage gain, offset current, CMRR and PSRR on op amps as well as other circuits requiring measurement of the change of a parameter with the change of a forcing function.

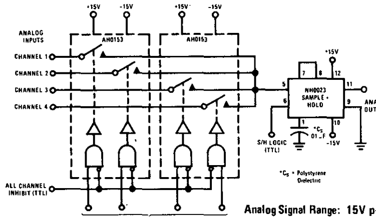
Precision Long Time Constant Integrator with Reset



Integration Internal = 10 sec
*Integration Error = 100 μV
Reset Time: 30 μs

*Note: V_{OS} adjusted to zero.

Four Channel Commutator



Analog Signal Range: 15V p-p
Sample Rate: 1 MHz
Acquisition Time: 25 μs
Drift Rate: 0.5 mV/sec

Analog Switches

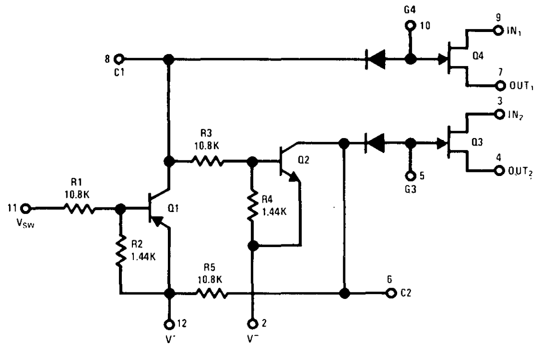
AH2114/AH2114C DPST analog switch general description

The AH2114 is a DPST analog switch circuit comprised of two junction FET switches and their associated driver. The AH2114 is designed to fulfill a wide variety of high level analog switching applications including multiplexers, A to D Converters, integrators, and choppers. Design features include:

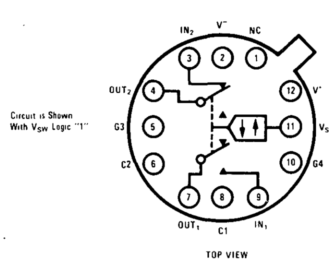
- Low ON resistance, typically 75Ω
- High OFF resistance, typically $10^{11}\Omega$
- Large output voltage swing, typically ±10V
- Powered from standard op-amp supply voltages of ±15V
- Input signals in excess of 1 MHz
- Turn-ON and turn-OFF times typically 1 µs

The AH2114 is guaranteed over the temperature range −55°C to +125°C whereas the AH2114C is guaranteed over the temperature range 0°C to +85°C.

schematic and connection diagrams



Metal Can Package



ac test circuit and waveforms

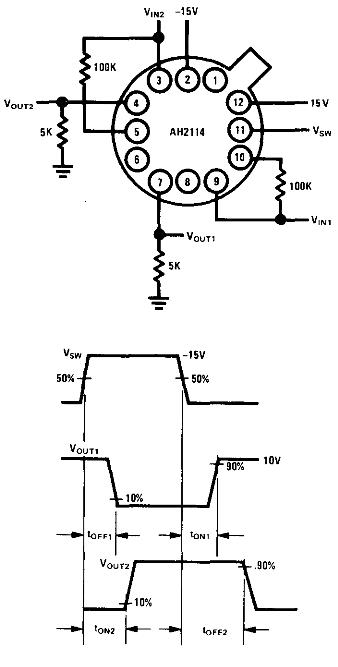


FIGURE 1.

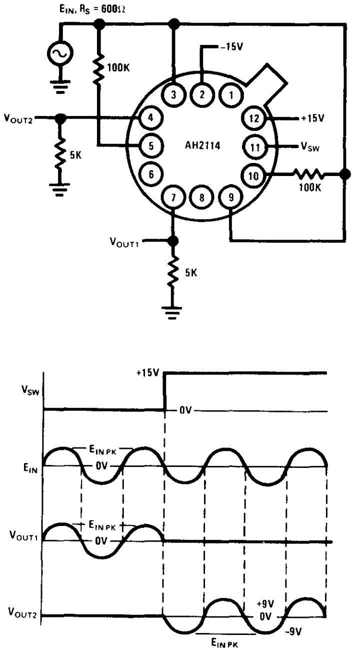


FIGURE 2.

absolute maximum ratings

Vplus Supply Voltage	+25V
Vminus Supply Voltage	-25V
Vplus—Vminus Differential Voltage	40V
Logic Input Voltage	25V
Power Dissipation (Note 3)	1.36W
Operating Temperature Range	
AH2114	-55°C to +125°C
AH2114C	0°C to +85°C
Storage Temperature Range	-65°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Notes 1 and 2)

PARAMETER	CONDITIONS	AH2114			AH2114C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Static Drain-Source "On" Resistance	$I_D = 1.0$ mA, $V_{GS} = 0V$, $T_A = 25°C$		75	100		75	125	Ω
	$I_D = 1.0$ mA, $V_{GS} = 0V$			150			160	Ω
Drain-Gate Leakage Current	$V_{DS} = 20V$, $V_{GS} = -7V$, $T_A = 25°C$		0.2	1.0		0.2	5.0	nA
				60			60	nA
FET Gate-Source Breakdown Voltage	$I_G = 1.0\,\mu A$ $V_{DS} = 0V$	35			35			V
Drain-Gate Capacitance	$V_{DG} = 20V$, $I_S = 0$ f = 1.0 MHz, $T_A = 25°C$		4.0	5.0		4.0	5.0	pF
Source-Gate Capacitance	$V_{DG} = 20V$, $I_D = 0$ f = 1.0 MHz, $T_A = 25°C$		4.0	5.0		4.0	5.0	pF
Input 1 Turn-ON Time	$V_{IN1} = 10V$, $T_A = 25°C$ (See Figure 1)		35	60		35	60	ns
Input 2 Turn-ON Time	$V_{IN2} = 10V$, $T_A = 25°C$ (See Figure 1)		1.2	1.5		1.2	1.2	μs
Input 1 Turn-OFF Time	$V_{IN1} = 10V$, $T_A = 25°C$ (See Figure 1)		0.6	0.75		0.6	0.75	μs
Input 2 Turn-OFF Time	$V_{IN2} = 10V$, $T_A = 25°C$ (See Figure 1)		50	80		50	80	ns
DC Voltage Range	$T_A = 25°C$ (See Figure 2)	±9.0	±10.0		±9.0	±10.0		V
AC Voltage Range	$T_A = 25°C$ (See Figure 2)	±9.0	±10.0		±9.0	±10.0		V

Note 1: Unless otherwise specified these specifications apply for pin 12 connected to +15V, pin 2 connected to −15V, −55°C to 125°C for the AH2114, and 0°C to 85°C for the AH2114C.

Note 2: All typical values are for $T_A = 25°C$.

Note 3: Derate linearly at 100°C/W above 25°C.

Analog Switches

AM1000,AM1001,AM1002 silicon N-channel high speed analog switch

general description

The AM1000 series are junction FET integrated circuit analog switches. These devices commutate faster and with less voltage spiking than any other analog switch presently available. By comparison, discrete JFET switches require elaborate drive circuits to obtain reasonable performance for high toggle rates. Encapsulated in a four pin TO-72 package, these units require a minimum of circuit board area. Switching transients are greatly reduced by a monolithic integrated circuit process. The resulting analog switch device provides the following features:

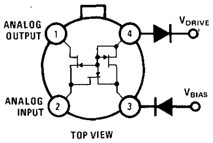
■ Low ON Resistance	30Ω
■ High Analog Signal Frequency	100 MHz
■ High Toggle Rate	4 MHz
■ Low Leakage Current	250 pA
■ Large Analog Signal Swing	±15V
■ Break Before Make Action	

The AM1000 series of analog switches are particularly suitable for the following applications:

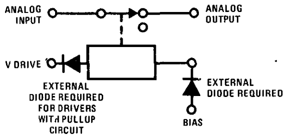
- High Speed Commutators
- Multiplexers
- Sample and Hold Circuits
- Reset Switching
- Video Switching

schematic diagram

TO-72 Package

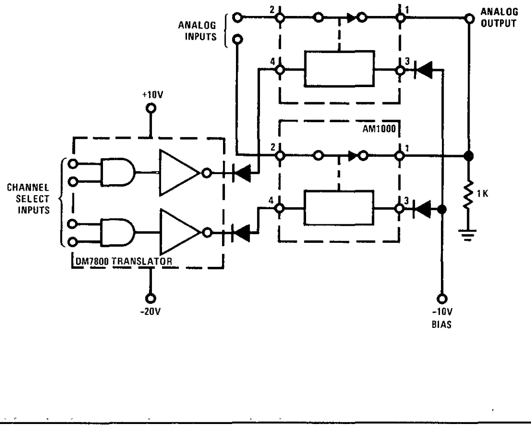


equivalent circuit

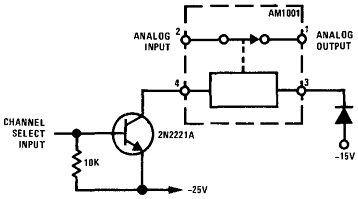


typical applications

±10 Volt Swing Analog Switch 0.5% Accuracy



±15 Volt Swing Analog Switch



absolute maximum ratings

	AM1001	AM1000 AM1002
V_{IN} (Note 1)	+50V	+40V
V_{OUT} (Note 1)	+50V	+40V
V_{DRIVE} (Note 1)	−50V	−40V
V_{BIAS} (Note 1)	+50V	+40V

Power Dissipation @ $T_A = 25°C$	300 mW
Linear Derating Factor	1.7 mW/°C
Power Dissipation @ $T_C = 125°C$	150 mW
Linear Derating Factor	6 mW/°C
Maximum Junction Operating Temperature	−55°C to +150°C
Storage Temperature	+200°C
Lead Temperature (Solding, 10 sec)	+300°C

electrical characteristics

ON CHARACTERISTICS (Note 2)

PARAMETER	CONDITION		MIN	TYP	MAX	UNITS
R_{ON}	$V_{DRIVE} = +15V$, $V_{BIAS} = -15V$ $I_{IN} = 1$ mA, $V_{OUT} = 0V$	AM1001	20	40	50	Ω
R_{ON}	$V_{DRIVE} = +10V$, $V_{BIAS} = -10V$ $I_{IN} = 1$ mA, $V_{OUT} = 0V$	AM1000	20	25	30	Ω
		AM1002	20	50	100	Ω

OFF CHARACTERISTICS

PARAMETER	CONDITION	AM1000 AM1001			AM1002			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
$I_{OUT(OFF)}$	$V_{DRIVE} = -20V$, $V_{BIAS} = -10V$ $V_{IN} = -10V$, $V_{OUT} = +10V$							
	$T_A = +25°C$		.05	.25		0.5	1	nA
	$T_A = +125°C$		.025	.25		0.2	1	μA
$I_{OUT(OFF)}$	$V_{DRIVE} = -20V$, $V_{BIAS} = -10V$ $V_{IN} = +10V$, $V_{OUT} = -10V$							
	$T_A = +25°C$		.05	.25		0.5	1	nA
	$T_A = +125°C$		.05	.25		0.2	1	μA

DRIVE CHARACTERISTICS (Note 3)

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
I_{DRIVE} (Switch OFF)	$V_{DRIVE} = -20V$, $V_{BIAS} = -10V$ AM1000, 1001, 1002 $V_{IN} = \pm10V$, $V_{OUT} = \pm10V$		5	10	mA

SWITCHING CHARACTERISTICS

PARAMETER	CONDITION	AM1000 MAX	AM1001 MAX	AM1002 MAX	UNITS
t_{ON}	See Switching Time Test Circuit	100	150	200	ns
t_{OFF}		100	100	100	ns

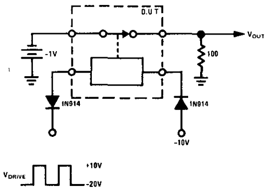
Note 1: The maximum voltage ratings may be applied between any pin or pins simultaneously. Power dissipation may be exceeded in some modes if the voltage pulse exceeds 10 ms. Normal operation will not cause excessive power dissipation even in a "D.C." switching application.

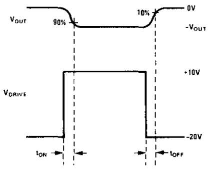
Note 2: All parameters are measured with external silicon diodes. See electrical connection diagram for proper diode placement.

Note 3: I_{BIAS} (Switch OFF) is equal to I_{DRIVE} (Switch OFF). $I_{(BIAS)}$ (Switch ON), is equal to external diode leakage.

Note 4: Rise and fall times of V_{DRIVE} shall be 15 ns maximum for switching time testing.

switching time test circuit and waveforms





Analog Switches

AM3705/AM3705C 8-channel MOS analog multiplexer

general description

The AM3705/AM3705C is an eight-channel MOS analog multiplex switch. TTL compatible logic inputs that require no level shifting or input pull-up resistors and operation over a wide range of supply voltages is obtained by constructing the device with low threshold P-channel enhancement MOS technology. To simplify external logic requirements, a one-of-eight decoder and an output enable are included in the device.

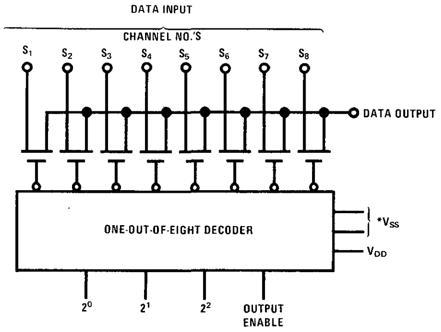
Important design features include:

- TTL/DTL compatible input logic levels
- Operation from standard +5V and −15V supplies
- Wide analog voltage range — ±5V
- One-of-eight decoder on chip
- Output enable control
- Low ON resistance — 150Ω
- Input gate protection
- Low leakage currents — 0.5 nA

The AM3705/AM3705C is designed as a low cost analog multiplex switch to fulfill a wide variety of data acquisition and data distribution applications including cross-point switching, MUX front ends for A/D converters, process controllers, automatic test gear, programmable power supplies and other military or industrial instrumentation applications.

For information on other National analog switches, see listing on page 162.

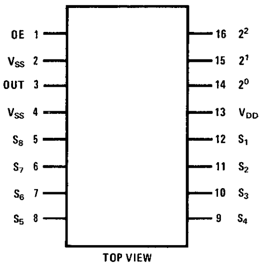
block diagram (MIL-STD-806B)



*Both V_{SS} lines are internally connected; either one or both may be used.

connection diagram

Dual-In-Line Package

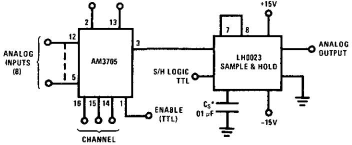


truth table

LOGIC INPUTS				CHANNEL
2^0	2^1	2^2	OE	ON
L	L	L	H	S_1
H	L	L	H	S_2
L	H	L	H	S_3
H	H	L	H	S_4
L	L	H	H	S_5
H	L	H	H	S_6
L	H	H	H	S_7
H	H	H	H	S_8
X	X	X	L	OFF

typical applications

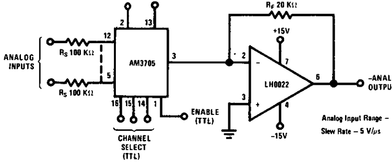
Buffered 8-Channel Multiplex, Sample and Hold



*Polystyrene Dielectric

Analog Signal Range – ±5V
Acquisition Time – 25 ns
Drift Rate – 0 5 mV/sec
Aperature Time – 250 ns

Wide Input Range Analog Switch



Analog Input Range – ±25V
Slew Rate – 5 V/μs

absolute maximum ratings

Positive Voltage on Any Pin (Note 1)	+0.3V
Negative Voltage on Any Pin (Note 1)	−35V
Source to Drain Current	±30 mA
Logic Input Current	±0.1 mA
Power Dissipation (Note 2)	500 mW
Operating Temperature Range AM3705	−55°C to +125°C
AM3705C	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 3)

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
ON Resistance	R_{ON}	$V_{IN} = V_{SS}$; $I_{OUT} = 100\,\mu A$		80	250	Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$; $I_{OUT} = -100\,\mu A$		160	400	Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$; $I_{OUT} = -100\,\mu A$				
AM3705		$T_A = +125°C$			400	Ω
AM3705C		$T_A = +70°C$			400	Ω
ON Resistance	R_{ON}	$V_{IN} = +5V$; $V_{DD} = -15V$; $I_{OUT} = 100\,\mu A$		100		Ω
ON Resistance	R_{ON}	$V_{IN} = 0V$, $V_{DD} = -15V$, $I_{OUT} = -100\,\mu A$		150		Ω
ON Resistance	R_{ON}	$V_{IN} = -5V$; $V_{DD} = -15V$; $I_{OUT} = -100\,\mu A$		250		Ω
OFF Resistance	R_{OFF}			10^{10}		Ω
Output Leakage Current	I_{LO}	$V_{SS} - V_{OUT} = 15V$		0.5	10	nA
AM3705	I_{LO}	$V_{SS} - V_{OUT} = 15V$; $T_A = 125°C$		150	500	nA
AM3705C	I_{LO}	$V_{SS} - V_{OUT} = 15V$; $T_A = 70°C$		35	500	nA
Data Input Leakage Current	I_{LDI}	$V_{SS} - V_{IN} = 15V$		0.1	3.0	nA
AM3705	I_{LDI}	$V_{SS} - V_{IN} = 15V$; $T_A = 125°C$		25	500	nA
AM3705C	I_{LDI}	$V_{SS} - V_{IN} = 15V$; $T_A = 70°C$		0.5	500	nA
Logic Input Leakage Current	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$		.001	1	μA
AM3705	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$; $T_A = 125°C$		.05	10	μA
AM3705C	I_{LI}	$V_{SS} - V_{Logic\ In} = 15V$; $T_A = 70°C$		.05	10	μA
Logic Input LOW Level	V_{IL}	$V_{SS} = +5.0V$		0.5	1.0	V
Logic Input LOW Level	V_{IL}		V_{DD}		$V_{SS} - 4.0$	V
Logic Input HIGH Level	V_{IH}	$V_{SS} = +5.0V$	3.0	3.5		V
Logic Input HIGH Level	V_{IH}		$V_{SS} - 2.0$		$V_{SS} + 0.3$	V
Channel Switching Time-Positive	t^+	Switching Time Test Circuit		300		ns
Channel Switching Time-Negative	t^-			600		ns
Channel Separation		f = 1 kHz		62		dB
Output Capacitance	C_{db}	$V_{SS} - V_{OUT} = 0$; f = 1 MHz		35		pF
Data Input Capacitance	C_{sb}	$V_{SS} - V_{DIP} = 0$; f = 1 MHz		6.0		pF
Logic Input Capacitance	C_{cg}	$V_{SS} - V_{Logic\ In} = 0$; f = 1 MHz		6.0		pF
Power Dissipation	P_D	$V_{DD} = -31V$, $V_{SS} = 0V$		125	175	mW

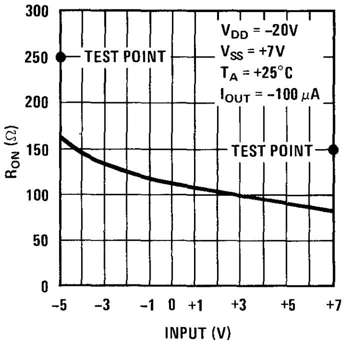
Note 1: All voltages referenced to V_{SS}.

Note 2: Rating applies for ambient temperatures to +25°C, derate linearly at 3 mW/°C for ambient temperatures above +25°C.

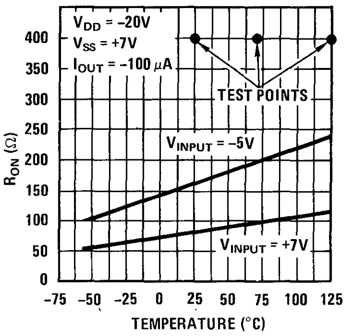
Note 3: Specifications apply for $T_A = 25°C$, $-24V \leq V_{DD} \leq -20V$, and $+5.0V \leq V_{SS} \leq +7.0V$; unless otherwise specified (all voltages are referenced to ground).

typical performance characteristics

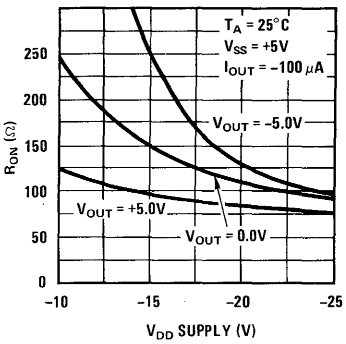
ON Resistance vs Analog Input Voltage



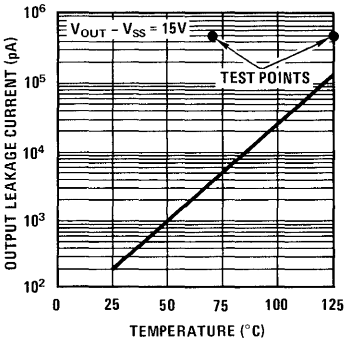
ON Resistance vs Ambient Temperature



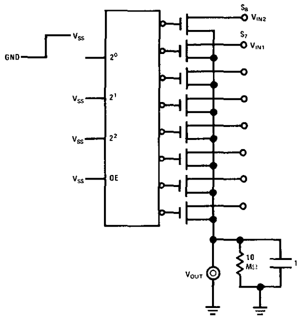
ON Resistance vs V_{DD} Supply Voltage

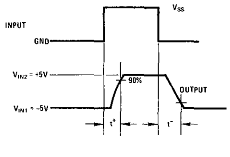


Output Leakage Current vs Ambient Temperature



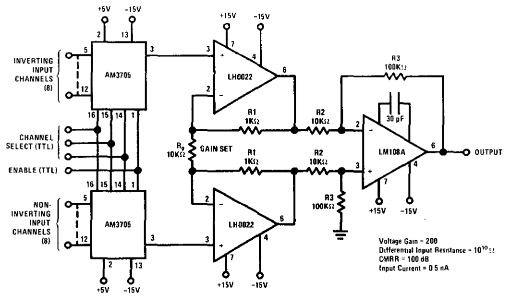
switching time test circuit





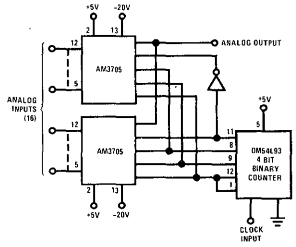
typical applications (con't.)

Differential Input MUX

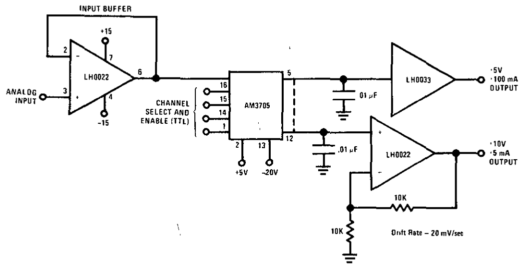


Voltage Gain = 200
Differential Input Resistance = 10^{10} Ω
CMRR = 100 dB
Input Current = 0.5 nA

16-Channel Commutator

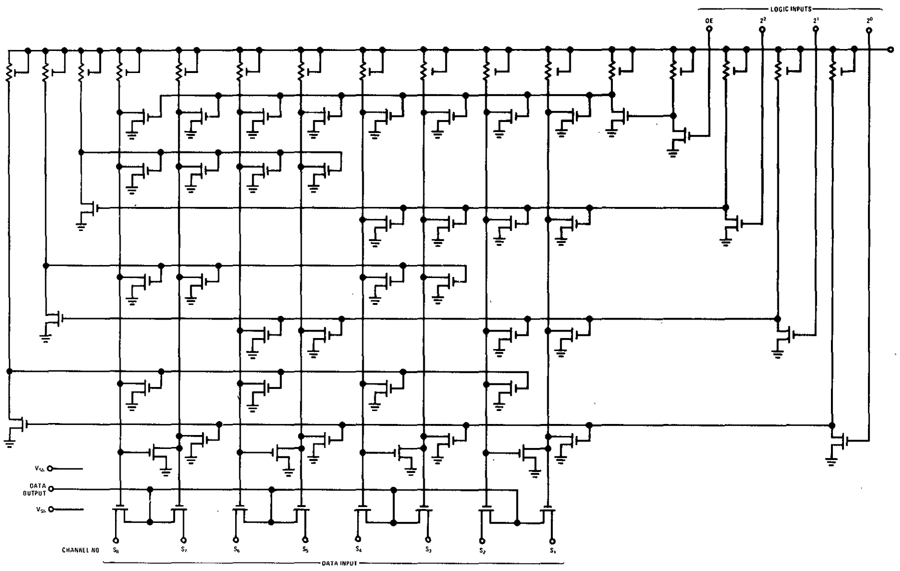


8-Channel Demultiplexer with Sample and Hold



Drift Rate – 20 mV/sec

schematic diagram



analog switch data sheets

For specifications on other National analog switches and analog interface circuits, see the following data sheets:

MOS Analog Switches

Dual Differential – MM450/MM550
Triple – MM455/MM555
Quad – MM452/MM552
Four Channel – MM451/MM551
Four Channel with Commutator – MM454/MM554
Six Channel – AM2009/AM2009C

TTL/DTL Compatible MOS

DPDT – AH0014/AH0014C
Quad SPST – AH0015/AH0015C
DPST – AH0019/AH0019C

TTL/DTL Compatible J-FET

Dual DPST
Dual SPST
Dual DPDT (Diff) } AH0100/AH0100C Series
SPDT (Diff)

High Level Compatible J-FET

DPST – AH2114/AH2114C

Ultra High Speed J-FET

±10V; 30Ω – AM1000
±15V; 50Ω – AM1001
±10V; 100Ω – AM1002

N-Channel Discrete J-FET Switches

5 Ohm – 2N5432
7 Ohm – 2N5433
10 Ohm – 2N5434

ANALOG SWITCH DRIVERS

TTL Dual Level Translator – DM7800/DM8800
TTL Dual High Speed Translator – DH0034/DH0034C
Analog Comparator/Level Translator – LM111 Series

SAMPLE AND HOLD CIRCUITS

Low Drift Precision – LH0023/LH0023C
High Speed – LH0043/LH0043C

Plus a complete line of amplifiers comparators and voltage regulators.

Analog Switches

NH0014/NH0014C DPDT
NH0019/NH0019C(MH453/MH553) dual DPST
DTL/TTL compatible MOS analog switches

general description

This series of DTL/TTL compatible MOS analog switches feature high speed with internal level shifting and driving. The package contains two monolithic integrated circuit chips: the MOS analog chip is similar to the MM450 type which consists of four MOS analog switch transistors connected in dual differential configuration; the second chip is a bipolar I.C. gate and level shifter. The devices feature:

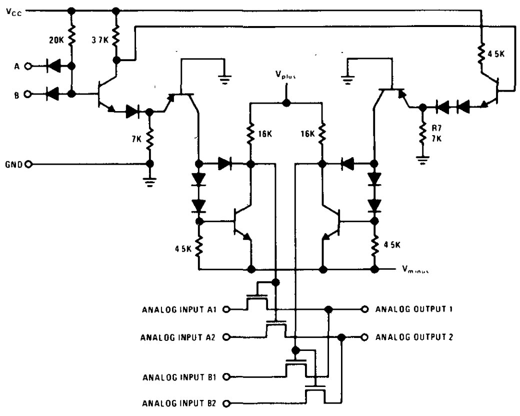
■ Large Analog Voltage Switching	±10V
■ Low ON Resistance	200Ω
■ High OFF Resistance	10^{11} Ω

- Fully compatible with DTL or TTL logic
- Includes gating and level shifting

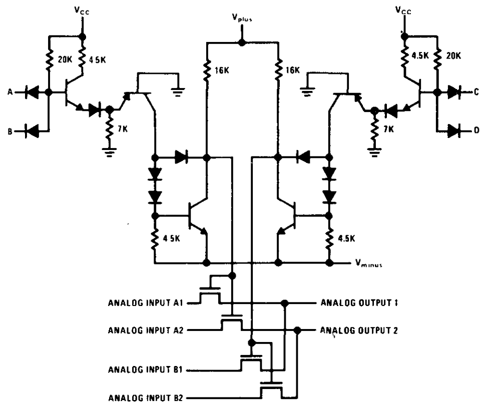
The devices, packaged in hermetic 14 lead flat and dual-in-line packages, are suitable for many airborne communication and analog signal switching applications.

schematic and connection diagrams

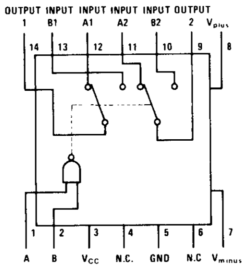
NH0014



NH0019

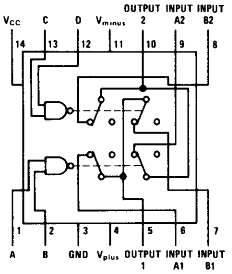


Flat Package



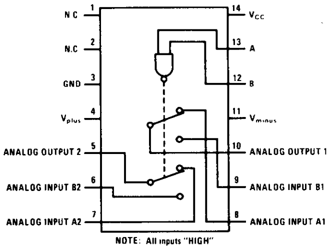
NOTE: All inputs "HIGH"

Flat Package



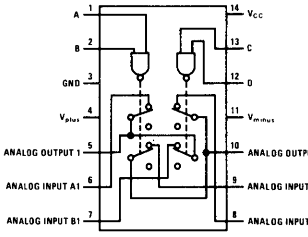
NOTE: All inputs "HIGH"

Dual-In-Line Package



NOTE: All inputs "HIGH"

Dual-In-Line Package



NOTE All inputs "HIGH"

absolute maximum ratings

V_{CC} Supply Voltage	7.0V
Vminus Supply Voltage	-30V
Vplus Supply Voltage	+30V
Vplus/Vminus Voltage Differential	40V
Logic Input Voltage	5.5V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range NH0014, NH0019	-55°C to +125°C
NH0014C, NH0019C	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Note 1)

PARAMETER	CONDITIONS	MIN	TYP (Note 3)	MAX	UNITS
Logical "1" Input Voltage	V_{CC} = 4.5V	2.0			V
Logical "0" Input Voltage	V_{CC} = 4.5V			0.8	V
Logical "1" Input Current	V_{CC} = 5.5V V_{IN} = 2.4V			5	μA
Logical "1" Input Current	V_{CC} = 5.5V V_{IN} = 5.5V			1	mA
Logical "0" Input Current	V_{CC} = 5.5V V_{IN} = 0.4V		0.2	0.4	mA
Power Supply Current Logical "1" input NH0019, NH0019C—each gate (Note 2)	V_{CC} = 5.5V V_{IN} = 4.5V		0.85	1.6	mA
Power Supply Current Logical "0" input NH0019, NH0019C—each gate (Note 2)	V_{CC} = 5.5V V_{IN} = 0V		0.22	0.41	mA
Power Supply Current Logical "1" input NH0014, NH0014C (Note 2)	V_{CC} = 5.5V V_{IN} = 4.5V		0.85	1.6	mA
Power Supply Current Logical "0" input NH0014, NH0014C (Note 2)	V_{CC} = 5.5V V_{IN} = 0V		1.5	3.0	mA
Analog Switch ON Resistance	V_{IN} (Analog) = +10V		75	200	Ω
(each gate)	V_{IN} (Analog) = -10V		200	600	Ω
Analog Switch OFF Resistance			10^{11}		Ω
Analog Switch Input Leakage Current	V_{IN} = -10V T_A = 25°C		0.05	10	nA
NH0014C, NH0019C	(Note 4) T_A = 70°C		4	50	nA
NH0014, NH0019	V_{IN} = -10V T_A = 25°C		25	200	pA
	(Note 4) T_A = 125°C		25	200	nA
Analog Switch Output Leakage Current	V_{OUT} = -10V T_A = 25°C		0.1	10	nA
NH0014C, NH0019C	(Note 4) T_A = 70°C		30	100	nA
NH0014, NH0019	V_{OUT} = -10V T_A = 25°C		40	400	pA
	(Note 4) T_A = 125°C		40	400	nA
Analog Input (Drain) Capacitance	1 MHz @ Zero Bias		8	10	pF
Output Source Capacitance	1 MHz @ Zero Bias		11	13	pF
Output Transition Time for Logical "0" Input	T_A = 25°C		200		ns
Output Transition Time for	T_A = 25°C				
Logical "1" Input NH0019, NH0019C			100		ns
NH0014, NH0014C			250		ns

Note 1: Min/max limits apply across the guaranteed temperature range of -55°C to +125°C for NH0014, NH0019 and 0°C to 70°C for NH0014C, NH0019C. V_{minus} = -20V, V_{plus} = +10V and an analog test current of 1 mA unless otherwise specified.

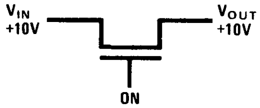
Note 2: Current measured is drawn from V_{CC} supply.

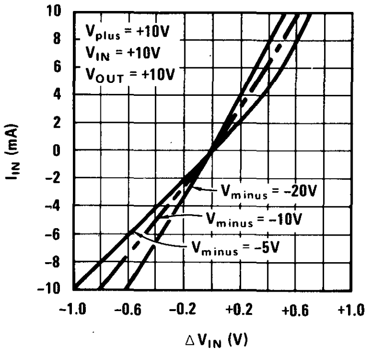
Note 3: All typical values are measured at T_A = 25°C with V_{CC} = 5.0V. V_{plus} = +10V, V_{minus} = -22V unless otherwise noted.

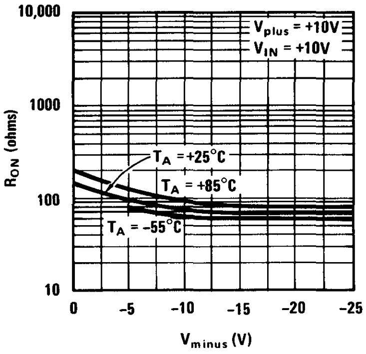
Note 4: All analog switch pins except measurement pin are tied to V_{plus}.

analog switch performance characteristics (Note 3)

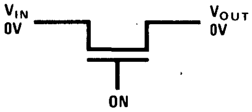
CONDITION 1 AT +10V

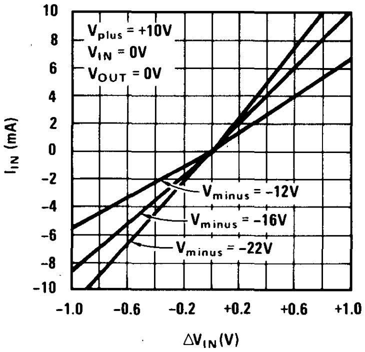


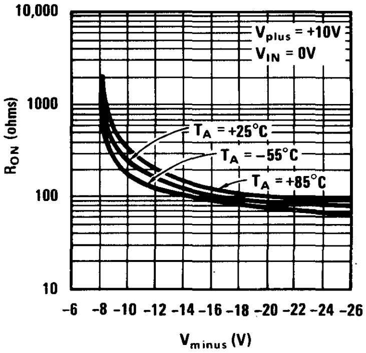

DYNAMIC R_{ON}


R_{ON} vs V_{minus}

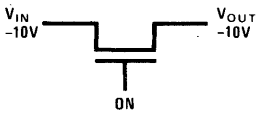
CONDITION 2 AT 0V

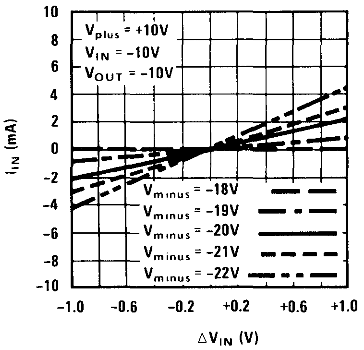


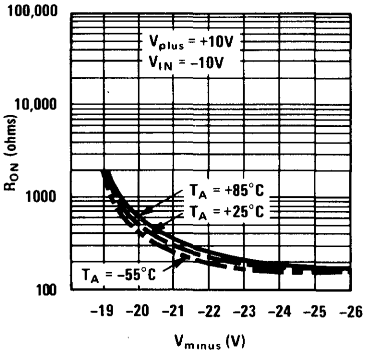

DYNAMIC R_{ON}

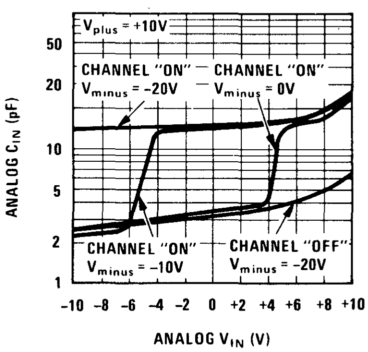

R_{ON} vs V_{minus}

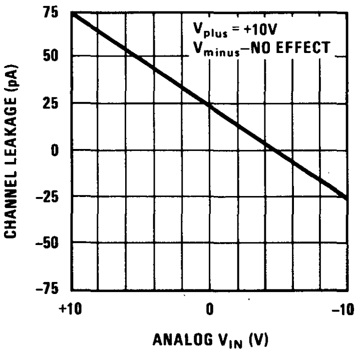
CONDITION 3 AT -10V

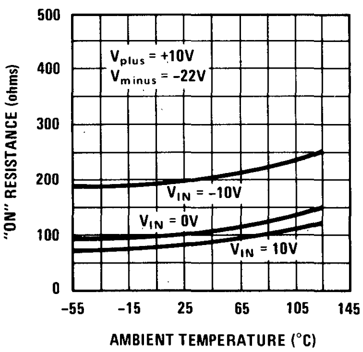



DYNAMIC R_{ON}


R_{ON} vs V_{minus}

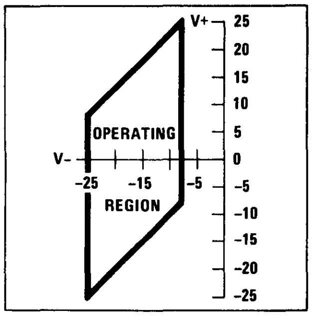

C_{IN} vs V_{IN}


Leakage vs V_{IN} (Channel "OFF"


R_{ON} vs Temperature

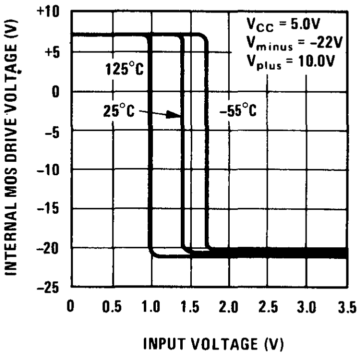
selecting power supply voltage

The graph shows the boundary conditions which must be used for proper operation of the unit. The range of operation for power supply V_{minus} is shown on the X axis. It must be between −25V and −8V. The allowable range for power supply V_{plus} is governed by supply V_{minus}. With a value chosen for V_{minus}, V_{plus} may be selected as any value along a vertical line passing through the V_{minus} value and terminated by the boundaries of the operating region. A voltage difference between power supplies of at least 5V should be maintained for adequate signal swing.



level shifter characteristics

V_{IN}-V_{OUT}



Logic Elements

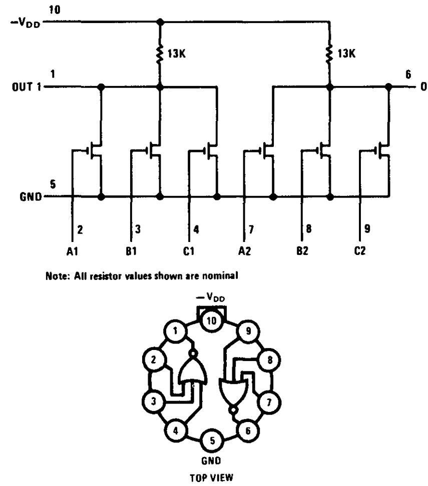
MM480/MM580 series MOS logic elements

general description

National's line of monolithic MOS gates and flip-flops are built utilizing P channel enhancement mode transistors. Zener diodes are used on all inputs to protect against static discharge. These devices are members of a family of compatible logic functions that feature low threshold voltage transistors, enabling operation at a V_{DD} supply of −10 volts and low power consumption in systems that operate at frequencies up to 2 MHz.

The JK flip-flops are particularly suited for counter and register applications in MOS systems. Both true and complement outputs are buffered to prevent false triggering from the outputs and also provide the capability to "wire AND" at the outputs.

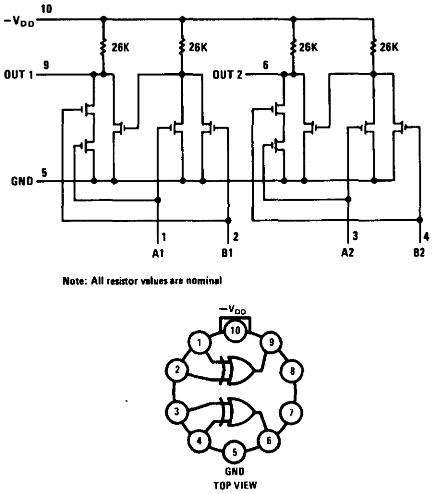
schematic and connection diagrams



Note: All resistor values shown are nominal

NOTE: Pin 5 connected to case

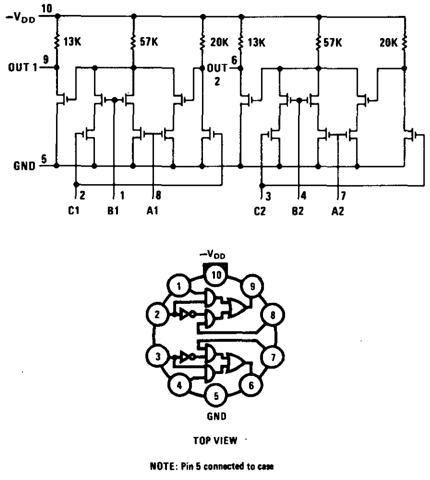
MM480/MM580 dual 3-input NOR gate



Note: All resistor values are nominal

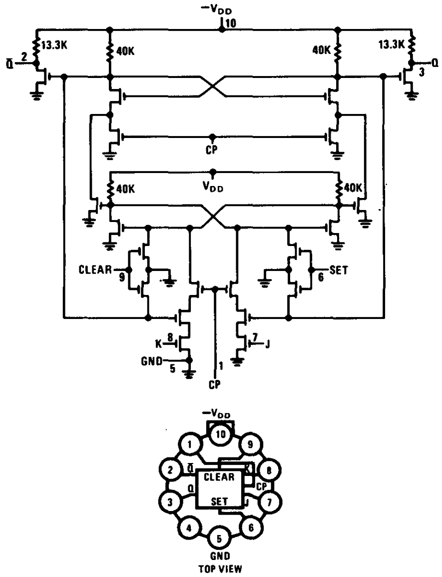
Note: Pin 5 connected to case

MM481/MM581 dual exclusive OR gate



NOTE: Pin 5 connected to case

MM482/MM582 dual digital multiplex switch



NOTE: Pin 5 connected to case.

MM483/MM583 JK flip flop

absolute maximum ratings

Supply Voltage (V_{DD})	+0.5V to −25V
Data Inputs	+0.5V to −25V
Operating Temperature (MM480, MM481, MM482, MM483)	−55°C to +125°C
(MM580, MM581, MM582, MM583)	− 25°C to +70°C
Storage Temperature	−65°C to +150°C

electrical characteristics (Note 1)

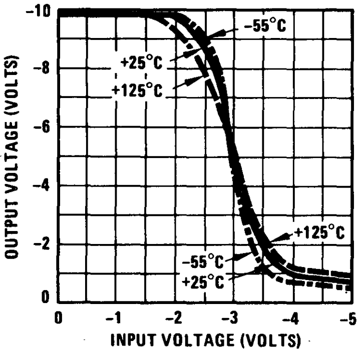
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage						
Logic "0"		V_{IN} = −7.0V for Logic "1"		−0.2	−1.0	V
Logic "1"		V_{IN} = −1.5V for Logic "0"	−8.0	−10.0		V
Input Leakage		V_{IN} = −11.0V		<1.0 nA	−3.0	μA
Fan Out			10			
Power Dissipation, Each Half						
	MM480/MM580	V_{OUT} = Logic "0"		7.5	12	mW
	MM481/MM581	$V_A = V_B = -10V$		7.5	12	mW
	MM482/MM582	$V_A = V_B = 0V$ $V_C = -10V$		12.7	20	mW
	MM483/MM583	Toggle Mode Clock Frequency = 100 kHz		13.0	20.5	mW
Propagation Delay (Gate Circuits)						
T_{PD1}	MM480/MM580	C_{LOAD} = 10 pF T_A = 25°C		25	50	ns
T_{PD2}	MM480/MM580			250	400	ns
T_{PD1}	MM481/MM581			425	600	ns
T_{PD2}	MM481/MM581			130	200	ns
T_{PD1}	MM482/MM582			230	350	ns
T_{PD2}	MM482/MM582			350	600	ns
Toggle Rate	MM483/MM583	C_{LOAD} = 10 pF	1.0	2.0		MHz
Transient Response	MM483/MM583					
Rise Time, T_R		C_{LOAD} = 10 pF T_A = 25°C		120	200	ns
Fall Time, T_F				300	450	ns
Propagation Delay	MM483/MM583					
T_{PD1}		C_{LOAD} = 10 pF T_A = 25°C		600	850	ns
T_{PD2}				400	550	ns
T_{PD3}				280	400	ns
T_{PD4}				350	500	ns

Note 1: These specifications apply over the specified operating temperature range for $V_{DD} = -10V$ ±10% unless otherwise specified. Typical values are for $V_{DD} = -10.0V$ and $T_A = 25°C$.

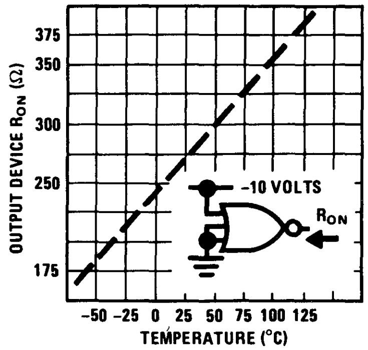
typical performance characteristics

MM480/MM580

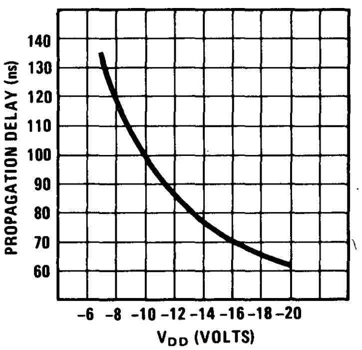
Voltage Transfer Characteristic



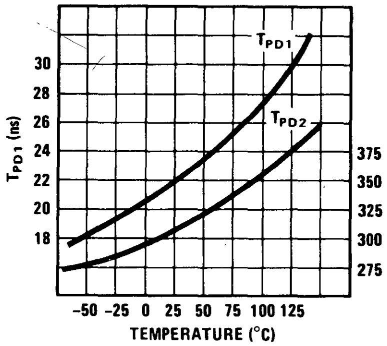
Output Device R_{ON} vs Temperature



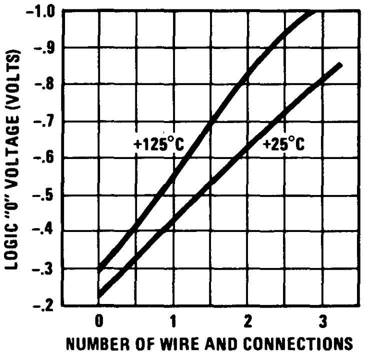
Average Propagation Delay vs Power Supply Voltage (V_{DD}) (See Figure 1)



Propagation Delay vs Temperature

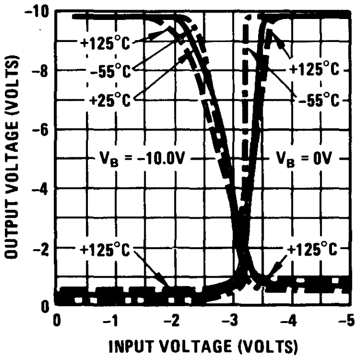


Logic "0" Voltage vs Wire AND Connections (See Figure 4)

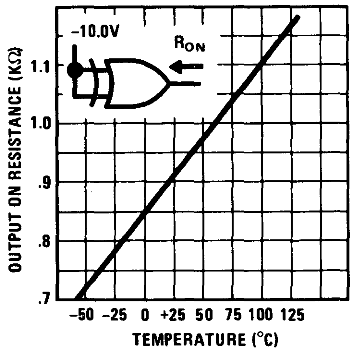


MM481/MM581

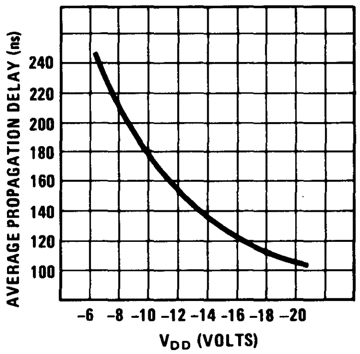
Voltage Transfer Characteristics



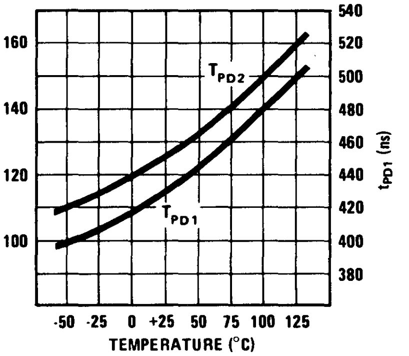
Output ON Resistance vs Temperature



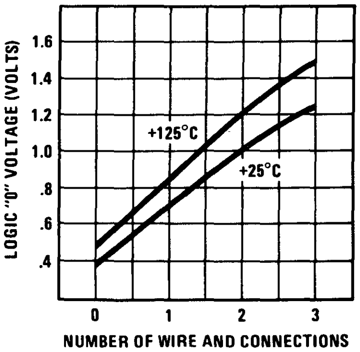
Average Propagation Delay vs Power Supply Voltage (V_{DD}) (See Figure 2)



Propagation Delay vs Temperature

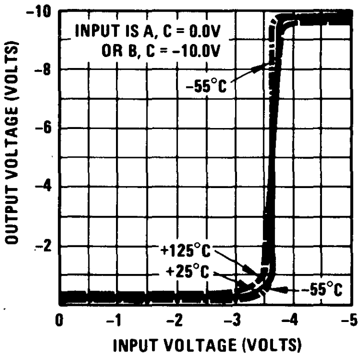


Logic "0" vs Wire AND Connectors (See Figure 5)

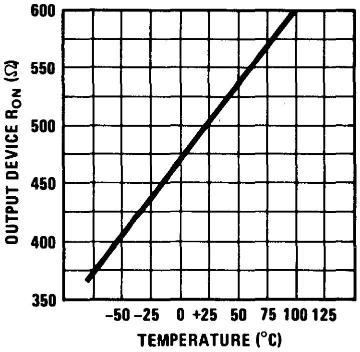


MM482/MM582

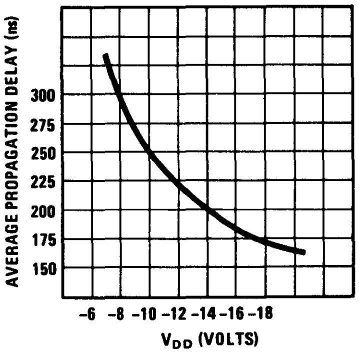
Voltage Transfer Characteristics



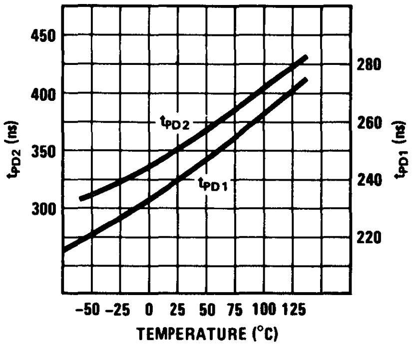
Output Device R_{ON} vs Temperature



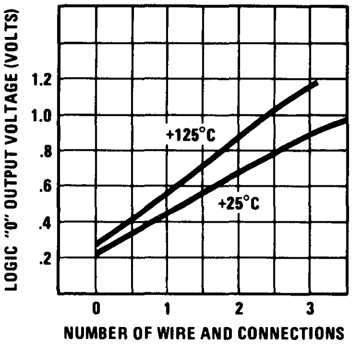
Average Propagation Delay vs Power Supply Voltage V_{DD} (See Figure 3)



Propagation Delay vs Temperature

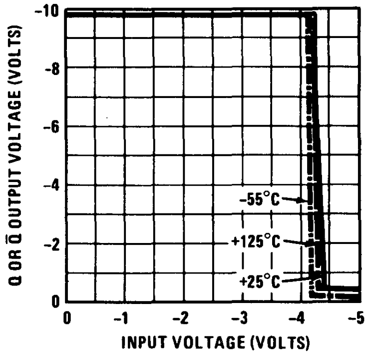


Logic "0" Output Voltage vs Wire AND Connection (See Figure 6)

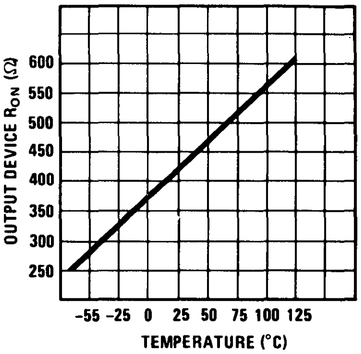


MM483/MM583

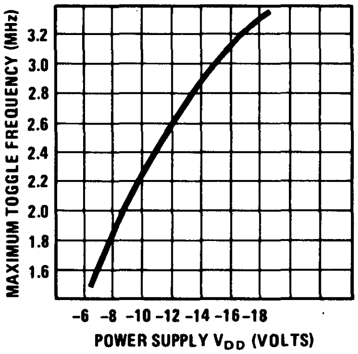
Voltage Transfer Characteristics Set and Clear Inputs



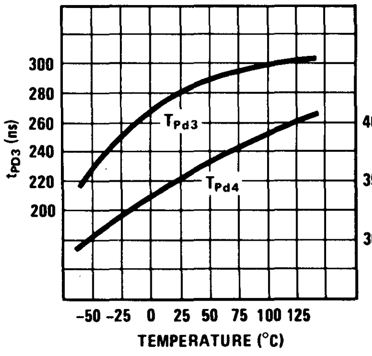
Output Device R_{on} vs Temperature



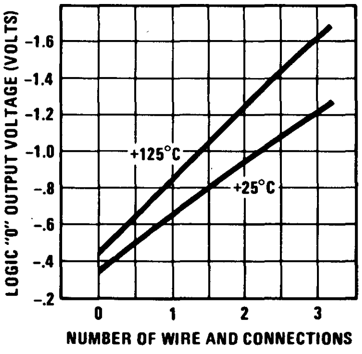
Toggle Frequency vs Power Supply Voltage (V_{DD})



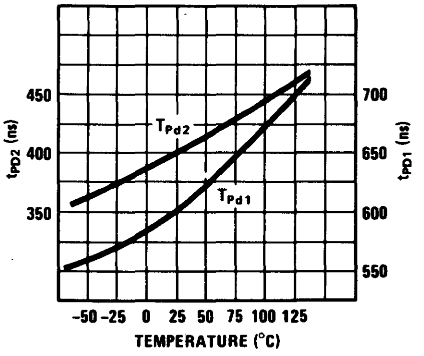
Propagation Delay vs Temperature



Logic "0" Voltage vs Wire AND Connection (See Figure 7)

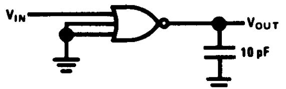


Propagation Delay vs Temperature

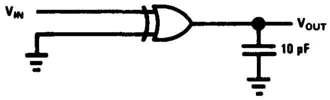


propagation delay test circuits (gates)

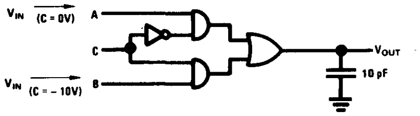
MM480/MM580



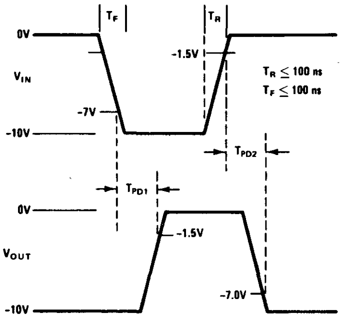
MM481/MM581



MM482/MM582



MM480/MM580,MM481/MM581,MM482/MM582



MM480/MM580

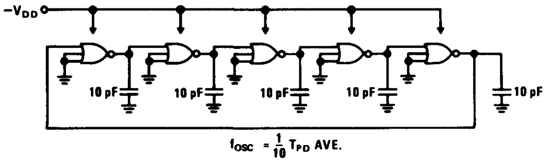


FIGURE 1. Ring Oscillator for Measuring Average Propagation Delay

MM481/MM581

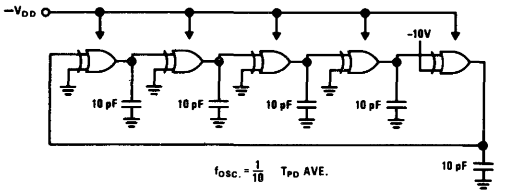


FIGURE 2. Ring Oscillator for Measuring Average Propagation Delay

MM482/MM582

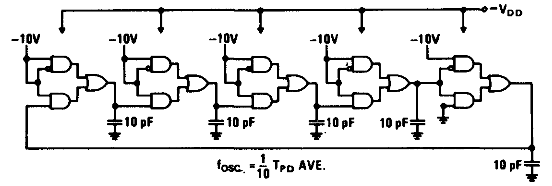
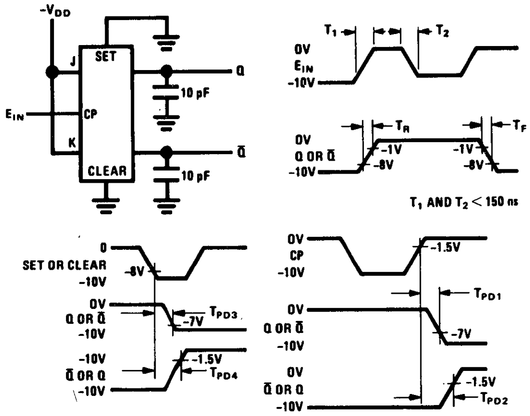


FIGURE 3. Ring Oscillator For Measuring Average Propagation Delay

transient response test circuits

MM483/MM583



wire "AND" test circuits

MM480/MM580

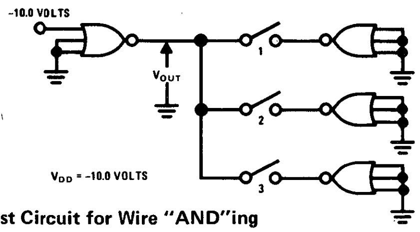


FIGURE 4. Test Circuit for Wire "AND"ing

MM481/MM581

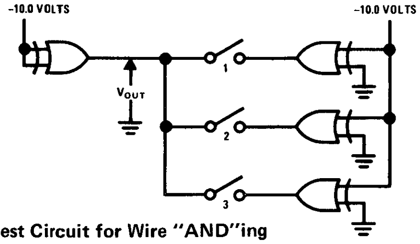


FIGURE 5. Test Circuit for Wire "AND"ing

MM482/MM582

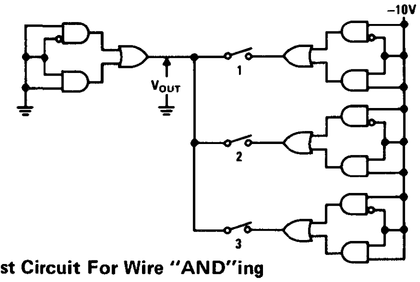


FIGURE 6. Test Circuit For Wire "AND"ing

MM483/MM583

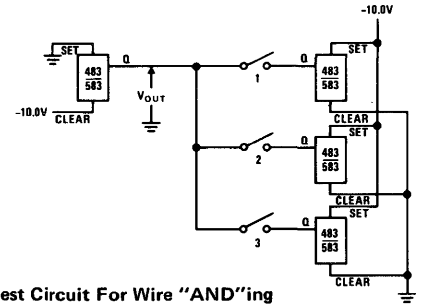


FIGURE 7. Test Circuit For Wire "AND"ing

ROM Character Generators

MM4220NP/MM5220NP, MM4230NN/MM5230NN, MM4230NO/MM5230NO, 7×9 horizontal scan display character generator

general description

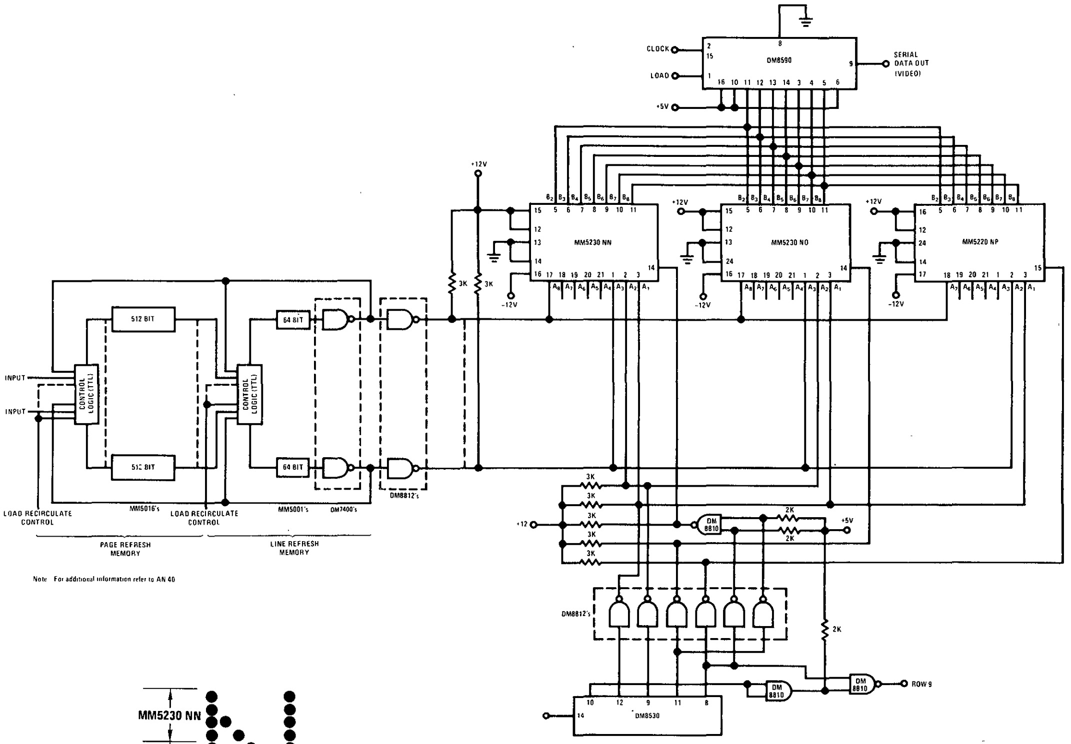
The MM4220NP/MM5220NP is a 1024-bit read-only memory and the MM4230NN/MM5230NN and MM4230NO/MM5230NO are 2048-bit read-only memories programmed to generate a font of 64 7x9 dot-type raster or horizontal-scan characters.

The typical application shows the ASCII-address system. The display refresh memory, built with MOS dynamic shift registers, and the TTL control techniques are similar to those described in *Application Note AN-40.* Designs for vertical-scan fonts, printer character generators, and designs for fonts larger than 7x9 are also outlined in *AN-40.*

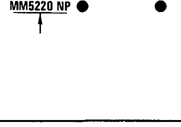
For full electrical, environmental and mechanical details, refer to the MM4220/MM5220 and MM4230/MM5230 data sheets.

typical application

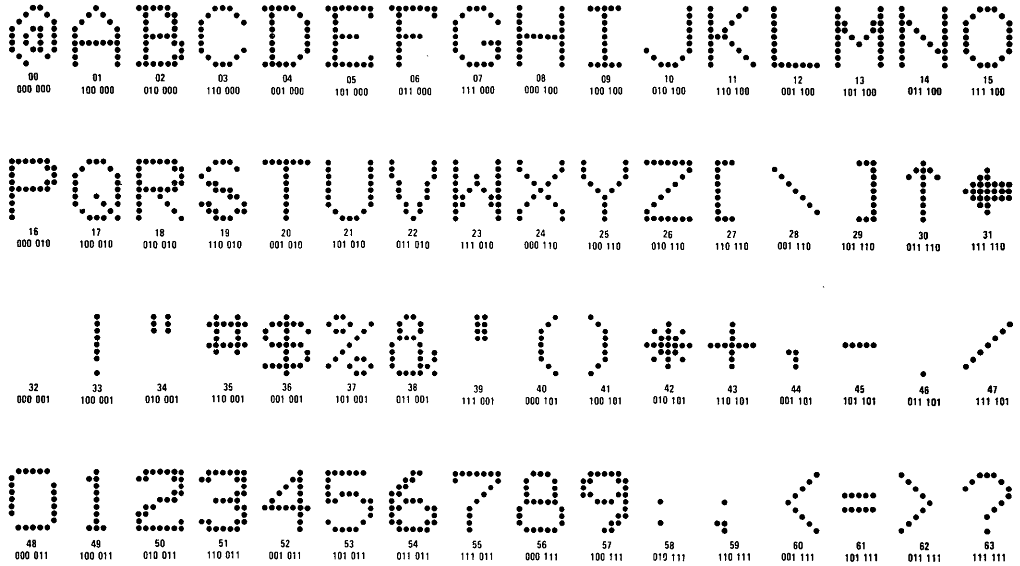
7x9 Character Generator System



Note: For additional information refer to AN 40



character font



Note. Input addresses are in six bit ASCII code and are shown in the sequence $A_0, A_1 \dots A_5$.

ROM Character Generators

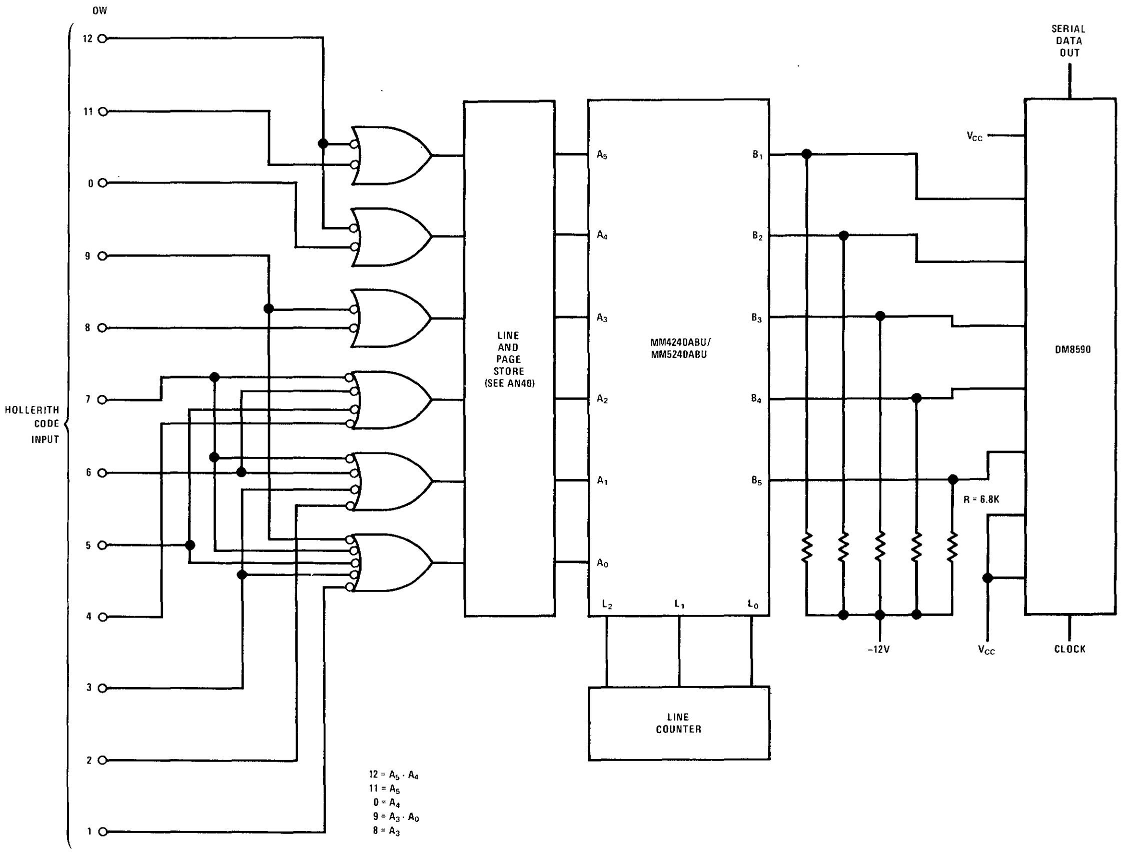
MM4240ABU/MM5240ABU hollerith character generator

general description

The MM4240ABU/MM5240ABU is a 64 x 8 x 5 read-only memory programmed to display a 64-character subset of the Hollerith 12-line code, normally used in punching 80 column cards. Compression from 12 lines to the six needed to make up a 64-character set may be accomplished as shown in the typical application.

For electrical, environmental and mechanical details, refer to the MM4240/MM5240 data sheet.

typical application



Note Hole present gives closure to GND

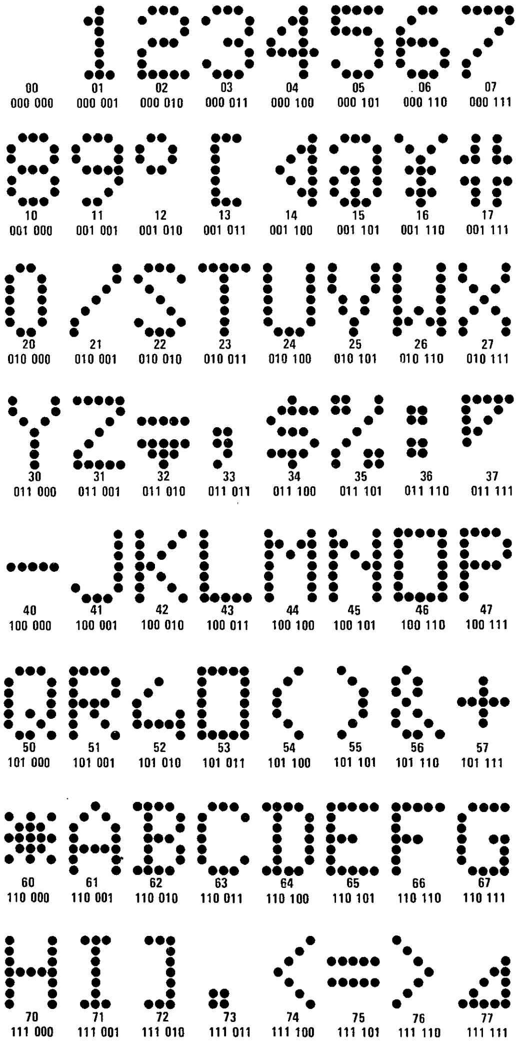
*For additional application information on incorporating this device in a display system, see AN40 "A Systems Approach to Character Generators".

code table

HOLLERITH INPUT CODE (NON-COMPRESSED)	OCTAL SEQUENCE	GRAPHIC DISPLAY
	00	(space)
1	01	1
2	02	2
3	03	3
4	04	4
5	05	5
6	06	6
7	07	7
8	10	8
9	11	9
8 2	12	
8 3	13	
8 4	14	
8 5	15	
8 6	16	
8 7	17	
	20	
0	21	0
0 1	22	/
0 2	23	S
0 3	24	T
0 4	25	U
0 5	26	V
0 6	27	W
0 7	28	X
0 8	30	Y
0 9	31	Z
0 8 2	32	
0 8 3	33	
0 8 4	34	
0 8 5	35	
0 8 6	36	
0 8 7	37	
11	40	
11 1	41	J
11 2	42	K
11 3	43	L
11 4	44	M
11 5	45	N
11 6	46	O
11 7	47	P
11 8	50	Q
11 9	51	R
11 8 2	52	
11 8 3	53	
11 8 4	54	
11 8 5	55	
11 8 6	56	
11 8 7	57	
12	60	
12 1	61	A
12 2	62	B
12 3	63	C
12 4	64	D
12 5	65	E
12 6	66	F
12 7	67	G
12 8	70	H
12 9	71	I
12 8 2	72	
12 8 3	73	. (period)
12 8 4	74	
12 8 5	75	
12 8 6	76	
12 8 7	77	

character font

MM4240ABU/MM5240ABU



ROM Character Generators

MM4240ABZ/MM5240ABZ EBCDIC-8 character generator

general description

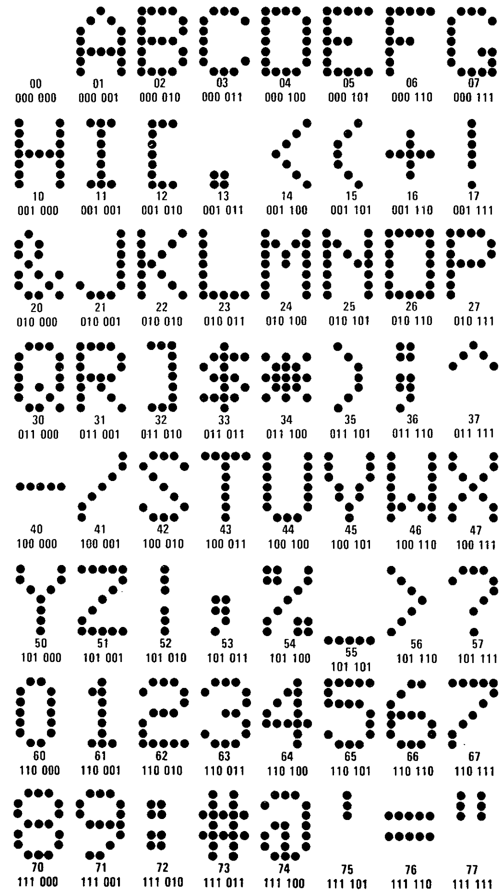
The MM4240ABZ/MM5240ABZ is a 64 x 8 x 5 read only memory that has been programmed to display the 64 character graphic subset of EBCDIC-8, an Extended Binary Coded Decimal Interchange Code with character assignments and locations conforming to the American Standard x 3.26–1970 (see MM5230QX data sheet for full EBCDIC-8 table).

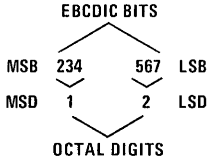
Compression of the eight bits of EBCDIC-8 to the six needed for a 64-character subset is accomplished by simply ignoring the two most significant EBCDIC bits, bit 0 and bit 1.

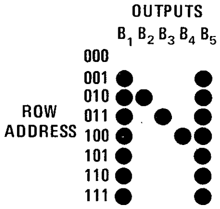
The octal character address digits are then formed as shown below.

For electrical, environmental and mechanical details, refer to the MM4240/MM5240 data sheet.

character font







ROM Character Generators

MM4240ACA/MM5240ACA EBCDIC character generator

general description

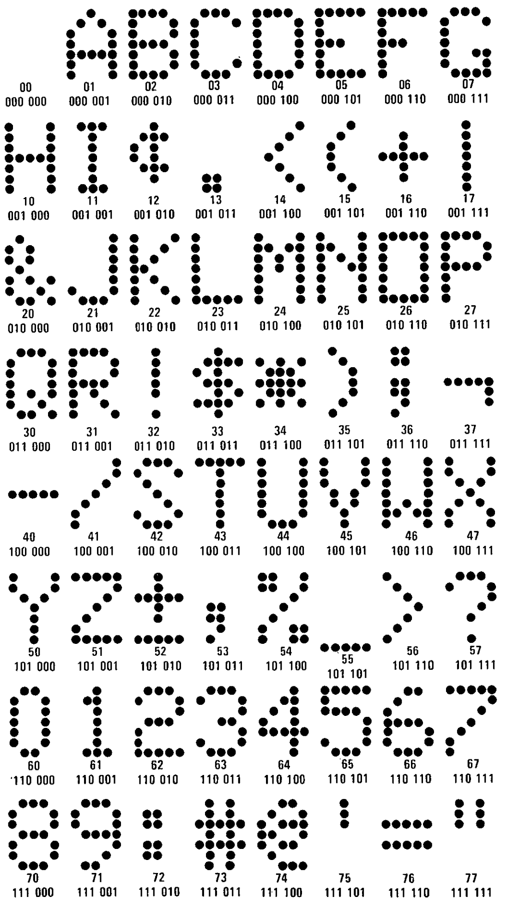
The MM4240ACA/MM5240ACA is a 64 x 8 x 5 read only memory that has been programmed to display the 64 character graphic subset of EBCDIC, an Extended Binary Coded Decimal Interchange code typically used in IBM systems.

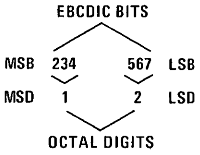
Compression of the eight bits of EBCDIC to the six needed for a 64-character subset is accomplished by simply ignoring the two most significant EBCDIC bits, bit zero and bit one.

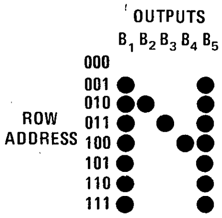
The octal character address digits are then formed as shown below.

For electrical, environmental and mechanical details, refer to the MM4240/MM5240 data sheet.

character font







ROM Code Converters

SK0003 sine/cosine look-up table kit

general description

The SK0003 Sine/Cosine Look-Up Table Kit consists of four MOS ROMs: three MM4210/MM5210's and one MM4220/MM5220-1024 bit static read only memories. They are P-channel enhancement mode monolithic MOS integrated circuits utilizing a low threshold technology.

THE SINE FUNCTION

The SK0003 implements the equation $\sin\theta = \sin M \cos L + \cos M \sin L$. Cos L was assumed to be 1 in the equation. However, it is a variable between 1 and 0.99998 and is a function of round off error. Worst case error is 1–5/8 bits in LSB at address 1415 (62.25°). The error increases from zero to .002% every 8 bits, therefore, the MM4220/MM5220 provides the error correction factor $\cos(M - 2.81°)\sin L$ in the equation $\sin\theta = \sin M + \cos(M - 2.81°)\sin L$. The circuitry to perform this function is shown in Figure 1. Additional information is available in *MOS Brief 10.*

THE COSINE FUNCTION

To generate the cosine function $\cos\theta = \sin(\theta - 90°)$, the input must be complemented and a logical "1" added. Figure 2A is a logic diagram of the circuitry used to provide the cosine function, as well as providing both sine and cosine functions in the same system. 11-bit resolution and 12-bit accuracy ±1–5/8-bits is achieved in this configuration.

A reduction in logic can be achieved as shown in Figure 2B if a loss in resolution of 1/2-bit in an 11-bit input or 1/4-bit in a 10-bit input is acceptable.

ELECTRICAL CHARACTERISTICS

Refer to the appropriate data sheet for each device shown in the figures. The devices noted are: MM4210/MM5210, MM4220/MM5220, DM5483/DM7483, DM7812/DM8812 and DM5486/DM7486.

logic diagram

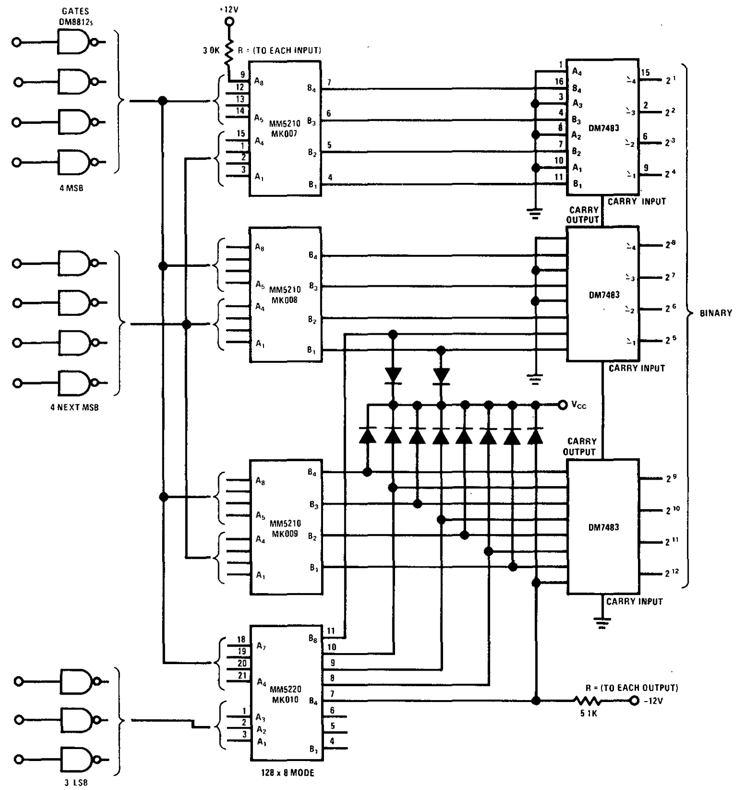


FIGURE 1. SK0003 Logic Diagram (Kit Includes ROMs Only). This Circuit Provides 11-Bit Resolution and 12-Bit Accuracy in a θ to Sin θ Converter.

logic diagram

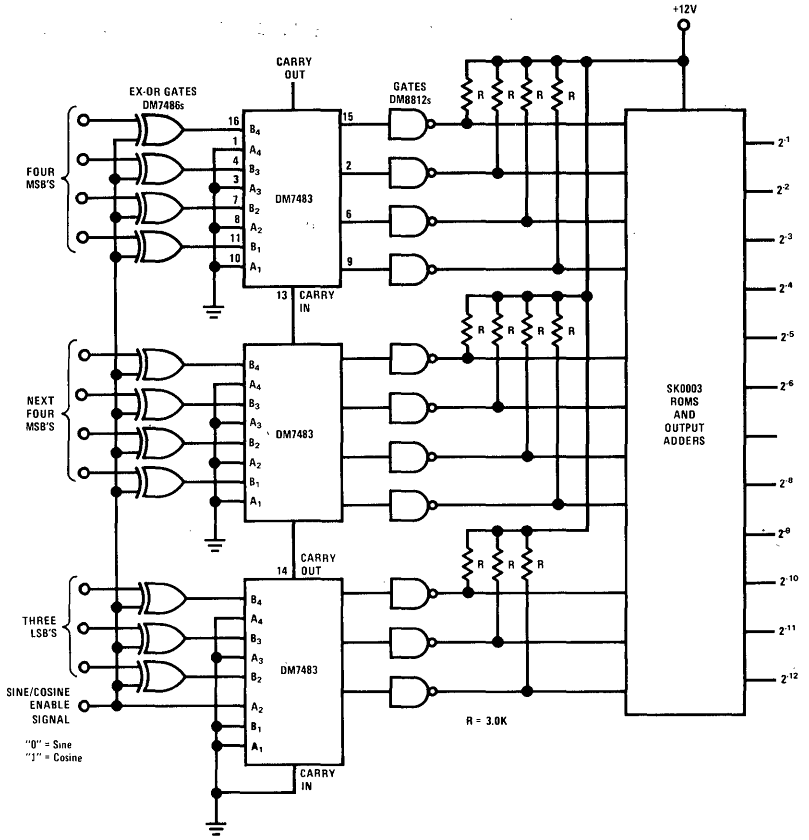


FIGURE 2A. Sine/Cosine Conversion Provides 11-Bit Resolution, 12-Bit ±1-5/8 Bit Accuracy.

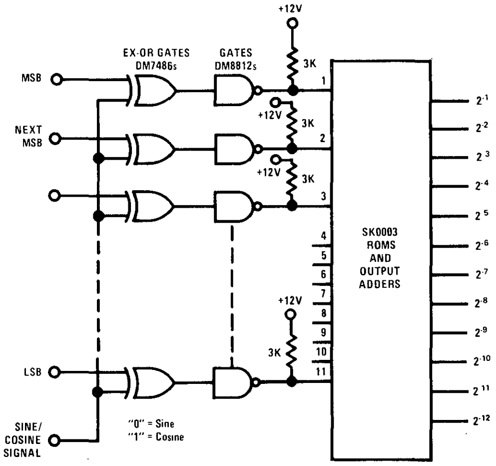


FIGURE 2B. Sine/Cosine Conversion with Cosine Approximated. (Cosine Conversion has 10-Bits Input Resolution and 12-Bit ±1-5/8-Bit Accuracy.)

ROM Code Converters

MM4220AE/MM5220AE ASCII-7 to hollerith code converter

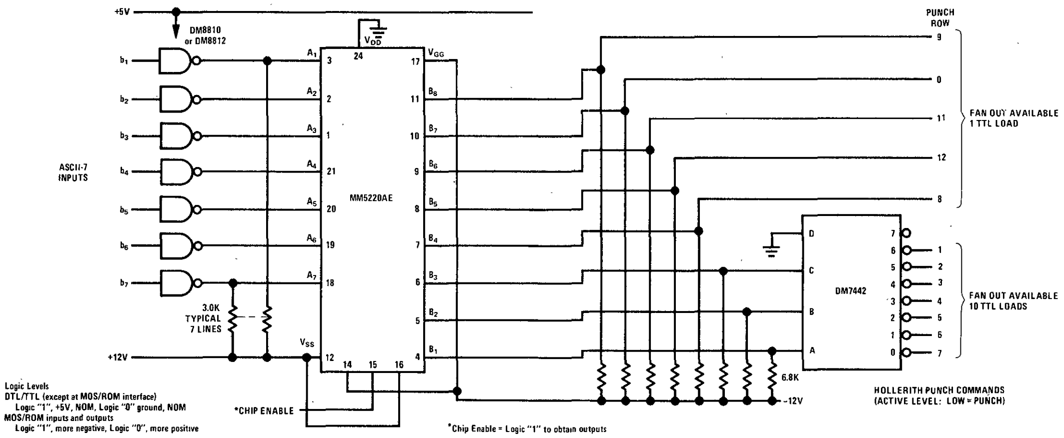
general description

The MM4220AE/MM5220AE 1024-bit read-only memory has been programmed to convert the 128 entries of the American Standard Code for Information Interchange in seven bits (ASCII-7) to Hollerith code (compressed to eight bits). The conversion performed follows the recommendation of American National Standard ANSI x 3.26–1970, Hollerith punched card code.

The typical application shows a recommended circuit for re-expansion of the Hollerith code to twelve lines.

For electrical, environmental and mechanical details, refer to the MM4220/MM5220 data sheet.

typical application



Logic Levels
DTL/TTL (except at MOS/ROM interface)
Logic "1", +5V, NOM, Logic "0" ground, NOM
MOS/ROM inputs and outputs
Logic "1", more negative, Logic "0", more positive

*Chip Enable = Logic "1" to obtain outputs

code conversion tables

	b_7 b_6 b_5	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b_4 b_3 b_2 b_1	COL ROW	0	1	2	3	4	5	6	7
0000	0	NUL 12-0-9-8-1	DLE 12-11-9-8-1	SP NO PCH	0 0	@ 8-4	P 11-7	8-1	p 12-11-7
0001	1	SCH 12-9-1	DC1 11-9-1	! ① 12-8-7	1 1	A 12-1	Q 11-8	a 12-0-1	q 12-11-8
0010	2	STX 12-9-2	DC2 11-9-2	" 8-7	2 2	B 12-2	R 11-9	b 12-0-2	r 12-11-9
0011	3	ETX 12-9-3	DC3 11-9-3	= 8-3	3 3	C 12-3	S 0-2	c 12-0-3	s 11-0-2
0100	4	ECT 9-7	DC4 9-8-4	$ 11-8-3	4 4	D 12-4	T 0-3	d 12-0-4	t 11-0-3
0101	5	ENQ 0-9-8-5	NAK 9-8-5	% 0-8-4	5 5	E 12-5	U 0-4	e 12-0-5	u 11-0-4
0110	6	ACK 0-9-8-6	SYN 9-2	& 12	6 6	F 12-6	V 0-5	f 12-0-6	v 11-0-5
0111	7	BEL 0-9-8-7	ETB 0-9-6	' 8-5	7 7	G 12-7	W 0-6	g 12-0-7	w 11-0-6
1000	8	BS 11-9-6	CAN 11-9-8	(12-8-5	8 8	H 12-8	X 0-7	h 12-0-8	x 11-0-7
1001	9	HT 12-9-5	EM 11-9-8-1	) 11-8-5	9 9	I 12-9	Y 0-8	i 12-0-9	y 11-0-8
1010	10	IF 0-9-5	SUB 9-8-7	* 11-8-4	: 8-2	J 11-1	Z 0-9	j 12-11-1	z 11-0-9
1011	11	VT 12-9-8-3	ESC 0-9-7	+ 12-8-6	, 11-8-6	K 11-2	[12-8-2	k 12-11-2	} 12-0
1100	12	FF 12-9-8-4	FS 11-9-8-4	, 0-8-3	< 12-8-4	L 11-3	\\ 0-8-2	1 12-11-3	: 12-11
1101	13	CR 12-9-8-5	GS 11-9-8-5	– 11	= 8-6	M 11-4	] 11-8-2	m 12-11-4	{ 11-0
1110	14	SO 12-9-8-6	RS 11-9-8-6	. 12-8-3	> 0-8-6	N 11-5	∧ ② 11-8-7	n 12-11-5	~ 11-0-1
1111	15	SI 12-9-8-7	US 11-9-8-7	/ 0-1	? 0-8-7	O 11-6	– 0-8-5	o 12-11-6	DEL 12-9-7

① may be "|"

② may be "¬"

③ The top line in each entry to the table represents an assigned character (Columns 0 to 7).
The bottom line in each entry is the corresponding card hole-pattern.

ADD-RESS	OUTPUT CODE							
	B8	B7	B6	B5	B4	B3	B2	B1
0	1	1	0	1	1	0	0	1
1	1	0	0	1	0	0	0	1
2	1	0	0	1	0	0	1	0
3	1	0	0	1	0	0	1	1
4	1	0	0	0	0	1	1	1
5	1	1	0	0	1	1	0	1
6	1	1	0	0	1	1	1	0
7	1	1	0	0	1	1	1	1
8	1	0	1	0	0	1	1	0
9	1	0	0	1	0	1	0	1
10	1	1	0	0	0	1	0	1
11	1	0	0	1	1	0	1	1
12	1	0	0	1	1	1	0	0
13	1	0	0	1	1	1	0	1
14	1	0	0	1	1	1	1	0
15	1	0	0	1	1	1	1	1
16	1	0	1	1	1	0	0	1
17	1	0	1	0	0	0	0	1
18	1	0	1	0	0	0	1	0
19	1	0	1	0	0	0	1	1
20	1	0	0	0	1	1	0	0
21	1	0	0	0	1	1	0	1
22	1	0	0	0	0	0	1	0
23	1	1	0	0	0	1	1	0
24	1	0	1	0	1	0	0	0
25	1	0	1	0	1	0	0	1
26	1	0	0	0	1	1	1	1
27	1	1	0	0	0	1	1	1
28	1	0	1	0	1	1	0	0
29	1	0	1	0	1	1	0	1
30	1	0	1	0	1	1	1	0
31	1	0	1	0	1	1	1	1
32	0	0	0	0	0	0	0	0
33	0	0	0	1	1	1	1	1
34	0	0	0	0	1	1	1	1
35	0	0	0	0	1	0	1	1
36	0	0	1	0	1	0	1	1
37	0	1	0	0	1	1	0	0
38	0	0	0	1	0	0	0	0
39	0	0	0	0	1	1	0	1
40	0	0	0	1	1	1	0	1
41	0	0	1	0	1	1	0	1
42	0	0	1	0	1	1	0	0
ROW	9	0	11	12	8	4	2	1

ADD-RESS	OUTPUT CODE							
	B8	B7	B6	B5	B4	B3	B2	B1
43	0	0	0	1	1	1	1	0
44	0	1	0	0	1	0	1	1
45	0	0	1	0	0	0	0	0
46	0	0	0	1	1	0	1	1
47	0	1	0	0	0	0	0	1
48	0	1	0	0	0	0	0	0
49	0	0	0	0	0	0	0	1
50	0	0	0	0	0	0	1	0
51	0	0	0	0	0	0	1	1
52	0	0	0	0	0	1	0	0
53	0	0	0	0	0	1	0	1
54	0	0	0	0	0	1	1	0
55	0	0	0	0	0	1	1	1
56	0	0	0	0	1	0	0	0
57	1	0	0	0	0	0	0	0
58	0	0	0	0	1	0	1	0
59	0	0	1	0	1	1	1	0
60	0	0	0	1	1	1	0	0
61	0	0	0	0	1	1	1	0
62	0	1	0	0	1	1	1	0
63	0	1	0	0	1	1	1	1
64	0	0	0	0	1	1	0	0
65	0	0	0	1	0	0	0	1
66	0	0	0	1	0	0	1	0
67	0	0	0	1	0	0	1	1
68	0	0	0	1	0	1	0	0
69	0	0	0	1	0	1	0	1
70	0	0	0	1	0	1	1	0
71	0	0	0	1	0	1	1	1
72	0	0	0	1	1	0	0	0
73	1	0	0	1	0	0	0	0
74	0	0	1	0	0	0	0	1
75	0	0	1	0	0	0	1	0
76	0	0	1	0	0	0	1	1
77	0	0	1	0	0	1	0	0
78	0	0	1	0	0	1	0	1
79	0	0	1	0	0	1	1	0
80	0	0	1	0	0	1	1	1
81	0	0	1	0	1	0	0	0
82	1	0	1	0	0	0	0	0
83	0	1	0	0	0	0	1	0
84	0	1	0	0	0	0	1	1
85	0	1	0	0	0	1	0	0
ROW	9	0	11	12	8	4	2	1

ADD-RESS	OUTPUT CODE							
	B8	B7	B6	B5	B4	B3	B2	B1
86	0	1	0	0	0	1	0	1
87	0	1	0	0	0	1	1	0
88	0	1	0	0	0	1	1	1
89	0	1	0	0	1	0	0	0
90	1	1	0	0	0	0	0	0
91	0	0	0	1	1	0	1	0
92	0	1	0	0	1	0	1	0
93	0	0	1	0	1	0	1	0
94	0	0	1	0	1	1	1	1
95	0	1	0	0	1	1	0	1
96	0	0	0	0	1	0	0	1
97	0	1	0	1	0	0	0	1
98	0	1	0	1	0	0	1	0
99	0	1	0	1	0	0	1	1
100	0	1	0	1	0	1	0	0
101	0	1	0	1	0	1	0	1
102	0	1	0	1	0	1	1	0
103	0	1	0	1	0	1	1	1
104	0	1	0	1	1	0	0	0
105	1	1	0	1	0	0	0	0
106	0	0	1	1	0	0	0	1
107	0	0	1	1	0	0	1	0
108	0	0	1	1	0	0	1	1
109	0	0	1	1	0	1	0	0
110	0	0	1	1	0	1	0	1
111	0	0	1	1	0	1	1	0
112	0	0	1	1	0	1	1	1
113	0	0	1	1	1	0	0	0
114	1	0	1	1	0	0	0	0
115	0	1	1	0	0	0	1	0
116	0	1	1	0	0	0	1	1
117	0	1	1	0	0	1	0	0
118	0	1	1	0	0	1	0	1
119	0	1	1	0	0	1	1	0
120	0	1	1	0	0	1	1	1
121	0	1	1	0	1	0	0	0
122	1	1	1	0	0	0	0	0
123	0	1	0	1	0	0	0	0
124	0	0	1	1	0	0	0	0
125	0	1	1	0	0	0	0	0
126	0	1	1	0	0	0	0	1
127	1	0	0	1	0	1	1	1
ROW	9	0	11	12	8	4	2	1

ROM Code Converters

MM4220AP/MM5220AP

BCDIC-to-ASCII code converter

general description

The MM4220AP/MM5220AP is used for the conversion of the Binary Coded Decimal Interchange Code(BCDIC) to the American Standard Code for Information Interchange (ASCII).

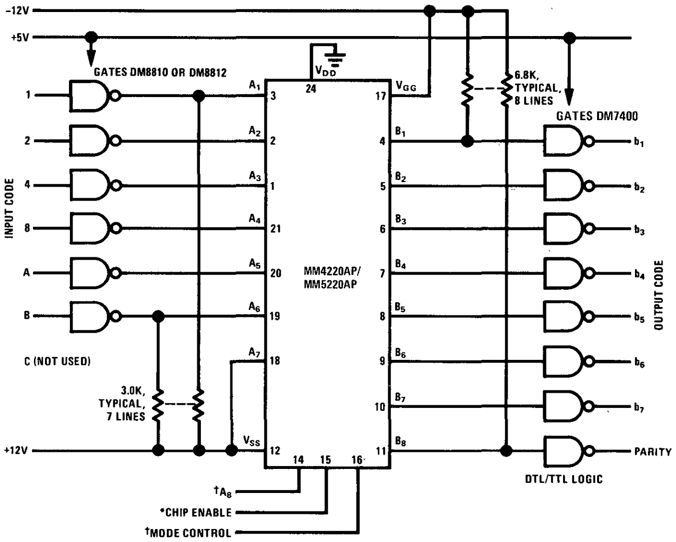
The input is a seven-bit BCDIC code with the exception of the parity (check) bit (pin 18) which is returned to +12V dc. The alternate set of input symbols is also shown in the Conversion Table for reference.

The output is a seven-bit ASCII code, with an eighth bit generated for even parity.

device characteristics

For full electrical, environmental, and mechanical details, refer to the MM4220/MM5220 1024-bit read only memory data sheet.

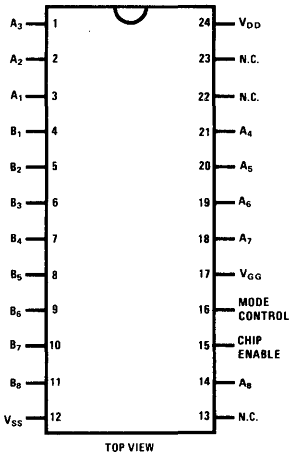
typical application



Logic Levels
DTL/TTL (except at MOS/ROM interface)
Logic "1", +5V, nom. Logic "0", ground, nom.
MOS/ROM Inputs & Output
Logic "1", more negative. Logic "0", more positive

†Mode Control = Logic "0"
A_8 = Logic "1"
*Chip Enable = Logic "1" to obtain outputs

connection diagram



code conversion table

	FUNCTION		CODE														
	INPUT	OUTPUT	INPUT							OUTPUT							
				BCDIC							ASCII						
ROM ADDRESS	BCDIC SYMBOL	ASCII SYMBOL	CODE	B	A	8	4	2	1	EP	b_7	b_6	b_5	b_4	b_3	b_2	b_1
0	Space	Space	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0
1	1	1	0	0	0	0	0	0	1	1	0	1	1	0	0	0	1
2	2	2	0	0	0	0	0	1	0	1	0	1	1	0	0	1	0
3	3	3	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1
4	4	4	0	0	0	0	1	0	0	1	0	1	1	0	1	0	0
5	5	5	0	0	0	0	1	0	1	0	0	1	1	0	1	0	1
6	6	6	0	0	0	0	1	1	0	0	0	1	1	0	1	1	0
7	7	7	0	0	0	0	1	1	1	1	0	1	1	0	1	1	1
8	8	8	0	0	0	1	0	0	0	1	0	1	1	1	0	0	0
9	9	9	0	0	0	1	0	0	1	0	0	1	1	1	0	0	1
10	0	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	0
11	# or =	#	0	0	0	1	0	1	1	1	0	1	0	0	0	1	1
12	@ or '	@	0	0	0	1	1	0	0	1	1	0	0	0	0	0	0
13	:	:	0	0	0	1	1	0	1	0	0	1	1	1	0	1	0
14	>	>	0	0	0	1	1	1	0	1	0	1	1	1	1	1	0
15	√	?	0	0	0	1	1	1	1	0	0	1	1	1	1	1	1
16	Blank	[	0	0	1	0	0	0	0	1	1	0	1	1	0	1	1
17	/	/	0	0	1	0	0	0	1	1	0	1	0	1	1	1	1
18	S	S	0	0	1	0	0	1	0	0	1	0	1	0	0	1	1
19	T	T	0	0	1	0	0	1	1	1	1	0	1	0	1	0	0
20	U	U	0	0	1	0	1	0	0	0	1	0	1	0	1	0	1
21	V	V	0	0	1	0	1	0	1	0	1	0	1	0	1	1	0
22	W	W	0	0	1	0	1	1	0	1	1	0	1	0	1	1	1
23	X	X	0	0	1	0	1	1	1	1	1	0	1	1	0	0	0
24	Y	Y	0	0	1	1	0	0	0	0	1	0	1	1	0	0	1
25	Z	Z	0	0	1	1	0	0	1	0	1	0	1	1	0	1	0
26	‡	LF	0	0	1	1	0	1	0	0	0	0	0	1	0	1	0
27	,	,	0	0	1	1	0	1	1	1	0	1	0	1	1	0	0
28	% or (	%	0	0	1	1	1	0	0	1	0	1	0	0	1	0	1
29	v	HT	0	0	1	1	1	0	1	0	0	0	0	1	0	0	1
30	\	'	0	0	1	1	1	1	0	0	0	1	0	0	1	1	1
31	⧻	"	0	0	1	1	1	1	1	0	0	1	0	0	0	1	0
32	–	–	0	1	0	0	0	0	0	0	0	1	0	1	1	0	1
33	J	J	0	1	0	0	0	0	1	1	1	0	0	1	0	1	0
34	K	K	0	1	0	0	0	1	0	0	1	0	0	1	0	1	1
35	L	L	0	1	0	0	0	1	1	1	1	0	0	1	1	0	0
36	M	M	0	1	0	0	1	0	0	0	1	0	0	1	1	0	1
37	N	N	0	1	0	0	1	0	1	0	1	0	0	1	1	1	0
38	O	O	0	1	0	0	1	1	0	1	1	0	0	1	1	1	1
39	P	P	0	1	0	0	1	1	1	0	1	0	1	0	0	0	0
40	Q	Q	0	1	0	1	0	0	0	1	1	0	1	0	0	0	1
41	R	R	0	1	0	1	0	0	1	1	1	0	1	0	0	1	0
42	!	!	0	1	0	1	0	1	0	0	0	1	0	0	0	0	1
43	$	$	0	1	0	1	0	1	1	0	0	1	0	0	1	0	0
44	*	*	0	1	0	1	1	0	0	1	0	1	0	1	0	1	0
45	]	)	0	1	0	1	1	0	1	1	0	1	0	1	0	0	1
46	;	;	0	1	0	1	1	1	0	1	0	1	1	1	0	1	1
47	Δ	]	0	1	0	1	1	1	1	1	1	0	1	1	1	0	1
48	& or +	&	0	1	1	0	0	0	0	1	0	1	0	0	1	1	0
49	A	A	0	1	1	0	0	0	1	0	1	0	0	0	0	0	1
50	B	B	0	1	1	0	0	1	0	0	1	0	0	0	0	1	0
51	C	C	0	1	1	0	0	1	1	1	1	0	0	0	0	1	1
52	D	D	0	1	1	0	1	0	0	0	1	0	0	0	1	0	0
53	E	E	0	1	1	0	1	0	1	1	1	0	0	0	1	0	1
54	F	F	0	1	1	0	1	1	0	1	1	0	0	0	1	1	0
55	G	G	0	1	1	0	1	1	1	0	1	0	0	0	1	1	1
56	H	H	0	1	1	1	0	0	0	0	1	0	0	1	0	0	0
57	I	I	0	1	1	1	0	0	1	1	1	0	0	1	0	0	1
58	?	+	0	1	1	1	0	1	0	0	0	1	0	1	0	1	1
59	.	.	0	1	1	1	0	1	1	0	0	1	0	1	1	1	0
60	¤ or)	⌒	0	1	1	1	1	0	0	1	1	0	1	1	1	1	0
61	[	(	0	1	1	1	1	0	1	0	0	1	0	1	0	0	0
62	<	<	0	1	1	1	1	1	0	0	0	1	1	1	1	0	0
63	‡	CR	0	1	1	1	1	1	1	1	0	0	0	1	1	0	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

ROM Code Converters

MM4220BL/MM5220BL baudot-to-ASCII code converter

general description

The MM4220BL/MM5220BL is used for conversion of the Communications Set Baudot code to the American Standard Code for Information Interchange (ASCII).

The Baudot and ASCII codes have different formats. ASCII has a unique code combination for each alphabetic, numerical, or control character. The correct interpretation of a five bit Baudot is dependent upon knowing its previous history; whether upper or lower case was *last* selected. In effect a sixth-bit, which can be called the Case Bit, is required to uniquely identify the Baudot input. The latch circuit shown in the typical application can store this information and will generate the Case Bit. If the bit is externally supplied, the feedback and latch circuits can be deleted (as shown with the X's).

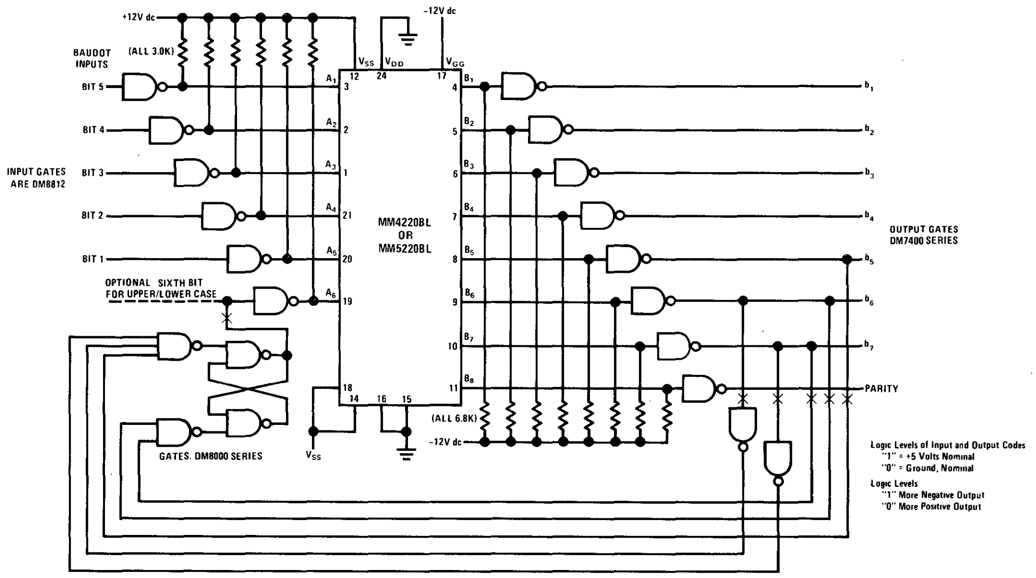
The accompanying table is applicable for the code conversion scheme as shown (or its alternate) rather than for the device itself. The input and output codes are defined at the TTL gates with the logic trues high (Logic "1" = +5 volts, nominal; Logic "0" = Ground, nominal).

device characteristics

For full electrical, environmental, and mechanical details, refer to the MM4220/MM5220 1024-bit read only memory data sheet.

typical application

Baudot to ASCII



Logic Levels of Input and Output Codes
"1" = +5 Volts Nominal
"0" = Ground, Nominal

Logic Levels
"1" More Negative Output
"0" More Positive Output

code conversion tables

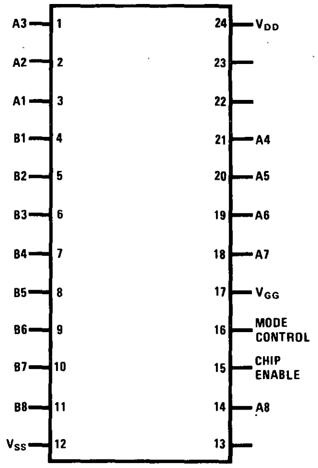
	FUNCTION		CODE													
	INPUT	OUTPUT	INPUT						OUTPUT							
				BAUDOT					ASCII							
ROM ADDRESS	BAUDOT SYMBOL	ASCII SYMBOL	CASE	1	2	3	4	5	EP	b_7	b_6	b_5	b_4	b_3	b_2	b_1
0	Blank	NULL	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	T	T	0	0	0	0	0	1	1	1	0	1	0	1	0	0
2	CR	CR	0	0	0	0	1	0	1	0	0	0	1	1	0	1
3	O	O	0	0	0	0	1	1	1	1	0	0	1	1	1	1
4	Space	Space	0	0	0	1	0	0	1	0	1	0	0	0	0	0
5	H	H	0	0	0	1	0	1	0	1	0	0	1	0	0	0
6	N	N	0	0	0	1	1	0	0	1	0	0	1	1	1	0
7	M	M	0	0	0	1	1	1	0	1	0	0	1	1	0	1
8	LF	LF	0	0	1	0	0	0	0	0	0	0	1	0	1	0
9	L	L	0	0	1	0	0	1	1	1	0	0	1	1	0	0
10	R	R	0	0	1	0	1	0	1	1	0	1	0	0	1	0
11	G	G	0	0	1	0	1	1	0	1	0	0	0	1	1	1
12	I	I	0	0	1	1	0	0	1	1	0	0	1	0	0	1
13	P	P	0	0	1	1	0	1	0	1	0	1	0	0	0	0
14	C	C	0	0	1	1	1	0	1	1	0	0	0	0	1	1
15	V	V	0	0	1	1	1	1	0	1	0	1	0	1	1	0
16	E	E	0	1	0	0	0	0	1	1	0	0	0	1	0	1
17	Z	Z	0	1	0	0	0	1	0	1	0	1	1	0	1	0
18	D	D	0	1	0	0	1	0	0	1	0	0	0	1	0	0
19	B	B	0	1	0	0	1	1	0	1	0	0	0	0	1	0
20	S	S	0	1	0	1	0	0	0	1	0	1	0	0	1	1
21	Y	Y	0	1	0	1	0	1	0	1	0	1	1	0	0	1
22	F	F	0	1	0	1	1	0	1	1	0	0	0	1	1	0
23	X	X	0	1	0	1	1	1	1	1	0	1	1	0	0	0
24	A	A	0	1	1	0	0	0	0	1	0	0	0	0	0	1
25	W	W	0	1	1	0	0	1	1	1	0	1	0	1	1	1
26	J	J	0	1	1	0	1	0	1	1	0	0	1	0	1	0
27	Upper	IS1/Can	0	1	1	0	1	1	0	0	0	1	1	0	0	0
28	U	U	0	1	1	1	0	0	0	1	0	1	0	1	0	1
29	Q	Q	0	1	1	1	0	1	1	1	0	1	0	0	0	1
30	K	K	0	1	1	1	1	0	0	1	0	0	1	0	1	1
31	Lower	Delete	0	1	1	1	1	1	1	1	1	1	1	1	1	1
32	Blank	NULL	1	0	0	0	0	0	0	0	0	0	0	0	0	0
33	5	5	1	0	0	0	0	1	0	0	1	1	0	1	0	1
34	CR	CR	1	0	0	0	1	0	1	0	0	0	1	1	0	1
35	9	9	1	0	0	0	1	1	0	0	1	1	1	0	0	1
36	Space	Space	1	0	0	1	0	0	1	0	1	0	0	0	0	0
37	#/£ S/S	BS/FE	1	0	0	1	0	1	1	0	0	0	1	0	0	0
38	.	,	1	0	0	1	1	0	1	0	1	0	1	1	0	0
39	.	.	1	0	0	1	1	1	0	0	1	0	1	1	1	0
40	LF	LF	1	0	1	0	0	0	0	0	0	0	1	0	1	0
41	)	)	1	0	1	0	0	1	1	0	1	0	1	0	0	1
42	4	4	1	0	1	0	1	0	1	0	1	1	0	1	0	0
43	&	&	1	0	1	0	1	1	1	0	1	0	0	1	1	0
44	8	8	1	0	1	1	0	0	1	0	1	1	1	0	0	0
45	0	0	1	0	1	1	0	1	0	0	1	1	0	0	0	0
46	:	:	1	0	1	1	1	0	0	0	1	1	1	0	1	0
47	,	,	1	0	1	1	1	1	1	0	1	1	1	0	1	1
48	3	3	1	1	0	0	0	0	0	0	1	1	0	0	1	1
49	"	"	1	1	0	0	0	1	0	0	1	0	0	0	1	0
50	$	$	1	1	0	0	1	0	0	0	1	0	0	1	0	0
51	?	?	1	1	0	0	1	1	0	0	1	1	1	1	1	1
52	Bell	Bell	1	1	0	1	0	0	1	0	0	0	0	1	1	1
53	6	6	1	1	0	1	0	1	0	0	1	1	0	1	1	0
54	!	!	1	1	0	1	1	0	0	0	1	0	0	0	0	1
55	/	/	1	1	0	1	1	1	1	0	1	0	1	1	1	1
56	–	-	1	1	1	0	0	0	0	0	1	0	1	1	0	1
57	2	2	1	1	1	0	0	1	1	0	1	1	0	0	1	0
58	'	'	1	1	1	0	1	0	0	0	1	0	0	1	1	1
59	Upper	Can	1	1	1	0	1	1	0	0	0	1	1	0	0	0
60	7	7	1	1	1	1	0	0	1	0	1	1	0	1	1	1
61	1	1	1	1	1	1	0	1	1	0	1	1	0	0	0	1
62	(	(	1	1	1	1	1	0	0	0	1	0	1	0	0	0
63	Lower	Delete	1	1	1	1	1	1	1	1	1	1	1	1	1	1

LEGEND

EP = Even Parity
LF = Line Feed
CR = Carriage Return
Can = Cancel

IS1 = Information Separator #1
S/S = Stop/Start
BS = Back Space

connection diagram



TOP VIEW

ROM Code Converters

MM4220BM/MM5220BM sine look-up table

general description

The MM4220BM/MM5220BM is a 1024-monolithic MOS read only memory that has been programmed to solve for the sine value x of a known angle θ; i.e., to obtain the solution of the equation $x = \sin \theta$.

Values of θ are defined in the look up table for $0^\circ \leq \theta < 90^\circ$ (quadrant I) which has corresponding solutions of $0 \leq x < 1$. For values of $90^\circ < \theta \leq 180^\circ$ (quadrant II), enter the complement $(180^\circ - \theta)$ to obtain the correct solution. Solutions for quadrants III and IV differ in sign with I and II. This is summarized in Table 1.

This input is divided into 128 parts for θ in each quadrant. Thus, the appropriate input address is $(\theta^1/90^\circ)(128)$ to the nearest whole integer. The actual input code to the ROM is the input address expressed in binary, with A_1 being the most significant bit.

The output is the value of X expressed in binary. The output lines $B_1, B_2, \ldots\ldots B_8$ are binary place values 1/2, 1/4, ... 1/256. The sign for negative values of X is externally generated.

The 8 bit output code has been rounded off from a larger word code, i.e., where A_9 was a binary "1" it carried into the LSB of the eight bit code, where A_9 was a binary "0" it was simply dropped.

EXAMPLE

Find the sine of 45°.

The input address is (45/90) 128 = 64 or 1000000, as expressed in binary. The converter generates the output .10110101 whose decimal equivalent is 0.707131. Thus, $\sin 45^\circ = 0.707$.

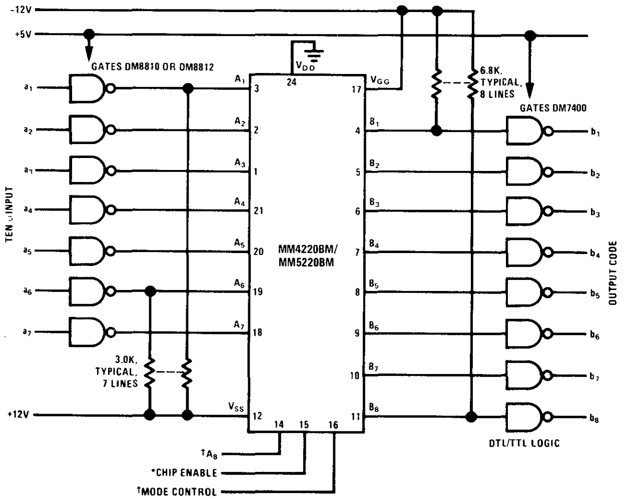
Find the sine of 210°.

This value is in quadrant III; therefore $\theta^1 = 210^\circ - 180^\circ = 30^\circ$. The input address is then (30/90) $128 \cong 43$ to the nearest whole integer. The binary input to the ROM is then 0101011. The output value is .10000001 or 0.503906. Thus, $\sin 210^\circ = -0.504$, with the sign generated by the external logic. The solution is within 1%; note that address 43 is actually equal to 30.23°.

device characteristics

For full electrical, environmental and mechanical details refer to the MM4220/MM5220 1024-bit read only memory data sheet.

typical application



Logic Levels
DTL/TTL (except at MOS/ROM interface)
Logic "1", +5V, nom. Logic "0", ground, nom.
MOS/ROM Inputs & Output
Logic "1", more negative. Logic "0", more positive

†Mode Control = Logic "0"
A_8 = Logic "1"
*Chip Enable = Logic "1" to obtain outputs

pattern selection form

ADDRESS REFERENCE	FUNCTION INPUT DEGREES	FUNCTION INPUT RADIANS	CODE OUTPUT B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
0	.00	.000	0	0	0	0	0	0	0	0
1	.70	.012	1	1	0	0	0	0	0	0
2	1.41	.025	0	1	1	0	0	0	0	0
3	2.11	.037	1	0	0	1	0	0	0	0
4	2.81	.049	0	0	1	1	0	0	0	0
5	3.52	.061	1	1	1	1	0	0	0	0
6	4.22	.074	1	1	0	0	1	0	0	0
7	4.92	.086	0	1	1	0	1	0	0	0
8	5.63	.098	1	0	0	1	1	0	0	0
9	6.33	.110	0	0	1	1	1	0	0	0
10	7.03	.123	1	1	1	1	1	0	0	0
11	7.73	.135	0	1	0	0	0	1	0	0
12	8.44	.147	1	0	1	0	0	1	0	0
13	9.14	.160	0	0	0	1	0	1	0	0
14	9.84	.172	0	0	1	1	0	1	0	0
15	10.55	.184	1	1	1	1	0	1	0	0
16	11.25	.196	0	1	0	0	1	1	0	0
17	11.95	.209	1	0	1	0	1	1	0	0
18	12.66	.221	0	0	0	1	1	1	0	0
19	13.36	.233	1	1	0	1	1	1	0	0
20	14.06	.245	0	1	1	1	1	1	0	0
21	14.77	.258	1	0	0	0	0	0	1	0
22	15.47	.270	0	0	1	0	0	0	1	0
23	16.17	.282	1	1	1	0	0	0	1	0
24	16.88	.295	0	1	0	1	0	0	1	0
25	17.58	.307	1	0	1	1	0	0	1	0
26	18.28	.319	0	0	0	0	1	0	1	0
27	18.98	.331	1	1	0	0	1	0	1	0
28	19.69	.344	0	1	1	0	1	0	1	0
29	20.39	.356	1	0	0	1	1	0	1	0
30	21.09	.368	0	0	1	1	1	0	1	0
31	21.80	.380	1	1	1	1	1	0	1	0
32	22.50	.393	0	1	0	0	0	1	1	0
33	23.20	.405	1	1	1	0	0	1	1	0
34	23.91	.417	1	1	1	0	0	1	1	0
35	24.61	.430	0	1	0	1	0	1	1	0
36	25.31	.442	1	0	1	1	0	1	1	0
37	26.02	.454	0	0	0	0	1	1	1	0
38	26.72	.466	1	1	0	0	1	1	1	0
39	27.42	.479	0	1	1	0	1	1	1	0
40	28.13	.491	0	0	0	1	1	1	1	0
41	28.83	.503	1	1	0	1	1	1	1	0
42	29.53	.515	0	1	1	1	1	1	1	0
43	30.23	.528	0	0	0	0	0	0	0	1
44	30.94	.540	1	1	0	0	0	0	0	1
45	31.64	.552	0	1	1	0	0	0	0	1
46	32.34	.565	1	0	0	1	0	0	0	1
47	33.05	.577	1	1	0	1	0	0	0	1
48	33.75	.589	0	1	1	1	0	0	0	1
49	34.45	.601	1	0	0	0	1	0	0	1
50	35.16	.614	1	1	0	0	1	0	0	1
51	35.86	.626	0	1	1	0	1	0	0	1
52	36.56	.638	0	0	0	1	1	0	0	1
53	37.27	.650	1	1	0	1	1	0	0	1
54	37.97	.663	1	0	1	1	1	0	0	1
55	38.67	.675	0	0	0	0	0	1	0	1
56	39.37	.687	0	1	0	0	0	1	0	1
57	40.08	.699	1	0	1	0	0	1	0	1
58	40.78	.712	1	1	1	0	0	1	0	1
59	41.48	.724	1	0	0	1	0	1	0	1
60	42.19	.736	0	0	1	1	0	1	0	1
61	42.89	.749	0	1	1	1	0	1	0	1
62	43.59	.761	0	0	0	0	1	1	0	1
63	44.30	.773	1	1	0	0	1	1	0	1

ADDRESS REFERENCE	FUNCTION INPUT DEGREES	FUNCTION INPUT RADIANS	CODE OUTPUT B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
64	45.00	.785	1	0	1	0	1	1	0	1
65	45.70	.798	1	1	1	0	1	1	0	1
66	46.41	.810	1	0	0	1	1	1	0	1
67	47.11	.822	1	1	0	1	1	1	0	1
68	47.81	.834	1	0	1	1	1	1	0	1
69	48.52	.847	0	0	0	0	0	0	1	1
70	49.22	.859	0	1	0	0	0	0	1	1
71	49.92	.871	0	0	1	0	0	0	1	1
72	50.62	.884	0	1	1	0	0	0	1	1
73	51.33	.896	0	0	0	1	0	0	1	1
74	52.03	.908	0	1	0	1	0	0	1	1
75	52.73	.920	1	1	0	1	0	0	1	1
76	53.44	.933	1	0	1	1	0	0	1	1
77	54.14	.945	1	1	1	1	0	0	1	1
78	54.84	.957	1	0	0	0	1	0	1	1
79	55.55	.969	1	1	0	0	1	0	1	1
80	56.25	.982	1	0	1	0	1	0	1	1
81	56.95	.994	0	1	1	0	1	0	1	1
82	57.66	1.006	0	0	0	1	1	0	1	1
83	58.36	1.019	0	1	0	1	1	0	1	1
84	59.06	1.031	1	1	0	1	1	0	1	1
85	59.77	1.043	1	0	1	1	1	0	1	1
86	60.47	1.055	0	1	1	1	1	0	1	1
87	61.17	1.068	0	0	0	0	0	1	1	1
88	61.87	1.080	0	1	0	0	0	1	1	1
89	62.58	1.092	1	1	0	0	0	1	1	1
90	63.28	1.104	0	0	1	0	0	1	1	1
91	63.98	1.117	0	1	1	0	0	1	1	1
92	64.69	1.129	1	1	1	0	0	1	1	1
93	65.39	1.141	0	0	0	1	0	1	1	1
94	66.09	1.154	0	1	0	1	0	1	1	1
95	66.80	1.166	1	1	0	1	0	1	1	1
96	67.50	1.178	0	0	1	1	0	1	1	1
97	68.20	1.190	1	0	1	1	0	1	1	1
98	68.91	1.203	1	1	1	1	0	1	1	1
99	69.61	1.215	0	0	0	0	1	1	1	1
100	70.31	1.227	1	0	0	0	1	1	1	1
101	71.02	1.239	0	1	0	0	1	1	1	1
102	71.72	1.252	1	1	0	0	1	1	1	1
103	72.42	1.264	0	0	1	0	1	1	1	1
104	73.12	1.276	1	0	1	0	1	1	1	1
105	73.83	1.289	0	1	1	0	1	1	1	1
106	74.53	1.301	0	1	1	0	1	1	1	1
107	75.23	1.313	1	1	1	0	1	1	1	1
108	75.94	1.325	0	0	0	1	1	1	1	1
109	76.64	1.338	1	0	0	1	1	1	1	1
110	77.34	1.350	0	1	0	1	1	1	1	1
111	78.05	1.362	0	1	0	1	1	1	1	1
112	78.75	1.374	1	1	0	1	1	1	1	1
113	79.45	1.387	1	1	0	1	1	1	1	1
114	80.16	1.399	0	0	1	1	1	1	1	1
115	80.86	1.411	0	0	1	1	1	1	1	1
116	81.56	1.424	1	0	1	1	1	1	1	1
117	82.27	1.436	1	0	1	1	1	1	1	1
118	82.97	1.448	0	1	1	1	1	1	1	1
119	83.67	1.460	0	1	1	1	1	1	1	1
120	84.38	1.473	1	1	1	1	1	1	1	1
121	85.08	1.485	1	1	1	1	1	1	1	1
122	85.78	1.497	1	1	1	1	1	1	1	1
123	86.48	1.509	1	1	1	1	1	1	1	1
124	87.19	1.522	1	1	1	1	1	1	1	1
125	87.89	1.534	1	1	1	1	1	1	1	1
126	88.59	1.546	1	1	1	1	1	1	1	1
127	89.30	1.559	1	1	1	1	1	1	1	1

connection diagram

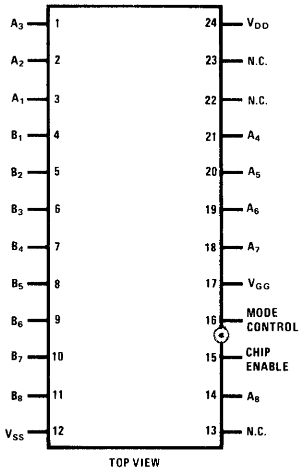
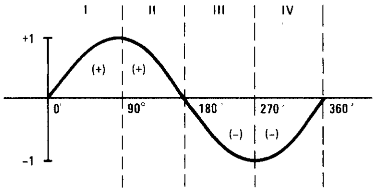


Table 1. SINE

	INPUT		OUTPUT	
Quadrant	Range	Entry to ROM (θ^1)	Binary Value	Sign
I	$\geq 0^\circ < 90^\circ$	Direct	Direct Reading	+
II	$> 90^\circ \leq 180^\circ$	$180^\circ - X$	Direct Reading	+
III	$\geq 180^\circ < 270^\circ$	$X - 180^\circ$	Direct Reading	–
IV	$> 270^\circ \leq 360^\circ$	$360^\circ - X$	Direct Reading	–



ROM Code Converters

MM4220BN/MM5220BN arctangent look-up table

general description

The MM4220BN/MM5220BN is a 1024-bit monolithic MOS read only memory that has been programmed to solve for the angle θ whose tangent value x is known; i.e., to obtain the solution to the equation: θ = arctan x.

Values of x are defined in the Look Up table for $0 \leq x < 1$ with angles corresponding from $0^\circ \leq \theta < 45^\circ$. For values $x \geq 1$, the reciprocal of x (i.e., 1/x) must be entered and the output angle must be complemented to obtain the actual value.

The input is divided into 128 equal parts for x. Thus, the appropriate input address is (128)(x) to the nearest whole integer for obtaining the appropriate ROM address. The input code is the ROM address expressed in binary with A_1 being the least significant bit. For input values greater than unity, the decimal reciprocal is to be taken prior to entry of the binary address.

The output has been normalized for 45°. To obtain the true angular reading, the output should be multiplied by 45°, i.e.: $\theta = (\theta_{output}) \times 45^\circ$ where θ_{output} is the decimal equivalent of the output. The output code is the normalized value of the angle θ expressed in binary. The output lines B_1, B_2, ... B_8 are binary place values 1/2, 1/4, ... 1/256. To obtain angles between 45° and 89.6° which occur when input values of x are equal to or greater than unity, either complement the output binary code and add a 1, or complement the resultant angular value (i.e., subtract from 90°).

The 8-bit output code has been rounded off. That is, if another bit of even lower significance had been computed for the given arctangent value was a binary "1", it would have carried over into the LSB of the eight bit code. If it was a binary "0", it would have been dropped.

EXAMPLE

Find the angle whose tangent is 0.258.

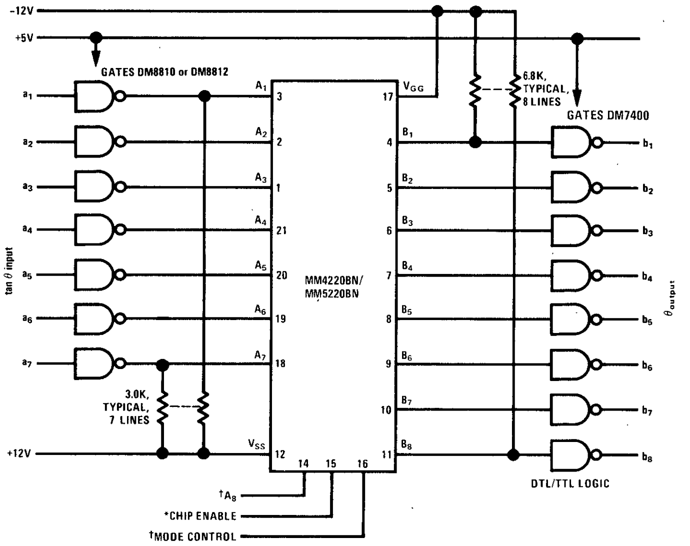
The input address is 128 x 0.258, or 33 to the nearest integer. Expressed in binary, this is 0100001, and is the actual input code to the converter. The converter will generate the binary value .01010010, whose decimal equivalent is 0.3203125.

Thus, $\theta = 0.320 \times 45^\circ = 14.4^\circ$

device characteristics

For full electrical, environmental and mechanical details refer to the MM4220/MM5220 1024-bit read only memory data sheet.

typical application



Logic Levels
DTL/TTL (except at MOS/ROM interface)
Logic "1", +5V, nom. Logic "0", ground, nom.
MOS/ROM Inputs & Output
Logic "1", more negative. Logic "0", more positive

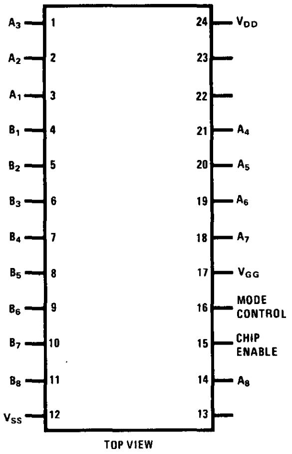
†Mode Control = Logic "0"
A_8 = Logic "1"
*Chip Enable = Logic "1" to obtain outputs

pattern selection form

ADDRESS 128 (x)	OUTPUT CODE (θ_{OUTPUT}) B8	B7	B6	B5	B4	B3	B2	B1
0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0
2	1	0	1	0	0	0	0	0
3	1	1	1	0	0	0	0	0
4	0	1	0	1	0	0	0	0
5	0	0	1	1	0	0	0	0
6	1	1	1	1	0	0	0	0
7	0	1	0	0	1	0	0	0
8	0	0	1	0	1	0	0	0
9	1	1	1	0	1	0	0	0
10	1	0	0	1	1	0	0	0
11	0	0	1	1	1	0	0	0
12	0	1	1	1	1	0	0	0
13	1	0	0	0	0	1	0	0
14	1	1	0	0	0	1	0	0
15	0	1	1	0	0	1	0	0
16	0	0	0	1	0	1	0	0
17	1	1	0	1	0	1	0	0
18	1	0	1	1	0	1	0	0
19	0	0	0	0	1	1	0	0
20	0	1	0	0	1	1	0	0
21	1	0	1	0	1	1	0	0
22	1	1	1	0	1	1	0	0
23	0	1	0	1	1	1	0	0
24	0	0	1	1	1	1	0	0
25	1	1	1	1	1	1	0	0
26	1	0	0	0	0	0	1	0
27	0	0	1	0	0	0	1	0
28	0	1	1	0	0	0	1	0
29	0	0	0	1	0	0	1	0
30	1	1	0	1	0	0	1	0
31	1	0	1	1	0	0	1	0
32	0	0	0	0	1	0	1	0
33	0	1	0	0	1	0	1	0
34	0	0	1	0	1	0	1	0
35	1	1	1	0	1	0	1	0
36	1	0	0	1	1	0	1	0
37	1	1	0	1	1	0	1	0
38	0	1	1	1	1	0	1	0
39	0	0	0	0	0	1	1	0
40	0	1	0	0	0	1	1	0
41	1	0	1	0	0	1	1	0
42	1	1	1	0	0	1	1	0
43	1	0	0	1	0	1	1	0
44	0	0	1	1	0	1	1	0
45	0	1	1	1	0	1	1	0
46	0	0	0	0	1	1	1	0
47	0	1	0	0	1	1	1	0
48	1	0	1	0	1	1	1	0
49	1	1	1	0	1	1	1	0
50	1	0	0	1	1	1	1	0
51	1	1	0	1	1	1	1	0
52	0	1	1	1	1	1	1	0
53	0	0	0	0	0	0	0	1
54	0	1	0	0	0	0	0	1
55	0	0	1	0	0	0	0	1
56	0	1	1	0	0	0	0	1
57	0	0	0	1	0	0	0	1
58	0	1	0	1	0	0	0	1
59	1	0	1	1	0	0	0	1
60	1	1	1	1	0	0	0	1
61	1	0	0	0	1	0	0	1
62	1	1	0	0	1	0	0	1
63	1	0	1	0	1	0	0	1
64	1	1	1	0	1	0	0	1
65	1	0	0	1	1	0	0	1
66	1	1	0	1	1	0	0	1
67	1	0	1	1	1	0	0	1
68	1	1	1	1	1	0	0	1
69	1	0	0	0	0	1	0	1
70	1	1	0	0	0	1	0	1
71	1	0	1	0	0	1	0	1
72	1	1	1	0	0	1	0	1
73	1	0	0	1	0	1	0	1
74	1	1	0	1	0	1	0	1
75	1	0	1	1	0	1	0	1
76	0	1	1	1	0	1	0	1
77	0	0	0	0	1	1	0	1
78	0	1	0	0	1	1	0	1
79	0	0	1	0	1	1	0	1
80	0	1	1	0	1	1	0	1
81	0	0	0	1	1	1	0	1
82	1	0	0	1	1	1	0	1
83	1	1	0	1	1	1	0	1
84	1	0	1	1	1	1	0	1
85	1	1	1	1	1	1	0	1
86	1	0	0	0	0	0	1	1
87	0	1	0	0	0	0	1	1
88	0	0	1	0	0	0	1	1
89	0	1	1	0	0	0	1	1
90	1	1	1	0	0	0	1	1
91	1	0	0	1	0	0	1	1
92	1	1	0	1	0	0	1	1
93	1	0	1	1	0	0	1	1
94	0	1	1	1	0	0	1	1
95	0	0	0	0	1	0	1	1
96	1	0	0	0	1	0	1	1
97	1	1	0	0	1	0	1	1
98	1	0	1	0	1	0	1	1
99	0	1	1	0	1	0	1	1
100	0	0	0	1	1	0	1	1
101	1	0	0	1	1	0	1	1
102	1	1	0	1	1	0	1	1
103	1	0	1	1	1	0	1	1
104	0	1	1	1	1	0	1	1
105	0	0	0	0	0	1	1	1
106	1	0	0	0	0	1	1	1
107	1	1	0	0	0	1	1	1
108	0	0	1	0	0	1	1	1
109	0	1	1	0	0	1	1	1
110	1	1	1	0	0	1	1	1
111	1	0	0	1	0	1	1	1
112	0	1	0	1	0	1	1	1
113	1	1	0	1	0	1	1	1
114	1	0	1	1	0	1	1	1
115	0	1	1	1	0	1	1	1
116	0	0	0	0	1	1	1	1
117	1	0	0	0	1	1	1	1
118	1	1	0	0	1	1	1	1
119	0	0	1	0	1	1	1	1
120	1	0	1	0	1	1	1	1
121	1	1	1	0	1	1	1	1
122	0	0	0	1	1	1	1	1
123	1	0	0	1	1	1	1	1
124	1	1	0	1	1	1	1	1
125	0	0	1	1	1	1	1	1
126	1	0	1	1	1	1	1	1
127	0	1	1	1	1	1	1	1

NOTE: 1 MORE NEGATIVE OUTPUT
0 MORE POSITIVE OUTPUT

connection diagram



TOP VIEW

ROM Code Converters

MM4220DF/MM5220DF

''quick brown fox'' generator

general description

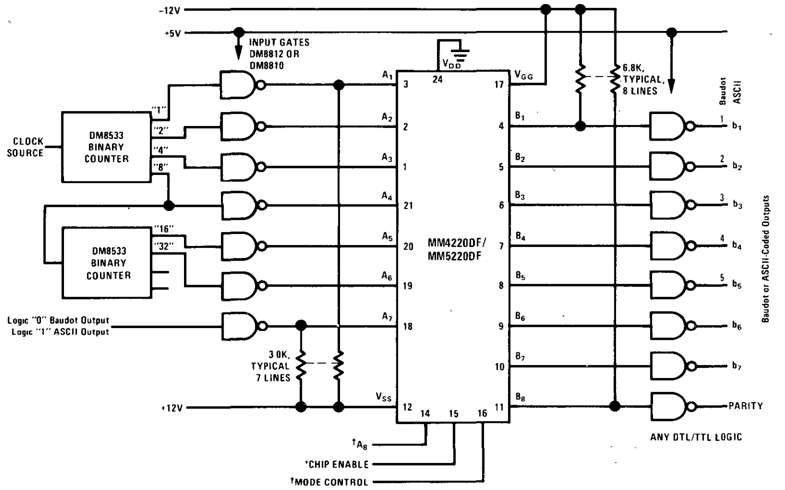
The MM4220DF/MM5220DF is designed for exercising and rapid testing of ASCII and Baudot-coded keyboards, typing mechanisms, and data communications links by generating the internationally accepted ''Quick Brown Fox'' message.

The input is a 7-bit binary sequential count. The output of a 6 stage up-counter can be used; a seventh bit selects the desired code. The message is generated in the 5-bit Baudot Communications Set code with a binary count input of 0 to 63. The message is generated in the 7-bit American Standard Code for Information Interchange (ASCII) along with an even parity bit for a binary count input of 64 to 127.

device characteristics

The message generator is fully contained on a monolithic MOS integrated circuit chip utilizing low threshold voltage technology for increased DTL/TTL compatibility. For complete electrical, environmental, and mechanical details, refer to the MM4220/MM5220 1024-bit read only memory data sheet.

typical applications

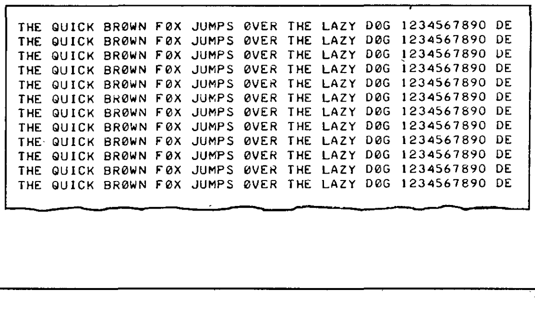


Logic Levels
DTL/TTL (except at MOS/ROM interface)
Logic "1", +5V, nom. Logic "0", ground, nom.
MOS/ROM Inputs & Outputs
Logic "1", more negative Logic "0", more positive

Outputs for circuit shown
Baudot: Logic "0" = "punch"
ASCII: Logic inversion

†Mode Control = Logic "0"
A_8 = Logic "1"
*Chip Enable = Logic "1" to obtain outputs

A typical application showing the ASCII-coded test message as received at a computer terminal.



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THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
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THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
THE QUICK BRØWN FØX JUMPS ØVER THE LAZY DØG 1234567890 DE
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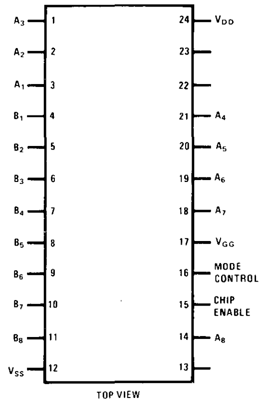
connection diagram



code conversion table

ADDRESS	OUTPUT CHARACTER	OUTPUT CODE								ADDRESS	OUTPUT CHARACTER	OUTPUT CODE							
		Baudot										PARITY	ASCII						
		–	–	–	5	4	3	2	1				b_7	b_6	b_5	b_4	b_3	b_2	b_1
0	CR	1	1	1	1	0	1	1	1	64	NULL	0	0	0	0	0	0	0	0
1	CR	1	1	1	1	0	1	1	1	65	CR	0	1	1	1	0	0	1	0
2	LF	1	1	1	1	1	1	0	1	66	CR	0	1	1	1	0	0	1	0
3	Ltr.	1	1	1	0	0	0	0	0	67	LF	1	1	1	1	0	1	0	1
4	T	1	1	1	0	1	1	1	1	68	T	0	0	1	0	1	0	1	1
5	H	1	1	1	0	1	0	1	1	69	H	1	0	1	1	0	1	1	1
6	E	1	1	1	1	1	1	1	0	70	E	0	0	1	1	1	0	1	0
7	SP	1	1	1	1	1	0	1	1	71	SP	0	1	0	1	1	1	1	1
8	Q	1	1	1	0	1	0	0	0	72	Q	0	0	1	0	1	1	1	0
9	U	1	1	1	1	1	0	0	0	73	U	1	0	1	0	1	0	1	0
10	I	1	1	1	1	1	0	0	1	74	I	0	0	1	1	0	1	1	0
11	C	1	1	1	1	0	0	0	1	75	C	0	0	1	1	1	1	0	0
12	K	1	1	1	1	0	0	0	0	76	K	1	0	1	1	0	1	0	0
13	SP	1	1	1	1	1	0	1	1	77	SP	0	1	0	1	1	1	1	1
14	B	1	1	1	0	0	1	1	0	78	B	1	0	1	1	1	1	0	1
15	R	1	1	1	1	0	1	0	1	79	R	0	0	1	0	1	1	0	1
16	O	1	1	1	0	0	1	1	1	80	O	0	0	1	1	0	0	0	0
17	W	1	1	1	0	1	1	0	0	81	W	0	0	1	0	1	0	0	0
18	N	1	1	1	1	0	0	1	1	82	N	1	0	1	1	0	0	0	1
19	SP	1	1	1	1	1	0	1	1	83	SP	0	1	0	1	1	1	1	1
20	F	1	1	1	1	0	0	1	0	84	F	0	0	1	1	1	0	0	1
21	O	1	1	1	0	0	1	1	1	85	O	0	0	1	1	0	0	0	0
22	X	1	1	1	0	0	0	1	0	86	X	0	0	1	0	0	1	1	1
23	SP	1	1	1	1	1	0	1	1	87	SP	0	1	0	1	1	1	1	1
24	J	1	1	1	1	0	1	0	0	88	J	0	0	1	1	0	1	0	1
25	U	1	1	1	1	1	0	0	0	89	U	1	0	1	0	1	0	1	0
26	M	1	1	1	0	0	0	1	1	90	M	1	0	1	1	0	0	1	0
27	P	1	1	1	0	1	0	0	1	91	P	1	0	1	0	1	1	1	1
28	S	1	1	1	1	1	0	1	0	92	S	1	0	1	0	1	1	0	0
29	SP	1	1	1	1	1	0	1	1	93	SP	0	1	0	1	1	1	1	1
30	O	1	1	1	0	0	1	1	1	94	O	0	0	1	1	0	0	0	0
31	V	1	1	1	0	0	0	0	1	95	V	1	0	1	0	1	0	0	1
32	E	1	1	1	1	1	1	1	0	96	E	0	0	1	1	1	0	1	0
33	R	1	1	1	1	0	1	0	1	97	R	0	0	1	0	1	1	0	1
34	SP	1	1	1	1	1	0	1	1	98	SP	0	1	0	1	1	1	1	1
35	T	1	1	1	0	1	1	1	1	99	T	0	0	1	0	1	0	1	1
36	H	1	1	1	0	1	0	1	1	100	H	1	0	1	1	0	1	1	1
37	E	1	1	1	1	1	1	1	0	101	E	0	0	1	1	1	0	1	0
38	SP	1	1	1	1	1	0	1	1	102	SP	0	1	0	1	1	1	1	1
39	L	1	1	1	0	1	1	0	1	103	L	0	0	1	1	0	0	1	1
40	A	1	1	1	1	1	1	0	0	104	A	1	0	1	1	1	1	1	0
41	Z	1	1	1	0	1	1	1	0	105	Z	1	0	1	0	0	1	0	1
42	Y	1	1	1	0	1	0	1	0	106	Y	1	0	1	0	0	1	1	0
43	SP	1	1	1	1	1	0	1	1	107	SP	0	1	0	1	1	1	1	1
44	D	1	1	1	1	0	1	1	0	108	D	1	0	1	1	1	0	1	1
45	O	1	1	1	0	0	1	1	1	109	O	0	0	1	1	0	0	0	0
46	G	1	1	1	0	0	1	0	1	110	G	1	0	1	1	1	0	0	0
47	SP	1	1	1	1	1	0	1	1	111	SP	0	1	0	1	1	1	1	1
48	Fig	1	1	1	0	0	1	0	0	112	1	0	1	0	0	1	1	1	0
49	1	1	1	1	0	1	0	0	0	113	2	0	1	0	0	1	1	0	1
50	2	1	1	1	0	1	1	0	0	114	3	1	1	0	0	1	1	0	0
51	3	1	1	1	1	1	1	1	0	115	4	0	1	0	0	1	0	1	1
52	4	1	1	1	1	0	1	0	1	116	5	1	1	0	0	1	0	1	0
53	5	1	1	1	0	1	1	1	1	117	6	1	1	0	0	1	0	0	1
54	6	1	1	1	0	1	0	1	0	118	7	0	1	0	0	1	0	0	0
55	7	1	1	1	1	1	0	0	0	119	8	0	1	0	0	0	1	1	1
56	8	1	1	1	1	1	0	0	1	120	9	1	1	0	0	0	1	1	0
57	9	1	1	1	0	0	1	1	1	121	0	1	1	0	0	1	1	1	1
58	0	1	1	1	0	1	0	0	1	122	SP	0	1	0	1	1	1	1	1
59	SP	1	1	1	1	1	0	1	1	123	D	1	0	1	1	1	0	1	1
60	Ltr	1	1	1	0	0	0	0	0	124	E	0	0	1	1	1	0	1	0
61	D	1	1	1	1	0	1	1	0	125	SP	0	1	0	1	1	1	1	1
62	E	1	1	1	1	1	1	1	0	126	DEL	0	0	0	0	0	0	0	0
63	SP	1	1	1	1	1	0	1	1	127	DEL	0	0	0	0	0	0	0	0
		B8	B7	B6	B5	B4	B3	B2	B1			B8	B7	B6	B5	B4	B3	B2	B1
		Baudot: Logic "0" = "punch"										ASCII. Logic inversion							

SP Space

NOTE WHEN CHIP ENABLE INPUT IS AT A LOGICAL 0, ALL OUTPUTS ARE AT A LOGICAL 1

ROM Code Converters

MM4220EK/MM5220EK

BCDIC-to-EBCDIC and ASCII-to-EBCDIC code converters

general description

The MM4220EK/MM5220EK is a 1024-bit read only memory that has been programmed to convert both Binary Coded Decimal Interchange Code (BCDIC) and the American Standard Code for Information Interchange (ASCII) to Extended Binary Coded Decimal Interchange Code (EBCDIC).

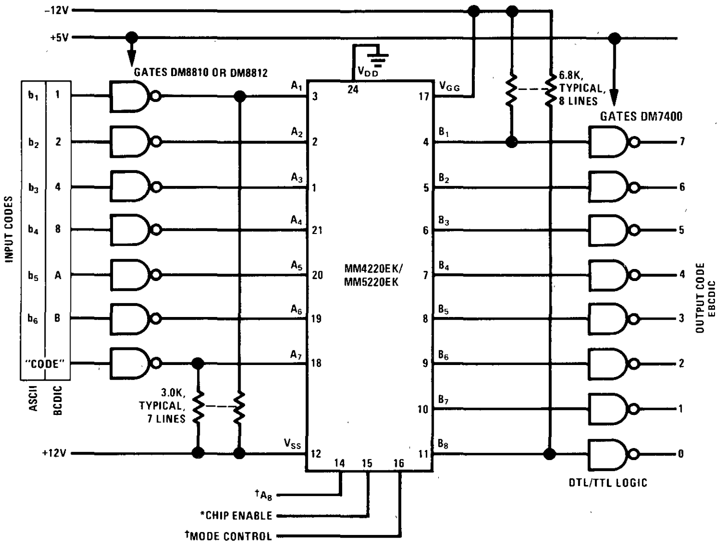
The BCDIC-to-EBCDIC converter is located in the first 64 8-bit bytes of the ROM. The unused parity check bit (the most significant input BCDIC bit) is always a "0".

The ASCII-to-EBCDIC converter is located in the second 64 8-bit bytes of the ROM. Thus, the input ASCII code in addresses 64 through 127 has a "1" in the most significant (A_7) bit which is used with the selection logic. The resulting 6-bit ASCII input is for display—only upper case and numerical codes, since it will not accept the control commands or the lower case characters.

device characteristics

For full electrical, environmental and mechanical details, refer to the MM4220/MM5220 1024-bit read only memory data sheet.

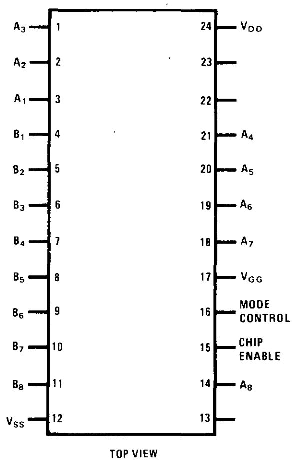
typical application



Logic Levels
DTL/TTL (except at MOS/ROM interface)
Logic "1", +5V, nom. Logic "0", ground, nom.
MOS/ROM Inputs & Output
Logic "1", more negative. Logic "0", more positive

†Mode Control = Logic "0"
A_8 = Logic "1"
*Chip Enable = Logic "1" to obtain outputs

connection diagram



TOP VIEW

code conversion tables

	FUNCTION		CODE														
	INPUT	OUTPUT	INPUT							OUTPUT							
ROM ADDRESS	BCDIC SYMBOL	EBCDIC SYMBOL	CODE	BCDIC B	A	8	4	2	1	EBCDIC 0	1	2	3	4	5	6	7
0	Space	Space	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	1	1	1	1	1	0	0	0	1
2	2	2	0	0	0	0	0	1	0	1	1	1	1	0	0	1	0
3	3	3	0	0	0	0	0	1	1	1	1	1	1	0	0	1	1
4	4	4	0	0	0	0	1	0	0	1	1	1	1	0	1	0	0
5	5	5	0	0	0	0	1	0	1	1	1	1	1	0	1	0	1
6	6	6	0	0	0	0	1	1	0	1	1	1	1	0	1	1	0
7	7	7	0	0	0	0	1	1	1	1	1	1	1	0	1	1	1
8	8	8	0	0	0	1	0	0	0	1	1	1	1	1	0	0	0
9	9	9	0	0	0	1	0	0	1	1	1	1	1	1	0	0	1
10	0	0	0	0	0	1	0	1	0	1	1	1	1	0	0	0	0
11	# or =	#	0	0	0	1	0	1	1	0	1	1	1	1	0	1	1
12	@ or '	@	0	0	0	1	1	0	0	0	1	1	1	1	1	0	0
13	:	:	0	0	0	1	1	0	1	0	1	1	1	1	0	1	0
14	>	>	0	0	0	1	1	1	0	0	1	1	0	1	1	1	0
15	√(TM)	TM	0	0	0	1	1	1	1	0	0	0	1	0	0	1	1
16	Space	Space	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0
17	/	/	0	0	1	0	0	0	1	0	1	1	0	0	0	0	1
18	S	S	0	0	1	0	0	1	0	1	1	1	0	0	0	1	0
19	T	T	0	0	1	0	0	1	1	1	1	1	0	0	0	1	1
20	U	U	0	0	1	0	1	0	0	1	1	1	0	0	1	0	0
21	V	V	0	0	1	0	1	0	1	1	1	1	0	0	1	0	1
22	W	W	0	0	1	0	1	1	0	1	1	1	0	0	1	1	0
23	X	X	0	0	1	0	1	1	1	1	1	1	0	0	1	1	1
24	Y	Y	0	0	1	1	0	0	0	1	1	1	0	1	0	0	0
25	Z	Z	0	0	1	1	0	0	1	1	1	1	0	1	0	0	1
26	‡(RM)	RM	0	0	1	1	0	1	0	1	1	1	0	0	0	0	0
27	,	,	0	0	1	1	0	1	1	0	1	1	0	1	0	1	1
28	% or (	%	0	0	1	1	1	0	0	0	1	1	0	1	1	0	0
29	v	+	0	0	1	1	1	0	1	0	1	0	0	1	1	1	0
30	\	¢	0	0	1	1	1	1	0	0	1	0	0	1	0	1	0
31	⧻	=	0	0	1	1	1	1	1	0	1	1	1	1	1	1	0
32	-	-	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0
33	J	J	0	1	0	0	0	0	1	1	1	0	1	0	0	0	1
34	K	K	0	1	0	0	0	1	0	1	1	0	1	0	0	1	0
35	L	L	0	1	0	0	0	1	1	1	1	0	1	0	0	1	1
36	M	M	0	1	0	0	1	0	0	1	1	0	1	0	1	0	0
37	N	N	0	1	0	0	1	0	1	1	1	0	1	0	1	0	1
38	O	O	0	1	0	0	1	1	0	1	1	0	1	0	1	1	0
39	P	P	0	1	0	0	1	1	1	1	1	0	1	0	1	1	1
40	Q	Q	0	1	0	1	0	0	0	1	1	0	1	1	0	0	0
41	R	R	0	1	0	1	0	0	1	1	1	0	1	1	0	0	1
42	!	!	0	1	0	1	0	1	0	0	1	0	1	1	0	1	0
43	$	$	0	1	0	1	0	1	1	0	1	0	1	1	0	1	1
44	*	*	0	1	0	1	1	0	0	0	1	0	1	1	1	0	0
45	]	)	0	1	0	1	1	0	1	0	1	0	1	1	1	0	1
46	,	,	0	1	0	1	1	1	0	0	1	0	1	1	1	1	0
47	Λ	"	0	1	0	1	1	1	1	0	1	1	1	1	1	1	1
48	& or +	&	0	1	1	0	0	0	0	0	1	0	1	0	0	0	0
49	A	A	0	1	1	0	0	0	1	1	1	0	0	0	0	0	1
50	B	B	0	1	1	0	0	1	0	1	1	0	0	0	0	1	0
51	C	C	0	1	1	0	0	1	1	1	1	0	0	0	0	1	1
52	D	D	0	1	1	0	1	0	0	1	1	0	0	0	1	0	0
53	E	E	0	1	1	0	1	0	1	1	1	0	0	0	1	0	1
54	F	F	0	1	1	0	1	1	0	1	1	0	0	0	1	1	0
55	G	G	0	1	1	0	1	1	1	1	1	0	0	0	1	1	1
56	H	H	0	1	1	1	0	0	0	1	1	0	0	1	0	0	0
57	I	I	0	1	1	1	0	0	1	1	1	0	0	1	0	0	1
58	?	?	0	1	1	1	0	1	0	0	1	1	0	1	1	1	1
59	.	.	0	1	1	1	0	1	1	0	1	0	0	1	0	1	1
60	⌑ or)	⌑	0	1	1	1	1	0	0	0	1	1	0	1	0	1	0
61	[	(	0	1	1	1	1	0	1	0	1	0	0	1	1	0	1
62	<	<	0	1	1	1	1	1	0	0	1	0	0	1	1	0	0
63	‡	'	0	1	1	1	1	1	1	0	1	1	1	1	1	0	1

	FUNCTION		CODE														
	INPUT	OUTPUT	INPUT							OUTPUT							
ROM ADDRESS	ASCII SYMBOL	EBCDIC SYMBOL	CODE	ASCII b_6	b_5	b_4	b_3	b_2	b_1	EBCDIC 0	1	2	3	4	5	6	7
64	@	@	1	0	0	0	0	0	0	0	1	1	1	1	1	0	0
65	A	A	1	0	0	0	0	0	1	1	1	0	0	0	0	0	1
66	B	B	1	0	0	0	0	1	0	1	1	0	0	0	0	1	0
67	C	C	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
68	D	D	1	0	0	0	1	0	0	1	1	0	0	0	1	0	0
69	E	E	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1
70	F	F	1	0	0	0	1	1	0	1	1	0	0	0	1	1	0
71	G	G	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
72	H	H	1	0	0	1	0	0	0	1	1	0	0	1	0	0	0
73	I	I	1	0	0	1	0	0	1	1	1	0	0	1	0	0	1
74	J	J	1	0	0	1	0	1	0	1	1	0	1	0	0	0	1
75	K	K	1	0	0	1	0	1	1	1	1	0	1	0	0	1	0
76	L	L	1	0	0	1	1	0	0	1	1	0	1	0	0	1	1
77	M	M	1	0	0	1	1	0	1	1	1	0	1	0	1	0	0
78	N	N	1	0	0	1	1	1	0	1	1	0	1	0	1	0	1
79	O	O	1	0	0	1	1	1	1	1	1	0	1	0	1	1	0
80	P	P	1	0	1	0	0	0	0	1	1	0	1	0	1	1	1
81	Q	Q	1	0	1	0	0	0	1	1	1	0	1	1	0	0	0
82	R	R	1	0	1	0	0	1	0	1	1	0	1	1	0	0	1
83	S	S	1	0	1	0	0	1	1	1	1	1	0	0	0	1	0
84	T	T	1	0	1	0	1	0	0	1	1	1	0	0	0	1	1
85	U	U	1	0	1	0	1	0	1	1	1	1	0	0	1	0	0
86	V	V	1	0	1	0	1	1	0	1	1	1	0	0	1	0	1
87	W	W	1	0	1	0	1	1	1	1	1	1	0	0	1	1	0
88	X	X	1	0	1	1	0	0	0	1	1	1	0	0	1	1	1
89	Y	Y	1	0	1	1	0	0	1	1	1	1	0	1	0	0	0
90	Z	Z	1	0	1	1	0	1	0	1	1	1	0	1	0	0	1
91	[	(	1	0	1	1	0	1	1	0	1	0	0	1	1	0	1
92	\	\	1	0	1	1	1	0	0	0	1	0	0	0	0	0	0
93	]	)	1	0	1	1	1	0	1	0	1	0	1	1	1	0	1
94	⌒ or ^	¬	1	0	1	1	1	1	0	0	1	0	1	1	1	1	1
95	—	—	1	0	1	1	1	1	1	0	1	1	0	1	1	0	1
96	Space	Space	1	1	0	0	0	0	0	0	1	0	0	0	0	0	0
97	!	!	1	1	0	0	0	0	1	0	1	0	1	1	0	1	0
98	"	"	1	1	0	0	0	1	0	0	1	1	1	1	1	1	1
99	#	#	1	1	0	0	0	1	1	0	1	1	1	1	0	1	1
100	$	$	1	1	0	0	1	0	0	0	1	0	1	1	0	1	1
101	%	%	1	1	0	0	1	0	1	0	1	1	0	1	1	0	0
102	&	&	1	1	0	0	1	1	0	0	1	0	1	0	0	0	0
103	'	'	1	1	0	0	1	1	1	0	1	1	1	1	1	0	1
104	(	(	1	1	0	1	0	0	0	0	1	0	0	1	1	0	1
105	)	)	1	1	0	1	0	0	1	0	1	0	1	1	1	0	1
106	*	*	1	1	0	1	0	1	0	0	1	0	1	1	1	0	0
107	+	+	1	1	0	1	0	1	1	0	1	0	0	1	1	1	0
108	,	,	1	1	0	1	1	0	0	0	1	1	0	1	0	1	1
109	-	-	1	1	0	1	1	0	1	0	1	1	0	0	0	0	0
110	.	.	1	1	0	1	1	1	0	0	1	0	0	1	0	1	1
111	/	/	1	1	0	1	1	1	1	0	1	1	0	0	0	0	1
112	0	0	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
113	1	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0	1
114	2	2	1	1	1	0	0	1	0	1	1	1	1	0	0	1	0
115	3	3	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1
116	4	4	1	1	1	0	1	0	0	1	1	1	1	0	1	0	0
117	5	5	1	1	1	0	1	0	1	1	1	1	1	0	1	0	1
118	6	6	1	1	1	0	1	1	0	1	1	1	1	0	1	1	0
119	7	7	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1
120	8	8	1	1	1	1	0	0	0	1	1	1	1	1	0	0	0
121	9	9	1	1	1	1	0	0	1	1	1	1	1	1	0	0	1
122	:	:	1	1	1	1	0	1	0	0	1	1	1	1	0	1	0
123	;	;	1	1	1	1	0	1	1	0	1	0	1	1	1	1	0
124	<	<	1	1	1	1	1	0	0	0	1	0	0	1	1	0	0
125	=	=	1	1	1	1	1	0	1	0	1	1	1	1	1	1	0
126	>	>	1	1	1	1	1	1	0	0	1	1	0	1	1	1	0
127	?	?	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1

ROM Code Converters

MM4220LR/MM5220LR BCDIC to ASCII-7/ ASCII-7 to BCDIC code converter

general description

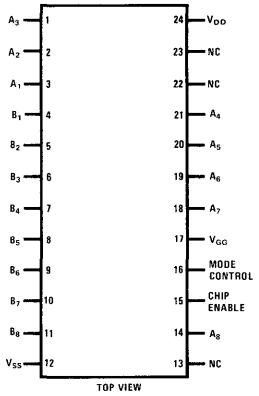
The MM4220LR/MM5220LR is a 128 x 8 read only memory which has been programmed to convert the 64 characters of the Binary Coded Decimal Interchange Code (BCDIC) to the American Standard code for Information Interchange in seven bits (ASCII-7).

The first half of the ROM, from address 0 to address 63, converts the 64 character ASCII graphic subset to BCDIC. The tables show the character assignments and their binary equivalents.

For electrical, environmental and mechanical details, refer to the MM4220/MM5220 data sheet.

connection diagram

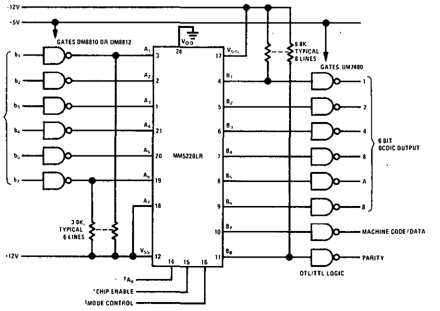
Dual-In-Line Package



TOP VIEW

typical applications

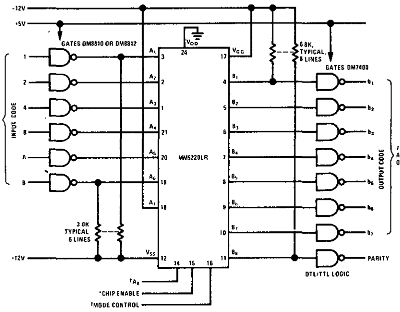
ASCII to BCDIC



Logic Levels
DTL/TTL (except at MOS/ROM interface)
Logic '1' +5V nom; Logic '0' ground, nom
MOS ROM Inputs & Output
Logic '1' more negative Logic '0' more positive

†Mode Control Logic "0"
A_8 Logic "1"
*Chip Enable Logic '1' to obtain outputs

BCDIC to ASCII



Logic Levels
DTL/TTL (except at MOS/ROM interface)
Logic '1', +5V, nom. Logic '0', ground, nom
MOS/ROM Inputs & Output
Logic '1' more negative Logic '0' more positive

†Mode Control Logic 0
A_8 Logic 1
*Chip Enable Logic '1' to obtain outputs

code conversion tables

ASCII to BCDIC

	FUNCTION		CODE														
	INPUT	OUTPUT		INPUT						OUTPUT							
				ASCII								BCDIC					
ROM ADDRESS	ASCII SYMBOL	BCDIC SYMBOL	CODE	b7	b5	b4	b3	b2	b1	MC/ DATA	E P	B	A	8	4	2	1
0	SP	SP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	!	!	0	0	0	0	0	0	1	0	1	1	0	1	0	1	0
2	"	+++	0	0	0	0	0	1	0	0	1	0	1	1	1	1	1
3	=	=	0	0	0	0	0	1	1	0	1	0	0	1	0	1	1
4	$	$	0	0	0	0	1	0	0	0	0	1	0	1	0	1	1
5	%	%	0	0	0	0	1	0	1	0	1	0	1	1	1	0	0
6	&	&	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0
7	'	V	0	0	0	0	1	1	1	0	0	0	1	1	1	0	1
8	(	Blank	0	0	0	1	0	0	0	0	1	0	1	0	0	0	0
9	)	Δ	0	0	0	1	0	0	1	0	1	1	0	1	1	1	1
10	*	*	0	0	0	1	0	1	0	0	1	1	0	1	1	0	0
11	VT	‡	0	0	0	1	0	1	1	1	0	0	1	1	0	1	0
12		,	0	0	0	1	1	0	0	0	0	0	1	1	0	1	1
13	CR	‡	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1
14			0	0	0	1	1	1	0	0	1	1	1	1	0	1	1
15	/	/	0	0	0	1	1	1	1	0	0	0	1	0	0	0	1
16	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	0
17	1	1	0	0	1	0	0	0	1	0	1	0	0	0	0	0	1
18	2	2	0	0	1	0	0	1	0	0	1	0	0	0	0	1	0
19	3	3	0	0	1	0	0	1	1	0	0	0	0	0	0	1	1
20	4	4	0	0	1	0	1	0	0	0	1	0	0	0	1	0	0
21	5	5	0	0	1	0	1	0	1	0	0	0	0	0	1	0	1
22	6	6	0	0	1	0	1	1	0	0	0	0	0	0	1	1	0
23	7	7	0	0	1	0	1	1	1	0	1	0	0	0	1	1	1
24	8	8	0	0	1	1	0	0	0	0	1	0	0	1	0	0	0
25	9	9	0	0	1	1	0	0	1	0	0	0	0	1	0	0	1
26			0	0	1	1	0	1	0	0	1	0	0	1	1	0	1
27		.	0	0	1	1	0	1	1	0	0	1	0	1	1	1	0
28	<	<	0	0	1	1	1	0	0	0	1	1	1	1	1	1	0
29	=	√	0	0	1	1	1	0	1	0	0	0	0	1	1	1	1
30	>	>	0	0	1	1	1	1	0	0	1	0	0	1	1	1	0
31	?	?	0	0	1	1	1	1	1	0	0	1	1	1	0	1	0
32	@	@	0	1	0	0	0	0	0	0	0	0	0	1	1	0	0
33	A	A	0	1	0	0	0	0	1	0	1	1	1	0	0	0	1
34	B	B	0	1	0	0	0	1	0	0	1	1	1	0	0	1	0
35	C	C	0	1	0	0	0	1	1	0	0	1	1	0	0	1	1
36	D	D	0	1	0	0	1	0	0	0	1	1	1	0	1	0	0
37	E	E	0	1	0	0	1	0	1	0	0	1	1	0	1	0	1
38	F	F	0	1	0	0	1	1	0	0	0	1	1	0	1	1	0
39	G	G	0	1	0	0	1	1	1	0	1	1	1	0	1	1	1
40	H	H	0	1	0	1	0	0	0	0	1	1	1	1	0	0	0
41	I	I	0	1	0	1	0	0	1	0	0	1	1	1	0	0	1
42	J	J	0	1	0	1	0	1	0	0	0	1	0	0	0	0	1
43	K	K	0	1	0	1	0	1	1	0	0	1	0	0	0	1	0
44	L	L	0	1	0	1	1	0	0	0	1	1	0	0	0	1	1
45	M	M	0	1	0	1	1	0	1	0	0	1	0	0	1	0	0
46	N	N	0	1	0	1	1	1	0	0	1	1	0	0	1	0	1
47	O	O	0	1	0	1	1	1	1	0	1	1	0	0	1	1	0
48	P	P	0	1	1	0	0	0	0	0	0	1	0	0	1	1	1
49	Q	Q	0	1	1	0	0	0	1	0	0	1	0	1	0	0	0
50	R	R	0	1	1	0	0	1	0	0	1	1	0	1	0	0	1
51	S	S	0	1	1	0	0	1	1	0	0	0	1	0	0	1	0
52	T	T	0	1	1	0	1	0	0	0	1	0	1	0	0	1	1
53	U	U	0	1	1	0	1	0	1	0	0	0	1	0	1	0	0
54	V	V	0	1	1	0	1	1	0	0	1	0	1	0	1	0	1
55	W	W	0	1	1	0	1	1	1	0	1	0	1	0	1	1	0
56	X	X	0	1	1	1	0	0	0	0	0	0	1	0	1	1	1
57	Y	Y	0	1	1	1	0	0	1	0	0	0	1	1	0	0	0
58	Z	Z	0	1	1	1	0	1	0	0	1	0	1	1	0	0	1
59	|	|	0	1	1	1	0	1	1	0	1	1	1	1	1	0	1
60	\	\	0	1	1	1	1	0	0	0	0	0	1	1	1	1	0
61	]	]	0	1	1	1	1	0	1	0	0	1	0	1	1	0	1
62	⌒	□	0	1	1	1	1	1	0	0	0	1	1	1	1	0	0
63	-	-	0	1	1	1	1	1	1	0	1	1	0	0	0	0	0
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

BCDIC to ASCII

	FUNCTION		CODE														
	INPUT	OUTPUT		INPUT							OUTPUT						
				BCDIC							ASCII						
ROM ADDRESS	BCDIC SYMBOL	ASCII SYMBOL	CODE	B	A	8	4	2	1	PARITY	b7	b6	b5	b4	b3	b2	b1
64	SP	SP	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0
65	1	1	1	0	0	0	0	0	1	1	0	1	1	0	0	0	1
66	2	2	1	0	0	0	0	1	0	1	0	1	1	0	0	1	0
67	3	3	1	0	0	0	0	1	1	0	0	1	1	0	0	1	1
68	4	4	1	0	0	0	1	0	0	1	0	1	1	0	1	0	0
69	5	5	1	0	0	0	1	0	1	0	0	1	1	0	1	0	1
70	6	6	1	0	0	0	1	1	0	0	0	1	1	0	1	1	0
71	7	7	1	0	0	0	1	1	1	1	0	1	1	0	1	1	1
72	8	8	1	0	0	1	0	0	0	1	0	1	1	1	0	0	0
73	9	9	1	0	0	1	0	0	1	0	0	1	1	1	0	0	1
74	0	0	1	0	0	1	0	1	0	0	0	1	1	0	0	0	0
75	=	=	1	0	0	1	0	1	1	1	0	1	0	0	0	1	1
76	@	@	1	0	0	1	1	0	0	1	1	0	0	0	0	0	0
77			1	0	0	1	1	0	1	0	0	1	1	1	0	1	0
78	>	>	1	0	0	1	1	1	0	1	0	1	1	1	1	1	0
79	√		1	0	0	1	1	1	1	1	0	1	1	1	1	0	1
80	Blank	(	1	0	1	0	0	0	0	0	0	1	0	1	0	0	0
81	/	/	1	0	1	0	0	0	1	1	0	1	0	1	1	1	1
82	S	S	1	0	1	0	0	1	0	0	1	0	1	0	0	1	1
83	T	T	1	0	1	0	0	1	1	1	1	0	1	0	1	0	0
84	U	U	1	0	1	0	1	0	0	0	1	0	1	0	1	0	1
85	V	V	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0
86	W	W	1	0	1	0	1	1	0	1	1	0	1	0	1	1	1
87	X	X	1	0	1	0	1	1	1	1	1	0	1	1	0	0	0
88	Y	Y	1	0	1	1	0	0	0	0	1	0	1	1	0	0	1
89	Z	Z	1	0	1	1	0	0	1	0	1	0	1	1	0	1	0
90	‡	VT	1	0	1	1	0	1	0	1	0	0	0	1	0	1	1
91	.		1	0	1	1	0	1	1	1	0	1	0	1	1	0	0
92	%	%	1	0	1	1	1	0	0	1	0	1	0	0	1	0	1
93	V	'	1	0	1	1	1	0	1	0	0	1	0	0	1	1	1
94	,		1	0	1	1	1	1	0	0	1	0	1	1	1	0	0
95	+++	"	1	0	1	1	1	1	1	0	0	1	0	0	0	1	0
96	-	-	1	1	0	0	0	0	0	0	1	0	1	1	1	1	1
97	J	J	1	1	0	0	0	0	1	1	1	0	0	1	0	1	0
98	K	K	1	1	0	0	0	1	0	0	1	0	0	1	0	1	1
99	L	L	1	1	0	0	0	1	1	1	1	0	0	1	1	0	0
100	M	M	1	1	0	0	1	0	0	0	1	0	0	1	1	0	1
101	N	N	1	1	0	0	1	0	1	0	1	0	0	1	1	1	0
102	O	O	1	1	0	0	1	1	0	1	1	0	0	1	1	1	1
103	P	P	1	1	0	0	1	1	1	0	1	0	1	0	0	0	0
104	Q	Q	1	1	0	1	0	0	0	1	1	0	1	0	0	0	1
105	R	R	1	1	0	1	0	0	1	1	1	0	1	0	0	1	0
106	!	!	1	1	0	1	0	1	0	0	0	1	0	0	0	0	1
107	$	$	1	1	0	1	0	1	1	0	0	1	0	0	1	0	0
108	*	*	1	1	0	1	1	0	0	1	0	1	0	1	0	1	0
109	]	]	1	1	0	1	1	0	1	1	1	0	1	1	1	0	1
110	.	,	1	1	0	1	1	1	0	1	0	1	1	1	0	1	1
111	Δ	)	1	1	0	1	1	1	1	1	0	1	0	1	0	0	1
112	&	&	1	1	1	0	0	0	0	1	0	1	0	0	1	1	0
113	A	A	1	1	1	0	0	0	1	0	1	0	0	0	0	0	1
114	B	B	1	1	1	0	0	1	0	0	1	0	0	0	0	1	0
115	C	C	1	1	1	0	0	1	1	1	1	0	0	0	0	1	1
116	D	D	1	1	1	0	1	0	0	0	1	0	0	0	1	0	0
117	E	E	1	1	1	0	1	0	1	1	1	0	0	0	1	0	1
118	F	F	1	1	1	0	1	1	0	1	1	0	0	0	1	1	0
119	G	G	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1
120	H	H	1	1	1	1	0	0	0	0	1	0	0	1	0	0	0
121	I	I	1	1	1	1	0	0	1	1	1	0	0	1	0	0	1
122	?	?	1	1	1	1	0	1	0	0	0	1	1	1	1	1	1
123			1	1	1	1	0	1	1	0	0	1	0	1	1	1	0
124	□	⌒	1	1	1	1	1	0	0	1	1	0	1	1	1	1	0
125	|	[	1	1	1	1	1	0	1	1	1	0	1	1	0	1	1
126	<	<	1	1	1	1	1	1	0	0	0	1	1	1	1	0	0
127	‡	CR	1	1	1	1	1	1	1	1	0	0	0	1	1	0	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

ROM Code Converters

MM4221RQ/MM5221RQ ASCII-7 to EIA RS244A/ EIA RS244A to ASCII-7

general description

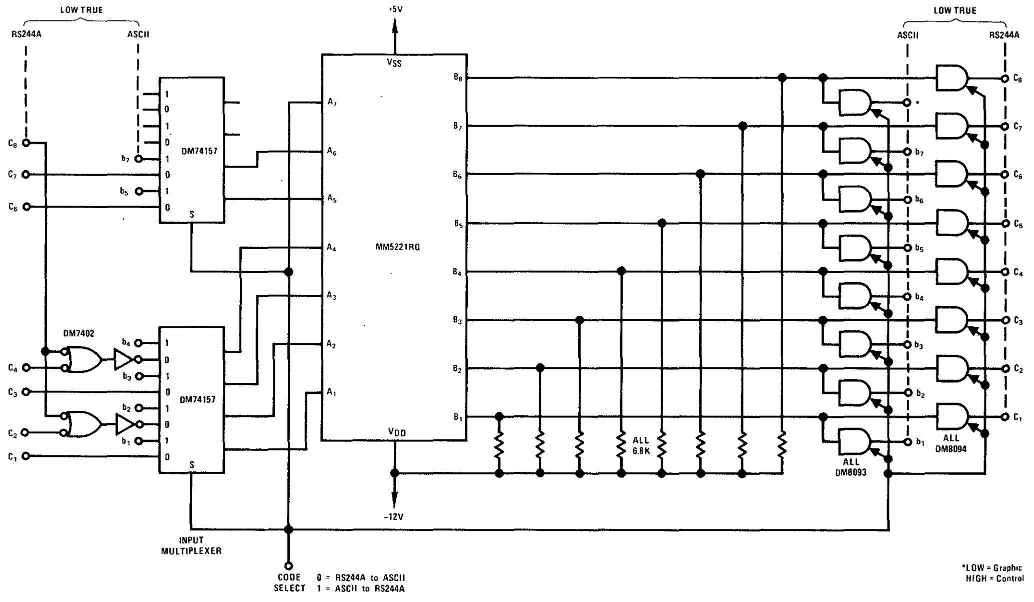
The MM4221RQ/MM5221RQ is a 1024-bit read only memory that has been programmed to convert between the American Standard Code for Information Interchange, compressed to six bits, and the Electronic Industries Association numerical control standard code, RS244A. The second group of addresses, from 64 to 127, effects the reverse conversion.

applications information

In the first 64 entries, compression of ASCII-7 to six bits has been accomplished by dropping bit b_6, and substituting the control codes listed for certain unused ASCII graphic symbols.

In the second 64 entries, the RS244A parity check bit, C_5 is ignored. The bit C_8, used only for the end of block code (EOB) is used externally to detect existence of this symbol, and to insert a redundant code, $C_4 . C_2$ (ROM address 74). This code will be translated arbitrarily as an ASCII EXT.

typical application



code conversion tables

ASCII to RS244A

ROM ADDRESS	FUNCTION		CODE	CODE													
	INPUT	OUTPUT		INPUT						OUTPUT							
	ASCII SYMBOL	EIA SYMBOL		b7	b5	b4	b3	b2	b1	c8	c7	c6	c5	c4	c3	c2	c1
0	SP	SP	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1			0	0	0	0	0	0	1								
2			0	0	0	0	0	1	0								
3	ETX	EOB	0	0	0	0	0	1	1	1	0	0	0	0	0	0	0
4	EOT	EOR	0	0	0	0	1	0	0	0	0	0	0	1	0	1	1
5	%	%	0							0	1	0	1	1	0	1	1
6	&	&	0							0	0	0	0	1	1	1	0
7			0														
8	BS	BS	0							0	0	1	0	1	0	1	0
9	HT	TAB	0							0	0	1	1	1	1	1	0
10			0							0	0	0	0	0	0	0	0
11	+	+	0							0	1	1	1	0	0	0	0
12	,	,	0							0	0	1	1	1	0	1	1
13	-		0							0	1	0	0	0	0	0	0
14			0							0	1	1	0	1	0	1	1
15	/	/	0							0	0	1	1	0	0	0	1
16	0	0	0							0	0	1	0	0	0	0	0
17	1	1	0							0	0	0	0	0	0	0	1
18	2	2	0							0	0	0	0	0	0	1	0
19	3	3	0							0	0	0	1	0	0	1	1
20	4	4	0							0	0	0	0	0	1	0	0
21	5	5	0							0	0	0	1	0	1	0	1
22	6	6	0							0	0	0	1	0	1	1	0
23	7	7	0							0	0	0	0	0	1	1	1
24	8	8	0							0	0	0	0	1	0	0	0
25	9	9	0							0	0	0	1	1	0	0	1
26			0														
27		UC	0														
28	FS	LC	0							0	1	1	1	1	0	1	0
29	GS		0							0	1	1	1	1	1	0	0
30			0														
31			0														
32			0														
33	a	a	0	Increasing Binary Sequence						0	1	1	0	0	0	0	1
34	b	b	0							0	1	1	0	0	0	1	0
35	c	c	0							0	1	1	1	0	0	1	1
36	d	d	0							0	1	1	0	0	1	0	0
37	e	e	0							0	1	1	0	0	1	0	1
38	f	f	0							0	1	1	1	0	1	1	0
39	g	g	0							0	1	1	0	0	1	1	1
40	h	h	0							0	1	1	0	1	0	0	0
41	i	i	0							0	1	1	1	1	0	0	1
42	j	j	0							0	1	0	1	0	0	0	1
43	k	k	0							0	1	0	1	0	0	1	0
44	l	l	0							0	1	0	0	0	0	1	1
45	m	m	0							0	1	0	1	0	1	0	0
46	n	n	0							0	1	0	0	0	1	0	1
47	o	o	0							0	1	0	0	0	1	1	0
48	p	p	0							0	1	0	1	0	1	1	1
49	q	q	0							0	1	0	1	1	0	0	0
50	r	r	0							0	1	0	0	1	0	0	1
51	s	s	0							0	0	1	1	0	0	1	0
52	t	t	0							0	0	1	0	0	0	1	1
53	u	u	0							0	0	1	1	0	1	0	0
54	v	v	0							0	0	1	0	0	1	0	1
55	w	w	0							0	0	1	0	0	1	1	0
56	x	x	0							0	0	1	1	0	1	1	1
57	y	y	0							0	0	1	1	1	0	0	0
58	z	z	0							0	0	1	0	1	0	0	1
59			0														
60			0														
61			0														
62			0														
63	DEL	DEL	0							0	1	1	1	1	1	1	1
			A7	A6	A5	A4	A3	A2	A1	B8	B7	B6	B5	B4	B3	B2	B1

RS244A to ASCII

ROM ADDRESS	FUNCTION		CODE	CODE													
	INPUT	OUTPUT		INPUT						OUTPUT							
	EIA SYMBOL	ASCII SYMBOL		c7	c6	c4	c3	c2	c1	CC/G	b7	b6	b5	b4	b3	b2	b1
64	Space	Space	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0
65	1	1	1	0	0	0	0	0	1	1	0	1	1	0	0	0	1
66	2	2	1	0	0	0	0	1	0	1	0	1	1	0	0	1	0
67	3	3	1	0	0	0	0	1	1	1	0	1	1	0	0	1	1
68	4	4	1	0	0	0	1	0	0	1	0	1	1	0	1	0	0
69	5	5	1	0	0	0	1	0	1	1	0	1	1	0	1	0	1
70	6	6	1							1	0	1	1	0	1	1	0
71	7	7	1							1	0	1	1	0	1	1	1
72	8	8	1							1	0	1	1	1	0	0	0
73	9	9	1							1	0	1	1	1	0	0	1
74	EOB	ETX	1	0	0	1	0	1	0	0	0	0	0	0	0	1	1
75	EOR	EOT	1							0	0	0	0	0	1	0	0
76			1														
77			1														
78	&	&	1							1	0	1	0	0	1	1	0
79			1														
80	0	0	1							1	0	1	1	0	0	0	0
81	/	/	1							1	0	1	0	1	1	1	1
82	s	s	1							1	1	1	1	0	0	1	1
83	t	t	1							1	1	1	1	0	1	0	0
84	u	u	1							1	1	1	1	0	1	0	1
85	v	v	1	Increasing Binary Sequence						1	1	1	1	0	1	1	0
86	w	w	1							1	1	1	1	0	1	1	1
87	x	x	1							1	1	1	1	1	0	0	0
88	y	y	1							1	1	1	1	1	0	0	1
89	z	z	1							1	1	1	1	1	0	1	0
90	BS	BS	1							0	0	0	0	1	0	0	0
91			1							1	0	1	0	1	1	0	0
92			1														
93			1														
94	TAB	HT	1							0	0	0	0	1	0	0	1
95			1														
96			1	1	0	0	0	0	0	1	0	1	0	1	1	0	1
97	j	j	1	1	0	0	0	0	1	1	1	1	0	1	0	1	0
98	k	k	1							1	1	1	0	1	0	1	1
99	l	l	1							1	1	1	0	1	1	0	0
100	m	m	1							1	1	1	0	1	1	0	1
101	n	n	1							1	1	1	0	1	1	1	0
102	o	o	1							1	1	1	0	1	1	1	1
103	p	p	1							1	1	1	1	0	0	0	0
104	q	q	1							1	1	1	1	0	0	0	1
105	r	r	1							1	1	1	1	0	0	1	0
106			1														
107	%	%	1							1	0	1	0	0	1	0	1
108			1														
109			1														
110			1														
111			1														
112	+	+	1							1	0	1	0	1	0	1	1
113	a	a	1							1	1	1	0	0	0	0	1
114	b	b	1							1	1	1	0	0	0	1	0
115	c	c	1							1	1	1	0	0	0	1	1
116	d	d	1							1	1	1	0	0	1	0	0
117	e	e	1							1	1	1	0	0	1	0	1
118	f	f	1							1	1	1	0	0	1	1	0
119	g	g	1							1	1	1	0	0	1	1	1
120	h	h	1							1	1	1	0	1	0	0	0
121	i	i	1							1	1	1	0	1	0	0	1
122	LC	GS	1							0	0	0	1	1	1	0	1
123			1							1	0	1	0	1	1	1	0
124	UC	FS	1							0	0	0	1	1	1	0	0
125			1														
126			1														
127	DEL	DEL	1							0	1	1	1	1	1	1	1
			A7	A6	A5	A4	A3	A2	A1	B8	B7	B6	B5	B4	B3	B2	B1

ROM Code Converters

MM4221RR/MM5221RR ASCII-7 to EBCDIC code converter

general description

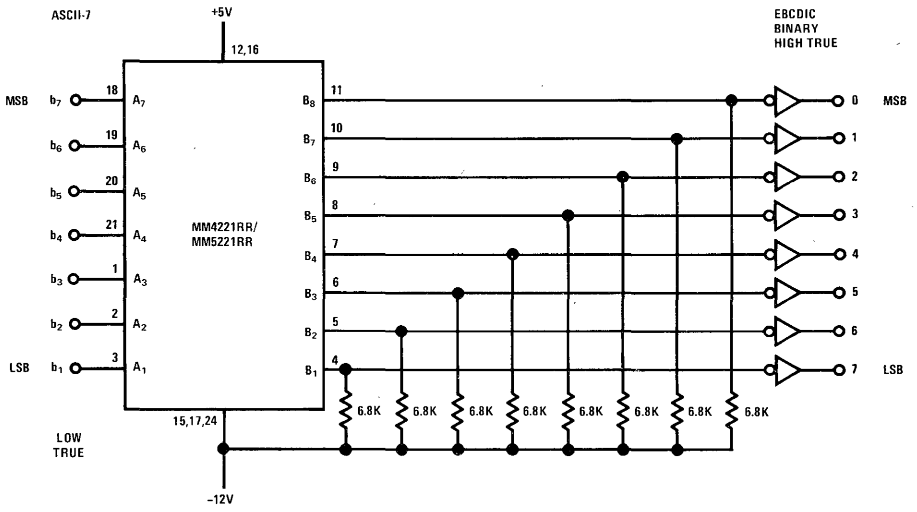
The MM4221RR/MM5221RR is a 1024-bit read-only memory that has been programmed to convert between the 128 characters of ASCII-7, the American Standard Code for Information Interchange in seven bits, and EBCDIC, an extended binary coded decimal interchange code. This conversion follows the EBCDIC character assignments used in the IBM 1130 computer.

Certain arbitrary assignments have also been made for maximum usefulness, and in these two areas the part differs from the MM4230QY/MM5230QY, which follows American National Standard ANSI X3.26 recommendations for character assignments.

For electrical, environmental and mechanical details, refer to the MM4221/MM5221 data sheet.

typical application

ASCII-7 to EBCDIC



code conversion tables

ROM ADDRESS	FUNCTION INPUT ASCII SYMBOL	FUNCTION OUTPUT EBCDIC SYMBOL	CODE INPUT MSB						LSB	CODE OUTPUT MSB							LSB
0	NULL	NULL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	SOH	SOH	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
2	STX	STX	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
3	ETX	ETX	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1
4	EOT	EOT	0	0	0	0	1	0	0	0	0	1	1	0	1	1	1
5	ENQ	ENQ	0	0	0	0	1	0	1	0	0	1	0	1	1	0	1
6	ACK	ACK	0	0	0	0	1	1	0	0	0	1	0	1	1	1	0
7	BEL	BEL	0	0	0	0	1	1	1	0	0	1	0	1	1	1	1
8	BS	BS	0	0	0	1	0	0	0	0	0	0	1	0	1	1	0
9	HT	HT	0	0	0	1	0	0	1	0	0	0	0	0	1	0	1
10	LF	LF	0	0	0	1	0	1	0	0	0	1	0	0	1	0	1
11	VT	VT	0	0	0	1	0	1	1	0	0	0	0	1	0	1	1
12	FF	FF	0	0	0	1	1	0	0	0	0	0	0	1	1	0	0
13	CR	CR	0	0	0	1	1	0	1	0	0	0	0	1	1	0	1
14	SO	SO	0	0	0	1	1	1	0	0	0	0	0	1	1	1	0
15	S1	S1	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
16	DLE	DLE	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0
17	DC1	DC1	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
18	DC2	DC2								0	0	0	1	0	0	1	0
19	DC3	DC3								0	0	0	1	0	0	1	1
20	DC4	RS								0	0	1	1	0	1	0	1
21	NAK	NAK								0	0	1	1	1	1	0	1
22	SYN	SYN								0	0	1	1	0	0	1	0
23	ETB	EOB								0	0	1	0	0	1	1	0
24	CAN	CAN								0	0	0	1	1	0	0	0
25	EM	EM				CONTINUING BINARY SEQUENCE				0	0	0	1	1	0	0	1
26	SUB	SUB								0	0	1	1	1	1	1	1
27	ESC	BYP								0	0	1	0	0	1	0	0
28	FS	FLS								0	0	0	1	1	1	0	0
29	GS	GS								0	0	0	1	1	1	0	1
30	RS	RDS								0	0	0	1	1	1	1	0
31	US	US								0	0	0	1	1	1	1	1
32	SP	SP	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0
33	!	!								0	1	0	1	1	0	1	0
34	"	"								0	1	1	1	1	1	1	1
35	#	#								0	1	1	1	1	0	1	1
36	$	$								0	1	0	1	1	0	1	1
37	%	%								0	1	1	0	1	1	0	0
38	&	&								0	1	0	1	0	0	0	0
39	'	'								0	1	1	1	1	1	0	1
40	(	(								0	1	0	0	1	1	0	1
41	)	)								0	1	0	1	1	1	0	1
42	*	*								0	1	0	1	1	1	0	0
43	+	+								0	1	0	0	1	1	1	0
44	,	,								0	1	1	0	1	0	1	1
45	-	-								0	1	1	0	0	0	0	0
46	.									0	1	0	0	1	0	1	1
47	/	/								0	1	1	0	0	0	0	1
48	0	0								1	1	1	1	0	0	0	0
49	1	1								1	1	1	1	0	0	0	1
50	2	2								1	1	1	1	0	0	1	0
51	3	3								1	1	1	1	0	0	1	1
52	4	4								1	1	1	1	0	1	0	0
53	5	5								1	1	1	1	0	1	0	1
54	6	6								1	1	1	1	0	1	1	0
55	7	7								1	1	1	1	0	1	1	1
56	8	8								1	1	1	1	1	0	0	0
57	9	9								1	1	1	1	1	0	0	1
58		:								0	1	1	1	1	0	1	0
59	;	;								0	1	0	1	1	1	1	0
60	<	<								0	1	0	0	1	1	0	0
61	=	=								0	1	1	1	1	1	1	0
62	>	>								0	1	1	0	1	1	1	0
63	?	?								0	1	1	0	1	1	1	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

ROM ADDRESS	FUNCTION INPUT ASCII SYMBOL	FUNCTION OUTPUT EBCDIC SYMBOL	CODE INPUT MSB						LSB	CODE OUTPUT MSB							LSB
64	@	@	1	0	0	0	0	0	0	0	1	1	1	1	1	0	0
65	A	A								1	1	0	0	0	0	0	1
66	B	B								1	1	0	0	0	0	1	0
67	C	C								1	1	0	0	0	0	1	1
68	D	D								1	1	0	0	0	1	0	0
69	E	E								1	1	0	0	0	1	0	1
70	F	F								1	1	0	0	0	1	1	0
71	G	G								1	1	0	0	0	1	1	1
72	H	H								1	1	0	0	1	0	0	0
73	I	I								1	1	0	0	1	0	0	1
74	J	J								1	1	0	1	0	0	0	1
75	K	K								1	1	0	1	0	0	1	0
76	L	L								1	1	0	1	0	0	1	1
77	M	M								1	1	0	1	0	1	0	0
78	N	N								1	1	0	1	0	1	0	1
79	O	O								1	1	0	1	0	1	1	0
80	P	P								1	1	0	1	0	1	1	1
81	Q	Q				CONTINUING BINARY SEQUENCE				1	1	0	1	1	0	0	0
82	R	R								1	1	0	1	1	0	0	1
83	S	S								1	1	1	0	0	0	1	0
84	T	T								1	1	1	0	0	0	1	1
85	U	U								1	1	1	0	0	1	0	0
86	V	V								1	1	1	0	0	1	0	1
87	W	W								1	1	1	0	0	1	1	0
88	X	X								1	1	1	0	0	1	1	1
89	Y	Y								1	1	1	0	1	0	0	0
90	Z	Z								1	1	1	0	1	0	0	1
91	[	[								1	0	1	0	1	1	0	1
92	\	NL								0	0	0	1	0	1	0	1
93	]	]								1	0	1	1	1	1	0	1
94	^	¬								0	1	0	1	1	1	1	1
95	-	-								0	1	1	0	1	1	0	1
96	`	RES	1	1	0	0	0	0	0	0	0	0	1	0	1	0	0
97	a	a								1	0	0	0	0	0	0	1
98	b	b								1	0	0	0	0	0	1	0
99	c	c								1	0	0	0	0	0	1	1
100	d	d								1	0	0	0	0	1	0	0
101	e	e								1	0	0	0	0	1	0	1
102	f	f								1	0	0	0	0	1	1	0
103	g	g								1	0	0	0	0	1	1	1
104	h	h								1	0	0	0	1	0	0	0
105	i	i								1	0	0	0	1	0	0	1
106	j	j								1	0	0	1	0	0	0	1
107	k	k								1	0	0	1	0	0	1	0
108	l	l								1	0	0	1	0	0	1	1
109	m	m								1	0	0	1	0	1	0	0
110	n	n								1	0	0	1	0	1	0	1
111	o	o								1	0	0	1	0	1	1	0
112	p	p								1	0	0	1	0	1	1	1
113	q	q								1	0	0	1	1	0	0	0
114	r	r								1	0	0	1	1	0	0	1
115	s	s								1	0	1	0	0	0	1	0
116	t	t								1	0	1	0	0	0	1	1
117	u	u								1	0	1	0	0	1	0	0
118	v	v								1	0	1	0	0	1	0	1
119	w	w								1	0	1	0	0	1	1	0
120	x	x								1	0	1	0	0	1	1	1
121	y	y								1	0	1	0	1	0	0	0
122	z	z								1	0	1	0	1	0	0	1
123	{	{								1	0	0	0	1	0	1	1
124	¦	¦								0	1	0	0	1	1	1	1
125	}	}								1	0	0	1	1	0	1	1
126	~	¢								0	1	0	0	1	0	1	0
127	DEL	DEL								0	0	0	0	0	1	1	1
			A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

ROM Code Converters

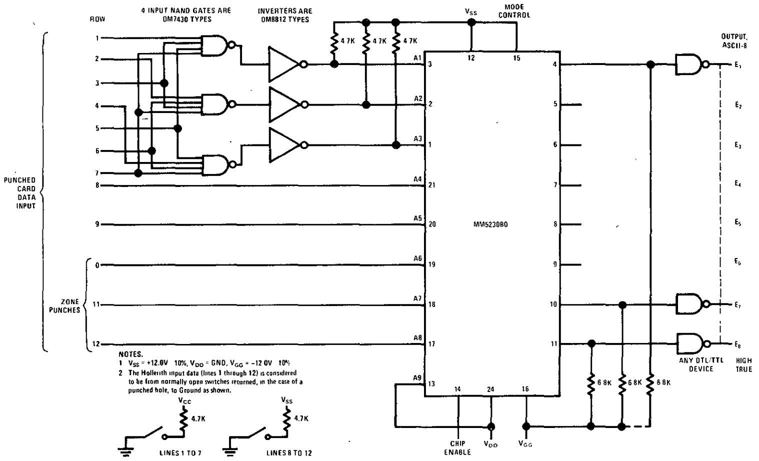
MM4230BO/MM5230BO hollerith to ASCII code converter

general description

The MM4230BO/MM5230BO 2048-bit MOS read-only memory has been programmed to convert the 12 line Hollerith punched card code to eight level ASCII. This conversion conforms to the American National Standard (ANSI x 3.26 – 1970). Three TTL 4-input NAND gates, and three inverters are used to compress the 12 Hollerith lines to eight-line binary encoded form suitable for use by the read-only memory. This application is shown below.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 data sheet.

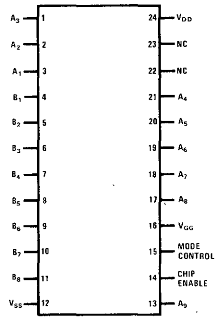
typical application



NOTES.
1 V_{SS} = +12.0V 10%, V_{DD} = GND, V_{GG} = −12.0V 10%
2 The Hollerith input data (lines 1 through 12) is considered to be from normally open switches returned, in the case of a punched hole, to Ground as shown.

connection diagram

Dual-In-Line Package



TOP VIEW

code conversion table

Hollerith to ASCII

	12	11	0		12 0	12 11	11 0	12 11 0	12	11	0		12 0	12 11	11 0	12 11 0	
	&	-	ϕ	SP	{	¦	}	11/10	10/8	11/1	11/9		12/3	12/10	13/1	13/8	8-1
1	A	J	/	1	a	j	~	13/9	SOH	DC1	8/1	9/1	10/0	10/9	9/15	11/11	9 -1
2	B	K	S	2	b	k	s	13/10	STX	DC2	8/2	SYN	10/1	10/10	11/2	11/12	9 -2
3	C	L	T	3	c	l	t	13/11	ETX	DC3	8/3	9/3	10/2	10/11	11/3	11/13	9 -3
4	D	M	U	4	d	m	u	13/12	9/12	9/13	8/4	9/4	10/3	10/12	11/4	11/14	9 -4
5	E	N	V	5	e	n	v	13/13	HT	8/5	LF	9/5	10/4	10/13	11/5	11/15	9 -5
6	F	O	W	6	f	o	w	13/14	8/6	BS	ETB	9/6	10/5	10/14	11/6	12/0	9 -6
7	G	P	X	7	g	p	x	13/15	DEL	8/7	ESC	EOT	10/6	10/15	11/7	12/1	9 -7
8	H	Q	Y	8	h	q	y	14/0	9/7	CAN	8/8	9/8	10/7	11/0	11/8	12/2	9 -8
9	I	R	Z	9	i	r	z	14/1	8/13	EM	8/9	9/9	NUL	DLE	8/0	9/0	9-8-1
8-2	[	]	\	:	12/4	12/11	13/2	14/2	8/14	9/2	8/10	9/10	14/8	14/14	15/4	15/10	9-8-2
8-3	.	$	,	=	12/5	12/12	13/3	14/3	VT	8/15	8/11	9/11	14/9	14/15	15/5	15/11	9-8-3
8-4	<	*	%	@	12/6	12/13	13/4	14/4	FF	FS	8/12	DC4	14/10	15/0	15/6	15/12	9-8-4
8-5	(	)	–	'	12/7	12/14	13/5	14/5	CR	GS	ENQ	NAK	14/11	15/1	15/7	15/13	9-8-5
8-6	+	;	>	=	12/8	12/15	13/6	14/6	SO	RS	ACK	9/14	14/12	15/2	15/8	15/14	9-8-6
8-7	! ①	②	?	"	12/9	13/0	13/7	14/7	SI	US	BEL	SUB	14/13	15/3	15/9	15/15	9-8-7

① may be "|"

② may be "¬"

Note: The entries of Form A/B refer to the unassigned locations in the right hand side of the ASCII table (bit E_8 = 1) designated for specialist use. (See National Bureau of Standards Technical Note No. 478.)

Note: For the full ASCII-8 Code Table, see MM4230QY/MM5230QY data sheet

ROM Code Converters

MM4230FE/MM5230FE selectric-to-EBCDIC/ EBCDIC-to-selectric code converter

general description

The MM4230FE/MM5230FE provides for the conversion of IBM Selectric Correspondence Code to Extended Binary Coded Decimal Interchange Code (EBCDIC) in both directions. These two decoders are contained on a monolithic MOS device.

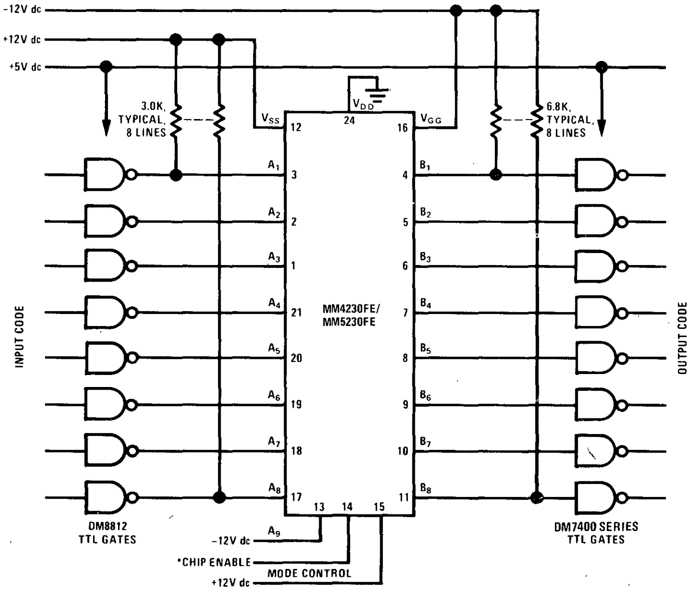
The Selectric-to-EBCDIC converter is located in binary addresses 0 through 127. Input bit A7 is used as a single line command to determine whether upper (denoted by a "1") or a lower (denoted by a "0") case has been selected.

The EBCDIC-to-Selectric converter is located in binary addresses 128 through 255. Since not all EBCDIC control commands have Selectric code counterparts, it is not necessary to encode bit position 0 (A8), which is used instead as the code converter selection bit. In addition to the Selectric Correspondence output code bits there is a bit to indicate upper or lower case. The odd parity bit generated does not account for the case bit.

device characteristics

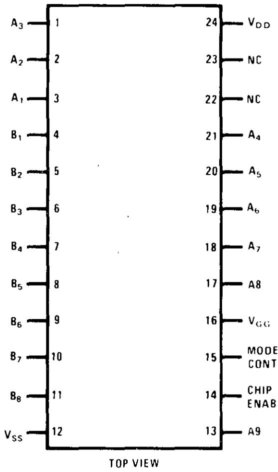
For full electrical, environmental, and mechanical details refer to the MM4230/MM5230 2048-bit read only memory data sheet.

typical application



Logic Levels
DTL/TTL (except at MOS/ROM interface)
Logic "1", +5V, nom. Logic "0", ground, nom.
MOS/ROM Inputs & Outputs
Logic "1", more negative. Logic "0", more positive
*Chip Enable = Logic "1" to obtain outputs

connection diagram



code conversion table—selectric-to-EBCDIC

ROM ADDRESS	FUNCTION		CODE															
	INPUT	OUTPUT	INPUT								OUTPUT							
	SELECTRIC SYMBOL	EBCDIC SYMBOL	CODE	CASE	SELECTRIC						EBCDIC							
					R_5	R_2	R_1	R_{2A}	T_1	T_2	0	1	2	3	4	5	6	7
0	-	-	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
1	b	b	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0
2	w	w	0	0	0	0	0	0	1	0	1	0	1	0	0	1	1	0
3	9	9	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	1
4	q	q	0	0	0	0	0	1	0	0	1	0	0	1	1	0	0	0
5	k	k	0	0	0	0	0	1	0	1	1	0	0	1	0	0	1	0
6	i	i	0	0	0	0	0	1	1	0	1	0	0	0	1	0	0	1
7	6	6	0	0	0	0	0	1	1	1	1	1	1	1	0	1	1	0
8	y	y	0	0	0	0	1	0	0	0	1	0	1	0	1	0	0	0
9	h	h	0	0	0	0	1	0	0	1	1	0	0	0	1	0	0	0
10	s	s	0	0	0	0	1	0	1	0	1	0	1	0	0	0	1	0
11	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0
12	p	p	0	0	0	0	1	1	0	0	1	0	0	1	0	1	1	1
13	e	e	0	0	0	0	1	1	0	1	1	0	0	0	0	1	0	1
14	'	'	0	0	0	0	1	1	1	0	0	1	1	1	1	1	0	1
15	5	5	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	1
16		NULL	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
17		NULL	0	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0
18		NULL	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0
19		NULL	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0
20	=	=	0	0	0	1	0	1	0	0	0	1	1	1	1	1	1	0
21	n	n	0	0	0	1	0	1	0	1	1	0	0	1	0	1	0	1
22	.		0	0	0	1	0	1	1	0	0	1	0	0	1	0	1	1
23	2	2	0	0	0	1	0	1	1	1	1	1	1	1	0	0	1	0
24		NULL	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
25		NULL	0	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0
26		NULL	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0
27		NULL	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0
28	j	j	0	0	0	1	1	1	0	0	1	0	0	1	0	0	0	1
29	t	t	0	0	0	1	1	1	0	1	1	0	1	0	0	0	1	1
30		NULL	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0
31	z	z	0	0	0	1	1	1	1	1	1	0	1	0	1	0	0	1
32		NULL	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
33		NULL	0	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0
34		NULL	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
35		NULL	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0
36	,	,	0	0	1	0	0	1	0	0	0	1	1	0	1	0	1	1
37	c	c	0	0	1	0	0	1	0	1	1	0	0	0	0	0	1	1
38	a	a	0	0	1	0	0	1	1	0	1	0	0	0	0	0	0	1
39	8	8	0	0	1	0	0	1	1	1	1	1	1	1	1	0	0	0
40	/	/	0	0	1	0	1	0	0	0	0	1	1	0	0	0	0	1
41	l	l	0	0	1	0	1	0	0	1	1	0	0	1	0	0	1	1
42	o	o	0	0	1	0	1	0	1	0	1	0	0	1	0	1	1	0
43	4	4	0	0	1	0	1	0	1	1	1	1	1	1	0	1	0	0
44	,	,	0	0	1	0	1	1	0	0	0	1	0	1	1	1	1	0
45	d	d	0	0	1	0	1	1	0	1	1	0	0	0	0	1	0	0
46	r	r	0	0	1	0	1	1	1	0	1	0	0	1	1	0	0	1
47	7	7	0	0	1	0	1	1	1	1	1	1	1	1	0	1	1	1
48		NULL	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
49		NULL	0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0
50		NULL	0	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0
51		NULL	0	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0
52	f	f	0	0	1	1	0	1	0	0	1	0	0	0	0	1	1	0
53	u	u	0	0	1	1	0	1	0	1	1	0	1	0	0	1	0	0
54	v	v	0	0	1	1	0	1	1	0	1	0	1	0	0	1	0	1
55	3	3	0	0	1	1	0	1	1	1	1	1	1	1	0	0	1	1
56		NULL	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
57		NULL	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0
58		NULL	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0
59		NULL	0	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0
60	g	g	0	0	1	1	1	1	0	0	1	0	0	0	0	1	1	1
61	x	x	0	0	1	1	1	1	0	1	1	0	1	0	0	1	1	1
62	m	m	0	0	1	1	1	1	1	0	1	0	0	1	0	1	0	0
63	1	1	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	1
64	–	–	0	1	0	0	0	0	0	0	0	1	1	0	1	1	0	1
65	B	B	0	1	0	0	0	0	0	1	1	1	0	0	0	0	1	0
66	W	W	0	1	0	0	0	0	1	0	1	1	1	0	0	1	1	0
67	(	(	0	1	0	0	0	0	1	1	0	1	0	0	1	1	0	1
68	Q	Q	0	1	0	0	0	1	0	0	1	1	0	1	1	0	0	0
69	K	K	0	1	0	0	0	1	0	1	1	1	0	1	0	0	1	0
70	I	I	0	1	0	0	0	1	1	0	1	1	0	0	1	0	0	1
71	¢	¢	0	1	0	0	0	1	1	1	0	1	0	0	1	0	1	0
72	Y	Y	0	1	0	0	1	0	0	0	1	1	1	0	1	0	0	0
73	H	H	0	1	0	0	1	0	0	1	1	1	0	0	1	0	0	0
74	S	S	0	1	0	0	1	0	1	0	1	1	1	0	0	0	1	0
75	)	)	0	1	0	0	1	0	1	1	0	1	0	0	1	1	0	1
76	P	P	0	1	0	0	1	1	0	0	1	1	0	1	0	1	1	1
77	E	E	0	1	0	0	1	1	0	1	1	1	0	0	0	1	0	1
78	"	"	0	1	0	0	1	1	1	0	0	1	1	1	1	1	1	1
79	%	%	0	1	0	0	1	1	1	1	0	1	1	0	1	1	0	0
80		NULL	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
81		NULL	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0
82		NULL	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0
83		NULL	0	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0
84	+	+	0	1	0	1	0	1	0	0	0	1	0	0	1	1	1	0
85	N	N	0	1	0	1	0	1	0	1	1	1	0	1	0	1	0	1
86	.		0	1	0	1	0	1	1	0	0	1	0	0	1	0	1	1
87	@	@	0	1	0	1	0	1	1	1	0	1	1	1	1	1	0	0
88		NULL	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
89		NULL	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0
90		NULL	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0
91		NULL	0	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0
92	J	J	0	1	0	1	1	1	0	0	1	1	0	1	0	0	0	1
93	T	T	0	1	0	1	1	1	0	1	1	1	1	0	0	0	1	1
94		NULL	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0
95	Z	Z	0	1	0	1	1	1	1	1	1	1	1	0	1	0	0	1
96		NULL	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
97		NULL	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0
98		NULL	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0
99		NULL	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0
100	,	,	0	1	1	0	0	1	0	0	0	1	1	0	1	0	1	1
101	C	C	0	1	1	0	0	1	0	1	1	1	0	0	0	0	1	1
102	A	A	0	1	1	0	0	1	1	0	1	1	0	0	0	0	0	1
103	*	*	0	1	1	0	0	1	1	1	0	1	0	1	1	1	0	0
104	?	?	0	1	1	0	1	0	0	0	0	1	1	0	1	1	1	1
105	L	L	0	1	1	0	1	0	0	1	1	1	0	1	0	0	1	1
106	O	O	0	1	1	0	1	0	1	0	1	1	0	1	0	1	1	0
107	$	$	0	1	1	0	1	0	1	1	0	1	0	1	1	0	1	1
108	:		0	1	1	0	1	1	0	0	0	1	1	1	1	0	1	0
109	D	D	0	1	1	0	1	1	0	1	1	1	0	0	0	1	0	0
110	R	R	0	1	1	0	1	1	1	0	1	1	0	1	1	0	0	1
111	&	&	0	1	1	0	1	1	1	1	0	1	0	1	0	0	0	0
112		NULL	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
113		NULL	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0
114		NULL	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0
115		NULL	0	1	1	1	0	0	1	1	0	0	0	0	0	0	0	0
116	F	F	0	1	1	1	0	1	0	0	1	1	0	0	0	1	1	0
117	U	U	0	1	1	1	0	1	0	1	1	1	1	0	0	1	0	0
118	V	V	0	1	1	1	0	1	1	0	1	1	1	0	0	1	0	1
119	#	#	0	1	1	1	0	1	1	1	0	1	1	1	1	0	1	1
120		NULL	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
121		NULL	0	1	1	1	1	0	0	1	0	0	0	0	0	0	0	0
122		NULL	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
123		NULL	0	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0
124	G	G	0	1	1	1	1	1	0	0	1	1	0	0	0	1	1	1
125	X	X	0	1	1	1	1	1	0	1	1	1	1	0	0	1	1	1
126	M	M	0	1	1	1	1	1	1	0	1	1	0	1	0	1	0	0
127	±	NULL	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
			128	64	32	16	8	4	2	1								
			(ROM ADDRESS IN BINARY)															
			(A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1)	(B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1)

code conversion table—EBCDIC-to-selectric

ROM ADDRESS	FUNCTION		CODE															
	INPUT	OUTPUT	INPUT								OUTPUT							
	EBCDIC SYMBOL	SELECTRIC SYMBOL	CODE	EBCDIC 1	2	3	4	5	6	7	PARITY	CASE	SELECTRIC R_5	R_2	R_1	R_{2A}	T_1	T_2
128	NUL	–	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
129	SOH a	a	1	0	0	0	0	0	0	1	0	0	1	0	0	1	1	0
130	STX b	b	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1
131	ETX c	c	1	0	0	0	0	0	1	1	0	0	1	0	0	1	0	1
132	PF d	d	1	0	0	0	0	1	0	0	1	0	1	0	1	1	0	1
133	HT e	e	1	0	0	0	0	1	0	1	0	0	0	0	1	1	0	1
134	LC f	f	1	0	0	0	0	1	1	0	0	0	1	1	0	1	0	0
135	DEL g	g	1	0	0	0	0	1	1	1	1	0	1	1	1	1	0	0
136	h	h	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	1
137	i	i	1	0	0	0	1	0	0	1	1	0	0	0	0	1	1	0
138	SMM	–	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
139	VT	–	1	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0
140	FF	–	1	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0
141	CR	–	1	0	0	0	1	1	0	1	0	0	0	0	0	0	0	0
142	SO	–	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0
143	SI	–	1	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
144	DLE	–	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
145	DC1 j	j	1	0	0	1	0	0	0	1	0	0	0	1	1	1	0	0
146	DC2 k	k	1	0	0	1	0	0	1	0	1	0	0	0	0	1	0	1
147	TM l	l	1	0	0	1	0	0	1	1	0	0	1	0	1	0	0	1
148	RES m	m	1	0	0	1	0	1	0	0	0	0	1	1	1	1	1	0
149	NL n	n	1	0	0	1	0	1	0	1	0	0	0	1	0	1	0	1
150	BS o	o	1	0	0	1	0	1	1	0	0	0	1	0	1	0	1	0
151	IL p	p	1	0	0	1	0	1	1	1	1	0	0	0	1	1	0	0
152	CAN q	q	1	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0
153	EM r	r	1	0	0	1	1	0	0	1	1	0	1	0	1	1	1	0
154	CC	–	1	0	0	1	1	0	1	0	0	0	0	0	0	0	0	0
155	CU1	–	1	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0
156	IFS	–	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0
157	IGS	–	1	0	0	1	1	1	0	1	0	0	0	0	0	0	0	0
158	IRS	–	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0
159	IUS	–	1	0	0	1	1	1	1	1	0	0	0	0	0	0	0	0
160	DS	–	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
161	SOS	–	1	0	1	0	0	0	0	1	0	0	0	0	0	0	0	0
162	FS s	s	1	0	1	0	0	0	1	0	1	0	0	0	1	0	1	0
163	t	t	1	0	1	0	0	0	1	1	1	0	0	1	1	1	0	1
164	BYP u	u	1	0	1	0	0	1	0	0	1	0	1	1	0	1	0	1
165	LF v	v	1	0	1	0	0	1	0	1	1	0	1	1	0	1	1	0
166	ETB w	w	1	0	1	0	0	1	1	0	0	0	0	0	0	0	1	0
167	ESC x	x	1	0	1	0	0	1	1	1	0	0	1	1	1	1	0	1
168	y	y	1	0	1	0	1	0	0	0	0	0	0	0	1	0	0	0
169	z	z	1	0	1	0	1	0	0	1	0	0	0	1	1	1	1	1
170	SM	–	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0
171	CU2	–	1	0	1	0	1	0	1	1	0	0	0	0	0	0	0	0
172		–	1	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0
173	ENQ	–	1	0	1	0	1	1	0	1	0	0	0	0	0	0	0	0
174	ACK	–	1	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0
175	BEL	–	1	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0
176		–	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0
177		–	1	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0
178	SYN	–	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0
179		–	1	0	1	1	0	0	1	1	0	0	0	0	0	0	0	0
180	PN	–	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0
181	RS	–	1	0	1	1	0	1	0	1	0	0	0	0	0	0	0	0
182	UC	–	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0
183	EOT	–	1	0	1	1	0	1	1	1	0	0	0	0	0	0	0	0
184		–	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0
185		–	1	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0
186		-	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0
187	CU3	–	1	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0
188	DC4	–	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0
189	NAK	–	1	0	1	1	1	1	0	1	0	0	0	0	0	0	0	0
190		–	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0
191	SUB	–	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
192	Space	–	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
193	A	A	1	1	0	0	0	0	0	1	0	1	1	0	0	1	1	0
194	B	B	1	1	0	0	0	0	1	0	0	1	0	0	0	0	0	1
195	C	C	1	1	0	0	0	0	1	1	0	1	1	0	0	1	0	1
196	D	D	1	1	0	0	0	1	0	0	1	1	1	0	1	1	0	1
197	E	E	1	1	0	0	0	1	0	1	0	1	0	0	1	1	0	1
198	F	F	1	1	0	0	0	1	1	0	0	1	1	1	0	1	0	0
199	G	G	1	1	0	0	0	1	1	1	1	1	1	1	1	1	0	0
200	H	H	1	1	0	0	1	0	0	0	1	1	0	0	1	0	0	1
201	I	I	1	1	0	0	1	0	0	1	1	1	0	0	0	1	1	0
202	¢	¢	1	1	0	0	1	0	1	0	0	1	0	0	0	1	1	1
203			1	1	0	0	1	0	1	1	0	0	0	1	0	1	1	0
204	<	–	1	1	0	0	1	1	0	0	0	0	0	0	0	0	0	0
205	(	(	1	1	0	0	1	1	0	1	1	1	0	0	0	0	1	1
206	+	+	1	1	0	0	1	1	1	0	1	1	0	1	0	1	0	0
207	|	–	1	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0
208	&	&	1	1	0	1	0	0	0	0	0	1	1	0	1	1	1	1
209	J	J	1	1	0	1	0	0	0	1	0	1	0	1	1	1	0	0
210	K	K	1	1	0	1	0	0	1	0	1	1	0	0	0	1	0	1
211	L	L	1	1	0	1	0	0	1	1	0	1	1	0	1	0	0	1
212	M	M	1	1	0	1	0	1	0	0	0	1	1	1	1	1	1	0
213	N	N	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
214	O	O	1	1	0	1	0	1	1	0	0	1	1	0	1	0	1	0
215	P	P	1	1	0	1	0	1	1	1	1	1	0	0	1	1	0	0
216	Q	Q	1	1	0	1	1	0	0	0	0	1	0	0	0	1	0	0
217	R	R	1	1	0	1	1	0	0	1	1	1	1	0	1	1	1	0
218	!	–	1	1	0	1	1	0	1	0	0	0	0	0	0	0	0	0
219	$	$	1	1	0	1	1	0	1	1	1	1	1	0	1	0	1	1
220	* or *	*	1	1	0	1	1	1	0	0	1	1	1	0	0	1	1	1
221	)	)	1	1	0	1	1	1	0	1	0	1	0	0	1	0	1	1
222	;	;	1	1	0	1	1	1	1	0	0	0	1	0	1	1	0	0
223	¬	–	1	1	0	1	1	1	1	1	0	0	0	0	0	0	0	0
224	–	–	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	0
225	/	/	1	1	1	0	0	0	0	1	1	0	1	0	1	0	0	0
226	S	S	1	1	1	0	0	0	1	0	1	1	0	0	1	0	1	0
227	T	T	1	1	1	0	0	0	1	1	1	1	0	1	1	1	0	1
228	U	U	1	1	1	0	0	1	0	0	1	1	1	1	0	1	0	1
229	V	V	1	1	1	0	0	1	0	1	1	1	1	1	0	1	1	0
230	W	W	1	1	1	0	0	1	1	0	0	1	0	0	0	0	1	0
231	X	X	1	1	1	0	0	1	1	1	0	1	1	1	1	1	0	1
232	Y	Y	1	1	1	0	1	0	0	0	0	1	0	0	1	0	0	0
233	Z	Z	1	1	1	0	1	0	0	1	0	1	0	1	1	1	1	1
234		–	1	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0
235	,	,	1	1	1	0	1	0	1	1	1	0	1	0	0	1	0	0
236	%	%	1	1	1	0	1	1	0	0	1	1	0	0	1	1	1	1
237	– or —	–	1	1	1	0	1	1	0	1	1	1	0	0	0	0	0	0
238	>	–	1	1	1	0	1	1	1	0	0	0	0	0	0	0	0	0
239	?	?	1	1	1	0	1	1	1	1	1	1	1	0	1	0	0	0
240	0	0	1	1	1	1	0	0	0	0	0	0	0	0	1	0	1	1
241	1	1	1	1	1	1	0	0	0	1	1	0	1	1	1	1	1	1
242	2	2	1	1	1	1	0	0	1	0	1	0	0	1	0	1	1	1
243	3	3	1	1	1	1	0	0	1	1	0	0	1	1	0	1	1	1
244	4	4	1	1	1	1	0	1	0	0	1	0	1	0	1	0	1	1
245	5	5	1	1	1	1	0	1	0	1	1	0	0	0	1	1	1	1
246	6	6	1	1	1	1	0	1	1	0	0	0	0	0	0	1	1	1
247	7	7	1	1	1	1	0	1	1	1	0	0	1	0	1	1	1	1
248	8	8	1	1	1	1	1	0	0	0	1	0	1	0	0	1	1	1
249	9	9	1	1	1	1	1	0	0	1	1	0	0	0	0	0	1	1
250			1	1	1	1	1	0	1	0	0	1	1	0	1	1	0	0
251	#	#	1	1	1	1	1	0	1	1	0	1	1	1	0	1	1	1
252	@	@	1	1	1	1	1	1	0	0	1	1	0	1	0	1	1	1
253	'	'	1	1	1	1	1	1	0	1	0	0	0	0	1	1	1	0
254	=	=	1	1	1	1	1	1	1	0	1	0	0	1	0	1	0	0
255	"	"	1	1	1	1	1	1	1	1	0	1	0	0	1	1	1	0
			128	64	32	16	8	4	2	1								
			(ROM ADDRESS IN BINARY)															
			(A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1)	(B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1)

ROM Code Converters

MM4230JT/MM5230JT BCDIC to EBCDIC/ EBCDIC to BCDIC code converter

general description

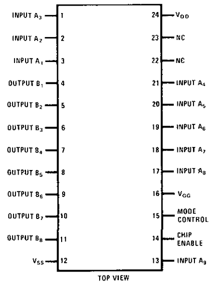
The MM4230JT/MM5230JT is a 2048-bit read-only memory that has been programmed to convert from the 64-entry, 6-bit Binary Coded Decimal Interchange Code (BCDIC) to the eight-bit extended BCD interchange code (EBCDIC) and back again. The tables show the two translations in binary.

Character assignments for the EBCDIC are given to IBM1130 specifications. All the non-alphanumeric assignments in BCDIC are subject to specialist usage, and care should be taken over them.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 data sheet.

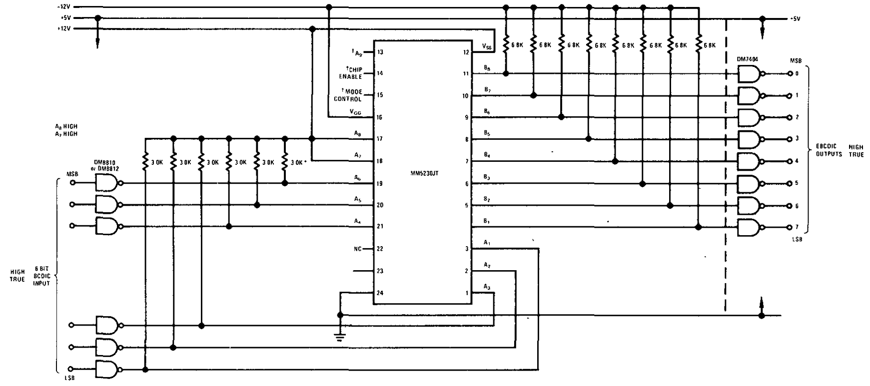
connection diagram

Dual-In-Line Package

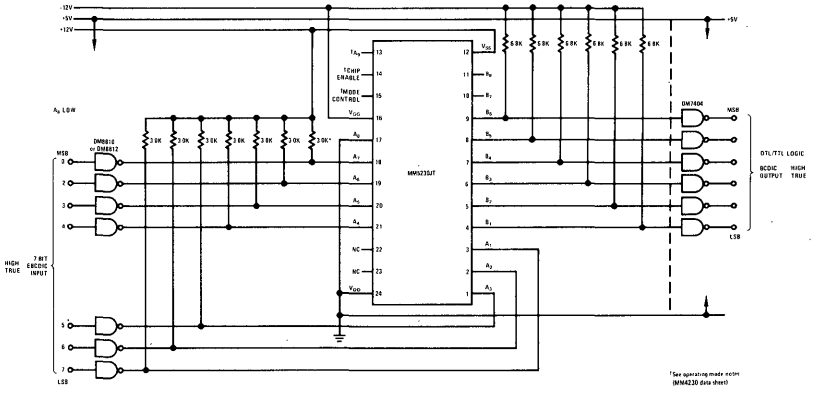


typical applications

BCDIC to EBCDIC



EBCDIC to BCDIC



code conversion tables

BCDIC to EBCDIC

	FUNCTION		CODE							
	INPUT	OUTPUT	OUTPUT							
ROM ADDRESS	BCDIC SYMBOL	EBCDIC SYMBOL	EBCDIC							
			B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
0	NULL	NULL	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	0	0	0	1
2	2	2	1	1	1	1	0	0	1	0
3	3	3	1	1	1	1	0	0	1	1
4	4	4	1	1	1	1	0	1	0	0
5	5	5	1	1	1	1	0	1	0	1
6	6	6	1	1	1	1	0	1	1	0
7	7	7	1	1	1	1	0	1	1	1
8	8	8	1	1	1	1	1	0	0	0
9	9	9	1	1	1	1	1	0	0	1
10	0	0	1	1	1	1	0	0	0	0
11	=	=	0	1	1	1	1	0	1	1
12	@	@	0	1	1	1	1	1	0	0
13		'	0	1	1	1	1	1	0	1
14			0	1	1	1	1	1	1	0
15	"	"	0	1	1	1	1	1	1	1
16	Space	Space	0	1	0	0	0	0	0	0
17	/	/	0	1	1	0	0	0	0	1
18	S	S	1	1	1	0	0	0	1	0
19	T	T	1	1	1	0	0	0	1	1
20	U	U	1	1	1	0	0	1	0	0
21	V	V	1	1	1	0	0	1	0	1
22	W	W	1	1	1	0	0	1	1	0
23	X	X	1	1	1	0	0	1	1	1
24	Y	Y	1	1	1	0	1	0	0	0
25	Z	Z	1	1	1	0	1	0	0	1
26	NULL	NULL	0	1	0	0	0	0	0	0
27	,	,	0	1	1	0	1	0	1	1
28	%	%	0	1	1	0	1	1	0	0
29	--	-	0	1	1	0	1	1	0	1
30			0	1	1	0	1	1	1	0
31	?	?	0	1	1	0	1	1	1	1
32	-		0	1	1	0	0	0	0	0
33	J	J	1	1	0	1	0	0	0	1
34	K	K	1	1	0	1	0	0	1	0
35	L	L	1	1	0	1	0	0	1	1
36	M	M	1	1	0	1	0	1	0	0
37	N	N	1	1	0	1	0	1	0	1
38	O	O	1	1	0	1	0	1	1	0
39	P	P	1	1	0	1	1	1	1	1
40	Q	Q	1	1	0	1	1	0	0	0
41	R	R	1	1	0	1	1	0	0	1
42	!	!	0	1	0	1	1	0	1	0
43	$	$	0	1	0	1	1	0	1	1
44	*	*	0	1	0	1	1	1	0	0
45	)	)	0	1	0	1	1	1	0	1
46			0	1	0	1	1	1	1	0
47	¬	¬	0	1	0	1	1	1	1	1
48	&	&	0	1	0	1	0	0	0	0
49	A	A	1	1	0	0	0	0	0	1
50	B	B	1	1	0	0	0	0	1	0
51	C	C	1	1	0	0	0	0	1	1
52	D	D	1	1	0	0	0	1	0	0
53	E	E	1	1	0	0	0	1	0	1
54	F	F	1	1	0	0	0	1	1	0
55	G	G	1	1	0	0	0	1	1	1
56	H	H	1	1	0	0	1	0	0	0
57	I	I	1	1	0	0	1	0	0	1
58	¢	¢	0	1	0	0	1	0	1	0
59			0	1	0	0	1	0	1	1
60	<	<	0	1	0	0	1	1	0	0
61	(	(	0	1	0	0	1	1	0	1
62	+	+	0	1	0	0	1	1	1	0
63	|	|	0	1	0	0	1	1	1	1
64	0	0	1	1	1	1	0	0	0	0
65	1	1	1	1	1	1	0	0	0	1
66	2	2	1	1	1	1	0	0	1	0
67	3	3	1	1	1	1	0	0	1	1
68	4	4	1	1	1	1	0	1	0	0
69	5	5	1	1	1	1	0	1	0	1
70	6	6	1	1	1	1	0	1	1	0
71	NULL	NULL	0	0	0	0	0	0	0	0
72	7	7	1	1	1	1	0	1	1	1
73	8	8	1	1	1	1	1	0	0	0
74	9	9	1	1	1	1	1	0	0	1
75	NULL	NULL	0	0	0	0	0	0	0	0
76	NULL	NULL	0	0	0	0	0	0	0	0
77	NULL	NULL	0	0	0	0	0	0	0	0
78	NULL	NULL	0	0	0	0	0	0	0	0
79	NULL	NULL	0	0	0	0	0	0	0	0
80	NULL	NULL	0	0	0	0	0	0	0	0
81	NULL	NULL	0	0	0	0	0	0	0	0
82	NULL	NULL	0	0	0	0	0	0	0	0
83	NULL	NULL	0	0	0	0	0	0	0	0
84	NULL	NULL	0	0	0	0	0	0	0	0
85	NULL	NULL	0	0	0	0	0	0	0	0
86	NULL	NULL	0	0	0	0	0	0	0	0
87	NULL	NULL	0	0	0	0	0	0	0	0
88	NULL	NULL	0	0	0	0	0	0	0	0
89	NULL	NULL	0	0	0	0	0	0	0	0
90	NULL	NULL	0	0	0	0	0	0	0	0
91	NULL	NULL	0	0	0	0	0	0	0	0
92	NULL	NULL	0	0	0	0	0	0	0	0
93	NULL	NULL	0	0	0	0	0	0	0	0
94	NULL	NULL	0	0	0	0	0	0	0	0
95	NULL	NULL	0	0	0	0	0	0	0	0
96	NULL	NULL	0	0	0	0	0	0	0	0
97	NULL	NULL	0	0	0	0	0	0	0	0
98	NULL	NULL	0	0	0	0	0	0	0	0
99	NULL	NULL	0	0	0	0	0	0	0	0
100	NULL	NULL	0	0	0	0	0	0	0	0
101	NULL	NULL	0	0	0	0	0	0	0	0
102	NULL	NULL	0	0	0	0	0	0	0	0
103	NULL	NULL	0	0	0	0	0	0	0	0
104	NULL	NULL	0	0	0	0	0	0	0	0
105	NULL	NULL	0	0	0	0	0	0	0	0
106	NULL	NULL	0	0	0	0	0	0	0	0
107	NULL	NULL	0	0	0	0	0	0	0	0
108	NULL	NULL	0	0	0	0	0	0	0	0
109	NULL	NULL	0	0	0	0	0	0	0	0
110	NULL	NULL	0	0	0	0	0	0	0	0
111	NULL	NULL	0	0	0	0	0	0	0	0
112	NULL	NULL	0	0	0	0	0	0	0	0
113	NULL	NULL	0	0	0	0	0	0	0	0
114	NULL	NULL	0	0	0	0	0	0	0	0
115	NULL	NULL	0	0	0	0	0	0	0	0
116	NULL	NULL	0	0	0	0	0	0	0	0
117	NULL	NULL	0	0	0	0	0	0	0	0
118	NULL	NULL	0	0	0	0	0	0	0	0
119	NULL	NULL	0	0	0	0	0	0	0	0
120	NULL	NULL	0	0	0	0	0	0	0	0
121	NULL	NULL	0	0	0	0	0	0	0	0
122	NULL	NULL	0	0	0	0	0	0	0	0
123	NULL	NULL	0	0	0	0	0	0	0	0
124	NULL	NULL	0	0	0	0	0	0	0	0
125	NULL	NULL	0	0	0	0	0	0	0	0
126	NULL	NULL	0	0	0	0	0	0	0	0
127	NULL	NULL	0	0	0	0	0	0	0	0

EBCDIC to BCDIC

	FUNCTION		CODE							
	INPUT	OUTPUT	OUTPUT							
ROM ADDRESS	EBCDIC SYMBOL	BCDIC SYMBOL	BCDIC							
			B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1
128	NULL	NULL	0	0	0	0	0	0	0	0
129	NULL	NULL	0	0	0	0	0	0	0	0
130	NULL	NULL	0	0	0	0	0	0	0	0
131	NULL	NULL	0	0	0	0	0	0	0	0
132	NULL	NULL	0	0	0	0	0	0	0	0
133	-	-	0	0	0	1	0	0	0	0
134		-	0	0	0	1	0	0	0	0
135	NULL	NULL	0	0	0	0	0	0	0	0
136	NULL	NULL	0	0	0	0	0	0	0	0
137	-	-	0	0	0	1	0	0	0	0
138	¢	¢	0	0	1	1	1	0	1	0
139			0	0	1	1	1	0	1	1
140	<	<	0	0	1	1	1	1	0	0
141	(	(	0	0	1	1	1	1	0	1
142	+	+	0	0	1	1	1	1	1	0
143	|	|	0	0	1	1	1	1	1	1
144	&	&	0	0	1	1	0	0	0	0
145	NULL	NULL	0	0	0	0	0	0	0	0
146	NULL	NULL	0	0	0	0	0	0	0	0
147	NULL	NULL	0	0	0	0	0	0	0	0
148	NULL	NULL	0	0	0	0	0	0	0	0
149	-	-	0	0	0	1	0	0	0	0
150	-	-	0	0	0	1	0	0	0	0
151	NULL	NULL	0	0	0	0	0	0	0	0
152	NULL	NULL	0	0	0	0	0	0	0	0
153	!	!	0	0	0	0	0	0	0	0
154	$	$	0	0	1	0	1	0	1	0
155	*	*	0	0	1	0	1	0	1	1
156	)	)	0	0	1	0	1	1	0	0
157			0	0	1	0	1	1	0	1
158	|	|	0	0	1	0	1	1	1	0
159			0	0	1	0	1	1	1	1
160			0	0	1	0	0	0	0	0
161	┘	┘	0	0	0	1	0	0	0	1
162	NULL	NULL	0	0	0	0	0	0	0	0
163	NULL	NULL	0	0	0	0	0	0	0	0
164	NULL	NULL	0	0	0	0	0	0	0	0
165	NULL	NULL	0	0	0	0	0	0	0	0
166	NULL	NULL	0	0	0	0	0	0	0	0
167	NULL	NULL	0	0	0	0	0	0	0	0
168	NULL	NULL	0	0	0	0	0	0	0	0
169	NULL	NULL	0	0	0	0	0	0	0	0
170	NULL	NULL	0	0	0	0	0	0	0	0
171		,	0	0	0	1	1	0	1	1
172	%	%	0	0	0	1	1	1	0	0
173			0	0	0	1	1	1	0	1
174			0	0	0	1	1	1	1	0
175	?	?	0	0	0	1	1	1	1	1
176	NULL	NULL	0	0	0	0	0	0	0	0
177	NULL	NULL	0	0	0	0	0	0	0	0
178	NULL	NULL	0	0	0	0	0	0	0	0
179	NULL	NULL	0	0	0	0	0	0	0	0
180	NULL	NULL	0	0	0	0	0	0	0	0
181		-	0	0	0	1	0	0	0	0
182	-	-	0	0	0	1	0	0	0	0
183	NULL	NULL	0	0	0	0	0	0	0	0
184	NULL	NULL	0	0	0	0	0	0	0	0
185	NULL	NULL	0	0	0	0	0	0	0	0
186			0	0	0	0	0	0	0	0
187	#	=	0	0	0	0	1	0	1	1
188	@	@	0	0	0	0	1	1	0	0
189	'		0	0	0	0	1	1	0	1
190			0	0	0	0	1	1	1	0
191		"	0	0	0	0	1	1	1	1
192	-	-	0	0	0	1	0	0	0	0
193	A	A	0	0	1	1	0	0	0	1
194	B	B	0	0	1	1	0	0	1	0
195	C	C	0	0	1	1	0	0	1	1
196	D	D	0	0	1	1	0	1	0	0
197	E	E	0	0	1	1	0	1	0	1
198	F	F	0	0	1	1	0	1	1	0
199	G	G	0	0	1	1	0	1	1	1
200	H	H	0	0	1	1	1	0	0	0
201	I	I	0	0	1	1	1	0	0	1
202	NULL	NULL	0	0	0	0	0	0	0	0
203	NULL	NULL	0	0	0	0	0	0	0	0
204	NULL	NULL	0	0	0	0	0	0	0	0
205	NULL	NULL	0	0	0	0	0	0	0	0
206	NULL	NULL	0	0	0	0	0	0	0	0
207	NULL	NULL	0	0	0	0	0	0	0	0
208	NULL	NULL	0	0	0	0	0	0	0	0
209	J	J	0	0	1	0	0	0	0	1
210	K	K	0	0	1	0	0	0	1	0
211	L	L	0	0	1	0	0	0	1	1
212	M	M	0	0	1	0	0	1	0	0
213	N	N	0	0	1	0	0	1	0	1
214	O	O	0	0	1	0	0	1	1	0
215	P	P	0	0	1	0	0	1	1	1
216	Q	Q	0	0	1	0	1	0	0	0
217	R	R	0	0	1	0	1	0	0	1
218	NULL	NULL	0	0	0	0	0	0	0	0
219	NULL	NULL	0	0	0	0	0	0	0	0
220	NULL	NULL	0	0	0	0	0	0	0	0
221	NULL	NULL	0	0	0	0	0	0	0	0
222	NULL	NULL	0	0	0	0	0	0	0	0
223	NULL	NULL	0	0	0	0	0	0	0	0
224	NULL	NULL	0	0	0	0	0	0	0	0
225	NULL	NULL	0	0	0	0	0	0	0	0
226	S	S	0	0	0	1	0	0	1	0
227	T	T	0	0	0	1	0	0	1	1
228	U	U	0	0	0	1	0	1	0	0
229	V	V	0	0	0	1	0	1	0	1
230	W	W	0	0	0	1	0	1	1	0
231	X	X	0	0	0	1	0	1	1	1
232	Y	Y	0	0	0	1	1	0	0	0
233	Z	Z	0	0	0	1	1	0	0	1
234	NULL	NULL	0	0	0	0	0	0	0	0
235	NULL	NULL	0	0	0	0	0	0	0	0
236	NULL	NULL	0	0	0	0	0	0	0	0
237	NULL	NULL	0	0	0	0	0	0	0	0
238	NULL	NULL	0	0	0	0	0	0	0	0
239	NULL	NULL	0	0	0	0	0	0	0	0
240	0	0	0	0	0	0	1	0	1	0
241	1	1	0	0	0	0	0	0	0	1
242	2	2	0	0	0	0	0	0	1	0
243	3	3	0	0	0	0	0	0	1	1
244	4	4	0	0	0	0	0	1	0	0
245	5	5	0	0	0	0	0	1	0	1
246	6	6	0	0	0	0	0	1	1	0
247	7	7	0	0	0	0	0	1	1	1
248	8	8	0	0	0	0	1	0	0	0
249	9	9	0	0	0	0	1	0	0	1
250	NULL	NULL	0	0	0	0	0	0	0	0
251	NULL	NULL	0	0	0	0	0	0	0	0
252	NULL	NULL	0	0	0	0	0	0	0	0
253	NULL	NULL	0	0	0	0	0	0	0	0
254	NULL	NULL	0	0	0	0	0	0	0	0
255	NULL	NULL	0	0	0	0	0	0	0	0

ROM Code Converters

MM4230KP/MM5230KP ASCII-7 to selectric code converter

general description

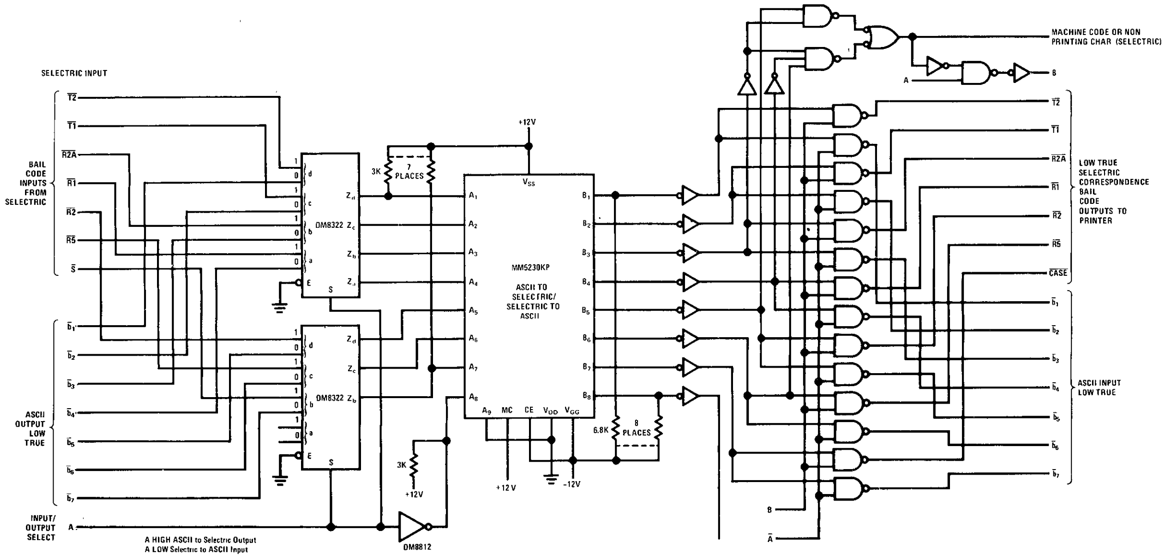
The MM4230KP/MM5230KP MOS read-only memory has been programmed to perform the conversion between the American Standard Code for Information Interchange in seven bits (ASCII) and the Selectric correspondence bail code transmitted and received by the IBM Series 7 input/output printers.

application hints

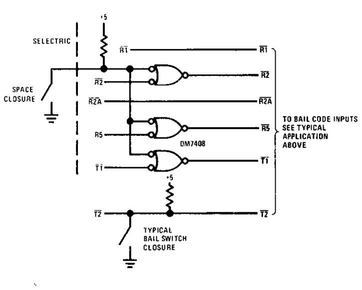
The ASCII field and Selectric bail code field as defined do not map exactly: for instance "space" is handled as a normal 7-bit code in ASCII, but is handled as a unique switch and solenoid pair in the Selectric printer. And even among the graphic characters, ± and ¢ exist only for Selectric, and > and < only for ASCII. The former problem is handled in the MM4230KP/MM5230KP by exploiting the inherent redundancy of the bail code (see Table 2). The latter inconsistency is resolved by making arbitrary equivalences between the unique characters. The two tables show the treatment of both the characters which have equivalents in both codes, and those characters, and the functions, which do not. Encoding and decoding the Selectric functions that the user requires is a matter of conventional Boolean logic. A typical example is shown below.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 data sheet.

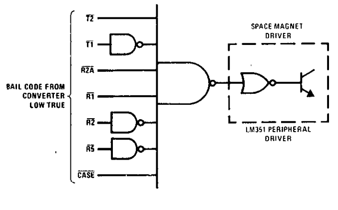
typical application



Encoding 'Space' by Gating In on Input



Decoding 'Space' on Output



code conversion tables

Table 1. ASCII-7 to Selectric

Bits b7 → b6 → b5 →					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
b4 ↓	b3 ↓	b2 ↓	b1 ↓	Row ↓ / Column →	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL 02	DLE 0A	SP 62	0	@	P	25	p
0	0	0	1	1	SOH 12	DCI IA	!	1	A	Q	a	q
0	0	1	0	2	STX 22	DC2 2A	"	2	B	R	b	r
0	0	1	1	3	ETX 32	DC3 3A	#	3	C	S	c	s
0	1	0	0	4	EOT 03	DC4 0B	$	4	D	T	d	t
0	1	0	1	5	ENQ 13	NAK 1B	%	5	E	U	e	u
0	1	1	0	6	ACK 23	SYN 2B	&	6	F	V	f	v
0	1	1	1	7	BEL 33	ETB 3B	25	7	G	W	g	w
1	0	0	0	8	BS 42	CAN 4A	(	8	H	X	h	x
1	0	0	1	9	HT 52	EM 5A	)	9	I	Y	i	y
1	0	1	0	A	LF 53	SUB 6A	*	:	J	Z	j	z
1	0	1	1	B	VT 72	ESC 7A	+	;	K	[7F	k	{ 7F
1	1	0	0	C	FF 72	FS 4B	,	< 40	L	\ 60	l	¦ 48
1	1	0	1	D	CR 53	GS 5B	–	=	M	] 77	m	} 77
1	1	1	0	E	SO 63	RS 6B	.	> 50	N	^ 70	n	~ 58
1	1	1	1	F	SI 73	US 7B	/	?	O	_	o	DEL 00

Table 2. Selectric to ASCII-7

R5 → T1 → T2 →					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
S ↓	R2A ↓	R2 ↓	R1 ↓	Row ↓ / Column →	0	1	2	3	4	5	6	7
0	0	0	0	0	- 2/D	b	w	9	▨ < 3/C	▨ > 3/E	▨ \ 5/C	▨ ^ 5/E
0	0	0	1	1	y	h	s	0 3/0	/	l 6/C	° 6/F	4
0	0	1	0	2	▨ NUL 0/0	▨ SOH 0/1	▨ STX 0/2	▨ ETX 0/3	▨ BS 0/8	▨ TAB 0/9	▨ SP 2/0	▨ IND 0/A
0	0	1	1	3	▨ EOT C/4	▨ ENQ 0/5	▨ ACK 0/6	▨ BELL 0/7	▨	▨ CR 0/D	▨ SO 0/E	▨ SI 0/F
0	1	0	0	4	Q	k	l	6	, 2/C	c	a	8
0	1	0	1	5	P	e	' 2/7	5	; 3/B	d	r	7
0	1	1	0	6	= 3/D	n	. 2/E	2	f	u	v	3
0	1	1	1	7	J	t	½! 2/1	z	g	x	m	1
1	0	0	0	8	_	B	W	(	▨ ¦ 7/C	▨ ~ 7/E	▨	▨
1	0	0	1	9	Y	H	S	)	?	L	° 4/F	$
1	0	1	0	A	▨ DLE 1/0	▨ DC1 1/1	▨ DC2 1/2	▨ DC3 1/3	▨ CAN 1/8	▨ EM 1/9	▨ SUB 1/A	▨ ESC 1/B
1	0	1	1	B	▨ DC4 1/4	▨ NAK 1/5	▨ SYN 1/6	▨ ETB 1/7	▨ FS 1/C	▨ GS 1/D	▨ RS 1/E	▨ US 1/F
1	1	0	0	C	Q	K	I 4/9	¢ 6/3	, 2/C	C	A	*
1	1	0	1	D	P	E	"	%	·	D	R	&
1	1	1	0	E	+	N	. 2/E	@	F	U	V	#
1	1	1	1	F	J	T	¼° F/F	Z	G	X	M	±[5/B

▨ Entries Thus are Redundant Bail Codes

ASCII shown thus: Column No./Row No.

ROM Code Converters

MM4230QW/MM5230QW hollerith to EBCDIC code converter

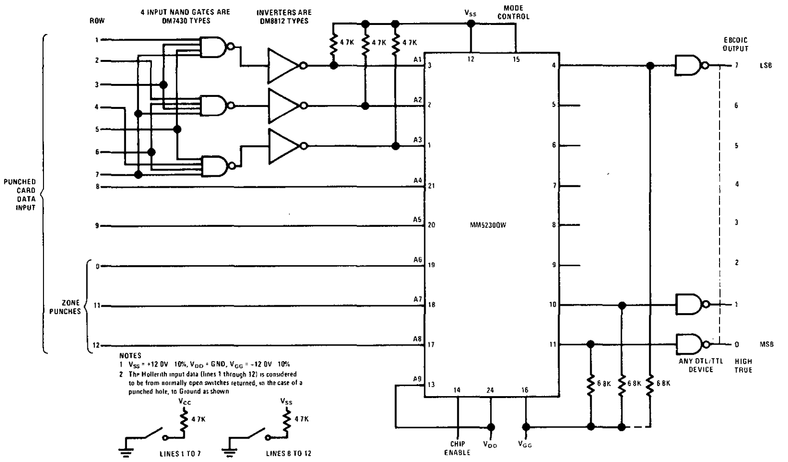
general description

The MM4230QW/MM5230QW 2048-bit MOS read only memory has been programmed to convert the 12 line Hollerith Code to the 8 line EBCDIC Code. Three TTL 4-input NAND gates and three TTL inverters are used to compress the 12 Hollerith lines to eight line binary encoded form suitable for use by the ROM.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 data sheet.

typical application

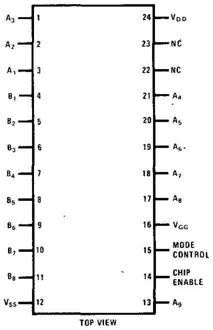
Hollerith to EBCDIC



NOTES
1. V_{SS} = +12.0V ± 10%, V_{DD} = GND, V_{GG} = −12.0V ± 10%
2. The Hollerith input data (lines 1 through 12) is considered to be from normally open switches returned, in the case of a punched hole, to Ground as shown

connection diagram

Dual-In-Line Package



code conversion table

Hollerith to EBCDIC

	12	11	0		12 0	12 11	11 0	12 11 0	12	11	0		12 0	12 11	11 0	12 11 0	
	&	-	ϕ	SP	{	¦	}	70	49	59	69	`	80	90	A0	B0	8-1
1	A	J	/	1	a	j	~	B1	SOH	DC1	21	31	41	51	E1	71	9 -1
2	B	K	S	2	b	k	s	B2	STX	DC2	22	SYN	42	52	62	72	9 -2
3	C	L	T	3	c	l	t	B3	ETX	DC3	23	33	43	53	63	73	9 -3
4	D	M	U	4	d	m	u	B4	04	14	24	34	44	54	64	74	9 -4
5	E	N	V	5	e	n	v	B5	HT	15	LF	35	45	55	65	75	9 -5
6	F	O	W	6	f	o	w	B6	06	BS	ETB	36	46	56	66	76	9 -6
7	G	P	X	7	g	p	x	B7	DEL	17	ESC	EOT	47	57	67	77	9 -7
8	H	Q	Y	8	h	q	y	B8	08	CAN	28	38	48	58	68	78	9 -8
9	I	R	Z	9	i	r	z	B9	09	EM	29	39	NUL	DLE	20	30	9-8-1
8-2	[	]	\		8A	9A	AA	BA	0A	1A	2A	3A	CA	DA	EA	FA	9-8-2
8-3	.	$	,	#	8B	9B	AB	BB	VT	1B	2B	3B	CB	DB	EB	FB	9-8-3
8-4	<	*	%	@	8C	9C	AC	BC	FF	FS	2C	DC4	CC	DC	EC	FC	9-8-4
8-5	(	)	–	'	8D	9D	AD	BD	CR	GS	ENQ	NAK	CD	DD	ED	FD	9-8-5
8-6	+	;	>	=	8E	9E	AE	BE	SO	RS	ACK	3E	CE	DE	EE	FE	9-8-6
8-7	! ①	` ②	?	"	8F	9F	AF	BF	SI	US	BEL	SUB	CF	DF	EF	FF	9-8-7

① may be "|"
② may be "¬"

Note: Unassigned entries e.g. AF refer to the EBCDIC code as a 16 x 16 table, column then row, in hexidecimal notation

Note: The relationship between Hollerith as 256 valid punch combinations and EBCDIC as eight binary digits is well established. This converter conforms to this practice. The assignments shown in the table above are the recommendations of the American National Standards Institute. For details on alternate non-alphanumeric graphic and control codes, see ANSI x 3.26 – 1970

ROM Code Converters

MM4230QX/MM5230QX

EBCDIC-8-to-ASCII-8 code converter

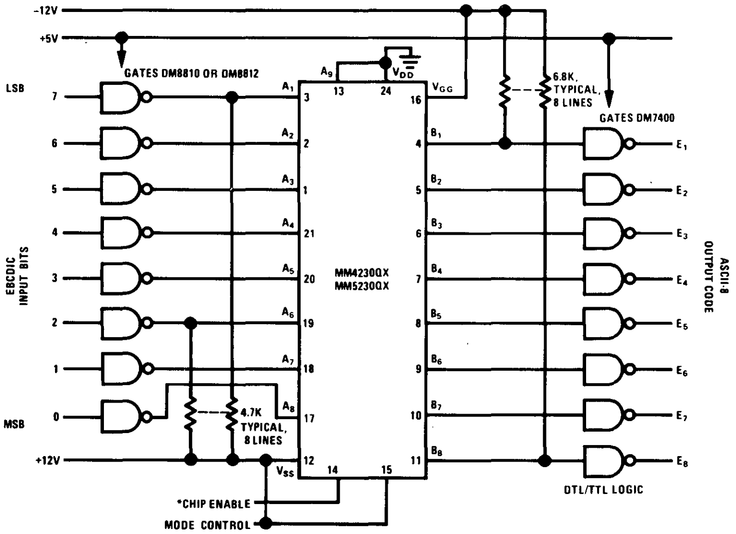
general description

The MM4230QX/MM5230QX is a 2048-bit read only memory that has been programmed to convert Extended Binary Coded Decimal Interchange Code (EBCDIC) to the American Standard Code for Information Interchange extended to eight bits (ASCII-8).

The conversion conforms to the practice established by the American National Standard ANSIx 3.26—1970. Exact details are shown in the code table.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 2048-bit read only memory data sheet.

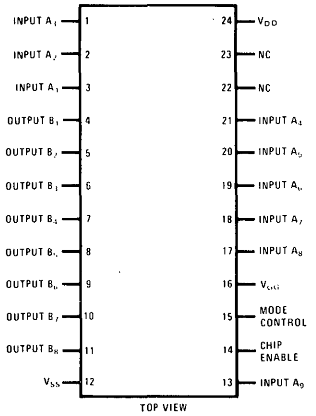
typical application



Logic Levels
DTL/TTL (except at MOS/ROM interface)
Logic "1", +5V, nom. Logic "0", ground, nom.
MOS/ROM Inputs & Output
Logic "1", more negative. Logic "0", more positive

*Chip Enable = Logic "1" to obtain outputs

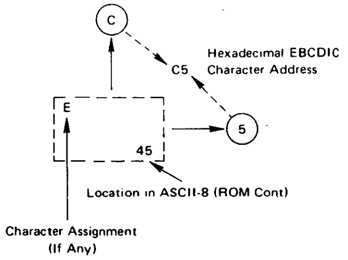
connection diagram



TOP VIEW

code conversion table

4 5 6 7	Column → Row ↓	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
	0 → 1 → 2 → 3 →	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1	
0 0 0 0	0	NUL 00	DLE 10	80	90	SP 20	& 26	– 2D	BA	C3	CA	D1	D8	{ 7B	} 7D	\ 5C	0 30	0
0 0 0 1	1	SOH 01	DC1 11	81	91	A0	A9	/ 2F	BB	a 61	j 6A	~ 7E	D9	A 41	J 4A	9F	1 31	1
0 0 1 0	2	STX 02	DC2 12	82	SYN 16	A1	AA	B2	BC	b 62	k 6B	s 73	DA	B 42	K 4B	S 53	2 32	2
0 0 1 1	3	ETX 03	DC3 13	83	93	A2	AB	B3	BD	c 63	l 6C	t 74	DB	C 43	L 4C	T 54	3 33	3
0 1 0 0	4	9C	9D	84	94	A3	AC	B4	BE	d 64	m 6D	u 75	DC	D 44	M 4D	U 55	4 34	4
0 1 0 1	5	HT 09	85	LF 0A	95	A4	AD	B5	BF	e 65	n 6E	v 76	DD	E 45	N 4E	V 56	5 35	5
0 1 1 0	6	86	BS 08	ETB 17	96	A5	AE	B6	C0	f 66	o 6F	w 77	DE	F 46	O 4F	W 57	6 36	6
0 1 1 1	7	DEL 7F	87	ESC 1B	EOT 04	A6	AF	B7	C1	h 67	p 70	x 78	DF	G 47	P 50	X 58	7 37	7
1 0 0 0	8	97	CAN 18	88	98	A7	B0	B8	C2	i 68	q 71	y 79	E0	H 48	Q 51	Y 59	8 38	8
1 0 0 1	9	8D	EM 19	89	99	A8	B1	B9	` 60	i 69	r 72	z 7A	E1	I 49	R 52	Z 5A	9 39	9
1 0 1 0	A	8E	92	8A	9A	[5B	] 5D	¦ 7C	: 3A	C4	CB	D2	E2	E8	EE	F4	FA	A
1 0 1 1	B	VT 0B	8F	8B	9B	. 2E	$ 24	, 2C	# 23	C5	CC	D3	E3	E9	EF	F5	FB	B
1 1 0 0	C	FF 0C	FS 1C	8C	DC4 14	< 3C	* 2A	% 25	@ 40	C6	CD	D4	E4	EA	F0	F6	FC	C
1 1 0 1	D	CR 0D	GS 1D	ENQ 05	NAK 15	(28	) 29	_ 5F	' 27	C7	CE	D5	E5	EB	F1	F7	FD	D
1 1 1 0	E	SO 0E	RS 1E	ACK 06	9E	+ 2B	; 3B	> 3E	= 3D	C8	CF	D6	E6	EC	F2	F8	FE	E
1 1 1 1	F	SI 0F	US 1F	BEL 07	SUB 1A	! 21	∧ 5E	? 3F	" 22	C9	D0	D7	E7	ED	F3	F9	E0 FF	F



ROM Code Converters

MM4230QY/MM5230QY

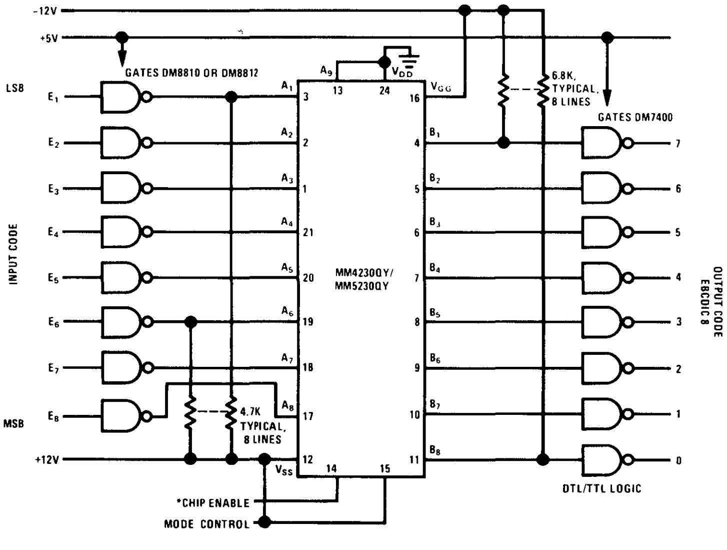
ASCII-8 -to- EBCDIC-8 code converter

general description

The MM4230QY/MM5230QY is a 2048-bit read only memory that has been programmed to convert the American Standard Code for Information Interchange extended to eight bits, (ASCII-8) to Extended Binary Coded Decimal Interchange Code (EBCDIC-8). The conversion conforms to the practice established by the American National Standard ANSIx3.26 1970. Exact details are shown in the code table.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 2048-bit read only memory data sheet.

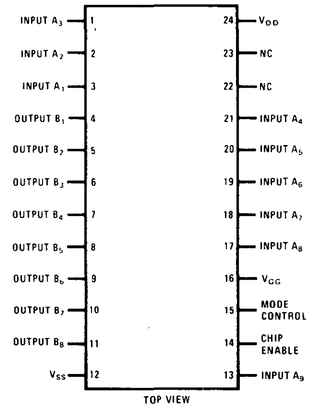
typical application



Logic Levels
DTL/TTL (except at MOS/ROM interface)
Logic "1", +5V, nom. Logic "0", ground, nom.
MOS/ROM Inputs & Output
Logic "1", more negative. Logic "0", more positive

*Chip Enable = Logic "1" to obtain outputs

connection diagram



code conversion table

	b8 → 0		0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
	b7 → 0		0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	
	b6 → 0		0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	
	b5 → 0		1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
b4 b3 b2 b1	Column → Row ↓	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	Column ← Row ↓
0 0 0 0	0	NUL 00	DLE 10	SP 40	0 0 F0	@ 7C	P D7	\ 79	p 97	20	30	41	58	76	9F	B8	DC	0
0 0 0 1	1	SOH 01	DC1 11	! ① 4F	1 F1	A C1	Q D8	a 81	q 98	21	31	42	59	77	AO	B9	DD	1
0 0 1 0	2	STX 02	DC2 12	" 7F	2 F2	B C2	R D9	b 82	r 99	22	1A	43	62	78	AA	BA	DE	2
0 0 1 1	3	ETX 03	DC3 13	# 7B	3 F3	C C3	S E2	c 83	s A2	23	33	44	63	80	AB	BB	DF	3
0 1 0 0	4	ECT 37	DC4 3C	$ 5B	4 F4	D C4	T E3	d 84	t A3	24	34	45	64	8A	AC	BC	EA	4
0 1 0 1	5	ENQ 2D	NAK 3D	% 6C	5 F5	E C5	U E4	e 85	u A4	15	35	46	65	8B	AD	BD	EB	5
0 1 1 0	6	ACK 2E	SYN 32	& 50	6 F6	F C6	V E5	f 86	v A5	06	36	47	66	8C	AE	BE	EC	6
0 1 1 1	7	BEL 2F	ETB 26	' 7D	7 F7	G C7	W E6	g 87	w A6	17	08	48	67	8D	AF	BF	ED	7
1 0 0 0	8	BS 16	CAN 18	(4D	8 F8	H C8	X E7	h 88	x A7	28	38	49	68	8E	B0	CA	EE	8
1 0 0 1	9	HT 05	EM 19	) 5D	9 F9	I C9	Y E8	i 89	y A8	29	39	51	69	8F	B1	CB	EF	9
1 0 1 0	A	IF 25	SUB 3F	* 5C	: 7A	J D1	Z E9	j 91	z A9	2A	3A	52	70	90	B2	CC	FA	10
1 0 1 1	B	VT OB	ESC 27	+ 4E	; 5E	K D2	[4A	k 92	} CO	2B	3B	53	71	9A	B3	CD	FB	11
1 1 0 0	C	FF OC	FS 1C	, 6B	< 4C	L D3	\ E0	l 93	¦ 6A	2C	04	54	72	9B	B4	CE	FC	12
1 1 0 1	D	CR OD	GS 1D	– 60	= 7E	M D4	] 5A	m 94	{ D0	09	14	55	73	9C	B5	CF	FD	13
1 1 1 0	E	SO OE	RS 1E	. 4B	> 6E	N D5	∧② 5F	n 95	~ A1	0A	3E	56	74	9D	B6	DA	FE	14
1 1 1 1	F	SI OF	US 1F	/ 61	? 6F	O D6	– 6D	o 96	DEL 07	1B	E1	57	75	9E	B7	DB	EO FF	15

1 may be "1"

2 may be "¬"

3 The top line in each entry to the table represents an assigned character (Columns 0 to 7). The bottom line in each entry is the corresponding EBCDIC Code, in hexadecimal notation.

The hexadecimal EBCDIC entry is formed thus:

Eight EBCDIC bits

$$\text{MSB}\ \underbrace{0\ 1\ 2\ 3}_{\text{1st Digit}}\ \ \underbrace{4\ 5\ 6\ 7}_{\text{2nd Digit}}\ \text{LSB}$$

$$\text{Example: } \underbrace{0\ 1\ 0\ 1}_{5}\ \ \underbrace{1\ 1\ 0\ 0}_{C}\ \text{ or } *$$

To convert ASCII-8 asterisk (*) to EBCDIC-8
E_8 E_1
* in ASCII is a 2A or binary 0010 1010
applying this as an address to the MM5230QY/MM4230QY
bit-0 bit-7
gives the output 0101 1100, which is an EBCDIC-8 asterisk.

ROM Code Converters

MM4230RS/MM5230RS binary to modulo-n divider code converter

general description

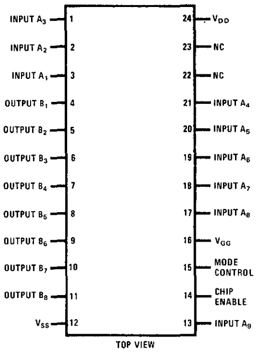
The MM4230RS/MM5230RS binary to modulo-n divider code converter is set up to generate the program input settings for a pair of DM7520/DM8520 modulo-n dividers, in order to divide by any binary number from one to 255. Detailed instructions for use of the DM7520/DM8520 are given in its data sheet.

Applying the required division ratio, in binary, to the inputs of the ROM as shown, generates two sets of four program inputs, one for each of the 2 DM7520/DM8520 dividers.

For electrical, environmental and mechanical details, refer to the MM4230/MM5230 data sheet.

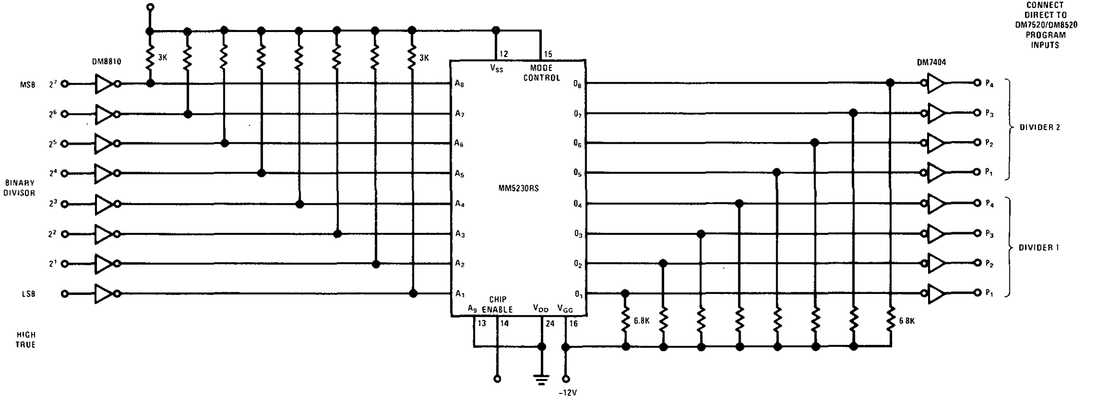
connection diagram

Dual-In-Line Package



typical application

Binary to Modulo-n Divider



code conversion table

SETTING								÷ BY	SETTING								÷ BY	SETTING								÷ BY
DIVIDER 1				DIVIDER 2					DIVIDER 1				DIVIDER 2					DIVIDER 1				DIVIDER 2				
B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1		B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1		B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1	
0	1	1	1	1	1	1	1	255	1	0	1	1	0	1	1	0	165	1	1	1	0	0	1	1	1	75
1	0	1	1	1	1	1	1	254	0	1	0	1	1	0	1	1	164	1	1	1	1	0	0	1	1	74
0	1	0	1	1	1	1	1	253	0	0	1	0	1	1	0	1	163	1	1	1	1	1	0	0	1	73
0	0	1	0	1	1	1	1	252	1	0	0	1	0	1	1	0	162	0	1	1	1	1	1	0	0	72
1	0	0	1	0	1	1	1	251	1	1	0	0	1	0	1	1	161	0	0	1	1	1	1	1	0	71
0	1	0	0	1	0	1	1	250	1	1	1	0	0	1	0	1	160	0	0	0	1	1	1	1	1	70
0	0	1	0	0	1	0	1	249	1	1	1	1	0	0	1	0	159	0	0	0	0	1	1	1	1	69
0	0	0	1	0	0	1	0	248	0	1	1	1	1	0	0	1	158	0	0	0	0	0	1	1	1	68
0	0	0	0	1	0	0	1	247	1	0	1	1	1	1	0	0	157	1	0	0	0	0	0	1	1	67
0	0	0	0	0	1	0	0	246	1	1	0	1	1	1	1	0	156	0	1	0	0	0	0	0	1	66
0	0	0	0	0	0	1	0	245	0	1	1	0	1	1	1	1	155	1	0	1	0	0	0	0	0	65
0	0	0	0	0	0	0	1	244	1	0	1	1	0	1	1	1	154	0	1	0	1	0	0	0	0	64
1	0	0	0	0	0	0	0	243	1	1	0	1	1	0	1	1	153	0	0	1	0	1	0	0	0	63
1	1	0	0	0	0	0	0	242	1	1	1	0	1	1	0	1	152	0	0	0	1	0	1	0	0	62
1	1	1	0	0	0	0	0	241	0	1	1	1	0	1	1	0	151	0	0	0	0	1	0	1	0	61
0	1	1	1	0	0	0	0	240	1	0	1	1	1	0	1	1	150	1	0	0	0	0	1	0	1	60
1	0	1	1	1	0	0	0	239	0	1	0	1	1	1	0	1	149	0	1	0	0	0	0	1	0	59
1	1	0	1	1	1	0	0	238	0	0	1	0	1	1	1	0	148	0	0	1	0	0	0	0	1	58
0	1	1	0	1	1	1	0	237	0	0	0	1	0	1	1	1	147	0	0	0	1	0	0	0	0	57
0	0	1	1	0	1	1	1	236	1	0	0	0	1	0	1	1	146	0	0	0	0	1	0	0	0	56
0	0	0	1	1	0	1	1	235	1	1	0	0	0	1	0	1	145	1	0	0	0	0	1	0	0	55
0	0	0	0	1	1	0	1	234	0	1	1	0	0	0	1	0	144	1	1	0	0	0	0	1	0	54
0	0	0	0	0	1	1	0	233	1	0	1	1	0	0	0	1	143	1	1	1	0	0	0	0	1	53
0	0	0	0	0	0	1	1	232	1	1	0	1	1	0	0	0	142	1	1	1	1	0	0	0	0	52
1	0	0	0	0	0	0	1	231	0	1	1	0	1	1	0	0	141	0	1	1	1	1	0	0	0	51
0	1	0	0	0	0	0	0	230	0	0	1	1	0	1	1	0	140	0	0	1	1	1	1	0	0	50
0	0	1	0	0	0	0	0	229	1	0	0	1	1	0	1	1	139	0	0	0	1	1	1	1	0	49
1	0	0	1	0	0	0	0	228	1	1	0	0	1	1	0	1	138	1	0	0	0	1	1	1	1	48
1	1	0	0	1	0	0	0	227	1	1	1	0	0	1	1	0	137	1	1	0	0	0	1	1	1	47
0	1	1	0	0	1	0	0	226	0	1	1	1	0	0	1	1	136	0	1	1	0	0	0	1	1	46
1	0	1	1	0	0	1	0	225	0	0	1	1	1	0	0	1	135	0	0	1	1	0	0	0	1	45
0	1	0	1	1	0	0	1	224	1	0	0	1	1	1	0	0	134	0	0	0	1	1	0	0	0	44
0	0	1	0	1	1	0	0	223	0	1	0	0	1	1	1	0	133	1	0	0	0	1	1	0	0	43
0	0	0	1	0	1	1	0	222	1	0	1	0	0	1	1	1	132	0	1	0	0	0	1	1	0	42
0	0	0	0	1	0	1	1	221	1	1	0	1	0	0	1	1	131	0	0	1	0	0	0	1	1	41
0	0	0	0	0	1	0	1	220	0	1	1	0	1	0	0	1	130	0	0	0	1	0	0	0	1	40
1	0	0	0	0	0	1	0	219	1	0	1	1	0	1	0	0	129	1	0	0	0	1	0	0	0	39
1	1	0	0	0	0	0	1	218	0	1	0	1	1	0	1	0	128	0	1	0	0	0	1	0	0	38
0	1	1	0	0	0	0	0	217	1	0	1	0	1	1	0	1	127	0	0	1	0	0	0	1	0	37
1	0	1	1	0	0	0	0	216	0	1	0	1	0	1	1	0	126	1	0	0	1	0	0	0	1	36
0	1	0	1	1	0	0	0	215	0	0	1	0	1	0	1	1	125	0	1	0	0	1	0	0	0	35
1	0	1	0	1	1	0	0	214	1	0	0	1	0	1	0	1	124	1	0	1	0	0	1	0	0	34
1	1	0	1	0	1	1	0	213	0	1	0	0	1	0	1	0	123	0	1	0	1	0	0	1	0	33
1	1	1	0	1	0	1	1	212	1	0	1	0	0	1	0	1	122	0	0	1	0	1	0	0	1	32
0	1	1	1	0	1	0	1	211	1	1	0	1	0	0	1	0	121	1	0	0	1	0	1	0	0	31
0	0	1	1	1	0	1	0	210	1	1	1	0	1	0	0	1	120	1	1	0	0	1	0	1	0	30
0	0	0	1	1	1	0	1	209	0	1	1	1	0	1	0	0	119	0	1	1	0	0	1	0	1	29
0	0	0	0	1	1	1	0	208	1	0	1	1	1	0	1	0	118	0	0	1	1	0	0	1	0	28
1	0	0	0	0	1	1	1	207	1	1	0	1	1	1	0	1	117	1	0	0	1	1	0	0	1	27
0	1	0	0	0	0	1	1	206	1	1	1	0	1	1	1	0	116	1	1	0	0	1	1	0	0	26
1	0	1	0	0	0	0	1	205	1	1	1	1	0	1	1	1	115	0	1	1	0	0	1	1	0	25
1	1	0	1	0	0	0	0	204	1	1	1	1	1	0	1	1	114	1	0	1	1	0	0	1	1	24
1	1	1	0	1	0	0	0	203	0	1	1	1	1	1	0	1	113	1	1	0	1	1	0	0	1	23
1	1	1	1	0	1	0	0	202	1	0	1	1	1	1	1	0	112	1	1	1	0	1	1	0	0	22
0	1	1	1	1	0	1	0	201	1	1	0	1	1	1	1	1	111	1	1	1	1	0	1	1	0	21
0	0	1	1	1	1	0	1	200	1	1	1	0	1	1	1	1	110	0	1	1	1	1	0	1	1	20
1	0	0	1	1	1	1	0	199	0	1	1	1	0	1	1	1	109	1	0	1	1	1	1	0	1	19
0	1	0	0	1	1	1	1	198	0	0	1	1	1	0	1	1	108	0	1	0	1	1	1	1	0	18
0	0	1	0	0	1	1	1	197	1	0	0	1	1	1	0	1	107	1	0	1	0	1	1	1	1	17
0	0	0	1	0	0	1	1	196	1	1	0	0	1	1	1	0	106	0	1	0	1	0	1	1	1	16
1	0	0	0	1	0	0	1	195	0	1	1	0	0	1	1	1	105	1	0	1	0	1	0	1	1	15
1	1	0	0	0	1	0	0	194	0	0	1	1	0	0	1	1	104	0	1	0	1	0	1	0	1	14
1	1	1	0	0	0	1	0	193	0	0	0	1	1	0	0	1	103	1	0	1	0	1	0	1	0	13
0	1	1	1	0	0	0	1	192	0	0	0	0	1	1	0	0	102	1	1	0	1	0	1	0	1	12
0	0	1	1	1	0	0	0	191	1	0	0	0	0	1	1	0	101	0	1	1	0	1	0	1	0	11
0	0	0	1	1	1	0	0	190	1	1	0	0	0	0	1	1	100	0	0	1	1	0	1	0	1	10
1	0	0	0	1	1	1	0	189	0	1	1	0	0	0	0	1	99	0	0	0	1	1	0	1	0	9
0	1	0	0	0	1	1	1	188	0	0	1	1	0	0	0	0	98	1	0	0	0	1	1	0	1	8
1	0	1	0	0	0	1	1	187	1	0	0	1	1	0	0	0	97	1	1	0	0	0	1	1	0	7
1	1	0	1	0	0	0	1	186	0	1	0	0	1	1	0	0	96	1	1	1	0	0	0	1	1	6
0	1	1	0	1	0	0	0	185	1	0	1	0	0	1	1	0	95	1	1	1	1	0	0	0	1	5
0	0	1	1	0	1	0	0	184	0	1	0	1	0	0	1	1	94	1	1	1	1	1	0	0	0	4
1	0	0	1	1	0	1	0	183	1	0	1	0	1	0	0	1	93	1	1	1	1	1	1	0	0	3
0	1	0	0	1	1	0	1	182	0	1	0	1	0	1	0	0	92	1	1	1	1	1	1	1	0	2
0	0	1	0	0	1	1	0	181	0	0	1	0	1	0	1	0	91									
1	0	0	1	0	0	1	1	180	0	0	0	1	0	1	0	1	90									
0	1	0	0	1	0	0	1	179	1	0	0	0	1	0	1	0	89									
0	0	1	0	0	1	0	0	178	0	1	0	0	0	1	0	1	88									
1	0	0	1	0	0	1	0	177	1	0	1	0	0	0	1	0	87									
1	1	0	0	1	0	0	1	176	0	1	0	1	0	0	0	1	86									
1	1	1	0	0	1	0	0	175	1	0	1	0	1	0	0	0	85									
0	1	1	1	0	0	1	0	174	1	1	0	1	0	1	0	0	84									
1	0	1	1	1	0	0	1	173	1	1	1	0	1	0	1	0	83									
0	1	0	1	1	1	0	0	172	1	1	1	1	0	1	0	1	82									
1	0	1	0	1	1	1	0	171	1	1	1	1	1	0	1	0	81									
1	1	0	1	0	1	1	1	170	1	1	1	1	1	1	0	1	80									
0	1	1	0	1	0	1	1	169	0	1	1	1	1	1	1	0	79									
1	0	1	1	0	1	0	1	168	0	0	1	1	1	1	1	1	78									
1	1	0	1	1	0	1	0	167	1	0	0	1	1	1	1	1	77									
0	1	1	0	1	1	0	1	166	1	1	0	0	1	1	1	0	76									

ROM Code Converters

MM4231RP/MM5231RP EBCDIC to ASCII-7 code converter

general description

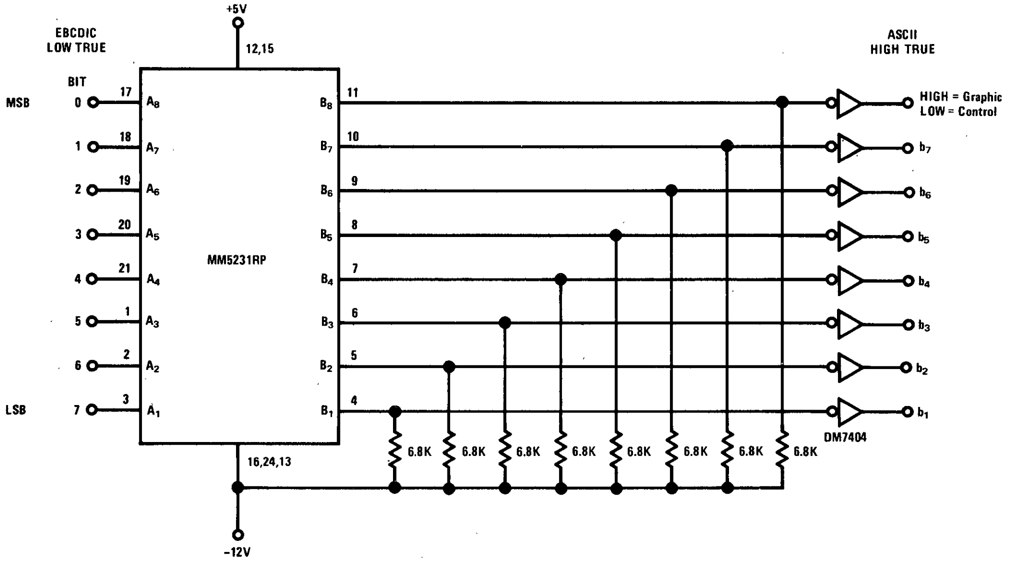
The MM4231RP/MM5231RP is a 2048-bit read-only memory that has been programmed to convert from EBCDIC, an extended binary coded decimal interchange code used in the IBM1130 computer, to ASCII-7, the American Standard Code for Information Interchange in seven bits.

This conversion differs from the ANSI x 3.26 conversion of the MM4230QX/MM5230QX in that it follows certain earlier IBM1130 character assignments. Also certain EBCDIC control codes are arbitrarily preserved and translated (see translation chart on truth table).

For electrical, environmental and mechanical details, refer to the MM4231/MM5231 data sheet.

typical application

EBCDIC TO ASCII-7



code conversion tables

ROM ADDRESS	FUNCTION INPUT EBCDIC SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE INPUT MSB							LSB	CODE OUTPUT CC/G	MSB						LSB
0	NULL	NUL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	SOH	SOH	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
2	STX	STX	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0
3	ETX	ETX	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1
4	PF		0	0	0	0	0	1	0	0								
5	HT	HT									0	0	0	0	1	0	0	1
6	LC																	
7	DEL	DEL									0	1	1	1	1	1	1	1
8																		
9																		
10	SMM																	
11	VT	VT									0	0	0	0	1	0	1	1
12	FF	FF									0	0	0	0	1	1	0	0
13	CR	CR									0	0	0	0	1	1	0	1
14	S0	S0									0	0	0	0	1	1	1	0
15	S1	S1									0	0	0	0	1	1	1	1
16	DLE	DLE									0	0	0	1	0	0	0	0
17	DC1	DC1									0	0	0	1	0	0	0	1
18	DC2	DC2									0	0	0	1	0	0	1	0
19	DC3	DC3									0	0	0	1	0	0	1	1
20	RES	`									1	1	1	0	0	0	0	0
21	NL	\									1	1	0	1	1	1	0	0
22	BS	BS									0	0	0	0	1	0	0	0
23	IDL																	
24	CAN	CAN									0	0	0	1	1	0	0	0
25	EM	EM									0	0	0	1	1	0	0	1
26	CC																	
27	CUI																	
28	FLS	FS									0	0	0	1	1	1	0	0
29	GS	GS									0	0	0	1	1	1	0	1
30	RDS	RS									0	0	0	1	1	1	1	0
31	US	US									0	0	0	1	1	1	1	1
32	DS																	
33	SOS																	
34	FS		CONTINUING BINARY SEQUENCE															
35																		
36	BYP										0	0	0	0	0	0	0	0
37	LF	LF									0	0	0	0	1	0	1	0
38	EOB	ETB									0	0	0	1	0	1	1	1
39	PRE	ESC									0	0	0	1	1	0	1	1
40																		
41																		
42	SM																	
43	CU2																	
44																		
45	ENQ	ENQ									0	0	0	0	0	1	0	1
46	ACK	ACK									0	0	0	0	0	1	1	0
47	BEL	BEL									0	0	0	0	0	1	1	1
48																		
49																		
50	SYN	SYN									0	0	0	1	0	1	1	0
51																		
52	PN																	
53	RS	DC4									0	0	0	1	0	1	0	0
54	UC																	
55	EOT	EOT									0	0	0	0	0	1	0	0
56																		
57																		
58																		
59	CU3																	
60	DCA																	
61	NAK	NAK									0	0	0	1	0	1	0	1
62																		
63	SUB	SUB									0	0	0	1	1	0	1	0
			A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

ROM ADDRESS	FUNCTION INPUT EBCDIC SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE INPUT MSB							LSB	CODE OUTPUT CC/G	MSB						LSB
128																		
129	a	a									1	1	1	0	0	0	0	1
130	b	b									1	1	1	0	0	0	1	0
131	c	c									1	1	1	0	0	0	1	1
132	d	d									1	1	1	0	0	1	0	0
133	e	e									1	1	1	0	0	1	0	1
134	f	f									1	1	1	0	0	1	1	0
135	g	g									1	1	1	0	0	1	1	1
136	h	h									1	1	1	0	1	0	0	0
137	i	i									1	1	1	0	1	0	0	1
138																		
139	{	{									1	1	1	1	1	0	1	1
140																		
141																		
142																		
143																		
144																		
145	j	j									1	1	1	0	1	0	1	0
146	k	k									1	1	1	0	1	0	1	1
147	l	l									1	1	1	0	1	1	0	0
148	m	m									1	1	1	0	1	1	0	1
149	n	n									1	1	1	0	1	1	1	0
150	o	o									1	1	1	0	1	1	1	1
151	p	p									1	1	1	1	0	0	0	0
152	q	q									1	1	1	1	0	0	0	1
153	r	r									1	1	1	1	0	0	1	0
154																		
155	}	}									1	1	1	1	1	1	0	1
156																		
157																		
158			CONTINUING BINARY SEQUENCE															
159																		
160																		
161																		
162	s	s									1	1	1	1	0	0	1	1
163	t	t									1	1	1	1	0	1	0	0
164	u	u									1	1	1	1	0	1	0	1
165	v	v									1	1	1	1	0	1	1	0
166	w	w									1	1	1	1	0	1	1	1
167	x	x									1	1	1	1	1	0	0	0
168	y	y									1	1	1	1	1	0	0	1
169	z	z									1	1	1	1	1	0	1	0
170																		
171																		
172																		
173	[	[									1	1	0	1	1	0	1	1
174																		
175																		
176																		
177																		
178																		
179																		
180																		
181																		
182																		
183																		
184																		
185																		
186																		
187																		
188																		
189	]	]									1	1	0	1	1	1	0	1
190																		
191																		
			A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

ROM ADDRESS	FUNCTION INPUT EBCDIC SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE INPUT MSB							LSB	CODE OUTPUT CC/G	MSB						LSB
64	SP	SP									1	0	1	0	0	0	0	0
65																		
66																		
67																		
68																		
69																		
70																		
71																		
72																		
73																		
74	¢	~									1	1	1	1	1	1	1	0
75											1	0	1	0	1	1	1	0
76	<	<									1	0	1	1	1	1	0	0
77	(	(									1	0	1	0	1	0	0	0
78	+	+									1	0	1	0	1	0	1	1
79	¦	¦									1	1	1	1	1	1	0	0
80	&	&									1	0	1	0	0	1	1	0
81																		
82																		
83																		
84																		
85																		
86																		
87																		
88																		
89																		
90	!	!									1	0	1	0	0	0	0	1
91	$	$									1	0	1	0	0	1	0	0
92	*	*									1	0	1	0	1	0	1	0
93	)	)									1	0	1	0	1	0	0	1
94		;	CONTINUING BINARY SEQUENCE								1	0	1	1	1	0	1	1
95	¬	^									1	1	0	1	1	1	1	0
96		-									1	0	1	0	1	1	0	1
97	/										1	0	1	0	1	1	1	1
98																		
99																		
100																		
101																		
102																		
103																		
104																		
105																		
106																		
107	,	,									1	0	1	0	1	1	0	0
108	%	%									1	0	1	0	0	1	0	1
109	—	—									1	1	0	1	1	1	1	1
110	>	>									1	0	1	1	1	1	1	0
111	?	?									1	0	1	1	1	1	1	1
112																		
113																		
114																		
115																		
116																		
117																		
118																		
119																		
120																		
121																		
122											1	0	1	1	1	0	1	0
123	#	#									1	0	1	0	0	0	1	1
124	@	@									1	1	0	0	0	0	0	0
125	'	'									1	0	1	0	0	1	1	1
126	=	=									1	0	1	1	1	1	0	1
127	"	"									1	0	1	0	0	0	1	0
			A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

ROM ADDRESS	FUNCTION INPUT EBCDIC SYMBOL	FUNCTION OUTPUT ASCII SYMBOL	CODE INPUT MSB							LSB	CODE OUTPUT CC/G	MSB						LSB
192	+ZERO																	
193	A	A									1	1	0	0	0	0	0	1
194	B	B									1	1	0	0	0	0	1	0
195	C	C									1	1	0	0	0	0	1	1
196	D	D									1	1	0	0	0	1	0	0
197	E	E									1	1	0	0	0	1	0	1
198	F	F									1	1	0	0	0	1	1	0
199	G	G									1	1	0	0	0	1	1	1
200	H	H									1	1	0	0	1	0	0	0
201	I	I									1	1	0	0	1	0	0	1
202																		
203																		
204																		
205																		
206																		
207																		
208	-ZERO																	
209	J	J									1	1	0	0	1	0	1	0
210	K	K									1	1	0	0	1	0	1	1
211	L	L									1	1	0	0	1	1	0	0
212	M	M									1	1	0	0	1	1	0	1
213	N	N									1	1	0	0	1	1	1	0
214	O	O									1	1	0	0	1	1	1	1
215	P	P									1	1	0	1	0	0	0	0
216	Q	Q									1	1	0	1	0	0	0	1
217	R	R									1	1	0	1	0	0	1	0
218																		
219																		
220																		
221																		
222			CONTINUING BINARY SEQUENCE															
223																		
224																		
225																		
226	S	S									1	1	0	1	0	0	1	1
227	T	T									1	1	0	1	0	1	0	0
228	U	U									1	1	0	1	0	1	0	1
229	V	V									1	1	0	1	0	1	1	0
230	W	W									1	1	0	1	0	1	1	1
231	X	X									1	1	0	1	1	0	0	0
232	Y	Y									1	1	0	1	1	0	0	1
233	Z	Z									1	1	0	1	1	0	1	0
234																		
235																		
236																		
237																		
238																		
239																		
240	0	0									1	0	1	1	0	0	0	0
241	1	1									1	0	1	1	0	0	0	1
242	2	2									1	0	1	1	0	0	1	0
243	3	3									1	0	1	1	0	0	1	1
244	4	4									1	0	1	1	0	1	0	0
245	5	5									1	0	1	1	0	1	0	1
246	6	6									1	0	1	1	0	1	1	0
247	7	7									1	0	1	1	0	1	1	1
248	8	8									1	0	1	1	1	0	0	0
249	9	9									1	0	1	1	1	0	0	1
250																		
251			1	1	1	1	1	0	1	1								
252			1	1	1	1	1	1	0	0								
253			1	1	1	1	1	1	0	1								
254			1	1	1	1	1	1	1	0								
255			1	1	1	1	1	1	1	1								
			A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	B_8	B_7	B_6	B_5	B_4	B_3	B_2	B_1

ROM Code Converters

DM5488/DM7488 (SN5488/SN7488)

256-bit read-only memory

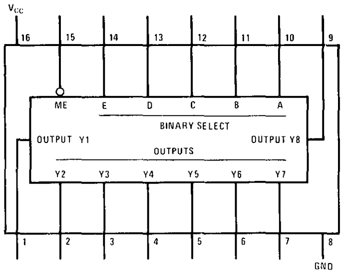
general description

The DM5488/DM7488 is a custom-programmed 256-bit read-only memory organized as 32 8-bit words. A 5-bit input code selects the appropriate word which then appears on the eight outputs. An enable input overrides the address inputs and turns off all eight output transistors.

features

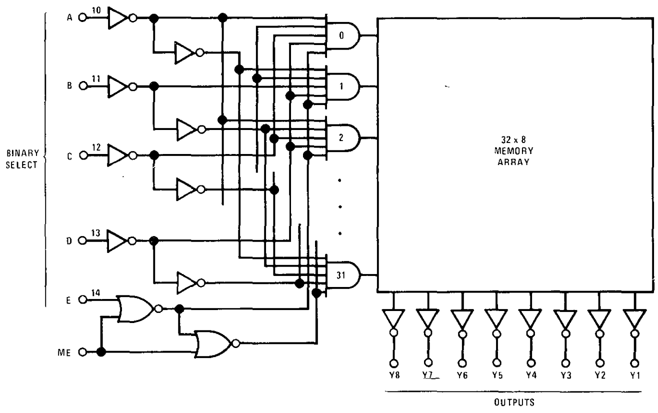
- Organized as 32 8-bit words
- Open collector outputs provide expansion to greater numbers of words
- On-chip decoding
- 30 ns typical access time
- 250 mW typical power dissipation
- Input clamp diodes

connection diagram



TOP VIEW

typical application



absolute maximum ratings (Note 1)

Supply Voltage		7V
Input Voltage		5.5V
Output Voltage		5.5V
Operating Temperature Range	DM5488	-55°C to +125°C
	DM7488	0°C to +70°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	DM5488	$V_{CC} = 4.5V$		2.0			V
	DM7488	$V_{CC} = 4.75V$					
Logical "0" Input Voltage	DM5488	$V_{CC} = 4.5V$				0.8	V
	DM7488	$V_{CC} = 4.75V$					
Logical "1" Output Current	DM5488	$V_{CC} = 5.5V$	$V_O = 5.5V$			100	μA
	DM7488	$V_{CC} = 5.25V$				40	μA
Logical "0" Output Voltage	DM5488	$V_{CC} = 4.5V$	$I_O = 12$ mA			0.4	V
	DM7488	$V_{CC} = 4.75V$					
Logical "1" Input Current	DM5488	$V_{CC} = 5.5V$	$V_I = 2.4V$			40	μA
	DM7488	$V_{CC} = 5.25V$					
	DM5488	$V_{CC} = 5.5V$	$V_I = 5.5V$			1	mA
	DM7488	$V_{CC} = 5.25V$					
Logical "0" Input Current	DM5488	$V_{CC} = 5.5V$	$V_I = 0.4V$			-1.6	mA
	DM7488	$V_{CC} = 5.25V$					
Supply Current	DM5488	$V_{CC} = 5.5V$			50	80	mA
	DM7488	$V_{CC} = 5.25V$					
Input Clamp Voltage	DM5488	$V_{CC} = 4.5V$	$I_I = -12$ mA			-1.5	V
	DM7488	$V_{CC} = 4.75V$					
Propagation Delay to a Logical "0" from Address to Output, t_{pd0}		$V_{CC} = 5.0V$ $T_A = 25°C$	$C_L = 15$ pF		32	50	ns
Propagation Delay to a Logical "0" from Enable to Output, t_{pd0}		$V_{CC} = 5.0V$ $T_A = 25°C$	$C_L = 15$ pF		34	50	ns
Propagation Delay to a Logical "1" from Address to Output, t_{pd1}		$V_{CC} = 5.0V$ $T_A = 25°C$	$C_L = 15$ pF		28	50	ns
Propagation Delay to a Logical "1" from Enable to Output, t_{pd1}		$V_{CC} = 5.0V$ $T_A = 25°C$	$C_L = 15$ pF		27	50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the -55°C to +125°C temperature range for the DM5488 and across the 0°C to 70°C range for the DM7488. All typicals are given for $V_{CC} = 5.0V$ and $T_A = 25°C$.

truth tables

DM5488A/DM7488A SINE LOOK-UP TABLE

A pattern has been generated for the DM5488/DM7488. The AA pattern provides a sine table. The 5-bit input code linearly divides 90° into 32 equal segments. Each 8-bit output is therefore the sine of the angle applied.

EXAMPLE: Input 11010 means 26/32 of 90°, or about 73°. The corresponding output 11110100 indicates (1/2 + 1/4 + 1/8 + 1/16 + 1/64) or about .95, which is close to the sine of 73°. Rounding-off has not been employed, since without rounding-off it is possible to extend the accuracy with additional ROMs.

INPUTS							OUTPUTS							
WORD	BINARY SELECT					ENABLE								
	E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	1	1	0	0
2	0	0	0	1	0	0	0	0	0	1	1	0	0	1
3	0	0	0	1	1	0	0	0	1	0	0	1	0	1
4	0	0	1	0	0	0	0	0	1	1	0	0	0	1
5	0	0	1	0	1	0	0	0	1	1	1	1	1	0
6	0	0	1	1	0	0	0	1	0	0	1	0	1	0
7	0	0	1	1	1	0	0	1	0	1	0	1	1	0
8	0	1	0	0	0	0	0	1	1	0	0	0	0	1
9	0	1	0	0	1	0	0	1	1	0	1	1	0	1
10	0	1	0	1	0	0	0	1	1	1	1	0	0	0
11	0	1	0	1	1	0	1	0	0	0	0	0	1	1
12	0	1	1	0	0	0	1	0	0	0	1	1	1	0
13	0	1	1	0	1	0	1	0	0	1	1	0	0	0
14	0	1	1	1	0	0	1	0	1	0	0	0	1	0
15	0	1	1	1	1	0	1	0	1	0	1	0	1	1
16	1	0	0	0	0	0	1	0	1	1	0	1	0	1
17	1	0	0	0	1	0	1	0	1	1	1	1	0	1
18	1	0	0	1	0	0	1	1	0	0	0	1	0	1
19	1	0	0	1	1	0	1	1	0	0	1	1	0	1
20	1	0	1	0	0	0	1	1	0	1	0	1	0	0
21	1	0	1	0	1	0	1	1	0	1	1	0	1	1
22	1	0	1	1	0	0	1	1	1	0	0	0	0	1
23	1	0	1	1	1	0	1	1	1	0	0	1	1	1
24	1	1	0	0	0	0	1	1	1	0	1	1	0	0
25	1	1	0	0	1	0	1	1	1	1	0	0	0	1
26	1	1	0	1	0	0	1	1	1	1	0	1	0	0
27	1	1	0	1	1	0	1	1	1	1	1	0	0	0
28	1	1	1	0	0	0	1	1	1	1	1	0	1	1
29	1	1	1	0	1	0	1	1	1	1	1	1	0	1
30	1	1	1	1	0	0	1	1	1	1	1	1	1	0
31	1	1	1	1	1	0	1	1	1	1	1	1	1	1
All	X	X	X	X	X	1	1	1	1	1	1	1	1	1

X Don't Care

DM5488/DM7488 TRUTH TABLE

The output levels are not shown on the truth table since the customer specifies the output condition he desires at each of the eight outputs for each of the 32 words (256 bits). The customer does this by filling out the truth table on this data sheet, and sending it in with his purchase order.

INPUTS							OUTPUTS							
WORD	BINARY SELECT					ENABLE								
	E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	0	0	0	0	0	0								
1	0	0	0	0	1	0								
2	0	0	0	1	0	0								
3	0	0	0	1	1	0								
4	0	0	1	0	0	0								
5	0	0	1	0	1	0								
6	0	0	1	1	0	0								
7	0	0	1	1	1	0								
8	0	1	0	0	0	0								
9	0	1	0	0	1	0								
10	0	1	0	1	0	0								
11	0	1	0	1	1	0								
12	0	1	1	0	0	0								
13	0	1	1	0	1	0								
14	0	1	1	1	0	0								
15	0	1	1	1	1	0								
16	1	0	0	0	0	0								
17	1	0	0	0	1	0								
18	1	0	0	1	0	0								
19	1	0	0	1	1	0								
20	1	0	1	0	0	0								
21	1	0	1	0	1	0								
22	1	0	1	1	0	0								
23	1	0	1	1	1	0								
24	1	1	0	0	0	0								
25	1	1	0	0	1	0								
26	1	1	0	1	0	0								
27	1	1	0	1	1	0								
28	1	1	1	0	0	0								
29	1	1	1	0	1	0								
30	1	1	1	1	0	0								
31	1	1	1	1	1	0								
All	X	X	X	X	X	1	1	1	1	1	1	1	1	1

X = Don't Care

Notice This sheet must be completed and signed by an authorized representative of the customer's company before an order can be entered

To be used by National only

______________ Part Number

______________ S O Number

______________ Date Received

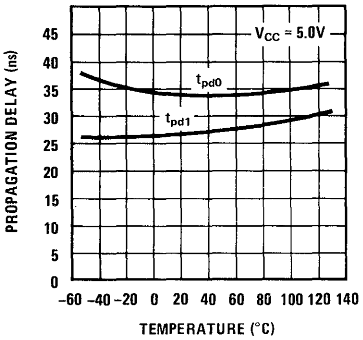
Authorized Representative______________ Date__________

Company______________________________

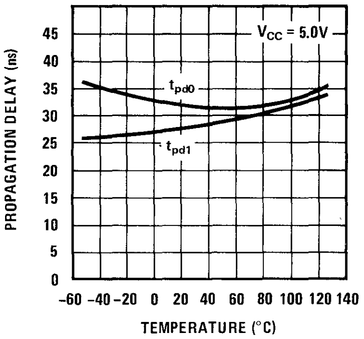
Desired Part ☐ DM5488 ☐ DM7488

typical performance characteristics

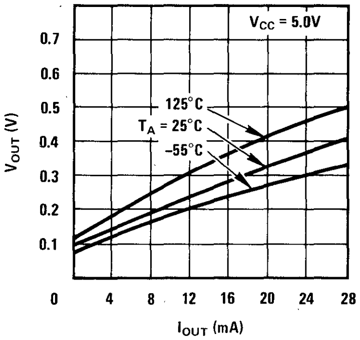
Delay from Enable to Output vs Temperature



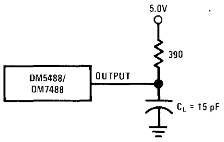
Delay from Address to Output vs Temperature



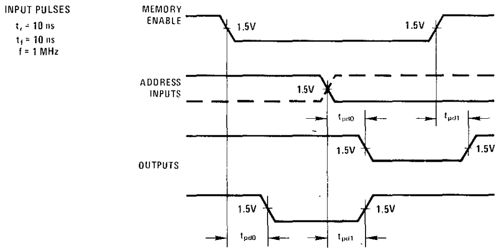
Logical "0" Output Voltage vs Sink Current



ac test circuit



switching time waveforms



ROM Code Converters

DM7598AA/DM8598AA TRI-STATE™ sine table look-up read only memory

general description

The DM7598AA/DM8598AA is a 256-bit bipolar read-only memory organized as 32 8-bit words. The 5-bit input code linearly divides 90° into 32 equal segments. Each 8-bit output is therefore the sine of the angle applies.

EXAMPLE: Input 11010 means 26/32 of 90°, or about 73°. The corresponding output 11110100 indicates (1/2 + 1/4 + 1/8 + 1/16 + 1/64) or about .95, which is close to the sine of 73°. Rounding-off has not been employed, since without rounding-off it is possible to extend the accuracy with additional ROM's.

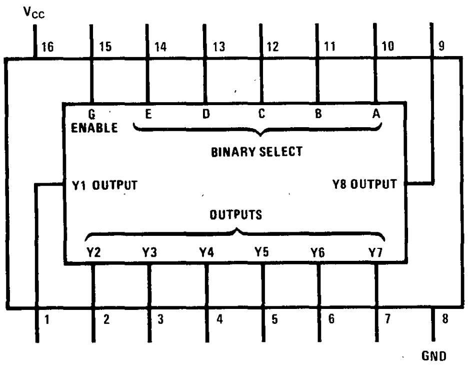
The DM8598 is identical to the SN7488 except that the Enable input on the SN7488 simply places all outputs in the logical "1" state, whereas the Enable input on the DM8598 places the outputs in a high impedance state. This high impedance state allows many outputs to be connected in parallel for expansion to greater numbers of words and/or connection to a common bus line.

features

- Organized as 32 8-bit words
- Party line capability
- On-chip decoding
- Pin compatible with SN7488
- Typical access time 30 ns
- Total power dissipation 350 mW
- Compatible with Series 74 TTL and 930 DTL
- Strobe input
- Input clamp diodes

connection diagram

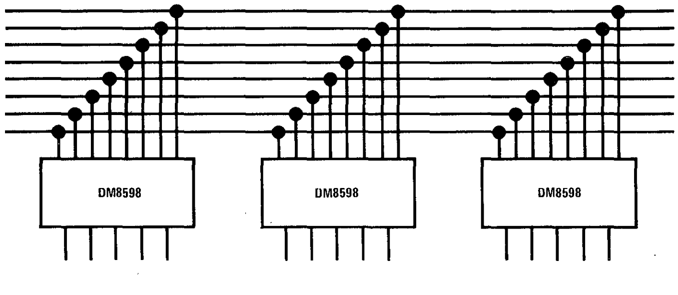
Dual-In-Line Package



TOP VIEW

G ENABLE	OUTPUTS
0	NORMAL
1	Hi-Z

typical system connection



truth table

INPUTS							OUTPUTS							
Word	Binary Select					Enable								
	E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	1	0	0	0	0	0	1	1	0	0
2	0	0	0	1	0	0	0	0	0	1	1	0	0	1
3	0	0	0	1	1	0	0	0	1	0	0	1	0	1
4	0	0	1	0	0	0	0	0	1	1	0	0	0	1
5	0	0	1	0	1	0	0	0	1	1	1	1	1	0
6	0	0	1	1	0	0	0	1	0	0	1	0	1	0
7	0	0	1	1	1	0	0	1	0	1	0	1	1	0
8	0	1	0	0	0	0	0	1	1	0	0	0	0	1
9	0	1	0	0	1	0	0	1	1	0	1	1	0	1
10	0	1	0	1	0	0	0	1	1	1	1	0	0	0
11	0	1	0	1	1	0	1	0	0	0	0	0	1	1
12	0	1	1	0	0	0	1	0	0	0	1	1	1	0
13	0	1	1	0	1	0	1	0	0	1	1	0	0	0
14	0	1	1	1	0	0	1	0	1	0	0	0	1	0
15	0	1	1	1	1	0	1	0	1	0	1	0	1	1
16	1	0	0	0	0	0	1	0	1	1	0	1	0	1
17	1	0	0	0	1	0	1	0	1	1	1	1	0	1
18	1	0	0	1	0	0	1	1	0	0	0	1	0	1
19	1	0	0	1	1	0	1	1	0	0	1	1	0	1
20	1	0	1	0	0	0	1	1	0	1	0	1	0	0
21	1	0	1	0	1	0	1	1	0	1	1	0	1	1
22	1	0	1	1	0	0	1	1	1	0	0	0	0	1
23	1	0	1	1	1	0	1	1	1	0	0	1	1	1
24	1	1	0	0	0	0	1	1	1	0	1	1	0	0
25	1	1	0	0	1	0	1	1	1	1	0	0	0	1
26	1	1	0	1	0	0	1	1	1	1	0	1	0	0
27	1	1	0	1	1	0	1	1	1	1	1	0	0	0
28	1	1	1	0	0	0	1	1	1	1	1	0	1	1
29	1	1	1	0	1	0	1	1	1	1	1	1	0	1
30	1	1	1	1	0	0	1	1	1	1	1	1	1	0
31	1	1	1	1	1	0	1	1	1	1	1	1	1	1
All	X	X	X	X	X	1	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z	HI-Z

Custom MOS/LSI

Custom MOS/LSI Product Flow

CUSTOM DESIGN	Interface between Customer and Design/Production Engineers	Product Definition
CAD SIMULATE	Time Sharing Computer Simulates Static and Dynamic Performance and Worst Case Parameters	Partitioning Simulation
CAD DIGITIZE	Macrodata FEDIS LSI Design System	Drafting Digitizing
CAG	David Mann Reticle Generator	10X Reticle Generation
MASK	David Mann Camera 6-Barrel Step & Repeat	Mask Making (In-House)
FAB	Wafer Fabrication	Volume Wafer Production Santa Clara Facility
ASSY	Assembly	Volume Assembly, Worldwide
TEST	Macrodata J259, J277 100, 230-2 LSI Tester	100% Wafer Probe Test 100% Finished Product Test
QA	Quality Assurance	Internal Spec to MIL-STD 883
REL	Reliability	High Rel Processing Available on all Products
SHIP	Shipping	

INTRODUCTION

While custom and standard MOS have advantages over each other for specific applications, there is a high demand for both in today's electronics industry. In most cases, the true test of whether a system can most economically be implemented with standard, custom, or both, can only be determined after partitioning. If the quantities in question do not exceed a few hundred units per year, the standard product approach is probably the best solution. However, if the total number of units is several thousand per year, then customizing is usually the best approach.

Custom MOS circuits are designed to do a specific job. You are not buying capability that is not needed. The entire chip is devoted to performing your specific function. Advantages are:

1) Fewer Packages
2) Lower Power Dissipation
3) Smaller P.C. Boards
4) Proprietary Design

These advantages result in lower system costs and protection of your system design.

RESOURCES

National has brought together a group of experienced circuit and system designers, separate from the standard product group, to offer a custom MOS/LSI design service to the industry. This group is prepared to aid in the logic design of a system, partition the system into feasible LSI circuits if the design requires more than one chip, develop the chips, assist the customer in prototype system checkout, and put the design into production.

National has one of the most advanced IC manufacturing facilities in the industry. Your custom design will go through the same production facilities where National's standard MOS products are manufactured, and thus benefit from our long experience in MOS processing.

As with its bipolar circuits, the key to National's MOS program is volume production. We are a leading producer of shift registers, read-only memories, and random access memories. In the latter category, National is supplying many second source and proprietary static and dynamic RAMs as well as several advanced large-capacity RAMs. National is also exploring other MOS device applications, such as MAPS (Microprogrammable Arithmetic Processor System). This unit contains five LSI chips which, with very few added parts, can comprise a high sophisticated electronic calculator, an "intelligent" computer terminal, or even a low-cost microprocessor.

National was the first company to offer MOS circuits that operate at voltage levels directly compatible with TTL. (Previously, level-shifters were needed if high-voltage MOS and low-voltage TTL were to work together). To achieve this so-called low-level MOS operation, National pioneered in the fabrication of circuits made from silicon cut along the (1-0-0) axis of the crystal. Subsequently, other companies developed bipolar compatible MOS circuits also. Today, National is investigating a variety of MOS technologies to determine the best process to use a specific function. During the past year, National introduced the silicon gate process to the MOS product line; other technologies such as ion-implantation, N-channel and CMOS are also being investigated. The company will use any available technology as a tool to achieve necessary performance for a given function.

1-0-0 P-channel metal gate and 1-1-1 silicon self-aligned gate enhancement mode MOS technologies are presently utilized by National in our standard MOS products. These processes have become industry standards. All of the P-channel MOS process devices offer bipolar compatibility.

Metal gate devices operate to 3.3 MHz. This technology is well-suited to random logic and ROM applications. Higher logic densities and operating frequencies approaching 10 MHz can be achieved by using silicon gate technology. This process lends itself to RAMs, registers, and random logic applications.

Static and dynamic logic is available in both metal and silicon gate devices (including ion-implants). In general, less power is dissipated if dynamic logic is employed, which also offers the advantage of synchronous operation and eliminates hazards due to race conditions. In any event, power dissipation of typical LSI functions (up to 1000 gate functions) approach 500 mW in devices fabricated with either metal gate or silicon gate technology.

Complementary MOS (CMOS) technology is presently being used on many standard products and will soon be available for custom products. Structured logic, ROMs, RAMs, and registers, designed with CMOS cannot achieve the density of P-channel MOS. However, quiescent power and dissipations are less than one microwatt per gate. Operation to 10 MHz can be achieved. One of the advantages of CMOS is that power dissipation is a function of frequency, with the DC (quiescent) state consuming the least power.

The N-channel process is also undergoing development at National. This process allows higher density and high frequency operation than P-channel. This process is slated for production capability before June 1972.

Ion implantation is a technique that can be applied to any of the previously mentioned processes. It allows threshold voltages to be adjusted to a desired level by implanting ions in the gate region. Depletion load devices and large value ohmic resistors are also being made with ion implantation, which greatly improves packing density on LSI chips.

DESIGN

Your custom design will benefit from National's longtime experience in the MOS business. Extensive use of computer-aided design (CAD) and computer simulation programs assure proper operation of your circuit before it goes into production.

All designs are verified with a circuit analysis program to assure proper operation. Worst case signal paths are checked to see that no signal race conditions exist.

Circuit layouts are performed using both manual and CAD techniques. Manual artwork generation is produced on rubylith cut and peel material. The CAD system bypasses this step entirely and goes directly from a digitized layout to 10X rectícles eliminating the need for rubylith and intermediate reduction steps. National's photomask generation laboratory is one of the best equipped in the industry including the Macrodata FEDIS System, the David Mann Pattern Generator, Reticle Generator, and 6-barrel step and repeat camera.

TESTING

National has a number of LSI testers that allow complete checkout of structured logic (ROMs, RAMs, shift registers, etc.) and random combinational logic. The random logic testers are computer programmed to test to the customer's input/output logic specifications. On-line testers include Teradyne J259, J277, Macrodata 230-2 LSI tester and Macrodata 100 memory system exercisors.

After fabrication, each wafer is checked for threshold voltage, breakdown voltage, oxide rupture and sheet resistivity. The wafer then goes into functional test. The logic on each die is thoroughly exercised. This 100% test of each wafer eliminates any functional defective die from being packaged.

After packaging, all devices are stressed to environmental extremes. The packaged devices are then returned for another functional test. Depending on the customer's requirement, packages can be tested under a variety of environmental conditions and can be subjected to a burn-in cycle. Full MIL-STD 883 processing is offered on all National custom and standard MOS devices.

QUALITY ASSURANCE

National's quality assurance department has a complete and comprehensive quality control program which effectively controls component parts and vendors at a quality level of functional, workmanship and dimensional criteria. The QA program also covers in-process controls of assembled devices, final electrical test, marking and final shipment of approved product. All procedures are documented at specification control and at respective quality inspection stations. Weekly and monthly reports are generated for quick feedback of information for corrective action purposes.

All inspections are performed to specified internal AQL inspection levels which meet or exceed MIL-STD 883.

RELIABILITY

The reliability evaluation program in effect at National is a continuous monitor on the process stability of assembled devices on extended life test. Tests which are performed on a continuous basis on each process are:

(a) High Temperature Operating Life Test (extended life)

(b) High Temperature Storage Test (extended life)

MIL-STD 883, which specifies testing procedures for integrated circuits, was innovatively handled by National. The company adopted 883 specs as its own, rather than to set up one procedure for military orders and another for industrial customers. Therefore, there are no dual standards at National. All devices are given the same quality control treatment and the company inventories devices with guaranteed 883 specs.

All standard devices undergo MIL-STD 883 testing. They are 100% subjected to a temperature cycle per Method 1003 Condition D, fine leak test per Method 1014 Condition A, Helium 5 x 10^{-7}, and gross leak test per Method 1014 Condition C.

The company has been informed by the National Aeronautics and Space Administration that it has received line certification under MIL-M-38510, the new military standard defining acceptable procedures for producing devices.

A customer may request any special rel processing per Document NSC/0002. The intent of this document is to provide the user with the ability to procure any integrated circuit manufactured by National to any class of MIL-STD 883 processing.

PACKAGES

National offers a variety of dual-in-line packages (DIPs), metal cans, flat packs, and specialized packages. Both ceramic and molded packages are available.

All packages meet the standard JEDEC registered outlines. Lead finishes are available in either gold or tin. The ceramic packages meet a leakage of 5 x 10^{-7} std cc He/sec leak rate. National's molded packages are the most advanced in the industry and afford reliability which rivals the ceramic packages.

FACILITIES

In addition to its 150,000-square foot Santa Clara facility, National has operations in Connecticut, Singapore, Hong Kong, Scotland, Germany and Australia totaling over 300,000 square feet. Personnel is presently over 3,000 worldwide.

In Singapore, National completed its 90,000-square foot facility prior to fiscal 1971 but assembly and test functions were substantially expanded during the past year. The Hong Kong plant doubled in size and will again expand in 1972. In Europe, test and warehousing facilities in Scotland and West Germany continued to grow in fiscal 1971 in preparation for future assembly operations. The establishment of NS Electronics Pty. in Australia provides the company with an assembly operation in that part of the world.

Application Notes

JUNE 1970

THE SYSTEMS APPROACH TO CHARACTER GENERATORS

A huge new market for man/machine interfaces is being created by the increasing availability of low cost data processing through computer time sharing, LSI calculators, minicomputers and digital business and control systems. In turn, the pressure is on to design CRT terminals, displays and teleprinters that are at least as compact and inexpensive as the new data processors.

MOS integrated circuit producers are in the thick of this competition. They have begun making read only memories and shift registers with enough storage capacity to put an appreciable dent in terminal and printer costs. Entire alphanumeric character fonts and CRT refresh channels now can be fabricated as single-chip arrays. Low threshold MOS processes and designs have been refined to make the storage arrays more compatible with bipolar logic and standard power supplies.

These developments have won MOS a place on the alphanumeric side of the readout family tree in Figure 1 (and some inroads are being made on the other side—see Appendix on Page 239. In fact, MOS has pushed beyond the state of the art. MOS/TTL assemblies can generate characters faster than they can be handled by moderately priced CRT video circuitry or printer mechanisms. However, the increased storage capacity and speed also make higher performance systems feasible. For example, designers are considering larger fonts that make characters more legible. Large fonts have generally been economically impractical in the past because even a small increase in font size can double the memory size needed.

MOS ROMS AND REGISTERS

Large capacity, high speed, and bipolar compatibility strike directly at the problems involved in lowering data terminal costs. To generate and update readouts with many characters and symbols takes thousands of bits of storage and fast manipulation of data and control signals. If this capability is supplied in a central processor, it must be paid for in the form of central system overhead and communications costs. Using pre-LSI memory techniques in the terminals, however, can easily double the cost of each console.[1]

Storage capacities per MOS chip have increased at least tenfold in the past few years, with comparable reductions in assembly costs. By the close of 1969, MOS/TTL character generators cost about half as much as those built with bipolar devices. The newest ROMs (read only memories) for character generation represent the integration of some 3,000 diodes and 50 packages of IC gates. One terminal manufacturer who made the changeover late in 1969 replaced six large printed circuit boards with one plug-in card.

The largest MOS ROMs mass produced last year stored 1024 and 2048 bits—general purpose sizes used for table lookup, microprogramming and random-logic functions as well as character generation. A typical generator contained three 1024-bit ROMs, such as National Semiconductor's SK0001 and SK0002 kits (see Table 1 and Figures 2 and 3). Generating the standard 64 ASCII-selected characters in a 5 x 7 font requires a storage capac-

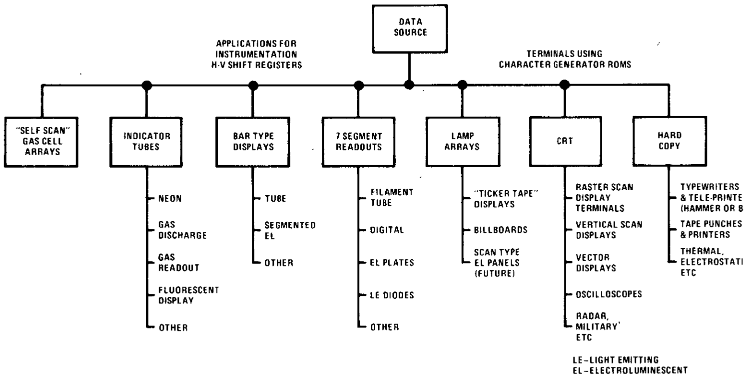


Figure 1. Display Family Tree

ity of at least 5 x 7 x 64. Each logical "1" bit stored in the ROM produces a black dot on a printout or a bright spot on a CRT screen, and each "0" bit a blank space.

Table 1. ROM Combinations for Various Fonts

FONT	CHARACTERISTICS	PARTS REQUIRED
5 x 7	Raster Scan	SK0001 or MM5240
7 x 5	Vertical Scan static ROM required	SK0002 or MM5241
7 x 9	Raster Scan	MM5241 (2 required)
9 x 7	Vertical Scan static ROM required	MM5240 (2 required)
8 x 10	Raster Scan	MM5241 (2 required)
10 x 8	Vertical Scan static ROM required	MM5240 (2 required)
9 x 11	Raster Scan	MM5240 (3 required)
11 x 9	Vertical Scan static ROM required	MM5241 (3 required)
12 x 16	Raster Scan	MM523 (6 required)
16 x 12	Vertical Scan static ROM required	MM5241 (4 required)

Two new soon-to-be-announced ROMs are the MM5240, storing 64 x 8 x 5 bits, and the MM5241 storing 64 x 6 x 8 bits. Each chip also contains decoding logic and sense amplifiers (as do the 1024 and 2048-bit chips). Thus, one ROM is ample for a standard 5 x 7 or 7 x 5 font. The added capacity can implement special needs, such as dropping comma tails below the other characters and symbols. But its main purpose is in providing the logic and programming flexibility that enables ROMs to be operated in tandem to generate the larger font sizes indicated in Table 1. The additional capacity costs little in terms of silicon real estate because these devices are made by low-threshold processes with p-channel-enhancement mode MOSFETs as the storage elements—the most LSI-able type of MOS.

In the past, when diode matrixes were used as character generators, the 5 x 7 or 7 x 5 fonts gave the best cost/legibility tradeoff. Because the new ROMs lower the cost per function, the 8 x 10 font will probably become the most attractive.

The input-output configurations of the MM5240 and MM5241 are outlined in Figure 4 for a standard ASCII-addressed font. The 6-bit ASCII code words will address any of 64 characters (2^6). The control logic generates the three additional address

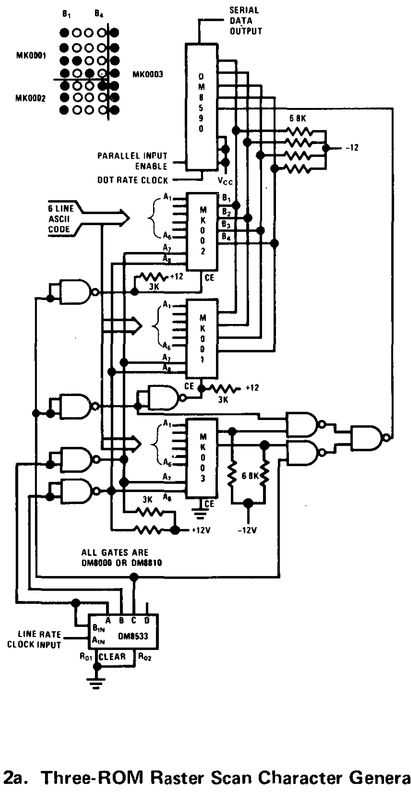


Figure 2a. Three-ROM Raster Scan Character Generators

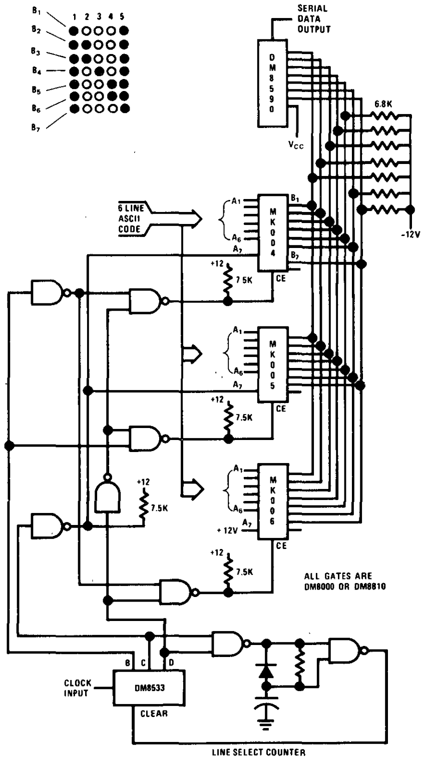


Figure 2b. Character Generator For Tape Printers and Other Vertical Scan Applications

CHARACTER SELECT

I_1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
I_2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
I_3	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
I_4	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
CHAR	0	8	4	12	2	10	6	14	1	9	5	13	3	11	7	15

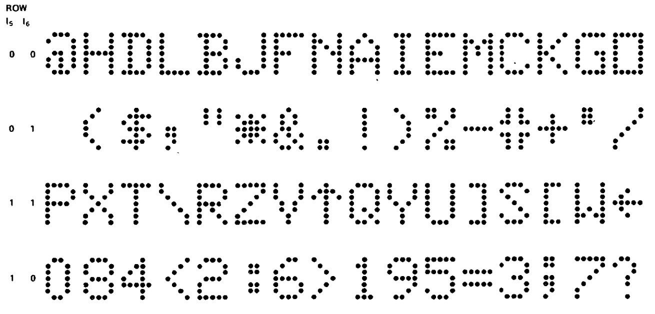


Figure 3a. Raster Scan Character Font

CHARACTER SELECT

I_6	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
I_5	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
I_4	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
I_3	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
CHAR.	0	8	4	12	2	10	6	14	1	9	5	13	3	11	7	15

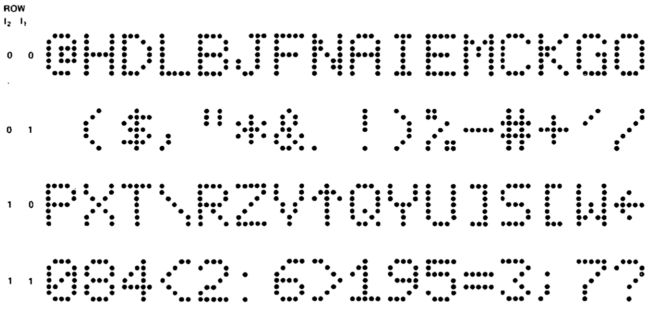


Figure 3b. Vertical Scan Character Font

bits needed to select the individual lines or columns of dots that form the characters in the 5 x 7 x 64 dot matrix. The output bits forming each dot line or column are presented in parallel. The parallel outputs are serialized by a TTL register and used to control the CRT beam or the printer mechanism. To simplify the selection process, the ROMs are programmed to generate the lines or columns in the correct sequence when addressed by the sequential outputs of a TTL counter.

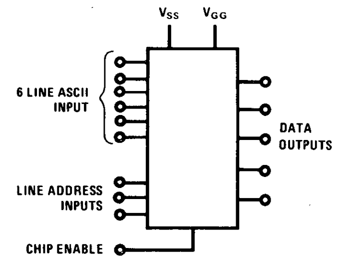


Figure 4a. MM5240 Raster Scan Character Generator Element

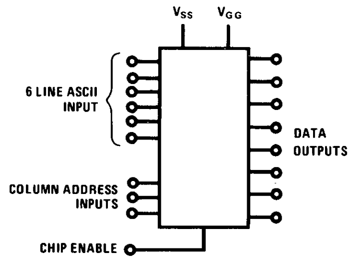


Figure 4b. MM5241 Vertical Scan Character Generator Element

As for registers, they became quite popular during 1969 because a CRT refresh memory of up to about 5,000 bits—enough for a display of more than 800 characters—could be built less expensively with MOS dynamic registers than with delay lines.[2] This was achieved with registers containing 200 storage stages per chip. During 1970, dynamic registers up to 512 bits long will go into mass production, giving rise to predictions of significant savings in refresh memory costs. Whether savings that large can actually be realized will depend upon how quickly the new devices catch on and go into volume production.

Aside from cost per function, other pertinent consideration are temperature sensitivity and functional flexibility. In a refresh memory, register outputs are fed back to the inputs. On each recirculation, the data readdresses the ROM, regenerating (refreshing) the display (Figure 5). The recirculation times must correspond to the CRT scanning time to keep the display legible. MOS register delay times are relatively insensitive to temperature variations because they are established by system clock rates rather than physical parameters.

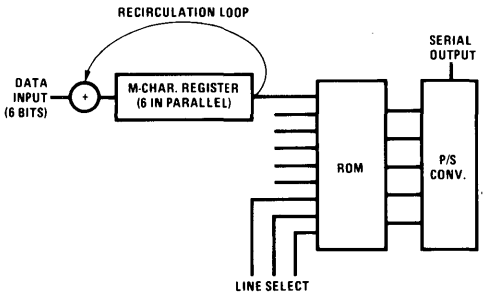


Figure 5. Basic Digital Character Generator and CRT Refresh Memory

Also, special requirements of data entry and output for display formatting and editing can be implemented much more easily with registers than with physical delay lines. Data bit positions in the recirculation loops are maintained in alignment and can be monitored and modulated precisely by the control logic (one recirculation loop is needed for each data bit—six loops, for example, in an ASCII-addressed system). Data entry and output for display or transmission thus becomes a straightforward exercise in logic design.

BIPOLAR COMPATIBILITY

A dynamic register is one that must be clocked at some minimum frequency. Data is retained in the form of charge storage and the charges would eventually leak out of the storage nodes if not re-established. In contrast, the ROMs being discussed are static devices, generating an output only when addressed. Specifically, they are designed and programmed to be sequenced by TTL ICs. Furthermore, the new generations of ROMs and registers accept and put out bipolar level signals and operate off +5 volt and −12 volt power supplies.

These features eliminate any need for special level-translating circuits between the MOS and bipolar devices. Also, special power supplies are not generally required because ±12V as well as ±5V supplies are usually provided in terminals for other parts of the system. Such compatibility is a convenience and a cost saver in any digital system containing MOS storage subsystems and bipolar logic, since it minimizes the interface and drive complexity. In terminals, though, compatibility is practically essential for efficient operation and lowest cost per function.

First, as the detailed system diagrams show, many of the interconnections have a MOS device at one end and a TTL device at the other, so that a large number of level translators would be needed if they were not compatible.

Second, several control logic operations must occur between memory outputs, and the output-serializing device must operate at least six or eight times as fast as the word (dot line or column) output rate of the ROM. Obviously, if high speed control logic—preferably TTL MSI devices such as single-chip binary counters and 8-bit parallel-input/serial-output shift registers—were not used, the character generating process would be slowed excessively. This would limit the number of characters that could be displayed in a CRT refresh cycle or printed out in a given time. The new generation of MOS ROMs can deliver up to eight bits in parallel in about 700 nanoseconds, compared with a microsecond or more for last year's models. Logic speeds around 10 MHz are therefore desirable (several times higher than the speed that can be achieved by MOS gates.) Likewise, dynamic registers can now easily be run at rates above 2 MHz—double the speed of early mass produced registers—so the logic controlling refresh storages must also be faster.

The improved compatibility and higher speed are largely due to better design and processing of the input and output stages of the registers and the sense amplifiers of the ROMs. They don't increase the complexity of the MOS circuitry, unlike other techniques for increasing MOS speed, and therefore they have permitted the capacity increases cited.

The net benefit to the system designer of this approach to MOS design is that it enables the system designer to capitalize on the best features of each technology—MOS storage for high density and low cost, and TTL for high speed processing of data and control signals. This is what produces lowest cost per function in most digital systems.

CRT RASTER SCAN DISPLAYS

The basic refresh mode in Figure 5 limits the number of characters that can be displayed. A better way of generating and refreshing raster scan displays, particularly those with many rows or lines of characters, is outlined in Figure 6. Figure 7 illustrates the timing and logical implementation for a multiple row system.

As before, coded data from a communications link or the console keyboard passes through the registers and addresses the character generator. In these examples, the 6-bit ASCII input and the 3-bit control logic input generate raster scan character formats that allow a conventional TV monitor to be used as a display. Communications codes other than ASCII can be used.

If the ROM contains a 5 x 7 font, each 5-bit character line output will form five horizontal bright spots on the CRT. That is, each ROM output generates one-seventh of each character in a row of displayed characters. The output is serialized by the TTL register and used to intensity modulate the CRT beam as it sweeps across the screen.

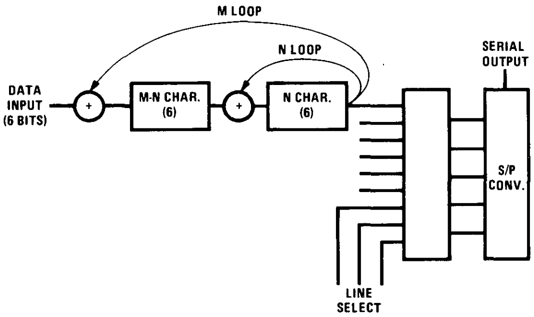


Figure 6. (M-N)+N Technique for Large Page Displays

The refresh memory registers are divided into M-N and N sections to facilitate page displays. M is the total number of characters displayed in several rows (lines of the page) and N is the number of characters in each row. To form such a display with single-loop registers, as in Figure 5, would take seven recirculations of all M data words during each refresh cycle of the CRT. The technique in Figures 6 and 7 only requires high speed recirculation of N bits at a time, with advantages that will be discussed shortly.

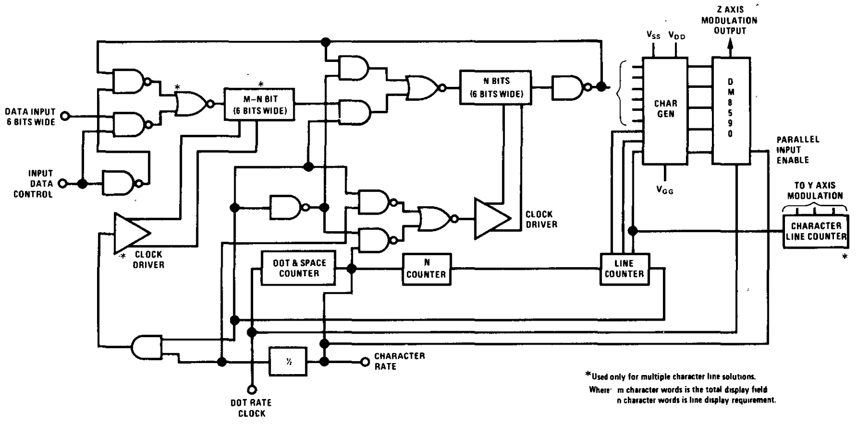
Assume that on the first sweep of the CRT beam, the ROM is being addressed by the six register outputs representing characters N_1, N_2, N_3, etc. The first horizontal, 5-dot line of each character in the display row are displayed in sequence. Then the line address inputs to the ROM from the control logic change to their second state at the time that N_1 has completed its recirculation to the N register's outputs. Thus, on the second CRT sweep, the second series of 5-dot lines are displayed horizontally for all N characters. At the end of seven recirculations, the complete row of N characters is on the display.

Now, the contents of the N register are not returned to the input of the N register. Instead, they are fed back to the input of the M-N register and this register is clocked to load the N register with the second group of N characters. The M-N register is then held still while the N register recirculates seven times to generate the second row of characters on the display. After all M characters are on the display, the first group of N characters is reloaded into the N register and the entire process is repeated to refresh the display.

Human factors—chiefly the eye's response time—dictate that the display be refreshed at least 30 to 35 times a second for good legibility. Most designers prefer to refresh at 60 Hz power line frequency because it is generally the most convenient frequency.

Besides generating the line address inputs (that is, the number of recirculations of the N register), the control logic keeps track of the number of dots and spaces in he output bit stream. The spaces between characters in a display row are inserted as "0" bits when the ROM outputs are serialized by the TTL register. The counters also control the loading and recirculations of the MOS registers in the refresh memory subsystem.

A multiple row raster scan display could be generated with the M-loop technique in Figure 5 but, the implementation is difficult and impractical. This technique is more appropriate for single row displays. Using this method of display, all M characters to be displayed must recirculate seven times



*Used only for multiple character line solutions.
Where m character words is the total display field
n character words is line display requirement.

Figure 7. Multiple Row Raster Scan Display System

to generate a 5 x 7 horizontal scan, so all stages of the registers must operate at the full character rate. To form several rows with a single-loop memory requires an interlaced scan rather than an ordinary raster scan. The first series of 5-dot lines are generated by the first N character outputs as before, but the next set of N inputs to the ROM will generate the first group of 5-dot lines in the second row of characters on the display. Therefore, the beam must jump to the new line position. To display four rows of 5 x 7 characters, for instance, would require a staircase generator that would step the beam by the height of nine scan lines (seven dot lines, plus two blank spacing lines between rows) three times after the initial scan. Then, as the second of the seven recirculations begins, the beam would have to be shifted an additional line to start the second series of line scans—and so forth.

The M-N-N technique does not require any more register stages than the M-loop technique and significantly reduces control and drive circuit requirements—again producing a lower cost per function.

REFRESH MEMORY MODULATION

The technique employed in the M-N-N refresh memory is called "clock modulation". In other applications, it has already been found to significantly reduce total storage costs.[3] It helps minimize power dissipation—in most terminals, the amount of power consumed is unimportant in itself since line power is used, but registers are powered by clock drivers and the cost and complexity of the drive network is certainly important. Furthermore, the technique allows long, very high-density MOS circuits, produced by relatively inexpensive low threshold (bipolar compatible) processes to operate at very high effective character rates.

As shown in Figure 7, the raster scan system uses nine clock intervals to generate a row of characters on the display. Seven are for the high-speed recirculations. During the other two intervals, the first N characters are fed back from the output of the N register to the input of the M-N register while the N register is loaded from the M-N register with a new row's worth of characters. Since two intervals are used for this operation, the registers operate at only half the character rate. The rest of the time, the M-N register is charge-quiescent. Its average clock frequency is only about 11% of the character rate.

In other words, most of the refresh memory (perhaps 90% in a large display system) operates at only half the character rate (say 1 MHz instead of 2 MHz) only two-ninths of the time. The savings in the drive network alone can be judged from the power-frequency plot for a typical MOS dynamic register (Figure 8)[3]. In addition, the designer can increase the number of characters generated per refresh cycle, for a larger display, or increase the number of dot lines, for a larger font, or both.

Remember, though, that dynamic registers must be clocked to retain data. How long can the M-N register be turned off? Long enough for practical applications. The guaranteed minimum frequency is temperature dependent, since temperature affects charge-storage time. The minimum for National Semiconductor's MM-series registers is 500 Hz at 25°C, rising to 3 kHz at 70°C (maximum operating temperature is 125°C, but that is not a display environment). At room temperature, the registers can safely be quiescent for as long as 2 msec. (The typical MM register will actually hold data for 10 msec.) Suppose the N register stores 40 characters and operates at 2 MHz. The quiescent period can be as short as 40 x 7 x 0.5 = 140 μs. If standard TV raster timing is maintained then the quiescent period will be 7 x 63 μs = 441 μs. Obviously, the designer has great leeway in character rates, operating temperatures, and register capacities.

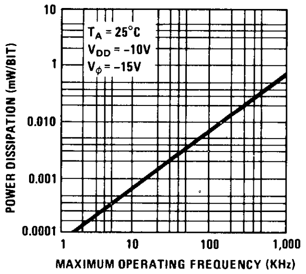


Figure 8. Power vs Frequency Plot of Typical MOS Dynamic Register

Other applications in displays for clock modulation include input-output buffering of data during data reception and transmission,[2] or during display editing and formatting through the console keyboard. The register rates can be adjusted via control logic to accommodate differences between I/O and recirculation rates. Note that the gating in Figure 7 permits data entry under TTL control into either register section.

CHARACTER GENERATION

The first generally available MOS character generators were kits such as those in Figure 2, using three 1024-bit ROMs (MM521). Although single-chip generators were being developed in 1969, they were in very short supply. The kits cost about half as much as diode generators and thus allowed terminal manufacturers to start the changeover to MOS.

The kits are also a good place to begin describing character generator operation in this application note, because they provide an "exploded view" of multi-ROM generator operation. Similar techniques will be needed to build larger fonts with the new devices. The external gating functions shown in Figure 2 are not needed for these fonts when the MM5240 and MM5241 are used. The "assembly" of the dot patterns is taken care of in the programming of the ROMs. However, to generate a large font, such as 8 x 10 or 12 x 16, with the new ROMs will require operation of two to four ROMs.

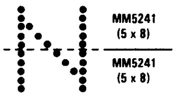
Each MM521 in the SK0001 raster scan kit can store 256 4-bit dot patterns. As the inset letter "N" in Figure 2a indicates, the MK001 ROM stores the first four 4-dot line segments of each of the 5 x 7 characters, the MK002 stores 4-bit segments of the other three-dot lines, and MK003 supplies the fifth bit of each of the seven-dot lines. All ROMs are addressed simultaneously.

The 6-bit ASCII code was devised to select 64 (2^6) characters. However, an 8-bit address is used to select the dot lines and the 6-bit ASCII code from the 256 (2^8) word locations in each ROM. These two additional bits are supplied by the A and B outputs of a TTL binary counter DM8533 (SN7493) and the counter's C output is used to commutate the MK001 and MK002. The ROMs are enabled by an output at the TTL logical "0" level. Thus, with the gating shown, the MK001 is enabled during the first four of seven line-rate clock inputs and the MK002 during the remaining three inputs.

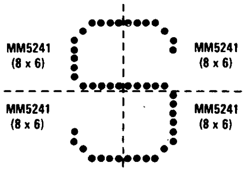
The MK003 is continuously enabled by grounding the chip-enabled pin, CE. It must generate a 1-bit output for each of the 7 x 64 dot lines in the 64-character set, which implies a 9-bit address. Rather than produce a special ROM just for this function—which would make it expensive—the MM521 was programmed to generate 256 2-bit outputs from the 8-bit address. The counter's C output simply gates out the unwanted bit.

For a 5 x 7 font, the new single-chip character generators are simply programmed to generate all 5 bits in each dot line, from a 9-bit address. Standard programming provides the 64-character ASCII set, but special characters can be substituted by changing the stored dot patterns. The reprogramming process consists of altering an etching mask that controls gate insultation thickness in the MOS field effect transistors of the storage array. If the oxide is left thick, the transistor will not switch when selected by the decoding logic, generating a "0" output from that location.

Figure 9 indicates why the storage capacity of the MM5240 is 5 x 8 x 64 rather than 5 x 7 x 64—each ROM can generate half of the 8 x 10 x 64 character set. The ROMs can be addressed simultaneously, as before, and be commutated by the control logic to put out the 8-dot horizontal lines in the correct sequence. For very high speed character generation, the addressing of the ROMs can be skewed or overlapped so that the outputs from one are generated while the inputs to the other are being decoded. The only real limitations to the character generation rates achievable with such techniques are the speed of the bit serializing logic and the bandwidth of the video circuitry.



8 x 10 RASTER SCAN CHARACTER



16 x 12 VERTICAL SCAN

Figure 9. Multiple ROM Character Fonts

CONTROL LOGIC

Starting with the dot/character or dot and space counter in Figure 7, the counter moduli are set to accomplish the following functions:

- The dot and space counter determines the number of horizontal spacing bits between characters in the character row on the display. Its output is loaded into the parallel inputs of the DM8590 serial-in/parallel-out shift register. For a 5 x 7 font, for example, a modulus of six inserts one spacing bit (logical "0" bit) between each 5-dot group in the serialized stream. During line recirculation periods, this counter also drives the N counter at the character shift rate of the N register.
- The N counter causes the line select counter to change state at the end of every recirculation of the row data in the N register. It generates a pulse at intervals of 6N dot clock periods (assuming one spacing bit).
- The line select counter generates seven sets of the three address bits that sequence dot-line selection from the ROM.
- A character line counter is needed in some raster-scan displays to keep track of which page line has just been generated. This time is signified by the C or D output of the line select counter.

Outputs of the first three counters actuate the register clock drivers, keeping the line select bits in synch with the data code. If the line select counter is a 4-bit binary device, eight states are available on the ABC outputs (000 through 111). The D output can be used to provide a ninth state and the reset function. Only seven states are needed for line select, so the eighth and ninth states provide the interval needed for loading the N register from the M-N register, as previously described.

VERTICAL SCANNERS AND PRINTERS

Vertical scan character generators are generally used in hard copy applications. Also, a vertical scan type of character generator can sometimes be more suitable for CRT displays than raster scan.

Displays or printouts of calculators and small business machines often show only numerals and a limited variety of symbols—not enough for a full alphanumeric generator. Such fonts are easily programmed into a small ROM such as the 1024-bit MM522, which stores 128 8-bit words. There's room for 16-5 x 7 dot characters on the chip.

These ROMs are also used in the SK0002 kit for a 64-character ASCII-addressed font (Figures 2b and 3b), which requires the storage of 320 7-dot columns and a 7-bit address. Connected as shown, the DM8533 TTL binary counter will reset on the count of 16. And with the gating and interconnections shown, the column select cycle is:

Counter Outputs DCB	ROMs Enabled
DCB	
000	MK004
001	MK005
010	MK004
011	MK005
100	MK006
101	reset (instantaneous)

A CRT beam can be intensity modulated by the serialized output, as in the raster scan technique. However, the electron beam traces either a saw-tooth or pedestal-type scan pattern on the screen (Figure 10). Every column of each character in the display line is scanned in sequence, starting at the left-hand side of the screen.

The sawtooth scan is straightforward, but the pedestal scan requires that the bit order be reversed in the second and fourth columns. To do this, the outputs of the MK005 ROM are simply connected to the output buses in the reverse order (i.e., output 1 to bus 7, output 2 to bus 6, etc.).

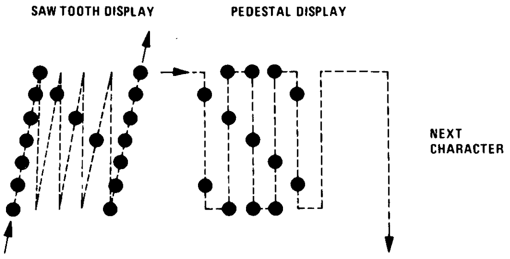


Figure 10a. Two Techniques for Vertical Scan


THE QUICK BROWN FOX JUMPS
OVER THE LAZY DOG X1234567890

Figure 10b. Example of Character Generation Using Pedestal-type Scan.

Long shift registers, operating at relatively slow rates can be used. The character rate—the register shift rate—is no more than 1/6 of the column-select rate for a 5 x 7 font, since the beam traces one complete character before going on the next one. A dot counter loads spacing bits between characters via the TTL shift register, a character counter triggers the sawtooth or pedestal scanning patterns, and a row counter would control positioning of the beam in a page display system.

In the new single ROM (MM5241) version of this system, (Figure 11), a 9-bit address is needed, 6 bits for the ASCII code and 3 bits for dot col-

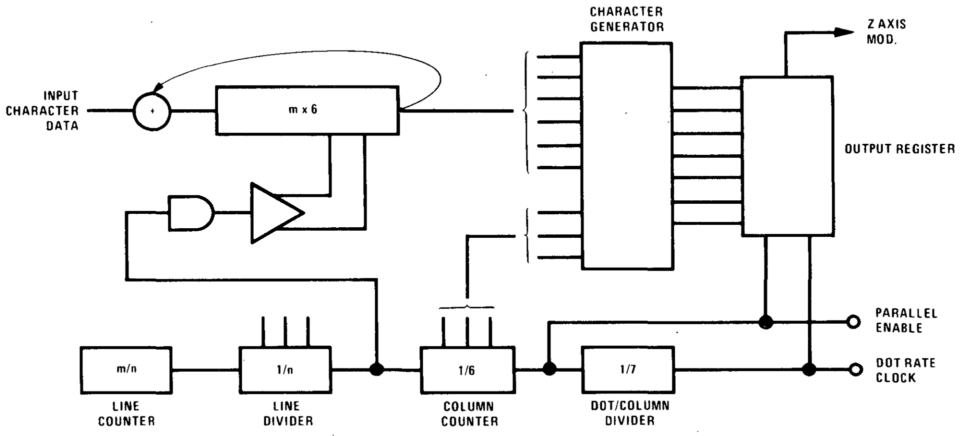


Figure 11. Vertical Scan Display System

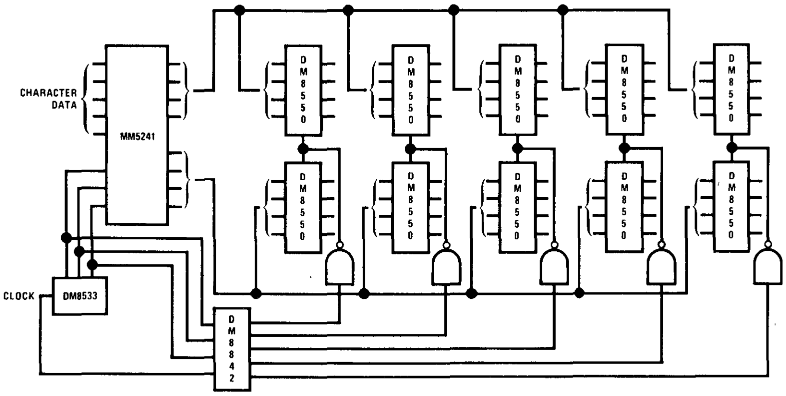


Figure 12. Printer Application Block Diagram

umn select, Since the ROM stores five dot columns for each of 64 characters in a 5 x 7 font, 3 decode line are necessary. Also, the ROMs are programmed differently for sawtooth or pedestal scanning. Because the output pins are committed for all columns, external connections cannot simply be used to reverse output bit order.

Hard-copy printers can use the same fonts as vertical scan CRT displays. MOS registers may be used for data input buffering, but of course refresh registers are not generally required. The character generator output may be used to select some combination of 35 hammers, needles or electrodes that print the 5 x 7 dot patterns on the paper. One technique for handling the character generator output is shown in Figure 12.

In Figure 12, a TTL counter connected to divide by six (five columns and the blank column space between characters) generates the column select address. The ROM's outputs are accumulated in TTL latches (or held in TTL serial-in/parallel-out shift registers). When all dots for a character are ready, they are printed. In tape printing applications in which a 7-transducer array sequentially prints or punches a column at a time as the paper moves under the transducers, the ROM outputs can be used as they are generated unless storage is required for some other purpose.

Character generators are not needed for conventional electromechanical typewriters. But MOS ROMs do have a role here—one version of the MM521, for example, is programmed to convert the ASCII communications code into the Selectric code used to control ball-type printers.

PRINTING APPLICATIONS

The application of character generators in a printing application is normally quite different from that of the display system. Most printers require that a total character font be available before the print is executed. An example of a practical method of accomplishing this (Figure 12) is to sequence the character generator element through the font sequence. Each of the character columns or rows is addressed. The character generator output data at each of these address intervals is transferred into bipolar memory. This memory not only satisfies the memory storage but also the general power buffer which is required between the MOS character generator and the electromechanical on thermo electric printer. In the printer application there may be a requirement to buffer the input data with data storage because of the relative differences in data and printer rates but generally there is no need to retain the printed character intelligence.

The data transfer from the character generator to the bipolar memory in Figure 12 is accomplished by sequencing the column address lines and enabling the appropriate memory simultaneously. Each pair of DM8550s (SN7475s) then contains the data for one of the five columns in a character. The DM8842 (SN7442)—one in 10 decoder provides the decoding functions which are connected to the enable line on the quad latches.

LARGER, FASTER SYSTEMS

Most low cost terminal designs have been based on the 5 x 7 font because of the high cost of diode matrixes and wideband video circuits. But it is by no means the most legible font. A 5 x 7 font is acceptable for applications in which the display changes slowly, but human engineering studies indicate that it causes severe eyestrain when an operator reads rapidly changing data.

The greatest portion of the discussion has dealt with a 5 x 7 font. A full 64 character display can be coded into a single MOS package. Now that LSI has entered the scene, we see a different trend towards larger, more stylized font. The economy of MOS ROMs will provide the customer with a more legible character font at the present cost of "discrete" character generators. An analysis of the most practical solutions to various fonts are tabulated in Table 2. The part types which have been used to generate a 64 x 7 x 5 raster scan font are the SK0001-3 ROM kit or the MM5240 which is under development. The vertical scan font is satisfied by the SK0002-3 ROM bit or the MM5241 which is under development. If we examine the other possible fonts, these same two monolithic elements will satisfy the requirements if they were 64 x 8 x 5 and 64 x 6 x 8 respectively. Therefore, the added memory storage is being incorporated into the MM5240 and MM5241. In some of these cases the font is scanned in the horizontal dimension while in others the font is scanned in the vertical dimension. You find both the 8 x 5 and 6 x 8 elements capable of satisfying the font matrix requirement. Since all the ROMs listed are static by design, there are no special clocking hardships induced with the solution of any of these larger fonts. This is not true for all dynamic ROM solutions.

As mentioned before and shown in the table, the same ROM element is used in both raster scan or vertical scan applications. If we recall the design solutions showing the refresh memory and character generator for a 5 x 7 display, the first thing which is apparent is that the sequencing of the character generator is different in each of the two basic techniques. In one case the character generator is sequenced at the character rate (raster scan) while in the other case the generator element is sequenced at the column rate (vertical scan) of the font.

Since a display utilizing the vertical scan techniques has input address changes at some multiple of the display character rate, a clocking system for a dynamic ROM character generator must be supplied. This requires the addition of a frequency divider and clock generator which results in a higher system cost when dynamic ROMs are used.

A second consideration which should not be overlooked in systems cost is the compatibility of ROMs in multi-package character fonts. Optimum ROM usage and organization will result in lower systems cost. ROMs will also find applications in micro-programming and code conversion where synchronous operation is preferred.

The 8 x 10 font is much better and 12 x 16 is almost optimum for legibility. Small, lower case characters can be sharply defined, too, and they almost appear to be drawn with continuous strokes.

System designers considering these fonts for low-cost displays run, at present, into CRT cost problems. The least expensive displays are television-type CRTs with limited video bandwidth. Bandwidth also limits the number of characters that can be displayed simultaneously. Not counting the times required for beam retrace and functions other than character generation, which reduce the time available in a refresh cycle for dot handling, the necessary bandwidth is roughly:

BW = (dots and spacing bits per character)
X (characters per display row or page)
X (refresh rate)

TV-type CRTs have a maximum bandwidth of about 4 MHz, of which only about 2.5 MHz is generally useful. If one uses a 5 x 7 font with one spacing bit (6 x 7 total) at a 60-Hz refresh rate, each displayed character needs 2.52 kHz of bandwidth, so the limit is about 1,000 characters. In contrast, the new ROMs take as little as 700 nanoseconds to generate a dot line, or about 5 μs per character. That's fast enough to generate 200,000 characters a second, or a display of more than 3,000 characters at the 60-Hz refresh rate. The actual dot rate in the serial bit stream to the CRT can approach 10 MHz. And if larger fonts are generated in some multiplexed addressing mode, the required bandwidth can be much higher.

Luckily, these problems are not insurmountable and there are alternatives to using oscilloscope-quality CRTs or storage tubes, which are fine for high performance applications but too rich for low cost terminals.

Obviously, the designer can drop the refresh rates. New CRTs with longer persistence phosphors facilitate this. Also, CRT manufacturers have been responding to the new terminal market by working on bandwidth improvements, and they are apparently going to reach 10 MHz in moderately priced video systems soon.

Finally, the designer is not obliged to display his characters digitally just because he uses a MOS ROM. Don't forget that the ROM is really working as a code converter, generating a 35-bit machine language code from a communications code. The language translation can be whatever the situation requires.

All that need be done is update methods used in analog displays, which form characters with strokes rather than dot lines or columns. The ROMs can be programmed such that the bit outputs, when integrated, control X and Y ramp generators. The slopes of the ramp functions are determined by the number of bits in a sequence and the lengths are determined by the locations chosen for turn-off bits. As in the vertical scan technique, the ROM is addressed at the character rate.

Even though some characters can be formed with one or two strokes (I, L, etc.), equal time should be given to all characters in a page display to keep the character rows aligned. A standard sized area of the MOSFET array, such as 6 x 8 or 5 x 8 should be used for each character. Most patterns would thus be a combination of stroke and no-stroke outputs. The single-chip fonts have an 8-stroke capacity for each of 64 characters which is more legible than the standard segmented type of instrument readout, since slant lines could be generated wherever needed.

APPENDIX

WHAT ABOUT INSTRUMENTS AND CONTROLS?

While it is safe to predict that 1970 will be "the year of the MOS" in alphanumeric terminals, MOS applications in numeric readouts are just beginning to emerge.

A new device with considerable promise in this field is a high voltage, MOS static shift register, the MM5081. Developed by National, it has a TTL-compatible serial input, 10 parallel outputs that can stand off −55V, 10 latching-type storage stages, and a serial output.

This novel combination of functions means that the MM5081 can drive lamps, numeric indicator tubes, filament tubes in segmented number and symbols displays, electroluminescent panels, and the new gas-cell arrays. In short, it provides MOS with a good foothold on the numeric side of the readout family tree in Figure 1.

The register stages can either shift the bits to the serial output for recirculation or store the data indefinitely. Hence, displayed characters can be swept along a line of indicators, "frozen" on a stationary display, or made to reappear periodically at any desired repetition rate.

A code-converting/character-generating ROM can be placed at the register input, to display numbers and symbols or alphanumerics. A designer can get almost as much flexibility from a lamp or panel display as from a CRT display. In fact, the first application of the MM5081 is controlling a matrix of neon lamps in a moving billboard display.

Some applications for character generators in instruments are also cropping up. Displaying range scales on an oscilloscope is a good idea that can be improved upon with the new ROMs. The display frees the operator of the chores of mentally calculating scale factors and manually writing these on scope photos. With an alphanumeric font, the camera can also record information such as test conditions, date and time of test, identification numbers, etc. Photo sequences and the data needed to analyze the curves can be coordinated automatically.

Similarly, a ROM can be programmed to display standard curves for go-no-go equipment checkout operations. For example, if a radar's pulse amplifier should have certain output characteristics, the ROM generates the correct output curves through a digital-to-analog converter and stroke generator. When an actual operating characteristic and the reference curve are displayed simultaneously, the operator can tell at a glance whether the radar is functioning properly. Many curves or general purpose curve segments can be programmed into a ROM and picked out as needed with selector switches or a ROM microprogrammer.

ROMs can be programmed as lookup tables, random-logic synthesizers,[4] encoders, decoders, and microprogrammers as well as character generators. A single ROM can perform limited combinations of these functions, virtually qualifying it as a microcomputer. It has been suggested that this capability be used in control panels to perform functions like actuating an alarm when a transducer level goes out of range and initiating corrective action. ROM addresses can be derived from digital meter circuitry. In multi-point measuring systems, this would provide the solid state equivalent of a rack of meter relays.

DEFINITIONS OF DISPLAY TERMS

Font: A set of printing or display characters of a particular style and size. A typical dot-character font is 5 x 7, referring to the number of dot locations per character.

Dot Character: A character formed by a pattern of bright dots on a CRT screen or dark spots on hard copy, rather than by continuous strokes. The dot pattern corresponds to bit-storage patterns in a digital memory.

Column: In a dot character matrix for vertical scanning, a column is a vertical series of dots. On a page display, a column contains several vertically aligned characters. In this article, a column refers to a dot column.

Row: A horizontally aligned group of characters on a display.

Line: In this report, line refers to the number of dots displayed in a single scan when a raster scan character is generated. In a 5 x 7 dot character, there are seven lines of 5 dots each.

Page: A display consisting of several rows of characters, corresponding to lines on a printed page.

Raster Scan: See Figure 9.

Vertical Scan: Two types of CRT vertical scans are shown in Figure 10. In hard copy applications, the dots in a column or character may be printed simultaneously by the printing transducers rather than being scanned.

Sawtooth Scan: See Figure 10.

Pedestal Scan: See Figure 10.

Dynamic Element: A digital device that must be clocked. A dynamic shift register must be clocked to retain data. A dynamic ROM is clocked to decode the address and generate an output.

Static Element: A device that does not have to be clocked to retain data. A static ROM uses direct coupled decoding for bit selection and static output buffers.

REFERENCES

1. A.D. Hughes, *Desired Characteristics of Automated Display Consoles, Proc. Society for Information Display,* Vol. 10, No. 1, Winter, 1969.

2. Dale Mrazek, *MOS Delay Lines,* Application Note AN-25, National Semiconductor, April, 1969.

3. Dale Mrazek, *Low Power MOS Clock-Modulated Memory Systems,* Application Note AN-19, National Semiconductor, April, 1969.

4. Floyd Kvamme, *Standard Read Only Memories Simplify Complex Logic Design,* Electronics, January 5, 1970.

Application Notes

MAY 1971

HIGH VOLTAGE SHIFT REGISTERS MOVE DISPLAYS

There was a time when one had to go to Times Square or Picadilly Circus to see a moving lamp display. But now they're going into stadium scoreboards, stock brokers' offices, waiting rooms and many other places where an attention-getting man-machine interface is wanted.

Naturally, display designers would like to make the control and drive circuitry more compact and less expensive. What's needed to replace the banks of discrete switching devices is storage and switching high-voltage circuits in monolithic form. That's exactly why National developed the MM5081 high-voltage MOS shift register.

This unusual IC is the first MOS device capable of driving gas-discharge tubes and other high-voltage display elements without going through a bipolar buffer such as a transistor or SCR. Moreover, it can "walk" the message around and around the display when operated in a recirculating mode. The latter feature provides a clear-cut division between system functions – the MM5081's take on the responsibility of display operation per se, while the system logic need only format messages and control updating by invading the registers. In other words, the main system logic need pay only intermittent attention to display operation. If the main system is a data-processing computer, for instance, it can handle the display like any other peripheral. Relieved of responsibilities for moving and refreshing the display, the main system can do more data processing between display updates.

REGISTER PLUS SWITCHES

Figure 1 shows in simplified form how one MM5081 would be connected to drive a bank of 10 neon lamps. A data bit stream is entered into the serial input and shifted at the clock rate to the serial output. Then, it can be routed back to the input and recirculated to repeat the display motion.

The states of the data bits circulating through the register control the switching of the MOS output transistors. When a bit in the true state (MOS logical "1") is being stepped down the 10 register stages, the lamps will turn on and off in sequence at the register clock rate. In this mode, the clock rate is the display rate. A typical display rate will move the light along by no more than two or three lamps per second, making any message displayed on parallel rows of lamps easy to follow and read. A latch-type register cell that can shift at frequencies to DC and a single-phase clock input are used in the MM5081 to achieve this effect. However, the logic formatting the data for display will have to run at some higher rate. If the control system has other functions as well, it may be desirable to load the register at a clock rate in the hundreds of kilohertz. At such a high rate, the bit stream flashes by the 10 parallel output switches too rapidly to see the lamps being turned on. After loading, when the main system logic is freed, the clock rate is dropped to the display rate and the message is seen. The message simply recirculates at the display rate until new data is ready for loading.

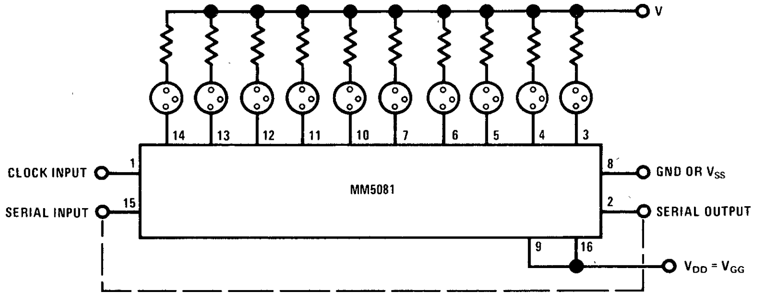


FIGURE 1. Block Diagram

The use of high-speed logic for control is facilitated by making the MM5081 with low-threshold, p-channel, enhancement-mode MOS transistors. As a rule, a low threshold device allows data to be entered at bipolar logic levels.

The output transistors do not need a large gate-voltage change to turn on and off. They are also low-threshold devices in this sense. But they have to withstand transients up to 100 volts and stand off steady state voltages up to 55V to operate lamp-type displays reliably. Adequate gate logic voltages for the output transistors must be ensured to make the lamps glow brightly when they should be on or to make them free of any residual glow due to switch leakage when the switching transistors are turned off. That is, a low R_{ON} and high R_{OFF} must be ensured despite very high voltage on the MOSFET drains. Because a pullup resistor is used, the input gate should be a TTL or DTL device with an uncommitted-collector output able to withstand at least 10V. Among such devices are the DM8810, DM8811 or DM7426 (SN7426) quad NOR-gates, or the DM8812 hex inverter. All these TTL devices will stand off to 14V.

The other two gates used in the input switch can be any TTL or DTL types. The arrangement shown brings the serial output back to the serial input through the top gate when the "new data enable" line is low (DTL/TTL logical "0") or permits the registers to be reloaded with new data when the enable line is high. A pull-down resistor is placed on the register output to handle 1.6 mA the current sinking required for operation of the TTL or DTL recirculation control gate.

TICKER-TAPE DISPLAY

A straightforward type of moving lamp display is illustrated in Figures 2 and 3. Simple messages such as CALLING DR. CASEY . . . CALLING DR. CASEY . . . DR. CASEY, PLEASE REPORT TO SURGERY . . . or stock quotes, or a series of instrument readings would be displayed as 7X5 characters by this system. That is, each character would be a lighted lamp pattern selected from a moving matrix seven lamps high by five lamps with a moving column of lamps turned off between characters. The off column is a space bit in each lamp row.

Assume that the display is long enough for 33 characters. Each row requires 33X6 lamps and 198 register stages. Each row is a cascade of 20 MM5081's. The input of the first register and the

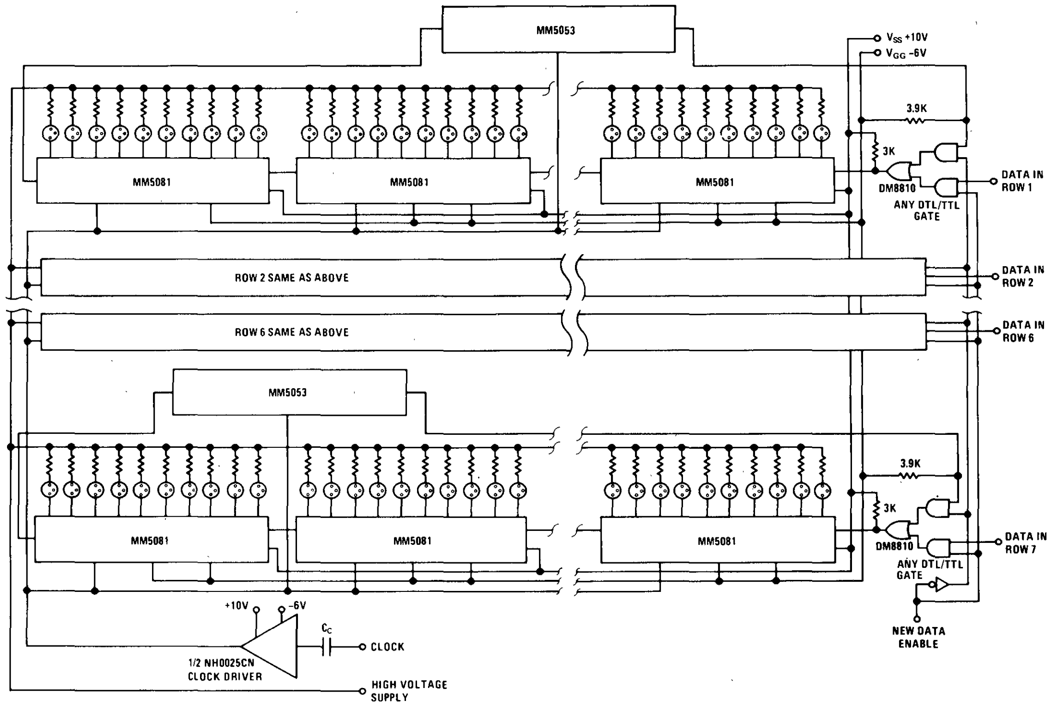


FIGURE 2. 7XN Bit Shift Register and Display

output of the last register are connected as in Figure 1, and the registers in between are simply daisy-chained by connecting each serial output to the next serial input. All seven rows would use 140 register packages.

The character data for this type of system can be formatted by a standard character generator. For instance, the standard ASCII code can address a bipolar compatible read-only memory such as National's MM5241AA, which is programmed to generate 5X7 dot-type characters for CRT display. However, in the lamp display system, the display refresh function is handled without an additional memory. The column bits are entered in each register chain, as before, through the input gating at a rate determined by the clock rate supplied the MH0025C clock driver. The MH0025C is a two-phase driver. However, since the MM5081 takes a single-phase clock input (converted to a two-phase clock inside the register package), only one of the dual drivers in the MH0025C package is shown (the other half can be used to share the clock-drive load).

After the registers are loaded, the clock into the driver is dropped to a frequency of 2 Hz, if the register was loaded at a higher frequency. This rate is stabilized by the coupling capacitor C_C. The coupling capacitor on this type of driver determines the maximum pulse width, but the minimum pulse width is established by the clock signal. So, at the lower frequency, the characters sweep smoothly from right to left across the display lamps. They repeat the message every 100 seconds because 200 register stages are in each of the seven parallel rows.

Both the clock driver and the registers operate off the 10V and –6V power supplied.

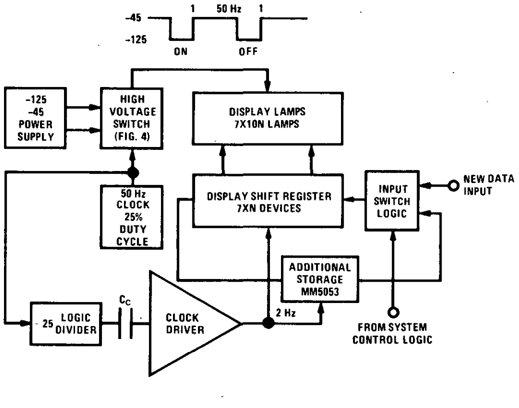


FIGURE 3. System Block Diagram

DISPLAY DRIVE

The high voltage supply (shown in the block diagram in Figure 3) is generated from a high voltage switch. The purpose is to limit the current and voltage across the lamps and the MOS output transistors to ensure that they operate reliably and have long lives. Also, the method reduces power consumption and allows lower power, inexpensive high-voltage power supplies to be used.

The high-voltage switch seen in Figure 3 and detailed in Figure 4 switches at a rate of 50 Hz and a duty cycle of 25%. Thus, when any of the MOS output transistors is on, the lamp that is "on" during that 250 msec display-rate interval (100% duty cycle at 2 Hz) is actually on for only 5 msec at a time. Then it turns off for 15 msec. This refresh rate was chosen because it provides a good lamp intensity with no apparent flicker.

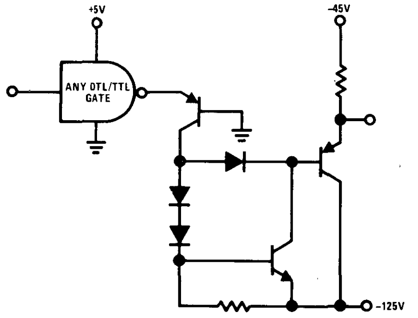


FIGURE 4. High Voltage Switch

The –125V supply turns on the lamps, and the –45V supply turns them off. But what is actually being used is the voltage difference, or bias. Most glow-discharge lamps require a 65V starting voltage and a 60V holding voltage. The switch keeps the lamps alternating between these levels while the MOS transistors are on, but imposes a maximum voltage of only –65V on the MOS transistors (that is, 125–60V) for the 5 msec "on" time. The MM5081 can easily take this – the spec allows –100V at 60 Hz (or 16.66 msec) and they are stress-tested to this level.

INDUSTRIAL DISPLAYS

The characters displayed can be any kind of symbol within the resolution of the lamp array – from letters to cartoon characters – and within the flexibility of the controls. Getting patterns to move back and forth while changing shape is technically feasible, but would require complex clocking techniques to put the bits in the desired location. Static pictorial displays would be fairly simple to implement, merely requiring loading of the registers at a high rate followed by storage at a DC display rate for the desired time. Although the characters would appear static, the high-voltage switch would keep the actual duty rate low.

There are many potential new applications for moving-lamp displays in industrial control systems. Functions such as process flow rates through several feeder pipelines or subassembly line rate in an assembly plant, cannot easily be set up on a CRT display. Complex computer graphic techniques or very expensive multi-gun displays may be needed.

The clock rates and lengths of a number of rows of lamps can readily be adjusted by hand-operated controls, such as voltage-controlled oscillators and gating between registers chosen by selector switches. Any feeder-line display rate that can be represented by the display rate could therefore be varied at a compressed scale of time and distance until the display operator arrived at the optimum balance of rates. This is a visual approach to a problem that generally requires complex mathematics and analog computers to solve.

Nor do the rows of lamps have to be aligned. Individual rows might represent route sections in a transportation network between junctions. By driving each section at a display rate simulating the speed of a particular train, and switching the "train" of moving lights from row to row via switches at the junctions (serial output to serial input register connections), control personnel could simulate system operation. Problems such as tie-ups — or worse — at junctions could be worked out by varying display rates for the trains whose schedules conflicted.

Application Notes

AUGUST 1971

DYNAMIC MOS RANDOM ACCESS MEMORIES SYSTEM CONSIDERATIONS

ABSTRACT

A new TRI-STATE™ common I/O configuration, capable of precharge decoding without losing system performance and bipolar compatibility, is employed in a 1024-bit MOS RAM. In combination, the techniques reduce typical memory module power dissipation some 66%, number of overhead circuits by 50%, and overhead costs by 66% without sacrificing system speed. Performance and cost of the new RAM are compared with those of an earlier design in a similar system application.

INTRODUCTION

Unlike earlier advances in MOS memories, the advantages offered by the MM5260 MOS RAM do not stem from a new process. Instead, a new combination of operating techniques is used to solve system cost/performance problems. The techniques are a TRI-STATE I/O structure at a common I/O terminal, precharge decoding, and bipolar-compatibility.

Memory size, cost and propagation delay of the monolithic MOS random-access device were not decreased. These savings could have been realized quite easily at the device level by foregoing some of the system advantages. The result at the system level though is very low average power dissipation, simplified timing control, fewer and faster interface devices with the external system, reduced cooling requirements; elimination of high-level MOS supplies, and other cost reductions. Chiefly, dissipation is reduced by 66%, overhead circuits by 50%, and overhead cost by 66% with no loss of speed.

To make these points realistic, the new design will be compared, in a system environment, with another MOS RAM design with slightly faster access and cycle times specified at the device level.

MOS STORAGE DEVICE

The internal design of the new MM5260 (Figure 1a) is fairly standard except for its bipolar compatibility, I/O structure, and precharge decoding.

The 1024 storage cells are in a 32 x 32 array. A 10-bit address is X-Y decoded on the chip to access a cell. In each cell, Q_1 is the storage element, Q_2 a read gate, and Q_3 a write gate. An MOS "1" is stored by charging the capacitance of Q_1 and an "0" by not charging it. Read consists of sensing the data level after an access is made.

Bipolar compatibility means that all data and address inputs sense bipolar data levels and that data is read out at the original data levels. This eliminates external level translators at inputs and sense amplifiers at outputs. Previous MOS designs required these interface circuits in a typical memory module. The common I/O terminal on the MM5260 is made possible by the I/O structure

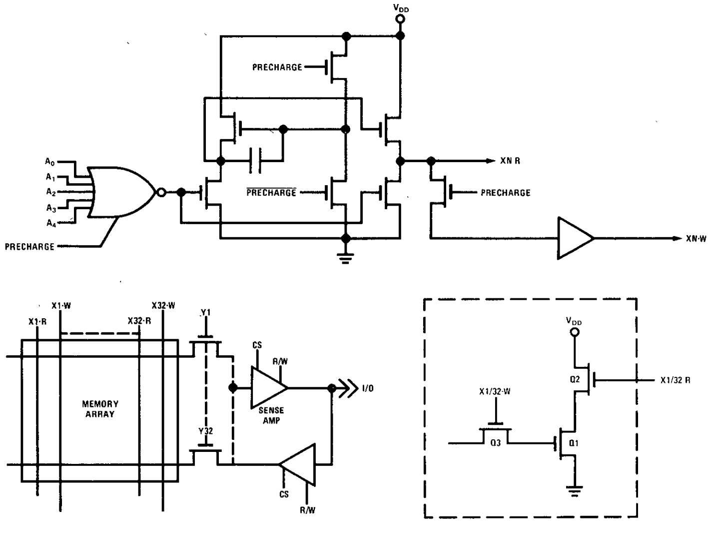


FIGURE 1a. Internal Design of the MM5260

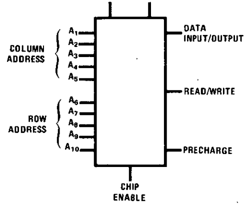


FIGURE 1b. MM5260 Connection Diagram

seen in Figure 1a. The I/O gating and sensing elements are TRI-STATE MOS. As the name implies, each element has three operating states. Two are the bipolar-compatible "1" and "0" states. The third is a high-impedance state that disables that element. In the third state, only a small leakage current flows at no definable logic level.

The third state prevents data transfer, allows one element to look into the other, and permits outputs of several packages to be bus-connected with no significant change in memory cycle time. One pin serves for I/O because the read output buffer is in the third state when write is enabled, and vice-versa. When these outputs are bus-connected, read speed is high because the disabled elements on the bus load the enabled output very lightly.

In addition, the MM5260 uses two standard supplies (+5V and −12V) instead of three high-level and non-standard supplies (+20V, +16V and +5V). A possible additional negative supply (−5V) will be required for a high speed sense amp.

A conventional MOS output could not share a common terminal with an input. Separate data-in and data-out terminals may be required. Several outputs also may be bus-connected. However, this multiplies the capacitive loading, causing a proportional increase in output transition times. To accommodate this, system cycle times must be increased. For maximum speed, each conventional MOS output should look directly into a low-level sense amplifier which also has a low impedance resistor at its input to minimize the data transfer time constant.

Dynamic RAMs require some special considerations. The storage cells are dynamic, meaning that stored charges leak from the storage transistors and must be refreshed periodically. Each cell must receive the refresh clock at intervals of 2 ms. Refresh is applied column by column at 62.5 μs clock intervals (an access also refreshes all other cells in a column). Since accesses are made every 600 ns, refresh overhead is less than 1% and does not significantly affect system efficiency. Refresh signals are given precedence over addresses in the system control logic.

The chief advantage of dynamic MOS RAMs is small cell size, about 4 or 6 square mils, which makes packing density high and cost low. Static MOS devices have latching cells that are not refreshed but are most costly since the cell size is 16 to 20 square mils. Therefore, fewer bits may be placed within the same package. Bipolar RAM cells are also large and costly, but operate in about 50 ns.

Dynamic MOS RAMs fit quite well into large memories and higher system memory hierarchies such as fast store, virtual memory and main memory. Their low cost, high density and relatively low power dissipation suit them to main memory.

SYSTEM ORGANIZATION

Having ten address inputs, the MM5260 is effectively a memory of 1024 1-bit words. Lengthening the bits per word merely require parallel access of several devices, such as nine for 1024 9-bit words. A chip-select input, enabled by decoding additional address bits, allows expansion of word capacity.

Figure 2 is a MM5260 module storing 4096 16-bit words (4k x 16) in four 1k x 16 submodules. One

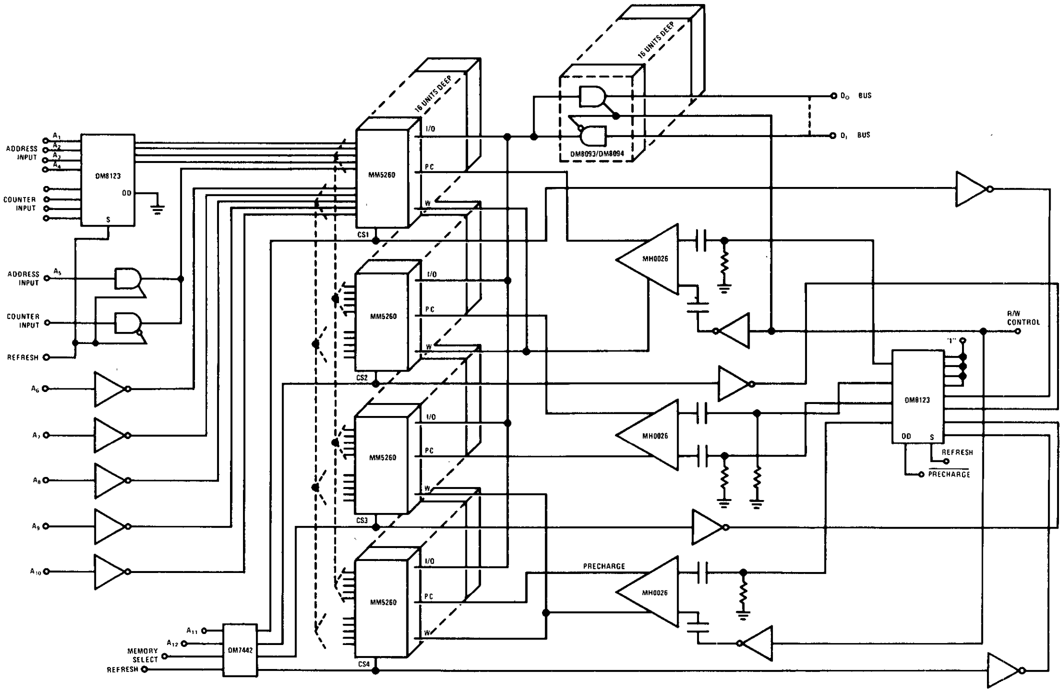


FIGURE 2. Main Memory Module Storing 4096 16-Bit Words Using MM5260

submodule is selected at a time by two bits of the DM7442 TTL decoder address. The same decoder could access eight submodules with a 3-bit address, and so forth. This is standard decoding practice.

The external data selectors (DM8123) and read/write bus buffers (DM8093 and DM8094) are TRI-STATE TTL devices.[1] These have high-speed, active-pullup outputs when enabled. The two types of buffers can operate in parallel with the internal MOS input/output mode read/write gates. One control line gates both in complementary fashion because one is enabled by an "0" and the other by a "1". The data selectors hold off accesses during a submodule's refresh intervals. Figure 3 is the TTL clock forming and timing control circuit for the module.

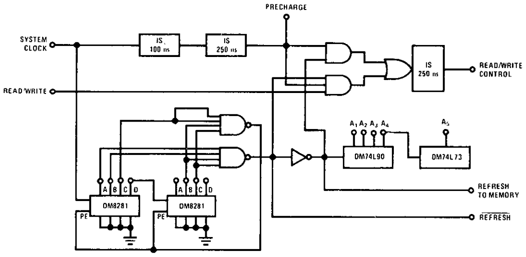


FIGURE 3. System Clock Timing and Control Circuit

PRECHARGE DECODING

During standby, each MOS RAM circuit dissipates about 75 mW. To achieve memory access, a pulse called the "precharge" is applied to set up the decoders and other I/O functions. Precharge minimizes system power dissipation by making it unnecessary to energize decoding logic between selects. During a 600 ns access, MM5260 power dissipation goes up to 400 mW.

It is important to keep as many as possible of the RAM circuits on standby to minimize system average power dissipation. Excessive dissipation, without adequate cooling in a high-density system, would overheat the semiconductor junctions. The only ways of preventing overheating, should average dissipation be high, are to slow down speed and lose performance, reduce packing density, or increase system cooling hardware. Average power supply and clock-driving requirements are also reduced by precharge modulation or by reducing the rate of precharge pulse. The added circuitry to effect power minimumization is only three elements.

Figures 2, 3 and 5 illustrate the most effective way yet developed to decrease precharge power dissipation. This "precharge decoding" method applies precharge to a submodule only when that module is selected. This is implemented by having the chip-enable of the decoder gate the precharge clock via the TRI-STATE TTL data selectors in the clock circuitry. Simultaneously, the I/O directions are controlled. Selective precharge decoding can yield an ultimate average power dissipation of 77 mW.

MEMORY TIMING

The MM5260 timing control is quite simple because of precharge decoding and the I/O structure. As indicated in Table 1, maximum cycle time is 600 ns. A delay of 100 ns before precharge is allowed for address settling and decoder operation. This allowable delay will not affect the access time under worst case conditions. This element design characteristic permits a very straightforward selective precharge decoding technique which does not affect the performance of the memory system. Precharge goes low for 250 ns to set up the decoders, then returns to conserve power.

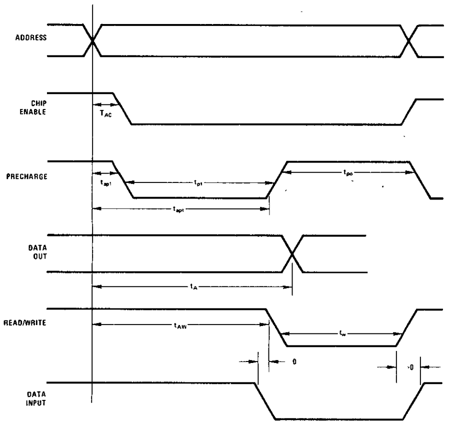


FIGURE 4. MM5260 Timing Diagram

If read is commanded, the read gates are enabled and the write gates disabled at the outputs. Stored data is available at the output within 350 ns of the start of the access. Write may be commanded just prior to the precharge trailing transition and is completed by the end of the 600 ns cycle.

Address, precharge, and chip select timing is not critical. A skew of about 50 ns between address timing by the CPU and leading and trailing edges of chip-select and precharge will not affect access time, cycle time, or overall memory speed.

DEVICE COMPARISONS

The 1103-type MOS RAM comes closest of previous MOS RAM designs to the MM5260 in performance and organization. It is also a 1024-bit device with chip select and on-chip decoding of 10-bit word addresses. The package has two additional pins, one for the extra power supply and another because data outputs and inputs are separate.

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[1] Don Femling, "TRI-STATE Logic in Modular System Organizations," *National Semiconductor AN-43,* April 1971.

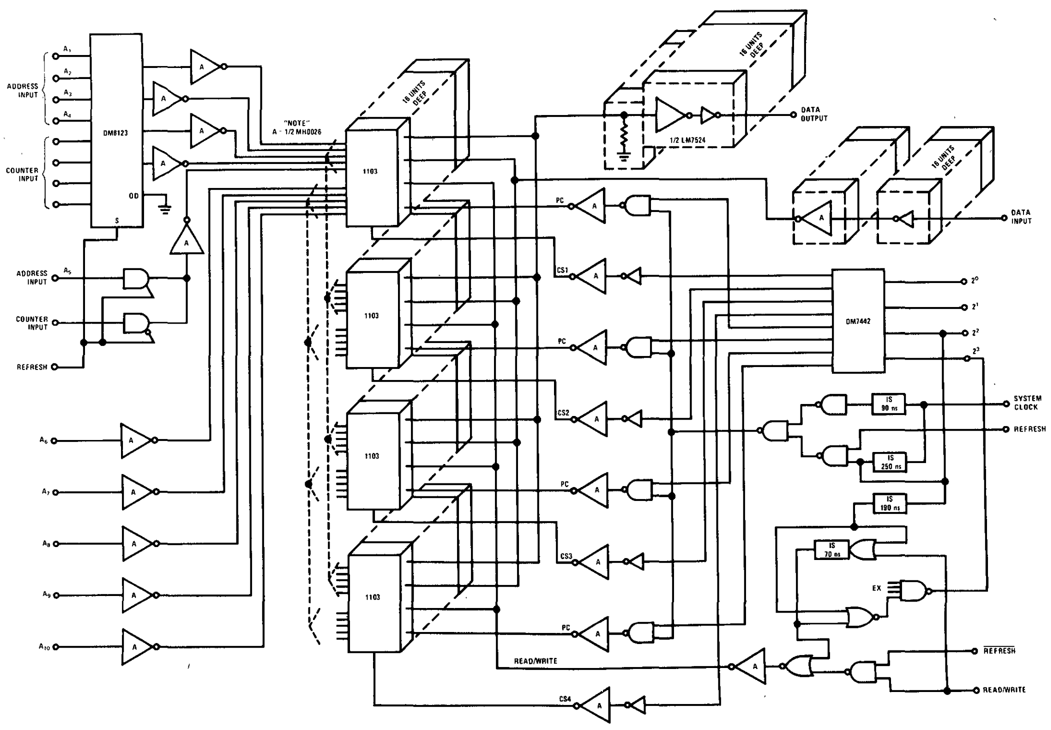


FIGURE 5. Main Memory Module with Conventional 1103-Type MOS RAMs

TABLE 1: Comparison of Major Characteristics of MM5260 and 1103

	MM5260	1103
Organization	1k x 1	1k x 1
Chip Select	Yes	Yes
Input Data Levels	TTL	High (+20V)
Output Data Levels	TTL	Low (800 μA)
Common I/O Bus	Yes	No
Power Supplies	+5, -12V	+20, +16, +5, -5
Package Pins	16	18
Access Time	350 ns	300–390 ns
Read Cycle Time	450 ns	540 ns
Write Cycle Time	600 ns	580 ns
Refresh Intervals	2 ms	2 ms
Power Dissipation During Access	400 mW	300 mW
Standby Power	75 mW	75 mW

TABLE 2: Components in Typical 4k x 16 Memory Module

	MM5260 UNITS	1103 UNITS
MOS RAM Packages	64	64
Total for Storage	64	64
Interface and Control Devices		
DM8123 Quad Data Selector	2	2
DM7442 BCD-to-Decimal Decoder	1	1
MH0026 Clock Drivers	3	
MH0027 Clock Drivers		18
DM74451 Power Translator		18
DM8093/DM8094 Bus Buffers	10	4
DM7402 Gates		2
DM7400 Gates	2	2
DM7404 Gates		5
DM7408 Gates	1	
DM7420 Gates		1
DM8281 Counter	1	1
DM86L76 Counter	2	2
DM74L73 Flip-Flops	1	1
DM9601 Monostable Multivibrator	3	4
LM7524 Dual Sense Amplifiers		8
Total for External Parts	26	69

Important differences between the MM5260 and 1103 characteristics are summarized in Tables 1 and 2. Their individual device costs are comparable and the 1103 appears to enjoy a performance edge (50 ns) at the device level. However, let's examine the 1103 specifications at the system level. Major modules, though not submodules, are almost interchangeable. As proof, compare the typical 1103 4k x 16 module in Figure 5 with Figure 2. Both are very similar conceptually.

MODULE COMPARISON

Power Dissipation

One significant difference is in the power requirements. The 1103 uses two high-level supplies and dissipates about three times as much power as the MM5260 module. Total dissipation in the MOS RAMs and by the circuitry outside the RAMs in Figure 5 is around 30W, while that of the MM5260 module is about 10W. As a benchmark, core memories with the same capacity dissipate about 25W. Clearly, the MM5260 has the advantage. The power dissipation factors are standby power—the same 75 mW for both device—precharge dissipation, and external dissipation.

A quick calculation shows that the MM5260 has precharge dissipation in only 16 out of 64 devices, due to precharge decoding. With standby dissipation in the other 48, total memory dissipation is about 10W. Dissipation in the logic devices is not large in either device.

Precharge dissipation in the 1103 is 300 mW, 100 mW less when it is accessed at a 600 ns rate.

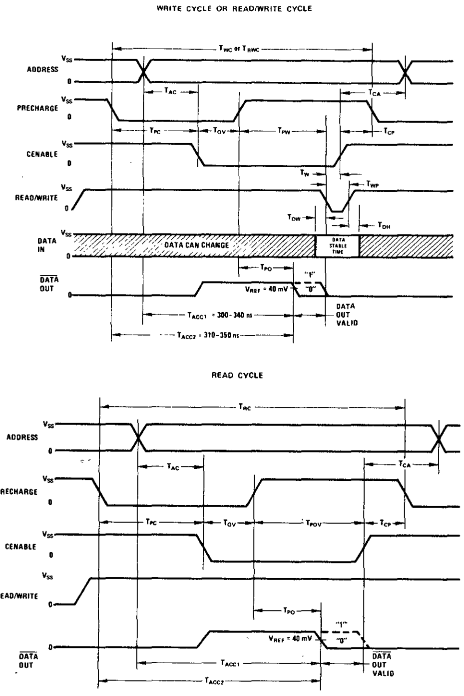


FIGURE 6. Timing Diagram of 1103-Type RAM

Precharge is used to reduce access time as well as average dissipation in the 1103, which compromises precharge power savings. Using precharge to save time precludes precharge decoding. Figure 6, the 1103 timing diagram, shows that precharge sets up the decoders to receive the addresses. Therefore, it must be applied to all 64 RAM circuits since the chip-enable portion of the address is not decoded until after precharge begins. After chip-enable decoding, precharge may be turned off for the unselected submodules. By then, these 49 circuits will have been precharged for some 100 ns, consuming an extra six watts.

A total of about 14W are dissipated in precharge and standby power in the 1103 memory module. In other words, the MM5260 memory solution has already saved 30%.

The extra amplifying devices account for the rest of the increase. Address, chip-enable and data inputs must be pulled up to +16V. These level translators must drive heavy capacitive loads. For example, each address input capacitance is 7 pF, a total of 450 pF for 64 in parallel. To avoid making input delays very long, high-power transistor drivers must be used. The low-level outputs must be detected with sense amplifiers to drive logic in the processor. Furthermore, the high-level supplies increase dissipation elsewhere in the system and add to the system cost since they are nonstandard.

Timing Tradeoffs

Next, is the question of access and cycle times. The access time of the 1103 is 300 ns if the precharge time can be anticipated. If address and precharge occur together, access time is 310 ns. Access time also depends upon the leading edge of chip-enable. The read and write slots are also quite critical.

Extra timing control circuits are needed. Conservative design must take into account Murphy's Law ("if anything can go wrong, it will") in module and address timing.

Good bipolar drivers at the inputs, such as a monolithic translator like the MH0027 or three transistors and several resistors in each, will hold the input delays to 40 to 60 ns. These add to the memory system cost. A low-cost alternative, open-collector TTL devices with passive pullup, would stretch input delay to about 225 ns (due to the RC time constant of a 450 pF load and 500Ω pullup resistor). Furthermore, these passive pullup devices would about double power dissipation again. The delays in the sense amplifiers are approximately 30 to 40 ns. Good sense amplifiers are essential to achieve a short read time and because the MOS outputs are wired-OR'ed. (64 rather than 16 sense amps aren't practical.) As mentioned before, wire-OR'ing also delays output transitions. Most of the high speed sense amplifiers also require an additional negative supply (about −5V).

In sum, there is a minimum increase of some 70 ns in 1103 access or cycle time, and an increase up to

100 ns might result in some system designs. This easily offsets the access specification of 350 ns in the MM5260. This included an output delay of some 40 to 50 ns in the MM5260 access and cycle times because of on chip output TTL compatible buffering. This delay in the TRI-STATE sense amplifier in the MOS chip was considered a worthwhile tradeoff to achieve the benefits already cited for the common TRI-STATE I/O technique.

It might be noted that the TRI-STATE TTL bus buffers will drive long buses at high speed with high noise immunity. Therefore, the common I/O bus can extend well into the system structure.

SYSTEM COST SAVINGS

The obvious savings in system costs are listed in Table 2. These consist of 17 interface and control circuits, 8 dual sense amplifiers, 14 resistors, and a need for only two supplies (+5, and −12) instead of high-level supplies of (+20, +16, +5 and −5). One can also add proportional savings in printed-circuit board costs, cooling hardware, assembly, component test, inventory control, and so forth.

Effective packing density is higher, because the MM5260 has two less pins than the 1103 (obtained by common I/O), one less supply, and less stringent cooling requirements. More RAM circuits can be packed into the same volume; more also can be added on bigger boards when system designers want to increase word length or module word capacity. Smaller boards, of course, further reduce system packaging costs.

CONCLUSIONS

Savings using the MM5260 in a typical memory system module are 66% less power dissipation, 50% fewer overhead circuits, and 66% less overhead cost. Speed performance is not curtailed and, in many applications, an improvement may be achieved.

These advantages stem from a combination of three techniques: TRI-STATE common I/O structure with an internal sense amplifier, precharge decoding, and bipolar compatibility. All are oriented toward system advantages, rather than cost/speed improvements at the device level.

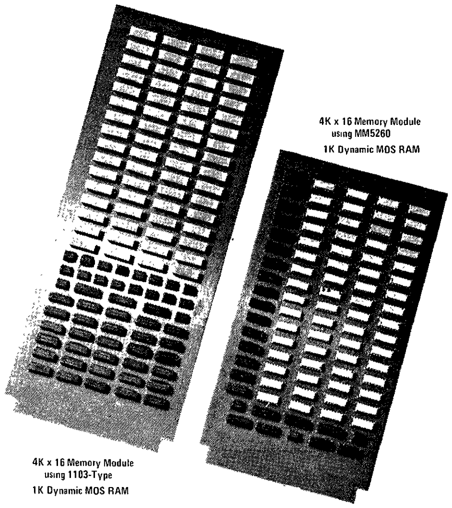


FIGURE 7. 1103-Type and MM5260 Modules. The 1103 memory module utilizes NH0026 level translators in place of 36 DM74451 and NH0027 elements.

Application Notes

NOVEMBER 1971

AN-52 Using The MM5704 Keyboard Interface in Keyboard Systems

USING THE MM5704 KEYBOARD INTERFACE IN KEYBOARD SYSTEMS

INTRODUCTION

When one contemplates the design of an MOS-LSI chip to perform the keyboard interface function, several elements immediately stand out for consideration. Among these is the obvious problem of encoding a key closure, and whether the bit pattern produced should be presented in a parallel or serial fashion. One must also consider what happens if more than one key is depressed, or more than two. How fast can keys be physically depressed and released? One at a time, or in a series? What is required to be compatible with the dynamic characteristics of the many different keyboards being manufactured? What is the best way to match the switch closure characteristics, i.e., switch bounce, etc.? How may various keyboard capacities best be accommodated, or what is required to allow for expansion of keyboard capacity? All of these considerations and more have been answered in the design of the first MOS-LSI chip manufactured by National, the MM5704. It is called the keyboard interface (KI) chip and it is one of a total of five chips, called MAPS – Microprogrammable Arithmetic Processing System, being designed to implement all the functions required of bit serial calculation systems.

All of these chips are unique in that they are designed to perform their functions in a defined system, hence implying a standard design. Yet each may be as individualized and as varied as there are ways to perform their functions. To explain how this apparently paradoxical situation is possible, let's take an example. The keyboard interface chip, MM5704, will accept 32 character key closures and provide 64, 9-bit encoded words in the output. Each key closure will generate and output a code up to 9-bits long for lower or upper case depending upon the state of the shift key. Thus, a standard function is performed, that of providing a 9-bit pattern with each key closure. However, the bit pattern itself may be programmed according to the desires of the individual user. This ability is possible because the 9-bit pattern is generated through the use of a read-only memory (ROM) located within the chip. The key closure merely addresses the ROM and its output becomes the custom encoded word.

These chips are P-channel, enhancement mode, monolithic MOS devices. They are manufactured using silicon 1-0-0 technology which provides the low thresholds required to interface directly with bipolar DTL or TTL integrated circuits. (This latter statement is true only if an output is not also used as an input, such as the μI bus.) The chips typically use +5 VDC (V_{SS}, Pin 12) and −12 VDC (V_{GG}, Pin 24) power supplies because this arrangement permits direct signal compatibility with bipolar logic systems. There is, however, nothing sacred about this power supply arrangement. It is the 17V differential across the chip that is important, and conceivably in an all MOS system one might have a single −17 VDC supply with respect to ground.

A two phase clock is required to operate this device. This is due to the dynamic nature of the MOS logic circuits used in its construction. This device is designed to accept clock speeds up to 1 MHz.

The MM5704 is packaged in a 24-pin cavity dual-in line package. The input-output pin configuration is shown in Figure 1 along with the pin configurations of all the MAPS elements of this set.

Pin	Arithmetic Unit (AU) MM5700	Register Unit (RU) MM5701	Timing & Control (T&C) MM5702	Control ROM (CROM) MM5703	Keyboard Interface Chip (KI) MM5704
1		RES	μI		$\overline{\text{AL OUT}}$
2	$\phi 2$		$\overline{\text{CM}}$		CS
3	RES	IO2	$\overline{\text{TE}}$	$\phi 2$	R7
4	IO2			μI	R6
5	IO1	IO1		$\overline{\text{CM}}$	R5
6	μI	$\phi 1$		$\phi 1$	R4
7	$\phi 1$		P1		R3
8	V_{SS}	V_{SS}	P2	V_{SS}	R2
9	$\overline{\text{CM}}$	$\phi 2$	$\phi 1$		Idle Key Reset
10	$\overline{\text{TE}}$	$\overline{\text{TE}}$			R1
11	$\overline{\text{PO2}}$		$\phi 2$		R0
12	$\overline{\text{PO1}}$	$\overline{\text{CM}}$	V_{SS}		V_{SS}
13	$\overline{\text{PO8}}$		FFO		$\phi 1$
14	$\overline{\text{PO4}}$		RES		$\phi 2$
15		μI			$\overline{\text{CM}}$
16	V_{GG}	V_{GG}		V_{GG}	T4
17			IO		T1
18					T2
19			DS		T3
20			B+9		T5
21					μI
22					$\overline{\text{BUS1}}$
23			A		$\overline{\text{BUS2}}$
24			V_{GG}		V_{GG}

FIGURE 1. MAPS Pin Assignments

WHAT IT DOES

In addition to the 32 character key switch closures that may be encoded, there are 8 static switches that may be interrogated. These static switches may be controlled by the user to form an 8-bit word which upon command will be sent via the keyboard interface output to the rest of the system. These switch closures are used to perform control functions. They may be used to form any desired data word especially if it is to be varied from time to time.

The output of this device is presented at Pin 21 in a bit serial fashion. This organization was required to be compatible with the bus structured organization of the five chip MAPS. The bit serial, digit serial, organization of this system was designed to keep to a minimum the number of pins required for each MOS-LSI chip used in this system. Actually, Pin 21 is a bidirectional bus, with input capability for controlling static switch interrogation, data interrogation, or control of the alarm and shift functions. In a system this is accomplished with time multiplexing. (Figure 5)

If a system contains more than 32 character key closures, the functions performed by the MM5704 may be expanded by paralleling two or more of these devices. Two devices will provide 64 key closures (128 data words), three provide 96, etc. The two key rollover and three key alarm functions will continue to function by paralleling the busy 1 (Pin 22) and busy 2 (Pin 23) signal lines. The alarm signal will be available at Pin 1 of the devices. This signal is not OR-tieable.

TWO KEY ROLLOVER

If a second key is depressed before the first key is released, a condition exists that is defined as two key rollover. In this situation, the device will acknowledge and transmit the encoded word generated by the initial key closure then acknowledge and transmit the encoded data word generated by the second key closure. At the time that the system responds to the initial key closure, the "busy 1" signal line becomes true (MOS logic "1" condition). This informs any parallel keyboard interface chips that a key closure has been detected. The "busy 1" signal will remain true until the encoded data word resulting from initial key closure has been transmitted and the key released.

If during the time that the "busy 1" signal is true and a second key closure is detected, the system will flag this condition by causing "busy 2" to go true. "Busy 2" will remain true until the encoded data word generated by the initial key closure has been transmitted and one key released. "Busy 1" will remain true until all keys are released. A key once depressed and acknowledged by the system must be released and depressed again before it will be accepted and acknowledged as valid by the system for the second time.

THREE KEY ALARM

If three or more keys are depressed, a condition exists that will be detected by the system and interpreted as the alarm condition. Because the KI chip cannot process more than two key closures, depression of more than two must alarm the system. When the alarm condition exists, a signal is generated at the alarm output (Pin 1) and an alarm pulse may be transmitted to the rest of the system via the data bus. The ability to signal the alarm condition on the data bus is a programmable feature. The signal made available at Pin 1 may be used to inform the operator of the existence of the alarm condition. The alarm condition will also be triggered if two or more keys are depressed simultaneously, such that the second key closure is detected before the first key closure can be processed and transmitted.

IDLE KEY RESET (PIN 9)

An automatic reset signal is generated during the idle key mode of operation. This mode is defined as no keys depressed and power is on. The reset signal is created by charging an external capacitor (CR) which enables the control logic to detect first key closure. The purpose of the reset is to prevent keyboard lock-up due to mass depression of the keys, or any other attempt to void the integrity of the keyboard interface chip. An example of this might be, depressing three or more keys (including the clear key) to force an alarm condition to repeat thereby voiding the keyboard logic. When such an attempt occurs, as soon as the keys are released and the bounce delay is timed out, the idle key reset enables the control logic.

The value of the reset capacitor (CR) is dependent on the keyboard scan cycle.

$$CR = \frac{i \cdot t}{V_1}$$

Where: i = average charging current = 1 mA

V_1 = reset voltage $\geq 3.0V$

t = charging time interval

$$t = \frac{E + n}{\theta_f}$$

Where: E = modulo of E counter

n = number of scan cycles beyond bounce out delay = 2

θ_f = frequency of clock θin.

Typical values for CR, that would fit most applications, range from 0.001 μF to 0.1 μF.

HOW IT WORKS

As may be seen by the simplified block diagram in Figure 2, the keyboard interface chip is partitioned into three basic logic areas. These areas are the Scan Logic, the ROM encoder (with its associated input control logic and output data converter), and the system housekeeping logic.

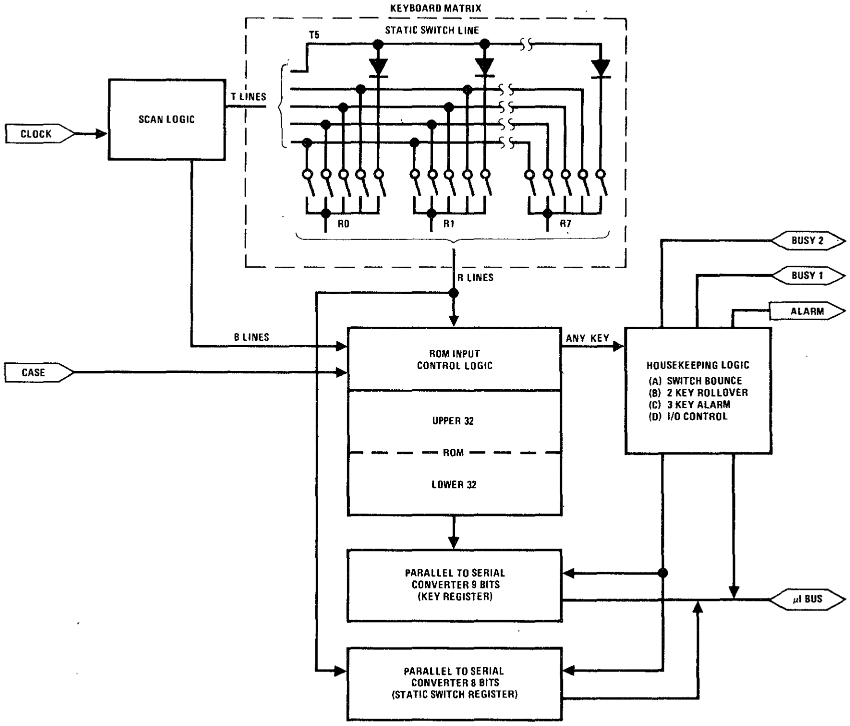


FIGURE 2. MM5704 KI Block Diagram

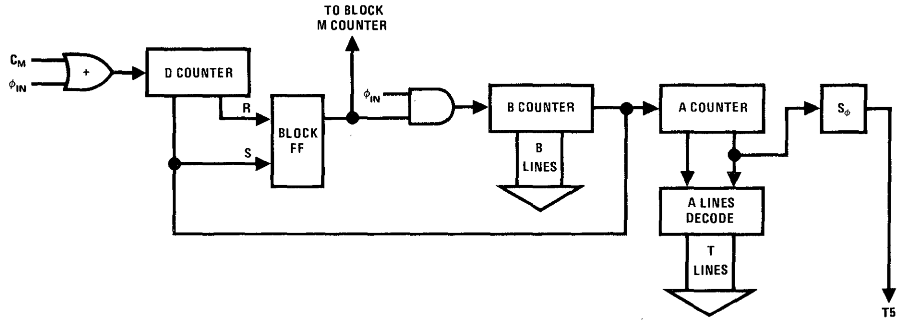


FIGURE 3. Scan Logic of MM5704

The Scan Logic will sequentially interrogate each key of the keyboard. It provides the timed interrogation pulses. The detection of a key closure is accomplished by the ROM input control logic. This results due to the R and B line being combined in an AND condition at the input to the ROM control logic. The rate at which the keyboard is scanned is basically determined by the clock input. Provision has been made internal to this logic block to compensate for the various capacitive loads that different keyboards might present. This is a programmed feature. The scan logic is shown in greater detail in Figure 3. It is designed to sequentially scan 32 keyboard switches in a 4 x 8 matrix as shown in Figure 2. The T lines enable each of the four quadrants in sequential fashion. The B lines are then used to sequentially decode the 8 R lines at the ROM input. As the A counter changes from state N to N+1 a programmable delay times out before the B counter is allowed to decode the R lines within the quadrant. This delay is necessary to allow the T line to charge the capacitance, associated with that quadrant of the keyboard switch matrix, to its full value, and discharge the capacitance associated with the last quadrant to be scanned.

The delay is accomplished through the use of the D counter in the following fashion: The same signal from the B counter output that advances the A counter sets a latch (block flip-flop) which in turn inhibits any further advancement of the B counter. It also sets the D counter to an initial state from which it must advance until a signal is generated in its output which resets the block flip-flop. This enables the B counter to advance through its cycle until its terminal state is reached and the A counter is again advanced, at which time the cycle is reinitiated. The degree of delay that is generated by the D counter is a function of the clock input to the counter and the modulus of the counter. The modulus of the D counter may be specified by the customer to be any value from 1 to 15. Either the θ in clock or the cycle marker (CM) from the system may be used to advance the D counter. Since both of the signals are generated and controlled external to the device, the delay resulting from this technique is completely adjustable over a reasonably broad range. This delay must exceed that time required by the system to fully charge or discharge any keyboard capacitance associated with any given T line. T4 duration will always be equal to and may be greater than the duration of the other T lines.

The following example will serve to clarify the use of the D counter to develop a programmed delay for a given keyboard capacitance. Assume a keyboard capacitance of 300 pF and a clock (θ) rate of 500 kHz with a pulse width of 500 ns. Also, we are given a .5 mA current source to charge the T/R line capacitance with each 500 ns clock pulse width. Using the math function:

$$V = \frac{i \,.\, t}{c}$$

Where V = the voltage developed across the capacitor

i = the charging current

t = the charging time

c = the capacitance

$$V = \frac{(15 \times 10^{-3})\ (500 \times 10^{-9})}{(.3 \times 10^{-9})} = .83V$$

We know that a voltage of 8V is a safe MOS "1" level voltage, and if our capacitance charges .83V with each clock pulse then we will need approximately 10 clock cycles to charge the T line capacitance of 8V or greater.

$$10 \times .83V = 8.3V$$

Therefore, the modulus of the D counter should be specified at 10 and it should be driven from the clock (θ) to meet the requirements of this particular keyboard.

The ROM accepts detection of any given key closure along with the "Case" signal input and produces a 9-bit parallel output. The ROM output is serialized and transmitted on the data bus at the proper time and upon command to the rest of the system. The output of the ROM will be taken from the upper 32, 9-bit words if the upper case condition is specified (Pin 2 = V_{GG}). If lower case is specified (Pin 2 = V_{SS}) the output will be generated by the lower 32, 9-bit words. The output from the ROM is loaded in parallel into a 9-bit shift register (Key Register) upon command from the housekeeping logic. This command is generated after the housekeeping logic has acknowledged a genuine key closure. A "Character Ready" signal is also sent out via the data bus to the rest of the system, at the same time. Upon receipt of the transmit signal (Xmit key) the key register will transmit its information out on the data bus in a bit serial manner, at the proper time. The contents of the ROM contain character codes that are completely specified by the customer. Therefore this device becomes in effect part of his customized system.

The static switches are interrogated by the scan logic and entered into the static switch holding register at T5 time with each scan cycle. These signals bypass the ROM and are switched directly from the static switch holding register onto the data bus serial fashion upon command from the system.

The housekeeping logic performs many timing and control functions which are initiated upon detection of a key closure or an input from the data bus. These are listed below:

1. Provides for elimination of switch bounce. (For both conditions—when the key is depressed and released). This feature is adjustable to accommodate the different switch bounce times that exist with different keyboard switches.
2. Provides two key rollover.
   (a) Detects first key closure and generates "Busy 1"
   (b) Detects second key closure and generates "Busy 2"
3. Provides three key alarm.
4. Provides the signals ("Alarm" and "Character Ready") to the data bus at the proper time.
5. Accepts input commands (Xmit key, Alarm Reset, etc.) from the data bus and processes them. (See Figure 5.)

The housekeeping logic performs most of its functions upon initiation from any key signal. This signal is generated by detecting when any of the R lines are true. Two key rollover detection is accomplished through the use of a counter (M counter) whose modulus is equal to the keyboard scan counter (33). The sequence of events is as follows: The initial key closure is detected and the "Any Key" signal is generated, which performs the following functions: It sets a flip-flop which generates the "Busy 1" signal. It initializes the M and the E counters (the E counter will be dealt with later). It sets another latch (1st character FF) which prevents any additional "Any Key" signals from affecting the state of M and E counters and the "Busy 1" latch. The M counter is now time locked to the first detected "Any Key" signal. The signal that delays the B counter in the scan logic also delays the M counter. This enables the M counter to remain time locked to the scan counters and permits multiple key depressions to be detected. The first key time slot will always be coincidental with the M counter equal to 0 time. Any other key depression will generate the "Any Key" signal at the time when the M counter doesn't equal 0. This is more clearly illustrated in Figure 4.

For purposes of illustration it is assumed that key closure was detected at scan counter time 18. The "1st character" and "busy 1" latches will remain in the true state until the system has delayed long enough to eliminate switch bounce (key closure) and acknowledges the receipt of the valid character. This action switches the contents of the ROM into its output shift register, and sends out a "data ready" signal on the data bus. The "1st character" and "busy 1" latches go false when the release of the first key is detected, again with sufficient delay to eliminate switch bounce (key release).

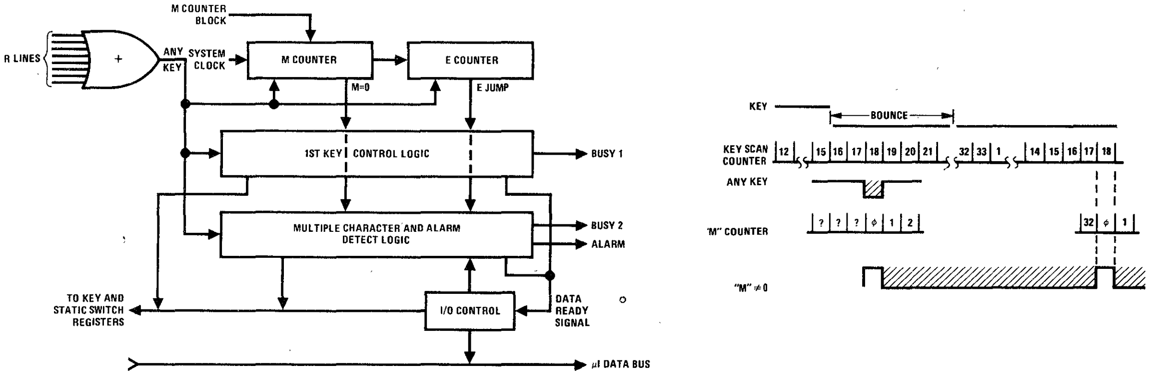


FIGURE 4. Housekeeping Logic of MM5704

The delay required to avoid switch bounce is accomplished through the use of the E counter. This counter is incremented each time the M counter completes a cycle. The E counter will continue to advance until it counts out its programmed modulus at which time all switch bounce is a thing of the past and the system is allowed to accept the initial key closure as valid. When the first key is released, the E counter is again set to its initial state and allowed to advance to its terminal state. Upon reaching its terminal state for the second time, when all switch bounce associated with the first key release is over, the reset procedure for the "1st character" and "busy 1" latches will take place. The modulus of the E counter may be varied to accommodate the switch bounce times of the various switches that may be used with this device. This is a parameter specified by the customer. The modulus of the E counter may be anything from 1 to 15.

If a second key is depressed, while the first key is held down, a sequence of events very similar to that already described will occur. The basic differences are that detection of the second key will occur as a function of the "any key" signal and the M counter not equal to 0. The data ready signal, from the first key closure, must have been serviced by the system. Otherwise, this is an alarm condition (two keys depressed simultaneously). After transmission of the first key data and detection of the second key depression, the "2nd character" and "busy 2" latches will be set. The E counter will inject its delay and the system will acknowledge and transmit the second character.

Should the system be processing two key closures and receive yet a third, the alarm latch will go true. The third key depression is detected when the "any key", $M \neq 0$", and "second character" in process" signals occur simultaneously. When the alarm latch goes true, a signal may be transmitted to the rest of the system on the data bus. The alarm latch is reset through the use of the clear key or by a reset pulse on the data bus.

The remainder of the housekeeping logic accepts the input signals from the data bus and transmits data out on the bus at the proper time. The timed sequence for the data bus associated with this device is shown in Figure 5. We have already discussed the nature of the keyboard alarm, character ready, and Xmit key signals. The alarm set and reset signals are inputs from the rest of the system that cause or remove the alarm condition. The test input is for testing purposes only. It is used to speed up the testing of this device when the inputs to the device are generated from controlled (bounce free) sources. Therefore there is no need for the normal system delays. The system could conceivably be used by the O.E.M. manufacturer for incoming receiving inspection, just as the factory uses it. A more exact understanding of its use should be acquired from the factory before it is used.

The static Xmit inputs are used to cause the keyboard interface to deliver the data stored in the static switch holding register at the immediate next appropriate time. There are four of these static Xmit input pulses to permit use of up to

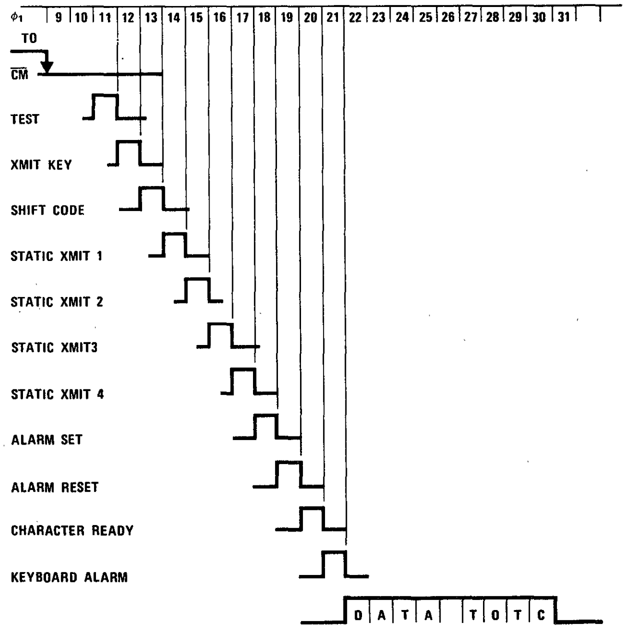


FIGURE 5. MM5704 I/O Time Slots

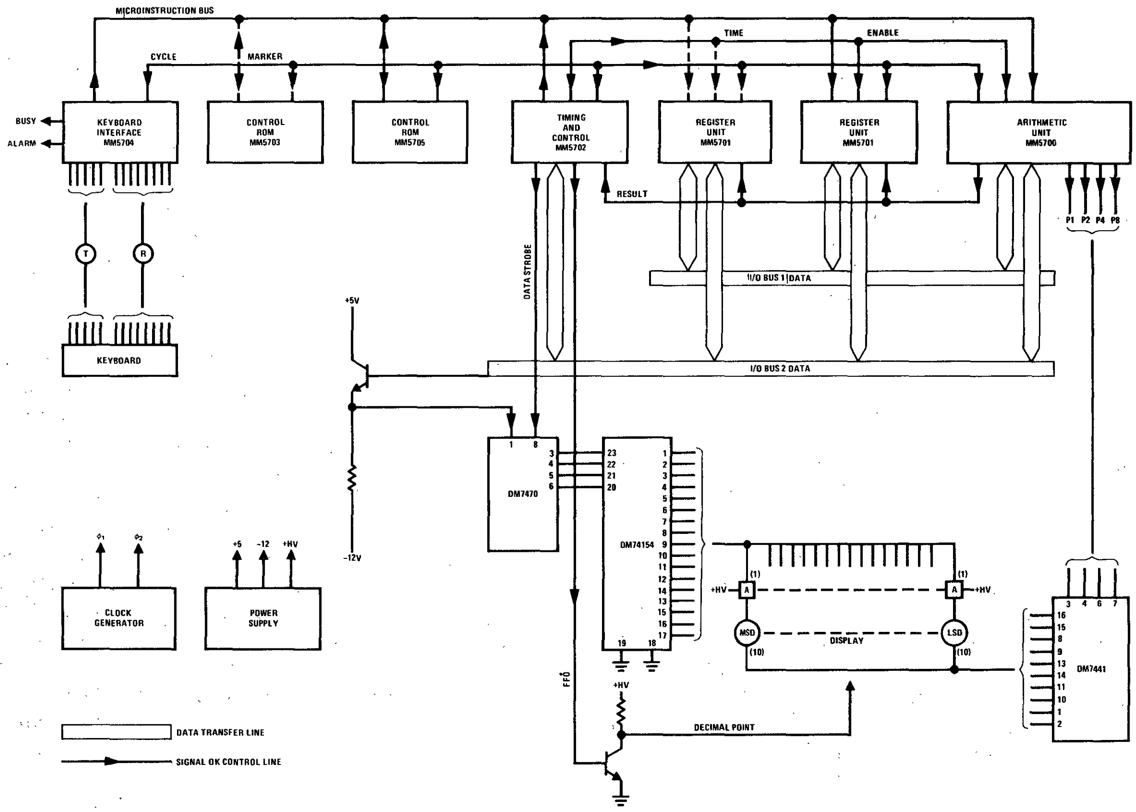


FIGURE 6. MAPS Block Diagram

four keyboard interface chips and associated static switches in parallel. The device user may specify which time slot will be used with a given device. This is especially important when two or more of these devices are to be used in a system. If this is left unspecified in a single keyboard interface chip system, this will generally be programmed to the Xmit static 1 time slot. It is an illegal condition for both a static transmit and key code transmit request to occur in the same word cycle.

THE KEYBOARD INTERFACE AS USED IN MAPS

The natural environment for this device is to operate in conjunction with the "timing and control" (T&C) chip (MM5702) of MAPS. MAPS (Microprogrammable Arithmetic Processing System) is a five MOS-LSI chip, mini-processor system. The block diagram shown in Figure 6 illustrates the system's primary components and their interconnections. Besides the clock lines and power supplies, the keyboard interface chip has a cycle marker (CM) input from the MAPS system. This signal (CM) is generated in the T & C chip from a master timing clock and is used to synchronize the entire system including the KI. This procedure is mandatory in a system, such as this, where all data as well as command and operation signals are transmitted in a serial by bit and serial by digit basis. The exchange of all information between the system blocks is time multiplexed onto single wire buses; therefore, all of the system components must be in step. The cycle marker flags the beginning of a 76 bit word cycle time. The important bit times for the KI chip in MAPS are, for example, 11 through 30. These are the bit times in any given word cycle that are allotted for the KI to communicate with the rest of the system through the T & C chip. The detailed nature of this time period is more completely defined and illustrated in Figure 5.

The various time slots are logically defined and implemented within the KI chip as follows: The CM initiates a delay line composed of a series of MOS inverters. The outputs of these inverters become true in a sequential fashion, one after another in step with each clock transition. Therefore, once the sequence is initiated at the proper time (CM) the MOS delay line will behave as a special decoded counter in step with the master counter in the T & C chip. The output of each stage will define a precise bit time with respect to the CM. This occurs within the housekeeping block (Figure 2). When the KI has acknowledged a key closure it will send out a character ready signal (bit time 20), and continue to send it until it is acknowledged by the T & C chip. The T & C chip will receive this and, in some subsequent word cycle at bit time 12, will send a transmit key

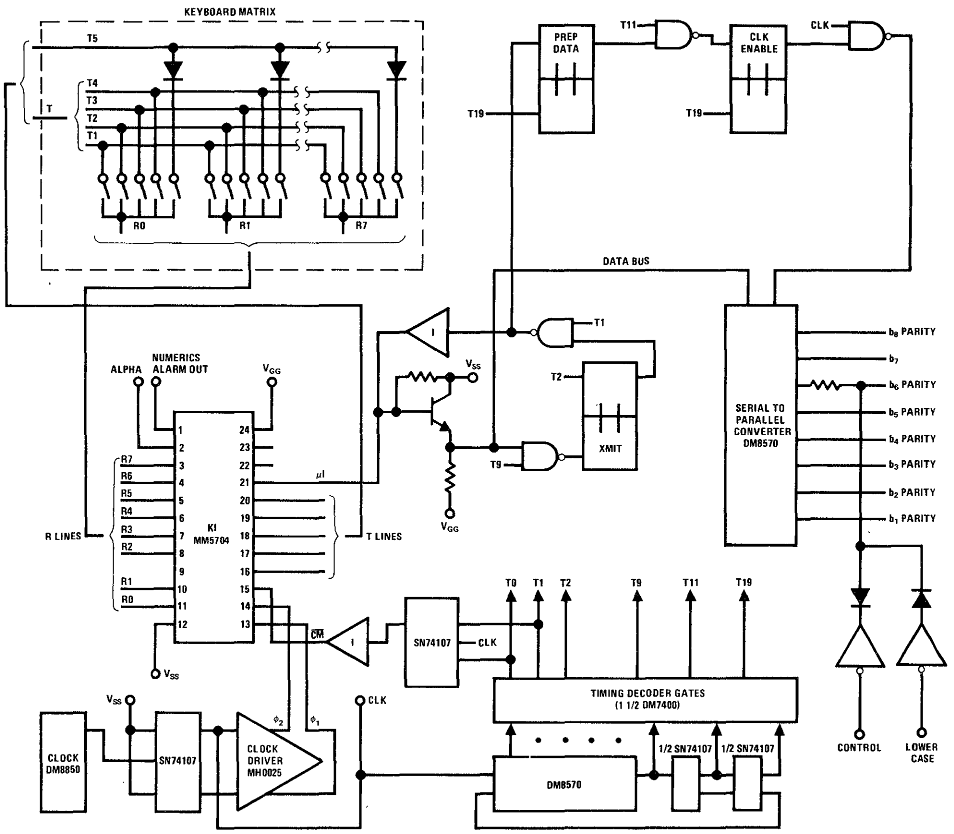


FIGURE 7. ASCII Keyboard Encoder Using the MM5704

command. This will cause the keyboard to send its data from the keyboard shift register out onto the data bus (microinstruction) during time slot 22 through 30 immediately following the receipt of the transmit command. The data bits are received by the T & C chip. The static switch information, from the keyboard, is handled in a similar manner by the system. It is the intent of this section to only deal with the interaction of the KI chip with the rest of the system. Therefore, a more detailed treatment of the operation beyond this point belongs in a description of the T & C chip, as related to MAPS.

THE KEYBOARD INTERFACE ELEMENT AS A STANDARD ASCII ENCODE SYSTEM

The MM5704 may be used quite conveniently in applications other than as part of the calculator chip system for which it was designed. To illustrate how this may be done, a small keyboard system was designed to perform the keyboard to ASCII encoding function. Only one of the MM5704s was required to provide for all 128 characters in the ASCII 7-bit communications code. This system is illustrated in Figure 7.

A two phase clock must be generated and a master counter designed to operate from the clock system. A DM8850 (9601) is used to drive a JK flip-flop in the toggle mode of operation. This forms a master clock that has an equal duty cycle. One eight bit shift register and one SN74107 is used to form a twisted ring counter. This type of counter was chosen because of the ease with which its states may be decoded. One and 1/2 quad 2 input NAND gates are used to decode the counter outputs into the discrete time slots required for the bit serial operation of the KI. Because there is no need to concern ourselves with anything other than the time slots required to operate the KI chips, the time slots have been reorganized and the word length shortened. This is more clearly defined and illustrated in Figure 8. The cycle marker signal is generated by setting a latch at time 0 and resetting it at time 1. $\overline{CM}$ is only used, in this system, by the KI chip.

The keyboard switch entry operation is accomplished exactly as described in a previous section of this application note. The KI chip will interrogate the keyboard switch matrix. The alpha/numeric control is accomplished externally by a

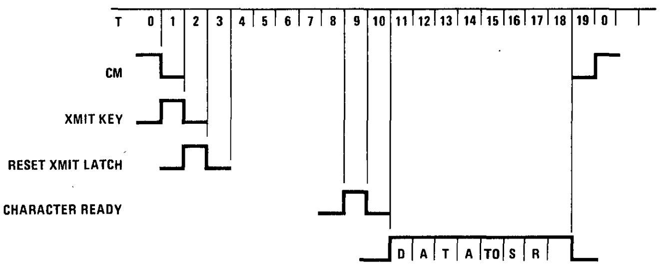


FIGURE 8. ASCII Keyboard I/O Time Slots

mechanical latch on the keyboard. If the keyboard should lack this facility, an integrated circuit latch could be added to perform this function.

At character read time (T9), the data bus (μI) is gated to an RS flip-flop. For the sake of illustrating the action sequence, let's assume that a character ready (T9) signal appears on the μI data bus and the Xmit latch is set. The data bus line is the data input to an eight bit shift register. This shift register is used to perform the serial to parallel conversion. Nothing further occurs until the next word cycle is initiated and time slot 1 is reached. The Xmit flip-flop has enabled a gate that will generate the Xmit key signal at T1 and place this on the μI bus. This will be received by the KI chip and trigger the transmission of data from the keyboard holding shift register beginning with time slot 11 and ending with time slot 18 (8 bits long). The Xmit latch will automatically be reset at time T2. The generation of the Xmit latch will automatically be reset at time T2. The generation of the Xmit key signal at T1 also causes another latch to be energized (prepare for data). This latch will enable a gate which at time T11 (the beginning of the data word) will set a clock control latch. This action enables the clock to the output shift register for 8 clock pulses. The clock enable latch is reset at time T19. The eight clock pulses to the shift register will permit the entry of the data coming from the KI μI bus and accomplish the serial to parallel conversion. At time T19, the data prep. latch is reset.

The character and control codes associated with the KI device are illustrated in Table 1. The con-

TABLE 1. ASCII Keyboard Assignments

	b_7=0		b_7=1			
		CON.	UC	LC		
	b_6=1	b_6=0	b_6=0	b_6=1		
0	SP	N+1	@	\	T4	R6
1	1	S04	A	a	T2	R0
2	"	STX	B	b	T3	R4
3	#	ETX	C	c	T3	R2
4	$	EOT	D	d	T2	R2
5	%	ENQ	E	e	T1	R2
6	&	ACK	F	f	T2	R3
7	'	BEL	G	g	T2	R4
8	(	BS	H	h	T2	R5
9	)	HT	I	i	T1	R7
10	*	LF	J	j	T2	R6
11	+	VT	K	k	T2	R7
12	,	FF	L	l	T3	R7
13	–	CR	M	m	T3	R6
14	.	S0	N	n	T3	R5
15	/	S1	O	o	T4	R0
16	0	DLE	P	p	T4	R1
17	1	DC1	Q	q	T1	R0
18	2	DC2	R	r	T1	R3
19	3	DC3	S	s	T2	R1
20	4	DC4	T	t	T1	R4
21	5	NAK	U	u	T1	R6
22	6	SYN	V	v	T3	R3
23	7	ETB	W	w	R1	R1
24	8	CAN	X	x	T3	R1
25	9	EM	Y	y	T1	R5
26	:	SUB	Z	z	T3	R0
27	;	ESC	[	{	T4	R2
28	<	FS	\	:	T4	R3
29	=	GS	]	}	T4	R4
30	>	RS	⌢	~	T4	R5
31	?	US	–	DEL	T4	R7

b_7=1=Alpha
b_7=0=Numerics

LC=alpha • b6=1
UC=alpha • b6=0

Numbers=Numerics • b6=1
Control=Numerics • b6=0

Key Legend example

TABLE 2. American Standard Code for Information Interchange

b_7 → b_6 → b_5 →					0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
Bits b_4 ↓	b_3 ↓	b_2 ↓	b_1 ↓	COLUMN → ROW ↓	0	1	2	3	4	5	6	7
0	0	0	0	0	NUL	DLE	SP	0	@	P		p
0	0	0	1	1	SOH	DC1	!	1	A	Q	a	q
0	0	1	0	2	STX	DC2	"	2	B	R	b	r
0	0	1	1	3	ETX	DC3	#	3	C	S	c	s
0	1	0	0	4	EOT	DC4	$	4	D	T	d	t
0	1	0	1	5	ENQ	NAK	%	5	E	U	e	u
0	1	1	0	6	ACK	SYN	&	6	F	V	f	v
0	1	1	1	7	BEL	ETB	'	7	G	W	g	w
1	0	0	0	8	BS	CAN	(	8	H	X	h	x
1	0	0	1	9	HT	EM	)	9	I	Y	i	y
1	0	1	0	10	LF	SUB	*	:	J	Z	j	z
1	0	1	1	11	VT	ESC	+	;	K	[	k	{
1	1	0	0	12	FF	FS	,	<	L	\	l	:
1	1	0	1	13	CR	GS	–	=	M	]	m	}
1	1	1	0	14	SO	RS	.	>	N	⌢	n	~
1	1	1	1	15	SI	US	/	?	O	–	o	DEL

This coded character set is to be used for the general interchange of information among information processing systems, communication systems, and associated equipment.

trol codes are identical with the numerics section of this device, except that bit b6 is a logic "0" instead of "1". The lower case letters are the same as the capital letters (alpha section) except that bit b6 is a logic "1" instead of "0". A glance at the 7-bit ASCII standard MAPS (Table 2) will show this to be consistent with the accepted standard. The manner in which this is implemented in our stand alone system is as follows: When the control key is depressed bit b6 is slaved low in the output of the serial to parallel shift register, then if the numeric characters are being generated by the KI, control codes will result in the output of the shift register. If character key $, for example, was depressed, the resulting data code from the serial to parallel converter would be modified from 01001000 ($) to 00001000 (EOT).

The features of the KI chip will permit a more elaborate system than this, but this is all that is required to accomplish the use of the KI chip into a bipolar system. The total parts count is as follows:

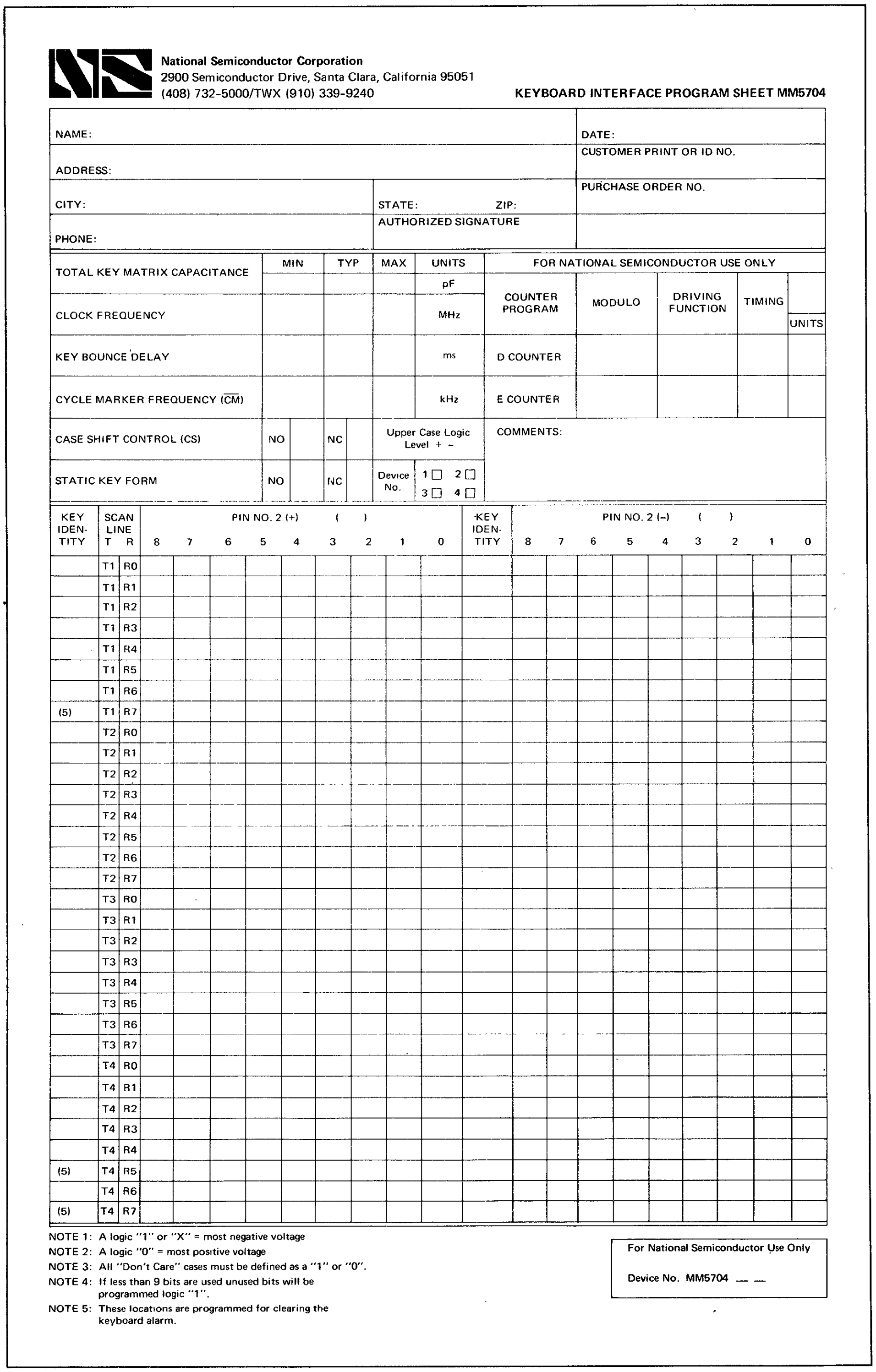
1 – MM5704
1 – DM8850
2 – SN74107
1 – MH0025
1 – DM8800
2 – DM8570
4 – DM7400
1 – SN7404

PROGRAMMING THE KEYBOARD INTERFACE CHIP

Within this device, there are nine areas that may be specified, or programmed, by the customer. The largest of these is the encoding ROM with its 64 9-bit words. The ROM is actually programmed during the process with a masking step that either leaves or removes gate oxide from a given node depending upon whether a 1 or 0 is desired from that node. To assist in programming the modulus of D and E counters, which may vary from 1 to 15, vital information pertaining to keyboard performance is required. This information will enable the KI chip to overcome T line delays and switch bounce as explained in an earlier section of this article. The D counter clock may also be specified to be either θ in or $\overline{CM}$. The fifth area to be specified as the static switch recognition code. If more than one chip is used in any given system, each chip must be given a unique internal code that will enable it to respond when the system calls for static switch data from a specific device.

The sixth area to be defined is an option that will permit the static switch information to be generated from normally open, or normally closed, switch contacts. The seventh programmable function permits specifying the shift key switch as either normally open or closed. Within the chip itself, these functions are implemented by inserting, or not inserting an inverter in the appropriate place. Programmable function number eight permits the user to inhibit or transmit the alarm pulse on the μI bus. Number nine specifies whether the system will accept or reject, set and reset alarm pulses from the μI bus. These latter conditions result from making or not making the appropriate internal connections.

Figure 9 is a copy of the form used to manually program this device. Because a great deal of the actual process involved in programming this device is accomplished with the use of a computer, a normal computer input such as IBM cards may be submitted by the customer to program this device.



National Semiconductor Corporation
2900 Semiconductor Drive, Santa Clara, California 95051
(408) 732-5000/TWX (910) 339-9240

KEYBOARD INTERFACE PROGRAM SHEET MM5704

NAME:
DATE:
ADDRESS:
CUSTOMER PRINT OR ID NO.
CITY:
STATE:
ZIP:
PURCHASE ORDER NO.
PHONE:
AUTHORIZED SIGNATURE

	MIN		TYP		MAX	UNITS
TOTAL KEY MATRIX CAPACITANCE						pF
CLOCK FREQUENCY						MHz
KEY BOUNCE DELAY						ms
CYCLE MARKER FREQUENCY ($\overline{CM}$)						kHz
CASE SHIFT CONTROL (CS)	NO		NC		Upper Case Logic Level + –	
STATIC KEY FORM	NO		NC		Device No.	1 ☐ 2 ☐ 3 ☐ 4 ☐

FOR NATIONAL SEMICONDUCTOR USE ONLY

COUNTER PROGRAM	MODULO	DRIVING FUNCTION	TIMING	UNITS
D COUNTER				
E COUNTER				

COMMENTS:

KEY IDEN-TITY	SCAN LINE T	R	PIN NO. 2 (+) ( ) 8	7	6	5	4	3	2	1	0	KEY IDEN-TITY	PIN NO. 2 (–) ( ) 8	7	6	5	4	3	2	1	0
	T1	R0																			
	T1	R1																			
	T1	R2																			
	T1	R3																			
	T1	R4																			
	T1	R5																			
	T1	R6																			
(5)	T1	R7																			
	T2	R0																			
	T2	R1																			
	T2	R2																			
	T2	R3																			
	T2	R4																			
	T2	R5																			
	T2	R6																			
	T2	R7																			
	T3	R0																			
	T3	R1																			
	T3	R2																			
	T3	R3																			
	T3	R4																			
	T3	R5																			
	T3	R6																			
	T3	R7																			
	T4	R0																			
	T4	R1																			
	T4	R2																			
	T4	R3																			
	T4	R4																			
(5)	T4	R5																			
	T4	R6																			
(5)	T4	R7																			

NOTE 1: A logic "1" or "X" = most negative voltage
NOTE 2: A logic "0" = most positive voltage
NOTE 3: All "Don't Care" cases must be defined as a "1" or "0".
NOTE 4: If less than 9 bits are used unused bits will be programmed logic "1".
NOTE 5: These locations are programmed for clearing the keyboard alarm.

For National Semiconductor Use Only

Device No. MM5704 __ __

FIGURE 9. KI Programming Form

The input must, however, follow the format as illustrated in Table 3. The output bit pattern is converted to a three digit decimal number. Each card contains eight of these numbers using the first 32 columns on the card. The associated address (Tx, Rx) is specified by card number and output digit location. Only the ROM portion of the keyboard interface chip may be programmed. All other programmable features must be specified in another fashion.

TABLE 3. Computer Programming Format

		R7	R0	R5	R1	R2	R3	R4	R6	
L.C.	T1	XXX	XXX	XXX	XXX	XXX	XXX	XXX	XXX	1st Card
	T2	XXX	XXX	XXX	XXX	XXX	XXX	XXX	XXX	2nd Card
	T3	XXX	XXX	XXX	XXX	XXX	XXX	XXX	XXX	3rd Card
	T4	XXX	XXX	XXX	XXX	XXX	XXX	XXX	XXX	4th Card
U.C.	T1	XXX	XXX	XXX	XXX	XXX	XXX	XXX	XXX	5th Card
	T2	XXX	XXX	XXX	XXX	XXX	XXX	XXX	XXX	6th Card
	T3	XXX	XXX	XXX	XXX	XXX	XXX	XXX	XXX	7th Card
	T4	XXX	XXX	XXX	XXX	XXX	XXX	XXX	XXX	8th Card

Column 1

Example (for column 1)

Number R7, T1	Bit 8	–	–	–	–	–	–	–	Bit 0 (1st out)
	1	0	0	1	0	1	1	1	0
Output Conversion Example	256	128	64	32	16	8	4	2	1

= 2
4
8
32
256
302

L.C. = lower case
U.C. = upper case

AN-55 Low Frequency Operation with Dynamic Shift Registers

Application Notes

OCTOBER 1971

LOW FREQUENCY OPERATION WITH DYNAMIC SHIFT REGISTERS

In many dynamic shift register applications, it is advantageous to operate the circuit at low clock frequencies or in clock burst modes where high frequency clock rate periods are followed by long intervals in which the clocks are absent. To insure that his system will operate correctly under these conditions, the designer should be aware of the limitations of the type of shift register he is using.

There are two basic forms of dynamic shift register cells: the ratioless and the ratio. The ratioless circuit of Figure 1a is based on a capacitor precharge concept. During ϕ_{IN} clock time, node B is precharged by transistor Q_3; i.e., Q_3 is turned on by ϕ_{IN}, creating a low impedance path from node B to V_{GG} which charges the node capacitor C_2 to a negative voltage. Data is coupled at the same time through transfer transistor Q_1 to node A, the gate of Q_2. If the incoming data is a positive or "0" level, Q_2 will be in a high impedance off state, and node B will charge to a negative voltage one threshold more positive than the ϕ_{IN} clock amplitude. When ϕ_{IN} returns to a positive level. Q_3 is shut off, isolating the precharged voltage of node B. The stored charge of node B, coupled with an additional increment contributed by C_4, redistributes between nodes B and C when the ϕ_{OUT} clock turns on transistor Q_4. The redistributed charge develops a negative voltage "1" level across C_3 which becomes isolated when ϕ_{OUT} returns to a "0" level. The "1" level turns on Q_5, resulting in a low impedance path between the output of the cell and V_{SS}, establishing a "0" level at the output.

In the ratioless cell, there are two nodes which become isolated from any charge replenishing source during normal operation of the circuit: nodes B and C. These are the nodes which establish the low frequency limitations of the cell. In most designs node C, the gate of the logic transistor Q_5, is the limiting node because total capacitance is less. If we had assumed the initial data coupled by Q_1 during ϕ_{IN} to be a "1" level, then node A would of course be the limiting node of the cell.

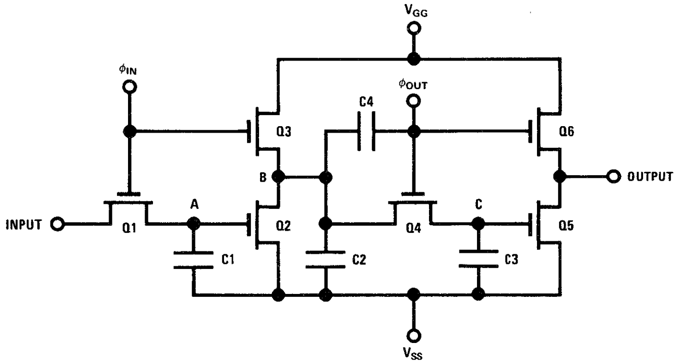


FIGURE 1a. Ratioless Dynamic Shift Register Cell

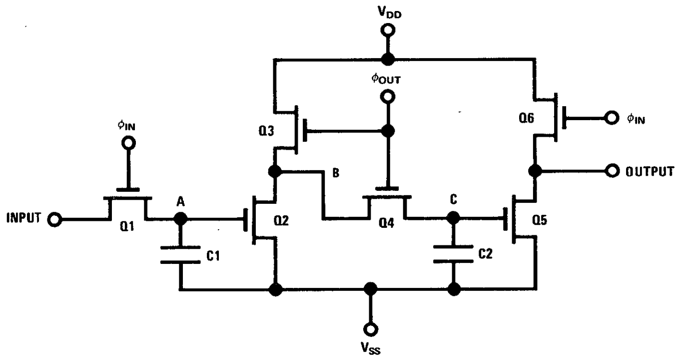


FIGURE 1b. Ratio Type Dynamic Shift Register Cell

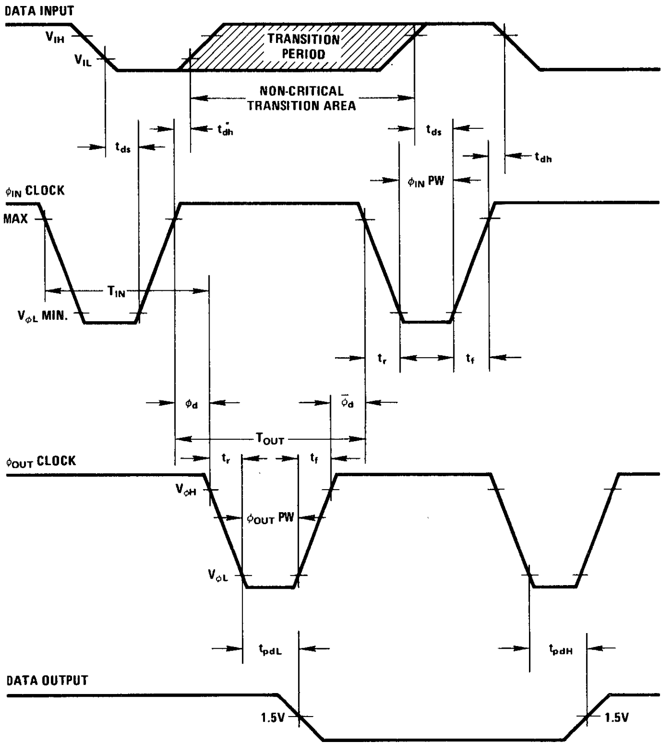


FIGURE 2. Timing Diagram For Two Phase Dynamic Shift Registers

The ratio dynamic shift register cell of Figure 1b has only one isolated node which limits minimum frequency operation. It, like the ratioless cell, is the gate node of the logic transistor. The ratio cell does not rely on stored precharge to establish a "1" level on a succeeding logic gate mode. If a "0" level had been transferred to node A of the ratio cell by Q_1 during ϕ_{IN} time, Q_2 would be off. A ϕ_{OUT} "1" level would turn on Q_3 and Q_4 creating a charging path between node C and V_{DD}, resulting in a "1" level at node C. The node would be isolated by Q_4, just as in the ratioless cell, when ϕ_{OUT} returns to a "0" level.

If the data coupled by Q_1 had been a "1", both Q_2 and Q_3 would be on during ϕ_{OUT} time. To establish a "0" at node B in that case, an electrical ratio between the on impedance of Q_2 and Q_3 must be considered by the cell designer.

Charge must be stored at the logic transistor gate node of the ratioless cell for the period of time between leading edges of the two phase clocks. This is because no charge enters the node B and C network after the leading edge of the transfer clock (ϕ_{OUT}) and there is no way for charge which leaks off the nodes to be replaced. This portion of the clock period is defined as a Partial Bit Time. The Partial Bit Time between the leading edge of ϕ_{IN} and the leading edge of ϕ_{OUT} is the T_{IN} period, and the time between the leading edge of ϕ_{OUT} and the leading edge of ϕ_{IN} is T_{OUT} (Figure 2).

The period of the minimum operating frequency is the sum of the two, or

$$\phi_f\,(\mathrm{MIN}) = \frac{1}{T_{IN} + T_{OUT}} \qquad (1)$$

Obviously the lowest operating frequency can be attained when T_{IN} and T_{OUT} are each at their maximum limit and therefore equal. This says that for minimum frequency, 50% clock phasing should be used, i.e., the clocks should be equally spaced within the bit time.

The ratio cell has a similar storage requirement, but with one difference. During the time the transfer clock (ϕ_{OUT} in Figure 1b) is on, a source of charge is available to node C through the ON transistors Q_3 and Q_4, assuming Q_2 is OFF. Therefore, charge must be stored on the critical capacitor C_2 only after the transfer clock has returned to a "0" level, and isolated the node. This required storage time is usually referred to as Clock Phase Delay Time (ϕ_d). The phase delay time between the trailing edge of ϕ_{IN} and the leading edge of ϕ_{OUT} is ϕ_d; the time between the trailing edge of ϕ_{OUT} and the leading edge of ϕ_{IN} is $\overline{\phi}_d$ (Figure 2). Minimum clock operating frequency is:

$$\phi_f\,(\mathrm{MIN}) = \frac{1}{\phi_{IN}\,\mathrm{PW} + \phi_d + \phi_{OUT}\,\mathrm{PW} + \overline{\phi}_d} \qquad (2)$$

assuming clock rise and fall time $<< \phi_{PW}$.

Optimum low frequency operation can be obtained when the clock pulsewidths and phase delays are maximized and made equal. In most cases this would mean 10 μs clock pulsewidths and 50% clock phasing. For power or system application reasons it is usually not convenient to use such wide pulsewidths, and the minimum clock frequency is simplified to

$$\phi_f\,(\mathrm{MIN}) \cong \frac{1}{\phi_d + \overline{\phi}_d} \qquad (3)$$

assuming $\phi_{PW} << \phi_d$ or $\overline{\phi}_d$.

Maximum Partial Bit Times and Clock Phase Delays for a given circuit are a measure of the ability of the critical nodes within the cell to store a minimum voltage level. Charge is usually lost due to leakage currents associated with the semiconductor junctions of the nodes. The total reverse leakage current for a p-n junction is the sum of three components; the bulk diffusion current, charge generation current and surface leakage current. Within the normal operating junction temperature range of MOS shift registers (−55°C to 150°C), the charge generation current is the primary component of leakage. Charge generation is usually attributed to recombination centers within the depletion layer of the junction. Leakage current generated in this manner is usually approximated by the expression

$$I_L = KT^{3/2}\,\epsilon\ {-7020/T} \qquad (4)$$

Where T = Junction temperature, °K
K = Proportionality constant
I_L = Leakage current of P-N junction

Therefore Partial Bit Times and Clock Phase Delays will be a definite function of temperature. Figure 3 shows a curve for Partial Bit Times as a function of temperature for a typical shift register using a ratio-less cell. Figure 4 gives the corresponding minimum operating frequency versus temperature for two cases: when $T_{IN} = T_{OUT}$ (50% clock phasing), and when one of the Partial Bit Times is minimized, the other maximized. Minimum Partial Bit Time is:

$$T_{(MIN)} = \phi\,\mathrm{PW}_{(MIN)} + \phi_{tr} + \phi_{tf} + \phi_{d(MIN)} \qquad (5)$$

Any Partial Bit Time between minimum and maximum at a given temperature can be used. The minimum clock rate would be calculated using Equation 1.

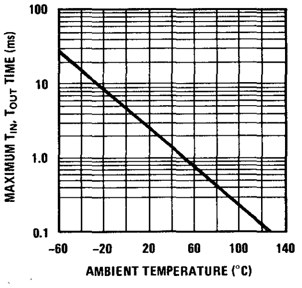


FIGURE 3. Maximum Partial Bit Time vs Ambient Temperature

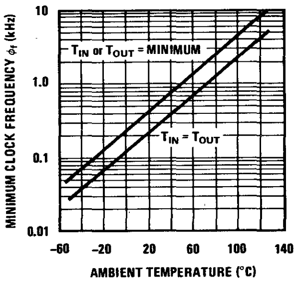


FIGURE 4. Minimum Clock Frequency vs Ambient Temperature

If the shift register utilizes a ratio cell, a curve identical to Figure 3 could be used to obtain maximum Clock Phase Delays for any required temperature. Equation 2 or Equation 3 could then be used to calculate minimum clock frequency at that temperature.

The shift register user can often increase his margin of safety when operating at low frequency, or for long periods of time with the clocks stopped, by designing the system with that operation in mind. The ambient operating temperature of the registers should always be minimized. The cell requires a minimum voltage at the critical node to operate, and the time to discharge the node to that value is dependent upon the initial voltage, as well as capacitance and leakage:

$$t_d \approx \frac{C_{NODE}\,(V_{INITIAL} - V_{MIN})}{I_L} \qquad (6)$$

t_d = T_{IN} or T_{OUT} for ratioless cells;
= ϕ_d or $\overline{\phi}_d$ for ratio cells
C_{NODE} = Total capacitance at critical node
$V_{INITIAL}$ = Voltage at critical node immediately after isolation of that node by transfer clock.
V_{MIN} = Minimum voltage required at critical node for operation.
I_L = Total leakage current at critical node.

The initial voltage can be optimized in two ways: by using the highest clock amplitude possible and by allowing something greater than minimum clock pulsewidth to insure that the maximum amount of charge is coupled to the node (and in the case of the ratioless cell, that the maximum precharge voltage is obtained before transfer). A high value of V_{GG} or V_{DD}, the negative supply voltage, increases on-chip power and therefore junction temperature, as well as increasing the minimum required node voltage. It is a good idea, therefore, to stay away from very high supply voltages. When both the clock driver reference voltage and V_{GG} or V_{DD} are the same supply, the best tradeoff is toward the higher end of the specified range, however. One other consideration which applies during operation at any frequency, but particularly at low frequency, is excursions of the clock line more positive than V_{SS}. This forward biases internal junctions which results in parasitic PNP transistors. If the collector of the parasitic PNP happens to be a critical node, the circuit will fail. Because critical nodes are often closer to the minimum required voltage during low frequency operation, registers are usually more sensitive to positive clock spikes.

When calculating temperature effects of a system operating in the clock burst mode, the designer must remember that power dissipation in the shift register is approximately double at 2.5 MHz what it is at 100 kHz. High frequency bursts will heat the chip, causing high junction temperatures which reduce the time the clocks can be off.

SUMMARY

Dynamic shift registers can be operated at very low clock rates if manufacturers data sheets are consulted and the proper clock phasing is used. Added margin can be designed into systems by keeping clock amplitudes high, the clock pulsewidths 10 to 20% wider than specified minimums, power supplies low and temperatures as low as possible. Beware of circuit board hot spots which increase the temperature of individual packages, or extensive interlead coupling or ringing which could result in positive clock spikes.

Application Notes

JANUARY 1971

AMERICAN AND EUROPEAN FONTS IN STANDARD CHARACTER GENERATORS

Ten popular American and European 64-character subsets for displays and printers are now available from National as single-chip, standard character generators. These parts, listed in Table 1, are sold off-the-shelf without a ROM masking charge.

The ROMs are static, bipolar-compatible types, operating without clocks on standard power supplies. Row and column access times are typically 450 and 700 ns respectively. An MM4240/MM5240 2560-bit ROM is used for the 5 x 7 horizontal-scan fonts and an MM4241/MM5241 3072-bit ROM for the 7 x 5 vertical-scan fonts. The MM4240 and MM4241 operate at −55°C to +125°C and the MM5240 and MM5241 at −25°C to +70°C.

Input-output configurations and character formats for the ROMs are shown in Figures 1 and 2. Application Note *AN-40 The Systems Approach to Character Generators* gives examples of line and column address-control logic, and CRT and printer operating techniques.

Note that each ROM has a chip-enable input to permit multi-ROM operation with common control logic. For instance, two horizontal-scan ASCII character generators may be operated in tandem to obtain upper and lower-case characters. In this case, chip-enable would be controlled with bit b_6 of the normal 7-bit ASCII code, and its complement, $\overline{b}_6$.

TYPE NUMBER	CODE	64-CHARACTER SUBSET	FIGURE
Horizontal Scan (5 x 7)			
MM4240AA/MM5240AA	ASCII	Upper-case alphanumeric	3
MM4240AE/MM5240AE	ASCII	Lower-case alpha and symbols	4
MM4240ABU/MM5240ABU	Hollerith	Upper-case alphanumeric	5
MM4240ABZ/MM5240ABZ	EBCDIC-8	Upper-case alphanumeric	6
MM4240ACA/MM5240ACA	EBCDIC	Upper-case alphanumeric (IBM)	7
Vertical Scan (7 x 5)			
MM4241ABL/MM5241ABL	ASCII	Upper-case alphanumeric	8
MM4241ABV/MM5241ABV	ECMA	Upper-case A/N, Scandinavian	9
MM4241ABW/MM5241ABW	ECMA	Upper-case A/N, German	10
MM4241ABX/MM5241ABX	ECMA	Upper-case A/N, general European (French, British, Italian)	11
MM4241ABY/MM5241ABY	ECMA	Upper-case A/N, Spanish	12

TABLE 1. Single-Chip, Standard Horizontal-Scan and Vertical-Scan Character Generators

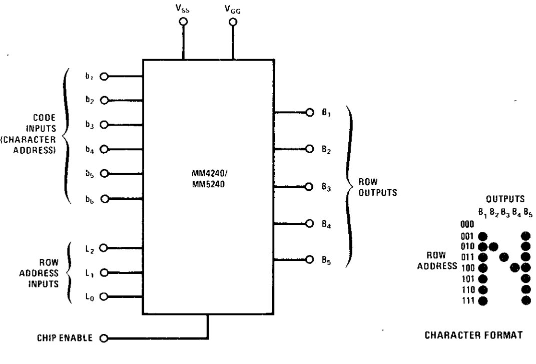


FIGURE 1. Horizontal-Scan Character Generator ROM

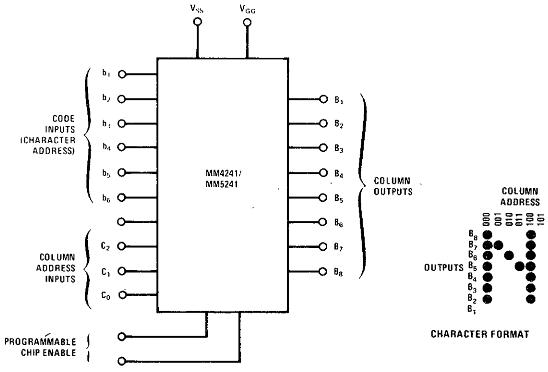


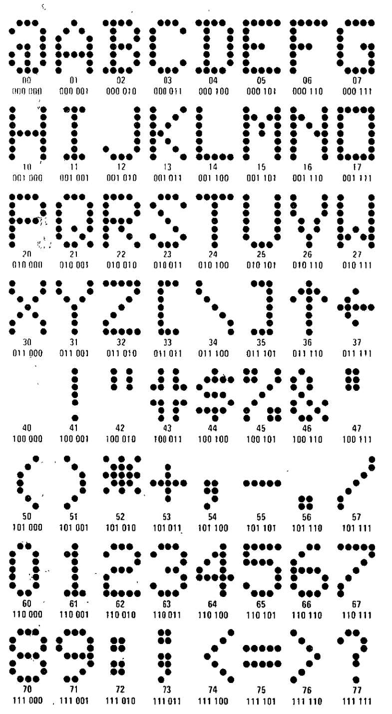
FIGURE 2. Vertical-Scan Character Generator ROM

HORIZONTAL SCAN FONTS

The subsets of 64 5 x 7 characters in the horizontal-scan fonts are the ones most commonly used in low-cost TV and CRT raster-scan displays and dot-matrix line printers.

MM4240AA/MM5240AA contains the ASCII-6 preferred graphic subset, formed from ASCII-7 by ignoring bit b_6. The remaining six bits form two octal address characters. One is formed by the three more significant bits, b_7, b_5 and b_4, and the second by b_3, b_2 and b_1.

Also, characters 36 and 37 in ASCII (x3.4 1968)* are respectively a carat (or circumflex), and an underscore. These are awkward in a video display, so they are replaced by the more useful arrows. (The arrows are related to characters in an older teletypewriter set.) This font, shown in Figure 3, is also described on the MM4240/MM5240 data sheet (which should be referred to for operating characteristics of all the horizontal-scan character generators).



Input addresses are in six bit ASCII code and are shown in the squence A_5, A_4, . . A_0; the octal equivalent is also shown for reference.

FIGURE 3. MM4240AA/MM5240AA Horizontal-Scan ASCII-7 Graphic Subset

MM4240AE/MM5240AE generates unique symbols describing the ASCII-7 control codes, as well as lower-case letters (Figure 4). The designer may not wish to display or dot-print the symbols. Since the symbols are generated only when the most significant address bit is logic "0", this bit line may be used to disable the chip, and blank the screen when control signals are transmitted. If not, the system designer can use the symbols as he likes.

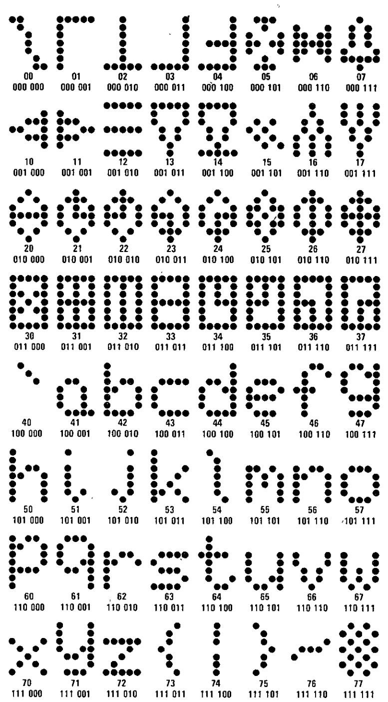


FIGURE 4. MM4240AE/MM5240AE Horizontal-Scan ASCII-7 Lower-Case Graphic and Control Symbol Subset

The Hollerith character subset in Figure 5b is formed by using six gates to compress the 12-line Hollerith code to the 6-bit address for 64 characters, as shown in Figure 5a

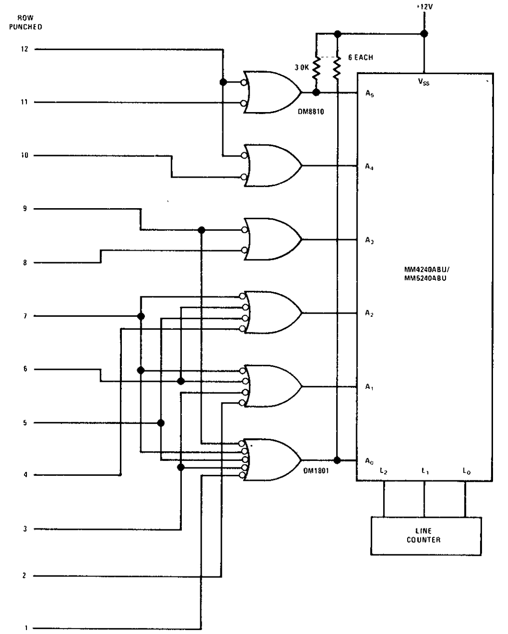


FIGURE 5a. MM4240ABU/MM5240ABU Typical Address Inputs

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*American National Standards Institute (ANSI)

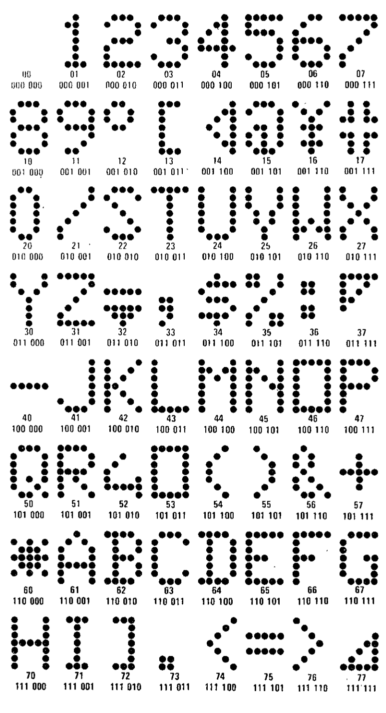


FIGURE 5b. MM4240ABU/MM5240ABU Horizontal Scan Hollerith Graphics Subset

As shown in Figure 6, an ASCII-compatible subset is provided by the EBCDIC-8 character generator (MM4240ABZ/MM5240ABZ) by simply ignoring the two most significant bits, b_0 and b_1, in the EBCDIC-8 code. The ABZ version follows the ANSI standard, while the ACA version follows the IBM style. A cent sign, and IBM's logical OR and logic NOT signs are given by the ACA subset (characters 12, 17, and 37). And a plus or minus sign is provided, as character 52. (See Figure 7.)

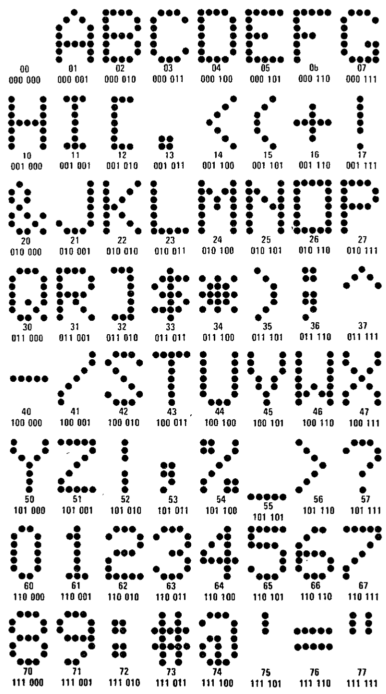


FIGURE 6. MM4240BABZ/MM5240BABZ Horizontal-Scan EBCDIC-8 Graphic Subset

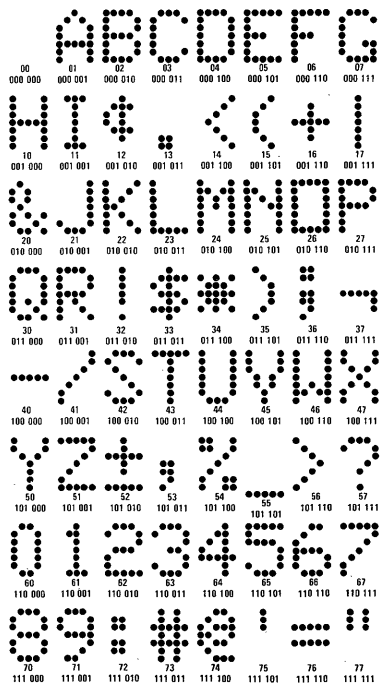


FIGURE 7. MM4240ACA/MM5240ACA Horizontal-Scan IBM EBCDIC Graphic Subset

VERTICAL SCAN FONTS

All five of the standard vertical-scan subsets in Figures 8 through 12 are generated with 6-bit codes derived from code recommendations R646 of the International Organization for Standardization. These recommendations cover ASCII-7, European ECMA-7 and CCITT alphabet number 5.

The ASCII subset for American use, in Figure 8, is practically identical to the horizontal-scan subset. Those in Figures 9 through 12 follow preferred character styles in the countries indicated. The underscore (character 37) is dropped below the line so that it may be used as a cursor.

Vertical-scan character generators are generally used in dot-matrix tape printers, ink-dot spray printers and high-definition sawtooth or pedestal-scan CRT displays. They may also be used to control raster-scan TV tubes or CRTs if the tube is turned on its side so that the raster scan is made vertically to provide a page-like format.

With standard programming, the bits in the column outputs are sequenced for a sawtooth scan with dot columns running in the same direction, as illustrated in Figure 13a. For a pedestal scan, Figure 13b, alternate columns can be reversed by putting an 8-bit shift left/shift right TTL shift register (DM74198) on the output as illustrated in Figure 14.

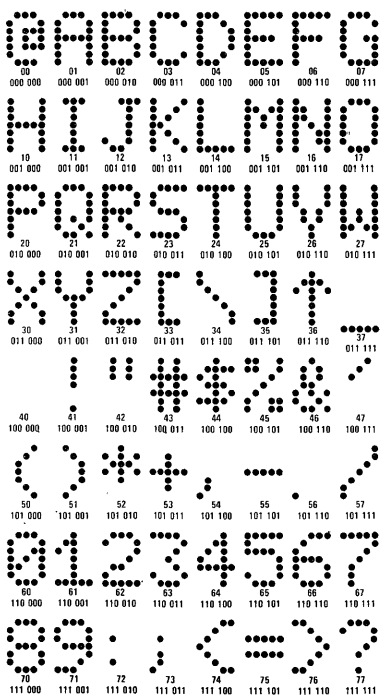


FIGURE 8. MM4241ABL/MM5241ABL Vertical-Scan ASCII-7 Graphic Subset

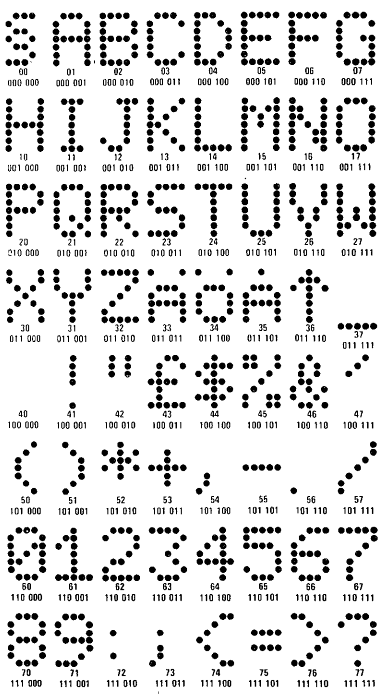


FIGURE 9. MM4241ABV/MM5241ABV Vertical Scan ECMA-7 Font for Scandinavian Use

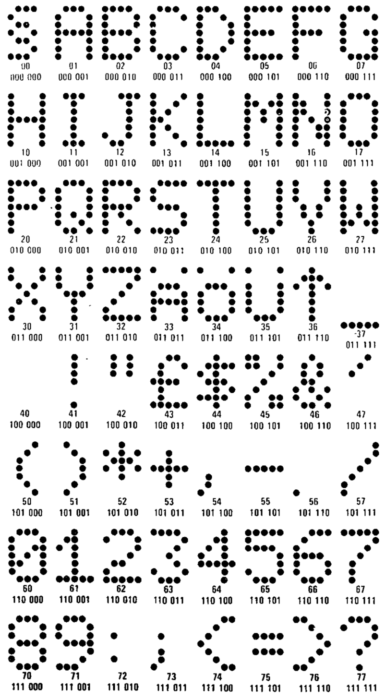


FIGURE 10. MM4241ABW/MM5241ABW Vertical-Scan ECMA-7 Font for German Use

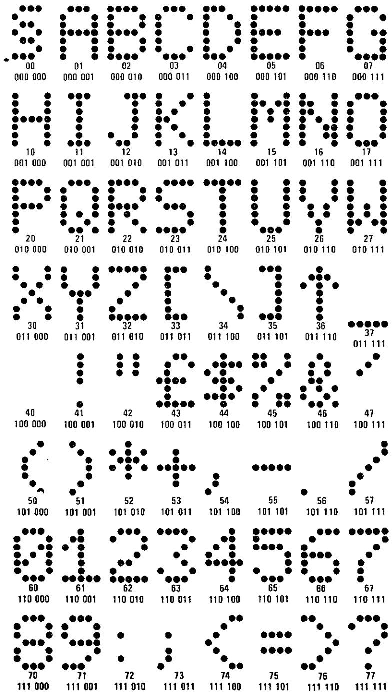


FIGURE 11. MM4241ABX/MM5241ABX Vertical-Scan ECMA-7 Font for General European Use (French, British, Italian)

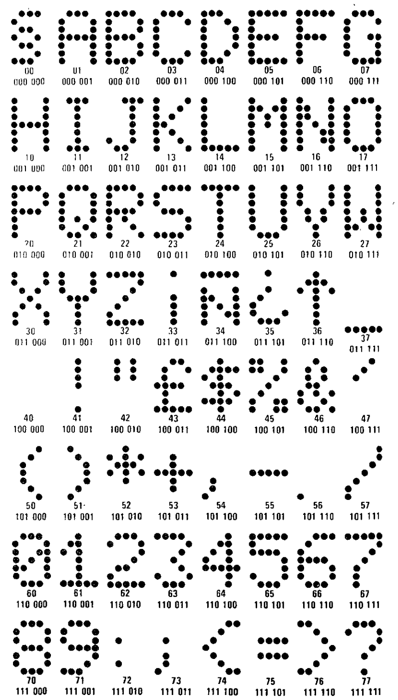


FIGURE 12. MM4241ABY/MM5241ABY Vertical-Scan ECMA-7 Font for Spanish Use

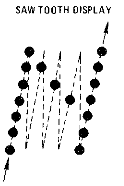


FIGURE 13a. Sawtooth Vertical Scan

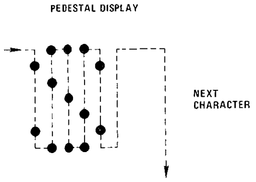


FIGURE 13b. Pedestal Vertical Scan

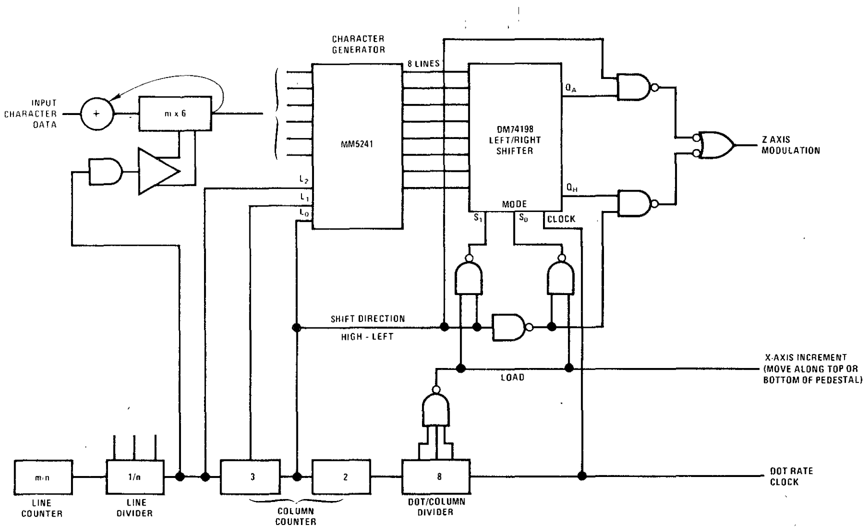


FIGURE 14. Conversion of Sawtooth Output to Pedestal Scan

CUSTOM FONTS

The two ROMs can also be custom-programmed to provide special characters, or fonts larger than 5 x 7. The MM4240/MM5240 actually stores 64 5 x 8 characters or character segments and the MM4241/MM5241 stores 64 8 x 6 characters or segments. They are not limited to 5 x 7 and 7 x 5. For example, the extra height may be used in an otherwise 5 x 7 font to drop the tails of commas, semicolons and lower-case letters below the bottom line of the capital letters. Fonts as large as 16 x 12 are entirely practical without additional control logic, using the chip-enable feature of four MM5241s. Large-font organizations are discussed in AN-40.

Briefs

JANUARY 1970

TRIG FUNCTION GENERATORS

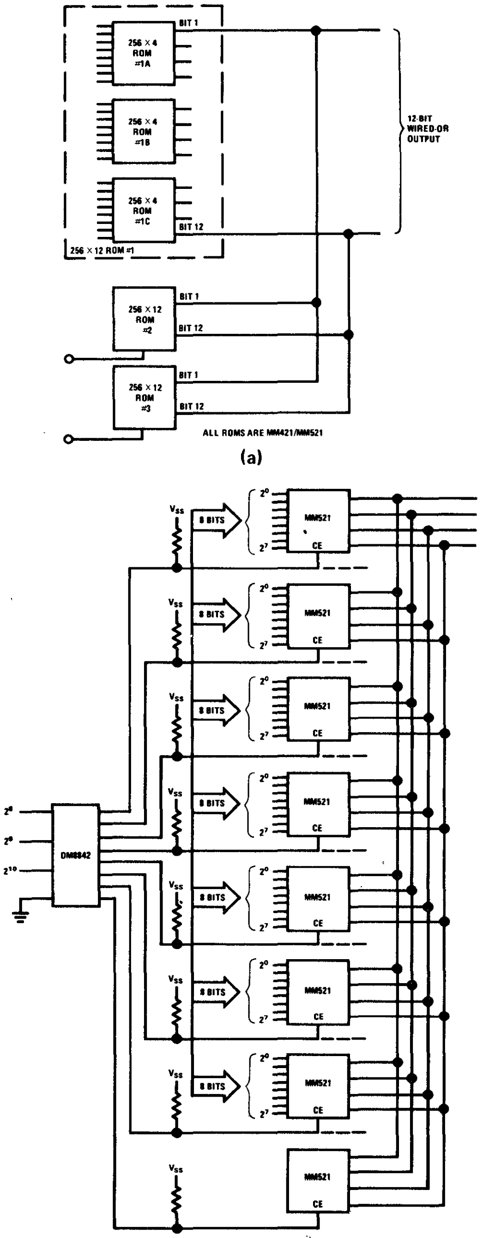
Accuracy is the major design variable of trigonometric lookup tables built with MOS read-only memories. Only a few ROMs are needed for most practical applications, but accuracy can be made to increase very rapidly with memory capacity if interpolation techniques are used.

For instance, without interpolation a single 1024-bit ROM can store 128 angular increments and generate an 8-bit output that will be better than 99.9% of the handbook value (Table 1).

ADDRESS	DEGREES	BINARY OUTPUT	DECIMAL SINE
0	0	.00000000	0.000
1	0.7	.00000011	0.012
2	1.4	.00000110	0.023
3	2.1	.00001001	0.035
•			
•			
•			
127	89.3	.11111111	0.996

TABLE 1. MM422BM/MM522BM Sine Function Generator

If one simply cascaded ROMs to improve input resolution and output accuracy for a high-accuracy trig solution (X=sin θ) as in Figure 1, large numbers of ROMs might be needed. This 24-ROM system stores 2048 12-bit values of sin x (or other trig functions), giving angular resolution of 1 part in 2^{11} (0.05%) and output accuracy of 1 part in 2^{12} (0.024%). The system in Figure 2 has the same resolution and is accurate to the limit of its 12 output bits (0.024%), which makes it just as good. But it only requires four 1024-bit ROMs and three 4-bit TTL full adders, so it only costs about one-fifth as much as the more obvious solution of Figure 1.



(a)

(b)

FIGURE 1. Conventional 2048-Increment Sine Table Uses 24 ROMs

Instead of producing x = sin θ, the Figure 2 system divides the angle into two parts and implements the equation

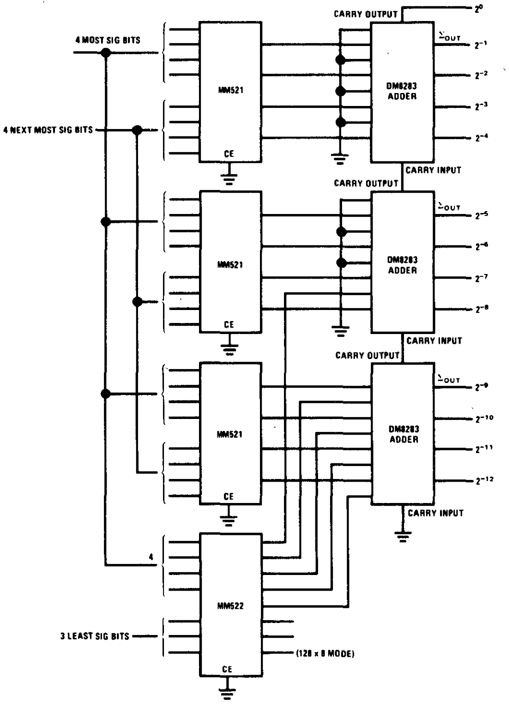
$$x = \sin\theta = \sin(M + L)$$
$$= \sin M \cos L + \cos M \sin L$$

It can be programmed for any angular range. Assume the range is 0 to 90 degrees and let M be the 8 most significant bits of θ and L be the 3 least significant bits of θ (θ being the 11-bit input angular increments, equal to $90^\circ/2048$, or 0.044 deg.) as in Table 2.

With an 8-bit address, the three 256x4 ROMs will give the 12-bit value of sin M at increments of $M = 90^\circ/2^8$, or 0.352 deg. The cos L can only vary between 1 and 0.99998. So we assume cos L=1 and store values of sin M at 0.352 deg. resolution in the top three ROMs, reducing the equation to

$$\sin\theta = \sin M + \cos M \sin L$$

Values of the second term are stored in the fourth ROM. The maximum value of the second term in the above equation can only be cos Msin L = 0.00539 where cos M_{max} = 1, sin L_{max} = 0.00539. This is the maximum value to be added to sin M above. Only the five least significant bits of a 12-bit output are needed to form the maximum output, so an MM522 is used in its 128x8 configuration.



MM522 in 128 × 8 MODE generates $\cos(M_4 - 2.8) \sin L$ 3 MM521 generate $\sin M$
$\sin\theta = \sin M + \cos(M_4 - 2.8) \sin L$

FIGURE 2. Four-ROM Lookup Table Generates 2048 Values of Sin x by Interpolation Technique.

Let the 4 most significant bits of M be called M_4 and the angle at these increments be $X_m = 90^\circ/2^4 = 5.63$ deg. Sin L (the 3 least significant bits of θ) has the same maximum as before and cos M_4 has a maximum of cos 5.63 deg. = 0.99517, and continuing as follows:

$$\cos(11.26) = 0.98076$$
$$\cos(16.89) = 0.95686$$
$$\cos(84.37) = 0.09810$$

through the 16 increments of M_4. Now

$$\sin\theta = \sin M + \cos M_4 \sin L$$

and the appropriate cos M sin L values are stored in the fourth ROM. In effect, we have divided the 0° to 90° sine curve into 16 slope sectors with M_4, each sector into 16 subsections with M, and each subsection into 8 interpolation segments with L.

Since we are using an approximation, accuracy is not quite as good as the Figure 1 system. The additional error term is cos L, assumed 1 but actually is a variable between 1 and 0.99998. At every eighth increment, L is zero, making cos M sin L=0, and sin x=sin M to 12-bit accuracy. Then the error rises to a limit of near 0.002% at every eighth increment where L is 0.352–0.044. This error can be halved by adjusting the fourth ROM's output so that

	M			
ADDRESS	M_4		L	
0			0	
1			1	L = 0.044°
2			1 0	
3			1 1	
4			1 0 0	
5			1 0 1	
6			1 1 0	
7			1 1 1	
8		1	0 0 0	M = 0.352°
9		1	0 0 1	
16		1 0	0 0 0	
32		1 0 0	0 0 0	
64		1 0 0 0	0 0 0	
128	1	0 0 0 0	0 0 0	M_4 = 5.63°
256	1 0	0 0 0 0	0 0 0	
512	1 0 0	0 0 0 0	0 0 0	
1024	1 0 0 0	0 0 0 0	0 0 0	
2048-1	1 1 1 1	1 1 1 1	1 1 1	

TABLE 2. Programming of 2048-Increment Sine Table

$$\sin\theta = \sin M + \cos(M - 2.81^\circ) \sin L$$

If five ROMs are used—four MM521's and all eight outputs of the MM522—15-bit accuracy can be achieved, and thus improving the accuracy by a factor of eight. The resolution could also be smaller, of course, if the angular range were smaller as in an application involving a sensor with a limited field of view. Variations of the system could be used to space the increments irregularly to compensate for sensor nonlinearities, to improve accuracy in specific angular ranges.

This example has a binary fraction output, like the sine function generator in Table 1. For instance, the 8-bit output at the 64th increment representing sin x = sin 45° is 10110101. This equals $1 \times 2^{-1} + 0 \times 2^{-2} + 1 \times 2^{-3} + 1 \times 2^{-4} + 0 \times 2^{-5} + 1 \times 2^{-6} + 0 \times 2^{-7} + 1 \times 2^{-8}$, which reduces to 181/256 or 0.7070. Handbooks give the four-place sine of 45° as 0.7071, so at this increment the output is accurate to approximately 0.01%. This table, the MM422BM/MM522BM, is used in fast Fourier transform, radar, and other signal-processing applications.

Other standard tables that are available off the shelf include an arctan generator, several code generators (EBCDIC to ASCII, BCD to Selectric, and Selectric to BCD) and ASCII-addressed character generators for electronic, electrical and electromechanical display and printout systems. All interface with TTL logic and operate off 12-volt power supplies. Write for data sheets, or use one of our programming tables to jot down any special input-output logic functions you need.

Briefs

SEPTEMBER 1971

MASK PROGRAMMING SPECIALIZES MOS SHIFT REGISTER DESIGNS

A quick, economical way of customizing MOS shift register bit lengths is programming the metallization mask, the mask that defines the thin-film wiring pattern etched on the silicon wafer. Metallization etching is the most convenient process step to specialize because it is consistent from wafer to wafer and is the last major process step before testing.

Utilizing this technique, National Semiconductor has developed two variable-length dynamic MOS register designs. Both of them, MM4007/MM5007 and MM4019/MM5019, are bipolar compatible. Dual registers 20 to 256 bits long, single registers 40 to 512 bits long, and a variety of taps and pinouts provide the system designer with a method of obtaining custom length shift registers quickly and at reasonable cost.

Up to metal masking, wafer design and fabrication are standardized. No time is lost—or money spent—in developing custom arrays or tuning up the process. Automatic test systems further reduce turnaround time and production costs.

Programming the metallization mask mainly involves routing signal connections past selected storage cells to adjust total register length to the desired number of cells. Wire-bonding changes provide output tap options.

DUAL REGISTER DESIGNS

Basically, each of the variable-length types is a dual register (Figure 1 and Table 1A).

There are enough storage cells, I/O stages, clock and power supply lines on each MM4007 chip to make up to two 100-bit registers. The minimum length of each register half, M_A and M_B, is 20 bits. The programmable parts, P_A and P_B, may be 0 to 80 bits long. Lengths need not be equal. For instance, register A may be 29 bits and register B 76 bits ($P_A = 9$, $P_B = 56$).

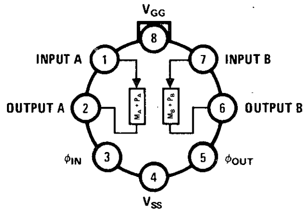


FIGURE 1. Dual Shift Registers

An MM4019/MM5019 chip is similarly organized, except that M_A and M_B are 40 bits and P_A and P_B vary from 0 to 216 bits. Again, lengths may be unequal, such as 240 bits in the A half and 136 bits in the B half.

Clock and supply line pin locations are standardized, but I/O pinouts are selectable. The I/O terminals on the chip may be bonded to package pins which are more convenient for the PC board layout. For example, a couple of board feedthroughs might be eliminated by bonding the A register input to Pin 7 (rather than Pin 1) if data comes in from the right and exits on the left. Or, A and B could share an input pin when they have the same signal source.

TABLE 1 Register Length Options

	MM4007/MM5007			MM4019/MM5019		
	M (BITS)	P (BITS)	TOTAL (BITS)	M (BITS)	P (BITS)	TOTAL (BITS)
A. DUAL REGISTERS						
A Register	20	0 to 80	20 to 100	40	0 to 216	40 to 256
B Register	20	0 to 80	20 to 100	40	0 to 216	40 to 256
	$M_A + M_B$	$P_A + P_B$		$M_A + M_B$	$P_A + P_B$	
B. SINGLE REGISTERS	40	0 to 160	40 to 200	80	0 to 432	80 to 512
C. TAPPED SINGLE REGISTERS Total register length same as single registers with tap locations determined by either half of the dual registers.						

SINGLE-REGISTER OPTIONS

Since clock rates are synchronized by the common clock inputs, the registers may also be serially connected inside the package, as diagrammed in Figure 2. One output is internally connected to the other input.

This extends the maximum length of an MM4007/MM5007 to 200 bits and the MM4019/MM5019 maximum to 512 bits. However, each half still has the same minimum, so the minimums become 40 and 80 bits, respectively (Table 1B). Again, the customer specifies the most convenient I/O pin connections.

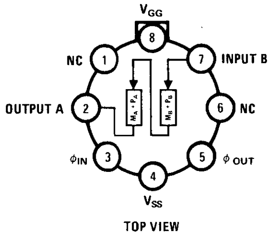


FIGURE 2a

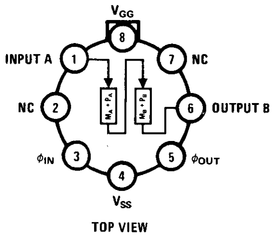


FIGURE 2b

FIGURE 2. Single Registers

Going to the output tap designs of Figure 3 takes only one more wire bond; from the first register output to any available pin. Tap locations are selected by specifying the bit lengths of each of the dual registers. For example, an MM5007 105 bits long may be tapped at any stage from 20 to 85 bits. Generally, this flexibility makes input taps unnecessary—an output at 29 bits in a 105-bit register usually serves the same purpose as an input at 76 bits.

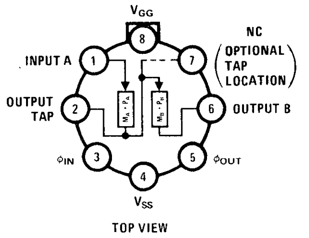


FIGURE 3a

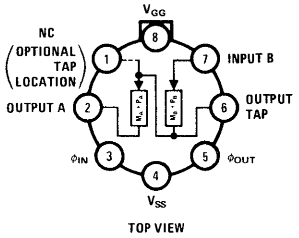


FIGURE 3b

FIGURE 3. Output Tap Options

OPERATING CHARACTERISTICS

All specifications, except bit lengths, are the same as those of other MM4000/MM5000 series dynamic shift registers with the same number of I/O stages.

Clock-line capacitance, power dissipation, as well as other AC and DC parameters, are independent of the lengths programmed. This is accomplished by standardizing clock and supply wiring patterns to achieve minimum turnaround time and cost.

The MM4007/MM5007 and MM4019/MM5019 are fabricated using a low-threshold, p-channel enhancement-mode technology developed for the MM4000/MM5000 series of registers. This means that they are bipolar compatible, sensing TTL or DTL data without input pull-up resistors and driving TTL or DTL loads without output pull-down resistors. They operate on standard +5V and −12V supplies. The clock frequency range is also the same, from 300 Hz to 2.5 MHz, guaranteed.

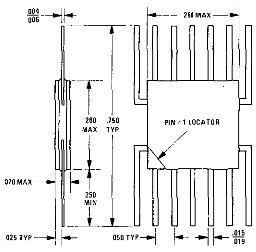
Either TO-99 or dual-in-line packages may be specified. MM4007 and MM4019 operate at −55°C to +125°C. MM5007 and MM5019 are commerical types, specified for −25°C to +70°C.

Ordering Information/ Physical Dimensions

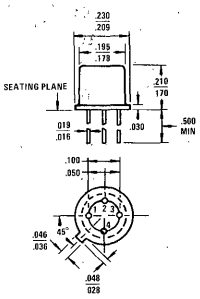
ORDERING INFORMATION

When ordering, indicate the appropriate part number followed by the package designation, e.g., MM5230D.

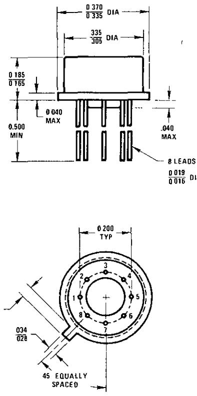
PACKAGE DESIGNATION	PACKAGE TYPE
N	Molded Dual-In-Line Package
D	Cavity Dual-In-Line Package
Q	Quartz Lid Cavity Dual-In-Line Package (MM4203/MM5203 only)
F	Flat Package
H	Metal Can Package
G	12-Lead Metal Can Package (Hybrids Only)



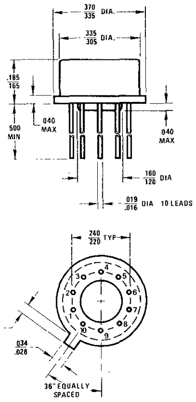
14-Pin Flat Package (F)



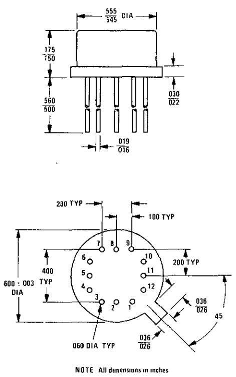
4-Lead Metal Can Package (H)



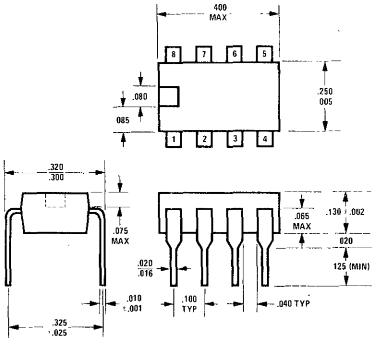
8-Lead Metal Can Package (H)



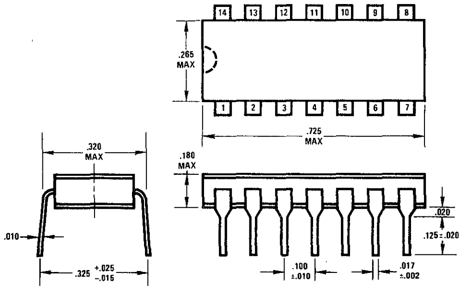
10-Lead Metal Can Package (H)



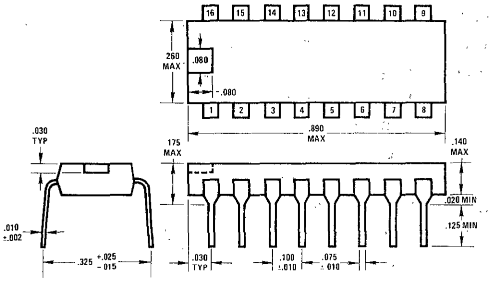
12-Lead Metal Can Package (G)



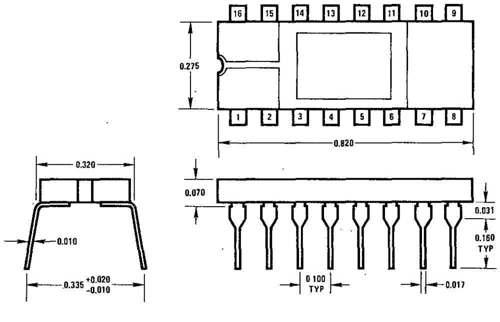
8-Pin Molded Mini-Dual-In-Line Package (N)



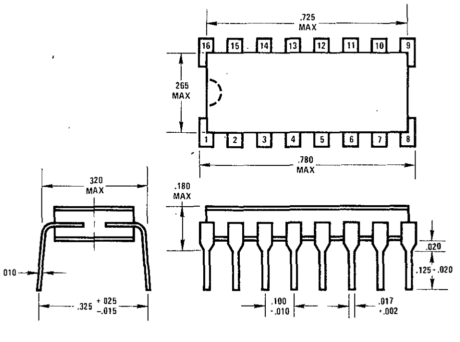
14-Pin Cavity Dual-In-Line Package (D)



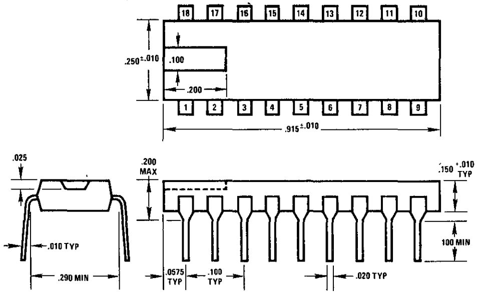
16-Pin Molded Dual-In-Line Package (N)



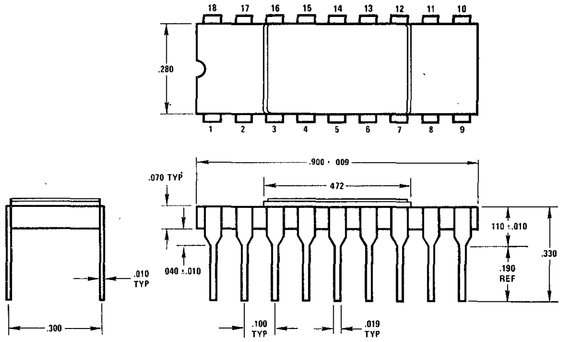
16-Pin Cavity Dual-In-Line Package (D)



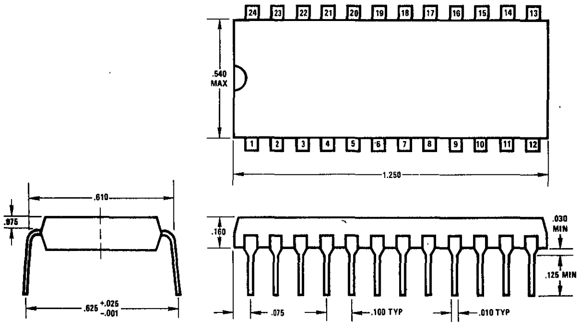
16-Pin Cavity Dual-In-Line Package (D)



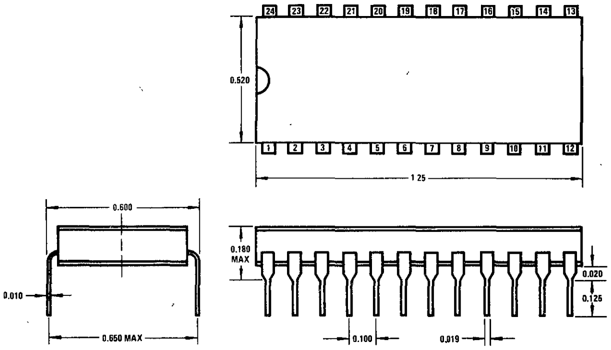
18-Pin Molded Dual-In-Line Package (N)



18-Pin Cavity Dual-In-Line Package (D)



24-Pin Molded Dual-In-Line Package (N)



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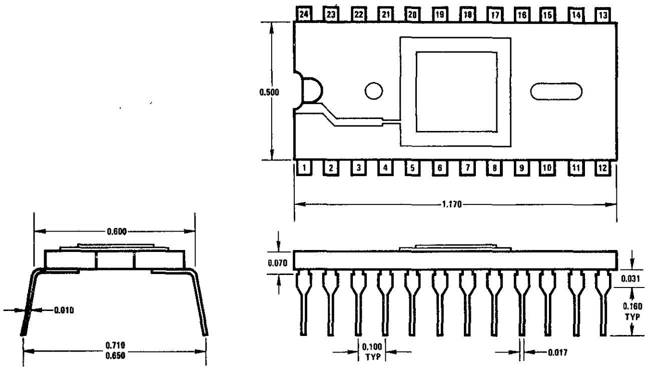
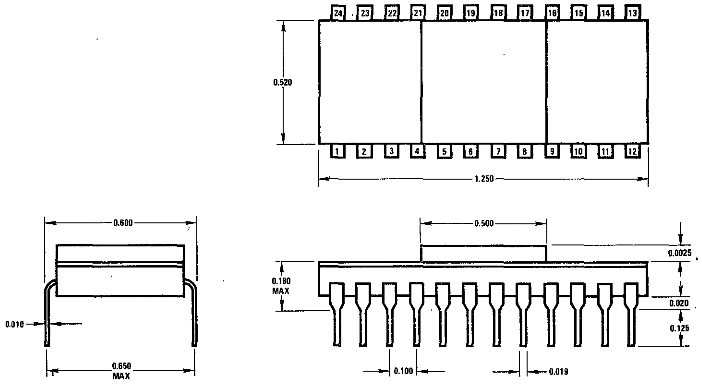


24-Pin Cavity Dual-In-Line Package (D)



24-Pin Quartz Lid Cavity Dual-In-Line Package (Q)

Definition of Terms

Clock Repetition Rate: The range of clock frequencies for which register operation is guaranteed.

Clock Frequency ϕ_f: The range of clock frequencies which register operation is guaranteed. Maximum clock frequencies are dependent upon minimum and maximum clock pulse width restrictions, as presented by the Guaranteed Operating Curves.

Clock Delay ϕ_d: ϕ_d is defined to be that minimum amount of time that must expire after ϕ_1 has undergone a $V_{\phi L}$ to $V_{\phi H}$ transition and the start of a ϕ_2 $V_{\phi H}$ to $V_{\phi L}$ transition. The same spacings apply, when ϕ_2 preceeds ϕ_1.

Clock Phase Delay ϕ_d, $\overline{\phi}_d$: The time between the $V_{\phi H}$ levels of ϕ_{IN} and ϕ_{OUT}. ϕ_d is the time between the trailing edge of ϕ_{IN} and the leading edge of ϕ_{OUT}. $\overline{\phi}_d$ is the time between the trailing edge of ϕ_{OUT} and the leading edge of ϕ_{IN}.

Clock Pulse Risetime, $t_{r\phi}$: The time delay between the 10% and 90% voltage points on the clock pulse as it traverses between its logic $V_{\phi L}$ and logic $V_{\phi H}$ levels.

Clock Pulse Falltime, $t_{f\phi}$: The time delay between the 10% to 90% voltage points on the clock pulse as it traverses between its logic $V_{\phi H}$ and logic $V_{\phi L}$ levels.

Clock Pulse Width, ϕ_{PW}: The duration of time that the clock pulse is greater than 1.5V.

Clock Input Levels: The voltage levels (logic $V_{\phi L}$ or $V_{\phi H}$) which the clock driver must assume to insure proper device operation.

Clock Control Setup Time, t_{cs}: The time prior to the clock Low to High transition at which the clock control must be at its desired logic level.

Clock Control Hold Time, t_{ch}: The time after the High to Low transition for which the clock control must be held at its desired logic level.

Data Setup Time, t_{ds}: The time prior to the clock High to Low transition at which the data input level must be present to guarantee being clocked into the register by that clock pulse.

Data Pulse Width, t_{dw}: The time during which the data pulse is in its V_{IH} or V_{IL} state.

Data Hold Time, t_{dh}: The time after the clock High to Low transition which the data input level must be held to guarantee being clocked into the register by that clock pulse.

Data Input Voltage Levels: The voltage levels (logic V_{IL} or V_{IH}) which the data input terminal must assume to insure proper logic inputs.

Data Output Voltage Levels: The output voltage levels (logic V_{OL} or V_{OH}) which the output will assume under normal operating conditions.

Data Input Capacitance: The capacitance between the data input terminal and ground reference measured at 1 MHz.

Output Resistance to Ground: The resistance between the output terminal and ground with the output in the logic V_{OH} state.

Partial Bit Times T_{IN}, T_{OUT}: The time between leading edges of clocks, measured at the $V_{\phi H}$ levels. T_{IN} is the time between the leading edge of ϕ_{IN} and the leading edge of ϕ_{OUT}. T_{OUT} is the time between the leading edge of ϕ_{OUT} and the leading edge of ϕ_{IN}.

Output Sink Current: The current which flows into the output terminal of the register when the output is a logical low level. Conventional current flow is assumed.

Output Source Current: The current which flows out of the output terminal of the register when the output is a logical High level. Conventional current flow is assumed.

Input Voltage Levels: The logical Low level, V_{IL} or $V_{\phi L}$ is the more negative level. This level is generally referred to as a TTL or DTL logical "0" and an MOS logical "1". The logical High level, V_{IH} or $V_{\phi H}$ is the more positive level. This level is generally referred to as a TTL or DTL logical "1" and an MOS logical "0".

Output Voltage Levels: The logical Low level, V_{OL}, is the more negative level. This is the state in which the output is capable of sinking current. The logical High level, V_{OH}, is the more positive level. This is the state in which the output is capable of sourcing current.

V_{GG} Current Drain: The average current flow out of the V_{GG} terminal of the package with the output open circuited.

Power Supply Voltage, V_{GG}: The negative power supply potential required for proper device operation; referenced to V_{SS}.

Power Supply Return, V_{SS}: The V_{SS} terminal is the reference point for the device. It must always be the most positive potential applied to the device.

V_{SS} Current Drain: The average current flow into the V_{SS} terminal of the package. It is equal to the sum of the I_{GG} and I_{DD} currents.

Power Supply Voltage, V_{DD}: The negative power supply potential required for proper device operation, referenced to V_{SS}.

Clock Input Voltage Levels, $V_{\phi H} V_{\phi L}$: The voltage levels (logic "1" or "0") which the clock driver must assume to insure proper device operation.

Data Output Voltage Levels, V_{OH}, V_{OL}: The output voltage levels (logic "1" or "0") which the output will assume with a specified load connected between output and V_{SS} line.

Data Input Voltage Levels, $V_{IH} V_{IL}$: The voltage levels (logic "1" or "0") which the data input terminal must assume to insure proper logic inputs.

Control Release Time, t_{cr}: The maximum time that a load command signal can be changed prior to the $V_{\phi L}$ to $V_{\phi H}$ transition of the output clock, ϕ_{OUT}, without affecting the data during bit time t_n.

Control Initiate Window: The time in which a load command signal must be applied to affect bit time t_n. This time extends from the start of t_{cr} to the start of t_{cs}.

Control Hold Time: The time that the load command signal must remain stable during t_n bit time. See control timing diagram.

Logical "0": The logical zero voltage is the voltage state occurring near ground. At the output of the device the logical zero voltage is guaranteed to be not more than −1.0 volt under worst case conditions of power supply and ambient temperature. The input requirements are guaranteed so that any voltage up to −1.5 volts will be interpreted as a logical zero. This implies a 0.5 volt noise immunity for the logical zero state.

Logical "1": The logical one voltage is the more negative voltage state occurring near the negative supply (V_{DD}) value. At the output of the device the logical one voltage is guaranteed to be not less than −8.0 volts under worst case conditions of power supply and ambient temperature. The input requirements are guaranteed so that any voltage more negative than −7.0 volts will be interpreted as a logical one. This implies a 1.0 volt noise immunity for the logical one state.

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