INTERFACE
INTEGRATED CIRCUITS

National

INTERFACE INTEGRATED CIRCUITS OCT 1975 National

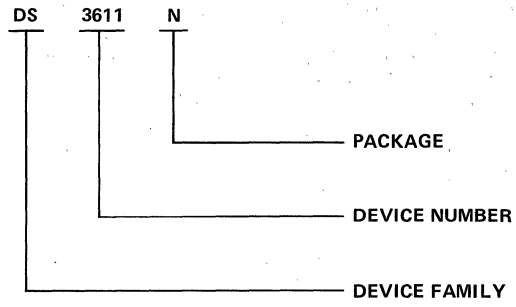
Edge Index by Product Family

Here is the new INTERFACE catalog from National Semiconductor Corporation. It contains complete information on all of National's INTERFACE products and we hope it becomes your most important INTERFACE guide. For your convenience, two different Tables of Contents are provided. One lists the products by type—Line Driver, Sense Amplifier, etc.—and the other lists the products alphanumerically by part number. Product selection guides and a complete product applications section are also included. For information on products that become available after this catalog goes to print, contact your local National office. The addresses are listed on the back cover.

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248.

Ordering Information

Ordering information for National devices covered in this catalog is as follows:



DEVICE FAMILY

DM – Digital Monolithic
DS – Digital Special
NCT – Opto Couplers

DEVICE NUMBER

3, 4 or 5 digit number

Suffix Indicators:
A – Improved Electrical Specification

PACKAGE

D – Glass/Metal Dual-In-Line Package
F – Flat Package (0.25" wide)
G – TO-8 (12 lead) Metal Can
H – TO-5 (multi-lead) Metal Can
J – Glass/Glass Dual-In-Line Package
N – Molded Dual-In-Line Package
W – Flat Package (0.275" wide)

National's interface products use a 16/36 prefix. The 16 is used to denote the military temperature range (–55°C to +125°C) and the 36 denotes the commercial temperature range (0°C to +70°C), i.e. DS1630/DS3630. Display drivers and line drivers and receivers employ a 76/86 or a 78/88 prefix. The 76 or 78 applies to the military part, and the 86 or 88 to the commercial part, i.e. DS7830/DS8830. Some interface circuits and sense amplifiers employ a 55 as the first two digits for the military temperature range part, and a 75 for the commercial part, i.e. DS5520/DS7520. Digital products employ a 54 as the first two digits for the military temperature range part, and a 74 for the commercial part, i.e. DM5446/DM7446.

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Thermal Ratings For IC's

MAXIMUM POWER DISSIPATION

To insure reliable long term operation of its Interface Integrated Circuits, National Semiconductor has specified maximum junction temperature (T_J) limits. These limits are at 150°C for circuits packaged in a molded dual-in-line package (Epoxy B), and 175°C for all other package types.

Maximum power dissipation (P_D) of an integrated circuit is limited by maximum allowable junction temperature of the silicone die, and thermal resistance (θ_{J-X}) of the package. *Figure 1* illustrates the relationship between power dissipation and junction temperature.

The line indicating "Maximum Power Rating of Package" is projected from the maximum junction temperature limit (150°C in this example) at a slope corresponding to the package thermal resistance ($1/\theta_{J-X}$). Below this line is the safe operating area of the device. Additional constraints are Maximum Power Dissipation and Maximum Operating Temperature (T_A). These parameters may be determined from device data sheets. For this example, $P_{D(MAX)}$ = 300 mW and $T_{A(MAX)}$ = 70°C.

Point "A" in *Figure 1* is an operating point corresponding to T_A = 50°C and P_D = 100 mW. Determine device junction temperature by projecting a line from point "A," parallel to the Maximum Power Rating curve, until it intersects the horizontal axis. T_J is determined from the point of intersection with the horizontal axis. For this example, T_j is 45°C.

THERMAL INFORMATION

Figure 2 illustrates thermal resistance characteristics for Interface Integrated Circuit packages.

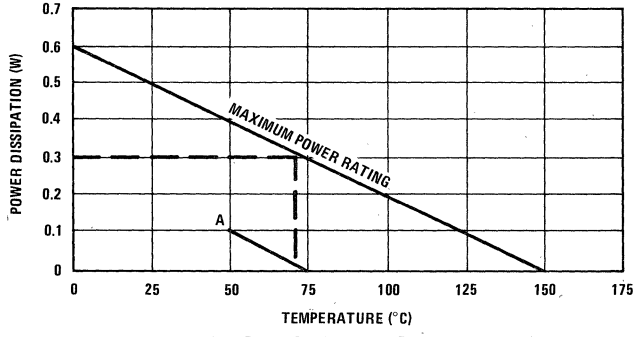
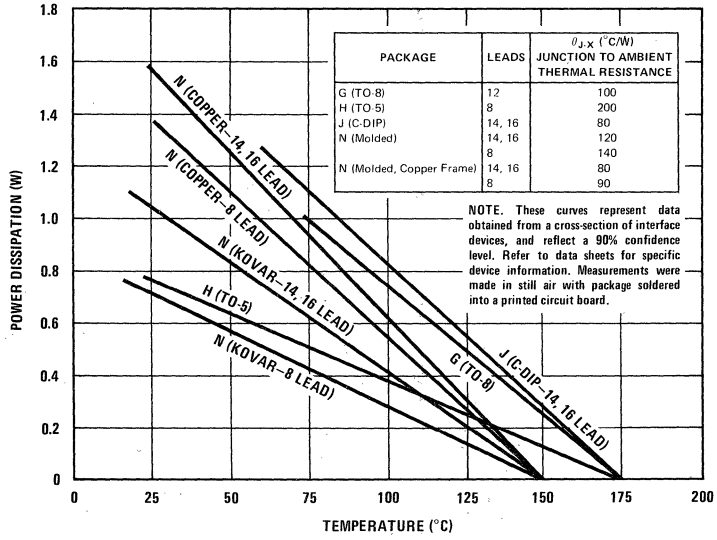


FIGURE 1. Power Dissipation vs Temperature



PACKAGE	LEADS	θ_{J-X} (°C/W) JUNCTION TO AMBIENT THERMAL RESISTANCE
G (TO-8)	12	100
H (TO-5)	8	200
J (C-DIP)	14, 16	80
N (Molded)	14, 16	120
	8	140
N (Molded, Copper Frame)	14, 16	80
	8	90

NOTE. These curves represent data obtained from a cross-section of interface devices, and reflect a 90% confidence level. Refer to data sheets for specific device information. Measurements were made in still air with package soldered into a printed circuit board.

FIGURE 2. Maximum θ_{J-X} Values for IC Packages

NATIONAL

Interface Cross Reference Guide

DEVICE NUMBER	NATIONAL EXACT REPLACEMENT
Fairchild	
9374	DS8674
Motorola	
MC1488	DS1488
MC1489	DS1489
MC1489A	DS1489A
MC3437	DS8837
MC3438	DS8838
MC3441	DS3651
MC3443	DS3653
MC3450	DS3650
MC3452	DS3652
MC3460	DS3674
MC3483	DS8833
MC3484	DS8834
MC3485	DS8835
MC3489	DS8839
Signetics	
SP380	DS8640
8T13	DS75121
8T14	DS75122
8T23	DS75123
8T24	DS75124
8T25	DS3625
8T26	DS8826
8T34	DS8834
8T37	DS8837
8T38	DS8838
8T51	DS8856
8T59	DS8857
8T74	DS8672
8T380	DS8836
Texas Instruments	
SN5520	DS5520
SN5521	DS5521
SN5522	DS5522
SN5523	DS5523
SN5524	DS5524
SN5525	DS5525
SN5528	DS5528
SN5529	DS5529
SN5534	DS5534
SN5535	DS5535
SN5538	DS5538
SN5539	DS5539
SN7520	DS7520
SN7521	DS7521
SN7522	DS7522
SN7523	DS7523
SN7524	DS7524
SN7525	DS7525
SN7528	DS7528
SN7529	DS7529
SN7534	DS7534
SN7535	DS7535
SN7538	DS7538
SN7539	DS7539
SN55107	DS55107
SN55108	DS55108
SN55109	DS55109

DEVICE NUMBER	NATIONAL EXACT REPLACEMENT
Texas Instruments (con't)	
SN55110	DS55110
SN55121	DS55121
SN55122	DS55122
SN55150	DS55150
SN55154	DS55154
SN55180	DS7800
SN55182	DS7820A
SN55183	DS7830A
SN55207	DS55207
SN55208	DS55208
SN55325	DS55325
SN55361	DS55361
SN55365	DS55365
SN55369	DS0026
SN55450	DS55450
SN55451	DS55451
SN55452	DS55452
SN55453	DS55453
SN55454	DS55454
SN55460	DS55460
SN55461	DS55461
SN55462	DS55462
SN55463	DS55463
SN55464	DS55464
SN55480	DS7880
SN55493	DS55493
SN55494	DS55494
SN75107	DS75107
SN75108	DS75108
SN75109	DS75109
SN75110	DS75110
SN75121	DS75121
SN75122	DS75122
SN75123	DS75123
SN75124	DS75124
SN75150	DS75150
SN75154	DS75154
SN75180	DS8800
SN75182	DS8820A
SN75183	DS8830
SN75188	DS1488
SN75189	DS1489
SN75189A	DS1489A
SN75207	DS75207
SN75208	DS75208
SN75324	DS75324
SN75325	DS75325
SN75361	DS75361
SN75362	DS75362
SN75365	DS75365
SN75369	DS0026C
SN75450	DS75450
SN75451	DS75451
SN75452	DS75452
SN75453	DS75453
SN75454	DS75454
SN75460	DS75460
SN75461	DS75461
SN75462	DS75462
SN75463	DS75463
SN75464	DS75464
SN75480	DS8880
SN75491	DS75491
SN75492	DS75492
SN75493	DS75493
SN75494	DS75494

NATIONAL

Transmission Line Driver and Receiver Product Guide

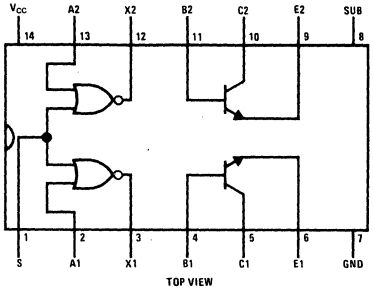
DEVICE	DRIVER OR RECEIVER	COMMON MODE OR DIFFERENTIAL	INPUT THRESHOLD	OUTPUT LEVELS	POWER SUPPLY	DESCRIPTION AND COMMENTS
DS7820/DS8820	Receiver	Differential	200 mV	TTL	+5.0	Dual ±15V Common Mode Range
DS78LS20	Receiver	Differential	±200 mV	TTL	+5.0	DS7820 EIA Standards RS422 and RS423
DS1689/DS3689	Receiver	Differential	±200 mV	TTL	+5.0	Quad EIA Standards RS422 and RS423
DS1688/DS3688	Driver	Differential	TTL	TTL	+5.0	Quad EIA Standard RS422
DS7820A/DS8820A	Receiver	Differential	200 mV	TTL	+5.0	High Performance DS7820
DS7822/DS8822	Receiver	Differential/ Common Mode	−2.0 to +20	TTL	+5.0	Dual EIA Standard RS232
DS7830/DS8830	Driver	Differential	TTL	TTL	+5.0	Dual
DS7831/DS8831	Driver	Differential/ Common Mode	TTL	TTL	+5.0	TRI-STATE® DS7830
DS7832/DS8832	Driver	Differential/ Common Mode	TTL	TTL	+5.0	DS7831 Without V_{CC} Clamp Diodes
DS55107/DS75107	Receiver	Differential	25 mV	TTL	±5.0	10 mV Threshold DS55107 Dual
DS55207/DS75207	Receiver	Differential	10 mV	TTL	±5.0	10 mV Threshold DS55107
DS55108/DS75108	Receiver	Differential	25 mV	TTL	±5.0	Open Collector DS55107
DS55208/DS75208	Receiver	Differential	10 mV	TTL	±5.0	10 mV Threshold DS55108
DS3650	Receiver	Differential	±25 mV	TTL	±5.0	Quad DS75107
DS3651	Receiver	Differential	±7 mV	TTL	±5.0	Quad DS75107
DS3652	Receiver	Differential	±25 mV	TTL	±5.0	Quad DS75108
DS3653	Receiver	Differential	±7 mV	TTL	±5.0	Quad DS75108
DS1603/DS3603	Receiver	Differential	25 mV	TTL	±5.0	TRI-STATE® DS55107
DS3604	Receiver	Differential	10 mV	TTL	±5.0	10 mV Threshold DS1603
DS55109/DS75109	Driver	Differential	TTL	6.0 mA	±5.0	Dual
DS55110/DS75110	Driver	Differential	TTL	12 mA	±5.0	12 mA DS55109
DS55121/DS75121	Driver	Common Mode	TTL	TTL	+5.0	Dual 50Ω or Coax Driver
DS55122/DS75122	Receiver	Common Mode	0.8 to 2.0	TTL	+5.0	Triple with Hysteresis
DS55123/DS75123	Driver	Common Mode	TTL	TTL	+5.0	DS55121 for IBM Interface
DS55124/DS75124	Receiver	Common Mode	0.7 to 1.7	TTL	+5.0	DS55123 for IBM Interface
DS7834/DS8834	Transceiver	Common Mode	TTL	TTL	+5.0	Quad TRI-STATE® Hysteresis
DS7835/DS8835	Transceiver	Common Mode	TTL	TTL	+5.0	DS7834 with Strobed Receiver
DS7839/DS8839	Transceiver	Common Mode	TTL	TTL	+5.0	Non-Inverting DS7834
DS7833/DS8833	Transceiver	Common Mode	TTL	TTL	+5.0	DS7839 with Strobed Receiver
DS7836	Receiver	Common Mode	TTL	TTL	+5.0	Quad NOR with Hysteresis
DS7640/DS8640	Receiver	Common Mode	TTL	TTL	+5.0	DS7836 with No Hysteresis
DS7641/DS8641	Transceiver	Common Mode	TTL	TTL	+5.0	DS7838 with No Hysteresis
DS8642	Transceiver	Common Mode	TTL	TTL	+5.0	Quad Open Collector with 100 mA Sink
DS7837/DS8837	Receiver	Common Mode	TTL	TTL	+5.0	Hex with Hysteresis
DS7838/DS8838	Receiver	Common Mode	TTL	TTL	+5.0	Quad Open Collector with Hysteresis
DS1488	Driver	Common Mode	TTL	±7.0V	±9.0 to 15	Quad EIA Standard RS232
DS1489	Receiver	Common Mode	0.75 to 1.5	TTL	+5.0	Quad EIA Standard RS232 with Hysteresis
DS1489A	Receiver	Common Mode	0.75 to 2.25	TTL	+5.0	Higher Noise Immunity DS1489
DS75150	Driver	Common Mode	TTL	±8V	±12	Dual EIA Standard RS232
DS75154	Receiver	Common Mode	0.8 to 3	TTL	+5.0	Quad EIA Standard RS232 with Hysteresis

Peripheral Driver Guide

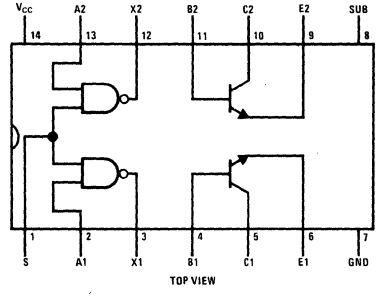
GENERAL DESCRIPTION

Series or Device Number	Nominal V_{CC} (Volts)	Output Breakdown Voltage (Volts)	Maximum Output Leakage Current (μA)	Maximum Output On Current (mA)	V_{OL} (Max) At Maximum Output Current (Volts)	Typical Propagation Delay (ns)
DS75450 Series (DS75450, DS350, DS75451, DS75452, DS75453, DS75454)	5.0	30	100	300	0.7	15
DS3611 Series (DS3611, DS3612, DS3613, DS3614)	5.0	80	100	300	0.7	130
DS75460 Series	5.0	35	100	300	0.7	40

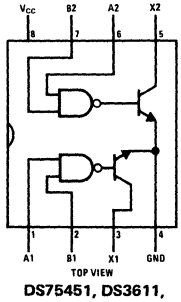
CONNECTION DIAGRAMS



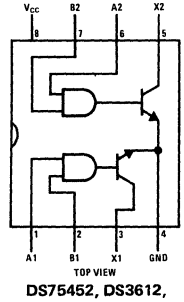
DS350



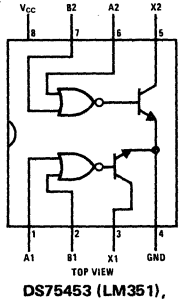
DS75450
DS75460



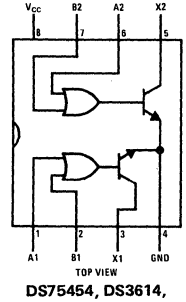
DS75451, DS3611, DS75461



DS75452, DS3612, DS75462



DS75453 (LM351), DS3613, DS75463



DS75454, DS3614, DS75464

NATIONAL

LED Driver Guide

NSC #	DESCRIPTION	STATUS	I_{OUT} (Note 1) TYP mA	V_{OUT} MAX V	# PINS	DEC.	INV.	INPUTS	COMMENTS
DIGIT DRIVERS									
DS8646	6 Digit LED Dr	F	84	5	Dice		•	MOS	For CMOS Watch Ckts
DS8650	4 Digit LED Watch Dr	P	50	5	Dice		•	MOS	For CMOS Watch Ckts
DS8658	4 Digit LED Watch Dr	P	84	5	Dice		•	MOS	For CMOS Watch Ckts
DS8664	14 Digit LED Dr	F	80	10	24	•		MOS	On Chip Clock, 9V LBI
DS8665	14 Digit LED Dr	F	−15	10	24	•		MOS	On Chip Clock
DS8666	14 Digit LED Dr	F	*	10	24	•		MOS	*POS Circuit, On Chip Clock
DS8844	17 Digit LED Dr	P	50	10	16		•	MOS	
DS8855	9 Digit LED Dr	P	50	10	22		•	MOS	
DS8863	8 Digit LED Dr	P	500	10	18		•	MOS	
DS8864	9 Digit LED Dr	P	50	10	22		•	MOS	9V LBI
DS8865	8 Digit LED Dr	P	50	10	18		•	MOS	
DS8866	7 Digit LED Dr	P	50	10	18		•	MOS	9V LBI
DS8868	12 Digit LED Dr	P	110	5	18	•		MOS	4.5V LBI
DS8870	6 Digit LED Dr	P	350	10	14			MOS	DS75492 Pin-Out
DS8871	8 Digit LED Dr	P	40	10	18		•	MOS	
DS8872	9 Digit LED Dr	P	40	10	22		•	MOS	
DS8873	9 Digit LED Dr	P	40	10	22		•	MOS	9V LBI
DS8874	9 Digit LED Dr	F	50	10	14	•		MOS	Serial Input, 9V LBI
DS8876	9 Digit LED Dr	F	50	10	14	•		MOS	Serial Input, 6V LBI
DS8877	6 Digit LED Dr	P	40	10	14		•	MOS	DS75492 Pin-Out
DS8879	9 Digit LED Dr	F	50	10	14	•		MOS	Serial Input, 4.5V LBI
DS8892	6 Digit LED Dr	P	250 Max	10	16		•	MOS	Programmable
DS8920	9 Digit LED Dr	F	40	10	20		•	MOS	
DS8962	6 Digit LED Dr	P	250	10	18				DS75492 Pin-Out
DS8963	8 Digit LED Dr	P	500	10	18				
DS8972	7 Digit LED Dr	F	100	10	18		•	MOS	9V LBI
DS8973	9 Digit LED Dr	F	100	10	22		•	MOS	4.5V LBI
DS8974	9 Digit LED Dr	F	100	10	22		•	MOS	6V LBI
DS8975	9 Digit LED Dr	F	100	10	22		•	MOS	
DS8976	9 Digit LED Dr	F	100	10	22		•	MOS	9V LBI
DS8977	7 Digit LED Dr	P	40	10	18		•	MOS	9V LBI
DS75492	6 Digit LED Dr	P	250	10	14		•	MOS	
DS75494	6 Digit LED Dr	P	180	10	16		•	MOS	
SEGMENT DRIVERS									
DM7446A	BCD to 7 Seg. Decoder/Driver	P	40	30	16		•	TTL	
DM7447A	BCD to 7 Seg. Decoder/Driver	P	40	15	16		•	TTL	
DM7448	BCD to 7 Seg. Decoder/Driver	P	−2	N/A	16		•	TTL	Requires External Transistor
DS8647	9 Seg. LED Watch Dr	F	−10	−4	Dice		•	MOS	For CMOS Watch Ckts
DS8648	9 Seg. LED Watch Dr	F	−10	−4	Dice			MOS	For CMOS Watch Ckts
DS8649	8 Seg. LED Watch Dr	F	−10	−4	Dice			MOS	For CMOS Watch Ckts
DS8651	7 Seg. LED Watch Dr	P	−6.5	−4	Dice		•	MOS	For CMOS Watch Ckts
DS8659	7 Seg. LED Watch Dr	P	−10	−4	Dice		•	MOS	For CMOS Watch Ckts
DS8672	BCD to 7 Seg. LED Decoder/Latch/Dr	F	20	5	16	•		TTL	Decodes 0-9, A, E, H, L, P
DS8673	BCD to 7 Seg. LED Decoder/Latch/Dr	F	15	5.5	16	•		TTL	Alpha-Numeric Output
DS8674	BCD to 7 Seg. LED Decoder/Latch/Dr	F	15	5.5	16	•		TTL	Decodes 0-9, −, E, H, L, P
DS8675	BCD to 7 Seg. LED Decoder/Latch/Dr	F	40 Max	5.5	16	•		TTL	Alpha-Numeric Output, I_{OUT} Externally Set
DS8676	BCD to 7 Seg. LED Decoder/Latch/Dr	F	25 Max	5.5	16	•		TTL	Alpha-Numeric Output, I_{OUT} Programmable
DS8856	BCD to 7 Seg. LED Dr	P	−6	5.5	16	•		TTL	Requires External Transistor
DS8857	BCD to 7 Seg. LED Dr	P	−50	5.5	16	•		TTL	I_{OUT} Internally Set
DS8858	BCD to 7 Seg. LED Dr	P	−50	5.5	16	•		TTL	I_{OUT} Externally Set
DS8861	5 Seg. LED Dr	P	±50	10	18		*	MOS	*Inverting with Emitter Grounded
DS8867	8 Seg. LED Dr	P	−14	8	18			MOS	Preset I_{OUT}
DS8895	4 Seg. LED Dr	P	−14	10	16			MOS	I_{OUT} Internally Set
DS8910	1 Decade Counter/Latch 7 Seg. Decoder/Driver	F	15	5.5	16	•		TTL	
DS8960	4 Seg. LED Dr	F	±50	18	14		*	MOS	*Inverting with Emitter Grounded
DS8961	5 Seg. LED Dr	F	±50	18	18		*	MOS	*Inverting with Emitter Grounded
DS75491	4 Seg. LED Dr	P	±50	10	14		*	MOS	*Inverting with Emitter Grounded
DS75493	4 Seg. LED Dr	P	−30	10	16			MOS	I_{OUT} Set by External Res.

Note 1: Positive current is going into device.

Opto-Coupler Cross Reference Guide

DEVICE TYPE	NATIONAL NUMBER	COMMENTS
Fairchild		
FCD810	NCT200	Direct Replacement
FCD811	4N25	Direct Replacement
FCD820	NCT200	Direct Replacement
Monsanto		
MCT2	NCT200	Direct Replacement
MCT2E	4N25	Direct Replacement
MCT26	NCT260	Direct Replacement
Litronics		
IL1	4N25	Direct Replacement
IL5	4N25	Selection Required For 50% C.T.R.
IL12	NCT260	Direct Replacement
IL15	NCT260	Direct Replacement
IL16	NCT260	Selection Required For Maximum 14% C.T.R.
IL74	NCT200	Direct Replacement
IL100	DS3661	Direct Replacement
Texas Instrument		
TIL-111	NCT200	Direct Replacement
TIL-112	NCT260	Direct Replacement
TIL-114	4N25	Direct Replacement
TIL-117	4N25	Selection Required For 50% C.T.R.
TIL-118	NCT260	Direct Replacement
General Electric		
H11A1	4N25	Selection Required For 50% C.T.R.
H11A2	NCT200	Direct Replacement
H11A3	4N25	Direct Replacement
H11A4	NCT200	Direct Replacement
H11A5	NCT260	Direct Replacement
Clairex		
CL1-2	NCT200	Selection Required For Minimum 30% And Maximum 100% C.T.R.
CL1-3	NCT200	Selection Required For Minimum 100% And Maximum 200% C.T.R.
CL1-5	NCT200	Direct Replacement
CL1-20	NCT200	Selection Required For Maximum 100% C.T.R.
Optron		
OP1022	NCT260	Direct Replacement
OP1032	NCT200	Selection Required For Minimum 100% C.T.R.
OP1062	NCT200	Selection Required For Minimum 25% C.T.R.
OP1064	NCT200	Selection Required For Minimum 25% C.T.R.
JEDEC Registered Opto-Couplers		
4N25	4N25	Direct Replacement
4N26	4N26	Direct Replacement
4N27	4N27	Direct Replacement
4N28	4N28	Direct Replacement
4N35	NCT200	Selection Required For 3.5 kV Isolation And Minimum 100% C.T.R.
4N36	NCT200	Selection Required For 2.5 kV Isolation And Minimum 100% C.T.R.
4N37	NCT200	Selection Required For Minimum 100% C.T.R.
Motorola		
MOC1001	4N25	Direct Replacement
MOC1000	4N26	Direct Replacement
MOC1002	4N27	Direct Replacement
MOC1003	4N28	Direct Replacement
Hewlett Packard		
HP 4360	DS3660	Direct Replacement

NATIONAL

DS1611/DS3611, DS1612/DS3612, DS1613/DS3613, DS1614/DS3614 dual peripheral drivers

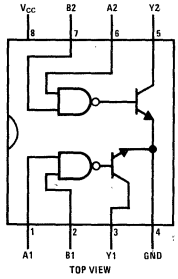
general description

The DS1611 series of dual peripheral drivers was designed for those applications where a higher breakdown voltage is required than that provided by the DS75451 series. The pin outs for the circuits are identical to those of the DS75451 through DS75454. The DS1611 series parts feature high voltage outputs (80V breakdown in the "OFF" state) as well as high current (300 mA in the "ON" state). Typical applications include power drivers, relay drivers, lamp drivers, MOS drivers, and memory drivers.

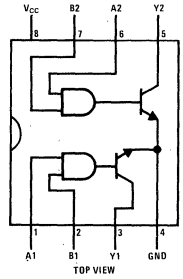
features

- 300 mA output current capability per driver
- High voltage outputs (80V)
- TTL or DTL compatible
- Input clamping diodes
- Choice of logic function

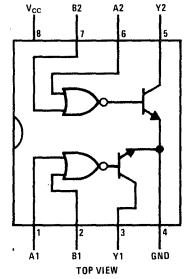
connection diagrams (Dual-In-Line and Metal Can Packages)



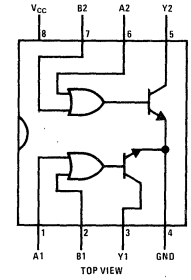
Order Number DS3611N



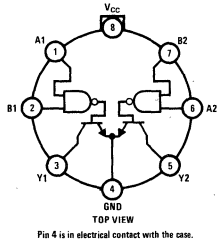
Order Number DS3612N



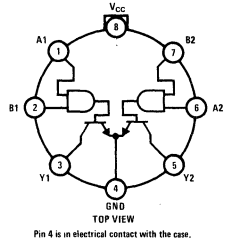
Order Number DS3613N



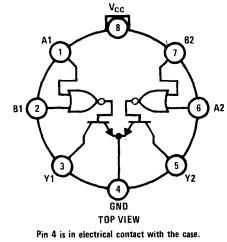
Order Number DS3614N



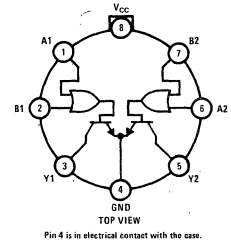
Order Number DS1611H or DS3611H



Order Number DS1612H or DS3612H



Order Number DS1613H or DS3613H



Order Number DS1614H or DS3614H

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage (Note 5)	80V
Continuous Output Current	300 mA
Continuous Total Power Dissipation (Note 4)	800 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS161X	4.5	5.5	V
DS361X	4.75	5.25	V
Temperature (T_A)			
DS161X	−55	+125	°C
DS361X	0	+70	°C

electrical characteristics

DS1611/DS3611, DS1612/DS3612, DS1613/DS3613, DS1614/DS3614 (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	*(Figure 1)*			2			V
V_{IL}	Low Level Input Voltage	*(Figure 2)*					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA, *(Figure 3)*				−1.2	−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, *(Figure 1)*	DS1611, V_{IL} = 0.8V	I_{OL} = 100 mA		0.2	0.5	V
				I_{OL} = 300 mA		0.45	0.8	V
			DS1612, V_{IH} = 2V	I_{OL} = 100 mA		0.2	0.5	V
				I_{OL} = 300 mA		0.45	0.8	V
			DS1613, V_{IL} = 0.8V	I_{OL} = 100 mA		0.2	0.5	V
				I_{OL} = 300 mA		0.45	0.8	V
			DS1614, V_{IH} = 2V	I_{OL} = 100 mA		0.2	0.5	V
				I_{OL} = 300 mA		0.45	0.8	V
			DS3611, V_{IL} = 0.8V	I_{OL} = 100 mA		0.2	0.4	V
				I_{OL} = 300 mA		0.45	0.7	V
			DS3612, V_{IH} = 2V	I_{OL} = 100 mA		0.2	0.4	V
				I_{OL} = 300 mA		0.45	0.7	V
			DS3613, V_{IL} = 0.8V	I_{OL} = 100 mA		0.2	0.4	V
				I_{OL} = 300 mA		0.45	0.7	V
			DS3614, V_{IH} = 2V	I_{OL} = 100 mA		0.2	0.4	V
				I_{OL} = 300 mA		0.45	0.7	V
V_{OH}	Output Breakdown Voltage	V_{CC} = Min, *(Figure 1)*	V_{IH} = 2V, I_{OH} = 300 μA	DS1611, DS1613	80			V
			V_{IH} = 2V, I_{OH} = 100 μA	DS3611, DS3613	80			V
			V_{IL} = 0.8V, I_{OH} = 300 μA	DS1612, DS1614	80			V
			V_{IL} = 0.8V, I_{OH} = 100 μA	DS3612, DS3614	80			V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 2)*					1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 2)*					40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 3)*				−1	−1.6	mA
I_{CCH}	Supply Current	V_{CC} = Max, Outputs High, *(Figures 4 and 5)*	V_I = 5V	DS1611/ DS3611			11	mA
				DS1613/ DS3613			14	mA
			V_I = 0V	DS1612/ DS3612			14	mA
				DS1614/ DS3614			17	mA
I_{CCL}	Supply Current	V_{CC} = Max, Outputs Low, *(Figures 4 and 5)*	V_I = 0V	DS1611/ DS3611			69	mA
				DS1613/ DS3613			73	mA
			V_I = 5V	DS1612/ DS3612			71	mA
				DS1614/ DS3614			79	mA

switching characteristics V_{CC} = 5.0V, T_A = 25°C

DS1611/DS3611, DS1612/DS3612, DS1613/DS3613, DS1614/DS3614

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PD1}	Propagation Delay Time, Low-To-High Level Output	$I_O \approx 200$ mA, C_L = 15 pF, $R_L = 50\Omega$, *(Figure 6)*	DS1611/ DS3611		130		ns
			DS1612/ DS3612		110		ns
			DS1613/ DS3613		125		ns
			DS1614/ DS3614		220		ns
t_{PD0}	Propagation Delay Time, High-To-Low Level Output	$I_O \approx 200$ mA, C_L = 15 pF, $R_L = 50\Omega$, *(Figure 6)*	DS1611/ DS3611		125		ns
			DS1612/ DS3612		110		ns
			DS1613/ DS3613		125		ns
			DS1614/ DS3614		150		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS3611, DS3612, DS3613, DS3614, and −55°C to +125°C temperature range for the DS1611, DS1612, DS1613 and DS1614. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

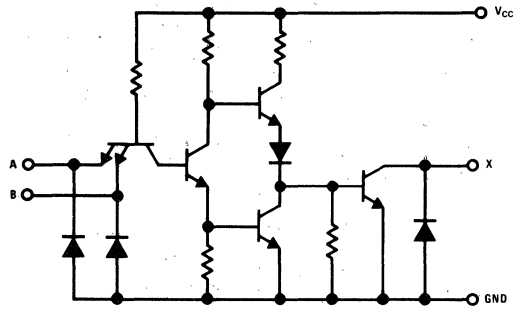
Note 4: Maximum junction temperature is 150°C. For operating at elevated temperatures, the package must be derated based on a thermal resistance, θ_{JA}, of 110°C/W.

Note 5: Maximum voltage to be applied to either output in the "OFF" state.

Note 6: Delay is measured with a 50Ω load to 10V, 15 pF load capacitance, measured from 1.5V input to 50% point on output.

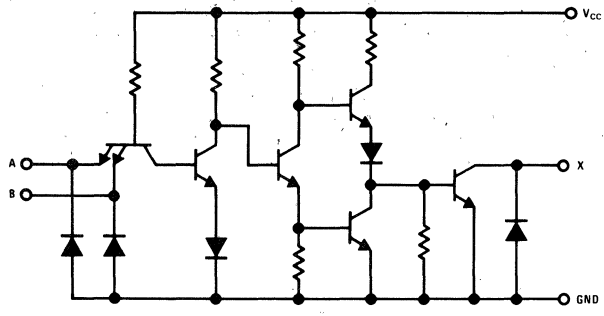
schematic diagrams (each driver)

DS3611 Dual AND Peripheral Drive



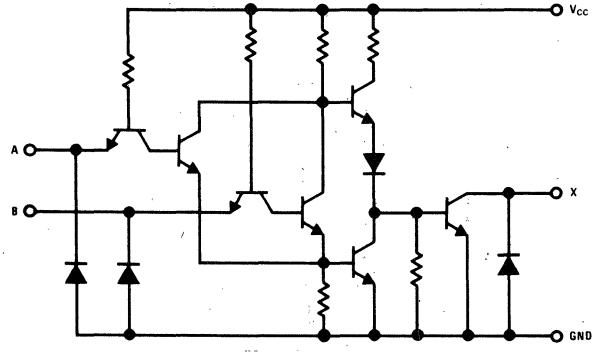
Note: 1/2 of unit shown.

DS3612 Dual NAND Peripheral Driver



Note: 1/2 of unit shown.

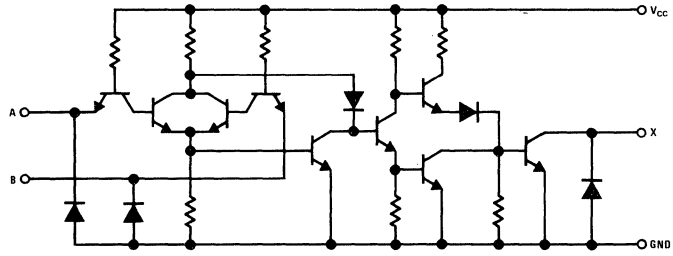
DS3613 Dual OR Peripheral Driver



Note: 1/2 of unit shown.

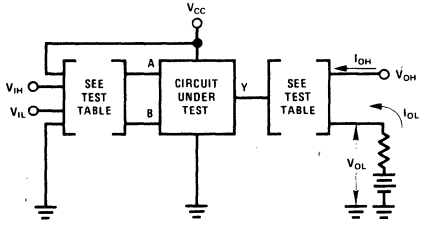
schematic diagrams (con't)

DS3614 Dual NOR Peripheral Driver



Note: 1/2 of unit shown.

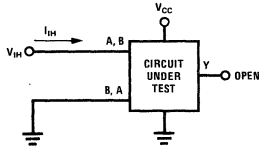
test circuits



CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
DS3611	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OH} I_{OL}	V_{OH} V_{OL}
DS3612	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} I_{OH}	V_{OL} V_{OH}
DS3613	V_{IH} V_{IL}	GND V_{IL}	I_{OH} I_{OL}	V_{OH} V_{OL}
DS3614	V_{IH} V_{IL}	GND V_{IL}	I_{OL} I_{OH}	V_{OL} V_{OH}

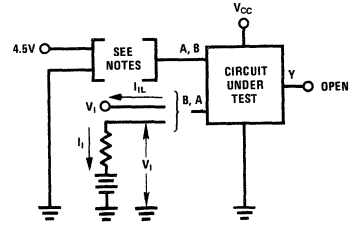
NOTE: Each input is tested separately.

FIGURE 1. V_{IH}, V_{IL}, V_{OH}, V_{OL}



Each input is tested separately.

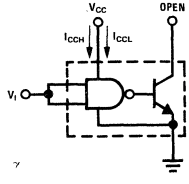
FIGURE 2. I_I, I_{IH}



Note 1: Each input is tested separately.

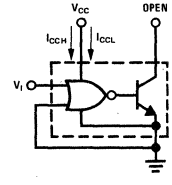
Note 2: When testing DS3613 and DS3614 input not under test is grounded. For all other circuits it is at 4.5V.

FIGURE 3. V_I, I_{IL}



Both gates are tested simultaneously.

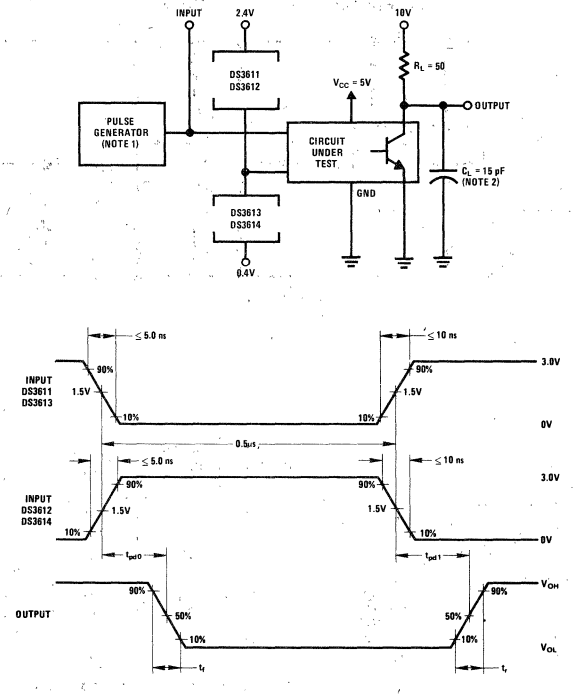
FIGURE 4. I_{CCH}, I_{CCL} for AND, NAND Circuits



Both gates are tested simultaneously.

FIGURE 5. I_{CCH}, I_{CCL} for OR, NOR Circuits

test circuit and switching time waveforms



Note 1: The pulse generator has the following characteristics: PRR = 1.0 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

FIGURE 6. Switching Times of Complete Drivers

NATIONAL

DS1631/DS3631, DS1632/DS3632, DS1633/DS3633, DS1634/DS3634
CMOS dual peripheral drivers

general description

The DS1631 series of dual peripheral drivers was designed to be a universal set of interface components for CMOS circuits.

Each circuit has CMOS compatible inputs with thresholds that track as a function of V_{CC} (approximately 1/2 V_{CC}). The inputs are PNPs providing the high impedance necessary for interfacing with CMOS.

Outputs have high voltage capability, minimum breakdown voltage is 56V at 250μA.

The outputs are Darlington connected transistors. This allows high current operation (300 mA max) at low internal V_{CC} current levels since base drive for the output transistor is obtained from the load in proportion to the required loading conditions. This is essential in order to minimize loading on the CMOS logic supply.

Typical V_{CC} = 5V power is 28 mW with both outputs ON. V_{CC} operating range is 4.5V to 15V.

The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance OFF state with the same breakdown levels as when V_{CC} was applied.

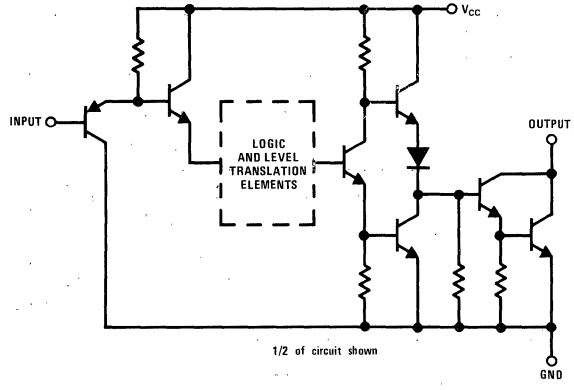
Pin-outs are the same as the respective logic functions found in the following popular series of circuits: DS75451, DS75461, DS3611. This feature allows direct conversion of present systems to the DM74C CMOS family and DS1631 series circuits with great power savings.

The DS1631 series is also TTL/DTL compatible at V_{CC} = 5V.

features

- CMOS compatible inputs
- TTL/DTL compatible inputs
- High impedance inputs — PNP's
- High output voltage breakdown — 56V min
- High output current capability — 300 mA max
- Same pin-outs and logic functions as DS75451, DS75461 and DS3611 series circuits
- Low V_{CC} power dissipation (28 mW both outputs "ON" at 5V)

schematic diagram (Equivalent Circuit)



SEE CONNECTION DIAGRAMS FOR ORDERING INFORMATION

absolute maximum ratings (Note 1)

Supply Voltage	16V
Voltage at Inputs	−0.3V to V_{CC} +0.3V
Output Voltage	56V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS1631/DS1632/ DS1633/DS1634	4.5	15	V
DS3631/DS3632/ DS3633/DS3634	4.75	15	V
Temperature, T_A			
DS1631/DS1632/ DS1633/DS1634	−55	+125	°C
DS3631/DS3632/ DS3633/DS3634	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
All Circuits								
V_{IH}	Logical "1" Input Voltage	*(Figure 1)*	V_{CC} = 5V		3.5	2.5		V
			V_{CC} = 10V		8.0	5		V
			V_{CC} = 15V		12.5	7.5		V
V_{IL}	Logical "0" Input Voltage	*(Figure 1)*	V_{CC} = 5V			2.5	1.5	V
			V_{CC} = 10V			5.5	2.0	V
			V_{CC} = 15V			7.5	2.5	V
I_{IH}	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V, *(Figure 2)*				0.1		µA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V, *(Figure 3)*	V_{CC} = 5V			−50		µA
			V_{CC} = 15V			−200		µA
V_{OH}	Output Breakdown Voltage	V_{CC} = 15V, I_{OH} = 250µA, *(Figure 1)*			56	65		V
V_{OL}	Output Low Voltage	V_{CC} = Min, *(Figure 1)*	I_{OL} = 100 mA			0.9		V
			I_{OL} = 300 mA			1.1		V
DS1631/DS3631								
$I_{CC(0)}$	Supply Currents	V_{IN} = 0V, *(Figure 4)*	V_{CC} = 5V	Output Low		7		mA
			V_{CC} = 15V	Both Drivers		14		mA
$I_{CC(1)}$		*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output High		2		mA
			V_{CC} = 15V, V_{IN} = 15V	Both Drivers		7.5		mA
t_{pd1}	Propagation to "1"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				200		ns
t_{pd0}	Propagation to "0"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
DS1632/DS3632								
$I_{CC(0)}$	Supply Currents	*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output Low		8		mA
			V_{CC} = 15V, V_{IN} = 15V			18		mA
$I_{CC(1)}$		V_{IN} = 0V, *(Figure 4)*	V_{CC} = 5V	Output High		2.5		mA
			V_{CC} = 15V			9		mA
t_{pd1}	Propagation to "1"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
t_{pd0}	Propagation to "0"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
DS1633/DS3633								
$I_{CC(0)}$	Supply Currents	V_{IN} = 0V, *(Figure 4)*	V_{CC} = 5V	Output Low		7.5		mA
			V_{CC} = 15V			16		mA
$I_{CC(1)}$		*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output High		2		mA
			V_{CC} = 15V, V_{IN} = 15V			7.2		mA
t_{pd1}	Propagation to "1"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				200		ns
t_{pd0}	Propagation to "0"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns

electrical characteristics (con't)

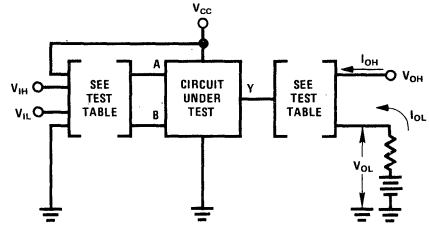
PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
DS1634/DS3634								
$I_{CC(0)}$	Supply Currents	*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output Low		7.5		mA
			V_{CC} = 15V, V_{IN} = 15V			18		mA
$I_{CC(1)}$		V_{IN} = 0V, *(Figure 4)*	V_{CC} = 5V	Output High		3		mA
			V_{CC} = 15V			11		mA
t_{pd1}	Propagation to "1"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
t_{pd0}	Propagation to "0"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1631, DS1632, DS1633 and DS1634 and across the 0°C to +70°C range for the DS3631, DS3632, DS3633 and DS3634. All typical values are for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

test circuits



CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
LM3611	V_{IH}	V_{IH}	I_{OH}	V_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
LM3612	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	I_{OH}	V_{OH}
LM3613	V_{IH}	GND	I_{OH}	V_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OL}
LM3614	V_{IH}	GND	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	I_{OH}	V_{OH}

Note: Each input is tested separately.

FIGURE 1. V_{IH}, V_{IL}, V_{OH}, V_{OL}

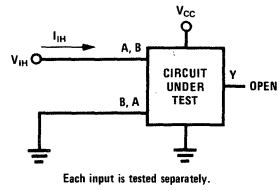
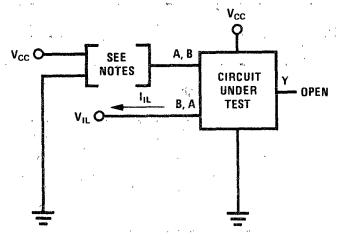


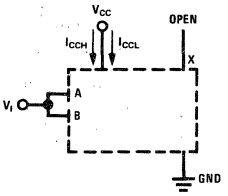
FIGURE 2. I_{IH}

test circuits (con't) and switching time waveforms



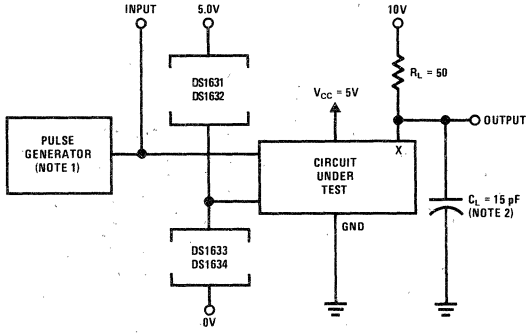
Note A: Each input is tested separately.
Note B: When testing DS1633 and DS1634 input not under test is grounded. For all other circuits it is at V_{CC}.

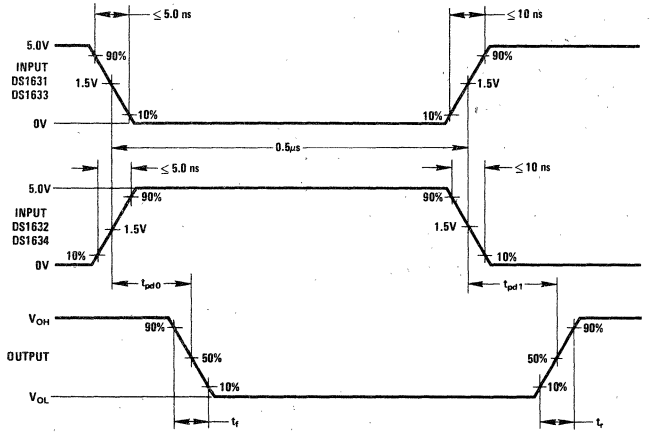
FIGURE 3. I_{IL}



Both gates are tested simultaneously.

FIGURE 4. I_{CC}



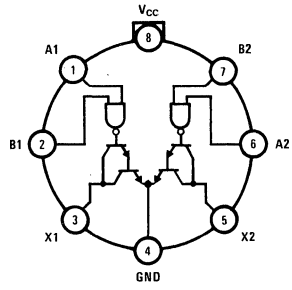


Note 1: The pulse generator has the following characteristics: PRR = 500 kHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

FIGURE 5. Switching Times.

connection diagrams, truth tables and ordering information

DS1631
Metal Can Package

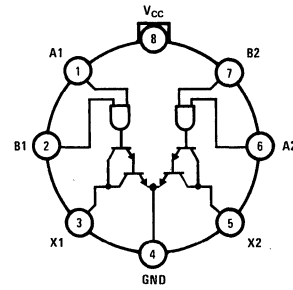


TOP VIEW

(Pin 4 is electrically connected to the case.)

Order Number DS1631H/DS3631H

DS1632
Metal Can Package

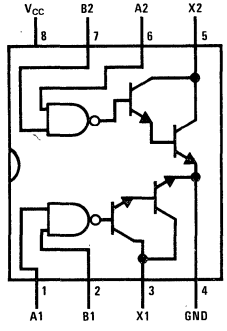


TOP VIEW

(Pin 4 is electrically connected to the case.)

Order Number DS1632H/DS3632H

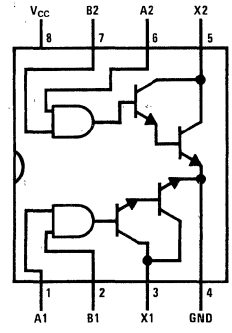
Dual-In-Line Package



TOP VIEW

Order Number 3631N

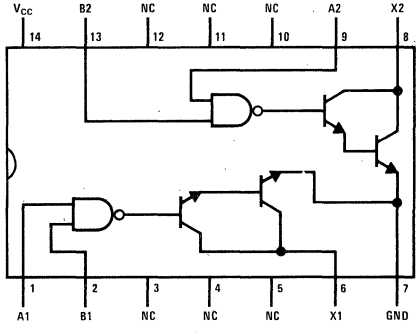
Dual-In-Line Package



TOP VIEW

Order Number DS3632N

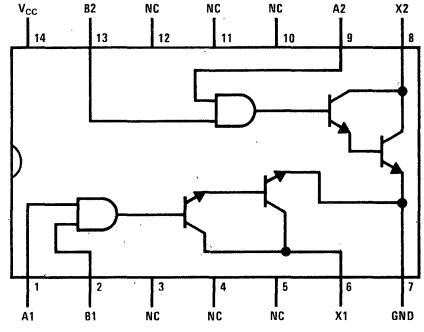
Dual-In-Line Package



TOP VIEW

Order Number DS1631J/DS3631J

Dual-In-Line Package



TOP VIEW

Order Number DS1632J/DS3632J

Positive logic: AB=X

A	B	OUTPUT X
0	0	0
1	0	0
0	1	0
1	1	1

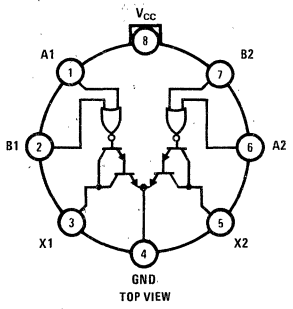
Positive logic: $\overline{AB}$=X

A	B	OUTPUT X
0	0	1
1	0	1
0	1	1
1	1	0

connection diagrams, truth tables and ordering information

DS1633

Metal Can Package

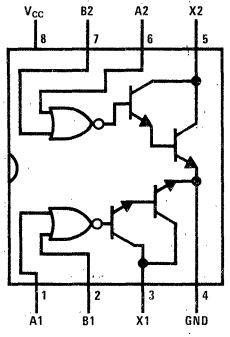


TOP VIEW

(Pin 4 is electrically connected to the case.)

Order Number DS1633H/DS3633H

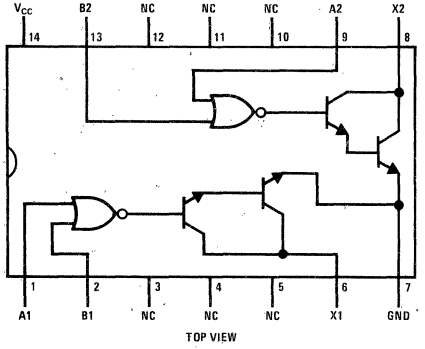
Dual-In-Line Package



TOP VIEW

Order Number DS3633N

Dual-In-Line Package



TOP VIEW

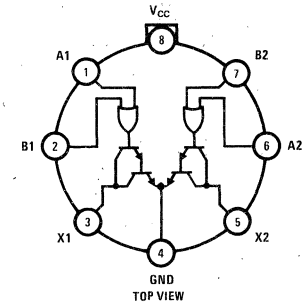
Order Number DS1633J/DS3633J

Positive logic: A + B = X

A	B	OUTPUT X
0	0	0
1	0	1
0	1	1
1	1	1

DS1634

Metal Can Package

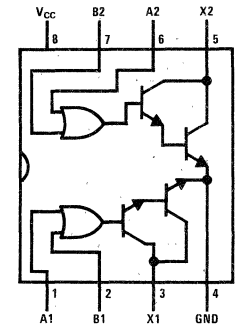


TOP VIEW

(Pin 4 is electrically connected to the case.)

Order Number DS1634H/DS3634H

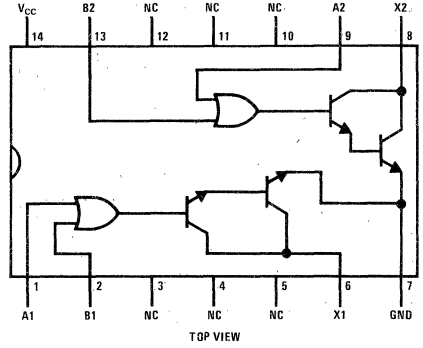
Dual-In-Line Package



TOP VIEW

Order Number DS3634N

Dual-In-Line Package



TOP VIEW

Order Number DS1634J/DS3634J

Positive logic: $\overline{A + B} = X$

A	B	OUTPUT X
0	0	1
1	0	0
0	1	0
1	1	0

NATIONAL

DS1686/DS3686 positive voltage relay driver

general description

The DS1686/DS3686 is a high voltage/current positive voltage relay driver having many features not available in present relay drivers.

PNP inputs provide both TTL/DTL compatibility and high input impedance for low input loading.

Output leakage is specified over temperature at an output voltage of 54V. Minimum output breakdown (ac/latch breakdown) is specified over temperature at 5 mA. This clearly defines the actual breakdown of the device since the circuit has incorporated in it an internal reference which does not allow output breakdown latching found in existing relay drivers. Additionally, this internal reference circuit feature will eliminate the need in most cases of an external clamping (inductive transient voltage protection) diode. When the output is turned "OFF" by input logic conditions the resulting inductive voltage transient seen at the output is detected by an internal zener reference. The reference then momentarily activates the output transistor long enough so that the relay energy is discharged. This feature eliminates the need of external circuit protection components and insures output transistor protection.

The outputs are Darlington connected transistors, which allow high current operation at low internal V_{CC} current levels—base drive for the output transistor is obtained from the load in proportion to the required loading conditions. Typical V_{CC} power with both outputs ON is 90 mW.

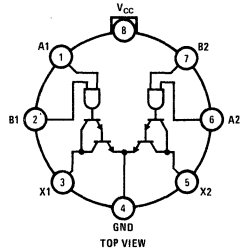
The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance OFF state with the same breakdown levels as when V_{CC} was applied.

features

- TTL/DTL/CMOS compatible inputs
- High impedance inputs (PNP's)
- High output voltage breakdown (65V typ)
- High output current capability (300 mA max)
- Internal protection circuit eliminates need for output protection diode in most applications
- Output breakdown protection if V_{CC} supply is lost
- Low V_{CC} power dissipation (90 mW (typ) both outputs "ON")
- Voltage and current levels compatible for use in telephone relay applications

connection diagrams

Metal Can Package

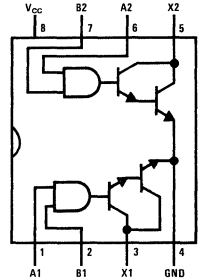


TOP VIEW

Pin 4 is in electrical contact with the case

Order Number DS1686H or DS3686H

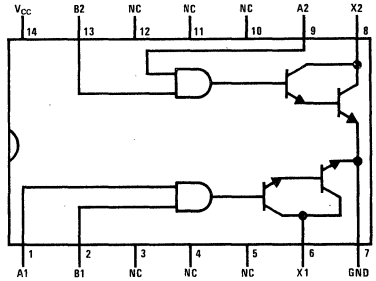
Dual-In-Line Package



TOP VIEW

Order Number DS3686N

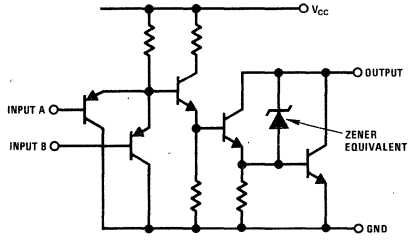
Dual-In-Line Package



TOP VIEW

Order Number DS1686J or DS3686J

schematic diagram



truth table

Positive logic: $\overline{AB} = X$

A	B	OUTPUT X
0	0	1
1	0	1
0	1	1
1	1	0

Logic "0" output "ON"
Logic "1" output "OFF"

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	15V
Output Voltage	56V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS1686	4.5	5.5	V
DS3686	4.75	5.25	V
Temperature, T_A			
DS1686	−55	+125	°C
DS3686	0	+70	°C

electrical characteristics (Notes 2 and 3)

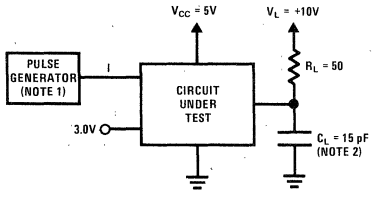
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage			2.0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 5.5V			1		μA
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−150		μA
V_{CD}	Input Clamp Voltage	V_{CC} = 5V, I_{CLAMP} = −12 mA, T_A = 25°C			−1.0		V
V_{OH}	Output Breakdown	V_{CC} = Max, V_{IN} = 0V, I_{OUT} = 5 mA			65		V
I_{OH}	Output Leakage	V_{CC} = Max, V_{IN} = 0V, V_{OUT} = 54V			2		μA
V_{OL}	Output "ON" Voltage	V_{CC} = Min, V_{IN} = 2V	I_{OUT} = 100 mA		0.9		V
			I_{OUT} = 300 mA		1.1		V
$I_{CC(1)}$	Supply Current (Both Drivers)	V_{CC} = Max, V_{IN} = 0V, Outputs Open			2.0		mA
$I_{CC(0)}$	Supply Current (Both Drivers)	V_{CC} = Max, V_{IN} = 3V, Outputs Open			18.0		mA
t_{pd0}	Propagation Delay to a Logical "0" (Output Turn "ON")	C_L = 15 pF, V_L = 10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5.0V			100		ns
t_{pd1}	Propagation Delay to a Logical "1" (Output Turn "OFF")	C_L = 15 pF, V_L = 10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5.0V			500		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1686 and across the 0°C to +70°C range for the DS3686. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

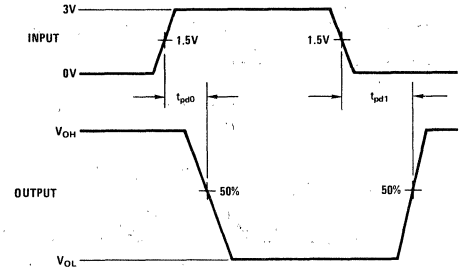
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

ac test circuit and switching time waveforms



Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, 50% duty cycle, $Z_{OUT} \geq 50\Omega$, $t_r = t_f \leq 10$ ns.

Note 2: C_L includes probe and jig capacitance.



Peripheral/Power Drivers

DS1687/DS3687 negative voltage relay driver

general description

The DS1687/DS3687 is a high voltage/current negative voltage relay driver having many features not available in present relay drivers.

PNP inputs provide both TTL/DTL compatibility and high input impedance for low input loading.

Output leakage is specified over temperature at an output voltage of −54V. Minimum output breakdown (ac/latch breakdown) is specified over temperature at −5 mA. This clearly defines the actual breakdown of the device since the circuit has incorporated in it an internal reference which does not allow output breakdown latching found in existing relay drivers. Additionally, this internal reference circuit feature will eliminate the need in most cases of an external clamping (inductive transient voltage protection) diode. When the output is turned "OFF" by input logic conditions the resulting inductive voltage transient seen at the output is detected by an internal zener reference. The reference then momentarily activates the output transistor long enough so that the relay energy is discharged. This feature eliminates the need of external circuit protection components and insures output transistor protection.

The outputs are Darlington connected transistors, which allow high current operation at low internal V_{CC} current levels—base drive for the output transistor is obtained from the load in proportion to the required loading conditions. Typical V_{CC} power with both outputs ON is 90 mW.

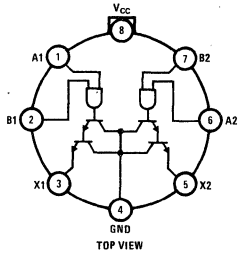
The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance OFF state with the same breakdown levels as when V_{CC} was applied.

features

- TTL/DTL/CMOS compatible inputs
- High impedance inputs (PNP's)
- High output voltage breakdown (−65V typ)
- High output current capability (300 mA max)
- Internal protection circuit eliminates need for output protection diode in most applications
- Output breakdown protection if V_{CC} supply is lost
- Low V_{CC} power dissipation (90 mW (typ) both outputs "ON")
- Voltage and current levels compatible for use in telephone relay applications

connection diagrams

Metal Can Package

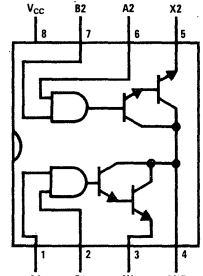


TOP VIEW

Pin 4 is in electrical contact with the case

Order Number DS1687H or DS3687H

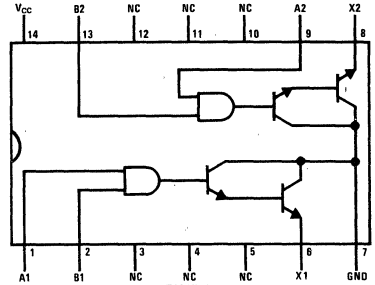
Dual-In-Line Package



TOP VIEW

Order Number DS3687N

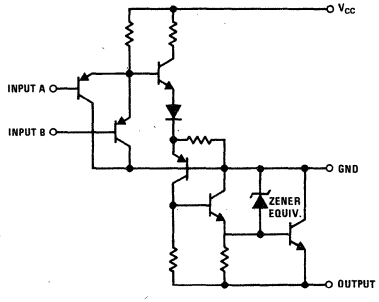
Dual-In-Line Package



TOP VIEW

Order Number DS1687J or DS3687J

schematic diagram



truth table

Positive logic: $\overline{AB} = X$

A	B	OUTPUT X
0	0	1
1	0	1
0	1	1
1	1	0

Logic "0" output "ON"
Logic "1" output "OFF"

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	15V
Output Voltage	−56V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS1687	4.5	5.5	V
DS3687	4.75	5.25	V
Temperature, T_A			
DS1687	−55	+125	°C
DS3687	0	+70	°C

electrical characteristics (Notes 2 and 3)

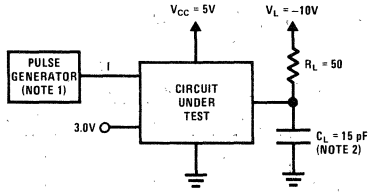
	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage			2.0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 5.5V			1.0		μA
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−150		μA
V_{CD}	Input Clamp Voltage	V_{CC} = 5V, I_{CLAMP} = −12 mA, T_A = 25°C			−1.0		V
V_{OH}	Output Breakdown	V_{CC} = Max, V_{IN} = 0V, I_{OUT} = −5 mA			−65		V
I_{OH}	Output Leakage	V_{CC} = Max, V_{IN} = 0V, V_{OUT} = −54V			−2		μA
V_{OL}	Output "ON" Voltage	V_{CC} = Min, V_{IN} = 2V	I_{OUT} = −100 mA		−0.9		V
			I_{OUT} = −300 mA		−1.1		V
$I_{CC(1)}$	Supply Current (Both Drivers)	V_{CC} = Max, V_{IN} = 0V, Outputs Open			2.0		mA
$I_{CC(0)}$	Supply Current (Both Drivers)	V_{CC} = Max, V_{IN} = 3V, Outputs Open			18.0		mA
$t_{pd(ON)}$	Propagation Delay to a Logical "0" (Output Turn "ON")	C_L = 15 pF, V_L = −10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5.0V			100		ns
$t_{pd(OFF)}$	Propagation Delay to a Logical "1" (Output Turn "OFF")	C_L = 15 pF, V_L = −10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5.0V			500		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1687 and across the 0°C to +70°C range for the DS3687. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

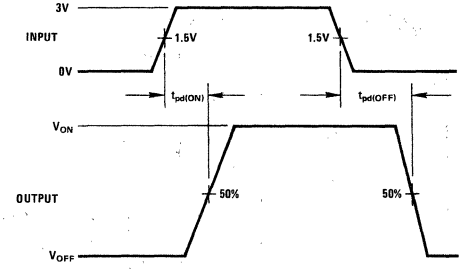
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

ac test circuit and switching time waveforms



Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, 50% duty cycle, $Z_{OUT} \approx 50\Omega$, $t_r = t_f \leq 10$ ns.

Note 2: C_L includes probe and jig capacitance.



Peripheral/Power Drivers

NATIONAL

DS55450/DS75450 series dual peripheral drivers

general description

The DS55450/DS75450 series of dual peripheral drivers are a family of versatile devices designed for use in systems that use TTL or DTL logic. Typical applications include high speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, bus drivers and memory drivers.

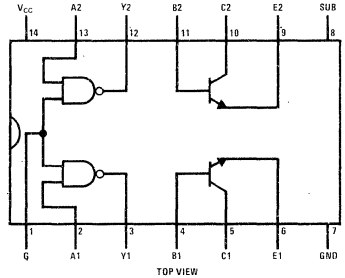
The DS55450/DS75450 series are unique general purpose devices each featuring two standard Series 54/74 TTL gates and two uncommitted, high current, high voltage NPN transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The DS55451/DS75451, DS55452/DS75452, DS55453/DS75453 and DS55454/DS75454 are dual peripheral AND, NAND, OR and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

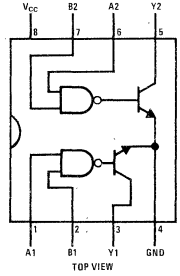
features

- 300 mA output current capability
- High voltage outputs
- No output latch-up at 20V
- High speed switching
- Choice of logic function
- TTL or DTL compatible diode-clamped inputs
- Standard supply voltages
- Replaces TI "A" and "B" series

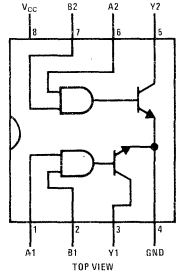
connection diagrams (Dual-In-Line and Metal Can Packages)



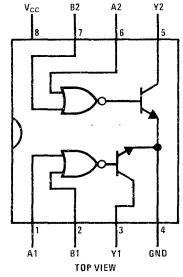
Order Number
DS55450J, DS75450J, or DS75450N



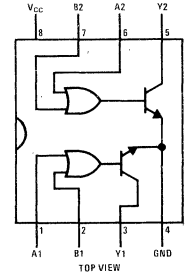
Order Number DS75451N



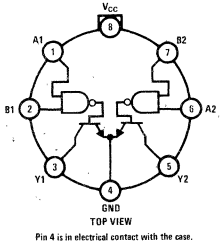
Order Number DS75452N



Order Number DS75453N

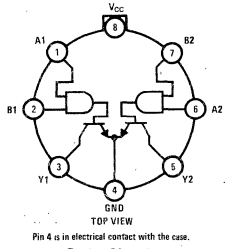


Order Number DS75454N



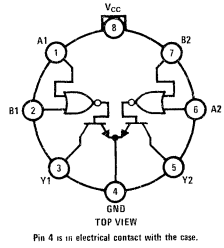
Pin 4 is in electrical contact with the case.

Order Number
DS55451H or DS75451H



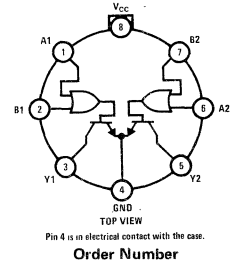
Pin 4 is in electrical contact with the case.

Order Number
DS55452H or DS75452H



Pin 4 is in electrical contact with the case.

Order Number
DS55453H or DS75453H



Pin 4 is in electrical contact with the case.

Order Number
DS55454H or DS75454H

absolute maximum ratings (Note 1)

Supply Voltage, (V_{CC}) (Note 2)	7.0V
Input Voltage	5.5V
Inter-emitter Voltage (Note 3)	5.5V
V_{CC}-to-Substrate Voltage	
DS55450/DS75450	35V
Collector-to-Substrate Voltage	
DS55450/DS75450	35V
Collector-Base Voltage	
DS55450/DS75450	35V
Collector-Emitter Voltage (Note 4)	
DS55450/DS75450	30V
Emitter-Base Voltage	
DS55450/DS75450	5.0V
Output Voltage (Note 5)	
DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454	30V
Collector Current (Note 6)	
DS55450/DS75450	300 mA
Output Current (Note 6)	
DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454	300 mA
Continuous Total Dissipation	800 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C

operating conditions (Note 7)

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS5545X	4.5	5.5	V
DS7545X	4.75	5.25	V
Temperature, (T_A)			
DS5545X	−55	+125	°C
DS7545X	0	+70	°C

dc electrical characteristics DS55450/DS75450 (Notes 8 and 9)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
TTL GATES								
V_{IH}	High Level Input Voltage	*(Figure 1)*			2			V
V_{IL}	Low Level Input Voltage	*(Figure 2)*					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA, *(Figure 3)*					−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, I_{OH} = −400μA, *(Figure 2)*			2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, I_{OL} = 16 mA *(Figure 1)*		DS55450		0.22	0.5	V
				DS75450		0.22	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 4)*		Input A			1	mA
				Input G			2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 4)*		Input A			40	μA
				Input G			80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 3)*		Input A			−1.6	mA
				Input G			−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max, *(Figure 5)*, (Note 10)			−18		−55	mA
I_{CCH}	Supply Current	V_{CC} = Max, V_I = 0V, Outputs High, *(Figure 6)*				2	4	mA
I_{CCL}	Supply Current	V_{CC} = Max, V_I = 5V, Outputs Low, *(Figure 6)*				6	11	mA
OUTPUT TRANSISTORS								
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100μA, I_E = 0			35			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100μA, R_{BE} = 500Ω			30			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100μA, I_C = 0			5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3V, (Note 11)	DS55450, T_A = +25°C	I_C = 100 mA	25			V
				I_C = 300 mA	30			V
			DS55450, T_A = −55°C	I_C = 100 mA	10			V
				I_C = 300 mA	15			V
			DS75450, T_A = +25°C	I_C = 100 mA	25			V
				I_C = 300 mA	30			V
			DS75450, T_A = 0°C	I_C = 100 mA	20			V
				I_C = 300 mA	25			V
V_{BE}	Base-Emitter Voltage	(Note 11)	DS55450	I_B = 10 mA, I_C = 100 mA		0.85	1.2	V
				I_B = 30 mA, I_C = 300 mA		1.05	1.4	V
			DS75450	I_B = 10 mA, I_C = 100 mA		0.85	1	V
				I_B = 30 mA, I_C = 300 mA		1.05	1.2	V
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	(Note 11)	DS55450	I_B = 10 mA, I_C = 100 mA		0.25	0.5	V
				I_B = 30 mA, I_C = 300 mA		0.5	0.8	V
			DS75450	I_B = 10 mA, I_C = 100 mA		0.25	0.4	V
				I_B = 30 mA, I_C = 300 mA		0.5	0.7	V

dc electrical characteristics (con't)

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (Notes 8 and 9)

PARAMETER		CONDITIONS				MIN	TYP	MAX	UNITS
V_{IH}	High-Level Input Voltage	*(Figure 7)*				2			V
V_{IL}	Low-Level Input Voltage							0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA						−1.5	V
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, *(Figure 7)*	V_{IL} = 0.8V	I_{OL} = 100 mA	DS55451, DS55453		0.25	0.5	V
					DS75451, DS75453		0.25	0.4	V
				I_{OL} = 300 mA	DS55451, DS55453		0.5	0.8	V
					DS75451, DS75453		0.5	0.7	V
			V_{IH} = 2V	I_{OL} = 100 mA	DS55452, DS55454		0.25	0.5	V
					DS75452, DS75454		0.25	0.4	V
				I_{OL} = 300 mA	DS55452, DS55454		0.5	0.8	V
					DS75452, DS75454		0.5	0.7	V
I_{OH}	High-Level Output Current	V_{CC} = Min, *(Figure 7)*	V_{OH} = 30V	V_{IH} = 2V	DS55451, DS55453			300	μA
					DS75451, DS75453			100	μA
				V_{IL} = 0.8V	DS55452, DS55454			300	μA
					DS75452, DS75454			100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 9)*						1	mA
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 9)*						40	μA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 8)*					−1	−1.6	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = Max, *(Figure 10)*	V_I = 5V		DS55451/DS75451		7	11	mA
			V_I = 0V		DS55452/DS75452		11	14	mA
			V_I = 5V		DS55453/DS75453		8	11	mA
			V_I = 0V		DS55454/DS75454		13	17	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = Max, *(Figure 10)*	V_I = 0V		DS55451/DS75451		52	65	mA
			V_I = 5V		DS55452/DS75452		56	71	mA
			V_I = 0V		DS55453/DS75453		54	68	mA
			V_I = 5V		DS55454/DS75454		61	79	mA

ac switching characteristics

DS55450/DS75450 (V_{CC} = 5V, T_A = 25°C)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-To-High Level Output	C_L = 15 pF	R_L = 400Ω, TTL Gates, *(Figure 12)*		12	22	ns
			R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*		20	30	ns
t_{PHL}	Propagation Delay Time, High-To-Low Level Output	C_L = 15 pF	R_L = 400Ω, TTL Gates, *(Figure 12)*		8	15	ns
			R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*		20	30	ns
t_{TLH}	Transition Time, Low-To-High Level Output	C_L = 15 pF, R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*			7	12	ns
t_{THL}	Transition Time, High-To-Low Level Output	C_L = 15 pF, R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*			9	15	ns
V_{OH}	High-Level Output Voltage After Switching	V_S = 20V, $I_C \approx$ 300 mA, R_{BE} = 500Ω, *(Figure 15)*		V_S−6.5			mV
t_D	Delay Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, I_B = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, *(Figure 13)*, (Note 12)			8	15	ns
t_R	Rise Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, I_B = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, *(Figure 13)*, (Note 12)			12	20	ns
t_S	Storage Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, I_B = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, *(Figure 13)*, (Note 12)			7	15	ns
t_F	Fall Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, I_B = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, *(Figure 13)*, (Note 12)			6	15	ns

ac switching characteristics (con't)

DS55451/DS75451, DS55452/DS75452, DS55453/DS75453, DS55454/DS75454 (V_{CC} = 5V, T_A = 25°C)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-To-High Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)*	DS55451/DS75451		18	25	ns
			DS55452/DS75452		26	35	ns
			DS55453/DS75453		18	25	ns
			DS55454/DS75454		27	35	ns
t_{PHL}	Propagation Delay Time, High-To-Low Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)*	DS55451/DS75451		18	25	ns
			DS55452/DS75452		24	35	ns
			DS55453/DS75453		16	25	ns
			DS55454/DS75454		24	35	ns
t_{TLH}	Transition Time, Low-To-High Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)*			5	8	ns
t_{THL}	Transition Time, High-To-Low Level Output	C_L = 15 pF, R_L = 50Ω, $I_O \approx$ 200 mA, *(Figure 14)*			7	12	ns
V_{OH}	High-Level Output Voltage After Switching	V_S = 20V, $I_O \approx$ 300 mA, *(Figure 15)*		V_S–6.5			mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: The voltage between two emitters of a multiple-emitter transistor.

Note 4: Value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500Ω.

Note 5: The maximum voltage which should be applied to any output when it is in the "OFF" state.

Note 6: Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

Note 7: For the DS55450/DS75450 only, the substrate (pin 8) must always be at the most-negative device voltage for proper operation.

Note 8: Unless otherwise specified min/max limits apply across the –55°C to +125°C temperature range for the DS55450 series and across the 0°C to +70°C range for the DS75450 series. All typicals are given for V_{CC} = +5V and T_A = 25°C.

Note 9: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

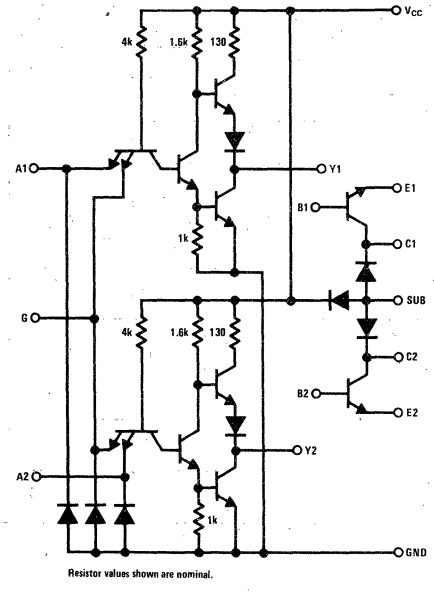
Note 10: Only one output at a time should be shorted.

Note 11: These parameters must be measured using pulse techniques. t_W = 300μs, duty cycle < 2%.

Note 12: Applies to output transistors only.

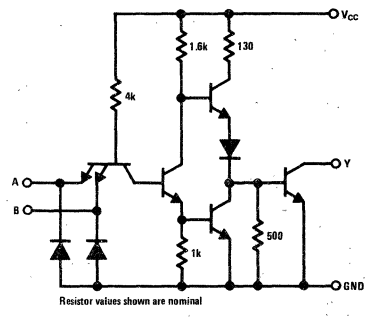
schematic diagrams

DS55450/DS75450



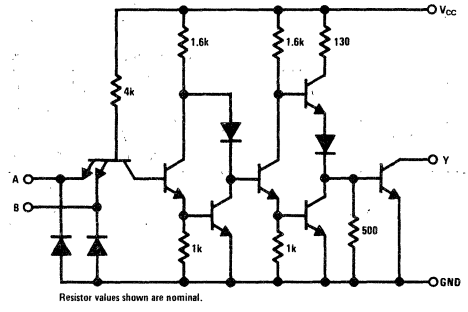
Resistor values shown are nominal.

DS55451/DS75451



Resistor values shown are nominal.

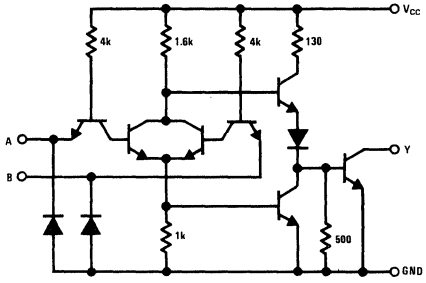
DS55452/DS75452



Resistor values shown are nominal.

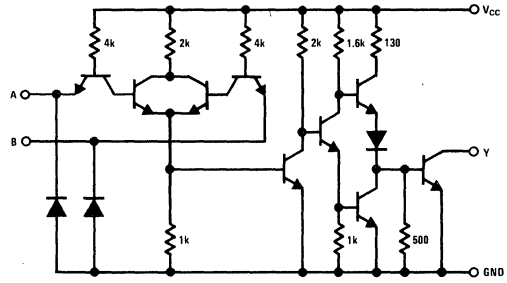
schematic diagrams (con't)

DS55453/DS75453



Resistor values shown are nominal.

DS55454/DS75454



Resistor values shown are nominal.

truth tables (H = high level, L = low level)

DS55451/DS75451

A	B	Y
L	L	L (ON State)
L	H	L (ON State)
H	L	L (ON State)
H	H	H (OFF State)

DS55452/DS75452

A	B	Y
L	L	H (OFF State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	L (ON State)

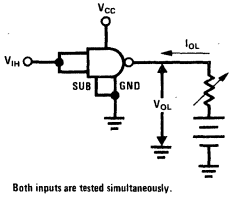
DS55453/DS75453

A	B	Y
L	L	L (ON State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	H (OFF State)

DS55454/DS75454

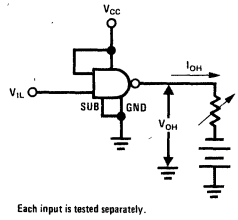
A	B	Y
L	L	H (OFF State)
L	H	L (ON State)
H	L	L (ON State)
H	H	L (ON State)

dc test circuits



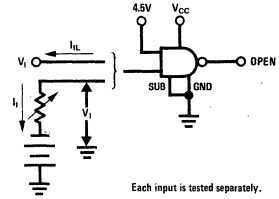
Both inputs are tested simultaneously.

FIGURE 1. V_{IH}, V_{OL}



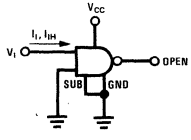
Each input is tested separately.

FIGURE 2. V_{IL}, V_{OH}



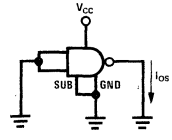
Each input is tested separately.

FIGURE 3. V_I, I_{IL}



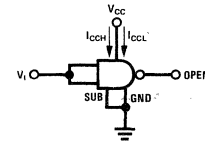
Each input is tested separately.

FIGURE 4. I_I, I_{IH}



Each gate is tested separately.

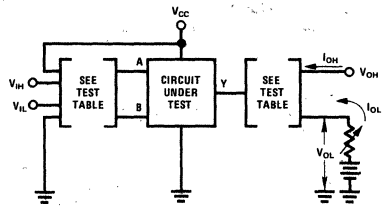
FIGURE 5. I_{OS}



Both gates are tested simultaneously

FIGURE 6. I_{CCH}, I_{CCL}

dc test circuits (con't)



CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
DS54451	V_{IH} V_{IL}	V_{IH} V_{CC}	V_{OH} I_{OL}	I_{OH} V_{OL}
DS54452	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} V_{OH}	V_{OL} I_{OH}
DS54453	V_{IH} V_{IL}	Gnd V_{IL}	V_{OH} I_{OL}	I_{OH} V_{OL}
DS54454	V_{IH} V_{IL}	Gnd V_{IL}	I_{OL} V_{OH}	V_{OL} I_{OH}

FIGURE 7. V_{IH}, V_{IL}, I_{OH}, V_{OL}

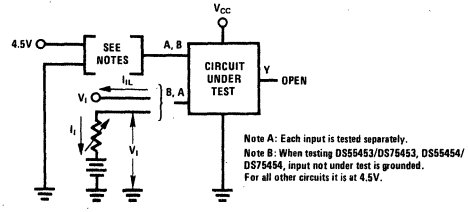


FIGURE 8. V_I, I_{IL}

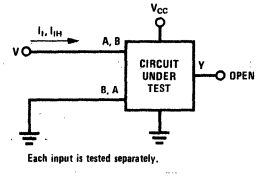


FIGURE 9. I_I, I_{IH}

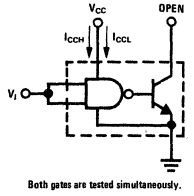


FIGURE 10. I_{CCH}, I_{CCL} for AND, NAND Circuits

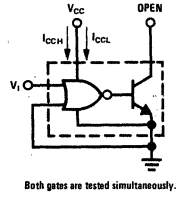
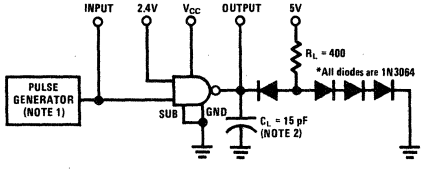
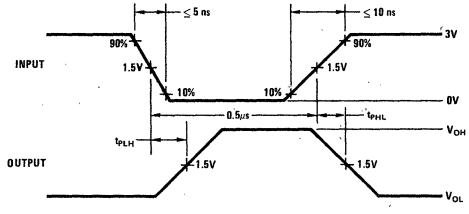


FIGURE 11. I_{CCH}, I_{CCL} for OR, NOR Circuits

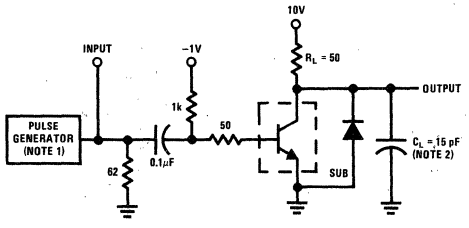
ac test circuits and switching time waveforms

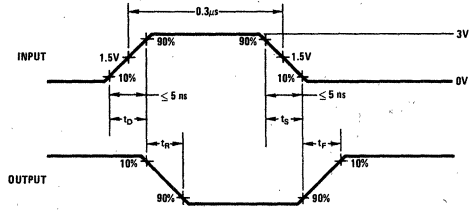




Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L include probe and jig capacitance.

FIGURE 12. Propagation Delay Times, Each Gate (DS55450/DS75450 Only)

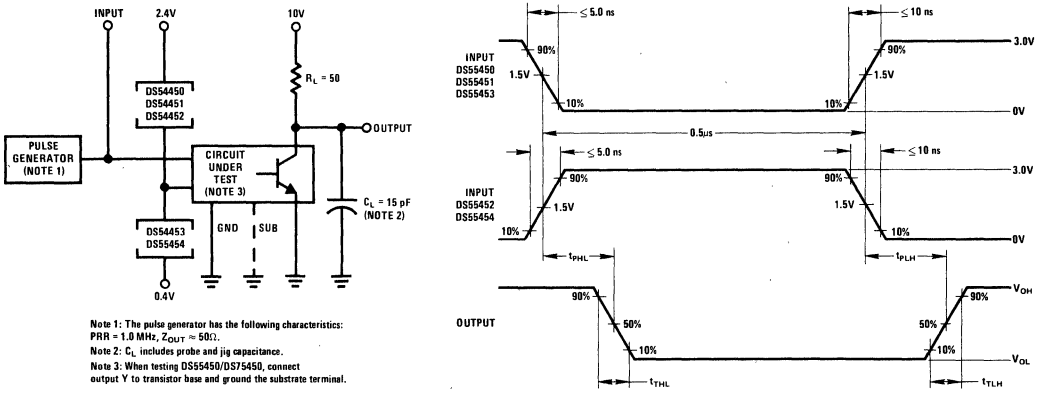




Note 1: The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

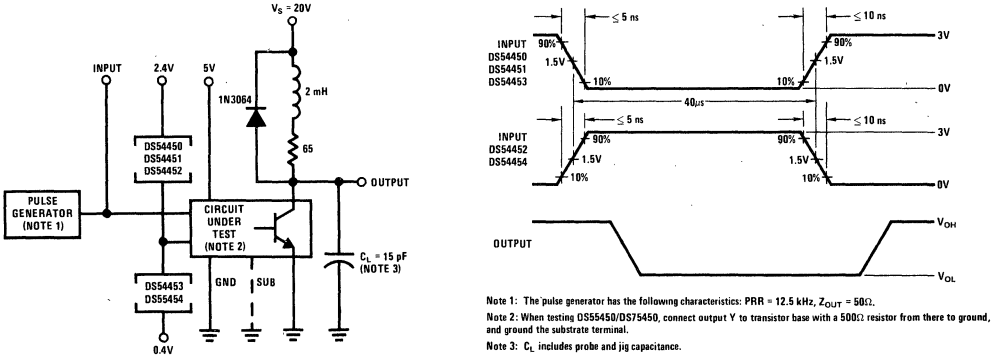
FIGURE 13. Switching Times, Each Transistor (DS55450/DS75450 Only)

ac test circuits and switching time waveforms (con't)



Note 1: The pulse generator has the following characteristics: PRR = 1.0 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.
Note 3: When testing DS55450/DS75450, connect output Y to transistor base and ground the substrate terminal.

FIGURE 14. Switching Times of Complete Drivers



Note 1: The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{OUT} = 50\Omega$.
Note 2: When testing DS55450/DS75450, connect output Y to transistor base with a 500Ω resistor from there to ground, and ground the substrate terminal.
Note 3: C_L includes probe and jig capacitance.

FIGURE 15. Latch-Up Test of Complete Drivers

typical performance characteristics

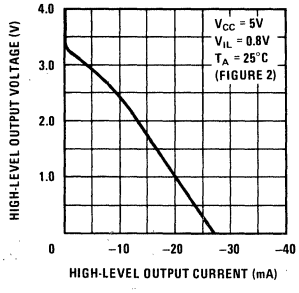


FIGURE 16. DS55450/DS75450 TTL Gate High-Level Output Voltage vs High-Level Output Current

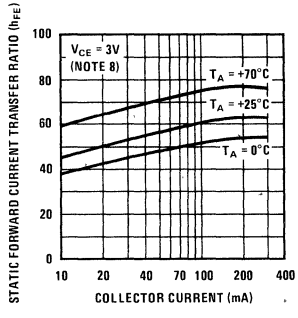


FIGURE 17. DS55450/DS75450 Transistor Static Forward Current Transfer Ratio vs Collector Current

typical performance characteristics (con't)

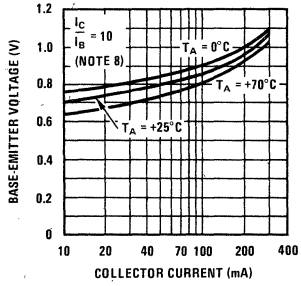


FIGURE 18. DS55450/DS75450 Transistor Base-Emitter Voltage vs Collector Current

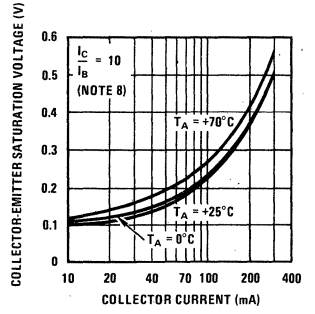


FIGURE 19. Transistor Collector-Emitter Saturation Voltage vs Collector Current

typical applications

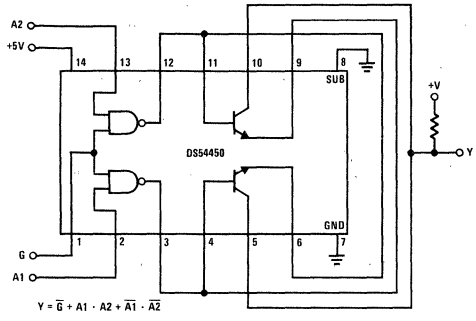


FIGURE 20. Gated Comparator

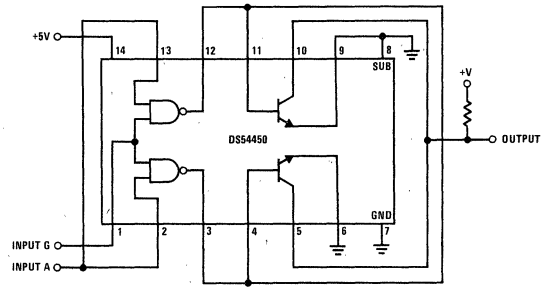


FIGURE 21. 500 mA Sink

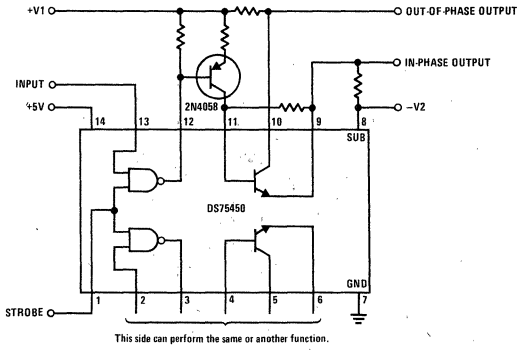


FIGURE 22. Floating Switch

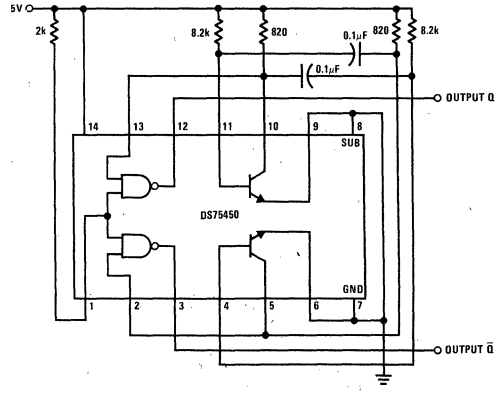
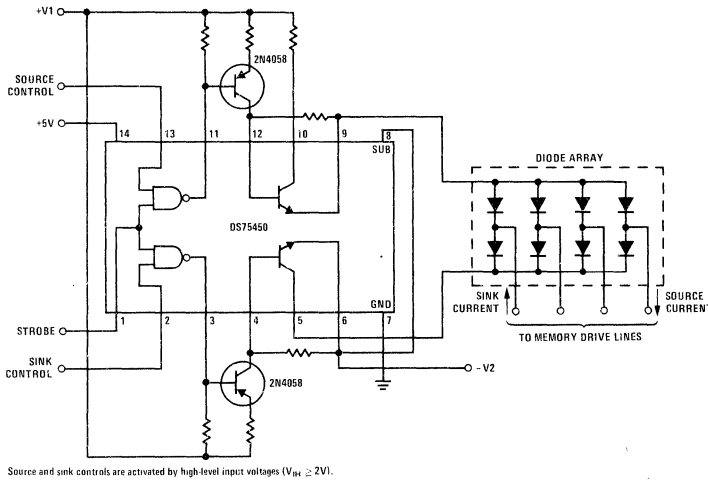


FIGURE 23. Square-Wave Generator

typical applications (con't)



Source and sink controls are activated by high-level input voltages ($V_{IH} \geq 2V$).

FIGURE 24. Core Memory Driver

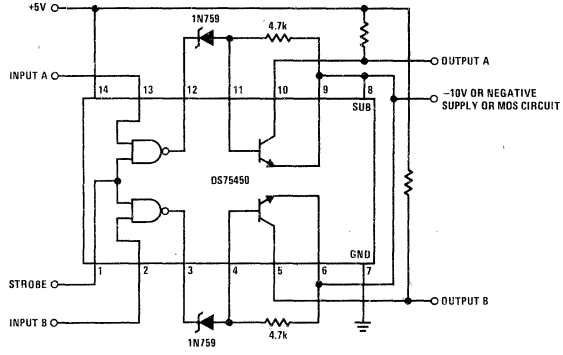


FIGURE 25. Dual TTL-to-MOS Driver

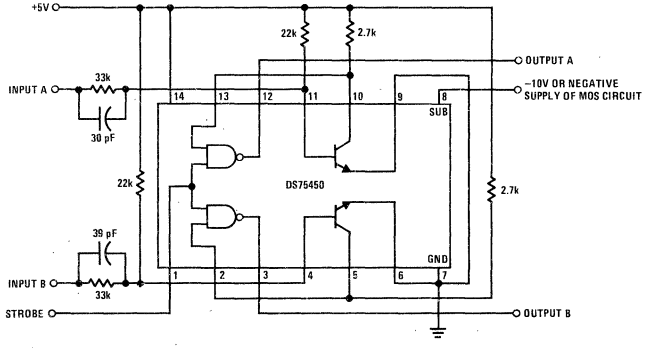


FIGURE 26. Dual MOS-to-TTL Driver

typical applications (con't)

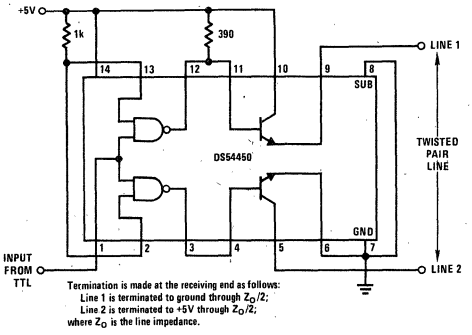


FIGURE 27. Balanced Line Driver

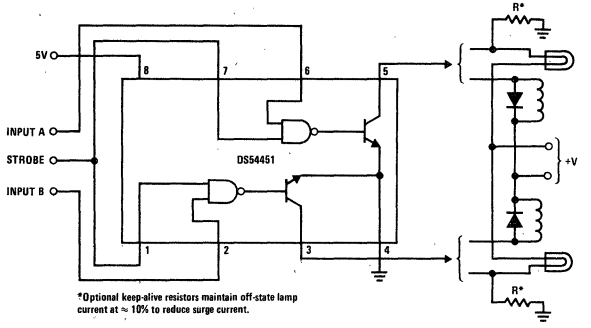


FIGURE 28. Dual Lamp or Relay Driver

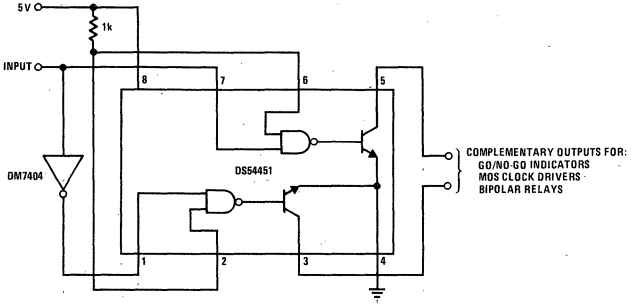


FIGURE 29. Complementary Driver

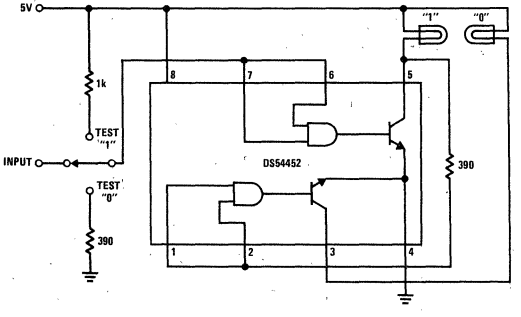


FIGURE 30. TTL or DTL Positive Logic-Level Detector

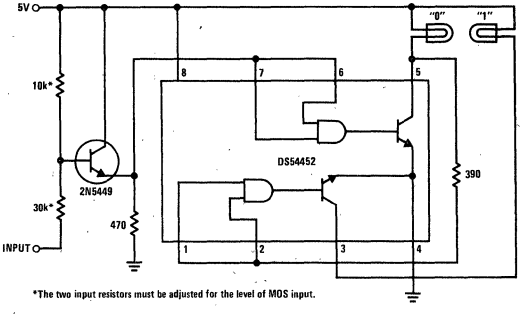


FIGURE 31. MOS Negative Logic-Level Detector

typical applications (con't)

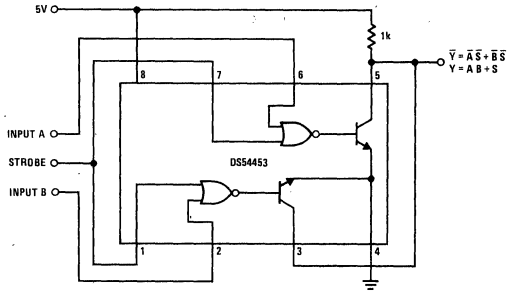
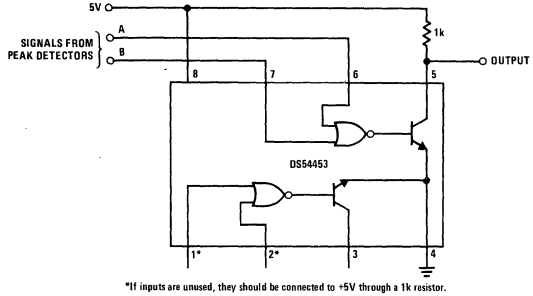
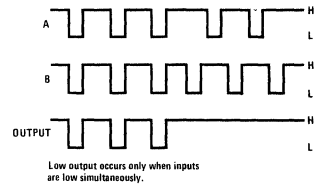


FIGURE 32. Logic Signal Comparator



*If inputs are unused, they should be connected to +5V through a 1k resistor.



Low output occurs only when inputs are low simultaneously.

FIGURE 33. In-Phase Detector

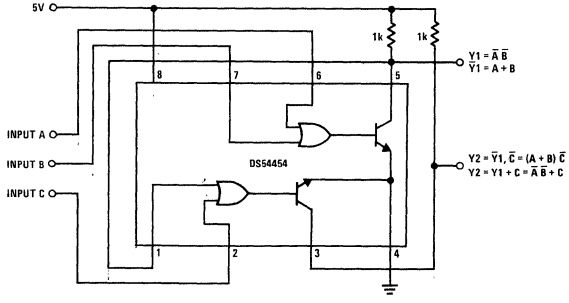


FIGURE 34. Multifunction Logic-Signal Comparator

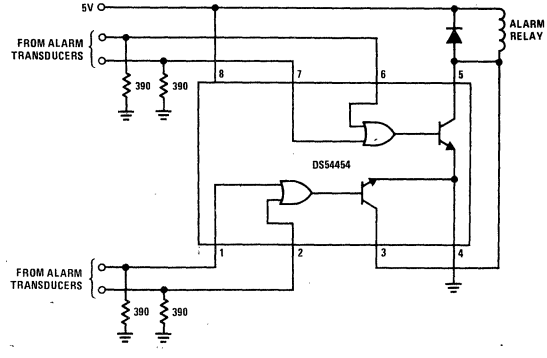


FIGURE 35. Alarm Detector

NATIONAL

Peripheral/Power Drivers

DS55460/DS75460 series dual peripheral drivers

general description

The DS55460/DS75460 series of dual peripheral drivers are functionally interchangeable with DS55450/DS75450 series peripheral drivers, but are designed for use in systems that require higher breakdown voltages than DS55450/DS75450 series can provide at the expense of slightly slower switching speeds. Typical applications include power drivers, logic buffers, lamp drivers, relay drivers, MOS drivers, line drivers and memory drivers.

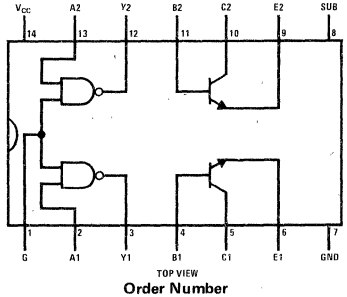
The DS55460 and DS75460 are unique general-purpose devices each featuring two standard 54/74 series TTL gates and two uncommitted, high current, high voltage, NPN transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The DS55461/DS75461, DS55462/DS75462, DS55463/DS75463 and DS55464/DS75464 are dual peripheral AND, NAND, OR and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

features

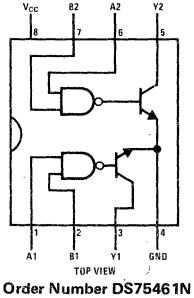
- 300 mA output current capability
- High voltage outputs
- No output latch-up at 30V
- Medium speed switching
- Circuit flexibility for varied applications and choice of logic function
- TTL or DTL compatible diode-clamped inputs
- Standard supply voltages

connection diagrams (Dual-In-Line and Metal Can Packages)



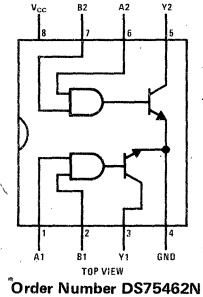
TOP VIEW

Order Number
DS55460J, DS75460J, or DS75460N



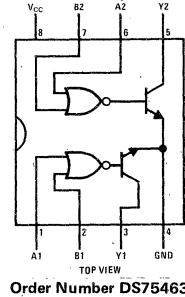
TOP VIEW

Order Number DS75461N



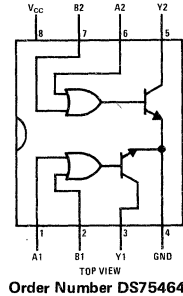
TOP VIEW

Order Number DS75462N



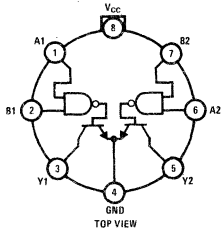
TOP VIEW

Order Number DS75463N



TOP VIEW

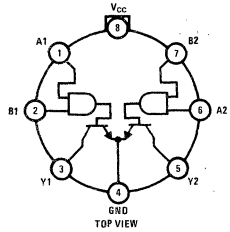
Order Number DS75464N



TOP VIEW

Pin 4 is in electrical contact with the case.

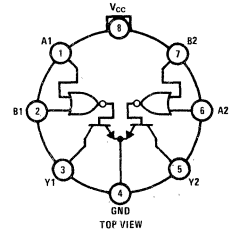
Order Number
DS55461H or DS75461H



TOP VIEW

Pin 4 is in electrical contact with the case.

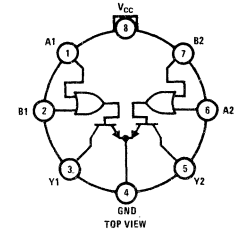
Order Number
DS55462H or DS75462H



TOP VIEW

Pin 4 is in electrical contact with the case.

Order Number
DS55463H or DS75463H



TOP VIEW

Pin 4 is in electrical contact with the case.

Order Number
DS55464H or DS75464H

absolute maximum ratings (Note 1)

Supply Voltage (Note 2)	7V
Input Voltage	5.5V
Inter-emitter Voltage (Note 3)	5.5V
V_{CC}-to-Substrate Voltage	
DS55460/DS75460	40V
Collector-to-Substrate Voltage	
DS55460/DS75460	40V
Collector-Base Voltage	
DS55460/DS75460	40V
Collector-Emitter Voltage	
DS55460/DS75460 (Note 4)	40V
DS55460/DS75460 (Note 5)	25V
Emitter-Base Voltage	
DS55460/DS75460	5V
Output Voltage (Note 6)	
DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464	35V
Collector Current (Note 7)	
DS55460/DS75460	300 mA
Output Current (Note 7)	
DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464	300 mA
Continuous Total Dissipation	800 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C

operating conditions (Note 7)

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS5546X	4.5	5.5	V
DS7546X	4.75	5.25	V
Temperature (T_A)			
DS5546X	−55	+125	°C
DS7546X	0	+70	°C

dc electrical characteristics

DS55460/DS75460 (Notes 8 and 9)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
TTL GATES								
V_{IH}	High Level Input Voltage	*(Figure 1)*			2			V
V_{IL}	Low Level Input Voltage	*(Figure 2)*					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA, *(Figure 3)*				−1.2	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, I_{OH} = −400μA, *(Figure 2)*			2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, I_{OL} = 16 mA, *(Figure 1)*	DS55460			0.25	0.5	V
			DS75460			0.25	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 4)*	Input A				1	mA
			Input G				2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 4)*	Input A				40	μA
			Input G				80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 3)*	Input A				−1.6	mA
			Input G				−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max, (Note 10), *(Figure 5)*			−18	−35	−55	mA
I_{CCH}	Supply Current	V_{CC} = Max, V_I = 0V, Outputs High, *(Figure 6)*				2.8	4	mA
I_{CCL}	Supply Current	V_{CC} = Max, V_I = 5V, Outputs Low, *(Figure 6)*				7	11	mA
OUTPUT TRANSISTORS								
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100μA, I_E = 0			40			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100μA, R_{BE} = 500Ω			40			V
$V_{(BR)CEO}$		I_C = 10 mA, I_B = 0 (Note 12)			25			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100μA, I_C = 0			5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3V, (Note 12)	DS55460, T_A = 25°C	I_C = 100 mA	25			
				I_C = 300 mA	30			
			DS55460, T_A = −55°C	I_C = 100 mA	10			
				I_C = 300 mA	15			
			DS75460, T_A = 25°C	I_C = 100 mA	25			
				I_C = 300 mA	30			
			DS75460, T_A = 0°C	I_C = 100 mA	20			
				I_C = 300 mA	25			

dc electrical characteristics (con't)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{BE}	Base-Emitter Voltage	(Note 12)	DS55460	I_B = 10 mA, I_C = 100 mA		0.85	1.2	V
				I_B = 30 mA, I_C = 300 mA		1	1.4	V
			DS75460	I_B = 10 mA, I_C = 100 mA		0.85	1	V
				I_B = 30 mA, I_C = 300 mA		1	1.2	V
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	(Note 12)	DS55460	I_B = 10 mA, I_C = 100 mA		0.25	0.5	V
				I_B = 30 mA, I_C = 300 mA		0.45	0.8	V
			DS75460	I_B = 10 mA, I_C = 100 mA		0.25	0.4	V
				I_B = 30 mA, I_C = 300 mA		0.45	0.7	V

ac switching characteristics

DS55460/DS75460 V_{CC} = 5V, T_A = 25°C

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-To-High Level Output	C_L = 15 pF	R_L = 400Ω, TTL Gates Only, *(Figure 12)*		22		ns
			R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*		45	65	ns
t_{PHL}	Propagation Delay Time, High-To-Low Level Output	C_L = 15 pF	R_L = 400Ω, TTL Gates Only, *(Figure 12)*		8		ns
			R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*		35	50	ns
t_{TLH}	Transition Time, Low-To-High Level Output	C_L = 15 pF, R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*			10	20	ns
t_{THL}	Transition Time, High-To-Low Level Output	C_L = 15 pF, R_L = 50Ω, $I_C \approx$ 200 mA, Gates and Transistors Combined, *(Figure 14)*			10	20	ns
V_{OH}	High Level Output Voltage After Switching	V_S = 30V, $I_C \approx$ 300 mA, R_{BE} = 500Ω, *(Figure 15)*		V_S−10			mV
t_d	Delay Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, (Note 13), *(Figure 13)*			10		ns
t_r	Rise Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω. (Note 13), *(Figure 13)*			16		ns
t_s	Storage Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, (Note 13), *(Figure 13)*			23		ns
t_f	Fall Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, (Note 13), *(Figure 13)*			14		ns

dc electrical characteristics

DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464 (Notes 8 and 9)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	*(Figure 7)*			2			V
V_{IL}	Low Level Input Voltage	*(Figure 7)*					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.2	−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, *(Figure 7)*	DS55461, V_{IL} = 0.8V	I_{OL} = 100 mA		0.15	0.5	V
				I_{OL} = 300 mA		0.36	0.8	V
			DS55462, V_{IH} = 2V	I_{OL} = 100 mA		0.16	0.5	V
				I_{OL} = 300 mA		0.35	0.8	V
			DS55463, V_{IL} = 0.8V	I_{OL} = 100 mA		0.18	0.5	V
				I_{OL} = 300 mA		0.39	0.8	V
			DS55464, V_{IH} = 2V	I_{OL} = 100 mA		0.17	0.5	V
				I_{OL} = 300 mA		0.38	0.8	V
			DS75461, V_{IL} = 0.8V	I_{OL} = 100 mA		0.15	0.4	V
				I_{OL} = 300 mA		0.36	0.7	V
			DS75462, V_{IH} = 2V	I_{OL} = 100 mA		0.16	0.4	V
				I_{OL} = 300 mA		0.35	0.7	V
			DS75463, V_{IL} = 0.8V	I_{OL} = 100 mA		0.18	0.4	V
				I_{OL} = 300 mA		0.39	0.7	V
			DS75464, V_{IH} = 2V	I_{OL} = 100 mA		0.17	0.4	V
				I_{OL} = 300 mA		0.38	0.7	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{OH} = 35V, *(Figure 7)*	V_{IH} = 2V	DS55461, DS55463			300	μA
				DS75461, DS75463			100	μA
			V_{IL} = 0.8V	DS55462, DS55464			300	μA
				DS75462, DS75464			100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 9)*					1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 9)*					40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 8)*				−1	−1.6	mA
I_{CCH}	Supply Current	V_{CC} = Max, Outputs High, *(Figure 11)*	V_I = 5V	DS55461/ DS75461, DS55463/ DS75463		8	11	mA
			V_I = 0V	DS55462/ DS75462		13	17	mA
				DS55464/ DS75464		14	19	mA
I_{CCL}	Supply Current	V_{CC} = Max, Outputs Low, *(Figure 11)*	V_I = 0V	DS55461/ DS75461		61	76	mA
				DS55463/ DS75463		63	76	mA
			V_I = 5V	DS55462/ DS75462		65	76	mA
				DS55464/ DS75464		72	85	mA

ac switching characteristics

DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464 V_{CC} = 5V, T_A = 25°C

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-To-High Level Output	$I_O \approx 200$ mA, C_L = 15 pF, $R_L = 50\Omega$, *(Figure 14)*	DS55461/ DS75461, DS55463/ DS75463		45	55	ns
			DS55462/ DS75462, DS55464/ DS75464		50	65	ns
t_{PHL}	Propagation Delay Time, High-To-Low Level Output	$I_O \approx 200$ mA, C_L = 15 pF, $R_L = 50\Omega$, *(Figure 14)*	DS55461/ DS75461, DS55463/ DS75463		30	40	ns
			DS55462/ DS75462, DS55464/ DS75464		40	50	ns
t_{TLH}	Transition Time, Low-To-High Level Output	$I_O \approx 200$ mA, C_L = 15 pF, $R_L = 50\Omega$, *(Figure 14)*	DS55461/ DS75461		8	20	ns
			DS55462/ DS75462		12	25	ns
			DS55463/ DS75463		8	25	ns
			DS55464/ DS75464		12	20	ns
t_{THL}	Transition Time, High-To-Low Level Output	$I_O \approx 200$ mA, C_L = 15 pF, $R_L = 50\Omega$, *(Figure 14)*	DS55461/ DS75461		10	20	ns
			DS55462/ DS75462, DS55464/ DS75464		15	20	ns
			DS55463/ DS75463		10	25	ns
V_{OH}	High-Level Output Voltage After Switching	V_S = 30V, $I_O \approx 300$ mA, *(Figure 15)*		V_S–10			mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: This is the voltage between two emitters of a multiple-emitter transistor.

Note 4: This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.

Note 5: This value applies between 0 and 10 mA collector current when the base-emitter diode is open circuited.

Note 6: This is the maximum voltage which should be applied to any output when it is in the "OFF" state.

Note 7: Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

Note 8: Unless otherwise specified min/max limits apply across the –55°C to +125°C temperature range for the DS55460 series and across the 0°C to +70°C range for the DS75460 series. All typicals are given for V_{CC} = +5V and T_A = 25°C.

Note 9: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 10: Only one output at a time should be shorted.

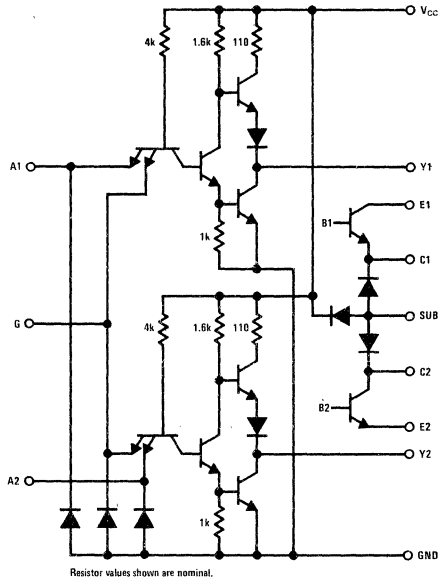
Note 11: For the DS55460/DS75460 only, the substrate (pin 8) must always be at the most negative device voltage for proper operation.

Note 12: These parameters must be measured using pulse techniques. t_W = 300μs, duty < 2%.

Note 13: Applies to output transistors only.

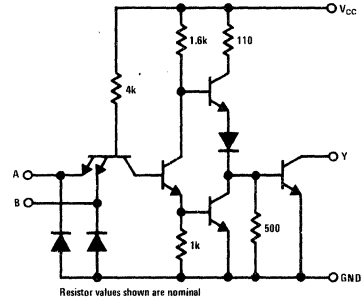
schematic diagrams

DS55460/DS75460



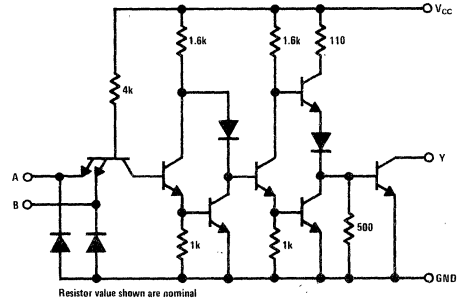
Resistor values shown are nominal.

DS55461/DS75461



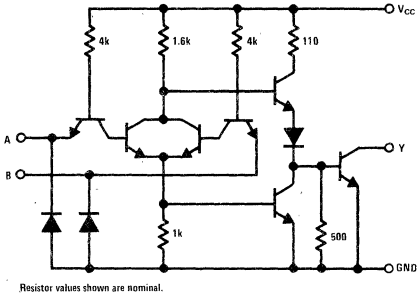
Resistor values shown are nominal

DS55462/DS75462



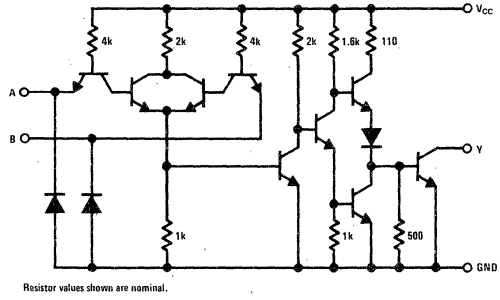
Resistor value shown are nominal

DS55463/DS75463



Resistor values shown are nominal.

DS55464/DS75464



Resistor values shown are nominal.

truth tables (H = high level, L = low level)

DS55461/DS75461

A	B	Y
L	L	L (ON State)
L	H	L (ON State)
H	L	L (ON State)
H	H	H (OFF State)

DS55462/DS75462

A	B	Y
L	L	H (OFF State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	L (ON State)

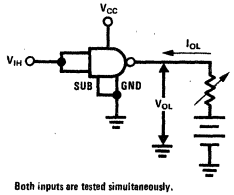
DS55463/DS75463

A	B	Y
L	L	L (ON State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	H (OFF State)

DS55464/DS75464

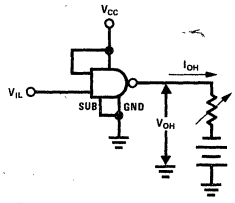
A	B	Y
L	L	H (OFF State)
L	H	L (ON State)
H	L	L (ON State)
H	H	L (ON State)

dc test circuits



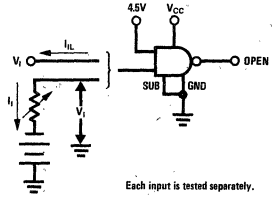
Both inputs are tested simultaneously.

FIGURE 1. V_{IH}, V_{OL}



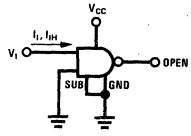
Each input is tested separately.

FIGURE 2. V_{IL}, V_{OH}



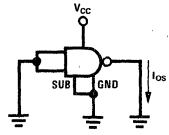
Each input is tested separately.

FIGURE 3. V_I, I_{IL}



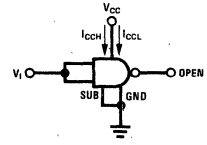
Each input is tested separately.

FIGURE 4. I_I, I_{IH}



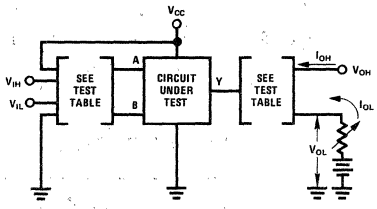
Each gate is tested separately.

FIGURE 5. I_{OS}



Both gates are tested simultaneously

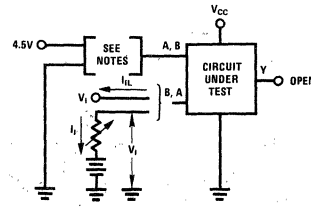
FIGURE 6. I_{CCH}, I_{CCL}



CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
DS55461	V_{IH} V_{IL}	V_{IH} V_{CC}	V_{OH} I_{OL}	I_{OH} V_{OL}
DS55462	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} V_{OH}	V_{OL} I_{OH}
DS55463	V_{IH} V_{IL}	Gnd V_{IL}	V_{OH} I_{OL}	I_{OH} V_{OL}
DS55464	V_{IH} V_{IL}	Gnd V_{IL}	I_{OL} V_{OH}	V_{OL} I_{OH}

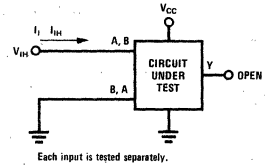
Each input is tested separately.

FIGURE 7. V_{IH}, V_{IL}, I_{OH}, V_{OL}



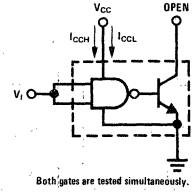
Note 1: Each input is tested separately.
Note 2: When testing DS55463/DS75463 and DS75464, input not under test is grounded.
For all other circuits it is at 4.5V.

FIGURE 8. V_I, I_{IL}



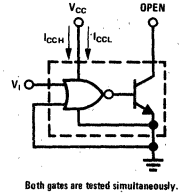
Each input is tested separately.

FIGURE 9. I_I, I_{IH}



Both gates are tested simultaneously.

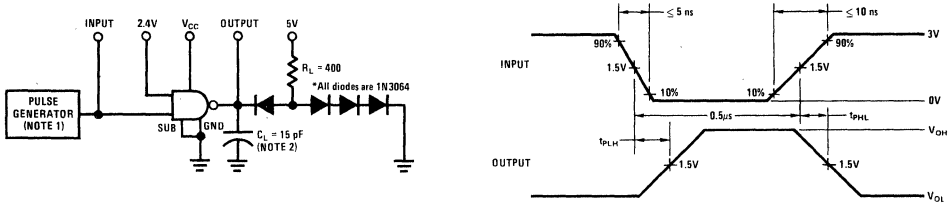
FIGURE 10. I_{CCH}, I_{CCL} for AND, NAND Circuits



Both gates are tested simultaneously.

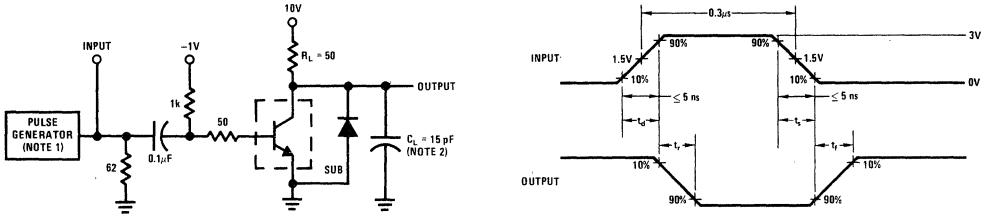
FIGURE 11. I_{CCH}, I_{CCL} for OR, NOR Circuits

switching characteristics



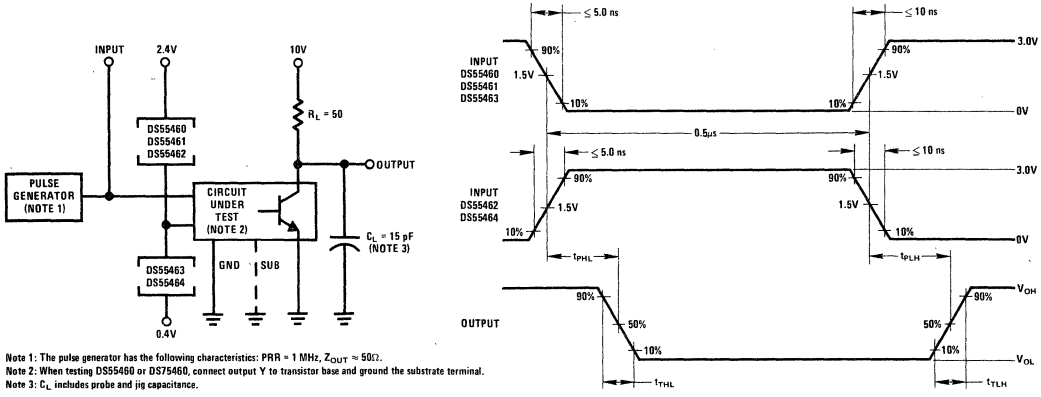
Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L include probe and jig capacitance.

FIGURE 12. Propagation Delay Times, Each Gate (DS55460 and DS75460 Only)



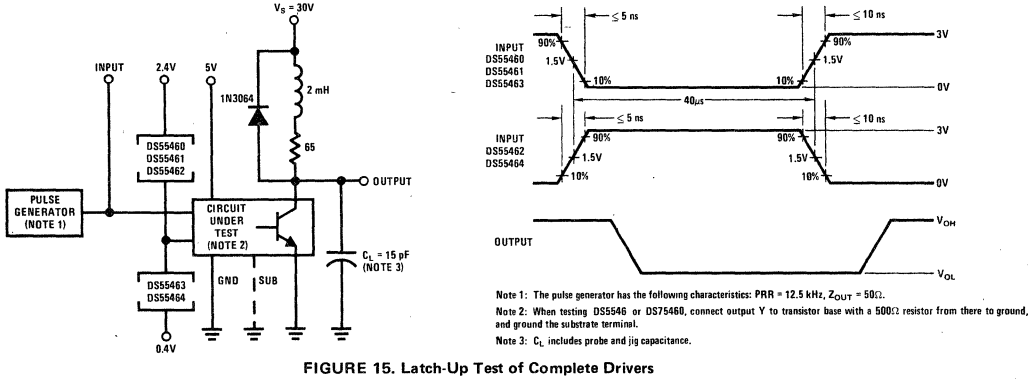
Note 1: The pulse generator has the following characteristics: duty cycle ≤ 1%, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

FIGURE 13. Switching Times, Each Transistor (DS55460 and DS75460 Only)



Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: When testing DS55460 or DS75460, connect output Y to transistor base and ground the substrate terminal.
Note 3: C_L includes probe and jig capacitance.

FIGURE 14. Switching Times of Complete Drivers



Note 1: The pulse generator has the following characteristics: PRR = 12.5 kHz, $Z_{OUT} = 50\Omega$.
Note 2: When testing DS5546 or DS75460, connect output Y to transistor base with a 500Ω resistor from there to ground, and ground the substrate terminal.
Note 3: C_L includes probe and jig capacitance.

FIGURE 15. Latch-Up Test of Complete Drivers

NATIONAL

Level Translators/Buffers
Advance Information*

DS1630/DS3630 hex CMOS compatible buffer

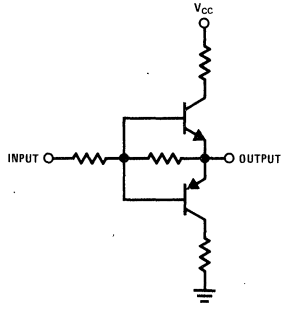
general description

The DS1630/DS3630 is a high current buffer intended for use with CMOS circuits interfacing with peripherals requiring high drive currents. The DS1630/DS3630 features low quiescent power consumption (typically 50μW) as well as high-speed driving of capacitive loads such as large MOS memories. The design of the DS1630/DS3630 is such that V_{CC} current spikes commonly found in standard CMOS circuits cannot occur, thereby, reducing the total transient and average power when operating at high frequencies.

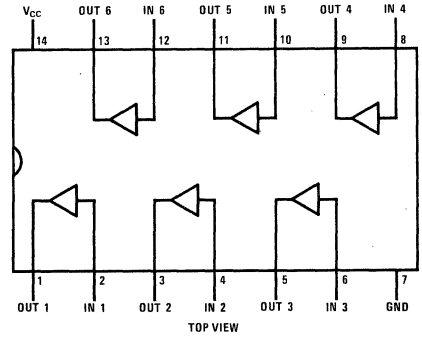
features

- High-speed capacitive driver
- Wide supply voltage range
- Input/output TTL compatibility
- Input/output CMOS compatibility
- No internal transient V_{CC} current spikes
- 50μW typical standby power
- Fan out of 10 standard TTL loads

equivalent schematic and connection diagrams

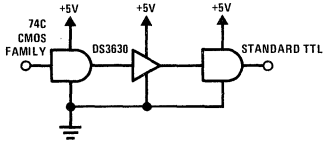


Dual-In-Line Package

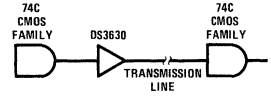


Order Number DS1630J, DS3630J or DS3630N

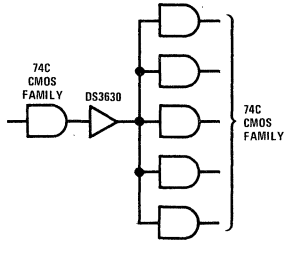
typical applications



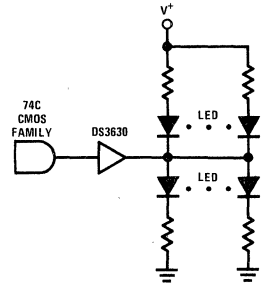
CMOS to TTL Interface



CMOS To Transmission Line Interface



CMOS To CMOS Interface



LED Driver

*Specifications may change.

absolute maximum ratings (Note 1)

Supply Voltage	16V
Input Voltage	16V
Output Voltage	16V
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	3	15	V
Temperature (T_A)			
DS1630	−55	+125	°C
DS3630	0	+70	°C

dc electrical characteristics (Notes 2 and 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{INH} Logical "1" Input Current	$V_{IN} = V_{CC}$, $I_{OUT} = -400\mu A$	DS1630		90	200	μA
		DS3630		90	200	μA
	$V_{IN} = V_{CC} - 2.0V$, $I_{OUT} = 16$ mA	DS1630		0.5	3.2	mA
		DS3630		0.5	1.5	mA
I_{INL} Logical "0" Input Current	$V_{IN} = 0.4V$, $I_{OUT} = 16$ mA	DS1630		−0.15	−1	mA
		DS3630		$V_{CC}-150$	−800	μA
V_{OH} Logical "1" Output Voltage	$V_{IN} = V_{CC}$, $I_{OUT} = -400\mu A$	DS1630	$V_{CC}-1$	$V_{CC}-0.75$		V
		DS3630	$V_{CC}-0.9$	$V_{CC}-0.75$		V
	$V_{IN} = V_{CC} - 0.4V$, $I_{OUT} = 16$ mA	DS1630	$V_{CC}-2.5$	$V_{CC}-2.0$		V
		DS3630	$V_{CC}-2.5$	$V_{CC}-2.0$		V
V_{OL} Logical "0" Output Voltage	$V_{IN} = 0V$, $I_{OUT} = 400\mu A$	DS1630		0.75	1	V
		DS3630		0.75	0.9	V
	$V_{IN} = 0V$, $I_{OUT} = 16$ mA	DS1630		0.95	1.3	V
		DS3630		0.95	1.3	V
	$V_{IN} = 0.4V$, $I_{OUT} = 16$ mA	DS1630		1.2	1.6	V
		DS3630		1.2	1.5	V

ac electrical characteristics $V_{CC} = 5.0V$, $T_A = 25°C$ unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0} Propagation Delay to a Logical "0"	$C_L = 50$ pF		30	45	ns
	$C_L = 250$ pF		40	60	ns
	$C_L = 500$ pF		50	75	ns
t_{pd1} Propagation Delay to a Logical "1"	$C_L = 50$ pF		15	25	ns
	$C_L = 250$ pF		35	50	ns
	$C_L = 500$ pF		50	75	ns

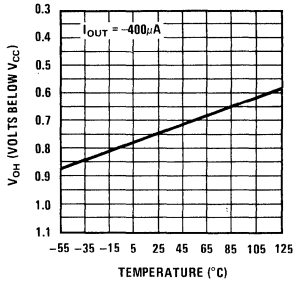
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1630 and across the 0°C to +70°C range for the DS3630. All typicals are given for $V_{CC} = 5.0V$ and $T_A = 25°C$.

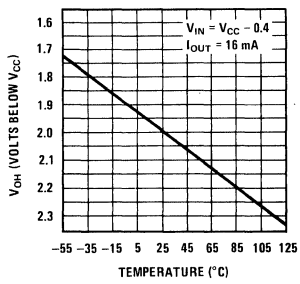
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

typical performance characteristics

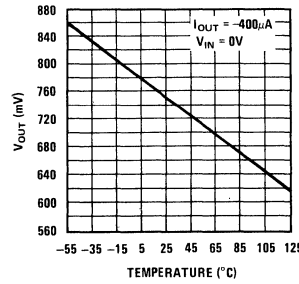
V_{OH} vs Temperature, $V_{IN} = V_{CC}$



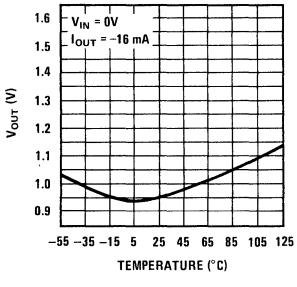
V_{OH} Active vs Temperature



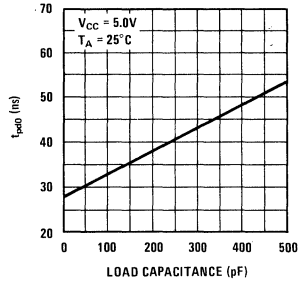
V_{OL} vs Temperature



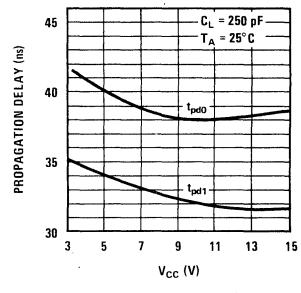
V_{OL} vs Temperature



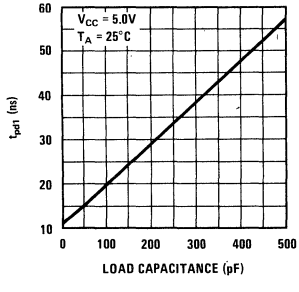
t_{pdo} vs Load Capacitance



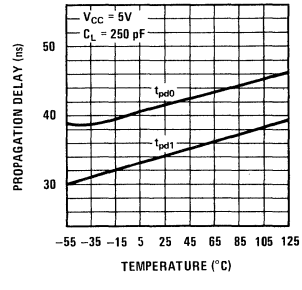
Propagation Delay vs V_{CC}



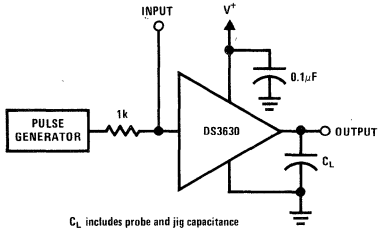
t_{pd1} vs Load Capacitance



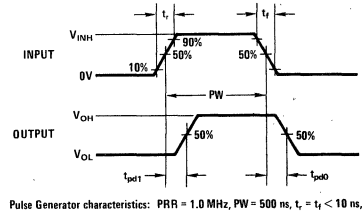
Propagation Delay vs Temperature



ac test circuit and switching time waveforms



C_L includes probe and jig capacitance



Pulse Generator characteristics: PRR = 1.0 MHz, PW = 500 ns, $t_r = t_f < 10$ ns, V_{IN} = 0 to V_{CC}

NATIONAL

Level Translators/Buffers

DS7800/DS8800 dual voltage translator

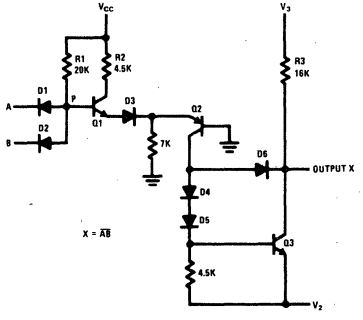
general description

The DS7800/DS8800 are dual voltage translators designed for interfacing between conventional TTL or DTL voltage levels and those levels associated with high impedance junction or MOS FET-type devices. The design allows the user a wide latitude in his selection of power supply voltages, thus providing custom control of the output swing. The translator is especially useful in analog switching; and since low power dissipation occurs in the "off" state, minimum system power is required.

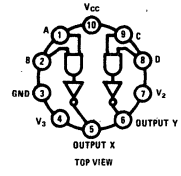
features

- 31 volt (max) output swing
- 1 mW power dissipation in normal state
- Standard 5V power supply
- Temperature range:
  DS7800 −55°C to +125°C
  DS8800 0°C to +70°C
- Compatible with all MOS devices

schematic and connection diagrams



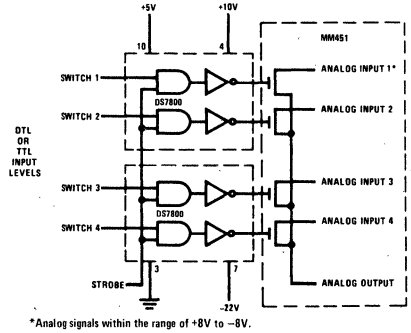
Metal Can Package



Order Number DS7800H or DS8800H

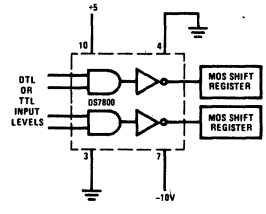
typical applications

4-Channel Analog Switch



*Analog signals within the range of +8V to −8V.

Bipolar to MOS Interfacing



absolute maximum ratings (Note 1)

V_{CC} Supply Voltage	7.0V
V2 Supply Voltage	−30V
V3 Supply Voltage	30V
V3-V2 Voltage Differential	40V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7800	4.5	5.5	V
DS8800	4.75	5.25	V
Temperature (T_A)			
DS7800	−55	+125	°C
DS8800	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP (NOTE 6)	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			5	μA
			V_{IN} = 5.5V			1	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−0.2	−0.4	mA
I_{OH}	Output Leakage Current	V_{CC} = Max, V_{IN} = 0.8V (Notes 4 and 7)				10	μA
R_O	Output Collector Resistor	T_A = 25°C		11.5	16.0	20.0	kΩ
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 2.0V (Note 7)				V_2 + 2.0	V
$I_{CC(MAX)}$	Power Supply Current Output "ON"	V_{CC} = Max, V_{IN} = 4.5V (Note 5)			0.85	1.6	mA
$I_{CC(MIN)}$	Power Supply Current Output "OFF"	V_{CC} = Max, V_{IN} = 0V (Note 5)			0.22	0.41	mA

switching characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Transition Time to Logical "0" Output	T_A = 25°C, C = 15 pF (Note 8)	25	70	125	ns
t_{pd1}	Transition Time to Logical "1" Output	T_A = 25°C, C = 15 pF (Note 9)	25	62	125	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7800 and across the 0°C to +70°C range for the DS8800.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Current measured is drawn from V_3 supply.

Note 5: Current measured is drawn from V_{CC} supply.

Note 6: All typical values are measured at T_A = 25°C with V_{CC} = 5.0V, V_2 = −22V, V_3 = +8V.

Note 7: Specification applies for all allowable values of V_2 and V_3.

Note 8: Measured from 1.5V on input to 50% level on output.

Note 9: Measured from 1.5V on input to logic "0" voltage, plus 1V.

theory of operation

The two input diodes perform the AND function on TTL or DTL input voltage levels. When at least one input voltage is a logical "0", current from V_{CC} (nominally 5.0V) passes through R_1 and out the input(s) which is at the low voltage. Other than small leakage currents, this current drawn from V_{CC} through the 20 kΩ resistor is the only source of power dissipation in the logical "1" output state.

When both inputs are at logical "1" levels, current passes through R_1 and diverts to transistor Q_1, turning it on and thus pulling current through R_2. Current is then supplied to the PNP transistor, Q_2. The voltage losses caused by current through Q_1, D_3, and Q_2 necessitate that node P reach a voltage sufficient to overcome these losses before current begins to flow. To achieve this voltage at node P, the inputs must be raised to a voltage level which is one diode potential lower than node P. Since these levels are exactly the same as those experienced with conventional TTL and DTL, the interfacing with these types of circuits is achieved.

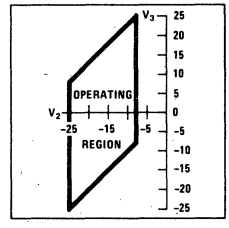
Transistor Q_2 provides "constant current switching" to the output due to the common base connection of Q_2. When at least one input is at the logical "0" level, no current is delivered to Q_2, so that its collector supplies essentially zero current to the output stage. But when both inputs are raised to a logical "1" level current is supplied to Q_2. Since this current is relatively constant, the collector of Q_2 acts as a constant current source for the output stage. Logic inversion is performed since logical "1" input voltages cause current to be supplied to Q_2 and to Q_3. And when Q_3 turns on the output voltage drops to the logical "0" level.

The reason for the PNP current source, Q_2, is so that the output stage can be driven from a high impedance. This allows voltage V_2 to be adjusted in accordance with the application. Negative voltages to −25V can be applied to V_2. Since the output will neither source nor sink large amounts of current, the output voltage range is almost exclusively dependent upon the values selected for V_2 and V_3.

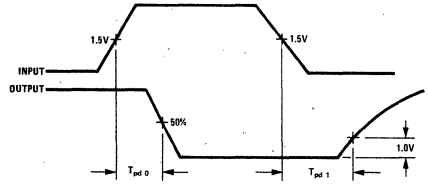
Maximum leakage current through the output transistor Q_3 is specified at 10 μA under worst-case voltage between V_2 and V_3. This will result in a logical "1" output voltage which is 0.2V below V_3. Likewise the clamping action of diodes D_4, D_5, and D_6, prevents the logical "0" output voltage from falling lower than 2V above V_2, thus establishing the output voltage swing at typically 2 volts less than the voltage separation between V_2 and V_3.

selecting power supply voltage

The graph shows the boundary conditions which must be used for proper operation of the unit. The range of operation for power supply V_2 is shown on the X axis. It must be between −25V and −8V. The allowable range for power supply V_3 is governed by supply V_2. With a value chosen for V_2, V_3 may be selected as any value along a vertical line passing through the V_2 value and terminated by the boundaries of the operating region. A voltage difference between power supplies of at least 5V should be maintained for adequate signal swing.



switching time waveforms



Level Translators/Buffers

NATIONAL

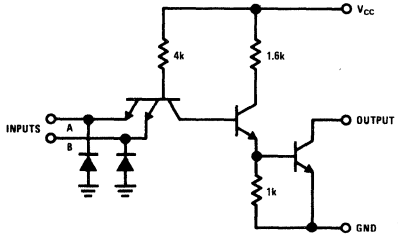
DS7810/DS8810 quad 2-input TTL-MOS interface gate
DS7811/DS8811 quad 2-input TTL-MOS interface gate
DS7812/DS8812 TTL-MOS hex inverter

general description

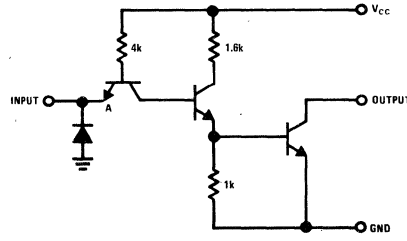
These Series 54/74 compatible gates are high output voltage versions of the DM5401/DM7401 (SN5401/SN7401), DM5403/DM7403 (SN5403/SN7403), and DM5405/DM7405 (SN5405/SN7405). Their open-collector outputs may be "pulled-up" to +14 volts in the logical "1" state thus providing guaranteed interface between TTL and MOS logic levels.

In addition the devices may be used in applications where it is desirable to drive low current relays or lamps that require up to 14 volts.

schematic and connection diagrams

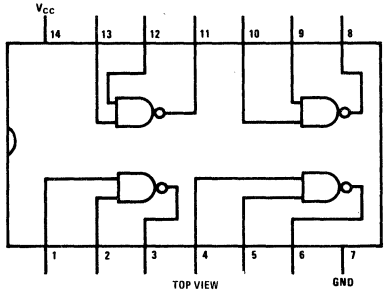


DS7810/DS8810, DS7811/DS8811



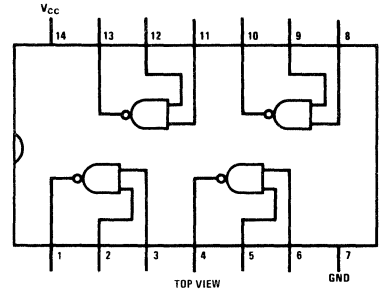
DS7812/DS8812

Dual-In-Line Package



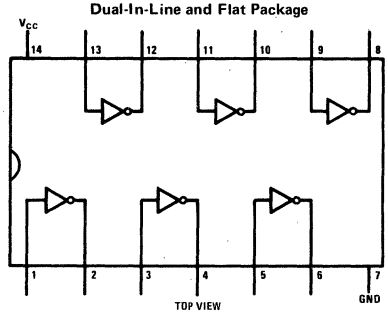
DS7810/DS8810

Dual-In-Line and Flat Package



DS7811/DS8811

Dual-In-Line and Flat Package



DS7812/DS8812

Order Number

DS7810J	DS8810N
DS7811J	DS8811N
DS7812J	DS8812N
DS8810J	DS7810W
DS8811J	DS7811W
DS8812J	DS7812W

2

absolute maximum ratings (Note 1)

V_{CC}	7V
Input Voltage	5.5V
Output Voltage	14V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS78XX	4.5	5.5	V
DS88XX	4.75	5.25	V
Temperature (T_A)			
DS78XX	−55	+125	°C
DS88XX	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{CLAMP}	Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA				−1.5	V
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{OH}	Logical "1" Output Current	V_{CC} = Min,	V_{IN} = 0.8V			250	μA
		V_{OUT} = 10V	V_{IN} = 0.0V			40	μA
I_{OL}	Logical "0" Output Current	V_{CC} = Min, V_{IN} = 2.0V, V_{OUT} = 0.4V		16			mA
V_{OH}	Logical "1" Output Breakdown Voltage	V_{CC} = Min, V_{IN} = 0V, I_{OUT} = 1 mA		14			V
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 2.0V, I_{OUT} = 16 mA				0.4	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			40	μA
			V_{IN} = 5.5V			1	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.6	mA
$I_{CC(MAX)}$	Logical "0" Supply Current (Each Gate)	V_{CC} = Max, V_{IN} = 5.0V			3.0	5.1	mA
$I_{CC(MIN)}$	Logical "1" Supply Current (Each Gate)	V_{CC} = Max, V_{IN} = 0V			1.0	1.8	mA

switching characteristics

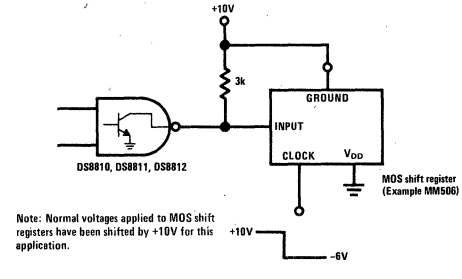
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay Time to a Logical "0"	V_{CC} = 5.0V, T_A = 25°C, C_{OUT} = 15 pF, R_L = 1k	4	12	18	ns
t_{pd1}	Propagation Delay Time to a Logical "1"	V_{CC} = 5.0V, T_A = 25°C, C_{OUT} = 15 pF, R_L = 1k	18	29	45	ns

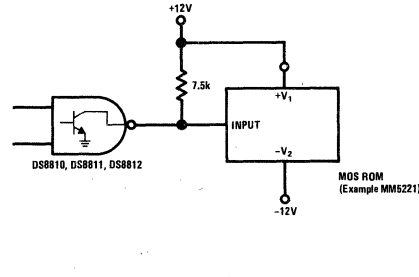
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7810, DS7811 and DS7812 and across the 0°C to +70°C range for the DS7810, DS7811 and DS7812.

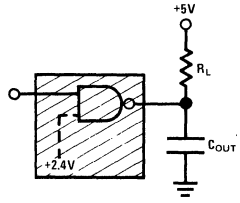
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

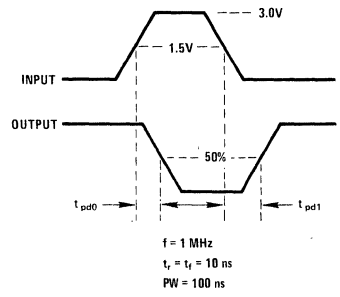
typical applications





ac test circuit and switching time waveforms





f = 1 MHz
$t_r = t_f = 10$ ns
PW = 100 ns

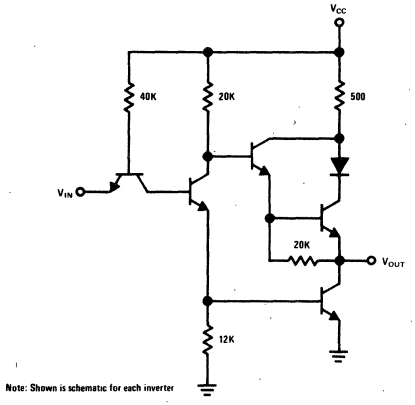
Level Translators/Buffers

DS78L12/DS88L12 TTL-MOS hex inverter/interface gate

general description

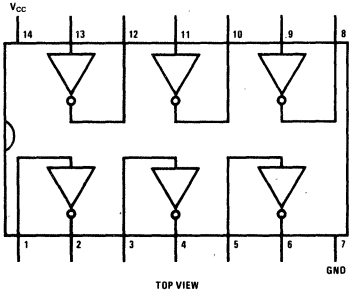
The DS78L12/DS88L12 is a low power TTL to MOS hex inverter element. The outputs may be "pulled up" to +14V in the logical "1" state, thus providing guaranteed interface between TTL and MOS logic levels. The gate may also be operated with V_{CC} levels up to +14V without resistive pull-ups at the outputs and still providing a guaranteed logical "1" level of V_{CC} − 2.2V with an output current of −200μA.

schematic and connection diagrams



Note: Shown is schematic for each inverter

Dual-In-Line and Flat Package

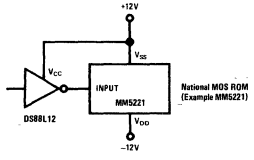


TOP VIEW

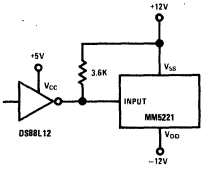
Order Number DS78L12J, DS88L12J
Order Number DS88L12N
Order Number DS78L12W

typical applications

TTL Interface to MOS ROM
Without Resistive Pull-Up



TTL Interface to MOS ROM
With Resistive Pull-Up



ac test circuits

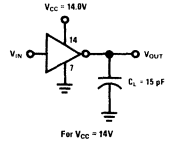


Figure 1

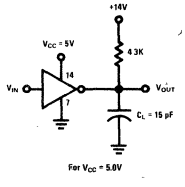
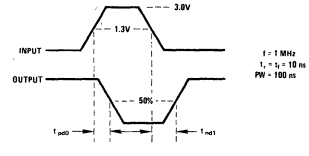


Figure 2

switching time waveforms



absolute maximum ratings (Note 1)

Supply Voltage	15V
Input Voltage	5.5V
Output Voltage	15V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS78L12	4.5	5.5	V
DS88L12	4.75	5.25	V
Temperature (T_A)			
DS78L12	−55	125	°C
DS88L12	0	70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = 14.0V		2.0	1.3		V
		V_{CC} = Min		2.0	1.3		V
V_{IL}	Logical "0" Input Voltage	V_{CC} = 14.0V			1.3	0.7	V
		V_{CC} = Min			1.3	0.7	V
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.7V	V_{CC} = 14.0V, I_{OUT} = −200μA	11.8	12.0		V
			V_{CC} = Min, I_{OUT} = 200μA	14.5	15.0		V
		V_{IN} = 0V, V_{CC} = Min, I_{OUT} = −5.0μA (Note 6)					V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 2.0V	V_{CC} = 14.0V, I_{OUT} = 12 mA		0.5	1.0	V
			V_{CC} = Min, I_{OUT} = 3.6 mA		0.2	0.4	V
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V	V_{CC} = 14.0V		<1	20	μA
			V_{CC} = Max		<1	10	μA
		V_{IN} = 5.5V	V_{CC} = 14.0V		<1	100	μA
			V_{CC} = Max		<1	100	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V	V_{CC} = 14.0V		−320	−500	μA
			V_{CC} = Max		−100	−180	μA
I_{SC}	Output Short Circuit Current	V_{OUT} = 0V (Note 4)	V_{CC} = 14.0V	−10	−25	−50	mA
			V_{CC} = Max	−3	−8	−15	mA
I_{CCH}	Supply Current — Logical "1" (Each Inverter)	V_{IN} = 0V	V_{CC} = 14.0V		0.32	0.50	mA
			V_{CC} = Max		0.11	0.16	mA
I_{CCL}	Supply Current — Logical "0" (Each Inverter)	V_{IN} = 5.25V	V_{CC} = 14.0V		1.0	1.5	mA
			V_{CC} = Max		0.3	0.5	mA

switching characteristics

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0" from Input to Output	T_A = 25°C	V_{CC} = 5.0V *(Figure 2)*		27	45	ns
			V_{CC} = 14.0V *(Figure 1)*		11	20	ns
t_{pd1}	Propagation Delay to a Logical "1" from Input to Output	T_A = 25°C	V_{CC} = 5.0V *(Figure 2)*, (Note 5)		79	100	ns
			V_{CC} = 14.0V *(Figure 1)*		34	55	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78L12 and across the 0°C to +70°C range for the DS88L12.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: t_{pd1} for V_{CC} = 5.0V is dependent upon the resistance and capacitance used.

Note 6: $V_{OL} = V_{CC} - 1.1V$ for the DS88L12 and $V_{CC} - 1.4V$ for the DS78L12.

NATIONAL

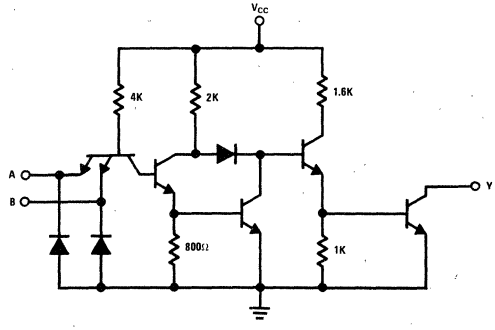
Level Translators/Buffers

DS7819/DS8819 quad 2-input TTL-MOS AND gate

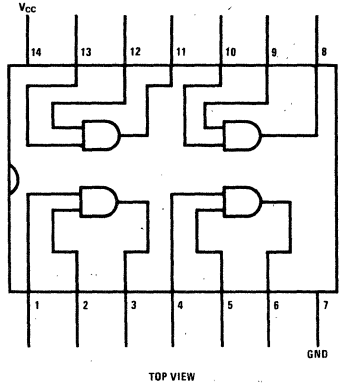
general description

The DS7819/DS8819 is the high output voltage version of the SN5409. Its open-collector outputs may be "pulled-up" to 14V in the logical "1" state thus providing guaranteed interface between TTL and MOS logic levels.

schematic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

Order Number DS7819J or DS8819J
Order Number DS8819N
Order Number DS7819W

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7819	4.5	5.5	V
DS8819	4.75	5.25	V
Temperature (T_A)			
DS7819	−55	+125	°C
DS8819	0	70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{OH}	Logical "1" Output Current	V_{CC} = Min	V_{IN} = 2.0V, V_{OUT} = 10V			40.0	μA
			V_{IN} = 4.5V, V_{OUT} = 14V			1.0	mA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 0.8V, I_{OUT} = 16 mA				0.4	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			40.0	μA
			V_{IN} = 5.5V			1.0	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.6	mA
I_{CCH}	Logical "1" Supply Current	V_{CC} = Max, V_{IN} = 5V			11.0	21.0	mA
I_{CCL}	Logical "0" Supply Current	V_{CC} = Max, V_{IN} = 0V			20.0	33.0	mA
V_{CL}	Input Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA				−1.5	V

switching characteristics

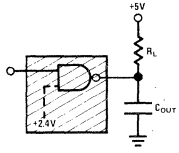
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0"	V_{CC} = 5.0V, T_A = 25°C		16.0	24.0	ns
t_{pd1}	Propagation Delay to a Logical "1"	V_{CC} = 5.0V, T_A = 25°C		16.0	32.0	ns

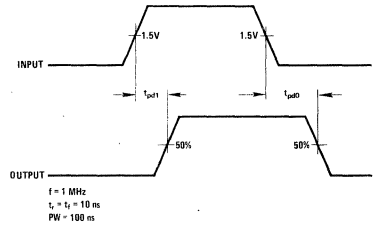
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7819 and across the 0°C to +70°C range for the DS8819.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

ac test circuit and switching time waveforms





Line Drivers/Receivers

DS1488 quad line driver

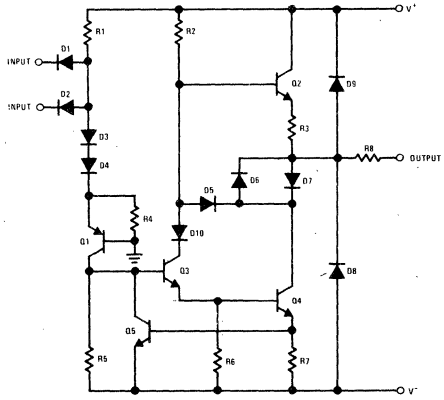
general description

The DS1488 is a quad line driver which converts standard DTL/TTL input logic levels through one stage of inversion to output levels which meet EIA Standard No. RS-232C and CCITT Recommendation V. 24.

features

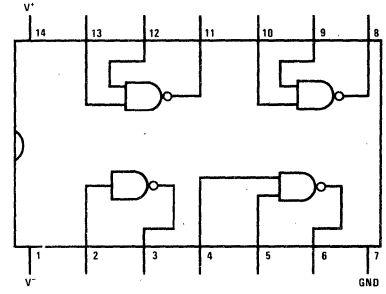
- Current limited output ±10 mA typ
- Power-off source impedance 300Ω min
- Simple slew rate control with external capacitor
- Flexible operating supply range
- Inputs are DTL/TTL compatible

schematic and connection diagrams



1/4 Circuit

Dual-In-Line Package

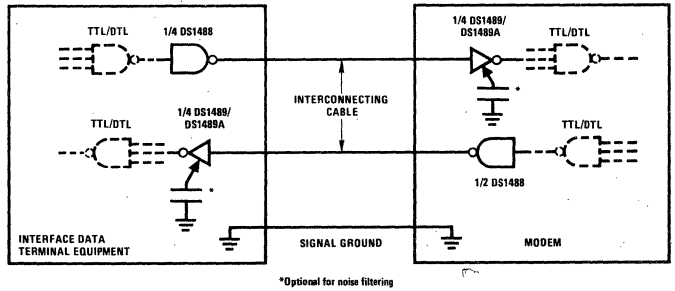


TOP VIEW

Order Number DS1488J

typical applications

RS232C Data Transmission



*Optional for noise filtering

absolute maximum ratings (Note 1)

Supply Voltage	
V^+	+15V
V^-	−15V
Input Voltage (V_{IN})	$-15V \leq V_{IN} \leq 7.0V$
Output Voltage	±15V
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Notes 2, 3 and 4)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	Logical "0" Input Current	V_{IN} = 0V			−1.0	−1.3	mA
I_{IH}	Logical "1" Input Current	V_{IN} = +5.0V			0.005	10.0	μA
V_{OH}	High Level Output Voltage	R_L = 3.0 kΩ,	V^+ = 9.0V, V^- = −9.0V	6.0	7.0		V
		V_{IN} = 0.8V	V^+ = 13.2V, V^- = −13.2V	9.0	10.5		V
V_{OL}	Low Level Output Voltage	R_L = 3.0 kΩ,	V^+ = 9.0V, V^- = −9.0V	−6.0	−6.8		V
		V_{IN} = 1.9V	V^+ = 13.2V, V^- = −13.2V	−9.0	−10.5		V
I_{OS}^+	High Level Output Short-Circuit Current	V_{OUT} = 0V, V_{IN} = 0.8V		−6.0	−10.0	−12.0	mA
I_{OS}^-	Low Level Output Short-Circuit Current	V_{OUT} = 0V, V_{IN} = 1.9V		6.0	10.0	12.0	mA
R_{OUT}	Output Resistance	$V^+ = V^-$ = 0V, V_{OUT} = ±2V		300			Ω
I_{CC}^+	Positive Supply Current (Output Open)	V_{IN} = 1.9V	V^+ = 9.0V, V^- = −9.0V		15.0	20.0	mA
			V^+ = 12V, V^- = −12V		19.0	25.0	mA
			V^+ = 15V, V^- = −15V		25.0	34.0	mA
		V_{IN} = 0.8V	V^+ = 9.0V, V^- = −9.0V		4.5	6.0	mA
			V^+ = 12V, V^- = −12V		5.5	7.0	mA
			V^+ = 15V, V^- = −15V		8.0	12.0	mA
I_{CC}^-	Negative Supply Current (Output Open)	V_{IN} = 1.9V	V^+ = 9.0V, V^- = −9.0V		−13.0	−17.0	mA
			V^+ = 12V, V^- = −12V		−18.0	−23.0	mA
			V^+ = 15V, V^- = −15V		−25.0	−34.0	mA
		V_{IN} = 0.8V	V^+ = 9.0V, V^- = −9.0V		−0.001	−1.0	mA
			V^+ = 12V, V^- = −12V		−0.001	−1.0	mA
			V^+ = 15V, V^- = −15V		−0.01	−2.5	mA
P_d	Power Dissipation	V^+ = 9.0V, V^- = −9.0V			252	333	mW
		V^+ = 12V, V^- = −12V			444	576	mW

switching characteristics

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Propagation Delay to a Logical "1"	R_L = 3.0 kΩ, C_L = 15 pF, T_A = 25°C		230	350	ns
t_{pd0}	Propagation Delay to a Logical "0"	R_L = 3.0 kΩ, C_L = 15 pF, T_A = 25°C		70	175	ns
t_r	Rise Time	R_L = 3.0 kΩ, C_L = 15 pF, T_A = 25°C		75	100	ns
t_f	Fall Time	R_L = 3.0 kΩ, C_L = 15 pF, T_A = 25°C		40	75	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +75°C temperature range for the DS1488.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

applications

By connecting a capacitor to each driver output the slew rate can be controlled utilizing the output current limiting characteristics of the DS1488. For a set slew rate the appropriate capacitor value may be calculated using the following relationship

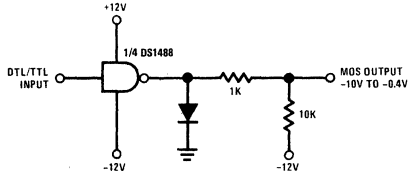
$$C = I_{SC} (\Delta T/\Delta V)$$

where C is the required capacitor, I_{SC} is the short circuit current value, and $\Delta V/\Delta T$ is the slew rate.

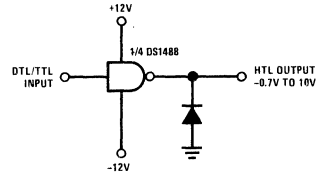
RS232C specifies that the output slew rate must not exceed 30V per microsecond. Using the worst case output short circuit current of 12 mA in the above equation, calculations result in a required capacitor of 400 pF connected to each output.

typical applications (con't)

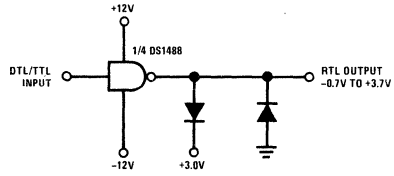
DTL/TTL-to-MOS Translator



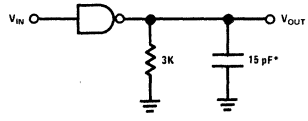
DTL/TTL-to-HTL Translator



DTL/TTL-to-RTL Translator

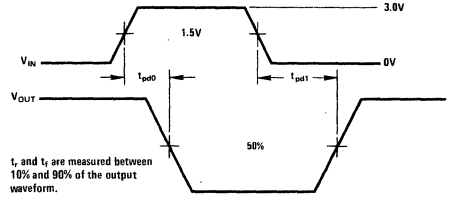


ac load circuit



*C_L includes probe and jig capacitance.

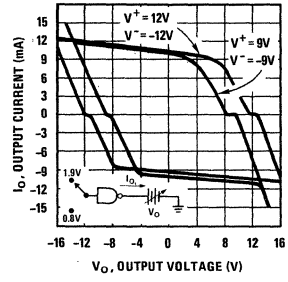
switching time waveforms



t_r and t_f are measured between 10% and 90% of the output waveform.

typical performance characteristics

Output Voltage and Current-Limiting Characteristics



Line Drivers/Receivers

DS1489/DS1489A quad line receiver

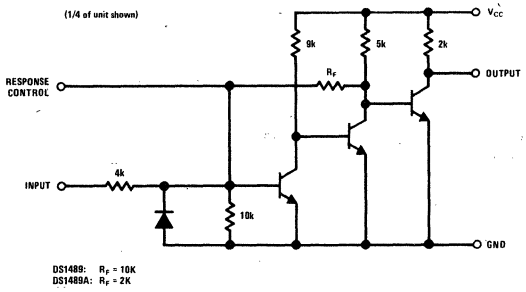
general description

The DS1489/DS1489A are quad line receivers designed to interface data terminal equipment with data communications equipment. They are constructed on a single monolithic silicon chip. These devices satisfy the specifications of EIA standard No. RS232C. The DS1489/DS1489A meet and exceed the specifications of MC1489/MC1489A and are pin-for-pin replacements. The DS1489/DS1489A are available in 14-lead ceramic dual-in-line package.

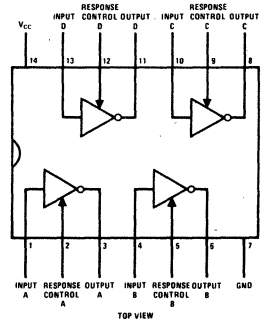
features

- Four totally separate receivers per package
- Programmable threshold
- Built-in input threshold hysteresis
- "Fail safe" operating mode
- Inputs withstand ±30V

schematic and connection diagrams

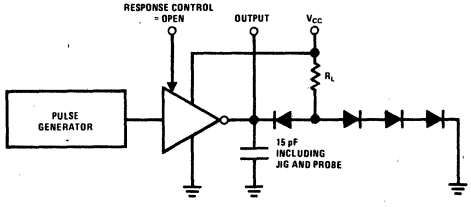


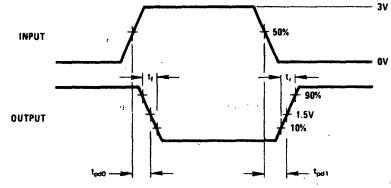
Dual-In-Line Package



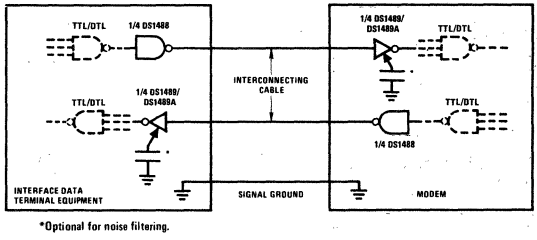
Order Number DS1489J or DS1489AJ

ac test circuit and voltage waveforms



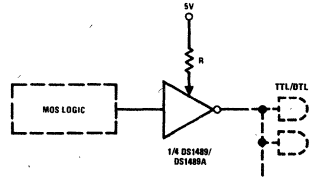


typical applications



*Optional for noise filtering.

RS232C Data Transmission



MOS to TTL/DTL Translator

absolute maximum ratings (Note 1)

The following apply for $T_A = 25^\circ C$ unless otherwise specified.

Power Supply Voltage	10V
Input Voltage Range	±30V
Output Load Current	20 mA
Power Dissipation (Note 2)	1W
Operating Temperature Range	$0^\circ C$ to $+75^\circ C$
Storage Temperature Range	$-65^\circ C$ to $+150^\circ C$

electrical characteristics (Notes 2, 3 and 4)

DS1489/DS1489A: The following apply for $V_{CC} = 5.0V \pm 1\%$, $0^\circ C \leq T_A \leq +75^\circ C$ unless otherwise specified.

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	Input High Threshold Voltage	$T_A = 25^\circ C$, $V_{OUT} \leq 0.45V$, $I_{OUT} = 10$ mA	DS1489	1.0		1.5	V
			DS1489A	1.75		2.25	V
V_{TL}	Input Low Threshold Voltage	$T_A = 25^\circ C$, $V_{OUT} \geq 2.5V$, $I_{OUT} = -0.5$ mA		0.75		1.25	V
I_{IN}	Input Current	$V_{IN} = +25V$		+3.6	+5.6	+8.3	mA
		$V_{IN} = -25V$		−3.6	−5.6	−8.3	mA
		$V_{IN} = +3V$		+0.43	+0.53		mA
		$V_{IN} = -3V$		−0.43	−0.53		mA
V_{OH}	Output High Voltage	$I_{OUT} = -0.5$ mA	$V_{IN} = 0.75V$	2.6	3.8	5.0	V
			Input = Open	2.6	3.8	5.0	V
V_{OL}	Output Low Voltage	$V_{IN} = 3.0V$, $I_{OUT} = 10$ mA			0.33	0.45	V
I_{SC}	Output Short Circuit Current	$V_{IN} = 0.75V$			3.0		mA
I_{CC}	Supply Current	$V_{IN} = 5.0V$			14	26	mA
P_d	Power Dissipation	$V_{IN} = 5.0V$			70	130	mW

switching characteristics

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Input to Output "High" Propagation Delay	$R_L = 3.9k$, *(Figure 1)* (ac Test Circuit)		28	85	ns
t_{pd0}	Input to Output "Low" Propagation Delay	$R_L = 390\Omega$, *(Figure 1)* (ac Test Circuit)		20	50	ns
t_r	Output Rise Time	$R_L = 3.9k$, *(Figure 1)* (ac Test Circuit)		110	175	ns
t_f	Output Fall Time	$R_L = 390\Omega$, *(Figure 1)* (ac Test Circuit)		9	20	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2. Unless otherwise specified min/max limits apply across the $0^\circ C$ to $+75^\circ C$ temperature range for the DS1489 and DS1489A.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: These specifications apply for response control pin = open.

NATIONAL

Line Drivers/Receivers
Advance Information*

DS1688/DS3688 quad TRI-STATE® differential line driver

general description

The DS1688/DS3688 are high-performance quad differantial line drivers, optimized for digital data transmission over balanced lines. The outputs are compatible with EIA Standards RS-422. The circuit uses Schottky-clamped transistor logic for minimum propagation delay and the inputs are fully compatible with 54LS/74LS series low power logic.

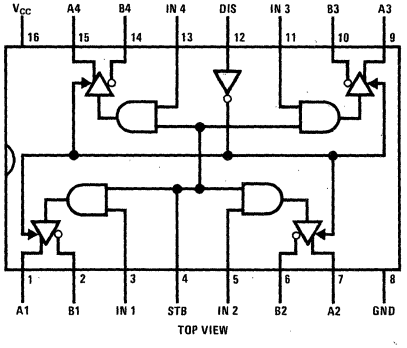
The DS1688/DS3688 provide a strobe and TRI-STATE control common to all four drivers. The DS1688 is specified over −55°C to +125°C and the DS3688 is specified over 0°C to +70°C temperature range.

features

- Compatible with RS-422
- Single 5V ±10% supply
- Series 54LS/74LS compatible
- Dual version of DS8830

connection diagram and truth table

Dual-In-Line Package

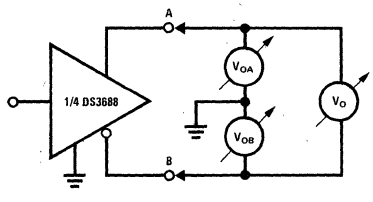


Order Number DS1688J, DS3688J or DS3688N

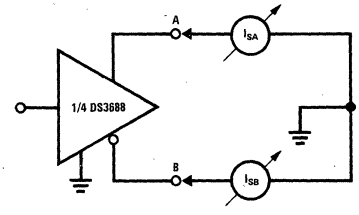
STROBE	DISABLE	INPUT	OUTPUTS	
			A	B
1	0	0	0	1
1	0	1	1	0
0	0	X	0	1
X	1	X	Hi-Z	Hi-Z

X = Don't Care

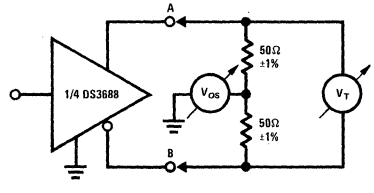
test circuits



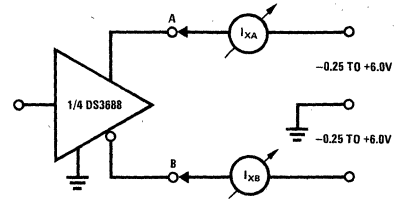
Open Circuit Measurement



Short Circuit Measurement



Test Termination Measurement



Power "OFF" Measurement

*Specifications may change

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	20V
Output Sink Current	100 mA
Power Dissipation	600 mW
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1688	−55	+125	°C
DS3688	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.5V	2			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.5V			0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 20V			100	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0V			−0.36	mA
V_{CLAMP}	Input Clamp Voltage	I_{IN} = −12 mA			1.5	V
V_{OA}, V_{OB}	Logical "1" Output Voltage	V_{CC} = 5.5V, Output Open Circuit			5.5	V
$\overline{V}_{OA}$, $\overline{V}_{OB}$	Logical "0" Output Voltage	V_{CC} = 4.5V, 450Ω to V_{CC}			1	V
V_O	Open Circuit Differential Voltage	V_{CC} = 5.5V			5.5	V
V_T	Output Terminated Differential Voltage	V_{CC} = 4.5V, Terminated 100Ω	2			V
ΔV_T	Difference in Differential Voltage	V_{CC} = 5.5V			0.4	V
V_{OS}	Driver Offset Voltage	Terminated 100Ω			3	V
ΔV_{OS}	Difference in Offset Voltage	V_{CC} = 5.5V, 100Ω			0.4	V
I_{SA}, I_{SB}	Output Short Circuit Current	V_{CC} = 5.5V, (Note 4)			−150	mA
I_{XA}, I_{XB}	Output Power "OFF" Current	V_{CC} = 0V, V_{OUT} = −0.25V			−100	μA
		V_{CC} = 0V, V_{OUT} = 6V			100	μA
I_{CC}	Supply Current	V_{CC} = 5.5V		13		mA
t_{pd1}, t_{pd0}	Propagation Delay Differential	Terminated 100Ω, 25°C		20		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

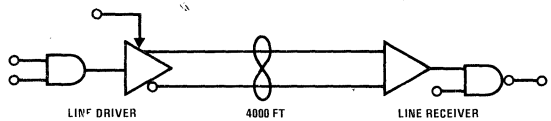
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1688 and across the 0°C to +70°C range for the DS3688. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Refer to EIA-RS-422 for exact conditions.

typical application



Multiple drivers and receivers may be bussed on common transmission line.

NATIONAL

Line Drivers/Receivers

Advance Information*

DS1689/DS3689, DS1690/DS3690 quad differential line receivers

general description

The DS1689/DS3689 and DS1690/DS3690 are high-performance quad differential line receivers, optimized for digital data transmission over balanced and unbalanced lines. The inputs are compatible with EIA and Federal standards, and the Schottky-clamped outputs are fully compatible with 54LS/74LS series low power logic.

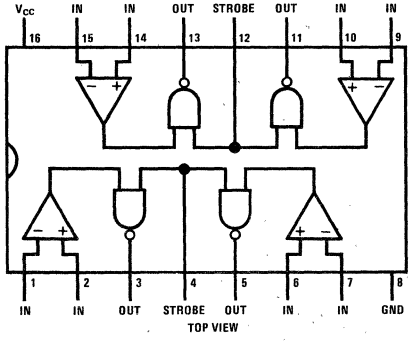
The DS1689/DS3689 provide a TTL strobe input for each pair of receivers, in a 16-lead package, while the DS1690/DS3690 include a separate strobe for each of the four receivers in an 18-lead package. The DS1689 and DS1690 are specified over a −55°C to +125°C operating temperature range, the DS3689 and DS3690 over a 0°C to +70°C range.

features

- Full compatibility with EIA standards RS-232-C, RS-422 and RS-423, and Federal standards 1020 and 1030
- Input voltage range of ±15V (differential or common-mode)
- 5k input impedance
- 50 mV input hysteresis
- 200 mV input threshold
- Four receivers in single 16-lead or 18-lead package
- Single 5V, ±10% supply

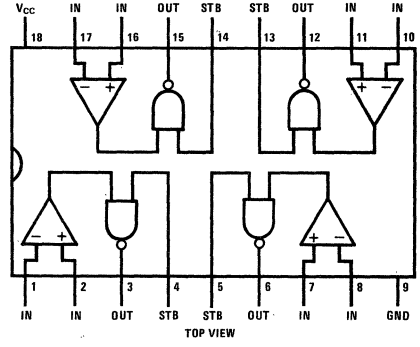
connection diagrams

Dual-In-Line Package



Order Number DS1689J, DS3689J or DS3689N

Dual-In-Line Package



Order Number DS1690J, DS3690J or DS3690N

*Specifications may change

absolute maximum ratings (Note 1)

Supply Voltage	8.0V
Common-Mode Voltage	±25V
Differential Input Voltage	±25V
Strobe Voltage	8.0V
Output Sink Current	50 mA
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1689, DS1690	−55	+125	°C
DS3689, DS3690	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V
Voltage Differential (V_{DIFF})		≤6	V

electrical characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	Differential Threshold Voltage	$-10V \le V_{CM} < +10V$	$I_{OUT} = -400\mu A$, $V_{OUT} \ge 2.5V$		0.06	0.2	V
			$I_{OUT} = 4$ mA, $V_{OUT} \le 0.4V$		−0.08	−0.2	V
		$-15V \le V_{CM} \le +15V$	$I_{OUT} = -400\mu A$, $V_{OUT} \ge 2.5V$		0.06	0.3	V
			$I_{OUT} = 4$ mA, $V_{OUT} \le 0.4V$		−0.08	−0.3	V
R_{IN}	Input Resistance	$-15V \le V_{CM} \le +15V$			5		kΩ
$I_{IN(D)}$	Data Input Current (Unterminated)	$V_{CM} = 15V$			3.0	4.2	mA
		$V_{CM} = 0V$			0	−0.5	mA
		$V_{CM} = -15V$			−3.0	−4.2	mA
	Input Balance	(Note 6)	$I_{OUT} = -400\mu A$, $V_{DIFF} = 0.4V$	2.5			V
		$-7V \le V_{CM} \le +7V$	$I_{OUT} = 4$ mA, $V_{DIFF} = -0.4V$			0.4	V
I_{CC}	Power Supply Current	$V_{DIFF} = -0.5V$, (Note 5)			4.5		mA
V_{OH}	Logical "1" Output Voltage	$I_{OUT} = -400\mu A$, $V_{DIFF} = 1V$		2.5	3.5		V
V_{OL}	Logical "0" Output Voltage	$I_{OUT} = 4$ mA, $V_{DIFF} = -1V$		0	0.25	0.4	V
$V_{IN(1)}$	Logical "1" Strobe Input Voltage	$I_{OUT} = 4$ mA, $V_{OUT} \le 0.4V$, $V_{DIFF} = -3V$		2.0			V
$V_{IN(0)}$	Logical "0" Strobe Input Voltage	$I_{OUT} = -400\mu A$, $V_{OUT} \ge 2.5V$, $V_{DIFF} = -3V$				0.8	V
$I_{IN(1)}$	Logical "1" Strobe Input Current	$V_{STROBE} = 5.5V$, $V_{DIFF} = 3V$				100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	$V_{STROBE} = 0V$, $V_{DIFF} = -3V$				−0.36	mA
I_{OS}	Output Short Circuit Current	$I_{OUT} = 0V$, $V_{STROBE} = 0V$, $V_{CC} = 5.5V$, (Note 4)			−40		mA
$t_{pdo(D)}$	Differential Input to "0" Output	$V_{CC} = 5V$, $T_A = 25°C$			30		ns
$t_{pd1(D)}$	Differential Input to "1" Output				20		ns
$t_{pd0(S)}$	Strobe Input to "0" Output				11		ns
$t_{pd1(S)}$	Strobe Input to "1" Output				10		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1689 and DS1690 and across the 0°C to +70°C range for the DS3689 and DS3690. All typical values are for $T_A = 25°C$, $V_{CC} = 5V$ and $V_{CM} = 0V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: The specifications given are for one receiver only. Therefore, the total package dissipation and supply currents will be four times the values given when all receivers are operated under identical conditions.

Note 6: Refer to EIA-RS-422 for exact conditions.

NATIONAL

Line Drivers/Receivers

DS3650, DS3652 quad TTL compatible line receivers

general description

The DS3650 and DS3652 are TTL compatible quad high speed circuits intended primarily for line receiver applications. Switching speeds have been enhanced over conventional line receivers by the use of Schottky technology, and TRI-STATE® strobing is incorporated offering a high impedance output state for bused organizations.

The DS3650 has active pull-up outputs and offers a TRI-STATE strobe, while the DS3652 offers open collector outputs providing implied "AND" operation.

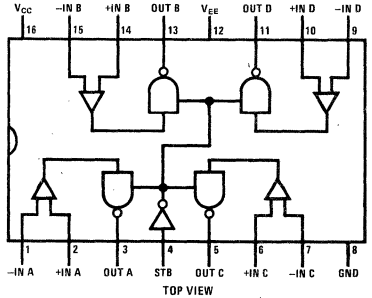
The DS3652 can be used for address decoding as illustrated below. All outputs of the DS3652 are tied together through a common resistor to 5V. In this configuration the DS3652 provides the "AND" function. All addresses have to be true before the output will go high. This scheme eliminates the need for an "AND" gate and enhances speed throughput for address decoding.

features

- High speed 8 ns (typ)
- TTL compatible
- Input sensitivity ±25 mV
- TRI-STATE outputs for high speed buses
- Standard supply voltages ±5V
- Pin and function compatible with MC3450 and MC3452

connection diagram

Dual-In-Line Package



TOP VIEW

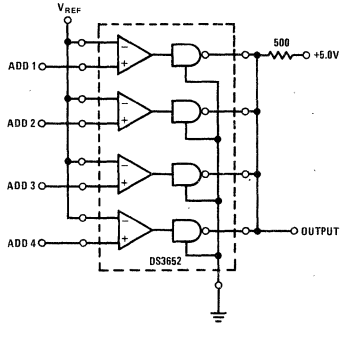
Order Number DS3650J, DS3650N, DS3652J or DS3652N

truth table

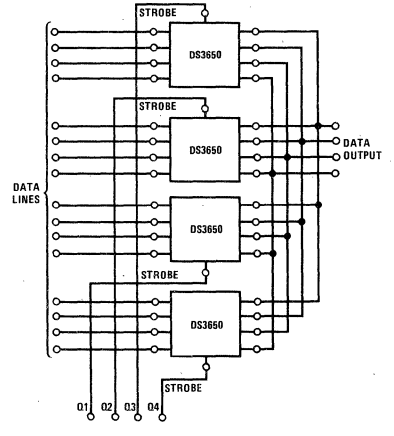
INPUT	STROBE	OUTPUT	
		DS3650	DS3652
$V_{ID} \geq +25$ mV	L	H	Open
	H	Open	Open
-25 mV $\leq V_{ID} \leq +25$ mV	L	X	X
	H	Open	Open
$V_{ID} \leq -25$ mV	L	L	L
	H	Open	Open

L = Low Logic State
H = High Logic State
Open = TRI-STATE
X = Indeterminate State

typical applications



Implied "AND" Gating



Wired "OR" Data Selecting Using TRI-STATE Logic

absolute maximum ratings

(Note 1)

Power Supply Voltages	
V_{CC}	±7.0 V_{DC}
V_{EE}	±7.0 V_{DC}
Differential-Mode Input Signal Voltage Range, V_{IDR}	±6.0 V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	±5.0 V_{DC}
Strobe Input Voltage, $V_{I(S)}$	5.5 V_{DC}
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

(T_A = 0°C to +70°C unless otherwise noted.)

	MIN	MAX	UNITS
Power Supply Voltages			
V_{CC}	+4.75	+5.25	V_{DC}
V_{EE}	−4.75	−5.25	V_{DC}
Output Load Current, I_{OL}		16	mA
Differential-Mode Input Voltage Range, V_{IDR}	−5.0	+5.0	V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	−3.0	+3.0	V_{DC}
Input Voltage Range (any input to GND), V_{IR}	−5.0	+3.0	V_{DC}
Operating Temperature Range, T_A	0	+70	°C

electrical characteristics

(V_{CC} = +5.0 V_{DC}, V_{EE} = −5.0 V_{DC}, T_A = 0°C to +70°C unless otherwise noted) (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{IH(I)}$	High Level Input Current to Receiver Input	*(Figure 5)*				75	µA
$I_{IL(I)}$	Low Level Input Current to Receiver Input	*(Figure 6)*				−10	µA
$I_{IH(S)}$	High Level Input Current to Strobe Input	*(Figure 3)*	$V_{IH(S)}$ = 2.4V			40	µA
			$V_{IH(S)}$ = 5.25V			1	mA
$I_{IL(S)}$	Low Level Input Current to Strobe Input		$V_{IH(S)}$ = 0.4V			−1.6	mA
V_{OH}	High Level Output Voltage	*(Figure 1)*	DS3650	2.4			V_{DC}
I_{CEX}	High Level Output Leakage Current		DS3652			250	µA
V_{OL}	Low Level Output Voltage	*(Figure 1)*				0.4	V_{DC}
I_{OS}	Short-Circuit Output Current (Note 4)	*(Figure 4)*	DS3650	−18		−70	mA
I_{OFF}	Output Disable Leakage Current	*(Figure 7)*	DS3650			40	µA
I_{CCH}	High Logic Level Supply Current from V_{CC}	*(Figure 2)*			45	60	mA
I_{EEH}	High Logic Level Supply Current from V_{EE}				−17	−30	mA

switching characteristics (V_{CC} = +5.0 V_{DC}, V_{EE} = −5.0 V_{DC}, T_A = +25°C unless otherwise noted.)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{PHL(D)}$	High-to-Low Logic Level Propagation Delay Time (Differential Inputs)	*(Figure 8)*	DS3650		9		ns
			DS3652		10		ns
$t_{PLH(D)}$	Low-to-High Logic Level Propagation Delay Time (Differential Inputs)		DS3650		9		ns
			DS3652		10		ns
$t_{POH(S)}$	TRI-STATE to High Logic Level Propagation Delay Time (Strobe)	*(Figure 9)*	DS3650		8		ns
$t_{PHO(S)}$	High Logic Level to TRI-STATE Propagation Delay Time (Strobe)		DS3650		8		ns
$t_{POL(S)}$	TRI-STATE to Low Logic Level Propagation Delay Time (Strobe)		DS3650		10		ns
$t_{PLO(S)}$	Low Logic Level to TRI-STATE Propagation Delay Time (Strobe)		DS3650		10		ns
$t_{PHL(S)}$	High-to-Low Logic Level Propagation Delay Time (Strobe)	*(Figure 10)*	DS3650		7		ns
			DS3652		8		ns
$t_{PLH(S)}$	Low-to-High Logic Level Propagation Delay Time (Strobe)		DS3650		7		ns
			DS3652		8		ns

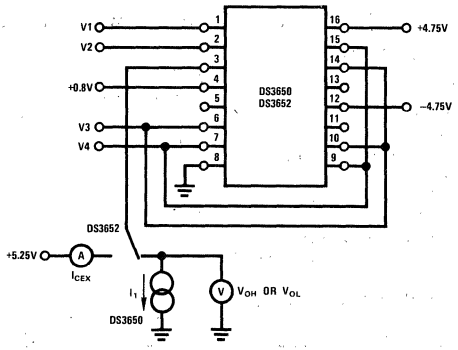
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3650 and DS3652. All typical values are for T_A = 25°C, V_{CC} = 5V, and V_{EE} = −5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

ac test circuits and switching time waveforms



	V1		V2		V3		V4		I_I
	DS3650	DS3652	DS3650	DS3652	DS3650	DS3652	DS3650	DS3652	
V_{OH}	+2.975V		+3.0V		+3.0V		GND		+0.4 mA
	−3.0V		−2.975V		GND		−3.0V		+0.4 mA
I_{CEX}		+2.975V		+3.0V		+3.0V		GND	
		−3.0V		−2.975V		GND		−3.0V	
V_{OL}	+3.0V	+3.0V	+2.975V	+2.975V	GND	GND	+3.0V	+3.0V	−16 mA
	−2.975V	−2.975V	−3.0V	−3.0V	−3.0V	−3.0V	GND	GND	−16 mA

Channel A shown under test. Other channels are tested similarly.

FIGURE 1. I_{CEX}, V_{OH}, and V_{OL}

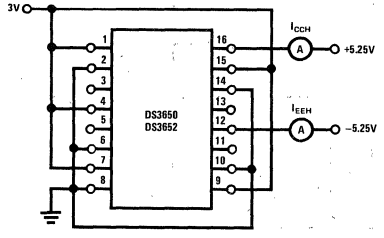


FIGURE 2. I_{CCH} and I_{EEH}

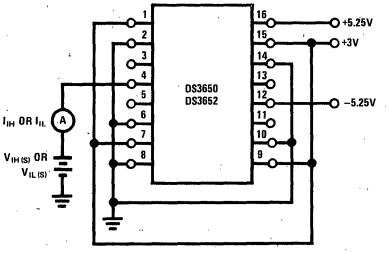
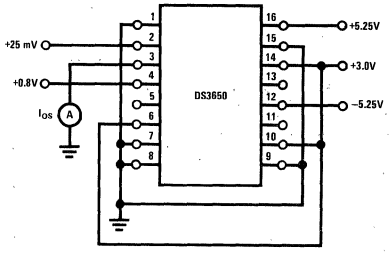
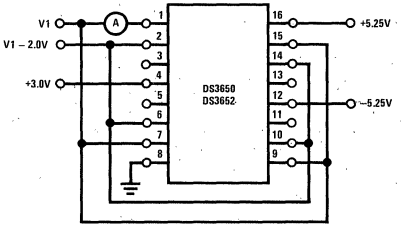


FIGURE 3. $I_{IH(S)}$ and $I_{IL(S)}$



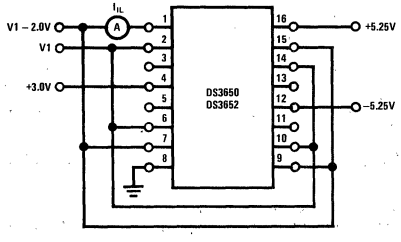
Note: Channel A shown under test, other channels are tested similarly. Only one output shorted at a time.

FIGURE 4. I_{OS}



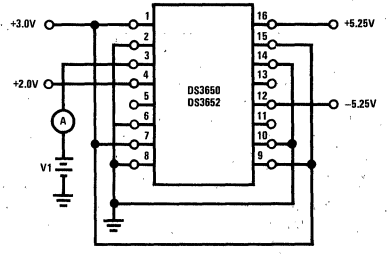
Note: Channel A(−) shown under test, other channels are tested similarly. Devices are tested with V1 from +3.0V to −3.0V.

FIGURE 5. I_{IH}



Note: Channel A(−) shown under test, other channels are tested similarly. Devices are tested with V1 from +3.0V to −3.0V.

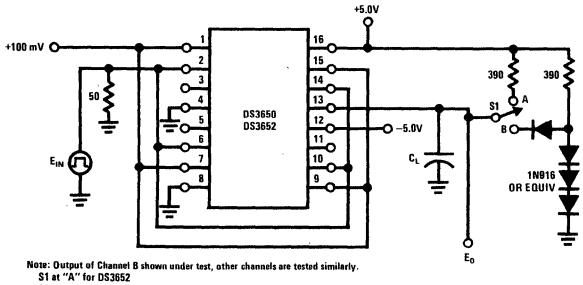
FIGURE 6. I_{IL}



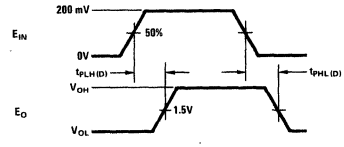
Note: Output of Channel A shown under test, other outputs are tested similarly for V1 = 0.4V and +2.4V.

FIGURE 7. I_{OFF}

ac test circuits and switching time waveforms (con't)

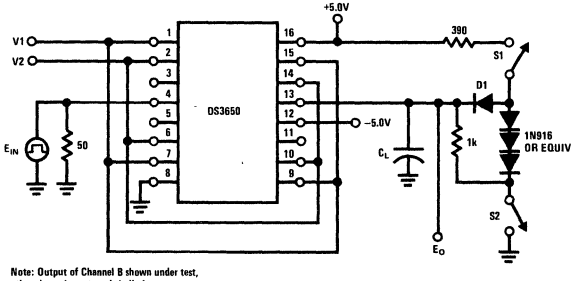


Note: Output of Channel B shown under test, other channels are tested similarly.
S1 at "A" for DS3652
S1 at "B" for DS3650
C_L = 15 pF total for DS3652
C_L = 50 pF total for DS3650



E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1.0 MHz
Duty Cycle = 500 ns

FIGURE 8. Receiver Propagation Delay $t_{PLH(D)}$ and $t_{PHL(D)}$

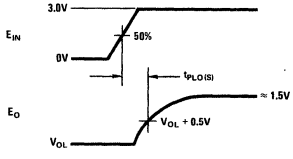


Note: Output of Channel B shown under test, other channels are tested similarly.

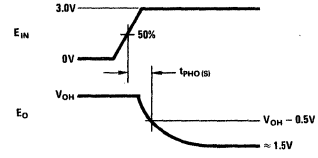
	V1	V2	S1	S2	C_L
$t_{PLO(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{POL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHO(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{POH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.
E_{IN} waveform characteristics: t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%.
PRR = 1.0 MHz
Duty Cycle = 50%

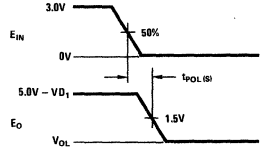
$t_{PLO(S)}$



$t_{PHO(S)}$



$t_{POL(S)}$



$t_{POH(S)}$

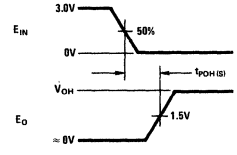
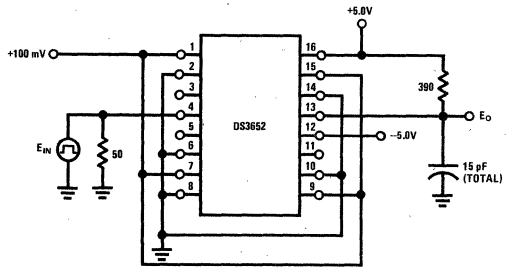


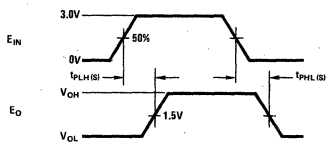
FIGURE 9. Strobe Propagation Delay Times $t_{PLO(S)}$, $t_{POL(S)}$, $t_{PHO(S)}$ and $t_{POH(S)}$

3

ac test circuits and switching time waveforms (con't)



Note: Output of Channel B shown under test, other channels are tested similarly.

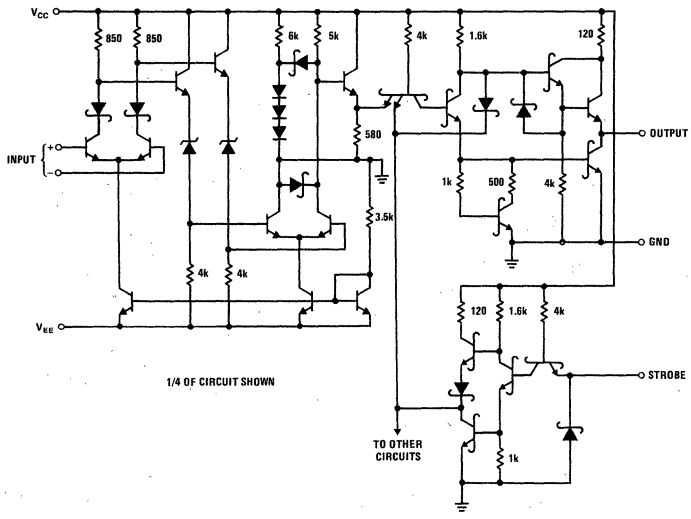


Note: E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1.0 MHz
Duty Cycle = 500 ns

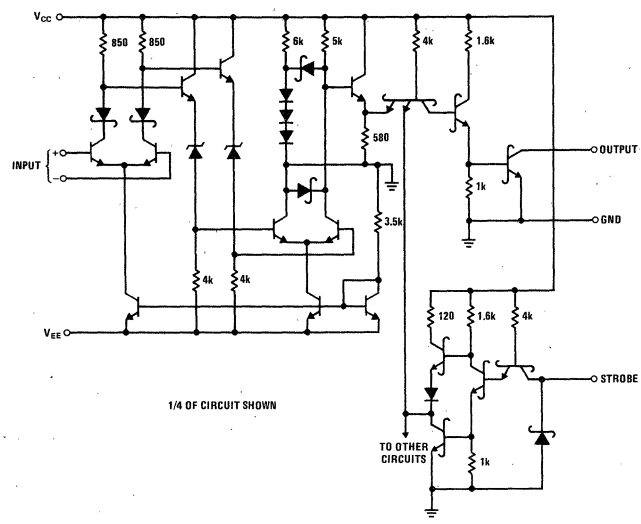
FIGURE 10. Strobe Propagation Delay $t_{PLH(S)}$ and $t_{PHL(S)}$

schematic diagrams

DS3650



DS3652



NATIONAL

Line Drivers/Receivers

DS7640/DS8640 quad NOR unified bus receiver

general description

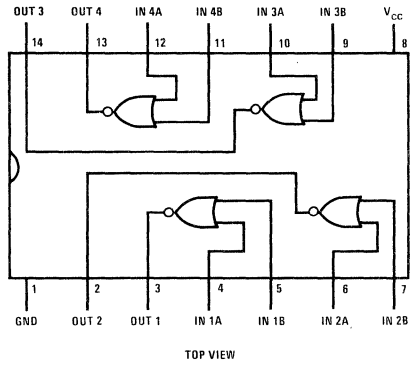
The DS7640 and DS8640 are quad 2-input receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The design employs a built-in input threshold providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus. This receiver has been specifically configured to replace the SP380 gate pin-for-pin.

features

- Plug-in replacement for SP380 gate
- Low input current with normal V_{CC} or V_{CC} = 0V (30μA typ)
- High noise immunity (1.1V typ)
- Temperature-insensitive input thresholds track bus logic levels
- DTL/TTL compatible output
- Matched, optimized noise immunity for "1" and "0" levels
- High speed (19 ns typ)

connection diagram

Dual-In-Line Package

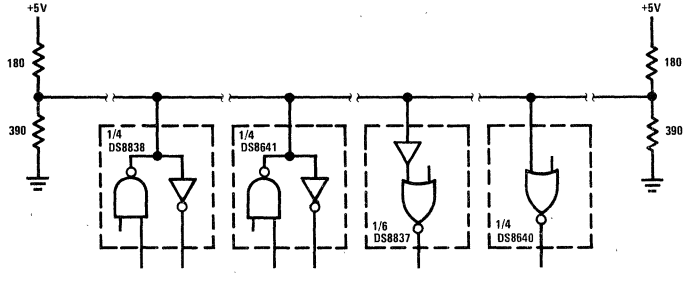


TOP VIEW

Order Number DS7640J, DS8640J
DS8640N or DS7640W

typical application

120Ω Unified Data Bus



3

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7640	4.5	5.5	V
DS8640	4.75	5.25	V
Temperature (T_A)			
DS7640	−55	+125	°C
DS8640	0	+70	°C

electrical characteristics

The following apply for $V_{MIN} \leq V_{CC} \leq V_{MAX}$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Threshold	$V_{OUT} = V_{OL}$	DS7640	1.80	1.50		V
			DS8640	1.70	1.50		V
V_{IL}	Low Level Input Threshold	$V_{OUT} = V_{OH}$	DS7640		1.50	1.20	V
			DS8640		1.50	1.30	V
I_{IH}	Maximum Input Current	$V_{IN} = 4V$	$V_{CC} = V_{MAX}$		30	80	μA
			$V_{CC} = 0V$		1.0	50	μA
I_{IL}	Maximum Input Current	$V_{IN} = 0.4V$, $V_{CC} = V_{MAX}$			1.0	50	μA
V_{OH}	Output Voltage	$I_{OH} = -400\mu A$, $V_{IN} = V_{IL}$		2.4			V
V_{OL}	Output Voltage	$I_{OL} = 16$ mA, $V_{IN} = V_{IH}$			0.25	0.4	V
I_{OS}	Output Short Circuit Current	$V_{IN} = 0.5V$, $V_{OS} = 0V$, $V_{CC} = V_{MAX}$, (Note 4)		−18		−55	mA
I_{CC}	Power Supply Current	$V_{IN} = 4V$, (Per Package)			25	40	mA

switching characteristics

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd}	Propagation Delays	(Notes 5 and 6)	Input to Logic "1" Output	10	23	35	ns
			Input to Logic "0" Output	10	15	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7640 and across the 0°C to +70°C range for the DS8640. All typical values are for $T_A = 25°C$ and $V_{CC} = 5V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Fan-out of 10 load, $C_{LOAD} = 15$ pF total, measured from $V_{IN} = 1.5V$ to $V_{OUT} = 1.5V$, $V_{IN} = 0V$ to 3V pulse.

Note 6: Apply for $V_{CC} = 5V$, $T_A = 25°C$.

Line Drivers/Receivers

DS7641/DS8641 quad unified bus transceiver

general description

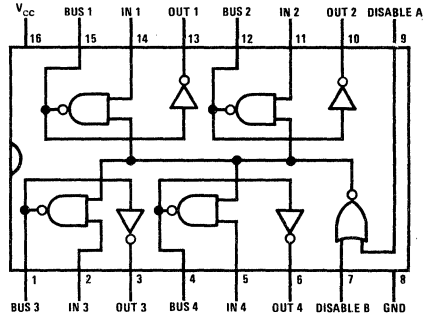
The DS7641 and DS8641 are quad high speed drivers/receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be a 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when V_{CC} = 0V. The receivers incorporate tight thresholds for better bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously.

features

- 4 separate driver/receiver pairs per package
- Guaranteed minimum bus noise immunity of 0.6V, 1.1V typ
- Temperature insensitive receiver thresholds track bus logic levels
- 30μA typical bus terminal current with normal V_{CC} or with V_{CC} = 0V
- Open collector driver output allows wire-OR connection
- High speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs

connection diagram

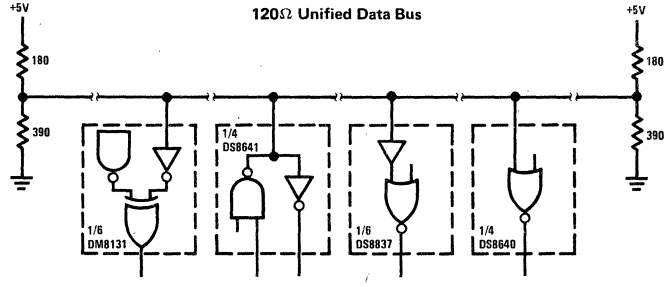
Dual-In-Line and Flat Package



TOP VIEW

Order Number DS7641J, DS8641J
or DS8641N

typical application



3

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input and Output Voltage	5.5V
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, (V_{CC})			
DS7641	4.5	5.5	V
DS8641	4.75	5.25	V
Temperature Range, (T_A)			
DS7641	−55	+125	°C
DS8641	0	+70	°C

electrical characteristics

The following apply for $V_{MIN} \leq V_{CC} \leq V_{MAX}$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER AND DISABLE INPUTS							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_I	Logical "1" Input Current	V_{IN} = 5.5V				1	mA
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V				40	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V				−1.6	mA
V_{CL}	Input Diode Clamp Voltage	I_{DIS} = −12 mA, I_{IN} = −12 mA, I_{BUS} = −12 mA, T_A = 25°C			−1	−1.5	V
DRIVER OUTPUT/RECEIVER INPUT							
V_{OLB}	Low Level Bus Voltage	V_{DIS} = 0.8V, V_{IN} = 2V, I_{BUS} = 50 mA			0.4	0.7	V
I_{IHB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4V, V_{CC} = V_{MAX}			30	100	μA
I_{ILB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4V, V_{CC} = 0V			2	100	μA
V_{IH}	High Level Receiver Threshold	V_{IND} = 0.8V, V_{OL} = 16 mA	DS7641	1.80	1.50		V
			DS8641	1.70	1.50		V
V_{IL}	Low Level Receiver Threshold	V_{IND} = 0.8V, V_{OH} = −400μA	DS7641		1.50	1.20	V
			DS8641		1.50	1.30	V
RECEIVER OUTPUT							
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.8V, V_{BUS} = 0.5V, I_{OH} = −400μA		2.4			V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 0.8V, V_{BUS} = 4V, I_{OL} = 16 mA			0.25	0.4	V
I_{OS}	Output Short Circuit Current	V_{DIS} = 0.8V, V_{IN} = 0.8V, V_{BUS} = 0.5V, V_{OS} = 0V, V_{CC} = V_{MAX}, (Note 4)		−18		−55	mA
I_{CC}	Supply Current	V_{DIS} = 0V, V_{IN} = 2V, (Per Package)			50	70	mA

switching characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd}	Propagation Delays (Note 7)					
	Disable to Bus "1"	(Note 5)		19	30	ns
	Disable to Bus "0"			15	23	ns
	Driver Input to Bus "1"			17	25	ns
	Driver Input to Bus "0"			9	15	ns
	Bus to Logical "1" Receiver Output	(Note 6)		20	30	ns
	Bus to Logical "0" Receiver Output			18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7641 and across the 0°C to +70°C range for the DS8641. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: 91Ω from bus pin to V_{CC} and 200Ω from bus pin to ground. C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.5V to V_{BUS} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 6: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.5V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 7: The following apply for V_{CC} = 5V, T_A = 25°C unless otherwise specified.

NATIONAL

Line Drivers/Receivers

DS8642 quad transceiver

general description

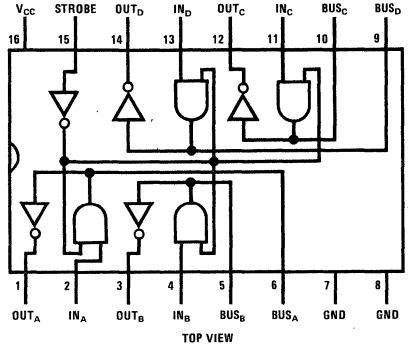
The DS8642 is a quad transceiver designed for bus organized data transmission systems terminated by 50Ω impedance. The bus can be terminated at one or both ends. It has four bus drivers with a common strobe gate and four bus receivers. Bus driver outputs can be "OR-tied" with up to 19 other drivers and with up to 20 bus receiver loads. The bus loading is 2k when V_{CC} = 0V.

features

- 100 mA Drive Capability
- Four separate driver/receiver pairs
- Open collector driver output allows wire-OR connection
- 50Ω line termination
- Completely TTL compatible on driver and disable inputs, and receiver outputs

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DS8642J
or DS8642N

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	600 mW
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
DISABLE/DRIVER INPUT							
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−0.9	−1.6	mA
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			40	μA
			V_{IN} = 5.5V			1	mA
V_{CD}	Input Clamp Voltage	I_{IN} = −12 mA			−0.8	−1.5	V
RECEIVER INPUT/BUS OUTPUT							
V_{IHB}	Logical "1" Input Voltage	V_{CC} = Max		3.1			V
V_{ILB}	Logical "0" Input Voltage	V_{CC} = Min				1.4	V
V_{CDB}	Input Clamp Diode	I_{IN} = −50 mA			−1.0	−1.5	V
I_{IHB}	Logical "1" Input Current	V_{CC} = Max, V_{INB} = V_{CC}			180	450	μA
I_{ILB}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−40	μA
V_{OLB}	Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 100 mA			0.4	0.8	V
I_{OL}	Logical "0" Output Current	V_{CC} = Min, V_{OL} = 0.8V		100			mA
I_{OHB}	Power "OFF" Bus Current	V_{CC} = 0V, V_{INB} = 5.25V			1.7	2.65	mA
RECEIVER OUTPUT							
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −1 mA		2.4	3.2		V
I_{OH}	Logical "1" Output Current	V_{CC} = Min, V_{OUT} = 5.5V				100	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Min, V_{OUT} = 0V, (Note 4)		−10	−28	−55	mA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA			0.3	0.45	V
I_{CC}	Supply Current	V_{CC} = Max			49	64	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8642. All typicals are given for V_{CC} = 5V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

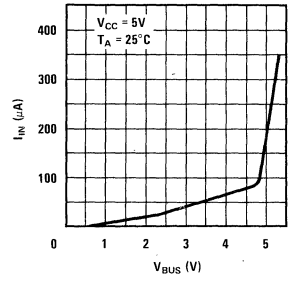
Note 4: Only one output at a time should be shorted.

switching characteristics

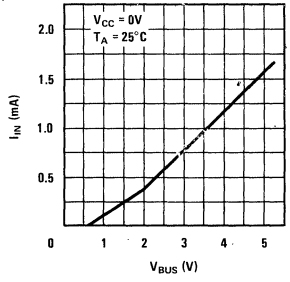
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0" From Data Input to Receiver Output	*(Figure 1)*		34	50	ns
t_{pd1}	Propagation Delay to a Logical "1" From Data Input to Receiver Output	*(Figure 1)*		25	50	ns
t_{pd0}	Propagation Delay to a Logical "0" From Strobe Input to Receiver Output	*(Figure 1)*		38	55	ns
t_{pd1}	Propagation Delay to a Logical "1" From Strobe Input to Receiver Output	*(Figure 1)*		25	55	ns

typical performance characteristics

Receiver ON Impedance



Receiver OFF Impedance



ac test circuit and switching time waveforms

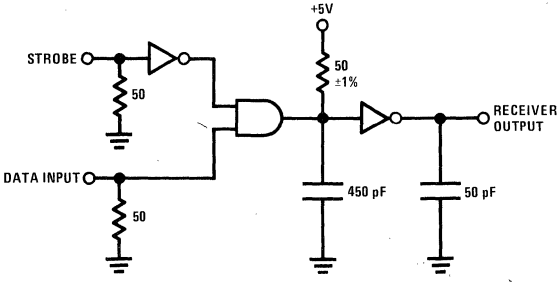
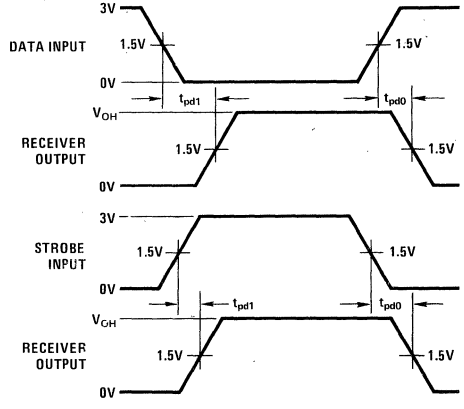


FIGURE 1.



f = 5 MHz
Pulse Width = 100 ns
$t_r = t_f \approx 5$ ns

NATIONAL

Line Drivers/Receivers

DS7820/DS8820 dual line receiver

general description

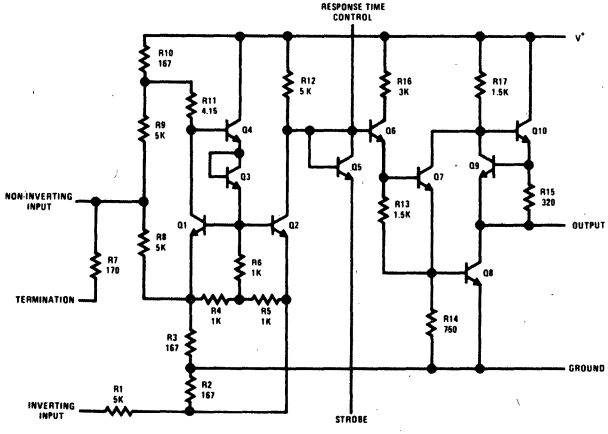
The DS7820, specified from −55°C to +125°C, and the DS8820, specified from 0°C to +70°C, are digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits.

features

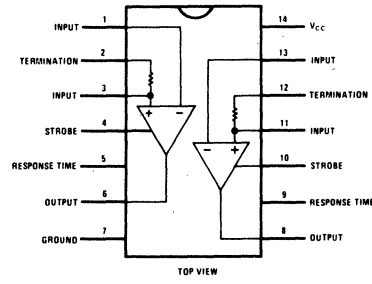
- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Each channel can be strobed independently
- High input resistance
- Fanout of two with either DTL or TTL integrated circuits

The response time can be controlled with an external capacitor to eliminate noise spikes, and the output state is determined for open inputs. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820 and the DS8820 are specified, worst case, over their full operating temperature range, for ±10-percent supply voltage variations and over the entire input voltage range.

schematic and connection diagrams

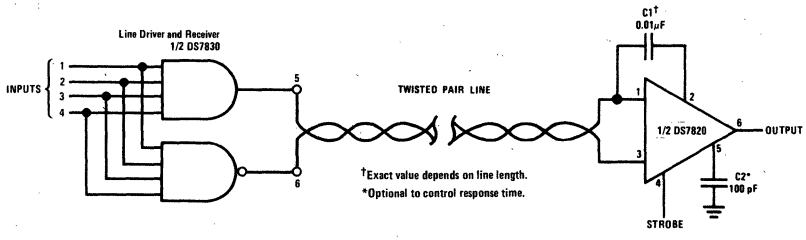


Dual-In-Line and Flat Package



Order Number DS7820J or DS8820J
Order Number DS8820N
Order Number DS7820W or DS8820W

typical application



absolute maximum ratings (Note 1)

Supply Voltage	8.0V
Input Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	25 mA
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7820	4.5	5.5	V
DS8820	4.75	5.25	V
Temperature (T_A)			
DS7820	−55	+125	°C
DS8820	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{TH}	Input Threshold Voltage	$V_{IN} = 0$	−0.5	0	0.5	V
		$-15V \leq V_{IN} \leq 15V$	−1.0	0	1.0	V
V_{OH}	High Output Level	$I_{OUT} \leq 0.2$ mA	2.5		5.5	V
V_{OL}	Low Output Level	$I_{SINK} \leq 3.5$ mA	0		0.4	V
R_I^-	Inverting Input Resistance		3.6	5.0		kΩ
R_I^+	Non-Inverting Input Resistance		1.8	2.5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$	120	170	250	Ω
t_r	Response Time	$C_{DELAY} = 0$		40		ns
		$C_{DELAY} = 100$ pF		150		ns
I_{ST}	Strobe Current	$V_{STROBE} = 0.4V$		1.0	1.4	mA
		$V_{STROBE} = 5.5V$			−5.0	μA
I_{CC}	Power Supply Current	$V_{IN} = 15V$		3.2	6.0	mA
		$V_{IN} = 0$		5.8	10.2	mA
		$V_{IN} = -15V$		8.3	15.0	mA
I_{IN}^+	Non-Inverting Input Current	$V_{IN} = 15V$		5.0	7.0	mA
		$V_{IN} = 0$	−1.6	−1.0		mA
		$V_{IN} = -15V$	−9.8	−7.0		mA
I_{IN}^-	Inverting Input Current	$V_{IN} = 15V$		3.0	4.2	mA
		$V_{IN} = 0$		0	−0.5	mA
		$V_{IN} = -15V$	−4.2	−3.0		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

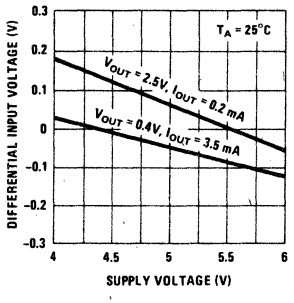
Note 2: These specifications apply for $4.5V \leq V_{CC} \leq 5.5V$, $-15V \leq V_{CM} \leq 15V$ and $-55°C \leq T_A \leq +125°C$ for the DS7820 or $0°C \leq T_A \leq +70°C$ for the DS8820 unless otherwise specified; typical values given are for $V_{CC} = 5.0V$, $T_A = 25°C$ and $V_{CM} = 0$ unless stated differently.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

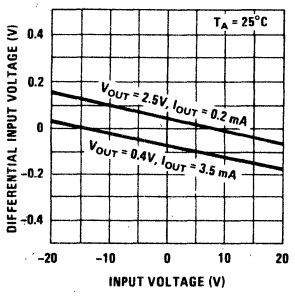
Note 4: The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

typical performance characteristics (Note 3)

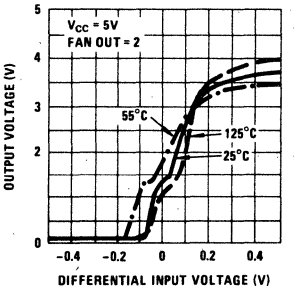
Supply Voltage Sensitivity



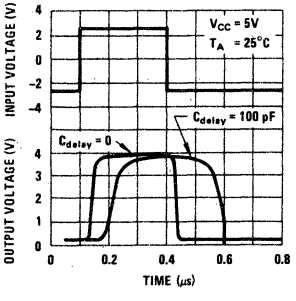
Common Mode Rejection



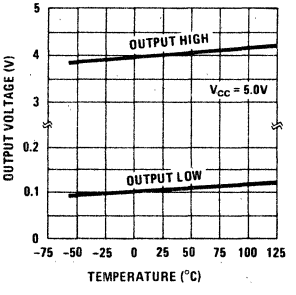
Transfer Function



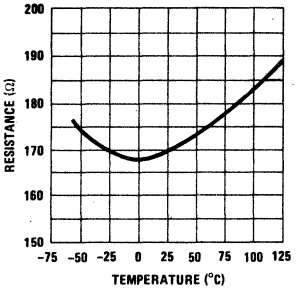
Response Time



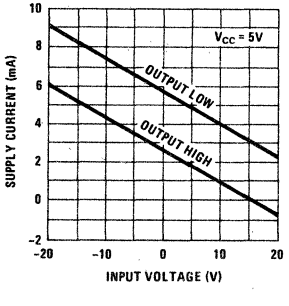
Output Voltage Levels



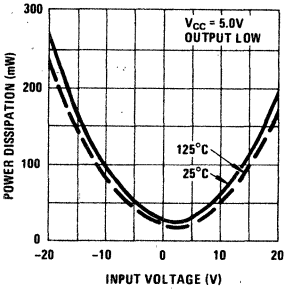
Termination Resistance



Positive Supply Current



Internal Power Dissipation



NATIONAL

Line Drivers/Receivers

DS7820A/DS8820A dual line receiver

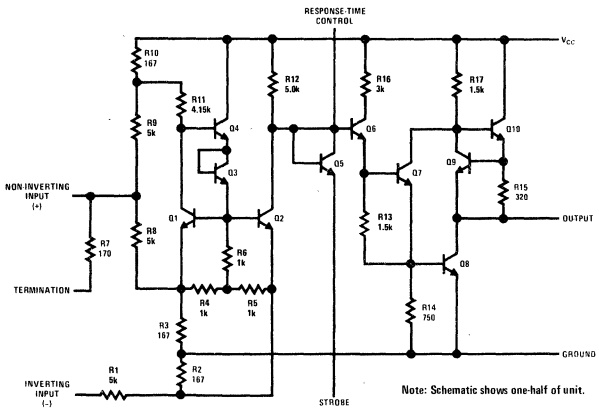
general description

The DS7820A and the DS8820A are improved performance digital line receivers with two completely independent units fabricated on a single silicon chip. Intended for use with digital systems connected by twisted pair lines, they have a differential input designed to reject large common mode signals while responding to small differential signals. The output is directly compatible with RTL, DTL or TTL integrated circuits. Some important design features include:

- Operation from a single +5V logic supply
- Input voltage range of ±15V
- Strobe low forces output to "1" state
- High input resistance
- Fanout of ten with either DTL or TTL integrated circuits
- Outputs can be wire OR'ed
- Series 54/74 compatible

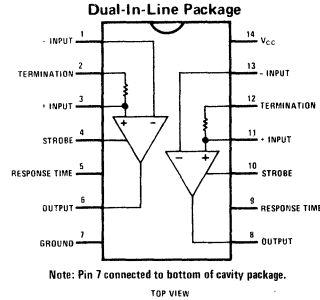
The response time can be controlled with an external capacitor to reject input noise spikes. The output state is a logic "1" for both inputs open. Termination resistors for the twisted pair line are also included in the circuit. Both the DS7820A and the DS8820A are specified, worst case, over their full operating temperature range (−55°C to 125°C and 0°C to 70°C respectively), over the entire input voltage range, for ±10% supply voltage variations.

schematic and connection diagrams



Note: Schematic shows one-half of unit.

Dual-In-Line Package



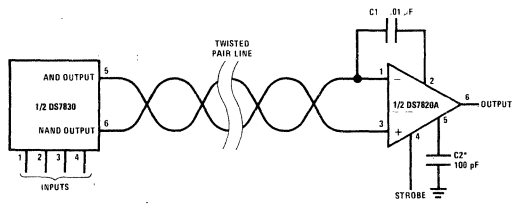
Note: Pin 7 connected to bottom of cavity package.

TOP VIEW

Order Number DS7820AJ or DS8820AJ
Order Number DS8820AN
Order Number DS7820AW or DS8820AW

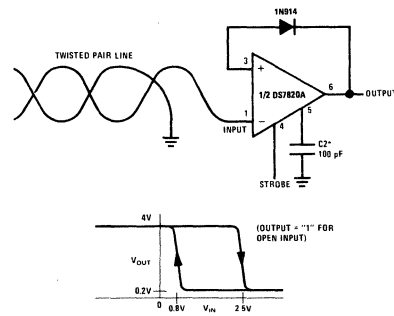
typical applications

Differential Line Driver and Receiver



*Optional to control response time.

Single Ended (EIA-RS232C) Receiver with Hysteresis



absolute maximum ratings (Note 1)

Supply Voltage	8.0V
Common-Mode Voltage	±20V
Differential Input Voltage	±20V
Strobe Voltage	8.0V
Output Sink Current	50 mA
Power Dissipation	600 mW
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7820A	4.5	5.5	V
DS8820A	4.75	5.25	V
Temperature (T_A)			
DS7820A	−55	+125	°C
DS8820A	0	+70	°C

electrical characteristics (Notes 2, 3, 4 and 5)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{TH}	Differential Threshold Voltage	I_{OUT} = −400μA, $V_{OUT} \geq$ 2.5V	−3V ≤ V_{CM} ≤ +3V			0.06	0.5	V
			−15V ≤ V_{CM} ≤ +15V			0.06	1.0	V
		I_{OUT} = +16 mA, $V_{OUT} \leq$ 0.4V	−3V ≤ V_{CM} ≤ +3V			−0.08	−0.5	V
			−15V ≤ V_{CM} ≤ +15V			−0.08	−1.0	V
R_I^-	Inverting Input Resistance	−15V ≤ V_{CM} ≤ +15V			3.6	5		kΩ
R_I^+	Non-Inverting Input Resistance	−15V ≤ V_{CM} ≤ +15V			1.8	2.5		kΩ
R_T	Line Termination Resistance	T_A = 25°C			120	170	250	Ω
I_I^-	Inverting Input Current	V_{CM} = 15V				3.0	4.2	mA
		V_{CM} = 0V				0	−0.5	mA
		V_{CM} = −15V				−3.0	−4.2	mA
I_I^+	Non-Inverting Input Current	V_{CM} = 15V				5.0	7.0	mA
		V_{CM} = 0V				−1.0	−1.6	mA
		V_{CM} = −15V				−7.0	−9.8	mA
I_{CC}	Power Supply Current	I_{OUT} = Logical "0"	V_{DIFF} = −1V	V_{CM} = 15V		3.9	6.0	mA
				V_{CM} = −15V		9.2	14.0	mA
			V_{DIFF} = −0.5V,	V_{CM} = 0V		6.5	10.2	mA
V_{OH}	Logical "1" Output Voltage	I_{OUT} = −400μA, V_{DIFF} = 1V			2.5	4.0	5.5	V
V_{OL}	Logical "0" Output Voltage	I_{OUT} = +16 mA, V_{DIFF} = −1V			0	0.22	0.4	V
V_{SH}	Logical "1" Strobe Input Voltage	I_{OUT} = +16 mA, $V_{OUT} \leq$ 0.4V, V_{DIFF} = −3V			2.1			V
V_{SL}	Logical "0" Strobe Input Voltage	I_{OUT} = −400μA, $V_{OUT} \geq$ 2.5V, V_{DIFF} = −3V					0.9	V
I_{SH}	Logical "1" Strobe Input Current	V_{STROBE} = 5.5V, V_{DIFF} = 3V				0.01	5.0	μA
I_{SL}	Logical "0" Strobe Input Current	V_{STROBE} = 0.4V, V_{DIFF} = −3V				−1.0	−1.4	mA
I_{SC}	Output Short Circuit Current	I_{OUT} = 0V, V_{CC} = 5.5V, V_{STROBE} = 0V			−2.8	−4.5	−6.7	mA

switching characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay, Differential Input to "0" Output	V_{CC} = 5V, T_A = 25°C		30	45	ns
t_{pd1}	Propagation Delay, Differential Input to "1" Output	V_{CC} = 5V, T_A = 25°C		27	40	ns
t_{pd0}	Propagation Delay, Strobe Input to "0" Output	V_{CC} = 5V, T_A = 25°C		16	25	ns
t_{pd1}	Propagation Delay, Strobe Input to "1" Output	V_{CC} = 5V, T_A = 25°C		18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These specifications apply for 4.5V ≤ V_{CC} ≤ 5.5V, −15V ≤ V_{CM} ≤ 15V and −55°C ≤ T_A ≤ +125°C for the DS7820A or 0°C ≤ T_A ≤ +70°C for the DS8820A unless otherwise spedified. Typical values given are for V_{CC} = 5.0V, T_A = 25°C and V_{CM} = 0V unless stated differently.

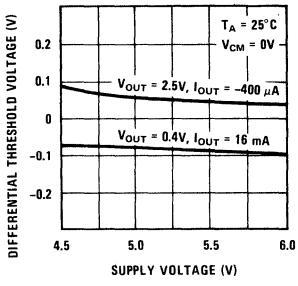
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

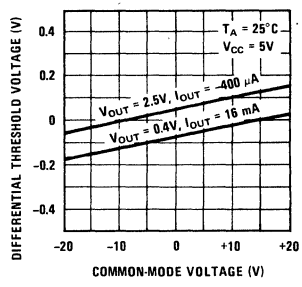
Note 5: The specifications and curves given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

typical performance characteristics (Note 3)

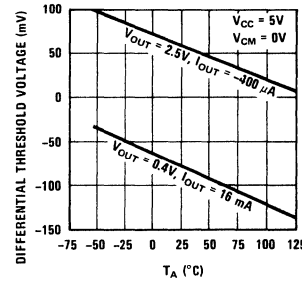
Supply Voltage Sensitivity



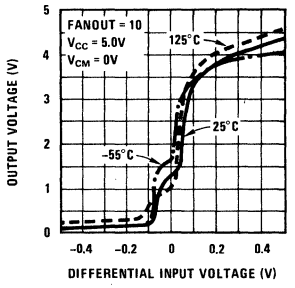
Common-Mode Voltage Sensitivity



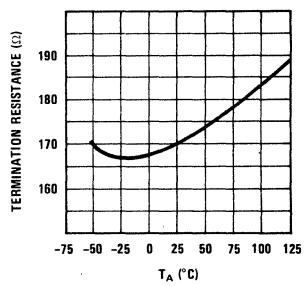
Temperature Sensitivity



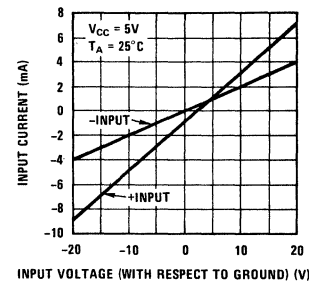
Transfer Function



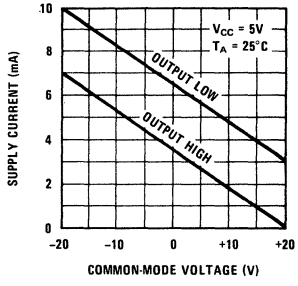
Termination Resistance



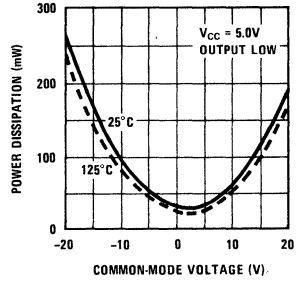
Input Characteristics



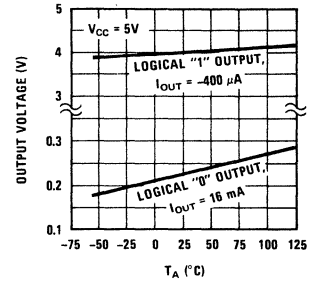
Power Supply Current



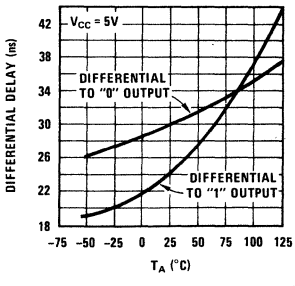
Internal Power Dissipation



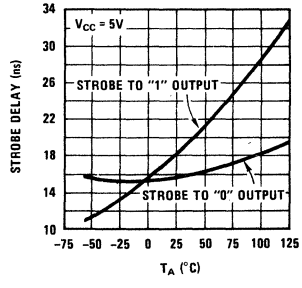
Output Voltage Levels



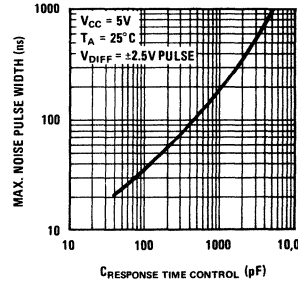
Differential Input Delays



Strobe Delays

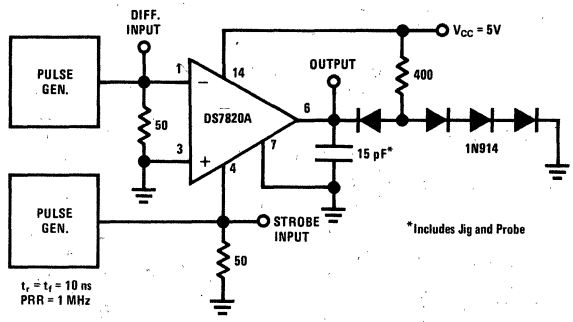


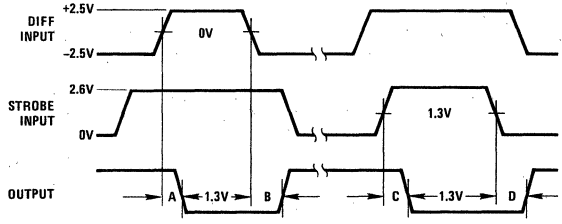
Noise Rejection



3

ac test circuit and waveforms





A = Differential Input to "0" Output
B = Differential Input to "1" Output
C = Strobe Input to "0" Output
D = Strobe Input to "1" Output

NATIONAL

Line Drivers/Receivers
Advance Information*

DS78LS20/DS88LS20 dual differential line receiver

general description

The DS78LS20 and DS88LS20 are high performance dual differential line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA and Federal Standards, and the Schottky-clamped output gate is fully compatible with low power Schottky logic (54LS). Input specifications meet or exceed those of the popular DS7820 line receiver, and the pinout is identical.

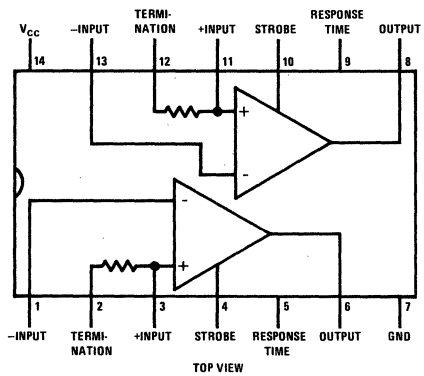
A response pin is provided for controlling sensitivity to input noise spikes with an external capacitor. Each receiver includes a 180 ohm terminating resistor, which may be used optionally on twisted pair lines. The DS78LS20 is specified over a −55°C to +125°C operating temperature range, and the DS88LS20 over a 0°C to +70°C range.

features

- Full compatibility with EIA Standards RS-232-C, RS-422 and RS-423, and Federal Standards 1020 and 1030
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- 5k input impedance
- 50 mV input hysteresis
- 200 mV input threshold
- Fanout 10 54LS/74LS gate inputs
- Operation from single +5V, ±10% supply

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number
DS78LS20J, DS88LS20J, DS88LS20N
or DS78LS20W

*Specifications may change

absolute maximum ratings (Note 1)

Supply Voltage	8.0V
Common-Mode Voltage	±25V
Differential Input Voltage	±25V
Strobe Voltage	8.0V
Output Sink Current	50 mA
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS78LS20	−55	+125	°C
DS88LS20	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V
Differential Input Voltage (V_{DIFF})		≤ 6	V

electrical characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	Differential Threshold Voltage	$I_{OUT} = -400\mu A$, $V_{OUT} \geq 2.5V$	$-10V \leq V_{CM} \leq 10V$		0.06	0.2	V
			$-15V \leq V_{CM} \leq 15V$		0.06	0.3	V
		$I_{OUT} = 4$ mA, $V_{OUT} \leq 0.4V$	$-10V \leq V_{CM} \leq 10V$		−0.08	−0.2	V
			$-15V \leq V_{CM} \leq 15V$		−0.08	−0.3	V
R_{IN}	Input Resistance	$-15V \leq V_{CM} \leq 15V$			5		kΩ
R_T	Line Termination Resistance	$T_A = 25°C$			180		Ω
$I_{IN(D)}$	Data Input Current (Unterminated)	$V_{CM} = 15V$			3.0	4.2	mA
		$V_{CM} = 0V$			0	−0.5	mA
		$V_{CM} = -15V$			−3.0	−4.2	mA
	Input Balance	$-7V \leq V_{CM} \leq 7V$, (Note 6)	$I_{OUT} = -400\mu A$, $V_{DIFF} = 0.4V$	2.5			V
			$I_{OUT} = 4$ mA, $V_{DIFF} = -0.4V$		0.4		V
I_{CC}	Power Supply Current	$15V \leq V_{CM} \leq -15V$, $V_{DIFF} = -0.5V$, (Note 5)			4.5		mA
V_{OH}	Logical "1" Output Voltage	$I_{OUT} = -400\mu A$, $V_{DIFF} = 1V$		2.5	4.0	5.5	V
V_{OL}	Logical "0" Output Voltage	$I_{OUT} = 4$ mA, $V_{DIFF} = -1V$		0	0.25	0.4	V
$V_{IN(1)}$	Logical "1" Strobe Input Voltage	$I_{OUT} = 4$ mA, $V_{OUT} \leq 0.4V$, $V_{DIFF} = -3V$		2.0			V
$V_{IN(0)}$	Logical "0" Strobe Input Voltage	$I_{OUT} = -400\mu A$, $V_{OUT} \geq 2.5V$, $V_{DIFF} = -3V$				0.8	V
$I_{IN(1)}$	Logical "1" Strobe Input Current	$V_{STROBE} = 5.5V$, $V_{DIFF} = 3V$				100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	$V_{STROBE} = 0V$, $V_{DIFF} = -3V$				−0.36	mA
I_{OS}	Output Short Circuit Current	$V_{OUT} = 0V$, $V_{CC} = 5.5V$, $V_{STROBE} = 0V$, (Note 4)			−40		mA

switching characteristics

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{pd0(D)}$	Differential Input to "0" Output	$V_{CC} = 5V$, $T_A = 25°C$		30		ns
$t_{pd1(D)}$	Differential Input to "1" Output	$V_{CC} = 5V$, $T_A = 25°A$		20		ns
$t_{pd0(S)}$	Strobe Input to "0" Output	$V_{CC} = 5V$, $T_A = 25°C$		11		ns
$t_{pd1(S)}$	Strobe Input to "1" Output	$V_{CC} = 5V$, $T_A = 25°C$		10		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78LS20 and across the 0°C to +70°C range for the DS88LS20. All typical values are for $T_A = 25°C$, $V_{CC} = 5V$ and $V_{CM} = 0V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: The specifications given are for one side only. Therefore, the total package dissipation and supply currents will be double the values given when both receivers are operated under identical conditions.

Note 6: Refer to EIA-RS-422 for exact conditions.

Line Drivers /Receivers

DS7822/DS8822 dual line receiver

general description

The DS7822/DS8822 is a dual inverting line receiver which meets the requirements of EIA specification RS232 Revision B. The device contains both receivers on a single monolithic silicon chip. The receivers share common power supply and ground connections, otherwise their operation is fully independent.

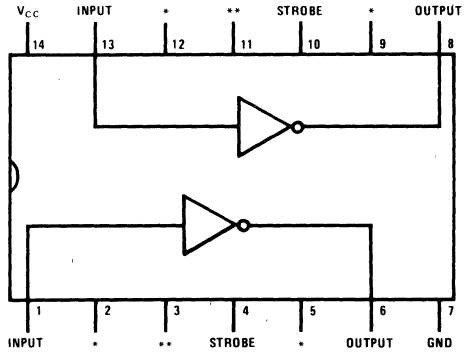
In addition to meeting the requirements of RS232, the DS7822/DS8822 also has independent strobe inputs which allow the receiver to be placed in the high state independent of the information being received at the input.

The output of the DS7822/DS8822 is completely compatible with 5V DTL and TTL logic families.

The DS7822 is specified for operation over the −55°C to +125°C military temperature range. The DS8822 is specified for operation over the 0°C to +70°C temperature range.

connection diagram

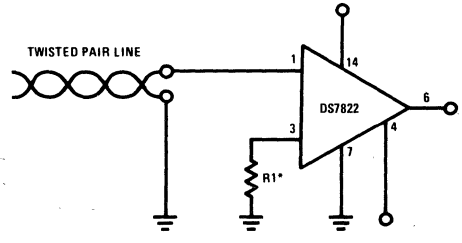
Dual-In-Line Package



*Make no connection to these pins.
**For operation requiring "Mark Hold" with the input open connect a 470Ω resistors from each of these pins to ground.

Order Number DS7822J
or DS8822N

typical connection



*For Mark Hold R1 = 470Ω, otherwise connect pin 3 to ground.

absolute maximum ratings (Note 1)

Supply Voltage		8.0V
Input Voltage		±30V
Strobe Voltage		8.0V
Output Sink Current		25 mA
Power Dissipation		600 mW
Operating Temperature Range	DS7822	−55°C to +125°C
	DS8822	0°C to 70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7822	4.5	5.5	V
DS8822	4.75	5.25	V
Temperature (T_A)			
DS7822	−55	+125	°C
DS8822	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{TH}^-	Negative Input Threshold Voltage	$V_{OUT} \geq 2.5V$	−2.0			V
V_{TH}^+	Positive Input Threshold Voltage	$V_{OUT} \leq 0.4V$, (Note 4)			2.0	V
R_{IN}	Input Resistance		3.0	5.0	7.0	kΩ
I_{IN}	Input Current	$V_{IN} = 25V$	3.57	5	8.33	mA
		$V_{IN} = 0V$		0		mA
		$V_{IN} = -25V$	−8.33	−5	−3.57	mA
V_{IO}	Open Circuit Input Voltage	$V_{IN} = 0V$		0.03	0.5	V
V_{OH}	Logical "1" Output Voltage	$I_{OUT} \leq -0.2$ mA	2.5			V
V_{OL}	Logical "0" Output Voltage	$I_{OUT} = 3.5$ mA			0.4	V
I_{ST}	Strobe Current	$V_{STROBE} = 0.4V$		1.0	1.4	mA
		$V_{STROBE} = 5.5V$		−5.0μA	−1.0 mA	
I_{CC}	Power Supply Current (Both Receivers)	$-25V \leq V_{IN} \leq 25V$			24.0	mA
t_r	Response Time, t_1 or t_2	$T_A = 25°C$, $V_{CC} = 5.0V$, Input Ramp Rate ≤ 10 ns		65	125	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

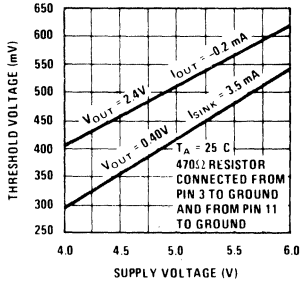
Note 2: Min/max limits apply across the guaranteed temperature range of −55°C to +125°C for the DS7822 and 0°C to +70°C for the DS8822 unless otherwise specified. Likewise the limits apply across the guaranteed V_{CC} range of 4.5V to 5.5V for the DS7822 and 4.75V to 5.25V for the DS8822 unless otherwise specified. Typical values are given for $V_{CC} = 5.0V$ and $T_A = 25°C$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

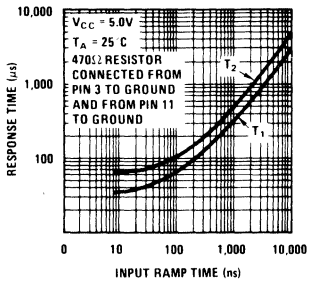
Note 4: Since the EIA RS-232 specification requires the threshold to be between −3V and +3V, the immunity limits shown here guarantee 1V additional noise immunity.

typical performance characteristics

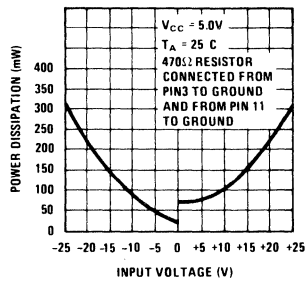
Threshold Voltage vs Supply Voltage



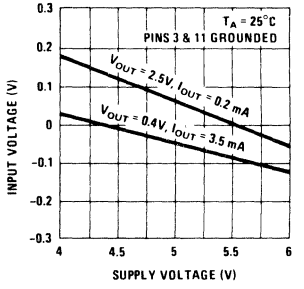
Response Time vs Input Ramp Time



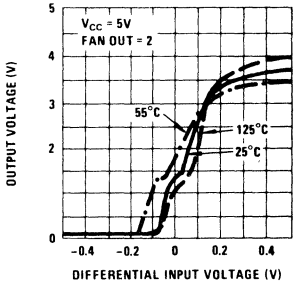
Internal Power Dissipation



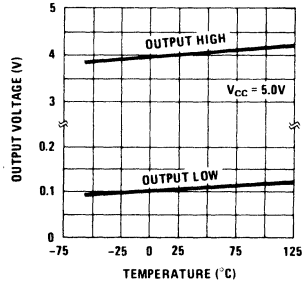
Threshold Voltage vs Supply Voltage



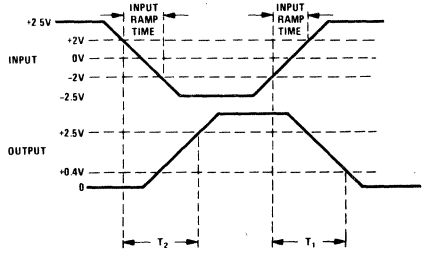
Transfer Function



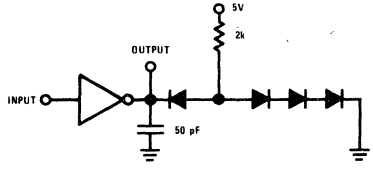
Output Voltage Levels



switching time waveforms



ac test circuit



NATIONAL

Line Drivers/Receivers

DS7830/DS8830 dual differential line driver

general description

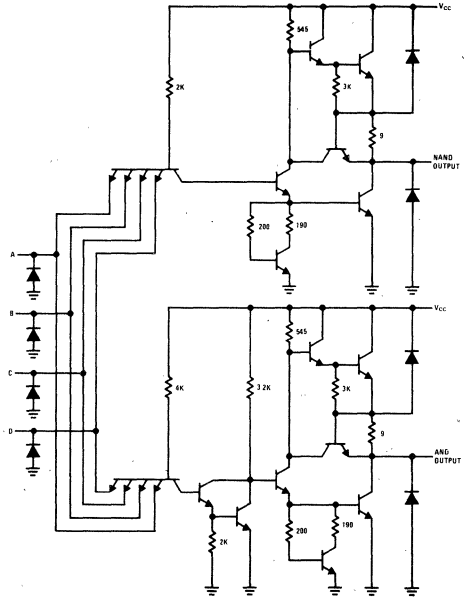
The DS7830/DS8830 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function.

TTL (Transistor-Transistor-Logic) multiple emitter inputs allow this line driver to interface with standard TTL or DTL systems. The differential outputs are balanced and are designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines with characteristic impedances of 50Ω to 500Ω. The differential feature of the output eliminates troublesome ground-loop errors normally associated with single-wire transmissions.

features

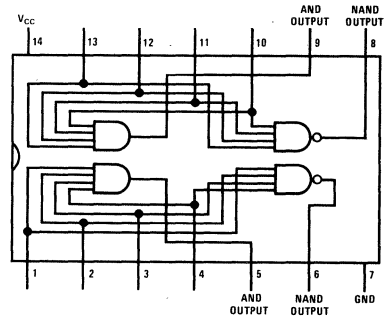
- Single 5 volt power supply
- Diode protected outputs for termination of positive and negative voltage transients
- Diode protected inputs to prevent line ringing
- High Speed
- Short Circuit Protection

schematic* and connection diagrams



*2 PER PACKAGE.

Dual-In-Line and Flat Package

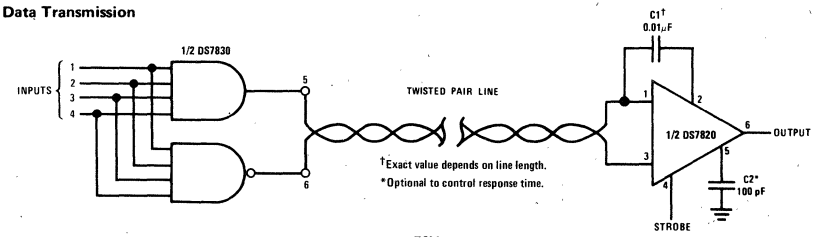


TOP VIEW

Order Number DS7830J or DS8830J
Order Number DS8830N
Order Number DS7830W or DS8830W

typical application

Digital Data Transmission



†Exact value depends on line length.
*Optional to control response time.

absolute maximum ratings (Note 1)

V_{CC}	7.0V
Input Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Output Short Circuit Duration (125°C)	1 second

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7830	4.5	5.5	V
DS8830	4.75	5.25	V
Temperature (T_A)			
DS7830	−55	+125	°C
DS8830	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.8V	I_{OUT} = −0.8 mA	2.4			V
			I_{OUT} = 40 mA	1.8	3.3		V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 2.0V	I_{OUT} = 32 mA		0.2	0.4	V
			I_{OUT} = 40 mA		0.22	0.5	V
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V				120	μA
		V_{IN} = 5.5V				2	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V				4.8	mA
I_{SC}	Output Short Circuit Current	V_{CC} = 5.0V, T_A = 125°C, (Note 4)		40	100	120	mA
I_{CC}	Supply Current	V_{IN} = 5.0V, (Each Driver)			11	18	mA

switching characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Propagation Delay AND Gate	T_A = 25°C, V_{CC} = 5.0V,		8	12	ns
t_{pd0}		C_L = 15 pF, *(Figure 1)*		11	18	ns
t_{pd1}	Propagation Delay NAND Gate	T_A = 25°C, V_{CC} = 5.0V,		8	12	ns
t_{pd0}		C_L = 15 pF, *(Figure 1)*		5	8	ns
t_1	Differential Delay	Load, 100Ω and 5000 pF, *(Figure 2)*		12	16	ns
t_2	Differential Delay	Load, 100Ω and 5000 pF, *(Figure 2)*		12	16	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7830 and across the 0°C to +70°C range for the DS8830. Typical values are for T_A = 25°C and V_{CC} = 5.0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

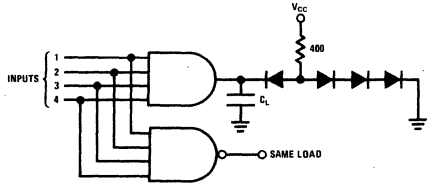


FIGURE 1.

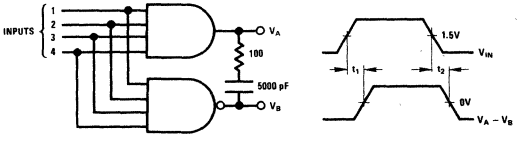
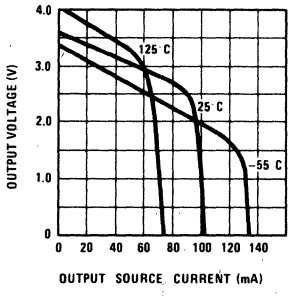


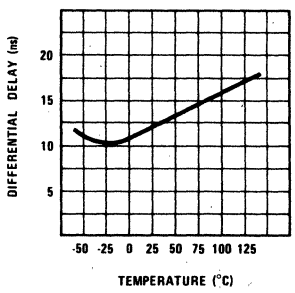
FIGURE 2.

typical performance characteristics

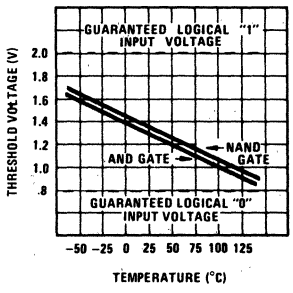
Output High Voltage (Logical "1") Vs Output Current



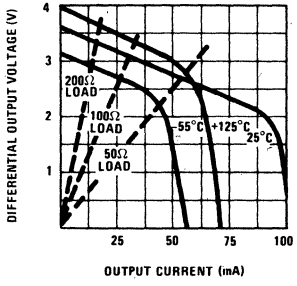
Differential Delay Vs Temperature



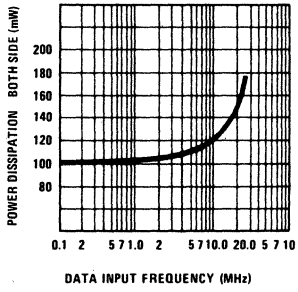
Threshold Voltage Vs Temperature



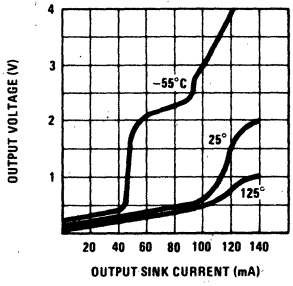
Differential Output Voltage ($|V_{AND} - V_{NAND}|$) Vs Differential Output Current



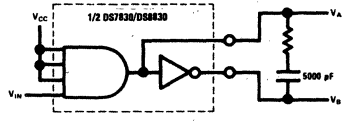
Power Dissipation (No Load) Vs Data Input Frequency



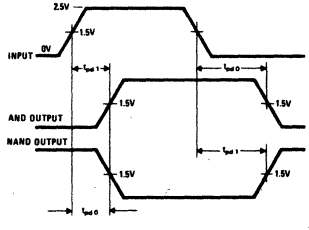
Output Low Voltage (Logical "0") Vs Output Current

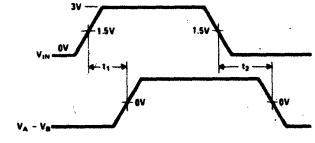


ac test circuit



switching time waveforms





Line Drivers/Receivers

DS7831/DS8831, DS7832/DS8832 TRI-STATE® line driver

general description

Through simple logic control, the DS7831/DS8831, DS7832/DS8832 can be used as either a quad single-ended line driver or a dual differential line driver. They are specifically designed for party line (bus-organized) systems. The DS7832/DS8832 does not have the V_{CC} clamp diodes found on the DS7831/DS8831.

The DS7831 and DS7832 are specified for operation over the −55°C to +125°C military temperature range. The DS8831 and DS8832 are specified for operation over the 0°C to +70°C temperature range.

features

- Series 54/74 compatible
- 17 ns propagation delay
- Very low output impedance—high drive capability
- 40 mA sink and source currents
- Gating control to allow either single-ended or differential operation
- High impedance output state which allows many outputs to be connected to a common bus line.

mode of operation

To operate as a quad single-ended line driver apply logical "0"s to the Output Disable pins (to keep the outputs in the normal low impedance mode) and apply logical "0"s to both Differential/Single-ended Mode Control inputs. All four channels will then operate independently and no signal inversion will occur between inputs and outputs.

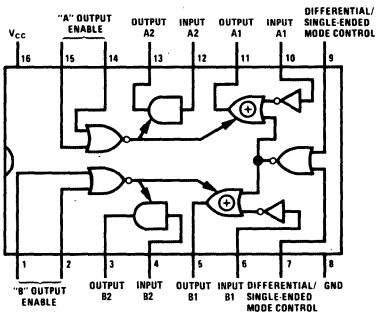
To operate as a dual differential line driver apply logical "0"s to the Output Disable pins and apply at least one logical "1" to the Differential/Single-ended Mode Control inputs. The inputs to the A channels should be connected together and the inputs to the B channels should be connected to- In this mode the signals applied to the resulting inputs will pass non-inverted on the A_2 and B_2 outputs and inverted on the A_1 and B_1 outputs.

When operating in a bus-organized system with outputs tied directly to outputs of other

(continued)

connection and logic diagram

Dual-In-Line Package



TOP VIEW

Order Number DS7831J, DS8831J, DS7832J, DS8832J, DS8831N, DS8832N, DS7831W, or DS7832W

truth table (Shown for A Channels Only)

"A" OUTPUT DISABLE		DIFFERENTIAL/ SINGLE-ENDED MODE CONTROL		INPUT A1	OUTPUT A1	INPUT A2	OUTPUT A2
0	0	0	0	Logical "1" or Logical "0"	Same as Input A1	Logical "1" or Logical "0"	Same as Input A2
0	0	X	1	Logical "1" or Logical "0"	Opposite of Input A1	Logical "1" or Logical "0"	Same as Input A2
		1	X				
1	X	X	X	X	High impedance state	X	High impedance state
X	1						

X = Don't Care

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Time that 2 bus-connected devices may be in opposite low impedance states simultaneously	∞

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7831, DS7832	4.5	5.5	V
DS8831, DS8832	4.75	5.25	V
Temperature (T_A)			
DS7831, DS7832	−55	+125	°C
DS8831, DS8832	0	+70	°C

electrical characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min			2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min					0.8	V
V_{OH}	Logical "1" Output Voltage	DS7831, DS7832	V_{CC} = Min	I_O = −40 mA	1.8	2.3		V
				I_O = −2 mA	2.4	2.7		V
		DS8831, DS8832		I_O = −40 mA	1.8	2.5		V
				I_O = −5.2 mA	2.4	2.9		V
V_{OL}	Logical "0" Output Voltage	DS7831, DS7832	V_{CC} = Min	I_O = 40 mA		0.29	0.50	V
				I_O = 32 mA			0.40	V
		DS8831, DS8832		I_O = 40 mA		0.29	0.50	V
				I_O = 32 mA			0.40	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	DS7831, DS7832, V_{IN} = 5.5V				1	mA
			DS8831, DS8832, V_{IN} = 2.4V				40	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	−1.6	mA
I_{OD}	Output Disable Current	V_{CC} = Max, V_O = 2.4V or 0.4V			−40		40	μA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, (Note 4)			−40	−100	−120	mA
I_{CC}	Supply Current	V_{CC} = Max				65	90	mA
V_{CLI}	Input Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA					−1.5	V
V_{CLO}	Output Diode Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C	I_{OUT} = −12 mA	DS7831/DS8831 DS7832/DS8832			−1.5	V
			I_{OUT} = 12 mA	DS7831/DS8831			V_{CC}+1.5	V

switching characteristics

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0" from Inputs A1, A2, B1, B2 Differential Single-ended Mode Control to Outputs	V_{CC} = 5.0V, T_A = 25°C		13	25	ns
t_{pd1}	Propagation Delay to a Logical "1" from Inputs A1, A2, B1, B2 Differential Single-ended Mode Control to Outputs	V_{CC} = 5.0V, T_A = 25°C		13	25	ns
t_{1H}	Delay from Disable Inputs to High Impedance State (from Logical "1" Level)	V_{CC} = 5.0V, T_A = 25°C		6	12	ns
t_{0H}	Delay from Disable Inputs to High Impedance State (from Logical "0" Level)	V_{CC} = 5.0V, T_A = 25°C		14	22	ns
t_{H1}	Propagation Delay from Disable Inputs to Logical "1" Level (from High Impedance State)	V_{CC} = 5.0V, T_A = 25°C		14	22	ns
t_{H0}	Propagation Delay from Disable Inputs to Logical "0" Level (from High Impedance State)	V_{CC} = 5.0V, T_A = 25°C		18	27	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7831 and DS7832 and across the 0°C to +70°C range for the DS8831 and DS8832. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Applies for T_A = 125°C only. Only one output should be shorted at a time.

mode of operation (cont.)

DS7831/DS8831's, DS7832/DS8832's *(Figure 1)*, all devices except one must be placed in the "high impedance" state. This is accomplished by ensuring that a logical "1" is applied to at least one of the Output Disable pins of each device which is to be in the "high impedance" state. A NOR gate was purposely chosen for this function since it is possible with only two DM5442/DM7442, BCD-to-decimal decoders, to decode as many as 100 DS7831/DS8831's, DS7832/DS8832's *(Figure 2)*.

The unique device whose Disable inputs receive two logical "0" levels assumes the normal low impedance output state, providing good capacitive drive capability and waveform integrity especially during the transition from the logical "0" to logical "1" state. The other outputs—in the high impedance state—take only a small amount of leakage current from the low impedance outputs. Since the logical "1" output current from the selected device is 100 times that of a conventional Series 54/74 device (40 mA vs. 400 μA), the output is easily able to supply that leakage current for several hundred other DS7831/DS8831's, DS7832/DS8832's and still have available drive for the bus line *(Figure 3)*.

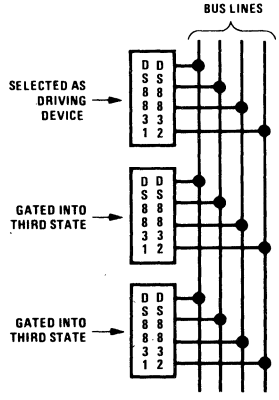


Figure 1

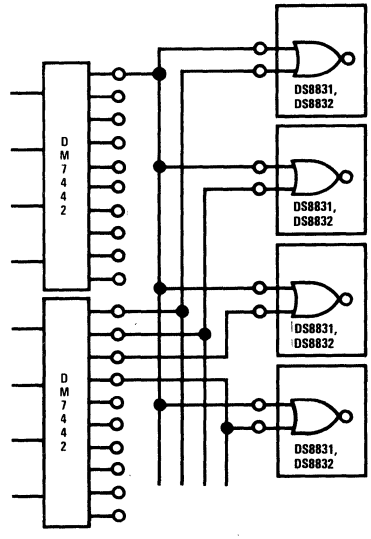


Figure 2

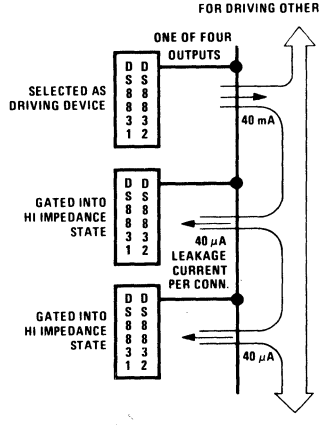
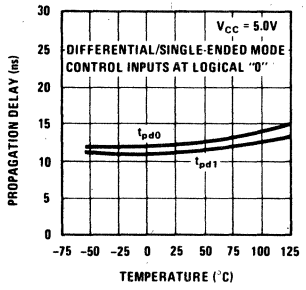


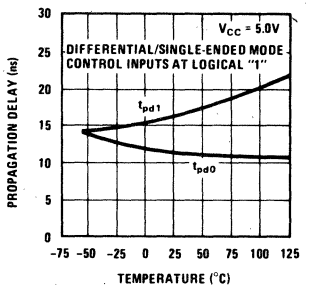
Figure 3

typical performance characteristics

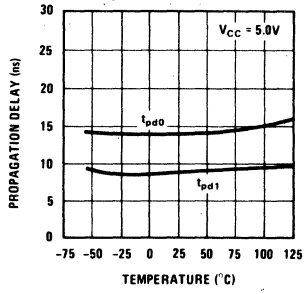
Propagation Delay from Input to Output (Channel 1)



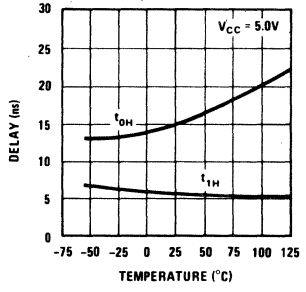
Propagation Delay from Input to Output (Channel 1)



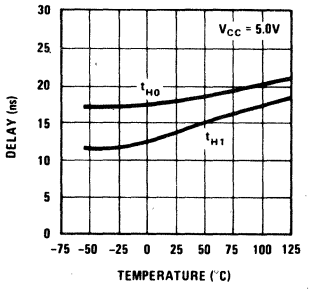
Propagation Delay from Input to Output (Channel 2)



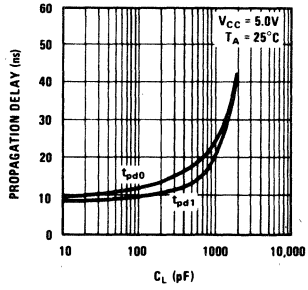
Delay from Disable to High Impedance State



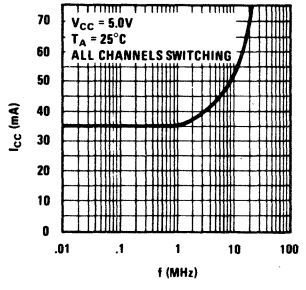
Delay from Disable to Low Impedance State



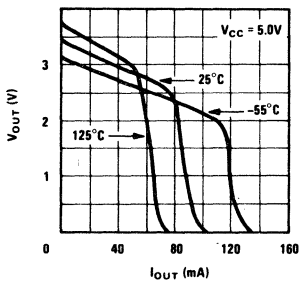
Propagation Delay vs Load Capacitance



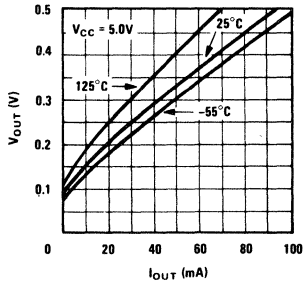
Total Supply Current vs Frequency



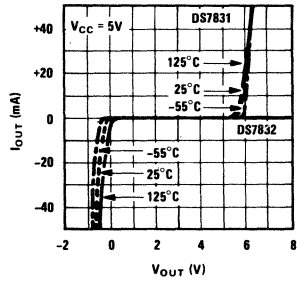
Logical "1" Output Voltage vs Source Current



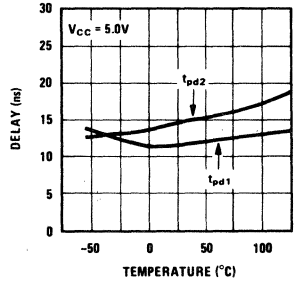
Logical "0" Output Voltage vs Sink Current

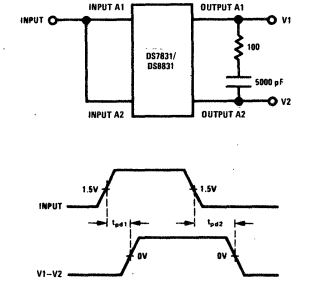


I_{OUT} vs V_{OUT} High Impedance Output State

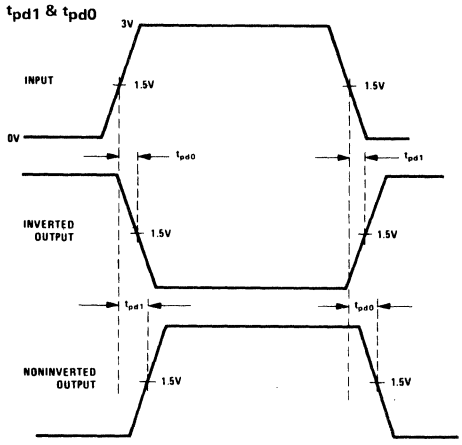


Propagation Delay in Differential Mode



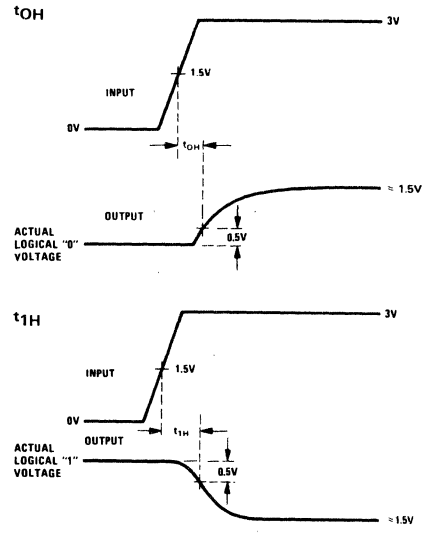


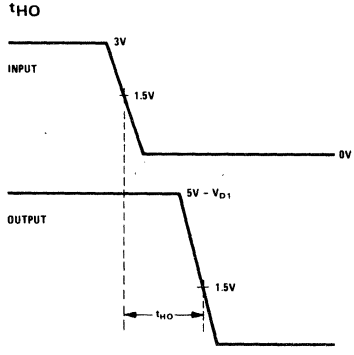
switching time waveforms

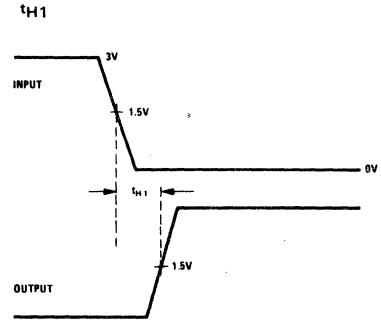


Input characteristic:

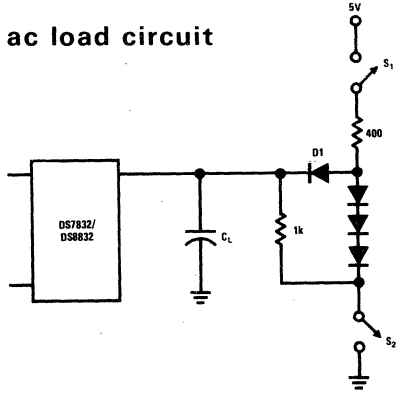
Amplitude = 3.0V
Frequency = 1.0 MHz, 50% duty cycle
$t_r = t_f \leq 10$ ns (10% to 90%)







ac load circuit



	Switch S1	Switch S2	C_L
t_{pd1}	closed	closed	50 pF
t_{pd0}	closed	closed	50 pF
t_{0H}	closed	closed	* 5 pF
t_{1H}	closed	closed	* 5 pF
t_{H0}	closed	open	50 pF
t_{H1}	open	closed	50 pF

*Jig capacitance.

NATIONAL

Line Drivers/Receivers

DS7833/DS8833, DS7835/DS8835 quad TRI-STATE® party line transceivers

general description

This family of TRI-STATE Party Line Transceivers offer extreme versatility in bus organized data transmission systems. The data bus may be unterminated, or terminated dc or ac, at one or both ends. Drivers in the third (high impedance) state load the data bus with a negligible leakage current. The receiver input current is low allowing at least 100 driver/receiver pairs to utilize a single bus. The bus loading is unchanged when V_{CC} = 0V. The receiver incorporates hysteresis to provide greater noise immunity. All devices utilize a high current TRI-STATE output driver. The DS7833/DS8833 and DS7835/DS8835 employ TRI-STATE outputs on the receiver also.

The DS7833/DS8833 are non-inverting quad transceivers with a common inverter driver disable control and a common inverter receiver disable control.

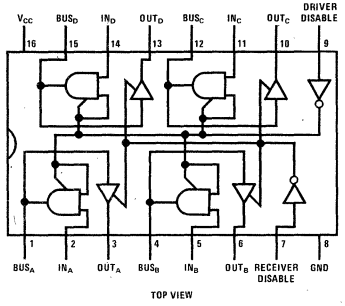
The DS7835/DS8835 are inverting quad transceivers with a common inverter driver disable control and a common inverter receiver disable control.

features

- Receiver hysteresis — 400 mV typ
- Receiver noise immunity — 1.4V typ
- Bus terminal current for normal V_{CC} or V_{CC} = 0V — 80μA max
- Receivers
  - Sink — 16 mA at 0.4V max
  - Source — 2.0 mA (Mil) at 2.4V min; 5.2 mA (Com) at 2.4V min
- Drivers
  - Sink — 50 mA at 0.5V max; 32 mA at 0.4V max
  - Source — 10.4 mA (Com) at 2.4V min; 5.2 mA (Mil) at 2.4V min
- Drivers have TRI-STATE outputs
- DS7833/DS8833, DS7835/DS8835 receivers have TRI-STATE outputs
- Capable of driving 100Ω dc–terminated buses
- Compatible with Series 54/74

connection diagrams

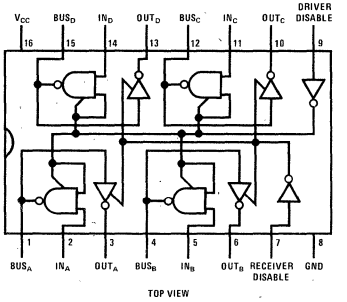
Dual-In-Line and Flat Package



TOP VIEW

Order Number DS7833J, DS8833J, DS8833N or DS7833W

Dual-In-Line and Flat Package



TOP VIEW

Order Number DS7835J, DS8835J, DS8835N or DS7835W

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7833, DS7835	4.5	5.5	V
DS8833, DS8835	4.75	5.25	V
Temperature (T_A)			
DS7833, DS7835	−55	+125	°C
DS8833, DS8835	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
DISABLE/DRIVER INPUT								
V_{IH}	High Level Input Voltage	V_{CC} = Min			2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min					0.8	V
I_{IH}	High Level Input Current	V_{CC} = Max	V_{IN} = 2.4V				40	μA
			V_{IN} = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	−1.6	mA
V_{CL}	Input Clamp Diode	V_{CC} = 5.0V, I_{IN} = −12 mA, T_A = 25°C				−0.8	−1.5	V
I_{IT}	Driver Low Level Disabled Input Current	Driver Disable Input = 2.0V, V_{IN} = 0.4V					−40	μA
RECEIVER INPUT/BUS OUTPUT								
V_{TH}	High Level Threshold Voltage			DS7833, DS7835	1.4	1.75	2.1	V
				DS8833, DS8835	1.5	1.75	2.0	V
V_{TL}	Low Level Threshold Voltage			DS7833, DS7835	0.8	1.35	1.6	V
				DS8833, DS8835	0.8	1.35	1.5	V
I_B	Bus Current, Output Disabled or High	V_{BUS} = 4.0V	V_{CC} = Max			25	80	μA
			V_{CC} = 0V			5.0	80	μA
		V_{CC} = Max, V_{BUS} = 0.4V				−2.0	−40	μA
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −5.2 mA	DS7833, DS7835	2.4	2.75		V
			I_{OUT} = −10.4 mA	DS8833, DS8835	2.4	2.75		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min	I_{OUT} = 50 mA			0.28	0.5	V
			I_{OUT} = 32 mA				0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)			−40	−62	−120	mA
RECEIVER OUTPUT								
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −2.0 mA	DS7833, DS7835	2.4	3.0		V
			I_{OUT} = −5.2 mA	DS8833, DS8835	2.4	2.9		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA				0.22	0.4	V
I_{OT}	Output Disabled Current	V_{CC} = Max, Disable Inputs = 2.0V	V_{OUT} = 2.4V				40	μA
			V_{OUT} = 0.4V				−40	μA
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)		DS7833, DS7835	−28	−40	−70	mA
				DS8833, DS8835	−30		−70	mA
I_{CC}	Supply Current	V_{CC} = Max				75	95	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7833, DS7835 and across the 0°C to +70°C range for the DS8833, DS8835. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

switching characteristics V_{CC} = 5.0V, T_A = 25°C

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logic "0" From Input to Bus	*(Figure 1)*	DS7833/DS8833		14	30	ns
			DS7835/DS8835		10	20	ns
t_{pd1}	Propagation Delay to a Logic "1" From Input to Bus	*(Figure 1)*	DS7833/DS8833		14	30	ns
			DS7835/DS8835		11	30	ns
t_{pd0}	Propagation Delay to a Logic "0" From Bus to Output	*(Figure 2)*	DS7833/DS8833		24	45	ns
			DS7835/DS8835		16	35	ns
t_{pd1}	Propagation Delay to a Logic "1" From Bus to Output	*(Figure 2)*	DS7833/DS8833		12	30	ns
			DS7835/DS8835		18	30	ns
t_{1H}	Delay From Disable Input to High Impedance State (From Logic "1" Level)	C_L = 5.0 pF, *(Figures 1 and 2)*	Driver		8.0	20	ns
			Receiver		6.0	15	ns
t_{0H}	Delay From Disable Input to High Impedance State (From Logic "0" Level)	C_L = 5.0 pF, *(Figures 1 and 2)*	Driver		20	35	ns
			Receiver		13	25	ns
t_{H1}	Delay From Disable Input to Logic "1" Level (From High Impedance State)	C_L = 50 pF, *(Figures 1 and 2)*	Driver		24	40	ns
			Receiver		16	35	ns
t_{H0}	Delay From Disable Input to Logic "0" Level (From High Impedance State)	C_L = 50 pF, *(Figures 1 and 2)*	Driver		19	35	ns
			Receiver DS7833		15	30	ns
			Receiver DS7835		33	50	ns
f_{MAX}	Maximum Clock Frequency						

ac test circuits

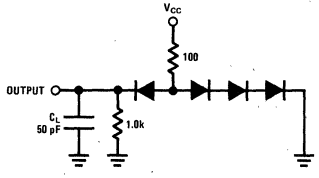


FIGURE 1. Driver Output Load

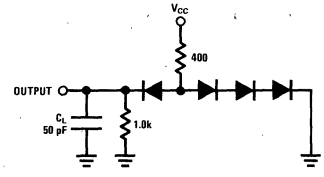
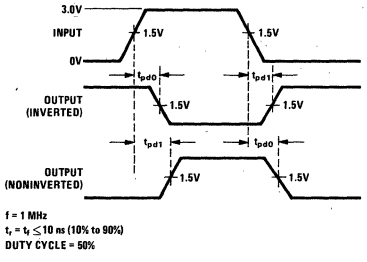


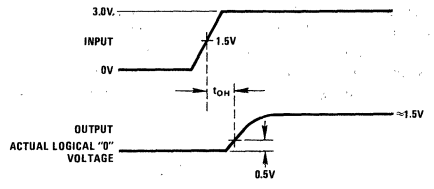
FIGURE 2. Receiver Output Load

switching time waveforms

t_{pd1} & t_{pd0}

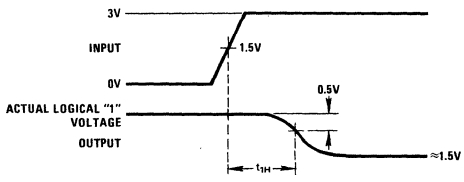


t_{0H}

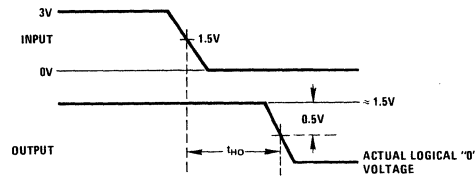


switching time waveforms (con't)

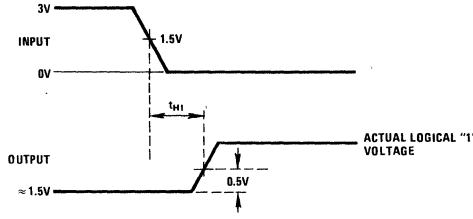
t_{1H}



t_{H0}



t_{H1}



NATIONAL

Line Drivers/Receivers

DS7834/DS8834, DS7839/DS8839 quad TRI-STATE® party line transceivers

general description

This family of TRI-STATE party line transceivers offer extreme versatility in bus organized data transmission systems. The data bus may be unterminated, or terminated dc or ac, at one or both ends. Drivers in the third (high impedance) state load the data bus with a negligible leakage current. The receiver input current is low allowing at least 100 driver/receiver pairs to utilize a single bus. The bus loading is unchanged when V_{CC} = 0V. The receiver incorporates hysteresis to provide greater noise immunity. Both devices utilize a high current TRI-STATE output driver. The DS7834/DS8834 and DS7839/DS8839 employ TTL outputs on the receiver.

The DS7839/DS8839 are non-inverting quad transceivers with two common inverter driver disable controls.

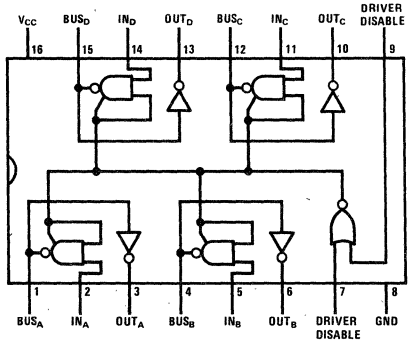
The DS7834/DS8834 are inverting quad transceivers with two common inverter driver disable controls.

features

- Receiver hysteresis — 400 mV typ
- Receiver noise immunity — 1.4V typ
- Bus terminal current for normal V_{CC} or V_{CC} = 0V — 80μA max
- Receivers
  - Sink — 16 mA at 0.4V max
  - Source — 2.0 mA (Mil) at 2.4V min; 5.2 mA (Com) at 2.4V min
- Drivers
  - Sink — 50 mA at 0.5V max; 32 mA at 0.4V max
  - Source — 10.4 mA (Com) at 2.4V min; 5.2 mA (Mil) at 2.4V min
- Drivers have TRI-STATE outputs
- Receivers have TRI-STATE outputs
- Capable of driving 100Ω dc–terminated buses
- Compatible with Series 54/74

connection diagrams

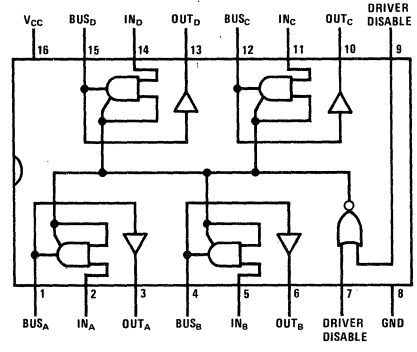
Dual-In-Line and Flat Package



TOP VIEW

Order Number DS7834J, DS8834J DS8843N or DS7834W

Dual-In-Line and Flat Package



TOP VIEW

Order Number DS7839J, DS8839J, DS8839N or DS7839W

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 Seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7834, DS7839	4.5	5.5	V
DS8834, DS8839	4.75	5.25	V
Temperature (T_A)			
DS7834, DS7839	−55	+125	°C
DS8834, DS8839	0	+70	°C

dc electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
DISABLE/DRIVER INPUT								
V_{IH}	High Level Input Voltage	V_{CC} = Min			2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = Min					0.8	V
I_{IH}	High Level Input Current	V_{CC} = Max	V_{IN} = 2.4V				40	μA
			V_{IN} = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.0	−1.6	mA
I_{IND}	Driver Disabled Input Low Current	Driver Disable Input = 2.0V, V_{IN} = 0.4V					−40	μA
V_{CL}	Input Clamp Diode	V_{CC} = 5.0V, I_{IN} = −12 mA, T_A = 25°C				−0.8	−1.5	V
RECEIVER INPUT/BUS OUTPUT								
V_{TH}	High Level Threshold Voltage			DS7834, DS7839	1.4	1.75	2.1	V
				DS8834, DS8839	1.5	1.75	2.0	V
V_{TL}	Low Level Threshold Voltage			DS7834, DS7839	0.8	1.35	1.6	V
				DS8834, DS8839	0.8	1.35	1.5	V
I_{BH}	Bus Current, Output Disabled or High	V_{BUS} = 4.0V	V_{CC} = Max, Disable Input = 2.0V			25	80	μA
			V_{CC} = 0V			5.0	80	μA
		V_{CC} = Max, V_{BUS} = 0.4V, Disable Input = 2.0V					−40	μA
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −5.2 mA	DS7834, DS7839	2.4	2.75		V
			I_{OUT} = −10.4 mA	DS7834, DS8839	2.4	2.75		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min	I_{OUT} = 50 mA			0.28	0.5	V
			I_{OUT} = 32 mA				0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)			−40	−62	−120	mA
RECEIVER OUTPUT								
V_{OH}	Logic "1" Output Voltage	V_{CC} = Min	I_{OUT} = −2.0 mA	DS7834, DS7839	2.4	3.0		V
			I_{OUT} = −5.2 mA	DS8834, DS8839	2.4	2.9		V
V_{OL}	Logic "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA				0.22	0.4	V
I_{OS}	Output Short Circuit Current	V_{CC} = Max, (Note 4)		DS7834, DS7839	−28	−40	−70	mA
				DS8834, DS8839	−30		−70	mA
I_{CC}	Supply Current	V_{CC} = Max				75	95	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7834, DS7839 and across the 0°C to +70°C range for the DS8834, DS8839. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

ac electrical characteristics V_{CC} = 5.0V, T_A = 25°C

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logic "0" from Input to Bus	*(Figure 1)*	DS7839/DS8839		14	30	ns
			DS7834/DS8834		10	20	ns
t_{pd1}	Propagation Delay to a Logic "1" from Input to Bus	*(Figure 1)*	DS7839/DS8839		14	30	ns
			DS7834/DS8834		11	30	ns
t_{pd0}	Propagation Delay to a Logic "0" from Bus to Output	*(Figure 2)*	DS7839/DS8839		24	45	ns
			DS7834/DS8834		16	35	ns
t_{pd1}	Propagation Delay to a Logic "1" from Bus to Output	*(Figure 2)*	DS7839/DS8839		12	30	ns
			DS7834/DS8834		18	30	ns
t_{1H}	Delay from Disable Input to High Impedance State (from Logic "1" Level)	C_L = 5.0 pF, *(Figures 1 and 2)*	Driver Only		8	20	ns
t_{0H}	Delay from Disable Input to High Impedance State (from Logic "0" Level)	C_L = 5.0 pF, *(Figures 1 and 2)*	Driver Only		20	35	ns
t_{H1}	Delay from Disable Input to Logic "1" Level (from High Impedance State)	C_L = 50 pF, *(Figures 1 and 2)*	Driver Only		24	40	ns
t_{H0}	Delay from Disable Input to Logic "0" Level (from High Impedance State)	C_L = 50 pF, *(Figures 1 and 2)*	Driver Only		19	35	ns

ac test circuits

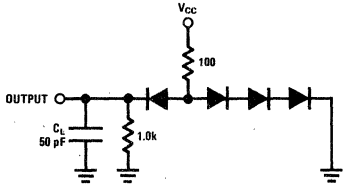


FIGURE 1. Driver Output Load

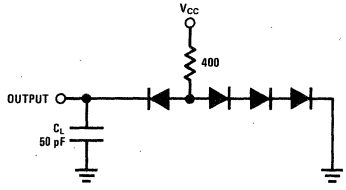
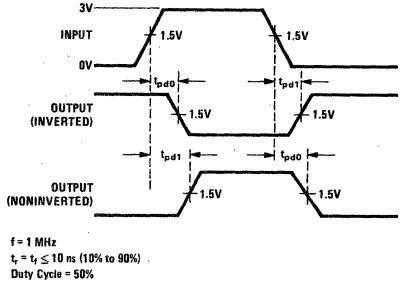


FIGURE 2. Receiver Output Load

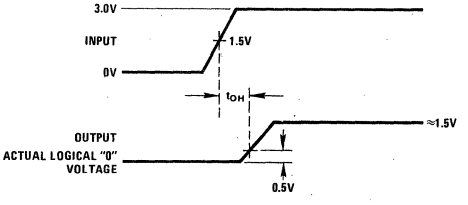
switching time waveforms

t_{pd1} and t_{pd0}



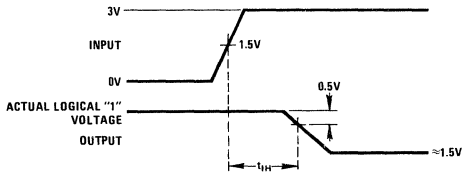
f = 1 MHz
$t_r = t_f \leq 10$ ns (10% to 90%)
Duty Cycle = 50%

t_{0H}

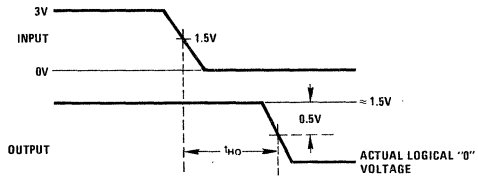


switching time waveforms (con't)

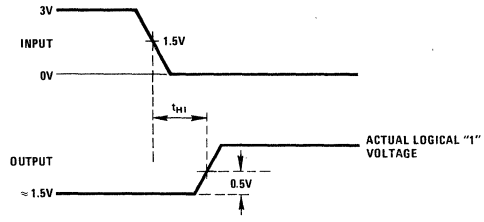
t_{1H}



t_{H0}



t_{H1}



3

NATIONAL

Line Drivers/Receivers

DS7836/DS8836 quad NOR unified bus receiver

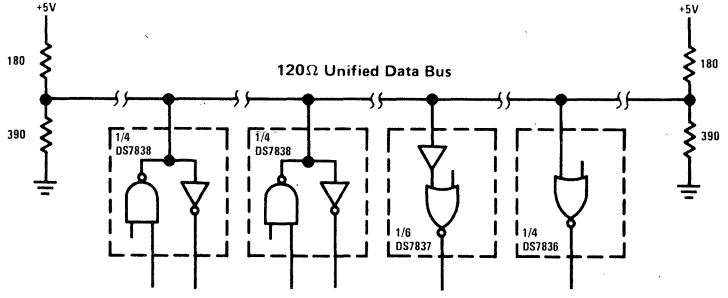
general description

The DS7836/DS8836 are quad 2-input receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The design employs a built-in input hysteresis providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus. This receiver has been specifically configured to replace the SP380 gate pin-for-pin to provide the distinct advantages of the DS7837 receiver with built-in hysteresis in existing systems. Performance is optimized for systems with bus rise and fall times $\leq 1.0\mu s/V$.

features

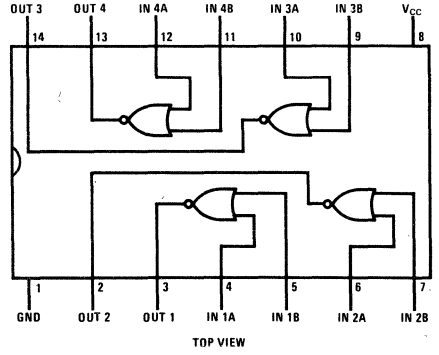
- Low input current with normal V_{CC} or V_{CC} = 0V (15 μA typ)
- Built-in input hysteresis (1V typ)
- High noise immunity (2V typ)
- Temperature-insensitive input thresholds track bus logic levels
- DTL/TTL compatible output
- Matched, optimized noise immunity for "1" and "0" levels
- High speed (18 ns typ)

typical application



connection diagram

Dual-In-Line and Flat Package



TOP VIEW

Order Number DS7836J or DS8836J Order Number DS8836N Order Number DS7836W

absolute maximum ratings

Supply Voltage	7.0V
Current Voltage	5.5V
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7836	4.5	5.5	V
DS8836	4.75	5.25	V
Temperature (T_A)			
DS7836	−55	+125	°C
DS8836	0	+70	°C

electrical characteristics

The following apply for $V_{MIN} \leq V_{CC} \leq V_{MAX}$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	High Level Input Threshold	DS7836		1.65	2.25	2.65	V
		DS8836		1.80	2.25	2.50	V
V_{IL}	Low Level Input Threshold	DS7836		0.97	1.30	1.63	V
		DS8836		1.05	1.30	1.55	V
I_{IN}	Maximum Input Current	V_{IN} = 4V	V_{CC} = Max		15	50	μA
			V_{CC} = 0V		1	50	μA
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.5V, I_{OUT} = −400μA		2.4			V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 4V, I_{OUT} = 16 mA			0.25	0.4	V
I_{SC}	Output Short Circuit Current	V_{IN} = 0.5V, V_{OUT} = 0V, V_{CC} = Max, (Note 4)		−18		−55	mA
I_{CC}	Power Supply Current	V_{IN} = 4V, (Per Package)			25	40	mA
V_{CL}	Input Clamp Diode Voltage	I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

switching characteristics

V_{CC} = 5V, T_A = 25°C unless otherwise specified.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd}	Propagation Delays	(Notes 4 and 5)	Input to Logical "1" Output		20	30	ns
			Input to Logical "0" Output		18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7836 and across the 0°C to +70°C range for the DS8836. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Fan-out of 10 load, C_{LOAD} = 15 pF total, measured from V_{IN} = 1.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 5: Fan-out of 10 load, C_{LOAD} = 15 pF total, measured from V_{IN} = 2.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

NATIONAL

Line Drivers/Receivers

DS7837/DS8837 hex unified bus receiver

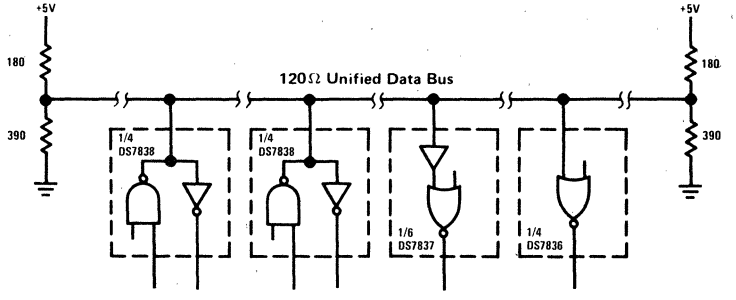
general description

The DS7837/DS8837 are high speed receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The receiver design employs a built-in input hysteresis providing substantial noise immunity. Low input current allows up to 27 driver/receiver pairs to utilize a common bus. Disable inputs provide time discrimination. Disable inputs and receiver outputs are DTL/TTL compatible. Performance is optimized for systems with bus rise and fall times $\leq$ 1.0μs/V.

features

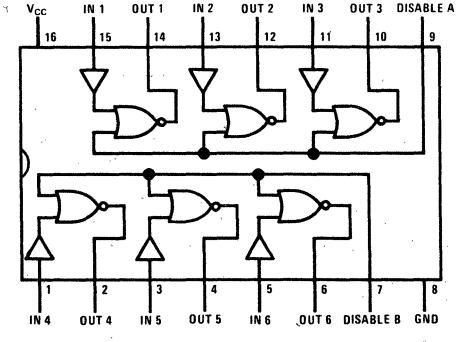
- Low receiver input current for normal V_{CC} or V_{CC} = 0V (15 μA typ)
- Six separate receivers per package
- Built-in receiver input hysteresis (1V typ)
- High receiver noise immunity (2V typ)
- Temperature insensitive receiver input thresholds track bus logic levels
- DTL/TTL compatible disable and output
- Molded or cavity dual-in-line or flat package
- High speed

typical application



connection diagram

Dual-In-Line and Flat Package



TOP VIEW

Order Number DS7837J or DS8837J **Order Number DS8837N** **Order Number DS7837W**

absolute maximum ratings

Supply Voltage	7V
Input Voltage	5.5V
Power Dissipation	600 mW
Operating Temperature Range	
DS7837	−55°C to +125°C
DS8837	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7837	4.5	5.5	V
DS8837	4.75	5.25	V
Temperature (T_A)			
DS7837	−55	+125	°C
DS8837	0	+70	°C

electrical characteristics

The following apply for $V_{MIN} \leq V_{CC} \leq V_{MAX}$, $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	High Level Receiver Threshold		DS7837	1.65	2.25	2.65	V
			DS8837	1.80	2.25	2.50	V
V_{TL}	Low Level Receiver Threshold		DS7837	0.97	1.30	1.63	V
			DS8837	1.05	1.30	1.55	V
I_{IH}	Maximum Receiver Input Current	V_{IN} = 4V	$V_{CC} = V_{MAX}$		15.0	50.0	μA
			V_{CC} = 0V		1.0	50.0	μA
I_{IL}	Logical "0" Receiver Input Current	V_{IN} = 0.4V, $V_{CC} = V_{MAX}$			1.0	50.0	μA
V_{IH}	Logical "1" Input Voltage		Disable	2.0			V
V_{IL}	Logical "0" Input Voltage		Disable			0.8	V
I_{IH}	Logical "1" Input Current	Disable Input	V_{IND} = 2.4V			80.0	μA
			V_{IND} = 5.5V			2.0	mA
I_{IL}	Logical "0" Input Current	V_{IN} = 4V, V_{IND} = 0.4V, Disable Input				−3.2	mA
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.5V, V_{IND} = 0.8V, I_{OH} = −400μA		2.4			V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 4V, V_{IND} = 0.8V, I_{OL} = 16 mA			0.25	0.4	V
I_{OS}	Output Short Circuit Current	V_{IN} = 0.5V, V_{IND} = 0V, V_{OS} = 0V, $V_{CC} = V_{MAX}$, (Note 4)		−18.0		−55.0	mA
I_{CC}	Power Supply Current	V_{IN} = 4V, V_{IND} = 0V, (Per Package)			45.0	60.0	mA
V_{CL}	Input Clamp Diode	V_{IN} = −12 mA, V_{IND} = −12 mA, T_A = 25°C			−1.0	−1.5	V

switching characteristics

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd}	Propagation Delays	V_{IND} = 0V, Receiver	Input to Logical "1" Output, (Note 5)		20	30	ns
			Input to Logical "0" Output, (Note 6)		18	30	ns
		V_{IN} = 0V, Disable, (Note 7)	Input to Logical "1" Output		9	15	ns
			Input to Logical "0" Output		4	10	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7837 and across the 0°C to +70°C range for the DS8837. All typicals values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positve, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 6: Fan-out of 10 load, C_{LOAD} =15 pF total. Measured from V_{IN} = 2.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

Note 7: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.5V to V_{OUT} = 1.5V, V_{IN} = 0V to 3V pulse.

NATIONAL

Line Drivers /Receivers

DS7838/DS8838 quad unified bus transceiver

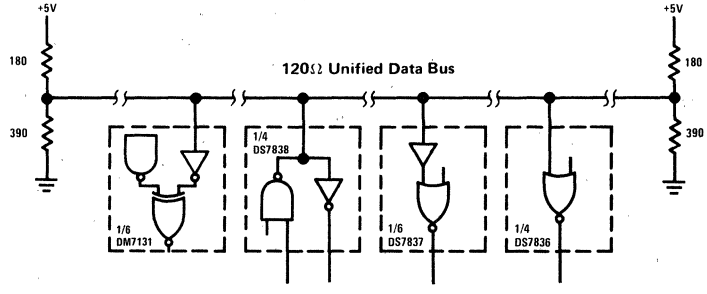
general description

The DS7838/DS8838 are quad high speed drivers/receivers designed for use in bus organized data transmission systems interconnected by terminated 120Ω impedance lines. The external termination is intended to be a 180Ω resistor from the bus to the +5V logic supply together with a 390Ω resistor from the bus to ground. The bus can be terminated at one or both ends. Low bus pin current allows up to 27 driver/receiver pairs to utilize a common bus. The bus loading is unchanged when V_{CC} = 0V. The receivers incorporate hysteresis to greatly enhance bus noise immunity. One two-input NOR gate is included to disable all drivers in a package simultaneously. Receiver performance is optimized for systems with bus rise and fall times $\leq$ 1.0μs/V.

features

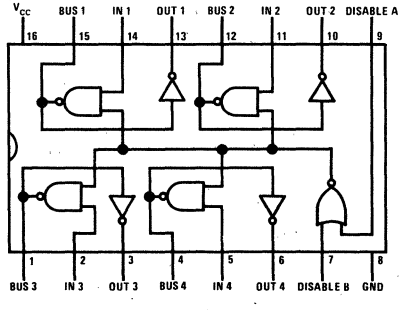
- 4 totally separate driver/receiver pairs per package
- 1V typical receiver input hysteresis
- Receiver hysteresis independent of receiver output load
- Guaranteed minimum bus noise immunity of 1.3V, 2V typ.
- Temperature-insensitive receiver thresholds track bus logic levels
- 20μA typical bus terminal current with normal V_{CC} or with V_{CC} = 0V
- Open collector driver output allows wire-OR connection
- High speed
- Series 74 TTL compatible driver and disable inputs and receiver outputs

typical application



connection diagram

Dual In-Line and Flat Package



TOP VIEW

Order Number DS7838J or DS8838J **Order Number DS8838N** **Order Number DS7838W**

absolute maximum ratings (Note 1)

Supply Voltage	7V	Operating Temperature Range	
Input and Output Voltage	5.5V	DS7838	−55°C to +125°C
Power Dissipation	600 mW	DS8838	0°C to +70°C
		Storage Temperature Range	−65°C to +150°C
		Lead Temperature, (Soldering, 10 sec)	300°C

electrical characteristics

DS7838/DS8838: The following apply for $V_{MIN} \leq V_{CC} \leq V_{MAX}$, $T_{MIN} \leq T_A \leq T_{MAX}$ unless otherwise specified (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER AND DISABLE INPUTS							
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_I	Logical "1" Input Current	V_{IN} = 5.5V				1	mA
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V				40	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V				−1.6	mA
V_{CL}	Input Diode Clamp Voltage	I_{DIS} = −12 mA, I_{IN} = −12 mA, I_{BUS} = −12 mA, T_A = 25°C			−1	−1.5	V
DRIVER OUTPUT/RECEIVER INPUT							
V_{OLB}	Low Level Bus Voltage	V_{DIS} = 0.8V, V_{IN} = 2V, I_{BUS} = 50 mA			0.4	0.7	V
I_{IHB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4V, V_{CC} = V_{MAX}			20	100	μA
I_{ILB}	Maximum Bus Current	V_{IN} = 0.8V, V_{BUS} = 4V, V_{CC} = 0V			2	100	μA
V_{IH}	High Level Receiver Threshold	V_{IND} = 0.8V, V_{OL} = 16 mA	DS7838	1.65	2.25	2.65	V
			DS8838	1.80	2.25	2.50	V
V_{IL}	Low Level Receiver Threshold	V_{IND} = 0.8V, V_{OH} = −400μA	DS7838	0.97	1.30	1.63	V
			DS8838	1.05	1.30	1.55	V
RECEIVER OUTPUT							
V_{OH}	Logical "1" Output Voltage	V_{IN} = 0.8V, V_{BUS} = 0.5V, I_{OH} = −400μA		2.4			V
V_{OL}	Logical "0" Output Voltage	V_{IN} = 0.8V, V_{BUS} = 4V, I_{OL} = 16 mA			0.25	0.4	V
I_{OS}	Output Short Circuit Current	V_{DIS} = 0.8V, V_{IN} = 0.8V, V_{BUS} = 0.5V, V_{OS} = 0V, V_{CC} = V_{MAX}, (Note 4)		−18		−55	mA
I_{CC}	Supply Current	V_{DIS} = 0V, V_{IN} = 2V, (Per Package)			50	70	mA
t_{pd}	Propagation Delays (Note 8)						
	Disable to Bus "1"	(Note 5)			19	30	ns
	Disable to Bus "0"	(Note 5)			15	23	ns
	Driver Input to Bus "1"	(Note 5)			17	25	ns
	Driver Input to Bus "0"	(Note 5)			9	15	ns
	Bus to Logical "1" Reciever Output	(Note 6)			20	30	ns
	Bus to Logical "0" Receiver Output	(Note 7)			18	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7838 and across the 0°C to +70°C range for the DS8838. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: 91Ω from bus pin to V_{CC} and 200Ω from bus pin to ground, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.5V to V_{BUS} = 1.5V, V_{IN} = 0V to 3.0V pulse.

Note 6: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 1.3V to V_{OUT} = 1.5V, V_{IN} = 0V to 3.0V pulse.

Note 7: Fan-out of 10 load, C_{LOAD} = 15 pF total. Measured from V_{IN} = 2.3V to V_{OUT} = 1.5V V_{IN} = 0V to 3.0V pulse.

Note 8: These apply for V_{CC} = 5V, T_A = 25°C unless otherwise specified.

NATIONAL

Line Drivers/Receivers

DS55107/DS75107, DS55108/DS75108, DS1603/DS3603, DS75207, DS75208, DS3604 dual line receivers

general description

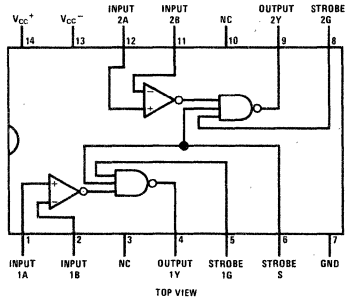
The nine products described herein are TTL compatible dual high speed circuits intended for sensing in a broad range of system applications. While the primary usage will be for line receivers or MOS sensing, any of the products may effectively be used as voltage comparators, level translators, window detectors, transducer preamplifiers, and in other sensing applications. As digital line receivers the products are applicable with the DS55109/DS75109 and DS55110/DS75110 companion drivers, or may be used in other balanced or unbalanced party-line data transmission systems. The improved input sensitivity and delay specifications of the DS75207, DS75208 and DS3604 make them ideal for sensing high performance MOS memories as well as high sensitivity line receivers and voltage comparators. TRI-STATE® products enhance bused organizations.

features

- Diode protected input stage for power "OFF" condition
- 17 ns typ high speed
- TTL compatible
- ±10 mV or ±25 mV input sensitivity
- ±3V input common-mode range
- High input impedance with normal V_{CC}, or $V_{CC} = 0V$
- Strobes for channel selection
- TRI-STATE outputs for high speed buses
- Dual circuits
- Sensitivity gntd. over full common-mode range
- Logic input clamp diodes—meets both "A" and "B" version specifications
- ±5V standard supply voltages

connection diagrams

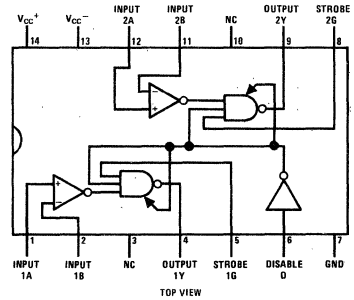
Dual-In-Line Package



TOP VIEW

Order Number DS55107J, DS75107J, DS55108J, DS75108J, DS75207J or DS75208J
Order Number DS75107N, DS75108N, DS75207N or DS75208N
Order Number DS55107W or DS55108W

Dual-In-Line Package



TOP VIEW

Order Number DS1603J, DS3603J DS3604J or DS1603W
Order Number DS3603N or DS3604N

product selection guide

TEMPERATURE→ / PACKAGE→	$-55°C \leq T_A \leq +125°C$ CAVITY DIP	$0°C \leq T_A \leq +70°C$ CAVITY OR MOLDED DIP	
INPUT SENSITIVITY→ / OUTPUT LOGIC↓	±25 mV	±25 mV	±10 mV
TTL Active Pull-up	DS55107	DS75107	DS75207
TTL Open Collector	DS55108	DS75108	DS75208
TTL TRI-STATE	DS1603	DS3603	DS3604

absolute maximum ratings (Notes 1, 2 and 3)

Supply Voltage, V_{CC}^+	7V	Strobe Input Voltage	5.5V
Supply Voltage, V_{CC}^-	−7V	Storage Temperature Range	−65°C to +150°C
Differential Input Voltage	±6V	Power Dissipation	600 mW
Common Mode Input Voltage	±5V	Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	DS55107, DS55108, DS1603			DS75107, DS75207 DS75108, DS75208 DS3603, DS3604		
	MIN	NOM	MAX	MIN	NOM	MAX
Supply Voltage V_{CC}^+	4.5V	5V	5.5V	4.75V	5V	5.25V
Supply Voltage V_{CC}^-	−4.5V	−5V	−5.5V	−4.75V	−5V	−5.25V
Operating Temperature Range	−55°C	to	+125°C	0°C	to	+70°C

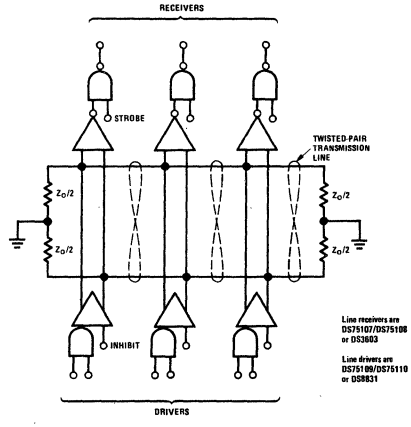
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1603, DS55107 and DS55108 and across the 0°C to +70°C range for the DS3603, DS3604, DS75107, DS75108. All typical values are for T_A = 25°C and V_{CC} = 5V.

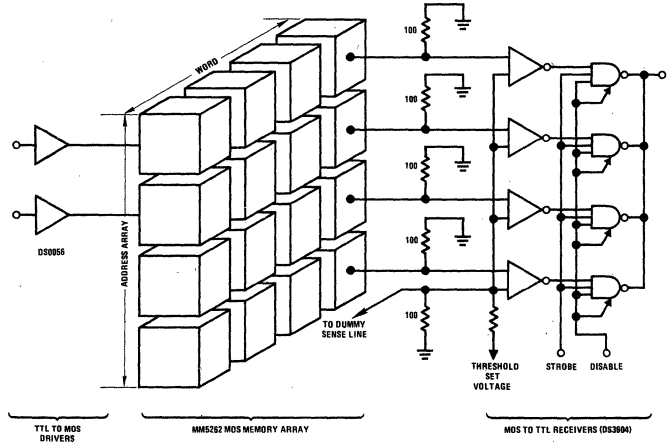
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

typical applications

Line Receiver Used in a Party-Line or Data-Bus System

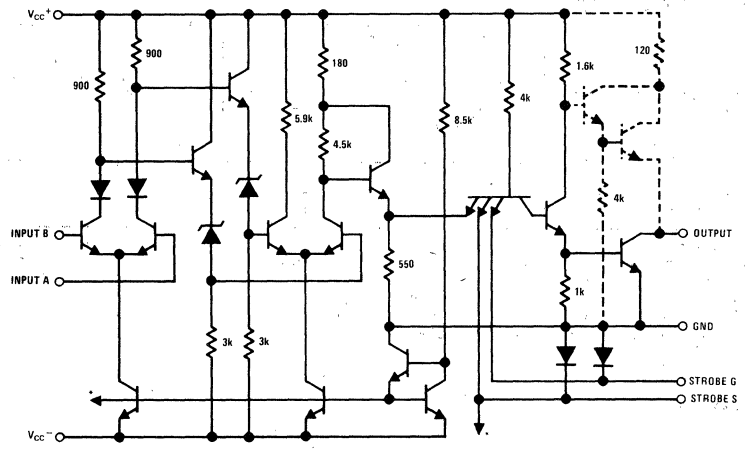


Line Receiver Used in MOS Memory System



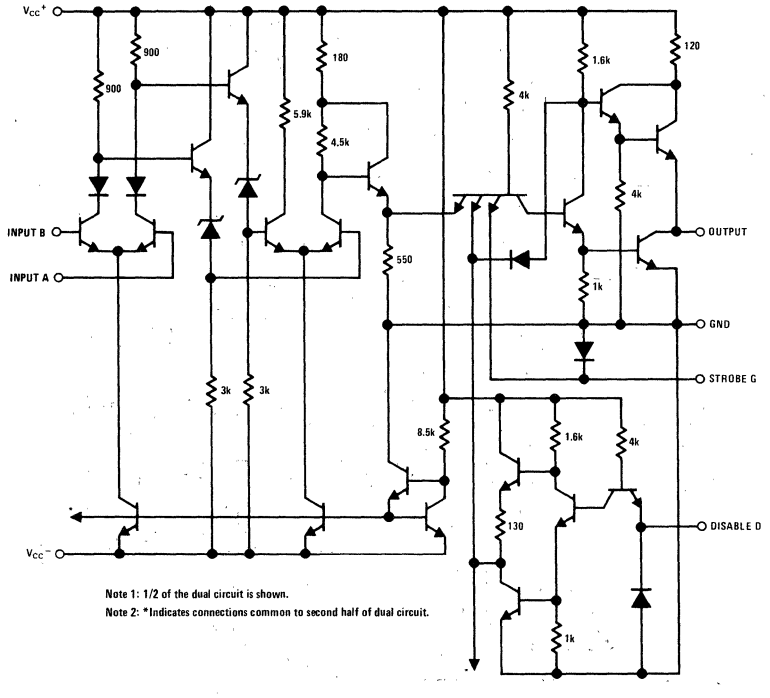
schematic diagrams

DS55107/DS75107, DS75207
DS55108/DS75108, DS75208



Note 1: 1/2 of the dual circuit is shown.
Note 2: *Indicates connections common to second half of dual circuit.
Note 3: Components shown with dash lines are applicable to the DS55107, DS75107 and DS75207 only.

DS1603/DS3603, DS3604



Note 1: 1/2 of the dual circuit is shown.
Note 2: *Indicates connections common to second half of dual circuit.

DS55107/DS75107, DS55108/DS75108

electrical characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{IH}	High Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Low Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	High Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			40	μA
			$V_{IH(S)}$ = Max V_{CC+}			1	mA
I_{IL}	Low Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(S)}$ = 0.4V				−1.6	mA
I_{IH}	High Level Input Current Into S	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			80	μA
			$V_{IH(S)}$ = Max V_{CC+}			2	mA
I_{IL}	Low Level Input Current Into S	V_{CC+} = Max, V_{CC-} = Max $V_{IL(S)}$ = 0.4V				−3.2	mA
V_{OH}	High Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{LOAD} = −400μA, V_{ID} = 25 mV, V_{IC} = −3V to 3V, (Note 3)		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{SINK} = 16 mA, V_{ID} = −25 mV, V_{IC} = −3V to 3V				0.4	V
I_{OH}	High Level Output Current	V_{CC+} = Min, V_{CC-} = Min V_{OH} = Max V_{CC+}, (Note 4)				250	μA
I_{OS}	Short Circuit Output Current	V_{CC+} = Max, V_{CC-} = Max, (Notes 2 and 3)		−18		−70	mA
I_{CCH+}	High Logic Level Supply Current From V_{CC}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 25 mV, T_A = 25°C			18	30	mA
I_{CCH-}	High Logic Level Supply Current From V_{CC}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 25 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or S	V_{CC+} = Min, V_{CC-} = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

switching characteristics (V_{CC+} = 5V, V_{CC-} = −5V, T_A = 25°C)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{PLH(D)}$	Propagation Delay Time, Low to High Level, From Differential Inputs A and B to Output	R_L = 390Ω, C_L = 50 pF, (Note 1)	(Note 3)		17	25	ns
			(Note 4)		19	25	ns
$t_{PHL(D)}$	Propagation Delay Time, High to Low Level, From Differential Inputs A and B to Output	R_L = 390Ω, C_L = 50 pF, (Note 1)	(Note 3)		17	25	ns
			(Note 4)		19	25	ns
$t_{PLH(S)}$	Propagation Delay Time, Low to High Level, From Strobe Input G or S to Output	R_L = 390Ω, C_L = 50 pF	(Note 3)		10	15	ns
			(Note 4)		13	20	ns
$t_{PHL(S)}$	Propagation Delay Time, High to Low Level, From Strobe Input G or S to Output	R_L = 390Ω, C_L = 50 pF	(Note 3)		8	15	ns
			(Note 4)		13	20	ns

Note 1: Differential input is +100 mV to −100 mV pulse. Delays read from 0 mV on input to 1.5V on output.
Note 2: Only one output at a time should be shorted.
Note 3: DS55107/DS75107 only.
Note 4: DS55108/DS75108 only.

DS75207, DS75208

electrical characteristics ($0°C \leq T_A \leq +70°C$)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
I_{IH}	High Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Low Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	High Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			40	μA
			$V_{IH(S)}$ = Max V_{CC+}			1	mA
I_{IL}	Low Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(S)}$ = 0.4V				−1.6	mA
I_{IH}	High Level Input Current Into S	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			80	μA
			$V_{IH(S)}$ = Max V_{CC+}			2	mA
I_{IL}	Low Level Input Current Into S	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(S)}$ = 0.4V				−3.2	mA
V_{OH}	High Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{LOAD} = −400μA, V_{ID} = 10 mV, V_{IC} = −3V to 3V, (Note 3)		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{SINK} = 16 mA, V_{ID} = −10 mV, V_{IC} = −3V to 3V				0.4	V
I_{OH}	High Level Output Current	V_{CC+} = Min, V_{CC-} = Min, V_{OH} = Max V_{CC+}, (Note 4)				250	μA
I_{OS}	Short Circuit Output Current	V_{CC+} = Max, V_{CC-} = Max (Notes 2, 3 and 4)		−18		−70	mA
I_{CCH+}	High Logic Level Supply Current From V_{CC}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 10 mV, T_A = 25°C			18	30	mA
I_{CCH-}	High Logic Level Supply Current From V_{CC}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 10 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or S	V_{CC+} = Min, V_{CC-} = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

switching characteristics (V_{CC+} = 5V, V_{CC-} = −5V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$t_{PLH(D)}$	Propagation Delay Time, Low-to-High Level, From Differential Inputs A and B to Output	R_L = 470Ω, C_L = 15 pF, (Note 1)			35	ns
$t_{PHL(D)}$	Propagation Delay Time, High-to-Low Level, From Differential Inputs A and B to Output	R_L = 470Ω, C_L = 15 pF, (Note 1)			20	ns
$t_{PLH(S)}$	Propagation Delay Time, Low-to-High Level, From Strobe Input G or S to Output	R_L = 470Ω, C_L = 15 pF			17	ns
$t_{PHL(S)}$	Propagation Delay Time, High-to-Low Level, From Strobe Input G or S to Output	R_L = 470Ω, C_L = 15 pF			17	ns

Note 1: Differential input is +10 mV to −30 mV pulse. Delays read from 0 mV on input to 1.5V on output.
Note 2: Only one output at a time should be shorted.
Note 3: DS75207 only.
Note 4: DS75208 only.

DS1603/DS3603

electrical characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{IH}	High Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Low Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	High Level Input Current Into G1, G2 or D	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			40	μA
			$V_{IH(S)}$ = Max V_{CC+}			1	mA
I_{IL}	Low Level Input Current Into D	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(D)}$ = 0.4V				−1.6	mA
I_{IL}	Low Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(G)}$ = 0.4V	$V_{IH(D)}$ = 2V			−40	μA
			$V_{IL(D)}$ = 0.8V			−1.6	mA
V_{OH}	High Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{LOAD} = −2 mA, V_{ID} = 25 mV $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{SINK} = 16 mA, V_{ID} = −25 mV, $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V				0.4	V
I_{OD}	Output Disable Current	V_{CC+} = Max, V_{CC-} = Max $V_{IH(D)}$ = 2V	V_{OUT} = 2.4V			40	μA
			V_{OUT} = 0.4V			−40	μA
I_{OS}	Short Circuit Output Current	V_{CC+} = Max, $V_{IL(D)}$ = 0.8V, V_{CC-} = Max, (Note 2)		−18		−70	mA
I_{CCH+}	High Logic Level Supply Current From V_{CC+}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 25 mV, T_A = 25°C			28	40	mA
I_{CCH-}	High Logic Level Supply Current From V_{CC-}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 25 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or D	V_{CC+} = Min, V_{CC-} = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

switching characteristics (V_{CC+} = 5V, V_{CC-} = −5V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{PLH(D)}$	Propagation Delay Time, Low-to-High Level, From Differential Inputs A and B to Output	R_L = 390Ω, C_L = 50 pF, (Note 1)		17	25	ns
$t_{PHL(D)}$	Propagation Delay Time, High-to-Low Level, From Differential Inputs A and B to Output	R_L = 390Ω, C_L = 50 pF, (Note 1)		17	25	ns
$t_{PLH(S)}$	Propagation Delay Time, Low-to-High Level, From Strobe Input G to Output	R_L = 390Ω, C_L = 50 pF		10	15	ns
$t_{PHL(S)}$	Propagation Delay Time, High-to-Low Level, From Strobe Input G to Output	R_L = 390Ω, C_L = 50 pF		8	15	ns
t_{1H}	Disable Low-to-High to Output High to Off	R_L = 390Ω, C_L = 5 pF			20	ns
t_{0H}	Disable Low-to-High to Output Low to Off	R_L = 390Ω, C_L = 5 pF			30	ns
t_{H1}	Disable High-to-Low to Output Off to High	R_L = 1k to 0V, C_L = 50 pF			25	ns
t_{H0}	Disable High-to-Low to Output Off to Low	R_L = 390Ω, C_L = 50 pF			25	ns

Note 1: Differential input is +100 mV to −100 mV pulse. Delays read from 0 mV on input to 1.5V on output.
Note 2: Only one output at a time should be shorted.

DS3604

electrical characteristics ($0°C \leq T_A \leq +70°C$)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{IH}	High Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 0.5V, V_{IC} = −3V to 3V			30	75	μA
I_{IL}	Low Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = −2V, V_{IC} = −3V to 3V				−10	μA
I_{IH}	High Level Input Current Into G1, G2 or D	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(S)}$ = 2.4V			40	μA
			$V_{IH(S)}$ = Max V_{CC+}			1	mA
I_{IL}	Low Level Input Current Into D	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(D)}$ = 0.4V				−1.6	mA
I_{IL}	Low Level Input Current Into G1 or G2	V_{CC+} = Max, V_{CC-} = Max,	$V_{IH(D)}$ = 2V			−40	μA
		$V_{IL(G)}$ = 0.4V	$V_{IL(D)}$ = 0.8V			−1.6	mA
V_{OH}	High Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{LOAD} = −2 mA, V_{ID} = 10 mV, $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC+} = Min, V_{CC-} = Min, I_{SINK} = 16 mA, V_{ID} = −10 mV, $V_{IL(D)}$ = 0.8V, V_{IC} = −3V to 3V				0.4	V
I_{OD}	Output Disable Current	V_{CC+} = Max, V_{CC-} = Max, $V_{IH(D)}$ = 2V	V_{OUT} = 2.4V			40	μA
			V_{OUT} = 0.4V			−40	μA
I_{OS}	Short Circuit Output Current	V_{CC+} = Max, $V_{IL(D)}$ = 0.8V, V_{CC-} = Max, (Note 2)		−18		−70	mA
I_{CCH+}	High Logic Level Supply Current From V_{CC+}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 10 mV, T_A = 25°C			28	40	mA
I_{CCH-}	High Logic Level Supply Current From V_{CC-}	V_{CC+} = Max, V_{CC-} = Max, V_{ID} = 10 mV, T_A = 25°C			−8.4	−15	mA
V_I	Input Clamp Voltage on G or D	V_{CC+} = Min, V_{CC-} = Min, I_{IN} = −12 mA, T_A = 25°C			−1	−1.5	V

switching characteristics (V_{CC+} = 5V, V_{CC-} = −5V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{PLH(D)}$	Propagation Delay Time, Low-to-High Level, From Differential Inputs A and B to Output	R_L = 470Ω, C_L = 15 pF, (Note 1)			35	ns
$t_{PHL(D)}$	Propagation Delay Time, High-to-Low Level, From Differential Inputs A and B to Output	R_L = 470Ω, C_L = 15 pF, (Note 1)			20	ns
$t_{PLH(S)}$	Propagation Delay Time, Low-to-High Level, From Strobe Input G to Output	R_L = 470Ω, C_L = 15 pF			17	ns
$t_{PHL(S)}$	Propagation Delay Time, High-to-Low Level, From Strobe Input G to Output	R_L = 470Ω, C_L = 15 pF			17	ns
t_{1H}	Disable Low-to-High to Output High to Off	R_L = 470Ω, C_L = 5 pF			20	ns
t_{0H}	Disable Low-to-High to Output Low to Off	R_L = 470Ω, C_L = 5 pF			30	ns
t_{H1}	Disable High-to-Low to Output Off to High	R_L = 1k to 0V, C_L = 15 pF			25	ns
t_{H0}	Disable High-to-Low to Output Off to Low	R_L = 470Ω, C_L = 15 pF			25	ns

Note 1: Differential input is +10 mV to −30 mV pulse. Delays read from 0 mV on input to 1.5V on output.
Note 2: Only one output at a time should be shorted.

NATIONAL

Line Drivers/Receivers

Advance Information*

DS55109/DS75109, DS55110/DS75110 dual line drivers

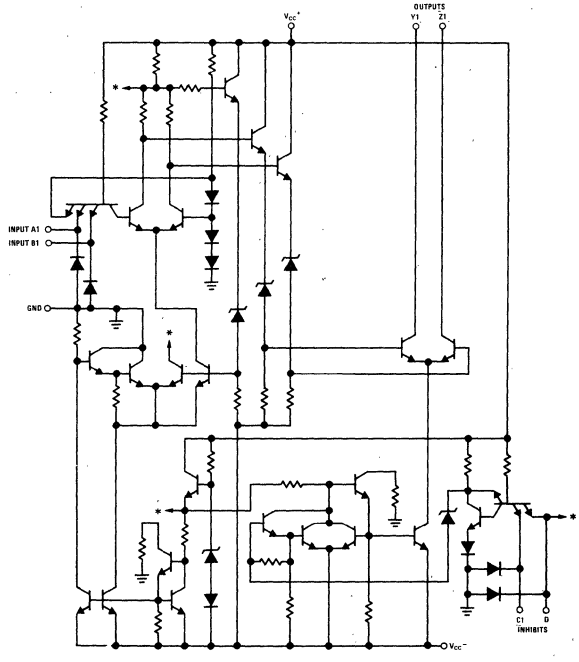
general description

These products are TTL compatible high speed differential line drivers intended for use in terminated twisted-pair party-line data transmission systems. They may also be used for level shifting since output common-mode range is −3V to +10V. An internal current sink is switched to either output dependent on input logic conditions. The current sink may be turned off by appropriate inhibit input conditions.

features

- Tightly controlled output currents over temperature, V_{CC}, and common-mode variations
- High speed 15 ns max
- Wide output common-mode range
- High output impedance
- Inhibits for party-line applications
- Current sink outputs 6 or 12 mA
- Dual circuits
- Standard supply voltages ±5V
- Input clamp diodes
- 14 pin cavity or molded DIP

schematic diagram

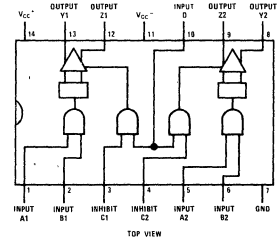


Note 1: 1/2 of the dual circuit shown.

Note 2: *Indicates connections common to second half of circuit.

connection diagram

Dual-In-Line Package

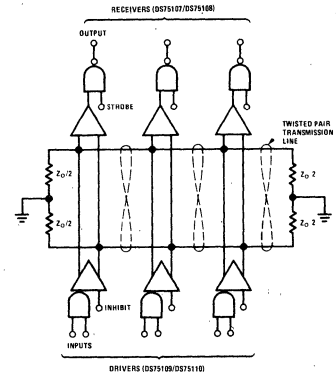


Order Number DS55109J, DS55110J, DS75109J or DS75110J

Order Number DS75109N or DS75110N

typical application

Party-Line Data Transmission System



*Specifications may change

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}^+	7V
Supply Voltage, V_{CC}^-	−7V
Logic and Inhibitor Input Voltages	5.5V
Common-mode Output Voltage	−5V to 12V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	600 mW
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS55109, DS55110	4.5	5.5	V
DS75109, DS75110	4.75	5.25	V
Temperature (T_A)			
DS55109, DS55110	−55	+125	°C
DS75109, DS75110	0	+70	°C
Positive Common-Mode Output Voltage (Note 4)	0	10	V
Negative Common-Mode Output Voltage (Note 4)	0	−3	V

electrical characteristics ($T_{MIN} \leq T_A \leq T_{MAX}$) (Notes 2 and 3)

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
$I_{IH(L)}$	High Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(L)}$ = 2.4V				40	μA
			$V_{IH(L)}$ = Max V_{CC+}				1	mA
$I_{IL(L)}$	Low Level Input Current Into A1, B1, A2 or B2	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(L)}$ = 0.4V					−3	mA
$I_{IH(I)}$	High Level Input Current Into C1 or C2	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(I)}$ = 2.4V				40	μA
			$V_{IH(I)}$ = Max V_{CC+}				1	mA
$I_{IL(I)}$	Low Level Input Current Into C_1 or C2	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(I)}$ = 0.4V					−3	mA
$I_{IH(I)}$	High Level Input Current Into D	V_{CC+} = Max, V_{CC-} = Max	$V_{IH(I)}$ = 2.4V				80	μA
			$V_{IH(I)}$ = Max V_{CC+}				2	mA
$I_{IL(I)}$	Low Level Input Current Into D	V_{CC+} = Max, V_{CC-} = Max, $V_{IL(I)}$ = 0.4V					−6	mA
$I_{O(ON)}$	On State Output Current	V_{CC-} = Max	V_{CC+} = Max	DS55109/DS75109			7	mA
				DS55110/DS75110			15	mA
			V_{CC+} = Min	DS55109/DS75109	3.5			mA
				DS75110/DS75110	6.5			mA
$I_{O(OFF)}$	"OFF" State Output Current	V_{CC+} = Min, V_{CC-} = Min					100	μA
$I_{CC+(ON)}$	Supply Current From V_{CC+} With Driver Enabled	$V_{IL(L)}$ = 0.4V, $V_{IH(I)}$ = 2V		DS55109/DS75109		18	30	mA
				DS55110/DS75110		23	35	mA
$I_{CC-(ON)}$	Supply Current From V_{CC-} With Driver Enabled	$V_{IL(L)}$ = 0.4V, $V_{IH(I)}$ = 2V		DS55109/DS75109		−18	−30	mA
				DS55110/DS75110		−34	−50	mA
$I_{CC+(OFF)}$	Supply Current From V_{CC+} With Driver Inhibited	$V_{IL(L)}$ = 0.4V, $V_{IL(I)}$ = 0.4V		DS55109/DS75109		18		mA
				DS55110/DS75110		21		mA
$I_{CC-(OFF)}$	Supply Current From V_{CC-} With Driver Inhibited	$V_{IL(L)}$ = 0.4V, $V_{IL(I)}$ = 0.4V		DS55109/DS75109		−10		mA
				DS55110/DS75110		−17		mA
V_I	Input Clamp Voltage on Inputs or Inhibits	V_{CC+} = Min, V_{CC-} = Min, I_{IN} = −12 mA, T_A = 25°C				−1	−1.5	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55109, DS55110 and across the 0°C to +70°C range for the DS75109, DS75110. All typical values are for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: These voltage values are with respect to the network ground terminal.

switching characteristics (V_{CC+} = 5V, V_{CC-} = 5V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$t_{PLH(L)}$	Propagation Delay Time, Low-to-High Level, From Logic Input A or B to Output Y or Z	R_L = 50Ω, C_L = 40 pF		9	15	ns
$t_{PHL(L)}$	Propagation Delay Time, High-to-Low Level, From Logic Input A or B to Output Y or Z	R_L = 50Ω, C_L = 40 pF		9	15	ns
$t_{PLH(I)}$	Propagation Delay Time, Low-to-High Level, From Inhibitor Input C or D to Output Y or Z	R_L = 50Ω, C_L = 40 pF		16	25	ns
$t_{PHL(I)}$	Propagation Delay Time, High-to-Low Level, From Inhibitor Input C or D to Output Y or Z	R_L = 50Ω, C_L = 40 pF		13	25	ns

NATIONAL

Line Drivers/Receivers

DS55121/DS75121 dual line drivers

general description

The DS55121/DS75121 are monolithic dual line drivers designed to drive long lengths of coaxial cable, strip line, or twisted pair transmission lines having impedances from 50 to 500 ohms. Both are compatible with standard TTL logic and supply voltage levels.

The DS55121/DS75121 will drive terminated low impedance lines due to the low-impedance emitter-follower outputs. In addition the outputs are uncommitted allowing two or more drivers to drive the same line.

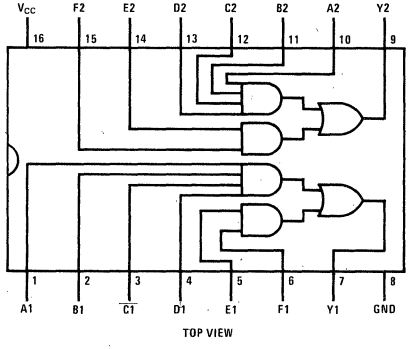
Output short-circuit protection is incorporated to turn off the output when the output voltage drops below approximately 1.5V.

features

- Designed for digital data transmission over 50 to 500 ohms coaxial cable, strip line, or twisted pair transmission lines
- TTL compatible
- Open emitter-follower output structure for party-line operation
- Short-circuit protection
- AND-OR logic configuration
- High speed (max propagation delay time 20 ns)
- Plug-in replacement for the SN55121/SN75121 and the 8T13

connection diagram

Dual-In-Line Package

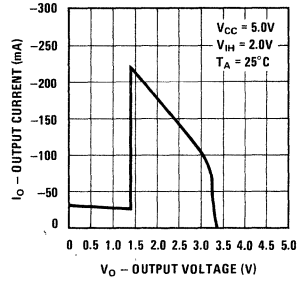


TOP VIEW

Order Number DS55121J, DS75121J, DS75121N or DS55121W

typical performance characteristics

Output Current vs Output Voltage

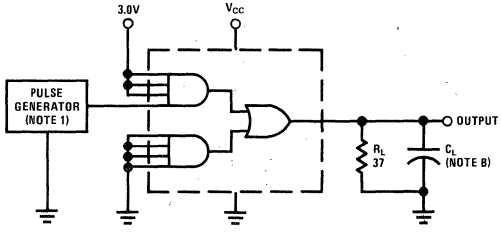


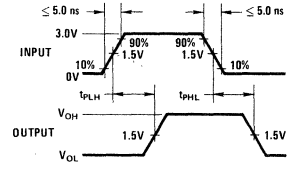
truth table

INPUTS A	B	C	D	E	F	OUTPUT Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Input Combinations						L

H = high level, L = low level, X = irrelevant

ac test circuit and switching time waveforms





Note 1: The pulse generators have the following characteristics: $Z_{OUT} \approx 50\Omega$, t_W = 200 ns, duty cycle = 50%, $t_r = t_f$ = 5.0 ns.

Note 2: C_L includes probe and jig capacitance.

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	6.0V
Input Voltage	6.0V
Output Voltage	6.0V
Output Current	−75 mA
Power Dissipation	600 mW
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A			
DS55121	−55	+125	°C
DS75121	0	+75	°C

electrical characteristics V_{CC} = 4.75V to 5.25V (unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA			−1.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V			1	mA
V_{OH}	High Level Output Voltage	V_{IH} = 2.0V, I_{OH} = −75 mA (Note 4)	2.4			V
I_{OH}	High Level Output Current	V_{CC} = 5.0V, V_{IH} = 4.75V, V_{OH} = 2.0V, T_A = 25°C (Note 4)	−100		−250	mA
I_{OL}	Low Level Output Current	V_{IL} = 0.8V, V_{OL} = 0.4V (Note 4)			−800	μA
$I_{O(OFF)}$	Off State Output Current	V_{CC} = 0V, V_O = 3.0V			500	μA
I_{IH}	High Level Input Current	V_I = 4.5V			40	μA
I_{IL}	Low Level Input Current	V_I = 0.4V	−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C			−30	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = 5.25V, All Inputs at 2.0V, Outputs Open			28	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = 5.25V, All Inputs at 0.8V, Outputs Open			60	mA

switching characteristics V_{CC} = 5.0V, T_A = 25°C

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 37Ω, (See ac Test Circuit and Switching Time Waveforms)	C_L = 15 pF		11	20	ns
			C_L = 1000 pF		22	50	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 37Ω, (See ac Test Circuit and Switching Time Waveforms)	C_L = 15 pF		8.0	20	ns
			C_L = 1000 pF		20	50	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55121 and across the 0°C to +70°C range for the DS75121. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

NATIONAL

Line Drivers/Receivers

DS55122/DS75122 triple line receivers

general description

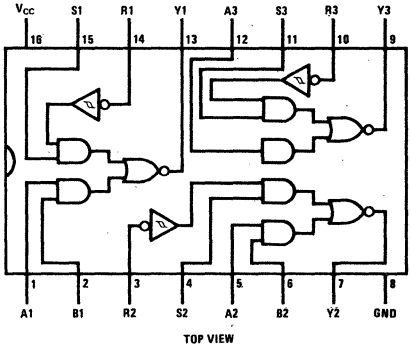
The DS55122/DS75122 are triple line receivers designed for digital data transmission with line impedances from 50Ω to 500Ω. Each receiver has one input with built-in hysteresis which provides a large noise margin. The other inputs on each receiver are in a standard TTL configuration. The DS55122/DS75122 are compatible with standard TTL logic and supply voltage levels.

features

- Built-in input threshold hysteresis
- High speed . . . typical propagation delay time 20 ns
- Independent channel strobes
- Input gating increases application flexibility
- Single 5.0V supply operation
- Fanout to 10 series 54/74 standard loads
- Plug-in replacement for the SN55122/SN75122 and the 8T14

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DS55122J, DS75122J, DS75122N or DS55122W

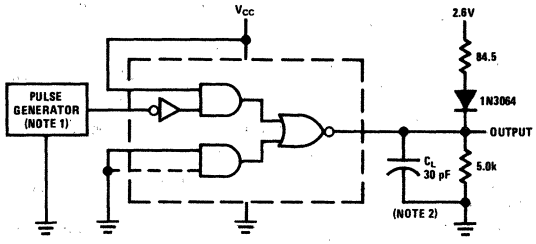
truth table

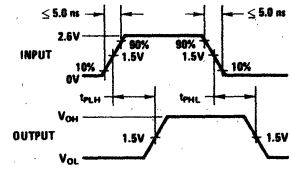
INPUTS A	INPUTS B†	INPUTS R	INPUTS S	OUTPUT Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = high level, L = low level, X = irrelevant

†B input and last two lines of the truth table are applicable to receivers 1 and 2 only.

ac test circuit and switching time waveforms





Note 1: The pulse generator has the following characteristics: $Z_{OUT} \approx 50\Omega$, $t_W = 200$ ns, duty cycle = 50%, $t_r = t_f = 5.0$ ns.

Note 2: C_L includes probe and jig capacitance.

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	6.0V
Input Voltage	
R Input	6.0V
A, B, or S Input	5.5V
Output Voltage	6.0V
Output Current	±100 mA
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
Operating Temperature, T_A			
DS55122	−55	+125	°C
DS75122	0	+75	°C
High Level Output Current, I_{OH}		−500	μA
Low Level Output Current, I_{OL}		16	mA

electrical characteristics V_{CC} = 4.75V to 5.25V (unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	A, B, R, or S		2.0			V
V_{IL}	Low Level Input Voltage	A, B, R, or S				0.8	V
$V_{T+}-V_{T-}$	Hysteresis	V_{CC} = 5.0V, T_A = 25°C, R,(Note 6)		0.3	0.6		V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA, A, B, or S				−1.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V, A, B, or S				1.0	mA
V_{OH}	High Level Output Voltage	I_{OH} = −500μA	V_{IH} = 2V, V_{IL} = 0.8V, (Note 4)	2.6			V
			$V_{I(A)}$ = 0V, $V_{I(B)}$ = 0V, $V_{I(R)}$ = 1.45V, $V_{I(S)}$ = 2.0V, (Note 7)	2.6			V
V_{OL}	Low Level Output Voltage	I_{OL} = 16 mA	V_{IH} = 2.0V, V_{IL} = 0.8V, (Note 4)			0.4	V
			$V_{I(A)}$ = 0V, $V_{I(B)}$ = 0V, $V_{I(R)}$ = 1.45V, $V_{I(S)}$ = 2.0V, (Note 8)			0.4	V
I_{IH}	High Level Input Current	V_I = 4.5V, A, B, or S				40	μA
		V_I = 3.8V, R				170	μA
I_{IL}	Low Level Input Current	V_I = 0.4V, A, B, or S		−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C, (Note 5)		−50		−100	mA
I_{CC}	Supply Current	V_{CC} = 5.25V				72	mA

switching characteristics V_{CC} = 5.0V, T_A = 25°C

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output from R Input	(See ac Test Circuit and Switching Time Waveforms)		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output from R Input	(See ac Test Circuit and Switching Time Waveforms)		20	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

Note 3: Min/max limits apply across the guaranteed operating temperature range of −55°C to +125 °C for DS55122 and 0°C to +75°C for DS75122, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

Note 5: Not more than one output should be shorted at a time.

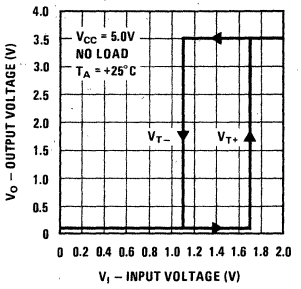
Note 6: Hysteresis is the difference between the positive going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

Note 7: Receiver input was at a high level immediately before being reduced to 1.45V.

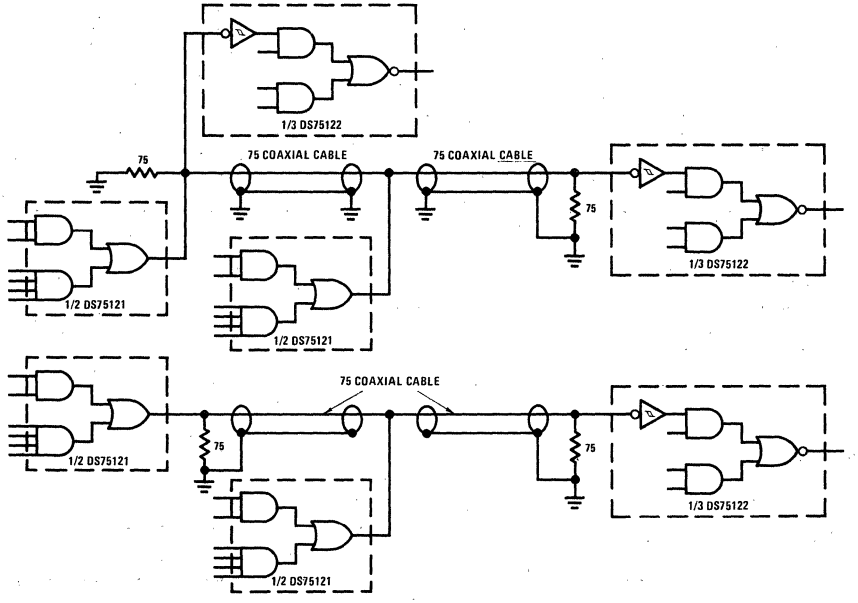
Note 8: Receiver input was at a low level immediately before being raised to 1.45V.

typical performance characteristics

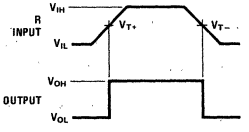
Output Voltage vs Receiver Input Voltage



typical applications



Single-Ended Party Line Circuits



The high gain and built-in hysteresis of the DS55122/DS75122 line receivers enable them to be used as Schmitt triggers in squaring up pulses.

Pulse Squaring

Line Drivers/Receivers

DS75123 dual line driver

general description

The DS75123 is a monolithic dual line driver designed specifically to meet the I/O interface specifications for IBM System 360. It is compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower outputs of the DS75123 enable driving terminated low impedance lines. In addition the outputs are uncommited allowing two or more drivers to drive the same line.

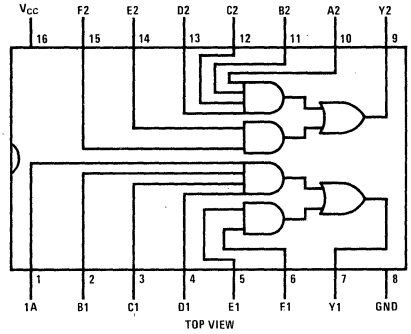
Output short-circuit protection is incorporated to turn off the output when the output voltage drops below approximately 1.5V.

features

- Meet IBM System 360 I/O interface specifications for digital data transmission over 50Ω to 500Ω coaxial cable, strip line, or terminated pair transmission lines
- TTL compatible with single 5.0V supply
- 3.11V output at I_{OH} = −59.3 mA
- Open emitter-follower output structure for party-line operation
- Short circuit protection
- AND-OR logic configuration
- Plug-in replacement for the SN75123 and the 8T23

connection diagram

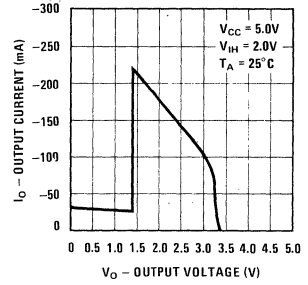
Dual-In-Line Package



Order Number DS75123J
Order Number DS75123N

typical performance characteristics

Output Current vs Output Voltage

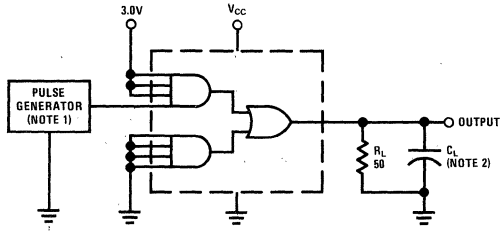


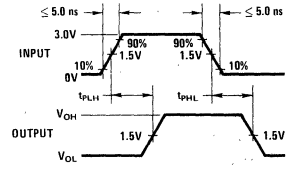
truth table

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All Other Input Combinations						L

H = high level, L = low level, X = irrelevant

ac test circuit and switching time waveforms





Note 1: THE PULSE GENERATORS HAVE THE FOLLOWING CHARACTERISTICS: $Z_{OUT} \approx 50\Omega$, t_W = 200 ns, DUTY CYCLE = 50%.
Note 2: C_L INCLUDES PROBE AND JIG CAPACITANCE.

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	7.0V
Power Dissipation	600 mW
Operating Free-Air Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
High Level Output Current, I_{OH}		−100	mA
Temperature, T_A	0	+75	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage			2.0			V
V_{IL}	Low Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA				−1.5	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V				1	mA
V_{OH}	High Level Output Voltage	V_{CC} = 5.0V, V_{IH} = 2.0V,	T_A = 25°C	3.11			V
		I_{OH} = −59.3 mA, (Note 4)	T_A = 0°C to +75°C	2.9			V
I_{OH}	High Level Output Current	V_{CC} = 5.0V, V_{IH} = 4.5V, T_A = 25°C, V_{OH} = 2.0V, (Note 4)		−100		−250	mA
V_{OL}	Low Level Output Voltage	V_{IL} = 0.8V, I_{OL} = −240μA, (Note 4)				0.15	V
$I_{O(OFF)}$	Off State Output Current	V_{CC} = 0, V_O = 3.0V				40	μA
I_{IH}	High Level Input Current	V_I = 4.5V				40	μA
I_{IL}	Low Level Input Current	V_I = 0.4V		−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C				−30	mA
I_{CCH}	Supply Current, Outputs High	V_{CC} = 5.25V, All Inputs at 2.0V, Outputs Open				28	mA
I_{CCL}	Supply Current, Outputs Low	V_{CC} = 5.25V, All Inputs at 0.8V, Outputs Open				60	mA

switching characteristics V_{CC} = 5.0V, T_A = 25°C

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	R_L = 50Ω, (See ac Test Circuit and Switching Time Waveforms	C_L = 15 pF		12	20	ns
			C_L = 100 pF		20	35	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	R_L = 50Ω, (See ac Test Circuit and Switching Time Waveforms	C_L = 15 pF		12	20	ns
			C_L = 100 pF		15	25	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

Note 3: Min/max limits apply across the guaranteed operating temperature range of 0°C to +75°C for DS75123, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

Line Drivers/Receivers

DS75124 triple line receivers

general description

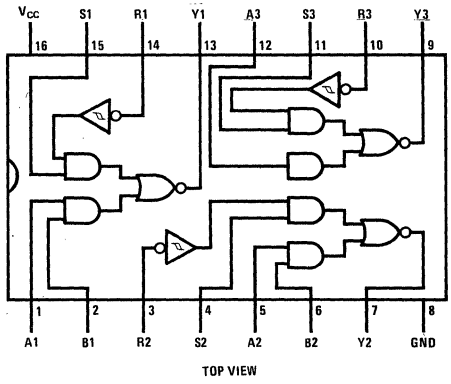
The DS75124 is designed to meet the input/output interface specifications for IBM System 360. It has built-in hysteresis on one input on each of the three receivers to provide large noise margin. The other inputs on each receiver are in a standard TTL configuration. The DS75124 is compatible with standard TTL logic and supply voltage levels.

features

- Built-in input threshold hysteresis
- High speed . . typ propagation delay time 20 ns
- Independent channel strobes
- Input gating increases application flexibility
- Single 5.0V supply operation
- Plug-in replacement for the SN75124 and the 8T24

connection diagram and truth table

Dual-In-Line Package



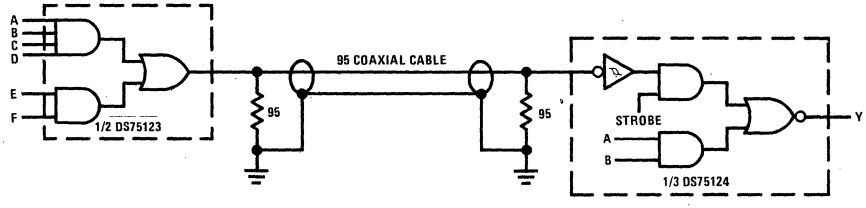
TOP VIEW

INPUTS				OUTPUT
A	B†	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

H = high level, L = low level, X = irrelevant
†B input and last two lines of the truth table are applicable to receivers 1 and 2 only.

Order Number DS75124J **Order Number DS75124N**

typical application



absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7.0V
Input Voltage	
R Input with V_{CC} Applied	7.0V
R Input with V_{CC} not Applied	6.0V
A, B, or S Input	5.5V
Output Voltage	7.0V
Output Current	±100 mA
Power Dissipation	600 mW
Operating Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
High Level Output Current, I_{OH}		−800	μA
Low Level Output Current, I_{OL}		16	mA
Operating Temperature, T_A	0	+75	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	A, B, or S		2.0			V
		R		1.7			V
V_{IL}	Low Level Input Voltage	A, B, or S				0.8	V
		R				0.7	V
$V_{T+}-V_{T-}$	Hysteresis	V_{CC} = 5.0V, T_A = 25°C, R, (Note 6)		0.2	0.4		V
V_I	Input Clamp Voltage	V_{CC} = 5.0V, I_I = −12 mA, A, B, or S				−1.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.25V, V_{IN} = 5.5V, A, B, or S				1	mA
		R	V_I = 7.0V			5.0	mA
			V_I = 6.0V, V_{CC} = 0			5.0	mA
V_{OH}	High Level Output Voltage	$V_{IH} = V_{IH\,MIN}$, $V_{IL} = V_{IL\,MAX}$, I_{OH} = −800μA, (Note 4)		2.6			V
V_{OL}	Low Level Output Voltage	$V_{IH} = V_{IN\,MIN}$, $V_{IL} = V_{IL\,MAX}$, I_{OL} = 16 mA, (Note 4)				0.4	V
I_{IH}	High Level Input Current	V_I = 4.5V, A, B, or S				40	μA
		V_I = 3.11V, R				170	μA
I_{IL}	Low Level Input Current	V_I = 0.4V, A, B, or S		−0.1		−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = 5.0V, T_A = 25°C, (Note 5)		−50		−100	mA
I_{CC}	Supply Current	V_{CC} = 5.25V				72	mA

switching characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output from R Input	(See ac Test Circuit and Switching Time Waveforms)		20	30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output from R Input	(See ac Test Circuit and Switching Time Waveforms)		20	30	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All currents into device pins are shown as positive, currents out of device pins shown as negative, all voltage values are referenced with respect to network ground terminal, unless otherwise noted. All values shown as max or min on absolute value basis.

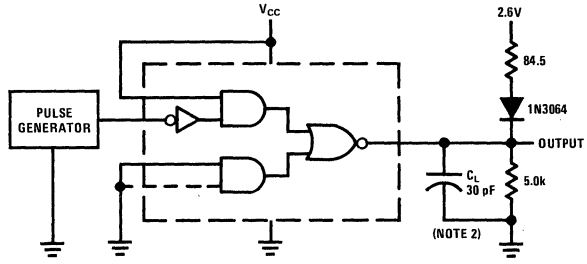
Note 3: Min/max limits apply across the guaranteed operating temperature range of 0°C to +75°C for DS75124, unless otherwise specified. Typicals are for V_{CC} = 5.0V, T_A = 25°C. Positive current is defined as current into the referenced pin.

Note 4: The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the truth table for the desired output.

Note 5: Not more than one output should be shorted at a time.

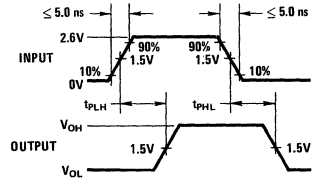
Note 6: Hysteresis is the difference between the positive going input threshold voltage, V_{T+}, and the negative going input threshold voltage, V_{T-}.

ac test circuit and switching time waveforms

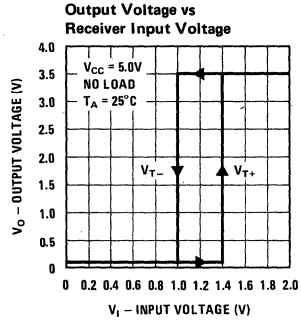


Note 1: THE PULSE GENERATOR HAS THE FOLLOWING CHARACTERISTICS: $Z_{OUT} \approx 50\Omega$, $t_W = 200$ ns, DUTY CYCLE = 50%.

Note 2: C_L INCLUDES PROBE AND JIG CAPACITANCE.



typical performance characteristics



NATIONAL

Line Drivers/Receivers

DS75150 dual line driver

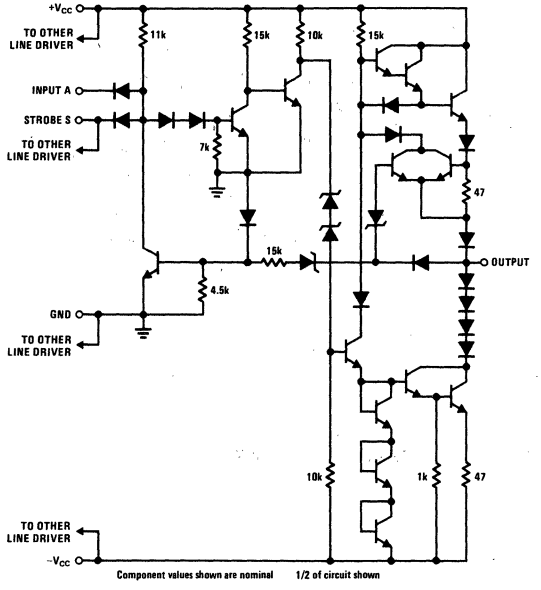
general description

The DS75150 is a dual monolithic line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500 pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and DTL families. Operation is from −12V and +12V power supplies.

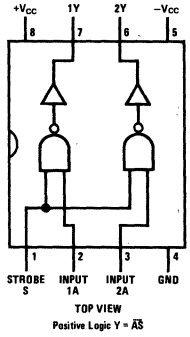
features

- Withstands sustained output short-circuit to any low impedance voltage between −25V and +25V
- 2μs max transition time through the −3V to +3V transition region under full 2500 pF load
- Inputs compatible with most TTL and DTL families
- Common strobe input
- Inverting output
- Slew rate can be controlled with an external capacitor at the output
- Standard supply voltages ±12V

schematic and connection diagrams

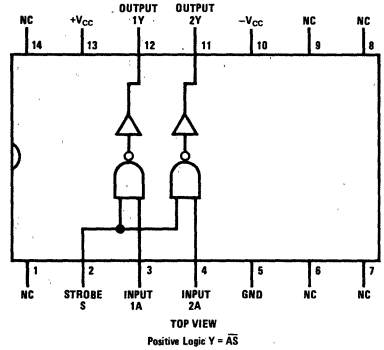


Dual-In-Line Package



Order Number DS75150N

Dual-In-Line Package



Order Number DS75150J

absolute maximum ratings (Note 1)

Supply Voltage $+V_{CC}$	15V
Supply Voltage $-V_{CC}$	−15V
Input Voltage	15V
Applied Output Voltage	±25V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage ($+V_{CC}$)	10.8	13.2	V
Supply Voltage ($-V_{CC}$)	−10.8	−13.2	V
Input Voltage (V_I)	0	+5.5	V
Output Voltage (V_O)		±15	V
Operating Ambient Temperature Range (T_A)	0	+70	°C

dc electrical characteristics (Notes 2, 3, 4 and 5)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High-Level Input Voltage	*(Figure 1)*		2			V
V_{IL}	Low-Level Input Voltage	*(Figure 2)*				0.8	V
V_{OH}	High-Level Output Voltage	$+V_{CC}$ = 10.8V, $-V_{CC}$ = −13.2V, V_{IL} = 0.8V, R_L = 3 kΩ to 7 kΩ, *(Figure 2)*		5	8		V
V_{OL}	Low-Level Output Voltage	$+V_{CC}$ = 10.8V, $-V_{CC}$ = −10.8V, V_{IH} = 2V, R_L = 3 kΩ to 7 kΩ, *(Figure 1)*			−8	−5	V
I_{IH}	High-Level Input Current	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 2.4V, *(Figure 3)*	Data Input		1	10	μA
		$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 2.4V, *(Figure 3)*	Strobe Input		2	20	μA
I_{IL}	Low-Level Input Current	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0.4V, *(Figure 3)*	Data Input		−1	−1.6	mA
		$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0.4V, *(Figure 3)*	Strobe Input		−2	−3.2	mA
I_{OS}	Short-Circuit Output Current	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, *(Figure 4)*, Note 4	V_O = 25V		2		mA
			V_O = −25V		−3		mA
			V_O = 0V, V_I = 3V		15		mA
			V_O = 0V, V_I = 0V		−15		mA
$+I_{CCH}$	Supply Current From $+V_{CC}$, High-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			10	22	mA
$-I_{CCH}$	Supply Current From $-V_{CC}$, High-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 0V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			−1	−10	mA
$+I_{CCL}$	Supply Current From $+V_{CC}$, Low-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 3V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			8	17	mA
$-I_{CCL}$	Supply Current From $-V_{CC}$, Low-Level Output	$+V_{CC}$ = 13.2V, $-V_{CC}$ = −13.2V, V_I = 3V, R_L = 3 kΩ, T_A = 25°C, *(Figure 5)*			−9	−20	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75150. All typical values are for T_A = 25°C and $+V_{CC}$ = 12V, $-V_{CC}$ = −12V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic levels only, e.g., when −5V is the maximum, the typical value is a more-negative voltage.

ac electrical characteristics ($+V_{CC} = 12V, -V_{CC} = -12V, T_A = 25°C$)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ, *(Figure 6)*	0.2	1.4	2	μs
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ, *(Figure 6)*	0.2	1.5	2	μs
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		40		ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		20		ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		60		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF, R_L = 7 kΩ, *(Figure 6)*		45		ns

dc test circuits

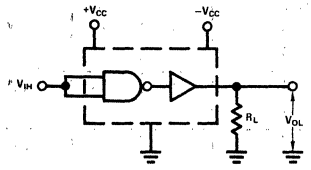
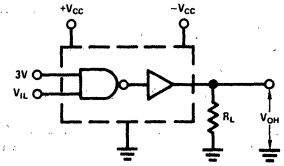
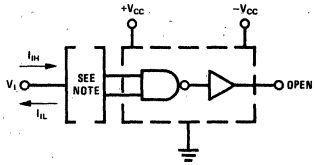


FIGURE 1. V_{IH}, V_{OL}



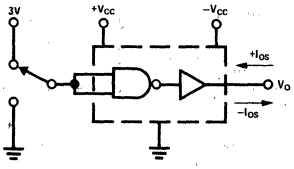
Each input is tested separately.

FIGURE 2. V_{IL}, V_{OH}



Note: When testing I_{IH}, the other input is at 3V; when testing I_{IL}, the other input is open.

FIGURE 3. I_{IH}, I_{IL}



I_{OS} is tested for both input conditions at each of the specified output conditions.

FIGURE 4. I_{OS}

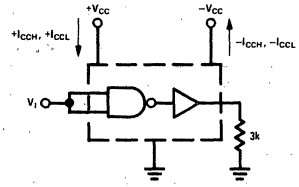
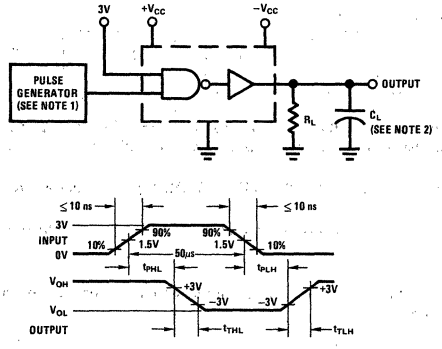


FIGURE 5. I_{CCH+}, I_{CCH-}, I_{CCL+}, I_{CCL-}

ac test circuit and switching time waveforms



Note 1: The pulse generator has the following characteristics: duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

FIGURE 6.

typical performance characteristics

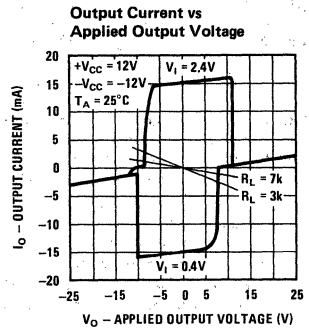


FIGURE 7.

Line Drivers/Receivers

DS75154 quadruple line receiver

general description

The DS75154 is a quad monolithic line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. Other applications are in relatively short, single-line, point-to-point data transmission systems and for level translators. Operation is normally from a single 5V supply; however, a built-in option allows operation from a 12V supply without the use of additional components. The output is compatible with most TTL and DTL circuits when either supply voltage is used.

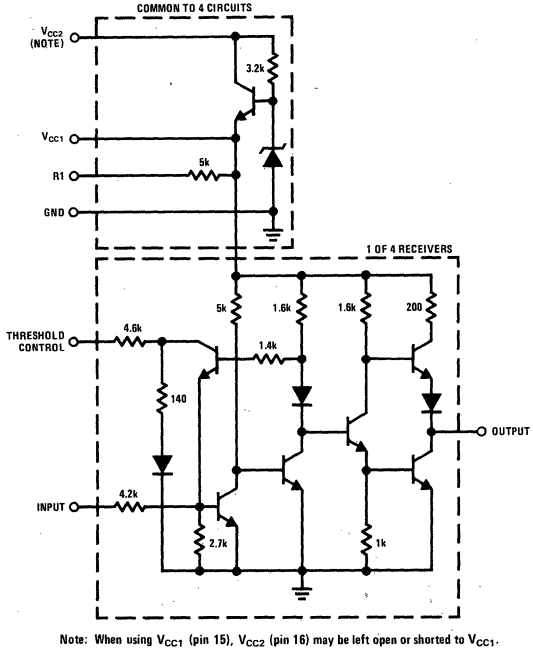
In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, pin 15, even if power is being supplied via the alternate V_{CC2} terminal, pin 16. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold voltages. In this mode, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

features

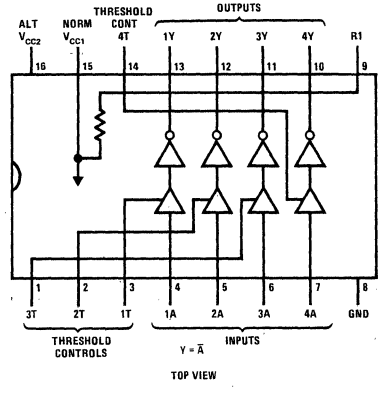
- Input resistance, 3 kΩ to 7 kΩ over full RS-232C voltage range
- Input threshold adjustable to meet "fail-safe" requirements without using external components
- Inverting output compatible with DTL or TTL
- Built-in hysteresis for increased noise immunity
- Output with active pull-up for symmetrical switching speeds
- Standard supply voltage—5V or 12V

schematic and connection diagrams



Note: When using V_{CC1} (pin 15), V_{CC2} (pin 16) may be left open or shorted to V_{CC1}. When using V_{CC2}, V_{CC1} must be left open or connected to the threshold control pins.

Dual-In-Line Package



TOP VIEW

Order Number DS75154J or DS75154N

absolute maximum ratings (Note 1)

Normal Supply Voltage (Pin 15), (V_{CC1})	7V
Alternate Supply Voltage (Pin 16), (V_{CC2})	14V
Input Voltage	±25V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (Pin 15), (V_{CC1})	4.5	5.5	V
Alternate Supply Voltage (Pin 16) (V_{CC2})	10.8	13.2	V
Input Voltage		±15	V
Temperature, (T_A)	0	+70	°C

electrical characteristics (Notes 2, 3 and 4)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High-Level Input Voltage	*(Figure 1)*		3			V
V_{IL}	Low-Level Input Voltage	*(Figure 1)*				−3	V
V_{T+}	Positive-Going Threshold Voltage	*(Figure 1)*	Normal Operation	0.8	2.2	3	V
			Fail-Safe Operation	0.8	2.2	3	V
V_{T-}	Negative-Going Threshold Voltage	*(Figure 1)*	Normal Operation	−3	−1.1	0	V
			Fail-Safe Operation	0.8	1.4	3	V
$V_{T+}-V_{T-}$	Hysteresis	*(Figure 1)*	Normal Operation	0.8	3.3	6	V
			Fail-Safe Operation	0	0.8	2.2	V
V_{OH}	High-Level Output Voltage	I_{OH} = −400μA, *(Figure 1)*		2.4	3.5		V
V_{OL}	Low-Level Output Voltage	I_{OL} = 16 mA, *(Figure 1)*			0.23	0.4	V
r_I	Input Resistance	*(Figure 2)*	ΔV_I = −25V to −14V	3	5	7	kΩ
			ΔV_I = −14V to −3V	3	5	7	kΩ
			ΔV_I = −3V to +3V	3	6		kΩ
			ΔV_I = 3V to 14V	3	5	7	kΩ
			ΔV_I = 14V to 25V	3	5	7	kΩ
$V_{I(OPEN)}$	Open-Circuit Input Voltage	I_I = 0, *(Figure 3)*		0	0.2	2	V
I_{OS}	Short-Circuit Output Current (Note 5)	V_{CC1} = 5.5V, V_I = −5V, *(Figure 4)*		−10	−20	−40	mA
I_{CC1}	Supply Current From V_{CC1}	V_{CC1} = 5.5V, T_A = 25°C, *(Figure 5)*			20	35	mA
I_{CC2}	Supply Current From V_{CC2}	V_{CC2} = 13.2V, T_A = 25°C, *(Figure 5)*			23	40	mA

switching characteristics (V_{CC1} = 5V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 50 pF, R_L = 390Ω, *(Figure 6)*		22		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 50 pF, R_L = 390Ω, *(Figure 6)*		20		ns
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 50 pF, R_L = 390Ω, *(Figure 6)*		9		ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 50 pF, R_L = 390Ω, *(Figure 6)*		6		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

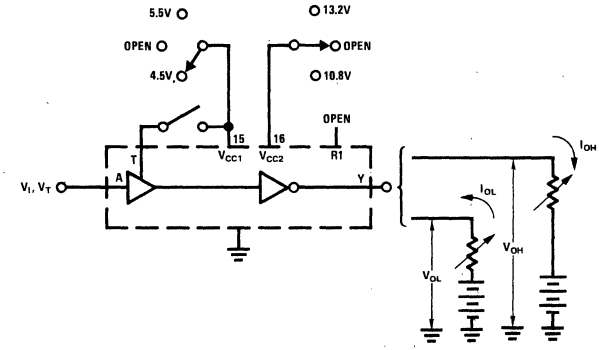
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75154. All typical values are for T_A = 25°C and V_{CC1} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this data sheet for logic and threshold levels only, e.g., when −3V is the maximum, the minimum limit is a more-negative voltage.

Note 5: Only one output at a time should be shorted.

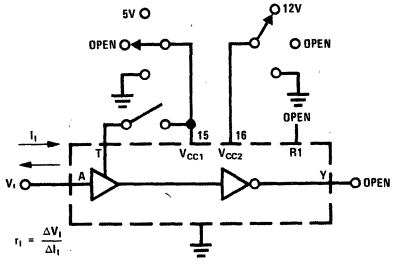
dc test circuits and truth tables



TEST	MEASURE	A	T	Y	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open-Circuit Input (fail-safe)	V_{OH} V_{OH}	Open Open	Open Open	I_{OH} I_{OH}	4.5V Open	Open 10.8V
V_{T+} min, V_{T-} (fail-safe)	V_{OH} V_{OH}	0.8V 0.8V	Open Open	I_{OH} I_{OH}	5.5V Open	Open 13.2V
V_{T+} min (Normal)	V_{OH} V_{OH}	Note 1 Note 1	Pin 15 Pin 15	I_{OH} I_{OH}	5.5V and T T	Open 13.2V
V_{IL} max, V_{T-} min (Normal)	V_{OH} V_{OH}	–3V –3V	Pin 15 Pin 15	I_{OH} I_{OH}	5.5V and T T	Open 13.2V
V_{IH} min, V_{T+} max, V_{T-} max (fail-safe)	V_{OL} V_{OL}	3V 3V	Open Open	I_{OL} I_{OL}	4.5V Open	Open 10.8V
V_{IH} min, V_{T+} max (Normal)	V_{OL} V_{OL}	3V 3V	Pin 15 Pin 15	I_{OL} I_{OL}	4.5V and T T	Open 10.8V
V_{T-} max (Normal)	V_{OL} V_{OL}	Note 2 Note 2	Pin 15 Pin 15	I_{OL} I_{OL}	5.5V and T T	Open 13.2V

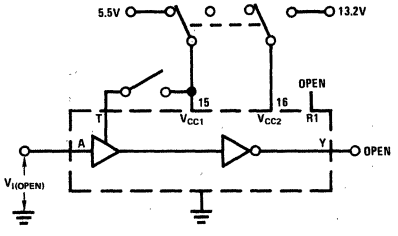
Note 1: Momentarily apply –5V, then 0.8V.
Note 2: Momentarily apply 5V, then ground.

FIGURE 1. V_{IH}, V_{IL}, V_{T+}, V_{T-}, V_{OH}, V_{OL}



T	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open	5V	Open
Open	Gnd	Open
Open	Open	Open
Pin 15	T and 5V	Open
Gnd	Gnd	Open
Open	Open	12V
Open	Open	Gnd
Pin 15	T	12V
Pin 15	T	Gnd
Pin 15	T	Open

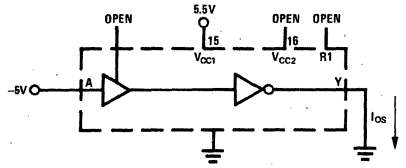
FIGURE 2. r_I



T	V_{CC1} (Pin 15)	V_{CC2} (Pin 16)
Open	5.5V	Open
Pin 15	5.5V	Open
Open	Open	13.2V
Pin 15	T	13.2V

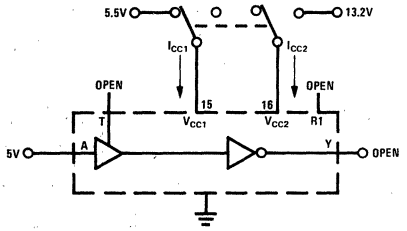
FIGURE 3. $V_{I(OPEN)}$

dc test circuits (con't)



Each output is tested separately.

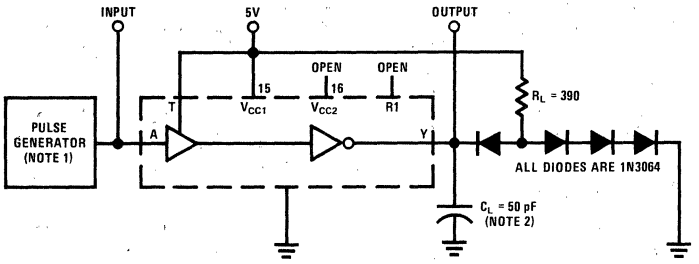
FIGURE 4. I_{OS}

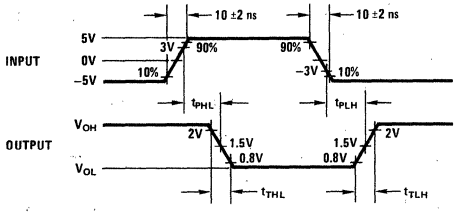


All four line receivers are tested simultaneously.

FIGURE 5. I_{CC}

ac test circuit and switching time waveforms

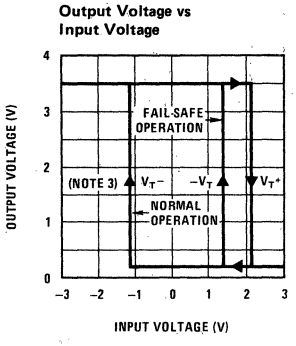




Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, t_W = 200 ns, duty cycle ≤ 20%.
Note 2: C_L includes probe and jig capacitance

FIGURE 6.

typical performance characteristics



Memory/Clock Drivers

DS0025/DS0025C two phase MOS clock driver

general description

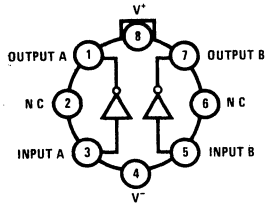
The DS0025/DS0025C is monolithic, low cost, two phase MOS clock driver that is designed to be driven by TTL/DTL line drivers or buffers such as the DM932, DS8830 or DM7440. Two input coupling capacitors are used to perform the level shift from TTL/DTL to MOS logic levels. Optimum performance in turn-off delay and fall time are obtained when the output pulse is logically controlled by the input. However, output pulse widths may be set by selection of the input capacitors eliminating the need for tight input pulse control.

features

- 8-lead TO-5 or 8-lead dual-in-line package
- High Output Voltage Swings—up to 30V
- High Output Current Drive Capability—up to 1.5A
- Rep. Rate: 1.0 MHz into > 1000 pF
- Driven by DM932, DS8830, DM7440 (SN7440)
- "Zero" Quiescent Power

connection diagrams

Metal Can Package

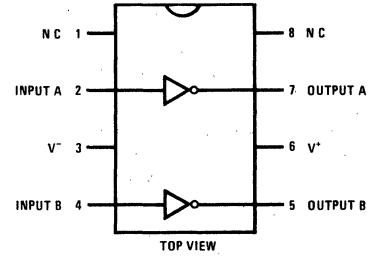


Note: Pin 4 connected to case.

TOP VIEW

Order Number DS0025H or DS0025CH

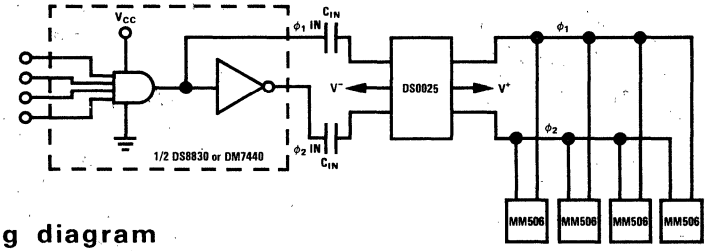
Dual-In-Line Package



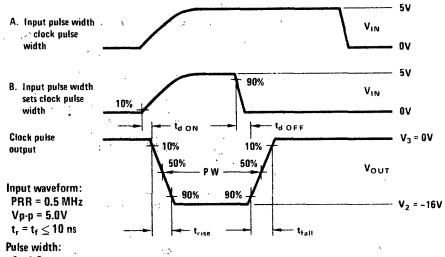
TOP VIEW

Order Number DS0025CN

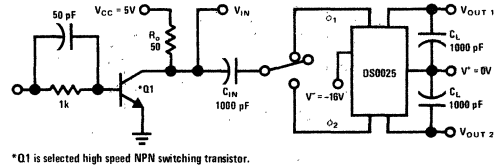
typical application



timing diagram



ac test circuit



*Q1 is selected high speed NPN switching transistor.

absolute maximum ratings (Note 1)

$(V^+ - V^-)$ Voltage Differential	30V
Input Current	100 mA
Peak Output Current	1.5A
Storage Temperature	−65°C to +150°C
Operating Temperature DS0025	−55°C to +125°C
DS0025C	0°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics (Notes 2 and 3) See test circuit.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{dON}	Turn-On Delay Time	C_{IN} = 0.001μF, R_{IN} = 0Ω, C_L = 0.001μF			15	30	ns
t_{RISE}	Rise Time	C_{IN} = 0.001μF, R_{IN} = 0Ω, C_L = 0.001μF			25	50	ns
t_{dOFF}	Turn-Off Delay Time	C_{IN} = 0.001μF, R_{IN} = 0Ω, C_L = 0.001μF, (Note 4)			30	60	ns
t_{FALL}	Fall Time	C_{IN} = 0.001μF, R_{IN} = 0Ω,	(Note 4)	60	90	120	ns
		C_L = 0.001μF	(Note 5)	100	150	250	ns
PW	Pulse Width (50% to 50%)	C_{IN} = 0.001μF, R_{IN} = 0Ω, C_L = 0.001μF (Note 5)			500		ns
V_{O+}	Positive Output Voltage Swing	V_{IN} = 0V, I_{OUT} = −1 mA		V^+−1.0	V^+−0.7V		V
V_{O-}	Negative Output Voltage Swing	I_{IN} = 10 mA, I_{OUT} = 1 mA			V^-+0.7V	V^-+1.5V	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS0025 and across the 0°C to +70°C range for the DS0025C.

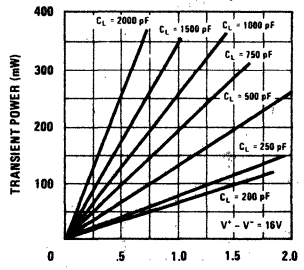
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Parameter values apply for clock pulse width determined by input pulse width.

Note 5: Parameter values for input pulse width greater than output clock pulse width.

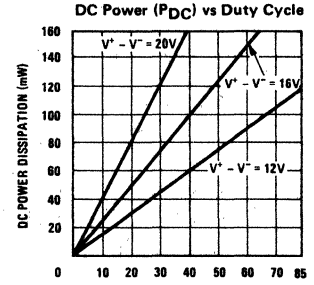
typical performance

Transient Power vs Rep. Rate



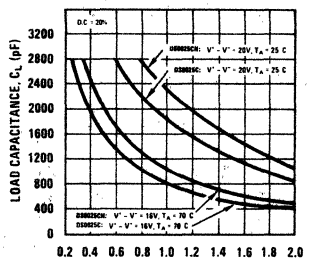
$$P_{AC} = (V^+ - V^-)^2 f C_L$$

DC Power (P_{DC}) vs Duty Cycle



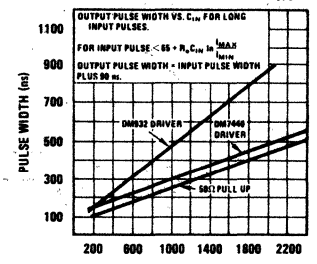
$$P_{DC} = \frac{(V^+ - V^-)^2 (DC)}{1k}$$

Maximum Load Capacitance



$$C_L \leq \frac{(P_{MAX})\,(1k) - (V^+ - V^-)^2\,(DC)}{(f)\,(1k)\,(V^+ - V^-)^2} \leq \frac{(I_{pk})\,(t_r)}{V^+ - V^-}$$

Output PW Controlled by C_{IN}



I_{MAX} = Peak current delivered by driver

$$I_{MIN} \cong \frac{V_{BE}}{R1} = \frac{0.6}{1k}$$

applications information

Circuit Operation

Input current forced into the base of Q_1 through the coupling capacitor C_{IN} causes Q_1 to be driven into saturation, swinging the output to $V^- + V_{CE}(sat) + V_{Diode}$.

When the input current has decayed, or has been switched, such that Q_1 turns off, Q_2 receives base drive through R_2, turning Q_2 on. This supplies current to the load and the output swings positive to $V^+ - V_{BE}$.

It may be noted that Q_1 must switch off before Q_2 begins to supply current, hence high internal transients currents form V^- to V^+ cannot occur.

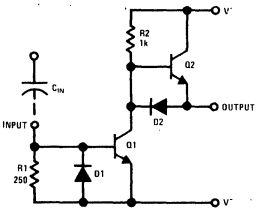


FIGURE 1. DS0025 Schematic (One-Half Circuit)

Fan-Out Calculation

The drive capability of the DS0025 is a function of system requirements, i.e. speed, ambient temperature, voltage swing, drive circuitry, and stray wiring capacity.

The following equations cover the necessary calculations to enable the fan-out to be calculated for any system condition.

Transient Current

The maximum peak output current of the DS0025 is given as 1.5A. Average transient current required from the driver can be calculated from:

$$I = \frac{C_L\ (V^+ - V^-)}{t_r} \qquad (1)$$

Typical rise times into 1000 pF load is 25 ns For $V^+ - V^- = 20V$, I = 0.8A.

Transient Output Power

The average transient power (P_{ac}) dissipated, is equal to the energy needed to charge and discharge the output capacitive load (C_L) multiplied by the frequency of operation (f).

$$P_{AC} = C_L \times (V^+ - V^-)^2 \times f \qquad (2)$$

For $V^+ - V^- = 20V$, f = 1.0 MHz, C_L = 1000 pF, P_{AC} = 400 mW.

Internal Power

"0" State Negligible (<3 mW)

"1" State

$$P_{int} = \frac{(V^+ - V^-)^2}{R_2} \times \text{Duty Cycle} \qquad (3)$$

= 80 mW for $V^+ - V^- = 20V$, DC = 20%

Package Power Dissipation

Total average power = transient output power + internal power

example calculation

How many MM506 shift registers can be driven by a DS0025CN driver at 1 MHz using a clock pulse width of 200 ns, rise time 30-50 ns and 16V amplitude over the temperature range 0-70°C?

Power Dissipation:

At 70°C the DS0025CN can dissipate 870 mW when soldered into printed circuit board.

Transient Peak Current Limitation:

From equation (1), it can be seen that at 16V and 30 ns, the maximum load that can be driven is limited to 2800 pF.

Average Internal Power:

Equation (3), gives an average power of 50 mW at 16V and a 20% duty cycle.

For one-half of the DS0025C, 870 mW ÷ 2 can be dissipated.

435 mW = 50 mW + transient output power

385 mW = transient output power

Using equation (2) at 16V, 1 MHz and 350 mW, each half of the DS0025CN can drive a 1367 pF load. This is less than the load imposed by the transient current limitation of equation (1) and so a maximum load of 1367 pF would prevail.

From the data sheet for the MM506, the average clock pulse load is 80 pF. Therefore the number of devices driven is 1367/80 or 17 registers.

NATIONAL

DS0026, DS0056 5 MHz two phase MOS clock drivers

general description

DS0026/DS0056 are low cost monolithic high speed two phase MOS clock drivers and interface circuits. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. They may be driven from standard 54/74 series and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The DS0026 and DS0056 are intended for applications in which the output pulse width is logically controlled; i.e., the output pulse width is equal to the input pulse width.

The DS0026/DS0056 are designed to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon-gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for a 8k by 16-bit 1103 RAM memory system. Information on the correct usage of the DS0026 in these as well as other systems is included in the application note AN-76A.

The DS0026 and DS0056 are identical except each driver in the DS0056 is provided with a V_{BB} connection to supply a higher voltage to the output stage. This aids in pulling up the output when it is in the high state. An external resistor tied between these extra pins and a supply higher than V^+ will cause the output to pull up to ($V^+ - 0.1V$) in the off state.

For DS0056 applications, it is required that an external resistor be used to prevent damage to the device when the driver switches low. A typical V_{BB} connection is shown on the next page.

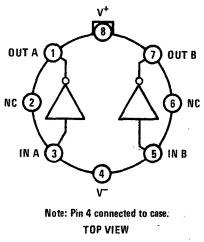
These devices are available in 8-lead TO-5, one watt copper lead frame 8-pin mini-DIP, and one and a half watt ceramic DIP, and TO-8 packages.

features

- Fast rise and fall times—20 ns with 1000 pF load
- High output swing—20V
- High output current drive—±1.5 amps
- TTL/DTL compatible inputs
- High rep rate—5 to 10 MHz depending on power dissipation
- Low power consumption in MOS "0" state—2 mW
- Drives to 0.4V of GND for RAM address drive

connection diagrams

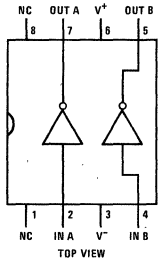
TO-5 Package



Note: Pin 4 connected to case.
TOP VIEW

Order Number DS0026H or DS0026CH

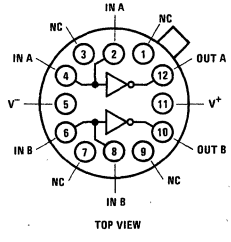
Dual-In-Line Package



TOP VIEW

Order Number DS0026CN

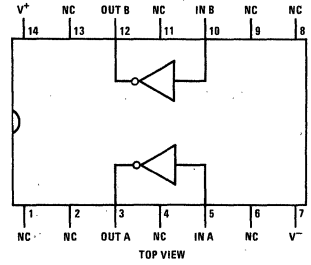
TO-8 Package



TOP VIEW

Order Number DS0026G or DS0026CG

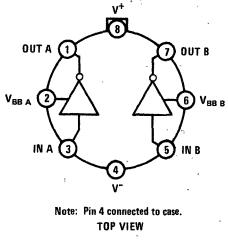
Dual-In-Line Package



TOP VIEW

Order Number DS0026J, DS0026CJ or DS0026W

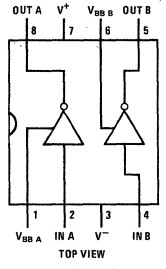
TO-5 Package



Note: Pin 4 connected to case.
TOP VIEW

Order Number DS0056H or DS0056CH

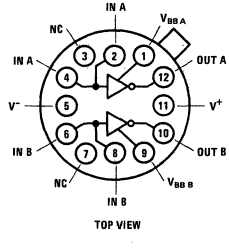
Dual-In-Line Package



TOP VIEW

Order Number DS0056CN

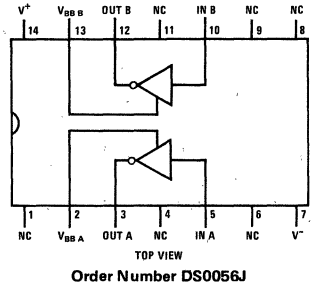
TO-8 Package



TOP VIEW

Order Number DS0056G or DS0056CG

Dual-In-Line Package



TOP VIEW

Order Number DS0056J or DS0056CJ

absolute maximum ratings (Note 1)

$V^+ - V^-$ Differential Voltage	22V
Input Current	100 mA
Input Voltage ($V_{IN} - V^-$)	5.5V
Peak Output Current	1.5A

Operating Temperature Range	
DS0026, DS0056	−55°C to +125°C
DS0026C, DS0056C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logic "1" Input Voltage	$V^- = 0V$		2	1.5		V
I_{IH}	Logic "1" Input Current	$V_{IN} - V^- = 2.4V$			10	15	mA
V_{IL}	Logic "0" Input Voltage	$V^- = 0V$			0.6	0.4	V
I_{IL}	Logic "0" Input Current	$V_{IN} - V^- = 0V$			−3	−10	μA
V_{OL}	Logic "1" Output Voltage	$V_{IN} - V^- = 2.4V$			V^-+0.7	V^-+1.0	V
V_{OH}	Logic "0" Output Voltage	$V_{IN} - V^- = 0.4V$, $V_{BB} \geq V^+ + 1.0V$	DS0026	V^+−1.0	V^+−0.7		V
			DS0056	V^+−0.3	V^+−0.1		V
$I_{CC(ON)}$	"ON" Supply Current	$V^+ - V^- = 20V$ $V_{IN} - V^- = 2.4V$	DS0026		30	40	mA
		(Note 6) (one side on)	DS0056		12	30	mA
$I_{CC(OFF)}$	"OFF" Supply Current	$V^+ - V^- = 20V$, $V_{IN} - V^- = 0V$			10	100	μA
					50	500	μA

switching characteristics ($T_A = 25°C$) (Notes 5 and 7)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{ON}	Turn-on Delay	*(Figure 1)*		5	7.5	12	ns
		(Figure 2)			11		ns
t_{OFF}	Turn-off Delay	*(Figure 1)*			12	15	ns
		(Figure 2)			13		ns
t_r	Rise Time	*(Figure 1)*,	C_L = 500 pF		15	18	ns
		(Note 5)	C_L = 1000 pF		20	35	ns
		(Figure 2),	C_L = 500 pF		30	40	ns
		(Note 5)	C_L = 1000 pF		36	50	ns
t_f	Fall Time	*(Figure 1)*,	C_L = 500 pF		12	16	ns
		(Note 5)	C_L = 1000 pF		17	25	ns
		(Figure 2),	C_L = 500 pF		28	35	ns
		(Note 5)	C_L = 1000 pF		31	40	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These specifications apply for $V^+ - V^-$ = 10V to 20V, C_L = 1000 pF, over the temperature range of −55°C to +125°C for the DS0026, DS0056 and 0°C to +70°C for the DS0026C, DS0056C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

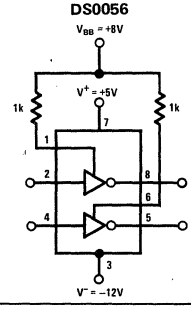
Note 4: All typical values for the $T_A = 25°C$.

Note 5: Rise and fall time are given for MOS logic levels; i.e., rise time is transition from logic "0" to logic "1" which is voltage fall.

Note 6: I_{BB} for DS0056 is approximately $(V_{BB} - V^-)/1\ k\Omega$ (for one side) when output is low.

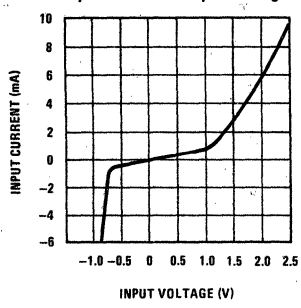
Note 7: The high current transient (as high as 1.5A) through the resistance of the external interconnecting V^- lead during the output transition from the high state to the low state can appear as negative feedback to the input. If the external interconnecting lead from the driving circuit to V^- is electrically long, or has significant dc resistance, it can subtract from the switching response.

typical V_{BB} connection

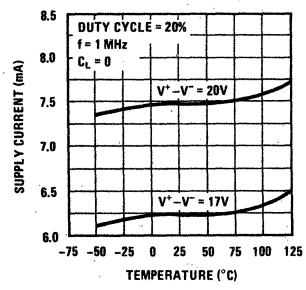


typical performance characteristics

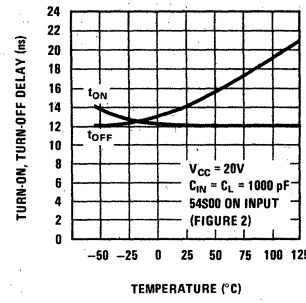
Input Current vs Input Voltage



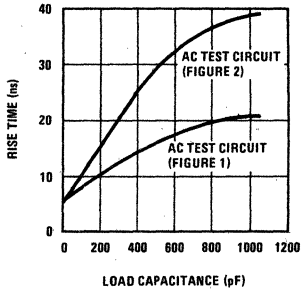
Supply Current vs Temperature



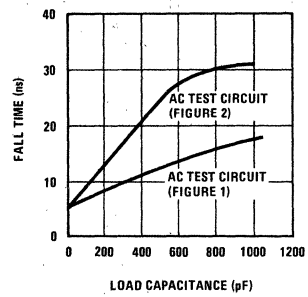
Turn-On and Turn-Off Delay vs Temperature



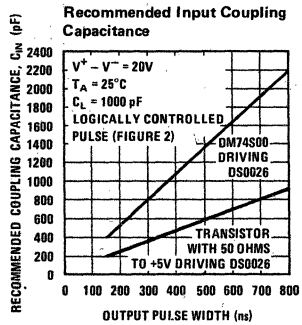
Rise Time vs Load Capacitance



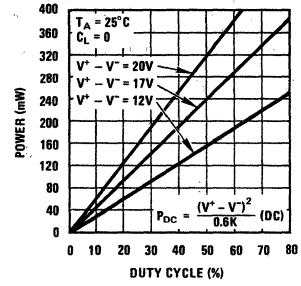
Fall Time vs Load Capacitance



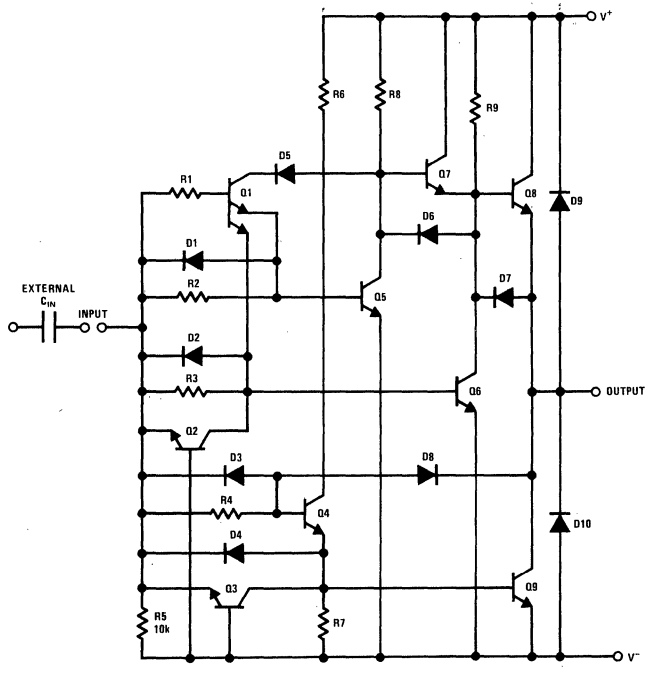
Recommended Input Coupling Capacitance



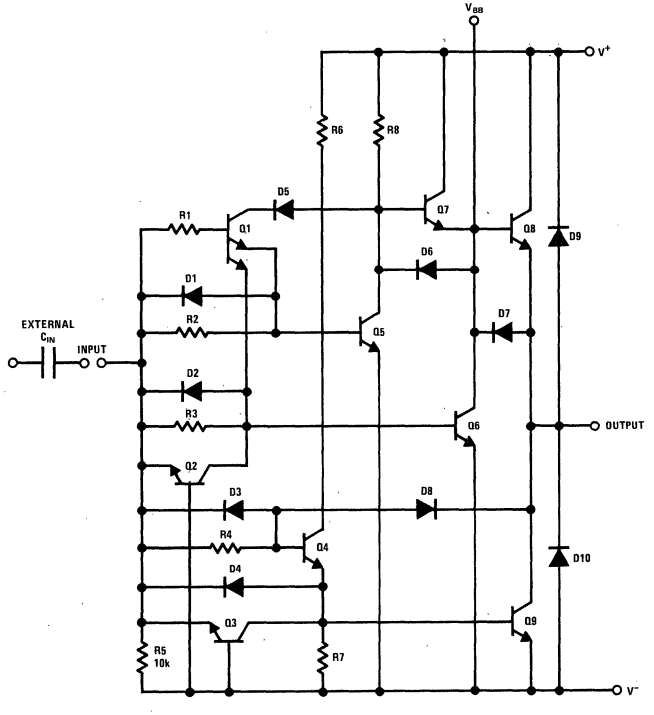
DC Power (P_{DC}) vs Duty Cycle



schematic diagrams

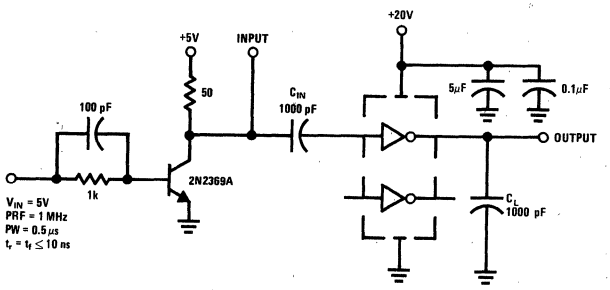


1/2 DS0026



1/2 DS0056

ac test circuits and switching time waveforms



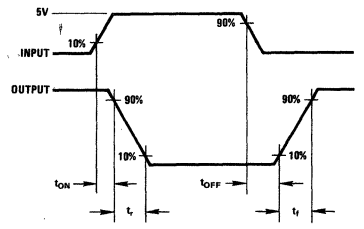
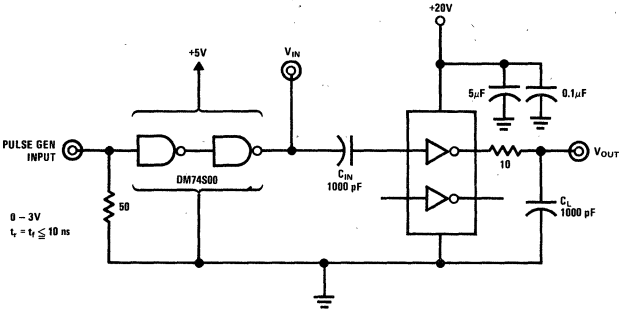


FIGURE 1.



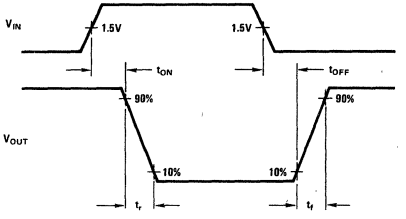
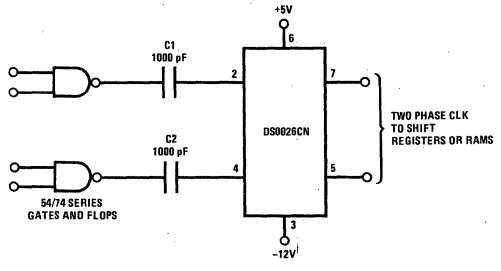


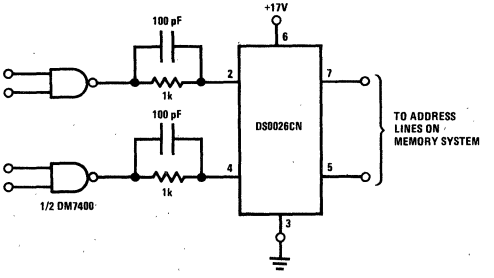
FIGURE 2.

typical applications

AC Coupled MOS Clock Driver



DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)



application hints

DRIVING THE MM5262 WITH THE DS0056 CLOCK DRIVER

The clock signals for the MM5262 have three requirements which have the potential of generating problems for the user. These requirements, high speed, large voltage swing and large capacitive loads, combine to provide ample opportunity for inductive ringing on clock lines, coupling clock signals to other clocks and/or inputs and outputs and generating noise on the power supplies. All of these problems have the potential of causing the memory system to malfunction. Recognizing the source and potential of these problems early in the design of a memory system is the most critical step. The object here is to point out the source of these problems and give a quantitative feel for their magnitude.

Line ringing comes from the fact that at a high enough frequency any line must be considered as a transmission line with distributed inductance and capacitance. To see how much ringing can be tolerated we must examine the clock voltage specification. *Figure 6* shows the clock

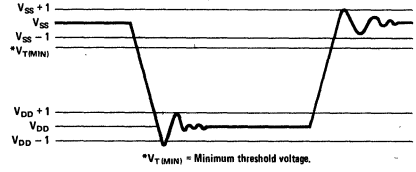


FIGURE 6. Clock Waveform

specification, in diagram form, with idealized ringing sketched in. The ringing of the clock about the V_{SS} level is particularly critical. If the $V_{SS} - 1$ V_{OH} is not maintained, at *all* times, the information stored in the memory could be altered. Referring to *Figure 1*, if the threshold voltage of a transistor were −1.3V, the clock going to $V_{SS} - 1$ would mean that all the devices, whose gates are tied to that clock, would be only 300 mV from turning on. The internal circuitry needs this noise margin and from the functional description of the RAM it is easy to see that turning a clock on at the wrong time can have disastrous results.

Controlling the clock ringing is particulary difficult because of the relative magnitude of the allowable ringing, compared to the magnitude of the transition. In this case it is 1V out of 20V or only 5%. Ringing can be controlled by damping the clock driver and minimizing the line inductance.

Damping the clock driver by placing a resistance in series with its output is effective, but there is a limit since it also slows down the rise and fall time of the clock signal. Because the typical clock driver can be much faster than the worst case driver, the damping resistor serves the useful function of limiting the minimum rise and fall time. This is very important because the faster the rise and fall times, the worse the ringing problem becomes. The size of the damping resistor varies because it is dependent on the details of the actual application. It must be determined empirically. In practice a resistance of 10 ohms to 20 ohms is usually optimum.

Limiting the inductance of the clock lines can be accomplished by minimizing their length and by laying out the lines such that the return current is closely coupled to the clock lines. When minimizing the length of clock lines it is important to minimize the distance from the clock driver output to the furthest point being driven. Because of this, memory boards are usually designed with clock drivers in the center of the memory array, rather than on one side, reducing the maximum distance by a factor of 2.

Using multilayer printed circuit boards with clock lines sandwiched between the V_{DD} and V_{SS} power plains minimizes the inductance of the clock lines. It also serves the function of preventing the clocks from coupling noise into input and output lines. Unfortunately multilayer printed circuit boards are more expensive than two sided boards. The user must make the decision as to the necessity of multilayer boards. Suffice it to say here, that reliable memory boards can be designed using two sided printed circuit boards.

The recommended clock driver for use with the MM4262/MM5262 is the DS0056/DS0056C dual clock driver. This device is designed specifically for use with dynamic circuits using a substrate, V_{BB}, supply. Typically it will drive a 1000 pF load with 20 ns rise and fall times. *Figure 7* shows a schematic of a single driver.

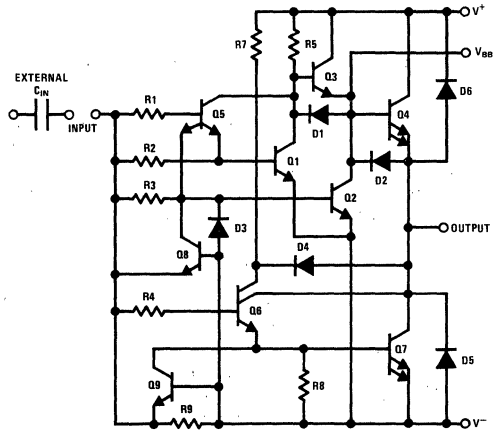


FIGURE 7. Schematic of 1/2 DS0056

In the case of the MM5262, V^+ is a +5V and V_{BB} is +8.5V. V_{BB} should be connected to the V_{BB} pin shown in *Figure 7* through a 1 kΩ resistor. This allows transistor Q4 to saturate, pulling the output to within a $V_{CE(SAT)}$ of the V^+ supply. This is critical because as was shown before, the $V_{SS} - 1.0$V clock level must not be exceeded at any time. Without the V_{BB} pull up on the base of Q4 the output at best will be 0.6V below the V^+ supply and can be 1V below the V^+ supply reducing the noise margin or this line to zero.

application hints (cont')

Because of the amount of current that the clock driver must supply to its capacitive load, the distribution of power to the clock driver must be considered. *Figure 8* gives the idealized voltage and current waveforms for a clock driver driving a 1000 pF capacitor with 20 ns rise and fall time.

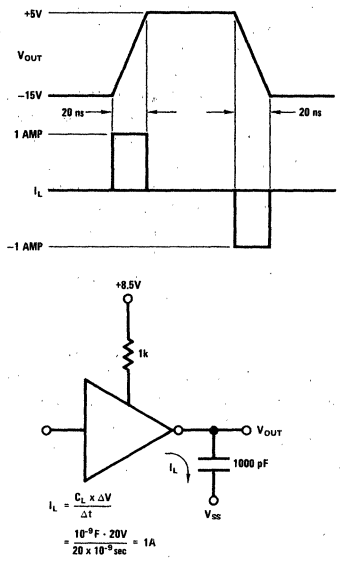


FIGURE 8. Clock Waveforms (Voltage and Current)

As can be seen the current is significant. This current flows in the V_{DD} and V_{SS} power lines. Any significant inductance in the lines will produce large voltage transients on the power supplies, A bypass capacitor, as close as possible to the clock driver, is helpful in minimizing this problem. This bypass is most effective when connected between the V_{SS} and V_{DD} supplies. A bypass capacitor for each DS0056 is recommended. The size of the bypass capacitor depends on the amount of capacitance being driven. Using a low inductance capacitor, such as a ceramic or silver mica, is most effective. Another helpful technique is to run the V_{DD} and V_{SS} lines, to the clock driver, adjacent to each other. This tends to reduce the lines inductance and therefore the magnitude of the voltage transients.

While discussing the clock driver, it should be pointed out that the DS0056 is a relatively low input impedance device. It is possible to couple current noise into the input without seeing a significant voltage. Since this noise is difficult to detect with an oscilloscope it is often overlooked.

Lastly, the clock lines must be considered as noise generators. *Figure 9* shows a clock coupled through a parasitic coupling capacitor, C_C, to eight data input lines being driven by a 7404. A parasitic lumped line inductance, L, is also shown. Let us assume, for the sake of argument, that C_C is 1 pF and that the rise time of the clock is high enough to completely isolate the clock tranisent from the 7404 because of the inductance, L.

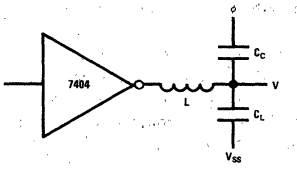


FIGURE 9. Clock Coupling

With a clock transition of 20V the magnitude of the voltage generated across C_L is:

$$V = 20V \times \frac{C_C}{C_L + C_C} = 20V \times \left(\frac{1}{56+1}\right) = 0.35V$$

This has been a hypothetical example to emphasize that with 20V low rise/fall time transitions, parasitic elements can not be neglected. In this example, 1 pF of parasitic capacitance could cause system malfunction, because a 7404 without a pull up resistor has typically only 0.3V of noise margin in the "1" state at 25°C. Of course it is stretching things to assume that the inductance, L, completely isolates the clock transient from the 7404. However, it does point out the need to minimize inductance in input/output as well as clock lines.

The output is current, so it is more meaningful to examine the current that is coupled through a 1 pF parasitic capacitance. The current would be:

$$I = C_C \times \frac{\Delta V}{\Delta t} = \frac{1 \times 10^{-12} \times 20}{20 \times 10^{-9}} = 1\ mA$$

This exceeds the total output current swing so it is obviously significant.

Clock coupling to inputs and outputs can be minimized by using multilayer printed circuit boards, as mentioned previously, physically isolating clock lines and/or running clock lines at right angles to input/output lines. All of these techniques tend to minimize parasitic coupling capacitance from the clocks to the signals in question.

In considering clock coupling it is also important to have a detailed knowledge of the functional characteristics of the device being used. As an example, for the MM5262, coupling noise from the $\phi 2$ clock to the address lines is of no particular consequence. On the other hand the address inputs will be sensitive to noise coupled from $\phi 1$ clock.

Memory/Clock Drivers

DS3629 memory driver with decode inputs

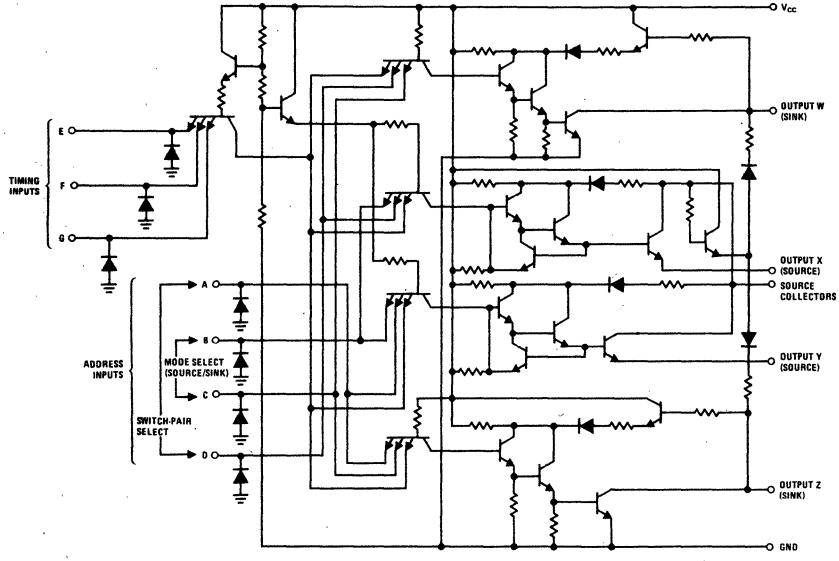
general description

The DS3629 is a monolithic memory driver which features two 400 mA (source/sink) switch pairs along with decoding capability from four address lines. Inputs B and C function as mode selection lines (source or sink) while lines A and D are used for switch-pair selection (output pair Y/Z or W/X). The DS3629 has the same pin-out and function as the DS75324 except that the source emitter voltage capability has been raised from 3V to 7V. This allows the DS3629 to drive larger memory systems at the same current levels of the DS75324.

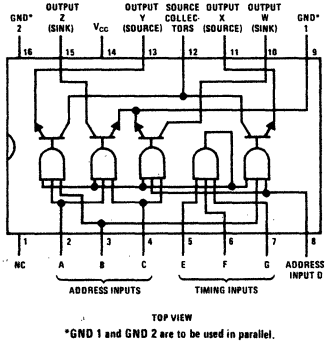
features

- Source emitter voltage of 7V (max) at 400 mA source
- Identical pin-out and function as DS75324
- 400 mA output capability
- High voltage outputs
- Dual sink/source outputs
- Internal decoding and timing circuitry
- Fast switching times
- DTL/TTL compatible
- Input clamping diodes

schematic and connection diagrams



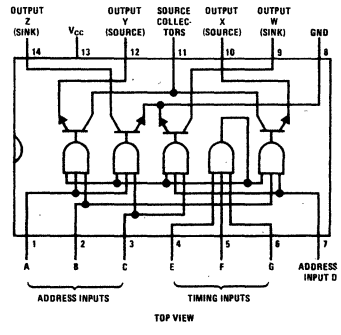
Dual-In-Line Package



*GND 1 and GND 2 are to be used in parallel.

Order Number DS3629J

Dual-In-Line Package



Order Number DS3629N

absolute maximum ratings (Note 1)

Supply Voltage V_{CC} (Note 4)	17V
Input Voltage (Note 5)	5.5V
Operating Case Temperature Range	0°C to +70°C
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics (Notes 2 and 3) (V_{CC} = 14V, T_C = 0°C to +70°C unless otherwise noted)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Input Voltage Required to Insure Logical "1" At Any Input	*(Figure 1)*			3.5			V
$V_{IN(0)}$	Input Voltage Required to Insure Logical "0" At Any Input	*(Figure 1)*					0.8	V
$I_{IN(1)}$	Logical "1" Level Input Current	V_{IN} = 5V, *(Figure 1)*		Address Input			200	μA
				Timing Input			100	μA
$I_{IN(0)}$	Logical "0" Level Input Current	V_{IN} = 0V, *(Figure 1)*		Address Input			−6	mA
				Timing Input			−12	mA
V_{SAT}	Saturation Voltage	*(Figure 2)*	$I_{SINK} \simeq$ 420 mA, R_L = 53Ω	Sink		0.75	0.85	V
			$I_{SOURCE} \simeq$ 420 mA, R_L = 39.0Ω	Source		0.75	0.85	V
I_{OFF}	Output Reverse Current ("OFF" State)	V_{IN} = 0V, *(Figure 1)*				125	200	μA
I_{CC}	Supply Current	V_{IN} = 0V, *(Figure 3)*		All Sources and Sinks "OFF"		12.5	15	mA
		(Figure 4)		Either Sink Selected		30	40	mA
				Either Source Selected		25	35	mA
V_I	Input Clamp Voltage	I_{IN} = −12 mA, T_A = 25°C					−1.5	V

ac electrical characteristics (V_{CC} = 14V, T_C = 25°C)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
t_{pd1}	Propagation Delay Time to Logical "1" Level	C_L = 20 pF	R_{L1} = 53Ω, R_{L2} = 500Ω, *(Figure 5)*	Source Output			90	ns
			R_L = 53Ω, *(Figure 6)*	Sink Output			110	ns
t_{pd0}	Propagation Delay Time to Logical "0" Level	C_L = 20 pF	R_{L1} = 53Ω, R_{L2} = 500Ω, *(Figure 5)*	Source Output			50	ns
			R_L = 53Ω, *(Figure 6)*	Sink Output			40	ns
t_s	Sink Storage Time	R_L = 53Ω, C_L = 20 pF, *(Figure 6)*					70	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS3629. All typical values are for T_A = 25°C and V_{CC} = 14V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

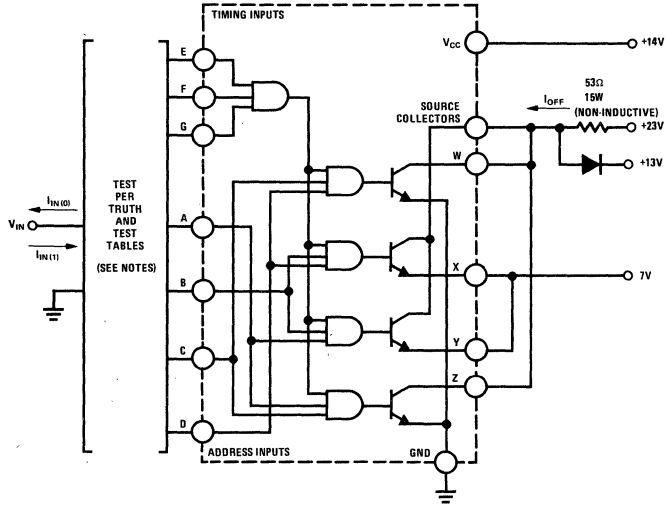
Note 4: Voltage values are with respect to network ground terminal.

Note 5: Input signals must be zero or positive with respect to network ground terminal.

truth table

INPUTS							OUTPUTS			
ADDRESS				TIMING			SINK	SOURCES		SINK
A	B	C	D	E	F	G	W	X	Y	Z
0	0	1	1	1	1	1	ON	OFF	OFF	OFF
0	1	0	1	1	1	1	OFF	ON	OFF	OFF
1	1	0	0	1	1	1	OFF	OFF	ON	OFF
1	0	1	0	1	1	1	OFF	OFF	OFF	ON
X	X	X	X	0	X	X	OFF	OFF	OFF	OFF
X	X	X	X	X	0	X	OFF	OFF	OFF	OFF
X	X	X	X	X	X	0	OFF	OFF	OFF	OFF

test circuits and switching time waveforms



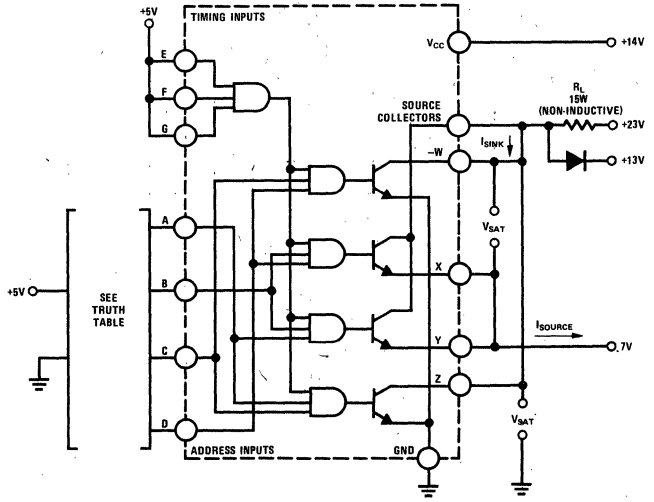
Note 1: Check $V_{IN(1)}$ and $V_{IN(0)}$ per truth table.
Note 2: Measure $I_{IN(0)}$ per test table.
Note 3: When measuring $I_{IN(1)}$, all other inputs are at ground. Each input is tested separately.

TEST TABLE FOR $I_{IN(0)}$

APPLY 3.5V	GROUND	TEST $I_{IN(0)}$
B, C, E, F, and G	A and D	A
B, C, E, F, and G	A and D	D
A, D, E, F, and G	B and C	B
A, D, E, F, and G	B and C	C
A, B, C, D, F, and G	E	E
A, B, C, D, E, and G	F	F
A, B, C, D, E, and F	G	G

FIGURE 1. $V_{IN(0)}$, $V_{IN(1)}$, $I_{IN(0)}$, $I_{IN(1)}$ and I_{OFF}

test circuits and switching time waveforms (con't)



Note: This parameter must be measured using pulse techniques.
t_p = 500 ns, duty cycle $\leq$ 1%.

FIGURE 2. $V_{(SAT)}$

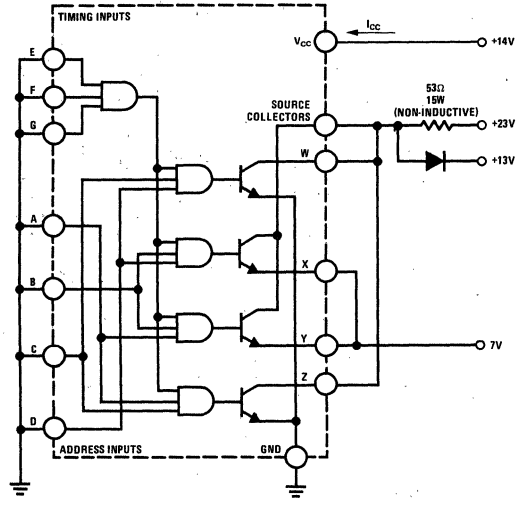
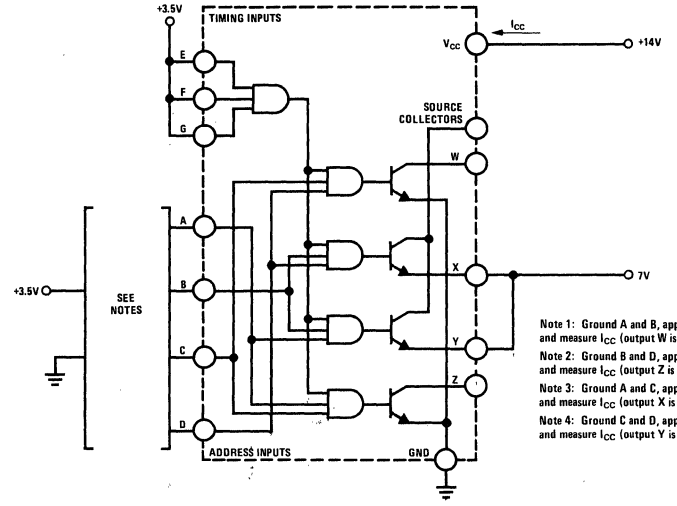


FIGURE 3. I_{CC} (All Outputs OFF)

test circuits and switching time waveforms (con't)



Note 1: Ground A and B, apply +3.5V, to C and D, and measure I_{CC} (output W is on).

Note 2: Ground B and D, apply +3.5V to A and C, and measure I_{CC} (output Z is on).

Note 3: Ground A and C, apply +3.5V to B and D, and measure I_{CC} (output X is on).

Note 4: Ground C and D, apply +3.5V to A and B, and measure I_{CC} (output Y is on).

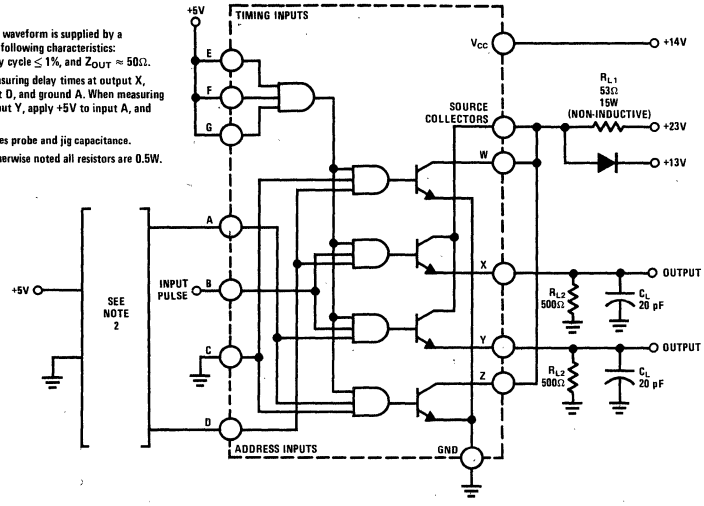
FIGURE 4. I_{CC} (One Output ON)

Note 1: The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10$ ns, duty cycle $\leq 1\%$, and $Z_{OUT} \approx 50\Omega$.

Note 2: When measuring delay times at output X, apply +5V to input D, and ground A. When measuring delay times at output Y, apply +5V to input A, and ground D.

Note 3: C_L includes probe and jig capacitance.

Note 4: Unless otherwise noted all resistors are 0.5W.



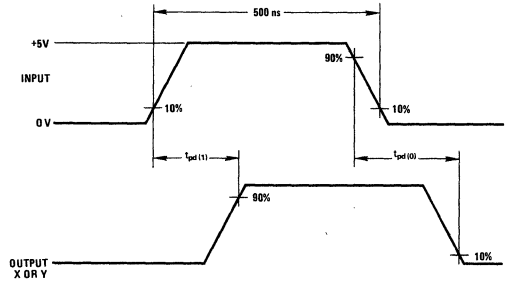
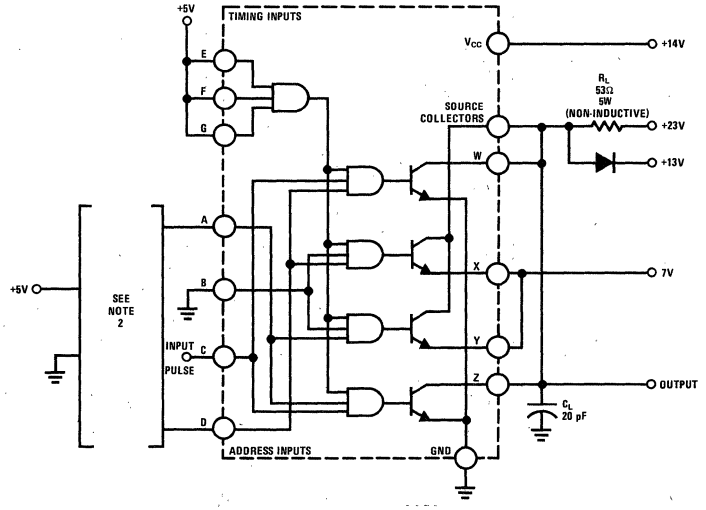


FIGURE 5. Source-Output Switching Times

test circuits and switching time waveforms (con't)



Note 1: The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10$ ns, duty cycle $\leq 1\%$, $Z_{OUT} \approx 50\Omega$.

Note 2: When measuring delay times at output W, apply +5V to input D, and ground A. When measuring delay times at output Z, apply +5V to input A, and ground D.

Note 3: C_L includes probe and jig capacitance.

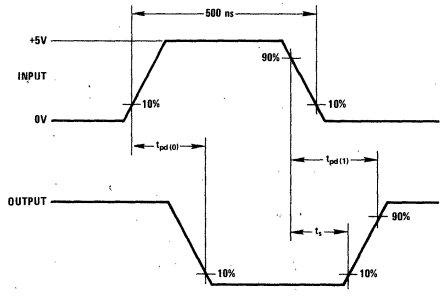


FIGURE 6. Sink-Output Switching Times

NATIONAL

Memory/Clock Drivers

Advance Information*

DS1640/DS3640, DS1670/DS3670 quad MOS TRI-SHARE™ port drivers

general description

The DS1640/DS3640 and DS1670/DS3670 are quad MOS TRI-SHARE port drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input current, allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay.

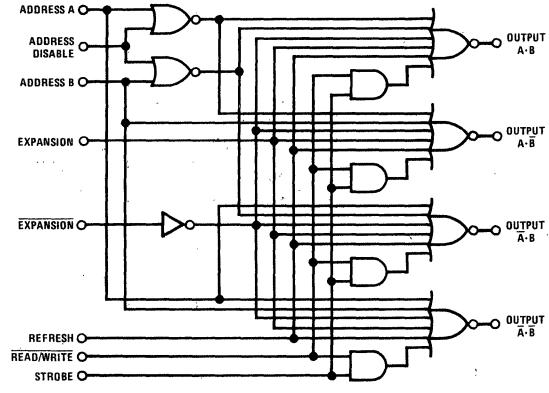
The DS1640/DS3640 has a 15 ohm resistor in series with the outputs to dampen transients caused by the fast switching output circuit. The DS1670/DS3670 has a direct, low impedance output source for use with or without an external resistor.

The DS1640/DS1670 has two address inputs which decode to one-of-four-high outputs. Provisions are made for address expansion. For example, two packages may be used to implement a three-input, eight-output decoder. Also included is a refresh control, read/write, and strobe input. These functions are required by the MM5270 4k TRI-SHARE MOS RAM.

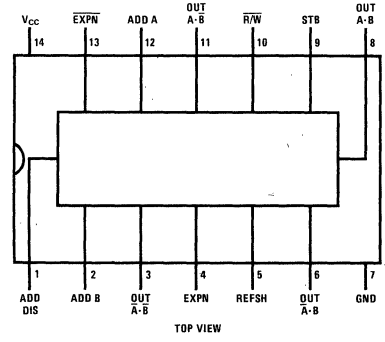
features

- TRI-SHARE port driver for MM5270 RAM
- TTL/DTL compatible inputs
- PNP inputs minimize loading
- Capacitance-driving outputs
- Built-in damping resistor (DS1640/DS3640)

logic and connection diagrams



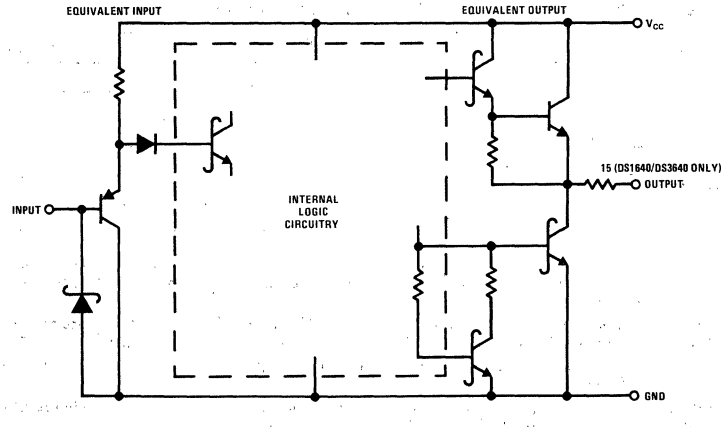
Dual-In-Line Package



TOP VIEW

Order Number DS1640J, DS1670J, DS3640J, DS3670J or DS3640N, DS3670N

schematic diagram



*Specifications may change.

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7V
Logical "1" Input Voltage, $V_{IN(1)}$	7V
Logical "0" Input Voltage, $V_{IN(0)}$	−1.5V
Logical "1" Output Current, $I_{OS(1)}$	1A
Logical "0" Output Current, $I_{OS(0)}$	1A
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation (P_D)	
Ceramic Package	1160 mW
Molded Package	1000 mW

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1640, DS1670	−55	+125	°C
DS3640, DS3670	0	+70	°C

* Derate ceramic package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C.

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage				2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage						0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V	Address Disable, $\overline{\text{Expansion}}$ Inputs			0.1	40	μA
			Address Inputs			0.3	120	μA
			Other Inputs			0.4	160	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.5V	Address Disable, $\overline{\text{Expansion}}$ Inputs			−90	−250	μA
			Address Inputs			−270	−750	μA
			Other Inputs			−360	−1000	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA					−1.2	V
$V_{OH(NL)}$	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = 0 mA			3.4	4.25		V
$V_{OL(NL)}$	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 0 mA				0.25	0.45	V
$V_{OH(WL)}$	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA		DS1640/DS3640	2.4	3.5		V
				DS1670/DS3670	2.5	3.5		V
$V_{OL(WL)}$	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA		DS1640/DS3640		0.6	1.1	V
				DS1670/DS3670		0.3	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V, (Note 4)				−170		mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V, (Note 4)				170		mA
$I_{CC(MAX)}$	Maximum Power Supply Current	V_{CC} = 5.5V				60		mA
$I_{CC(MIN)}$	Minimum Power Supply Current	V_{CC} = 5.5V				45		mA

switching characteristics T_A = 25°C, V_{CC} = 5V, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$t_{pd(0)}$	Propagation Delay to Logical "0" (Note 4)	C_L = 50 pF		7		ns
		C_L = 250 pF		15		ns
		C_L = 500 pF		25		ns
$t_{pd(1)}$	Propagation Delay to Logical "1" (Note 4)	C_L = 50 pF		7		ns
		C_L = 250 pF		15		ns
		C_L = 500 pF		25		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1640 and DS1670 and across the 0°C to +70°C range for the DS3640 and DS3670. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

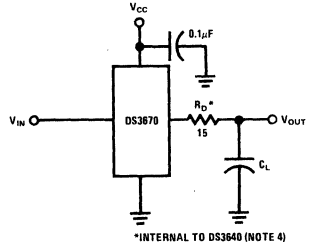
Note 4: When measuring output drive current and switching response for the DS1670 and DS3670 a 15 ohm resistor should be placed in series with each output. This resistor is internal to the DS1640/DS3640, and need not be added.

truth table

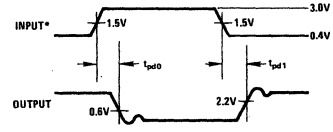
ADD A	ADD B	ADD DSBL	EXPAN	$\overline{\text{EXPAN}}$	RFSH	$\overline{\text{R/W}}$	STB	OUT $\overline{A} \cdot \overline{B}$	OUT $\overline{A} \cdot B$	OUT $A \cdot \overline{B}$	OUT $A \cdot B$
0	0	0	0	1	0	*	*	1	0	0	0
0	1	0	0	1	0	*	*	0	1	0	0
1	0	0	0	1	0	*	*	0	0	1	0
1	1	0	0	1	0	*	*	0	0	0	1
0	0	1	0	1	0	*	*	1	1	1	1
X	X	X	1	X	X	X	X	0	0	0	0
X	X	X	X	0	X	X	X	0	0	0	0
X	X	X	X	X	1	X	X	0	0	0	0
X	X	X	X	X	X	1	1	0	0	0	0

X = Don't Care; * = $\overline{\text{read/write}}$ and strobe not both high at same time.

ac test circuit and switching time waveforms



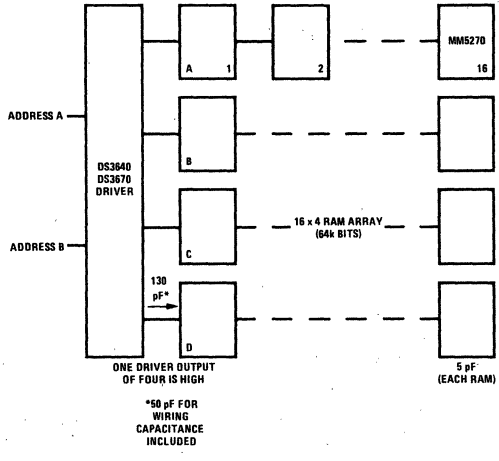
*INTERNAL TO DS3640 (NOTE 4)



*Input frequency = 1 MHz, duty cycle = 50%, $t_r = t_f$ 2.5 ns

typical application

The DS3640/DS3670 driver is intended for use in driving the TRI-SHARE port of the MM5270 4k MOS RAM. Its address inputs facilitate decoding, and its direct controls simplify the refresh cycle.



NATIONAL

Memory/Clock Drivers

Advance Information*

DS1642/DS3642, DS1672/DS3672 dual bootstrapped MOS clock driver

general description

The DS1672 is a dual bipolar-to-MOS clock driver designed to provide high output current and voltage capabilities necessary for driving high capacitance (up to 500 pF) MOS memory systems. The circuit needs only one power supply, (12V typical). This feature greatly reduces high stand-by power levels and at the same time simplifies system design.

The circuit also features output bootstrapping capability. This feature eliminates the need for an additional high level supply to provide a higher voltage to the output stage. The function is accomplished by connecting a small value capacitor (typically 200 pF) from each output to each driver's bootstrap pin.

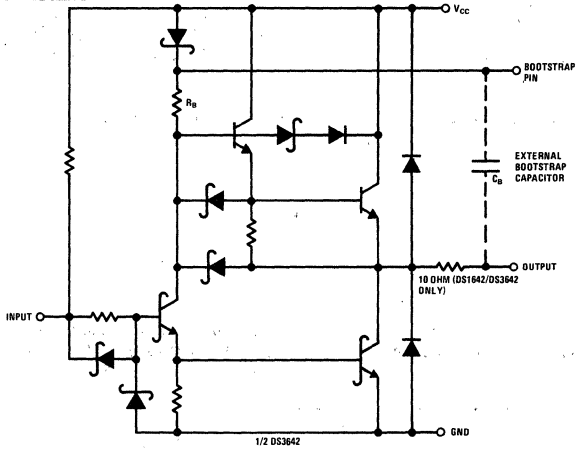
The circuit has Schottky-clamped transistor logic for minimum propagation delay. Typical stand-by power (output low) is 45 mW per driver. A fail-safe condition is provided for in the circuit, so if the input is opened the output assumes the logic "0" state.

The DS1642/DS3642 has a 10 ohm resistor in series with each output to dampen transients caused by the fast-switching output. The DS1672/DS3672 has a direct low impedance output for use with or without an external resistor.

features

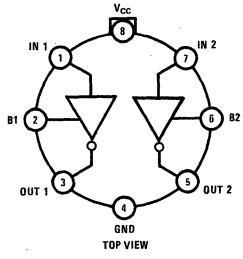
- 15V output voltage capability
- TTL/DTL compatible inputs
- High speed operation
- Bootstrapping eliminates extra supplies—reduces power
- 45 mW/driver stand-by power
- Built-in 10 ohm damping resistor (DS1642/DS3642)

schematic diagram



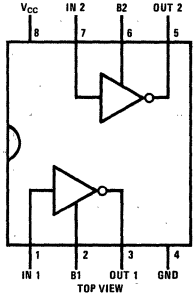
connection diagrams

Metal Can Package



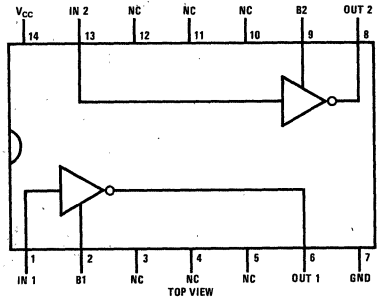
Order Number DS1642H, DS3642H, DS1672H or DS3672H

Dual-In-Line Package



Order Number DS3642N or DS3672N

Dual-In-Line Package



Order Number DS1642J, DS3642J, DS1672J or DS3672J

*Specifications may change.

absolute maximum ratings (Note 1)

Supply Voltage	15V
Bootstrap–V_{CC} Differential	15V
Bootstrap Pin Voltage	30V
Input Voltage	5.5V
Input Current	10 mA
Output Voltage	−1.0V to +15V
Storage Temperature Range	−65°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation* (P_D)	
Ceramic Package	1160 mW
Molded Package	890 mW
Metal Can	525 mW

* Derate ceramic package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C; derate metal can package at 200°C/W above 70°C.

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS1642, DS1672	10.8	13.2	V
DS3642, DS3672	11.4	12.6	V
Bootstrap–V_{CC} Differential Voltage (V_B–V_{CC})			
DS1642, DS1672	10.8	13.2	V
DS3642, DS3672	11.4	12.6	V
Temperature (T_A)			
DS1642, DS1672	−55	+125	°C
DS3642, DS3672	0	+70	°C

dc electrical characteristics

DS1642, DS1672 V_{CC} = 12V ±10%, $-55°C \leq T_A \leq +125°C$, unless otherwise noted.
DS3642, DS3672 V_{CC} = 12V ±5%, $0°C \leq T_A \leq +70°C$, unless otherwise noted.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage			2.0	1.4		V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IH}	Logical "1" Input Current	V_{IN} = 2.4V			900		μA
		V_{IN} = 5.5V			4		mA
I_{IL}	Logical "0" Input Current	V_{IN} = 0V			−240		μA
V_{CD}	Input Clamp Voltage	I_{IN} = −5 mA			−0.9		V
V_{OH}	Logical "1" Output Voltage	$V_B \geq V_{CC}$ + 2V, I_{OUT} = −400μA			V_{CC}−0.2		V
V_{OL}	Logical "0" Output Voltage	I_{OUT} = 400μA, Bootstrap Pin (V_B) Open			0.3		V
R_B	Bootstrap Resistor				3.0		kΩ
$I_{CC(1)}$	Supply Current	V_{IN} = 0V,(Both Drivers OFF), Outputs Open	Bootstrap Pin (V_B) Open		0.9		mA
			V_B = V_{CC} + 7V		−3.8		mA
$I_{B(1)}$	Bootstrap Current	(Both Drivers)			3.8		mA
$I_{CC(0)}$	Supply Current	V_{IN} = 2.4V, Bootstrap Pin (V_B) Open	(Both Drivers ON) Outputs Open		7.7		mA

switching characteristics (Note 4) V_{CC} = 12V, T_A = 25°C, *(Figure 1)*

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0"	R_D = 10Ω	C_L = 50 pF		14		ns
			C_L = 250 pF		20		ns
			C_L = 500 pF		29		ns
t_{pd1}	Propagation Delay to a Logical "1"	R_D = 10Ω	C_L = 50 pF		16		ns
			C_L = 250 pF		23		ns
			C_L = 500 pF		30		ns

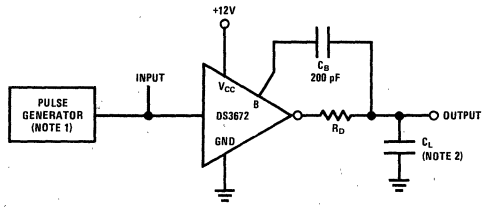
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1672 and across the 0°C to +70°C range for the DS3672. All typicals are given for V_{CC} = 12V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS1672 and DS3672, a 10 ohm resistor should be placed in series with each output. This resistor is internal to the DS1642/DS3642 and need not be added.

ac test circuit



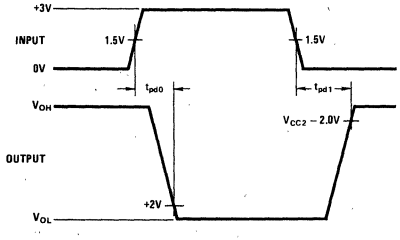
Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, 50% Duty Cycle, Z_{OUT} = 50Ω, $t_r = t_f \leq 10$ ns.

Note 2: C_L includes probe and jig capacitance.

Note 3: The high current transient (as high as 1.0A) through the resistance of the external interconnecting ground lead during the output transition from the high state to the low state can appear as negative feedback to the input. If the external interconnecting load from the driving circuit to ground is electrically long, or has significant dc resistance, it can subtract from the switching response.

FIGURE 1

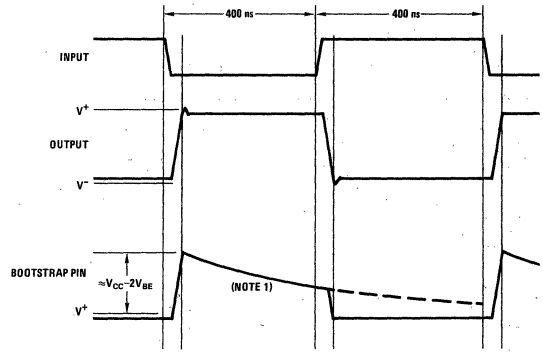
switching time waveforms



Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $t_R \leq 10$ ns, $t_f \leq 10$ ns, Z_{OUT} = 50Ω.

Note 2: C_L includes probe and jig capacitance.

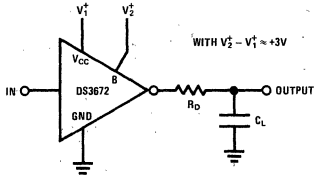
node voltage waveforms



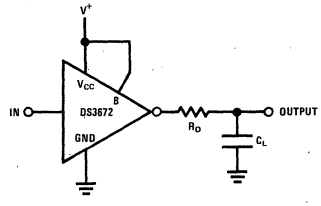
Note 1: The fall time has an exponential decay with the following time constant: $t_B = C_B R_B$. The range of values for R_B (resistor tolerance, and temperature coefficient included) can be found in the table of electrical characteristics.

typical applications

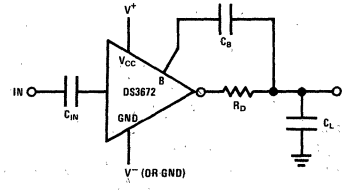
DS3672 Operating with Extra Supply to Enhance Output Voltage Level



DS3672 in Non-Bootstrap Application with Single Supply—When Output High Level is Non-Critical.



DS3672 Bootstrap Mode of Application with Capacitively Coupled Input and Negative Supply.



NATIONAL

Memory/Clock Drivers

Advance Information*

DS3643, DS3673 decoded quad MOS clock drivers

general description

The DS3643 and DS3673 are quad bipolar-to-MOS decoder/clock drivers with TTL/DTL compatible inputs. They are designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

The device features full decoding of input address lines from two inputs to one of four outputs. Also featured is the capability of expanding to three inputs to one of eight outputs with the use of the Expansion and $\overline{\text{Expansion}}$ inputs. Also included are clock and refresh inputs.

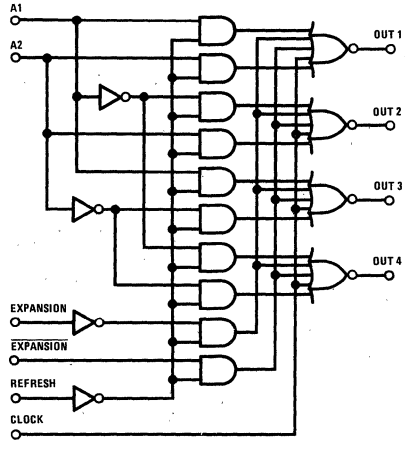
The circuit was designed for driving large capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs, thereby minimizing input loading.

The DS3643 has a 10 ohm damping resistor in series with each output to dampen transients caused by the fast switching output, while the DS3673 has a direct, low impedance output, for use with or without an external resistor.

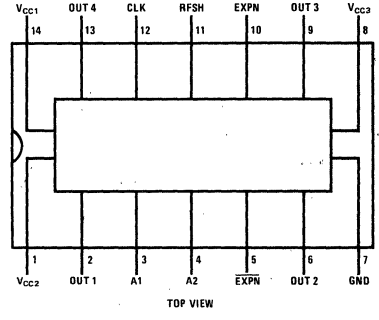
features

- TTL/DTL compatible inputs
- Operates from standard bipolar and MOS supplies
- PNP inputs minimize input loading
- Full logic decoding for either two inputs to one of four outputs or three inputs to one of eight outputs
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Built-in damping resistors (DS3643)

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS3643J or DS3643N

Order Number DS3673J or DS3673N

truth table

INPUTS						OUTPUTS			
CLOCK	REFRESH	EXPANSION	$\overline{\text{EXPANSION}}$	A_2	A_1	OUT 1	OUT 2	OUT 3	OUT 4
1	X	X	X	X	X	0	0	0	0
0	1	X	X	X	X	1	1	1	1
0	0	1	0	0	0	1	0	0	0
0	0	1	0	0	1	0	1	0	0
0	0	1	0	1	0	0	0	1	0
0	0	1	0	1	1	0	0	0	1
0	0	1	1	X	X	0	0	0	0
0	0	0	1	X	X	0	0	0	0
0	0	0	0	X	X	0	0	0	0

X = Don't Care State.

*Specifications may change.

absolute maximum ratings (Note 1)

Supply Voltage	
V_{CC1}	7V
V_{CC2}	13V
V_{CC3}	16V
Input Voltage	−1.0V to 7V
Output Voltage	−1.0V to 16V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation (P_D)	
Ceramic Package	1160 mW
Molded Package	1000 mW

* Derate ceramic package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C.

operating conditions

	MIN	MAX	UNITS
Supply Voltage			
V_{CC1}	4.75	5.25	V
V_{CC2}	11.4	12.6	V
V_{CC3}	*	**	V
Temperature, T_A	0	+70	°C

*V_{CC2} + (3V − 5%), **V_{CC2} + (3V + 5%)

electrical characteristics

T_A = 0°C to +70°C, V_{CC1} = 5.0V ±5%, V_{CC2} = 12V ±5%, V_{CC3} = V_{CC2} + (3V ±5%) unless otherwise noted. (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage			2			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IH}	Logical "1" Input Current	V_{IN} = 5.5V	Refresh, Exp., $\overline{Exp.}$			10	μA
			A1, A2, Clock			40	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V	Refresh, Exp.		−40	−250	μA
			A1, A2, Clock, $\overline{Exp.}$		−1.6	−1.0	mA
V_{CD}	Input Clamp Voltage	I_I = −12 mA				−1.5	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −1 mA, V_{IL} = 0.8V			V_{CC2}−0.2		V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 5 mA, V_{IH} = 2.0V			0.3		V
V_{OC}	Output Clamp Voltage	I_{OC} = 5 mA, V_{IL} = 0.8V				V_{CC2}+1.5	V
I_{CC}	Supply Current Outputs High						
	I_{CC1}	Refresh = 5V, All Other Inputs = 0V	V_{CC1} = 5.25V		20		mA
	I_{CC2}		V_{CC2} = 12.6V		−2		mA
	I_{CC3}		V_{CC3} = 15.75V		2		mA
I_{CLO}	Supply Currents Outputs Low						
	I_{CC1}	All Inputs = 5V	V_{CC1} = 5.25V		30		mA
	I_{CC2}		V_{CC2} = 12.6V		0.1		mA
	I_{CC3}		V_{CC3} = 15.75V		15		mA

switching characteristics V_{CC1} = 5V, V_{CC2} = 12V, V_{CC3} = 15V (Note 4)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0" from A_1, A_2, Clock, $\overline{Exp.}$ to Out 1	R_D = 10Ω	C_L = 400 pF		20		ns
			C_L = 100 pF		12		ns
t_{pd0}	Propagation Delay to a Logical "0" from Refresh, Exp. to Out 1	R_D = 10Ω	C_L = 400 pF		25		ns
			C_L = 100 pF		17		ns
t_{pd1}	Propagation Delay to a Logical "1" from A_1, A_2, Clock, $\overline{Exp.}$ to Out 1	R_D = 10Ω	C_L = 400 pF		20		ns
			C_L = 100 pF		12		ns
t_{pd1}	Propagation Delay to a Logical "1" from Refresh, Exp. to Out 1	R_D = 10Ω	C_L = 400 pF		25		ns
			C_L = 100 pF		17		ns

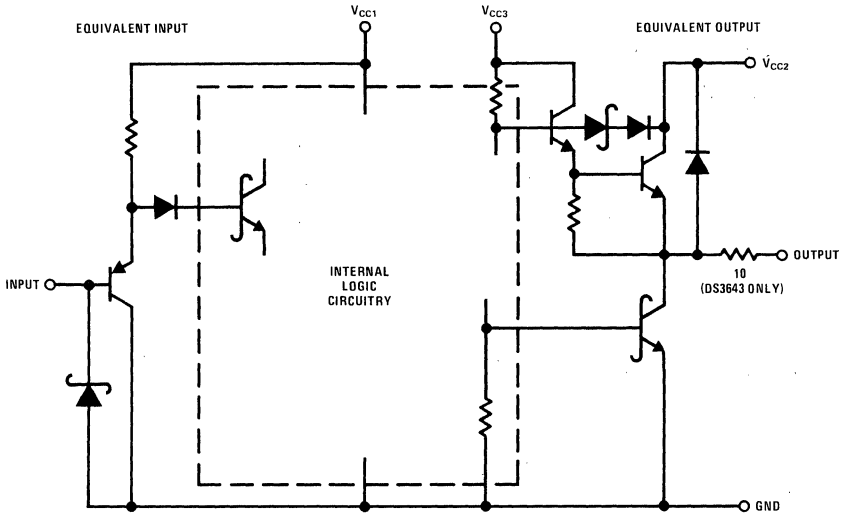
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3673. All typicals are given for V_{CC1} = 5.0V, V_{CC2} = 12V, V_{CC3} = 15V, and T_A = 25°C.

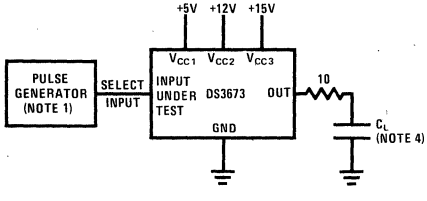
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

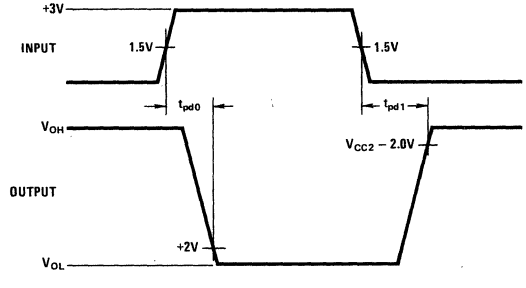
Note 4: For ac measurements, a 10 ohm resistor must be placed in series with the output of the DS3673. This resistor is internal to the DS3643, however, and need not be added.

schematic diagram



ac test circuit and switching time waveforms

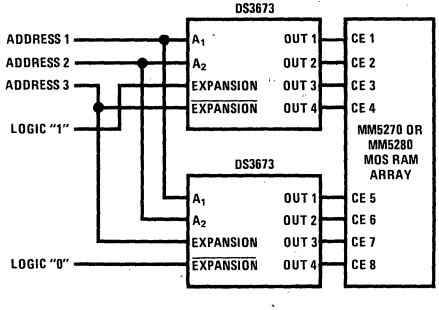




Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $t_R \leq 10$ ns, $t_f \leq 10$ ns, $Z_{OUT} = 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

typical application



NATIONAL

Memory/Clock Drivers

Advance Information*

DS3644, DS3674 quad MOS clock drivers

general description

The DS3644 and DS3674 are quad bipolar-to-MOS clock drivers with TTL/DTL compatible inputs. They are designed to provide high output current and voltage capabilities necessary for optimum driving of high capacitance N-channel MOS memory systems.

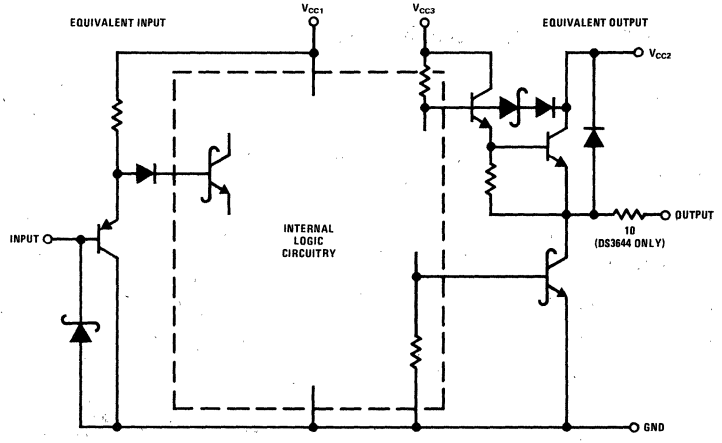
The device features two common enable inputs, a refresh input, and a clock control input for simplified system designs. The circuit was designed for driving highly capacitive loads at high speeds and uses Schottky-clamped transistors. PNP transistors are used on all inputs thereby minimizing input loading.

The DS3644 contains a 10 ohm resistor in series with each output to dampen the transients caused by the fast-switching output, while the DS3674 has a direct, low impedance output for use with or without an external damping resistor.

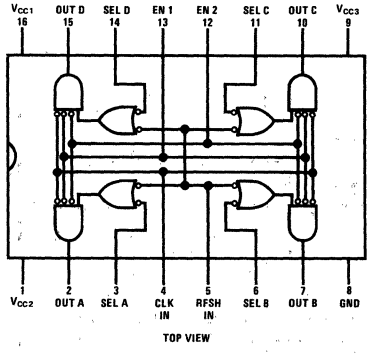
features

- TTL/DTL compatible inputs
- Operates from standard bipolar and MOS supplies
- PNP inputs minimize loading
- High voltage/current outputs
- Input and output clamping diodes
- Control logic optimized for use with MOS memory systems
- Pin and function compatible with MC3460 and 3235
- Built-in damping resistors (DS3644)

schematic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS3644J, DS3674J, DS3644N or DS3674N

*Specifications may change.

absolute maximum ratings (Note 1)

Supply Voltage	
V_{CC1}	7V
V_{CC2}	13V
V_{CC3}	16V
Input Voltage	−1.0V to +7V
Output Voltage	−1.0V to +16V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation (P_D)	
Ceramic Package	1160 mW
Molded Package	1000 mW

operating conditions

	MIN	MAX	UNITS
Supply Voltage			
V_{CC1}	4.75	5.25	V
V_{CC2}	11.4	12.6	V
V_{CC3}	V_{CC2} + (3V−5%)	V_{CC2} + (3V + 5%)	V
Temperature, T_A	0	+70	°C

* Derate ceramic package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C.

electrical characteristics

T_A = 0°C to +70°C, V_{CC1} = 5.0V ±5%, V_{CC2} = 12V ±5%, V_{CC3} = V_{CC2} + (3V ±5%) unless otherwise noted. (Notes 2, 3 and 4)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage			2			V
V_{IL}	Logical "0" Input Voltage					0.8	V
I_{IH}	Logical "1" Input Current	V_{IN} = 5.0V	Select Inputs			10	μA
			All Other Inputs			40	μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V	Select Inputs		−40	−250	μA
			All Other Inputs			−1.0	mA
V_{CD}	Input Clamp Voltage	I_I = −12 mA				−1.5	V
V_{OH}	Logical "1" Output Voltage	I_{OH} = −1 mA, V_{IL} = 0.8V		V_{CC2}−0.5			V
V_{OL}	Logical "0" Output Voltage	I_{OL} = 5 mA, V_{IH} = 2.0V				0.5	V
V_{OC}	Output Clamp Voltage	I_{OC} = 5 mA, V_{IL} = 0.8V				V_{CC2}+1.5	V
I_{CCH}	Supply Current Outputs High	All Inputs V_{IN} = 0V, Outputs Open					
	I_{CC1}		V_{CC1} = 5.25V		18	27	mA
	I_{CC2}		V_{CC2} = 12.6V		−2	−4	mA
	I_{CC3}		V_{CC3} = 15.75V		2	4	mA
I_{CCL}	Supply Currents Outputs Low	All Inputs V_{IN} = 5V, Outputs Open					
	I_{CC1}		V_{CC1} = 5.25V		26.8	40	mA
	I_{CC2}		V_{CC2} = 12.6V			3	mA
	I_{CC3}		V_{CC3} = 15.75V		15	25	mA

switching characteristics V_{CC1} = 5V, V_{CC2} = 12V, V_{CC3} = 15V, T_A = 25°C unless otherwise noted

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0"	R_D = 10Ω	C_L = 400 pF		20		ns
			C_L = 100 pF		12		ns
t_{pd1}	Propagation Delay to a Logical "1"	R_D = 10Ω	C_L = 400 pF		20		ns
			C_L = 100 pF		12		ns

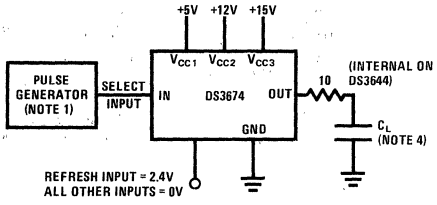
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typicals are given for V_{CC1} = 5V, V_{CC2} = 12V, V_{CC3} = 15V and T_A = 25°C.

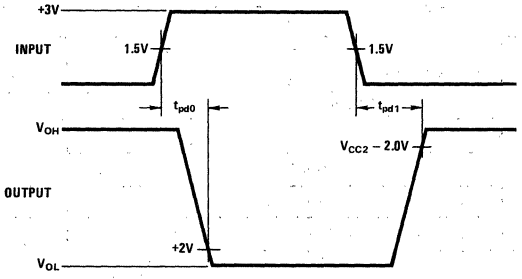
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: For ac measurements, a 10 ohm resistor must be placed in series with the output of the DS3674. This resistor is internal to the DS3644, however, and need not be added.

ac test circuit



switching time waveforms



Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $t_R \leq 10$ ns, $t_f \leq 10$ ns, $Z_{OUT} = 50\Omega$.

Note 2: C_L includes probe and jig capacitance.

truth table

INPUT					OUTPUT
ENABLE 1	ENABLE 2	SELECT INPUT	CLOCK INPUT	REFRESH INPUT	
1	X	X	X	X	0
X	1	X	X	X	0
X	X	X	1	X	0
X	X	1	X	1	0
0	0	0	0	X	1
0	0	X	0	0	1

NATIONAL

Memory/Clock Drivers

Advance Information*

DS1645/DS3645, DS1675/DS3675 hex TRI-STATE® MOS latch/drivers

general description

The DS1645/DS3645 and DS1675/DS3675 are hex MOS latch/drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are used to reduce input currents, allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE® outputs which allow bus operation.

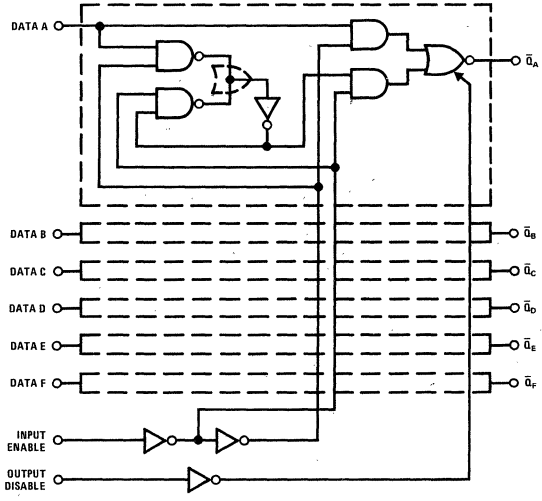
The DS1645/DS3645 has a 15 ohm resistor in series with the outputs to dampen transients caused by the fast switching output circuit. The DS1675/DS3675 has a direct, low impedance output for use with or without an external resistor.

The circuit employs a fall-through-latch which captures the data in parallel with the output, thereby eliminating the delay normally encountered in other latch circuits. The DS1645/DS3645 and DS1675/DS3675 may be used for input address lines or input/output data lines of a MOS memory system.

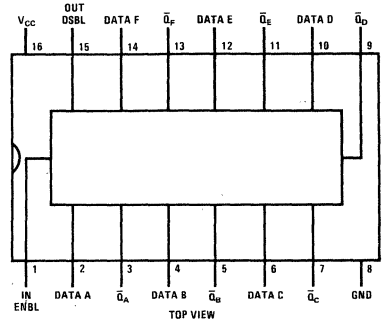
features

- TTL/DTL compatible inputs
- PNP inputs minimize loading
- Capacitance-driving outputs
- TRI-STATE outputs
- Built-in damping resistor (DS1645/DS3645)

logic and connection diagrams



Dual-In-Line Package



Order Number DS1645J, DS1675J DS3645J, DS3675J, DS3645N or DS3675N

truth table

INPUT ENABLE	OUTPUT DISABLE	DATA	OUTPUT	OPERATION
1	0	1	0	Data Feed-Through
1	0	0	1	Data Feed-Through
0	0	X	Q	Latched to Data Present when Enable Went Low
X	1	X	Hi-z	High Impedance Output

X = Don't care.

*Specifications may change.

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7V
Logical "1" Input Voltage, $V_{IN(1)}$	7V
Logical "0" Input Voltage, $V_{IN(0)}$	−1.5V
Logical "1" Output Current, $I_{OS(1)}$	−1A
Logical "0" Output Current, $I_{OS(0)}$	1A
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation (P_D)	
Ceramic Package	1160 mW
Molded Package	1000 mW

* Derate ceramic package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C.

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1645, DS1675	−55	+125	°C
DS3645, DS3675	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage				2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage						0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 5.5V, V_{CC} = 5.5V	Enable Inputs			0.1	40	μA
			Data Inputs				80	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0.5V, V_{CC} = 5.5V	Enable Inputs			−90	−250	μA
			Data Inputs			−180	−500	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA					−1.2	V
$V_{OH(NL)}$	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = 0 mA			3.4	4.25		V
$V_{OL(NL)}$	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 0 mA				0.25	0.45	V
$V_{OH(WL)}$	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA		DS1645/DS3645	2.4	3.5		V
				DS1675/DS3675	2.5	3.5		V
$V_{OL(WL)}$	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA		DS1645/DS3645		0.6	1.1	V
				DS1675/DS3675		0.3	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V (Note 4)				170		mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V (Note 4)				170		mA
$I_{CC(MAX)}$	Maximum Power Supply Current	V_{CC} = 5.5V				60		mA
$I_{CC(MIN)}$	Minimum Power Supply Current	V_{CC} = 5.5V				40		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1645 and DS1675 and across the 0°C to +70°C range for the DS3645 and DS3675. All typical values are for T_A = 25°C and V_{CC} = 5V.

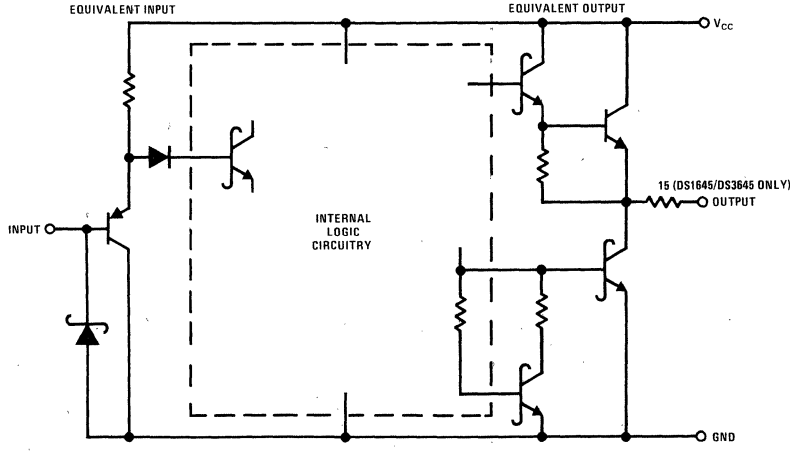
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS1675 and DS3675 a 15 ohm resistor should be placed in series with each output. This resistor is internal to the DS1645/DS3645, and need not be added.

switching characteristics (Note 4) V_{CC} = 5V, T_A = 25°C unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{pd(0)}$	Propagation Delay to Logical "0," Data Input to Output	C_L = 50 pF		7		ns
		C_L = 250 pF		15		ns
		C_L = 500 pF		25		ns
$t_{pd(1)}$	Propagation Delay to Logical "1," Data Input to Output	C_L = 50 pF		7		ns
		C_L = 250 pF		15		ns
		C_L = 500 pF		25		ns
t_{SET-UP}	Set-up Time on Data Input before Input Enable goes Low			0		ns
t_{HOLD}	Hold Time on Data Input after Input Enable goes Low			10		ns
t_{HO}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to V_{CC}		15		ns
t_{H1}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to Ground		15		ns
t_{OH}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF, R_L = 400Ω to V_{CC}		15		ns
t_{1H}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF, R_L = 400Ω to Ground		15		ns

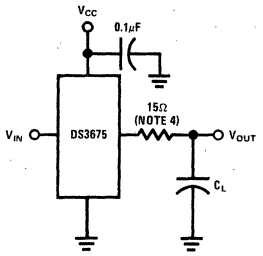
schematic diagram

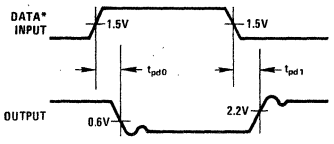


DS3645/DS3675

ac test circuits and switching time waveforms (con't)

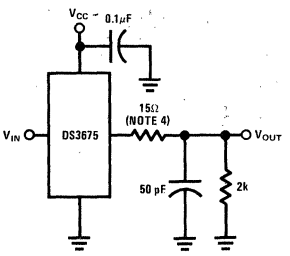
t_{pd0} and t_{pd1}



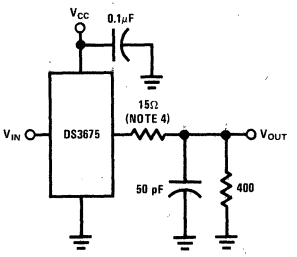


*Input Signal Characteristics:
Freq = 1 MHz
Duty cycle = 50%
Amplitude = 0.4V to 3.0V
$t_r = t_f = 2.5$ ns

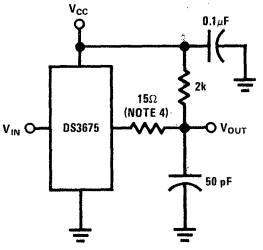
t_{H1}

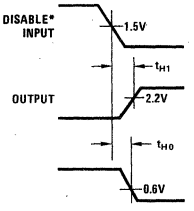


t_{1H}

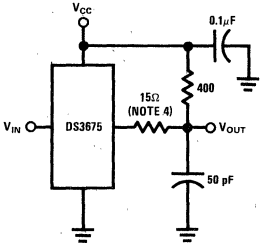


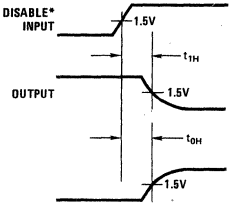
t_{H0}





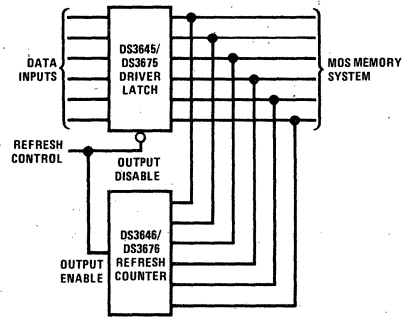
t_{0H}





typical applications

The DS3645 and DS3675 latch/driver has TRI-STATE outputs, which allows the outputs to be tied with those of another TRI-STATE driver, such as the DS3646 and DS3676 refresh counter. The DS3645 and DS3675 can be disabled while the alternate driver controls the address lines into the memory system.



Memory/Clock Drivers

Advance Information*

DS1646/DS3646, DS1676/DS3676 6-bit TRI-STATE® MOS refresh counter/driver

general description

The DS1646/DS3646 and DS1676/DS3676 are 6-bit refresh counters with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE® outputs allow it to be used on common data buses.

The DS1646/DS3646 has a 15 ohm resistor in series with the outputs to dampen transients caused by the fast switching output circuit. The DS1676/DS3676 has a direct, low impedance output, for use with or without an external resistor.

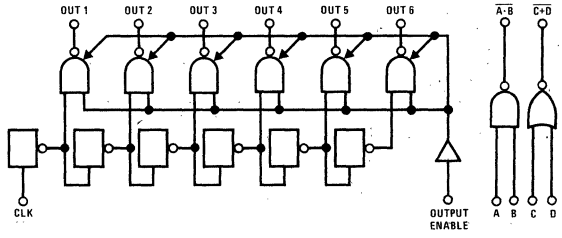
The counter uses as its input the RAM clock signal, and with each clock input, it advances the count by one, thus generating a new refresh address.

Extra pins in the package are used for a two input NAND gate and a two input NOR gate, both of which have capacitive drive outputs.

features

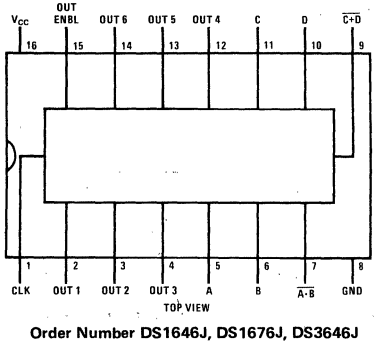
- Circuit counts when clock goes high
- TTL/DTL compatible inputs
- PNP inputs minimize loading
- Capacitance-driver outputs
- TRI-STATE outputs
- Extra gates on unused pins
- Built-in damping resistor (DS1646/DS3646)

logic diagram



connection diagram

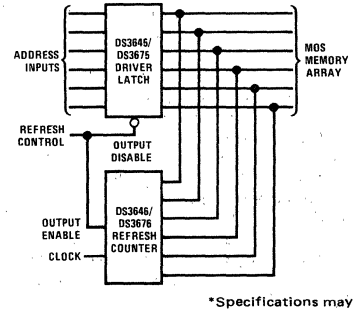
Dual-In-Line Package



Order Number DS1646J, DS1676J, DS3646J
DS3676J or DS3646N, DS3676N

typical application

The DS1646/DS3646 and DS1676/DS3676 have TRI-STATE outputs which can be tied to the outputs of another TRI-STATE driver. The refresh counter can control the address lines into a memory array during a short refresh cycle, and then return to the high-impedance state to allow the primary driver to control the address lines.



*Specifications may change.

absolute maximum ratings (Note 1)

Supply Voltage, V_{CC}	7V
Logical "1" Input Voltage, $V_{IN(1)}$	7V
Logical "0" Input Voltage, $V_{IN(0)}$	−1.5V
Logical "1" Output Current, $I_{OS(1)}$	1A
Logical "0" Output Current, $I_{OS(0)}$	1A
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation (P_D)	
Ceramic Package	1160 mW
Molded Package	1000 mW

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1646, DS1676	−55	+125	°C
DS3646, DS3676	0	+70	°C

* Derate ceramic package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C.

dc electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage				2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage						0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V,	Enable Input			0.1	40	μA
		V_{IN} = 5.5V	Clock Input				80	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V	V_{IN} = 0.5V			−90	−250	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V	I_{IN} = −18 mA				−1.2	V
$V_{OH(NL)}$	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V	I_{OH} = 0 mA		3.4	4.25		V
$V_{OL(NL)}$	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V	I_{OL} = 0 mA			0.25	0.45	V
$V_{OH(WL)}$	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V	I_{OH} = −1.0 mA	DS1646/DS3646	2.4	3.5		V
				DS1676/DS3676	2.5	3.5		V
$V_{OL(WL)}$	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V	I_{OL} = 20 mA	DS1646/DS3646		0.6	1.1	V
				DS1676/DS3676		0.3	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V	V_{OUT} = 0V, (Note 4)			−170		mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V	V_{OUT} = 4.5V			170		mA
$I_{CC(MAX)}$	Maximum Power Supply Current	V_{CC} = 5.5V				60		mA
$I_{CC(MIN)}$	Minimum Power Supply Current	V_{CC} = 5.5V				40		mA

ac electrical characteristics (V_{CC} = 5V, T_A = 25°C) (Note 4)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$t_{pd(0)}$	Propagation Delay to Logical "0"	C_L = 50 pF			7		ns
		C_L = 250 pF			15		ns
		C_L = 500 pF			25		ns
$t_{pd(1)}$	Propagation Delay to Logical "1"	C_L = 50 pF			7		ns
		C_L = 250 pF			15		ns
		C_L = 500 pF			25		ns
	Settling Time Delay from Clock Input to Output O6	C_L = 50 pF			65		ns
t_{H0}	Delay from Enable Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF	R_L = 2 kΩ to V_{CC}		10		ns
t_{H1}	Delay from Enable Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF	R_L = 2 kΩ to Gnd		10		ns
t_{0H}	Delay from Enable Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF	R_L = 390Ω to V_{CC}		10		ns
t_{1H}	Delay from Enable Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF	R_L = 390Ω to Gnd		10		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

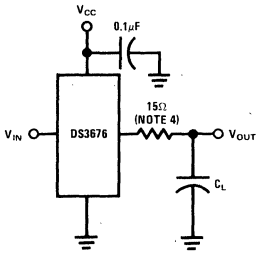
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1646 and DS1676 and across the 0°C to +70°C range for the DS3646 and DS3676. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

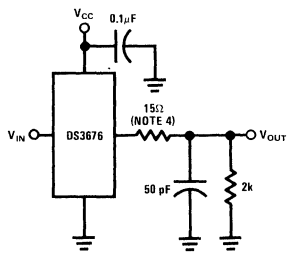
Note 4: When measuring output drive current and switching response for the DS1676 and DS3676 a 15 ohm resistor should be placed in series with each output. This resistor is internal to the DS1646/DS3646, and need not be added.

ac test circuits and switching time waveforms

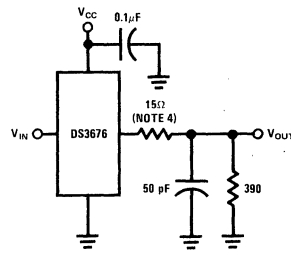
t_{pd0} & t_{pd1}



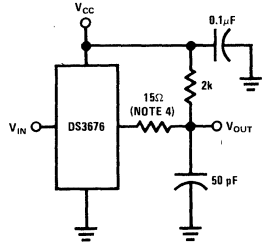
t_{H1}



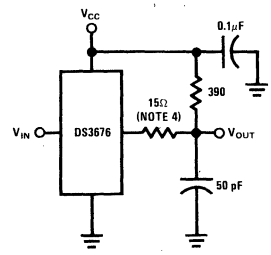
t_{1H}

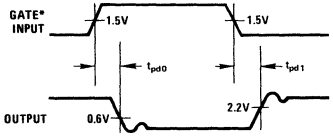


t_{H0}

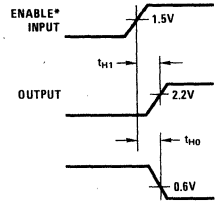


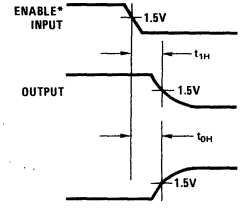
t_{0H}



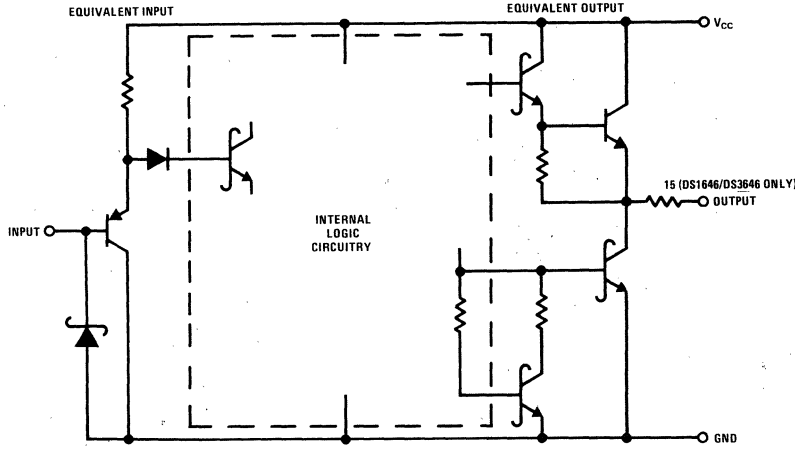


*Input Signal Characteristics:
Freq = 1 MHz
Duty cycle = 50%
Amplitude = 0.4V to 3.0V
$t_r = t_f = 2.5$ ns





schematic diagram



DS3646/DS3676

NATIONAL

Memory/Clock Drivers

Advance Information*

DS1647/DS3647, DS1677/DS3677, DS16147/DS36147, DS16177/DS36177 quad TRI-STATE® MOS memory I/O registers

general description

The DS1647/DS3647 series are 4-bit I/O buffer registers intended for use in MOS memory systems. The circuits employ a fall-through latch for data storage. This method of latching captures the data in parallel with the output, thus eliminating the delays encountered in other designs. The circuits use Schottky-clamped transistor logic for minimum propagation delay and employ PNP input transistors so that input currents are low, allowing large fan-out to these circuits needed in a memory system.

Two pins per bit are provided, and data transfer is bi-directional so that the register can handle both input and output data. The direction of data flow is controlled through the input enables. The latch control, when taken low, will cause the register to hold the data present at that time and display it at the outputs. Data can be latched into the register independent of the output disables or EXPANSION input. Either or both of the outputs may be taken to the high-impedance state with the output disables. The EXPANSION pin disables both outputs to facilitate multiplexing with other I/O registers on the same data lines.

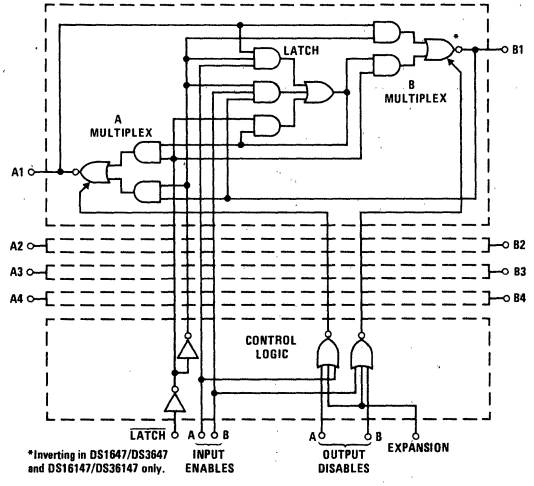
The "B" port outputs in the DS16147/DS36147 and DS16177/DS36177 are open collectors, and in the DS1647/DS3647 and DS1677/DS3677 they are TRI-STATE. The "B" port outputs are also designed for use in bus organized data transmission systems and can sink 80 mA and source −5.2 mA. The "A" port outputs in all four types are TRI-STATE.

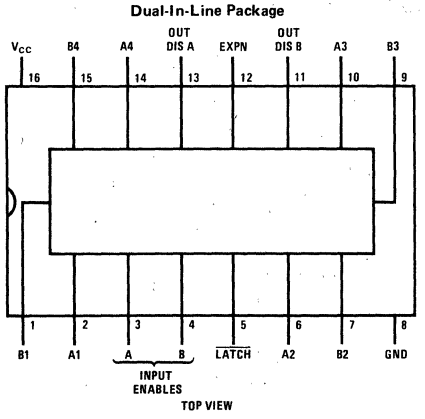
Data going from port "A" to port "B" is inverted in the DS1647/DS3647 and DS16147/DS36147 and is not inverted in the DS1677/DS3677 and DS16177/DS36177. Data going from port "B" to port "A" is inverted in all four types.

features

- PNP inputs minimize loading
- Fall-through latch design
- Propagation delay of only 15 ns
- TRI-STATE outputs
- EXPANSION control
- Bi-directional data flow
- TTL/DTL compatible
- Transmission line driver output

logic and connection diagrams





Order Number DS1647J, DS3647J, DS1677J, DS3677J, DS16147J, DS36147J, DS16177J, DS36177J or DS3647N, DS3677N, DS36147N DS36177N

*Specifications may change.

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	−1.5V to +7V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation (P_D)	
Ceramic Package	1160 mW
Molded Package	1000 mW

* Derate ceramic package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C.

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1677	−55	+125	°C
DS3677	0	+70	°C

electrical characteristics (Notes 2 and 3)

Over recommended operating temperature range (unless otherwise noted).

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage			2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 5.5V	Latch, Disable Inputs			40	μA
			Data Pins (A, B)			80	μA
			Enable Inputs			200	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.5V	Latch, Disable Inputs			−250	μA
			Data Pins (A, B)			−400	μA
			Enable Inputs			−1250	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−1.2	V
$V_{OH(A)}$	Logical "1" Output Voltage A Port	V_{CC} = 4.5V, I_{OH} = −1 mA	DS16XX	2.5	3.4		V
			DS36XX	2.7	3.4		V
$V_{OL(A)}$	Logical "0" Output Voltage A Port	V_{CC} = 4.5V, I_{OL} = 20 mA	DS16XX			0.5	V
			DS36XX			0.5	V
$V_{OH(B)}$	Logical "1" Output Voltage B Port	V_{CC} = 4.5V, I_{OH} = −5.2 mA, (Note 4)	DS16XX	2.4	3.3		V
			DS36XX	2.4	3.3		V
$V_{OL(B)}$	Logical "0" Output Voltage B Port	V_{CC} = 4.5V, I_{OL} = 100 mA	DS16XX			0.7	V
			DS36XX			0.7	V
$I_{CC(MAX)}$	Power Supply Current	V_{CC} = 5.5V				100	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1677 and across the 0°C to +70°C range for the DS3677. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

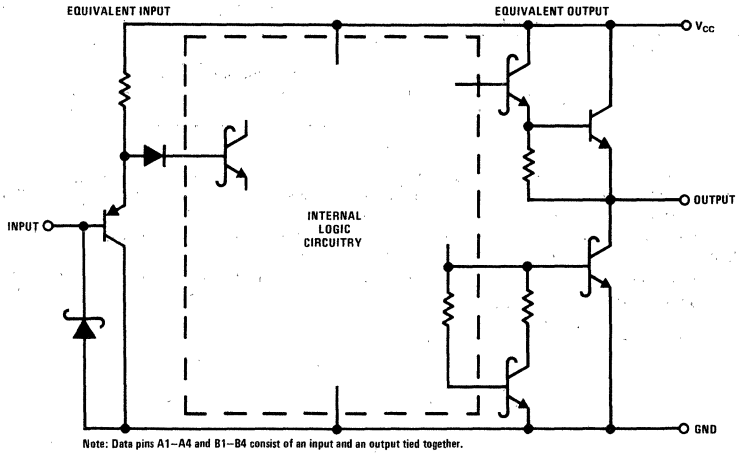
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted.

Note 4: Not applicable to DS16147/DS36147 or DS16177/DS36177.

switching characteristics (V_{CC} = 5.0V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0" from A_i to B_i or B_i to A_i	C_L = 50 pF		7		ns
t_{pd1}	Propagation Delay to a Logical "1" from A_i to B_i or B_i to A_i	C_L = 50 pF		7		ns
t_{1H}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF R_L = 390Ω to Gnd		15		ns
t_{0H}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF R_L = 390Ω to V_{CC}		15		ns
t_{H1}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF R_L = 2 kΩ to Gnd		15		ns
t_{H0}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF R_L = 2 kΩ to V_{CC}		15		ns
t_{SET-UP}	Setup Time of Data Input Before $\overline{LATCH}$ Goes Low			0		ns
t_{HOLD}	Hold Time of Data Input After $\overline{LATCH}$ Goes Low			7		ns

schematic diagram



Note: Data pins A1–A4 and B1–B4 consist of an input and an output tied together.

logic table

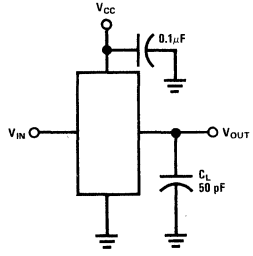
INPUT ENABLES A	INPUT ENABLES B	$\overline{\text{LATCH}}$	OUTPUT DISABLES A	OUTPUT DISABLES B	EXPANSION	A1–4	B1–4	COMMENTS
1	0	1	0	0	0	Hi-Z	$\overline{A}$	Data In on A, Output to B
0	1	1	0	0	0	$\overline{B}$	Hi-Z	Data In on B, Output to A
1	0	0	0	0	0	Hi-Z	$\overline{Q}$	Data Stored Which is Present When $\overline{\text{LATCH}}$ Goes Low
0	1	0	0	0	0	$\overline{Q}$	Hi-Z	Same as Above
1	0	X	0	1	0	Hi-Z	Hi-Z	Both A and B In Hi-Z State; Data Input on A, May Be Latched
0	1	X	1	0	0	Hi-Z	Hi-Z	Both A and B In Hi-Z State; Data Input on B, May Be Latched
X	X	X	X	X	1	Hi-Z	Hi-Z	Both A and B In Hi-Z State

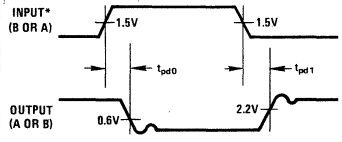
X = Don't Care

Note: Data may be latched into the register independent of the output disables or expansion.

ac test circuits and switching time waveforms

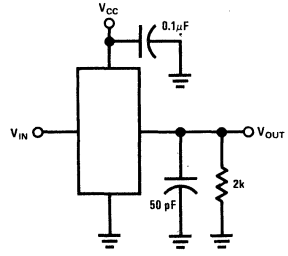
t_{pd0} & t_{pd1}



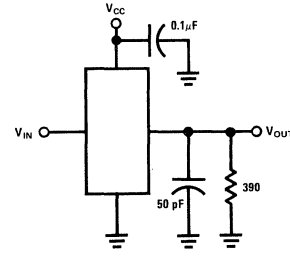


*Input Signal Characteristics:
Freq = 1 MHz
Duty cycle = 50%
Amplitude = 0.4V to 3.0V
$t_r = t_f = 2.5$ ns

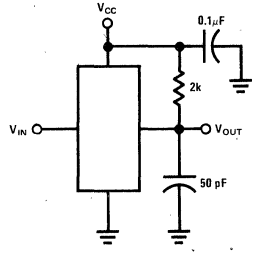
t_{H1}

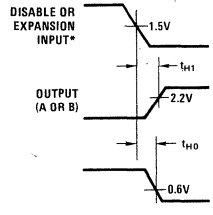


t_{1H}

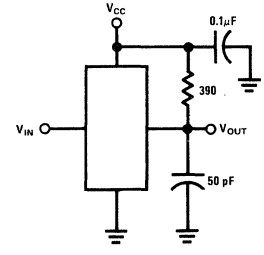


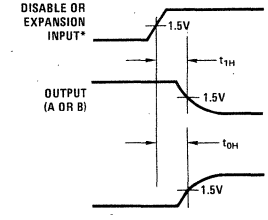
t_{H0}



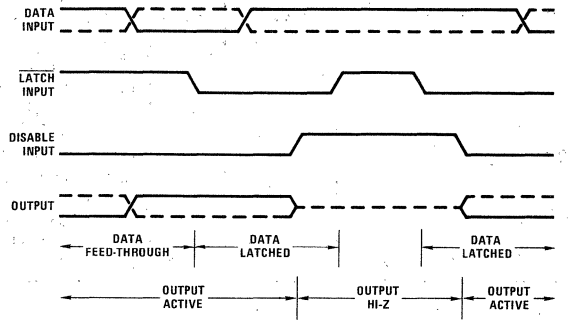


t_{0H}



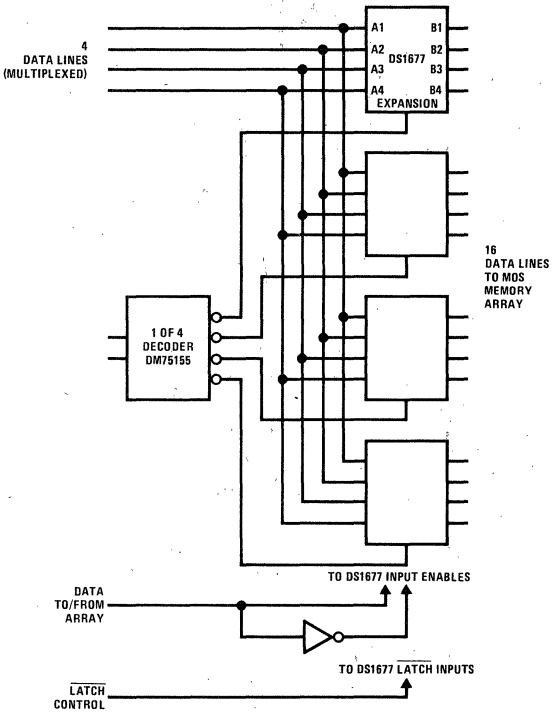


operating waveforms



typical application

The diagram below shows how the DS1677 can be used as a register capable of multiplexing data lines.



Memory/Clock Drivers

Advance Information*

DS1648/DS3648, DS1678/DS3678 TRI-STATE® MOS multiplexer/drivers

general description

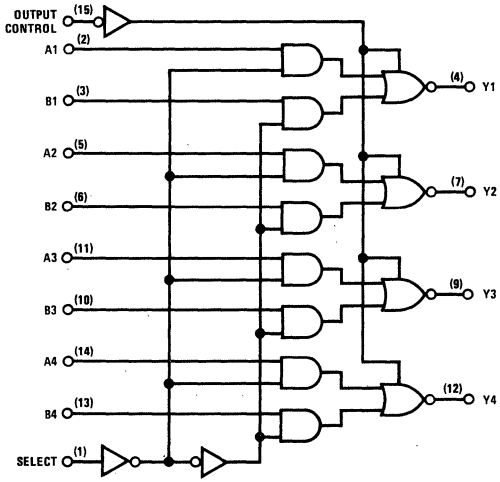
The DS1648/DS3648 and DS1678/DS3678 are quad 2-input multiplexers with TRI-STATE outputs designed to drive the large capacitive loads (up to 500 pF) associated with MOS memory systems. A PNP input structure is employed to minimize input currents so that driver loading in large memory systems is reduced. The circuit employs Schottky-clamped transistors for high speed and TRI-STATE outputs for bus operation.

The DS1648/DS3648 has a 15 ohm resistor in series with the outputs which dampens the transients caused by the fast-switching output circuit, while the DS1678/DS3678 has a direct, low impedance output for use with or without an external resistor.

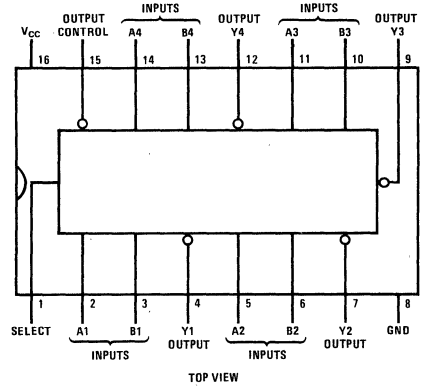
features

- TRI-STATE outputs interface directly with system bus
- Schottky-clamped for better ac performance
- PNP inputs to minimize input loading
- DTL and TTL compatible
- High-speed capacitive load drivers
- Built-in damping resistor (DS1648/DS3648 only)

logic and connection diagrams

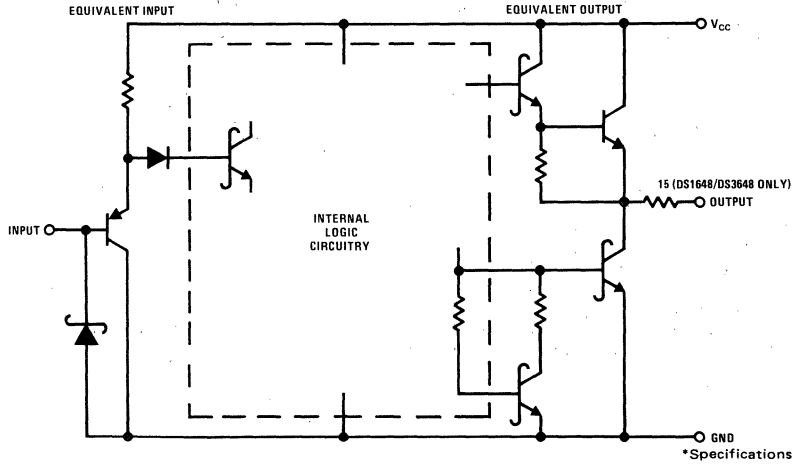


Dual-In-Line Package



Order Number DS1648J, DS1678J DS3648J, DS3678 or DS3648N, DS3678N

schematic diagram



*Specifications may change.

absolute maximum ratings (Note 1)

Supply Voltage	7V
Logical "1" Input Voltage	7V
Logical "0" Input Voltage	−1.5V
Logical "1" Output Current	
DS1648/DS1678	<0.7A
DS3648/DS3678	<1A
Logical "0" Output Current	
DS1648/DS1678	<0.7A
DS3648/DS3678	<1A
Storage Temperature Range	
DS1648/DS1678	−65°C to +175°C
DS3648/DS3678	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation (P_D)	
Ceramic Package	1160 mW
Molded Package	1000 mW

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	5.5	V
Temperature (T_A)			
DS1648, DS1678	−55	+125	°C
DS3648, DS3678	0	+70	°C

* Derate ceramic package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C.

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage			2.0	1.6		V
$V_{IN(0)}$	Logical "0" Input Voltage					0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V			0.1	40	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V, V_{IN} = 0.5V			−90	−250	μA
V_{CLAMP}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18 mA				−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OH} = 0 mA	DS1648/DS1678	3.4	4.25		V
			DS3648/DS3678	3.5	4.25		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V, I_{OL} = 0 mA	DS1648/DS1678		0.25	0.45	V
			DS3648/DS3678		0.25	0.40	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OH} = −1.0 mA	DS1648	2.5	3.5		V
			DS1678	2.4	3.5		V
			DS3648	2.7	3.5		V
			DS3678	2.6	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V, I_{OL} = 20 mA	DS1648		0.6	1.1	V
			DS1678		0.3	0.5	V
			DS3648		0.6	1.0	V
			DS3678		0.3	0.5	V
I_{1D}	Logical "1" Drive Current	V_{CC} = 4.5V, V_{OUT} = 0V, (Note 4)	DS1648/DS1678		−170		mA
			DS3648/DS3678		−170		mA
I_{0D}	Logical "0" Drive Current	V_{CC} = 4.5V, V_{OUT} = 4.5V, (Note 4)	DS1648/DS1678		170		mA
			DS3648/DS3678		170		mA
$I_{CC(MAX)}$	Maximum Power Supply Current	V_{CC} = 5.5V	DS1648/DS1678		36		mA
			DS3648/DS3678		36		mA
$I_{CC(MIN)}$	Minimum Power Supply Current	V_{CC} = 5.5V	DS1648/DS1678		7.1		mA
			DS3648/DS3678		7.1		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1648 and DS1678 and across the 0°C to +70°C range for the DS3648 and DS3678. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

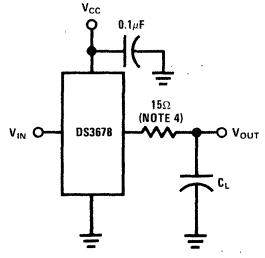
Note 4: When measuring output drive current and switching response for the DS1678 and DS3678 a 15Ω resistor should be placed in series with each output. This resistor is internal to the DS1648/DS3648 and need not be added.

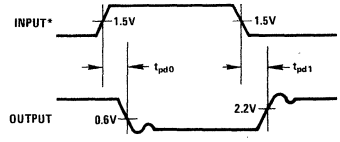
switching characteristics (V_{CC} = 5V, T_A = 25°C) (Note 4)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{pd(0)}$	Propagation Delay to Logical "0"	C_L = 50 pF		7		ns
		C_L = 250 pF		15		ns
		C_L = 500 pF		25		ns
$t_{pd(1)}$	Propagation Delay to Logical "1"	C_L = 50 pF		7		ns
		C_L = 250 pF		15		ns
		C_L = 500 pF		25		ns
t_{H0}	Delay from Output Control Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to V_{CC}		14		ns
t_{H1}	Delay from Output Control Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF, R_L = 2 kΩ to Gnd		14		ns
t_{0H}	Delay from Output Control Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF, R_L = 400Ω to V_{CC}		14		ns
t_{1H}	Delay from Output Control Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF, R_L = 400Ω to Gnd		14		ns
$t_{pd(0)}$	Propagation Delay to Logical "0" When Select Selects A	C_L = 50 pF		14		ns
$t_{pd(1)}$	Propagation Delay to Logical "1" When Select Selects A	C_L = 50 pF		14		ns
$t_{pd(0)}$	Propagation Delay to Logical "0" When Select Selects B	C_L = 50 pF		18		ns
$t_{pd(1)}$	Propagation Delay to Logical "1" When Select Selects B	C_L = 50 pF		18		ns

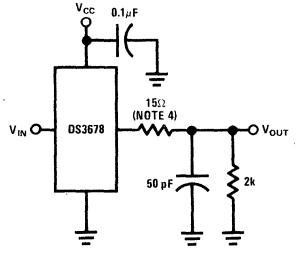
ac test circuits and switching time waveforms

t_{pd0} & t_{pd1}

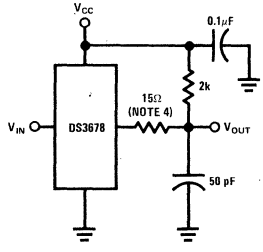


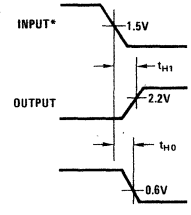


t_{H1}



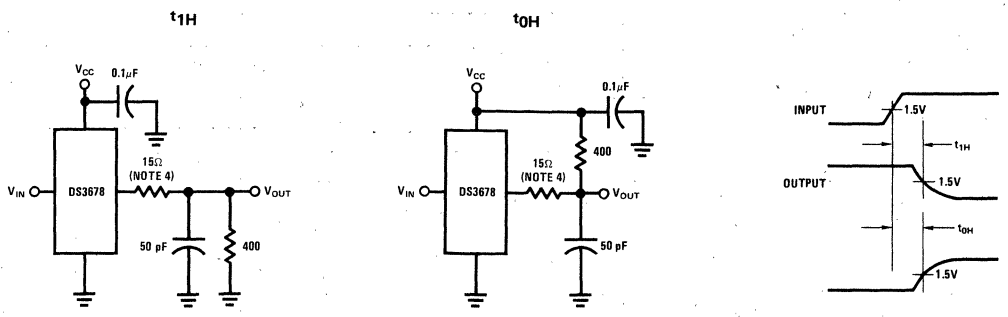
t_{H0}





*Input Signal Characteristics:
Freq = 1 MHz
Duty cycle = 50%
Amplitude = 0.4V to 3.0V
$t_r = t_f$ = 2.5 ns

ac test circuits and switching time waveforms (con't)

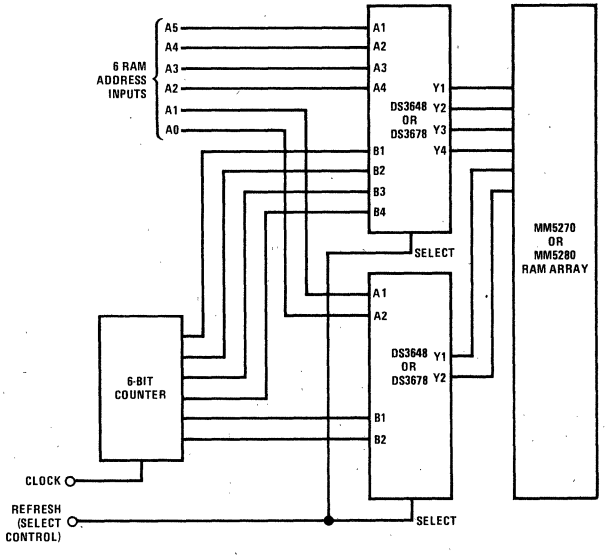


truth table

OUTPUT CONTROL	INPUTS			OUTPUTS
	SELECT	A	B	
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

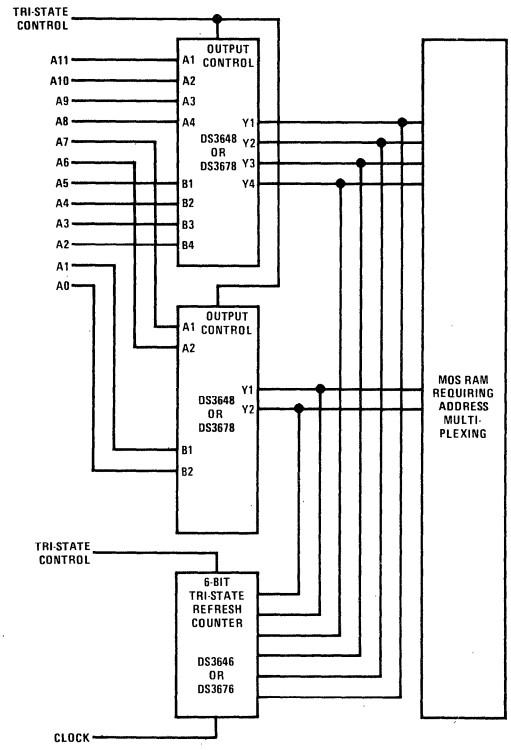
H = High level
L = Low level
X = Don't care
Z = High impedance (OFF)

typical applications

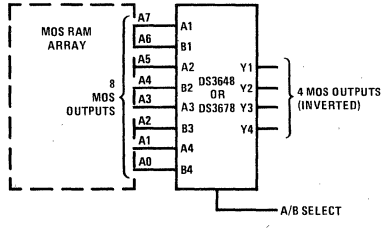


Refreshing a 4k RAM Array

typical applications (con't)



Refreshing Using TRI-STATE Counter



2:1 Multiplexing of RAM Outputs

NATIONAL

Memory/Clock Drivers

Advance Information*

DS1649/DS3649, DS1679/DS3679 hex TRI-STATE® MOS drivers

general description

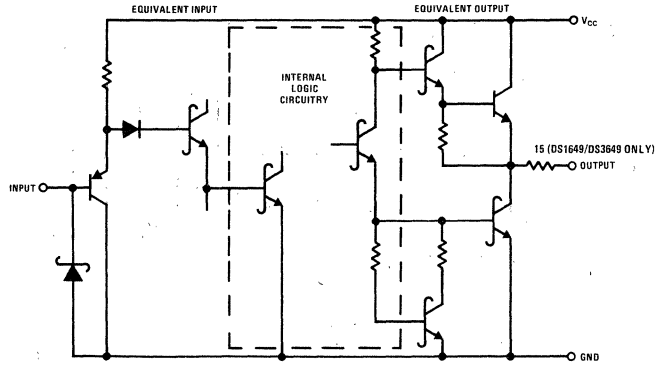
The DS1649/DS3649 and DS1679/DS3679 are Hex TRI-STATE MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and TRI-STATE outputs for bus operation.

The DS1649/DS3649 has a 15 ohm resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS1679/DS3679 has a direct low impedance output for use with or without an external resistor.

features

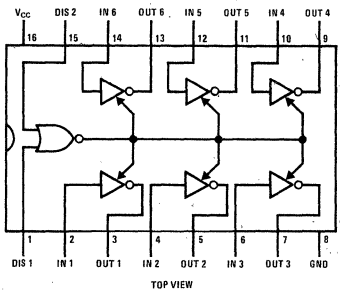
- High speed capabilities
  - Typ 7 ns driving 50 pF
  - Typ 25 ns driving 500 pF
- TRI-STATE outputs for data bussing
- Built-in 15 ohm damping resistor (DS1649/DS3649)
- Same pin-out as DS8096 and DS74366

schematic diagram



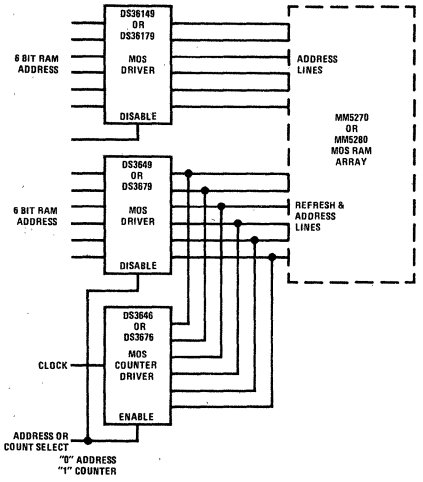
connection diagram

Dual-In-Line Package



Order Number DS1649J, DS1679J, DS3649J, DS3679J or DS3649N, DS3679N

typical application



truth table

DISABLE INPUT		INPUT	OUTPUT
DIS 1	DIS 2		
0	0	0	1
0	0	1	0
0	1	X	Hi-Z
1	0	X	Hi-Z
1	1	X	Hi-Z

X = Don't care
Hi-Z = TRI-STATE mode

*Specifications may change.

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Power Dissipation	600 mW
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Logical "1" Output Current	<1.0 A
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation (P_D)	
Ceramic Package	1160 mW
Molded Package	1000 mW

operating conditions

	MIN	MAX	UNITS
Logical "0" Output Current, ($I_{OS(0)}$)		<1	A
Operating Temperature Range,			
DM1649	−55	+125	°C
DM3649	0	+70	°C

* Derate ceramic package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C.

electrical characteristics (Note 2 and 3)

Over recommended operating temperature range (unless otherwise noted) (Note 1)

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage				2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage						0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V	V_{IN} = 5.5V			0.1	40	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V	V_{IN} = 0.5V			−90	−250	μA
V_{CLAMP}	Input Clamp Voltage		I_{IN} = −18 mA				−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V	I_{OH} = 0 mA	DS1649/DS1679	3.4	4.25		V
				DS3649/DS3679	3.5	4.25		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V	I_{OL} = 0 mA	DS1649/DS1679		0.25	0.45	V
				DS3649/DS3679		0.25	0.40	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V	I_{OH} = −1.0 mA	DS1649	2.5	3.5		V
				DS1679	2.4	3.5		V
				DS3649	2.7	3.5		V
				DS3679	2.6	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V	I_{OL} = 20 mA	DS1649		0.6	1.1	V
				DS1679		0.3	0.5	V
				DS3649		0.6	1.0	V
				DS3679		0.3	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V	V_{OUT} = 0V (Note 2)	DS1649/DS1679		−170		mA
				DS3649/DS3679		−170		mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V	V_{OUT} = 4.5V (Note 2)	DS1649/DS1679		170		mA
				DS3649/DS3679		170		mA
$I_{CC(MAX)}$	Maximum Power Supply Current	V_{CC} = 5.5V		DS1649/DS1679		42		mA
				DS3649/DS3679		42		mA
$I_{CC(MIN)}$	Minimum Power Supply Current	V_{CC} = 5.5V		DS1649/DS1679		11		mA
				DS3649/DS3679		11		mA

switching characteristics

(V_{CC} = 5V, T_A = 25°C) (Note 4)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{pd(0)}$	Propagation Delay to Logical "0"	*(Figure 1)*	C_L = 50 pF		7		ns
			C_L = 250 pF		15		ns
			C_L = 500 pF		25		ns
$t_{pd(1)}$	Propagation Delay to Logical "1"	*(Figure 1)*	C_L = 50 pF		7		ns
			C_L = 250 pF		15		ns
			C_L = 500 pF		25		ns
t_{H0}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	C_L = 50 pF to Gnd	R_L = 2 kΩ to V_{CC} *(Figure 2)*		14		ns
t_{H1}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	C_L = 50 pF to Gnd	R_L = 2 kΩ to Gnd *(Figure 2)*		14		ns
t_{0H}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	C_L = 50 pF to Gnd	R_L = 400Ω to V_{CC} *(Figure 3)*		14		ns
t_{1H}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	C_L = 50 pF to Gnd	R_L = 400Ω to Gnd *(Figure 3)*		14		ns

notes

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

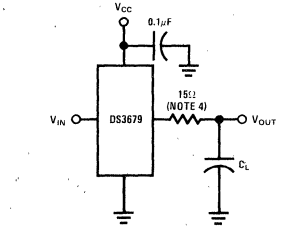
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1649 and DS1679 and across the 0°C to +70°C range for the DS3649 and DS3679. All typical values are for T_A = 25°C and V_{CC} = 5V.

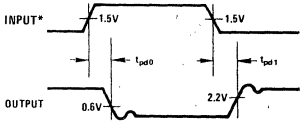
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS1679 and DS3679 a 15 ohm resistor should be placed in series with each output. This resistor is internal to the DS1649/DS3649 and need not be added.

ac test circuits and switching time waveforms

t_{pd0} and t_{pd1}

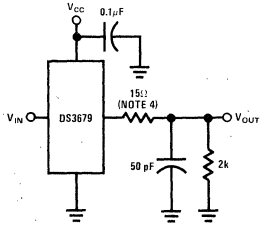




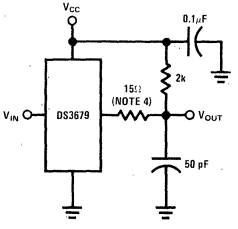
*Input Signal Characteristics:
Freq = 1 MHz
Duty cycle = 50%
Amplitude = 0.4V to 3.0V
$t_r = t_f$ = 2.5 ns

FIGURE 1

t_{H1}



t_{H0}



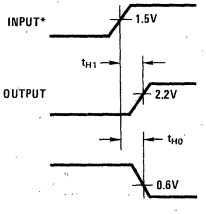
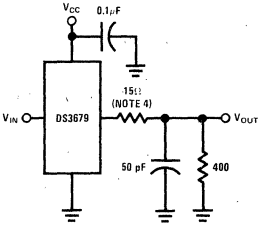
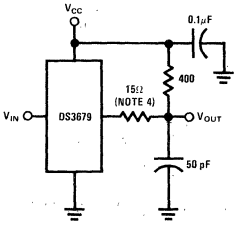


FIGURE 2

t_{1H}



t_{0H}



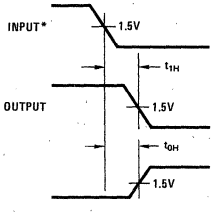


FIGURE 3

NATIONAL

Memory/Clock Drivers

Advance Information*

DS1671/DS3671 bootstrapped two phase MOS clock driver

general description

The DS1671/DS3671 is a high speed dual MOS clock driver and interface circuit. Unique circuit design provides both very high speed operation and the ability to drive large capacitive loads. The device accepts standard TTL/DTL outputs and converts them to MOS logic levels. It may be driven from standard 54/74 and 54S/74S series gates and flip-flops or from drivers such as the DS8830 or DM7440. The circuit can be used in both P-channel and N-channel MOS memory system drive applications.

The DS1671/DS3671 is intended to fulfill a wide variety of MOS interface requirements. As a MOS clock driver for long silicon gate shift registers, a single device can drive over 10k bits at 5 MHz. Six devices provide input address and precharge drive for an 8k by 16-bit 1103 RAM memory system.

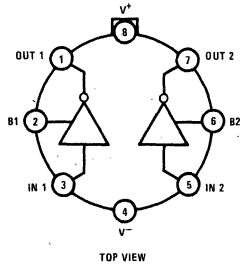
Each driver uses output bootstrapping to provide a higher voltage to the output stage, thus eliminating the need for an additional V_{DD} supply. The bootstrapping function is accomplished by connecting a small value capacitor (typically 200 pF) from each output to each drivers bootstrap node.

features

- Fast rise and fall times—20 ns with 1000 pF load
- High output swing—20V
- High output current drive—±1.5A
- TTL/DTL compatible inputs
- High rep rate—5 to 10 MHz depending on power dissipation
- Low power consumption in MOS "0" state—2 mW
- Swings to 0.4V of GND for RAM address drive

connection diagrams

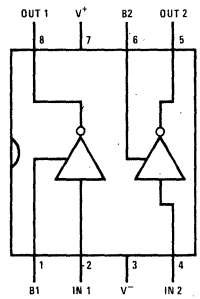
Metal Can Package



TOP VIEW

Order Number DS1671H or DS3671H

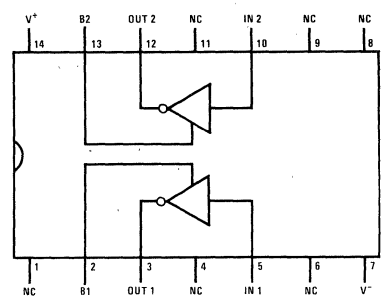
Dual-In-Line Package



TOP VIEW

Order Number DS3671N

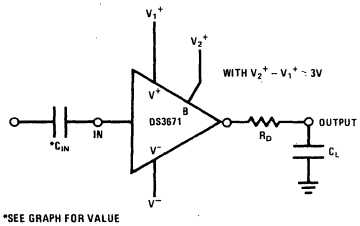
Dual-In-Line Package



TOP VIEW

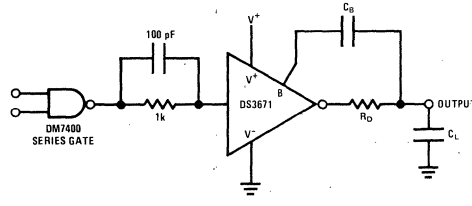
Order Number DS1671J or DS3671J

typical applications



*SEE GRAPH FOR VALUE

DS3671 Operating with Extra Supply to Inhance Output Voltage Level



Bootstrap Clock Driver Driven from a TTL Gate

*Specifications may change.

absolute maximum ratings (Note 1)

$V^+ - V^-$ Differential	22V
$V_B - V^-$ Differential	40V
$V_B - V^+$ Differential	20V
Input Voltage ($V_{IN} - V^-$)	5.5V
Input Current	100 mA
Peak Output Current	1.5A
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation* (P_D)	
Ceramic Package	1160 mW
Molded Package	890 mW
Metal Can	525 mW

operating conditions

	MIN	MAX	UNITS
Supply Voltage			
$V^+ - V^-$ Differential		20	V
$V_B - V^-$ Differential		40	V
$V_B - V^+$ Differential		20	V
Operating Temperature Range			
DS3671	0	+70	°C
DS1671	−55	+125	°C

* Derate ceramic package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C; derate metal can package at 200°C/W above 70°C.

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	$V^- = 0V$		2.0	1.5		V
I_{IH}	Logical "1" Input Current	$V_{IN} - V^- = 2.4V$			10	15	mA
V_{IL}	Logical "0" Input Voltage	$V^- = 0V$			0.6	0.4	V
I_{IL}	Logical "0" Input Current	$V_{IN} - V^- = 0V$			−3	−10	μA
V_{OH}	Logical "1" Output Voltage	$V_B \geq V^+ + 1.0V$, $V_{IN} - V^- \equiv 0.4V$, $I_O = 0$ mA	DS3671	V^+−1.0	V^+−0.75		V
			DS1671	V^+−1.2	V^+−0.75		V
V_{OL}	Logical "0" Output Voltage	$V_{IN} - V^- = 2.4V$, $I_O = 0$ mA			V^-+0.6	V^-+1.0	V
R_B	Bootstrap Control Resistor			1.1	2.0	3.3	kΩ
$I_{CC(ON)}$	Supply Current One Side "ON"	$V^+ - V^- = 20V$, $V_{IN} - V^- = 2.4V$, $V_B = V^+$ (One Side Only)			30	40	mA
$I_{CC(OFF)}$	Supply Current "OFF"	$V^+ - V^- = 20V$, $V_{IN} - V^- = 0V$	DS3671		10	100	μA
			DS1671		50	500	μA

switching characteristics $T_A = 25°C$, $V^+ = 20V$, $V^- = 0V$

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0"	$R_D = 10\Omega$, $C_L = 1000$ pF			7.5		ns
t_{pd1}	Propagation Delay to a Logical "1"	$R_D = 10\Omega$, $C_L = 1000$ pF			12		ns
t_r	Rise Time	$R_D = 10\Omega$	$C_L = 500$ pF		25		ns
			$C_L = 1000$ pF		31		ns
t_f	Fall Time	$R_D = 10\Omega$	$C_L = 500$ pF		30		ns
			$C_L = 1000$ pF		38		ns

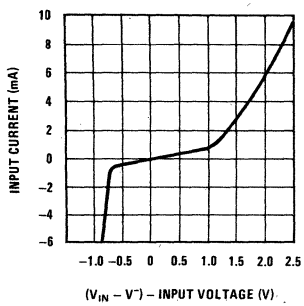
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1671 and across the 0°C to +70°C range for the DS3671. All typicals at 25°C.

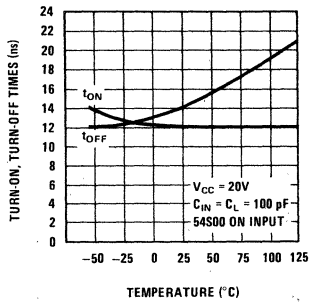
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

typical performance characteristics

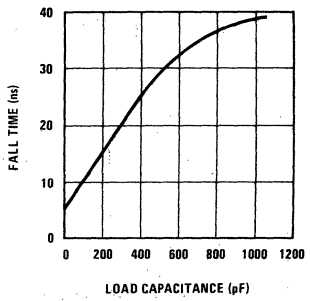
Input Current vs Input Voltage



Turn-On and Turn-Off Time vs Temperature

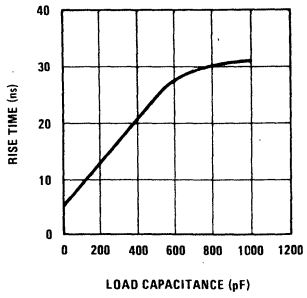


Fall Time vs Load Capacitance

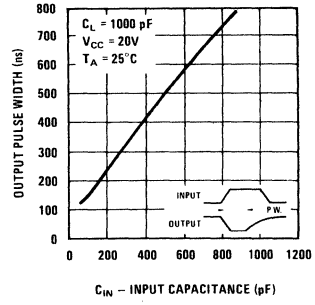


typical performance characteristics (con't)

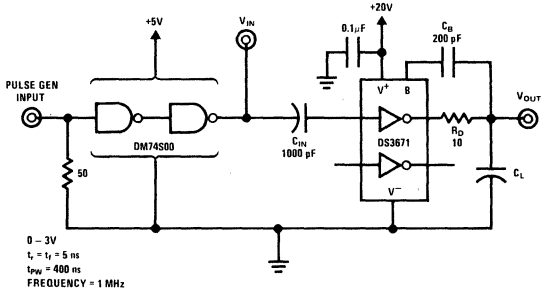
Rise Time vs Load Capacitance

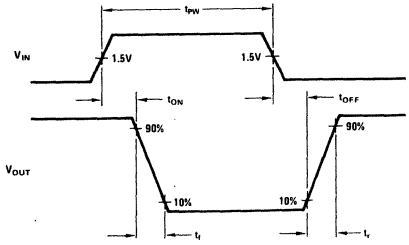


Output Pulse Width When Controlled Only by Input Coupling Capacitor

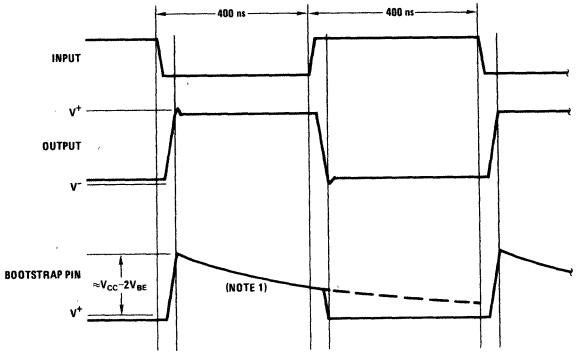


ac test circuit and switching time waveforms





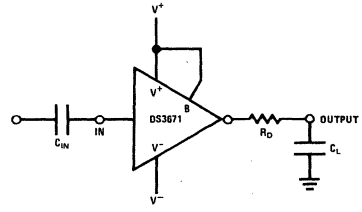
node voltage waveforms



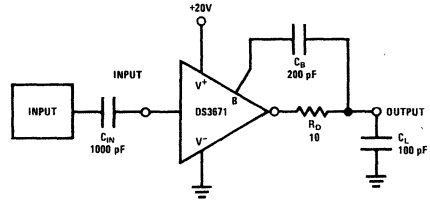
Note 1: The fall time has an exponential decay with the following time constant: $t_8 = C_B R_B$. The range of values for R_B (resistor tolerance, and temperature coefficient included) can be found in the table of electrical characteristics.

Note 2: The high current transient (as high as 1.5A) through the resistance of the external interconnecting V^- lead during the output transition from the high state to the low state can appear as negative feedback to the input. If the external interconnecting lead from the driving circuit to V^- is electrically long, or has significant DC resistance, it can subtract from the switching response.

typical applications (con't)

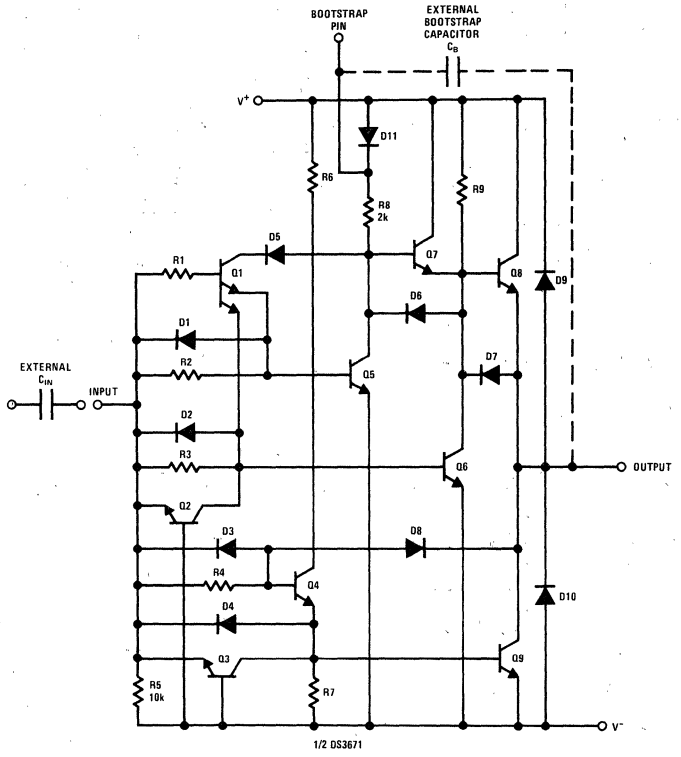


DS3671 Connected as DS0026 with Equivalent Characteristics



Typical Bootstrap

schematic diagram (One Driver)



NATIONAL

Memory/Clock Drivers
Advance Information*

DS16149/DS36149, DS16179/DS36179 hex MOS drivers

general description

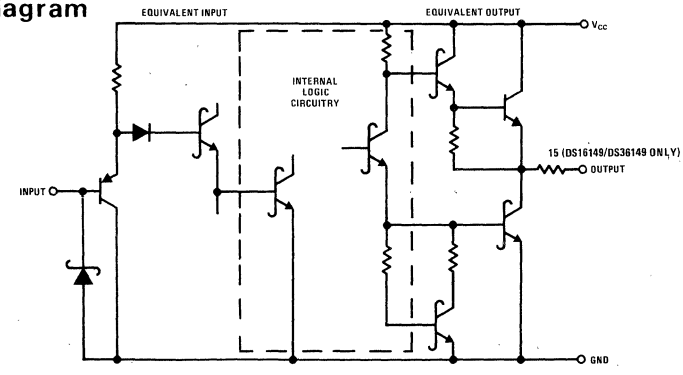
The DS16149/DS36149 and DS16179/DS36179 are Hex MOS drivers with outputs designed to drive large capacitive loads up to 500 pF associated with MOS memory systems. PNP input transistors are employed to reduce input currents allowing the large fan-out to these drivers needed in memory systems. The circuit has Schottky-clamped transistor logic for minimum propagation delay, and a disable control that places the outputs in the logical "1" state (see truth table). This is especially useful in MOS RAM applications where a set of address lines has to be in the logical "1" state during refresh.

The DS16149/DS36149 has a 15 ohm resistor in series with the outputs to dampen transients caused by the fast-switching output. The DS16179/DS36179 has a direct low impedance output for use with or without an external resistor.

features

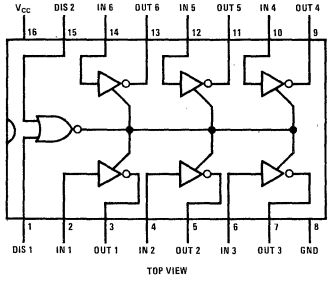
- High speed capabilities
  - Typ 7 ns driving 50 pF
  - Typ 25 ns driving 500 pF
- Built-in 15 ohm damping resistor (DS16149/DS36149)
- Same pin-out as DS8096 and DS74366

schematic diagram



connection diagram

Dual-In-Line Package



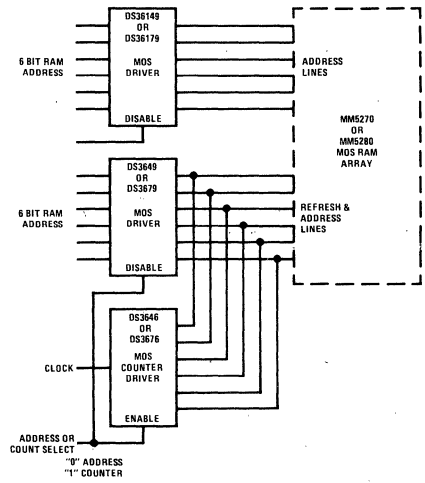
Order Number DS16149J, DS16179J, DS36149J, DS3617J, DS36149N or DS36179N

truth table

DISABLE INPUT		INPUT	OUTPUT
DIS 1	DIS 2		
0	0	0	1
0	0	1	0
0	1	X	1
1	0	X	1
1	1	X	1

X = Don't care

typical application



*Specifications may change.

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Power Dissipation	600 mW
Logical "1" Input Voltage	7.0V
Logical "0" Input Voltage	−1.5V
Logical "1" Output Current	<1.0 A
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation (P_D)	
Ceramic Package	1160 mW
Molded Package	1000 mW

operating conditions

	MIN	MAX	UNITS
Logical "0" Output Current, ($I_{OS(0)}$)		<1	A
Operating Temperature Range, (T_{MAX})	0	+70	°C

* Derate ceramic package at 80°C/W above 70°C; derate molded package at 90°C/W above 70°C.

electrical characteristics (Note 2 and 3)

Over recommended operating temperature range (unless otherwise noted) (Note 1)

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage				2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage						0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.5V	V_{IN} = 5.5V			0.1	40	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.5V	V_{IN} = 0.5V			−90	−250	μA
V_{CLAMP}	Input Clamp Voltage		I_{IN} = −18 mA				−1.2	V
V_{OH}	Logical "1" Output Voltage (No Load)	V_{CC} = 4.5V	I_{OH} = 0 mA	DS16149/DS16179	3.4	4.25		V
				DS36149/DS36179	3.5	4.25		V
V_{OL}	Logical "0" Output Voltage (No Load)	V_{CC} = 4.5V	I_{OL} = 0 mA	DS16149/DS16179		0.25	0.45	V
				DS36149/DS36179		0.25	0.40	V
V_{OH}	Logical "1" Output Voltage (With Load)	V_{CC} = 4.5V	I_{OH} = −1.0 mA	DS16149	2.5	3.5		V
				DS16179	2.4	3.5		V
				DS36149	2.7	3.5		V
				DS36179	2.6	3.5		V
V_{OL}	Logical "0" Output Voltage (With Load)	V_{CC} = 4.5V	I_{OL} = 20 mA	DS16149		0.6	1.1	V
				DS16179		0.3	0.5	V
				DS36149		0.6	1.0	V
				DS36179		0.3	0.5	V
I_{ID}	Logical "1" Drive Current	V_{CC} = 4.5V	V_{OUT} = 0V (Note 2)	DS16149/DS16179	−170			mA
				DS36149/DS36179	−170			mA
I_{OD}	Logical "0" Drive Current	V_{CC} = 4.5V	V_{OUT} = 4.5V (Note 2)	DS16149/DS16179		170		mA
				DS36149/DS36179		170		mA
$I_{CC(MAX)}$	Maximum Power Supply Current	V_{CC} = 5.5V		DS16149/DS16179		42		mA
				DS36149/DS36179		42		mA
$I_{CC(MIN)}$	Minimum Power Supply Current	V_{CC} = 5.5V		DS16149/DS16179		11		mA
				DS36149/DS36179		11		mA

switching characteristics

(V_{CC} = 5V, T_A = 25°C) (Note 4)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{pd(0)}$	Propagation Delay to Logical "0"	*(Figure 1)*	C_L = 50 pF		7		ns
			C_L = 250 pF		15		ns
			C_L = 500 pF		25		ns
$t_{pd(1)}$	Propagation Delay to Logical "1"	*(Figure 1)*	C_L = 50 pF		7		ns
			C_L = 250 pF		15		ns
			C_L = 500 pF		25		ns
t_{H1}	Delay from Disable Input to Logical "1"	C_L = 500 pF to Gnd	R_L = 2 kΩ to Gnd *(Figure 2)*		25		ns

notes

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS16149 and DS16179 and across the 0°C to +70°C range for the DS36149 and DS36179. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: When measuring output drive current and switching response for the DS16179 and DS36179 a 15 ohm resistor should be placed in series with each output. This resistor is internal to the DS16149/DS36149 and need not be added.

ac test circuits and switching time waveforms

t_{pd0} and t_{pd1}

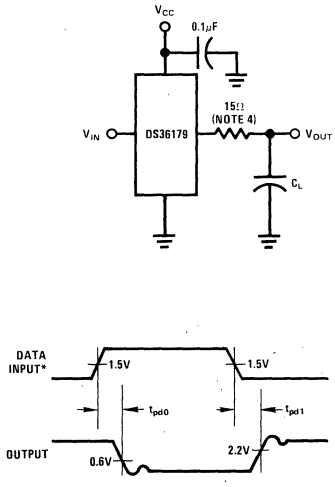


FIGURE 1

t_{H1}

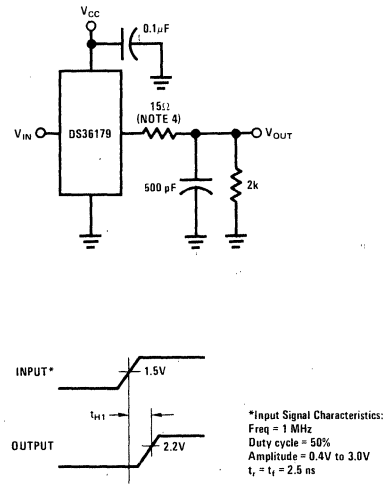


FIGURE 2

NATIONAL

Memory/Clock Drivers

DS7803/DS8803, DS8813 two phase oscillator/clock driver

general description

The DS7803 is a self contained two phase oscillator/clock driver. It requires no external components to generate one of three primary oscillator frequencies and pulse widths. Other frequencies can easily be obtained by programming input voltages. Three sets of outputs are provided: damped and undamped MOS outputs and TTL monitor outputs. The MOS outputs easily drive 500 pF loads with less than 150 ns rise and fall times. In addition the outputs have current limiting to protect against momentary shorts to the supplies.

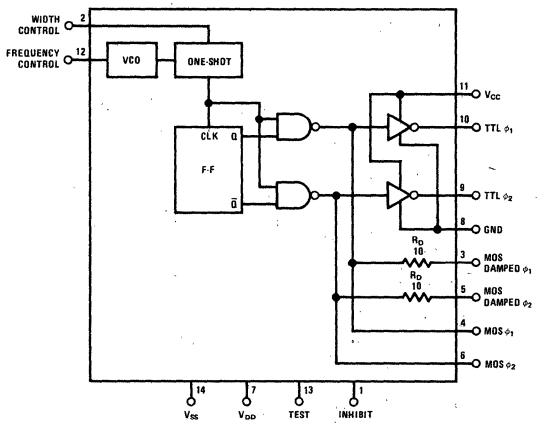
The DS7803 and DS8803 are available in a 14-lead cavity DIP. The DS8803 is also available in a 14-pin molded DIP. The DS8813 comes in an 8-pin molded DIP, providing damped MOS outputs only.

features

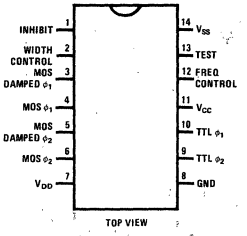
- Two phase non-overlapping outputs
- No external timing components required
- Frequency adjustable from 100 kHz to 500 kHz
- Pulse width adjustable from 260 ns to 1.4μs
- Damped and undamped MOS outputs
- TTL monitor outputs

block and connection diagrams

DS7803/DS8803

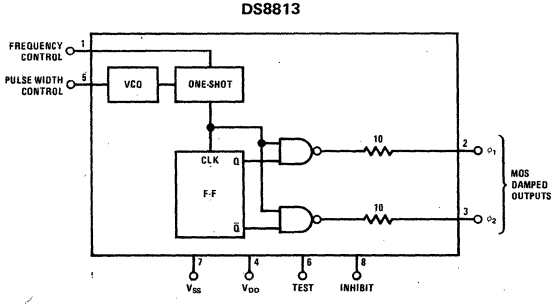


Dual-In-Line Package

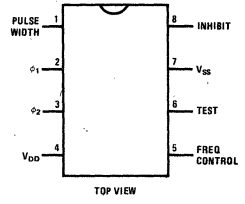


Order Number DS7803J, DS8803J or DS8803N

DS8813



Dual-In-Line Package



Order Number DS8813N

absolute maximum ratings

$V_{SS} - V_{DD}$	22V	Operating Temperature Range	
V_{CC} – Gnd	7.0V	DS7803	–55°C to +125°C
Pulse Width Adjust Voltage	V_{SS}	DS8803, DS8813	0°C to +70°C
Frequency Adjust Voltage	V_{SS}	Storage Temperature Range	–65°C to +150°C
$V_{SS} - V_{DD}$, Minimum	14V	Lead Temperature (Soldering, 10 seconds)	300°C
Test and Inhibit Input Voltages	V_{SS}		

electrical characteristics (Notes 1, 3)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
F Frequency	T_A = 25°C	Pin 12 at 17V		300	500	600	kHz
		Pin 12 Open		175	300	350	kHz
		Pin 12 at 0V		60	100	150	kHz
ΔF Frequency Change from 25°C	Pin 12 at 17V	DS7803	DS7803		±20	±30	%
			DS8803		±10	±15	%
PW Pulse Width	C_L = 15 pF, T_A = 25°C, (Note 2)	Pin 2 at 17V		0.2	0.26	0.4	μs
		Pin 2 Open		0.5	0.75	1.3	μs
		Pin 2 at 0V		1.0	1.4	2.6	μs
ΔPW Pulse Width Change from 25°C	Pin 2 at 17V		DS7803		±20	±30	%
			DS8803		±10	±15	%
V_{OH} Logical "1" Output Voltage	I_{OH} = –100μA	MOS		V_{SS}–1.1	V_{SS}–0.8		V
	I_{OH} = –200μA	TTL		2.4	3.7		V
V_{OL} Logical "0" Output Voltage	MOS Outputs	I_{OL} = 2.0 mA			V_{DD}+0.15	V_{DD}+0.5	V
	TTL Outputs	I_{OL} = 2.0 mA	DS7803		0.17	0.3	V
		I_{OL} = 3.2 mA	DS8803		0.2	0.4	V
I_{OS} Output Short Circuit Current	TTL Outputs			3.0	8.0	15	mA
I_{OS} Output Current Limit	MOS Outputs				±70		mA
I_{SS} Supply Current	Pins 2, 12, 13 at 0V, and Pin 1 at –0.3V				10	17	mA
I_{CC} Supply Current	Pins 2 and 12 at 0V, and Pin 1 at –0.3V				0.75	1.1	mA
R_D Damping Resistor			DS7803	7.0	10	13	Ω
			DS8803	5.0	10	15	Ω
t_r,t_f Rise and Fall Times	T_A = 25°C, MOS	C_L = 500 pF			100	150	ns
		C_L = 50 pF			20	30	ns

Note 1: These specifications apply for the DS7803 at $V_{SS} - V_{DD}$ = 17V ±10% and over –55°C to +125°C; for the DS8803, DS8813 at $V_{SS} - V_{DD}$ = 17V ±5% and over 0°C to +70°C unless otherwise specified.

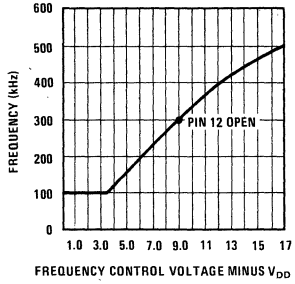
Note 2: The duty cycle can not physically exceed 50% at any output. At high frequencies the frequency adjust pin will affect the pulse width by limiting the duty cycle to slightly less than 50%. Under this condition the pulse width spec does not apply.

Note 3: The above specs apply to the DS8813 only where applicable, and approriate pin numbers should be substituted.

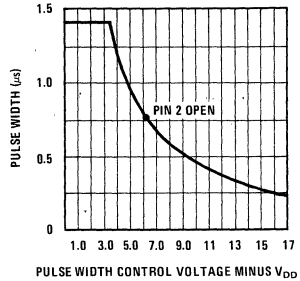
4

typical performance characteristics

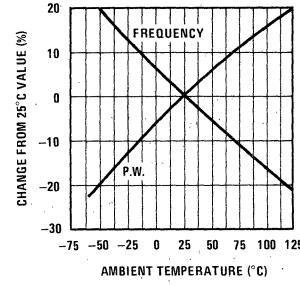
Frequency Control Voltage



Pulse Width Control Voltage

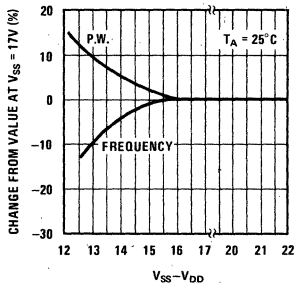


Frequency and Pulse Width vs Temperature

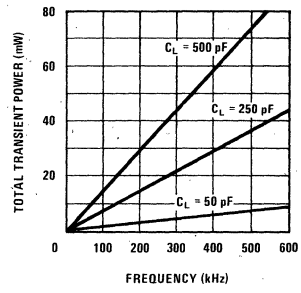


typical performance characteristics (con't)

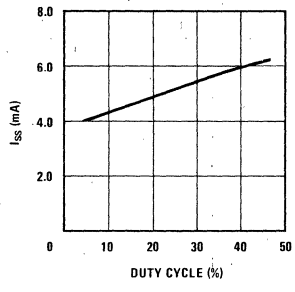
Frequency and Pulse Width



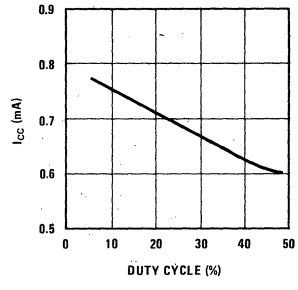
Total Transient Power vs Frequency



I_{SS} vs Duty Cycle



I_{CC} vs Duty Cycle



applications information

TTL MONITOR OUTPUTS

The TTL outputs are extra functions provided for monitor or synchronization applications. In some systems these outputs may not be required. For these cases, the V_{CC} pin may be left open and the TTL circuitry power consumption will be virtually zero. For small space requirements, the DS8813 8-pin DIP is available, which has the TTL outputs deleted.

The TTL outputs are slaved to the MOS outputs. Thus the TTL outputs start to switch when the MOS outputs cross the TTL threshold voltage (about 1.5V above ground). *Figure 1* depicts the effect of different supply voltages on the TTL waveform when the MOS outputs are driving capacitive loads.

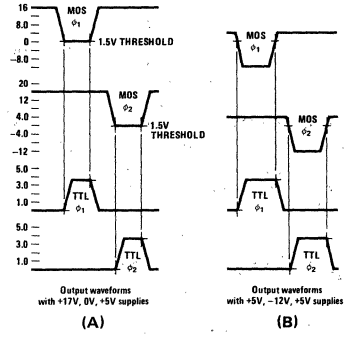


FIGURE 1.

DAMPED MOS OUTPUTS

An extra set of MOS outputs provides a 10 ohm resistor in series with each output line. These resistors give the output pulses an RC rolloff which tends to minimize ringing or peaking problems associated with board layout.

INHIBIT AND TEST INPUTS

The INHIBIT and TEST inputs are designed to facilitate testing of the device. They were not included in the IC for system use. The truth table of *Figure 2* supplements the following functional description:

INHIBIT Input: in the low state prevents pulses from being initiated on either phase output.

High Level Input:

$$V_{IH} \geq V_{DD} + 2.0V$$

Low level Input:

$$V_{DD} + 0.2V \geq V_{IL} \geq V_{DD} - 0.5V$$

applications information (cont.)

INHIBIT INPUT	TEST INPUT	OUTPUT
Open	Open	Normal Operation
Low	Open	High
Low	Low	Low

FIGURE 2. Truth Table

TEST Input: in the low state forces a "1" state on all outputs. The test input should only be used with the INHIBIT input also in the low state.

High Level:

$$V_{IH} \geq V_{DD} + 8.0V$$

Low Level:

$$V_{DD} + 0.5V \geq V_{IL} \geq V_{DD}$$

A pull-up resistor is connected from the TEST pin to V_{SS} internally.

POWER CONSIDERATIONS

Internal power dissipation is affected by three factors:

1. dc power
2. ac power
3. package dissipation capability

The total average power dissipation is the summation of the dc power and ac power. This sum must be less than the maximum package dissipation capability at the particular operating temperature to insure safe operation, i.e.:

$$P_{DISS} = P_{AC} + P_{DC} \leq P_{MAX}$$

Where:

$$P_{AC} = P_{AC\ TTL} + P_{AC\ MOS}$$

$$P_{AC} = [(V_{CC} - Gnd)^2 \times f \times C_L]_{TTL} + [(V_{SS} - V_{DD})^2 \times f \times C_L]_{MOS}$$

And

$$P_{DC} = (I_{CC}) \times (V_{CC} - Gnd) + (I_{SS}) \times (V_{SS} - V_{DD})$$

for I_{CC} and I_{SS} at the appropriate duty cycle.

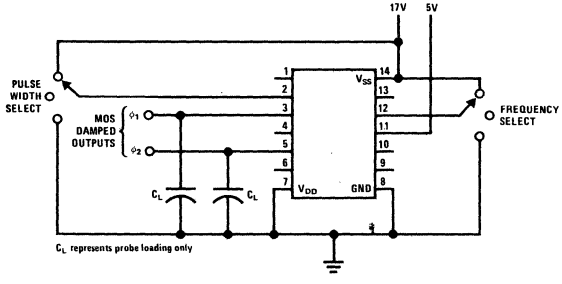
For practical cases the $P_{AC\ TTL}$ can be neglected as being very small compared to $P_{AC\ MOS}$.

Thus P_{DISS} is the sum of the MOS transient power (total for both sides of the DS7803) and the standby power of the TTL and MOS sections of the DS7803.

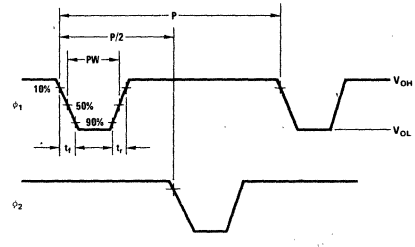
DECOUPLING

It is recommended that each device be decoupled with a 0.1μF capacitor from V_{SS} to V_{DD}. If there is noise on the supply lines, better frequency and pulse width stability can be obtained by connecting a 0.001μF capacitor from the frequency control pin to V_{DD} and another 0.001μF capacitor from the pulse width control pin to V_{DD}.

ac test circuit



timing diagram



4

DS7807/DS8807, DS8817 two phase oscillator/clock driver

general description

The DS7807 is a self contained two phase oscillator/clock driver. It requires no external components to generate one of three primary oscillator frequencies and pulse widths. Other frequencies can easily be obtained by programming input voltages. Three sets of outputs are provided: damped and un-damped MOS outputs and TTL monitor outputs. The MOS outputs easily drive 500 pF loads with less than 75 ns rise and fall times. In addition the outputs have current limiting to protect against momentary shorts to the supplies.

The DS7807 and DS8807 are available in a 14-lead cavity DIP. The DS8807 is also available in a 14-pin molded DIP.

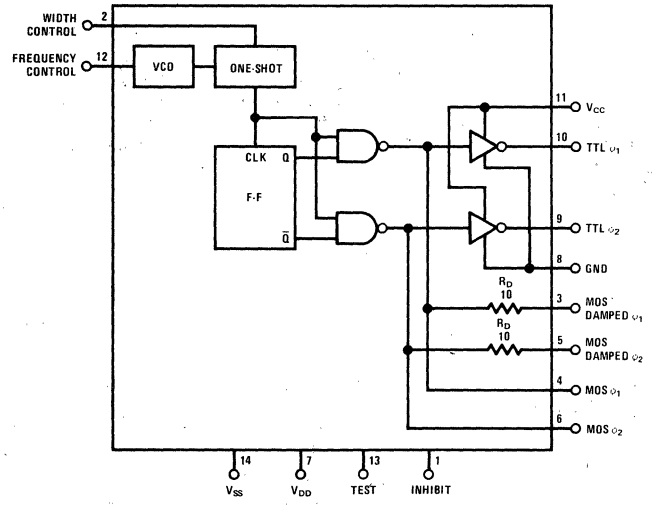
The DS8817 comes in an 8-pin molded DIP, providing damped MOS outputs only.

features

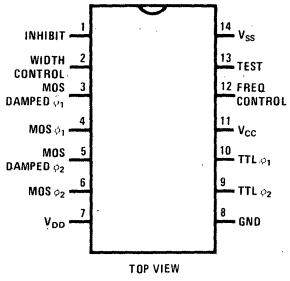
- Two phase non-overlapping outputs
- No external timing components required
- Frequency adjustable from 400 kHz to 2 MHz
- Pulse width adjustable from 130 ns to 700 ns
- Damped and un-damped MOS outputs
- TTL monitor outputs

block and connection diagrams

DS7807/DS8807



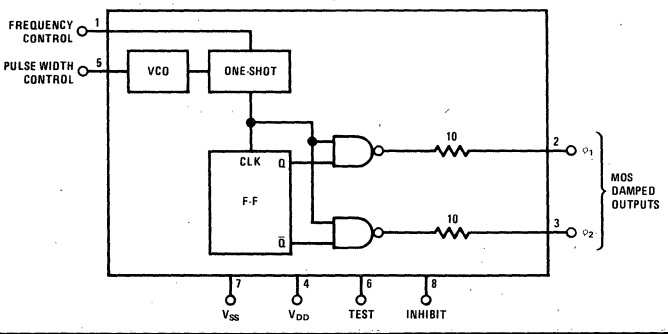
Dual-In-Line Package



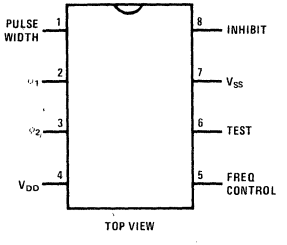
TOP VIEW

Order Number DS7807J, DS8807J or DS8807N

DS8817



Dual-In-Line Package



TOP VIEW

Order Number DS8817N

absolute maximum ratings

$V_{SS}-V_{DD}$	22V
$V_{CC}-GND$	7.0V
Pulse Width Adjust Voltage	V_{SS}
Frequency Adjust Voltage	V_{SS}
$V_{SS}-V_{DD}$, Minimum	14V
Test and Inhibit Input Voltages	V_{SS}
Operating Temperature Range	
DS7807	−55°C to +125°C
DS8807, DS8817	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Notes 1 and 3)

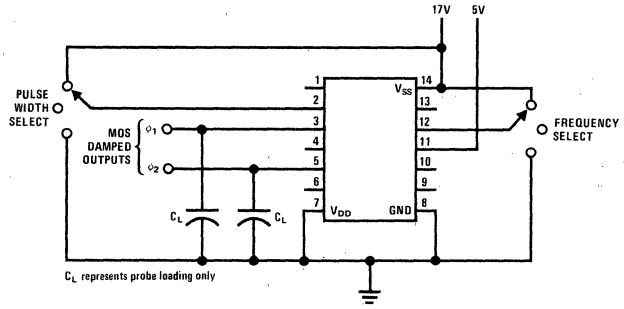
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
F	Frequency	T_A = 25°C	Pin 12 at 17V		2.0		MHz
			Pin 12 Open		1.2		MHz
			Pin 12 at 0V		400		kHz
ΔF	Frequency Change from 25°C	Pin 12 at 17V	DS7807		±20		%
			DS8807		±10		%
PW	Pulse Width	C_L = 15 pF, T_A = 25°C, (Note 2)	Pin 2 at 17V		0.13		μs
			Pin 2 Open		0.38		μs
			Pin 2 at 0V		0.70		μs
ΔPW	Pulse Width Change from 25°C	Pin 2 at 17V	DS7807		±20		%
			DS8807		±10		%
V_{OH}	Logical "1" Output Voltage	MOS, I_{OH} = −100μA		V_{SS}−1.1	V_{SS}−0.8		V
		TTL, I_{OH} = −200μA		2.4	3.7		V
V_{OL}	Logical "0" Output Voltage	MOS, I_{OL} = 2.0 mA			V_{DD}+0.15	V_{DD}+0.5	V
		TTL	I_{OL} = 2.0 mA, DS7807		0.17	0.3	V
			I_{OL} = 3.2 mA, DS8807		0.2	0.4	V
I_{OS}	Output Short Circuit Current	TTL		3.0	8.0	15	mA
I_{OS}	MOS Output Current Limit				±140		mA
I_{SS}	Supply Current	Pins 2, 12, 13 at 0V, and Pin 1 at −0.3V			13		mA
I_{CC}	Supply Current	Pins 2, 12 at 0V, and Pin 1 at −0.3V			0.75	1.1	mA
R_D	Damping Resistor		DS7807	7.0	10	13	Ω
			DS8707	5.0	10	15	Ω
t_r, t_f	Rise Time and Fall Time	T_A = 25°C, MOS	C_L = 500 pF		50		ns
			C_L = 50 pF		10		ns

Note 1: These specifications apply for the DS7807 at $V_{SS} - V_{DD}$ = 17V ±10% and over −55°C to +125°C; for the DS8807, DS8817 at $V_{SS} - V_{DD}$ = 17V ±5% and over 0°C to +70°C unless otherwise specified.

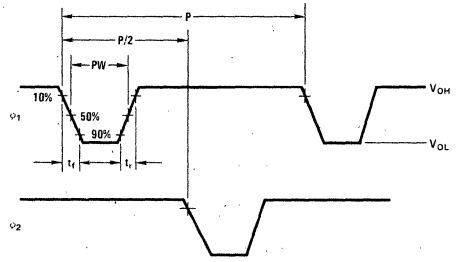
Note 2: The duty cycle can not physically exceed 50% at any output. At high frequencies the frequency adjust pin will affect the pulse width by limiting the duty cycle to approximately 40%. Under this condition the pulse width spec does not apply.

Note 3: The above specs apply to the DS8817 only where applicable, and appropriate pin numbers should be substituted.

ac test circuit



timing diagram



applications information

TTL MONITOR OUTPUTS

The TTL outputs are extra functions provided for monitor or synchronization applications. In some systems these outputs may not be required. For these cases the V_{CC} pin may be left open and the TTL circuitry power consumption will be virtually zero. For small space requirements, the DS8817 8-pin DIP is available which has the TTL outputs deleted.

The TTL outputs are slaved to the MOS outputs. Thus the TTL outputs start to switch when the MOS outputs cross the TTL threshold voltage (about 1.5V above ground). *Figure 1* depicts the effect of different supply voltages on the TTL waveform when the MOS outputs are driving capacitive loads.

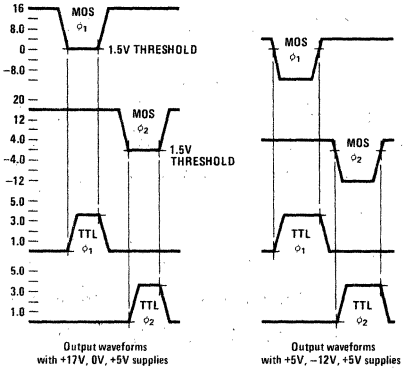


FIGURE 1.

DAMPED MOS OUTPUTS

An extra set of MOS outputs provides a 10 ohm resistor in series with each output line. These resistors give the output pulses an RC rolloff which tends to minimize ringing or peaking problems associated with board layout.

INHIBIT AND TEST INPUTS

The INHIBIT and TEST inputs are designed to facilitate testing of the device. They were not included in the IC for system use.

INHIBIT INPUT	TEST INPUT	OUTPUT
Open	Open	Normal Operation
Low	Open	High
Low	Low	Low

FIGURE 2. Truth Table

The truth table of *Figure 2* supplements the following functional description:

INHIBIT Input: in the low state prevents pulses from being initiated on either phase output.

High Level Input:

$$V_{IH} \geq V_{DD} + 2.0V$$

Low Level Input:

$$V_{DD} + 0.2V \geq V_{IL} \geq V_{DD} - 0.5V$$

applications information (con't)

TEST Input: in the low state forces a ONE state on all outputs. The test input should only be used with the INHIBIT input also in the low state.

High Level:

$$V_{IH} \geq V_{DD} + 8.0V$$

Low Level:

$$V_{DD} + 0.5V \geq V_{IL} \geq V_{DD}$$

A pull-up resistor is connected from the TEST pin to V_{SS} internally.

POWER CONSIDERATIONS

Internal power dissipation is affected by three factors:

1. dc power
2. ac power
3. Package dissipation capability

The total average power dissipation is the summation of the dc power and ac power. This sum must be less than the maximum package dissipation capability at the particular operating temperature to insure safe operation, i.e.:

$$P_{DISS} = P_{AC} + P_{DC} \leq P_{MAX}$$

Where

$$P_{AC} = P_{AC\ TTL} + P_{AC\ MOS}$$

$$P_{AC} = [(V_{CC} - GND)^2 \times f \times C_L]_{TTL} + [(V_{SS} - V_{DD})^2 \times f \times C_L]_{MOS}$$

And

$$P_{DC} = (I_{CC}) \times (V_{CC} - GND) + (I_{SS}) \times (V_{SS} - V_{DD})$$

for I_{CC} and I_{SS} selected at the apporpriate duty cycle.

For practical cases the P_{ACTTL} can be neglected as being very small compared to $P_{AC\ MOS}$.

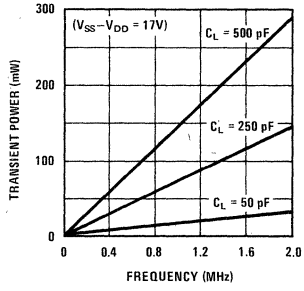
Thus P_{DISS} is the sum of the MOS transient power (total for both sides of the DS7807) and the standby power of the TTL and MOS sections of the DS7807.

DECOUPLING

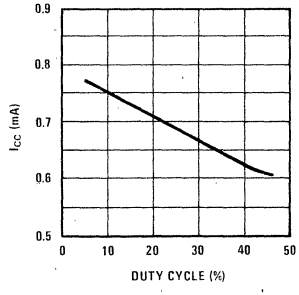
It is recommended that each device be decoupled with a 0.1μF capacitor from V_{SS} to V_{DD}. If there is noise on the supply lines, better frequency and pulse width stability can be obtained by connecting a 0.001μF capacitor from the frequency control pin to V_{DD} and another 0.001μF capacitor from the pulse width control pin to V_{DD}.

typical performance characteristics

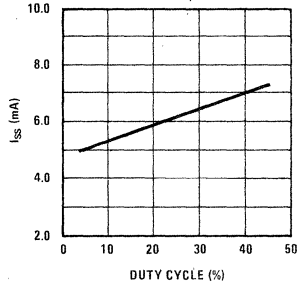
Transient Power vs Frequency



I_{CC} vs Duty Cycle



I_{SS} vs Duty Cycle



4

Memory/Clock Drivers

DS75324 memory driver with decode inputs

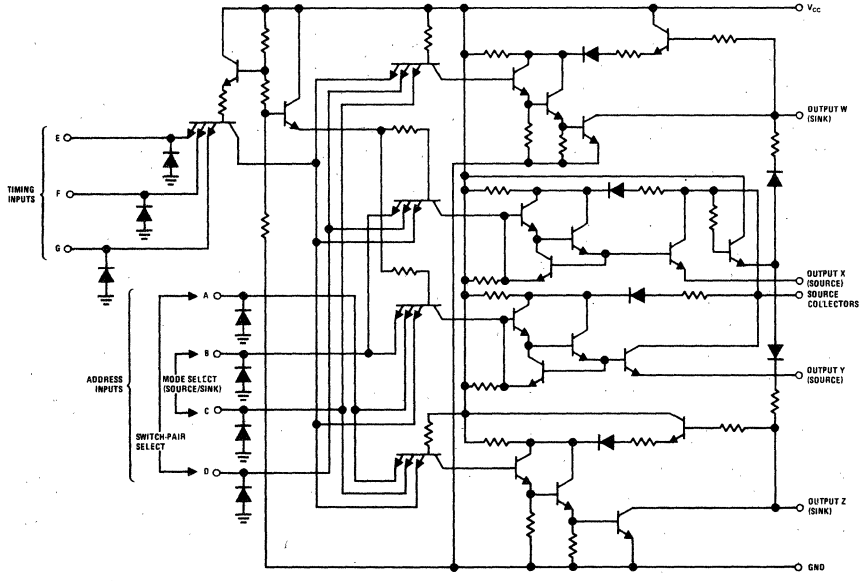
general description

The DS75324 is a monolithic memory driver which features two 400 mA (source/sink) switch pairs along with decoding capability from four address lines. Inputs B and C function as mode selection lines (source or sink) while lines A and D are used for switch-pair selection (output pair Y/Z or W/X).

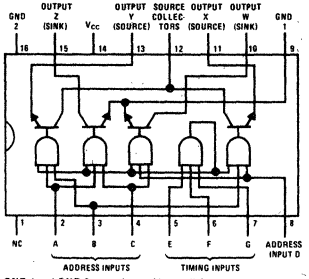
features

- High voltage outputs
- Dual sink/source outputs
- Internal decoding and timing circuitry
- 400 mA output capability
- DTL/TTL compatible
- Input clamping diodes

schematic and connection diagrams



Dual-In-Line Package

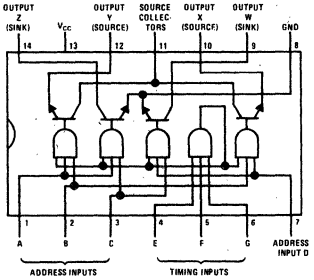


GND 1 and GND 2 are to be used in parallel.

TOP VIEW

Order Number DS75324J

Dual-In-Line Package



TOP VIEW

Order Number DS75324N

absolute maximum ratings (Note 1)

Supply Voltage V_{CC} (Note 4)	17V
Input Voltage (Note 5)	5.5V
Operating Case Temperature Range	0°C to +70°C
Power Dissipation	800 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics (V_{CC} = 14V, T_C = 0°C to +70°C unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Input Voltage Required to Insure Logical "1" At Any Input	*(Figure 1)*		3.5			V
$V_{IN(0)}$	Input Voltage Required to Insure Logical "0" At Any Input	*(Figure 1)*				0.8	V
$I_{IN(1)}$	Logical "1" Level Input Current	V_{IN} = 5V, *(Figure 1)*	Address Input			200	μA
			Timing Input			100	μA
$I_{IN(0)}$	Logical "0" Level Input Current	V_{IN} = 0V, *(Figure 1)*	Address Input			−6	mA
			Timing Input			−12	mA
V_{SAT}	Saturation Voltage	*(Figure 2)*	Sink, $I_{SINK} \simeq$ 420 mA, R_L = 53Ω		0.75	0.85	V
			Source, $I_{SOURCE} \simeq$ −420 mA, R_L = 47.5Ω		0.75	0.85	V
I_{OFF}	Output Reverse Current ("OFF" State)	V_{IN} = 0V, *(Figure 1)*			125	200	μA
I_{CC}	Supply Current	All Sources and Sinks OFF, V_{IN} = 0V, *(Figure 3)*			12.5	15	mA
		(Figure 4)	Either Sink Selected		30	40	mA
			Either Source Selected		25	35	mA
V_I	Input Clamp Voltage	I_{IN} = −12 mA, T_A = 25°C				−1.5	V

ac switching characteristics (V_{CC} = 14V, T_C = 25°C)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd1}	Propagation Delay Time to Logical "1" Level	C_L = 20 pF	Sink Output, R_L = 53Ω, *(Figure 6)*			110	ns
			Source Output, R_{L1} = 53Ω, R_{L2} = 500Ω, *(Figure 5)*			90	ns
t_{pd0}	Propagation Delay Time to Logical "0" Level	C_L = 20 pF	Sink Output, R_L = 53Ω, *(Figure 6)*			40	ns
			Source Output, R_{L1} = 53Ω, R_{L2} = 500Ω, *(Figure 5)*			50	ns
t_s	Sink Storage Time					70	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS75324.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

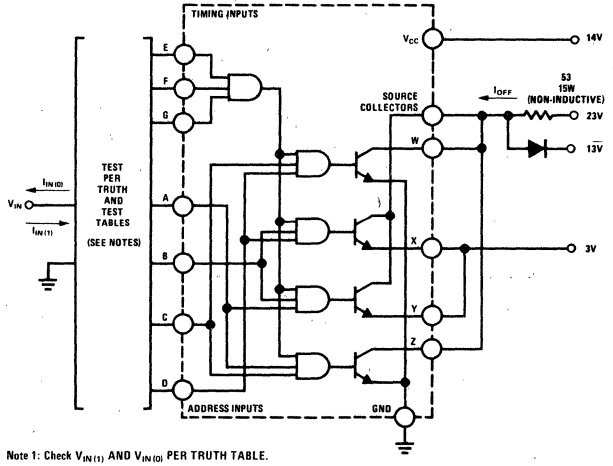
Note 4: Voltage values are with respect to network ground terminal.

Note 5: Input signals must be zero or positive with respect to network ground terminal.

truth table

INPUTS							OUTPUTS			
ADDRESS				TIMING			SINK	SOURCES		SINK
A	B	C	D	E	F	G	W	X	Y	Z
0	0	1	1	1	1	1	ON	OFF	OFF	OFF
0	1	0	1	1	1	1	OFF	ON	OFF	OFF
1	1	0	0	1	1	1	OFF	OFF	ON	OFF
1	0	1	0	1	1	1	OFF	OFF	OFF	ON
X	X	X	X	0	X	X	OFF	OFF	OFF	OFF
X	X	X	X	X	0	X	OFF	OFF	OFF	OFF
X	X	X	X	X	X	0	OFF	OFF	OFF	OFF

test circuits and switching time waveforms



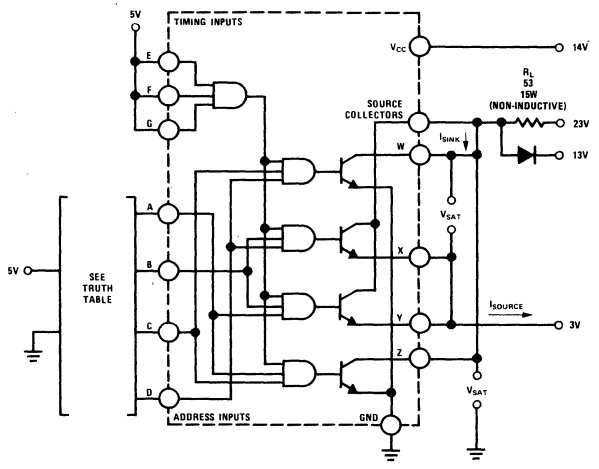
Note 1: Check $V_{IN(1)}$ AND $V_{IN(0)}$ PER TRUTH TABLE.
Note 2: Measure $I_{IN(0)}$ per test table.
Note 3: When measuring $I_{IN(1)}$, all other inputs are at GND. Each input is tested separately.

TEST TABLE FOR $I_{IN(0)}$

APPLY 3.5V	GROUND	TEST $I_{IN(0)}$
B, C, E, F, and G	A and D	A
B, C, E, F, and G	A and D	D
A, D, E, F, and G	B and C	B
A, D, E, F, and G	B and C	C
A, B, C, D, F, and G	E	E
A, B, C, D, E, and G	F	F
A, B, C, D, E, and F	G	G

FIGURE 1. $V_{IN(0)}$, $V_{IN(1)}$, $I_{IN(0)}$, $I_{IN(1)}$, and I_{OFF}

test circuits and switching time waveforms (con't)



Note: This parameter must be measured using pulse techniques.
t_P = 500 ns, duty cycle $\leq$ 1%.

FIGURE 2. $V_{(SAT)}$

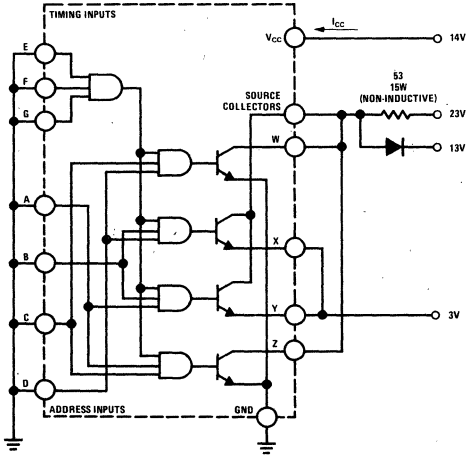
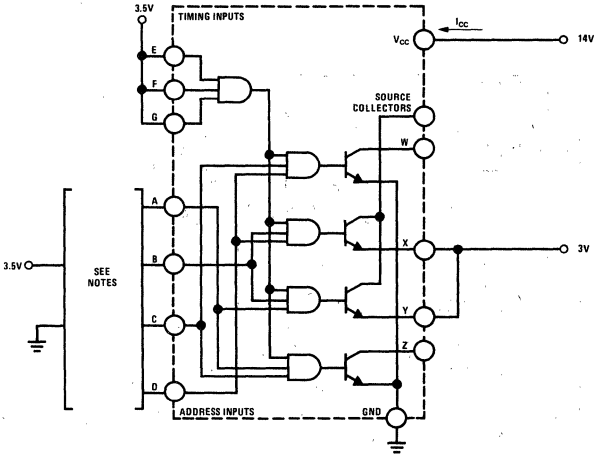


FIGURE 3. I_{CC} (All Outputs "OFF")

test circuits and switching time waveforms (con't)



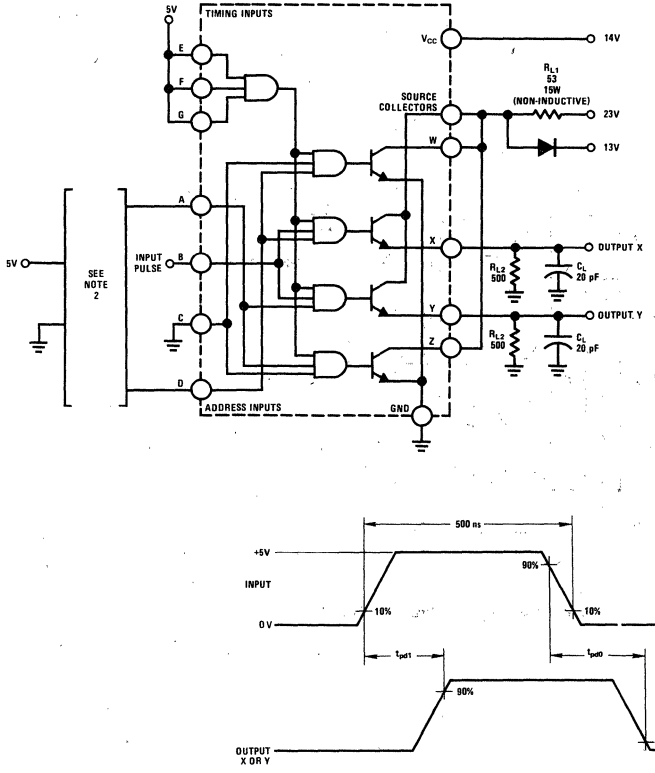
Note 1: GND A and B, apply +3.5V to C and D, and measure I_{CC} (output W is on).

Note 2: GND B and D, apply +3.5V to A and C, and measure I_{CC} (output Z is on).

Note 3: GND A and C, apply +3.5V to B and D, and measure I_{CC} (output X is on).

Note 4: GND C and D, apply +3.5V to A and B, and measure I_{CC} (output Y is on).

FIGURE 4. I_{CC} (One Output "ON")



Note 1: The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10$ ns, duty cycle $\leq 1\%$, and $Z_{OUT} \approx 50\Omega$.

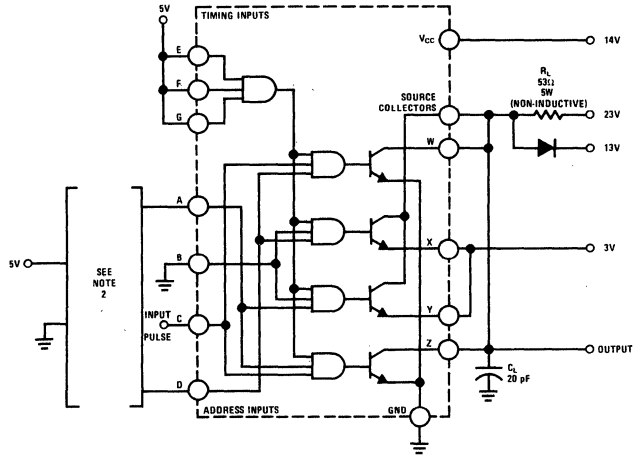
Note 2: When measuring delay times at output X, apply +5V to input D, and GND A. When measuring delay times at output Y, apply +5V to input A, and GND D.

Note 3: C_L includes probe and jig capacitance.

Note 4: Unless otherwise noted all resistors are 0.5W.

FIGURE 5. Source-Output Switching Times

test circuits and switching time waveforms (con't)



Note 1: The input waveform is supplied by a generator with the following characteristics: $t_r = t_f = 10$ ns, duty cycle $\leq 1\%$, $Z_{OUT} \approx 50\Omega$.

Note 2: When measuring delay times at output W, apply +5V to input D, and GND A. When measuring delay times at output Z, apply +5V to input A, and GND D.

Note 3: C_L includes probe and jig capacitance.

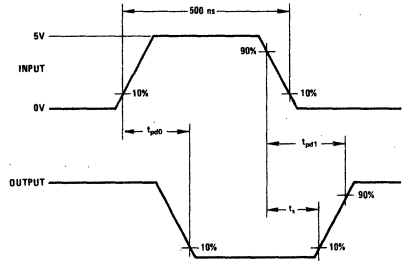


FIGURE 6. Sink-Output Switching Times

Memory/Clock Drivers

DS55325/DS75325 memory drivers general description

The DS55325 and DS75325 are monolithic memory drivers which feature high current outputs as well as internal decoding of logic inputs. These circuits are designed for use with magnetic memories.

The circuit contains two 600 mA sink-switch pairs and two 600 mA source-switch pairs. Inputs A and B determine source selection while the source strobe (S_1) allows the selected source turn on. In the same manner, inputs C and D determine sink selection while the sink strobe (S_2) allows the selected sink turn on.

Sink-output collectors feature an internal pull-up resistor in parallel with a clamping diode connected to V_{CC2}. This protects the outputs from voltage surges associated with switching inductive loads.

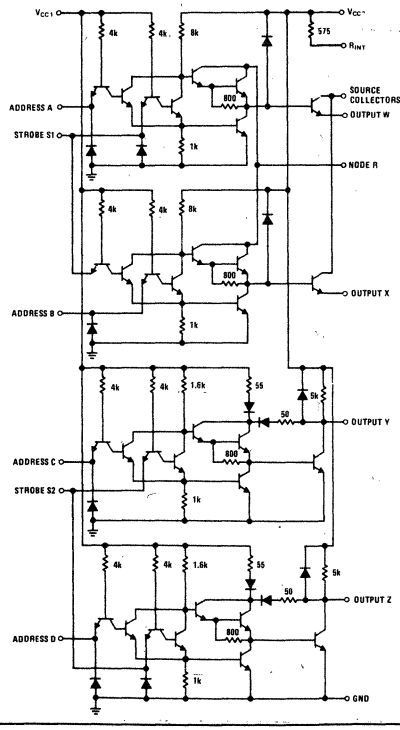
The source stage features Node R which allows extreme flexibility in source current selection by controlling the amount of base drive to each source transistor. This method of setting the base drive brings the power associated with the resistor outside the package thereby allowing the circuit to operate at higher source currents for a given junction temperature. If this method of source current setting is not desired, then Nodes R and R_{INT} can be shorted externally activating an internal resistor connected from V_{CC2} to Node R. This provides adequate base drive for source currents up to 375 mA with V_{CC2} = 15V or 600 mA with V_{CC2} = 24V.

The DS55325 operates over the fully military temperature range of −55°C to +125°C, while the DS5325 operates from 0°C to +70°C.

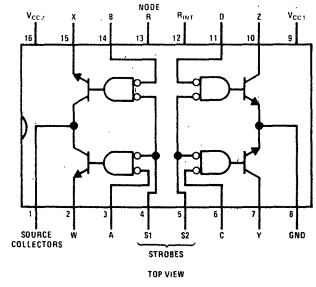
features

- 600 mA output capability
- 24V output capability
- Dual sink and dual source outputs
- Fast switching times
- Source base drive externally adjustable
- Input clamping diodes
- DTL/TTL compatible

schematic and connection diagrams



Dual-In-Line Package



Order Number DS55325J, DS75325J DS75325N or DS55325W

truth table

ADDRESS INPUTS				STROBE INPUTS		OUTPUTS			
SOURCE		SINK		SOURCE	SINK	SOURCE		SINK	
A	B	C	D	S1	S2	W	X	Y	Z
L	H	X	X	L	H	ON	OFF	OFF	OFF
H	L	X	X	L	H	OFF	ON	OFF	OFF
X	X	L	H	H	L	OFF	OFF	ON	OFF
X	X	H	L	H	L	OFF	OFF	OFF	ON
X	X	X	X	H	H	OFF	OFF	OFF	OFF
H	H	H	H	X	X	OFF	OFF	OFF	OFF

H = high level, L = low level, X = irrelevant

NOTE: Not more than one output is to be on at any one time.

absolute maximum ratings (Note 1)

Supply Voltage V_{CC1} (Note 5)	7V
Supply Voltage V_{CC2} (Note 5)	25V
Input Voltage (Any Address or Strobe Input)	5.5V
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Temperature (T_A)			
DS55325	−55	+125	°C
DS75325	0	+70	°C

dc electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	*(Figures 1 and 2)*			2			V
V_{IL}	Low Level Input Voltage	*(Figures 3 and 4)*					0.8	V
V_I	Input Clamp Voltage	V_{CC1} = 4.5V, V_{CC2} = 24V, I_{IN} = −12 mA, T_A = 25°C, *(Figure 5)*				−1.3	−1.7	V
I_{OFF}	Source Collectors Terminal "OFF" State Current	V_{CC1} = 4.5V, V_{CC2} = 2.4V, *(Figure 1)*	Full Range	DS55325			500	μA
				DS75325			200	μA
			T_A = 25°C	DS55325		3	150	μA
				DS75325		3	200	μA
V_{OH}	High Level Sink Output Voltage	V_{CC1} = 4.5V, V_{CC2} = 24V, I_{OUT} = 0V, *(Figure 2)*			19	23		V
V_{SAT}	Saturation Voltage Source Outputs	V_{CC1} = 4.5V, V_{CC2} = 15V, R_L = 24Ω, I_{SOURCE} ≈ −600 mA, *(Figure 3)*, (Notes 4 and 6)	Full Range				0.9	V
			T_A = 25°C	DS55325		0.43	0.7	V
				DS75325		0.43	0.75	V
V_{SAT}	Saturation Voltage Sink Outputs	V_{CC1} = 4.5V, V_{CC2} = 15V, R_L = 24Ω, I_{SINK} ≈ 600 mA, *(Figure 4)*, (Notes 4 and 6)	Full Range				0.9	V
			T_A = 25°C	DS55325		0.43	0.7	V
				DS75325		0.43	0.75	V
I_I	Input Current at Maximum Input Voltage	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 5.5V, *(Figure 5)*	Address Inputs				1	mA
			Strobe Inputs				2	mA
I_{IH}	High Level Input Current	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 2.4V, *(Figure 5)*	Address Inputs			3	40	μA
			Strobe Inputs			6	80	μA
I_{IL}	Low Level Input Current	V_{CC1} = 5.5V, V_{CC2} = 24V, V_I = 0.4V, *(Figure 5)*	Address Inputs			−1	−1.6	mA
			Strobe Inputs			−2	−3.2	mA
$I_{CC\,OFF}$	Supply Current, All Sources and Sinks "OFF"	V_{CC1} = 5.5V, V_{CC2} = 24V, T_A = 25°C, *(Figure 6)*	V_{CC1}			14	22	mA
			V_{CC2}			7.5	20	mA
I_{CC1}	Supply Current From V_{CC1}, Either Sink "ON"	V_{CC1} = 5.5V, V_{CC2} = 24V, I_{SINK} = 50 mA, T_A = 25°C, *(Figure 7)*				55	70	mA
I_{CC2}	Supply Current From V_{CC2}, Either Source "ON"	V_{CC1} = 5.5V, V_{CC2} = 24V, I_{SOURCE} = −50 mA, T_A = 25°C, *(Figure 8)*				32	50	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55325 and across the 0°C to +70°C range for the DS75325. All typical values are at T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

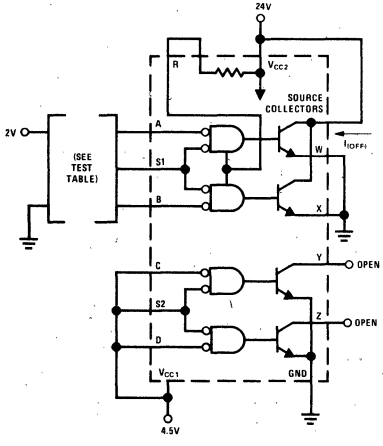
Note 5: Voltage values are with respect to network ground terminal.

Note 6: These parameters must be measured using pulse techniques. t_W = 200μs, duty cycle ≤ 2%.

ac switching characteristics (V_{CC1} = 5V, T_A = 25°C)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, *(Figure 9)*	Source Collectors		25	50	ns
			Sink Outputs		20	45	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, *(Figure 9)*	Source Collectors		25	50	ns
			Sink Outputs		20	45	ns
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 25 pF	Source Outputs, V_{CC2} = 20V, R_L = 1 kΩ, *(Figure 10)*		55		ns
			Sink Outputs, V_{CC2} = 15V, R_L = 24Ω, *(Figure 9)*		7	15	ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 25 pF	Source Outputs, V_{CC2} = 20V, R_L = 1 kΩ, *(Figure 10)*		7		ns
			Sink Outputs, V_{CC2} = 15V, R_L = 24Ω, *(Figure 9)*		9	20	ns
t_S	Storage Time, Sink Outputs	V_{CC2} = 15V, R_L = 24Ω, C_L = 25 pF, *(Figure 9)*			15	30	ns

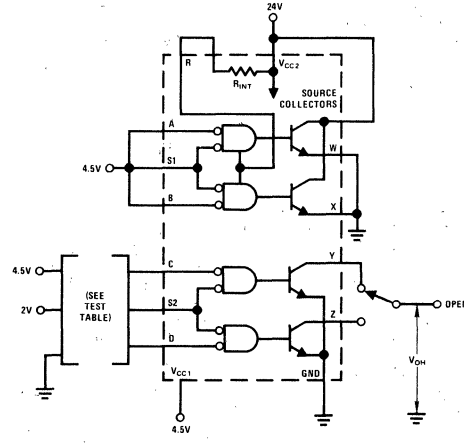
dc test circuits



TEST TABLE

A	B	S1
GND	GND	2V
2V	2V	GND

FIGURE 1. I_{OFF}

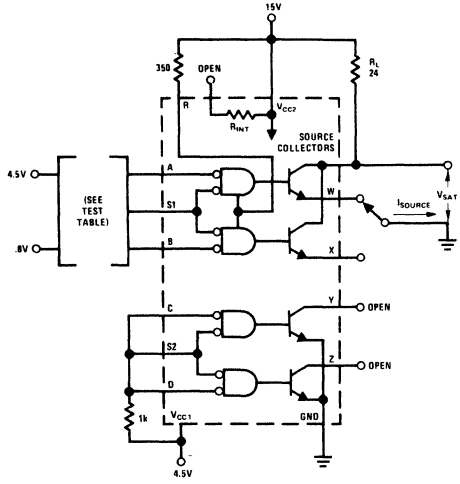


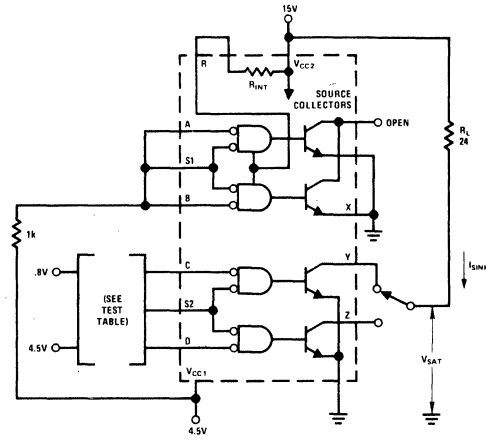
TEST TABLE

C	D	S2	Y	Z
2V	4.5V	GND	V_{OH}	OPEN
GND	4.5V	2V	V_{OH}	OPEN
4.5V	2V	GND	OPEN	V_{OH}
4.5V	GND	2V	OPEN	V_{OH}

FIGURE 2. V_{IH} and V_{OH}

dc test circuits(con't)





Note 1: Figures 3 and 4 parameters must be measured using pulse techniques. t_W = 200μs, duty cycle ≤ 2%.

TEST TABLE

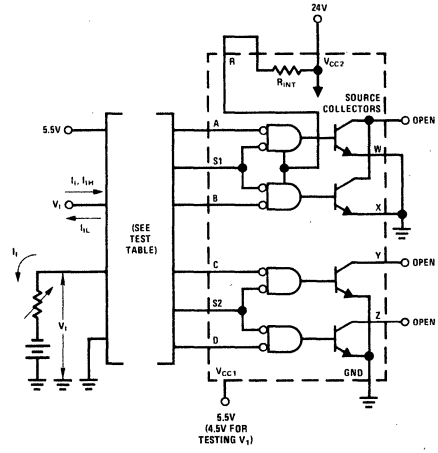
A	B	S1	W	X
0.8V	4.5V	0.8V	GND	OPEN
4.5V	0.8V	0.8V	OPEN	GND

FIGURE 3. V_{IL} and Source V_{SAT}

TEST TABLE

C	D	S2	Y	Z
0.8V	4.5V	0.8V	R_L	OPEN
4.5V	0.8V	0.8V	OPEN	R_L

FIGURE 4. V_{IL} and Sink V_{SAT}



TEST TABLES

I_I, I_{IH}

APPLY V_I = 5.5V MEASURE I_I / APPLY V_I = 2.4V MEASURE I_{IH}	GROUND	APPLY 5.5V
A	S1	B, C, S2, D
S1	A, B	C, S2, D
B	S1	A, C, S2, D
C	S2	A, S1, B, D
S2	C, D	A, S1, B
D	S2	A, S1, B, C

V_I, I_{IL}

APPLY V_I = 0.4V, MEASURE I_{IL} / APPLY I_I = −10 mA, MEASURE V_I	APPLY 5.5V
A	S1, B, C, S2, D
S1	A, B, C, S2, D
B	A, S1, C, S2, D
C	A, S1, B, S2, D
S2	A, S1, B, C, D
D	A, S1, B, C, S2

FIGURE 5. V_I, I_I, I_{IH}, and I_{IL}

dc test circuits(con't)

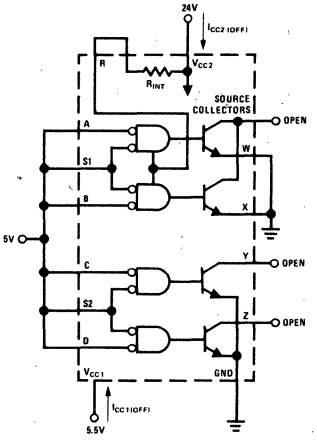
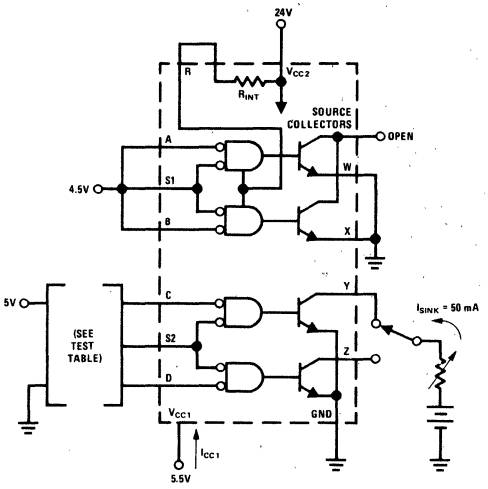


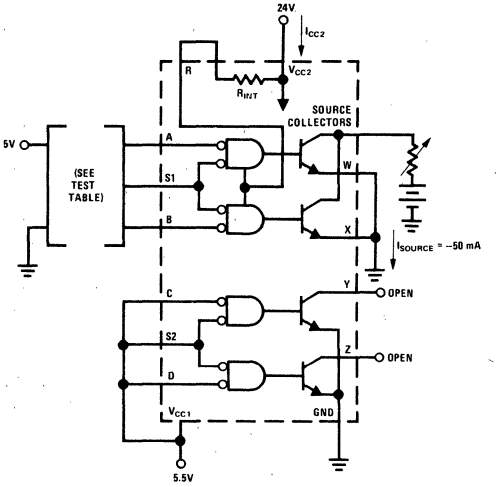
FIGURE 6. $I_{CC1(OFF)}$ and $I_{CC2(OFF)}$



TEST TABLE

C	D	S2	Y	Z
GND	5V	GND	$I_{(SINK)}$	OPEN
5V	GND	GND	OPEN	$I_{(SINK)}$

FIGURE 7. I_{CC1}, Either Sink On

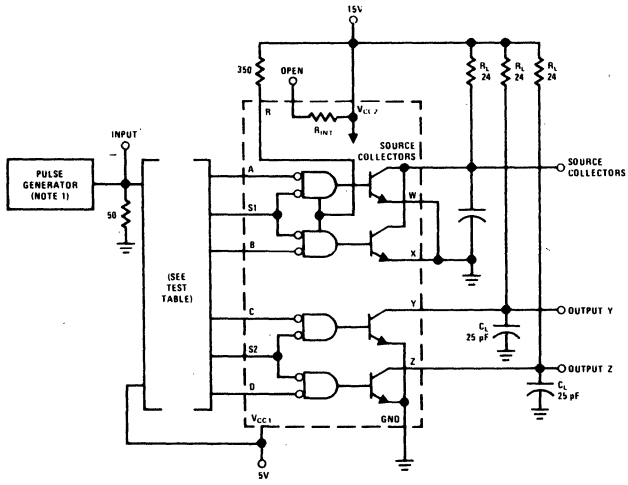


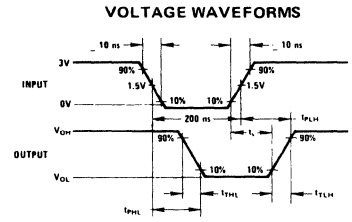
TEST TABLE

A	B	S1
GND	5V	GND
5V	GND	GND

FIGURE 8. I_{CC2}, Either Source On

dc test circuits(con't)





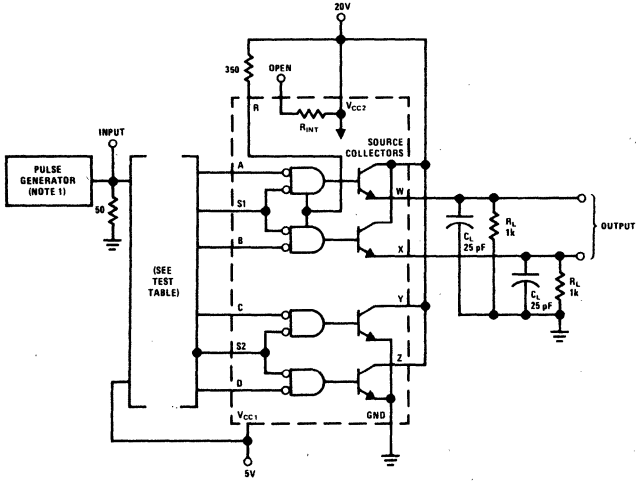
Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, duty cycle ≤ 1%.

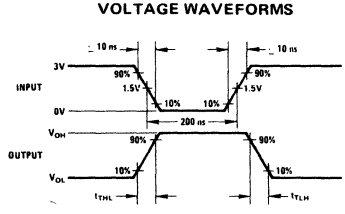
Note 2: C_L includes probe and jig capacitance.

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5V
t_{PLH} and t_{PHL}	Source collectors	A and S1	B, C, D and S2
		B and S1	A, C, D and S2
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, and t_s	Sink output Y	C and S2	A, B, D and S1
	Sink output Z	D and S2	A, B, C and S1

FIGURE 9. Switching Times





Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, duty cycle ≤ 1%.

Note 2: C_L includes probe and jig capacitance.

TEST TABLE

PARAMETER	OUTPUT UNDER TEST	INPUT	CONNECT TO 5V
t_{TLH} and t_{THL}	Source output W	A and S1	B, C, D, and S2
	Source output X	B and S1	A, C, D, and S2

FIGURE 10. Transition Times of Source Outputs

applications

External Resistor Calculation

A typical magnetic-memory word drive requirement is shown in Figure 11. A source-output transistor of one DS75325 delivers load current (I_L). The sink-output transistor of another DS75325 sinks this current.

The value of the external pull-up resistor (R_{ext}) for a particular memory application may be determined using the following equation:

$$R_{ext} = \frac{16\,[V_{CC2(min)} - V_S - 2.2]}{I_L - 1.6\,[V_{CC2(min)} - V_S - 2.9]} \quad (1)$$

where: R_{ext} is in kΩ,

$V_{CC2(min)}$ is the lowest expected value of V_{CC2} in volts, V_S is the source output voltage in volts with respect to ground, I_L is in mA.

The power dissipated in resistor R_{ext} during the load current pulse duration is calculated using Equation 2.

$$P_{Rext} \approx \frac{I_L}{16}\,[V_{CC2(min)} - V_S - 2] \quad (2)$$

where: P_{Rext} is in mW.

After solving for R_{ext}, the magnitude of the source collector current (I_{CS}) is determined from Equation 3.

$$I_{CS} \approx 0.94\, I_L \quad (3)$$

where: I_{CS} is in mA.

As an example, let $V_{CC2(min)}$ = 20V and V_L = 3V while I_L of 500 mA flows. Using Equation 1:

$$R_{ext} = \frac{16\,(20 - 3 - 2.2)}{500 - 1.6\,(20 - 3 - 2.9)} = 0.5\ k\Omega$$

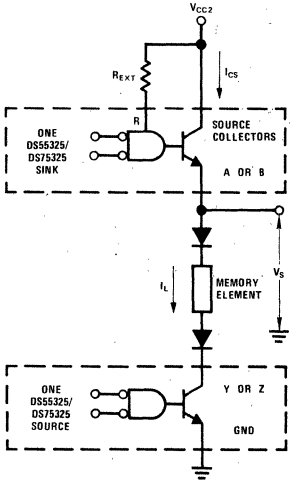
and from Equation 2:

$$P_{Rext} \approx \frac{500}{16}\,[20 - 3 - 2] \approx 470\ mW$$

The amount of the memory system current source (I_{CS}) from Equation 3 is:

$$I_{CS} \approx 0.94\,(500) \approx 470\ mA$$

In this example the regulated source-output transistor base current through the external pull-up resistor (R_{ext}) and the source gate is approximately 30 mA. This current and I_{CS} comprise I_L.



Note 1: For clarity, partial logic diagrams of two DS55325's are shown.

Note 2: Source and sink shown are in different packages.

FIGURE 11. Typical Application Data

DS75361 dual TTL-to-MOS driver

general description

The DS75361 is a monolithic integrated dual TTL-to-MOS driver interface circuit. The device accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103 and MM5270 and MM5280.

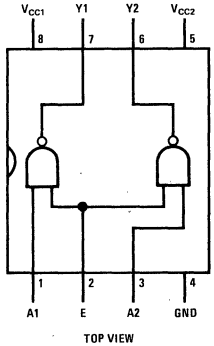
The DS75361 operates from standard TTL 5V supplies and the MOS V_{SS} supply in many applications. The device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V; however, it is designed for use over a much wider range of V_{CC2}.

features

- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- V_{CC2} supply voltage variable over wide range to 24V
- Diode-clamped inputs
- TTL and DTL compatible
- Operates from standard bipolar and MOS supplies
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

connection diagrams

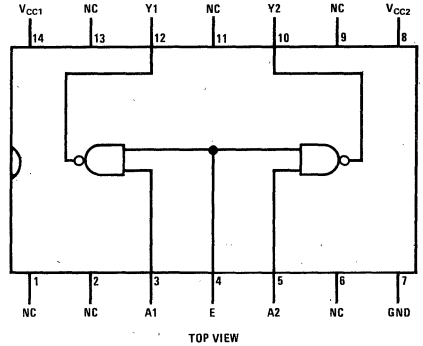
Dual-In-Line Package



TOP VIEW

Order Number DS75361N

Dual-In-Line Package



TOP VIEW

Order Number DS75361J

absolute maximum ratings (Note 1)

Supply Voltage Range of V_{CC1} (Note 1)	−0.5V to 7V
Supply Voltage Range of V_{CC2}	−0.5V to 25V
Input Voltage	5.5V
Inter-Input Voltage (Note 4)	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature 1/16 Inch from Case for 60 Seconds: J Package	300°C
Lead Temperature 1/16 Inch from Case for 10 Seconds: N or P Package	200°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC1})	4.75	5.25	V
Supply Voltage (V_{CC2})	4.75	24	V
Operating Temperature (T_A)	0	+70	°C

dc electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	I_I = −12 mA				−1.5	V
V_{OH}	High-Level Output Voltage	V_{IL} = 0.8V, I_{OH} = −50μA		V_{CC2}−1	V_{CC2}−0.7		V
		V_{IL} = 0.8V, I_{OH} = −10 mA		V_{CC2}−2.3	V_{CC2}−1.8		V
V_{OL}	Low-Level Output Voltage	V_{IH} = 2V, I_{OL} = 10 mA			0.15	0.3	V
		V_{CC2} = 15V to 24V, V_{IH} = 2V, I_{OL} = 40 mA			0.25	0.5	V
V_O	Output Clamp Voltage	V_I = 0V, I_{OH} = 20 mA				V_{CC2}+1.5	V
I_I	Input Current at Maximum Input Voltage	V_I = 5.5V				1	mA
I_{IH}	High-Level Input Current	V_I = 2.4V	A Inputs			40	μA
			E Input			80	μA
I_{IL}	Low-Level Input Current	V_I = 0.4V	A Inputs		−1	−1.6	mA
			E Input		−2	−3.2	mA
$I_{CC1(H)}$	Supply Current from V_{CC1}, Both Outputs High	V_{CC1} = 5.25V, V_{CC2} = 24V, All Inputs at 0V, No Load			2	4	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, Both Outputs High					0.5	mA
$I_{CC1(L)}$	Supply Current from V_{CC1}, Both Outputs Low	V_{CC1} = 5.25V, V_{CC2} = 24V, All Inputs at 5V, No Load			16	24	mA
$I_{CC2(L)}$	Supply Current from V_{CC2}, Both Outputs Low				7	11	mA
$I_{CC2(S)}$	Supply Current from V_{CC2}, Stand-by Condition	V_{CC1} = 0V, V_{CC2} = 24V, All Inputs at 5V, No Load				0.5	mA

switching characteristics (V_{CC1} = 5V, V_{CC2} = 20V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{DLH}	Delay Time, Low-to-High Level Output	C_L = 390 pF, R_D = 10Ω (*Figure 1*)		11	20	ns
t_{DHL}	Delay Time, High-to-Low Level Output			10	18	ns
t_{TLH}	Transition Time, Low-to-High Level Output			25	40	ns
t_{THL}	Transition Time, High-to-Low Level Output			21	35	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		10	36	55	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	31	47	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

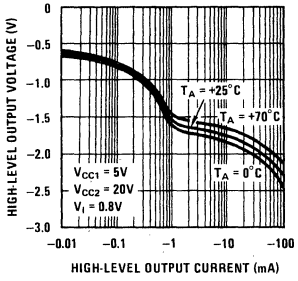
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75361. All typical values are for T_A = 25°C and V_{CC1} = 5V and V_{CC2} = 20V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

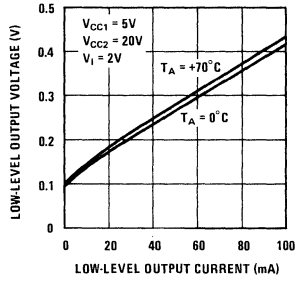
Note 4: This rating applies between the A input of either driver and the common E input.

typical performance characteristics

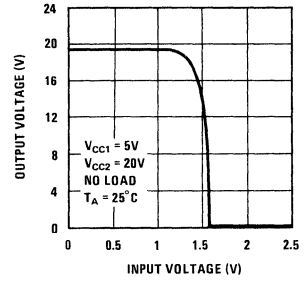
High-Level Output Voltage vs Output Current



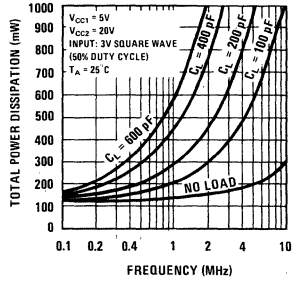
Low-Level Output Voltage vs Output Current



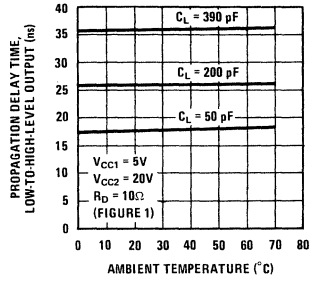
Voltage Transfer Characteristics



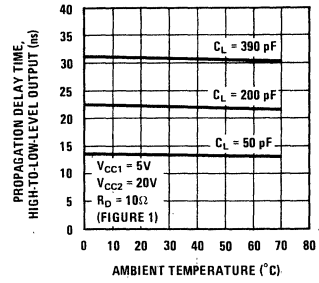
Total Dissipation (Both Drivers) vs Frequency



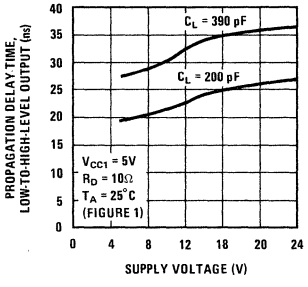
Propagation Delay Time, Low-to-High Level Output vs Ambient Temperature



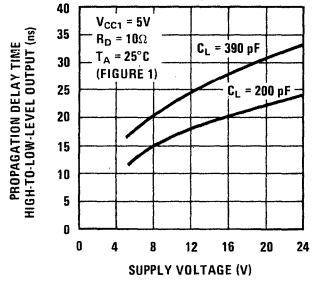
Propagation Delay Time, High-to-Low Level Output vs Ambient Temperature



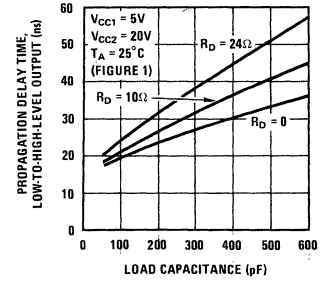
Propagation Delay Time, Low-to-High Level Output vs V_{CC2} Supply Voltage



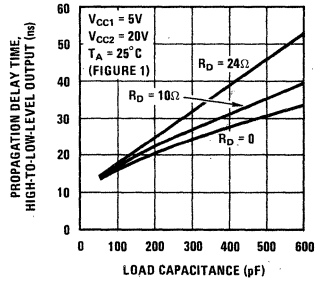
Propagation Delay Time, High-to-Low Level Output vs V_{CC2} Supply Voltage



Propagation Delay Time, Low-to-High Level Output vs Load Capacitance

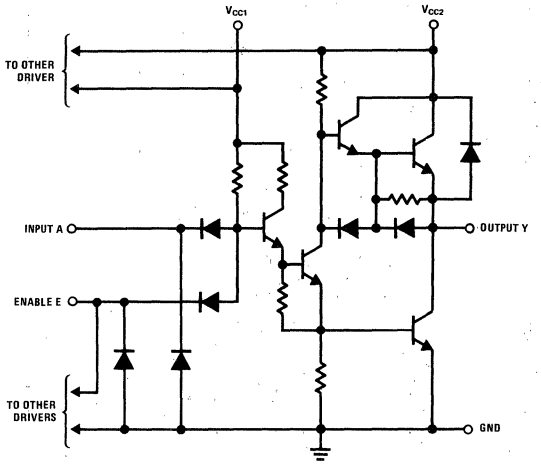


Propagation Delay Time, High-to-Low Level Output vs Load Capacitance

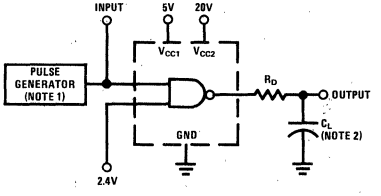


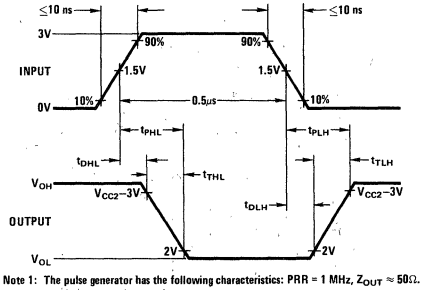
4

schematic diagram (1/2 shown)



ac test circuit and switching time waveforms





Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

FIGURE 1. Switching Times, Each Driver

typical applications

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor to use depends on the specific load characteristics and switching speed. A typical value would be between 10Ω and 30Ω *(Figure 3)*.

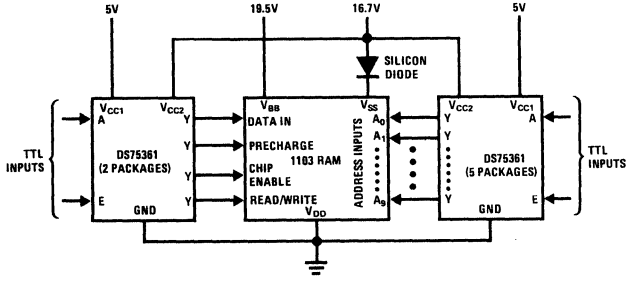


FIGURE 2. Interconnection of DS75361 Devices with 1103 RAM

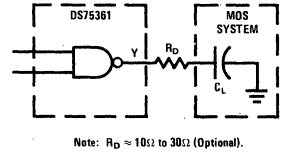


FIGURE 3. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot in Certain DS75361 Applications

thermal information

POWER DISSIPATION PRECAUTIONS

Significant power may be dissipated in the DS75361 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. The total dissipation curve shows the power dissipated in a typical DS75361 as a function of load capacitance and frequency. Average power dissipated by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{p_L t_L + p_H t_H}{T}$$

$$P_{C(AV)} \approx C V_C^2 f$$

$$P_{S(AV)} = \frac{p_{LH} t_{LH} + p_{HL} t_{HL}}{T}$$

where the times are as defined in *Figure 4*.

p_L, p_H, p_{LH}, and p_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The DS75361 is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H \gg t_{LH} + t_{HL}$ so that P_S can be neglected. The total dissipation curve for no load demonstrates this point. The power dissipation contributions from both channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume both channels are operating identically with C = 200 pF, f = 2 MHz, V_{CC1} = 5V, V_{CC2} = 20V, and duty cycle = 60% outputs high (t_H/T = 0.6). Also, assume V_{OH} = 19.3V, V_{OL} = 0.1V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is high.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5V)\left(\frac{2\text{ mA}}{2}\right) + (20V)\left(\frac{0\text{ mA}}{2}\right)\right](0.6) + \left[(5V)\left(\frac{16\text{ mA}}{2}\right) + (20V)\left(\frac{7\text{ mA}}{2}\right)\right](0.4)$$

$$P_{DC(AV)} = 47 \text{ mW per channel}$$

$$P_{C(AV)} \approx (200\text{ pF})\,(19.2V)^2\,(2\text{ MHz})$$

$$P_{C(AV)} \approx 148 \text{ mW per channel.}$$

For the total device dissipation of the two channels:

$$P_{T(AV)} \approx 2\,(47 + 148)$$

$$P_{T(AV)} \approx 390 \text{ mW typical for total package.}$$

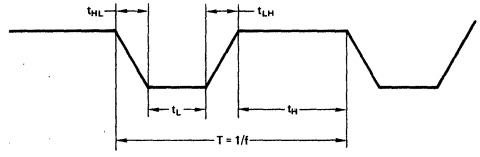


FIGURE 4. Output Voltage Waveform

NATIONAL

Memory/Clock Drivers

DS75362 dual TTL-to-MOS driver

general description

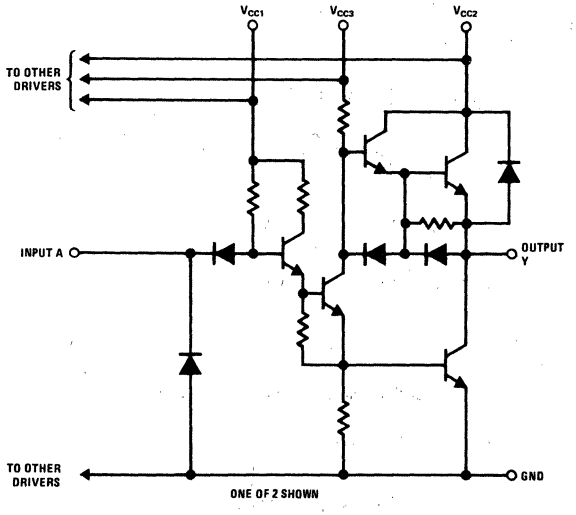
The DS75362 is a dual monolithic integrated TTL-to-MOS driver and interface circuit that accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103.

The DS75362 operates from the TTL 5V supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V, and with nominal V_{CC3} supply voltage from 3V to 4V higher than V_{CC2}. However, it is designed so as to be usable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

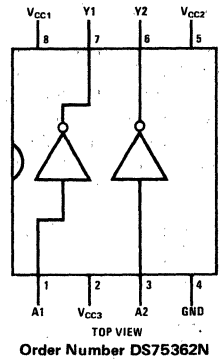
features

- Dual positive-logic NAND TTL-to-MOS driver
- Versatile interface circuit for use between TTL and high-current, high-voltage systems
- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- V_{CC2} supply voltage variable over wide range to 24V maximum
- V_{CC3} supply voltage pin available
- V_{CC3} pin can be connected to V_{CC2} pin in some applications
- TTL and DTL compatible diode-clamped inputs
- Operates from standard bipolar and MOS supply voltages
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

schematic and connection diagrams

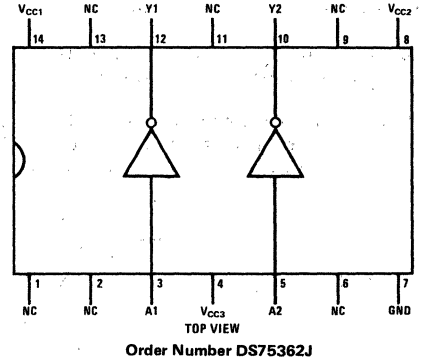


Dual-In-Line Package



Order Number DS75362N

Dual-In-Line Package



Order Number DS75362J

absolute maximum ratings (Note 1)

Supply Voltage Range of V_{CC1}	−0.5V to 7V
Supply Voltage Range of V_{CC2}	−0.5V to 25V
Supply Voltage Range of V_{CC3}	−0.5V to 30V
Input Voltage	5.5V
Inter-Input Voltage (Note 4)	5.5V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC1})	4.75	5.25	V
Supply Voltage (V_{CC2})	4.75	24	V
Supply Voltage (V_{CC3})	V_{CC2}	28	V
Voltage Difference Between Supply Voltages: $V_{CC3}-V_{CC2}$	0	10	V
Operating Ambient Temperature Range (T_A)	0	70	°C

electrical characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	High-Level Input Voltage		2			V
V_{IL}	Low-Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	$I_I = -12$ mA			−1.5	V
V_{OH}	High-Level Output Voltage	$V_{CC3} = V_{CC2}+3V$, $V_{IL} = 0.8V$, $I_{OH} = -100\mu A$	$V_{CC2}-0.3$	$V_{CC2}-0.1$		V
		$V_{CC3} = V_{CC2}+3V$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA	$V_{CC2}-1.2$	$V_{CC2}-0.9$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -50\mu A$	$V_{CC2}-1$	$V_{CC2}-0.7$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA	$V_{CC2}-2.3$	$V_{CC2}-1.8$		V
V_{OL}	Low-Level Output Voltage	$V_{IH} = 2V$, $I_{OL} = 10$ mA		0.15	0.3	V
		$V_{CC3} = 15V$ to 28V, $V_{IH} = 2V$, $I_{OL} = 40$ mA		0.25	0.5	V
V_O	Output Clamp Voltage	$V_I = 0V$, $I_{OH} = 20$ mA			$V_{CC2}+1.5$	V
I_I	Input Current at Maximum Input Voltage	$V_I = 5.5V$			1	mA
I_{IH}	High-Level Input Current	$V_I = 2.4V$			40	μA
I_{IL}	Low-Level Input Current	$V_I = 0.4V$		−1	−1.6	mA
$I_{CC1(H)}$	Supply Current from V_{CC1}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$, $V_{CC3} = 28V$, All Inputs at 0V, No Load		2	4	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High			−1.1	+0.25	mA
				−1.1	−1.6	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High			1.1	1.8	mA
$I_{CC1(L)}$	Supply Current from V_{CC1}, All Outputs Low	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$, $V_{CC3} = 28V$, All Inputs at 5V, No Load		15	23.5	mA
$I_{CC2(L)}$	Supply Current from V_{CC2}, All Outputs Low				1.5	mA
$I_{CC3(L)}$	Supply Current from V_{CC3}, All Outputs Low			8	12.5	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$, $V_{CC3} = 24V$, All Inputs at 0V, No Load			0.25	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High				0.5	mA
$I_{CC2(S)}$	Supply Current from V_{CC2}, Stand-by Condition	$V_{CC1} = 0V$, $V_{CC2} = 24V$, $V_{CC3} = 24V$, All Inputs at 5V, No Load			0.25	mA
$I_{CC3(S)}$	Supply Current from V_{CC3}, Stand-by Condition				0.5	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75362. All typical values are for $T_A = 25°C$ and $V_{CC1} = 5V$ and $V_{CC2} = 20V$ and $V_{CC3} = 24V$.

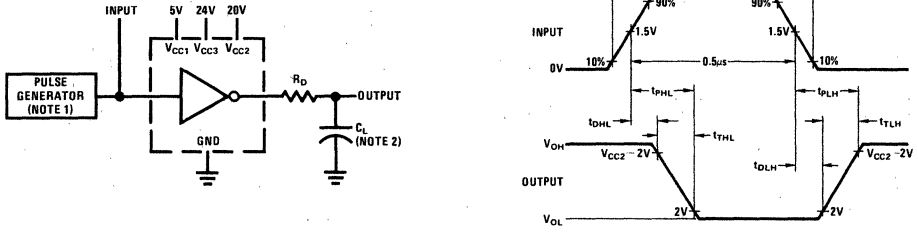
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: This rating applies between any two inputs of any one of the gates.

switching characteristics (V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V, T_A = 25°C)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{DLH}	Delay Time, Low-to-High Level Output	C_L = 200 pF, R_D = 24Ω, (*Figure 1*)		11	20	ns
t_{DHL}	Delay Time, High-to-Low Level Output			10	18	ns
t_{TLH}	Transition Time, Low-to-High Level Output			20	33	ns
t_{THL}	Transition Time, High-to-Low Level Output			20	33	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		10	31	48	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	30	46	ns

ac test circuit and switching time waveforms

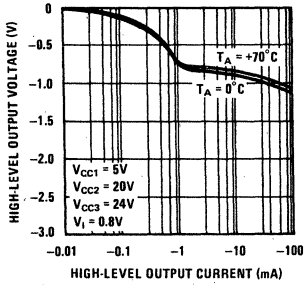


Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

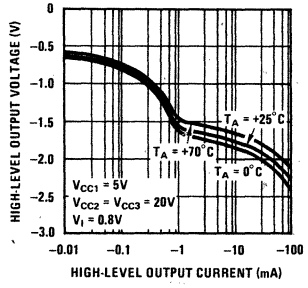
FIGURE 1. Switching Times, Each Driver

typical performance characteristics

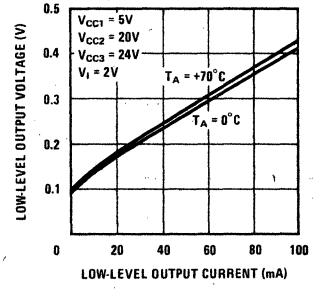
High-Level Output Voltage vs Output Current



High-Level Output Voltage vs Output Current

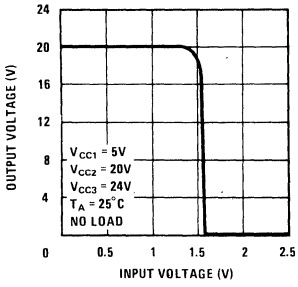


Low-Level Output Voltage Output Current

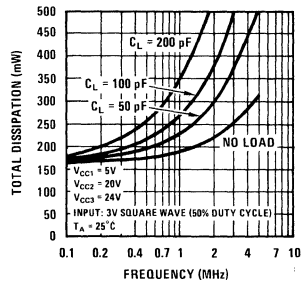


typical performance characteristics (con't)

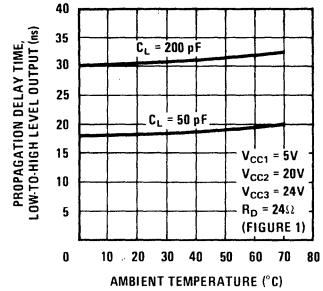
Voltage Transfer Characteristics



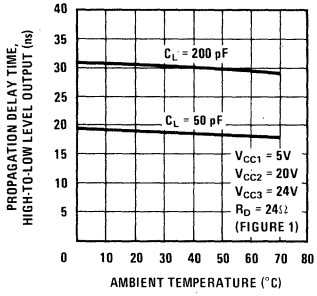
Total Dissipation (Two Drivers) vs Frequency



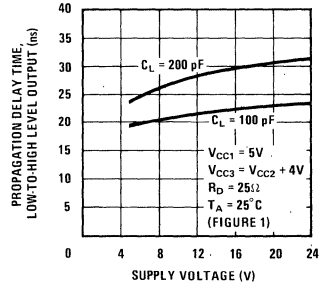
Propagation Delay Time, Low-to-High Level Output vs Ambient Temperature



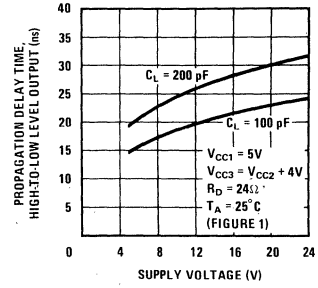
Propagation Delay Time, High-to-Low Level Output vs Ambient Temperature



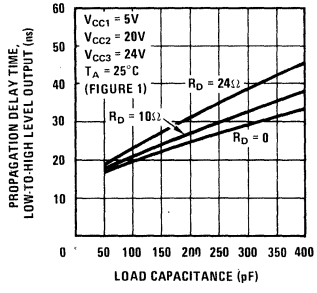
Propagation Delay Time, Low-to-High Level Output vs V_{CC2} Supply Voltage



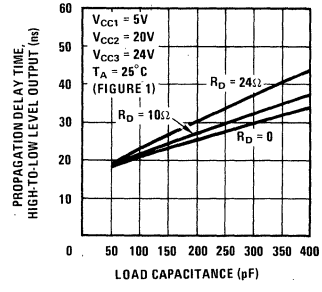
Propagation Delay Time, High-to-Low Level Output vs V_{CC2} Supply Voltage



Propagation Delay Time, Low-to-High Level Output vs Load Capacitance



Propagation Delay Time, High-to-Low Level Output vs Load Capacitance



typical applications

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typical value would be between 10Ω and 30Ω *(Figure 2)*.

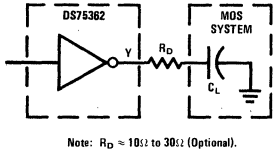


FIGURE 2. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot In Certain DS75362 Applications.

thermal information

POWER DISSIPATION PRECAUTIONS

Significant power may be dissipated in the DS75362 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. The total dissipation curve shows the power dissipated in a typical DS75362 as a function of load capacitance and frequency. Average power dissipation by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{p_L t_L + p_H t_H}{T}$$

$$P_{C(AV)} \approx C\, V_C^2\, f$$

$$P_{S(AV)} = \frac{p_{LH} t_{LH} + p_{HL} t_{HL}}{T}$$

where the times are as defined in *Figure 3*.

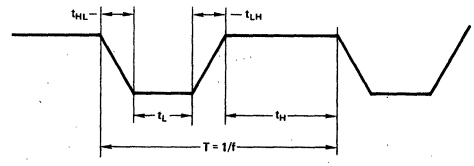


FIGURE 3. Output Voltage Waveform

p_L, p_H, p_{LH}, and p_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The DS75362 is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H \gg t_{LH} + t_{HL}$ so that P_S can be neglected. The total dissipation curve for no load demonstrates this point. The power dissipation contributions from two channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume two channels are operating identically with C = 100 pF, f = 2 MHz, V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V and duty cycle = 60% outputs high (t_H/T = 0.6). Also, assume V_{OH} = 20V, V_{OL} = 0.1V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is low.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5V)\left(\frac{4\text{ mA}}{4}\right) + (20V)\left(\frac{-2.2\text{ mA}}{4}\right) + (24V)\left(\frac{2.2\text{ mA}}{4}\right)\right](0.6) + \left[(5V)\left(\frac{31\text{ mA}}{4}\right) + (20V)\left(\frac{0\text{ mA}}{4}\right) + (24V)\left(\frac{16\text{ mA}}{4}\right)\right](0.4)$$

$P_{DC(AV)}$ = 58 mW per channel

$P_{C(AV)} \approx (100\text{ pF})\,(19.9V)^2\,(2\text{ MHz})$

$P_{C(AV)} \approx 79$ mW per channel.

For the total device dissipation of the two channels

$P_{T(AV)} \approx 2\,(58 + 79)$

$P_{T(AV)} \approx 274$ mW typical for total package.

NATIONAL

DS75364 dual MOS clock driver

general description

The DS75364 is a dual MOS driver and interface circuit that operates with either current source or voltage source input signals. The device accepts signals from TTL levels or other logic systems and provides high current and high voltage output levels suitable for driving MOS circuits. It may be used to drive address, control and/or timing inputs for several types of MOS RAMs and MOS shift registers.

The DS75364 operates from standard MOS and bipolar supplies, and has been optimized for operation with V_{CC1} supply voltage from 12–20V positive with respect to V_{EE}, and with nominal V_{CC2} supply voltage from 3–4V more positive than V_{CC1}. However, it is designed so as to be useable over a much wider range of V_{CC1} and V_{CC2}. In some applications the V_{CC2} power supply can be eliminated by connecting the V_{CC2} pin to the V_{CC1} pin.

Inputs of the DS75364 are referenced to the V_{EE} terminal and contain a series current limiting resistor. The device will operate with either positive input current signals or input voltage signals which are positive with respect to V_{EE}. In many applications the V_{EE} terminal is connected to the MOS V_{DD} supply of −12V to −15V with the inputs to be driven from TTL levels or other positive voltage levels. The required negative level shifting may be done with an external PNP transistor current source or by use of capacitive coupling and appropriate input voltage pulse characteristics.

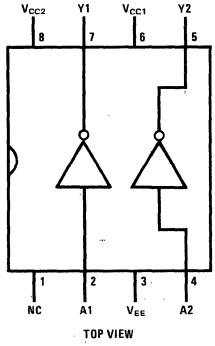
The DS75364 is characterized for operation over the 0°C to +70°C temperature range.

features

- Versatile interface circuit for use between TTL levels and level shifted high current, high voltage systems
- Inputs may be level shifted by use of a current source or capacitive coupling or driven directly by a voltage source
- Capable of driving high capacitance loads
- Compatible with many popular MOS RAMs and MOS shift registers
- V_{CC1} supply voltage variable over wide range to 22V maximum with respect to V_{EE}
- V_{CC2} pull-up supply voltage pin available
- Operates from standard bipolar and/or MOS supply voltages
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

connection diagrams

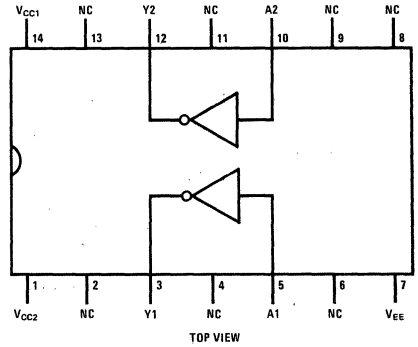
Dual-In-Line Package



TOP VIEW

Order Number DS75364N

Dual-In-Line Package



TOP VIEW

Order Number DS75364J

absolute maximum ratings (Note 1)

Supply Voltage Range of V_{CC1}	−0.5V to 22V
Supply Voltage Range of V_{CC2}	−0.5V to 30V
Input Voltage	15V
Most Positive Voltage at Any Input with Respect to V_{CC2}	0.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNIT
Supply Voltage			
V_{CC1}	4.75	22	V
V_{CC2}	V_{CC1}	28	V
Voltage Difference Between Supply Voltages	0	10	V
Input Voltage		V_{CC2}	
Temperature (T_A)	0	70	°C

electrical characteristics (Notes 2, 3, 4 and 5)

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	Voltage Mode Input Logic Levels			5		10	V
V_{IL}	Low Level Input Voltage	Voltage Mode Input Logic Levels					1	V
I_{IH}	High Level Input Current	Current Mode Input Logic Levels			8		15	mA
I_{IL}	Low Level Input Current	Current Mode Input Logic Levels					0.7	mA
V_{OH}	High Level Output Voltage	$V_{CC2} = V_{CC1} + 3V$, (Note 4)	$I_{OH} = -100\mu A$	$V_{IL} = 1V$	$V_{CC2}-0.3$	$V_{CC2}-0.1$		V
				$I_{IL} = 0.7$ mA	$V_{CC2}-0.3$	$V_{CC2}-0.1$		V
			$I_{OH} = -10$ mA	$V_{IL} = 1V$	$V_{CC2}-1.2$	$V_{CC2}-0.9$		V
				$I_{IL} = 0.7$ mA	$V_{CC2}-1.2$	$V_{CC2}-0.9$		V
		$V_{CC2} = V_{CC1}$, (Note 4)	$I_{OH} = -50\mu A$	$V_{IL} = 1V$	$V_{CC2}-1$	$V_{CC2}-0.7$		V
				$I_{IL} = 0.7$ mA	$V_{CC2}-1$	$V_{CC2}-0.7$		V
			$I_{OH} = -10$ mA	$V_{IL} = 1V$	$V_{CC2}-2.3$	$V_{CC2}-1.8$		V
				$I_{IL} = 0.7$ mA	$V_{CC2}-2.3$	$V_{CC2}-1.8$		V
V_{OL}	Low Level Output Voltage	$I_{OL} = 10$ mA	$V_{IH} = 5V$			0.15	0.3	V
			$I_{IH} = 8$ mA			0.15	0.3	V
		$V_{CC2} = 15$ to 28V, $I_{OL} = 40$ mA	$V_{IH} = 5V$			0.25	0.5	V
			$I_{IH} = 8$ mA			0.25	0.5	V
V_O	Output Clamp Voltage	$V_I = 0V$, $I_{OH} = 20$ mA					$V_{CC1}+1.5$	V
I_I	Input Current at Maximum Input Voltage	$V_{CC2} = 10V$ to 28V, $V_I = 10V$				17	26	mA
V_I	Input Voltage at Maximum Input Current	$V_{CC2} = 13.5V$ to 28V, $I_I = 15$ mA				9	13.5	V
I_{IH}	High Level Input Current	$V_I = 5V$				7	11	mA
V_{IH}	High Level Input Voltage	$I_I = 8$ mA				5.5	8	V
I_{IL}	Low Level Input Current	$V_I = 1V$				1.1	1.6	mA
V_{IL}	Low Level Input Voltage	$I_I = 0.7$ mA				0.7	1	V
$I_{CC1(H)}$	Supply Current From V_{CC1}, Both Outputs High	$V_{CC1} = 22V$, $V_{CC2} = 26V$, Both Inputs at 0V, No Load				−1.1	−1.6	mA
							0.25	mA
$I_{CC2(H)}$	Supply Current From V_{CC2}, Both Outputs High	$V_{CC1} = 22V$, $V_{CC2} = 26V$, Both Inputs at 0V, No Load				1.1	2	mA
$I_{CC1(L)}$	Supply Current From V_{CC1}, Both Outputs Low	$V_{CC1} = 22V$, $V_{CC2} = 28V$, Both Inputs at 7V, No Load				0.5	1	mA
$I_{CC2(L)}$	Supply Current From V_{CC2}, Both Outputs Low	$V_{CC1} = 22V$, $V_{CC2} = 28V$, Both Inputs at 7V, No Load				8	14	mA
$I_{CC1(H)}$	Supply Current From V_{CC1}, Both Outputs High	$V_{CC1} = 22V$, $V_{CC2} = 22V$, Both Inputs at 0V, No Load					0.25	mA
$I_{CC2(H)}$	Supply Current From V_{CC2}, Both Outputs High	$V_{CC1} = 22V$, $V_{CC2} = 22V$, Both Inputs at 0V, No Load					0.5	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75364. All typical values are for $T_A = 25°C$, $V_{CC1} = 20V$, $V_{CC2} = 24V$ and $V_{EE} = 0V$.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

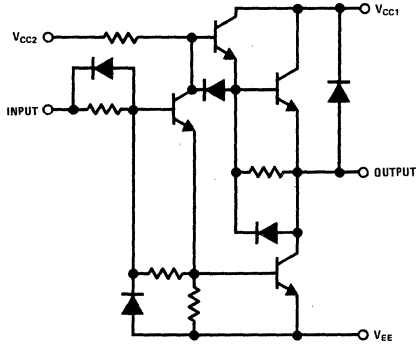
Note 4: Many of these parameters are specified independently for either voltage source or current source external forcing functions at the inputs. Use the appropriate set of specifications for each application.

Note 5: All parameters are specified with $V_{EE} = 0V$ and for input voltage no more positive than V_{CC2}.

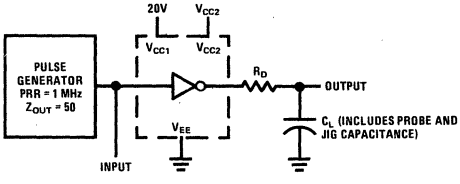
switching characteristics V_{CC1} = 20V, V_{EE} = 0V, T_A = 25°C

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{DLH}	Delay Time, Low-to-High Level Output	C_L = 390 pF, R_D = 10Ω, *(Figure 1)*	V_{CC2} = 24V		13		ns
			V_{CC2} = 20V		14		ns
t_{DHL}	Delay Time, High-to-Low Level Output	C_L = 390 pF, R_D = 10Ω, *(Figure 1)*	V_{CC2} = 24V		9		ns
			V_{CC2} = 20V		10		ns
t_{TLH}	Transition Time, Low-to-High Level Output	C_L = 390 pF, R_D = 10Ω, *(Figure 1)*	V_{CC2} = 24V		21		ns
			V_{CC2} = 20V		21		ns
t_{THL}	Transition Time, High-to-Low Level Output	C_L = 390 pF, R_D = 10Ω, *(Figure 1)*	V_{CC2} = 24V		19		ns
			V_{CC2} = 20V		18		ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_L = 390 pF, R_D = 10Ω, *(Figure 1)*	V_{CC2} = 24V		34		ns
			V_{CC2} = 20V		35		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 390 pF, R_D = 10Ω, *(Figure 1)*	V_{CC2} = 24V		28		ns
			V_{CC2} = 20V		28		ns

schematic diagram (1/2 shown)



ac test circuit and switching time waveforms



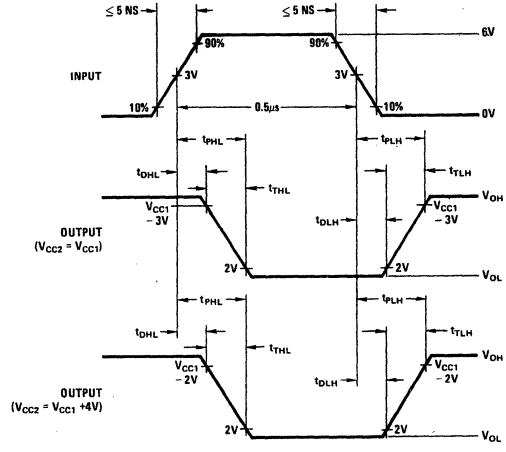


FIGURE 1. Switching Times, Each Driver

typical applications

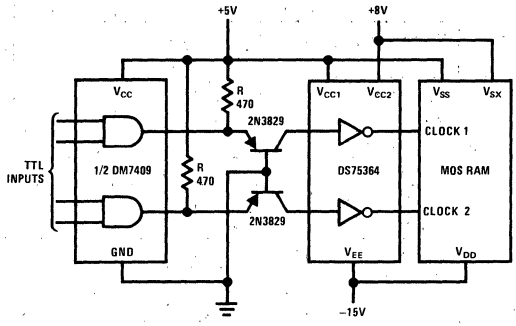


FIGURE 2. MOS RAM Clock Driver System with PNP Transistor Current Source used to Level-Shift to Inputs of DS75364

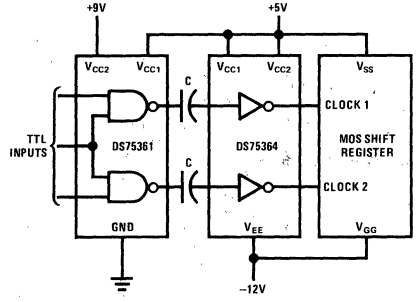


FIGURE 3. MOS Shift Register Clock Driver System with Capacitive Coupling used to Level-Shift to Inputs of DS75364

application hints

Applications of the DS75364 used as an interface device in systems converting TTL signals to negative polarity MOS clock signals are shown in *Figures 2 and 3*. In both applications the DS75364 V_{EE} pin is connected to a negative MOS supply voltage. The V_{CC2} supply pin may be connected to the V_{CC1} pin as shown in *Figure 3* or connected to a separate voltage more-positive than V_{CC1} as shown in *Figure 2*. The DS75364 may be used over a wide range of V_{CC1} and V_{CC2} supply voltages which are positive with respect to V_{EE}. However, for proper operation the voltage at the inputs of the DS75364 should not be more positive than the voltage at V_{CC2}.

Both applications shown require negative level shifting from positive voltage levels to the inputs of the DS75364 which are referenced to the V_{EE} terminal. A PNP transistor current source is used to level shift in *Figure 2*. Resistor R sets the current and an open-collector TTL gate is used to switch the PNP transistor. *Figure 3* shows capacitive coupling being used to level shift with the DS75361 TTL-to-MOS driver used as a low impedance voltage source driver. The value of coupling capacitor C depends on the frequency and characteristics of the signal applied to the capacitor.

The fast switching of the DS75364 may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typical value would be between 10 and 30 ohms (*Figure 4*).

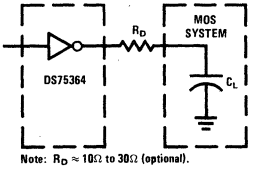


FIGURE 4. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot in Certain DS75364 Applications

NATIONAL

Memory/Clock Drivers

DS75365 quad TTL-to-MOS driver

general description

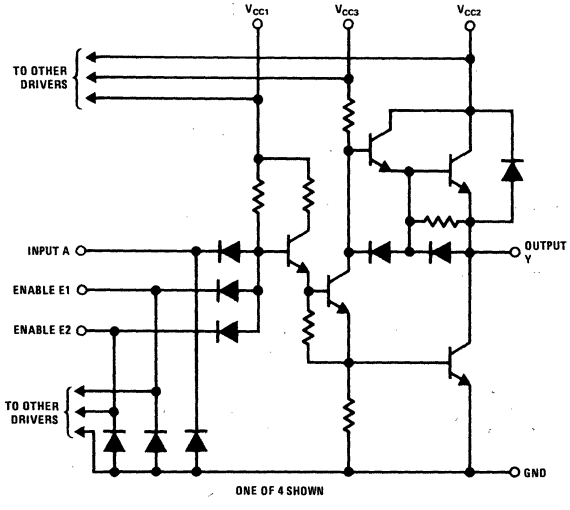
The DS75365 is a quad monolithic integrated TTL-to-MOS driver and interface circuit that accepts standard TTL and DTL input signals and provides high-current and high-voltage output levels suitable for driving MOS circuits. It is used to drive address, control, and timing inputs for several types of MOS RAMs including the 1103.

The DS75365 operates from the TTL 5V supply and the MOS V_{SS} and V_{BB} supplies in many applications. This device has been optimized for operation with V_{CC2} supply voltage from 16V to 20V, and with nominal V_{CC3} supply voltage from 3V to 4V higher than V_{CC2}. However, it is designed so as to be usable over a much wider range of V_{CC2} and V_{CC3}. In some applications the V_{CC3} power supply can be eliminated by connecting the V_{CC3} pin to the V_{CC2} pin.

features

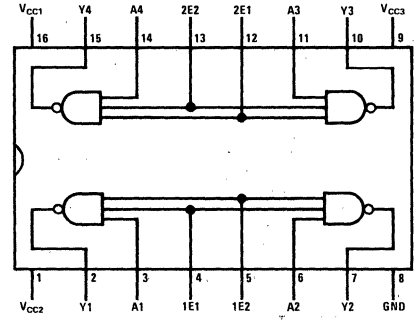
- Quad positive-logic NAND TTL-to-MOS driver
- Versatile interface circuit for use between TTL and high-current, high-voltage systems
- Capable of driving high-capacitance loads
- Compatible with many popular MOS RAMs
- Interchangeable with Intel 3207
- V_{CC2} supply voltage variable over wide range to 24V maximum
- V_{CC3} supply voltage pin available
- V_{CC3} pin can be connected to V_{CC2} pin in some applications
- TTL and DTL compatible diode-clamped inputs
- Operates from standard bipolar and MOS supply voltages
- Two common enable inputs per gate-pair
- High-speed switching
- Transient overdrive minimizes power dissipation
- Low standby power dissipation

schematic and connection diagrams



ONE OF 4 SHOWN

Dual-In-Line Package



TOP VIEW

Positive Logic: $Y = \overline{A \cdot E1 \cdot E2}$

Order Number DS75365J or DS75365N

absolute maximum ratings (Note 1)

Supply Voltage Range of V_{CC1}	−0.5V to 7V
Supply Voltage Range of V_{CC2}	−0.5V to 25V
Supply Voltage Range of V_{CC3}	−0.5V to 30V
Input Voltage	5.5V
Inter-Input Voltage (Note 4)	5.5V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC1})	4.75	5.25	V
Supply Voltage (V_{CC2})	4.75	24	V
Supply Voltage (V_{CC3})	V_{CC2}	28	V
Voltage Difference Between Supply Voltages: $V_{CC3}-V_{CC2}$	0	10	V
Operating Ambient Temperature Range (T_A)	0	70	°C

electrical characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_I	Input Clamp Voltage	$I_I = -12$ mA				−1.5	V
V_{OH}	High-Level Output Voltage	$V_{CC3} = V_{CC2}+3V$, $V_{IL} = 0.8V$, $I_{OH} = -100\mu A$		$V_{CC2}-0.3$	$V_{CC2}-0.1$		V
		$V_{CC3} = V_{CC2}+3V$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA		$V_{CC2}-1.2$	$V_{CC2}-0.9$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -50\mu A$		$V_{CC2}-1$	$V_{CC2}-0.7$		V
		$V_{CC3} = V_{CC2}$, $V_{IL} = 0.8V$, $I_{OH} = -10$ mA		$V_{CC2}-2.3$	$V_{CC2}-1.8$		V
V_{OL}	Low-Level Output Voltage	$V_{IH} = 2V$, $I_{OL} = 10$ mA			0.15	0.3	V
		$V_{CC3} = 15V$ to 28V, $V_{IH} = 2V$, $I_{OL} = 40$ mA			0.25	0.5	V
V_O	Output Clamp Voltage	$V_I = 0V$, $I_{OH} = 20$ mA				$V_{CC2}+1.5$	V
I_I	Input Current at Maximum Input Voltage	$V_I = 5.5V$				1	mA
I_{IH}	High-Level Input Current	$V_I = 2.4V$	A Inputs			40	μA
			E1 and E2 Inputs			80	μA
I_{IL}	Low-Level Input Current	$V_I = 0.4V$	A Inputs		−1	−1.6	mA
			E1 and E2 Inputs		−2	−3.2	mA
$I_{CC1(H)}$	Supply Current from V_{CC1}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$, $V_{CC3} = 28V$, All Inputs at 0V, No Load			4	8	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High				−2.2	+0.25	mA
					−2.2	−3.2	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High				2.2	3.5	mA
$I_{CC1(L)}$	Supply Current from V_{CC1}, All Outputs Low	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$, $V_{CC3} = 28V$, All Inputs at 5V, No Load			31	47	mA
$I_{CC2(L)}$	Supply Current from V_{CC2}, All Outputs Low					3	mA
$I_{CC3(L)}$	Supply Current from V_{CC3}, All Outputs Low				16	25	mA
$I_{CC2(H)}$	Supply Current from V_{CC2}, All Outputs High	$V_{CC1} = 5.25V$, $V_{CC2} = 24V$, $V_{CC3} = 24V$, All Inputs at 0V, No Load				0.25	mA
$I_{CC3(H)}$	Supply Current from V_{CC3}, All Outputs High					0.5	mA
$I_{CC2(S)}$	Supply Current from V_{CC2}, Stand-by Condition	$V_{CC1} = 0V$, $V_{CC2} = 24V$, $V_{CC3} = 24V$, All Inputs at 5V, No Load				0.25	mA
$I_{CC3(S)}$	Supply Current from V_{CC3}, Stand-by Condition					0.5	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75365. All typical values are for $T_A = 25°C$ and $V_{CC1} = 5V$ and $V_{CC2} = 20V$ and $V_{CC3} = 24V$.

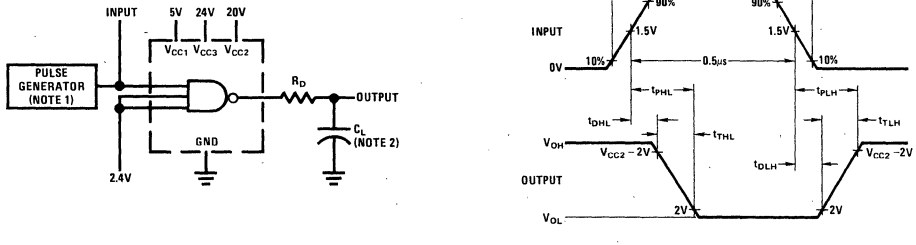
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: This rating applies between any two inputs of any one of the gates.

switching characteristics (V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{DLH}	Delay Time, Low-to-High Level Output	C_L = 200 pF, R_D = 24Ω, (*Figure 1*)		11	20	ns
t_{DHL}	Delay Time, High-to-Low Level Output			10	18	ns
t_{TLH}	Transition Time, Low-to-High Level Output			20	33	ns
t_{THL}	Transition Time, High-to-Low Level Output			20	33	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		10	31	48	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output		10	30	46	ns

ac test circuit and switching time waveforms

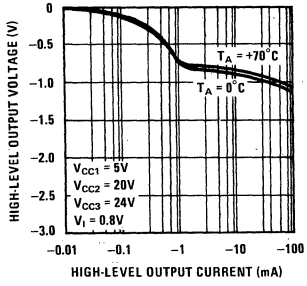


Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{OUT} \approx 50\Omega$.
Note 2: C_L includes probe and jig capacitance.

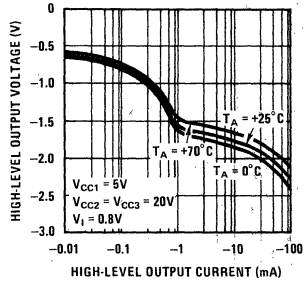
FIGURE 1. Switching Times, Each Driver

typical performance characteristics

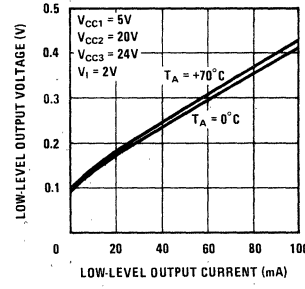
High-Level Output Voltage vs Output Current



High-Level Output Voltage vs Output Current

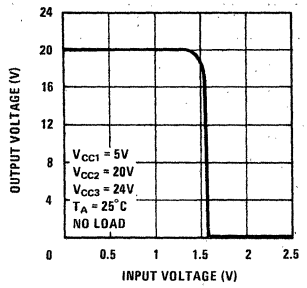


Low-Level Output Voltage Output Current

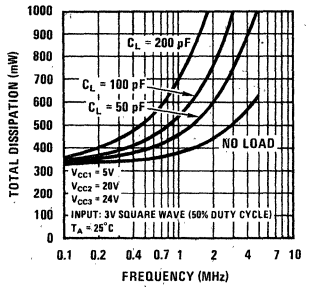


typical performance characteristics (con't)

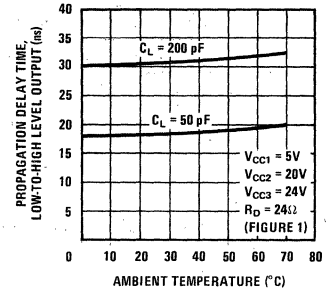
Voltage Transfer Characteristics



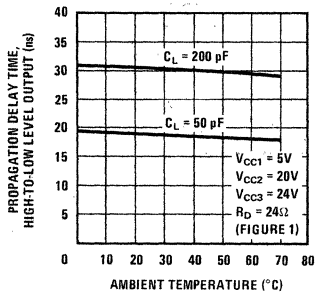
Total Dissipation (All Four Drivers) vs Frequency



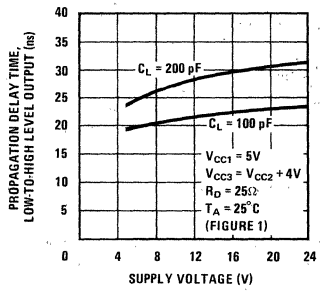
Propagation Delay Time, Low-to-High Level Output vs Ambient Temperature



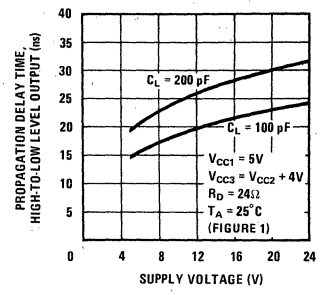
Propagation Delay Time, High-to-Low Level Output vs Ambient Temperature



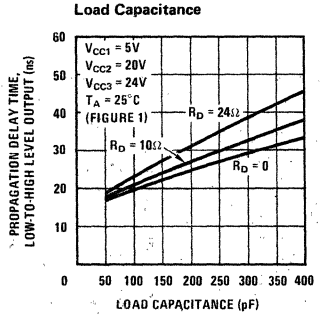
Propagation Delay Time, Low-to-High Level Output vs V_{CC2} Supply Voltage



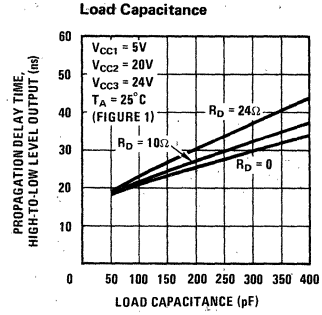
Propagation Delay Time, High-to-Low Level Output vs V_{CC2} Supply Voltage



Propagation Delay Time, Low-to-High Level Output vs Load Capacitance



Propagation Delay Time, High-to-Low Level Output vs Load Capacitance



typical applications

The fast switching speeds of this device may produce undesirable output transient overshoot because of load or wiring inductance. A small series damping resistor may be used to reduce or eliminate this output transient overshoot. The optimum value of the damping resistor depends on the specific load characteristics and switching speed. A typical value would be between 10Ω and 30Ω *(Figure 3)*.

typical applications (con't)

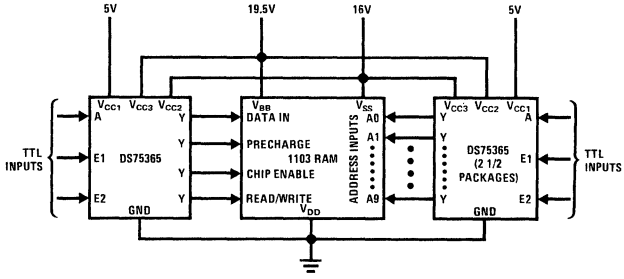


FIGURE 2. Interconnection of DS75365 Devices With 1103-Type Silicon-Gate MOS RAM

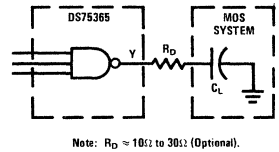


FIGURE 3. Use of Damping Resistor to Reduce or Eliminate Output Transient Overshoot In Certain DS75365 Applications

thermal information

POWER DISSIPATION PRECAUTIONS

Significant power may be dissipated in the DS75365 driver when charging and discharging high-capacitance loads over a wide voltage range at high frequencies. The total dissipation curve shows the power dissipated in a typical DS75365 as a function of load capacitance and frequency. Average power dissipation by this driver can be broken into three components:

$$P_{T(AV)} = P_{DC(AV)} + P_{C(AV)} + P_{S(AV)}$$

where $P_{DC(AV)}$ is the steady-state power dissipation with the output high or low, $P_{C(AV)}$ is the power level during charging or discharging of the load capacitance, and $P_{S(AV)}$ is the power dissipation during switching between the low and high levels. None of these include energy transferred to the load and all are averaged over a full cycle.

The power components per driver channel are:

$$P_{DC(AV)} = \frac{p_L t_L + p_H t_H}{T}$$

$$P_{C(AV)} \approx C V_C^2 f$$

$$P_{S(AV)} = \frac{p_{LH} t_{LH} + p_{HL} t_{HL}}{T}$$

where the times are as defined in *Figure 4.*

p_L, p_H, p_{LH}, and p_{HL} are the respective instantaneous levels of power dissipation and C is load capacitance.

The DS75365 is so designed that P_S is a negligible portion of P_T in most applications. Except at very high frequencies, $t_L + t_H \gg t_{LH} + t_{HL}$ so that P_S can be neglected. The total dissipation curve for no load demonstrates this point. The power dissipation contributions from all four channels are then added together to obtain total device power.

The following example illustrates this power calculation technique. Assume all four channels are operating identically with C = 100 pF, f = 2 MHz, V_{CC1} = 5V, V_{CC2} = 20V, V_{CC3} = 24V and duty cycle = 60% outputs high (t_H/T = 0.6). Also, assume V_{OH} = 20V, V_{OL} = 0.1V, P_S is negligible, and that the current from V_{CC2} is negligible when the output is low.

On a per-channel basis using data sheet values:

$$P_{DC(AV)} = \left[(5V)\left(\frac{4\text{ mA}}{4}\right) + (20V)\left(\frac{-2.2\text{ mA}}{4}\right) + (24V)\left(\frac{2.2\text{ mA}}{4}\right)\right](0.6) + \left[(5V)\left(\frac{31\text{ mA}}{4}\right) + (20V)\left(\frac{0\text{ mA}}{4}\right) + (24V)\left(\frac{16\text{ mA}}{4}\right)\right](0.4)$$

$P_{DC(AV)}$ = 58 mW per channel

$P_{C(AV)} \approx (100\text{ pF})(19.9V)^2(2\text{ MHz})$

$P_{C(AV)} \approx 79$ mW per channel.

For the total device dissipation of the four channels:

$P_{T(AV)} \approx 4(58 + 79)$

$P_{T(AV)} \approx 548$ mW typical for total package.

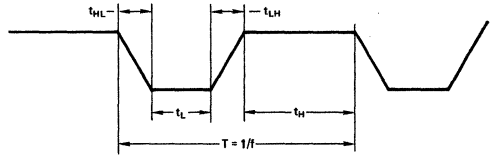


FIGURE 4. Output Voltage Waveform

Sense Amplifiers

DS1605/DS3605, DS1606/DS3606, DS1607/DS3607, DS1608/DS3608 hex MOS sense amplifiers (MOS to TTL converters)

general description

The DS3605 series is a new series of programmable hex MOS sense amplifiers featuring high speed direct MOS sense capability with high impedance states to allow use of a common bus line. The DS1605/DS3605 and the DS1606/DS3606 have TRI-STATE® outputs. The DS1607/DS3607 and DS1608/DS3608 have both TRI-STATE inputs and outputs. High impedance states are controlled by an enable input.

Input current threshold (the level at which the output changes state) is determined by the current at the programming pin. The current threshold is 100μA with the programming pin grounded and 250μA with the pin unconnected. The threshold can be set from 100μA to 300μA by connecting a resistor from the pin to ground, and set above 300μA by connecting a resistor from the pin to the positive supply.

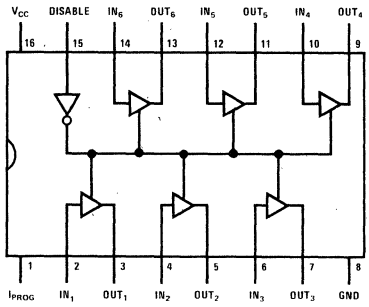
Outputs are high current drivers capable of sinking 50 mA in the low state and sourcing 5 mA in the high state.

features

- Non-inverting inputs (DS1605/DS3605, DS1607/DS3607)
- Inverting inputs (DS1606/DS3606, DS1608/DS3608)
- No external components required (direct MOS sensing)
- Programmable input thresholds
- Current sensing—100μA minimum
- 50 mA drive capability
- TRI-STATE control
- Single 5V supply
- 15 ns typical propagation delay (DS3605)

connection diagram

Dual-In-Line Package



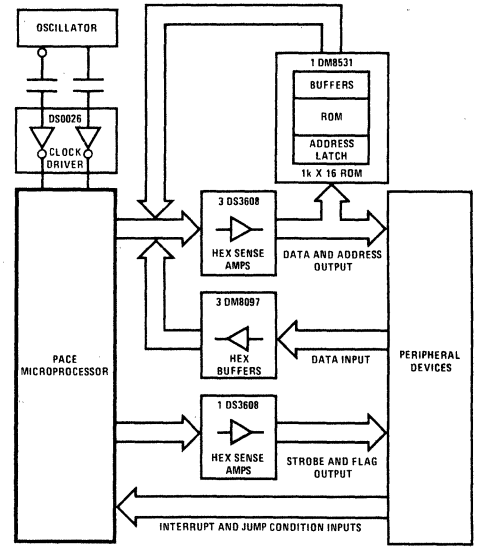
TOP VIEW

ordering information

ORDER NUMBERS	PACKAGE
DS1605J, DS1606J, DS1607J, DS1608J	Cavity DIP (J)
DS3605J, DS3606J, DS3607J, DS3608J	Cavity DIP (J)
DS3605N, DS3606N, DS3607N, DS3608N	Molded DIP (N)

typical application

PACE Interface



DS3608 shown as an interface between the PACE microprocessor and TTL data bus and I/O bus.

5

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Input Drive Current per Input	25 mA
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS3605/DS3606, DS3607/DS3608	4.75	5.25	V
DS1605/DS1606, DS1607/DS1608	4.5	5.5	V
Temperature, T_A			
DS3605/DS3606, DS3607/DS3608	0	+70	°C
DS1605/DS1606, DS1607/DS1608	−55	+125	°C

dc electrical characteristics (Notes 2 and 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH} Logical "1" Input Voltage Disable	V_{CC} = Min		2			V
I_{IH} Logical "1" Input Current Disable	V_{CC} = Max, V_{IN} = 2.4V				40	μA
V_{IL} Logical "0" Input Voltage Disable	V_{CC} = Min				0.8	V
I_{IL} Logical "0" Input Current Disable	V_{IN} = 0.4V				−1.6	mA
V_{CD} Input Clamp Voltage Disable	V_{CC} = Min, I_{IN} = −12 mA			−1	−1.5V	V
V_{OH} Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −5 mA		2.4			V
I_{OS} Output Short Circuit Current	V_{CC} = Max, V_{OUT} = 0V (Note 4)		−20	−50	−90	mA
V_{OL} Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 50 mA			0.3	0.4	V
I_{OL} Logical "0" Output Current	V_{CC} = Min, V_{OL} = 0.4		50			mA
I_{OUT} TRI-STATE Output Current	V_{CC} = Max, 0.4V ≤ V_{OUT} ≤ 2.4V		−40		40	μA
I_{IN} TRI-STATE Input Current	V_{CC} = Max, 0.4V ≤ V_{IN} ≤ 5V		−40		40	μA
I_{TH} Input Threshold Current	V_{CC} = 5V, T_A = 25°C, I_P = 0μA		100	250	400	μA
	V_{CC} = 5V, T_A = 25°C, I_P = 1 mA		1000	1250	1500	μA
I_{MAX} Maximum Input Driver Per Input	V_{CC} = Max			15	8	mA
I_{CC} Supply Current	V_{CC} = Max	DS1605/DS3605		80	115	mA
		DS1606/DS1607		90	115	mA
		DS3606/DS3607		90	130	mA
		DS1608/DS3608		80	115	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1605, DS1606, DS1607 and DS1608, and across the 0°C to +70°C range for the DS3605, DS3606, DS3607 and DS3608. All typicals are given for V_{CC} = 5.0V, and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

ac electrical characteristics

Unless otherwise specified, $T_A = 25°C$, $V_{CC} = 5V$

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PD0} Propagation Delay	C_L = 50 pF, R_L = 80Ω, I_P = 750μA, I_{IN} = 2 mA	DS1605/DS3605		15	22	ns
		DS1606/DS3606		26	39	ns
		DS1607/DS3607		24	35	ns
		DS1608/DS3608		20	30	ns
t_{PD1} Propagation Delay	C_L = 50 pF, R_L = 80Ω, I_P = 750μA, I_{IN} = 2 mA	DS1605/DS3605		15	22	ns
		DS1606/DS3606		19	29	ns
		DS1607/DS3607		19	29	ns
		DS1608/DS3608		14	21	ns
t_{0H} TRI-STATE Delays (Input/Output)	C_L = 5 pF, R_L = 80Ω, I_P = 750μA, I_{IN} = 2 mA	DS1605/DS3605		18	32	ns
		DS1606/DS3606		18	32	ns
		DS1607/DS3607		20	35	ns
		DS1608/DS3608		20	35	ns
t_{1H} TRI-STATE Delays (Input/Output)	C_L = 5 pF, R_L = 80Ω, I_P = 750μA, I_{IN} = 2 mA	DS1605/DS3605		8	14	ns
		DS1606/DS3606		8	14	ns
		DS1607/DS3607		10	18	ns
		DS1608/DS3608		10	18	ns
t_{H0}* TRI-STATE Delays (Input/Output)	C_L = 50 pF, R_L = 80Ω, I_P = 750μA, I_{IN} = 2 mA	DS1605/DS3605		22	40	ns
		DS1606/DS3606		20	35	ns
		DS1607/DS3607		45	80	ns
		DS1608/DS3608		45	80	ns
t_{H1}* TRI-STATE Delays (Input/Output)	C_L = 50 pF, R_L = 80Ω, I_P = 750μA, I_{IN} = 2 mA	DS1605/DS3605		25	45	ns
		DS1606/DS3606		26	45	ns
		DS1607/DS3607		35	60	ns
		DS1608/DS3608		35	60	ns

*Data valid only after this delay.

truth tables

DS1605/DS3605 (Note 1)

I_{IN}	DIS	OUT
X	H	Hi-Z
$>I_T$	L	H
$<I_T$	L	L

DS1606/DS3606 (Note 2)

I_{IN}	DIS	OUT
X	H	Hi-Z
$>I_T$	L	L
$<I_T$	L	H

DS1607/DS3607 (Note 1)

I_{IN}	DIS	OUT
X	H	Hi-Z
$>I_T$	L	L
$<I_T$	L	H

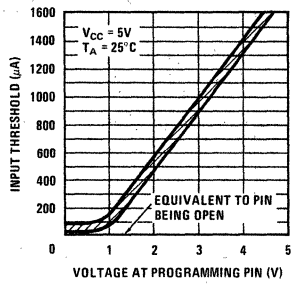
DS1608/DS3608 (Note 2)

I_{IN}	DIS	OUT
X	H	Hi-Z
$>I_T$	L	H
$<I_T$	L	L

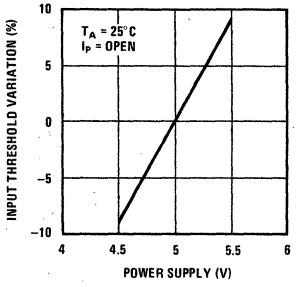
Note 1: Non-inverting inputs
Note 2: Inverting inputs

typical performance characteristics

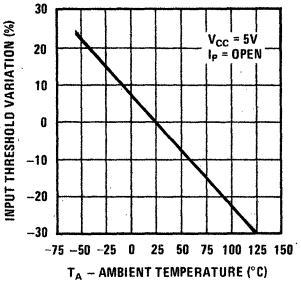
Typical Input Threshold vs Voltage at Programming Pin



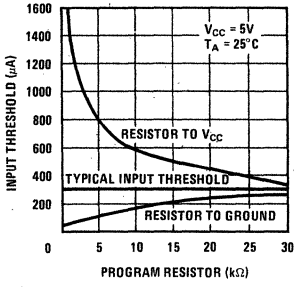
Input Threshold vs Power Supply Variation



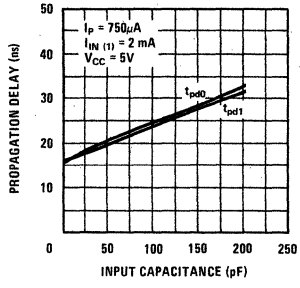
Input Threshold vs Temperature



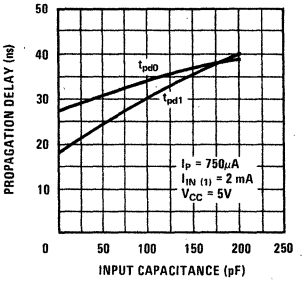
Typical Input Threshold Current vs Program Resistor DS3605 Series



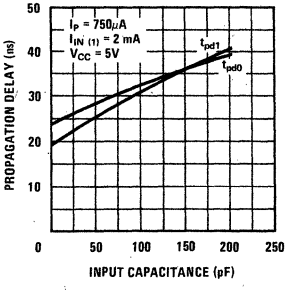
Typical Propagation Delay vs Input Capacitance DS1605/DS3605



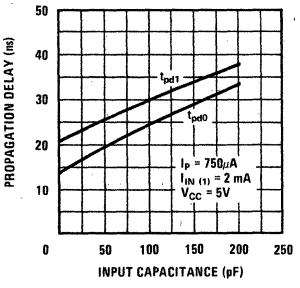
Typical Propagation Delay vs Input Capacitance DS1606/DS3606



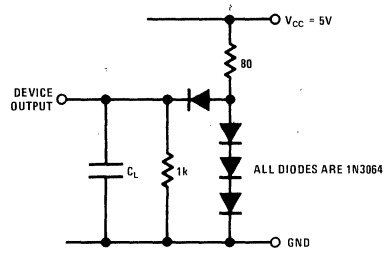
Typical Propagation Delay vs Input Capacitance DS1607/DS3607



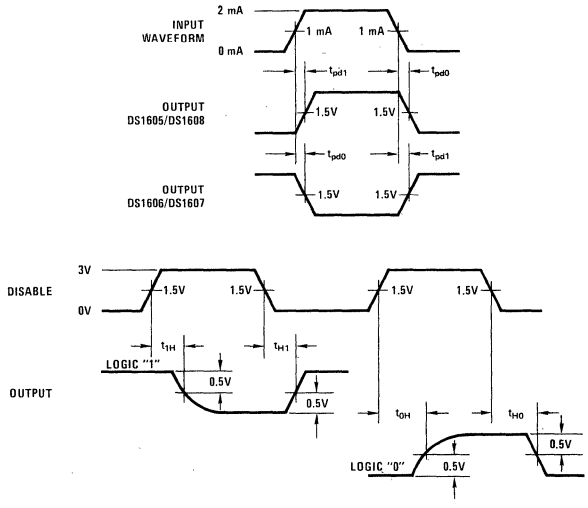
Typical Propagation Delay vs Input Capacitance DS1608/DS3608



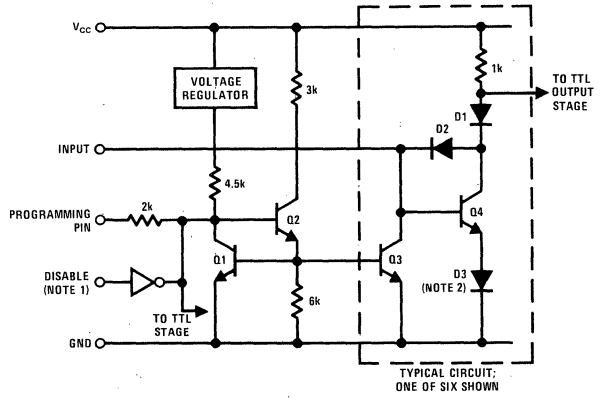
ac test circuit



switching time waveforms



equivalent circuit



Note 1: On the DS3605 and DS3606, the disable is only connected to the output stage. On the DS3607 and DS3608, it is connected to both the input and output.

Note 2: Diode D3 is used in the DS3607 and DS3608 only. In the DS3605 and DS3606, the emitter of Q4 is connected directly to ground.

NATIONAL

Sense Amplifiers

DS3625 dual high speed MOS sense amp

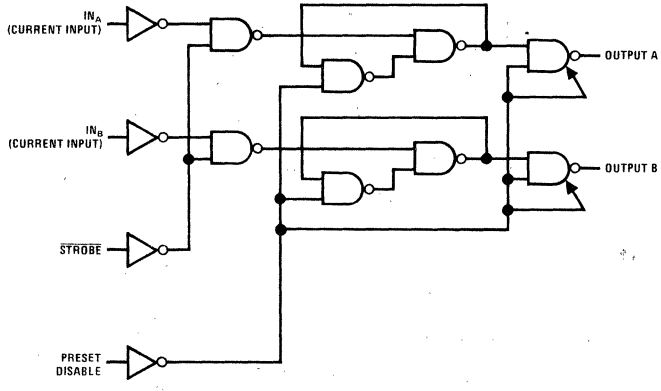
general description

The DS3625 is a dual high speed MOS to TTL level converter. It acts as an interface level converter between MOS and TTL logic devices. It consists of two 1-input converters with common strobe input to inhibit "0" entry when strobe is high. It allows parallel entry when strobe is low and the internal latch is preset by the common preset input. TRI-STATE® output logic is implemented in this circuit to facilitate high speed time sharing of decoder-drivers, fast random-access (or sequential) memory arrays, etc.

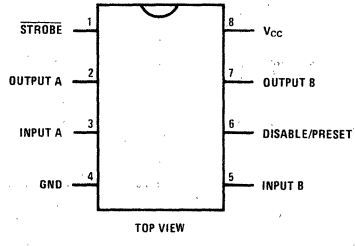
features

- Easily interfaces with most popular 1k and 2k dynamic MOS RAMs
- Pin-for-pin replacement for the 8T25
- Very low output impedance — high drive ability
- High impedance output state which allows many outputs to be connected to a common bus line
- Average power dissipation 110 mW per converter

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS3625N

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	+70	°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
I_{INA}, I_{INB}	Logical "1" Input Current	V_{CC} = Min		400			μA
I_{INA}, I_{INB}	Logical "0" Input Current	V_{CC} = Min				200	μA
V_{IH}	Logical "1" Input Voltage	Strobe, Preset/Disable, V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	Strobe, Preset/Disable, V_{CC} = Min				0.8	V
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −1.5 mA		2.8			V
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA				0.4	V
I_O	TRI-STATE Output Current	V_{CC} = Max	V_O = 3.9V			100	μA
			V_O = 0.0V			−100	μA
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			40	μA
			V_{IN} = 5.5V			1.0	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max, $V_{IN(PRE/DIS)}$ = 2.0V, Other Inputs = 0V				40	mA
V_{CD}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA				1.5	V
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_O = 0V, (Note 3)		−20		−70	mA

switching characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{ds}	Propagation Delay to a Logical "0" from Strobe to Output	V_{CC} = 5.0V, T_A = 25°C		17	25	ns
t_{1H}	Delay from Disable Input to High Impedance State (from Logical "1" Level)	V_{CC} = 5.0V, T_A = 25°C		7.0	11	ns
t_{0H}	Delay from Disable Input to High Impedance State (from Logical "0" Level)	V_{CC} = 5.0V, T_A = 25°C		17	25	ns
t_{H1}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	V_{CC} = 5.0V, T_A = 25°C		9.0	14	ns
t_{H0}	Delay from Disable Input to Logical "0" Level (from High Impedance State)	V_{CC} = 5.0V, T_A = 25°C		13.5	16	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for V_{CC}=5.0V, T_A = 25°C.

Note 3: Only one output at a time should be shorted.

NATIONAL

Sense Amplifiers

Advance Information*

DS3651, DS3653 quad high speed MOS sense amplifiers

general description

The DS3651 and DS3653 are TTL compatible high speed circuits intended for sensing in a broad range of MOS memory system applications. Switching speeds have been enhanced over conventional sense amplifiers by application of Schottky technology, and TRI-STATE® strobing is incorporated offering a high impedance output state for bused organization.

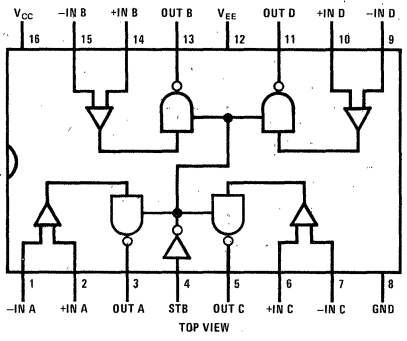
The DS3651 has active pull-up outputs, and the DS3653 offers open collector outputs providing implied "AND" operations.

features

- High speed — 15 ns (typ)
- TTL compatible
- Input sensitivity — ±7 mV
- TRI-STATE outputs for high speed buses
- Standard supply voltages — ±5V
- Pin and function compatible with MC3430 and MC3432

connection diagram

Dual-In-Line Package



Order Number DS3651J, DS3651N, DS3653J or DS3653N

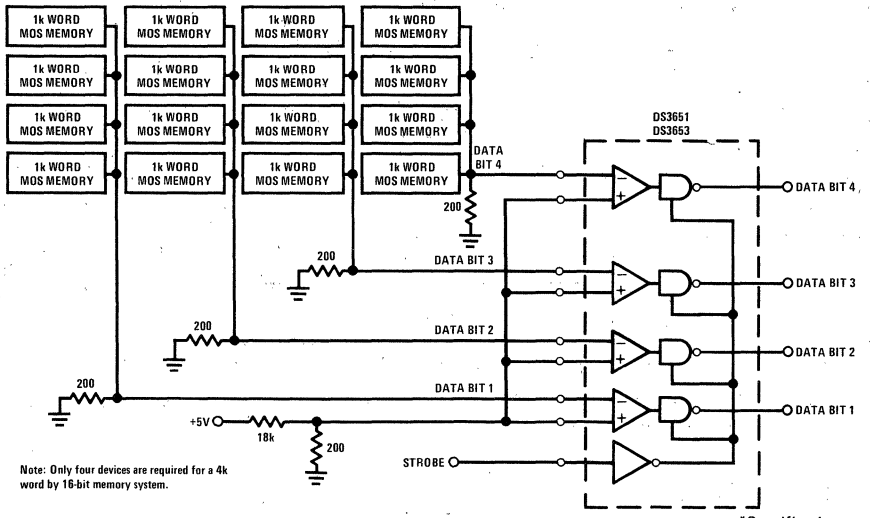
truth table

INPUT	STROBE	OUTPUT	
		DS3651	DS3653
$V_{ID} \geq +7.0$ mV, $T_A = 0°C$ to $+70°C$	L	H	Open
	H	Open	Open
-7.0 mV $\leq V_{ID} \leq +7.0$ mV, $T_A = 0°C$ to $+70°C$	L	X	X
	H	Open	Open
$V_{ID} \leq -7.0$ mV, $T_A = 0°C$ to $+70°C$	L	L	L
	H	Open	Open

L = Low logic state
H = High logic state
Open = TRI-STATE
X = Indeterminate State

typical applications

A Typical MOS Memory Sensing Application for a 4k word by 4-bit memory arrangement employing 1103 type memory devices



Note: Only four devices are required for a 4k word by 16-bit memory system.

*Specifications may change

absolute maximum ratings

(Note 1)

Power Supply Voltages	
V_{CC}	±7.0 V_{DC}
V_{EE}	±7.0 V_{DC}
Differential-Mode Input Signal Voltage Range, V_{IDR}	±6.0 V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	±5.0 V_{DC}
Strobe Input Voltage, $V_{I(S)}$	5.5 V_{DC}
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

(T_A = 0°C to +70°C unless otherwise noted.)

	MIN	MAX	UNITS
Power Supply Voltages			
V_{CC}	+4.75	+5.25	V_{DC}
V_{EE}	−4.75	−5.25	V_{DC}
Output Load Current, I_{OL}		16	mA
Differential-Mode Input Voltage Range, V_{IDR}	−5.0	+5.0	V_{DC}
Common-Mode Input Voltage Range, V_{ICR}	−3.0	+3.0	V_{DC}
Input Voltage Range (any input to GND), V_{IR}	−5.0	+3.0	V_{DC}
Operating Temperature Range	0	+70	°C

electrical characteristics

(V_{CC} = +5.0 V_{DC}, V_{EE} = −5.0 V_{DC}, T_A = 0°C to +70°C unless otherwise noted.) (Notes 2 and 3)

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{IS}	Input Sensitivity , (Note 5) (Common-Mode Voltage Range = −3.0V ≤ V_{IN} ≤ 3.0V)	4.75 ≤ V_{CC} ≤ 5.25V −4.75 ≥ V_{EE} ≥ −5.25V					±7.0	mV
V_{IO}	Input Offset Voltage					2		mV
I_{IB}	Input Bias Current	V_{CC} = 5.25V, V_{EE} = −5.25V					20	μA
I_{IO}	Input Offset Current					1		μA
$V_{IL(S)}$	Strobe Input Voltage (Low State)						0.8	V
$V_{IH(S)}$	Strobe Input Voltage (High State)				2			V
$I_{IL(S)}$	Strobe Current (Low State)	V_{CC} = 5.25V, V_{EE} = −5.25V, V_{IN} = 0.4V					−1.6	mA
$I_{IH(S)}$	Strobe Current (High State)	V_{CC} = 5.25V, V_{EE} = −5.25V	V_{IN} = 2.4V V_{IN} = 5.25V				40 1	μA mA
V_{OH}	Output Voltage (High State)	V_{CC} = 4.75V, V_{EE} = −4.75V	I_O = −400μA	DS3651	2.4			V
V_{OL}	Output Voltage (Low State)	V_{CC} = 4.75V V_{EE} = −4.75V	I_O = 16 mA				0.4	V
I_{CEX}	Output Leakage Current	V_{CC} = 4.75V, V_{EE} = −4.75V	V_O = 5.25V	DS3652			250	μA
I_{OS}	Output Current Short Circuit	V_{CC} = 5.25V, V_{EE} = −5.25V (Note 4)		DS3651	−18		−70	mA
I_{OFF}	Output Disable Leakage Current	V_{CC} = 5.25V, V_{EE} = −5.25V		DS3651			40	μA
I_{CC}	High Logic Level Supply Current	V_{CC} = 5.25V, V_{EE} = −5.25V				45	60	mA
I_{EE}	High Logic Level Supply Current	V_{CC} = 5.25V, V_{EE} = −5.25V				−17	−30	mA

switching characteristics (V_{CC} = +5.0 V_{DC}, V_{EE} = −5.0 V_{DC}, T_A = +25°C unless otherwise noted.)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{PHL(D)}$	High-to-Low Logic Level Propagation Delay Time (Differential Inputs)	5.0 mV + V_{IS}, *(Figure 3)*	DS3651		10		ns
			DS3653		12		ns
$t_{PLH(D)}$	Low-to-High Logic Level Propagation Delay Time (Differential Inputs)	5.0 mV + V_{IS}, *(Figure 3)*	DS3651		15		ns
			DS3653		18		ns
$t_{POH(S)}$	TRI-STATE to High Logic Level Propagation Delay Time (Strobe)	*(Figure 1)*	DS3651		8		ns
$t_{PHO(S)}$	High Logic Level to TRI-STATE Propagation Delay Time (Strobe)	*(Figure 1)*	DS3651		8		ns
$t_{POL(S)}$	TRI-STATE to Low Logic Level Propagation Delay Time (Strobe)	*(Figure 1)*	DS3651		10		ns
$t_{PLO(S)}$	Low Logic Level to TRI-STATE Propagation Delay Time (Strobe)	*(Figure 1)*	DS3651		10		ns
$t_{PHL(S)}$	High-to-Low Logic Level Propagation Delay Time (Strobe)	*(Figure 2)*	DS3651		7		ns
			DS3653		8		ns
$t_{PLH(S)}$	Low-to-High Logic Level Propagation Delay Time (Strobe)	*(Figure 2)*	DS3651		7		ns
			DS3653		8		ns

5

notes

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

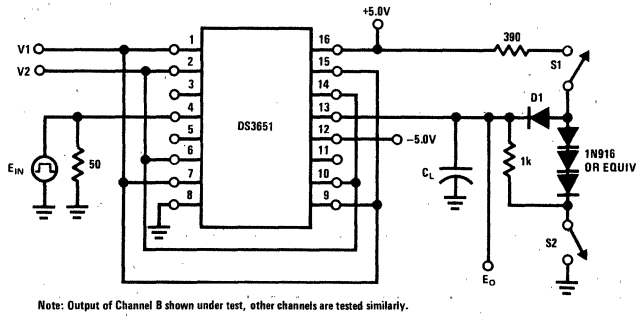
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS3651 and DS3653. All typical values are for T_A = 25°C, V_{CC} = 5V, and V_{EE} = −5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: A parameter which is of primary concern when designing with sense amplifiers is, what is the minimum differential input voltage required at the sense amplifier input terminals to guarantee a given output logic state. This parameter is commonly referred to as threshold voltage. It is well known that design considerations of threshold voltage are plagued by input offset currents, bias currents, network source resistances, and voltage gain. As a design convenience, the DS3651 and DS3653 are specified to a parameter called input sensitivity (V_{IS}). This parameter takes into consideration input offset currents and bias currents, and guarantees a minimum input differential voltage to cause a given output logic state with respect to a maximum source impedance of 200 ohms at each input.

ac test circuits and switching time waveforms



Note: Output of Channel B shown under test, other channels are tested similarly.

	V1	V2	S1	S2	C_L
$t_{PLO(S)}$	100 mV	GND	Closed	Closed	15 pF
$t_{POL(S)}$	100 mV	GND	Closed	Open	50 pF
$t_{PHO(S)}$	GND	100 mV	Closed	Closed	15 pF
$t_{POH(S)}$	GND	100 mV	Open	Closed	50 pF

C_L includes jig and probe capacitance.

E_{IN} waveform characteristics: t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%.

PRR = 1.0 MHz

Duty Cycle = 50%

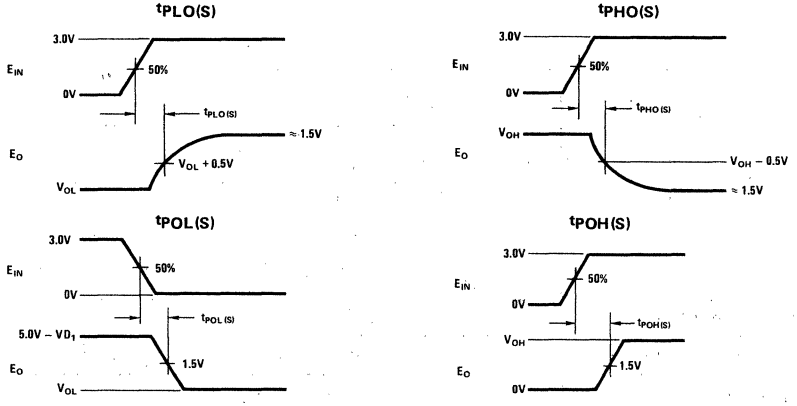
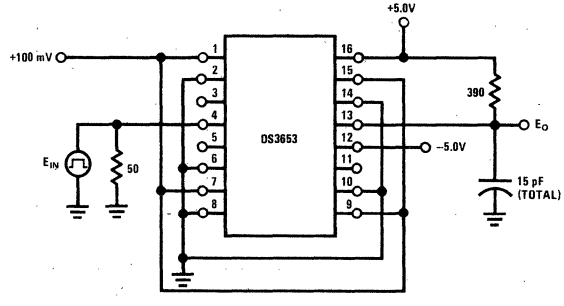
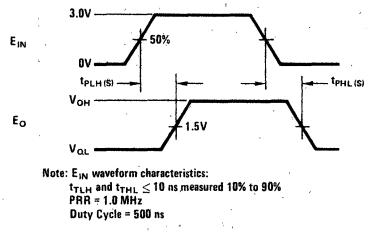


FIGURE 1. Strobe Propagation Delay Times $t_{PLO(S)}$, $t_{POL(S)}$, $t_{PHL(S)}$ and $t_{POH(S)}$



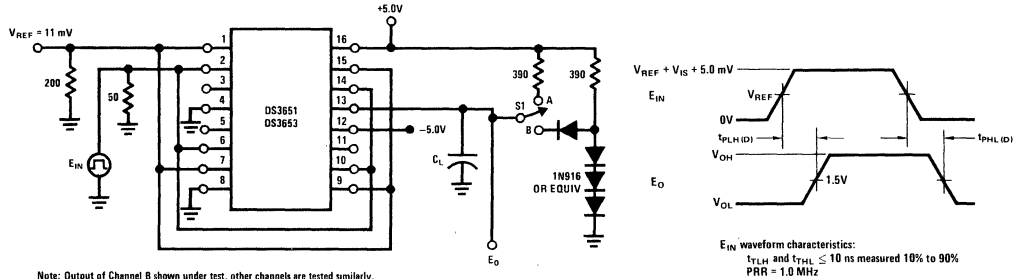
Note: Output of Channel B shown under test, other channels are tested similarly.



Note: E_{IN} waveform characteristics:
t_{TLH} and $t_{THL} \leq 10$ ns measured 10% to 90%
PRR = 1.0 MHz
Duty Cycle = 500 ns

FIGURE 2. Strobe Propagation Delay $t_{PLH(S)}$ and $t_{PHL(S)}$

ac test circuits and switching time waveforms (con't)

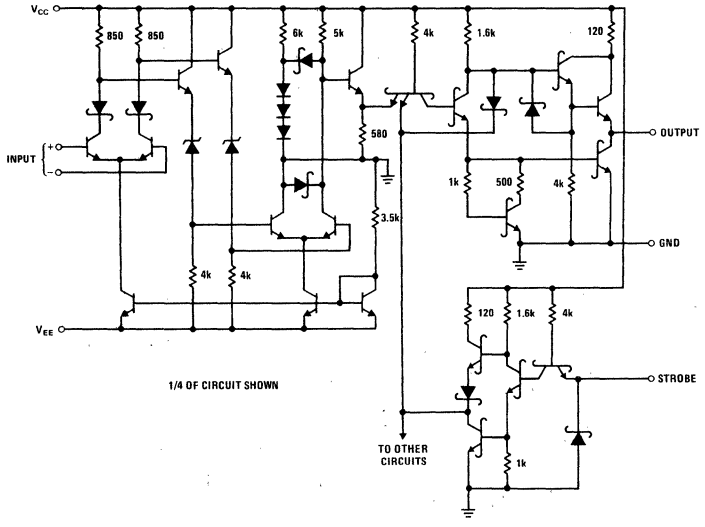


Note: Output of Channel B shown under test, other channels are tested similarly.
S1 at "A" for DS3653 C_L = 15 pF total for DS3653
S1 at "B" for DS3651 C_L = 50 pF total for DS3651

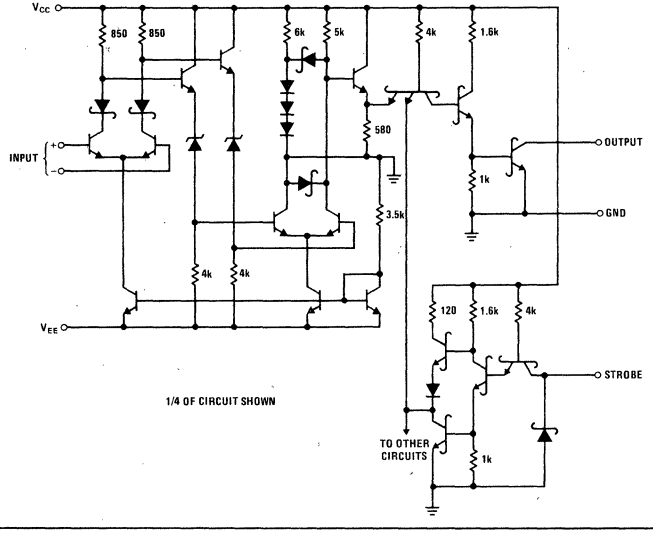
FIGURE 3. Differential Input Propagation Delay $t_{PLH(D)}$ and $t_{PHL(D)}$

schematic diagrams

DS3651



DS3653



typical applications (con't)

4-Bit Parallel A/D Converter

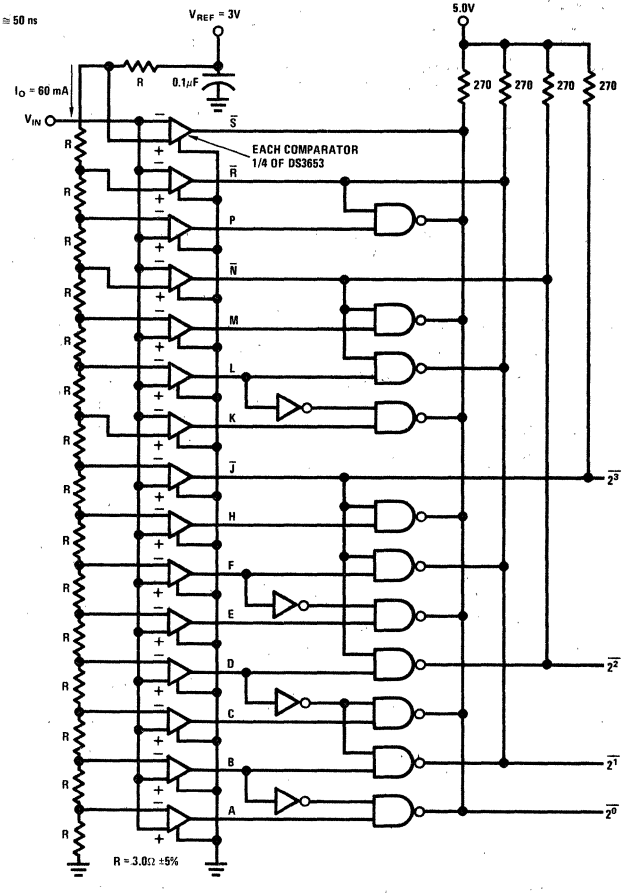
$\overline{2^0} = (\overline{A} + B)(\overline{C} + D)(\overline{E} + F)(\overline{H} + J)(\overline{K} + L)(\overline{M} + N)(\overline{P} + R)(\overline{S})$

$\overline{2^1} = (\overline{B} + D)(\overline{F} + J)(\overline{L} + N)(\overline{R})$

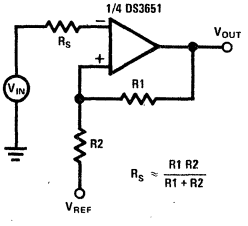
$\overline{2^2} = (\overline{D} + J)(\overline{N})$

$\overline{2^3} = \overline{J}$

CONVERSION TIME ≈ 50 ns

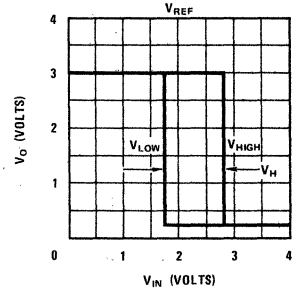


Level Detector with Hysteresis



$$R_S \approx \frac{R1\ R2}{R1 + R2}$$

Transfer Characteristics and Equations for Level Detector with Hysteresis



$$V_{HIGH} = V_{REF} + \frac{R2\ [V_{O(MAX)} - V_{REF}]}{R1 + R2}$$

$$V_{LOW} = V_{REF} + \frac{R2\ [V_{O(MIN)} - V_{REF}]}{R1 + R2}$$

HYSTERESIS LOOP (V_H)

$$V_H = V_{HIGH} - V_{LOW} = \frac{R2}{R1 + R2}\ [V_{O(MAX)} - V_{O(MIN)}]$$

Sense Amplifiers

NATIONAL

DS5520/DS7520, DS5520A/DS7520A series dual core memory sense amplifiers general description

The devices in this series of dual core sense amplifiers convert bipolar millivolt-level memory sense signals to saturated logic levels. The design employs a common reference input which allows the input threshold voltage level of both amplifiers to be adjusted. Separate strobe inputs provide time discrimination for each channel. Logic inputs and outputs are DTL/TTL compatible. All devices of the series have identical preamplifier configurations, while various logic connections are provided to suit the specific application.

The DS5520/DS7520 has output latch capability and provides sense, strobe, and memory function for two sense lines. The DS5522/DS7522 contains a single open collector output which may be used to expand the number of inputs of the DS5520/DS7520, or to drive an external Memory Data Register (MDR). Intended for small memories, the two channels of the DS5524/DS7524 are independent with two separate outputs. The DS5534/DS7534 is similar to the DS5524/DS7524 but has uncommitted, wire-ORable outputs. The DS5528/DS7528 has the same logic configuration of the DS5524/DS7524 and in addition provides separate low impedance Test Points at each preamplifier output. A similar device having uncommitted, wire-ORable outputs is the DS5538/DS7538.

features

- High speed
- Guaranteed narrow threshold uncertainty over temperature
- Adjustable input threshold voltage
- Fast overload recovery times
- Two amplifiers per package
- Molded or cavity dual-in-line package
- Six logic configurations

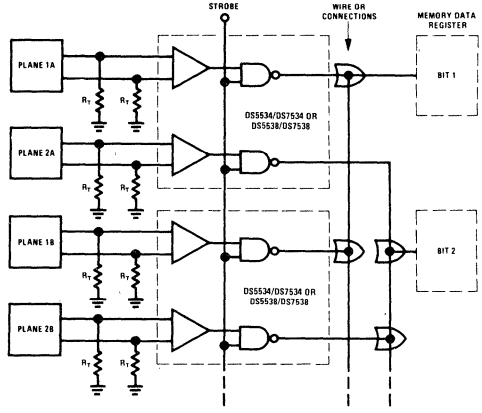
Part numbers ending with an even number followed by an "A" (e.g., DS5520A) correspond to a very tight input threshold of ±2 mV. Part numbers ending with an even number (DS5520) correspond to an input threshold of ±4 mV. Part numbers ending with an odd number (e.g., DS5521) correspond to an input threshold of ±8 mV. The remaining specifications for the three are identical. All devices meet or exceed the specifications for the corresponding device (where applicable) in the SN5520/SN7520 series and are pin-for-pin replacements.

Because these devices are duals that contain an internal regulator, care must be exercised in testing to insure that while one half is being tested, the other inputs must be grounded or connected to a signal that is within the input range of the device.

absolute maximum ratings

Supply Voltage	±7V
Differential or Reference Input Voltage	±5V
Logic Input Voltage	5.5V
Operating Temperature Range	
DS55XX	−55°C to +125°C
DS75XX	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

typical application



Expanded Small Memory System

5

electrical characteristics

DS5520/DS5520A, DS5521: The following apply for $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
DS7520/DS7520A, DS7521: The following apply for $0^{\circ}C \leq T_A \leq +70^{\circ}C$

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{TH}	Differential Input Threshold Voltage	$V_{CC} = \pm 5.0V$ (Note 4)	V_{REF} = 15 mV	DS5520/DS7520	11	15	19	mV
				DS5520A/DS7520A	13	15	17	mV
				DS5521/DS7521	8	15	22	mV
			V_{REF} = 40 mV	DS5520/DS7520	36	40	44	mV
				DS5520A/DS7520A	38	40	42	mV
				DS5521/DS7521	33	40	47	mV
I_{BIAS}	Differential and Reference Input Bias Current	$V_{CC} = \pm 5.25V$, $V_{IN} = 0V$		DS5520/DS5520A, DS5521		30	100	μA
				DS7520/DS7520A, DS7521		30	75	μA
I_{OS}	Differential Input Offset Current	$V_{CC} = \pm 5.25V$ $V_{DIFF} = 0V$, $V_{IN} = 0V$				0.5		μA
V_{IH}	Logical "1" Input Voltage				2			V
I_{IH}	Logical "1" Input Current Strobe, Gate Inputs	$V_{CC} = \pm 5.25V$	V_{IN} = 2.4V			5	40	μA
			V_{IN} = 5.5V				1	mA
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IL}	Logical "0" Input Current, Strobe, Gate Inputs	$V_{CC} = \pm 5.25V$, $V_{IN} = 0.4V$				−1	−1.6	mA
V_{CD}	Input Clamp Voltage	$I_{IN} = -12$ mA					−1.5	V
V_{OH}	Logical "1" Output Voltage	$V_{CC} = \pm 4.75V$, $I_O = -400\mu A$			2.4	3.9		V
I_{SC}	Output Short Circuit Current	$V_{CC} = \pm 5.25V$, $V_O = 0V$		Q Output	−3	−4	−5	mA
				$\overline{Q}$ Output	−2.1	−2.8	−3.5	mA
V_{OL}	Logical "0" Output Voltage	$V_{CC} = \pm 4.75V$, $I_O = 16$ mA				0.25	0.4	V
I_{CEX}	Output Leakage Current	$V_O = 5.25V$					250	μA
I_{CC^+}	V^+ Supply Current	$V_{CC} = \pm 5.25V$				21	35	mA
I_{CC^-}	V^- Supply Current	$V_{CC} = \pm 5.25V$				−13	−18	mA

Note 1: For $0^{\circ}C \leq T_A \leq +70^{\circ}C$ operation, electrical characteristics for DS5520/DS5520A and DS5521 are guaranteed the same as DS7520/DS7520A, and DS7521, respectively.

Note 2: Positive current is defined as current into the referenced pin.

Note 3: Pin 1 to have $\geq$ 100 pF capacitor connected to ground.

Note 4: For minimum V_{TH}, logic output is < 0.4V at 16 mA. For maximum V_{TH} logic output is > 2.4V at −400μA.

switching characteristics

$V^+ = 5.0V$, $V^- = -5.0V$, $T_A = 25°C$

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd1}	Differential Input to Logical "1"	V_{REF} = 20 mV, ac Test Circuit 1	Q Output		20	40	ns
			$\overline{Q}$ Output		36		ns
t_{pd0}	Differential Input to Logical "0"	V_{REF} = 20 mA, ac Test Circuit 1	Q Output		28		ns
			$\overline{Q}$ Output		28	55	ns
t_{pd1}	Strobe Input to Logical "1"	V_{REF} = 20 mA, ac Test Circuit 1	Q Output		10	30	ns
			$\overline{Q}$ Output		33		ns
t_{pd0}	Strobe Input to Logical "0"	V_{REF} = 20 mA, ac Test Circuit 1	Q Output		20		ns
			$\overline{Q}$ Output		16	55	ns
t_{pd1}	Gate Q Input to Logical "1"	V_{REF} = 20 mV, ac Test Circuit 2	Q Output		12		ns
			$\overline{Q}$ Output		17	20	ns
t_{pd0}	Gate Q Input to Logical "0"	V_{REF} = 20 mV, ac Test Circuit 2	Q Output		6		ns
			$\overline{Q}$ Output		19	30	ns
t_{pd1}	Gate $\overline{Q}$ Input to Logical "1"	V_{REF} = 20 mV, ac Test Circuit 2, $\overline{Q}$ Output			12		ns
t_{pd0}	Gate $\overline{Q}$ Input to Logical "0"	V_{REF} = 20 mV, ac Test Circuit 2, $\overline{Q}$ Output			6	20	ns
t_{DR}	Differential Input Overload Recovery Time	V_{REF} = 20 mV, ac Test Circuit 2			10		ns
t_{CMR}	Common-Mode Input Overload Recovery Time	V_{REF} = 20 mV, ac Test Circuit 2			5		ns
t_{CY}	Minimum Cycle Time	V_{REF} = 20 mV, ac Test Circuit 2			200		ns
V_{CM}	AC Common-Mode Input Firing Voltage	Pulse			±2.5		V

Note 1: For $0°C \leq T_A \leq +70°C$ operation, electrical characteristics for DS5520/DS5520A and DS5521 are guaranteed the same as DS7520/DS7520A, and DS7521, respectively.

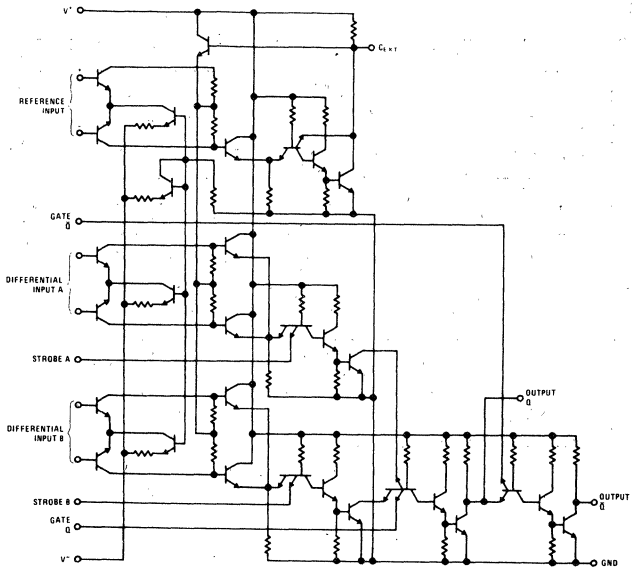
Note 2: Positive current is defined as current into the referenced pin.

Note 3: Pin 1 to have $\geq$ 100 pF capacitor connected to ground.

Note 4: For minimum V_{TH}, logic output is < 0.4V at 16 mA. For maximum V_{TH} logic output is > 2.4V at –400μA.

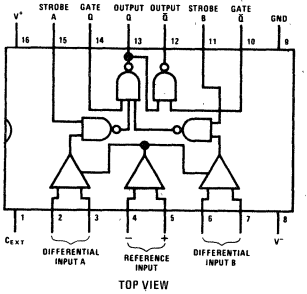
DS5520/DS7520, DS5520A/DS7520A and DS5521/DS7521

schematic diagram



connection diagram

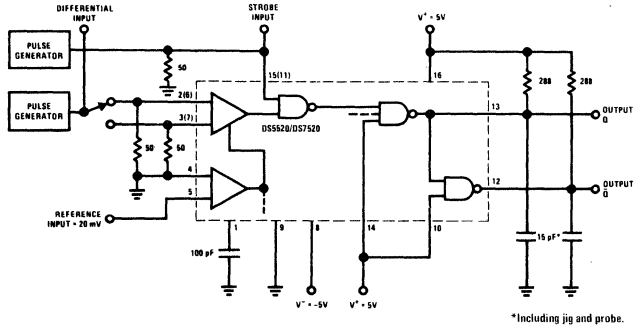
Dual-In-Line Package



TOP VIEW

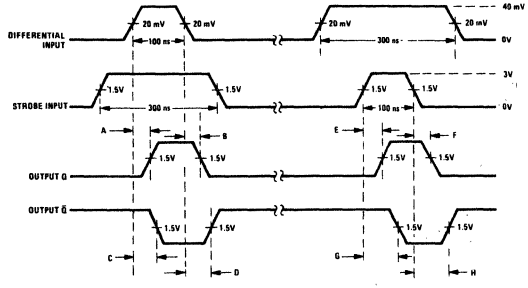
Order Number DS5520J, DS5520AJ, DS5521J, DS7520J, DS7520AJ, DS7521J, DS7520N DS7520AN or DS7521N

DS5520/DS7520, DS5520A/DS7520A and DS5521/DS7521
AC test circuit (1)



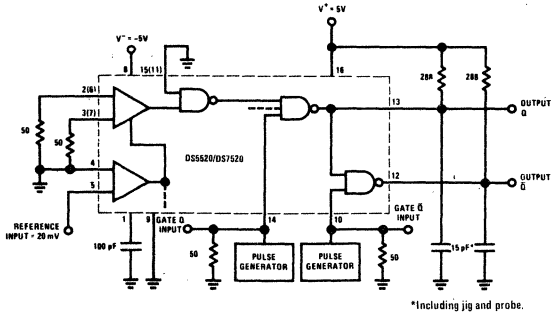
*Including jig and probe.

voltage waveforms (1)



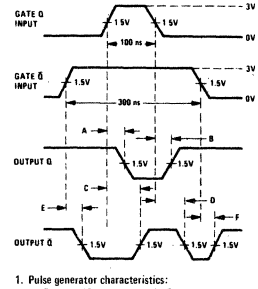
1. Pulse generator characteristics:
   Z_{OUT} = 50Ω, t_r = t_f = 15 ±5 ns, PRR = 1 MHz
2. Propagation delays:
   A = Differential input to logical "1" output Q
   B = Differential input to logical "0" output Q
   C = Differential input to logical "0" output Q̄
   D = Differential input to logical "1" output Q̄
   E = Strobe input to logical "1" output Q
   F = Strobe input to logical "0" output Q
   G = Strobe input to logical "0" output Q̄
   H = Strobe input to logical "1" output Q̄

AC test circuit (2)



*Including jig and probe.

voltage waveforms (2)



1. Pulse generator characteristics:
   Z_{OUT} = 50Ω, t_r = t_f = 15 ±5 ns, PRR = 1 MHz
2. Propagation delays:
   A = Gate Q input to logical "0" output Q
   B = Gate Q input to logical "1" output Q̄
   C = Gate Q input to logical "1" output Q̄
   D = Gate Q̄ input to logical "0" output Q̄
   E = Gate Q̄ input to logical "0" output Q̄
   F = Gate Q̄ input to logical "1" output Q̄

DS5522/DS7522, DS5522A/DS7522A and DS5523/DS7523

electrical characteristics

DS5522/DS5522A, DS5523: The following apply for $-55°C \leq T_A \leq +125°C$

DS7522/DS7522A, DS7523: The following apply for $0°C \leq T_A \leq +70°C$

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{TH}	Differential Input Threshold Voltage	$V_{CC} = \pm5.0V$ (Note 4)	$V_{REF} = 15\,mV$	DS5522/DS7522	11	15	19	mV
				DS5522A/DS7522A	13	15	17	mV
				DS5523/DS7523	8	15	22	mV
			$V_{REF} = 40\,mV$	DS5522/DS7522	36	40	44	mV
				DS5522A/DS7522A	38	40	42	mV
				DS5523/DS7523	33	40	47	mV
I_{BIAS}	Differential and Reference Input Bias Current	$V_{CC} = \pm5.25V$, $V_{IN} = 0V$		DS5522/DS5522A, DS5523		30	100	μA
				DS7522/DS7522A, DS7523		30	75	μA
I_{OS}	Differential Input Offset Current	$V_{CC} = \pm5.25V$ $V_{DIFF} = 0V$, $V_{IN} = 0V$				0.5		μA
V_{IH}	Logical "1" Input Voltage				2			V
I_{IH}	Logical "1" Input Current Strobe, Gate Inputs	$V_{CC} = \pm5.25V$	$V_{IN} = 2.4V$			5	40	μA
			$V_{IN} = 5.5V$				1	mA
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IL}	Logical "0" Input Current, Strobe, Gate Inputs	$V_{CC} = \pm5.25V$, $V_{IN} = 0.4V$				−1	−1.6	mA
V_{CD}	Input Clamp Voltage	$I_{IN} = -12\,mA$					−1.5	V
V_{OH}	Logical "1" Output Voltage	$V_{CC} = \pm4.75V$, $I_O = -400\mu A$			2.4	3.9		V
I_{SC}	Output Short Circuit Current	$V_{CC} = \pm5.25V$, $V_O = 0V$			−2.1	−2.8	−3.5	mA
V_{OL}	Logical "0" Output Voltage	$V_{CC} = \pm4.75V$, $I_O = 16\,mA$				0.25	0.4	V
I_{CEX}	Output Leakage Current	$V_O = 5.25V$					250	μA
I_{CC^+}	V^+ Supply Current	$V_{CC} = \pm5.25V$				23	36	mA
I_{CC^-}	V^- Supply Current	$V_{CC} = \pm5.25V$				−13	−18	mA

switching characteristics

The following apply for $T_A = 25°C$, $V^+ = 5.0V$, $V^- = -5.0V$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Differential Input to Logical "1" Output	AC Test Circuit		26		ns
t_{pd1}	Strobe Input to Logical "1" Output	AC Test Circuit		22		ns
t_{pd1}	Gate Input to Logical "1" Output	$V_{CC} = \pm5.0V$, AC Test Circuit		4		ns
t_{pd0}	Differential Input to Logical "0" Output	AC Test Circuit		21	45	ns
t_{pd0}	Strobe Input to Logical "0" Output	AC Test Circuit		12	40	ns
t_{pd0}	Gate Input to Logical "0" Output	AC Test Circuit		15	25	ns
t_{DR}	Differential Input Overload Recovery Time			10		ns
t_{CMR}	Common-Mode Input Overload Recovery Time			5		ns
t_{CY}	Minimum Cycle Time			200		ns
V_{CM}	AC Common-Mode Input Firing Voltage	Pulse		±2.5		V

Note 1: For $0°C \leq T_A \leq +70°C$ operation, electrical characteristics for DS5522/DS5522A and DS5523 are guaranteed the same as DS7522/DS7522A and DS7523, respectively.

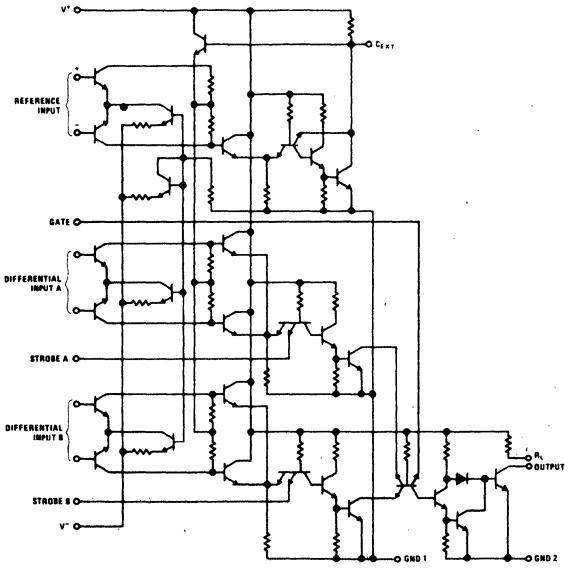
Note 2: Positive current is defined as current into the referenced pin.

Note 3: Pin 1 to have ≥ 100 pF capacitor connected to ground.

Note 4: For min V_{TH}, logic output is > 2.4 V at −400μA. For max V_{TH}, logic output is < 0.4V at 16 mA.

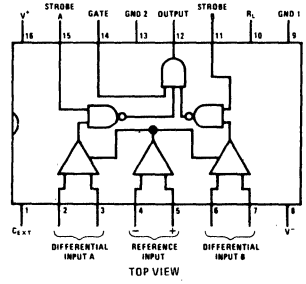
DS5522/DS7522, DS5522A/DS7522A and DS5523/DS7523

schematic diagram



connection diagram

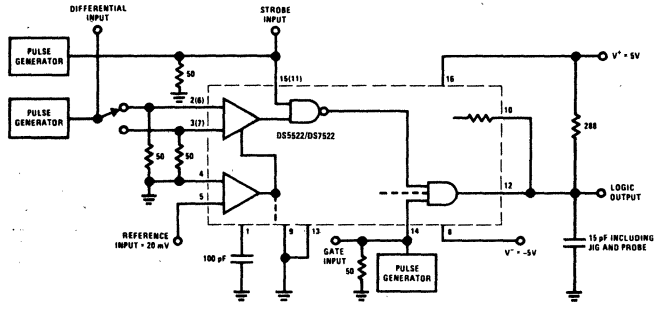
Dual-In-Line Package



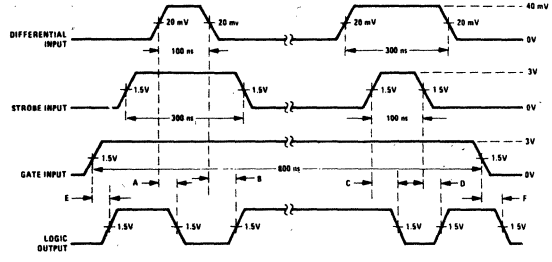
TOP VIEW

Order Number DS5522J, DS5522AJ, DS5523J, DS7522J, DS7522AJ, DS7523J, DS7522N, DS7522AN or DS7523N

AC test circuit



voltage waveforms



1. One strobe is grounded when the other side is being tested.
2. Pulse generator characteristics:
   $Z_{OUT} = 50\Omega$, $t_r = t_f = 15 \pm 5$ ns, PRR = 1 MHz
3. Propagation delays:
   A = Differential input to logical "0" output
   B = Differential input to logical "1" output
   C = Strobe input to logical "0" output
   D = Strobe input to logical "1" output
   E = Gate input to logical "1" output
   F = Gate input to logical "0" output

5

DS5524/DS7524, DS5524A/DS7524A and DS5525/DS7525

electrical characteristics

DS5524/DS5524A, DS5525: The following apply for $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
DS7524/DS7524A, DS7525: The following apply for $0^{\circ}C \leq T_A \leq +70^{\circ}C$

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{TH}	Differential Input Threshold Voltage	$V_{CC} = \pm5.0V$ (Note 4)	$V_{REF} = 15\,mV$	DS5524/DS7524	11	15	19	mV
				DS5524A/DS7524A	13	15	17	mV
				DS5525/DS7525	8	15	22	mV
			$V_{REF} = 40\,mV$	DS5524/DS7524	36	40	44	mV
				DS5524A/DS7524A	38	40	42	mV
				DS5525/DS7525	33	40	47	mV
I_{BIAS}	Differential and Reference Input Bias Current	$V_{CC} = \pm5.25V$, $V_{IN} = 0V$		DS5524/DS5524A, DS5525		30	100	μA
				DS7524/DS7524A, DS7525		30	75	μA
I_{OS}	Differential Input Offset Current	$V_{CC} = \pm5.25V$ $V_{DIFF} = 0V$, $V_{IN} = 0V$				0.5		μA
V_{IH}	Logical "1" Input Voltage				2			V
I_{IH}	Logical "1" Input Current Strobe, Gate Inputs	$V_{CC} = \pm5.25V$	$V_{IN} = 2.4V$			5	40	μA
			$V_{IN} = 5.5V$				1	mA
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IL}	Logical "0" Input Current, Strobe, Gate Inputs	$V_{CC} = \pm5.25V$, $V_{IN} = 0.4V$				−1	−1.6	mA
V_{CD}	Input Clamp Voltage	$I_{IN} = -12\,mA$					−1.5	V
V_{OH}	Logical "1" Output Voltage	$V_{CC} = \pm4.75V$, $I_O = -400\mu A$			2.4	3.9		V
I_{SC}	Output Short Circuit Current	$V_{CC} = \pm5.25V$, $V_O = 0V$			−2.1	−2.8	−3.5	mA
V_{OL}	Logical "0" Output Voltage	$V_{CC} = \pm4.75V$, $I_O = 16\,mA$				0.25	0.4	V
I_{CC+}	V^+ Supply Current	$V_{CC} = \pm5.25V$				29	40	mA
I_{CC-}	V^- Supply Current	$V_{CC} = \pm5.25V$				−13	−18	mA

switching characteristics

The following apply for $T_A = 25^{\circ}C$, $V^+ = 5.0V$, $V^- = -5.0V$

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Differential Input to Logical "1" Output	AC Test Circuit		20	40	ns
t_{pd1}	Strobe Input to Logical "1" Output	AC Test Circuit		10	30	ns
t_{pd0}	Differential Input to Logical "0" Output	$V_{CC} = \pm5.0V$, AC Test Circuit		28		ns
t_{pd0}	Strobe Input to Logical "0" Output	AC Test Circuit		20		ns
t_{DR}	Differential Input Overload Recovery Time			10		ns
t_{CMR}	Common-Mode Input Overload Recovery Time			5		ns
t_{CY}	Minimum Cycle Time			200		ns
V_{CM}	AC Common-Mode Input Firing Voltage	Pulse		±2.5		V

Note 1: For $0^{\circ}C \leq T_A \leq +70^{\circ}C$ operation, electrical characteristics for DS5524/DS5524A and DS5525 are guaranteed the same as DS7524/DS7524A and DS7525 respectively.

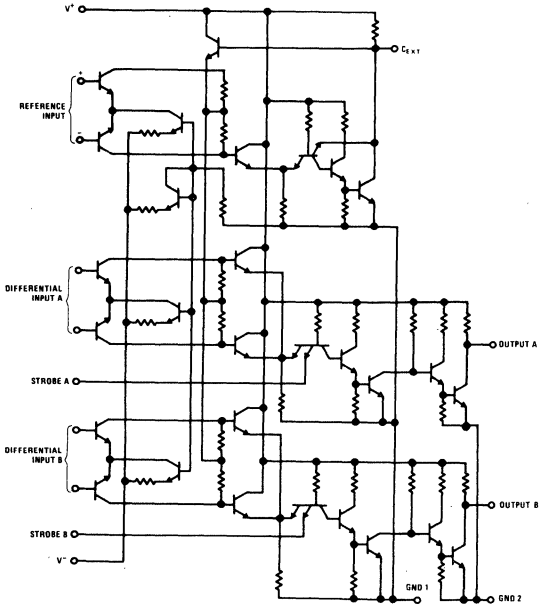
Note 2: Positive current is defined as current into the referenced pin.

Note 3: Pin 1 to have ≥ 100 pF capacitor connected to ground.

Note 4: For min V_{TH}, logic output is < 0.4V at 16 mA. For max V_{TH}, logic output is > 2.4V at $-400\mu A$.

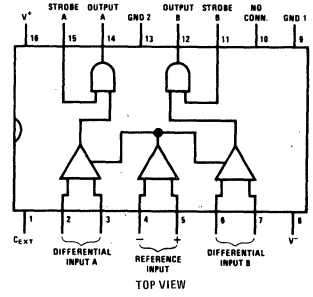
DS5524/DS7524, DS5524A/DS7524A and DS5525/DS7525

schematic diagram



connection diagram

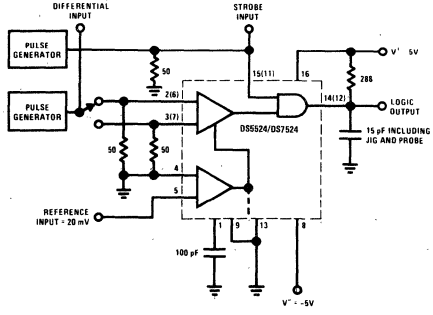
Dual-In-Line Package



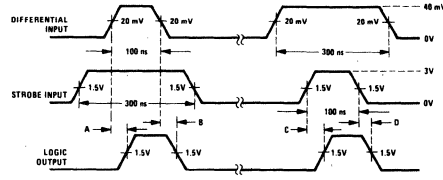
TOP VIEW

Order Number DS5524J, DS5524AJ, DS5525J, DS7524J, DS7524AJ, DS7525J, DS7524N, DS7524AN or DS7525N

AC test circuit



voltage waveforms



1. Pulse generator characteristics:
   Z_{OUT} = 50Ω, t_r = t_f = 15 ±5 ns, PRR = 1 MHz
2. Propagation delays:
   A = Differential input to logical "1" output
   B = Differential input to logical "0" output
   C = Strobe input to logical "1" output
   D = Strobe input to logical "0" output

5

DS5528/DS7528, DS5528A/DS7528A and DS5529/DS7529

electrical characteristics

DS5528/DS5528A, DS5529: The following apply for $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
DS7528/DS7528A, DS7529: The following apply for $0^{\circ}C \leq T_A \leq +70^{\circ}C$

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{TH}	Differential Input Threshold Voltage	$V_{CC} = \pm5.0V$ (Note 5)	$V_{REF} = 15$ mV	DS5528/DS7528	11	15	19	mV
				DS5528A/DS7528A	13	15	17	mV
				DS5529/DS7529	8	15	22	mV
			$V_{REF} = 40$ mV	DS5528/DS7528	36	40	44	mV
				DS5528A/DS7528A	38	40	42	mV
				DS5529/DS7529	33	40	47	mV
I_{BIAS}	Differential and Reference Input Bias Current	$V_{CC} = \pm5.25V$, $V_{IN} = 0V$		DS5528/DS5528A, DS5529		30	100	μA
				DS7528/DS7528A, DS7529		30	75	μA
I_{OS}	Differential Input Offset Current	$V_{CC} = \pm5.25V$ $V_{DIFF} = 0V$, $V_{IN} = 0V$				0.5		μA
V_{IH}	Logical "1" Input Voltage				2			V
I_{IH}	Logical "1" Input Current Strobe, Gate Inputs	$V_{CC} = \pm5.25V$	$V_{IN} = 2.4V$			5	40	μA
			$V_{IN} = 5.5V$				1	mA
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IL}	Logical "0" Input Current, Strobe, Gate Inputs	$V_{CC} = \pm5.25V$, $V_{IN} = 0.4V$				−1	−1.6	mA
V_{CD}	Input Clamp Voltage	$I_{IN} = -12$ mA					−1.5	V
V_{OH}	Logical "1" Output Voltage	$V_{CC} = \pm4.75V$, $I_O = -400\mu A$			2.4	3.9		V
I_{SC}	Output Short Circuit Current	$V_{CC} = \pm5.25V$, $V_O = 0V$			−2.1	−2.8	−3.5	mA
V_{OL}	Logical "0" Output Voltage	$V_{CC} = \pm4.75V$, $I_O = 16$ mA				0.25	0.4	V
I_{CC}^+	V^+ Supply Current	$V_{CC} = \pm5.25V$				29	40	mA
I_{CC}^-	V^- Supply Current	$V_{CC} = \pm5.25V$				−13	−18	mA

switching characteristics

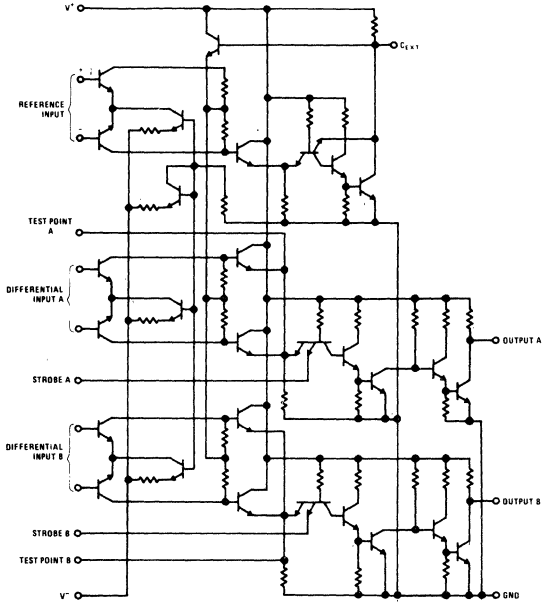
The following apply for $T_A = 25^{\circ}C$, $V^+ = 5.0V$, $V^- = -5.0V$

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Differential Input to Logical "1" Output	AC Test Circuit		20	40	ns
t_{pd1}	Strobe Input to Logical "1" Output	AC Test Circuit		10	30	ns
t_{pd0}	Differential Input to Logical "0" Output	$V_{CC} = \pm5.0V$, AC Test Circuit		28		ns
t_{pd0}	Strobe Input to Logical "0" Output	AC Test Circuit		20		ns
t_{DR}	Differential Input Overload Recovery Time			10		ns
t_{CMR}	Common-Mode Input Overload Recovery Time			5		ns
t_{CY}	Minimum Cycle Time			200		ns
V_{CM}	AC Common-Mode Input Firing Voltage	Pulse		±2.5		V

Note 1: For $0^{\circ}C \leq T_A \leq +70^{\circ}C$ operation, electrical characteristics for DS5528/DS5528A and DS5529 are guaranteed the same as DS7528/DS7528A and DS7529 respectively.
Note 2: Positive current is defined as current into the referenced pin.
Note 3: Pin 1 to have ≥ 100 pF capacitor connected to ground.
Note 4: Each test point to have ≤ 15 pF capacitive load to ground.
Note 5: For min V_{TH}, logic output is < 0.4V at 16 mA. For max V_{TH}, logic output is > 2.4V at $-400\mu A$.

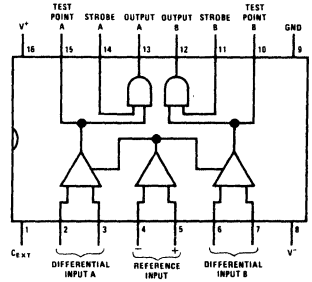
DS5528/DS7528, DS5528A/DS7528A and DS5529/DS7529

schematic diagram



connection diagram

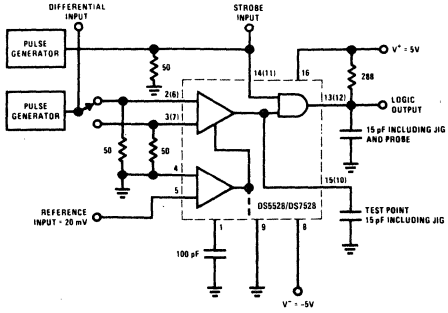
Dual-In-Line Package



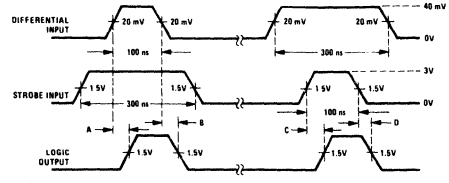
TOP VIEW

Order Number DS5528J, DS5528AJ, DS5529J, DS7528J, DS7528AJ, DS7529J, DS7528N, DS7528AN or DS7529N

AC test circuit



voltage waveforms



1. Pulse generator characteristics:
   $Z_{OUT} = 50\Omega$, $t_r = t_f = 15 \pm 5$ ns, PRR = 1 MHz
2. Propagation delays:
   A = Differential input to logical "1" output
   B = Differential input to logical "0" output
   C = Strobe input to logical "1" output
   D = Strobe input to logical "0" output

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DS5534/DS7534, DS5534A/DS7534A and DS5535/DS7535

electrical characteristics

DS5534/DS5534A, DS5535: The following apply for $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
DS7534/DS7534A, DS7535: The following apply for $0^{\circ}C \leq T_A \leq +70^{\circ}C$

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{TH}	Differential Input Threshold Voltage	$V_{CC} = \pm5.0V$ (Note 4)	$V_{REF} = 15\,mV$	DS5534/DS7534	11	15	19	mV
				DS5534A/DS7534A	13	15	17	mV
				DS5535/DS7535	8	15	22	mV
			$V_{REF} = 40\,mV$	DS5534/DS7534	36	40	44	mV
				DS5534A/DS7534A	38	40	42	mV
				DS5535/DS7535	33	40	47	mV
I_{BIAS}	Differential and Reference Input Bias Current	$V_{CC} = \pm5.25V$, $V_{IN} = 0V$		DS5534/DS5534A, DS5535		30	100	μA
				DS7534/DS7534A, DS7535		30	75	μA
I_{OS}	Differential Input Offset Current	$V_{CC} = \pm5.25V$ $V_{DIFF} = 0V$, $V_{IN} = 0V$				0.5		μA
V_{IH}	Logical "1" Input Voltage				2			V
I_{IH}	Logical "1" Input Current Strobe, Gate Inputs	$V_{CC} = \pm5.25V$	$V_{IN} = 2.4V$			5	40	μA
			$V_{IN} = 5.5V$				1	mA
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IL}	Logical "0" Input Current, Strobe, Gate Inputs	$V_{CC} = \pm5.25V$, $V_{IN} = 0.4V$				−1	−1.6	mA
V_{CD}	Input Clamp Voltage	$I_{IN} = -12\,mA$					−1.5	V
V_{OL}	Logical "0" Output Voltage	$V_{CC} = \pm4.75V$, $I_O = 16\,mA$				0.25	0.4	V
I_{CEX}	Output Leakage Current	$V_O = 5.25V$					250	μA
I_{CC+}	V^+ Supply Current	$V_{CC} = \pm5.25V$				28	38	mA
I_{CC-}	V^- Supply Current	$V_{CC} = \pm5.25V$				−13	−18	mA

switching characteristics

The following apply for $T_A = 25^{\circ}C$, $V^+ = 5.0V$, $V^- = -5.0V$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Differential Input to Logical "1" Output	AC Test Circuit		24		ns
t_{pd1}	Strobe Input to Logical "1" Output	AC Test Circuit		16		ns
t_{pd0}	Differential Input to Logical "0" Output	$V_{CC} = \pm5.0V$, AC Test Circuit		20	40	ns
t_{pd0}	Strobe Input to Logical "0" Output	AC Test Circuit		10	30	ns
t_{DR}	Differential Input Overload Recovery Time			10		ns
t_{CMR}	Common-Mode Input Overload Recovery Time			5		ns
t_{CY}	Minimum Cycle Time			200		ns
V_{CM}	AC Common-Mode Input Firing Voltage	Pulse		±2.5		V

Note 1: For $0^{\circ}C \leq T_A \leq +70^{\circ}C$ operation, electrical characteristics for DS5534/DS5534A and DS5535 are guaranteed the same as DS7534/DS7534A and DS7535, respectively.

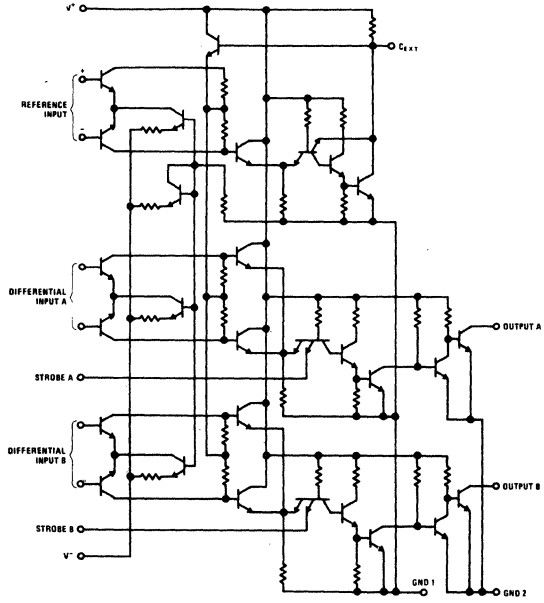
Note 2: Positive current is defined as current into the referenced pin.

Note 3: Pin 1 to have ≥ 100 pF capacitor connected to ground.

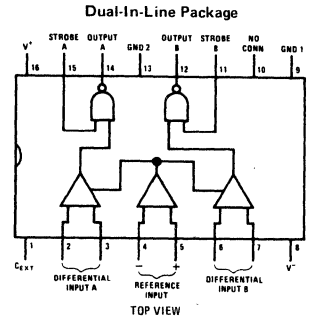
Note 4: For min V_{TH}, logic output is < 250μA at 5.25V. For max V_{TH}, logic output is < 0.4V at 20 mA.

DS5534/DS7534, DS5534A/DS7534A and DS5535/DS7535

schematic diagram

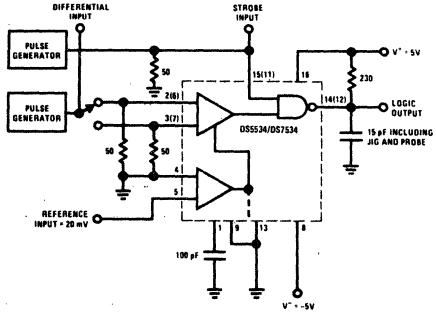


connection diagram

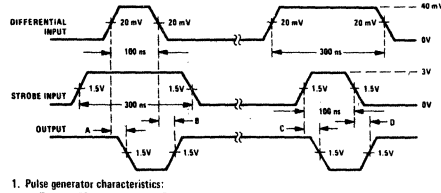


Order Number DS5534J, DS5534AJ, DS5535J, DS7534J, DS7534AJ, DS7535J, DS7534N, DS7534AN or DS7535N

AC test circuit



voltage waveforms



1. Pulse generator characteristics:
   Z_{OUT} = 50Ω, t_r = t_f = 15 ± 5 ns, PRR = 1 MHz
2. Propagation delays:
   A = Differential input to logical "0" output
   B = Differential input to logical "1" output
   C = Strobe input to logical "0" output
   D = Strobe input to logical "1" output

DS5538/DS7538, DS5538A/DS7538A and DS5539/DS7539

electrical characteristics

DS5538/DS5538A, DS5539: The following apply for $-55^{\circ}C \leq T_A \leq +125^{\circ}C$
DS7538/DS7538A, DS7539: The following apply for $0^{\circ}C \leq T_A \leq +70^{\circ}C$

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{TH}	Differential Input Threshold Voltage	$V_{CC} = \pm 5.0V$ (Note 5)	$V_{REF} = 15$ mV	DS5538/DS7538	11	15	19	mV
				DS5538A/DS7538A	13	15	17	mV
				DS5539/DS7539	8	15	22	mV
			$V_{REF} = 40$ mV	DS5538/DS7538	36	40	44	mV
				DS5538A/DS7538A	38	40	42	mV
				DS5539/DS7539	33	40	47	mV
I_{BIAS}	Differential and Reference Input Bias Current	$V_{CC} = \pm 5.25V$, $V_{IN} = 0V$		DS5538/DS5538A, DS5539		30	100	μA
				DS7538/DS7538A, DS7539		30	75	μA
I_{OS}	Differential Input Offset Current	$V_{CC} = \pm 5.25V$ $V_{DIFF} = 0V$, $V_{IN} = 0V$				0.5		μA
V_{IH}	Logical "1" Input Voltage				2			V
I_{IH}	Logical "1" Input Current Strobe, Gate Inputs	$V_{CC} = \pm 5.25V$	$V_{IN} = 2.4V$			5	40	μA
			$V_{IN} = 5.5V$				1	mA
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IL}	Logical "0" Input Current, Strobe, Gate Inputs	$V_{CC} = \pm 5.25V$, $V_{IN} = 0.4V$				-1	-1.6	mA
V_{CD}	Input Clamp Voltage	$I_{IN} = -12$ mA					-1.5	V
V_{OL}	Logical "0" Output Voltage	$V_{CC} = \pm 4.75V$, $I_O = 16$ mA				0.25	0.4	V
I_{CEX}	Output Leakage Current	$V_O = 5.25V$					250	μA
I_{CC+}	V^+ Supply Current	$V_{CC} = \pm 5.25V$				28	38	mA
I_{CC-}	V^- Supply Current	$V_{CC} = \pm 5.25V$				-13	-18	mA

switching characteristics

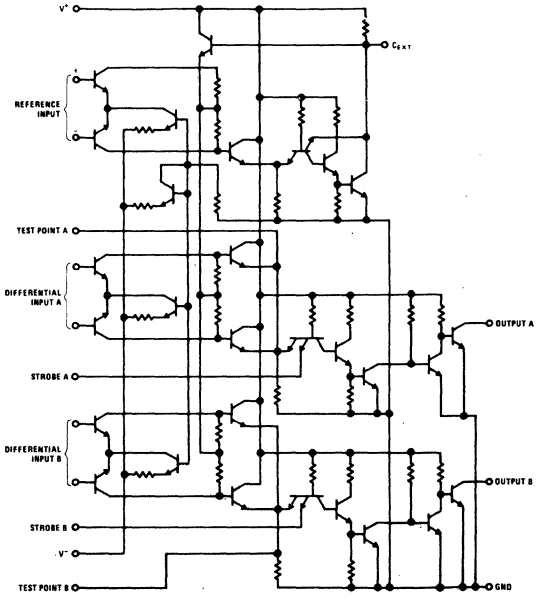
The following apply for $T_A = 25^{\circ}C$, $V^+ = 5.0V$, $V^- = -5.0V$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}	Differential Input to Logical "1" Output	AC Test Circuit		24		ns
t_{pd1}	Strobe Input to Logical "1" Output	AC Test Circuit		16		ns
t_{pd0}	Differential Input to Logical "0" Output	$V_{CC} = \pm 5.0V$, AC Test Circuit		20	40	ns
t_{pd0}	Strobe Input to Logical "0" Output	AC Test Circuit		10	30	ns
t_{DR}	Differential Input Overload Recovery Time			10		ns
t_{CMR}	Common-Mode Input Overload Recovery Time			5		ns
t_{CY}	Minimum Cycle Time			200		ns
V_{CM}	AC Common-Mode Input Firing Voltage	Pulse		± 2.5		V

Note 1: For $0^{\circ}C \leq T_A \leq +70^{\circ}C$ operation, electrical characteristics for DS5538/DS5538A and DS5539 are guaranteed the same as DS7538/DS7538A and DS7539 respectively.
Note 2: Positive current is defined as current into the referenced pin.
Note 3: Pin 1 to have ≥ 100 pF capacitor connected to ground.
Note 4: Each test point to have ≤ 15 pF capacitive load to ground.
Note 5: For min V_{TH}, logic output is $< 250\mu A$ at 5.25V. For max V_{TH}, logic output is $< 0.4V$ at 20 mA.

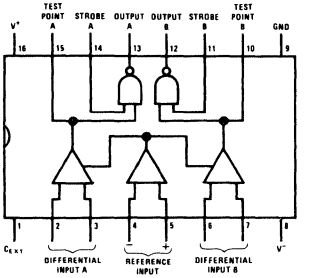
DS5538/DS7538, DS5538A/DS7538A and DS5539/DS7539

schematic diagram



connection diagram

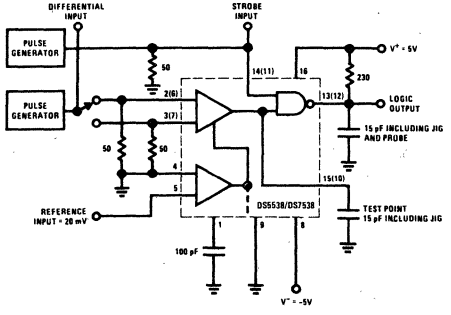
Dual-In-Line Package



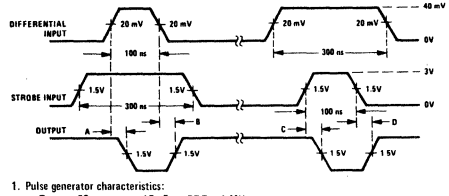
TOP VIEW

Order Number DS5538J, DS5538AJ, DS5539J, DS7538J, DS7538AJ, DS7539J, DS7538N, DS7538AN or DS7539N

AC test circuit



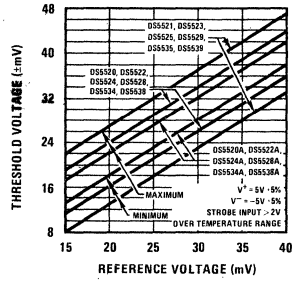
voltage waveforms



1. Pulse generator characteristics:
   $Z_{OUT} = 50\Omega$, $t_r = t_f = 15 \pm 5$ ns, PRR = 1 MHz
2. Propagation delays:
   A = Differential input to logical "0" output
   B = Differential input to logical "1" output
   C = Strobe input to logical "0" output
   D = Strobe input to logical "1" output

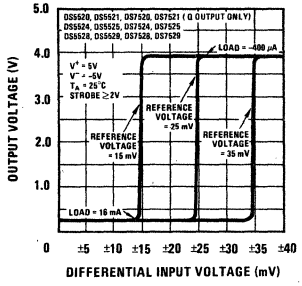
guaranteed performance characteristics

Differential Input Threshold Voltage

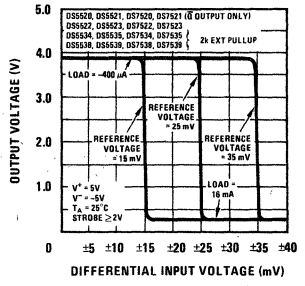


typical performance characteristics

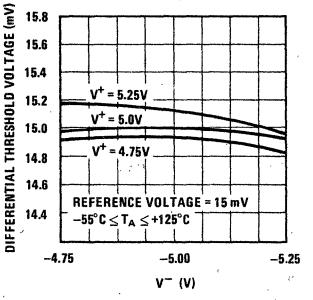
Transfer Characteristics



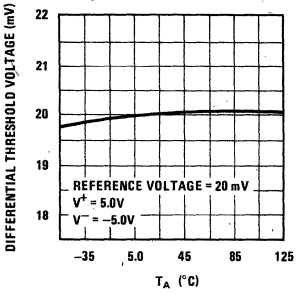
Transfer Characteristics



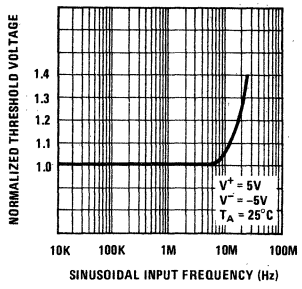
Power Supply Rejection



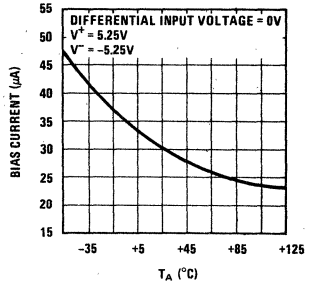
Temperature Coefficient



Differential Input Frequency Response

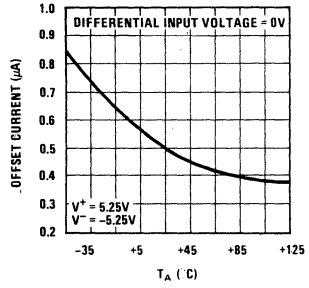


Differential Input Bias Current

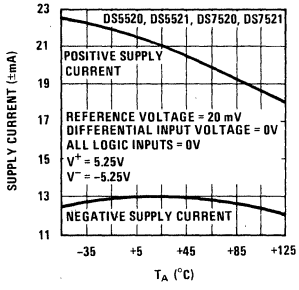


typical performance characteristics (cont.)

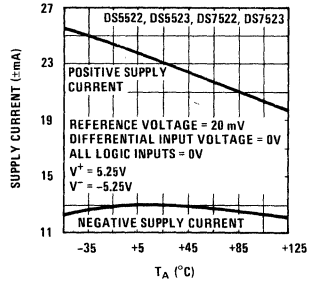
Differential Input Offset Current



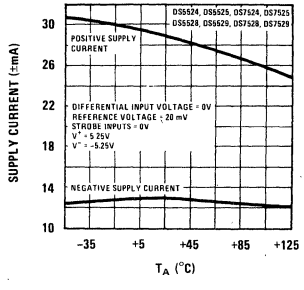
Power Supply Currents



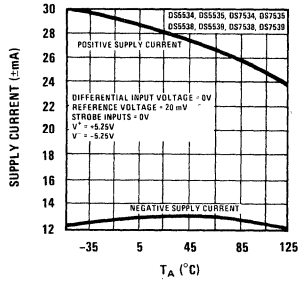
Power Supply Currents



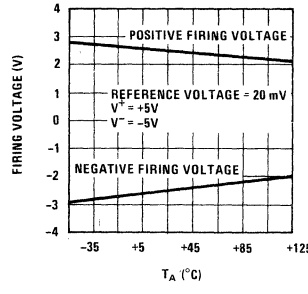
Power Supply Currents



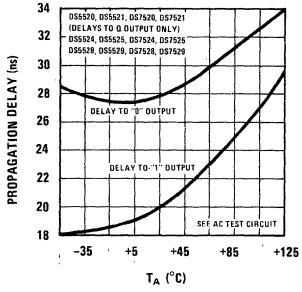
Power Supply Currents



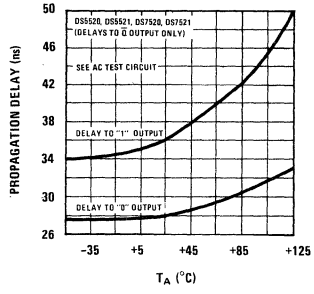
AC Common-Mode Firing Voltage



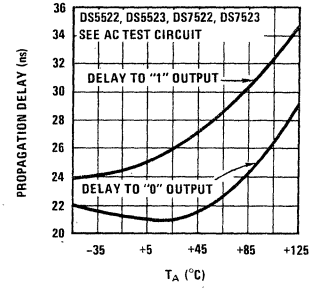
Differential Input to Output Propagation Delays



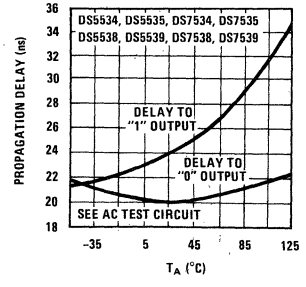
Differential Input to Output Propagation Delays



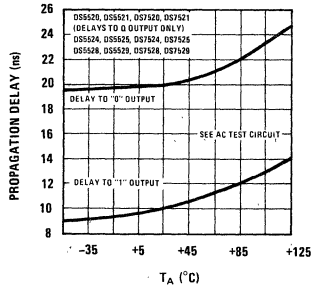
Differential Input to Output Propagation Delays



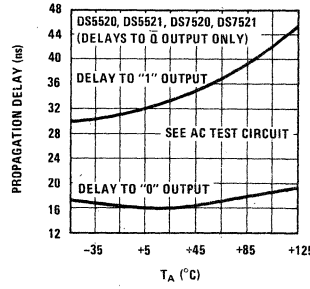
Differential Input to Output Propagation Delays



Strobe to Output Propagation Delays



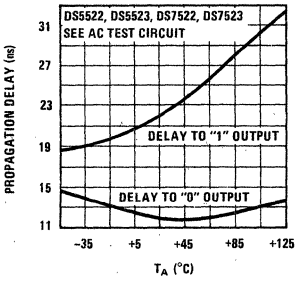
Strobe to Output Propagation Delays



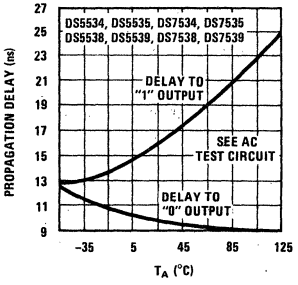
5

typical performance characteristics (cont.)

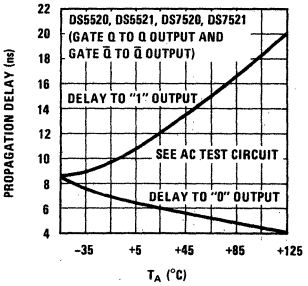
Strobe to Output Propagation Delays



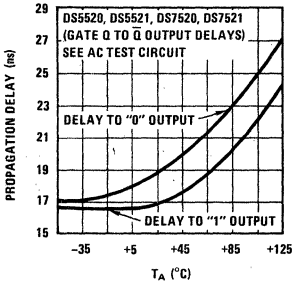
Strobe to Output Propagation Delays



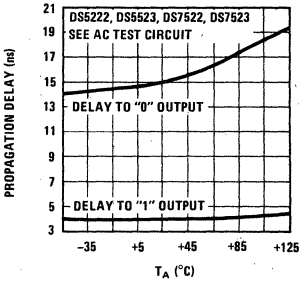
Gate to Output Propagation Delays



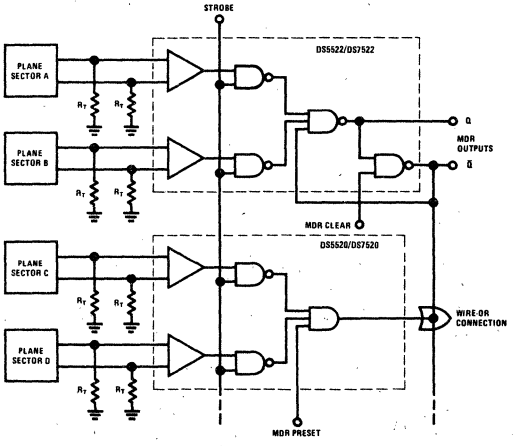
Gate to Output Propagation Delays



Gate to Output Propagation Delays

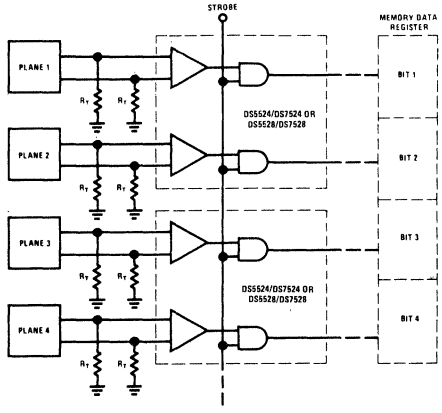


typical applications

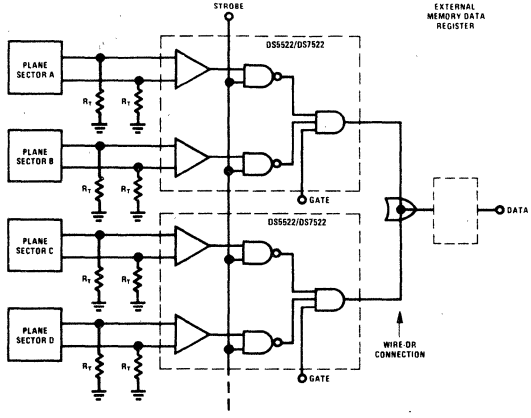


Large Memory System with Sectored Core Planes

typical applications (cont.)



Small Memory System



Large Memory System

NATIONAL

Sense Amplifiers

DS7802/DS8802, DS7806/DS8806
high speed MOS to TTL level converters

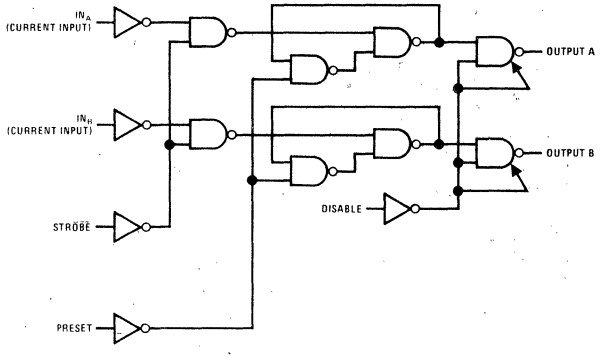
general description

The DS7802/DS8802, DS7806/DS8806 are high speed MOS to TTL level converters. These circuits act as an interface level converter between MOS and TTL logic devices. It consists of two 1-input converters with common strobe input to inhibit "0" entry when strobe is high. It allows parallel entry when strobe is low and the internal latch is preset by the common preset input. TRI-STATE® output logic is implemented in this circuit to facilitate high speed time sharing of decoder-drivers, fast random-access (or sequential) memory arrays, etc.

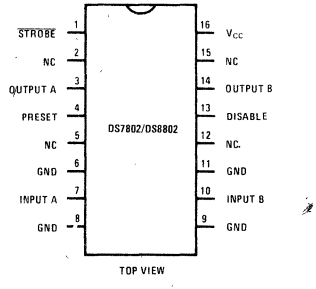
features

- Very low output impedance — high drive ability
- High impedance output state which allows many outputs to be connected to a common bus line
- Average power dissipation 110 mW per converter

logic and connection diagrams

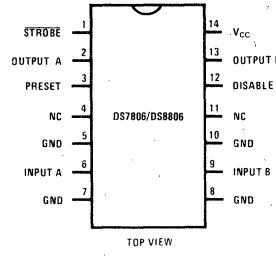


Dual-In-Line Package



Order Number DS7802J, DS8802J or DS8802N

Dual-In-Line and Flat Package



Order Number DS7806J, DS8806J, DS8806N or DS7806W

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7802, DS7806	4.5	5.5	V
DS8802, DS8806	4.75	5.25	V
Temperature (T_A)			
DS7802, DS7806	−55	+125	°C
DS8802, DS8806	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
I_{INA}, I_{INB}	Logical "1" Input Current	V_{CC} = Min		500			μA
I_{INA}, I_{INB}	Logical "0" Input Current	V_{CC} = Min				200	μA
V_{IH}	Logical "1" Input Voltage	Strobe, Preset, Disable, V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	Strobe, Preset, Disable, V_{CC} = Min				0.8	V
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −1.5 mA		2.4			V
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 16 mA				0.4	V
I_O	TRI-STATE Output Current	V_{CC} = Max	V_O = 2.4V			40	μA
			V_O = 0.4V			−40	μA
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V			40	μA
			V_{IN} = 5.5V			1.0	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max, $V_{IN(DISABLE)}$ = 2V, Other Inputs = ϕV				40	mA
V_{CD}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −12 mA				−1.5	V
I_{SC}	Output Short Circuit Current	V_{CC} = Max, V_O = 0V, (Note 4)	DS7802, DS7806	−20		−70	mA
			DS8802, DS8806	−18		−70	mA

switching characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{ds}	Propagation Delay to a Logical "0" From Strobe to Output	V_{CC} = 5.0V (See Waveforms), T_A = 25°C		17	25	ns
t_{dp}	Propagation Delay to a Logical "1" From Preset to Output	V_{CC} = 5.0V (See Waveforms), T_A = 25°C		22	32	ns
t_{1H}	Delay From Disable Input to High Impedance State (From Logical "1" Level)	V_{CC} = 5.0V (See ac Test Circuit), T_A = 25°C		7.0	11	ns
t_{0H}	Delay From Disable Input to High Impedance State (From Logical "0" Level)	V_{CC} = 5.0V (See ac Test Circuit), T_A = 25°C		17	25	ns
t_{H1}	Delay From Disable Input to Logical "1" Level (From High Impedance State)	V_{CC} = 5.0V (See ac Test Circuit), T_A = 25°C		9.0	14	ns
t_{H0}	Delay From Disable Input to Logical "0" Level (From High Impedance State)	V_{CC} = 5.0V (See ac Test Circuit), T_A = 25°C		13.5	16	ns

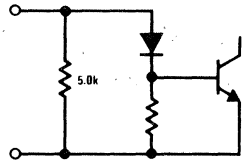
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7802, DS7806 and across the 0°C to +70°C range for the DS8802, DS8806. All typicals are given for V_{CC} = 5.0V, T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

typical input circuit

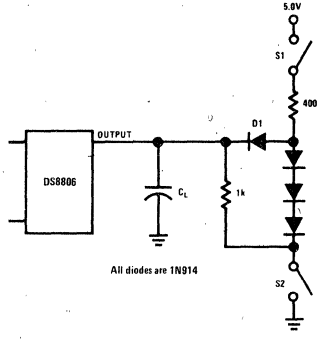


truth table

IN A OR B	ST	P	D	Q_A OR Q_B
0	1	1	0	1
1	1	1	0	1
0	0	1	0	0
1	0	1	0	1
X	X	X	1	Hi-Z

X = Don't care

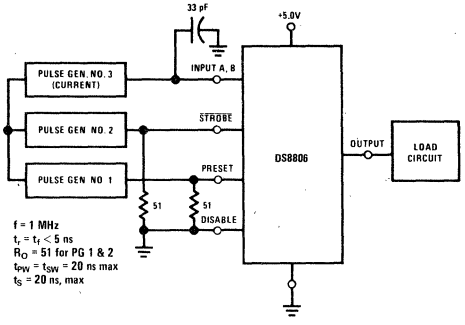
ac test circuits



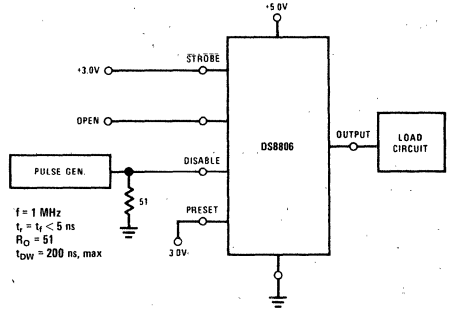
	SWITCH S_1	SWITCH S_2	C_L
t_{dp}	Closed	Closed	50 pF
t_{ds}	Closed	Closed	50 pF
t_{0H}	Closed	Closed	*5 pF
t_{1H}	Closed	Closed	*5 pF
t_{H0}	Closed	Open	50 pF
t_{H1}	Open	Closed	50 pF

*Jig capacitance

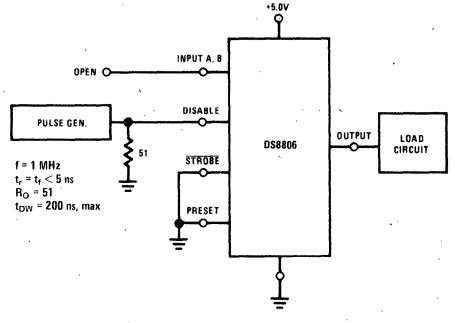
(a)



(b)



(c)

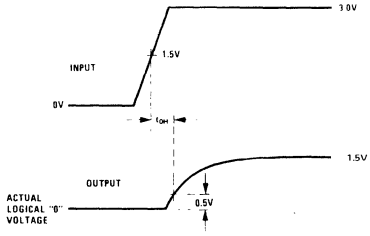


(d)

Test Circuit 20

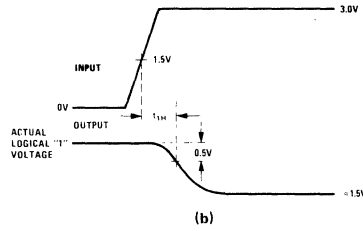
switching time waveforms

t_{0H}



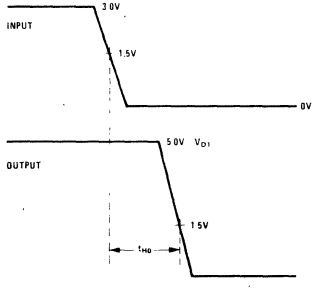
(a)

t_{1H}



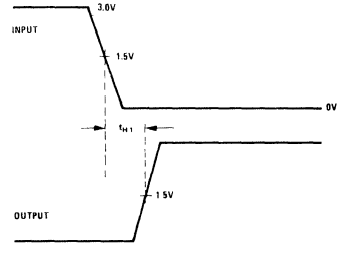
(b)

t_{H0}

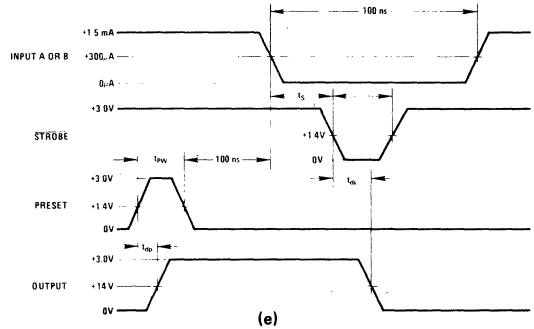


(c)

t_{H1}



(d)



(e)

NATIONAL

Display Drivers

DM5441A/DM7441A
BCD to decimal decoder/nixie* driver

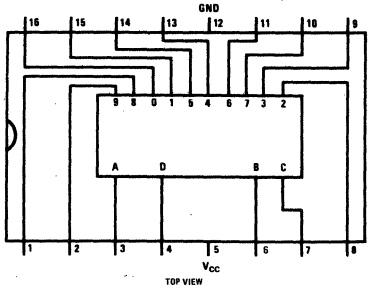
general description

The DM5441A/DM7441A is monolithic binary-coded-decimal to decimal decoder. The BCD number to be decoded is applied to the four input lines; and the unique output corresponding to the decimal equivalent of the input number falls to a logical 0 level. Outputs are designed to drive gas-filled-readout (Nixie*) tubes but are also able to operate with other low current lamps and relays.

An over-range feature provides that if binary numbers between 10 and 15 are applied to the input the least significant bit of these numbers (0 through 5) will be decoded on the output.

connection diagram

Dual-In-Line and Flat Package



Order Number DM5441AJ or DM7441AJ

Order Number DM7441N

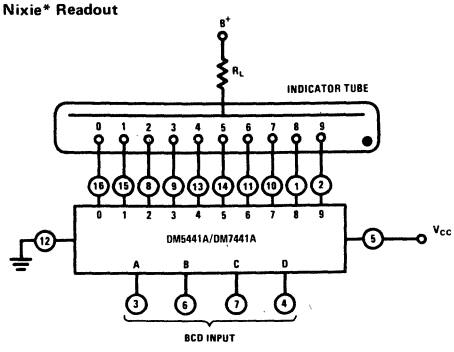
Order Number DM5441AW

logic table

INPUT D	C	B	A	LOW OUTPUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
(OVER-RANGE)				
1	0	1	0	0
1	0	1	1	1
1	1	0	0	2
1	1	0	1	3
1	1	1	0	4
1	1	1	1	5

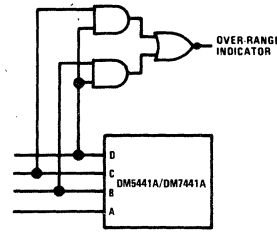
typical applications

Nixie* Readout



Note: Values for B+ and R_L are as specified by the tube manufacturer.

Over-Range Decoding



*Trademark of Burroughs Corporation

6

absolute maximum ratings (Note 1)

Supply Voltage (V_{CC})	7.0V
Output Voltage	70V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM5441A	4.5	5.5	V
DM7441A	4.75	5.25	V
Temperature (T_A)			
DM5441A	−55	+125	°C
DM7441A	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V, All Inputs		3	40	μA
			V_{IN} = 5.5V			1	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1.0	−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max, V_{IN} = 0.0V			21	36	mA
V_{OH}	Logical "1" Output Breakdown Voltage	V_{CC} = Max, I_{OUT} = 1.0 mA		70	85		V
I_{OH}	Logical "1" Output Current	V_{CC} = Max, V_{OUT} = 50V	T_A = +125°C			60	μA
			T_A = +70°C			40	μA
			T_A = +25°C			1.8	μA
			T_A = 0°C			1.8	μA
			T_A = −55°C			1.8	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 7 mA	T_A = +125°C			3.0	V
			T_A = +70°C			2.5	V
			T_A = +25°C		1.4	2.5	V
			T_A = 0°C			2.5	V
			T_A = −55°C			2.5	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS5441A and across the 0°C to +70°C range for the DM7441A. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

NATIONAL

Display Drivers

DM5446A/DM7446A, DM5447A/DM7447A, DM5448/DM7448 BCD-to-7-segment decoder/drivers

general description

This versatile series of 7-segment display drivers fulfills a wide variety of requirements for most active high (common cathode) and active low (common anode) Light Emitting Diodes (LED) or lamp displays. Each device fully decodes a 4-bit BCD input into a number from 0 through 9 in the standard 7-segment display format, and BCD numbers above 9 into unique patterns that verify operation. All circuits operate from a single 5.0V supply.

The DM5446A/DM7446A has active-low, open-collector outputs that will drive segments requiring up to 40 mA of current. The outputs are capable of withstanding 30V at a maximum leakage current of 250μA. This configuration is particularly well suited for common anode LED displays or higher voltage lamp displays. The high sink current capability also allows this circuit to be used in the multiplex or nonmultiplex mode of display drive. In addition, the device may be used to drive logic circuits since its normalized fanout is 25.

The DM5447A/DM7447A has the same output characteristics as the DM5446A/DM7446A except that the outputs withstand 15V at a maximum leakage current of 250μA. Since its output configuration is the same as the DM5446A/DM7446A its applications will also be the same, the only restriction is that a lower voltage type display be used because of the reduced output voltage limit of 15V.

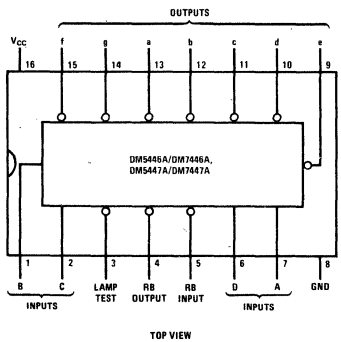
The DM5448/DM7448 has active-high, passive-pull up outputs with a fanout of 4. Typical source current is 2.0 mA at an output voltage of 0.85V. The sink capability is 6.4 mA at a maximum voltage of 0.4V. It is normally used to drive logic circuits, operate high-voltage loads such as electro-luminescent displays through buffer transistors or SCR switches, and in low current common cathode Non-Multiplex LED applications.

features

- Lamp-test input
- Leading/trailing zero suppression (RBI and RBO)
- Blanking input that may be used to modulate lamp intensity or inhibit output
- TTL and DTL compatible
- Input clamping diodes

connection diagrams

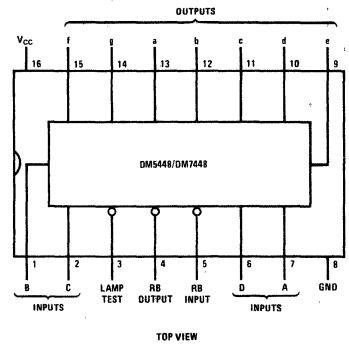
Dual-In-Line and Flat Package



TOP VIEW

Order Number DM5446AJ, DM7446AJ, DM5447AJ, DM7447AJ, DM5448J, or DM7448J

Dual-In-Line and Flat Package



TOP VIEW

Order Number DM5446AN, DM7446AN, DM5447AN, DM7447AN, DM5448N, or DM7448N

Order Number DM5446AW, DM7446AW, DM5447AW, DM7447AW, DM5448W or DM7448W

6

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DM5446A, DM5447A, DM5448	4.5	5.5	V
DM7446A, DM7447, DM7448	4.75	5.25	V
Temperature (T_A)			
DM5446A, DM5447A, DM5448	−55	+125	°C
DM7446A, DM7447A, DM7448	0	+70	°C
Output Voltage			
DM5446A, DM7446A		30	V
DM5447A, DM7447A		15	V
DM5448, DM7448		5.5	V
Output Sink Current (per segment)			
DM5446A, DM7446A,		40	mA
DM5447A, DM7447A		40	mA
DM5448, DM7448		6.4	mA

electrical characteristics (Note 2) The following is applicable to all parts.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −200μA, BI/RBO Node		2.4	3.7		V
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{IN} = 8.0 mA, BI/RBO Node			0.3	0.4	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max Any Input Except BI/RBO Node	V_{IN} = 2.4V			40	μA
			V_{IN} = 5.5V			1.0	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V	Except BI/RBO Node			−1.6	mA
			BI/RBO Node			−4.2	mA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, BI/RBO Node				−4.0	mA
V_{CD}	Input Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA				−1.5	V

output characteristics and supply current

DM5446A/DM7446A, DM5447A/DM7447A (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{OH}	Logical "1" Output Voltage Outputs a through g	V_{CC} = Max, I_{OUT} = 250μA	DM5446A/DM7446A	30			V
			DM5447A/DM7447A	15			V
V_{OL}	Logical "0" Output Voltage Outputs a through g	V_{CC} = Min, I_{OUT} = 40 mA			0.3	0.4	V
I_{CC}	Supply Current	V_{CC} = Max	DM5446A, DM5447A		60	85	mA
			DM7446A, DM7447A		60	103	mA

output characteristics and supply current

DM5448/DM7448 (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{OH}	Logical "1" Output Voltage Outputs a through g	V_{CC} = Min, I_{OUT} = −400μA		2.4	3.2		V
V_{OL}	Logical "0" Output Voltage Outputs a through g	V_{CC} = Min, I_{OUT} = 6.4 mA			0.25	0.4	V
I_{OL}	Logical "1" Load Current Available, Outputs a through g	V_{CC} = Min, V_{OUT} = 0.85V		−1.3	−2.0		mA
I_{SC}	Output Short Circuit Current Outputs a through g	V_{CC} = Max, (Note 3)			−3.0	−4.0	mA
I_{CC}	Supply Current	V_{CC} = Max	DM5448		50	76	mA
			DM7448		50	90	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for DM5446A, DM5447A and DM5448, and across the 0°C to +70°C range for DM7446A, DM7447A and DM7448. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

switching characteristics

DM5446A/DM7446A, DM5447A/DM7447A, DM5448/DM7448 (V_{CC} = 5.0V, T_A = 25°C)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0"	C_L = 15 pF	R_L = 120Ω	DM5446A/DM7446A			100	ns
				DM5447A/DM7447A			100	ns
			R_L = 1 kΩ, DM5448				100	ns
			R_L = 667Ω, DM7448				100	ns
t_{pd1}	Propagation Delay to a Logical "1"	C_L = 15 pF	R_L = 120Ω	DM5446A/DM7446A			100	ns
				DM5447A/DM7447A			100	ns
			R_L = 1 kΩ, DM5448				100	ns
			R_L = 667Ω, DM7448				100	ns

truth tables

DM5446A/DM7446A, DM5447A/DM7447A

DECIMAL OR FUNCTION	INPUTS LT	RBI	D	C	B	A	BI/RBO	OUTPUTS a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	0	0	0	0	0	0	1	1
1	1	X	0	0	0	1	1	1	0	0	1	1	1	1	1
2	1	X	0	0	1	0	1	0	0	1	0	0	1	0	
3	1	X	0	0	1	1	1	0	0	0	0	1	1	0	
4	1	X	0	1	0	0	1	1	0	0	1	1	0	0	
5	1	X	0	1	0	1	1	0	1	0	0	1	0	0	
6	1	X	0	1	1	0	1	1	1	0	0	0	0	0	
7	1	X	0	1	1	1	1	0	0	0	1	1	1	1	
8	1	X	1	0	0	0	1	0	0	0	0	0	0	0	
9	1	X	1	0	0	1	1	0	0	0	1	1	0	0	
10	1	X	1	0	1	0	1	1	1	1	0	0	1	0	
11	1	X	1	0	1	1	1	1	1	0	0	1	1	0	
12	1	X	1	1	0	0	1	1	0	1	1	1	0	0	
13	1	X	1	1	0	1	1	0	1	1	0	1	0	0	
14	1	X	1	1	1	0	1	1	1	1	0	0	0	0	
15	1	X	1	1	1	1	1	1	1	1	1	1	1	1	
BI	X	X	X	X	X	X	0	1	1	1	1	1	1	1	2
RBI	1	0	0	0	0	0	0	1	1	1	1	1	1	1	3
LT	0	X	X	X	X	X	1	0	0	0	0	0	0	0	4

Note 1: BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input (BI) must be open or held at a logic "1" when output functions 0–15 are desired, and the ripple-blanking input (RBI) must be open or at a logical "1" if blanking of a decimal 0 is not desired. X = input may be high or low.

Note 2: When a logical "0" is applied directly to the blanking input (forced condition) all segment outputs go to a logical "1" regardless of the state of any other input condition.

Note 3: When the ripple-blanking input (RBI) and inputs A, B, C and D are at logical "0", with the lamp test input at logical "1," all segment outputs go to a logical "1" and the ripple-blanking output (RBO) goes to a logical "0" (response condition).

Note 4: When the blanking input/ripple-blanking output (BI/RBO) is open or held at a logical "1," and a logical "0" is applied to the lamp-test input, all segment outputs go to a logical "0."

DM5448/DM7448

DECIMAL OR FUNCTION	INPUTS LT	RBI	D	C	B	A	BI/RBO	OUTPUTS a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	1	X	0	0	0	1	1	0	1	1	0	0	0	0	1
2	1	X	0	0	1	0	1	1	1	0	1	1	0	1	
3	1	X	0	0	1	1	1	1	1	1	1	0	0	1	
4	1	X	0	1	0	0	1	0	1	1	0	0	1	1	
5	1	X	0	1	0	1	1	1	0	1	1	0	1	1	
6	1	X	0	1	1	0	1	0	0	1	1	1	1	1	
7	1	X	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	X	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	X	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	X	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	X	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	X	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	X	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	X	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	X	1	1	1	1	1	0	0	0	0	0	0	0	
BI	X	X	X	X	X	X	0	0	0	0	0	0	0	0	2
RBI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	3
LT	0	X	X	X	X	X	1	1	1	1	1	1	1	1	4

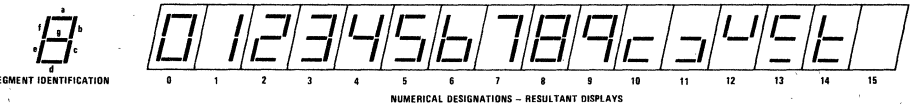
Note 1: BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input (BI) must be open or held at a logical "1" when output functions 0–15 are desired, and the ripple-blanking input (RBI) must be open or at a logical "1" if blanking of a decimal 0 is not desired. X = input may be high or low.

Note 2: When a logical "0" is applied directly to the blanking input (forced condition) all segment outputs go to a logical "0" regardless of the state of any other input condition.

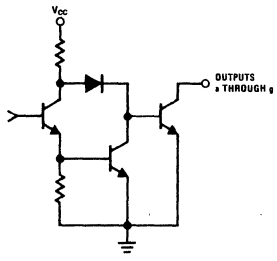
Note 3: When the ripple-blanking input (RBI) and inputs A, B, C and D are at logical "0," with the lamp test at logical "1" all segment outputs go to the logical "0" and the ripple blanking output (RBO) goes to a logical "0" (response condition).

Note 4: When the blanking input/ripple-blanking output (RI/RBO) is open or held at a logical "1," and a logical "0" is applied to the lamp-test input, all segment outputs go to a logical "1."

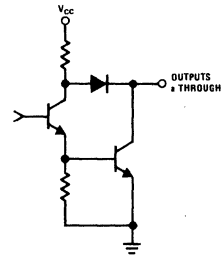
output display



output stage schematics

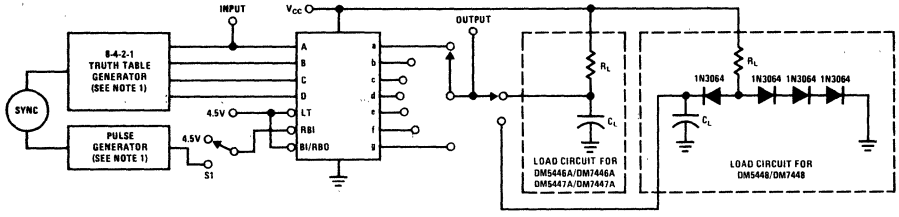


DM5446A/DM7446A
DM5447A/DM7447A

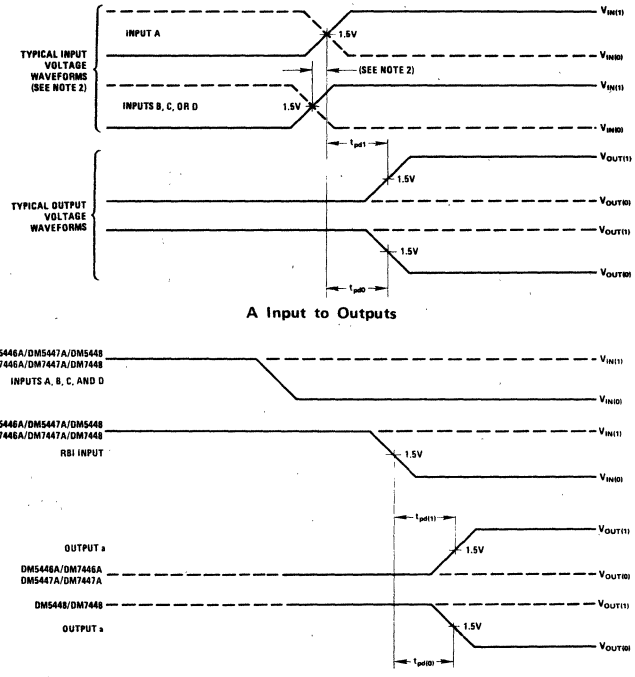


DM5448/DM7448

ac test circuit



switching time waveforms



A Input to Outputs

RBI Input to Outputs

Note 1: The truth table generator and pulse generator have the following characteristics: $V_{OUT(1)} \geq 2.4V$, $V_{OUT(0)} \leq 0.4V$, t_r and $t_f \leq 10$ ns, and PRR = 1.0 MHz.

Note 2: Inputs B, C, and D transitions occur simultaneously with or prior to input A transitions. RBI = 4.5V.

Note 3: C_L includes probe and jig capacitance.

NATIONAL

Display Drivers

DM54141/DM74141
BCD to decimal decoder/driver

general description

The DM54141/DM74141 is a second-generation BCD to decimal decoder designed specifically to drive cold cathode indicator tubes. This decoder demonstrates an improved capability to minimize switching transients in order to maintain a stable display.

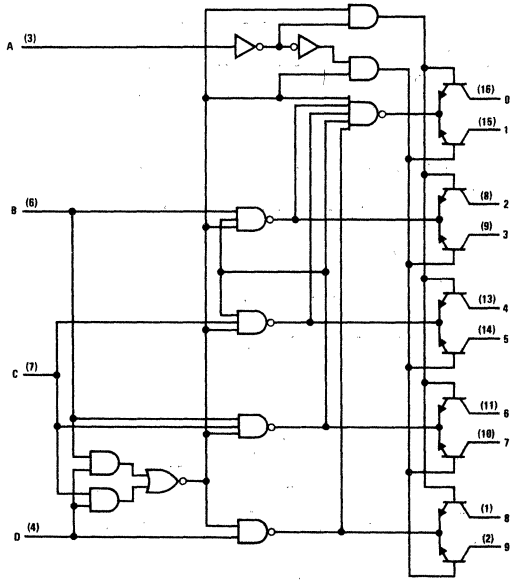
Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore the DM54141/DM74141, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing-edge zeros in a display as shown in the typical application data. The ten high-performance NPN output transistors have a maximum reverse current of 50μA at 55V.

Low-forward-impedance diodes are also provided for each input to clamp negative-voltage transitions in order to minimize transmission-line effects. Power dissipation is typically 55 mW, which is about one-half the power requirement of earlier designs.

features

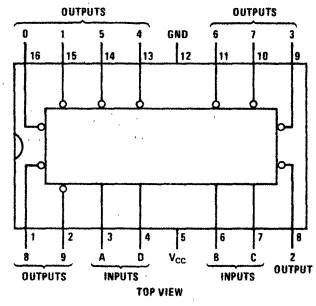
- Drives cold cathode numeric indicator tubes directly
- 50μA max leakage current at 55V
- Low power dissipation of 55 mW typ
- Fully decoded inputs ensure all outputs off for invalid codes
- Input clamp diodes for minimizing transmission line effects

logic diagram



connection diagram

Dual-In-Line and Flat Package



Order Number DM54141J or DM74141J

Order Number DM74141N

Order Number DM54141W or DM74141W

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	60V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DM74141	4.75	5.25	V
DM54141	4.5	5.5	V
Temperature, T_A			
DM74141	0	+70	°C
DM54141	−55	+125	°C

electrical characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min			2.0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IH} = 5.5V				0.1	mA
			V_{IH} = 2.4V	A Input			40	μA
				B, C, or D Input			80	μA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min					0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IL} = 0.4V		A Input			−1.6	mA
				B, C, or D Input			−3.2	mA
V_{CD}	Input Clamp Voltage	V_{CC} = Min, I_{CD} = −12 mA					−1.5	V
V_{OH}	Logical "1" Output Voltage	V_{CC} = Max, I_{OH} = 0.5 mA			60			V
I_{OH}	Logical "1" Output Current	V_{CC} = Max	V_O = 55V				50	μA
			V_O = 30V Input States 10–15				5.0	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OL} = 7.0 mA					2.5	V
I_{CC}	Supply Current	V_{CC} = Max, All Inputs Gnd, All Outputs Open				11	25	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54141 and across the 0°C to +70°C range for the DM74141. All typicals are given for V_{CC} = 5.0V and T_A = +25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

truth table

INPUT D	C	B	A	OUTPUT ON†
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	NONE
H	L	H	H	NONE
H	H	L	L	NONE
H	H	L	H	NONE
H	H	H	L	NONE
H	H	H	H	NONE

H = high level, L = low level

†All other outputs are off

NATIONAL

Display Drivers

DS8650 low voltage 4-digit LED driver

general description

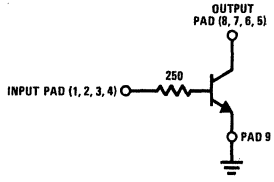
The DS8650 is a 4-digit LED display driver designed specifically for electronic watches. Its inputs interface directly with CMOS watch circuits such as the MM5829, and its outputs sink typically 75 mA from a common cathode LED watch display.

The DS8650 is supplied in dice form. Plastic DIP parts are available for device evaluation.

features

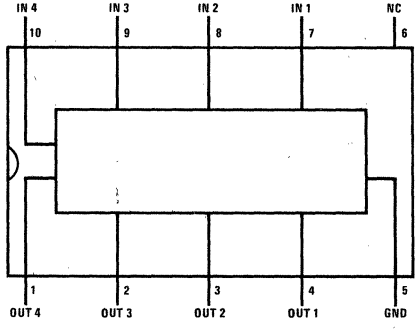
- Direct interface with CMOS watch circuits
- Grouped inputs and outputs
- Low voltage operation
- Packaged devices available for evaluation

schematic diagram

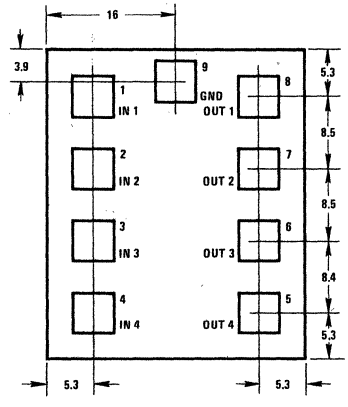


connection diagram and chip pad layout

Dual-In-Line Package



Order Number DS8650N
or DS8650 Dice



Note 1: All dimensions in millinches.
Note 2: Die size 33 mils x 36 mils.
Note 3: Pads 4.0 mils square clear area.

absolute maximum ratings

Applied Voltage V_{IN} = 1.5V
V_{OUT} = 5V

electrical characteristics (Note 1)

$2.7V \leq V_{CC} \leq 2.9V$; $-5°C \leq T_A \leq +70°C$, unless otherwise specified.

PARAMETER		CONDITION	MIN	TYP	MAX	UNITS
I_{IH}	Input "ON" Current	V_{IN} = 1.1V, I_{OUT} = 42 mA	0.84	1.4		mA
I_{IL}	Input "OFF" Current	V_{IN} = 0.2V, V_{OUT} = 5.0V		−0.01	−20	μA
V_{OL}	Output "ON" Voltage	I_{OL} = 42 mA, I_{IN} = 840μA, V_{CC} = 2.4V			0.40	V
		I_{OL} = 63 mA, I_{IN} = 1.3 mA, V_{CC} = 2.7V			0.55	V
I_{CEX}	Output Leakage Current (4 Outputs Tied Together)	V_{IN} = 0.2V, V_{OUT} = 5.0V		0.07	1.0	μA
I_{OL}	Output Sink Current	V_{OL} = 0.55V, I_{IN} = 1.3 mA	63	75		mA

Note 1: All references to V_{CC} apply on a system basis since the DS8650 has no V_{CC} connection.

NATIONAL

DS8651, DS8659 low voltage seven-segment LED drivers

general description

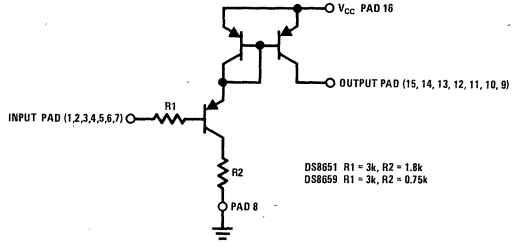
The DS8651 and DS8659 are seven segment LED display drivers specifically designed for electronic watches. Their inputs interface directly with CMOS watch circuits such as the MM5829, and their outputs provide a constant current drive for common cathode LED watch displays. Output current drive from the DS8651 is 6.5 mA typical per segment and the DS8659 provides 10 mA typically, thus no external resistors are needed.

Both circuits are supplied in dice form. Plastic DIP parts are available for device evaluation.

features

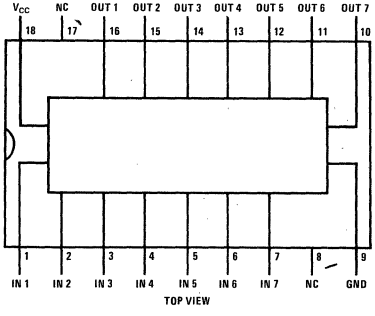
- Direct interface with CMOS watch circuit
- Internally set constant current drive
- Grouped inputs and outputs
- Packaged devices available for evaluation
- Low voltage operation

schematic diagram

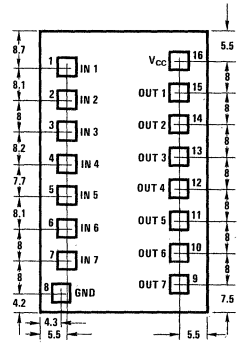


connection diagram and chip pad layout

Dual-In-Line Package



Order Number DS8651N
or DS8659N



Note 1: All dimensions in millinches.
Note 2: Die size 51 mils x 69 mils.
Note 3: Pads 4.5 mils square clear typically.

absolute maximum ratings (Note 1)

Maximum Applied Voltage	V_{CC} = 5V
Minimum Applied Voltage	V_{CC} = −0.3V

electrical characteristics (Notes 2 and 3)

2.4V ≤ V_{CC} ≤ 2.9V; −5°C ≤ T_A ≤ +70°C, unless otherwise specified.

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
I_{IH}	Input Current	V_{IN} = 0.8V, V_{CC} = 2.7V		DS8651		−150	−300	μA
				DS8659		−150	−300	μA
I_{IL}	Input "OFF" Current	V_{IN} = V_{CC} − 0.2V					−200	nA
I_{CEX}	Output "OFF" Current	V_{IN} = 2.9V, V_{CC} = 3.5V, V_{OUT} = 1.3V				0.06	2	μA
I_{OH}	Output "ON" Current	V_{IN} = 0.8	V_{CC} = 2.9, V_{OUT} = 2.3	DS8651			−10	mA
			V_{CC} = 2.7, V_{OUT} = 2.2		−5	−6.5	−8	mA
		V_{IN} = 0.5, V_{CC} = 2.4, V_{OUT} = 2.15			−3.5			mA
		V_{IN} = 0.5, V_{OUT} = 2.15	V_{CC} = 2.7	DS8659	−7	−10		mA
			V_{CC} = 2.4		−4.5			mA
I_{CC}	Supply Current	V_{CC} = 2.7V, V_{IN} = 0.5V, V_{OUT} = 2.15V, One Input-Output Pair "ON" at a Time		DS8659		12	15	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −5°C to +70°C range for the DS8651/DS8659. All typical values are for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

NATIONAL

DS8654 8 output buffer
DS8655 12 output decoder/driver and oscillator
DS8656 diode matrix

system description

The DS8654, DS8655 and DS8656 are specifically designed to operate a thermal printing head for calculator or other uses. In this application the same segment in each digit is selected at the same time, reducing the overall time for a complete print cycle. The DS8654 is an 8-digit driver. With a 15-digit print head, two of the DS8654 are required. The DS8655 is an 8-segment driver. It drives 15 mA to the base of an external power transistor, which in turn may have to sink up to 800 mA if all segments happen to be selected. The segment drive is sequential and is decoded from inputs A, B and C. These inputs with an enable input and an Indicator Status input operate four status drive outputs, which are also selected sequentially. These outputs, designated LV, ADD, MEM and CALC are designed to drive LED status lamps through a single external limiting resistor to ground. The DS8655 also provides the clock for the calculator circuit (MM5786) with an external resistor and capacitor for accuracy.

The DS8656 diode arrays are used to prevent "sneak" currents in the resistive print head. In a 15-digit print head with one alphanumeric digit there are 119 resistor segments requiring 119 diodes. For ease of assembly, the DS8656 is configured in four groups of three common cathode diodes in each group. In the system, ten parts of DS8656 are required.

The whole system, *Figure 1*, is designed to operate from a +19V supply for the print head and an 8-cell nickle-cadmium battery supplying −8V to −11.6V for the rest of the electronics. The 8-segment drive transistors require LV_{CER}'s of 33V min, B of > 100 at I_C = 500 mA, and $V_{SAT} \leq 1.0V$ at 800 mA with 15 mA drive.

general description

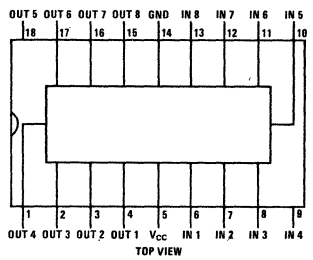
DS8654 is an 8-digit driver with emitter/follower outputs. It can source up to 50 mA at a low impedance, and operates with a constant internal drive current over a wide range of power supply—from 5V to 33V. The DS8654 can be used to drive electrical or mechanical, multiplexed or unmultiplexed display systems. It can be used as a segment driver for common cathode displays with external current limiting resistors or can drive incandescent or fluorescent displays directly, both digits (anodes) and segments (grids). It will be necessary to run the device at a lower duty cycle, to keep the maximum package dc power dissipation less than 600 mW while operating all 8 outputs at high supply voltage and large source current. The inputs are MOS compatible and eliminate the need for level shifting since inputs are referenced to the most negative supply of system.

The DS8655 is a 1-out-of-8 segment decoder/driver; also has 1-out-of-4 decoded status outputs and on-chip clock generator. The segment outputs and status outputs are controlled by enable and indicator status inputs respectively. The segment outputs can source 15 mA min. The status outputs are capable of sinking up to 40 mA at a low impedance. The device has a low-voltage battery indicator.

The clock frequency of the oscillator can be controlled by external timing components, R and C.

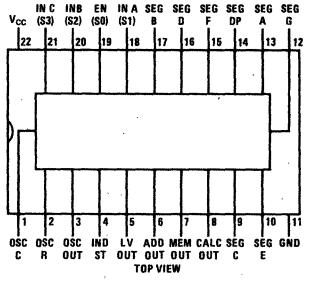
connection diagrams

Dual-In-Line Package



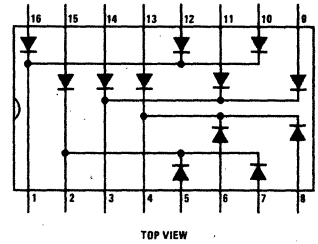
Order Number DS8654N

Dual-In-Line Package



Order Number DS8655N

Dual-In-Line Package



Order Number DS8656N

absolute maximum ratings DS8654 (Note 1)

Supply Voltage	36V
Input Voltage	36V
Output Voltage	0V
Storage Temperature Range	−65°C to +150°C
Maximum Package Power	600 mW
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions DS8654

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	22	33	V
Temperature (T_A)			
DS7654	−55	+125	°C
DS8654	0	+70	°C

electrical characteristics DS8654 (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 6.5V		390	500	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V		13	40	μA
I_{OH}	Logical "1" Output Current	V_{CC} = Max, V_{OUT} = Gnd		0.01	−100	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Max, I_{IN} = 500μA, I_{OH} = −50 mA		V_{CC}−1.8	V_{CC}−2.5	V
$I_{CC(OFF)}$	Supply Current	V_{CC} = Max, V_{IN} = V_{OUT} = Gnd		0.01	1.0	mA
$I_{CC(ON)}$	Supply Current (All Outputs "ON")	V_{CC} = Max, V_{IN} = 6.5V, I_{OUT} = 0 mA		7.5	10	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7654 and across the 0°C to +70°C range for the DS8654. All typicals are given for V_{CC} = 30V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

absolute maximum ratings DS8655 (Note 1)

Supply Voltage	13.5V
Input Voltage	11.6V
Output Voltage	6V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	600 mW
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions DS8655

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	8.0	11.6	V
Temperature (T_A)	0	+70	°C

electrical characteristics DS8655 (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
SEGMENT DECODER							
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 6.5V				500	μA
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 0.4V				40	μA
I_{OL1}	Logical "0" Output Current	V_{OL1} = 0V, V_{IN} = 0.4V				−10	μA
I_{OH1}	Logical "1" Output Current	V_{OH1} = 1.0V, V_{IN} = 6.5V		−15		−25	mA
STATUS OUTPUTS							
V_{OL2}	Logical "0" Output Voltage (Except LV)	V_{CC} = Min, V_{IN} = 6.5V, I_{OL2} = 40 mA				0.5	V
I_{OH}	Logical "1" Output Current	V_{OH} = 10V	V_{CC} = Max			500	μA
	LV "1" Output Current		V_{CC} = 9.0V			500	μA
V_{OL2}	LV "0" Output Voltage	V_{CC} = 8.6V, I_{OL2} = 40 mA				0.5	V
OSCILLATOR SECTION							
f_{OSC}	Oscillator Frequency	V_{CC} = Max, (Note 5)			100		kHz
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 2 mA				0.5	V
V_{OH}	Logical "1" Output Voltage	V_{CC} = Max, I_{OUT} = −100μA		V_{CC}−2.5			V
d	Duty Cycle			40		60	%
I_{CC}	Supply Current	V_{CC} = Max, One Output Selected (Note 4)				56	mA
$I_{CC(SB)}$	Stand-By Supply Current	V_{CC} = Max, V_{S0} = 6.5V				28	mA

switching characteristics DS8655 V_{CC} = 10V, T_A = 25°C unless otherwise specified.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0" From Input to Segment/Status Output	See ac Test Circuits			100	ns
t_{pd0}	Propagation Delay to a Logical "0" From Enable Indicator Status to Segment/Status Output	See ac Test Circuits			100	ns
t_{pd1}	Propagation Delay to a Logical "1" From Input to Segment/Status Output	See ac Test Circuits			100	ns
t_{pd1}	Propagation Delay to a Logical "1" From Enable/Indicator Status to Segment/Status Output	See ac Test Circuits			100	ns
f_{OSC}	Oscillator Frequency	R = 18k, C = 1500 pF		100		kHz
d	Duty Cycle	R = 18k, C = 1500 pF	40		60	%

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8655. All typicals are given for V_{CC} = 10V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

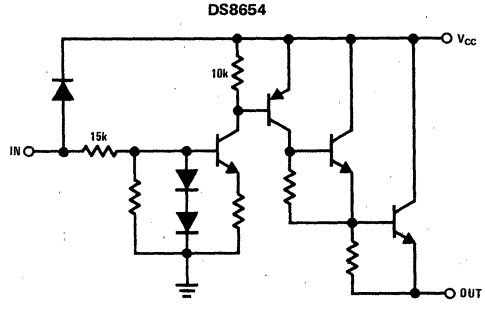
Note 4: Only one output at a time should be turned "ON."

Note 5: Oscillator frequency controlled by external timing components, resistor (2k to 20k) and capacitor.

electrical characteristics DS8656 (T_A = 0°C to +70°C)

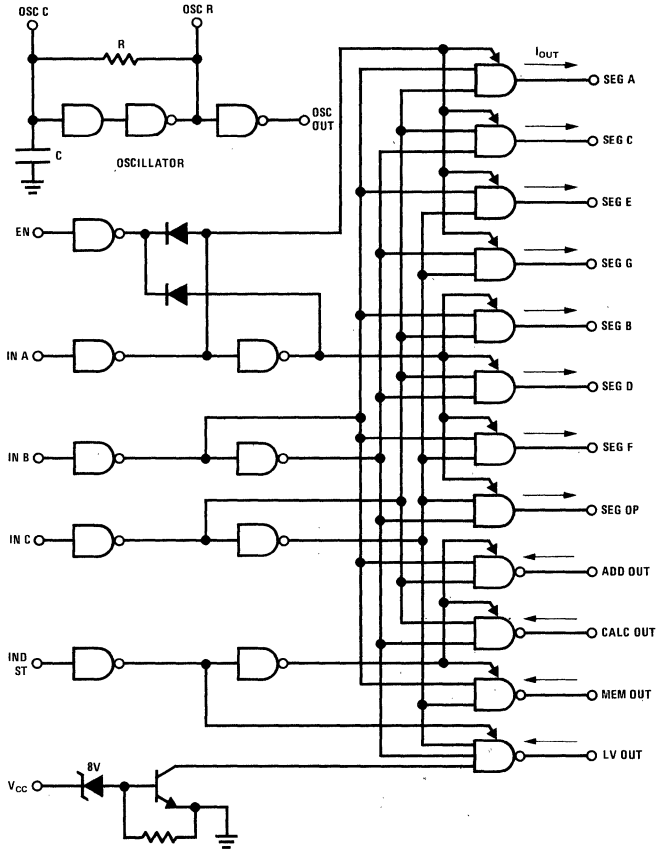
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_R	Peak Inverse Voltage	I_R = 0.1 mA	35			V
V_F	Forward Voltage	I_F = 50 mA			1.5	V
t_r	Reverse Recov. Time	I_F = 50 mA to I_R = 0.1 mA at V_R = 30V			1.0	μs

schematic diagram



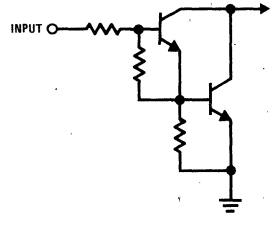
logic diagram

DS8655

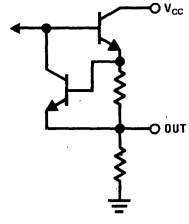


schematic diagrams (Input and Outputs)

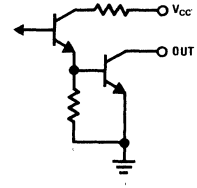
DS8655 Typical Input (Except Oscillator)



DS8655 Segment Output



DS8655 Status Output



truth tables DS8655

Segment Decoder

SELECTED OUTPUT	INC	INB	INA	EN
Seg. a	0	0	0	0
Seg. b	0	0	1	0
Seg. c	0	1	0	0
Seg. d	0	1	1	0
Seg. e	1	0	0	0
Seg. f	1	0	1	0
Seg. g	1	1	0	0
Seg. D.P.	1	1	1	0
None	X	X	X	1

X = Don't Care

Status Outputs

OUTPUT STATE				INC	INB	INDIC STATUS	V_{CC}
ADD	CALC	MEM	LV				
0	1	1	1	0	0	1	X
1	0	1	1	0	1	1	X
1	1	0	1	1	0	1	X
1	1	1	1	1	1	0	9.0–11.6V
1	1	1	0	1	1	0	8.0–8.6V

X = Don't Care

ac test circuits and switching time waveforms DS8655

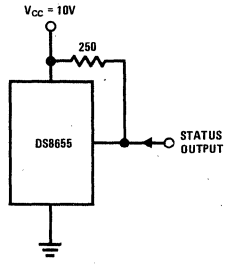


FIGURE 1.

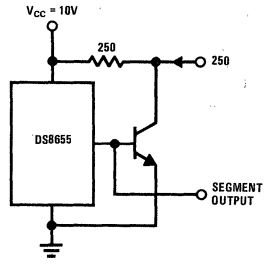


FIGURE 2.

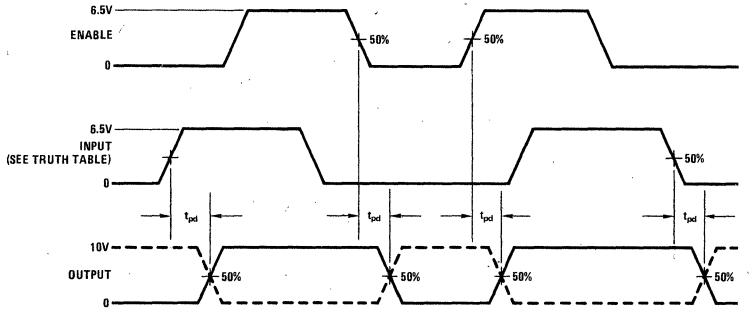
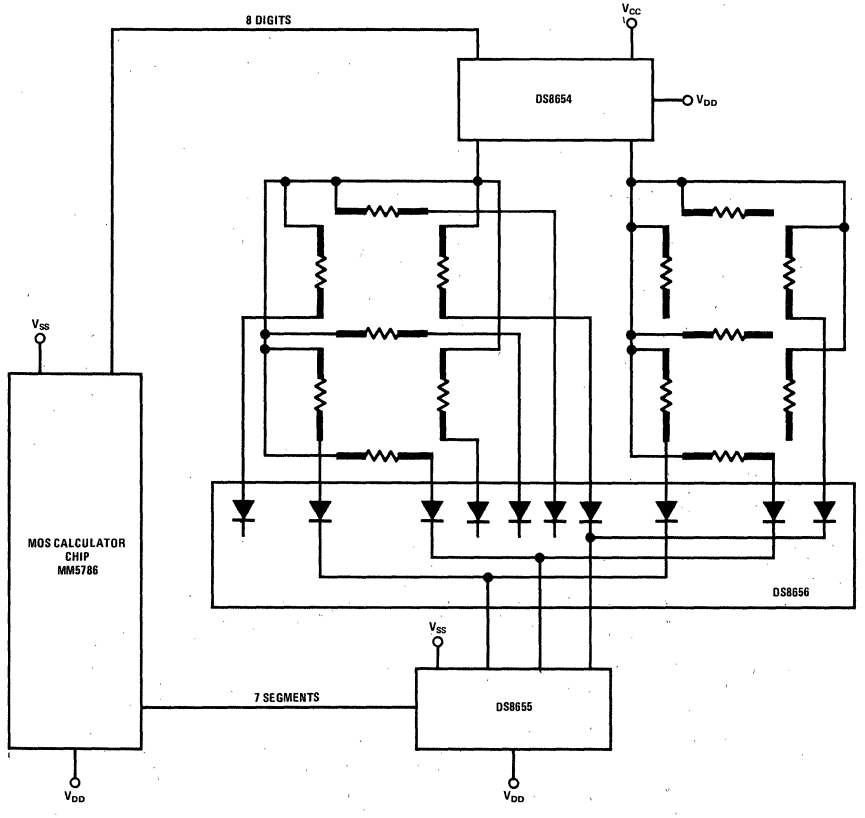
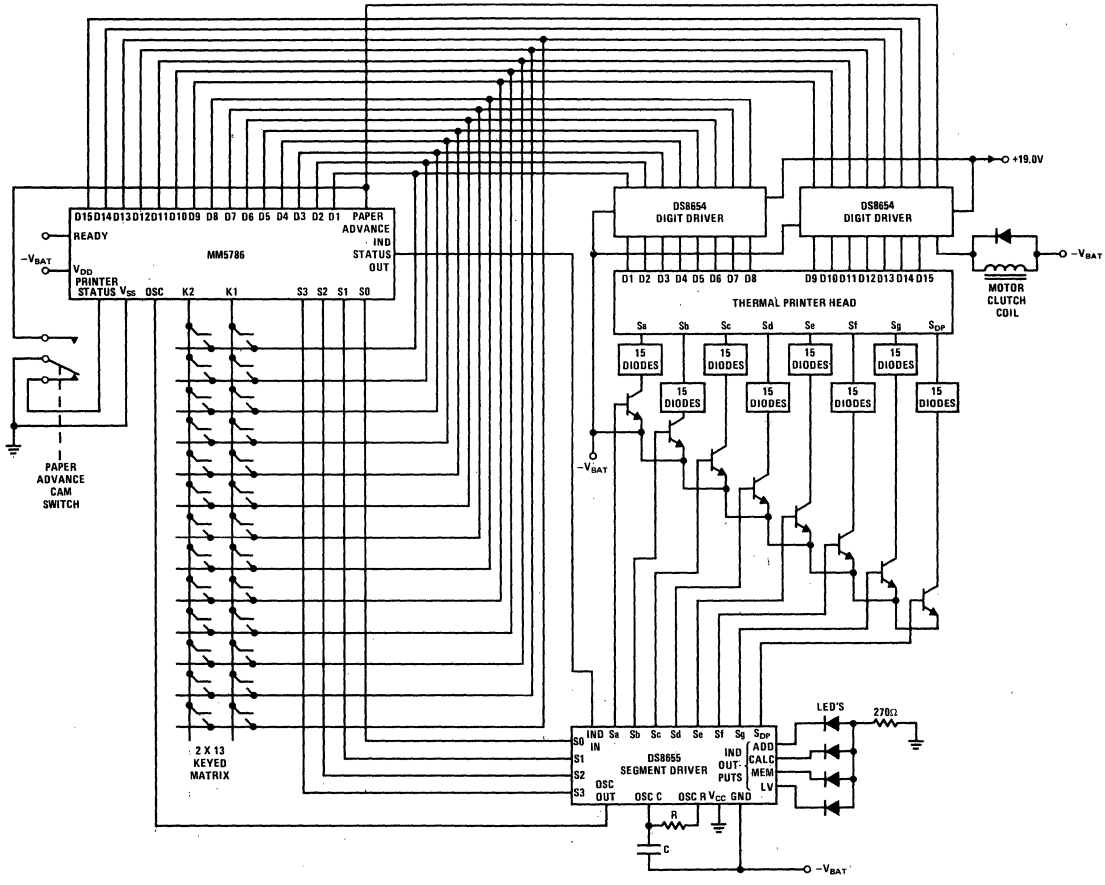


FIGURE 3.

typical application



system diagram



NATIONAL

DS8658 low voltage four-digit LED driver

general description

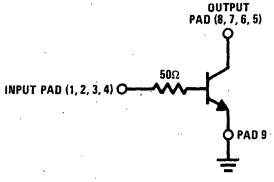
The DS8658 is a 4-digit LED display driver designed specifically for electronic watches. Its inputs interface directly with CMOS watch circuits such as the MM5829, and its outputs sink typically 100 mA from a common cathode LED watch display.

The DS8658 is supplied in dice form. Plastic DIP parts are available for device evaluation.

features

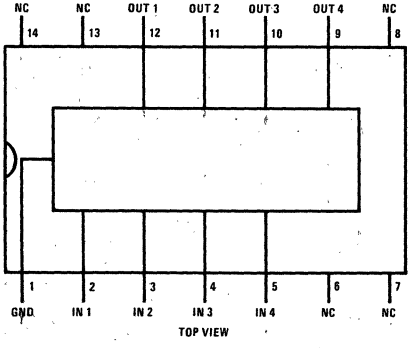
- Direct interface with CMOS watch circuits
- Grouped inputs and outputs
- Low voltage operation
- Packaged devices available for evaluation

schematic diagram

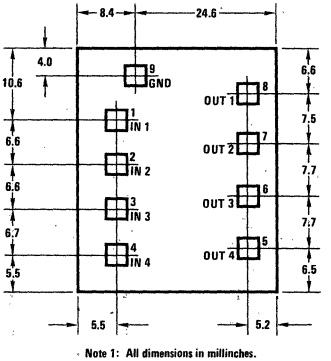


connection diagram and chip pad layout

Dual-In-Line Package



Order Number DS8658N



Note 1: All dimensions in millinches.
Note 2: Die size 33 mils x 36 mils.
Note 3: Pads 4.0 mils square clear area.

absolute maximum ratings

Applied Voltage $V_{IN} = 1.5V$
$V_{OUT} = 5V$

electrical characteristics (Note 1)

$2.7V \leq V_{CC} \leq 2.9V$; $-5°C \leq T_A \leq +70°C$, unless otherwise specified.

	PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
I_{IH}	Input "ON" Current	$V_{IN} = 1.1V$, $I_{OUT} = 56$ mA	0.84	6		mA
I_{IL}	Input "OFF" Current	$V_{IN} = 0.2V$, $V_{OUT} = 5V$		−0.01	−20	μA
V_{OL}	Output "ON" Voltage	$I_{OL} = 56$ mA, $I_{IN} = 840\mu A$, $V_{CC} = 2.4V$			0.40	V
		$I_{OL} = 84$ mA, $I_{IN} = 1.3$ mA, $V_{CC} = 2.7V$			0.55	V
I_{CEX}	Output Leakage Current (4 Outputs Tied Together)	$V_{IN} = 0.2V$, $V_{OUT} = 5V$		0.07	1.0	μA
I_{OL}	Output Sink Current	$V_{OL} = 0.55V$, $I_{IN} = 1.3$ mA	84	100		mA

Note 1: All references to V_{CC} apply on a system basis since the DS8658 has no V_{CC} connection.

NATIONAL

Display Drivers

Advance Information*

DS8673, DS8674 7-segment decoder/driver/latch

general description

The DS8673, DS8674 is a 7-segment decoder/driver with latches on the address inputs and active low constant current outputs to drive LEDs directly.

The DS8673, DS8674 accepts a 4-bit binary code and produces output drive to the appropriate segments of the 7-segment display. It has a decode format which produces numeric codes "0" through "9" and other codes as shown on subsequent pages (see truth table).

Latches on the four data inputs are controlled by an active low Latch Enable $\overline{E_L}$. When $\overline{E_L}$ is low, the state of the outputs is determined by the input data. When $\overline{E_L}$ goes high, the last data present at the inputs is stored in the latches and the outputs remain stable. The $\overline{E_L}$ pulse width necessary to accept and store data is typically 50 ns, which allows data to be strobed into the DS8673, DS8674 at normal TTL speeds. This feature means that data can be routed directly from high speed counters and frequency dividers into the display without slowing down the system clock or providing intermediate data storage.

The latch/decoder combination is a simple system which drives LED displays with multiplexed data inputs from MOS time clocks, DVMs, calculator chips, etc. Data inputs are multiplexed while the displays are in static mode. This lowers component and insertion costs, since several circuits—seven resistors per display, strobe drivers, a separate display voltage source, and clock failure detect circuits—traditionally found in multiplexed display systems are eliminated. It also allows low strobing rates to be used without display flicker.

Another feature of the DS8673, DS8674 is the reduced loading on the data inputs when the latch enable is high (only 10μA typ). This allows many DS8673, DS8674's to be driven from a MOS device in multiplex mode without the need for drivers on the data lines.

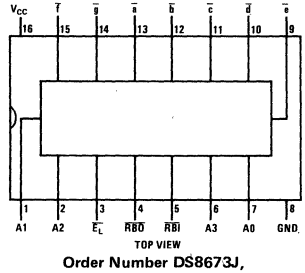
The DS8673, DS8674 also provides automatic blanking of the leading and/or trailing edge zeros in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice.

features

- High speed input latches for data storage
- 15 mA constant current sink capability to directly drive common anode LED displays. . . man 1 type
- Active low latch enable for easy interface with MSI circuits
- Data input loading essentially zero when latch disabled
- Automatic ripple blanking for suppression of leading edge zeros and/or trailing edge zeros
- Pin out compatible with other standard MSI decoders such as DM7446, DM7447 and DM7448
- Replaces Fairchild 9374 and Signetics 8T74 pin for pin

connection diagram

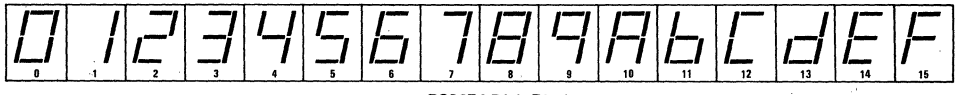
Dual-In-Line Package



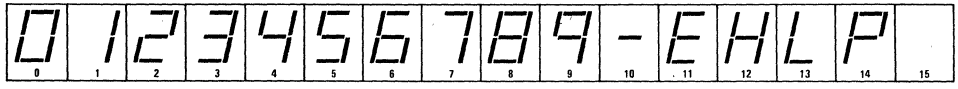
TOP VIEW

Order Number DS8673J, DS8674J or DS8673N, DS8674N

DS8673 Digit Display



DS8674 Digit Display



*Specifications may change.

absolute maximum ratings (Note 1)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Lead Potential to Ground Lead	−0.5V to +7.0V
*Input Voltage (dc)	−0.5V to +5.5V
*Input Current (dc)	−30 mA to +5.0 mA
Output Voltage (dc) Output "OFF"	10V
Output Voltage (dc) Output "ON"	8.0V
Lead Temperature (Soldering, 10 seconds)	300°C

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	+75	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Input High Voltage	Guaranteed Input High Voltage for All Inputs		2.0			V
V_{IL}	Input Low Voltage	Guaranteed Input Low Voltage for All Inputs				0.8	V
V_{CD}	Input Clamp Diode Voltage	V_{CC} = Min, I_{IN} = −12 mA, T_A = 25°C				−1.5	V
V_{OH}	Output High Voltage $\overline{RBO}$	V_{CC} = Min, I_{OH} = −40μA		2.4	3.5		V
V_{OL}	Output Low Voltage $\overline{RBO}$	V_{CC} = Min, I_{OL} = 0.8 mA			0.25	0.4	V
I_{OL}	Output Low Current $\overline{a}$ through $\overline{g}$	V_{CC} = 5.0V, V_{OL} = 3.0V		12	15	18	mA
		V_{CC} = 5.0V, V_{OL} = 0.5V			14		mA
I_{CEX}	Output High Leakage Current $\overline{a}$ through $\overline{g}$	V_{CC} = Max, V_{OUT} = 5.5V				250	μA
I_{IH}	Input High Current	V_{CC} = Max, V_{IN} = 2.4V	Data		10	40	μA
			$\overline{RBI}$ and $\overline{E_L}$		5	20	μA
I_{IH}	Input High Current	V_{CC} = Max, V_{IN} = 5.5V				1.0	mA
I_{IL}	Input Low Current	V_{CC} = Max, V_{IN} = 0.4V	$\overline{E_L}$ and $\overline{RBI}$		−0.25	−0.4	mA
			Data (Latch Enable Low)		−0.25	−0.4	mA
			Data (Latch Enable High)		±0.01	−0.06	mA
			$\overline{RBO}$ (Used as an Input)		−0.7	−1.2	mA
I_{CC}	Power Supply Current	V_{CC} = Max, V_{IN} = 0.0V, V_{OUT} = 3.0V			35	50	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +75° range for the DS8673 and DS8674. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

switching characteristics $T_A = 25°C$, $V_{CC} = 5.0V$

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}	Turn On Delay Data Input to Output	$R_L = 1\ k\Omega$, $C_L = 15\ pF$, *(Figure 3)*			140	ns
t_{PLH}	Turn Off Delay Data Input to Output	$R_L = 1\ k\Omega$, $C_L = 15\ pF$, *(Figure 3)*			140	ns
t_{PHL}	Turn On Delay $\overline{E_L}$ Input to Output	$R_L = 1\ k\Omega$, $C_L = 15\ pF$, *(Figure 2)*			140	ns
t_{PLH}	Turn Off Delay $\overline{E_L}$ Input to Output	$R_L = 1\ k\Omega$, $C_L = 15\ pF$, *(Figure 2)*			140	ns
$t_s(H)$	Set-Up Time High Data to Latch Enable	*(Figure 4)*	75			ns
$t_h(H)$	Hold Time High Data to Latch Enable	*(Figure 4)*	0			ns
$t_s(L)$	Set-Up Time Low Data to Latch Enable	*(Figure 4)*	30			ns
$t_h(L)$	Hold Time Low Data to Latch Enable	*(Figure 4)*	0			ns
$t_w(\overline{E_L})$	Latch Enable Pulse Width	*(Figure 5)*	85	50		ns

Set-Up Time: t_s is defined as the time required for the logic level to be present at the Data Input prior to the Enable transition from Low to High in order for the latch to recognize and store the new data.

Hold Time: t_h is defined as the minimum time following the Enable transition from Low to High that the logic level must be maintained at the data input in order to ensure continued recognition. A negative Hold Time indicates that the logic level may be released prior to the Enable transition from Low to High and still be recognized.

typical performance characteristics

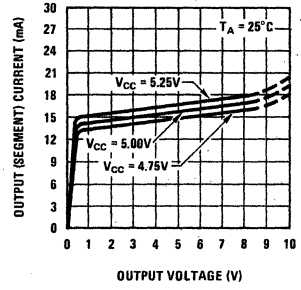


FIGURE 1. Typical Constant Segment Current vs Output Voltage

switching time waveforms

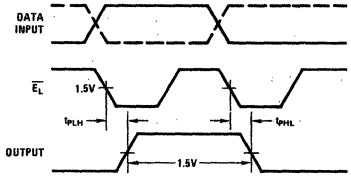


FIGURE 2.

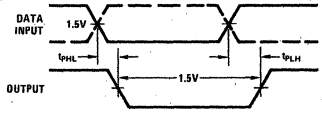


FIGURE 3.

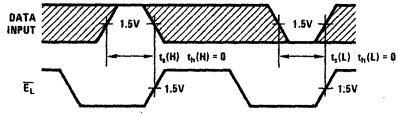


FIGURE 4.

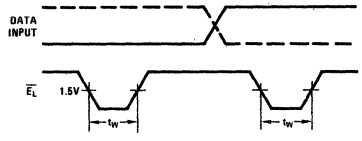
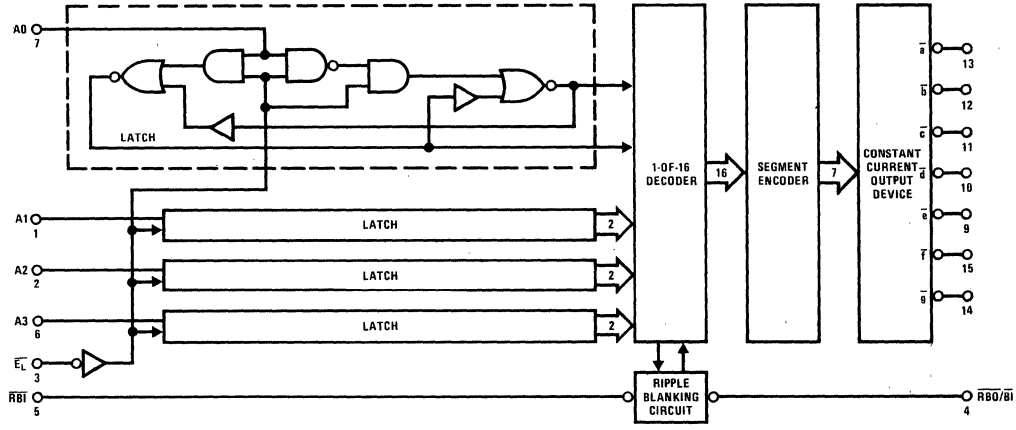


FIGURE 5.

block diagram



truth table

BINARY STATE	INPUTS $\overline{E_L}$	$\overline{RBI}$	A3	A2	A1	A0	OUTPUTS $\overline{a}$	$\overline{b}$	$\overline{c}$	$\overline{d}$	$\overline{e}$	$\overline{f}$	$\overline{g}$	$\overline{RBO}$	DISPLAY
–	H	*	X	X	X	X	← STABLE →							H	STABLE
0	L	L	L	L	L	L	H	H	H	H	H	H	H	L	BLANK
0	L	H	L	L	L	L	L	L	L	L	L	L	H	H	0
1	L	X	L	L	L	H	H	L	L	H	H	H	H	↓	1
2	L	↓	L	L	H	L	L	L	H	L	L	H	L	↓	2
3	L	↓	L	L	H	H	L	L	L	L	H	H	L	↓	3
4	L	↓	L	H	L	L	H	L	L	H	H	L	L	↓	4
5	L	↓	L	H	L	H	L	H	L	L	H	L	L	↓	5
6	L	↓	L	H	H	L	L	H	L	L	L	L	L	↓	6
7	L	↓	L	H	H	H	L	L	L	H	H	H	H	↓	7
8	L	↓	H	L	L	L	L	L	L	L	L	L	L	↓	8
9	L	↓	H	L	L	H	L	L	L	H	H	L	L	↓	9
10	L	↓	H	L	H	L	H	H	H	H	H	H	L	↓	-
11	L	↓	H	L	H	H	L	H	H	L	L	L	L	↓	E
12	L	↓	H	H	L	L	H	L	L	H	L	L	L	↓	H
13	L	↓	H	H	L	H	H	H	H	L	L	L	H	↓	L
14	L	↓	H	H	H	L	L	L	H	H	L	L	L	↓	P
15	L	X	H	H	H	H	H	H	H	H	H	H	H	H	BLANK
X	X	X	X	X	X	X	H	H	H	H	H	H	H	L**	BLANK

*The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.
**$\overline{RBO}$ used as an input overrides all other input conditions.

DEFINITION	INPUTS	OUTPUTS
H	High Voltage Level	Output is "OFF"
L	Low Voltage Level	Sinking Current
X	Don't Care	

Segment Identification

application hints

It is possible with common anode 7-segment LED displays and constant current sink decoder drivers to save substantial amounts of power by carefully choosing operating points on display supply voltage. First, examine the power used in the normal display driving method where the display and decoder driver are both operated from a 5V regulated supply ($V_{CC} = V_S$).

The power dissipated by the LED and the driver outputs is ($V_{CC} \times I_{SEG} \times$ n Segments). The total power dissipated with a 15 mA LED displaying an eight (8) would be:

$$P_{TOT} = 5.0V \times 15\ mA \times 7$$
$$= 525\ mW$$

Of this 525 mW, the power actually required to drive the LED is dependent on the V_F drop of each segment. Most GaAsP LEDs exhibit either a 1.7V or a 3.4V

application hints (con't)

forward voltage drop. Therefore, the required total power for seven segments would be:

$P_{(1.7)} = 1.7V \times 15\ mA \times 7$
$= 178.5\ mW$
$P_{(3.4)} = 3.4V \times 15\ mA \times 7$
$= 357\ mW$

The remaining power is dissipated by the driver outputs which are maintaining the 15 mA constant current required by the LEDs. Most of this power is wasted, since the driver can maintain approximately 15 mA with as little as 0.5V across the output device. By using a separate power source (V_S) for the LEDs, which is set to the LED V_F plus the offset voltage of the driver, as much as 280 mW can be saved per digit, i.e.,

$V_S = V_{F(MAX)} + V_{OFFSET}$
$= 2.0V + 0.5V$
$= 2.5V$
$P_T = 2.5V \times 14\ mA$ (from *Figure 2)* $\times 7$
$= 245\ mW$

These figures show that using a separate supply to drive the LEDs can offer significant display power savings. In battery powered equipment, two rechargeable nickle-cadmium cells in series would be sufficient to drive the display, while four such cells would be needed to operate the logic units.

LOW POWER, LOW COST DISPLAY POWER SOURCES

In small line operated systems using TTL/MSI and LED or incandescent displays, a significant portion of the total dc power is consumed to drive the displays. Since it is irrelevant whether displays are driven from unfiltered dc or pulsed dc (at fast rates), a dual power system can be used that makes better utilization of transformer rms ratings. The system utilizes a full wave rectified but unsmoothed dc voltage to provide the displays with 120 Hz pulsed power while the rest of the system is driven by a conventional dc power supply circuit. The frequency of 120 Hz is high enough to avoid display flicker problems. The main advantages of this system are:

a. Reduced transformer rating
b. Much small smoothing capacitor
c. Increased LED light output due to pulsed operation

With the standard capacitor filter circuit, the rms current (full wave) loading of the transformer is approximately twice the dc output. Most commercial transformer manufacturers rate transformers with capacitive input filters as follows:

Full Wave Bridge Rectifier Circuit
Transformer rms current = 1.8 x dc current required

Full Wave Center Tapped Rectifier Circuit
Transformer rms current = 1.2 x dc current required

Therefore, the removal of a large portion of the filtered dc current requirement (display power) substantially reduces the transformer loading.

There are two basic approaches. First *(Figure 7)* is the direct full wave rectified unregulated supply to power the displays. The DS8673, DS8674 decoder driver constant current feature maintains the specified segment current after the LED diode drop and 0.5V saturation voltage has been reached (≅2.2V). Care must be exercised not to exceed the drivers' power ratings and the maximum voltage that the decoder driver sees in both the "ON" and "OFF" modes.

The second approach *(Figure 8)* uses a 3-terminal voltage regulator such as the LM340T-5 to provide dc pulsed power to the display with the peak dc voltage limited to 5V. This approach allows easier system thermal management by heat sinking the regulator rather than the display or display drivers. When this power source is used with an intensity modulation scheme or with a multiplexed display system, the frequencies must be chosen such that they do not beat with the 120 Hz full wave rectified power frequency.

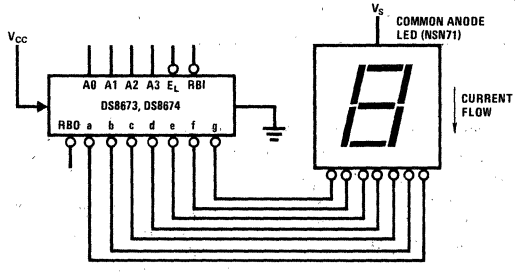


FIGURE 6.

application hints (con't)

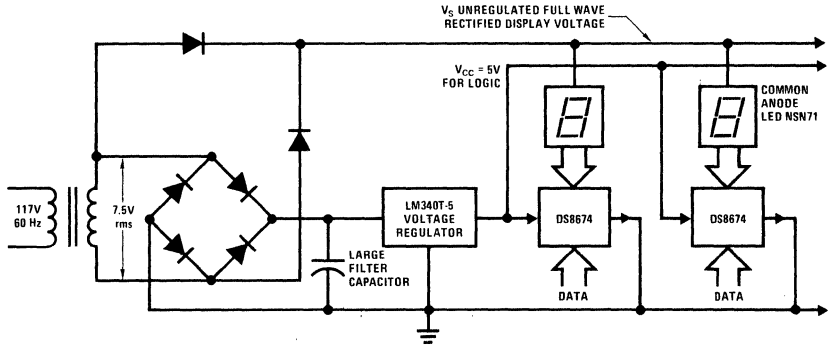


FIGURE 7.

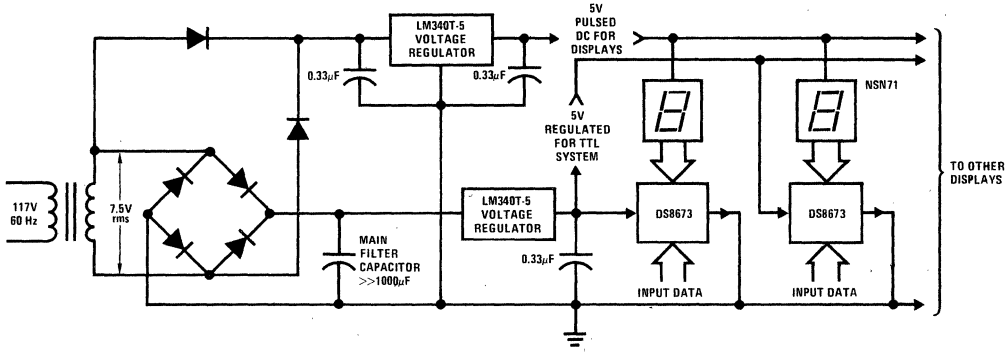


FIGURE 8.

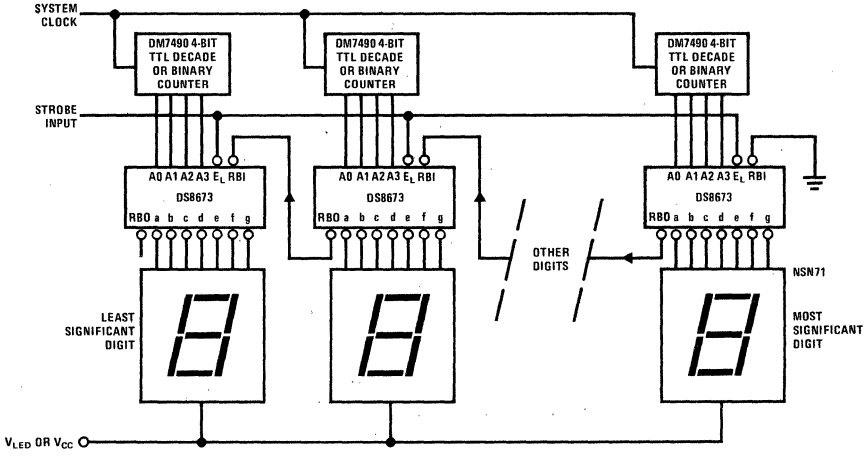


FIGURE 9.

DS8692, DS8693, DS8694 printing calculator interface set

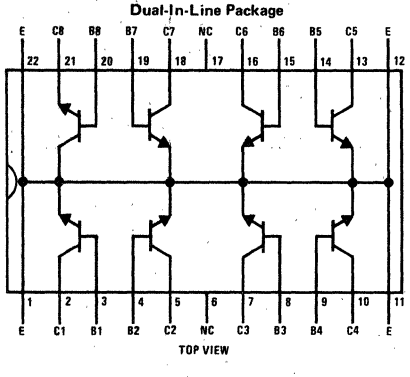
general description

Two DS8692 IC's and one each of the DS8693 and DS8694 provide the complete interface necessary between the MM5787 calculator chip and the Seiko Model 310 printing head. The DS8692 is an array of eight common emitter output transistors each capable of sinking 350 mA, with open collector saturating outputs. The DS8693 contains the interface logic for the color solenoid driver, motor driver, and 7-column character select solenoid drivers. The DS8694 contains the interface logic for 8-column solenoid drivers plus the clock oscillator and timing signal buffer. The color and character select solenoid driver outputs of both are constant current outputs supplying the base current for the DS8692 arrays. These outputs also feature active pull-down. The motor drive output is an open collector capable of sinking 20 mA.

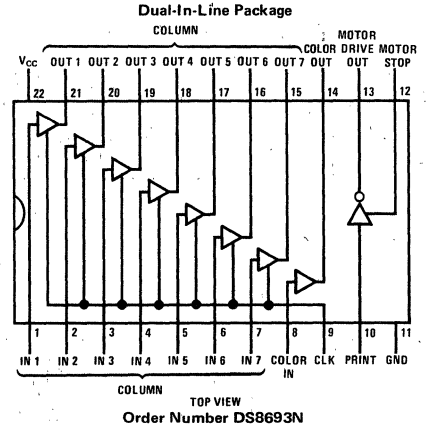
features

- Provides complete interface package for printing calculators with minimum number of packages and minimum number of external components
- 350 mA sink capability

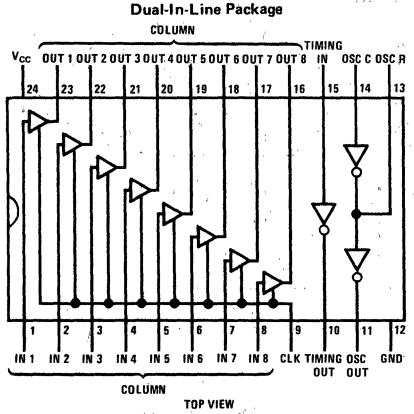
connection diagrams



Order Number DS8692N



Order Number DS8693N



Order Number DS8694N

absolute maximum ratings DS8692—Transistor Array (Note 1)

Collector to Base Voltage	35V	Power Dissipation (T_A = 25°C)	650 mW
Collector to Emitter Voltage	35V	Operating Junction Temperature	150°C max
Collector to Emitter Voltage (Note 4)	15V	Operating Temperature Range	0°C to +70°C
Emitter to Base Voltage	6V	Storage Temperature Range	−65°C to +150°C
Collector Current (Continuous)	0.4A	Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics DS8692 (Each Transistor, T_A = 25°C unless specified) (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{CE0}	Collector to Emitter Breakdown Voltage	I_C = 100μA, I_B = 0	15			V
V_{CES}	Collector to Emitter Breakdown Voltage	I_C = 100μA, V_{BE} = 0	35			V
V_{CB0}	Collector to Base Breakdown Voltage	I_C = 100μA, I_E = 0	35			V
h_{FE}	dc Current Gain	I_C = 165 mA @ V_{CE} = 5V I_C = 350 mA @ V_{CE} = 5V	80 70			V V
$V_{CE(SAT)}$	Collector to Emitter Saturation Voltage	I_C = 350 mA, I_B = 7.0 mA			1.0	V
$V_{BE(SAT)}$	Base to Emitter Saturation Voltage	I_C = 350 mA, I_B = 7.0 mA			0.95	V

absolute maximum ratings DS8693 (Note 1)

Supply Voltage	12V
Input Voltage	12V
Output Voltage	
All Pins Except Pin 13	12V
Pin 13	19V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions DS8693

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	8.5	11.0	V
Temperature (T_A)	0	+70	°C

electrical characteristics DS8693 (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
COLUMN DRIVERS						
I_{IN}	Input Current	V_{IN} = V_{CC} −1.5V			250	μA
V_{OL}	Output "OFF" Voltage	V_{CC} = Min, I_{IN} = 50.0μA, I_{CLOCK} = 300μA, I_{OUT} = 1 mA			0.4	V
I_{OH}	Output "ON" Current	V_{CC} = Min, V_{IN} = 7.0V, I_{CLOCK} = 300μA, V_{OUT} = 1.0V	−7		−17	mA
I_{OS}	Output Short Circuit Current	V_{CC} = Max, I_{IN} = 50μA, I_{CLOCK} = 300μA, V_{OUT} = 0.0V			−1.2	mA
CLOCK INPUT						
V_{IN}	Input Voltage	I_{IN} = 300μA I_{IN} = 50μA	4.1		 1.5	V V
I_{IH}	Logical "1" Input High Current		300			μA
I_{IL}	Logical "0" Input Low Current				50	μA
MOTOR DRIVER						
$I_{IN(PRINT)}$	Input Current	V_{IN} = V_{CC} −1.5V			250	μA
$I_{IL(STOP)}$	Input Low Current (Stop)	V_{CC} = Min, $V_{IN(STOP)}$ = 0.0V, (Stop Switch Closed)	−270			μA
$V_{IH(STOP)}$	Input High Voltage (Stop)	V_{CC} = Max, $I_{IN(STOP)}$ = 0μA, (Stop Switch Open)			1.35	V
V_{OL}	Output Low Voltage	V_{CC} = Min, V_{PRINT} = 7V, I_{OUT} = 15 mA			0.5	V
I_{OX}	Output Leakage Current	V_{CC} = Max, I_{PRINT} = 50μA, V_{STOP} = 0.0V, V_{OUT} = 15V			100	μA

electrical characteristics (con't) DS8693

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
COLOR DRIVER						
V_{IN}	Input Voltage	I_{IN} = 250μA	4.55			V
		I_{IN} = 50μA			1.65	V
V_{OL}	Output "OFF" Voltage	V_{CC} = Min, I_{IN} = 50μA, I_{OUT} = 1 mA			0.4	V
I_{OH}	Output "ON" Current	V_{CC} = Min, I_{IN} = 250μA, V_{OUT} = 1.0V	−8		−18	mA
$I_{CC(PEAK)}$	Peak Supply Current	V_{CC} = Max, $V_{COLUMN\ IN}/V_{PRINT}$ = 7V, I_{CLOCK}/I_{COLOR} = 300μA, (Note 6)			180	mA
$I_{CC(SB)}$	Stand-by Supply Current	V_{CC} = Max, $V_{COLUMN\ IN}/V_{PRINT}$ = 0V, I_{COLOR} = 0μA, I_{CLOCK} = 300μA			55	mA
$I_{CC(AVE)}$	Average Supply Current	V_{CC} = Max, Continuous Operation			68	mA

absolute maximum ratings DS8694 (Note 1)

Supply Voltage	12V
Input Voltage	
All Pins Except Pin 15	12V
Pin 15	19V
Output Voltage	12V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	8.5	11.0	V
Temperature (T_A)	0	+70	°C

dc electrical characteristics DS8694 (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
COLUMN DRIVER						
I_{IN}	Input Current	V_{IN} = V_{CC} −1.5V			250	μA
V_{OL}	Output "OFF" Voltage	V_{CC} = Min, I_{IN} = 50μA, I_{CLOCK} = 300μA, I_{OUT} = 1 mA			0.4	V
I_{OH}	Output "ON" Current	V_{CC} = Min, V_{IN} = 7.0V, I_{CLOCK} = 300μA, V_{OUT} = 1.0V	−7		−17	mA
I_{OS}	Output Short Circuit Current	V_{CC} = Max, I_{IN} = 50μA, I_{CLOCK} = 300μA, V_{OUT} = 0.0V			−1.2	mA
CLOCK INPUT						
V_{IN}	Input Voltage	I_{IN} = 300μA	4.1			V
		I_{IN} = 50μA			1.5	V
I_{IH}	Logical "1" Input High Current		300			μA
I_{IL}	Logical "0" Input Low Current				50	μA
TIMING BUFFER						
I_{IN}	Input Current	V_{IN} = 17V	380		880	μA
V_{OL}	Output Low Voltage	I_{OUT} = 50μA, V_{IN} = 10V			0.5	V
V_{OH}	Output High Voltage	I_{OUT} = −50μA, V_{IN} = 7V	V_{CC}−1.0			V
OSCILLATOR						
f_{OSC}	Frequency	V_{CC} = Max, R = 18k, C = 0.0015μFd, (Note 5)	85	100	115	kHz
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OUT} = 50μA			0.5	V
V_{OH}	Output High Voltage	I_{OUT} = −50μA	V_{CC}−1.0			V
d	Duty Cycle	V_{CC} = Max	40	50	60	%
V_{OSC}	Osc. V_{CC} Turn-On Voltage		7.2	7.7	8.2	V
$I_{CC(PEAK)}$	Peak Supply Current	V_{CC} = Max, $V_{COLUMN\ IN}/V_{PRINT}$ = 7V, I_{CLOCK} = 300μA, (Note 6)			200	mA
$I_{CC(SB)}$	Stand-by Supply Current	V_{CC} = Max, $V_{COLUMN\ IN}/V_{PRINT}$ = 0V, I_{CLOCK} = 300μA			55	mA
$I_{CC(AVE)}$	Average Supply Current	V_{CC} = Max, Continuous Operation			62	mA

ac electrical characteristics DS8694

V_{CC} = 5.0V, T_A = 25°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
COLUMN DRIVERS (DS8693, DS8694) *(Figure 3)*						
PW_{COLUMN}	Column In Pulse Width		1.1	360.0		μs
PW_{CLOCK}	Clock Pulse Width		1.0	150.0		μs
t_d	Delay of Column In Pulse After Clock Transitions to Low State for Output to Latch		0.1	160.0		μs
t_{pd0}	Propagation Delay to a Logical "0" From Clock to Column Out Output	Column In = 0V			10.0	μs
t_{pd1}	Propagation Delay to a Logical "1" From Clock to Column Output	Column In = 7V			1300	μs
t_{pd0}	Propagation Delay to a Logical "0" From Column In to Column Out	Clock = 7V			10	μs
t_{pd1}	Propagation Delay to a Logical "1" From Column In to Column Out	Clock = 7V			1300	μs
COLOR DRIVER (DS8693) *(Figure 4)*						
t_{pd0}	Propagation Delay to a Logical "0" From Color In to Color Out				10.0	μs
t_{pd1}	Propagation Delay to a Logical "1" From Color In to Color Out				10.0	μs
MOTOR DRIVER (DS8693) *(Figure 6)*						
PW_{PRINT}	Print Signal Pulse Width		1	2400		μs
PW_{STOP}	Stop Signal Pulse Width		1	3000		μs
PW_{CLOCK}	Clock Pulse Width		1	150		μs
t_{pd0}	Propagation Delay to a Logical "0" From Print to Motor Drive Out				100	μs
t_{pd1}	Propagation Delay to a Logical "1" From Motor Stop (High-to-Low Transition) to Motor Drive Out	Print = 0.0V, Clock = 7.0V			10	μs
TIMING SIGNAL BUFFER (DS8694) *(Figure 5)*						
PW_{TIMING}	Timing Signal Pulse Width			1		ms
t_r	Rise Time	C_{LOAD} = 35 pF			500	ns
t_f	Fall Time	C_{LOAD} = 35 pF			500	ns
t_{pd0}	Propagation Delay to a Logical "0" From Timing In to Timing Out				10	μs
t_{pd1}	Propagation Delay to a Logical "1" From Timing In to Timing Out				10	μs
CLOCK OSCILLATOR (DS8694) *(Figure 7)*						
f_{OSC}	Oscillator Frequency	(Note 5)	85	100	115	kHz
d	Duty Cycle		40	50	60	%
t_r	Rise Time	C_{LOAD} = 35 pF			500	ns
t_f	Fall Time	C_{LOAD} = 35 pF			500	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS8692, DS8693, DS8694. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values hsown as max or min on absolute basis.

Note 4: Ratings refer to a high current point where collector-emitter voltage is lowest.

Note 5: Oscillator frequency is determined by external R between "Osc R" and "Osc C" and external C from "Osc C" to ground. 2k > R > 20k.

Note 6: Column outputs operate on approximately 1/16 duty cycle in normal operation.

system connection diagram

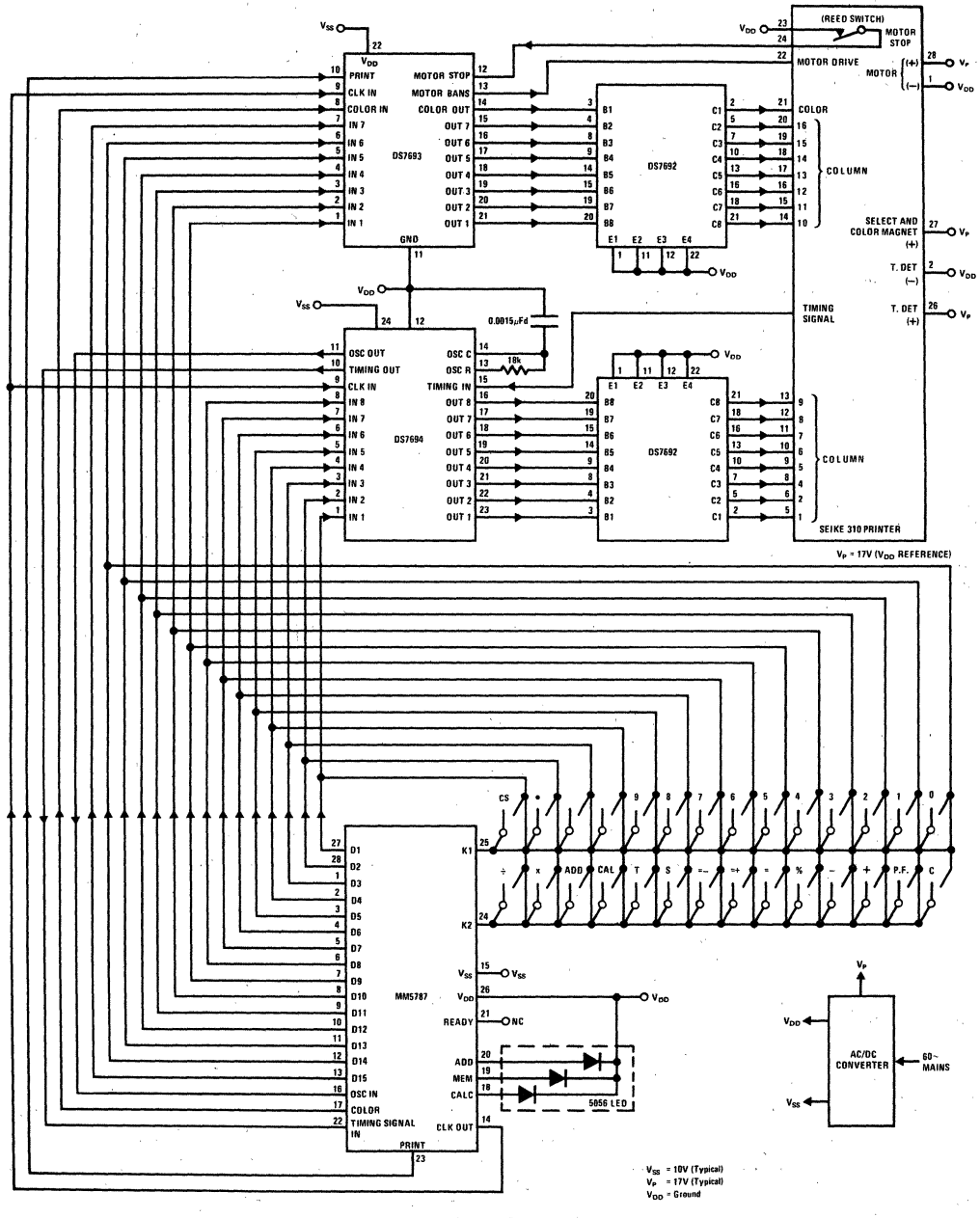
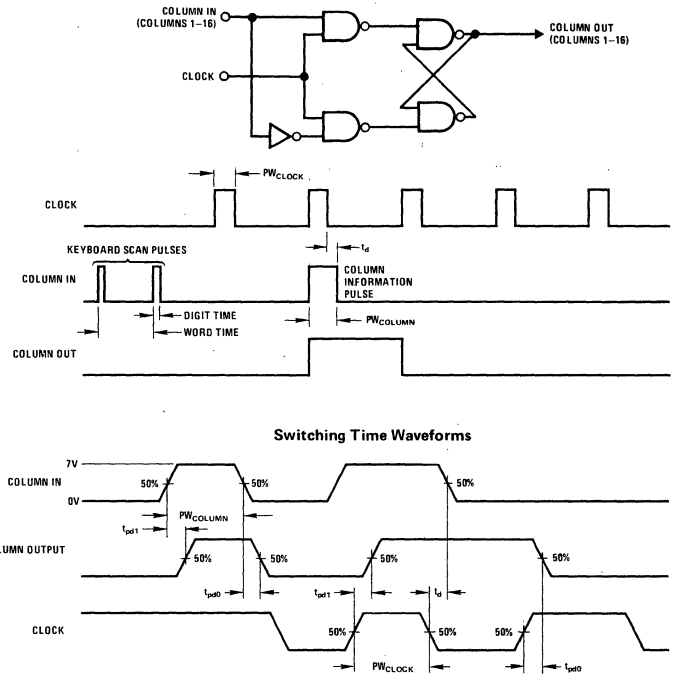


FIGURE 1.

Logic and Timing Diagrams



Switching Time Waveforms

FIGURE 3. DS8693/DS8694 Column Driver

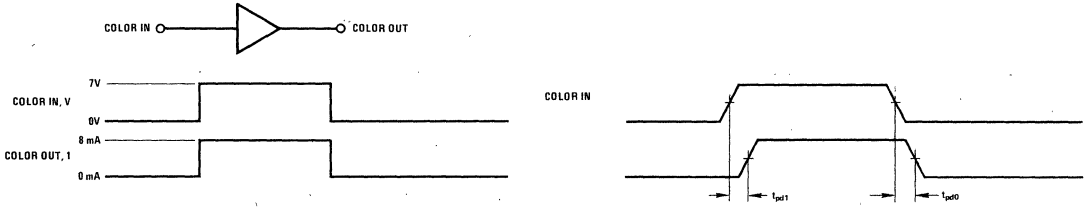


FIGURE 4. DS8693 Color Driver

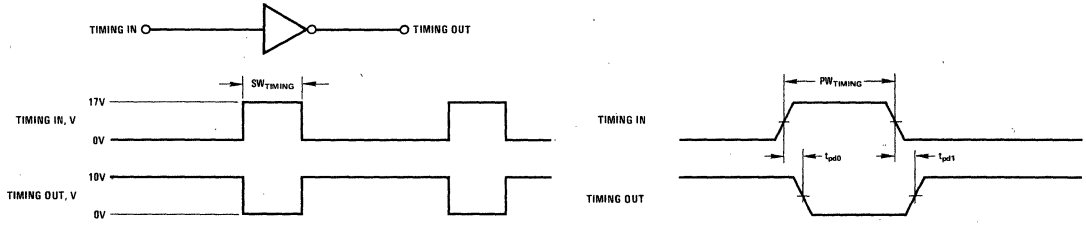
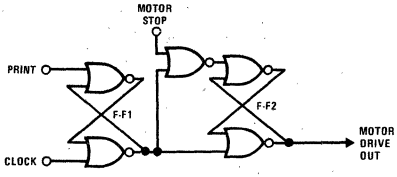
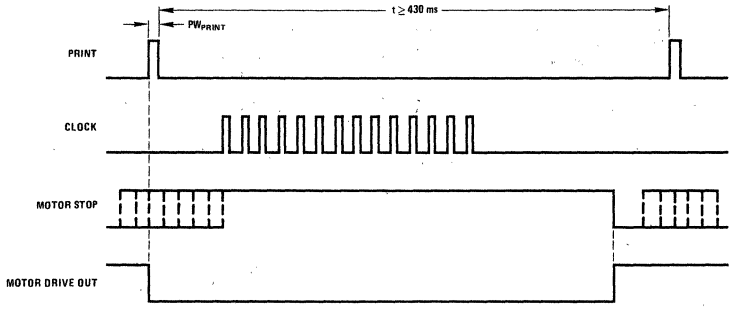


FIGURE 5. DS8694 Timing Signal Buffer

Logic and Timing Diagrams





Switching Time Waveforms

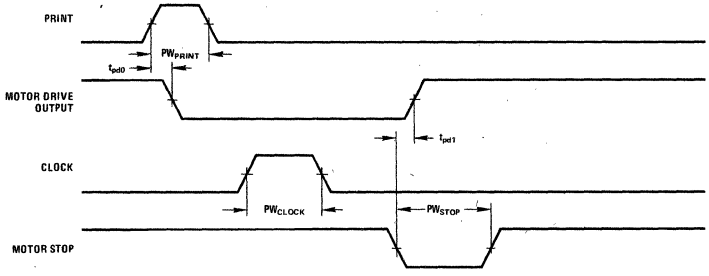


FIGURE 6. DS7693 Motor Drive Circuit

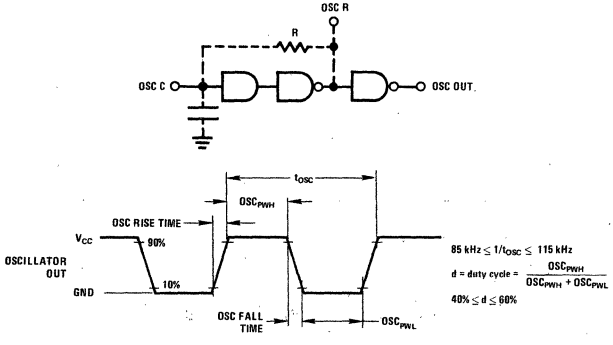


FIGURE 7. DS8694 Oscillator Diagram

NATIONAL

DS8844, DS8855, DS8864, DS8865, DS8866 LED cathode drivers

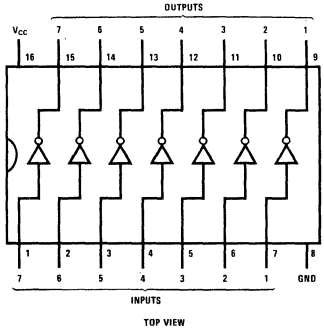
general description

The DS8844, DS8855, DS8864, DS8865 and DS8866 are cathode drivers for 7, 8 and 9 digit LED displays. They are designed to interface between MOS calculator or clock circuits supplying 2.0 mA, and LED displays operating up to 50 mA in a multiplex mode. The DS8864 and DS8866 feature a "low battery" indicator driver which will light a decimal point whenever a 9.0V battery drops below 6.5V typical.

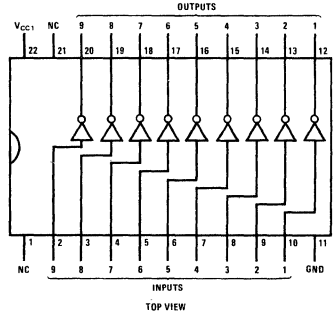
features

- Used with 50 mA LED displays
- "Low battery voltage" indicator
- Directly interfaced from MOS
- Inputs and outputs clustered for easy wiring
- Drivers consume no standby power

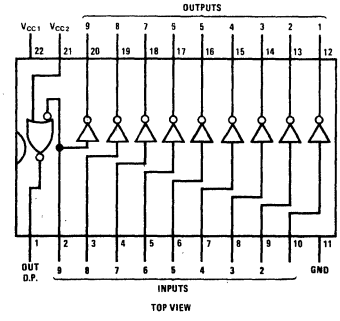
connection diagrams (Dual-In-Line Packages)



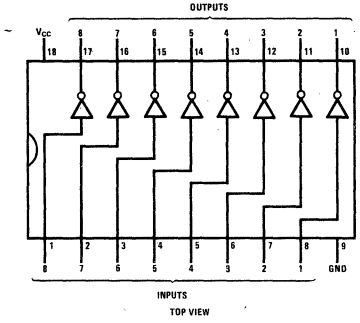
DS8844N



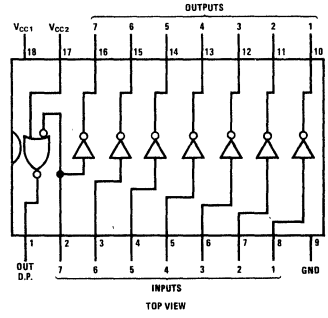
DS8855N



DS8864N

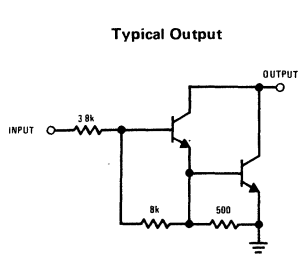


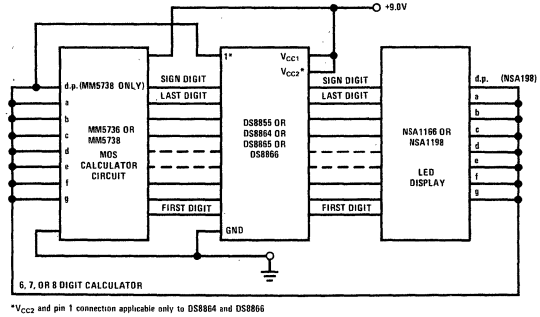
DS8865N



DS8866N

typical applications





*V_{CC2} and pin 1 connection applicable only to DS8864 and DS8866

6

absolute maximum ratings (Note 1)

Supply Voltage	11V
Input Voltage	11V
Output Voltage	8.0V
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	5.0	9.5	V
Temperature, T_A	0	+70	°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Max, I_{OL} = 50 mA		4.5	4.0		V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 6.5V		1.3	2.0	mA
			V_{IN} = 4.5V	0.50	0.65		mA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Max				0.4	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			40	60	μA
I_{DPON}	Decimal Point Output Current	V_{CC} = 6.00V, V_{DP} = 3.3V, V_{IN9} = 4.5V, (Pin 1), (Note 3)		−4.0	−6.0		mA
I_{DPOFF}	Decimal Point Output Current	V_{CC} = 7.0V, V_{DP} = 1.0V, V_{IN9} = 4.5V, (Pin 1), (Note 3)			−1.0	−50	μA
I_{OUT}	Output Current	V_{CC} = Min, V_{IN} = 4.5V, V_{OL} = 1.5V		−50			mA
I_{CEX}	Output Leakage Current	V_{CC} = Max, V_{OH} = 6.0V, I_{IN} = 40μA			1.0	40	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, V_{IN} = 4.5V, I_{OL} = 50 mA			1.0	1.5	V
I_{CC1}	Supply Current	V_{CC} = Max, V_{IN} = 0			0.001	0.1	mA
I_{CC2}	Decimal Point Supply Current	V_{CC} = Max, V_{IN} = 4.5V, V_{CC2} = Max			1.0	1.3	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range. All typical values applyf or T_A = 25°C.

Note 3: Not applicable to DS8844, DS8855 or DS8865.

NATIONAL

DS7856/DS8856, DS8857, DS7858/DS8858
BCD-to-7-segment LED drivers

general description

This series of 7-segment display drivers fulfills a wide variety of requirements for most active high (common cathode) Light Emitting Diodes (LEDs). Each device fully decodes a 4-bit BCD input into a number from 0 through 9 in the standard 7-segment display format, and BCD numbers above 9 into unique patterns that verify operation. All circuits operate off of a single 5.0V supply.

The DS7856/DS8856 has active-high, passive pull-up outputs which provide a typical source current of 6.0 mA at an output voltage of 1.7V. The applications are the same as for the DM5448/DM7448 except that more design freedom is allowed with higher source current levels. This circuit was designed to drive the MAN-4 or equivalent type display directly without the use of external current limit resistors, and replaces the MSD101.

The DS8857 has active-high outputs and is designed to be used with common cathode LED's in the multiplex mode. It provides a typical source current of 50 mA at an output voltage of 2.3V.

In addition, with the use of an external current limit résistor per segment, this circuit can be used in higher current non-multiplex LED applications. It replaces the MSD102.

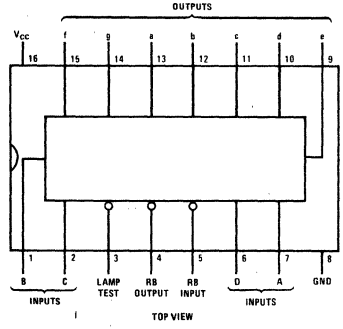
The DS7858/DS8858 has active high outputs with source current adjustable with the use of external current limit resistors, one per segment. This feature allows extreme flexibility in source current value selection for either multiplex or non-multiplex common cathode LED drive applications. It allows the system designer freedom to tailor the drive current for his particular applications.

features

- Lamp-test input
- Leading/trailing zero suppression (RBI and RBO)
- Blanking input that may be used to modulate lamp intensity or inhibit output
- TTL and DTL compatible
- Input clamping diodes

connection diagram

Dual-In-Line and Flat Package

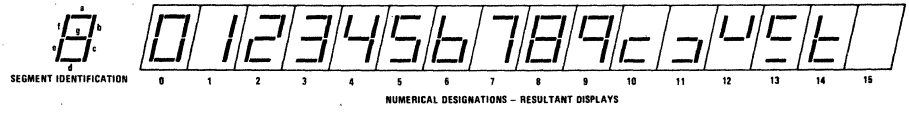


Order Number DS7856J, DS8856J, DS8857J, DS7858J, DS8858J

Order Number DS8856N or DS8858N

Order Number DS7856W or DS7858W

output display



6

absolute maximum ratings (Note 1)

Supply Voltage	7.0V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	600 mW

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7856, DS7858	4.5	5.5	V
DS8856, DS8857, DS8858	4.75	5.25	V
Temperature (T_A)			
DS7856, DS7858	−55	+125	°C
DS8856, DS8857, DS8858	0	+70	°C
Output Voltage			
All Circuits		5.5	V
Output Sink Current (per Segment)			
DS7856, DS8856		6.4	mA
Output Source Current (per Segment)			
DS8857		60	mA
DS7858, DS8858		50	mA

electrical characteristics (Note 2) The following is applicable to all parts.

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage			2.0			V
V_{IL}	Logical "0" Input Voltage					0.8	V
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −200μA, BI/RBO Node		2.4	3.7		V
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{IN} = 8.0 mA, BI/RBO Node			0.3	0.4	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, Except BI/RBO Node	V_{IN} = 2.4V			40	μA
			V_{IN} = 5.5V			1.0	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V	Except BI/RBO Node			−1.6	mA
			BI/RBO Node			−4.2	mA
I_{SC}	Output Short Circuit Current	V_{CC} = Max, BI/RBO Node				−4.0	mA
V_{CD}	Input Clamp Voltage	V_{CC} = 5.0V, T_A = 25°C, I_{IN} = −12 mA				−1.5	V

output characteristics and supply current

DS7856/DS8856 (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Logical "0" Output Voltage Outputs a through g	V_{CC} = Min, I_{OUT} = 6.4 mA			0.25	0.4	V
I_{OL}	Logical "1" Load Current Available, Outputs a through g	V_{CC} = 5.0V, V_{OUT} = 1.7V		−4.7	−6.0	−7.5	mA
I_{SC}	Output Short Circuit Current Outputs a through g	V_{CC} = Max, (Note 3)			−12	−15	mA
I_{CC}	Supply Current	V_{CC} = Max	DS7856		90	120	mA
			DS8856		90	130	mA

output characteristics and supply current (con't)

DS8857, DS7858/DS8858 (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
I_{OL}	Logical "1" Load Current Available, Outputs a through g	V_{CC} = 5.0V, V_{OUT} = 2.3V, DS8857		−40		−60	mA
V_{OH}	Logical "1" Output Voltage, Outputs a through g	V_{CC} = 5.0V, I_{OUT} = −50 mA, (Note 4)	DS7858	2.7	3.2		V
			DS8858	2.9	3.2		V
I_{CC}	Supply Current	V_{CC} = Max				60	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for DS7856, and DS7858 and across the 0°C to +70°C range for DS8856, DS8857 and DS8858. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: Care must be taken in not shorting the outputs to ground while they are in the "1" state because excessive current flow would result from the Darlington upper stages.

Note 4: Special care must be tken in the use of the DS7858 ceramic (J) and the DS8858 plastic (N) DIP's with regard to not exceeding the maximum operating junction temperature of the devices. The maximum junction temperature of the DS7858J is 175°C and must be derated based on a thermal resistance of 90°C/watt, junction to ambient. The maximum junction temperature for the DS8858N is 150°C and must be derated based on a thermal resistance of 120°C/watt junction to ambient.

truth table

	INPUTS						OUTPUTS								
DECIMAL OR FUNCTION	LT	RBI	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	NOTE
0	1	1	0	0	0	0	1	1	1	1	1	1	1	0	1
1	1	X	0	0	0	1	1	0	1	1	0	0	0	0	1
2	1	X	0	0	1	0	1	1	1	0	1	1	0	1	
3	1	X	0	0	1	1	1	1	1	1	1	0	0	1	
4	1	X	0	1	0	0	1	0	1	1	0	0	1	1	
5	1	X	0	1	0	1	1	1	0	1	1	0	1	1	
6	1	X	0	1	1	0	1	0	0	1	1	1	1	1	
7	1	X	0	1	1	1	1	1	1	1	0	0	0	0	
8	1	X	1	0	0	0	1	1	1	1	1	1	1	1	
9	1	X	1	0	0	1	1	1	1	1	0	0	1	1	
10	1	X	1	0	1	0	1	0	0	0	1	1	0	1	
11	1	X	1	0	1	1	1	0	0	1	1	0	0	1	
12	1	X	1	1	0	0	1	0	1	0	0	0	1	1	
13	1	X	1	1	0	1	1	1	0	0	1	0	1	1	
14	1	X	1	1	1	0	1	0	0	0	1	1	1	1	
15	1	X	1	1	1	1	1	0	0	0	0	0	0	0	
BI	X	X	X	X	X	X	0	0	0	0	0	0	0	0	2
RBI	1	0	0	0	0	0	0	0	0	0	0	0	0	0	3
LT	0	X	X	X	X	X	1	1	1	1	1	1	1	1	4

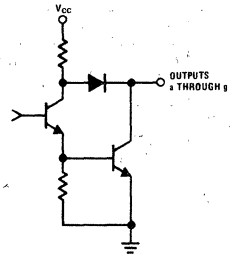
Note 1: BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO). The blanking input (BI) must be open or held at a logical "1" when output functions 0–15 are desired, and the ripple-blanking input (RBI) must be open or at a logical "1" if blanking of a decimal 0 is not desired. X = input may be high or low.

Note 2: When a logical "0" is applied directly to the blanking input (forced condition) all segment outputs go to a logical "1" regardless of the state of any other input condition.

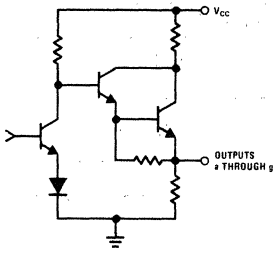
Note 3: When the ripple-blanking input (RBI) and inputs A, B, C and D are at logical "0," with the lamp test input at logical "1," all segment outputs go to a logical "1" and the ripple-blanking output (RBO) goes to a logical "0" (response condition).

Note 4: When the blanking input/ripple-blanking output (BI/RBO) is open or held at a logical "1," and a logical "0" is applied to the lamp-test input, all segment outputs go to a logical "0."

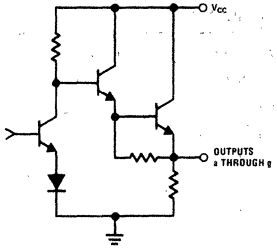
output stage schematics



DS7856/DS8856



DS8857



DS7858/DS8858

Display Drivers

DS8859, DS8869 open collector hex latch LED drivers

general description

The DS8859, DS8869 are TTL compatible open collector hex latch LED drivers with programmable current sink outputs. The current sinks are nominally set at 20 mA but may be adjusted by external resistors for any value between 0–40 mA. Each device contains six latches which may be set by input data terminals. An active low strobe common to all six latches enables the data input terminals. The DS8859 current sink outputs are switched on by entering a high level into the latches and the DS8869 current sink outputs are switched on by entering a low level into the latches.

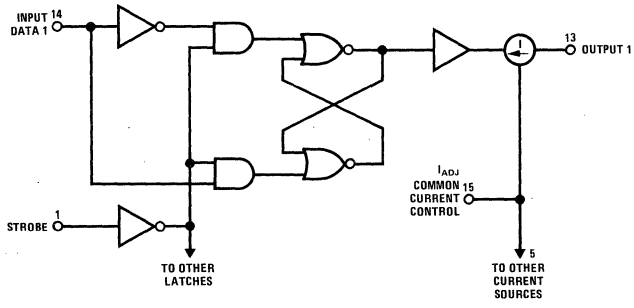
The devices are available in either a molded or cavity package. In order not to damage the devices there is a limit placed on the power dissipation allowable for each package type. This information is shown in the graph included in this data sheet.

features

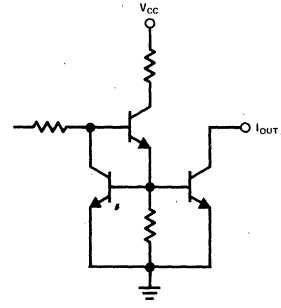
- Built-in latch
- Programmable output current
- TTL compatible inputs
- 40 mA output sink

logic diagram

DS8859

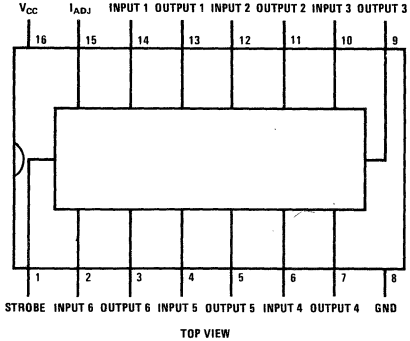


output circuit



connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DS8859J, DS8869J
or DS8859N, DS8869N

truth table

COMMON STROBE	INPUT DATA	DS8859 OUTPUT (t + 1)	DS8869 OUTPUT (t + 1)
0	0	OFF	ON
0	1	ON	OFF
1	X	OUTPUT (t)	OUTPUT (t)

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.75	5.25	V
Temperature, T_A	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 2.4V				40	μA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−1.0	−1.6	mA
V_{CD}	Input Clamp Voltage	I_{IN} = −12 mA			−1.1	−1.5	V
I_{OH}	Logical "1" Output Current	V_{CC} = Min, V_{IL} = 0.8V, V_{OH} = 5.5V, V_{IH} = 2.0V				250	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, I_{OL} = 16 mA, V_{IH} = 2V, V_{IADJ} = $V_{CC\,MIN}$		0.4			V
I_{CC}	Supply Current	V_{CC} = Max, Current Sources "OFF," (See Truth Table), (Note 4)				50	mA
I_{SINK}	Output Current	V_{CC} = 5.0V, V_{OUT} = 2.0V, T_A = 25°C, (Note 4)	V_{IADJ} = $V_{CC\,MIN}$	40			mA
			I_{ADJ} = Open	12	20	26	mA

switching characteristics

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to a Logical "0"	V_{CC} = 5.0V, T_A = 25°C, C_{OUT} = 15 pF, R_L = 390Ω, (Note 5)	Data to Output			36	ns
			Strobe to Output			50	ns
t_{pd1}	Propagation Delay to a Logical "1"	V_{CC} = 5.0V, T_A = 25°C, C_{OUT} = 15 pF, R_L = 390Ω, (Note 5)	Data to Output			150	ns
			Strobe to Output			150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

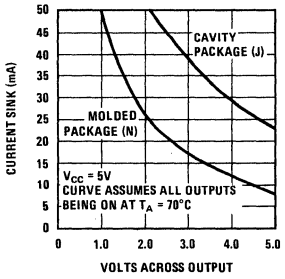
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: See graphs for changes in I_{SINK} versus changes in temperature and V_{CC}.

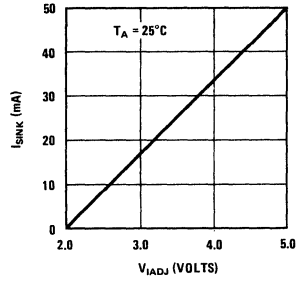
Note 5: C_{OUT} includes device output capacitance of approximately 8.5 pF and wiring capacitance.

typical performance characteristics

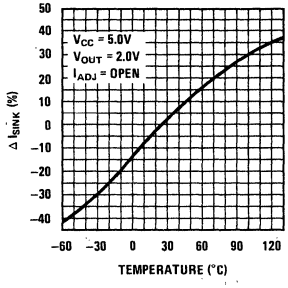
Max Power Dissipation Curves



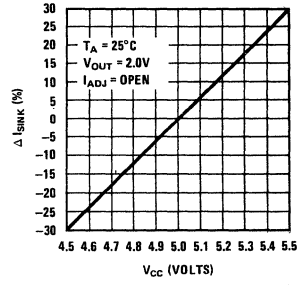
I_{SINK} vs V_{IADJ} (See Figure 1)



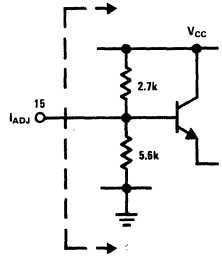
Δ I_{SINK} vs Temperature



Δ I_{SINK}/V_{CC}



I_{SINK} adjustment circuit



I_{ADJ} may be programmed by a voltage source or by resistors.

FIGURE 1.

NATIONAL

Display Drivers

DS8861 MOS-to-LED 5-segment driver
DS8863 MOS-to-LED 8-digit driver
DS8963 MOS-to-LED 8-digit driver

general description

The DS8861, DS8863 and DS8963 are designed to be used in conjunction with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays.

The DS8861 is a 5-segment driver capable of sinking or sourcing up to 50 mA from each driver.

The DS8863 is an 8-digit driver. Each driver is capable of sinking up to 500 mA.

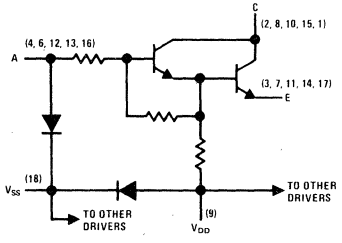
The DS8963 is identical to the DS8863 except it is intended for operation at up to 18V.

features

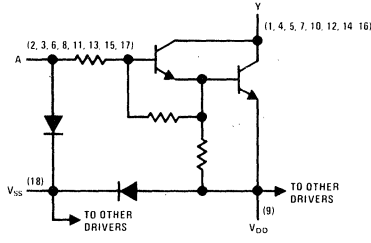
- 50 mA source or sink capability per driver, DS8861
- 500 mA sink capability per driver, DS8863, DS8963
- MOS compatibility (low input current)
- Low standby power
- High gain Darlington circuits

schematic and connection diagrams

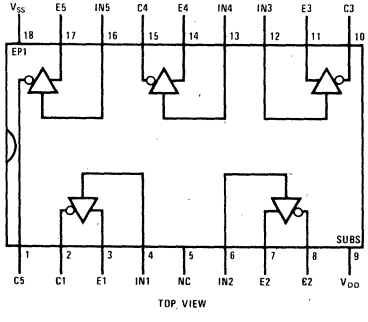
DS8861



DS8863/DS8963

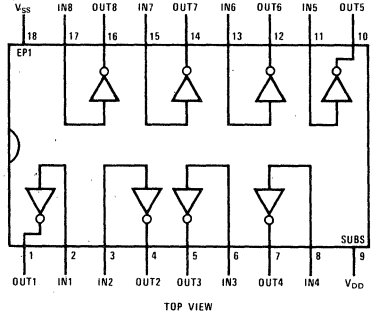


Dual-In-Line Package



TOP VIEW

Dual-In-Line Package



TOP VIEW

Order Numbers DS8861N, DS8863N or DS8963N

absolute maximum ratings

	DS8861	DS8863	DS8963
Input Voltage Range (Note 1)	−5V to V_{SS}	−5V to V_{SS}	−5V to V_{SS}
Collector (Output) Voltage (Note 2)	10V	10V	18V
Collector (Output)-to-Input Voltage	10V	10V	18V
Emitter-to-Ground Voltage ($V_I \geq 5V$)	10V		
Emitter-to-Input Voltage	5V		
Voltage at V_{SS} Terminal With Respect to Any Other Device Terminal	10V	10V	18V
Collector (Output) Current			
Each Collector (Output)	50 mA	500 mA	500 mA
All Collectors (Output)	200 mA	600 mA	600 mA
Continuous Total Dissipation	800 mW	800 mW	800 mW
Operating Temperature Range	0°C to +70°C	0°C to +70°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C	300°C	300°C

dc electrical characteristics

DS8861 (V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{CEON}	"ON" State Collector Emitter Voltage	Input = 8V through 1 kΩ, V_E = 5V, I_C = 50 mA	T_A = 25°C		0.9	1.2	V
						1.5	V
I_{COFF}	"OFF" State Collector Current	V_C = 10V, V_E = 0	I_{IN} = 40μA			100	μA
			V_{IN} = 0.7V			100	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, V_E = 0, I_C = 20 mA			2.2	3.3	mA
I_E	Emitter Reverse Current	V_{IN} = 0, V_E = 5V, I_C = 0				100	μA
I_{SS}	Current Into V_{SS} Terminal					1	mA

DS8863/DS8963 (V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Low Level Output Voltage	V_{IN} = 7V, I_{OUT} = 500 mA	T_A = 25°C			1.5	V
						1.6	V
I_{OH}	High Level Output Current	V_{OH} = 10V*	I_{IN} = 40μA			250	μA
			V_{IN} = 0.5V			250	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, I_{OL} = 20 mA				2	mA
I_{SS}	Current Into V_{SS} Terminal					1	mA

*18V for the DS8963

ac switching characteristics

DS8861 (V_{SS} = 7.5V, T_A = 25°C)

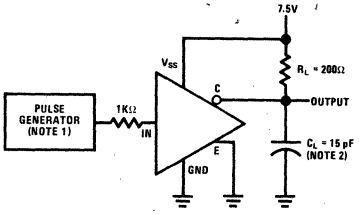
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output (Collector)	V_{IH} = 4.5V, V_E = 0		100		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output (Collector)	R_L = 200Ω, C_L = 15 pF		20		ns

DS8863/DS8963 (V_{SS} = 7.5V, T_A = 25°C)

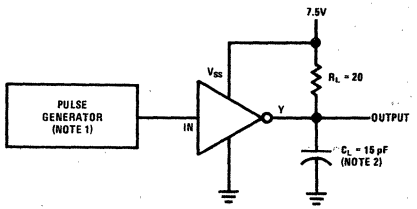
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{IH} = 8V, R_L = 21Ω,		300		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF		30		ns

Note 1: The input is the only device terminal which may be negative with respect to ground.
Note 2: Voltage values are with respect to network ground terminal unless otherwise noted.

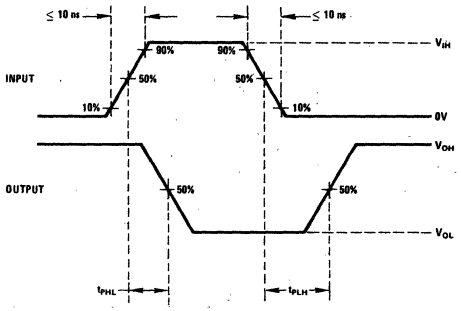
ac test circuits and waveforms



DS8861



DS8863



NOTE 1: THE PULSE GENERATOR HAS THE FOLLOWING CHARACTERISTICS: Z_{OUT} = 50Ω, PRR = 100 KHz, t_W = 1μs.

NOTE 2: C_L INCLUDES PROBE AND JIG CAPACITANCE.

Display Drivers

NATIONAL

DS8867 8-segment driver

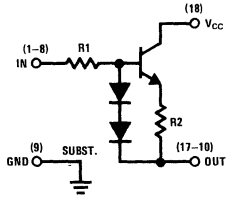
general description

The DS8867 is an 8-segment driver designed to be driven from MOS circuits operating at 8V ±10% minimum V_{SS} supply and will supply 14 mA to a LED display. The output current is insensitive to V_{CC} variations.

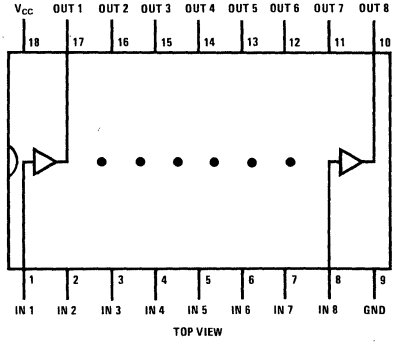
features

- Internal current control—no external resistors
- 100% efficient, no standby power
- Operates in three and four cell battery systems
- Inputs and outputs grouped for easy PC layout

schematic and connection diagrams



Dual-In-Line Package

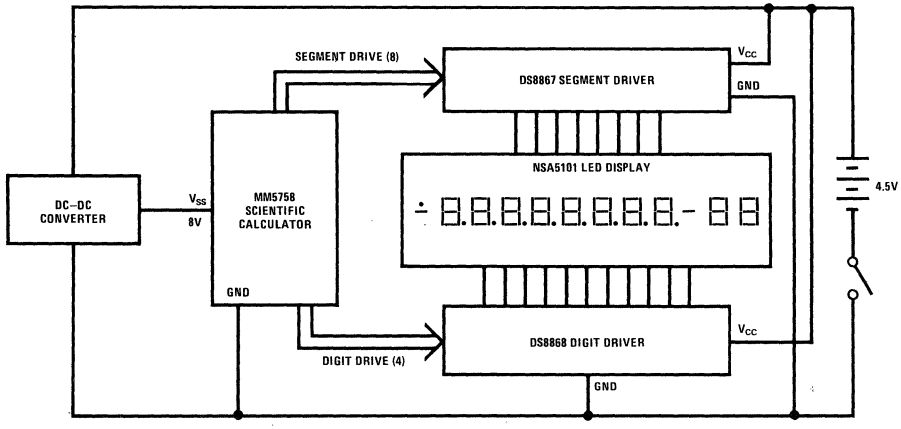


TOP VIEW

Order Number DS8867N

typical application

Typical 3 Cell Scientific Calculator Circuit



absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	10V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	3.3	6.0	V
Temperature, T_A	0	+70	°C

electrical characteristics (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min, V_{OH} = 2.3V, I_{IH} = 500μA			4.9	5.4	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{OL} = 1.8V, V_{IL} = 2.0V			0.1	10	μA
I_{OH}	Logical "1" Output Current	V_{CC} = Min, V_{OH} = 2.3V, I_{IH} = 500μA		−8	−14	−18	mA
I_{OL}	Logical "0" Output Current	V_{CC} = Max, V_{OL} = 1.0V, V_{IL} = 1.3V			−0.5	−10	μA
$I_{CC\ OFF}$	Supply Current	V_{CC} = Max	All V_{OL} = 1.0V, V_{IL} = 1.3V, (Standby)		4	50	μA
$I_{CC\ ON}$			All V_{OH} = 2.3V, V_{IH} = 7.8V		112	150	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C

NATIONAL

DS8868 12-digit decoder/driver

general description

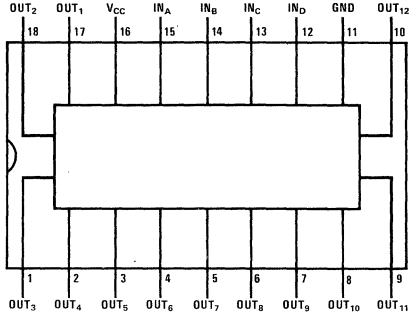
The DS8868 is a 12-digit decoder/driver designed to drive LED displays like the NSA5101 from the MM5758 calculator chip or equivalent which supplies a 4-line coded input (see truth table). It is designed to operate from a 3 cell battery (3.3V to 4.5V) and features a low battery indicator. The DS8868 can sink up to 110 mA min on each output.

features

- Direct interface with MM5758 calculator
- Low battery indicator
- 110 mA sink capability
- Low voltage operation

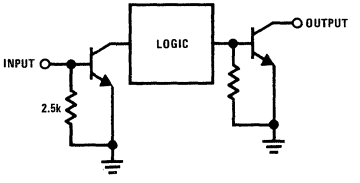
connection diagram

Dual-In-Line Package



Order Number DS8868J or DS8868N

equivalent schematic



truth table

INPUTS				OUTPUTS*											
IN_A	IN_B	IN_C	IN_D	O1	O2	O3	O4	O5	O6	O7	O8	O9	O10	O11	O12
L	L	L	H	L											
H	L	L	L		L										
H	H	L	L			L									
L	H	H	L				L								
H	L	H	H					L							
L	H	L	H						L						
H	L	H	L							L					
H	H	L	H								L				
H	H	H	L									L			
H	H	H	H										L		
L	L	H	H											L	
L	H	H	H												L

*A blank implies an H

absolute maximum ratings (Note 1)

Supply Voltage	6V
Input Current	10 mA
Output Voltage	9V
Storage Temperature Range	−65 to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	3.3	4.5	V
Temperature, T_A	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{CC} = Min, Selected Output $V_{OL} \leq 0.4V$		300	450	μA
V_{ILV}	Low Voltage Indicator (Measured on Pin 15)	V_{CC} = 3.1V, T_A = 25°C, $I_{INC} = I_{IND}$ = 450μA	2.8			V
I_{IL}	Logical "0" Input Current	V_{CC} = Min, Selected Output $I_{OM} \leq 50\mu A$	100	300		μA
I_{OH}	Logical "1" Output Current	V_{CC} = Max, V_{OH} = 7.0V, All Outputs "OFF"			100	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OL} = 110 mA			0.5	V
I_{CC}	Supply Current "OFF"	V_{CC} = Max, All Outputs "OFF", V_{OH} = 5V			8.0	mA
I_{CC}	Supply Current "ON"	V_{CC} = Max, One Output Selected			11.0	mA

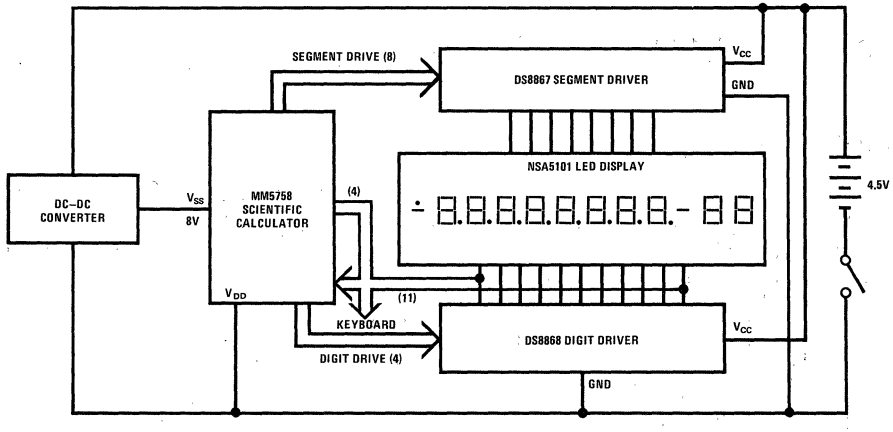
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Conditions" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for V_{CC} = 4.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

typical application

Typical 3-Cell Scientific Calculator Circuit



DS8870 hex LED digit driver

general description

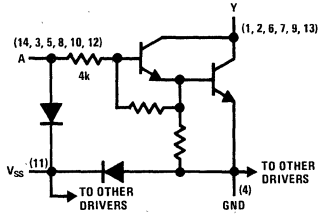
The DS8870 is an interface circuit designed to be used in conjunction with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays. The number of drivers required for this time-multiplexed system is minimized as a result of the segment-address-and-digit-scan method of LED drive.

features

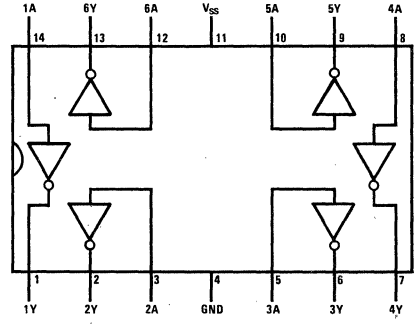
- Sink capability per driver—350 mA
- MOS compatibility (low input current)
- Low standby power
- High-gain Darlington circuits

schematic and connection diagrams

DS8870 (Each Driver)



Dual-In-Line Package



Order Number DS8870N
or DS8870J

absolute maximum ratings (Note 1)

Input Voltage Range (Note 4)	−5V to V_{SS}
Collector Output Voltage	10V
Collector Output to Input Voltage	10V
Voltage at V_{SS} Terminal with Respect to Any Other Device Terminal	10V
Collector Output Current	
Each Collector Output	350 mA
All Collector Outputs	600 mA
Continuous Total Dissipation	800 mW
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics (V_{SS} = 10V, T_A = 0°C to +70°C) (Notes 2 and 3)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OL}	Low Level Output Voltage	Input = 6.5V through 1 kΩ, I_{OUT} = 350 mA, T_A = 25°C		1.2	1.4	V
V_{OL}	Low Level Output Voltage	Input = 6.5V through 1 kΩ, I_{OUT} = 350 mA			1.6	V
I_{OH}	High Level Output Current	V_{OH} = 10V, I_{IN} = 40μA			200	μA
I_{OH}	High Level Output Current	V_{OH} = 10V, V_{IN} = 0.5V			200	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, I_{OL} = 20 mA		2.2	3.3	mA
I_{SS}	Current Into V_{SS} Terminal				1	mA

ac switching characteristics (V_{SS} = 7.5V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{IH} = 7.5V, R_L = 39Ω, C_L = 15 pF		300		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	V_{IH} = 7.5V, R_L = 39Ω, C_L = 15 pF		30		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: The input is the only device terminal which may be negative with respect to ground.

NATIONAL

DS8871, DS8872, DS8873, DS8977 saturating LED cathode drivers

general description

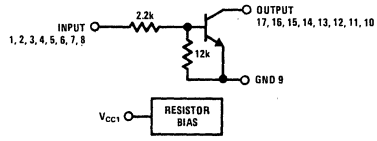
The DS8871, DS8872, DS8873 and DS8977 are bipolar integrated circuits designed to interface between MOS calculator circuits and common cathode LED displays operating in the multiplexed mode with a digit current of up tp 40 milliamps. The DS8871 is an 8-digit driver; the DS8872 is a 9-digit driver; and the DS8873 is a 9-digit driver with a built-in battery condition indicator that turns on the digit 9 decimal point when the battery voltage drops to 6.5V (typical). The DS8977 is a 7-digit version of the DS8873. In a typical calculator system operating on a 9V battery, the low battery indicator comes on as a warning that the battery should be replaced. But the calculator (MM5737 or equivalent) will still function properly for awhile.

features

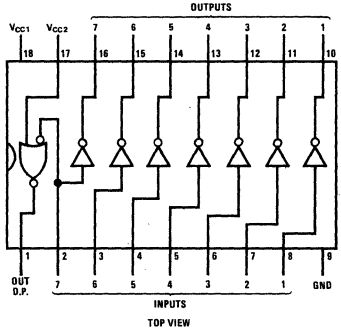
- Single saturating transistor output
- Low battery indicator
- MOS compatible inputs
- Inputs and outputs clustered for easy wiring
- Drivers consume no standby power

schematic and connection diagrams

DS8871

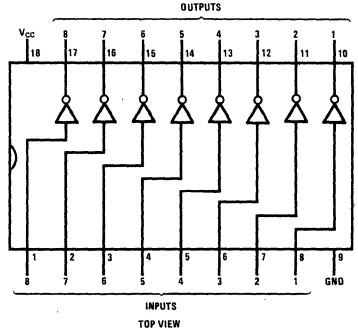


Dual-In-Line Package



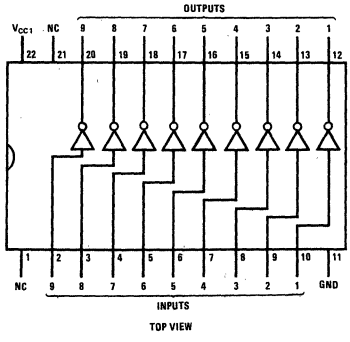
Order Number DS8977N

Dual-In-Line Package



Order Number DS8871N

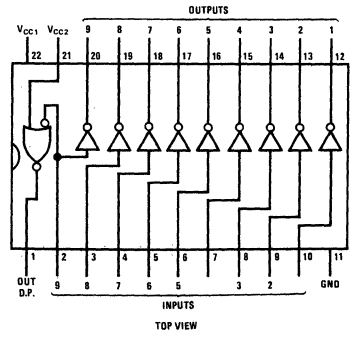
Dual-In-Line Package



*Make no connection to these pins.

Order Number DS8872N

Dual-In-Line Package



Order Number DS8873N

absolute maximum ratings (Note 1)

Supply Voltage	V_{CC1} = 11V
Supply Voltage (Note 4)	V_{CC2} = 11V
Input Voltage	11V
Output Voltage	8V
Storage Temperature Range	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC1}	4.0	9.5	V
Supply Voltage, V_{CC2} (Note 4)	4.0	9.5	V
Temperature, T_A	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V		1	45	μA
I_{IH}	Logical "1" Input Current	V_{IN} = 4.5V		1.7	2.5	mA
V_{OL}	Logical "0" Output Voltage	V_{IN} = 3.2V, I_{OL} = 40mA		0.35	0.5	V
I_{OL}	Logical "0" Output Current	V_{IN} = 3.2V, V_{OL} = 0.5V	40			mA
I_{CEX}	Output Leakage Current	V_{OH} = 6.0V, I_{IN} = 25μA			40	μA
$I_{DP(ON)}$	Decimal Point Output Current	V_{CC2} = 6.25V, V_{DP} = 2.5V, V_{IN9} = 3.2V (Note 4)	−5.0	−7.0		mA
$I_{DP(OFF)}$	Decimal Point Output Current	V_{CC2} = 7.0V, V_{IN9} = 3.2V, V_{DP} = 1.0V (Note 4)		−1	−100	μA
I_{CC1}	Supply Current, V_{CC1}	V_{CC1} = 6.5V, V_{IN} = 0.0V		1	100	μA
I_{CC2}	Supply Current, V_{CC2}	V_{CC2} = 11.3V, V_{IN9} = 4.5V (Note 4)		0.9	1.2	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Applies to DS8873 only.

typical applications

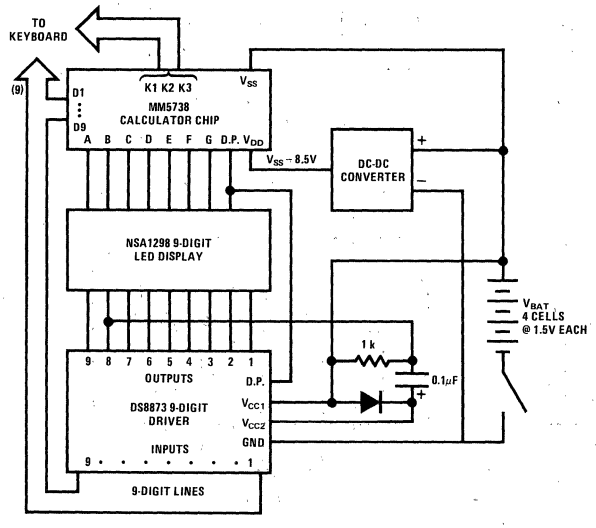


FIGURE 1. 4-Cell System

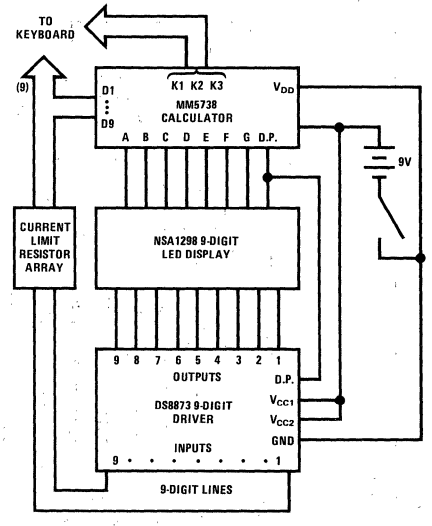


FIGURE 2. 9V System

NATIONAL

Display Drivers
Advance Information*

DS8874, DS8876, DS8879 9-digit shift input LED drivers

general description

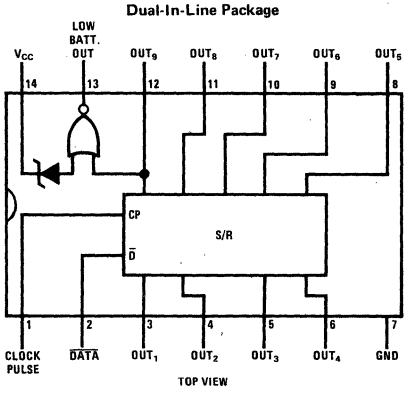
The DS8874, DS8876 and DS8879 are 9-digit LED drivers which incorporate a shift register input decoding circuit and a low battery indicator. Their outputs will sink 50 mA at less than 0.5V drop when sequentially selected. The DS8874 outputs are collectors pulled up to V_{CC} with internal 20k resistors. The DS8876 and DS8879 outputs are open collectors. When the V_{CC} supply falls below 6.5V typical on the DS8874 or 4.3V typical on the DS8876 or 3.2V typical on the DS8879, pin 13 will supply segment current at digit 9 time to indicate a low battery condition. This pin is generally connected to the decimal point segment on the display so that when a low battery condition exists, the left-most decimal point lights up. The digit drivers are intended to be used with the MM5784N five-function, nine-digit accumulating memory calculator circuit, or any other circuit which supplies the nine-digit information in a similar serial format.

features

- 50 mA digit sink
- Low battery indicator
- Minimum number of connections
- MOS compatible inputs

connection diagram

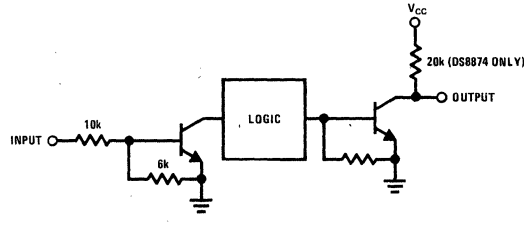
Dual-In-Line Package



TOP VIEW

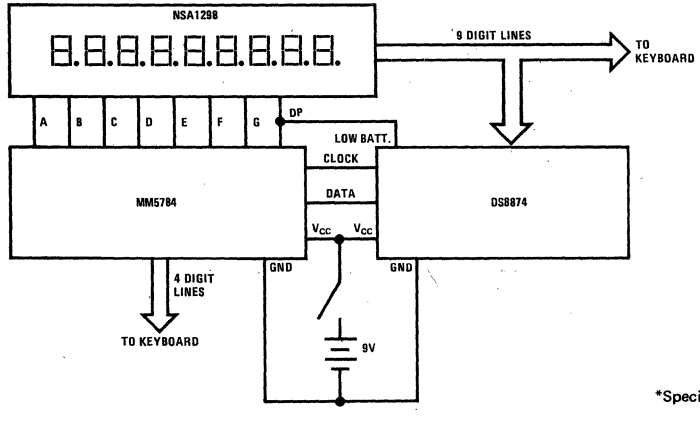
Order Number DS8874J, DS8876J, DS8879J
DS8874N, DS8876N or DS8879N

equivalent schematic



typical application

Typical Application of the DS8874 Digit Driver with the MM5784 5-Function Calculator Circuit, NSA1298 9-Digit LED Display and a 9V Battery.



*Specifications may change

6

absolute maximum ratings (Note 1)

Supply Voltage	10V
Input Voltage	10V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS8874	6.0	9.5	V
DS8876	4.4	6.0	V
DS8879	3.3	4.5	V
Temperature, T_A	0	+70	°C

electrical characteristics

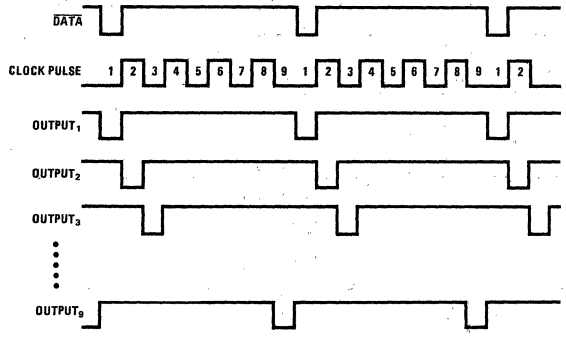
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Max		3.0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 6.5V		0.35	0.6	1.0	mA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Max				0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.8V			0.05	0.1	mA
V_{CCL}	Decimal Point "ON"	V_{dp} = 2.3V, I_{dp} = −4 mA, O_9 = V_{OL}	DS8874			6.0	V
			DS8876			4.0	V
			DS8879			3.1	V
V_{CCH}	Decimal Point "OFF"	V_{dp} = 1.0V, I_{dp} = −10μA, O_9 = V_{OL}	DS8874	7.0	6.5		V
			DS8876	4.7	4.4		V
			DS8879	3.5	3.3		V
V_{OH}	Logical "1" Output Voltage	V_{CC} = Max, Output Not Selected	DS8874 Only	9.0			V
I_{OH}	Logical "1" Output Current	V_{CC} = Max, Output Not Selected	DS8876, DS8879			20	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, Output Selected, I_{o1} = 50 mA				0.5	V
I_{OL}	Logical "0" Output Current	V_{CC} = Min, Output Selected, V_{OL} = 0.5V		50			mA
I_{CC}	Supply Current	V_{CC} = Max, One Output Selected			6.2	9.0	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

timing diagram (Upper Level More Positive)



DS8877 6-digit LED driver

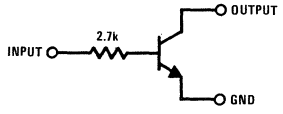
general description

The DS8877 is a 6-digit LED driver designed as a pin-for-pin replacement for the DS75492 in applications where digit current is in the 5 to 50 mA range. Since the outputs saturate to less than 0.6V, the DS8877 will work on lower battery voltages than most digit drivers. The DS8877 draws *no* standby power.

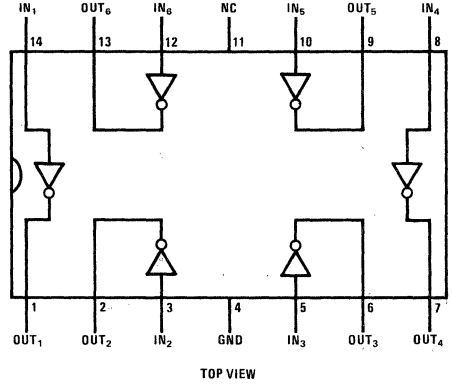
features

- No standby power
- No supply connection
- Operates in 4.5V,6V or 9V systems
- Pin-for-pin replacement for DS75492 in low current applications

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS8877J or DS8877N

absolute maximum ratings (Note 1)

Supply Voltage	None Required
Input Voltage	10V
Output Voltage	10V
Operating Temperature Range	0 to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Notes 2 and 3)

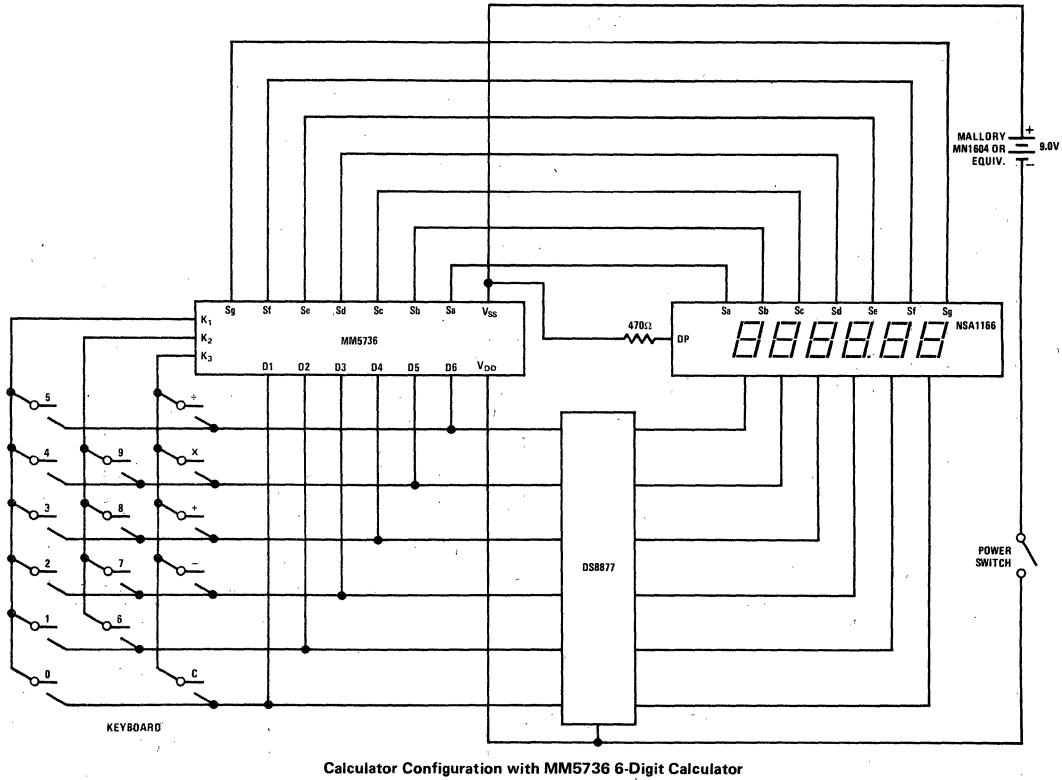
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage		5.0			V
I_{IH}	Logical "1" Input Current	V_{IH} = 5.0V			1.2	mA
V_{IL}	Logical "0" Input Voltage				0.35	V
I_L	Logical "0" Input Current	V_{IL} = 0.35V			20	μA
I_{CEX}	Logical "1" Output Current	V_C = 8.0V, V_{IN} = 0.35V			100	μA
V_{OL}	Logical "0" Output Voltage	I_{OL} = 35 mA, V_{IN} = 5.0V			0.5	V
I_{OL}	Logical "0" Output Current	V_{OL} = 0.5V, V_{IN} = 5.0V	35	50		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

typical application



Calculator Configuration with MM5736 6-Digit Calculator

Display Drivers

DS7880/DS8880 high voltage 7-segment decoder/driver (for driving Panaplex II™ and Sperry/Beckman displays)

general description

The DS7880/DS8880 is custom designed to decode four lines of BCD and drive a gas-filled seven-segment display tube.

Each output constitutes a switchable, adjustable current sink which provides constant current to the tube segment, even with high tube anode supply tolerance or fluctuation. These current sinks have a voltage compliance from 3V to at least 80V; typically the output current varies 1% for output voltage changes of 3 to 50V. Each bit line of the decoder switches a current sink on or off as prescribed by the input code. Each current sink is ratioed to the b-output current as required for even illumination of all segments.

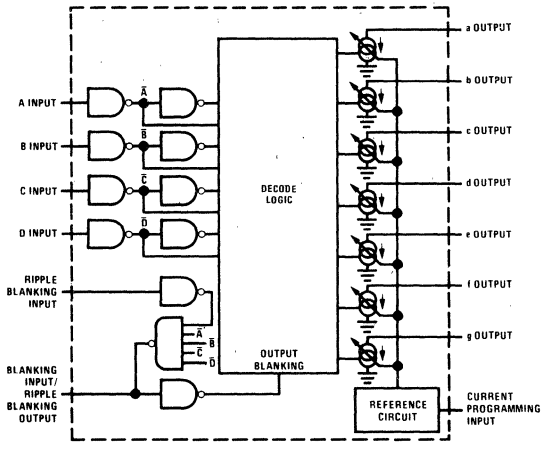
Output currents may be varied over the 0.2 to 1.5 mA range for driving various tube types or multiplex operation. The output current is adjusted by connecting an external program resistor (R_P) from V_{CC} to the Program input in accordance with the programming curve. The circuit design provides a one-to-one correlation between program input current and b-segment output current.

The Blanking Input provides unconditional blanking of any output display, while the Ripple Blanking pins allow simple leading- or trailing-zero blanking.

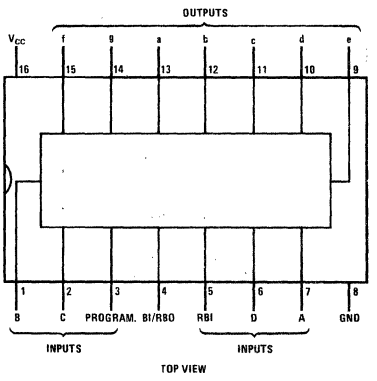
features

- Current sink outputs
- Adjustable output current – 0.2 to 1.5 mA
- High output breakdown voltage – 110V typ
- Suitable for multiplex operation
- Blanking and Ripple Blanking provisions
- Low fan-in and low power

logic and connection diagrams



Dual-In-Line Package



Order Number DS7880J or DS8880J

Order Number DS8880N

absolute maximum ratings (Note 1)

V_{CC}	7V
Input Voltage (Except BI)	6V
Input Voltage (BI)	V_{CC}
Segment Output Voltage	80V
Power Dissipation	600 mW
Transient Segment Output Current (Note 4)	50 mA
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7880	4.5	5.5	V
DS8880	4.75	5.25	V
Temperature (T_A)			
DS7880	−55	+125	C
DS8880	0	+70	C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
V_{OH}	Logical "1" Output Voltage	V_{CC} = Min, I_{OUT} = −200μA, RBO		2.4	3.7		V
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OUT} = 8 mA, RBO			0.13	0.4	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, Except BI	V_{IN} = 2.4V		2	15	μA
			V_{IN} = 5.5V		4	400	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V	Except BI		−300	−600	μA
			BI		−1.2	−2.0	mA
I_{CC}	Power Supply Current	V_{CC} = Max, R_P = 2.2k, All Inputs = 0V			27	43	mA
V_{CD}	Input Diode Clamp Voltage	V_{CC} = Max, T_A = 25°C, I_{IN} = −12 mA			−0.9	−1.5	V
ΔI_O	SEGMENT OUTPUTS "ON" Current Ratio	All Outputs = 50V, I_{OUT}b = Ref.	Outputs a, f, and g	0.84	0.93	1.02	
			Output c	1.12	1.25	1.38	
			Output d	0.90	1.00	1.10	
			Output e	0.99	1.10	1.21	
$I_{b\ ON}$	Output b "ON" Current	V_{CC} = 5V, V_{OUT}b = 50V, All Other Outputs ≥ 5V, T_A = 25°C	R_P = 18.1k	0.15	0.20	0.25	mA
			R_P = 7.03k	0.45	0.50	0.55	mA
			R_P = 3.40k	0.90	1.00	1.10	mA
			R_P = 2.20k	1.35	1.50	1.65	mA
V_{SAT}	Output Saturation Voltage	V_{CC} = Min, R_P = 1k±5%, I_{OUT}b = 2 mA, (Note 5)			0.8	2.5	V
I_{CEX}	Output Leakage Current	V_{OUT} = 75V, BI = 0V, R_P = 2.2k			0.003	3	μA
V_{BR}	Output Breakdown Voltage	I_{OUT} = 250μA, BI = 0V, R_P = 2.2k		80	110		V
t_{pd}	Propagation Delays	V_{CC} = 5V, T_A = 25°C					
	BCD Input to Segment Output				0.4	10	μs
	BI to Segment Output				0.4	10	μs
	RBI to Segment Output				0.7	10	μs
	RBI to RBO				0.4	10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7880 and across the 0°C to +70°C range for the DS8880. All typical values are for T_A = 25°C and V_{CC} = 5V.

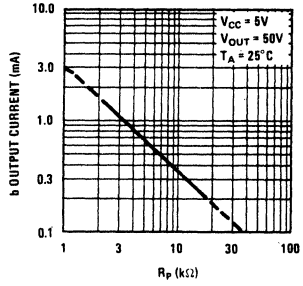
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: In all applications transient segment output current must be limited to 50 mA. This may be accomplished in dc applications by connecting a 2.2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

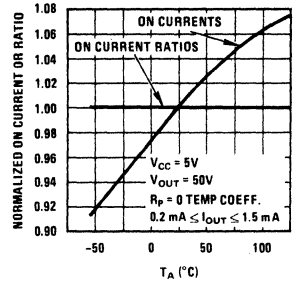
Note 5: For saturation mode the segment output currents are externally limited and ratioed.

typical performance characteristics

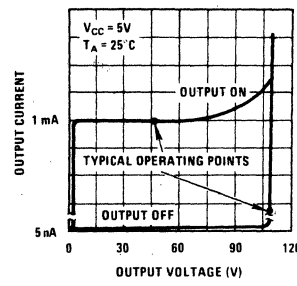
Output Current Programming



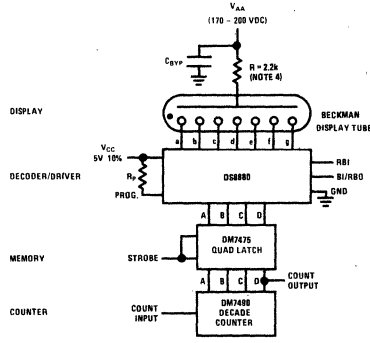
On Currents vs Temperature



Output Characteristic



typical application



truth table

DECIMAL OR FUNCTION	RBI†	D	C	B	A	BI/RBO	a	b	c	d	e	f	g	DISPLAY
0	1	0	0	0	0	1	0	0	0	0	0	0	1	0
1	X	0	0	0	1	1	1	0	0	1	1	1	1	1
2	X	0	0	1	0	1	0	0	1	0	0	1	0	2
3	X	0	0	1	1	1	0	0	0	0	1	1	0	3
4	X	0	1	0	0	1	1	0	0	1	1	0	0	4
5	X	0	1	0	1	1	0	1	0	0	1	0	0	5
6	X	0	1	1	0	1	0	1	0	0	0	0	0	6
7	X	0	1	1	1	1	0	0	0	1	1	1	1	7
8	X	1	0	0	0	1	0	0	0	0	0	0	0	8
9	X	1	0	0	1	1	0	0	0	0	1	0	0	9
10	X	1	0	1	0	1	0	0	0	1	0	0	0	A
11	X	1	0	1	1	1	1	1	0	0	0	0	0	b
12	X	1	1	0	0	1	0	1	1	0	0	0	1	C
13	X	1	1	0	1	1	1	0	0	0	0	1	0	d
14	X	1	1	1	0	1	0	1	1	0	0	0	0	E
15	X	1	1	1	1	1	0	1	1	1	0	0	0	F
BI*	X	X	X	X	X	0*	1	1	1	1	1	1	1	
RBI	0	0	0	0	0	0	1	1	1	1	1	1	1	

*Bi/RBO used as input only

†X = Don't care

SEGMENT IDENTIFICATION

6

NATIONAL

DS8884A high voltage cathode decoder/driver (for driving Panaplex II™ and Sperry/Beckman displays)

general description

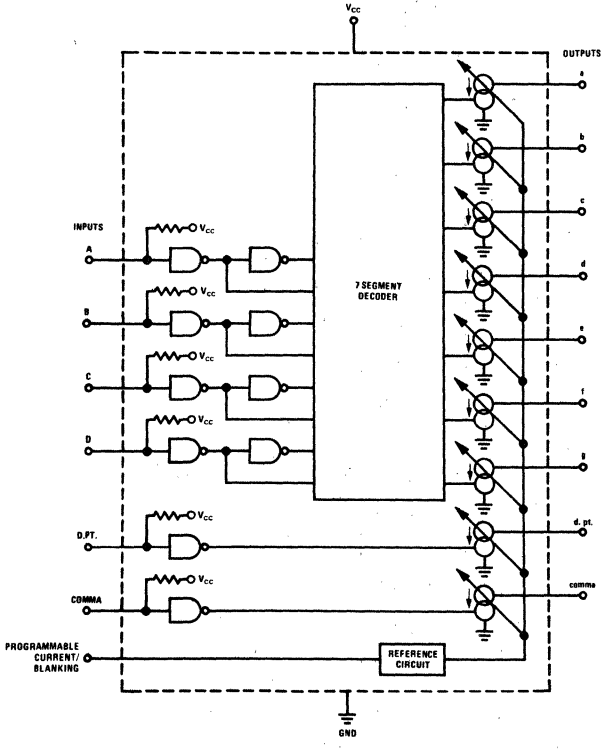
The DS8884A is designed to decode four lines of BCD input and drive seven-segment digits of gas-filled readout displays. Two separate inputs are provided for driving the decimal point and comma cathodes.

All outputs consist of switchable and programmable current sinks which provide constant current to the tube cathodes, even with high tube anode supply tolerance. Output currents may be varied over the 0.2 to 1.2 mA range for multiplex operation. The output current is adjusted by connecting an external program resistor (R_P) from V_{CC} to the program input in accordance with the programming curve.

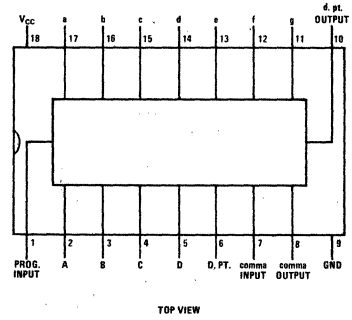
features

- Usable with AC or DC input coupling
- Current sink outputs
- High output breakdown voltage
- Low input load current
- Intended for multiplex operation.
- Input pullups increase noise immunity

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS8884AN

absolute maximum ratings (Note 1)

V_{CC}	7V
Input Voltage (Note 4)	V_{CC}
Segment Output Voltage	80V
Power Dissipation	600 mW
Transient Segment Output Current (Note 5)	50 mA
Storage Temperature Range	−65°C to +150°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.25	V
Temperature (T_A)	0	+70	°C

electrical characteristics ($0°C \leq T_A \leq 70°C$ – Unless otherwise noted) (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = 4.75V		2.0		V
V_{IL}	Logical "0" Input Voltage	V_{CC} = 4.75V			1.0	V
I_{IH}	Logical "1" Input Current	V_{CC} = 5.25V, V_{IN} = 2.4V			15	μA
I_{IL}	Logical "0" Input Current	V_{CC} = 5.25V, V_{IN} = 0.4V			−250	μA
I_{CC}	Power Supply Current	V_{CC} = 5.25V, R_P = 2.8k, All Inputs = 5V			40	mA
V_{I+}	Positive Input Clamp Voltage	V_{CC} = 4.75V, I_{IN} = 1 mA		5.0		V
V_{I-}	Negative Input Clamp Voltage	V_{CC} = 5V, I_{IN} = −12 mA, T_A = 25°C			−1.5	V
	SEGMENT OUTPUTS					
ΔI_O	"ON" Current Ratio	All Outputs = 50V, I_{OUT} b = Ref., All Outputs		0.9	1.1	
$I_{b\ ON}$	Output b "ON" Current	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C	R_P = 18.1k	0.15	0.25	mA
			R_P = 7.03k	0.45	0.55	mA
			R_P = 3.40k	0.90	1.10	mA
			R_P = 2.80k	1.08	1.32	mA
I_{CEX}	Output Leakage Current	V_{OUT} = 75V			5	μA
V_{BR}	Output Breakdown Voltage	I_{OUT} = 250μA		80		V
t_{pd}	Propagation Delay of Any Input to Segment Output	V_{CC} = 5V, T_A = 25°C			10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS8884A. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: This limit can be higher for a current limiting voltage source.

Note 5: In all applications transient segment output current must be limited to 50 mA. This may be accomplished in dc applications by connecting a 2.2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode driver in multiplex applications.

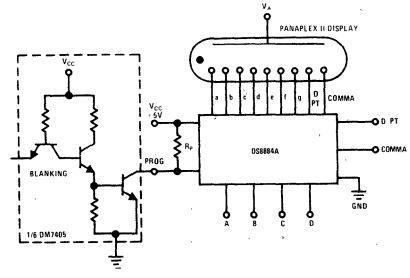
truth table

FUNCTION	D.PT.	COMMA	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
0	1	1	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	1	1	0	0	1	1	1	1	1
2	1	1	0	0	1	0	0	0	1	0	0	1	0	2
3	1	1	0	0	1	1	0	0	0	0	1	1	0	3
4	1	1	0	1	0	0	1	0	0	1	1	0	0	4
5	1	1	0	1	0	1	0	1	0	0	1	0	0	5
6	1	1	0	1	1	0	0	0	1	0	0	0	0	6
7	1	1	0	1	1	1	0	0	0	1	1	1	1	7
8	1	1	1	0	0	0	0	0	0	0	0	0	0	8
9	1	1	1	0	0	1	0	0	0	0	1	0	0	9
10	1	1	1	0	1	0	1	1	0	0	0	1	1	10
11	1	1	1	0	1	1	1	1	0	0	0	1	0	11
12	1	1	1	1	0	0	0	1	1	1	1	0	0	12
13	1	1	1	1	0	1	0	1	1	0	0	0	0	13
14	1	1	1	1	1	0	1	1	1	1	1	1	0	14
15	1	1	1	1	1	1	1	1	1	1	1	1	1	15
*D.PT	0	1	X	X	X	X	X	X	X	X	X	X	X	▫
*Comma	0	0	X	X	X	X	X	X	X	X	X	X	X	▫

□ Decimal Point
ρ Comma

*Decimal point and comma can be displayed with or without any numeral.

typical application



typical performance characteristics (see DS7880 data sheet)

NATIONAL

Display Drivers

DS7885/DS8885 MOS to high voltage cathode buffer

general discription

The DS7885/DS8885 interfaces MOS calculator or counter-latch-decoder-driver circuits directly to 7-segment high-voltage gas-filled displays. The six inputs A, B, D, E, F, G are decoded to drive the seven segment of the tube.

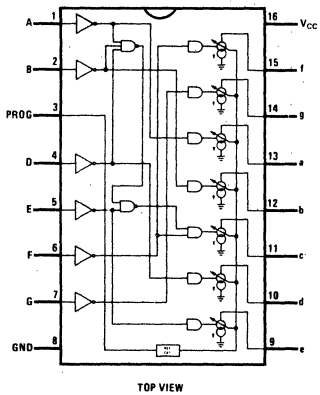
Each output constitutes a switchable, adjustable current source which provides constant current to the tube segment, even with high tube anode supply tolerance or fluctuation. These current sources have a voltage compliance from 3V to at least 80V. Each current source is ratioed to the b-output current as required for even illumination of all segments. Output currents may be varied over the 0.2 to 1.5 mA range for driving various tube types or multiplex operation. The output current is adjusted by connecting a program resistor (R_P) from V_{CC} to the program input.

features

- Current source outputs
- Adjustable output currents 0.2 to 1.5 mA
- High output breakdown voltage 80V min
- Suitable for multiplex operation
- Low fan-in and low power
- Blanking via program input
- Also drives overrange, polarity, decimal point cathodes

connection diagram

Dual-In-Line Package



TOP VIEW

Order Number DS7885J or DS8885J

Order Number DS8885N

truth tables

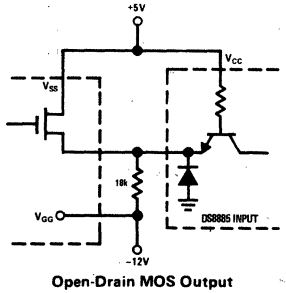
A	B	D	E	F	G	DISPLAY
1	1	1	1	1	0	0
0	1	0	0	0	0	1
1	1	1	1	0	1	2
1	1	1	0	0	1	3
0	1	0	0	1	1	4
1	0	1	0	1	1	5
1	0	1	1	1	1	6
1	1	0	0	0	0	7
1	1	1	1	1	1	8
1	1	1	0	1	1	9
0	0	1	1	1	1	b
1	1	0	0	1	1	c
1	1	0	1	1	1	A
0	1	0	1	1	1	H
0	1	1	1	1	0	U
0	0	0	0	0	1	-
0	0	0	0	0	0	

INPUT*	OUTPUT*
0	1 (OFF)
1	0 (ON)

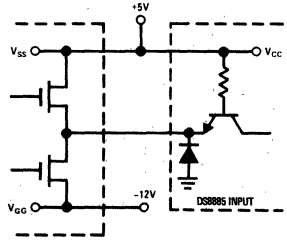
*Positive Logic

C = (Ā·B̄·D̄ + E)·F

typical applications



Open-Drain MOS Output



Push-Pull MOS Output

absolute maximum ratings (Note 1)

V_{CC}	7V
Input Voltage	6V
Segment Output Voltage	80V
Power Dissipation	600 mW
Transient Segment Output Current (Note 4)	50 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS7885	4.5	5.5	V
DS8885	4.75	5.25	V
Temperature (T_A)			
DS7885	−55	+125	°C
DS8885	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Min		2.0			V
V_{IL}	Logical "0" Input Voltage	V_{CC} = Min				0.8	V
I_{IH}	Logical "1" Input Current	V_{CC} = Max	V_{IN} = 2.4V		2	15	μA
			V_{IN} = 5.5V		4	400	μA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V			−300	−600	μA
I_{CC}	Power Supply Current	V_{CC} = Max, All Inputs = 0V, R_P = 2.2k			22	31	mA
V_I	Input Diode Clamp Voltage	V_{CC} = 5V, I_{IN} = −12 mA, T_A = 25°C			−0.9	−1.5	V
SEGMENT OUTPUTS							
ΔI_O	"ON" Current Ratio	All Outputs = 50V, I_{OUT} b = Ref.	Outputs a, f, and g	0.84	0.93	1.02	
			Output c	1.12	1.25	1.38	
			Output d	0.90	1.00	1.10	
			Output e	0.99	1.10	1.21	
$I_{b\ ON}$	Output b "ON" Current	V_{CC} = 5V, V_{OUT} b = 50V, T_A = 25°C	R_P = 18.1k	0.15	0.20	0.25	mA
			R_P = 7.03k	0.45	0.50	0.55	mA
			R_P = 3.40k	0.90	1.00	1.10	mA
			R_P = 2.20k	1.35	1.50	1.65	mA
V_{SAT}	Output Saturation Voltage	V_{CC} = Min, I_{OUT} b = 2 mA, R_P = 1k ±5%, (Note 5)			0.8	2.5	V
I_{CEX}	Output Leakage Current	V_{OUT} = 75V, V_{IN} = 0.8V, R_P = 1k			0.003	3	μA
V_{BR}	Output Breakdown Voltage	I_{OUT} = 250μA, V_{IN} = 0.8V		80	110		V
t_{pd}	Propagation Delay of Input to Segment Output	V_{CC} = 5V, T_A = 25°C			0.4	10	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7885 and across the 0°C to +70°C range for the DS8885. All typical values are for T_A = 25°C and V_{CC} = 5V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: In all applications transient segment output current must be limited to 50 mA. This may be accomplished in dc applications by connecting a 2.2k resistor from the anode-supply filter capacitor to the display anode, or by current limiting the anode drive in multiplex applications.

Note 5: For saturation mode the segment output currents are externally limited and ratioed.

typical performance characteristics (see DS7880 data sheet)

NATIONAL

Display Drivers

DS7887/DS8887 8-digit high voltage anode driver (active-high inputs)

DS7889/DS8889 8-digit high voltage cathode driver (active-high inputs)

DS7897/DS8897 8-digit high voltage anode driver (active-low inputs)

general description

The DS7887/DS8887 and DS7897/DS8897 are designed to drive the individual anodes of a 7-segment (cathodes) high-voltage gas discharge panel in a time multiplexed fashion.

When driven with appropriate input signals, the driver will switch voltage and impedance levels at the anode. This will allow or prevent ionization of gas around selected cathode in order to form a numeric display. This main application is to interface with MOS outputs (fully-decoded) and the anodes of a gas-discharge panel, since the devices can source up to 16 mA at a low impedance and can tolerate more than 55V in the "OFF" state.

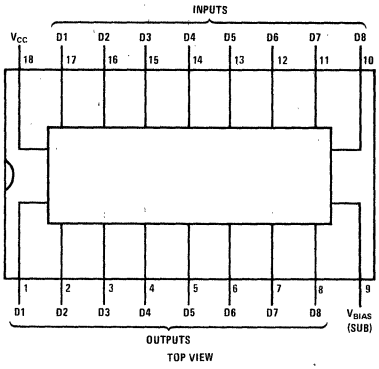
DS7889/DS8889 is capable of driving 8 segments of a high-voltage display tube with a constant output sink current, which can be adjusted by external program resistor, R_P. The program current is half that of output "ON" current. In the "OFF" state the outputs can tolerate more than 80V. The ratio of "ON" output currents is within ±10%. Inputs have negative clamp diodes. Active high input logic. The main application of the device is to interface MOS circuits to high-voltage displays.

features

- Versatile circuits for a wide range of display applications
- High breakdown voltages
- Low power dissipation

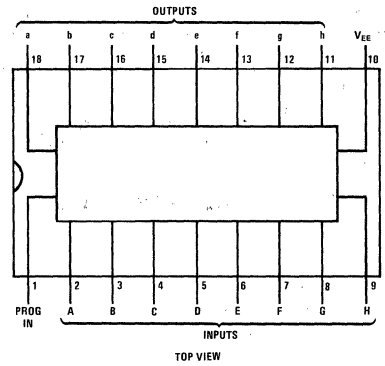
connection diagrams (dual-in-line packages)

DS7887/DS8887, DS7897/DS8897



Order Number DS7887J, DS8887J, DS8887N, DS7897J, DS8897J or DS8897N

DS7889/DS8889



Order Number DS7889J, DS8889J or DS8889N

absolute maximum ratings (Note 1)

Supply Voltage ($V_{CC} - V_{BIAS}$) (Note 2)
DS7887/DS8887, DS7897/DS8897 −60V
Package Power
DS7889/DS8889 600 mW
Input Voltage
DS7887/DS8887, DS7897/DS8897 −20V
DS7889/DS8889 (Note 3) 35V
Output Voltage
DS7887/DS8887, DS7897/DS8897 −65V
DS7889/DS8889 85V
Storage Temperature Range −65°C to +150°C
Lead Temperature (Soldering 10 seconds) 300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage ($V_{CC} - V_{BIAS}$)			
DS7887/DS8887, DS7897/DS8897	−40	−60	V
Temperature (T_A)			
DS7887, DS7889, DS7897	−55	+125	°C
DS8887, DS8889, DS8897	0	+70	°C

dc electrical characteristics (Notes 2, 3 and 4)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
DS8887, DS8897								
V_{IH}	Logical "1" Input Voltage	V_{OUT} = −1.4V, I_{OUT} = −16 mA, DS8887			−2.0			V
V_{IL}	Logical "0" Input Voltage	V_{OUT} = −60V, I_{OUT} = −100μA, DS8887					−5.5	V
I_{IH}	Logical "1" Input Current	V_{OUT} = −1.4, I_{OUT} = −16 mA, DS8897			−300			μA
I_{IL}	Logical "0" Input Current	V_{OUT} = −60V, I_{OUT} = −100μA, DS8897					−10	μA
I_I	Input Current	DS8887	V_{IN} = −1.0V			335	550	μA
			V_{IN} = −6.0V			−0.2	−25	μA
			V_{IN} = −12V		−0.30		−0.65	mA
		DS8897, V_{IN} = 12V			−0.6		−1.5	mA
$V_{OUT\ OFF}$	Output "OFF" Voltage	I_{OUT} = −100μA, I_{IN} = 0μA			−60	−77		V
$I_{OUT\ OFF}$	Output "OFF" Current	V_{OUT} = −55V, I_{IN} = 0μA				−0.03	−5.0	μA
$V_{OUT\ ON}$	Output "ON" Voltage	I_{OUT} = −16 mA	V_{IN} = −2.0V, DS8887			−1.0	−1.4	V
			I_{IN} = −300μA, DS8897				−1.4	V
I_{CC}	Supply Current	I_{OUT} = −16 mA, V_{BIAS} = −60V	V_{IN} = −1.0V, DS8887, (Note 5)			−2.2	−4.0	mA
			I_{IN} = −300μA, DS8897, (One Driver Only)				−100	μA
DS7889/DS8889								
I_I	Input Current	V_{IN} = 6.0V			150	250	350	μA
I_{IL}	Logical "0" Input Current	I_{OUT} = 5.0μA, V_{OUT} = 75V					7.0	μA
I_{IH}	Logical "1" Input Current	I_{OUT} = 1.4 mA, I_{IP} = 850μA, V_{OUT} = 50V			80			μA
V_I	Input Clamp Voltage	I_{IN} = −1.0 mA, T_A = 25°C				−0.68	−0.85	V
V_{OH}	Output Breakdown Voltage	I_{OUT} = 100μA, I_{IN} = 0μA			80			V
I_{CEX}	Output Leakage Current	V_{OUT} = 75V, −0.1 mA ≤ I_{IN} ≤ 7.0μA				0.02	5.0	μA
I_{PROG}	Prog. Input Voltage	I_{IP} = 150μA			1.8	2.3		V
		I_{IP} = 850μA				4.0	4.5	V
I_{OL}	Logical "0" Output Current	V_{OUT} = 50V, 80μA ≤ I_{IN} ≤ I_{IP}	I_{IP} = 150μA	DS7889	210	300	390	μA
				DS8889	240	300	360	μA
			I_{IP} = 400μA	DS7889	660	800	940	μA
				DS8889	680	800	920	μA
			I_{IP} = 850μA	DS7889	1.45	1.7	1.95	mA
				DS8889	1.53	1.7	1.87	mA
ΔI_O	Output Current Ratio	I_{OUT} b Ref = 1.7 mA, V_{OUT} = 50V			0.9	1.0	1.1	

6

ac electrical characteristics $T_A = 25°C$ unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
DS8887						
t_{ON}	Propagation Delay from Input to Output "ON"	(See ac Test Circuit and Switching Time Waveforms)			5.0	μs
t_{RISE}	Propagation Delay from Input to Output "ON"	(See ac Test Circuit and Switching Time Waveforms)			1.0	μs
DS7889/DS8889						
t_{pd0}	Propagation Delay to a Logical "0" from Input to Output	R_P = 6.0k to 6.0V, R_{OUT} = 1.0k to 6.0V		37	100	ns
t_{pd1}	Propagation Delay to a Logical "1" from Input to Output	Input Ramp Rate ≤ 15 ns, Freq = 1.0 MHz dc = 50%, Amplitude = 6.0V		92	200	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

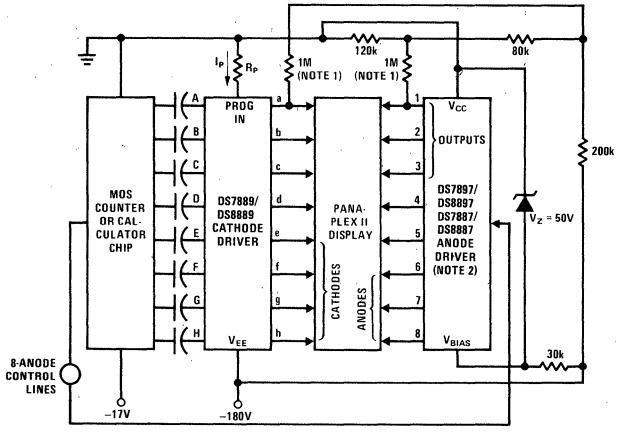
Note 2: All voltages shown for DS7887/DS8887, DS7897/DS8897 W.R.T. V_{CC} = 0V. All currents into device pins shown as positive, out of device pins as negative. All values shown as max or min on absolute basis.

Note 3: All voltages for DS7889/DS8889 with respect to V_{CC} = 0V.

Note 4: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7889 and across the 0°C to +70°C range for the DS8887, DS8889 and DS8897. All typicals are given for T_A = 25°C.

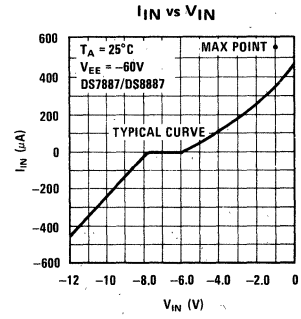
Note 5: Supply currents specified for any one input = −1.0V. All other inputs = −5.5V and selected output having 16 mA load.

typical application

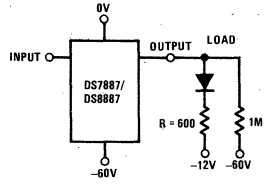


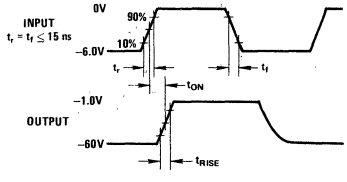
Note 1: All outputs of both cathode and anode driver have loads as shown for output a.
Note 2: Use DS7887/DS8887 for active-high inputs and DS7897/DS8897 for active-low inputs.

typical performance characteristics



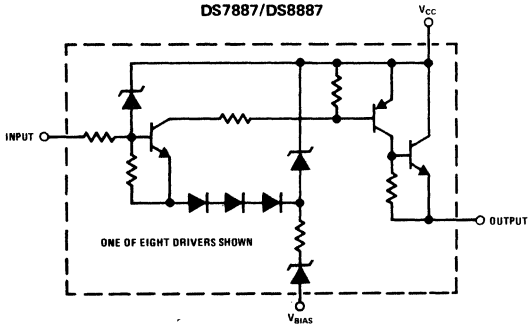
ac test circuit and switching time waveforms



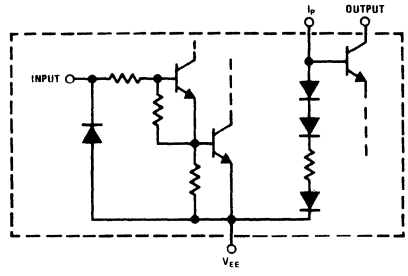


logic diagrams

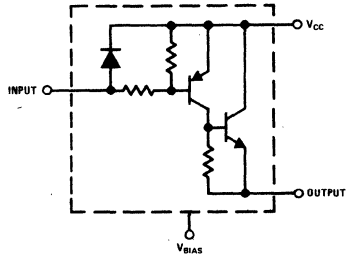
DS7887/DS8887



DS7889/DS8889



DS7897/DS8897



6

NATIONAL

DS7891/DS8891 high voltage anode drivers (active low inputs)

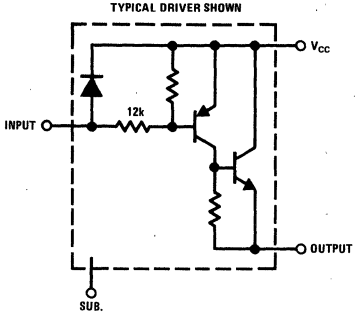
general description

The DS7891/DS8891 is a 6 digit anode driver intended for use with seven segment, common anode, high voltage, gas discharge display panels operating in a multiplexed mode. The driver switches voltage and impedance levels at the display's anode allowing or preventing ionization of gas around selected cathodes, forming a numeric display. The devices acts as a buffer between MOS outputs (fully decoded) and the anodes of a gas-discharge panel, and it can source up to 16 mA at a low impedance and can stand off more than 55V in the off state.

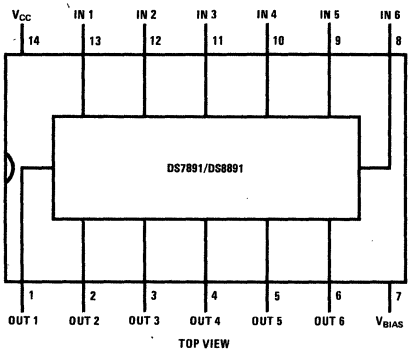
features

- High breakdown voltage
- Low power dissipation
- Easy interface to clock and calculator circuits

schematic and connection diagrams

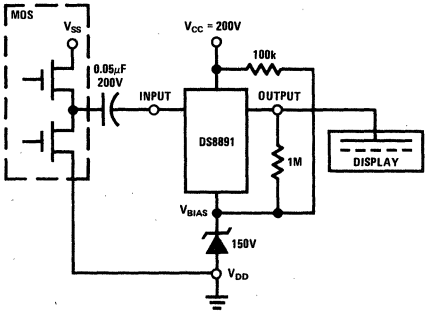


Dual-In-Line Package



Order Number DS7891J, DS8891J or DS8891N

typical application



absolute maximum ratings (Note 1)

Supply Voltage ($V_{CC} - V_{BIAS}$)	−60V
Input Voltage	−20V
Output Voltage	−65V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, $V_{CC} - V_{BIAS}$	−45	−55	V
Temperature, T_A			
DS8891	0	+70	°C
DS7891	−55	+125	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{IN}	Input Current	V_{BIAS} = Min, V_{IN} = −12V	−0.6		−1.5	mA
I_{IH}	Logical "1" Input Current	V_{BIAS} = Min, V_{OL} = −2.0V	−300			μA
I_{IL}	Logical "0" Input Current	V_{BIAS} = Min, V_{OUT} = −60V, I_{OUT} = −100μA			−10	μA
I_{OH}	Logical "1" Output Current	V_{BIAS} = Max, I_{IN} = 0μA, V_{OH} = −55V			−5	μA
V_{OL}	Logical "0" Output Voltage	I_{OL} = −16 mA, I_{IH} = −300μA			−2.0	V
V_{BD}	Output Breakdown Voltage	V_{BIAS} = Max, I_{IN} = 0μA, I_{OUT} = −100μA	−60			V
I_{BIAS}	Supply Current (Substrate)	V_{BIAS} = Max, I_{IH} = −300μA, I_{OL} = −16 mA, (One Driver Only)			−100	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7891 and across the 0°C to +70°C range for the DS8891.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to V_{CC} = 0V, unless otherwise noted. All values shown as max or min on absolute value basis.

NATIONAL

DS8892 programmable hex LED digit driver

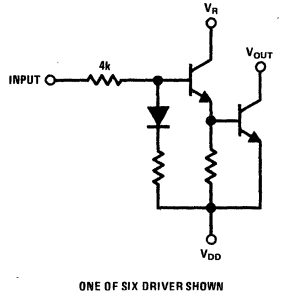
general description

The DS8892 is a hex LED digit driver similar to the DS75494, except that the DS8892 is programmable. The DS8892 will sink up to 200 mA per output, and the open collector outputs withstand a minimum of 8.8V in the off state. The main application of the DS8892 is to interface between MOS circuits and common cathode LED displays in systems where low battery drain is important. The DS8892, through the use of a single external resistor, allows the base drive to the output transistors to be programmed to the desired amount, thus saving battery current.

features

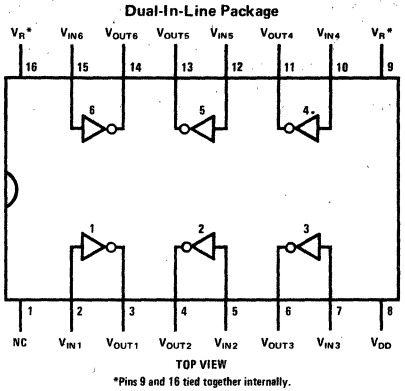
- Presettable current drain
- 200 mA sink capability
- MOS compatible inputs
- Low voltage operation

schematic and connection diagrams



ONE OF SIX DRIVER SHOWN

Dual-In-Line Package

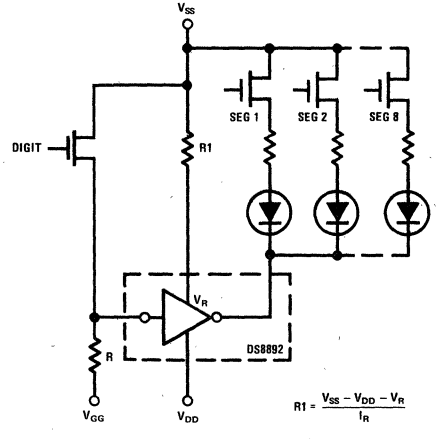


TOP VIEW

*Pins 9 and 16 tied together internally.

Order Number DS8892N

typical application



$$R1 = \frac{V_{SS} - V_{DD} - V_R}{I_R}$$

absolute maximum ratings (Note 1)

Supply Voltage, V_{SS} (Note 2)	8.8V
Input Voltage	8.8V
Output Voltage	8.8V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Notes 2 and 3) V_{DD} = 0V

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{IL}	Logical "0" Input Current	V_{SS} = 8.8V, R1 = 300Ω, I_{OUT} = 400μA		50			μA
I_{IH}	Logical "1" Input Current	V_{SS} = 8.8V, R_{IN} = 45Ω, I_R = 6 mA, I_{OUT} = 80 mA				2.7	mA
V_R	Logical "0" Phase-Splitter Voltage	V_{SS} = 6.0V, R_{IN} = 45Ω, I_R = 6 mA, I_{OUT} = 80 mA		0.9		1.4	V
I_{OH}	Logical "1" Output Current	V_{SS} = 8.8V, I_{IN} = 50μA, R1 = 300Ω, V_{OUT} = 8.5V				400	μA
V_{OL}	Logical "0" Output Voltage	R_{IN} = 140Ω	V_{SS} = 3.0V, I_R = 2 mA, I_{OUT} = 25 mA			0.35	V
			V_{SS} = 3.8V, I_R = 5.7 mA, I_{OUT} = 50 mA			0.35	V
			V_{SS} = 4.5V, I_R = 7.7 mA, I_{OUT} = 100 mA			0.40	V
			V_{SS} = 6.0V, I_R = 12 mA, I_{OUT} = 200 mA			0.50	V

switching characteristics

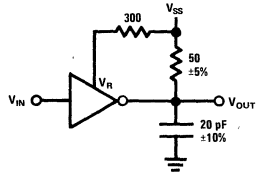
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{P(ON)}$	Propagation Delay to a Logical "0"	(See AC Test Circuit), V_{SS} = 6.0V			800	ns
$t_{P(OFF)}$	Propagation Delay to a Logical "1"	(See AC Test Circuit), V_{SS} = 6.0V			1.2	μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

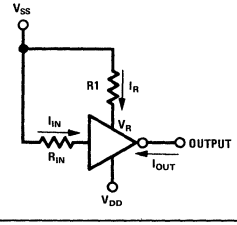
Note 2: V_{SS} is an external system supply, used as shown in the dc test circuit (V_{DD} = 0V).

Note 3: All currents into device pins shown as positive, out of device pins as negative. All voltages referenced to ground unless otherwise noted. All values shown as maximum or minimum on absolute value basis.

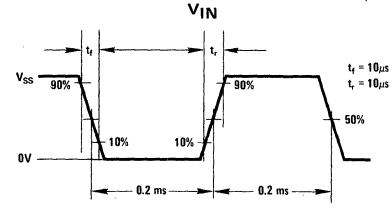
ac test circuit

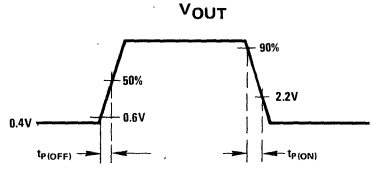


dc test circuit



switching time waveforms





DS7895/DS8895 quad LED segment driver

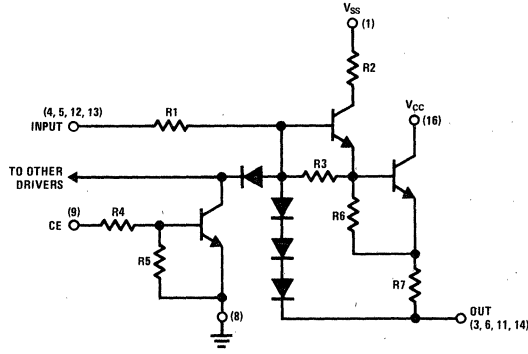
general description

The DS7895/DS8895 is a quad LED segment driver designed to interface between MOS IC's and LED displays. It provides a relatively constant output current —typically 17 mA—independent of the supply voltage. The DS8895 is similar to the DS75493 except on the DS8895 the output current is internally set—no external components are required for current limiting. Blanking can be achieved by taking the Chip Enable (CE) to a logic "1" level.

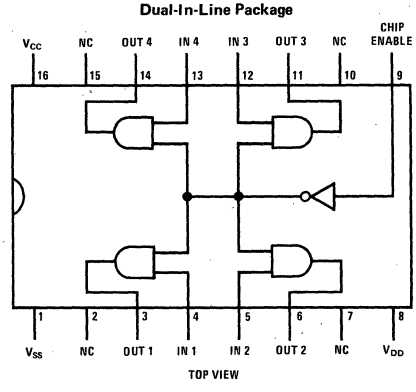
features

- Internally set output current
- Low voltage operation
- MOS compatible inputs
- Low standby power
- Blanking capability

schematic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS7895J, DS8895J, or DS8895N

absolute maximum ratings (Note 1)

Supply Voltage	10V
Input Voltage	10V
Output Voltage	V_{CC}
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
V_{CC}	3.2	8.8	V
V_{SS}	6.5	8.8	V
Temperature, T_A			
DS8895	0	+70	°C
DS7895	−55	+125	°C

electrical characteristics (Notes 2 and 3)

	PARAMETER	CONDITIONS (See *Figure 1*)		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = 3.2V, V_{SS} = 8.8V, I_{IN} = 2.0 mA, V_{OUT} = 1.75V		6.5			V
V_{IHCE}	Chip Enable	V_{CC} = 3.2V, V_{SS} = 8.8V, I_{IN} = 1.0 mA, V_{OUT} = 0V		3.5			V
I_{IH}	Logical "1" Input Current	V_{CC} = 3.2V, V_{SS} = 8.8V, V_{IN} = 8.8V, R = 0.1k, V_{OUT} = 1.75V				2.0	mA
V_{IL}	Logical "0" Input Voltage	V_{CC} = 8.8V, V_{SS} = 8.8V, V_{OUT} = 0V, I_{IN} = 0.1 mA				1.3	V
V_{ILCE}	Chip Enable	V_{CC} = 8.8V, V_{SS} = 8.8V, V_{OUT} = 1.75V, R = 0.1k				1.0	V
$I_{OUT\ MIN}$	Output Current	V_{CC} = 3.2V, V_{SS} = 6.5V, V_{OUT} = 2.15V, R = 1k, T_A = 25°C		12.5	16.5		mA
$I_{OUT\ MAX}$	Output Current	V_{CC} = 8.8V, V_{SS} = 8.8V, V_{OUT} = 1.75V, R = 0.1k, T_A = 25°C			18.5	22	mA
$I_{OUT\ TYP}$	Output Current	V_{CC} = 3.6V, V_{SS} = 7.2V, V_{OUT} = 2.0V, T_A = 25°C, R = 500Ω	DS7895	15.5	17	18.5	mA
			DS8895	14.5	17	19.5	mA
I_{OUT}	Output Current	V_{CC} = 3.6V, V_{SS} = 7.2V, V_{OUT} = 2.0V, R_L = 500Ω, Full Temperature Range	DS7895	10.5		23.0	mA
			DS8895	13.5		20.5	mA
$I_{OUT\ OFF}$	Output Current	V_{CC} = 8.8V, V_{OUT} = 0V, (All Drivers "OFF")	V_{SS} = 8.8V, R = 100k			100	μA
			V_{SS} = 6.5V, R = 0.1k, R_{CE} = 1k			200	μA
I_{SS}	Supply Current	V_{IN} = 6.5V	V_{CC} = 1.0V, V_{SS} = 8.8V (Outputs Open)			8	mA
I_{CC}	Supply Current	V_{IN} = 6.5V	V_{CC} = 3.2V V_{SS} = 8.8V, V_{OUT} = 1.75V DS7895			5	mA
			V_{CC} = 3.2V V_{SS} = 8.8V, V_{OUT} = 1.75V DS8895			4	mA
$t_{pd\ OFF}$	Propagation Delay to a Logical "0" from Input to Output	$t_r = t_f$ = 10 ns, (See *Figures 2 and 3*)			170	300	ns
$t_{pd\ ON}$	Propagation Delay to a Logical "1" from Input to Output	$t_r = t_f$ = 10 ns, (See *Figures 2 and 3*)			11	100	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS7895 and across the 0°C to +70°C range for the DS8895. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as maximum or minimum on absolute value basis.

truth table

CE	V_{IN}	I_{OUT}
0	1	ON
0	0	OFF
1	X	OFF

X = Don't care

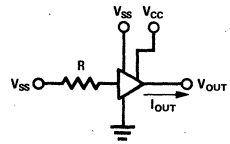


FIGURE 1.

ac test circuit and switching time waveforms

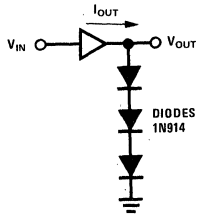


FIGURE 2.

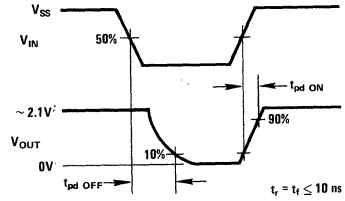


FIGURE 3.

NATIONAL

DS8973, DS8974, DS8976 LED 9-digit drivers

general description

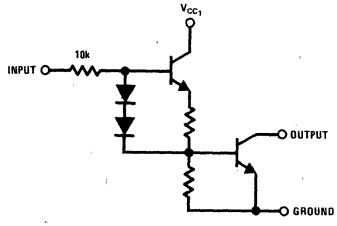
The DS8973, DS8974, and DS8976 are 9-digit drivers designed to operate from 4 cell (DS8973) or 3 cell (DS8974) or 6 cell (DS8976) battery supplies. Each driver will sink 100 mA to less than 0.5V when driven by only 0.1 mA. Each input is blocked by diodes so that the input can be driven below ground with virtually no current drain. This is especially important in calculator systems employing a dc-to-dc converter on the negative side of the battery. If the converter were on the positive side of the battery, the converter would have to handle all of the display current, as well as the MOS calculator chip current. But if it is on the negative side, it only has to handle the MOS current. The DS8973 and DS8974 are designed for the more efficient operating mode.

features

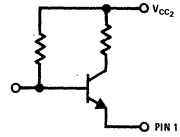
- Nine complete digit drivers
- Built-in low battery indicator
- High current outputs—100 mA
- Choice of 3 or 4-cell operation
- Straight through pin out for easy board layout

equivalent circuit and connection diagrams

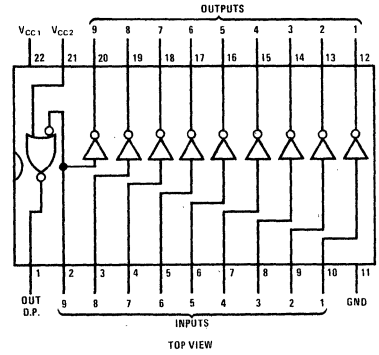
Typical Driver Circuit



Typical D.P. Out Circuit



Dual-In-Line Package



Order Number DS8973N, DS8974N or DS8976N

typical applications

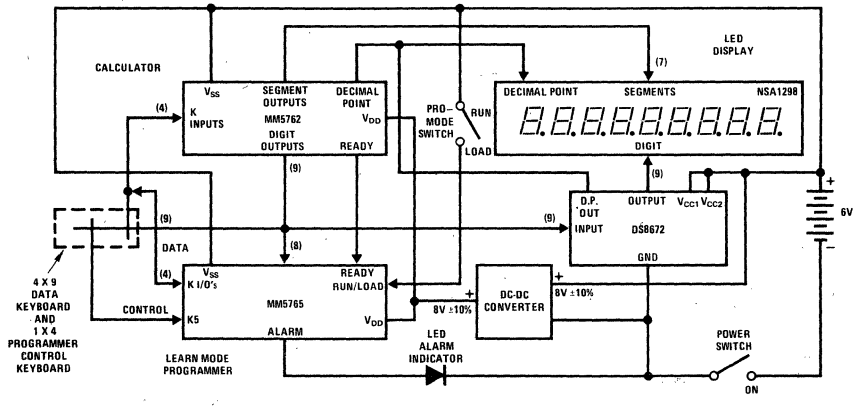


FIGURE 1. 6V Programmable Statistical Calculator

absolute maximum ratings (Note 1)

Supply Voltage	10V
Input Voltage	10V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS8973	4.4	10.0	V
DS8974, DS8976	3.3	4.5	V
Temperature (T_A)	0	70	°C

electrical characteristics

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage	V_{CC} = Max		3.9			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IH} = 3.9V		0.1		0.3	mA
V_{IL}	Logical "0" Input Voltage	V_{CC} = Max				0.5	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IL} = 0.5V				40	μA
V_{TH}	High Low Battery Threshold	V_{OT} (Pin 1) = 1V, $I_{OT} \leq -50\mu A$, $T_A = 25°C$	DS8973	3.5			V
		V_{IH} (Pin 2) = 3.9V	DS8974	4.6			V
			DS8976	7.0			V
V_{TL}	Low Low Battery Threshold	V_{OT} (Pin 1) = 2.3V, $I_{OT} \geq -6$ mA, $T_A = 25°C$	DS8973			3.1	V
		V_{IH} (Pin 2) = 3.9V	DS8974			4.2	V
			DS8976			6.2	V
I_{CEX}	Logical "1" Output Current	V_{CC} = Min, V_{OH} = 9.5V, V_{IL} = 0.5V				50	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OL} = 100 mA, V_{IH} = 3.9V				0.5	V
I_{OL}	Logical "0" Output Current	V_{CC} = Min, V_{OL} = 0.5V, V_{IH} = 3.9V		100			mA
I_{CC_1}	Supply Current	V_{CC} = Max, One Input "ON"				6	mA
I_{CC_2}	Pin 21 (Low Battery Supply)	V_{CC} = Max, $V_{CC_2} = V_{CCMAX}$				1.2	mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operations.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range. All typicals are given for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

typical applications (con't)

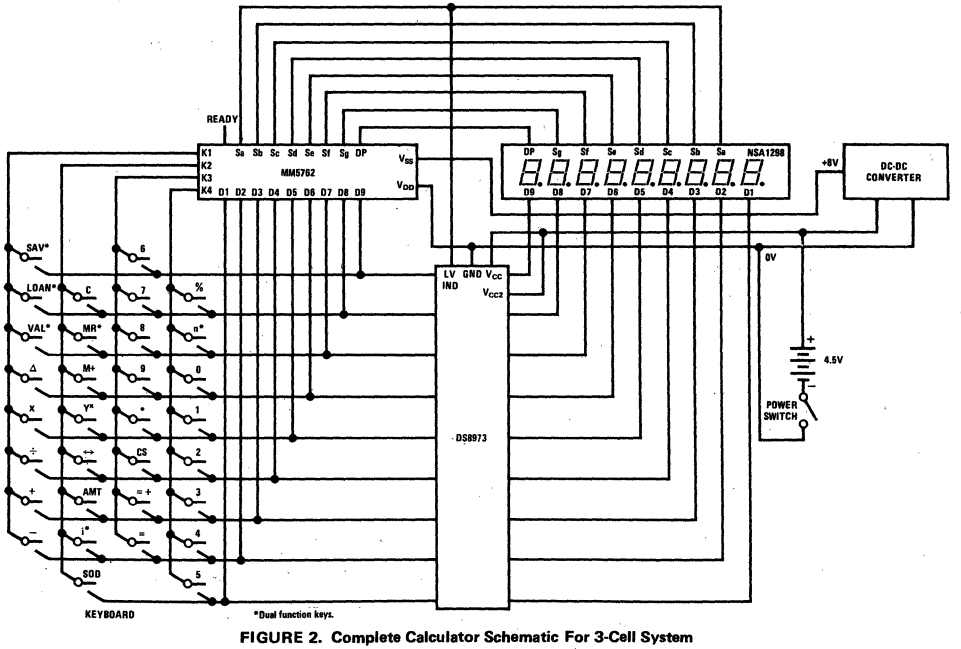


FIGURE 2. Complete Calculator Schematic For 3-Cell System

NATIONAL

Display Drivers

DS75491 MOS-to-LED quad segment driver
DS75492 MOS-to-LED hex digit driver

general description

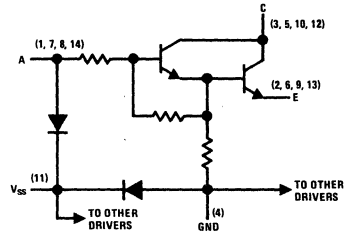
The DS75491 and DS75492 are interface circuits designed to be used in conjunction with MOS integrated circuits and common-cathode LED's in serially addressed multi-digit displays. The number of drivers required for this time-multiplexed system is minimized as a result of the segment-address-and-digit-scan method of LED drive.

features

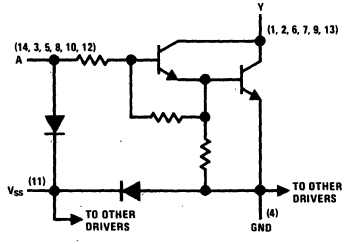
- 50 mA source or sink capability per driver (DS75491)
- 250 mA sink capability per driver (DS75492)
- MOS compatability (low input current)
- Low standby power
- High-gain Darlington circuits

schematic and connection diagrams

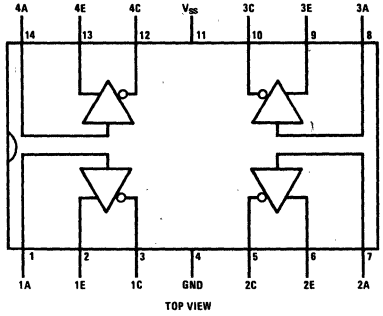
DS75491 (each driver)



DS75492 (each driver)

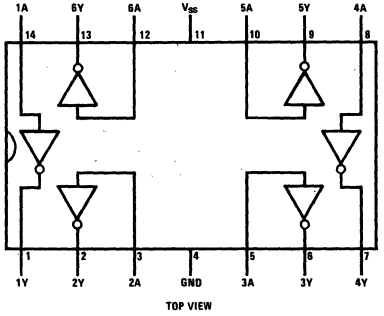


DS75491 Dual-In-Line Package



TOP VIEW

DS75492 Dual-In-Line Package



TOP VIEW

Order Number DS75491J or DS75492J

Order Number DS75491N or DS75492N

6

absolute maximum ratings (Note 1)

	DS75491	DS75492
Input Voltage Range (Note 4)	−5V to V_{SS}	−5V to V_{SS}
Collector Output Voltage (Note 5)	10V	10V
Collector Output to Input Voltage	10V	10V
Emitter to Ground Voltage ($V_I \geq 5V$)	10V	
Emitter to Input Voltage	5V	
Voltage at V_{SS} Terminal With Respect to Any Other Device Terminal	10V	10V
Collector Output Current		
Each Collector Output	50 mA	250 mA
All Collector Outputs	200 mA	600 mA
Continuous Total Dissipation	600 mW	600 mW
Operating Temperature Range	0°C to +70°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C	300°C

dc electrical characteristics

DS75491 (V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted) (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{CE\ ON}$	"ON" State Collector Emitter Voltage	Input = 8.5V through 1 kΩ, T_A = 25°C			0.9	1.2	V
		V_E = 5V, I_C = 50 mA				1.5	V
$I_{C\ OFF}$	"OFF" State Collector Current	V_C = 10V,	I_{IN} = 40μA			100	μA
		V_E = 0V	V_{IN} = 0.7V			100	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, V_E = 0, I_C = 20 mA			2.2	3.3	mA
I_E	Emitter Reverse Current	V_{IN} = 0, V_E = 5V, I_C = 0				100	μA
I_{SS}	Current Into V_{SS} Terminal					1	mA

DS75492 (V_{SS} = 10V, T_A = 0°C to +70°C unless otherwise noted) (Notes 2 and 3)

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Low Level Output Voltage	Input = 6.5V through 1 kΩ, T_A = 25°C			0.9	1.2	V
		I_{OUT} = 250 mA				1.5	V
I_{OH}	High Level Output Current	V_{OH} = 10V	I_{IN} = 40μA			200	μA
			V_{IN} = 0.5V			200	μA
I_I	Input Current at Maximum Input Voltage	V_{IN} = 10V, I_{OL} = 20 mA			2.2	3.3	mA
I_{SS}	Current Into V_{SS} Terminal					1	mA

ac switching characteristics

DS75491 (V_{SS} = 7.5V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output (Collector)	V_{IH} = 4.5V, V_E = 0,		100		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output (Collector)	R_L = 200Ω, C_L = 15 pF		20		ns

DS75492 (V_{SS} = 7.5V, T_A = 25°C)

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	V_{IH} = 7.5V, R_L = 39Ω,		300		ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	C_L = 15 pF		30		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

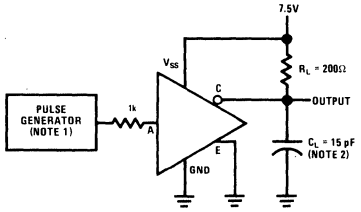
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C temperature range for the DS75491 and DS75492.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

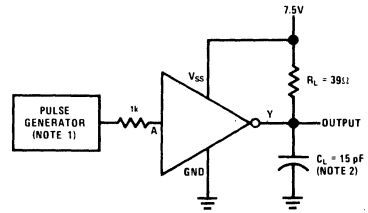
Note 4: The input is the only device terminal which may be negative with respect to ground.

Note 5: Voltage values are with respect to network ground terminal unless otherwise noted.

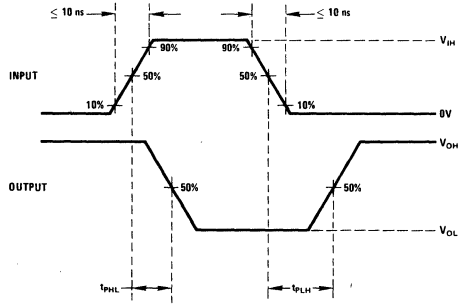
ac test circuits and switching time waveforms



DS75491



DS75492



Note 1: The pulse generator has the following characteristics: Z_{OUT} = 50Ω, PRR = 100 kHz, t_W = 1 μs.

Note 2: C_L includes probe and jig capacitance.

NATIONAL

Display Drivers

DS75493 quad LED segment driver

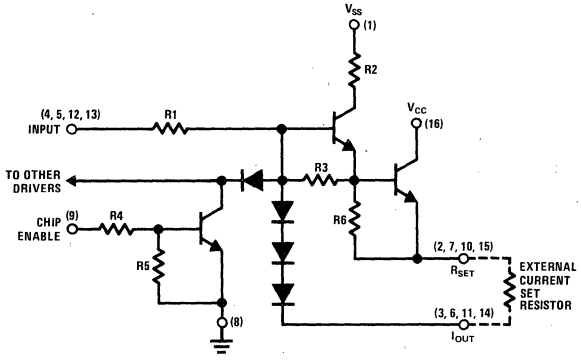
general description

The DS75493 is a quad LED segment driver. It is designed to interface between MOS IC's and LED's. An external resistor is required for each segment to drive the output current which is approximately equal to $0.7V/R_L$ and is relatively constant, independent of supply variations. Blanking can be achieved by taking the chip enable (CE) to a logical "1" level.

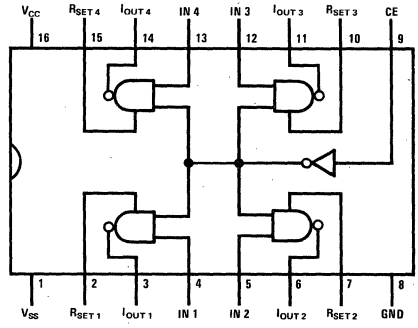
features

- Low voltage operation
- Low input current for MOS compatibility
- Low standby power
- Display blanking capability
- Output current regulation
- Quad high gain circuits

schematic and connection diagrams

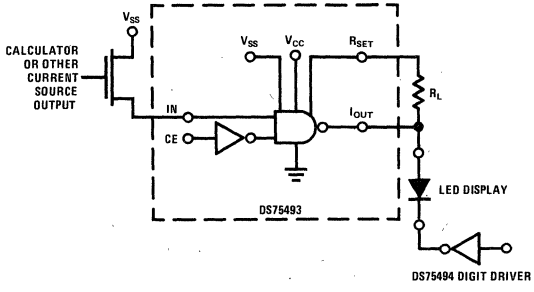


Dual-In-Line Package



Order Number DS75493J
or DS75493N

typical application



truth table

CE	V_{IN}	I_{OUT}
0	1	ON
0	0	OFF
1	X	OFF

X = Don't care

absolute maximum ratings (Note 1)

Supply Voltage	10V
Input Voltage	10V
Output Voltage	V_{CC}
Storage Temperature Range	+65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Output Current (I_{OUT})	−25 mA

operating conditions

	MIN	MAX	UNITS
Supply Voltage			
V_{CC}	3.2	8.8	V
V_{SS}	6.5	8.8	V
Temperature, T_A	0	+70	°C

electrical characteristics ($V_{SS} \geq V_{CC}$) $T_A = 25°C$ (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
I_{IN}	Input Current	V_{SS} = Max, V_{IN} = 8.8V, V_{CC} = Open, V_{CE} = 0V				3.2	mA
		$I_{OUT} = R_{SET}$ @ 0V, V_{CE} = 8.8V				3.6	mA
I_{CE}	Chip Enable Input Current	V_{CC} = Max, V_{SS} = Max, V_{CE} = 8.8V, All Other Pins to Gnd				2.1	mA
I_{OUT}	Output Current	I_{OUT} @ 2.15V, $R_L = 50\Omega$	V_{CC} = Min, V_{SS} = 6.5V, $I_{CE} = 80\mu A$, V_{IN} = 6.5V Through 1.0 kΩ	−8	−13		mA
			V_{CE} = 0V, V_{IN} = 8.8V		−16	−20	mA
I_{OL}	Output Leakage Current	$I_{OUT} = R_{SET}$ @ 0V, Measure Current to Gnd, V_{SS} = 8.8B	V_{CC} = Min, V_{CE} = 0V V_{IN} = 8.8V Through 100 kΩ			−100	μA
			V_{CE} = 6.5V Through 1.0 kΩ, V_{IN} = 8.8V			−200	μA
I_{CC}	Supply Current, V_{CC}	V_{CC} = Max, V_{SS} = Max, All Other Pins to Gnd				40	μA
I_{SS}	Supply Current	V_{CC} = 0V, All Other Pins to Gnd				40	μA
		V_{CC} = Min, V_{CC} = 8.8V	I_{OUT} @ 2.15V, V_{CE} = 8.8V Through 100 kΩ, $R_L = 50\Omega$		0.5	1.5	mA
			I_{OUT} = Open, R_{SET} = Open, V_{CE} = 0V			1.4	mA

switching characteristics

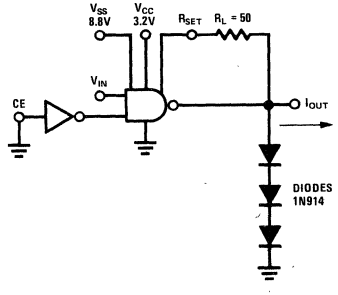
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$t_{pd(OFF)}$	Propagation Delay to a Logical "0" From Input to Output	(See AC Test Circuit)		170	300	ns
$t_{pd(ON)}$	Propagation Delay to a Logical "1" From Input to Output	(See AC Test Circuit)		11	100	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

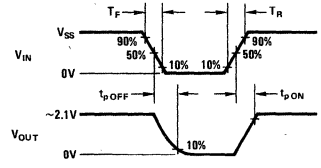
Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75493.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

ac test circuit



switching time waveforms



NATIONAL

Display Drivers

DS75494 hex digit driver

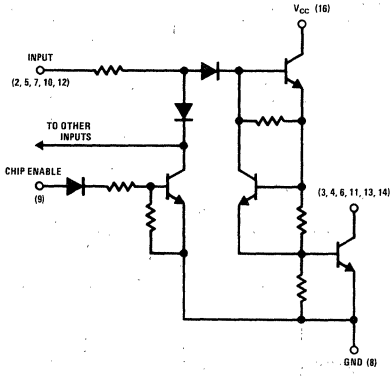
general description

The DS75494 is a hex digit driver designed to interface between most MOS devices and common cathodes configured LED's with a low output voltage at high operating currents. The enable input disables all the outputs when taken high.

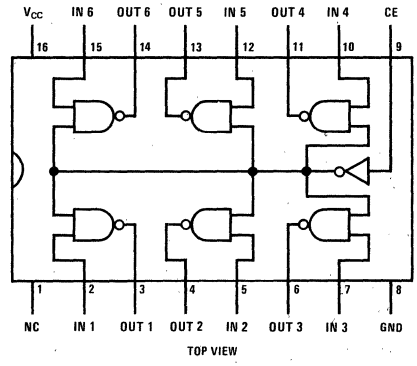
features

- 150 mA sink capability
- Low voltage operation
- Low input current for MOS compatibility
- Low standby power
- Display blanking capability
- Low voltage saturating outputs
- Hex high gain circuits

schematic and connection diagrams



Dual-In-Line Package



TOP VIEW

Order Number DS75494J
Order Number DS75494N

truth table

ENABLE	V_{IN}	V_{OUT}
0	0	1
0	1	0
1	X	1

X = don't care

absolute maximum ratings (Note 1)

Supply Voltage	10V
Input Voltage	10V
Output Voltage	10V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	3.2	8.8	V
Temperature, T_A	0	+70	°C

electrical characteristics (Notes 2 and 3)

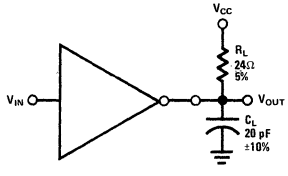
PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
I_{IH}	Logical "1" Input Current	V_{CC} = Min, V_{IN} = 8.8V	V_{CE} = 8.8V through 100k				2.0	mA
			V_{CE} = 8.8V				2.7	mA
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = −5.5V					−20	μA
I_{OH}	Logical "1" Output Current	V_{CC} = Max, V_{OH} = 8.8V	V_{IN} = 8.8V through 100k, V_{CE} = 0V				400	μA
			V_{IN} = 8.8V, V_{CE} = 6.5V through 1.0k				400	μA
V_{OL}	Logical "0" Output Voltage	V_{CC} = Min, I_{OL} = 150 mA, V_{IN} = 6.5V through 1.0k, V_{CE} = 8.8V through 100k				0.25	0.35	V
I_{CC}	Supply Current	V_{CC} = Max	One Driver "ON", V_{IN} = 8.8V				8.0	mA
			All Other Pins to GND	V_{CE} = 6.5V through 1.0k			100	μA
				V_{IN} = 8.8V through 100k			100	μA
			All Pins to GND				40	μA
t_{OFF}	Output "OFF" Time	C_L = 20 pF, R_L = 24Ω, V_{CC} = 4.0V, See ac Test Circuits				0.04	1.2	μs
t_{ON}	Output "ON" Time	C_L = 20 pF, R_L = 24Ω, V_{CC} = 4.0V, See ac Test Circuits				13	100	ns

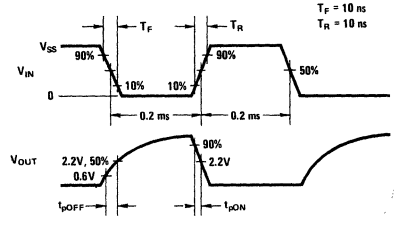
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the 0°C to +70°C range for the DS75494.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

ac test circuit and switching time waveforms





NATIONAL

Opto-Couplers
Advance Information*

DS3660/DS3661 optically isolated line receivers

general description

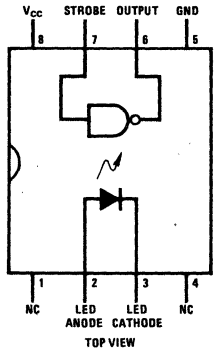
The DS3660 and DS3661 are TTL-compatible optically coupled isolators, with open-collector and TRI-STATE® outputs, respectively. They combine, in one 8-lead DIP, a GaAsP light-emitting diode and a monolithic silicon detector-amplifier. There is complete absence of any electrical connection between input and output terminals, allowing the input signal ground reference to float at any ac or dc potential relative to the output ground reference (within the common-mode range of the device). Thus, they are ideal line receivers, removing input common mode limitations, and eliminating all ground noise and current loops. A proprietary design provides excellent high-frequency common mode rejection, much greater than previously available in optical isolators. These line receivers are therefore especially suited for data interface requirements in transient and pulse noise environments.

features

- 200 V_{AC} peak-to-peak common mode rejection at 1 MHz
- 1500V typical dc isolation (input/output)
- 70 ns typical propagation delays
- TTL strobe input (forces output to logic "1" state)
- TRI-STATE logic output for bus-organized systems (DS3661)
- Open collector output for wire-ORing (DS3660)
- Fanout of 10 standard TTL loads
- Single +5V supply (±10% tolerance)

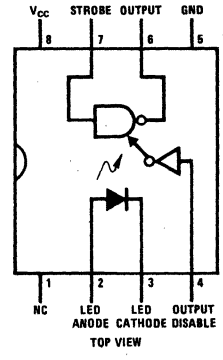
connection diagrams

Dual-In-Line Package



Order Number DS3660N

Dual-In-Line Package



Order Number DS3661N

truth tables (Positive logic convention; input "1" when LED is biased on, $I_F > 5$ mA.)

DS3660

INPUT	STROBE	OUTPUT
0	1	1
1	1	0
X	0	1

X = Don't Care

DS3661

INPUT	STROBE	DISABLE	OUTPUT
0	1	0	1
1	1	0	0
X	0	0	1
X	X	1	Hi-Z

X = Don't Care

*Specifications may change

7

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage (gate)	5.5V
Input Diode Forward Current	20 mA
Input Diode Reverse Voltage	5V
Output Voltage	
DS3660	7V
DS3661	5.5V
Storage Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}	4.5	5.5	V
Temperature, T_A	0	+70	°C

electrical characteristics (0°C – 70°C) (Note 2)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
$I_{IN(1)}$	Logical "1" Input Current	$V_{OUT} < 0.4V$, I_{OUT} (Sink) = 16 mA		5			mA
$I_{IN(0)}$	Logical "0" Input Current	$V_{OUT} > 2.4V$, I_{OUT} (Source) = −400μA				250	μA
$V_{IN(1)}$	Logical "1" Input Voltage (Strobe, Disable)	(See Truth Table for Output State)		2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage (Strobe, Disable)	(See Truth Table for Output State)				0.8	V
I_{IH}	Logical "1" Input Current (Strobe, Disable)	V_{IN} = +2.4V				40	μA
I_{IL}	Logical "0" Input Current (Strobe, Disable)	V_{IN} = 0.4V				−1.6	mA
V_{CL}	Input Clamp Voltage (Strobe, Disable)	I_{IN} = −12 mA, T_A = 25°C				−1.2	V
V_{OH}	Logical "1" Output Voltage	I_{OUT} (Source) = −400μA		2.4			V
V_{OL}	Logical "0" Output Voltage	I_{OUT} (Sink) = 16 mA				0.4	V
I_{OD}	Output Disable Current	V_O = 2.4V	DS3661			40	μA
		V_O = 0.4V	DS3661			−40	μA
I_{CC}	Supply Current	I_{IN} = 5 mA, V_{STROBE} = 2V	DS3660		10	15	mA
		I_{IN} = 5 mA, $V_{DISABLE}$ = 2V	DS3661		12	18	mA
V_F	Input Diode Forward Voltage	T_A = 25°C, I_{IN} = 10 mA			1.75		V
V_{BR}	Input Diode Reverse Breakdown	T_A = 25°C, I_{IN} = −100μA		5			V
V_{ISO}	DC Isolation (Input-Output)	T_A = 25°C			1500		V
CM_{RV}	AC Common Mode Rejection (Input-Output)	f = 1 MHz, Output Meets Worst-Case V_{OL} and V_{OH} Levels (above)			200		V_{AC}, p-p

switching characteristics (Note 3)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}	Propagation Delay to Logical "0" from LED Input	I_{IN} = 7.5 mA, Strobe High, Disable Low, (Note 4)		70		ns
t_{pd1}	Propagation Delay to Logical "1" from LED Input	I_{IN} = 7.5 mA, Strobe High, Disable Low, (Note 4)		70		ns
t_{S0}	Propagation Delay to Logical "0" from Strobe Input	I_{IN} = 7.5 mA, Disable Low		15		ns
t_{S1}	Propagation Delay to Logical "1" from Strobe Input	I_{IN} = 7.5 mA, Disable Low		15		ns
t_{1H}	Delay from Disable Input to High Impedance State, from Logical "1" Level	I_{IN} = 0 mA, Strobe High		6		ns
t_{0H}	Delay from Disable Input to High Impedance State, from Logical "0" Level	I_{IN} = 7.5 mA, Strobe High		12		ns
t_{H1}	Delay from Disable Input to Logical "1" Level, from High Impedance State	I_{IN} = 0 mA, Strobe High		14		ns
t_{H0}	Delay from Disable Input to Logical "0" Level, from High Impedance State	I_{IN} = 7.5 mA, Strobe High		10		ns

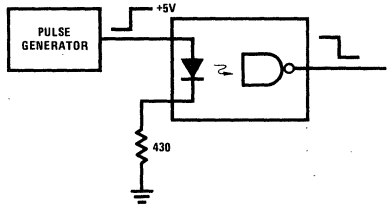
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These apply over V_{CC} range 4.5V to 5.5V unless otherwise noted. Typicals given for T_A = 25°C, V_{CC} = 5.0V. Max refers to absolute value in all cases.

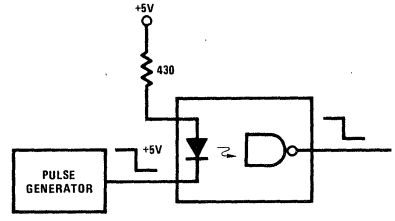
Note 3: All switching response characteristics given for output pull-up resistor R_L = 390Ω, shunt capacitance C_L = 15 pF.

Note 4: These propagation delays are independent of LED drive configuration, e.g., the same performance will be obtained with either test circuit shown below:

ac test circuits



Positive Input Pulse



Negative Input Pulse

NATIONAL

NCT200, NCT260 phototransistor opto-coupler

general description

The NCT200 and NCT260 are Gallium Arsenide diodes coupled with an NPN Silicon phototransistor in a six lead Epoxy dual-in-line package. These devices feature isolation voltage in excess of 2 kV. A GaAs light emitting diode radiates infrared light into a photosensitive transistor providing electrical isolation equivalent to a relay.

These devices are ideally suited where coupling is needed between two circuits but electrical isolation must be maintained. These devices find a wide range of application in data transmission as well as linear coupling.

applications

- Phase control
- Feedback control
- Telephone line receiver
- Line to digital logic isolation
- Solid state relays

features

- 2000V isolation
- High direct-current transfer ratio
- 0.5 pF coupling cap.
- Standard dual-in-line package

absolute maximum ratings

Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +100°C
Total Power Dissipation at 25°C	250 mW
Derate Linearly	3.3 mW/°C
Lead Temperature (Soldering, 10 seconds)	260°C

output transistor (T_A = 25°C, I_F = 0)

Power Dissipation	200 mW
Derate Linearly from 25°C	2.6 mW/°C
V_{CEO}	30V
V_{CER} (1 MΩ)	70V
V_{ECO}	7V

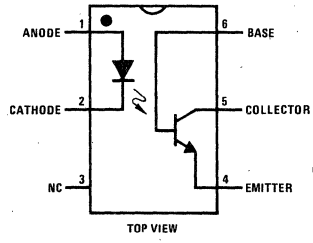
input diode (T_A = 25°C)

Power Dissipation	200 mW
Derate Linearly from 25°C	2.6 mW/°C
Forward DC Current Continuous	60 mA
Forward DC Current Intermittent Duty*	150 mA
Reverse Voltage	3V
Peak Forward Current (1 pulse; 300 pps)	3A

*Dictated by maximum power dissipation.

connection diagram

Dual-In-Line Package



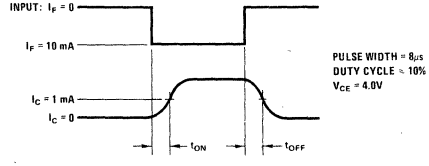
Order Number
NCT200 or NCT260

electro-optical characteristics (T_A = 25°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
INPUT DIODE							
V_F	Forward Voltage	I_F = 60 mA			1.2	1.5	V
I_R	Reverse Leakage Current	V_R = 3.0V				10	μA
C	Capacitance	V = 0, f = 1 MHz			150		pF
OUTPUT TRANSISTOR, I_F = 0							
H_{FE}	dc Forward Current Gain	V_{CE} = 10V, I_C = 1 mA, NCT200			500		
I_{CER}	Collector-Emitter Current	V_{CE} = 10V, R = 1MΩ	NCT200			50	nA
			NCT260			100	nA
LV_{CEO}	Collector-Emitter Sustaining Voltage	I_C = 1.0 mA		30	60		V
BV_{CER}	Collector-Emitter Breakdown Voltage	I_C = 100μA, R = 1 MΩ		70	110		V
BV_{CBO}	Collector-Base Breakdown Voltage	I_C = 10μA		70	110		V
BV_{ECO}	Emitter-Collector Breakdown Voltage	I_C = 100μA		7	8.2		V
COUPLED CHARACTERISTICS							
I_C/I_F	dc Current Transfer Ratio	I_F = 10 mA, V_{CE} = 10V,	NCT200	20	60		%
		R_{BE} = 1 MΩ	NCT260	6			%
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	I_F = 15.0 mA, I_C = 1.6 mA, NCT200			0.2	0.4	V
		I_F = 50 mA	I_C = 6.4 mA Pulsed NCT200			0.4	V
			I_C = 1.6 mA, NCT260			0.5	V
V_{ISO}	Isolation Voltage			2000			V
R_{ISO}	Isolation Resistance	V_{ISO} = 500V			10^{11}		Ω
C_{ISO}	Isolation Capacitance	t = 1 MHz			0.5		pF
BW	Bandwidth (Note)	I_F = 10 mA, V_{CC} = 5.0V, R_L = 100Ω			150		kHz
t_{ON}	Output "ON" Time	I_F = 10 mA, V_{CE} = 4.0V, R_L = 22Ω			2.0		μs
t_{OFF}	Output "OFF" Time	I_F = 10 mA, V_{CE} = 4.0V, R_L = 22Ω			3.0		μs

Note: Bandwidth is specified as the point where the collector current transfer ratio is 1/2 that of the low frequency current transfer ratio (100 Hz).

switching time waveforms



NATIONAL

4N25, 4N26, 4N27, 4N28 phototransistor opto-coupler

general description

Gallium Arsenide LED optically coupled to a Silicon Photo Transistor designed for applications requiring electrical isolation, high-current transfer ratios, small package size and low cost; such as interfacing and coupling systems, phase and feedback controls, solid-state relays and general-purpose switching circuits.

applications

- Phase control
- Feedback control
- Telephone line receiver
- Line to digital logic isolation
- Solid state relays

features

- High isolation voltage
  V_{ISO} = 2500V (min) – 4N25
  1500V (min) – 4N26, 4N27
  500V (min) – 4N28
- High Collector Output Current
  at I_F = 10 mA
  I_C = 10 mA (typ) 4N25, 4N26
- 0.5 pF coupling cap.
- Standard dual-in-line package

absolute maximum ratings*

(T_A = 25°C, unless otherwise specified)

Storage Temperature	−55°C to +150°C
Operating Temperature	−55°C to +100°C
Total Power Dissipation at 25°C	250 mW
Derate Linearly	3.3 mW/°C
Lead Temperature (Soldering, 10 seconds)	260°C

phototransistor* (T_A = 25°C)

Power Dissipation	150 mW
Derate Linearly from 25°C	2 mW/°C
V_{CEO}	30V
V_{ECO}	7V
V_{CBO}	70V

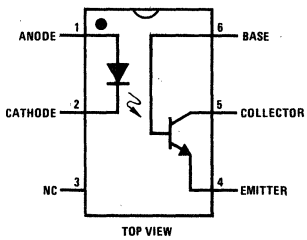
infrared emitting diode* (T_A = 25°C)

Power Dissipation	150 mW
Derate Linearly from 25°C	2 mW/°C
Forward DC Current Continuous	80 mA
Reverse Voltage	3V
Peak Forward Current (1 pulse; 300μs)	3A

*JEDEC Registered Data.

connection diagram

Dual-In-Line Package



TOP VIEW

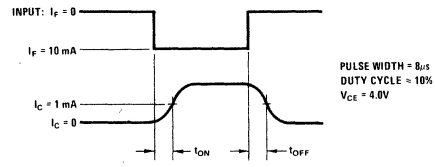
Order Number
4N25, 4N26, 4N27 or 4N28

electro-optical characteristics (T_A = 25°C, unless otherwise specified)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
LED CHARACTERISTICS							
I_R	Reverse Leakage Current	V_R = 3.0V, (Note 4)				100	μA
V_F	Forward Voltage	I_F = 50 mA, (Note 4)			1.2	1.5	V
C	Capacitance	V_R = 0V, f = 1.0 MHz			150		pF
PHOTOTRANSISTORS, I_F = 0							
H_{FE}	dc Current Gain	V_{CE} = 5.0V, I_C = 500μA			500		
I_{CBO}	Collector-Base Dark Current	V_{CB} = 10V, Emitter Open, (Note 4)				20	nA
BV_{CBO}	Collector-Base Breakdown Voltage	I_C = 100μA, I_E = 0, (Note 4)		70			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C = 1.0 mA, I_B = 0, (Note 4)		30			V
BV_{ECO}	Emitter-Collector Breakdown Voltage	I_E = 100μA, I_B = 0, (Note 4)		7.0			V
I_{CEO}	Collector-Emitter Dark Current	V_{CE} = 10V, Base Open, (Note 4)	4N25, 4N26, 4N27			50	nA
			4N28			100	nA
COUPLED CHARACTERISTICS							
I_C	Collector Output Current	V_{CE} = 10V, I_F = 10 mA, I_B = 0, (Note 4)	4N25, 4N26	2.0	10		mA
			4N27, 4N28	1.0			mA
V_{ISO}	Isolation Voltage	(Note 4)	4N25	2500			V
			4N26, 4N27	1500			V
			4N28	500			V
$V_{CE(SAT)}$	Collector-Emitter Saturation	I_C = 2.0 mA, I_F = 50 mA, (Note 4)			0.2	0.5	V
C_{ISO}	Isolation Capacitance	V = 0, f = 1.0 MHz			0.5		pF
BW	Bandwidth	I_F = 10 mA, V_{CE} = 5.0V, R_L = 100Ω, (Note 3)			150		kHz
t_{ON}	Output "ON" Time	I_F = 10 mA, pK = Fixed P.W. 8μs Fixed ≃ 10% dc, V_{CE} = 4V Fixed, R_L = 22Ω, (Notes 1 and 2)			1		μs
t_{OFF}	Output "OFF" Time	I_F = 10 mA, pK = Fixed P.W. 8μs Fixed ≅ 10% dc, V_{CE} = 4V Fixed, R_L = 22Ω, (Notes 1 and 2)			4		μs
R_{ISO}	Isolation Resistance	V = 500V			10^{11}		Ω

Note 1: Test conditions: from t = 0 of I_F until I_C exceeds 1.0 mA.
Note 2: Test condition: from end of I_F until I_C decreases below 1.0 mA.
Note 3: Specified as the point where the collector current transfer ratio is one-half that of the low frequency C.T.R. (100 Hz).
Note 4: JEDEC Registered Data.

switching time waveforms



NATIONAL

INTEGRATED CIRCUITS FOR DIGITAL DATA TRANSMISSION

INTRODUCTION

It is frequently necessary to transmit digital data in a high-noise environment where ordinary integrated logic circuits cannot be used because they do not have sufficient noise immunity. One solution to this problem, of course, is to use high-noise-immunity logic. In many cases, this approach would require worst case logic swings of 30V, requiring high power-supply voltages. Further, considerable power would be needed to transmit these voltage levels at high speed. This is especially true if the lines must be terminated to eliminate reflections, since practical transmission lines have a low characteristic impedance.

A much better solution is to convert the ground referred digital data at the transmission end into a differential signal and transmit this down a balanced, twisted-pair line. At the receiving end, any induced noise, or voltage due to ground-loop currents, appears equally on both ends of the twisted-pair line. Hence, a receiver which responds only to the differential signal from the line will reject the undesired signals even with moderate voltage swings from the transmitter.

Figure 1 illustrates this situation more clearly. When ground is used as a signal return as in Figure 1a, the voltage seen at the receiving end will be the output voltage of the transmitter plus any noise voltage induced in the signal line. Hence, the noise immunity of the transmitter-receiver combination must be equal to the maximum expected noise from both sources.

The differential transmission scheme diagrammed in Figure 1b solves this problem. Any ground noise or voltage induced on the transmission lines will appear equally on both inputs of the receiver. The receiver responds only to the differential signal coming out of the twisted-pair line and delivers a single-ended output signal referred to the ground

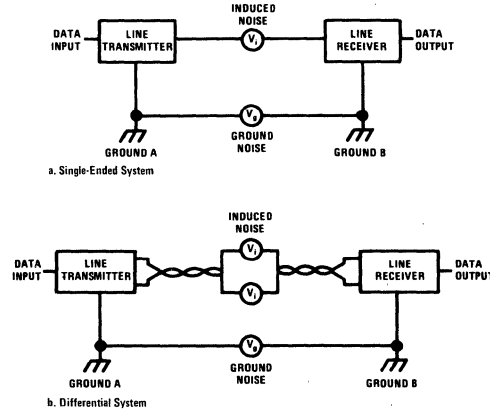


FIGURE 1. Comparing Differential and Single-Ended Data Transmission

at the receiving end. Therefore, extremely high noise immunities are not needed; and the transmitter and receiver can be operated from the same supplies as standard integrated logic circuits.

This article describes the operation and use of a line driver and line receiver for transmission systems using twisted-pair lines. The transmitter provides a buffered differential output from a DTL or TTL input signal. A four-input gate is included on the input so that the circuit can also perform logic. The receiver detects a zero crossing in the differential input voltage and can directly drive DTL or TTL integrated circuits at the receiving end. It also has strobe capability to blank out unwanted input signals. Both the transmitter and the receiver incorporate two independent units on a single silicon chip.

LINE DRIVER

Figure 2 shows a schematic diagram of the line transmitter. The circuit has a marked resemblance to a standard TTL buffer. In fact, it is possible to use a standard dual buffer as a transmitter. However, the DS7830 incorporates additional features. For one, the output is current limited to protect the driver from accidental shorts in the transmission lines. Secondly, diodes on the output clamp severe voltage transients that may be induced into the transmission lines. Finally, the circuit has internal inversion to produce a differential output signal, reducing the skew between the outputs and making the output state independent of loading.

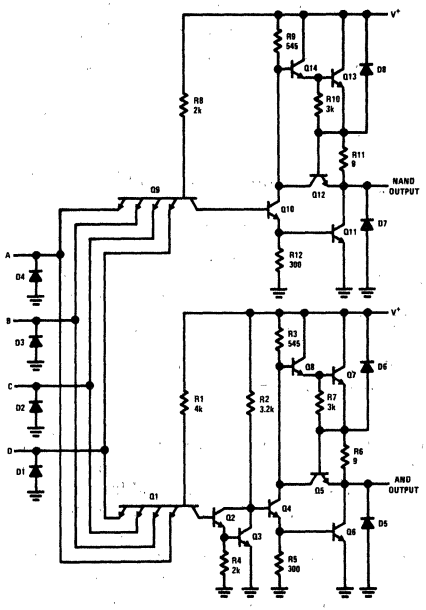


FIGURE 2. Schematic Diagram of the DS7830 Line Driver

As can be seen from the upper half of Figure 2, a quadruple-emitter input transistor, Q9, provides four logic inputs to the transmitter. This transistor drives the inverter stage formed by Q10 and Q11 to give a NAND output. A low state logic input on any of the emitters of Q9 will cause the base drive to be removed from Q10, since Q9 will be saturated by current from R8, holding the base of Q10 near ground. Hence, Q10 and Q11 will be turned off; and the output will be in a high state. When all the emitters of Q9 are at a one logic level, Q10 receives base drive from R8 through the forward biased collector-base junction of Q9. This saturates Q10 and also Q11, giving a low output state. The input voltage at which the transition occurs is equal to the sum of the emitter-base turn on voltages of Q10 and Q11 minus the saturation voltage of Q9. This is about 1.4V at 25°C.

A standard "totem-pole" arrangement is used on the output stage. When the output is switched to the high state, with Q10 and Q11 cut off, current is supplied to the load by Q13 and Q14 which are connected in a modified Darlington configuration. Because of the high compound current gain of these transistors, the output resistance is quite low and a large load current can be supplied. R10 is included across the emitter-base junction of Q13 both to drain off any collector-base leakage current in Q13 and to discharge the collector-base capacitance of Q13 when the output is switched to the low state. In the high state, the output level is approximately two diode drops below the positive supply, or roughly 3.6V at 25°C with a 5.0V supply.

With the output switched into the low state, Q10 saturates, holding the base of Q14 about one diode drop above ground. This cuts off Q13. Further, both the base current and the collector current of Q10 are driven into the base of Q11 saturating it and giving a low-state output of about 0.1V. The circuit is designed so that the base of Q11 is supplied 6 mA, so the collector can drive considerable load current before it is pulled out of saturation.

The primary purpose of R12 is to provide current to remove the stored charge in Q11 and charge its collector-base capacitance when the circuit is switched to the high state. Its value is also made enough less than R9 to prevent supply current transients which might otherwise occur* when the power supply is coming up to voltage.

*J. Kalb, "Design Considerations for a TTL Gate," *"National Semiconductor* TP-6, May, 1968.

The lower half of the transmitter in Figure 2 is identical to the upper, except that an inverter stage has been added. This is needed so that an input signal which drives the output of the upper half positive will drive the lower half negative, and vice versa, producing a differential output signal. Transistors Q2 and Q3 produce the inversion. Even though the current gain is not necessarily needed, the modified Darlington connection is used to produce the proper logic transition voltage on the input of the transmitter. Because of the low load capacitance that the inverter sees when it is completely within the integrated circuit, it is extremely fast, with a typical delay of 3 ns. This minimizes the skew between the outputs.

One of the schemes used when dual buffers are employed as a differential line driver is to obtain the NAND output in the normal fashion and provide the AND output by connecting the input of the second buffer to the NAND output. Using an internal inverter has some distinct advantages over this: for one, capacitive loads which slow down the response of the NAND output will not introduce a time skew between the two outputs; secondly, line transients on the NAND output will not cause an unwanted change of state on the AND output.

Clamp diodes, D1 through D4, are added on all inputs to clamp undershoot. This undershoot and ringing can occur in TTL systems because the rise and fall times are extremely short.

Output-current limiting is provided by adding a resistor and transistor to each of the complementary outputs. Referring again to Figure 2, when the current on the NAND output increases to a value where the voltage drop across R11 is sufficient to turn on Q12, the short circuit protection comes into effect. This happens because further increases in output current flow into the base of Q12 causing it to remove base drive from Q14 and, therefore, Q13. Any substantial increase in output current will then cause the output voltage to collapse to zero. Since the magnitude of the short circuit depends on the emitter base turn-on voltage of Q12, this current has a negative temperature coefficient. As the chip temperature increases from power dissipation, the available short circuit current is reduced. The current limiting also serves to control the current transient that occurs when the output is going through a transition with both Q11 and Q13 turned on.

The AND output is similarly protected by R6 and Q5, which limit the maximum output current to about 100 mA, preventing damage to the circuit from shorts between the outputs and ground.

The current limiting transistors also serve to increase the low state output current capability under severe transient conditions. For example, when the current into the NAND output becomes so high as to pull Q11 out of saturation, the output voltage will rise to two diode drops above ground. At this voltage, the collector-base junction of Q12 becomes forward biased and supplies additional base drive to Q11 through Q10 which is saturated. This minimizes any further increase in output voltage.

When either of the outputs are in the high state, they can drive a large current towards ground without a significant change in output voltage. However, noise induced on the transmission line which tries to drive the output positive will cut it off since it cannot sink current in this state. For this reason, D6 and D8 are included to clamp the output and keep it from being driven much above the supply voltage, as this could damage the circuit.

When the output is in a low state, it can sink a lot of current to clamp positive-going induced voltages on the transmission line. However, it cannot source enough current to eliminate negative-going transients so D5 and D7 are included to clamp those voltages to ground.

It is interesting to note that the voltage swing produced on one of the outputs when the clamp diodes go into conduction actually increases the diffferential noise immunity. For example with no induced common mode current, the low-state output will be a saturation voltage above ground while the high output will be two diode drops below the positive supply voltage. With positive-going common mode noise on the line, the low output remains in saturation; and the high output is clamped at a diode drop above the positive supply. Hence, in this case, the common mode noise increases the differential swing by three diode drops.

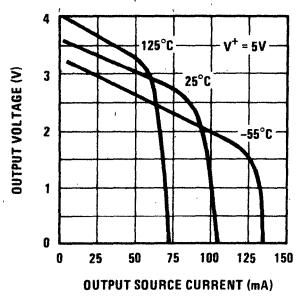


FIGURE 3. High State Output Voltage as a Function of Output Current

Having explained the operation of the line driver, it is appropriate to look at the performance in more detail. Figure 3 shows the high-state output characteristics under load. Over the normal range of output currents, the output resistance is about 10Ω. With higher output currents, the short circuit protection is activated, causing the output voltage to drop to zero. As can be seen from the figure, the short-circuit current decreases at higher temperatures to minimize the possibility of overheating the integrated circuit.

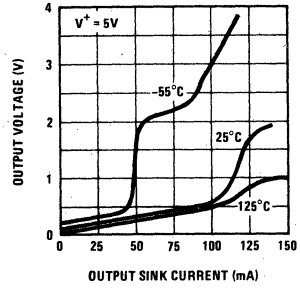


FIGURE 4. Low-State Output Current as a Function of Output Current

Figure 4 is a similar graph of the low-state output characteristics. Here, the output resistance is about 5Ω with normal values of output current. With larger currents, the output transistor is pulled out of saturation; and the output voltage increases. This is most pronounced at –55°C where the transistor current gain is the lowest. However, when the output voltage rises about two diode drops above ground, the collector-base junction of the current-limit transistor becomes forward biased, providing additional base drive for the output transistor. This roughly doubles the current available for clamping positive common-mode transients on the twisted-pair line. It is interesting to note that even though the output level increases to about 2V under this condition, the differential noise immunity does not suffer because the high-state output also increases by about 3V with positive going common-mode transients.

It is clear from the figure that the low state output current is not effectively limited. Therefore, the device can be damaged by shorts between the output and the 5V supply. However, protection against shorts between outputs or from the outputs to ground is provided by limiting the high-state current.

The curves in Figures 3 and 4 demonstrate the performance of the line driver with large, capacitively-coupled common-mode transients, or under

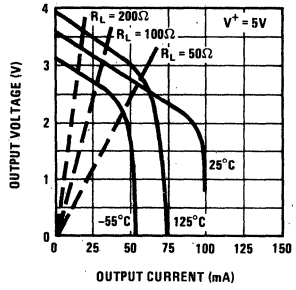


FIGURE 5. Differential Output Voltage as a Function of Differential Output Current

gross overload conditions. Figure 5 shows the ability of the circuit to drive a differential load: that is, the transmission line. It can be seen that for output currents less than 35 mA, the output resistance is approximately 15Ω. At both temperature extremes, the output falls off at high currents. At high temperatures, this is caused by current limiting of the high output state. At low temperatures, the falloff of current gain in the low-state output transistor produces this result.

Load lines have been included on the figure to show the differential output with various load resistances. The output swing can be read off from the intersection of the output characteristic with the load line. The figure shows that the driver can easily handle load resistances greater than 100Ω.

This is more than adequate for practical, twisted-pair lines.

Figure 6 shows the no load power dissipation, for one-half of the dual line driver, as a function of frequency. This information is important for two reasons. First, the increase in power dissipation at high frequencies must be added to the excess power dissipation caused by the load to determine the total package dissipation. Second, and more important, it is a measure of the "glitch" current which flows from the positive supply to ground through the output transistors when the circuit is going through a transition. If the output stage is

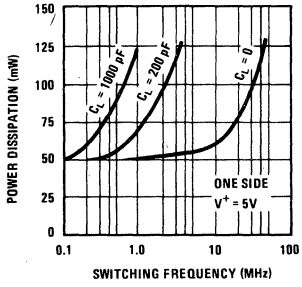


FIGURE 6. Power Dissipation as a Function of Switching Frequency

not properly designed, the current spikes in the power supplies can become quite large; and the power dissipation can increase by as much as a factor of five between 100 KHz and 10 MHz. The figure shows that, with no capacitive loading, the power increase with frequencies as high as 10 MHz is almost negligible. However, with large capacitive loads, more power is required.

The line receiver is designed to detect a zero crossing in the differential output of the line driver. Therefore, the propagation time of the driver is measured as the time difference between the application of a step input and the point where the differential output voltage crosses zero. A plot of the propagation time over temperature is shown in Figure 7. This delay is added directly to the propagation time of the transmission line and the delay of the line receiver to determine the total data-propagation time. However, in most cases, the delay of the driver is small, even by comparison to the uncertainties in the other delays.

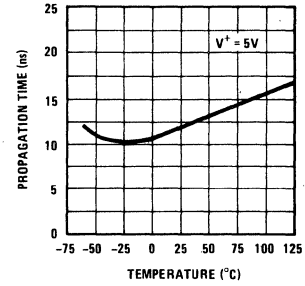


FIGURE 7. Propagation Time as a Function of Temperature

To summarize the characteristics of the DS7830 line driver, the input interfaces directly with standard DTL or TTL circuits. It presents a load which is equivalent to a fan out of 3 to the circuit driving it, and it operates from the 5.0V, ±10% logic supplies. The output can drive low impedance lines down to 50Ω and capacitive loads up to 5000 pF. The time skew between the outputs is minimized to reduce radiation from the twisted-pair lines, and the circuit is designed to clamp common mode transients coupled into the line. Short circuit protection is also provided. The integrated circuit consists of two independent drivers fabricated on a 41 x 53 mil-square die using the standard TTL process. A photomicrograph of the chip is shown in Figure 8.

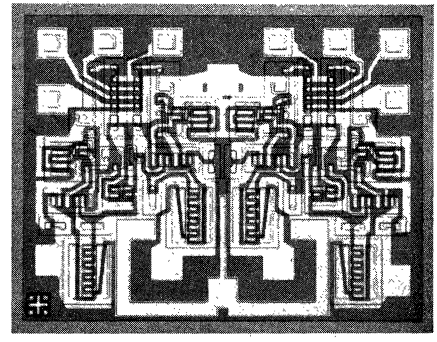


FIGURE 8. Photomicrograph of the DS7830 Dual Line Driver

LINE RECEIVER

As mentioned previously, the function of the line receiver is to convert the differential output signal of the line driver into a single ended, ground-referred signal to drive standard digital circuits on the receiving end. At the same time it must reject the common mode and induced noise on the transmission line.

Normally this would not be too difficult a task because of the large signal swings involved. However, it was considered important that the receiver operate from the +5V logic supply without requiring additional supply voltages, as do most other line receiver designs. This complicates the situation because the receiver must operate with ±15V input signals which are considerably greater than the operating supply voltage.

The large common mode range over which the circuit must work can be reduced with an attenuator on the input of the receiver. In this design, the input signal is attenuated by a factor of 30. Hence, the ±15V common mode voltage is reduced to ±0.5V, which can be handled easily by circuitry operating from a 5V supply. However, the differential input signal, which can go down as low as ±2.4V in the worst case, is also reduced to ±80 mV. Hence, it is necessary to employ a fairly accurate zero crossing detector in the receiver.

System requirements dictated that the threshold inaccuracy introduced by the zero crossing detector be less than 17 mV. In principle, this accuracy requirement should not pose insurmountable problems because it is a simple matter to make well matched parts in an integrated circuit.

Figure 9 shows a simplified schematic diagram of the circuit configuration used for the line receiver. The input signal is attenuated by the resistive dividers R1-R2 and R8-R3. This attenuated signal is fed into a balanced dc amplifier, operating in the common base configuration. This input amplifier, consisting of Q1 and Q2, removes the common mode component of the input signal. Further, it delivers an output signal at the collector of Q2, which is nearly equal in amplitude to the original differential input signal. This output signal is buffered by Q6 and drives an output amplifier, Q8. The output stage drives the logic load directly.

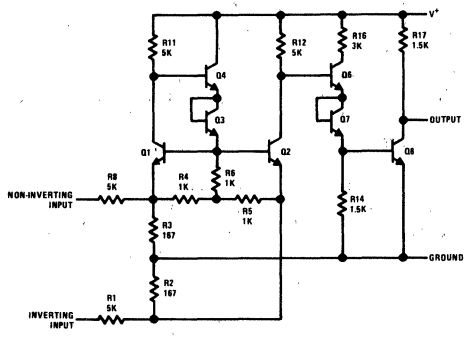


FIGURE 9. Simplified Schematic of the Line Receiver

An understanding of the circuit can be obtained by first considering the input stage. Assuming high current gains and neglecting the voltage drop across R3, the collector current of Q1 will be:

$$I_{C1} = \frac{V^+ - V_{BE1} - V_{BE3} - V_{BE4}}{R11}. \qquad (1)$$

With equal emitter-base voltages for all transistors, this becomes:

$$I_{C1} = \frac{V^+ - 3V_{BE}}{R11}. \qquad (2)$$

The output voltage at the collector of Q2 will be:

$$V_{C2} = V^+ - I_{C2}R12. \qquad (3)$$

When the differential input voltage to the receiver is zero, the voltages presented to the emitters of Q1 and Q2 will be equal. If Q1 and Q2 are matched devices, which is easy to arrange when they are fabricated close together on a single silicon chip, their collector currents will be equal with zero input voltage. Hence, the output voltage from Q2 can be determined by substituting (2) into (3):

$$V_{C2} = V^+ - \frac{R12}{R11}(V^+ - 3V_{BE}). \qquad (4)$$

For R11 = R12, this becomes:

$$V_{C2} = 3V_{BE}.$$

The voltage on the base of Q6 will likewise be $3V_{BE}$ when the output is on the verge of switching from a zero to a one state. A differential input signal which causes Q2 to conduct more heavily will then make the output go high, while an input signal in the opposite direction will cause the output to saturate.

It should be noted that the balance of the circuit is not affected by absolute values of components—only by how well they match. Nor is it affected by variations in the positive supply voltage, so it will perform well with standard logic supply voltages between 4.5V and 5.5V. In addition, component values are chosen so that the collector currents of Q4 and Q6 are equal. As a result, the base currents of Q4 and Q6 do not upset the balance of the input stage. This means that circuit performance is not greatly affected by production or temperature variations in transistor current gain.

A complete schematic of the line receiver, shown in Figure 10, shows several refinements of the basic circuit which are needed to secure proper operation under all conditions. For one, the explanation of the simplified circuit ignores the fact that the collector current of Q1 will be affected by common mode voltage developed across R3. This can give a 0.5V threshold error at the extremes of the ±15V common mode range. To compensate for this, a separate divider, R9 and R10, is used to maintain a constant collector current in Q1 with varying common mode signals. With an increasing common mode voltage on the non-inverting input, the voltage on the emitter of Q1 will increase. Normally, this would cause the voltage across R11 to decrease, reducing the collector current of Q1. However, the increasing common mode signal also drives the top end of R11 through R9 and R10 so as to hold the voltage drop across R11 constant.

In addition to improving the common mode rejection, R9 also forces the output of the receiver into the high state when nothing is connected to the input lines. This means that the output will be in a pre-determined state when the transmission cables are disconnected.

A diode connected transistor, Q5, is also added in the complete circuit to provide strobe capability. With a logic zero on the strobe terminal, the out-

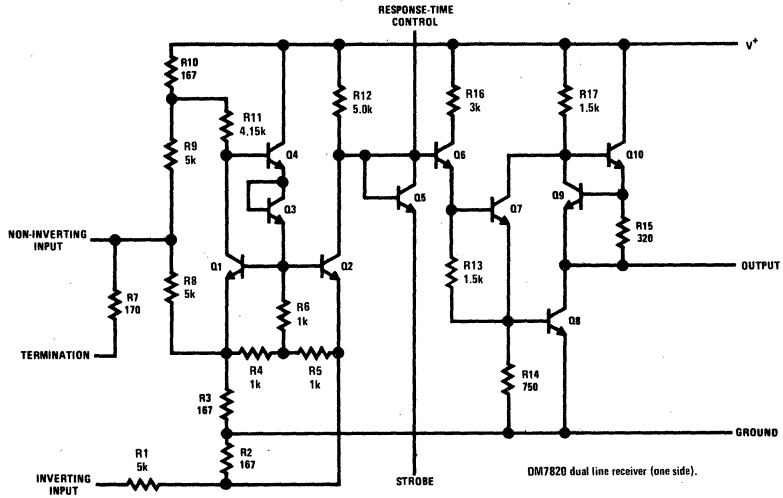


FIGURE 10. Complete Schematic of One Half of the DS7820 Line Receiver

put will be high no matter what the input signal is. With the strobe, the receiver can be made immune to any noise signals during intervals where no digital information is expected. The output state with the strobe on is also the same as the output state with the input terminals open.

The collector of Q2 is brought out so that an external capacitor can be used to slow down the receiver to where it will not respond to fast noise spikes. This capacitor, which is connected between the response-time-control terminal and ground, does not give exactly-symmetrical delays. The delay for input signals which produce a positive-going output will be less than for input signals of opposite polarity. This happens because the impedance on the collector of Q2 drops as Q6 goes into saturation, reducing the effectiveness of the capacitor.

Another difference in the complete circuit is that the output stage is improved both to provide more gain and to reduce the output resistance in the high output state. This was accomplished by adding Q9 and Q10. When the output stage is operating in the linear region, that is, on the verge of switching to either the high or the low state, Q9 and Q10 form sort of an active collector load for Q8. The current through R15 is constant at approximately 2 mA as the output voltage changes through the active region. Hence, the percentage change in the collector current of Q8 due to the voltage change across R17 is made smaller by this pre-bias current; and the effective stage gain is increased.

With the output in the high state (Q8 cut off), the output resistance is equal to R15, as long as the load current is less than 2 mA. When the load current goes above this value, Q9 turns on; and the output resistance increases to 1.5K, the value of R17.

This particular output configuration gives a higher gain than either a standard DTL or TTL output stage. It can also drive enough current in the high state to make it compatible with TTL, yet outputs can be wire OR'ed as with DTL.

Remaining details of the circuit are that Q7 is connected as an emitter follower to make the circuit even less sensitive to transistor current gains. R16 limits the base drive to Q7 with the output saturated, while R17 limits the base drive to the output transistor, Q8. A resistor, R7, which can be used to terminate the twisted-pair line is also included on the chip. It is not connected directly across the inputs. Instead, one end is left open so that a capacitor can be inserted in series with the resistor. The capacitor significantly reduces the power dissipation in both the line transmitter and receiver, especially in low-duty-cycle applications, by terminating the line at high frequencies but blocking steady-state current flow in the terminating resistor.

Since line receivers are generally used repetitively in a system, the DS7820 has been designed with two independent receivers on a single silicon chip. The device is fabricated on a 41 x 49 mil-square die using the standard six mask planar-epitaxial process. The processing employed is identical to that used on TTL circuits, and the design does not impose any unusual demands on the processing. It is only required that various parts within the circuit match well, but this is easily accomplished in a monolithic integrated circuit without any special effort in manufacturing. A photomicrograph of the integrated circuit chip is shown in **Figure 11**.

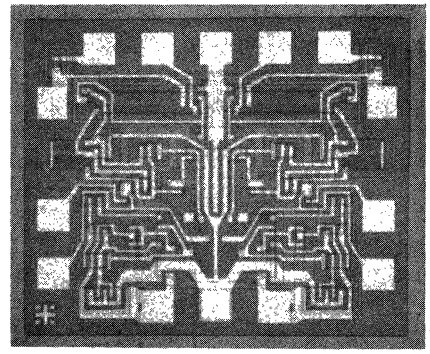


FIGURE 11. Photomicrograph of the DS7820 Dual Line Receiver

The only components in the circuit which see voltages higher than standard logic circuits are the resistors used to attenuate the input signal. These resistors, R1, R7, R8 and R9, are diffused into a separate, floating, N-type isolation tub, so that the higher voltage is not seen by any of the transistors. For a ±15V input voltage range, the breakdown voltages required for the collector-isolation and collector-base diodes are only 15V and 19V, respectively. These breakdown voltages can be achieved readily with standard digital processing.

The purpose of the foregoing was to provide some insight into circuit operation. A more exact mathematical analysis of the device is developed in Appendix A.

RECEIVER PERFORMANCE

The characteristics of the line receiver are described graphically in Figures 12 through 18. Figure 12 illustrates the effect of supply voltage variations on the threshold accuracy. The upper curve gives the differential input voltage required to hold the output at 2.5V while it is supplying 200 μA to the digital load. The lower curve shows the differential input needed to hold the output at 0.4V while it sinks 3.5 mA from the digital load. This load corresponds to a worst case fanout of 2 with either DTL or TTL integrated circuits. The data shows that the threshold accuracy is only affected by ±60 mV for a ±10% change in supply voltage. Proper operation can be secured over a wider range of supply voltages, although the error becomes excessive at voltages below 4V.

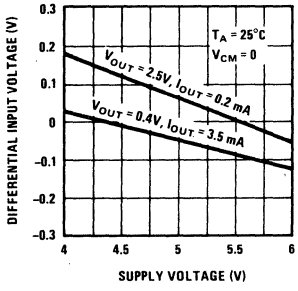


FIGURE 12. Differential Input Voltage Required for High or Low Output as a Function of Supply Voltage

Figure 13 is a similar plot for varying common mode input voltage. Again the differential input voltages are given for high and low states on the output with a worst case fanout of 2. With precisely matched components within the integrated circuit, the threshold voltage will not change with common mode voltage. The mismatches typically encountered give a threshold voltage change of ±100 mV over a ±20V common mode range. This change can have either a positive slope or a negative slope.

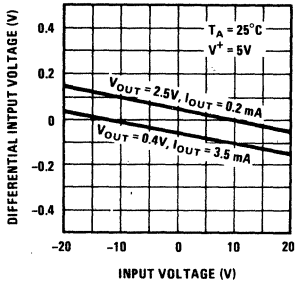


FIGURE 13. Differential Input Voltage Required for High or Low Output as a Function of Common Mode Voltage

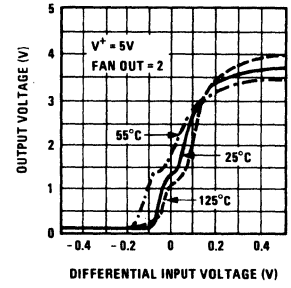


FIGURE 14. Voltage Transfer Function

The transfer function of the circuit is given in Figure 14. The loading is for a worst case fanout of 2. The digital load is not linear, and this is reflected as a non-linearity in the transfer function which occurs with the output around 1.5V. These transfer characteristics show that the only significant effect of temperature is a reduction in the positive swing at -55°C. However, the voltage available remains well above the 2.5V required by digital logic.

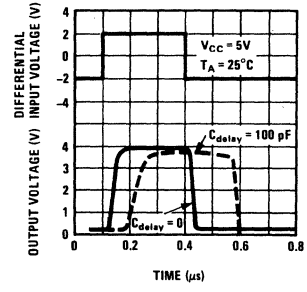


FIGURE 15. Response Time With and Without an External Delay Capacitor

Figure 15 gives the response time, or propagation delay, of the receiver. Normally, the delay through the circuit is about 40 ns. As shown, the delay can be increased, by the addition of a capacitor between the response-time terminal and ground, to make the device immune to fast noise spikes on the input. The delay will generally be longer for negative going outputs than for positive going outputs.

Under normal conditions, the power dissipated in the receiver is relatively low. However, with large common mode input voltages, dissipation increases markedly, as shown in Figure 16. This is of little consequence with common mode transients, but the increased dissipation must be taken into account when there is a dc difference between the grounds of the transmitter and the receiver. It is important to note that Figure 16 gives the dissipation for one half the dual receiver. The total package dissipation will be twice the values given when both sides are operated under identical conditions.

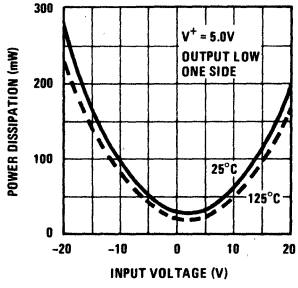


FIGURE 16. Internal Power Dissipation as a Function of Common Mode Input Voltage

Figure 17 shows that the power supply current also changes with common mode input voltage due to the current drawn out of or fed into the supply through R9. The supply current reaches a maximum with negative input voltages and can actually reverse with large positive input voltages. The figure also shows that the supply current with the output switched into the low state is about 3 mA higher than with a high output.

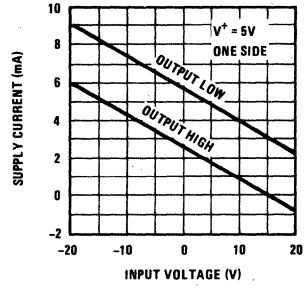


FIGURE 17. Power Supply Current as a Function of Common Mode Input Voltage

The variation of the internal termination resistance with temperature is illustrated in Figure 18.Taking into account the initial tolerance as well as the change with temperature, the termination resistance is by no means precise. Fortunately, in most cases, the termination resistance can vary appreciably without greatly affecting the characteristics of the transmission line. If the resistor tolerance is a problem, however, an external resistor can be used in place of the one provided within the integrated circuit.

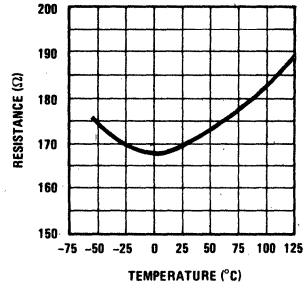


FIGURE 18. Variation of Termination Resistance With Temperature

DATA TRANSMISSION

The interconnection of the DS7830 line driver with the DS7820 line receiver is shown in Figure 19. With the exception of the transmission line, the design is rather straightforward. Connections on the input of the driver and the output or strobe of the receiver follow standard design rules for DTL or TTL integrated logic circuits. The load presented by the driver inputs is equal to 3 standard digital loads, while the receiver can drive a worst-case fanout of 2. The load presented by the receiver strobe is equal to one standard load.

The purpose of C1 on the receiver is to provide dc isolation of the termination resistor for the transmission line. This capacitor can both increase the differential noise immunity, by reducing attenuation on the line, and reduce power dissipation in both the transmitter and receiver. In some applications, C1 can be replaced with a short between Pins 1 and 2, which connects the internal termination resistor of the DS7820 directly across the line. C2 may be included, if necessary, to control the response time of the receiver, making it immune to noise spikes that may be coupled differentially into the transmission lines.

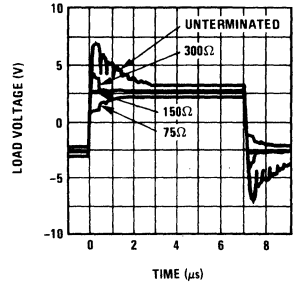


FIGURE 20. Transmission Line Response With Various Termination Resistances

The effect of termination mismatches on the transmission line is shown in Figure 20. The line was constructed of a twisted pair of No. 22 copper conductors with a characteristic impedance of approximately 170Ω. The line length was about 150 ns and it was driven directly from a DS7830 line driver. The data shows that termination resistances which are a factor of two off the nominal value do not cause significant reflections on the line. The lower termination resistors do, however, increase the attenuation.

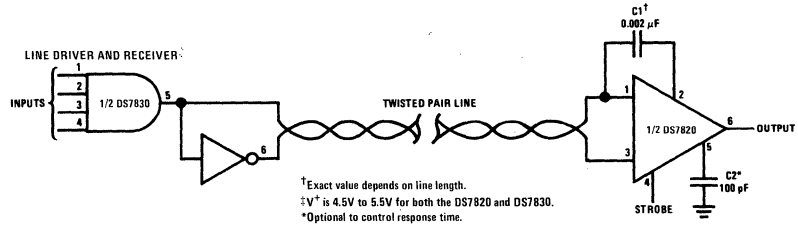


FIGURE 19. Interconnection of the Line Driver and Line Receiver

Figure 21 gives the line-transmission characteristics with various termination resistances when a dc isolation capacitor is used. The line is identical to that used in the previous example. It can be seen that the transient response is nearly the same as a dc terminated line. The attenuation, on the other hand, is considerably lower, being the same as an unterminated line. An added advantage of using the isolation capacitor is that the dc signal current is blocked from the termination resistor which reduces the average power drain of the driver and the power dissipation in both the driver and receiver.

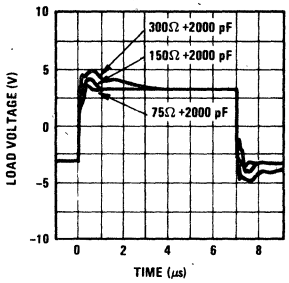


FIGURE 21. Line Response for Various Termination Resistances With a DC Isolation Capacitor

The effect of different values of dc isolation capacitors is illustrated in Figure 22. This shows that the RC time constant of the termination resistor/isolation capacitor combination should be 2 to 3 times the line delay. As before, this data was taken for a 150 ns long line.

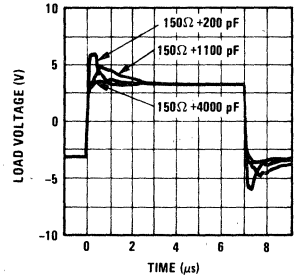
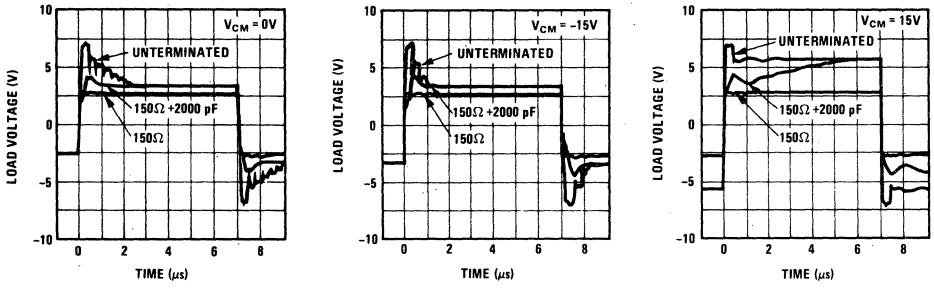


FIGURE 22. Response of Terminated Line With Different DC Isolation Capacitors

In Figure 23, the influence of a varying ground voltage between the transmitter and the receiver is shown. The difference in the characteristics arises because the source resistance of the driver is not constant under all conditions. The high output of



a. V_{CM} = 0V b. V_{CM} = –15V c. V_{CM} = 15V

FIGURE 23. Line Response With Different Terminations and Common Mode Input Voltages

the transmitter looks like an open circuit to voltages reflected from the receiving end of the transmission line which try to drive it higher than its normal dc state. This condition exists until the voltage at the transmitting end becomes high enough to forward bias the clamp diode on the 5V supply. Much of the phenomena which does not follow simple transmission-line theory is caused by this. For example, with an unterminated line, the overshoot comes from the reflected signal charging the line capacitance to where the clamp diodes are forward biased. The overshoot then decays at a rate determined by the total line capacitance and the input resistance of the receiver.

When the ground on the receiver is 15V more negative than the ground at the transmitting end, the decay with an unterminated line is faster, as shown in Figure 23b. This occurs because there is more current from the input resistor of the receiver to discharge the line capacitance. With a terminated line, however, the transmission characteristics are the same as for equal ground voltages because the terminating resistor keeps the line from getting charged.

Figure 23c gives the transmission characteristics when the receiver ground is 15V more positive than the transmitter ground. When the line is not terminated, the differential voltage swing is increased because the high output of the driver will be pulled against the clamp diodes by the common mode input current of the receiver. With a dc isolation capacitor, the differential swing will reach this same value with a time constant determined by the isolation capacitor and the input resistance of the receiver. With a dc coupled termination, the characteristics are unchanged because the differential load current is large by comparison to the common mode current so that the output transistors of the driver are always conducting.

The low output of the driver can also be pulled below ground to where the lower clamp diode conducts, giving effects which are similar to those described for the high output. However, a current of about 9 mA is required to do this, so it does not happen under normal operating conditions.

To summarize, the best termination is an RC combination with a time constant approximately equal to 3 times the transmission-line delay. Even though its value is not precisely determined, the internal termination resistor of the integrated circuit can be used because the line characteristics are not greatly affected by the termination resistor.

The only place that an RC termination can cause problems is when the data transmission rate approaches the line delay and the attenuation down the line (terminated) is greater than 3 dB. This would correspond to more than 1000 ft. of twisted-pair cable with No. 22 copper conductors. Under these conditions, the noise margin can disappear with low-duty-cycle signals. If this is the case, it is best to operate the twisted-pair line without a termination to minimize transmission losses. Reflections should not be a problem as they will be absorbed by the line losses.

CONCLUSION

A method of transmitting digital information in high-noise environments has been described. The technique is a much more attractive solution than high-noise-immunity logic as it has lower power consumption, provides more noise rejection, operates from standard 5V supplies, and is fully compatible with almost all integrated logic circuits. An additional advantage is that the circuits can be fabricated with integrated circuit processes used for standard logic circuits.

APPENDIX A

LINE RECEIVER

Design Analysis

The purpose of this appendix is to derive mathematical expressions describing the operation of the line receiver. It will be shown that the performance of the circuit is not greatly affected by the absolute value of the components within the integrated circuit or by the supply voltage. Instead, it depends mostly on how well the various parts match.

The analysis will assume that all the resistors are well matched in ratio and that the transistors are likewise matched, since this is easily accomplished over a broad temperature range with monolithic construction. However, the effects of component mismatching will be discussed where important. Further, large transistor current gains will be assumed, but it will be pointed out later that this is valid for current gains greater than about 10.

A schematic diagram of the DS7820 line receiver is shown in Figure A-1. Referring to this circuit, the collector current of the input transistor is given by

$$I_{C1} = \frac{V^+ - V_{BE1} - V_{BE3} - V_{BE4}}{R9 \,//\, R10 + R11 + R3 \,//\, R8} - \frac{\frac{R3}{R4 + 2R6 + R3} V_{BE1} - \frac{R3 \,//\, R11}{R8 + R3 \,//\, R1} V_{IN}}{R9 \,//\, R10 + R11 + R3 \,//\, R8} + \frac{(V_{IN} - V^+) \frac{R10 \,//\, R11}{R9 + R10 \,//\, R11}}{R9 \,//\, R10 + R11 + R3 \,//\, R8} \quad \text{(A. 1)}$$

where V_{IN} is the common mode input voltage and $R_a//R_b$ denotes the parallel connection of the two resistors. In Equation (A. 1), R8 = R9, R3 = R10, R10 << R11, R9 >> R10, R3 << R11, R8>>R3 and $\frac{R3}{R4 + 2R6 + R3}$ <<3 so it can be reduced to

$$I_{C1} = \frac{V^+ - 3V_{BE} - \frac{R10}{R9} V^+}{R10 + R11 + R3} \quad \text{(A. 2)}$$

which shows that the collector current of Q1 is not affected by the common mode voltage.

The output voltage on the collector of Q2 is

$$V_{C2} = V^+ - I_{C2} R12 \quad \text{(A. 3)}$$

For zero differential input voltage, the collector currents of Q1 and Q2 will be equal so Equation (A. 3) becomes

$$V_{C2} = V^+ - \frac{R12 \left(V^+ - 3V_{BE} - \frac{R10}{R9} V^+\right)}{R10 + R11 + R3} \quad \text{(A. 4)}$$

It is desired that this voltage be $3V_{BE}$ so that the output stage is just on the verge of switching with zero input. Forcing this condition and solving for R12 yields

$$R12 = (R10 + R11 + R3) \frac{V^+ - 3V_{BE}}{V^+ - 3V_{BE} - \frac{R10}{R9} V^+} \quad \text{(A. 5)}$$

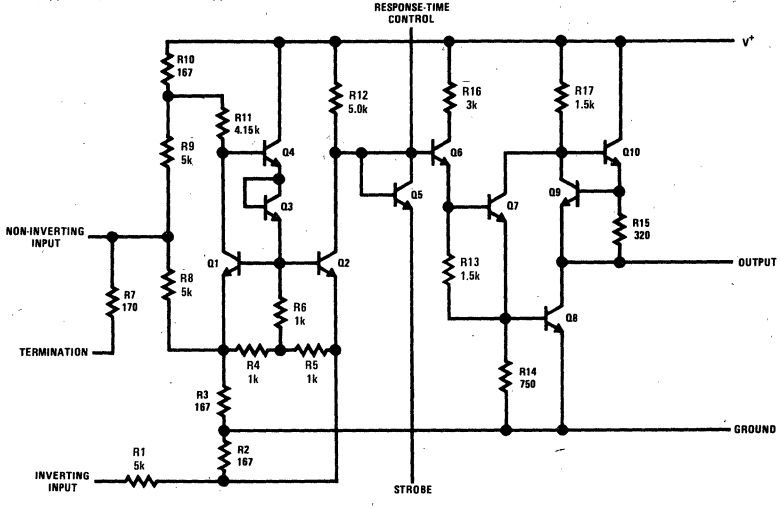


FIGURE A-1. Schematic Diagram of One Half of the DS7820 Line Receiver

This shows that the optimum value of R12 is dependent on supply voltage. For a 5V supply it has a value of 4.7 kΩ. Substituting this and the other component values into (A. 4),

$$V_{C2} = 2.83V_{BE} + 0.081V^{+}, \qquad \text{(A. 6)}$$

which shows that the voltage on the collector of Q2 will vary by about 80 mV for a 1V change in supply voltage.

The next step in the analysis is to obtain an expression for the voltage gain of the input stage.

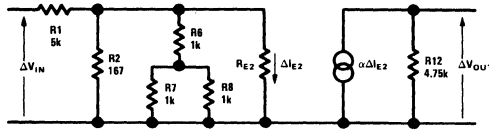


FIGURE A-2. Equivalent Circuit Used to Calculate Input Stage Gain

An equivalent circuit of the input stage is given in Figure A-2. Noting that R6 = R7 = R8 and R2 ≅ 0.1 (R6 + R7//R8), the change in the emitter current of Q1 for a change in input voltage is

$$\Delta I_{E2} = \frac{0.9\ R2}{R1\ (0.9\ R2 + R_{E2})}\ \Delta V_{IN}\ . \qquad \text{(A. 7)}$$

Hence, the change in output voltage will be

$$\Delta V_{OUT} = \alpha I_{E2} R12$$

$$= \frac{0.9\ \alpha\ R2\ R12}{R1\ (0.9\ R2 + R_{E2})}\ \Delta V_{IN}\ . \qquad \text{(A. 8)}$$

Since $\alpha \cong 1$, the voltage gain is

$$A_{V1} = \frac{0.9\ R2\ R12}{R1\ (0.9\ R2 + R_{E2})} \qquad \text{(A. 9)}$$

The emitter resistance of Q2 is given by

$$R_{E2} = \frac{kT}{qI_{C2}}\ , \qquad \text{(A. 10)}$$

where

$$I_{C2} = \frac{V^{+} - 3V_{BE}}{R12} \qquad \text{(A. 11)}$$

so

$$R_{E2} = \frac{kT\ R12}{q\ (V^{+} - 3V_{BE})} \qquad \text{(A. 12)}$$

Therefore, at 25°C where V_{BE} = 670 mV and kT/q = 26 mV, the computed value for gain is 0.745. The gain is not greatly affected by temperature as the gain at −55°C where V_{BE} = 810 mV and kT/q = 18 mV is 0.774, and the gain at 125°C where V_{BE} = 480 mV and kT/q = 34 mV is 0.730.

With a voltage gain of 0.75, the results of Equation (A. 6) show that the input referred threshold voltage will change by 0.11V for a 1V change in supply voltage. With the standard ±10-percent supplies used for logic circuits, this means that the threshold voltage will change by less than ±60 mV.

Finally, the threshold error due to finite gain in the output stage can be considered. The collector current of Q7 from the bleeder resistor R14, is large by comparison to the base current of Q8, if Q8 has a reasonable current gain. Hence, the collector current of Q7 does not change appreciably when the output switches from a logic one to a logic zero. This is even more true for Q6, an emitter follower which drives Q7. Therefore, it is safe to presume that Q6 does not load the output of the first-stage amplifier, because of the compounded current gain of the three transistors, and that Q8 is driven from a low resistance source.

It follows that the gain of the output stage can be determined from the change in the emitter-base voltage of Q8 required to swing the output from a logic one state to a logic zero state. The expression

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{C1}}{I_{C2}} \qquad \text{(A. 13)}$$

describes the change in emitter-base voltage required to vary the collector current from one value, I_{C1}, to a second, I_{C2}. With the output of the receiver in the low state, the collector current of Q8 is

$$I_{OL} = \frac{V^{+} - V_{OL} - V_{BE9} - V_{BE10}}{R17}$$

$$+ \frac{V_{BE9}}{R15} - \frac{V_{BE8}}{R14} + \frac{V_{BE7}}{R13} + I_{SINK}\ , \qquad \text{(A. 14)}$$

where V_{OL} is the low state output voltage and I_{SINK} is the current load from the logic that the receiver is driving. Noting that R13 = 2R14 and figuring that all the emitter-base voltages are the same, this becomes

$$I_{OL} = \frac{V^{+} - V_{OL} - 2V_{BE}}{R17} + \frac{V_{BE}}{R15}$$

$$- \frac{V_{BE}}{2R14} + I_{SINK}\ . \qquad \text{(A. 15)}$$

Similarly, with the output in the high state, the collector current of Q8 is

$$I_{OH} = \frac{V^{+} - V_{OH} - V_{BE9} - V_{BE10}}{R17}$$

$$+ \frac{V_{BE9}}{R15} - \frac{V_{BE8}}{R14}$$

$$+ \frac{V_{BE7}}{R13} - I_{SOURCE}\ , \qquad \text{(A. 16)}$$

where V_{OH} is the high-level output voltage and I_{SOURCE} is the current needed to supply the input leakage of the digital circuits loading the comparator.

With the same conditions used in arriving at (A. 15), this becomes

$$I_{OH} = \frac{V^+ - V_{OH} - 2V_{BE}}{R17} + \frac{V_{BE}}{R15}$$

$$- \frac{V_{BE}}{2R14} - I_{SOURCE} \cdot \qquad \text{(A. 17)}$$

From (A. 13) the change in the emitter-base voltage of Q8 in going from the high output level to the low output level is

$$\Delta V_{BE} = \frac{kT}{q} \log_e \frac{I_{OL}}{I_{OH}} \qquad \text{(A. 18)}$$

providing that Q8 is not quite in saturation, although it may be on the verge of saturation.

The change of input threshold voltage is then

$$\Delta V_{TH} = \frac{kT}{qA_{V1}} \log_e \frac{I_{OL}}{I_{OH}} \qquad \text{(A. 19)}$$

where A_{V1} is the input stage gain. With a worst case fanout of 2, where V_{OH} = 2.5V, V_{OL} = 0.4V, I_{SOURCE} = 40 μA and I_{SINK} = 3.2 mA, the calculated change in threshold is 37 mV at 25°C, 24 mV at −55°C and 52 mV at 125°C.

The measured values of overall gain differ by about a factor of two from the calculated gain. This is not too surprising because a number of assumptions were made which introduce small errors, and all these errors lower the gain. It is also not too important because the gain is high enough where another factor of two reduction would not cause the circuit to stop working.

The main contributors to this discrepancy are the non-ideal behavior of the emitter-base voltage of Q8 due to current crowding under the emitter and the variation in the emitter base voltage of Q7 and Q8 with changes in collector-emitter voltage (h_{RE}).

Although these parameters can vary considerably with different manufacturing methods, they are relatively fixed for a given process. The ΔV_{BE} errors introduced by these quantities, if known, can be added directly into Equation (A. 18) to give a more accurate gain expression.

The most stringent matching requirement in the receiver is the matching of the input stage divider resistors: R1 with R8 and R2 with R3. As little as 1% mismatch in one of these pairs can cause a threshold shift of 150 mV at the extremes of the ±15V common mode range. Because of this, it is necessary to make the resistors absolutely identical and locate them close together. In addition, since R1 and R8 do dissipate a reasonable amount of power, they have to be located to minimize the thermal gradient between them. To do this, R9 was located between R1 and R8 so that it would heat both of these resistors equally. There are not serious heating problems with R2 and R3; however, because of their low resistance value, it was necessary even to match the lengths of the aluminum interconnects, as the resistance of the aluminum is high enough to cause intolerable mismatches. Of secondary importance is the matching of Q1 and Q2 and the matching of ratios between R11 and R12. A 1 mV difference in the emitter-base voltages of Q1 and Q2 causes a 30 mV input offset voltage as does a 1% mismatch in the ratio of R11 to R12.

The circuit is indeed insensitive to transistor current gains as long as they are above 10. The collector currents of Q4 and Q6 are made equal so that their base currents load the collectors of Q1 and Q2 equally. Hence, the input threshold voltage is affected only by how well the current gains match. Low current gain in the output transistor, Q8, can cause a reduction in gain. But even with a current gain of 10, the error produced in the input threshold voltage is less than 50 mV.

NATIONAL

APPLYING MODERN CLOCK DRIVERS TO MOS MEMORIES

INTRODUCTION

MOS memories present unique system and circuit challenges to the engineer since they require precise timing of input wave forms. Since these inputs present large capacitive loads to drive circuits, it is often that timing problems are not discovered until an entire system is constructed. This paper covers the practical aspects of using modern clock drivers in MOS memory systems. Information includes selection of packages and heat sinks, power dissipation, rise and fall time considerations, power supply decoupling, system clock line ringing and crosstalk, input coupling techniques, and example calculations. Applications covered include driving various types shift registers and RAM's (Random Access Memories) using logical control as well as other techniques to assure correct non-overlap of timing waveforms.

Although the information given is generally applicable to any type of monolithic integrated circuit, the DS0025, DS0026 and DS0056 are selected as examples because of their low cost.

The DS0025 was the first monolithic clock driver. It is intended for applications up to one megacycle where low cost is of prime concern. Table I illustrates its performance while Appendix I describes its circuit operation. Its monolithic, rather than hybrid or module construction, was made possible by a new high voltage-gold doped process utilizing a collector sinker to minimize $V_{CE\,SAT}$.

The DS0026 is a high speed, low cost, monolithic clock driver intended for applications above one megacycle. Table II illustrates its performance characteristics while its unique circuit design is presented in Appendix II. The DS0056 is a variation of the DS0026 circuit which allows the system designer to modify the output performance of the circuit. The DS0056 can be connected (using a second power supply) to increase the positive output voltage level and reduce the effect of cross coupling capacitance between the clock lines in the system. Of course the above are just examples of the many different types that are commercially available. Other National Semiconductor MOS interface circuits are listed in Appendix III.

The following section will hopefully allow the design engineer to select and apply the best circuit to his particular application while avoiding common system problems.

PRACTICAL ASPECTS OF USING MOS CLOCK DRIVERS

Package and Heat Sink Selection

Package type should be selected on power handling capability, standard size, ease of handling, availability of sockets, ease or type of heat sinking required, reliability and cost. Power handling capability for various packages is illustrated in Table III. The following guidelines are recommended:

TABLE I. DS0025 Characteristics

PARAMETER	CONDITIONS ($V^+ - V^-$) = 17V	VALUE	UNITS
t_{ON}		15	ns
t_{OFF}	C_{IN} = 0.0022μF, R_{IN} = 0Ω	30	ns
t_r	C_L = 0.0001μF, R0 = 50Ω	25	ns
t_f		150	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = −1mA	$V^+ - 0.7$	V
Negative Output Voltage Swing	I_{IN} = 10mA, I_{OUT} = 1mA	$V^- + 1.0$	V
On Supply Current (V^+)	I_{IN} = 10 mA	17	mA

TABLE II. DS0026 Characteristics

PARAMETER	CONDITIONS ($V^+ - V^-$) = 17V	VALUE	UNITS
t_{ON}		7.5	ns
t_{OFF}	C_{IN} = 0.001μF, R_{IN} = 0Ω	7.5	ns
t_r	R0 = 50Ω, C_L = 1000 pF	25	ns
t_f		25	ns
Positive Output Voltage Swing	$V_{IN} - V^-$ = 0V, I_{OUT} = −1mA	$V^+ - 0.7$	V
Negative Output Voltage Swing	I_{IN} = 10mA, I_{OUT} = 1mA	$V^- + 0.5$	V
On Supply Current (V^+)	I_{IN} = 10 mA	28	mA

The TO-5 ("H") package is rated at 750 mW still air (derate at 200°C/W above 25°C) soldered to PC board. This popular cavity package is recommended for small systems. Low cost (about 10 cents) clip-on heat sink increases driving capability by 50%.

The 8-pin ("N") molded mini-DIP is rated at 600 mW still air (derate at 90°C/W above 25°C) soldered to PC board (derate at 1.39W). Constructed with a special copper lead frame, this package is recommended for medium size commercial systems particularly where automatic insertion is used. (Please note for prototype work, that this package is only rated at 600 mW when mounted in a socket and not one watt until it is soldered down.)

To TO-8 ("G") package is rated at 1.5W still air (derate at 100°C/W above 25°C) and 2.3W with clip-on heat sink (Wakefield type 215-1.9 or equivalent-derate at 15 mW/°C). Selected for its power handling capability and moderate cost, this hermetic package will drive very large systems at the lowest cost per bit.

Additional information is given in the section of this data book on Maximum Power Dissipation (page 2).

Power Dissipation Considerations

The amount of registers that can be driven by a given clock driver is usually limited first by internal power dissipation. There are four factors:

1. Package and heat sink selection
2. Average dc power, P_{DC}
3. Average ac power, P_{AC}
4. Numbers of drivers per package, n

From the package heat sink, and maximum ambient temperature one can determine P_{MAX}, which is the maximum internal power a device can handle and still operate reliably. The total average power dissipated in a driver is the sum of dc power and ac power in each driver times the number of drivers. The total of which must be less than the package power rating.

$$P_{DISS} = n \times (P_{AC} + P_{DC}) \leq P_{MAX} \qquad (1)$$

Average dc power has three components: input power, power in the "OFF" state (MOS logic "0") and power in the "ON" state (MOS logic "1").

$$P_{DC} = P_{IN} + P_{OFF} + P_{ON} \qquad (2)$$

For most types of clock drivers, the first two terms are negligible (less than 10 mW) and may be ignored.

Thus:

$$P_{DC} \cong P_{ON} = \frac{(V^+ - V^-)^2}{Req} \times (DC)$$

where:

$V^+ - V^-$ = Total voltage across the driver

Req = Equivalent device resistance in the "ON" state

$$= V^+ - V^- / I_{S(ON)} \qquad (3)$$

DC = Duty Cycle

$$= \frac{\text{"ON" Time}}{\text{"ON" Time + "OFF" Time}}$$

For the DS0025, Req is typically 1 kΩ while Req is typically 600Ω for the DS0026. Graphical solutions for P_{DC} appear in *Figure 1.* For example if V^+ = +5V, V^- = −12V, Req = 500 Ω, and DC = 25%, then P_{DC} = 145 mW. However, if the duty cycle was only 5%, P_{DC} = 29 mW. Thus to maximize the number of registers that can be driven by a given clock driver as well as minimizing average system power, the minimum allowable clock pulse width should be used for the particular type of MOS register.

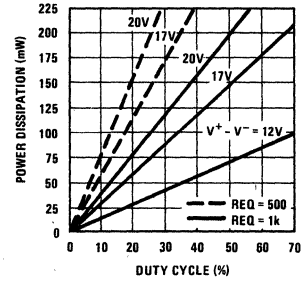


FIGURE 1. P_{DC} vs Duty Cycle

In addition to P_{DC}, the power driving a capacitive load is given approximately by:

$$P_{AC} = (V^+ - V^-)^2 \times f \times C_L \qquad (4)$$

where:

f = Operating frequency

C_L = Load capacitance

Graphical solutions for P_{AC} are illustrated in *Figure 2.* Thus, any type of clock driver will dissipate internally 290 mW per MHz per thousand pF of load. At 5 MHz, this would be 1.5W for a 1000 pF load. For long shift register applications, the driver with the highest package power rating will drive the largest number of bits.

Combining equations (1), (2), (3) and (4) yields a criterion for the maximum load capacitance which can be driven by a given driver:

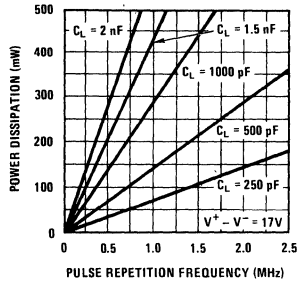


FIGURE 2. P_{AC} vs PRF

$$C_L \leq \frac{1}{f}\left[\frac{P_{MAX}}{n\,(V^+ - V^-)^2} - \frac{(DC)}{Req}\right] \qquad (5)$$

As an example, the DS0025CN can dissipate 890 mW at T_A = 70°C when soldered to a printed circuit board. Req is approximately equal to 1k. For V^+ = 5V, V^- = −12V, f = 1 MHz, and dc = 20%, C_L is:

$$C_L \leq \frac{1}{10^6}\left[\frac{(890 \times 10^{-3})}{(2)\,(17)^2} - \frac{0.2}{1 \times 10^3}\right]$$

$$C_L \leq 1340 \text{ pF (each driver)}$$

A typical application might involve driving an MM5013 triple 64-bit shift register with the DS0025. Using the conditions above and the clock line capacitance of the MM5013 of 60 pF, a single DS0025 can drive 1340 pF/60pF, or 22 MM5013's.

In summary, the maximum capacitive load that any clock driver can drive is determined by package type and rating, heat sink technique, maximum system ambient temperature, ac power (which depends on frequency, voltage across the device, and capacitive load) and dc power (which is principally determined by duty cycle).

Rise and Fall Time Considerations

In general rise and fall times are determined by (a) clock driver design, (b) reflected effects of heavy external load, and (C) peak transient current available. Details of these are included in Appendixes I and II. *Figures AI-3, AI-4, AII-2 and AIII-3* illustrate performance under various operating conditions. Under light loads, performance is determined by internal design of the driver; for moderate loads, by load C_L being reflected (usually as $C_{L/\beta}$) into the driver, and for large loads by peak output current where:

$$\frac{\Delta V}{\Delta T} = \frac{I_{OUT\ PEAK}}{C_L}$$

Logic rise and fall times must be known in order to assure non-overlap of system timing.

Note the definition of rise and fall times in this application note follow the convention that rise time is the transition from logic "0" to logic "1" levels and vice versa for fall times. Since MOS logic is inverted from normal TTL, "rise time" as used in this note is "voltage fall" and "fall time" is "voltage rise."

Power Supply Decoupling

Although power supply decoupling is a wide spread and accepted practice, the question often arises as to how much and how often. Our own experience indicates that each clock driver should have at least 0.1μF decoupling to ground at the V^+ and V^- supply leads. Capacitors should be located as close as is physically possible to each driver. Capacitors should be non-inductive ceramic discs. This decoupling is necessary because currents in the order of 0.5 to 1.5 amperes flow during logic transitions.

There is a high current transient (as high as 1.5A) during the output transition from high to low through the V^- lead. If the external interconnecting wire from the driving circuit to the V^- lead is electrically long, or has significant dc resistance the current transient will appear as negative feedback and subtract from the switching response. To minimize this effect, short interconnecting wires are necessary and high frequency power supply decoupling capacitors are required if V^- is different from the ground of the driving circuit.

Clock Line Overshoot and Cross Talk

Overshoot: The output waveform of a clock driver can, and often does, overshoot. It is particularly evident on faster drivers. The overshoot is due to the finite inductance of the clock lines. Since most MOS registers require that clock signals not exceed V_{SS}, some method must be found in large systems to eliminate overshoot. A straightforward approach is shown in *Figure 3.* In this instance,

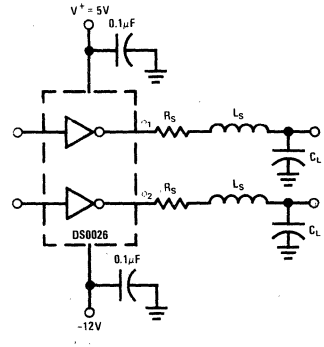


FIGURE 3. Use of Damping Resistor to Eliminate Clock Overshoot

a small damping resistor is inserted between the output of the clock driver and the load. The critical value for R_S is given by:

$$R_S = 2\sqrt{\frac{L_S}{C_L}} \qquad (6)$$

In practice, analytical determination of the value for R_S is rather difficult. However, R_S is readily determined empirically, and typical values range in value between 10 and 50Ω.

Use of the damping resistor has the added benefit of essentially unloading the clock driver; hence a greater number of loads may often be driven by a given driver. In the limit, however, the maximum value that may be used for R_S will be determined by the maximum allowable rise and fall time needed to assure proper operation of the MOS register. In short:

$$t_{r(MAX)} = t_{f(MAX)} \leq 2.2\, R_S\, C_L \qquad (7)$$

One last word of caution with regard to use of a damping resistor should be mentioned. The power dissipated in R_S can approach $(V^+ - V^-)^2 f C_L$ and accordingly the resistor wattage rating may be in excess of 1W. There are, obviously, applications where degradation of t_r and t_f by use of damping resistors cannot be tolerated. *Figure 4* shows a practical circuit which will limit overshoot to a diode drop. The clamp network should physically be located in the center of the distributed load in order to minimize inductance between the clamp and registers.

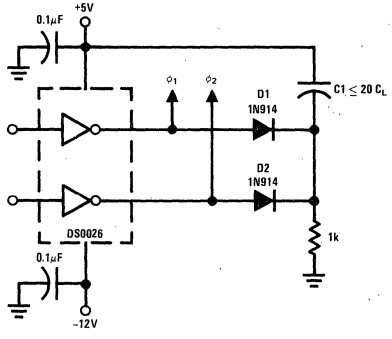


FIGURE 4. Use of High Speed Clamp to Limit Clock Overshoot

Cross Talk: Voltage spikes from ϕ_1 may be transmitted to ϕ_2 (and vice versa) during the transition of ϕ_1 to MOS logic "1." The spike is due to mutual capacitance between clock lines and is, in general, aggravated by long clock lines when numerous registers are being driven. *Figure 5* illustrates the problem.

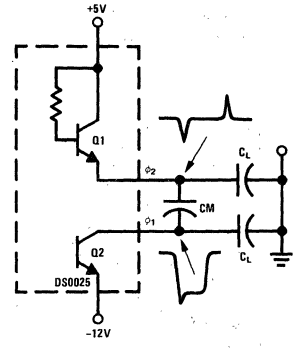


FIGURE 5. Clock Line Cross Talk

The negative going transition of ϕ_1 (to MOS logic "1") is capacitively coupled via C_M to ϕ_2. Obviously, the larger C_M is, the larger the spike. Prior to ϕ_1's transition, Q1 is "OFF" since only μA are drawn from the device.

The DS0056 connected as shown in *Figure 6* will minimize the effect of cross talk. The external resistors to the higher power supply pull the base of a Q1 up to a higher level and forward bias the collector base junction of Q1. In this bias condition the output impedance of the DS0056 is very low and will reduce the amplitude of the spikes.

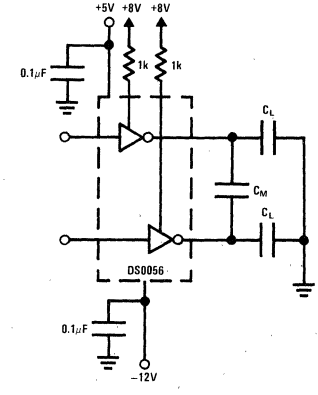


FIGURE 6. Use of DS0056 to Minimize Clock Line Cross Talk

Input Capacitive Coupling

Generally, MOS shift registers are powered from +5V and −12V supplies. A level shift from the TTL levels (+5V) to MOS levels (−12V) is therefore required. The level shift could be made utilizing a PNP transistor or zener diode. The disadvantage to dc level shifting is the increased power dissipation and propagation delay in the level shifting device. Both the DS0025, DS0026 and DS0056 utilize input capacitors when level shifting from

TTL to negative MOS capacitors. Not only do the capacitors perform the level shift function without inherent delay and power dissipation, but as will be shown later, the capacitors also enhance the performance of these circuits.

CONCLUSION

The practical aspects of driving MOS memories with low cost clock drivers has been discussed in detail. When the design guide lines set forth in this paper are followed and reasonable care is taken in circuit layout, the DS0025, DS0026 and DS0056 provide superior performance for most MOS input interface applications.

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6. Richard Percival, *"Dynamic MOS Shift Registers Can Also Simulate Stack and Silo Memories,"* Electronics Magazine, November 8, 1971.
7. Bapat and Mrazek, *"Dynamic MOS Random Access Memory System Considerations,"* National Semiconductor, AN-50, August 1971.
8. Don Femling, *"Using the MM5704 Keyboard Interface in Keyboard Systems,"* National Semiconductor, AN-52.

APPENDIX I

DS0025 Circuit Operation

The schematic diagram of the DS0025 is shown in *Figure AI-1.* With the TTL driver in the logic "0" state Q1 is "OFF" and Q2 is "ON" and the output is at approximately one V_{BE} below the V^+ supply.

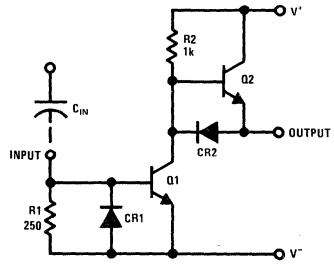


FIGURE AI-1. DS0026 Schematic (One-Half Circuit)

When the output of the TTL driver goes high, current is supplied to the base of Q1, through C_{IN}, turning it "ON." As the collector of Q1 goes negative, Q2 turns "OFF." Diode CR2 assures turn-on of Q1 prior to Q2's turn-off minimizing current spiking on the V^+ line, as well as providing a low impedance path around Q2's base emitter junction.

The negative voltage transition (to MOS logic "1") will be quite linear since the capacitive load will force Q1 into its linear region until the load is discharged and Q1 saturates. Turn-off begins when the input current decays to zero or the output of the TTL driver goes low. Q1 turns "OFF" and Q2 turns "ON" charging the load to within a V_{BE} of the V^+ supply.

Rise Time Considerations

The logic rise time (voltage fall) of the DS0025 is primarily a function of the ac load, C_L, the available input current and total voltage swing. As shown in *Figure AI-2,*

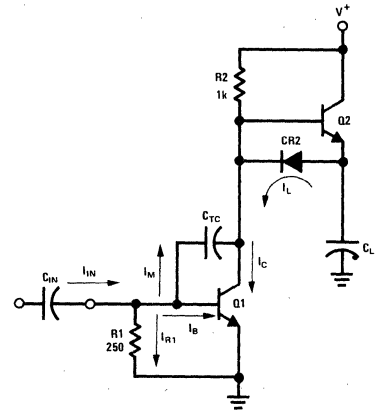


FIGURE AI-2. Rise Time Model for the DS0025

the input current must charge the Miller capacitance of Q1, C_{TC}, as well as supply sufficient base drive to Q1 to discharge C_L rapidly. By inspection:

$$I_{IN} = I_M + I_B + I_{R1} \qquad \text{(AI-1)}$$

$$I_{IN} \cong I_M + I_B, \text{ for } I_M \gg I_{R1} \;\&\; I_B \gg I_{R1}$$

$$I_B = I_{IN} - C_{TC}\frac{\Delta V}{\Delta t} \qquad \text{(AI-2)}$$

If the current through R2 is ignored,

$$I_C = I_B h_{FEQ1} = I_L + I_M \qquad \text{(AI-3)}$$

where:

$$I_L = C_L \frac{\Delta V}{\Delta t}$$

Combining equations AI-1, AI-2, AI-3 yields:

$$\frac{\Delta V}{\Delta t}[C_L + C_{TC}(h_{FEQ1} + 1)] = h_{FEQ1} I_{IN} \qquad \text{(AI-4)}$$

or

$$t_r \cong \frac{[C_L + (h_{FEQ1} + 1)C_{TC}]\,\Delta V}{h_{FEQ1} I_{IN}} \qquad \text{(AI-5)}$$

Equation (AI-5) may be used to predict t_r as a function of C_L and ΔV. Values for C_{TC} and h_{FE} are 10 pF and 25 respectively. For example, if a DM7440 with peak output current of 50 mA were used to drive a DS0025 loaded with 1000 pF, rise times of:

$$\frac{(1000\text{ pF} + 250\text{ pF})\,(17\text{V})}{(50\text{ mA})\,(20)}$$

or 21 ns may be expected for $V^+ = 5.0$V, $V^- = -12$V, *Figure AI-3* gives rise time for various values of C_L.

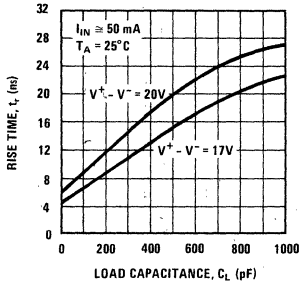


FIGURE AI-3. Rise Time vs C_L for the DS0025

Fall Time Considerations

The MOS logic fall time (voltage rise) of the DS0025 is dictated by the load, C_L, and the output capacitance of Q1. The fall time equivalent circuit of DS0025 may be approximated with the circuit of *Figure AI-4.* In actual

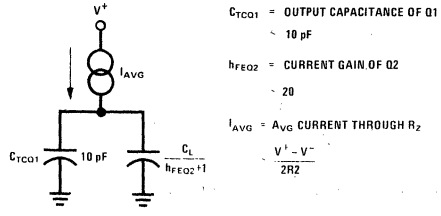


FIGURE AI-4. Fall Time Equivalent Circuit

practice, the base drive to Q2 drops as the output voltage rises toward V^+. A rounding of the waveform occurs as the output voltage reaches to within a volt of V^+. The result is that equation (AI-7) predicts conservative values of t_f for the output voltage at the beginning of the voltage rise and optimistic values at the end. *Figure AI-5* shows t_f as function of C_L.

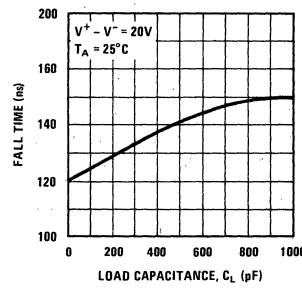


FIGURE AI-5. DS0025 Fall Time vs C_L

Assuming h_{FE2} is a constant of the total transition:

$$\frac{\Delta V}{\Delta t} = \frac{\left(\frac{V^+ - V^-}{2R2}\right)}{C_{TCQ1} + C_L/h_{FEQ1+1}} \qquad \text{(AI-6)}$$

or

$$t_f \cong 2R2\left(C_{TCQ1} + \frac{C_L}{h_{FEQ+1}}\right) \qquad \text{(AI-7)}$$

DS0025 Input Drive Requirements

Since the DS0025 is generally capacitively coupled at the input, the device is sensitive to current not input voltage. The current required by the input is in the 50–60 mA region. It is therefore a good idea to drive the DS0025 from TTL line drivers, such as the DM7440 or DM8830. It is possible to drive the DS0025 from standard 54/74 series gates or flip-flops but t_{ON} and t_r will be somewhat degraded.

Input Capacitor Selection

The DS0025 may be operated in either the logically controlled mode (pulse width out ≅ pulse width in) or C_{IN} may be used to set the output pulse width. In the latter mode a long pulse is supplied to the DS0025.

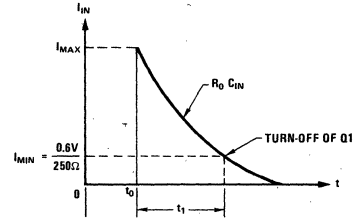


FIGURE AI-6. DS0025 Input Current Waveform

The input current is of the general shape as shown in *Figure AI-6*. I_{MAX} is the peak current delivered by the TTL driver into a short circuit (typically 50–60 mA). Q1 will begin to turn-off when I_{IN} decays below V_{BE}/R1 or about 2.5 mA. In general:

$$I_{IN} = I_{MAX}\, e^{-t/R0}\, C_{IN} \qquad \text{(AI-8)}$$

where:

R0 = Output impedance of the TTL driver

C_{IN} = Input coupling capacitor

Substituting $I_{IN} = I_{MIN} = \frac{V_{BE}}{R1}$ and solving for t_1 yields:

$$t_1 = R0C_{IN}\ \ln\ \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AI-9)}$$

The total pulse width must include rise and fall time considerations. Therefore, the total expression for pulse width becomes:

$$t_{PW} \cong \frac{t_r + t_f}{2} + t_1$$

$$= \frac{t_r + t_f}{2} + R0C_{IN}\ln\ \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AI-10)}$$

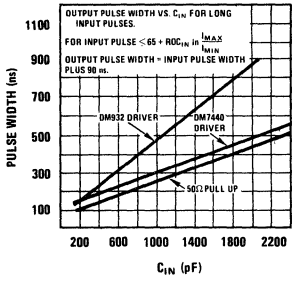


FIGURE AI-7. Output PW Controlled by C_{IN}

The logic "1" output impedance of the DM7440 is approximately 65Ω and the peak current (I_{MAX}) is about 50 mA. The pulse width for C_{IN} = 2,200 pF is:

$$t_{PW} \cong \frac{25\text{ ns} + 150\text{ ns}}{2} + (65\Omega)(2200\text{ pF})\ \ln$$

$$\frac{50\text{ mA}}{2.5\text{ mA}} = 517\text{ ns}$$

A plot of pulse width for various types of drivers is shown in *Figure AI-7*. For applications in which the output pulse width is logically controlled, C_{IN} should be chosen 2 to 3 times larger than the maximum pulse width dictated by equation (AI-10).

DC Coupled Operation

The DS0025 may be direct-coupled in applications when level shifting to a positive value only. For example, the MM1103 RAM typically operates between ground and +20V. The DS0025 is shown in *Figure AI-8* driving the addres or precharge line in the logically controlled mode.

If DC operation to a negative level is desired, a level translator such as the DS7800 or DS0034 may be employed as shown in *Figure AI-9*. Finally, the level shift may be accomplished using PNP transistors are shown in *Figure AI-10*.

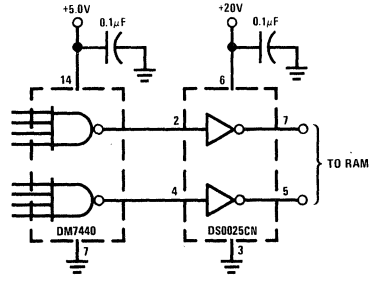


FIGURE AI-8. DC Coupled DS0025 Driving 1103 RAM

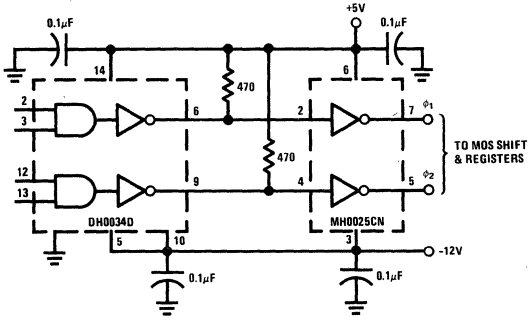


FIGURE AI-9. DC Coupled Clock Driver Using DS0034

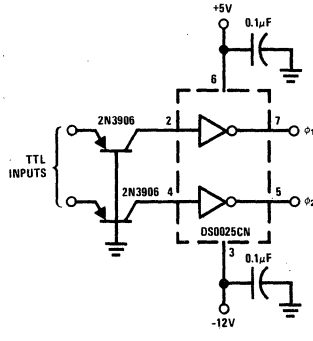


FIGURE AI-10. Transistor Coupled DS0025 Clock Driver

APPENDIX II

DS0026 Circuit Operation

The schematic of the DS0026 is shown in *Figure AII-1*. The device is typically ac coupled on the input and responds to input current as does the DS0025. Internal current gain allows the device to be driven by standard TTL gates and flip-flops.

With the TTL input in the low state Q1, Q2, Q5, Q6 and Q7 are "OFF" allowing Q3 and Q4 to come "ON." R6 assures that the output will pull up to within a V_{BE} of V^+ volts. When the TTL input starts toward logic "1," current is supplied via C_{IN} to the bases of Q1 and Q2 turning them "ON." Simultaneously, Q3 and Q4 are snapped "OFF." As the input voltage rises (to about 1.2V), Q5 and Q6 turn-on. Multiple emitter transistor Q5 provides additional base drive to Q1 and Q2 assuring their complete and rapid turn-on. Since Q3 and Q4 were rapidly turned "OFF" minimal power supply current spiking will occur when Q7 comes "ON."

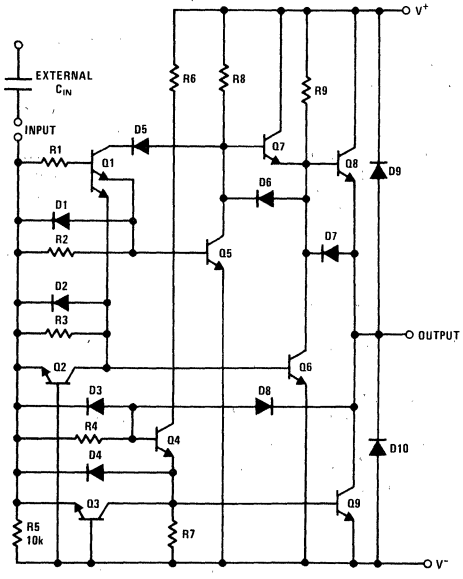


FIGURE AII-1. DS0025 Schematic (One-Half Circuit)

Q6 now provides sufficient base drive to Q7 to turn it "ON." The load capacitance is then rapidly discharged toward V^-. Diode D4 affords a low impedance path to Q6's collector which provides additional drive to the load through current gain of Q7. Diodes D1 and D2 prevent avalanching Q3's and Q4's base-emitter junction as the collectors of Q1 and Q2 go negative. The output of the DS0026 continues negative stopping about 0.5V more positive than V^-.

When the TTL input returns to logic "0," the input voltage to the DS0026 goes negative by an amount proportional to the charge on C_{IN}. Transistors Q8 and Q9 turn-on, pulling stored base charge out of Q7 and Q2 assuring their rapid turn-off. With Q1, Q2, Q6 and Q7 "OFF," Darlington connected Q3 and Q4 turn-on and rapidly charge the load to within a V_{BE} of V^+.

Rise Time Considerations

Predicting the MOS logic rise time (voltage fall) of the DS0026 is considerably involved, but a reasonable approximation may be made by utilizing equation (AI-5), which reduces to:

$$t_r \cong [C_L + 250 \times 10^{-12}]\ \Delta V \qquad \text{(AII-1)}$$

For C_L = 1000 pF, V^+ = 5.0V, V^- = −12V, $t_r \cong$ 21 ns. *Figure AII-2* shows DS0026 rise times vs C_L.

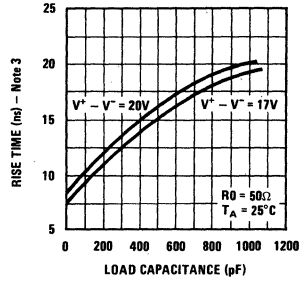


FIGURE AII-2. Rise Time vs Load Capacitance

Fall Time Considerations

The MOS logic fall time of the DS0026 is determined primarily by the capacitance Miller capacitance of Q5 and Q1 and R5. The fall time may be predicted by:

$$t_f \cong (2.2)(R5)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right) \cong (4.4 \times 10^3)\left(C_S + \frac{C_L}{h_{FE}{}^2}\right) \qquad \text{(AII-2)}$$

where:

C_S = Capacitance to ground seen at the base of Q3

= 2 pF

$h_{FE}{}^2 = (h_{FEQ3} + 1)\ (h_{FEQ4} + 1)$

$\cong$ 500

For the values given and C_L = 1000 pF, $t_f \cong$ 17.5 ns. *Figure AII-3* gives t_f for various values of C_L.

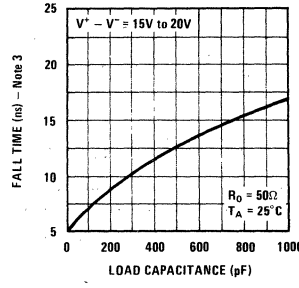


FIGURE AII-3. Fall Time vs Load Capacitance

DS0026 Input Drive Requirements

The DS0026 was designed to be driven by standard 54/74 elements. The device's input characteristics are shown in *Figure AII-4*. There is breakpoint at $V_{IN} \cong 0.6V$ which corresponds to turn-on of Q1 and Q2. The input current then rises with a slope of about 600Ω (R2 || R3) until a second breakpoint at approximately 1.2V is encountered, corresponding to the turn-on of Q5 and Q6. The slope at this point is about 150Ω (R1 || R2 || R3 || R4).

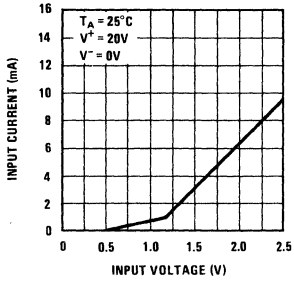


FIGURE AII-4. Input Current vs Input Voltage

The current demanded by the input is in the 5–10 mA region. A standard 54/74 gate can source currents in excess of 20 mA into 1.2V. Obviously, the minimum "1" output voltage of 2.5V under these conditions cannot be maintained. This means that a 54/74 element must be dedicated to driving 1/2 of a DS0026. As far as the DS0026 is concerned, the current is the determining turn-on mechanism not the voltage output level of the 54/74 gate.

Input Capacitor Selection

A major difference between the DS0025 and DS0026 is that the DS0026 requires that the output pulse width be logically controlled. In short, the input pulse width ≅ output pulse width. Selection of C_{IN} boils down to choosing a capacitor small enough to assure the capacitor takes on nearly full charge, but large enough so that the input current does not drop below a minimum level to keep the DS0026 "ON." As before:

$$t_1 = R0C_{IN} \ln \frac{I_{MAX}}{I_{MIN}} \qquad \text{(AII-3)}$$

or

$$C_{IN} = \frac{t_1}{R0 \ln \frac{I_{MAX}}{I_{MIN}}} \qquad \text{(AII-4)}$$

In this case R0 equals the sum of the TTL gate output impedance plus the input impedance of the DS0026 (about 150Ω). I_{MIN} from *Figure AII-5* is about 1 mA. A standard 54/74 series gate has a high state output impedance of about 150Ω in the logic "1" state and an output (short circuit) current of about 20 mA into 1.2V. For an output pulse width of 500 ns,

$$C_{IN} = \frac{500 \times 10^{-9}}{(150\Omega + 150\Omega) \ln \frac{20\text{ mA}}{1\text{ mA}}} = 560\text{ pF}$$

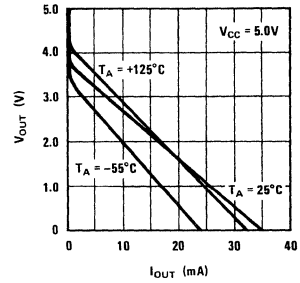


FIGURE AII-5. Logical "1" Output Voltage vs Source Current

In actual practice it's a good idea to use values of about twice those predicted by equation (AII-4) in order to account for manufacturing tolerances in the gate, DS0026 and temperature variations.

A plot of optimum value for C_{IN} vs desired output pulse width is shown in *Figure AII-6*.

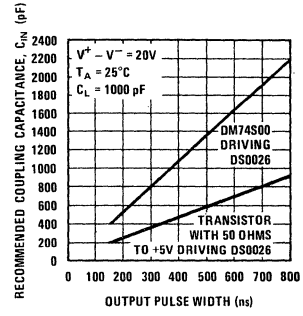


FIGURE AII-6. Suggested Input Capacitance vs Output Pulse Width

DC Coupled Applications

The DS0026 may be applied in direct coupled applications. *Figure AII-7* shows the device driving address or pre-charge lines on an MM1103 RAM.

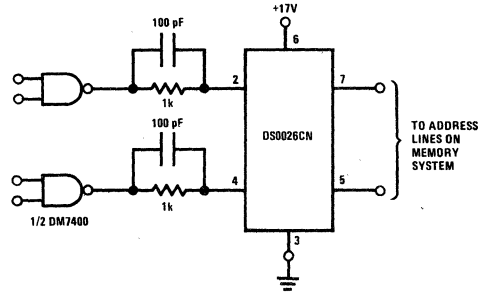


FIGURE AII-7. DC Coupled RAM Memory Address or Precharge Driver (Positive Supply Only)

For applications requiring a dc level shift, the circuit of *Figure AII-8 or AII-9* are recommended.

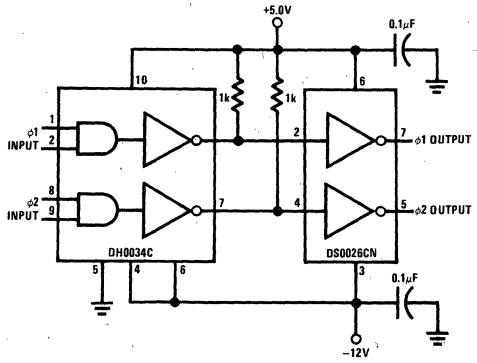


FIGURE AII-8. Transistor Coupled MOS Clock Driver

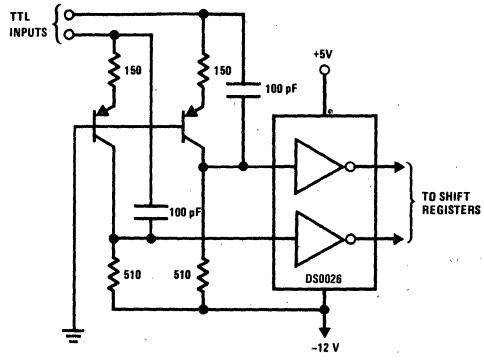


FIGURE AII-9. DC Coupled MOS Clock Driver

APPENDIX III

MOS Interface Circuits

MOS Clock Drivers

MH0007	Direct coupled, single phase, TTL compatible clock driver.
MH0009	Two phase, direct or ac coupled clock driver.
MH0012	10 MHz, single phase direct coupled clock driver.
MH0013	Two phase, ac coupled clock driver.
DS0025	Low cost, two phase clock driver.
DS0026	Low cost, two phase, high speed clock driver.
DS1671	Dual bootstrapped MOS driver.
DS1672	Dual TTL bootstrapped MOS driver.
DS1673	Quad decoded MOS clock driver.
DS1674	Quad MOS clock driver.
DS75361	Dual TTL-to-MOS driver.
DS75365	Quad TTL-to-MOS driver.

MOS Oscillator/Clock Drivers

DS7803/DS7807, DS7813/DS7817	Complete two phase clock system for MOS microprocessors and calculators.

MOS RAM Memory Address and Precharge Drivers

DS0025	Dual address and precharge driver.
DS0026	Dual high speed address and precharge driver.

TTL to MOS Interface

DH0034	Dual high speed TTL to negative level converter.
DS7800	Dual TTL to negative level converter.
DS7810/DS7812/ DS7819	Open collector TTL to positive high level MOS converter gates.
DS78L12	Active pull-up TTL to positive high level MOS converter gates.
DS1640/DS1670	Quad MOS TRI-SHARE™ driver.
DS1645/DS1675	Hex TRI-STATE® MOS driver.
DS1646/DS1676	6-bit TRI-STATE MOS driver refresh counter.
DS1647/DS1677	Quad TRI-STATE MOS driver I/O register.
DS1648/DS1678	TRI-STATE MOS driver multiplexer.
DS1649/DS1679	Hex TRI-STATE MOS driver.
DS16149/DS16179	Hex TRI-STATE MOS driver.

MOS to TTL Converters and Sense Amps

DS7802, DS7806*	Dual sense amp for MM5262 2k MOS RAM memory.
DS165 Series*	Hex sense amp MOS to TTL.
DS163, DS75107, DS75207*	Dual sense amp for MM1103 1k MOS RAM memory.

Voltage Regulators for MOS Systems

LM109, LM140 Series	Positive regulators.
LM120 Series	Negative regulators.
LM125 Series*	Dual +/— regulators.

*To be announced

NATIONAL

Applications

DATA BUS AND DIFFERENTIAL LINE DRIVERS AND RECEIVERS

INTRODUCTION

Monolithic circuits designed specifically to transmit and receive digital data via buses and differential cables have been available for two or three years. But important changes in transmission concepts and IC designs have been made recently. This note will bring designers up to data on circuits developed at National Semiconductor. Table I and Figure 1 outline the devices to be discussed.

In general, the new bus circuits offer these advances: self-isolation of powered-down receivers; much lower input currents, permitting more driver/receivers pairs per bus line; input hysteresis to raise noise immunity; higher speed with better control of bus levels; and eliminating of terminating pull-up resistors by the TRI-STATE® designs.

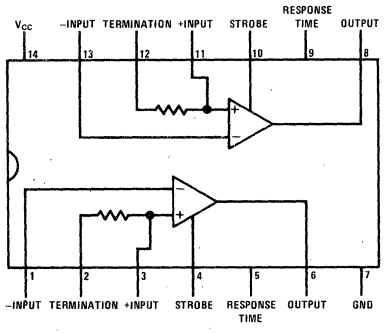
The DS7820/DS8820 and DS7830/DS8830 were described in Application Note AN-22. This note adds to the previous discussion of termination techniques and reports on new tests of their long-lines drive capability and crosstalk immunity.

TABLE I. Table of Devices Discussed

LINE DRIVERS DEVICE NO.	LINE RECEIVERS DEVICE NO.	DESCRIPTION	POWER SUPPLY	COMMENTS
DS1488	DS1489/DS1489A	Communication to EIA standard RS 232C.	±12V DS1489A +5.0V	Twisted pair single ended. Unidirectional.
DS7830/DS8830	DS7820A/DS8820A	Dual differential line driver and receiver.	+5.0V	True differential. ±15V common mode rejection. Unidirectional. Use of internal receiver termination recommended up to 100 feet.
DS7831/DS8831	DS7820A/DS8820A	Dual differential line driver and receiver.	+5.0V	True differential, bidirectional. Driver includes upper and lower level clamps to combat transients. Use of internal receiver termination optional.
DS7832/DS8832	DS7820A/DS8820A	Dual differential line driver and receiver.	+5.0V	As above, but without upper level clamping, so party line busses may be used, even with some peripherals powered down.
DS7831/DS8831	DS7837/DS8837 (hex) or DS7836/ DS8836 (quad)	Quad single-ended line driver and hex receiver, or a quad 2 input NOR receiver.	+5.0V	If used unidirectionally, receiver should be terminated. In party line applications disabled driver clamps line. Receiver input current is 15μA typical, has 1.0V hysteresis.

TRANSCEIVER DEVICE NO.	DESCRIPTION	POWER SUPPLY	COMMENTS
DS7838/DS8838	Quad open collector transceiver.	+5.0V	Receiver has typical 15μA input current 1.0V hysteresis. Driver will pull down double terminated 120Ω line.
DS7839/DS8839	Quad TRI-STATE® transceiver. Four transmitters all disabled by control NOR gate.	+5.0V	Drivers have 10.4 mA forward drive at 2.4V, sink 32 mA at 0.4V. Receivers have 1.0V hysteresis, input current is 15μA typical. Disabled driver clamps undershoots. A transceiver on the bus may be powered down without affecting bus logic levels.
DS7833/DS8833	Quad TRI-STATE transceiver. One control disables all transmitters; one control disables all receiver outputs.	+5.0V	
DS7834/DS8834	Quad TRI-STATE transceiver. Controls same as DM7839 but driver and receiver are inverting.	+5.0V	
DS7835/DS8835	Quad TRI-STATE transceiver. Controls same as DM7833 but driver and receiver are inverting.	+5.0V	

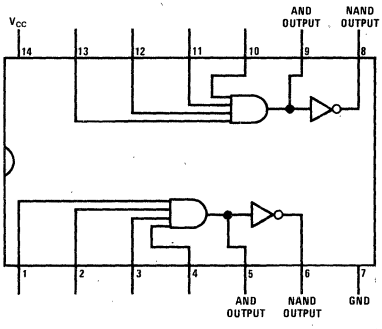
DS7820/DS8820, DS7820A/DS8820A



NOTE: PIN 7 CONNECTED TO BOTTOM OF CAVITY PACKAGE.

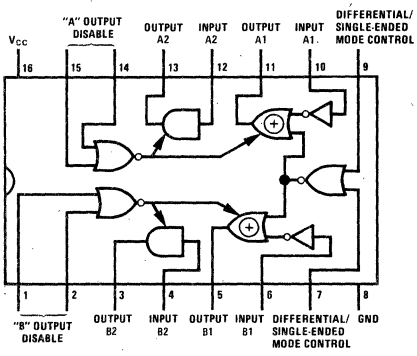
TOP VIEW

DS7830/DS8830



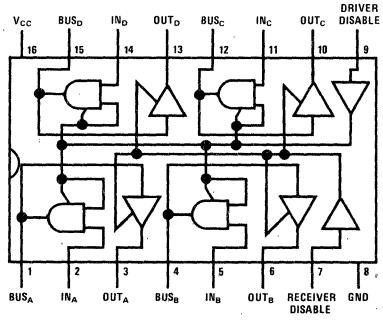
TOP VIEW

DS7831/DS8831, DS7832/DS8832



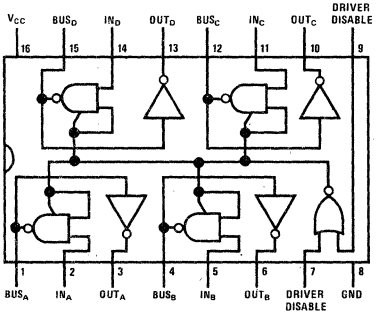
TOP VIEW

DS7833/DS8833



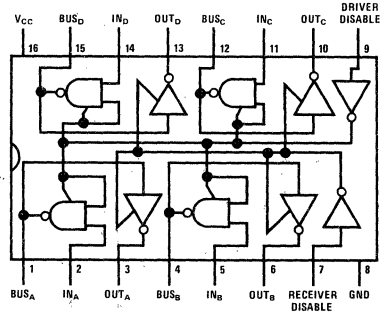
TOP VIEW

DS7834/DS8834



TOP VIEW

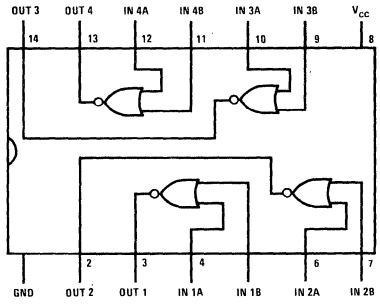
DS7835/DS8835



TOP VIEW

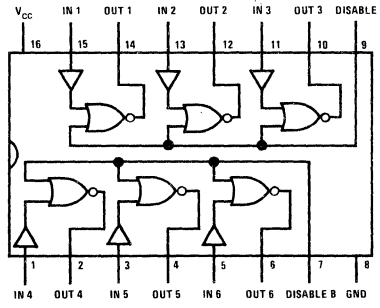
FIGURE 1.

DS7836/DS8836



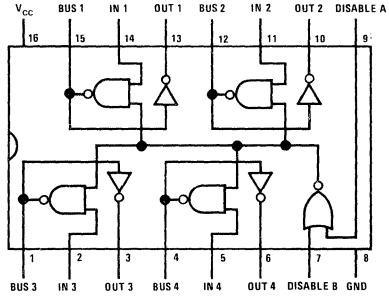
TOP VIEW

DS7837/DS8837



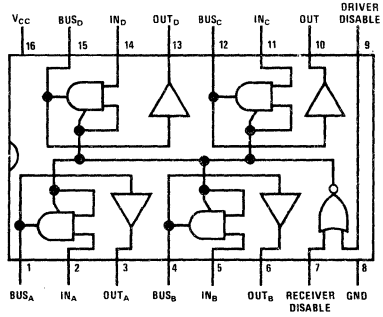
TOP VIEW

DS7838/DS8838



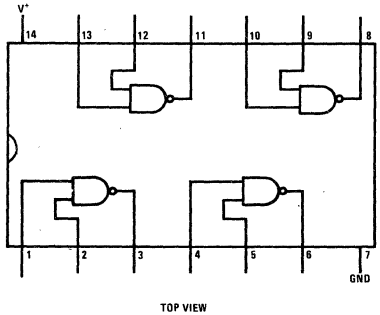
TOP VIEW

DS7839/DS8839



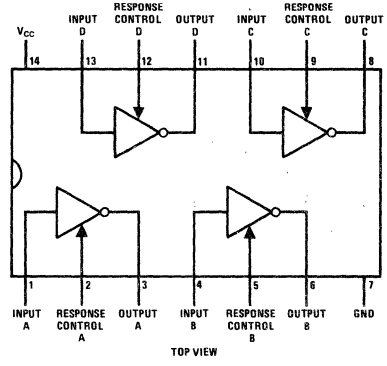
TOP VIEW

DS1488



TOP VIEW

DS1489/DS1489A



TOP VIEW

FIGURE 1. (Con't)

Not much need be said about the EIA RS232C designs. They meet or exceed a standard which is below today's attainable performance levels.

UNIFIED BUS

A typical unified bus is a flat, multiconductor cable interconnecting the CPU and peripherals of a minicomputer (Figure 2). The lines are single-ended (non-differential), ground-referenced, bi-directional, and terminated at each end in 120Ω to 3.2V. The line level is high except when an open-collector driver pulls the line low. Drivers take turns transmitting, as controlled by "polling" or other control sequences.

Single-ended communications are susceptible to common mode voltage induced by ground currents between chassis. In a computer room, the problem is usually minimized by linking the chassis with heavy-gauge grounding cables. Communications with remote points go through differential transmission links, or modems coupled to phone lines.

In early unified bus designs, open-collector TTL buffers were used as drivers, and standard gates as receivers. However, the low threshold voltage of the receiving gate (it can be as low as 1.0V) is too close to ground potential, which can itself be carrying transients of almost a volt. In addition, the gate's input current can be as high as 1.6 mA, severely limiting the number of receivers which can be controlled by one driver. This is true particularly if the driver has an open collector output, and must also be sinking the current from a 120Ω termination at each end of the unified bus.

That problem was solved by the SP380 gate. Its signal input is the base of an NPN emitter-follower, giving a higher threshold and lower input current. Unfortunately, the input transistor's collector-base junction becomes forward-biased when V_{CC} goes down. If a peripheral is shut off, the bus lines are clamped near ground unless the bus cable is disconnected manually.

The new unified bus designs in Table I have a receiver that is self-isolating when power is down. The main bus is still usable if peripherals are turned off.

Other improvements include: very low input current, typically 15μA whether V_{CC} is 5.0V or zero; input hysteresis of 1.0V, providing 1.8V noise immunity; thresholds of 1.3V and 2.3V; and temperature compensation to keep thresholds and noise immunity constant.

The DS7836/DS8836 is pin-compatible with the SP380 and adds the advantages of hystersis. The DS8640 is an exact replacement for the SP380. Each receiver trio in the DS7837/DS8837 has an enable control, so the system can force receiver outputs to zero whether the bus is pulled down or not. The four drivers in the DS7838/DS8838 transceiver are disabled by a NOR gate control.

Each open-collector driver in the transceiver sinks 50 mA at 0.7V. It has the power to pull down the double-terminated bus and drive 20 of the low-current receivers.

TRI-STATE BUS

TRI-STATE logic (or TSL) outputs are active in both the "1" and "0" state. This greatly improves risetimes and allows many more driver/receiver pairs to be connected to a bus since power is not wasted in terminations. Switching delays can be halved during certain data exchanges.

A disabled output switches into a third, high-impedance state. Only small leakage currents flow in the output in this state, virtually disconnecting the output from the bus. TSL outputs do not "wire-OR" – the bus is operated by one set of outputs at a time.

Figure 3 is a TSL bus line. Although there are no terminations, reflections are less of a problem than in a unified bus. The bus is tightly controlled without terminations because the disabled drivers actually clamp undershoots.

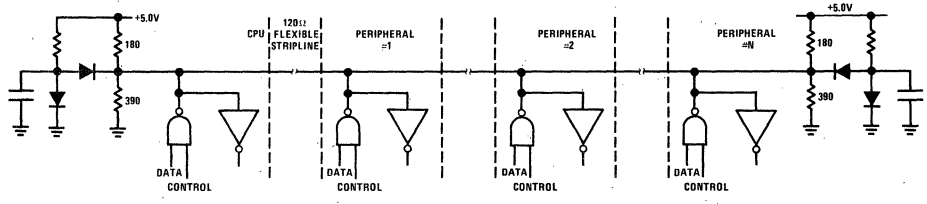


FIGURE 2. Unified Open Collector Bus

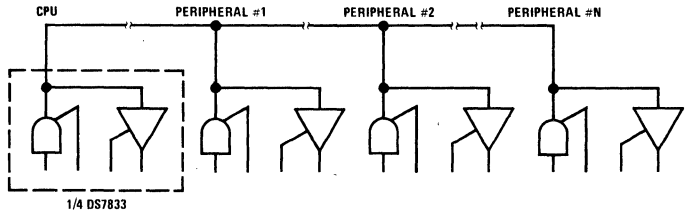


FIGURE 3. TRI-STATE Bus

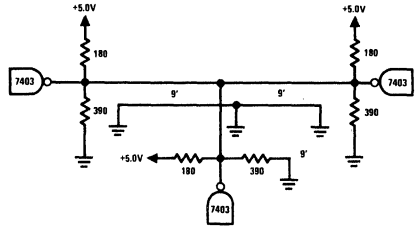


FIGURE 4. Open Collector Line With Stub

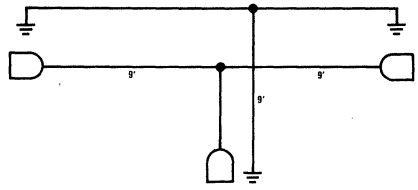


FIGURE 5. TRI-STATE Line With Stub

Tests indicate the transceivers can drive bus lines longer than 25 feet. They are guaranteed to source 10.4 mA at the minimum "one" level of 2.4V. Small-signal source impedance is typically 50Ω to 5.0V compared with 120Ω to 3.2V on the unified bus. That explains TSL's higher speed — the active-pull-up output charges the line capacitance much faster. If even greater source current capability is needed, the DS7831/DS8831 and DS7832/DS8832 are available. As quad single-ended drivers they can source and sink at least 40 mA (and have a source impedance of only 11Ω). They can drive lines with characteristic impedance down to 40Ω.

When a peripheral equipped with a transceiver is powered down or disabled, no current (apart from microamps of leakage) will flow in the input/output while the data levels move between ground and +5.0V. Other peripherals can still use the bus without their signals being shunted or degraded. The receivers are isolated like the unified bus designs. (The DS7832/DS8832 has the same degree of freedom, However, the DS7831/DS8831 has an output diode to V_{CC} to control transients when used in its differential mode. It will clamp the bus lines when powered-down, so it is not recommended for use in a peripheral which might be switched off in isolation from the rest of the system).

In the TSL transceiver family, typical receiver input characteristics are 17μA current, 400 mV hysteresis, and 1.4V noise immunity. All types are completely compatible with standard TTL.

Figure 4 shows a line with a stub (actually a branch of equal length, to ease analysis). It is terminated in the line's characteristic impedance at all three ends.

Figure 5 shows an identical hook-up, this time "terminated" only by a disabled TRI-STATE gate at the receiving end and the stub end.

The result of driving the circuit of Figure 4 is seen in Figure 6. The current pulled from the line by the driver (top trace) was determined by the effective impedance of the termination in parallel with the 120Ω line charged to 3.2V. When this wavefront reached the fork, half the current was drawn from each leg. So when the half-current front arrives at the stub only half the voltage pull-down results (Figure 6 lower trace).

A series of these timed halvings and quarterings produces the bathtub effect shown. The duty cycle distortion experienced by a receiver at the stub termination is obvious. If we take off the stub termination network, the situation gets no better. Figure 7 shows it (time base and sensitivity unchanged). The undershoot in the lower trace is followed by an overshoot which reaches 1.0V above ground: and the stub continues to ring (which isn't surprising since its two ends have terminations in 60Ω and infinity respectively). A receiver at the end of the stub would have to be ignored until the ringing had decayed, and its output had become valid.

Contrast this with Figure 8, demonstrating the results of the TRI-STATE driver of Figure 5. The same rapid falling edge at the receiving end is brought to a halt very sharply, and instead of reflective overshoots, there is a shallow series of level adjustments which never cross the maximum zero level of 0.4V above ground.

How is this achieved?

Figure 9 shows the schematic of the output stage of a TRI-STATE transceiver. Now if the output is disabled, point A is held by the TRI-STATE control at $V_{CE}sat + V_{BE}$, or 1.0V at 25°C.

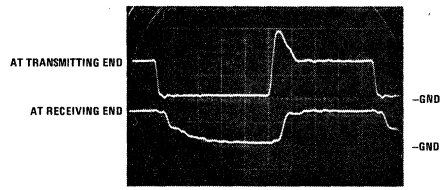


FIGURE 6. Open Collector Bus With Two Terminated Stubs 2.0V/div 20 ns/div

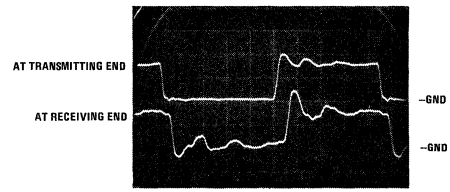


FIGURE 7. Open Collector Bus at an Unterminated Stub

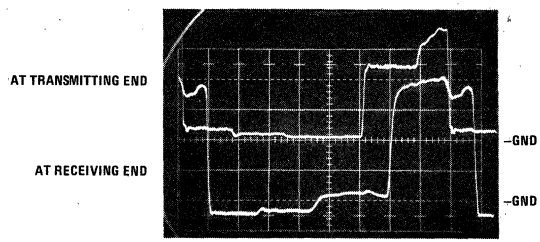


FIGURE 8. TRI-STATE® Bus at a Stub – Demonstration of the TSL Non-Linear Termination

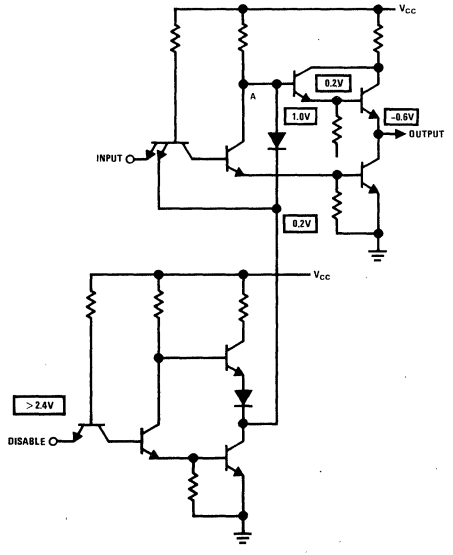


FIGURE 9. DC Levels in a Disabled TRI-STATE Element

So to turn on the Darlington pull-up stage will take an undershoot below ground on the bus line of 2 V_{BE} lower than point A. Or at 25°C, 1.0 − 1.6, = −0.6V. Allowing for a chip temperature somewhat above ambient, the output will begin to clamp at -0.4V. Figure 10 shows a typical result of

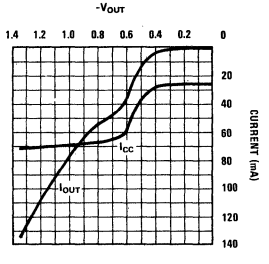


FIGURE 10. Current Available as a Function of Bus Voltage at a Disabled TRI-STATE Output

a test of pulling current out of a disabled TRI-STATE output.

O. A. Horna* has pointed out the effectiveness of a non-linear termination in emitter-coupled logic transmission lines. The ability of the disabled TSL output to turn on very hard in a precisely similar way in an otherwise uncontrollable situation has been conclusively demonstrated.

A further advantage for an unterminated line appears under certain special conditions of architecture. Figures 11 and 12 compare two test circuits, simulating two peripherals one on each

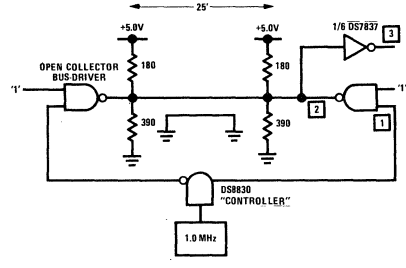


FIGURE 11. Central Controller in an Open Collector Environment

*O. A. Horna – *"Non-Linear Termination of Transmission Lines"* IEEE Transactions on Computers, Sept. 1972, pp. 1011-1-15.

side of a CPU, linked by, in the first case an open collector terminated bus; in the second case a TRI-STATE bus.

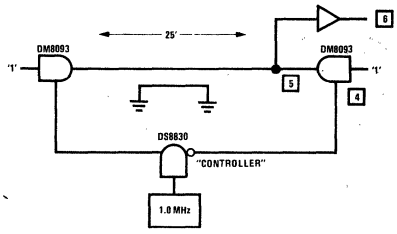


FIGURE 12. Central Controller in a TRI-STATE Environment

In both cases, the bus drivers are holding the bus in one state, and not switching data during the experiment.

Looking at Figure 13, in the open collector case, relinquishment by one driver and immediate taking up by the other at the low state still leaves the termination to pull the bus high for two line delays. And the receiver, waiting for data from the far end, must obviously be ignored until a safe amount of time after the glitch seen in Figure 13 trace 3 has died down. Contrast this with the TRI-STATE case shown in Figure 14. The relinquished bus, seeing only extremely low leakage current, does not move. It may be safely assumed that very shortly after the changeover, a change on the line will be a signal being propagated on the bus.

TRUE DIFFERENTIAL TRANSMISISON

Often, a zero ground reference can't be established between remote subsystems. One can overwhelm the ground difference with a high-amplitude, single-ended transmission. But a differential transmission not referenced to ground is more efficient (Figure 15). The data is complemented at normal logic levels, transmitted over a twisted-pair cable, and received with a comparator sensitive enough to overcome signal degradations, yet rejecting common mode voltages.

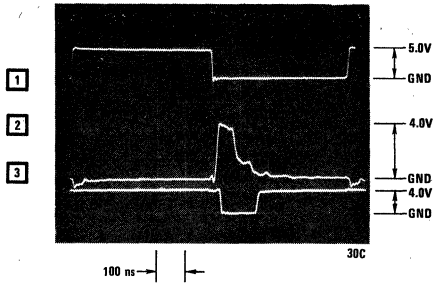


FIGURE 13. Open Collector Bus Signals With Central Controller

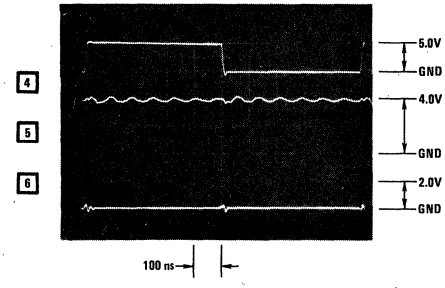


FIGURE 14. TRI-STATE Bus Signals With Central Controller

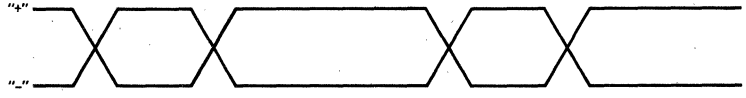


FIGURE 15. Differential Drive – Ideal

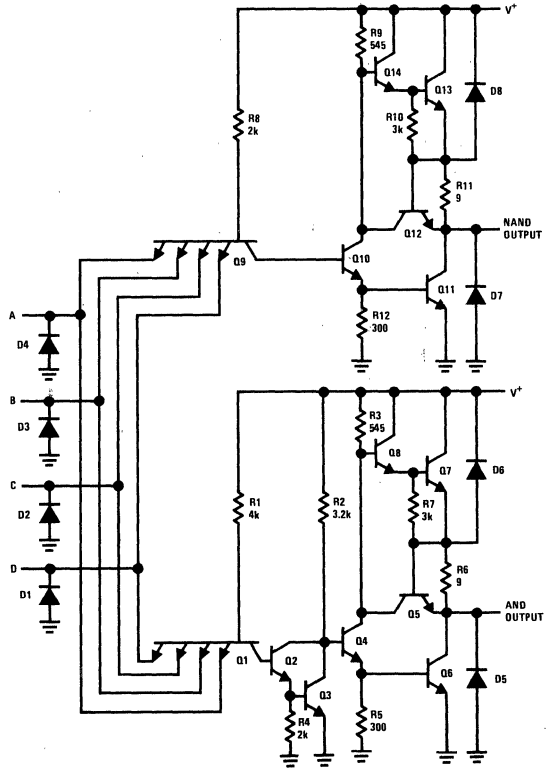


FIGURE 16. DS7830 Schematic

We implemented the differential concept several years ago with the DS7830/DS8830 driver and DS7820/DS8820 receiver. More recently, the two TRI-STATE drivers have been used in such applications. DS7831 output characteristics in the differential driving mode are shown in Figure 17.

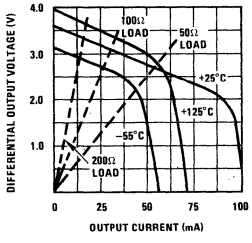
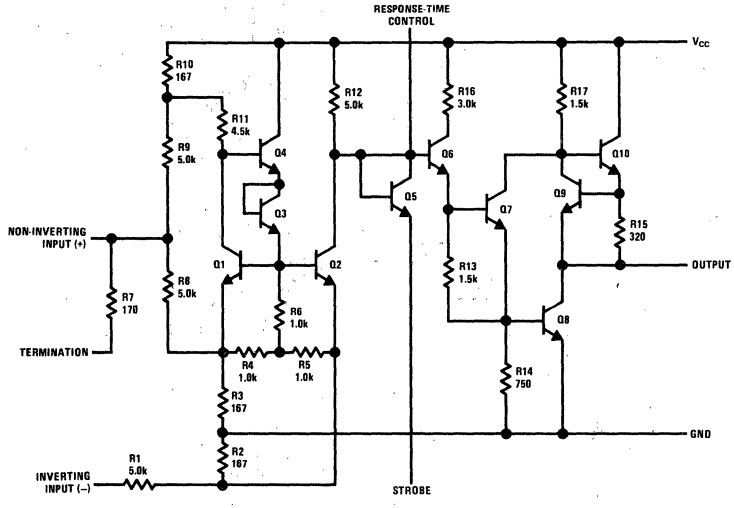


FIGURE 17. Differential Output Voltage as a Function of Differential Output Current in the DS7831

The DS7820 and DS7830 designs were explained in AN-22. Rather than repeat the information in that note, the following sections will answer questions frequently asked by users.

First, how does the new DS7820A differ from the DS7820? They both have the same schematic. One of the two receivers on the chip is shown in Figure 18. However, the "A" version's fanout is 10 TTL or DTL loads rather than 2, the strobe input is specified fully and is guaranteed to be driven by saturated logic, and the speeds are guaranteed.

Second, what establishes the driver current requirement? The receiver's non-inverting input is at the center of a voltage divider between V_{CC} and ground. This sets the voltage into the terminal at 1/2 V_{CC}, or 2.5V in a 5.0V system. The small-signal input impedance is the parallel combination of the two 5.0 kΩ +167Ω paths, or about 2.5 kΩ. When the input swings from high to ground, the current transient is about 1.0 mA. A similar analysis shows the driver must source about 1/2 mA to bring the inverting input up to 2.4V.



Note: Schematic shows one-half of unit.

FIGURE 18. DS7820 Schematic

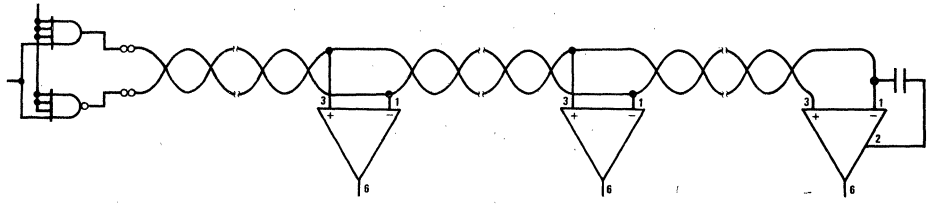


FIGURE 19. DS7830 Driving Daisy-Chained DS7820's

The DS7830 and DS7831 output curves are similar. Either can drive up to 12 DS7820 receivers strung along a cable, as in Figure 19, and have ample overdrive at the last receiver.

TERMINATING THE DIFFERENTIAL LINE

There are three modes of operation of the differential line, each of which demands a different answer to the commonly asked question of how to terminate the line. AN-22 only went into one case, namely, terminating a short line where data period exceeds two line lengths. The second case covers those lines where the period is less than two line lengths, and the third the case where the line is long.

Why is two line delay times significant? It's a question of power dissipation only. When the line is short, so that effectively no voltage is lost in the copper of the cable, running without a termination, where the differential capability of the driver exceeds 3.5V will produce reflections of 7.0V magnitude in the line.

This situation is best avoided, so a termination in the characteristic impedance of the line is advisable. When data rates are slow, this means that the driver, if the termination is dc, will continue to dissipate the power plotted on the load line of Figure 17, quite unnecessarily. If instead a capacitor is included in series with the dc termination, at the leading edge the termination appears dc, so Radio Frequency Interference (RFI) doesn't get generated. But as the capacitor charges, the voltage on the higher line rises, and the current in the driver drops, until at one V_{BE} below V_{CC}, line power ceases to be dissipated.

So long as the rise is controlled, RFI won't be a problem. And the rule of thumb of $R_1C = 3$ line lengths works very well. Where the driver is running so fast as never to be waiting for the reflection, it will be continuously dissipating the power indicated by the load line continuously.

As the line gets longer, the loop resistance gets up to the same order as the terminating resistor. That translates into an attenuation of the differential drive voltage at the receiver. Once the leading edge of the received voltage gets below 2.5V, the reflection ceases to have RFI significance, and a progressively worse mismatch is acceptable as the line gets longer, since the higher the termination resistor value, the more signal is available. For a typical cable, 1000 feet marks the point where any termination serves only to weaken the signal and narrow the channel bandwidth.

The bandwidth of the DS7820 receiver may be reduced by use of a shunt capacitor. The response curve is shown in Figure 20.

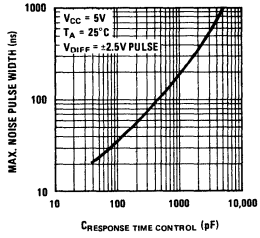


FIGURE 20. Noise Rejection in the DS7820A

MAXIMUM LINE LENGTHS

The tests in Table II were made with a DS7820 and DS7830 to settle questions about maximum line lengths and frequencies. Characteristics of the test cable were: 24 AWG gauge; 110Ω impedance; 5.6Ω/100 ft loop resistance; and 14 pF/ft capacitance.

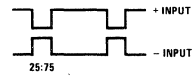
Receiver inputs were complementary pulses with 25/75% duty cycles. These simulate a string of alternating ones and zeros in an RZ (return to zero) format. The first results column indicates safe maximum data rates. The second column shows the rates at which attenuation reached a point where the signal could not switch the line receiver. These are typical, not maximum or safe rates.

Figure 21 illustrates the weaker signals which will switch the receiver. There is obviously no noise margin. For maximum performance, a single twisted-pair line should meet all three of these criteria:

1. High characteristic impedance (to maximize initial voltage step and voltage across the termination at the receiver)
2. Low capacitance (minimizes the "line charging" effect, which attenuates the signal's high-frequency components and makes dc loss worse by degrading the response to fast transients)
3. Low resistance to dc (use heavier-gauge cable for long runs driven at high frequency)

TABLE II. DS7830/DS7820A 24 Gauge 110Ω

Line Length	Point of Duty Cycle Distortion	Point of Failure To Invert
25'	10 MHz	25 MHz
200'	5.0 MHz	12 MHz
1000'	1.25 MHz	3.2 MHz
5000'	0.125 MHz	0.275 MHz



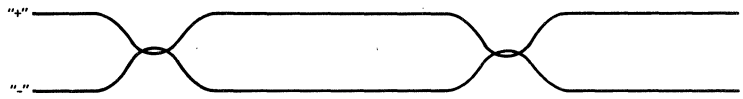


FIGURE 21. Differential Drive Long Distance

CROSSTALK IMMUNITY

One more question concerns crosstalk in multi-pair cables. The tests reported in Table III indicate that the individual pairs rarely, if ever, need individual shielding. One shield over all the pairs in the sheath should be adequate.

TABLE III.

NOISE THRESHOLD AT POINT A (VOLTS)		FREQUENCY
LOWER	UPPER	
1.22	1.26	500 kHz
1.22	1.27	100 kHz
1.24	1.30	10 kHz
1.24	1.30	1.0 kHz

Two side-by-side runs of twisted pairs in the cable were selected to provide two 800-foot lengths adjacent to each other in the bundle for their whole length. A DS7830 driver and a DS7820 receiver were connected to each pair. One driver's input was a pulse train and the other driver's input was a dc voltage. Tests were made to determine the susceptibility of the receiver on the dc line to signals cross-coupled into it from the pulsed line.

This driver/cable/receiver combination is susceptible in a transition region about 60 mV wide between the "1" and "0" states, indicated by the tabulated thresholds for the dc line. Signals from the ac side coupled-in sufficiently to trip the dc pair's receiver.

However, in a real system both driver outputs will swing through this region rapidly. The minimum swing is 2.0V. Therefore, the sensitive region is 60 mV/2,000 mV, or 3% of the swing and of the logic switching time. The minimum risetime of a non-damped DS7820 receiver output is 50 ns. Assuming this is the result of a straight voltage/time ramp input, the receiver is susceptible to crosstalk only if it is being driven with transition times greater than 50 ns/3%, or 1.6 ms.

In fact, the longest driver risetimes observed when the DS7830 was driving the longest cable in the previous test (Table II) were always less than 10 ns. We can conclude that a twisted pair with the driver and receiver is immune to crosstalk from another DS7830–DS7820 combination operating with any adjacent twisted pair.

EIA STANDARD CIRCUITS

The drivers and receivers listed as EIA RS232C circuits in Table I meet the specifications of that standard. It might be noted, however, that the standard's provisions antedate the availability of integrated circuits for such communications. Thus, it tends to restrict further development.

Compare the results in Table II, for example, with paragraph 1.3 of the standard. The standard indicates 20 kilobits/second is a nominal data transfer rate. And paragraph 1.4 requires single-ended, ground-referenced links even though true differential communications are demonstratedly more efficient in data exchanges between chassis.

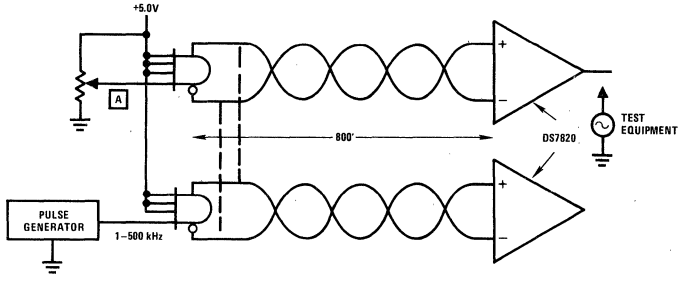


FIGURE 22. Crosstalk Between Close Twisted Pairs

NATIONAL

DRIVING 7-SEGMENT GAS DISCHARGE DISPLAY TUBES WITH NATIONAL SEMICONDUCTOR CIRCUITS

INTRODUCTION

Circuitry for driving high voltage cold cathode gas discharge 7-segment displays, such as Sperry Information Displays* and Burroughs Panaplex II, is greatly simplified by a complete new line of monolithic integrated circuits from National Semiconductor. The new products also make possible reduced cost of system implementation. They are: DS8880 high voltage cathode decoder/driver; DS8884A high voltage cathode decoder/driver; DS8885 MOS to high voltage cathode buffer; DS8889 low power cathode driver; and DS8887 8-digit anode driver.

In addition to satisfying all the displays' parameter requirements, including high output breakdown voltage, the new circuits have capability of programming segment current, and providing constant current sinking for the display segments. This feature alleviates the problem of achieving uniformity of brightness with unregulated display anode voltage. The National circuits can drive the displays directly.

Sperry Information Displays* and Burroughs Panaplex II are used principally in calculators and digital instruments. These 7-segment, multi-digit displays form characters by passing controlled currents through the appropriate anode/segment combinations. The cathode in any digit will glow when a voltage greater than the ionization voltage is applied between it (the cathode) and the anode for that digit. In the multiplexed mode of operation, a digit position is selected by driving the anode for that digit with a positive voltage pulse. At the same time, the selected cathode segments are driven with a negative current pulse. This causes the potential between the anode and the selected cathodes to exceed the ionization level, causing a visible glow discharge.

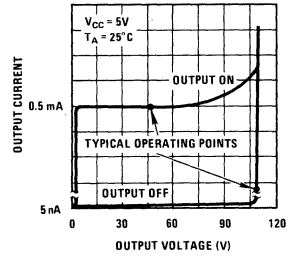
Generally, these displays exhibit the following characteristics: low "on" current per segment—from 200μA (in DC mode) to 1.2 mA (in multiplex mode); high tube anode supply voltage—180V to 200V; and moderate ionization voltage—170V. Once the element fires, operating voltage drops to approximately 150V and light output becomes a direct function of current, which is controlled by current limiting or current regulating cathode circuits. Current regulation therefore is most desirable since brightness will then be constant for large anode voltage changes. Tube anode to cathode "off" voltage is approximately 100V; and maximum "off" cathode leakage is 3μA to 5μA.

*Now called Beckman Displays

Correspondingly, specifications for the cathode driver must be complimentary, approximately as follows: A high "off" output breakdown voltage 80V minimum; typical "on" output voltage of 50V; maximum "on" output current of 1.5 mA per segment; and maximum "off" leakage current of 3μA to 5μA.

To allow operation without anode voltage regulation, the cathode driver must be able to sink a constant current in each output, with the output

(a) Cathode Driver Output Characteristic



(b) On Currents vs Temperature

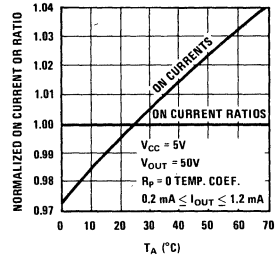


FIGURE 1.

"on" voltage ranging from 5V to 50V (see Figure 1). The following is a brief description of the circuits now offered by National:

DS8880 High Voltage Cathode Decoder/Driver

The DS8880 offers 7-segment outputs with high output breakdown voltage of 80V minimum; constant current-sink outputs; and programmable output current from 0.2 mA to 1.5 mA.

Application

The circuit has a built-in BCD decoder and can interface directly to Sperry and Panaplex II displays, minimizing external components (Figure 2). The inputs can be driven by TTL or MOS outputs directly. It is optimized for use in systems with 5V supplies.

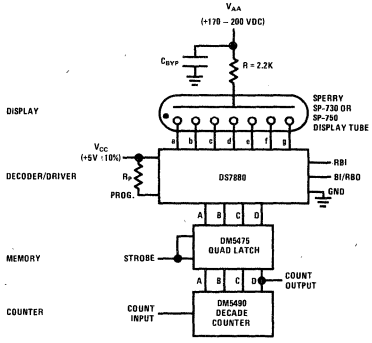


FIGURE 2. DC Operation From TTL

The DS8880 decoder/driver provides for unconditional as well as leading and trailing zero blanking. It utilizes negative input voltage clamp diodes. Typically, output current varies only 1% for output voltage changes of 3V to 50V. Operating power supply voltage is 5V. The device can be used for multiplexed or DC operation.

Available in 16-pin cavity DIP packages, the DS7880 is guaranteed over the full military operating temperature range of −55°C to +125°C; the DS8880 in molded DIP over the industrial range of 0°C to +70°C.

DS8884A High Voltage Cathode Decoder/Driver

The DS8884A offers 9-segment outputs with high output breakdown voltage of 80V minimum; constant current-sink outputs, programmable from 0.2 mA to 1.2 mA. It also offers input negative and positive voltage clamp diodes for DC restoring, and low input load current of −0.25 mA maximum.

Application

DS8884A decodes four lines of BCD input and drives 7-segment digits of gas-filled displays. There are two separate inputs and two additional outputs for direct control of decimal point and comma cathodes. The inputs can be DC coupled to TTL (Figure 3) or MOS outputs (Figure 4), or AC-coupled to TTL or MOS outputs (Figure 5) using only a capacitor. This means the device is useful in applications where level shifting is required. It can be used in multiplexed operation, and is available in an 18-pin molded DIP package.

Other advantages of the DS8884A are: typical output current variation of 1% for output voltage changes of 3V to 50V; and operating power supply

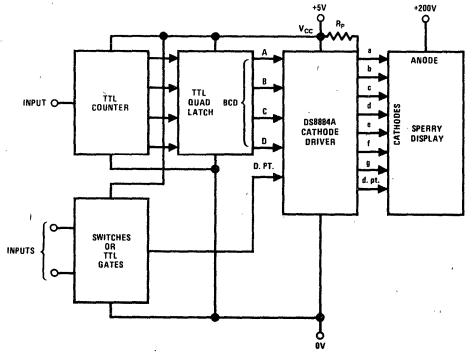


FIGURE 3. Interfacing Directly With TTL Output

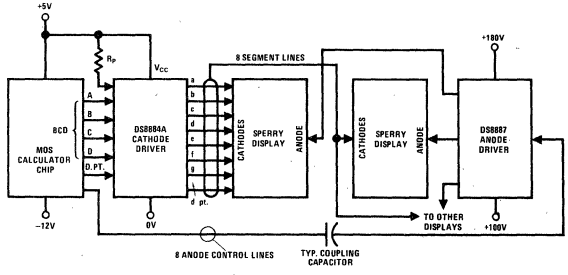


FIGURE 4. BCD Data Interfacing Directly With MOS Output

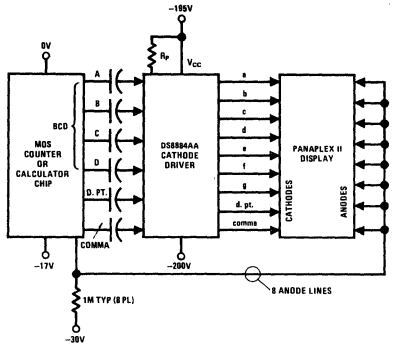


FIGURE 5. Cathode BCD Data AC Coupled From MOS Output

voltage of 5V. Inputs have pull-up resistors to increase noise immunity in AC coupled applications.

The DS8884A is guaranteed over the 0°C to +70°C operating temperature range.

DS8885 MOS to High Voltage Cathode Buffer

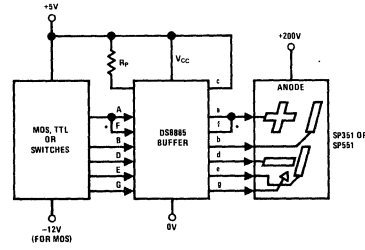
The DS8885 features seven constant current-sink outputs; programmable output current of 0.2 mA to 1.5 mA; high output breakdown voltage of 80V minimum; and capability for blanking through program current input. It operates from a +5V supply.

Application

DS8885 is best suited for interfacing 7-segment fully decoded MOS chips to digit displays. It is also useful for driving polarity, overrange, and decimal point segments.

DS8885 has 6 inputs and 7 outputs. Output c is decoded internally; the other 6 outputs are directly controlled by the 6 corresponding inputs. A typical application of this device is interfacing between an MOS calculator chip with 7-segment decoded outputs (open-drain or push-pull) and Sperry/Panaplex II displays (Figure 6).

When the DS8885 is used to drive minus and plus (polarity) cathodes, overrange, and decimal points, output c should be tied to V_{CC} so it does not saturate (Figure 7). This leaves 6 inputs and 6 outputs related one-to-one. The inputs can be driven directly from TTL or MOS outputs.



*Output may be paralleled for cathodes requiring more current, providing the corresponding inputs are also paralleled.

FIGURE 7. Polarity, Overrange, Decimal Point Driving

The DS8885 is available in 16-pin molded DIP package, and is guaranteed over the operating temperature range of 0°C to +70°C.

DS8889 Low Power Cathode Driver

The DS8889 requires no power supply since power is derived from program current. It offers extremely low standby power—only 1 mW internally. Features include programmable output currents 0.3 mA to 1.7 mA; 8 constant current-sink outputs; and input negative voltage clamp diodes for DC restoring. Outputs have 80V minimum breakdown voltage.

The device is suitable for multiplexed operation from fully decoded chips and is capable of driving decimal point segments simultaneously with numeric segments.

Application

The DS8889 has 8 inputs and 8 outputs, and interfaces directly between 7-segment decoded MOS outputs and numeric display tubes (Figures 8 and 9). It is optimized for use in systems with a limited number of power supplies.

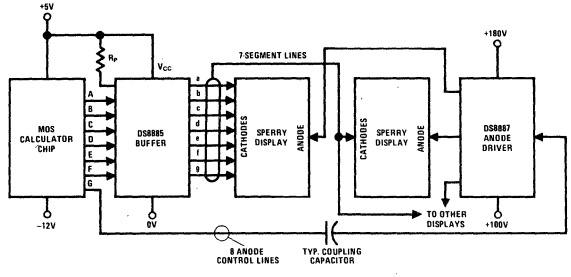


FIGURE 6. Fully Decoded MOS Cathode Outputs

The program input is characterized in terms of input current, therefore any supply (greater than 5V) can provide proper operation by connecting a single resistor to the program pin from the supply.

The DS8889, guaranteed for the 0°C to +70°C operating temperature range, is offered in the 18-pin molded DIP.

DS8887 8-Digit Anode Driver

The DS8887 interfaces directly to MOS chips and operates from a −40V to −80V power supply.

The DS8887 can operate virtually any multiplex display system requiring more output performance from the MOS chip than is available (Figures 4, 6, 8 and 9). It has low input current and voltage swing requirements but can drive up to 16 mA, and exhibits -55V minimum output breakdown voltage.

The DS8887 is available in the 18-pin molded DIP package; and is guaranteed over the operating temperature range of 0°C to +70°C.

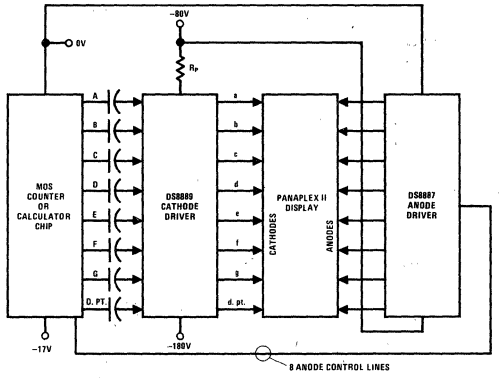


FIGURE 8. Decoded Cathode Data AC Coupled From MOS Output

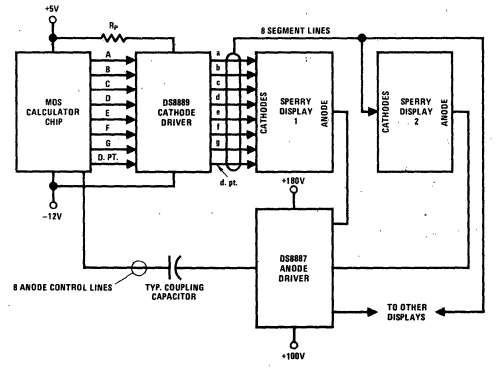


FIGURE 9. Decoded Cathode Data Direct Coupled From MOS Output

DRIVING 7-SEGMENT LED DISPLAYS WITH NATIONAL SEMICONDUCTOR CIRCUITS

INTRODUCTION

There are many different information display technologies available today, including liquid crystals, gas-discharge tubes, fluorescent tubes, incandescent lamps, and light emitting diodes (LEDs). Each technology has its own particular drive requirement. This note will focus on 7-segment LED display drive requirements and demonstrate that National Semiconductor has a full line of display drivers that meet the requirements for most any 7-segment LED drive application.

WHY ARE LED DRIVERS NEEDED?

The purpose of 7-segment LED drivers is to act as an interface element between data input and the display. This interface is necessary when either the input data format or circuitry current capabilities do not allow direct connection between input and display. To satisfy these needs, National's 7-segment LED drivers are divided into two basic categories.

1. Internally decoded (BCD to 7-segment)
   DS5446A/DS7446A
   DS5447A/DS7447A
   DS5448/DS7448
   DS7856/DS8856
   DS8857
   DS7858/DS8858

2. Non-decoding, direct drive (MOS to LED)

DS75491	DS8864
DS75492	DS8865
DS8861	DS8866
DS8863	

Thus, National has circuits that will drive 7-segment LEDs from either fully decoded circuits or from non-decoded outputs.

CONFIGURATIONS AND CONSTRUCTION OF 7-SEGMENT LEDs

LEDs are segregated into two groupings with regard to construction, see Figure 1.

Common anode displays are constructed on a common substrate which forms the anode of the diodes, while each of the seven cathodes are bonded out to separate pins. The second type, common cathode, has the cathode fabricated on a common substrate with the anodes bonded out to individual pins. Due to these radically different configurations, drive circuits are usually tailored in their design for one or the other type. Tailoring in this respect means either sinking current (active low) or sourcing current (active high) when referenced to segment drive. In addition, drive requirements are quite variable because of LED light intensity requirements as well as digit size

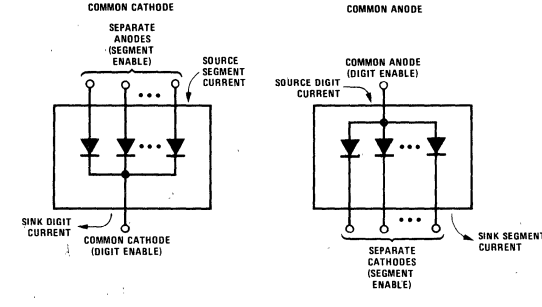


FIGURE 1. 7-Segment LED Construction

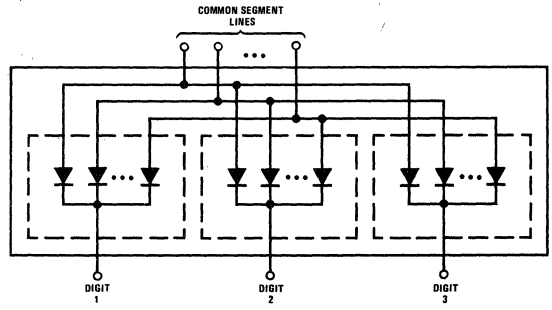


FIGURE 2. Multi-Digit 7-Segment LED

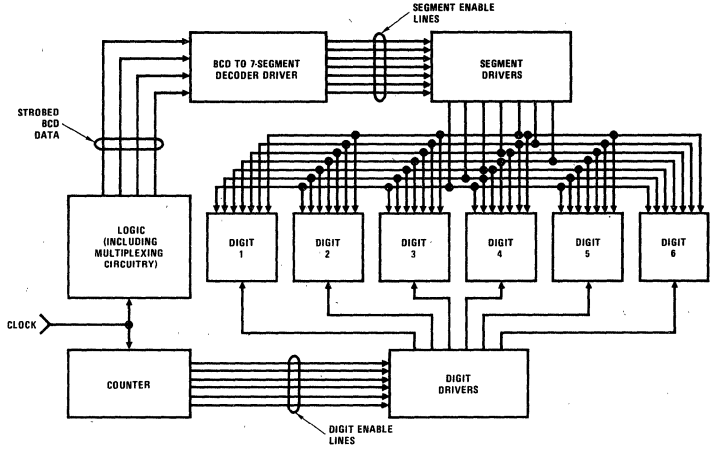


FIGURE 3. A Typical Multiplexing Scheme

and efficiency. Thus the system designer needs a degree of latitude not only with respect to the type of display used but also the drive current available.

7-segment LEDs can be purchased in either single or multi-digit display packages. Single digit displays have individual segment and common pins while multi-digits have paralleled segment pins and separate digit pins equal to the number of digits in the package, see Figure 2.

Multi-digit displays, due to their configuration, must be driven in a multiplex mode of drive, where segment drivers are time shared by all the digits. This is contrasted to the single digit displays which may be driven in either the multiplex or the non-multiplex (direct drive) mode. The nonmultiplex mode uses separate segment drivers for each digit of the display. Multiplex operation has a decided cost saving advantage over nonmultiplex operation especially when the number of digits being driven is large.

MODES OF 7-SEGMENT LED DRIVE

In the multiplex mode of drive the LED digits in a multi-digit format are driven by a single set of segment drivers while each digit is selected by its own digit driver. Figure 3 shows the circuitry needed to implement a typical six digit multiplexed display.

Each digit is selected individually by enabling its digit driver whose control is determined by a counter or equivalent circuitry operating at some clock frequency. Strobed data, by way of the counter and multiplex circuitry, is then displayed on the selected digit by the single set of segment drivers. If the strobe rate is high enough, from about 250 to 1,000 Hz depending on external conditions, the display will appear flicker free to the human eye. The BCD-to-7-segment decoder converts BCD data to the desired 7-segment output format.

In the multiplex mode each digit has a reduced duty cycle and is operated at somewhat higher than average or typical dc operating current levels. The amount of current will be a function of the number of digits, duty cycle, and the type and efficiency of the display used. Since currents are higher than average so also will be the LED brightness due to the nearly linear brightness versus current curve for most LEDs. The human eye will detect the brightness peaks and through a partially integrating and peak detecting action will perceive a higher display brightness at some average current level in the multiplex mode than the same average current in the nonmultiplex (direct drive) mode. The result is that a multiplexed display will operate at a lower total power than the same display operated in the nonmultiplex mode with the same apparent brightness.

In the nonmultiplex mode of 7-segment LED drive each digit has its own set of segment drivers thereby dropping the digit driver select requirement of multiplexed operation. In this case, the common digit pin may be tied to the highest potential if common anode or the lowest if common cathode. It is evident that in a nonmultiplexed display the driver package count would be high since each digit requires its own set of segment and possibly decoder drivers. If a large number of digits are used the segment driver package count would equal the number of digits while in the multiplex mode this count is equal to one. Granted, in the multiplex mode additional control circuitry is required. Consideration of the relative cost of this circuitry in comparison to the segment decoder driver circuitry in the nonmultiplex mode results, in general, in the fact that if the number of digits in the display equals or is more than four, total package count and/or cost is less in the multiplex mode of drive.

In most MOS circuits multiplex operation is ideal since the counter, multiplexer, and BCD to 7-segment decoders or equivalent circuitry can usually be incorporated on the same chip along with calculator, clock or other function. In this case the only external interface components required would be the digit and segment drivers since MOS circuits are generally unable to sink or source the higher current required for most multiplex operations.

In summary, LED driver requirements for multiplex or nonmultiplex drive operation require either segment, digit or BCD to 7-segment drivers. Analysis of the particular system needs with regard to the number of digits and relative circuit costs should be the determining factor for multiplex or nonmultiplex operation. Circuit requirements for multiplex operation will in general require relatively high current capabilities.

NATIONAL'S 7-SEGMENT LED DRIVERS

Table I lists the 7-segment LED drivers available from National. Each circuits application is divided into groupings with respect to common anode or cathode, digit or segment, multiplex or nonmultiplex areas. Additionally, current capabilities are also specified for each product.

From the table it is evident that some of the circuits may be used in dual roles – both multiplex or nonmultiplex; common cathode or anode. In general, what will determine whether one drivers application is multiplex or nonmultiplex is that drivers current capability. The direction of current flow through the driver (source or sink) is the determining factor in dual application with regard to common anode or cathode.

Table II lists the operating temperature range and package types for the 7-segment LED drivers.

In the following sections each circuit is described in greater detail and typical applications are given.

BCD TO 7-SEGMENT DECODER DRIVERS

DM5446A/DM7446A, DM5447A/DM7447A, DM5448/DM7448

This family of BCD to 7-segment decoder drivers was designed for the most general possible display drive applications including display technologies other than LEDs. The difference between the circuits is in their output stage configurations. These differences will be discussed separately later.

The circuits convert the standard 4-bit BCD input to the popular 7-segment output format. All input BCD codes above 9 are decoded into unique patterns that verify operation. The circuits are TTL-DTL compatible and operate off of a single 5.0V supply.

Added features included in all circuits are a ripple blanking input pin as well as a lamp test pin for display turn on. In addition the blanking input/ripple blanking output pin may be used to modulate display intensity.

TABLE I. National 7-Segment LED Drivers

Refer to LED Driver Guide in Front of Catalog

DEVICE NUMBER	COMMON CATHODE		COMMON ANODE		DIGIT DRIVER	SEGMENT DRIVER	INTERNAL DECODING	CURRENT CAPABILITY AND FEATURES
	Multiplex	Nonmultiplex	Multiplex	Nonmultiplex				
DM5446A/DM7446A DM5447A/DM7447A			X	X		X	X	Up to 40 mA Sink, Open Collector High Breakdown (30/15V) TTL Input Compatibility
DM5448/DM7448		X	X*	X*		X	X	1.3 mA Source, Adjustable Externally, TTL Input Compatibility
DS7856/DS8856		X	X*	X*		X	X	6.0 mA Typical Source, TTL Input Compatibility
DS8857	X	X				X	X	50 mA Typical Source, Externally Adjustable, TTL Input Compatibility
DS7858/DS8858	X	X				X	X	Adjustable Source Current 0 to 50 mA, TTL Input Compatibility
DS75491	X	X	X	X	X	X		50 mA Source/Sink, 4 Drivers per Package, MOS Input Compatibility
DS75492	X		X	X	X	X**		250 mA Sink, 6 Drivers per Package, MOS Input Compatibility
DS8861	X	X	X	X	X	X		50 mA Source/Sink, 5 Drivers per Package, MOS Input Compatibility
DS8863	X		X	X	X	X**		500 mA Sink, 8 Drivers per Package, MOS Input Compatibility
DS8864	X		X	X	X	X**		50 mA Sink, 9 Drivers per Package, MOS Input Compatibility
DS8865	X		X	X	X	X**		50 mA Sink, 8 Drivers per Package, MOS Input Compatibility
DS8866	X		X	X	X	X**		50 mA Sink, 7 Drivers per Package, MOS Input Compatibility

*With the use of an external transistor/segment.

**For common anode LED's.

TABLE II. Operating Temperature Range and Package Type

DEVICE NUMBER	OPERATING TEMPERATURE RANGE		NUMBER OF PINS			PACKAGE TYPE		
	0°C to +70°C	−55°C to +125°C	14	16	18	Plastic Molded DIP (N)	Ceramic DIP (J)	Flat Pack (W)
DM5446A, DM5447A		X		X			X	X
DM7446A, DM7447A	X			X		X	X	X
DM5448		X		X			X	X
DM7448	X			X		X	X	X
DS7856		X		X			X	X
DS8856	X			X		X	X	X
DS8857	X			X			X	
DS7858		X		X			X	X
DS8858	X			X		X	X	X
DS75491	X		X			X	X	X
DS75492	X		X			X	X	X
DS8861	X				X	X		
DS8863	X				X	X		
DS8865	X				X	X		
DS8866	X				X	X		
DS8864	X		22			X		

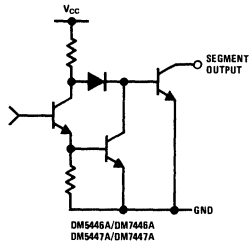


FIGURE 4a. Output Stage

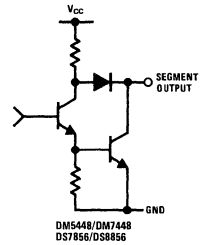
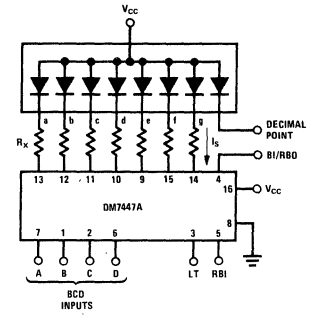


FIGURE 4b. Output Stage



The following equation may be used to determine the appropriate value of R_X (segment current limit resistor) for some LED current/segment I_S (mA).

$$R_X = \frac{V_{CC} - 0.3 - V_{LED\ (@\ I_S)}}{I_S} \quad k\Omega$$

$(I_S \leq 40\ mA)$

where $V_{LED\ (@\ I_S)}$ is the diode (LED) voltage drop at operating current I_S.

Example:

$I_S = 20\ mA$

$V_{LED\ (@\ I_S)} = 3.4V^*$

$V_{CC} = 5.0V$

$R_X = 65\Omega$

*MAN-1 or equivalent

FIGURE 5. Nonmultiplex Application of the DM7447A

DM5446A/DM7446A, DM5447A/DM7447A

These circuits feature active-low, open collector high current outputs (Figure 4a). Each output is capable of sinking up to 40 mA at a maximum internal drop of 0.4V. This high current capability makes these circuits particularly well suited for driving the large NSN71 or equivalent type displays directly. The circuits are also applicable, with or without the use of external current limit resistors, to driving lower current displays in the multiplex mode of drive.

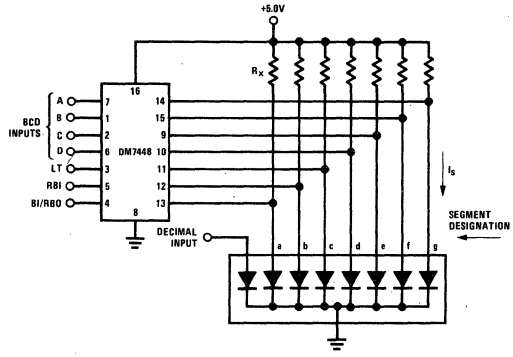
The DM5446A and DM7446A outputs are capable of withstanding 30V at a maximum leakage of 250μA over temperature. The DM5447A and DM7447A have a 15V output capability at a maximum leakage over temperature of 250μA. This standoff voltage ability makes the circuits applicable for direct drive to indicator lamp type displays. Figure 5 shows a typical application of the circuits with LEDs.

Refer to Table II for the operating temperature range and package types for the DM5446A/DM7446A and DM5447A/DM7447A.

DM5448/DM7448

The DM5448/DM7448 has active high passive pull-up outputs (Figure 4b) with a TTL fanout of 4. The typical output source current is 2.0 mA at an output voltage of 0.85V. Each output is capable of sinking 6.4 mA with a maximum internal drop of 0.4V. Since the output current level is low the circuit can be used to drive low current common cathode displays operating in the nonmultiplex mode.

The major application of the DM5448/DM7448 is to drive logic circuits, operate high-voltage loads such as electroluminescent displays through buffer transistors or SCR switches, or high-current



R_X may be calculated using the following equation

$$R_X = \frac{5.0 - V_{LED}}{I_S - 1.6}\ k\Omega = \frac{3.3}{I_S - 1.6}\ k\Omega \quad \left[\begin{array}{l} V_{LED} = 1.7V\ @\ 5.0\ mA \\ R_X \geq 650\Omega \end{array}\right]$$

where:

R_X = PULL-UP RESISTOR VALUE

I_S = CURRENT PER SEGMENT IN mA

Example:

I_S = 5.0 mA

R_X = 970Ω

FIGURE 6. Nonmultiplex Application of the DM7448

loads through buffer transistors. Figure 6 shows the DM7448 in a low current direct drive LED application.

The operating temperature range and package types for the DM5448/DM7448 are given in Table II.

BCD TO 7-SEGMENT LED DRIVERS

DS7856/DS8856, DS8857, DS7858/DS8858

This series of three circuits was designed to provide a wide range of current capabilities in driving common cathode 7-segment LEDs operating in the multiplex or nonmultiplex mode. The circuits, discussed individually below, have output stages with varying source current capability designed for specific as well as general applications.

All circuits accept 4-bit BCD and decode this input to the desired 7-segment output format for direct drive to LEDs. In addition, the circuits feature a lamp test pin for display turn-on check, ripple blanking-input pin and blanking input/ripple blanking output pin which may be used to modulate display intensity.

The three circuits are TTL-DTL compatible and provide full decoding of the 16 possible input combinations. All parts operate off of a single 5.0V supply.

DS7856/DS8856

The DS7856/DS8856 output stages, passive-pullup (active high, Figure 4b), provide a typical source current of 6.0 mA at an output voltage of 1.7V. This current level was designed for directly driving, without the use of external current limit resistors, the NSN74 or equivalent type displays in the nonmultiplex mode of operation.

Each output has a fan-out of 4 and is capable of sinking 6.4 mA with a maximum internal drop of 0.4V making the circuit suitable for use with logic circuits. With the use of an external buffer transistor per output the circuit may be used to drive high current common anode LED displays as well as high voltage electroluminescent displays. Figure 7 shows a typical application of the DS8856.

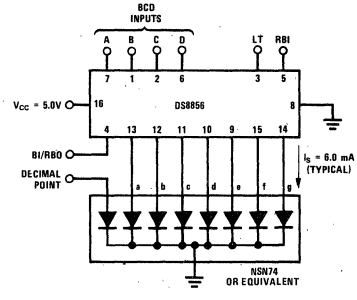


FIGURE 7. Nonmultiplex Application of the DS8856

Operating temperature range and package types for the DS7856/DS8856 are given in Table II.

DS8857

The output stages of the DS8857, active pull-up (active-high, Figure 4c), source a typical current of 50 mA at an output voltage of 2.3V. The circuit was designed to be used with NSN74 or equivalent type displays operating in the multiplex mode of drive. With this high current capability the circuit can drive up to 16 such digits.

The applications of this circuit obviously are not limited to just the NSN74 type of display. Common cathode displays with high dc current requirements or lower multiplex current levels may be driven by this circuit with the use of an external current limit resistor per segment. A typical application of the DS8857 is given in Figure 8.

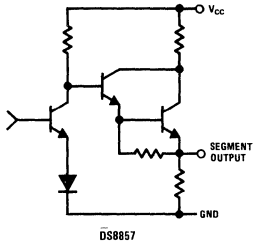


FIGURE 4c. Output Stage

Table II gives the operating temperature range and package type for the DS8857.

DS7858/DS8858

The DS7858/DS8858 output stages are active pull-up (active-high, Figure 4d) like those of the DS8857. The output stages are exactly the same as the DS8857 except that the internal current limit resistor per output has been removed. External current limit resistors must then be used. This allows the circuit to be customized for a particular common cathode multiplex or non-multiplex application. Each output stage, through its own external resistor, can be programmed to some current from 50 mA down to 0 mA. Care must be taken in not shorting the outputs to ground because of the excessive current flow that would result from the Darlington upper stage. See Figure 9 for a typical application of the DS8858.

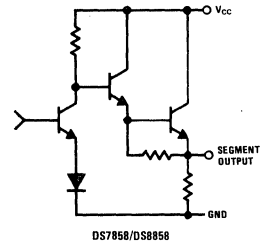
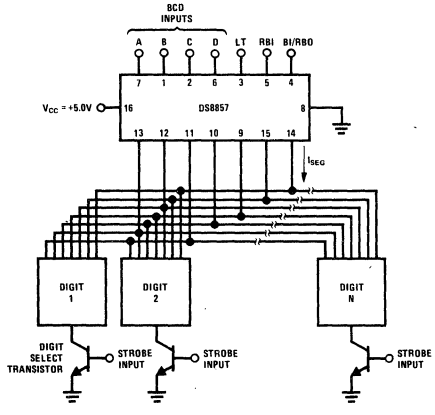


FIGURE 4d. Output Stage



For multiplex or nonmultiplex applications where an external current limit resistor per segment is required,see the output current vs voltage curve for the DS8857 and use the equation given in Figure 9 to calculator the resistor value.

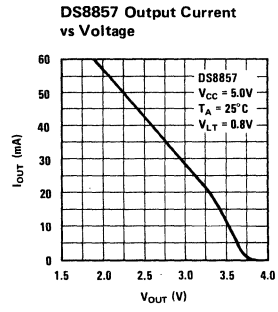


FIGURE 8. DS8857 Typical Multiplexing Scheme

Maximum output source current per segment for the DS7858/DS8858 is 50 mA. Operating temperature range and package types are given in Table II.

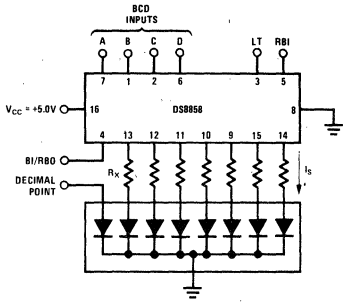
Special care must be taken in the use of the DS7858 ceramic and the DS8858 plastic DIP's with regard to not exceeding the maximum operating junction temperature of the devices. The maximum junction temperature of the DS7858J is 150°C and must be derated based on a thermal resistance of 80°C/Watt, junction to ambient. The maximum junction temperature for the DS8858N is 150°C and must be derated based on a thermal resistance of 140°C/Watt, junction to ambient.

DS75491, DS8861 MOS TO LED SEGMENT DRIVERS

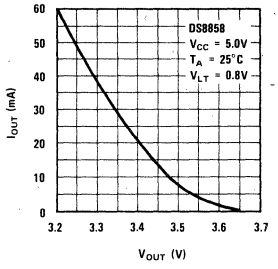
The DS75491 and DS8861 were designed for MOS calculator applications. Both circuits feature low input current, 3.3 mA maximum at 10V input, making them suitable for direct drive from MOS circuits. The circuits are used to drive the paralleled segments in multi-digit displays. Since both circuits feature accessable collectors and emitters they may be used as either common cathode or anode segment drivers. They feature a source or sink current capability of up to 50 mA with a maximum collector to emitter drop of 1.5V over the operating temperature range. In addition, each output is specified to have a maximum leakage of 100μA at an output voltage of 10V over temperature. Both circuits operate from a single supply that can have a maximum voltage of 10V.

DS75491 FOUR SEGMENT DRIVER

The DS75491 is a four-segment driver whose main application is with multi-digit LEDs operating in the multiplex mode of drive. Each package contains four separate segment drivers, each driver



DS8858 Output Current vs Voltage



To find the appropriate value of the segment current limit resistor R_X the following equation should be used.

$$R_X = \frac{V_{OUT} - V_D}{I_S}$$

where:

I_S = Segment current

V_D = LED diode drop at current I_S

V_{OUT} = DS8858 output voltage at current I_S (see graph)

Example:

I_S = 5.0 mA

V_D = 1.7V (AT 5.0 mA)

From graph (V_{CC} = 5.0V, T_A = 25°C)

V_{OUT} = 3.53V (AT 5.0 mA)

$$R_X = \frac{3.53V - 1.7V}{5.0\ mA}$$

R_X = 360Ω

The same equation may be used when either the DS7858 or the DS8858 are operating in the multiplex mode of drive. If the additional voltage drop due to the digit driver is taken into consideration,the new equation would have the following form:

$$R_X = \frac{V_{OUT} - V_D - V_{DR}}{I_S}$$

V_{DR} = Digit driver drop at current I_S

FIGURE 9. DS8858 Applications

with free collector and emitter points, see Figure 4e.

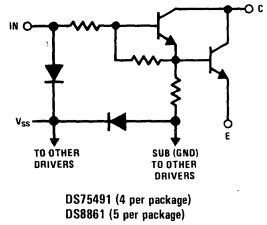


FIGURE 4e. Circuit Schematic

In the multiplex mode of drive, a six digit calculator needs only two DS75491's to drive the segments in the display, see Figure 10. The total of eight segment drivers allows drive to each of the individual seven segments plus logic control for the decimal point. Figure 11 shows the DS75491 used in an 8 digit calculator application.

Table II lists the package type and temperature range of the DS75491.

DM8861 FIVE SEGMENT DRIVER

The DS8861 is a five segment driver which like the DS75491 is used with multi-digit LEDs operating in the multiplex mode of drive. Each package contains five separate drivers, each driver with free collector and emitter points, Figure 4e.

A typical application of the DS8861 is given in Figure 11 where the DS8861 is combined with the DS75491 to provide a total of nine independent sources of LED segment current from an MOS calculator. This allows control of the 7-segments plus decimal point and minus sign. This combination of circuits is not solely applicable to just the 8 digit calculator configuration shown but can be used with a display having as many digits as desired as long as the multiplexed segment current requirement does not exceed 50 mA.

As with the DS75491, the DS8861 is also applicable to use with common anode displays as well as common cathode since each driver has its collector bonded out to a separate pin.

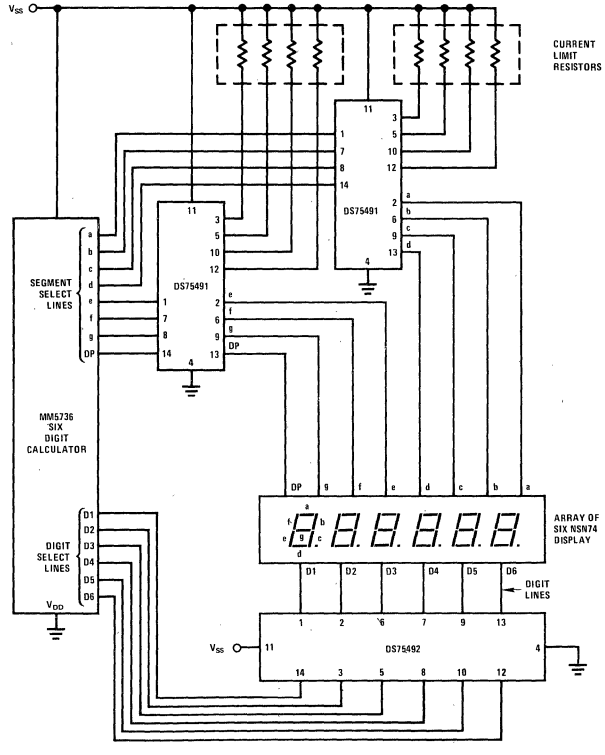


FIGURE 10. 6-Digit Calculator

Refer to Table II for operating temperature range and package type for the DS8861.

DS75492, DS8863 MOS TO LED DIGIT DRIVERS

The DS75492 and DS8863 are digit drivers designed to drive multi-digit common cathode LEDs directly from MOS circuits. Since digit currents are quite high in multiplex operation MOS circuits usually cannot sink the required digit select current, therefore these circuits provide the required current buffering. The two circuits have different current handling capability as well as different numbers of drivers per package, each will be discussed individually later.

The circuits are totally compatible for use with both the DS75491 and the DS8861. The most common usage of the circuits is in MOS calculator applications where the DS75491 or the DS8861 source the segment current and either the DS75492 or the DS8863 sink the digit current.

DS75492 SIX DIGIT DRIVER

The DS75492 is a six digit LED driver designed to be used with common cathode multi-digit displays operating in the multiplex mode of drive.

The circuit features six high gain Darlington connected transistors, with collectors open and emitters tied to ground (Figure 4f), capable of sinking up to 250 mA with a maximum collector to ground drop of 1.5V over the operating temperature range. Low input current of 3.3 mA maximum at 10V makes the drivers suitable for direct connection to MOS circuits. Output leakage is 200μA maximum at 10V over temperature. Maximum V_{CC} is 10V.

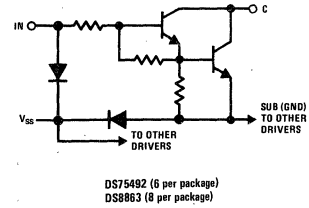


FIGURE 4f. Circuit Schematic

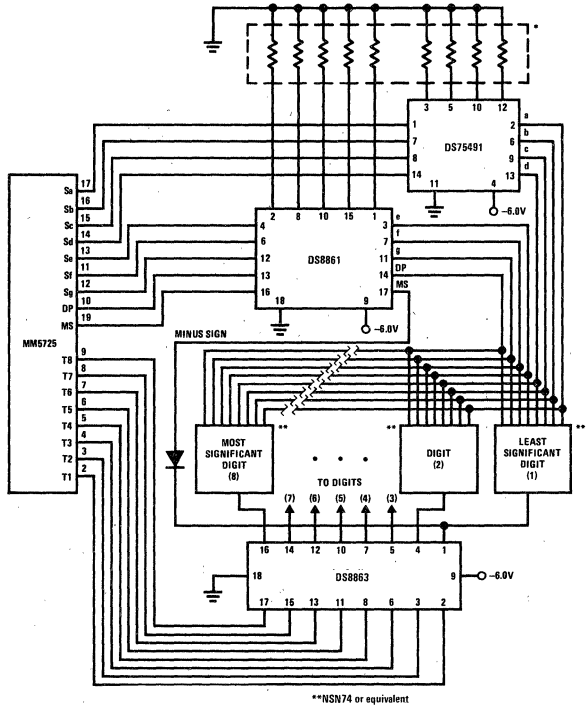


FIGURE 11. 8-Digit Calculator

In Figure 10 the DS75492 is shown along with the DS75491 in a typical six digit calculator application. Since the calculator circuit shown is operated in the multiplex mode of drive only one DS75492 is required, replacing at least six transistors and resistors for the equivalent discrete circuit.

The operating temperature range and package type for the DS75492 is given in Table II.

DS8863 EIGHT DIGIT DRIVER

The DS8863 is an eight digit LED driver designed to be used in conjunction with either the DS75491 and/or the DS8861 in driving eight common cathode LED digits operating in the multiplex mode of drive.

This circuit features eight separate high gain Darlington connected transistor circuits, see Figure 4f. Each Darlington transistor pair is capable of sinking 500 mA with a maximum collector to ground drop of 1.6V. Each collector can withstand 10V at a maximum leakage of 250μA in the off state. Maximum input current is 2.0 mA at 10V, making the circuit particularly well suited for direct drive from MOS circuits.

Figure 11 shows the DS8863 used in a typical 8-digit calculator application. The important feature of the DS8863 is the very high sink current capability. This allows multiplex operation of large digits or large numbers of digits without the use of discrete high current transistors.

Another application of the DS8863 is shown in Figure 12. In this case the DS8863 is used along with the MM5314 series digital clock circuits in the implementation of a 6-digit clock display. Here the DS8863 is used as a segment driver for a common anode display. The use of the DS8863 in this manner replaces a total of 14 resistors and 7 transistors.

The DS8863 uses a single supply with a maximum voltage of 10V. Table II specifies the operating temperature range and package type for the DS8863.

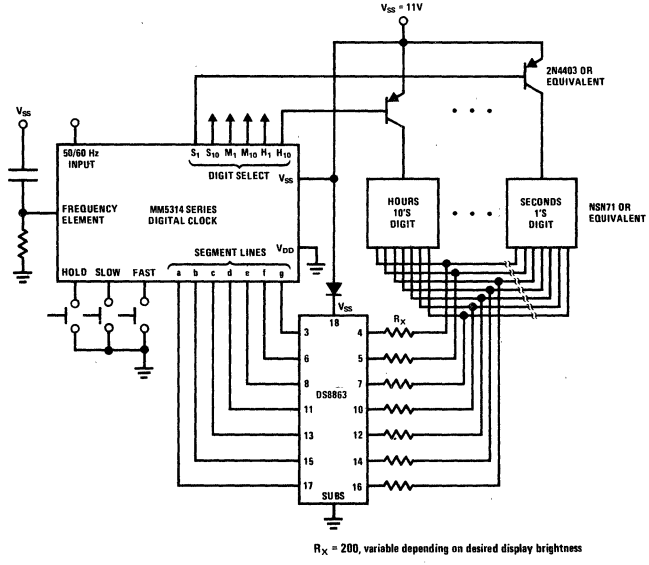


FIGURE 12. Digital Clock Using DS8863

DS8864, DS8865, DS8866 MOS TO LED DIGIT DRIVERS

The DS8864, DS8865, and DS8866 were designed to drive common cathode nine, eight, and seven digit displays respectively. The applications of these drivers are similar to those of the DS75492 and DS8863 except that operating current levels are lower.

All circuits feature maximum input current of 2.0 mA at a voltage of 6.5V. Output sink capability is 50 mA at a maximum collector to ground drop of 1.5V. Output leakage is 40μA (max) at an output voltage of 6.0V. All circuits operate from a supply that can vary from 5.0V to 9.5V.

DS8864 NINE DIGIT DRIVER

The DS8864 is a nine digit common cathode LED driver. Each package contains nine separate digit drivers. The circuit also features a "low battery" indicator driver which will light a decimal point whenever a 9.0V battery drops below 6.5V typical.

Figure 13 shows the DS8864 in a typical calculator drive application. The operating temperature range and package type for the DS8864 is given in Table II.

DS8865 EIGHT DIGIT DRIVER

The DS8865 is an eight digit common cathode LED driver. Eight separate drivers are contained within each package. As with the DS8864 and DS8866, the DS8865 can also be used as a segment driver for common anode displays in the multiplex or nonmultiplex mode as long as the segment current does not exceed 50 mA and is current limited with external resistors.

Table II gives the operating temperature range and package type for the DS8865.

DS8866 SEVEN DIGIT DRIVER

The DS8866 is a seven digit common cathode LED driver. Each package contains seven separate digit drivers. Logic is also provided for a "low battery" indicator which will detect a 9.0V battery drop to below 6.5V typical and drive a decimal point.

Table II lists the package type and temperature range of the DS8866.

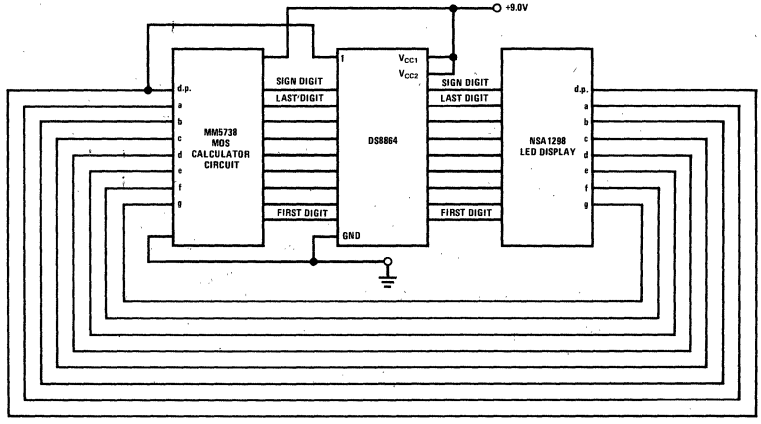


FIGURE 13. A Typical Application of the DS8864, Showing a Complete 8-Digit, 5 Function Calculator with Memory.

TRANSMISSION LINE CHARACTERISTICS

INTRODUCTION

Digital systems generally require the transmission of digital signals to and from other elements of the system. The component wavelengths of the digital signals will usually be shorter than the electrical length of the cable used to connect the subsystems together and, therefore, the cables should be treated as a transmissions line. In addition, the digital signal is usually exposed to hostile electrical noise source which will require more noise immunity then required in the individual subsystems environment.

The requirements for transmission line techniques and noise immunity are recognized by the designers of subsystems and systems, but the solution used vary considerably. Two widely used example methods of the solution are shown in *Figure 1*. The two methods

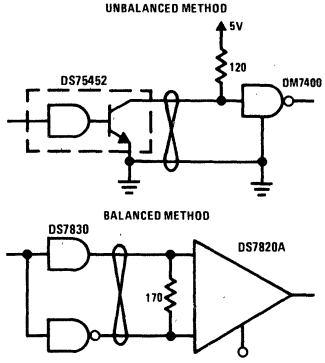


FIGURE 1.

illustrated use unbalanced and balanced circuit techniques. This application note will delineate the characteristics of digital signals in transmission lines and characteristics of the line that effect the quality, and will compare the unbalanced and balanced circuits performance in digital systems.

NOISE

The cables used to transmit digital signals external to a subsystem and in route between the subsystem, are exposed to external electromagnetic noise caused by switching transients from actuating devices of neighboring control systems. Also external to a specific subsystem, another subsystem may have a ground problem which will induce noise on the system, as indicated in *Figure 2*.

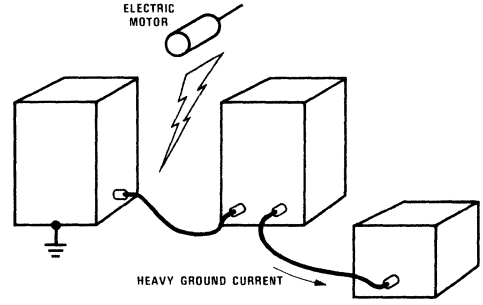


FIGURE 2. External Noise Sources

The signals in adjacent wires inside a cable may induce electromagnetic noise on other wires in the cable. The induced electromagnetic noise is worse when a line terminated at one end of the cable is near to a driver at the same end, as shown in *Figure 3*. Some noise may be

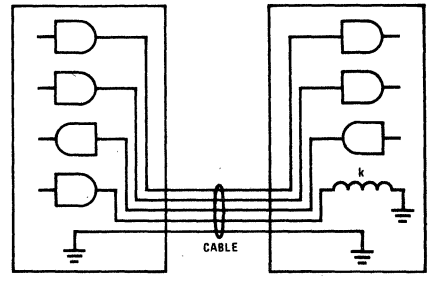


FIGURE 3. Internal Noise Sources

induced from relay circuits which have very large transient voltage swings compared to the digital signals in the same cable. Another source of induced noise is current in the common ground wire or wires in the cable.

DISTORTION

The objective is the transmission and recovery of digital intelligence between subsystems, and to this end, the characteristics of the data recovered must resemble the data transmitted. In *Figure 4* there is a difference in the pulse width of the data and timing signal transmitted, and the corresponding signal received. In addition there is a further difference in the signal when the data is "AND"ed with the timing signal. The distortion of the signal occurred in the transmission line and in the line driver and receiver.

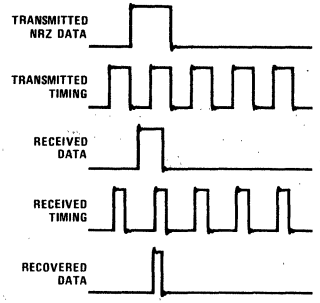


FIGURE 4. Effect of Distortion

A primary cause of distortion is the effect the transmission line has on the rise time of the transmitted data. *Figure 5* shows what happens to a voltage step from the driver as it travels down the line. The rise time of the signal increases as the signal travels down the line. This effect will tend to affect the timing of the recovered signal.

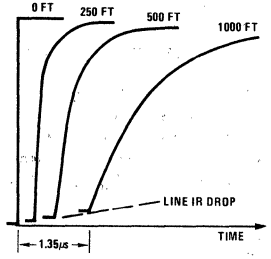


FIGURE 5. Signal Response at Receiver

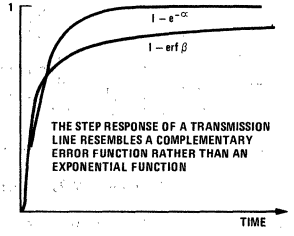


FIGURE 6. Signal Rise Time

The rise time in a transmission line is not an exponential function but a complementary error function. The high frequency components of the step input are attenuated and delayed more than the low frequency components. This attenuation is inversely proportional to the frequency. Notice in *Figure 6* particularly that the signal takes much longer to reach its final dc value. This effect is more significant for fast risetimes.

The Duty Cycle of the transmitted signal also causes distortion. The effect is related to the signal rise time as shown in *Figure 7*. The signal doesn't reach one logic level before the signal changes to another level. If the signal has a 1/2 (50%) Duty Cycle and the threshold of the receiver is halfway between the logic levels, the distortion is small. But if the Duty Cycle is 1/8 as shown in the second case the signal is considerably distorted. In some cases, the signal may not reach the receiver threshold at all.

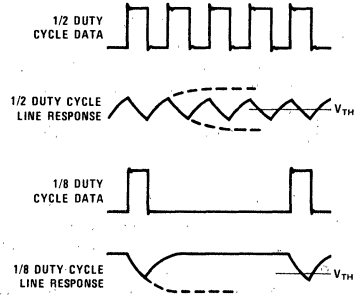


FIGURE 7. Signal Distortion Due to Duty Cycle

In the previous example, it was assumed that the threshold of the receiver was halfway between the ONE and ZERO logic levels. If the receiver threshold isn't halfway the receiver will contribute to the distortion of the recovered signal. As shown in *Figure 8*, the pulse time is lengthened or shortened, depending on the polarity of the signal at the receiver. This is due to the offset of the receiver threshold.

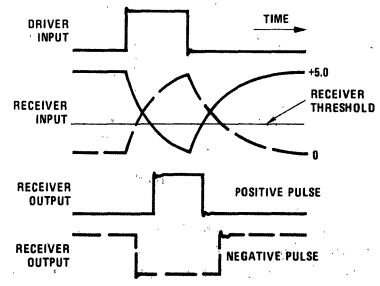


FIGURE 8. Slicing Level Distortion

UNBALANCED METHOD

Another source of distortion is caused by the IR losses in the wire. *Figure 9* shows the IR losses that occur in a thousand feet of no. 22 AWG wire. Notice in this

example that the losses reduce the signal below the threshold of the receiver in the unbalanced method. Also that part of the IR drop in the ground wire is common to other circuits—this ground signal will appear as a source of noise to the other unbalanced line receivers in the system.

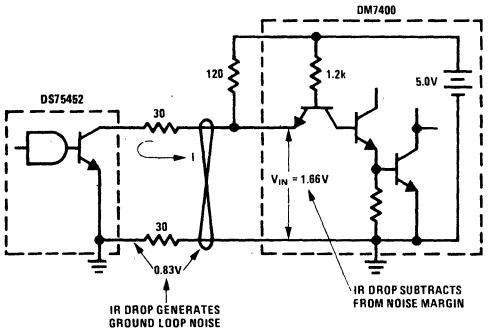


FIGURE 9. Unbalanced Method

Transmission lines don't necessarily have to be perfectly terminated at both ends, (as will be shown later) but the termination used in the unbalanced method will cause additional distortion. *Figure 10* shows the signal on the transmission line at the driver and at the receiver. In this case the receiver was terminated in 120Ω, but the characteristic impedance of the line is much less. Notice that the wave forms have significant steps due to the incorrect termination of the line. The signal is subject to misinterpretation by the line receiver during the period of this signal transient because of the distortion caused by Duty Cycle and attenuation. In addition, the noise margin of the signal is reduced.

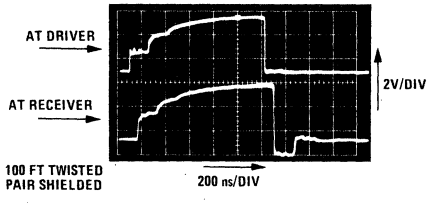


FIGURE 10. DS75451, DM7400 Line Voltage Waveforms

The signal waveforms on the transmission line can be estimated before hand by a reflection diagram. *Figure 11* shows the reflection diagram of the rise time wave forms. The voltage versus current plot on left is used to predict the transient rise time of the signal shown on the right. The initial condition on the transmission line is an IR drop across the line termination. The first transient on the line traverses from this initial point to zero current. The path it follows corresponds to the characteristic impedance of the line. The second transient on the diagram is at the line termination. As shown, the signal reflects back and forth until it reaches its final dc value.

Figure 12 shows the reflection diagram of the fall time. Again the signal reflects back and forth between the line termination until it reaches its final dc value. In both the rise and fall time diagrams, there are transient voltage and current signals that subtract from the particular signal and add to the system noise.

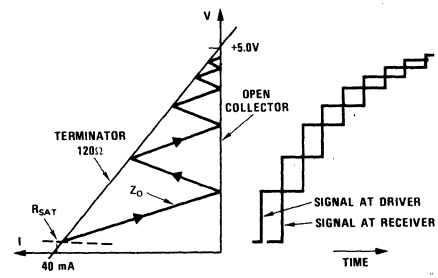


FIGURE 11. Line Reflection Diagram of Rise Time

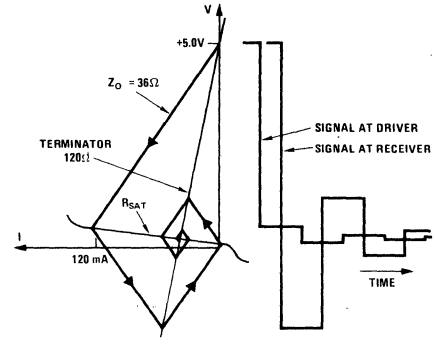


FIGURE 12. Line Reflection Diagram of Fall Time

BALANCED METHOD

In the balanced method shown in *Figure 13*, the transient voltages and currents on the line are equal and

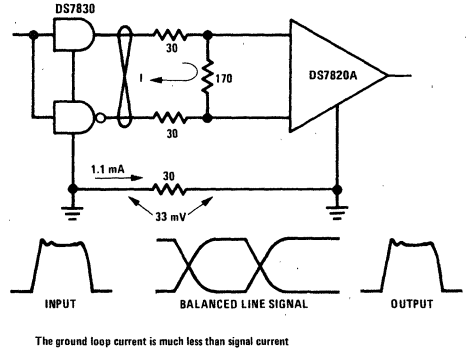


FIGURE 13. Cross Talk of Signals

opposite and cancel each others noise. Also unlike the unbalanced method, they generate very little ground noise. As a result, the balanced circuit doesn't contribute to the noise pollution of its environment.

The circuit used for a line receiver in the balanced method is a differential amplifier. *Figure 14* shows a noise transient induced equally on line A and line B from line C. Because the signals on line A and B are equal, the signals are ignored by the differential line receiver.

Likewise for the same reason, the differential signals on line A&B from the driver will not induce transients on line C. Thus, the balanced method doesn't generate noise and also isn't susceptible to noise. On the other hand the unbalanced method is more sensitive to noise and also generates more noise.

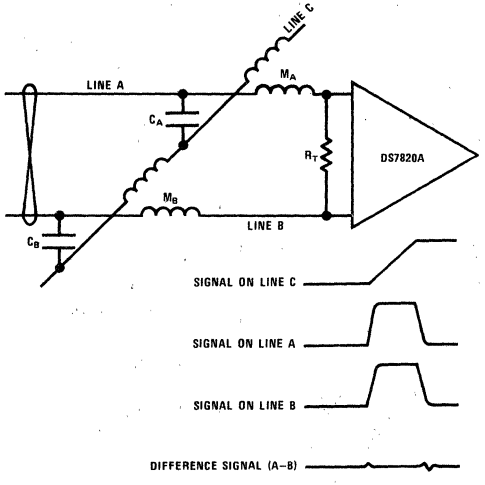


FIGURE 14. Cross Talk of Signals

The characteristic impedance of the unbalanced transmission line is less than the impedance of the balanced transmission line. In the unbalanced method there is more capacitance and less inductance than in the balanced method. In the balance method the Reactance to adjacent wires is almost cancelled (see *Figure 15*). As a result a transmission line may have a 60Ω unbalanced impedance and a 90Ω balanced impedance. This means that the unbalanced method, which is more susceptible to IR drop, must use a smaller value termination, which will further increase the IR drop in the line.

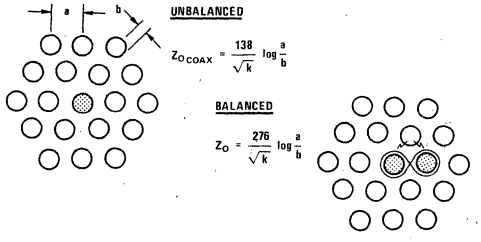


FIGURE 15. Z_O Unbalanced < Z_O Balanced

The impedance measurement of an unbalance and balance line must be made differently. The balanced impedance must be measured with a balanced signal. If there is any unbalance in the signal on the balanced line, there will be an unbalance reflection at the terminator. Therefore, the lines should also be terminated for unbalanced signals. *Figure 16* shows the perfect termination configuration of a balanced transmission line. This termination method is primarily required for accurate impedance measurements.

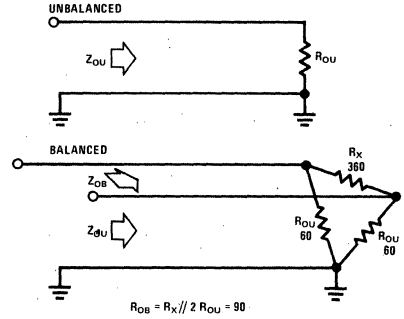


FIGURE 16. Impedance Measurement

The unbalanced method circuit used in this application note up to this point is the unbalanced circuit shown in *Figure 1*. The termination of its transmission line was greater than the characteristic impedance of the unbalanced line and the circuit had considerable threshold offset. The measured performance of the unbalanced circuit wasn't comparable to the balanced method. Therefore, for the following comparison of unbalanced and balanced circuits, an improved termination shown in *Figure 17* will be used. This circuit terminates the line in 60Ω and minimized the receiver threshold offset.

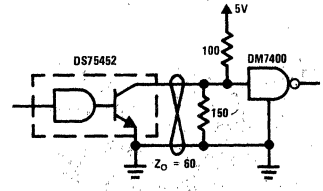


FIGURE 17. Improved Unbalanced Method

A plot of the Absolute Maximum Data Rate versus cable type is shown in *Figure 18*. The graph shows the different performances of the DS7820A line receiver and

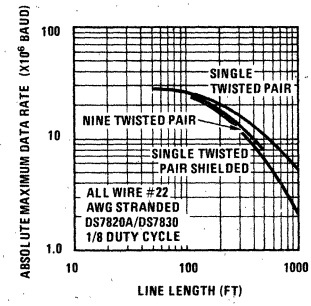


FIGURE 18. Data Rate vs Cable Type

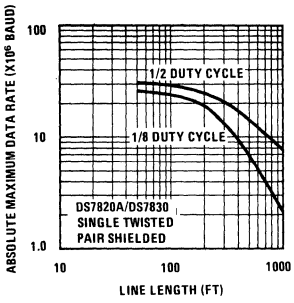


FIGURE 19. Data Rate vs Duty Cycle

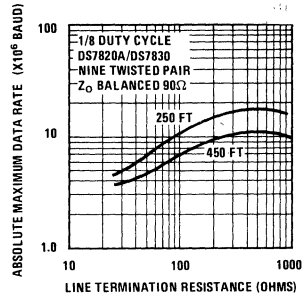


FIGURE 20. Data Rate vs Line Termination

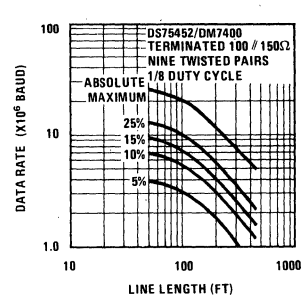


FIGURE 21. Data Rate vs Distortion of DS75452, DM7400

the DS7830 line driver circuits with a worse case 1/8 Duty Cycle in no. 22 AWG stranded wire cables. In a single twisted pair cable there is less reactance than in a cable having nine twisted pairs and in turn this cable has less reactance than shielded pairs. The line length is reduced in proportion to the increased line attenuation which is proportional to the line reactance. The plot shows that the reactance and attenuation has a significant effect on the cable length. Absolute Maximum Data Rate is defined as the Data Rate at which the output of the line receiver is starting to be degraded. The roll off of the performance above 20 mega baud is due to the circuit switching response limitation.

Figure 19 shows the reduction in Data Rate caused by Duty Cycle. It can be observed that the Absolute Maximum Duty Rate of 1/8 Duty Cycle is less than 1/2 Duty Cycle. The following performance curves will use 1/8 Duty Cycle since it is the worst case.

Absolute Maximum Duty Rate versus the Line Termination Resistance for two different lengths of cable is shown in *Figure 20*. It can be seen from the figure that the termination doesn't have to be perfect in the case of balanced circuits. It is better to have a termination resistor to minimize the extra transient signal reflecting between the ends of the line. The reason the Data Rate increases with increased Termination Resistance is that there is less IR drop in the cable.

The graphs in *Figure 21* shows the Data Rate versus the Line Length for various percentage of timing distortion using the unbalanced DS75452 and DM7400 circuits shown in *Figure 17*. The definition of Timing Distortion is the percentage difference in the pulse width of the data sent versus the data received.

Data Rate versus the Line Length for various percentage of timing distortion using the balanced DS7820A and DS7830 circuit is shown in *Figure 22*. The distortion of this method is improved over the unbalanced method, as was previously theorized.

The Absolute Maximum Data Rate versus Line Lengths shown in the previous two figures didn't include any induced signal noise. *Figure 23* shows the test configuration of the unbalanced circuits which was used to measure near end cross talk noise. In this configuration there are eight line drivers and one receiver at one end of the cable. The performance of the receiver measured in the presence of the driver noise is shown in *Figure 24*.

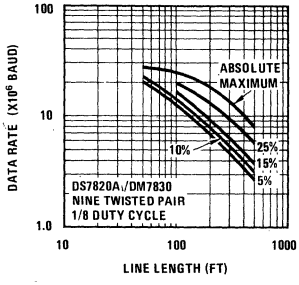


FIGURE 22. Data Rate vs Distortion of DS7820A, DS7830

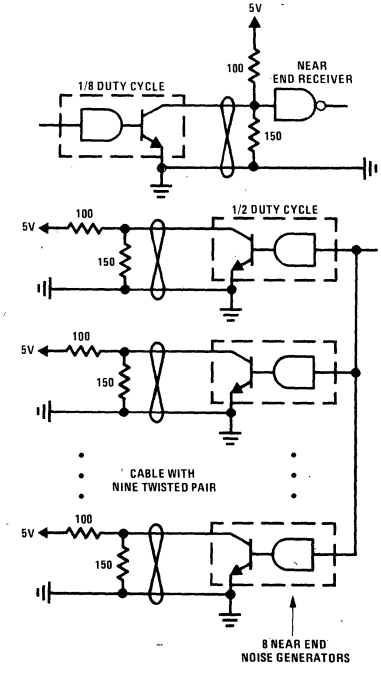


FIGURE 23. Signal Cross Talk Experiment Using DS75452, DM7400

Figure 24 shows the Absolute Maximum Duty Rate of the unbalanced method versus line length and versus the number of line drivers corresponding to the test configuration delineated in *Figure 23.* In the noise measurement set-up there was a ground return for each signal wire. If there is only one ground return in the cable the performance is worse. The graph shows that the effective line length is drastically reduced as additional Near End Drivers are added. When this performance is compounded by timing distortion the performance is further reduced.

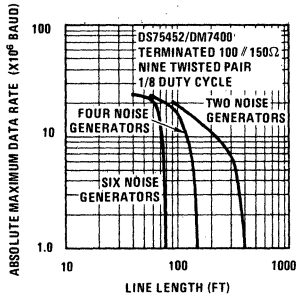


FIGURE 24. Data Rate vs Signal Cross Talk of DS75452, DM7400

Figure 25 shows the test configuration of the balanced circuit used to generate worst case Near End cross talk

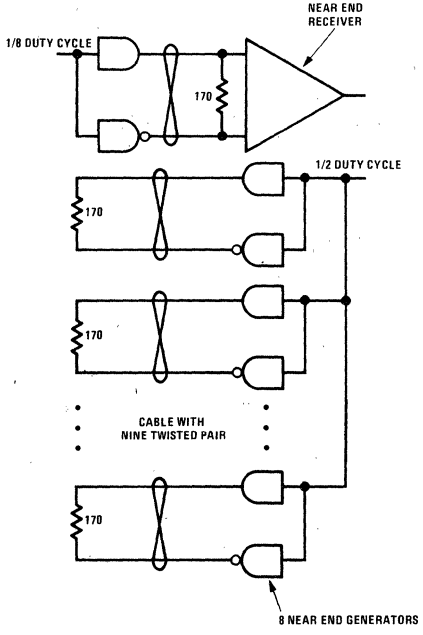


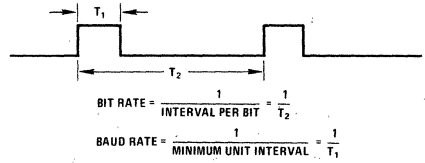
FIGURE 25. Signal Cross Talk Experiment Using DS7830, DS7820A

noise similar to the unbalance performance shown in the previous figure. Unlike the unbalanced case, there was no measurable degradation of the circuits Data Rate or distortion.

CONCLUSION

National has a full line of both Balanced and Unbalanced Line Drivers and Receivers. Both circuit types work well when used within their limitations. This application note shows that the balanced method is perferable for long lines in noisy electrical evironments. On the other hand the unbalanced circuit works perfectly well with shorter lines and reduced data rates. It should be kept in mind that when you are spending $500,000 for a CPU and $75,000 for peripherals, it pays to investigate the best way to transmit data between them.

DEFINITION OF BAUD RATE



The data in this note was plotted versus Baud Rate. The minimum unit interval reflected the worse case conditions and also normalized the diagrams so that the diagrams were independent of duty cycle. If the duty cycle is 50% then the Baud Rate is twice the Bit Rate.

REFERENCES

IC's for Digital Data Transmission , Widlar and Kubinec, *National Semiconductor Application Note AN-22.*

Data Bus and Differential Line Drivers and Receivers, Richard Percival, *National Semiconductor Application Note AN-83.*

RADC TR73-309, Experimental Analysis of the Transmission of Digital Signals over Twisted Pair Cable, Hendrickson and Evanowski, *Digital Communication Section Communications and Navigation Division,* Rome Air Development Center, Griffis Air Force Base, New York.

Fast Pulse Techniques, Thad Dreher, E-H Research Laboratories, Inc., *The Electronic Engineer*, Aug. 1969.

Transient Analysis of Coaxial Cables, Considering Skin Effects, Wigingtom and Nahmaj, *Proceedings of the IRE*, Feb. 1957.

Reflection and Crosstalk in Logic, Circuit Interconnections, John DeFalco, Honeywell, Inc., *IEEE Spectrum*, July 1970.

NATIONAL

DRIVER UPDATE—NEW DRIVERS FOR LED DISPLAYS

INTRODUCTION

Many new LED drivers have been introduced in the past year. This application note picks up where AN-99 left off and expands into recent developments in LED displays. If the particular display requirements are known, inspection of Table I will narrow down the selection of drivers to the most appropriate few, or the one that will do the job. Reading the description provided in this note, or on the data sheet for a particular driver should help complete the design project. If more information on drivers in general is desired, then read on. Since this is an application note, as many circuit applications as possible for each driver are included.

GENERAL CONSIDERATIONS

To multiplex or not to multiplex is an important consideration. Some of the reasoning and arguments, pro and con, are covered very well in AN-99 and reading of that application note is recommended. An important factor affecting display operation is that most multi-digit displays presently available are interconnected for multiplexing only, removing any choice by the systems designer.

The mathematics of multiplexing is fairly straightforward. The drive requirement for most LED displays is stated in the form of an *average* segment current. Peak segment current—the current a driver has to supply—is derived by dividing the average segment current by the duty cycle. For instance, it may be desirable to drive a 9-digit LED display, like National's NSA1298, with an average segment current of 0.7 mA. If the duty cycle were 10%, derived by driving the 9 digits for equal periods plus a 10% of period interdigit blanking time, then the peak segment current would be 7 mA (0.7 mA ÷10%). Digit current is then the peak segment current multiplied by the number of segments that are "ON." Including the decimal point, the maximum digit current would be 56 mA (7 mA x 8 segments). In addition to this rather simple example, the designer needs to account for the specified variation in segment currents due to resistor tolerance, etc. and its effect on the digit driver specification. However, the example serves to show the basic mathematics involved.

CATEGORIZING DRIVERS

Drivers may be categorized by various functions and conditions. Some of these are:

a) Segment drivers or digit drivers
b) Anode drivers or cathode drivers
c) MOS compatible or TTL compatible inputs
d) Inverting or non-inverting outputs
e) Decoded or straight through drivers
f) Number of outputs
g) Current handling capability
h) Design supply voltage, particularly if an integral low battery indicator is included

The design guide in Table I should help in locating devices in most of these categories.

FEATURES

There are many features available on the newer segment and digit drivers which help make the overall cost of production lower or make the end product more appealing or both.

One of these features is pinout. The newer segment and digit drivers have all the inputs grouped together and all the outputs grouped together, usually on opposite sides of the package. This vastly simplifies circuit board layout often eliminating costly jumper wires and very tight circuit board traces that lead to troublesome solder bridging.

Another feature is that some of the newer segment drivers incorporate the current setting resistors internally, saving the cost of purchasing, stocking, forming, inserting and board layout for discrete resistors.

On many of the newer digit drivers, a new feature is the self-contained low battery indicator. These indicators are generally set for 9V battery systems or 6V (4-cell) or 4 1/2V (3-cell) battery systems. They are an appealing sales feature that warns the purchaser when to recharge the batteries (if ni-cads) or replace them if they are throw-aways.

TABLE I.

Refer to LED Driver Guide in Front of Catalog

National Part Number	Status	Output Current (Note 1) Min (mA)	Off-State Output Voltage Max (V)	Package Size (Number of Pins)	Number of Drivers	Decoded	Inverting	Non-Inverting	Driver		Driver		For Common Anode	For Common Cathode	MOS Inputs	TTL Inputs	Comments
									Anode	Cathode	Digit	Segment					
DM7446A	Production	40	30	16	7	X				X		X	X			X	
DM7447A	Production	40	15	16	7	X				X		X	X			X	
DM7448	Production	−2	NA	16	7	X				X†		X	X†			X	†Through External Transistor
DS8646	Development	84	5	Dice	6		X			X	X			X	X		For CMOS Watch Circuits
DS8647	Development	−7	−4	Dice	9		X		X			X		X	X		For CMOS Watch Circuits
DS8648	Development	−7	−4	Dice	9			X	X			X		X	X		For CMOS Watch Circuits
DS8650	Production	50	5	Dice	4		X			X	X			X	X		For CMOS Watch Circuits
DS8651	Production	−5	−4	Dice	7		X		X			X		X	X		For CMOS Watch Circuits
DS8658	Production	84	5	Dice	4		X			X	X			X	X		For CMOS Watch Circuits
DS8659	Production	−7	−4	Dice	7		X		X			X		X	X		For CMOS Watch Circuits
DS8844	Production	50	10	16	7		X			X	X			X	X		
DS8855	Production	50	10	22	9		X			X	X			X	X		
DS8856	Production	−6 max	5.5	16	7	X				X†		X	X†			X	†Through External Transistor
DS8857	Production	−50 max	5.5	16	7	X			X			X		X		X	
DS8858	Production	−50 max	5.5	16	7	X			X			X		X		X	
DS8859	Production	0–40	5.5	16	6		X			X		X	X			X	Lamp Driver With Latch
DS8861	Production	±50	10	18	5		X*	X	X	X*	X*	X		X	X		*With Emitter Grounded
DS8863	Production	500	10	18	8		X			X	X			X	X		
DS8864	Production	50	10	22	9		X			X	X			X	X		For 9V Battery With Low Battery
DS8865	Production	50	10	18	8		X			X	X			X	X		
DS8866	Production	18	10	18	7		X			X	X			X	X		For 9V Battery With Low Battery
DS8867	Production	−10	8	18	8			X	X			X		X	X		Preset I_{OUT}
DS8868	Production	110	5	18	12	X				X	X			X	X		For 4.5V Battery With Low Battery
DS8869	Production	0–40	5.5	16	6			X		X		X	X			X	Lamp Driver With Latch
DS8870	Production	350	10	14	6		X			X	X			X	X		
DS8871	Production	50	10	18	8		X			X	X			X	X		
DS8872	Production	50	10	22	9		X			X	X			X	X		
DS8873	Production	50	10	22	9		X			X	X			X	X		For 9V Battery With Low Battery
DS8874	Development	50	10	14	9	X				X	X			X	X		For 9V Battery; Shift Input
DS8876	Development	50	10	14	9	X				X	X			X	X		For 6V Battery; Shift Input
DS8877	Production	40	10	14	6		X			X	X			X	X		DS75492 Pin Out
DS8879	Development	50	10	14	9	X				X	X			X	X		For 4.5V Battery; Shift Input
DS8895	Production	−14	10	16	4			X	X			X		X	X		Internal Set I_{OUT}
DS8973	Development	100	10	22	9		X			X	X			X	X		For 4.5V Battery With Low Battery
DS8974	Development	100	10	22	9		X			X	X			X	X		For 6V Battery With Low Battery
DS8976	Development	100	10	22	9		X			X	X			X	X		For 9V Battery With Low Battery
DS75491	Production	±50	10	14	4		X*	X	X	X*	X*	X		X	X		*With Emitter Grounded
DS75492	Production	250	10	14	6		X			X	X			X	X		
DS75493	Production	−30	10	16	4			X	X			X		X	X		I_{OUT} Set By R_{EXT}
DS75494	Production	180	10	16	6		X			X	X			X	X		

Note 1: Positive current is into the device (sinking).

Watch Circuits Using LED's

Two new drivers designed to drive LED displays in watches are the DS8658 and DS8659. The DS8658 is a 4-digit driver which is basically 4 NPN transistors on a chip with their emitters tied together. The 4 bases are brought out on one side of the chip and the 4 collectors on the opposite side to make assembly easier. The DS8659 is a constant current segment driver designed to supply 10 ±3 mA. To accomplish this with only a 2.4–2.7V battery, the circuit uses a PNP current mirror driven by a PNP emitter-follower. This is believed to be the first all PNP integrated circuit in large scale production. *Figure 1* shows a typical watch circuit using these drivers. If, for reasons of battery life or for a smaller ladies type watch, a smaller display is used, then lower segment currents can be generated. The watch circuit in *Figure 2* shows just such a circuit. The DS8651 will supply 6.5 ±1.5 mA per segment.

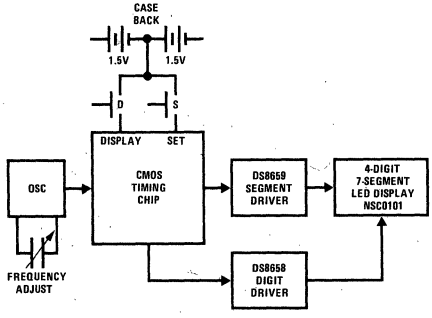


FIGURE 1. Typical Watch Circuit

The NSC0175 are 75% the height of the NSC0101 used in *Figure 1* and can be spaced closer together. An even smaller, brighter display can be made using the NSC0155 which are 55% the height of the NSC0101.

If the CMOS watch chip is designed to drive non-inverting segment drivers, then the DS8649 8-segment driver can be used. The output current of the DS8649 has a much higher battery voltage dependence than the DS8651 or DS8659, but is more efficient since all display driver current goes through the display. *Figure 3* shows how the DS8649 would be connected in a watch circuit. With a fresh set of batteries, the DS8649 delivers typically 10–12 mA per segment, dropping to 5 mA typically at 1/2 battery life.

As might be expected, digital watches are being designed with more and more features. One of these features includes the provision for an alpha-numeric representation for day of the week. This requires a 9-segment driver, such as the DS8647 (inverting) or DS8648 (non-inverting). Also some designs show a third pair of digits to show seconds or date at the same time hours and minutes are being displayed. For these applications, a 6-digit driver such as the DS8646 (inverting) can be used. An example of the application of these circuits is shown in *Figure 4*.

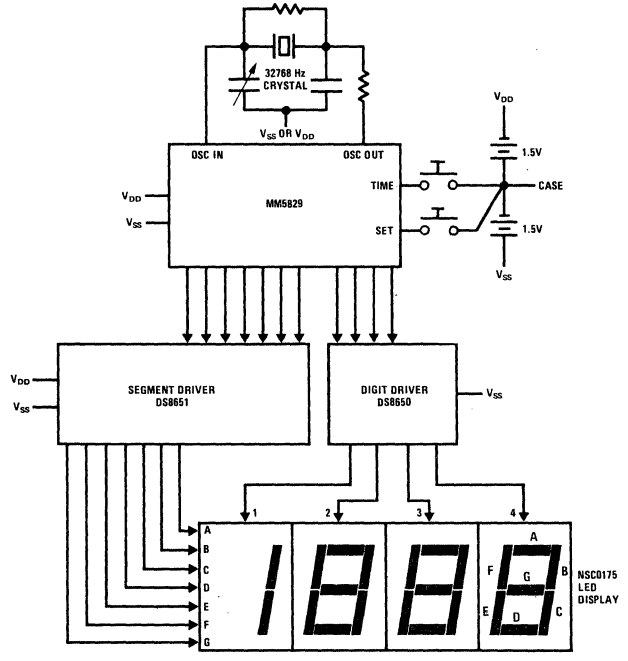


FIGURE 2. Low Power Watch Circuit

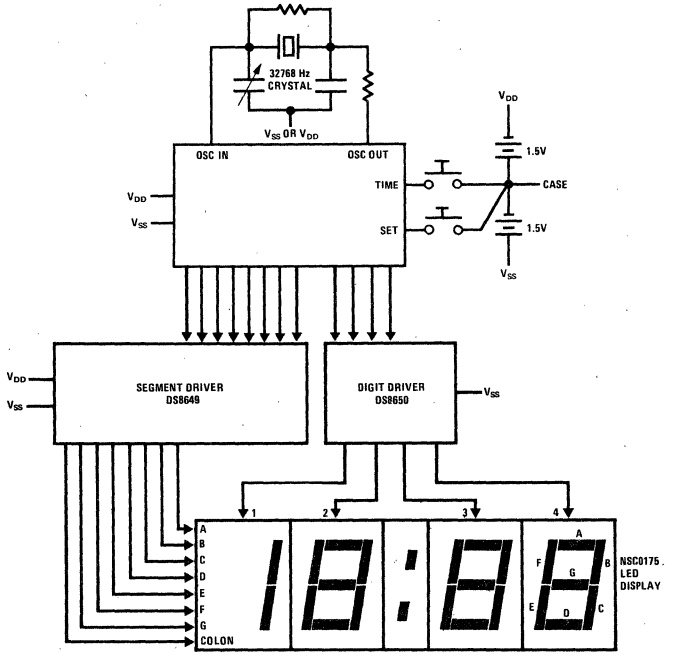


FIGURE 3. Watch Circuit Using DS8649

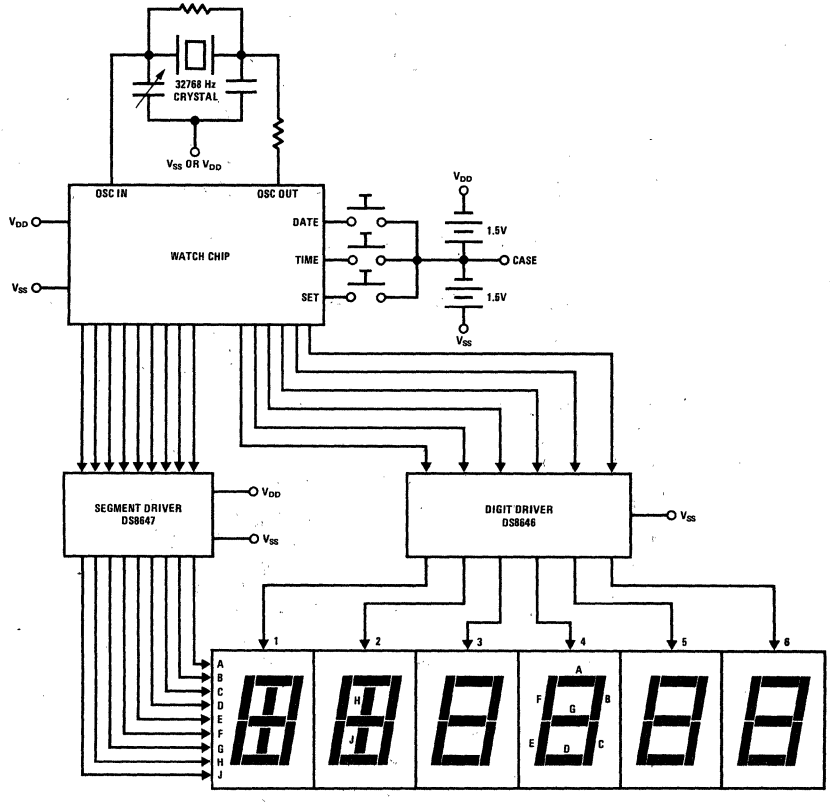


FIGURE 4. Alpha-Numeric Date Watch

Clock Applications of LED Drivers

Clocks are generally viewed at some distance, and therefore require larger displays. Larger displays in turn require higher operating segment currents. *Figure 5* shows a typical clock circuit—in this case a clock for automobiles. In this circuit, the segment currents are set to approximately 45 mA by the 4 resistors connected to each DS75491. The DS8870 hex digit driver will sink the 360 mA maximum digit current.

Clocks for home use don't require the high degree of light output that an auto clock requires. For these applications it becomes more cost-effective to use two DS8867's in parallel to produce a typical segment current of 28 mA. The digit driver in this case can be a DS75492 and each digit driver will sink typically 208 mA with a figure 8 displayed and the colon displayed. This application is illustrated in *Figure 6.*

If a high brightness, large display is desired, then the application shown in *Figure 7* can be used. In this circuit, 2-segment drivers rated at 50 mA each are paralleled to supply 100 mA of segment current to the large 0.6 inch NSN64R display. The digit drivers are also paralleled to sink the required 700 mA.

Calculator Applications of Display Drivers

The key to low cost calculators has been to reduce the number of components required to an absolute minimum. An example of an extremely simple, low cost calculator is shown in *Figure 8.* The DS8877 driver will sink 35 mA min and consists of 6 drivers per package.

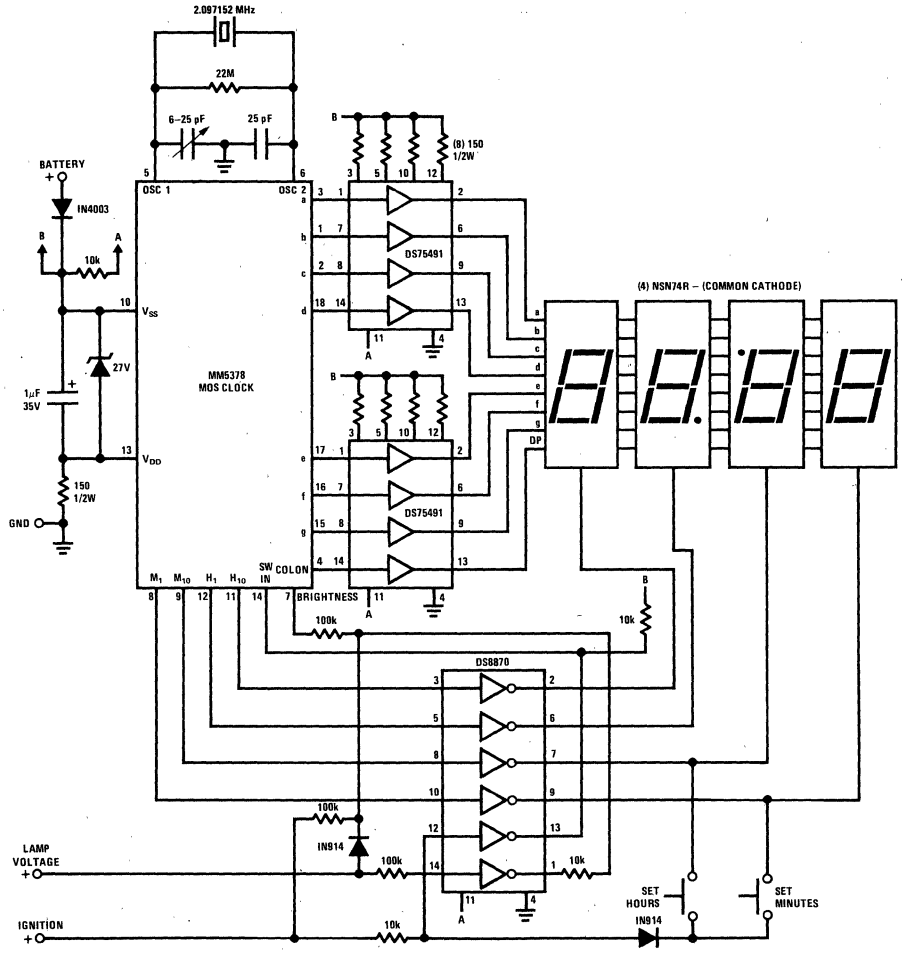
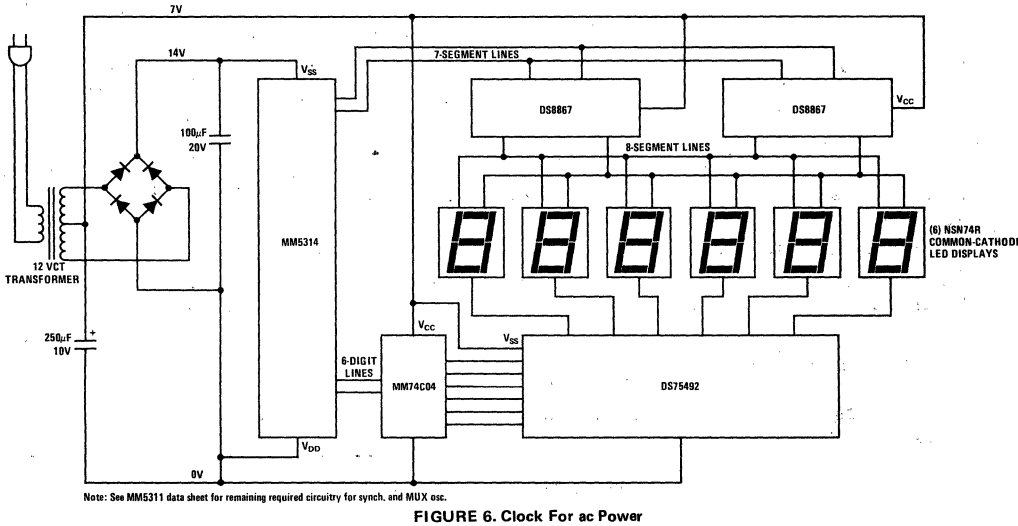


FIGURE 5. Automobile Clock



Note: See MM5311 data sheet for remaining required circuitry for synch. and MUX osc.

FIGURE 6. Clock For ac Power

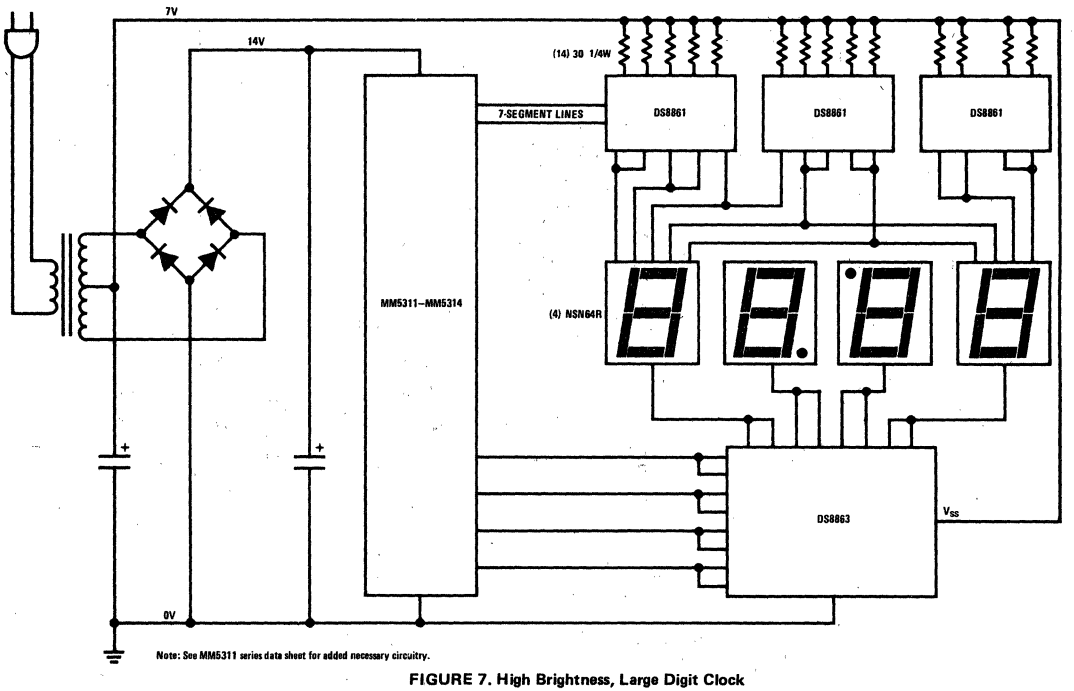


FIGURE 7. High Brightness, Large Digit Clock

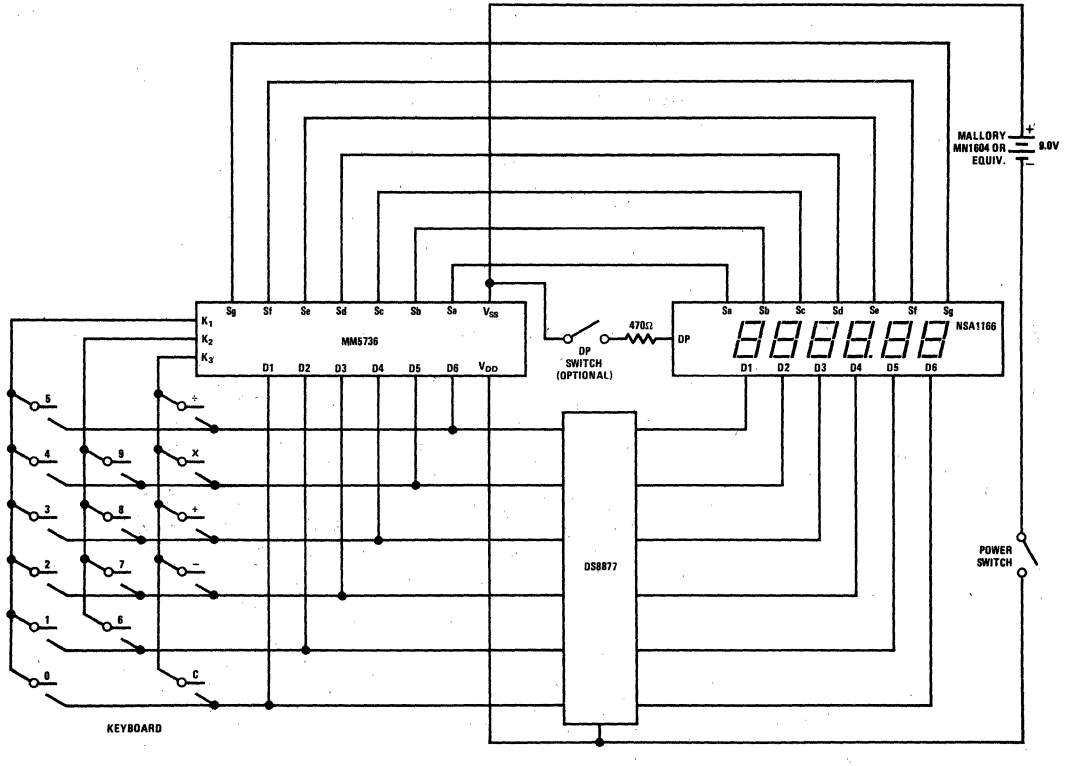


FIGURE 8. 6-Digit Calculator Configuration

Just because the calculator gets more complicated doesn't mean that the component count has to increase. In *Figure 9*, the calculator circuit has 2 *less* components than the circuit in *Figure 8* (one switch and one resistor).

Yet this calculator provides an 8-digit floating point display with memory and constant. In addition the DS8864 display driver supplies a low battery indication besides driving 9 digits. This low battery indicator supplies current to turn on the decimal point segment in the digit 9 position whenever the battery voltage drops into the 6–7V region. It is specified to be "ON" if the V_{CC} is 6V or less and to be "OFF" for any voltage over 7V.

Even a sophisticated circuit as the Programmable Financial Computer shown in *Figure 10* doesn't require any driver circuitry more complicated than a single DS8864.

If for some reason, such as ac operation, or different battery voltage, etc., a low battery indicator is not desired or needed, then the DS8855 can be used. It is identical in specification and pin out to the DS8864, except for the absence of any specification regarding a low battery indicator.

Rechargeable Battery and 3 or 4 Cell Systems

All of the previous discussion and applications have applied to a single 9V throw-away battery system. Rechargeable cells are expensive, and it would require 6 cells to work in the previously described circuits. It is even cost effective to replace an expensive rechargeable cell with a less expensive segment driver. Also dc-to-dc converters can be obtained for less than the cost of two cells. The following applications apply to just such systems.

But first let us consider the question of just how many cells to use. Any calculator system using less than 6 cells will supply less than 6.6V end of life (assuming 1.1V per cell to be end of useful life for a nickel-cadmium rechargeable cell.) Most calculator chips require at least 6.5V to work. Therefore any system of fewer than 6 cells will require a dc-to-dc converter to raise the voltage for the MOS calculator chip.

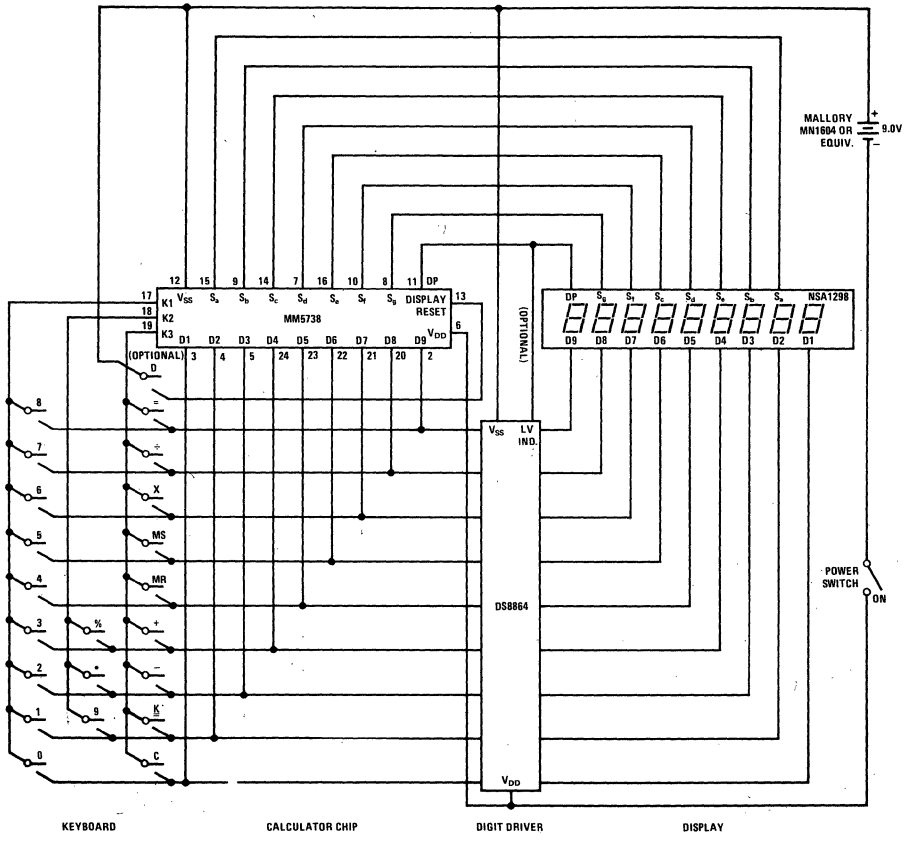


FIGURE 9. Memory Calculator

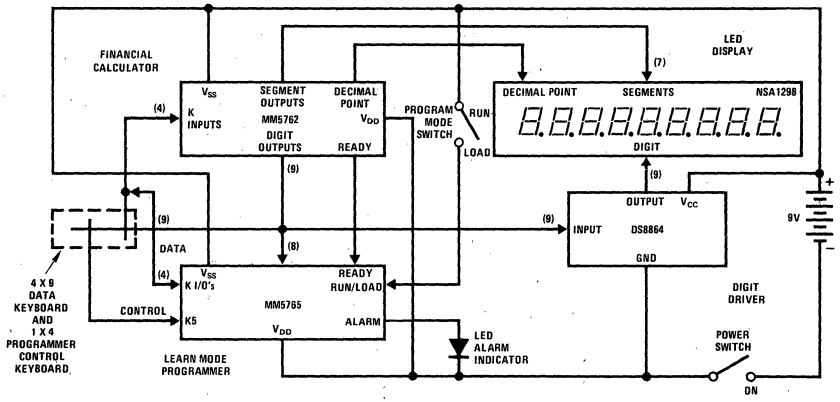


FIGURE 10. Low Cost Hand Held Programmable Financial Computer Using the MM5762 Calculator and MM5765 Programmer

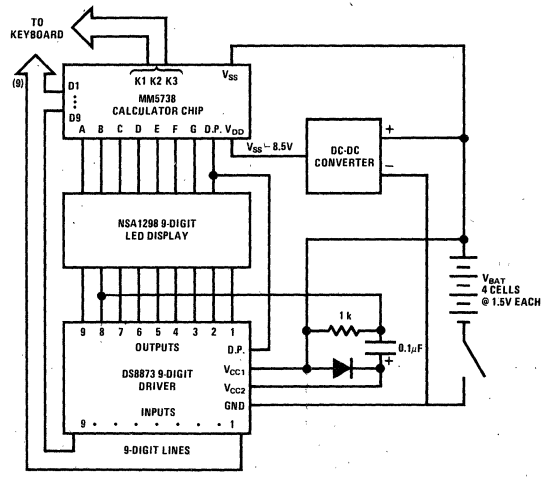


FIGURE 11. 4-Cell Calculator System

Next, a GAAs LED display requires a 1.7–2.0V drop to operate. If we could get segment and digit drivers that dropped less than 0.3V each, the required supply for the display would be 2.6V min. This eliminates the use of 1 or 2 cells to operate the display directly. The most efficient, least power wasting system would use 3 cells to operate the display directly (since it takes 3/4 or more of the power in a calculator) and use a 3V to 8V converter to run the MOS chip.

Any 3-cell system also requires the use of a segment driver, otherwise all of the segment current, e.g., display current, would have to be generated by the MOS chip off of the dc-to-dc converted 8V supply and all of the efficiency we hoped to gain from using 3 cells would be lost. Battery current drain would at least double and typically triple with the resultant drastic decrease in battery life.

A compromise system using 4 cells can be constructed. In this system the calculator chip's V_{SS} terminal is connected to the positive battery terminal, so that the MOS calculator chip supplies direct segment drive, yet all of this current flows from the battery, not the dc-to-dc converter. Such a system is shown in *Figure 11*. The reason 4 cells are required is that the MOS chip requires at least 2V across its segment drivers in order to generate the required segment current.

This system does require a digit driver with a lower output drop than the DS8864's Darlington outputs. The DS8864 is specified to be less than 1.5V which is adequate in 9V systems. Therefore a saturating output driver like the DS8872 or DS8873 is required. Their outputs are specified at less than 0.5V. Their pinouts are identical to the DS8864 and the DS8872 has no low battery indicator, while the DS8873 does.

In a 3 cell system, one cell of the 4 cell system above is traded for a segment driver *(Figure 12)*.

The DS8867 segment driver has 8 drivers, each designed to supply 14 mA segment current, independent of supply voltage. The DS8973 9-digit driver will sink 100 mA typically and has a low battery indicator set to turn on the decimal point segment at the digit 9 time if the battery voltage drops below 3.1V. It will be off for any battery voltage greater than 3.5V.

Some other drivers that have particular uses are the DS8844, DS8865 and DS8871. The DS8844 is a 7-digit driver with Darlington outputs which are specified like the DS8864. The DS8865 is an 8-digit driver which just adds one driver to the DS8844 and is in an 18-pin package instead of the DS8844's 16-pin package. The DS8871 has a saturating output similar to the DS8872 and DS8873 (specified at 0.5V) and has 8 drivers in an 18-pin package. These drivers are useful for smaller 6-digit calculators *(Figure 6)*. They are also useful for the newer scientific calculators that have 12 or more digits. One example of this application is shown in *Figure 13*.

Some Newer Driver Circuits

One scheme to reduce the number of drivers or the number of pins on a driver resulted in the DS8868 which is a 12-digit driver with low battery indicator all in an 18-pin package. This bit of magic is accomplished by incorporating a 4 input decoder on chip with the drivers and by feeding the low battery condition information back into the MOS calculator circuit through one of the input pins. Of course this requires a special calculator chip to drive the DS8868. One such calculator circuit is the MM5758 Scientific Calculator shown in the application block diagram in *Figure 14*.

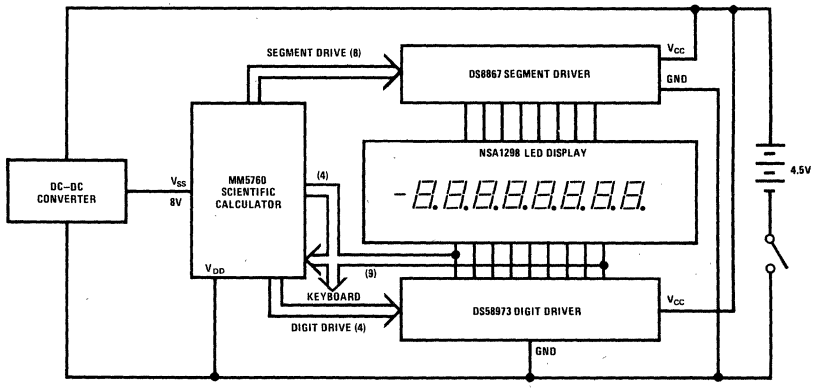


FIGURE 12. Typical 3-Cell Mathematical Calculator Circuit

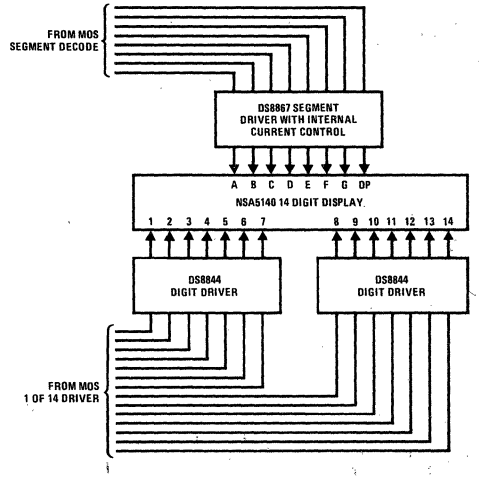


FIGURE 13. 14-Digit Calculator

Another interesting scheme to reduce package size and number of interconnections is shown in *Figure 15.*

The digit driver in this application, the DS8874, is a shift register that only requires a SET input to set the first digit driver and clock to step the "ON" signal from the first to the second and on down to the 9th driver. The SET signal also resets the 9th driver. One added pin is used for a low battery output. This allows a 9-digit driver to be put in a 14-pin package. In the DS8874, the low battery indicator is set for a 6-cell (9V) battery system. The DS8876 is a DS8874 with a 4-cell low battery system and a 3-cell version is the DS8879. This driver also requires a special compatible and complementary MOS calculator chip. One of these is the MM5784. The interconnection diagram is shown in *Figure 16.*

CONCLUSION

In this application note we have tried to stay away from a cookbook approach. Rather, we have tried to stir the interest and ingenuity of the reader in applying various LED drivers to the system design problem that may be facing the reader. You are invited to inspect the specific data sheets of any devices that seem to apply to your application to enable you to complete your design calculations. May your new design be a winner!

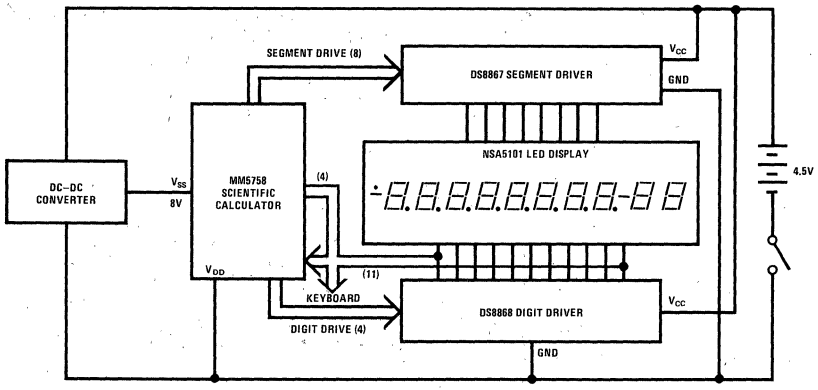


FIGURE 14. Typical 3-Cell Scientific Calculator System

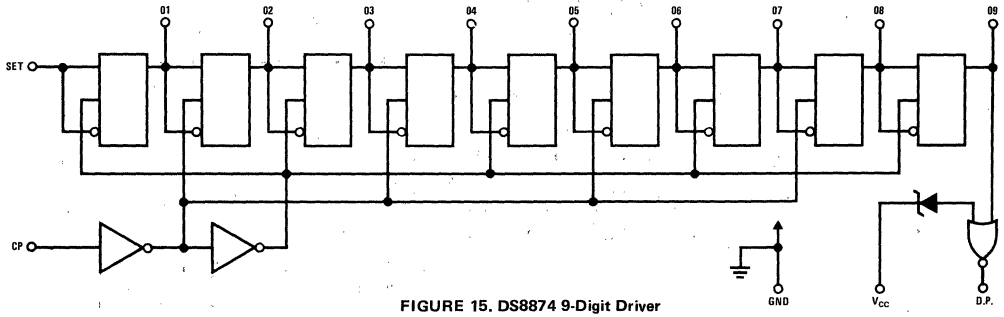


FIGURE 15. DS8874 9-Digit Driver

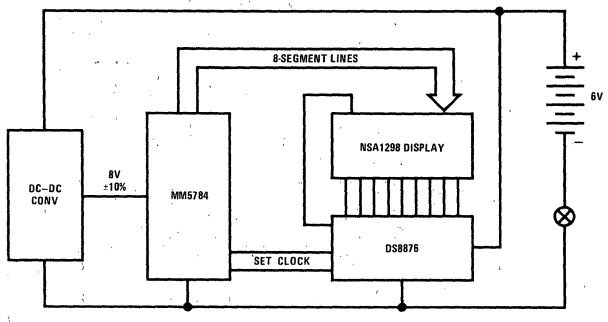


FIGURE 16. 4-Cell Shift Driver Calculator System

NATIONAL

OPTO BRIEF 1

SWITCHING TIME TESTING OF OPTO-COUPLERS

INTRODUCTION

Simple opto-couplers, such as those with transistor and darlington outputs, have improved much in the last few years, however the circuitry and the manner of obtaining switching times have not changed, thus leaving a lot to be desired. After all, the only real purpose of such measurements is to convey, via the spec sheet, the top speed of your device to a design engineer. This top speed must, however, be defined in a reasonable manner, and by logical terms, and to meaningful levels.

Present methods of specifying switching times are at some completely unknown LED drive from which of course no engineer can design. The LED forward current (I_F) is varied until the transistor collector current (I_C) reaches some specified limit (typically this is at 1 or 2 mA). The rise and fall times (t_r and t_f) are defined as the time it takes the I_C to reach from 10% to 90%, and 90% to 10% respectively its specified level. The t_r and t_f of the detectors I_C is not adequate in defining opto-coupler speed as both *lack* reference to the input, emitter waveform. A 1μs rise time of the detector's I_C is meaningless if I_F must flow for 2μs (delay time, t_d) before any I_C begins. As such, "on-time, t_{ON}, which is $t_d + t_r$" and "off-time, t_{OFF}, which is $t_s^* + t_f$" will better define opto-coupler speed. Note, that unlike t_r and t_f, t_{ON} and t_{OFF} both *have* reference to the input emitter waveform.

Since most transistor type opto-couplers are driven from TTL type logic, the input current to the LED is constant. Thus, I feel the following conditions are the most meaningful in testing opto-coupler speed. All emitter drive characteristics are fixed and constant in pulse width, pulse amplitude and duty cycle. This, also implies a completely fixed I_F for the emitter of the opto-coupler. The base terminal of the detector must have some electrical definition rather than the usual—no connection. A very high value resistor is connected between the base and the emitter of the detector. This resistor has a very minor effect on the speed and the current transfer ratio of the device. The V_{CE} of the detector must also be held as constant as reasonably possible. I have elected the following specific conditions for the measurement of National Semiconductor's opto-coupler's t_{ON} and t_{OFF} parameters.

The emitter I_F pulse is fixed and constant at 10 mA peak (−0%, +10%), 8μs in duration and a duty cycle of no greater than 10%. The V_{CE} of the detector is fixed and constant at 4.0 V_{DC} (−0%, +10%). The apparent R_L (detector load) is to be no greater than 50 ohms. Using these test conditions, the measured parameters are defined as:

- The Δt between the beginning of the on drive I_F pulse and time when I_C exceeds 1 mA. This is defined as t_{ON}.
- The Δt between the end of the on drive I_F pulse and time when I_C decreases below 1 mA. This is defined as t_{OFF}.

*t_S is storage time and is usually small compared to fall time (t_f)

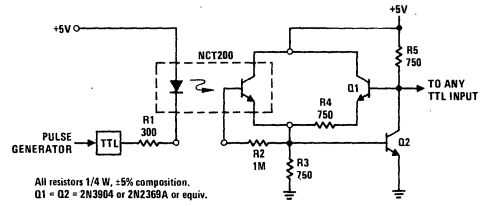
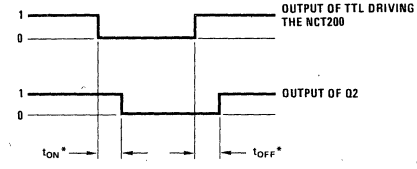


FIGURE 1.

The following circuit is used for the measurement of switching times with the conditions just stated.

The output of Q2 when compared to the input TTL is directly comparable to t_{ON} and t_{OFF} of the optocoupler as follows:



*As referenced to 1.0 mA I_C when 10 mA I_F is supplied to the emitter.

FIGURE 2.

If the user so wishes, the LED drive level, the I_C sort level and the R_L can be varied.

To change the LED I_F, the series limiting resistor (R1, 300Ω) can be increased or decreased to obtain less current or greater current respectively. If R1 is decreased in value, be sure the TTL can sink the particular I_F that is required.

The input impedance of the base-emitter of Q2 defines the apparent R_L. Little can be done to decrease this value. R_L can be increased at your discretion by inserting a resistor directly in series with the base of Q2 only. I feel, however, there is no reason to decrease the R_L below 25 ohms and no advantage can be seen in increasing this resistance.

The present I_C sort level is determined by R3. The 1 mA level presently used was arrived at by dividing 0.75V by the R3 value. The 0.75V is the $V_{BE(ON)}$ voltage of Q2 hence, if a 2 mA I_C level is desired, R3 must be halved, if a 1/2 mA level is desired, R3 must be doubled. Note that R4 must be approximately the same resistance as that of R3 at any sort point to assure a logic "1" level Q2 output. I_C sort points of 100μA to 10 mA can be obtained this way.

This method of measuring switching times is directly comparible to the methods used to obtain simple transistor switching times (i.e., fixed base drive, fixed collector current). In addition to switching time testing the circuit in *Figure 1* could be functional as an opto-coupler to TTL interface buffer amplifier.

NATIONAL

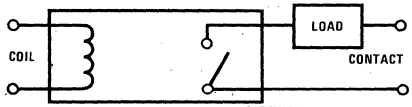
OPTO BRIEF 2

THE ODD COUPLER

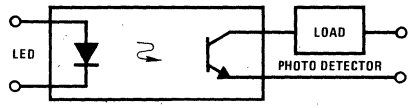
INTRODUCTION

The opto-coupler is not such an odd device as one would think. This simple opto-electronic system is an outgrowth of the LED technology which has matured in the last few years.

The basic opto-coupler consists of gallium-arsenide LED, which emits infrared light through a clear coupling media onto a photosensitive detector. The emitter and detector are both mounted in a sealed package, the most popular being the 6-lead plastic mini-DIP. A close analogy of an opto-coupler is the electro-magnetic relay.



Electro-Magnetic Relay



Opto-Coupler

In a relay, the coil is energized, the contact closes and starts conducting current through the load. In the opto-coupler, the LED is forward biased, emitting photons, which are intercepted by the detector causing it to conduct current. Electrical isolation is achieved in the coupler because there is no electrical connection between the LED terminals and the detector terminals. Isolation voltages up to 3500 volts dc can be achieved in a 6-lead DIP package.

The photon source of the coupler is an efficient gallium-arsenide die which, when forward biased, emits light in the 9000 angstrom region.

Most couplers have silicon phototransistor detectors that respond most efficiently to the infrared wavelength of 9000 angstrom region. In addition to phototransistors, photodiodes, photodarlingtons and photo SCRs are being used as detectors. The most important characteristics to consider in each device are:

- Current transfer ratio (CTR)
- Switching speed
- Isolation voltage
- Breakdown voltage of the detector

Most of these terms are self-explanatory, but it would be helpful to review current transfer ratio (CTR). CTR is the efficiency of current transfer from the input to the output of the opto-coupler. CTR is expressed as a percent ratio of the collector current compared to the input LED current. Generally, CTR has an inverse relationship with speed and bandwidth. In other words, the greater the CTR the less is the bandwidth and the lower the switching speed.

Photodiode couplers offer very low-current transfer ratios (usually less than 1%) and extremely high switching speeds in the 10 to 20 nanosecond range. Moreover, leakage is very low in these devices, usually less than a nanoamp. Photodiode couplers are especially desirable for dc coupling applications where very low-level circuitry is coupled to high-input signal level circuitry.

Photodarlington couplers offer high-current transfer ratios from 50% to 500%. This seeming paradox occurs because of the high gain of the paired transistor output stage. However, there is a trade-off for this gain: switching speed is relatively low—in the 50 to 150 microsecond range, and leakage is relatively high—in the microamp range. Unfortunately, leakage increases with temperature. Photodarlingtons are also used in dc applications for coupling low-power circuits to high-power circuits.

Phototransistor couplers generally offer current transfer ratios in the 5% to 100% range. These devices are fast with switching speed less than 10 microseconds. Leakage is relatively low—less than 5 nanoamps, and is related to the thermal characteristics of the transistor. Phototransistor couplers are the most popular type and are typically used where dc low-power circuits are coupled to high-power input signals. The NCT200 series couplers are such devices.

Photo SCR couplers are specialized devices used almost exclusively in high-current ac applications. Examples include driving larger SCRs as "on-off" switches rather than analog modulators. Current transfer ratio cannot be applied in the usual sense. The term "turn-on current" as applied to these devices refers to that current through the emitter which will cause the SCR to latch. Photo SCRs are generally used where it is desired to switch high-power ac circuitry with low to medium power signals. Typically this is a relay application.

Speaking of applications . . .

Wherever information is transmitted between switching circuits that must be electrically isolated, an opto-coupler could be used. Non-solid-state devices like relays and isolation transformers are still doing this job for some companies.

Most opto-coupler applications are in digital circuitry. Usually the common couplers (transistors and darlingtons) are not recommended for linear applications because of the CTR non-linearity which changes with temperature and input current. The opto-coupler can be used in data communications systems where line isolation is required between a remote computer terminal and a Central Processing Unit. With the power line isolated from the rest of the circuitry, the opto-coupler provides immunity from ground current noise.

An opto-coupler can be used between a telephone exchange and a telephone receiver for signaling digital logic levels to some other place in the system. The opto-coupler is faster than the standard relay coils that are being used.

In the medical electronics an opto-coupler could be used as the isolation element between the patient and an ac line. The opto-coupler will isolate the patient to keep lethal currents from flowing through him during a hospital test process. A solid-state relay can be built with distinct advantages over a mechanical relay. Faster speeds, longer life and no moving parts are some reasons for using a solid-state relay over a mechanical relay.

If you are in electronics, you are probably using switching circuits, and if you are using switching circuits there is most likely an application for opto-couplers in your company.

NATIONAL

MIL-STD-883/MIL-M-38510

MIL-STD-883

Mil-Standard-883 is a Test Methods and Procedures Document for Microelectronic Circuits. It was derived from MIL-S-19500, MIL-STD-750, and MIL-STD-202C for transistors and diodes at about the time that National Semiconductor Corporation was entering the military microelectronics market. As a result, our standard quality control operations are written around MIL-STD-883. The bonding control, visual inspections, and post seal screening requirements set forth by 883 (as well as added control procedures beyond the requirements of 883) have been part of National's quality control procedures almost from the start. Our Quality Assurance Procedures Manual is available upon request.

We offer a complete line of interface /883 (Class B) products as standard, off-the-shelf items. Special interface/883 data sheets have been prepared to reflect this capability. They show process flow, electrical parameters, end of test criteria, and test circuits. We save you the problem of specifying test and inspection procedures, and offer significant cost savings by having an off-the-shelf, "to the letter" 883 program. In addition, we will test any of our integrated circuits to any class of MIL-STD-883.

The detailed information concerning MIL-STD-883 screening is contained in National's specification NSC10002.

MIL-M-38510

MIL-M-38510 specifies the general requirements for supplying microcircuits. These are; product assurance, which includes screening and quality conformance inspection; design and construction; marking; and workmanship. The screening and quality conformance inspection are conducted in accordance with MIL-STD-883.

SCREENING

All microcircuits delivered in accordance with MIL-M-38510 must have been subjected to, and passed all the screening tests detailed in Method 5004 of MIL-STD-883 for the type of microcircuit and product assurance level.

The device electrical and package requirements of MIL-M-38510 are detailed by a device specification referred to as a slash sheet. Each slash sheet defines the microcircuit electrical performance and mechanical requirements. Each device listed on a slash sheet is referred to as a slash number and the group of the microcircuits contained on a slash sheet is defined as a family of devices. The device may be Class B or C as defined by MIL-STD-883, Method 5004 and 5005. Three lead finishes are allowed by the slash sheet, pot solder dip, bright tin plate, and gold plate.

The MIL-M-38510 specs for standard interface devices require 100% DC testing at 25°C, −55°C and +125°C. AC testing is performed at +25°C. The electrical parameters specified are tighter than the normal data sheet guaranteed limits. Additionally, MIL-M-38510 requires device traceability, extensive documentation and closely matched maintenance.

QUALITY CONFORMANCE

Quality conformance inspection is conducted in accordance with the applicable requirements of Group A, (electrical test), Group B and C, (environmental test) of Method 5005, MIL-STD-883. These tests are conducted on a sample basis with Group A performed on each sublot, Group B on each lot, and Group C as specified (usually every three months).

To supply devices to MIL-M-38510, the IC manufacturer must quality the devices he plans to supply to the detail specifications. Qualification consists of notifying the qualifying activity of one's intent to qualify to MIL-M-38510. After passing comprehensive audits of facilities and documentation systems, the IC manufacturer will subject the device to and demonstrate that they satisfy all of

MIL-M-38510 (con't)

the Group A, B, and C requirements of Method 5005 of MIL-STD-883 for the specified classes and types of IC. The qualification tests shall be monitored by the qualifying agency. Finally the IC manufacturer shall prepare and submit qualification test data to the qualifying agency. Groups A, B, and C inspections then shall be performed at intervals no greater than three months.

The purpose of qualification testing is to assure that the device and lot quality conform to certain standard limits. In effect, lot qualification tests tend to ensure that once a particular device type is demonstrated to be acceptable, it's production, including materials, processing, and testing will continue to be acceptable. These limits are specified in MIL-STD-883 in terms of LTPD's (Lot Tolerance Percent Defective) for the various qualification test sub-groups. Qualification testing is performed on a sample of devices which are chosen at random from a lot of devices that has satisfactorily completed the screening of Method 5004 must be performed on each device, i.e. on a 100% basis as opposed to qualification testing (Method 5005) which occurs on a random sample basis.

In summary, the entire purpose of MIL-M-38510 and MIL-STD-883 is to provide the military, through its contractors with standard devices.

We at National Semiconductor have supplied and are supplying devices to the MIL-M-38510 specifications. To order a MIL-M-38510 microcircuit, specify the following:

For example; to specify a DS55107 in a DIP processed to the requirements of MIL-M-38510, Class B, with gold plated leads, specify M-38510/10401 BCC.

MM38510/	XXX	XX	X	X	X
Specifies the General Requirements of MIL-M-38510	Slash Sheet No.	Device Type	Device Class	Case Outline	Lead Finish

NATIONAL

Definition of Terms

interface circuits

Common Mode Voltage: Arithmetic mean of voltages at the differential inputs referenced to ground pin at the receiver.

Common Mode Sensitivity: Rate of change of input differential voltage required to produce a given output level, against common mode voltage.

Supply Sensitivity: Rate of change of input differential voltage required to prodcue a given output level, against power supply voltage (V Pin 14 — V Pin 7).

Disabled Output Clamp Current: The current which flows from the output of a disabled TRI-STATE gate when it is dragged below ground (for instance by a transmission-line-associated transient). It is derived from the V_{CC} power rail.

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sense amplifiers

AC Common-Mode Input Firing Voltage: The peak level of a common-mode pulse which will exceed the input dynamic range and cause the logic output to switch. Pulse characteristics: $t_r = t_f \leq 15$ ns, PW = 50 ns.

Common-Mode Input Overload Recovery Time: The time necessary for the device to recover from a ±2V common-mode pulse ($t_r = t_f = 20$ ns) prior to the strobe enable signal.

Differential Input Offset Current: The absolute difference in the two input bias currents of one differential input.

Differential Input Overload Recovery Time: The time necessary for the device to recover from a 2V differential pulse ($t_f = t_r = 20$ ns) prior to the strobe enable signal.

Differential Input Threshold Voltage: The DC input voltage which forces the logic output to the logic threshold voltage (~1.5V) level.

Input Bias Current: The DC current which flows into each input pin with differential input of 0V.

Supply Current: The total DC current per package drawn from the voltage supply.

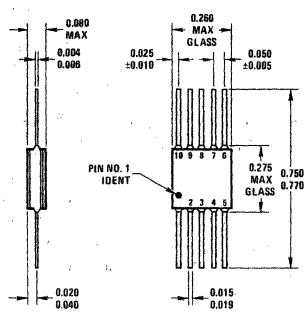
Offset Voltage: Difference between the absolute values of threshold voltage in positive- and negative-going directions.

Propagation Delay Time: Interval from switching input through 1.5V to output traversing its 50% voltage point. Measured with 50Ω load to +10V 15 pF total capacitance.

NATIONAL

Physical Dimensions

(All dimensions are in inches.)



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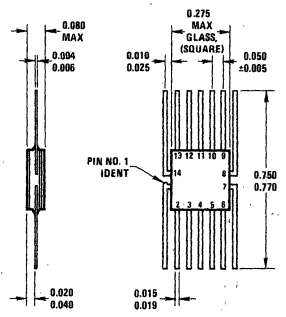

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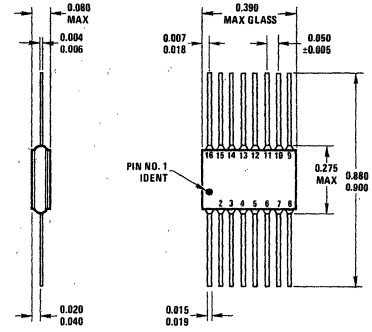

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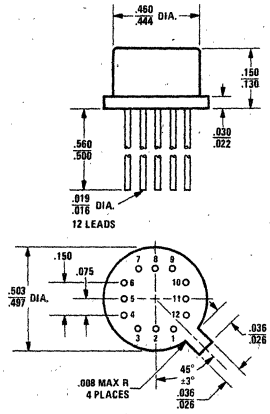
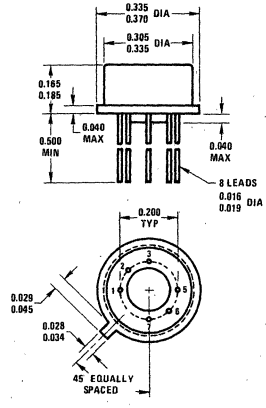
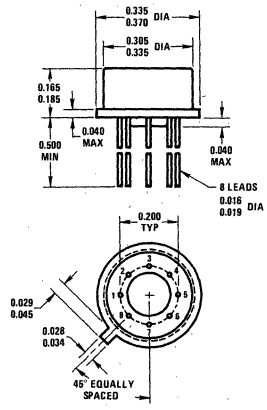


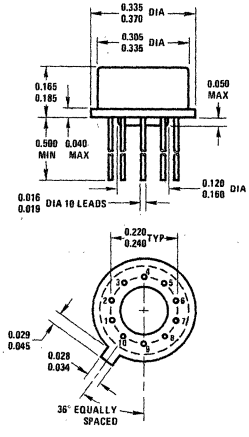
12 Lead TO-8 Metal Can (G)



6 Lead TO-5 Metal Can (H)



8 Lead TO-5 Metal Can (H)



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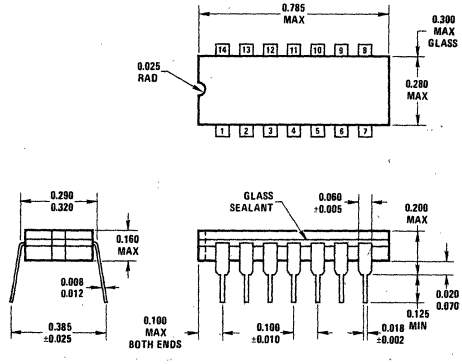
(Low Profile)



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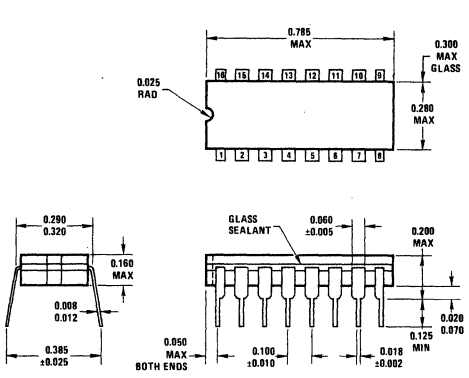

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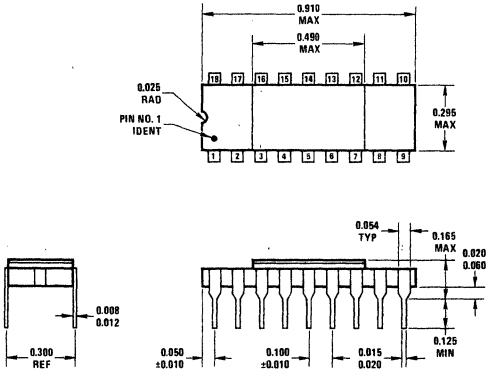

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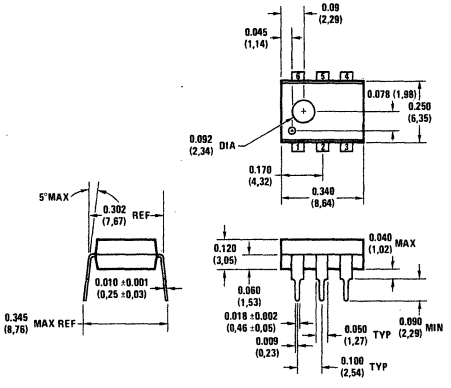

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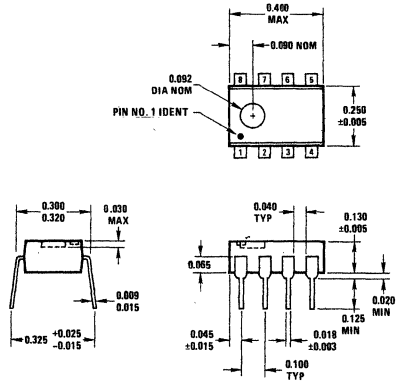

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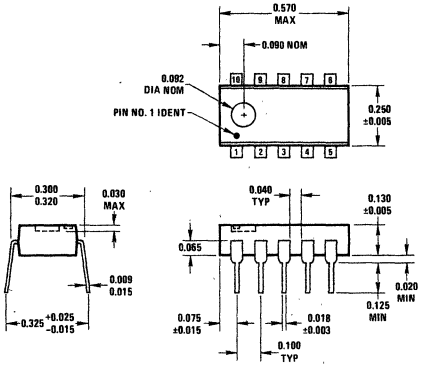

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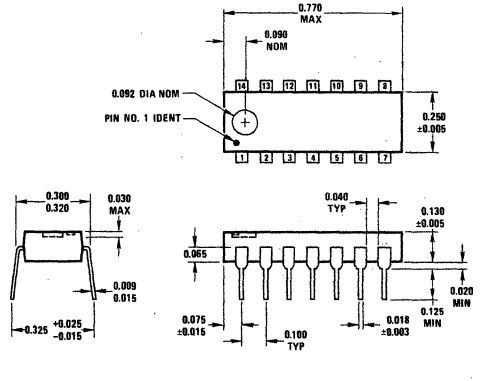

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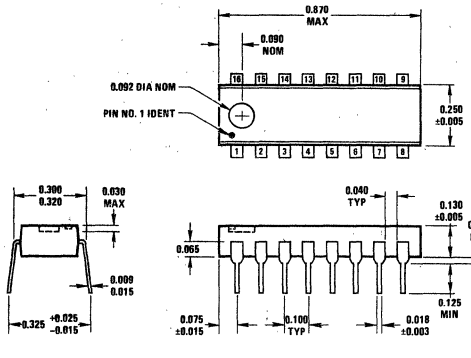

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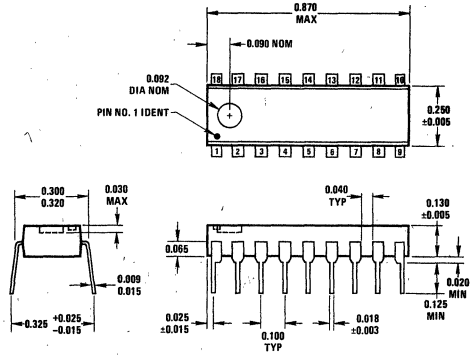

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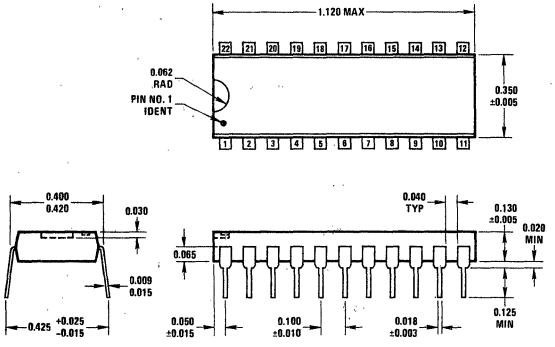

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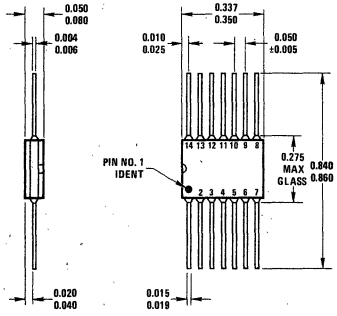

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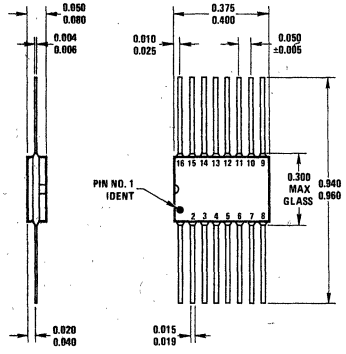

16 Lead Flat Package (W)

INCHES TO MILLIMETERS CONVERSION TABLE					
INCHES	MM	INCHES	MM	INCHES	MM
0.001	0.0254	0.010	0.254	0.100	2.54
0.002	0.0508	0.020	0.508	0.200	5.08
0.003	0.0762	0.030	0.762	0.300	7.62
0.004	0.1016	0.040	1.016	0.400	10.16
0.005	0.1270	0.050	1.270	0.500	12.70
0.006	0.1524	0.060	1.524	0.600	15.24
0.007	0.1778	0.070	1.778	0.700	17.78
0.008	0.2032	0.080	2.032	0.800	20.32
0.009	0.2286	0.090	2.286	0.900	22.86

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